Fall 2019

Characterization and modeling of ESD events and near-field scanning calibration structures

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CHARACTERIZATION AND MODELING OF ESD EVENTS AND NEAR-FIELD SCANNING CALIBRATION STRUCTURES

by

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A DISSERTATION

Presented to the Faculty of the Graduate School of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

DOCTOR OF PHILOSOPHY

in

ELECTRICAL ENGINEERING

2019

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PUBLICATION DISSERTATION OPTION

This dissertation consists of the following three articles, formatted in the style used by the Missouri University of Science and Technology:

Paper I: Pages 3-29; Software-Assisted Detection Methods for Secondary ESD Discharge During IEC 61000-4-2 Testing, has been accepted in IEEE Transactions on Electromagnetic Compatibility.

Paper II: Pages 30-57; Measurement-based Characterization and Full-wave Modeling of ESD to Display Touchscreen Sensors, will be submitted to IEEE Transactions on Electromagnetic Compatibility.

Paper III: Pages 58-81; Effect of Inhomogeneous Medium on Fields Above GCPW PCB for Near-Field Scanning Application, has been accepted in IEEE Transactions on Electromagnetic Compatibility.

ABSTRACT

This research is divided into three papers that cover, two major topics. The first topic, system-level electrostatic discharge (ESD), is discussed over the course of two papers. The second topic, a calibration structure for near-field scanning probe calibration application, is discussed in the last paper. In the first paper, software-assisted detection methods are proposed for secondary ESD discharges. The measured waveforms are analyzed with respect to waveform parameters, such as the vertical threshold of the rising edge, the derivative of the current waveform, and total charge delivered. These parameters enable automatic detection of secondary ESD while monitoring the discharge waveform at the ESD generator tip. In the second paper, the worst-case risk caused due to sparkless discharges to electronic touchscreens is investigated. The statistical behavior of the induced currents is determined for different parameters such as a change in glass thickness, indium tin oxide layer equivalent resistance, sensor spacing to the ground plane, ESD generator air discharge polarity and test voltage. In addition, a full-wave simulation model is developed to reproduce the displacement current flowing through the glass into the display's inner electronic structures. In the third paper, a method is proposed to calibrate a probe by placing it into a known field and referencing its output voltage to the known field. The near-field is measured by using E- and H-field electromagnetic interference probes. A calibration structure is built from a grounded coplanar waveguide to determine the probe factor for near-field scanning applications. The effect of non-TEM modes is easily underestimated such that non-TEM fields prevent the user from determining the unwanted field suppression of probes at higher frequencies.

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to my M.S. degree advisor, Dr. David Pommerenke, for guiding me throughout the course of both my M.S. and Ph.D. degree program. I would like to thank my Ph.D. degree advisor, Dr. Daryl Beetner, for his continuous guidance in my research work and enhancing my learning experience through numerous discussions. They guided me in developing both technical and non-technical skill sets, which helped me grow as an individual.

I would like to thank Dr. Jun Fan, Dr. Chulsoon Hwang, Dr. Victor Khilkevich, and Dr. Daniel Stutts for helping me with many useful discussions related to my research work. I would also like to thank all the former and current members of the EMC laboratory for their teamwork and help in my research and coursework. I am proud that I was a member of such an exceptional lab in the EMC area.

Lastly, I am deeply grateful to my parents and my sister for their constant support and encouragement towards achieving this goal.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

Page

PAPER I

PAPER II

PAPER III

LIST OF TABLES

Page

PAPER I

PAPER II

PAPER III

1. INTRODUCTION

1.1. SYSTEM-LEVEL ESD

In Paper I, software-assisted detection methods are proposed for secondary ESD discharges. When an ESD event reaches a nongrounded metallic part within a product, the voltage of this metallic part with respect to ground will increase. If the isolation to the ground is insufficient, a secondary ESD event can occur. Secondary ESD events are especially harmful to electronic products for multiple reasons. First, the peak discharge current within the secondary spark gap can be more than five times larger than the current of the primary ESD event from the ESD generator. Second, the rise time of the secondary ESD can be much shorter than the primary discharge—a consequence of discharging a highly overvoltaged gap. Third, the secondary ESD occurs within the product and can couple more strongly into the sensitive electronics. This can lead to soft and hard failures. As secondary ESD often leads to system upset or damage and to poorly reproducible results, it is important to detect the occurrence of secondary ESD. Secondary ESD can be detected in IEC 61000-4-2 setups by monitoring the currents, charge transfer, and sudden current increases due to the secondary ESD. An algorithm has been developed that automatically detects secondary ESD events.

Paper II investigates ESD sparkless surface discharges to displays. An evaluation PCB is designed to analyze the influence of touch screen sensor-geometry parameters such as display glass thickness, sensor-to-system-ground capacitance, and the ITO layer equivalent resistance. The setup measures the air discharge-induced displacement current into the touch sensors. As the ESD generator approaches the glass surface, a sparkless

surface corona discharge occurs, which rapidly changes the surface potential. The change in potential causes the displacement current to flow through the glass into the touch sensors. Statistical data is needed to understand the variation in peak level and the total charge delivered by the induced currents. Furthermore, a full-wave simulation model is developed to predict the worst-case induced currents flowing into the touch screen sensors.

1.2. CALIBRATION STRUCTURE FOR NEAR-FIELD SCANNING

Near-field scanning is used to visualize the near-field sources present inside an electronic device. The near-fields are measured using near-field E and H probes. The near-field data obtained using the probes are valuable; for example, identifying radio frequency interference in mobile devices. One of the applications of the near-field scanning technique is to generate models of ICs or emission sources on PCBs by obtaining the near-field data over the DUT. The emission frequency spectrum may range from a few KHz up to 40 GHz and higher. The goal of this work is to identify a single-probe calibration method that can work for large frequency bandwidth. From the available choices, the GCPW transmission line is selected as it supports wide frequency bandwidth and because of its convenience of measuring the field strength over small heights over the trace structure. At first glance, one may believe that the field structure over a GCPW or microstrip is not a function of frequency, as the structure supports a quasi-TEM wave. This paper discusses the effect of the inhomogeneous medium in GCPW PCB.

PAPER

I. SOFTWARE-ASSISTED DETECTION METHODS FOR SECONDARY ESD DISCHARGE DURING IEC 61000-4-2 TESTING

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ABSTRACT

When an electrostatic discharge (ESD) event reaches a nongrounded metallic part within a product, the voltage of this metal with respect to ground will increase. If the isolation to the ground is insufficient, a secondary ESD event can occur. As secondary ESD often leads to system upset or damage, and to poorly reproducible results, it is important to detect the occurrence of secondary ESD. If the discharge current is monitored using an oscilloscope, the test equipment may miss the secondary discharge waveform. This is because the time delay between the primary and secondary discharge events can vary between nanoseconds to milliseconds. Present oscilloscopes do not offer functionality to autodetect a secondary discharge event. The goal of this study is to analyze different types of secondary discharge events acquired with various measurement setups and identify

waveform parameters for software-assisted detection methods. A learning sequence is proposed for identifying secondary ESD events starting from low ESD gun test voltages. The data are analyzed with respect to the waveform parameters such as the vertical threshold of the rising edge, the *dI/dt* of the current waveform, and total charge delivered, which enable automatic detection of secondary ESD while monitoring the discharge waveform at the ESD gun tip.

Keywords: Current clamp, detection algorithm, electrostatic discharge (ESD), oscilloscope, secondary discharge, sequence mode acquisition.

1. INTRODUCTION

Secondary electrostatic discharge (ESD) events are especially harmful to electronic products for multiple reasons. First, the peak discharge current within the secondary spark gap can be more than five times larger than the current of the primary ESD event from the ESD gun [1]–[4]. Second, the rise time of the secondary ESD can be much shorter than the primary discharge—a consequence of discharging a highly overvoltaged gap. Third, the secondary ESD occurs within the product and can couple more strongly into the sensitive electronics. This can lead to soft and hard failures. From a testing point of view, another difficulty arises from the repeatability of secondary ESD. The secondary discharge varies much more than the primary event due to the variability of the statistical time lag [1]. Typically, during system-level ESD testing of compact electronics, the root cause of the observed failures may not be clear. For instance, cell phones are known to have ESD-induced risks to various system components and peripherals exposed to the end user [5]–

[8]. In the case of compact electronics, secondary ESD events are likely to cause failures as the spark gap distances inside the electronic products are small—ranging from micrometers to millimeters. Knowing if secondary ESD has occurred helps to understand test results and their repeatability, and assists root-cause analysis of observed failures. Detecting secondary ESD can be achieved by measuring the discharge currents and voltages or transient fields, then processing them with software algorithms to determine whether secondary ESD has occurred.

Investigations have been performed to develop a methodology to model the secondary discharge inside of a portable electronic product [3], [4], [19]. ESD guns are known to generate electromagnetic noise pulses during ESD testing. The switching of relays inside of the ESD gun before and following the discharge test leads to the prepulse and postpulse events [10], [11]. Additional pulses can be created during the ESD test due to reignition of the gap between the air discharge tip and the device under test (DUT). Here, the arc of the discharge may quench before most of the charge is depleted. As the ESD gun approaches toward the DUT test point, the gap is reduced and this may reignite the ESD gun. For contact mode discharges, a similar effect may be observed in which the spark in the relay may quench and reignite, or the relay may bounce. It is important to note that these occurrences should not be conflated with secondary ESD events, since these secondary sparks are instead generated by the ESD gun.

The various DUT configurations are placed on a horizontal coupling plane (HCP) during ESD testing and can include a grounded device, a device connected by a two-wire power supply, a battery-powered device, or a complex system with multiple cable connections. The cases where the DUT is not grounded, for example, a battery-powered

device, which has floating metal and a DUT connected to a two-wire power supply, are investigated. Measured current waveforms during secondary discharge events for the floating metal and the two-wire power supply setups [12] are used for identifying waveform parameters for software-assisted detection. First, the waveforms are measured for a controlled setup, which reproduces a DUT having a nongrounded decorative metal part. The second case consists of a DUT, which is connected to a two-wire power supply, in which the secondary ESD occurs inside of the two-wire power supply. The waveforms are acquired using an oscilloscope, a high-impedance voltage probe, and an F-65 current clamp.

A software-assisted methodology is proposed for secondary ESD event detection during IEC 61000-4-2 testing [13], which enables the distinction between the primary and secondary ESD events. The software tool implementation is based on a learning sequence during an ESD test session and requires an ESD gun voltage selection, DUT configuration input from the operator. The time domain data are acquired and postprocessing is performed to determine whether secondary ESD has occurred. The method is applied to various test setups, and results are discussed in Section III. This proposed detection methodology can be further implemented within the oscilloscope firmware as an additional tool set to assist ESD test engineers during system-level testing.

1.1. CONTROLLED SETUP

Figure 1 illustrates a measurement setup designed to understand one class of secondary discharge ESD waveforms as a controlled experiment. The setup emulates decorative metal present on electronic products which are not grounded. The controlled

setup generates repeatable occurrences of a secondary discharge event when subjected to a primary charging ESD event. The DUT is an aluminum plate with dimensions of 10 cm height × 10 cm width × 3 mm thickness mounted above a ground plane. A screw is inserted into the plate to form a spark gap with adjustable distance. Figure 2 depicts the nongrounded floating metal and the current target.

An F-65 current clamp is used to measure the primary discharge current from the ESD gun. To protect the oscilloscope, pulse attenuators [14] and overvoltage protectors are used.

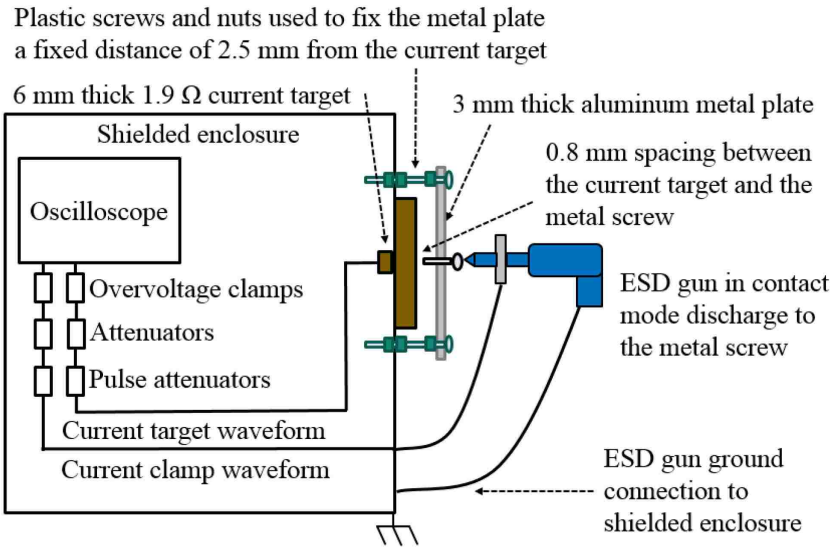
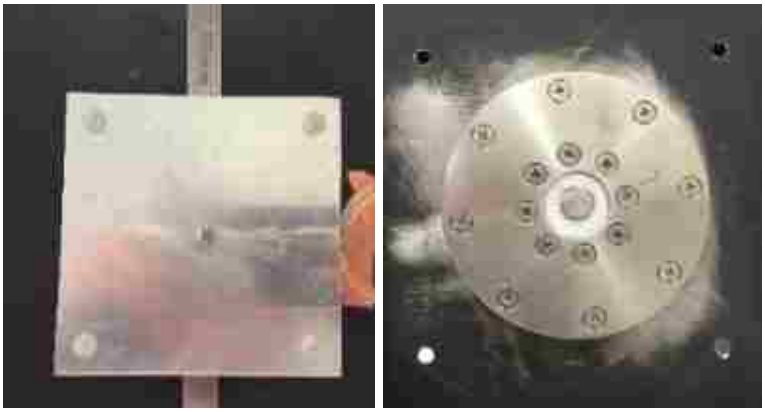


Figure 1. Block diagram of secondary ESD discharge measurement setup.

1.2. SETUP FOR SECONDARY DISCHARGE INSIDE OF A TWO-WIRE POWER SUPPLY

Next, a different setup configuration is investigated in which the secondary discharge occurs inside of a two-wire power supply. This presents a challenge for discharge

current measurement, since the event of interest occurs at a location inside of the DUT which cannot be directly probed. As a result, ESD-induced currents measured at the gun tip have degraded rise times and amplitudes, caused by the capacitive and inductive filtering between the injection point and the origin of the spark inside the system. To create a primary charging event, the ESD gun is discharged to the metal enclosure in contact mode. The metal enclosure is affixed to the low-voltage connector of the two-wire power supply. The two-wire power supply is connected directly to the power strip, while the metal enclosure is connected via a 1 GΩ high-voltage resistor to the same power strip. The F-65 current clamp is positioned at the tip of the ESD gun to monitor the discharge current during ESD testing as depicted in Figure 3.



(a) (b)

Figure 2. (a) Non grounded 10 cm × 10 cm plane. (b) 1.9 Ω current target mounted on the shielded enclosure, located underneath the plate.

A 100:1 passive probe is used to monitor voltage on the floating metal enclosure, while a wire loop probe is positioned near the two-wire power supply to detect the occurrence of ESD events.

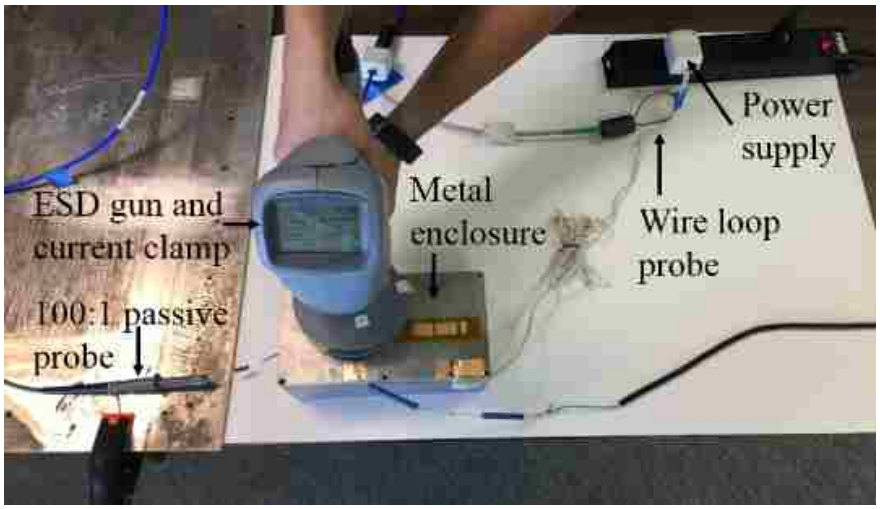


Figure 3. Measurement setup for secondary ESD discharge inside of a two-wire power supply.

2. SECONDARY DISCHARGE WAVEFORMS AND EVENT DETECTION

The secondary ESD event may follow a primary charging event by a variable time delay, ranging from nanoseconds to milliseconds. This variable time delay is known as the statistical time lag. Most modern oscilloscopes offer the capability to detect separate events as a sequence of individual captures. In sequential capture mode, the complete waveform consists of a number of fixed-sized segments. An oscilloscope utilizes sequenced acquisitions by selecting the desired number of segments, maximum segment length, and total available memory, which determines the actual number of events acquired. A sequential acquisition is useful for capturing many rapidly occurring ESD events, or for capturing intermittent ESD events separated by long time gaps.

To capture these waveforms in the time domain, the user sets the trigger level and enables a segmented acquisition mode in the oscilloscope [15]. However, a digital

oscilloscope is temporarily blind even with the segmented acquisition mode enabled [16]. The blind time refers to the duration in between two segmented events, which cannot be acquired by the oscilloscope. The blind time or the intersegment time may range from a few hundred nanoseconds to milliseconds depending upon the type of acquisition architecture used internally within the oscilloscope. In our measurement setup, the oscilloscope intersegment time was approximately 1 μs. One way to avoid losing signals due to the oscilloscope blind time is to select a sufficiently long time record in the range of few hundred milliseconds to several seconds for the oscilloscope time base. Increasing the time capture window size of the oscilloscope allows for the capture of secondary ESD events, but also results in reduced sampling rate of the acquired waveform. The concept of capturing both the primary and secondary discharge events is illustrated in Figure 4.

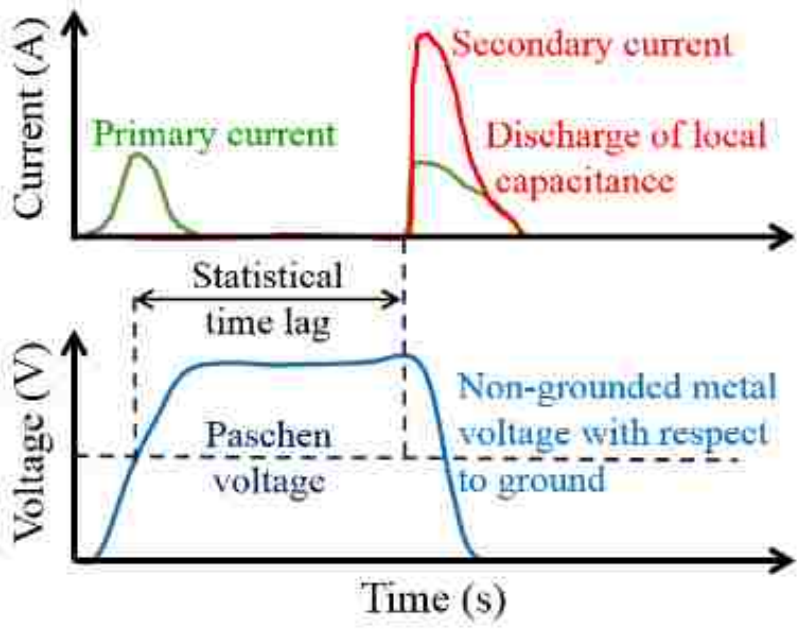
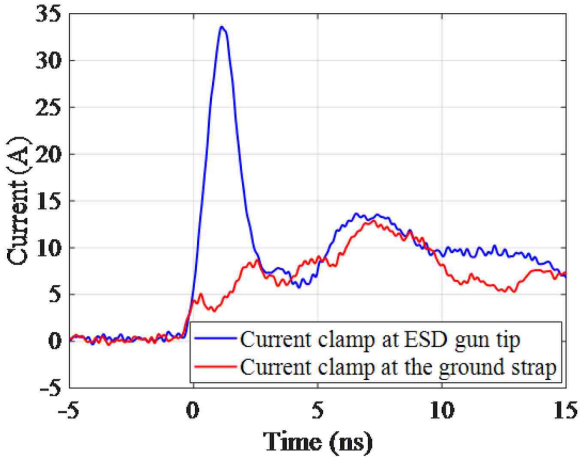


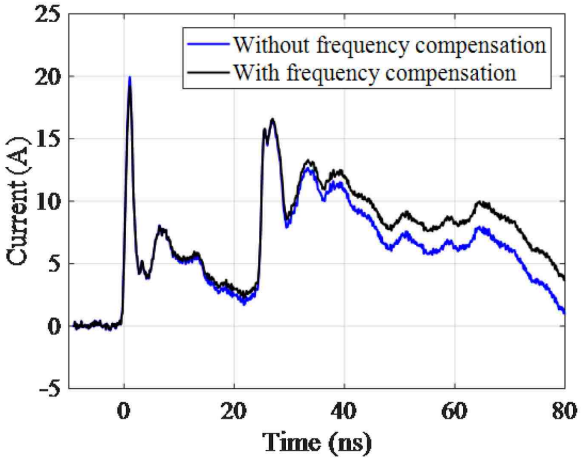
Figure 4. Graphical illustration of a typical ESD event followed by a secondary discharge event. The decrease in the metal plate voltage is the indication of the occurrence of a secondary discharge event.

Locations for monitoring discharge using an F-65 current clamp can include the tip of the ESD gun, the ground cable of the ESD gun, or the power cable connecting the DUT to the two-wire power supply. The advantage of positioning the F-65 current clamp at the tip of the ESD gun allows for highfrequency components of the discharge current to be detected. However, probe loading changes the waveform shape of the acquired discharge current in this configuration. A disadvantage of this configuration is that positioning the current clamp at the tip of the ESD gun adds another measurement cable into the setup. By contrast, positioning the F-65 current clamp at the ESD gun ground strap offers the advantages of being geometrically convenient and minimizing probe loading, however the relatively longer distance between the probe location and the ESD gun tip creates the disadvantage of not detecting the initial peak current due to high-frequency attenuation through the cables, impacting the measured waveform as shown in Figure 5(a).

In addition, the measurement waveforms acquired using the F-65 current clamp require frequency response compensation for the time-domain acquired waveform [17]. For example, the transfer impedance of a typical current clamp is not constant across its operational frequency range, but instead provides a flat response at high frequencies, and increased losses at low frequencies. Thus, the low-frequency slope of the current clamp transfer impedance can result in distortion of the acquired waveform. The high-frequency components associated with the rise time of an ESD pulse are sufficiently captured by the current clamp. However, compensation is needed for the low-frequency response corresponding to the low-frequency trailing end of the pulse. A method for compensating the low-frequency slope of a current clamp using deconvolution is presented in [17], and the resultant waveform is shown in Figure 5(b).



(a)



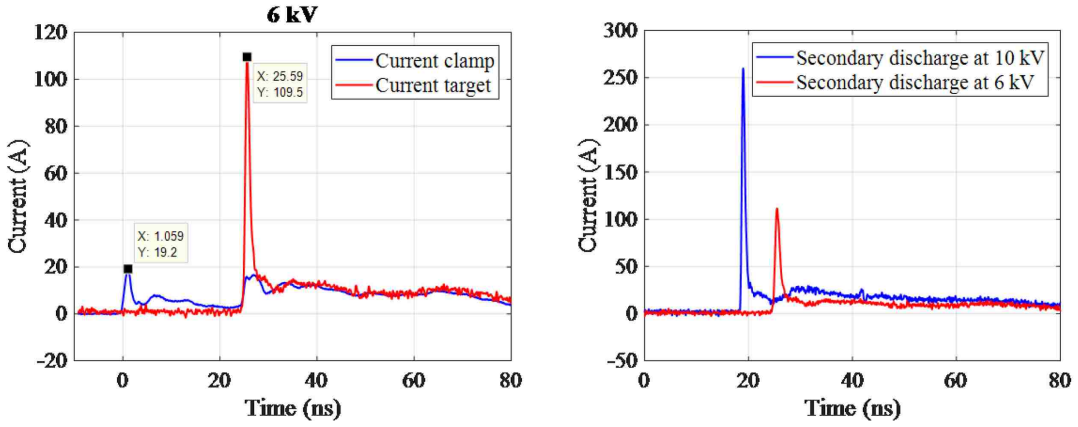
(b)

Figure 5. Waveforms acquired using F-65 current clamp. (a) Comparison of the F-65 current clamp monitor location at the ESD gun tip and the ESD gun ground strap. (b) Comparison of the uncompensated frequency response measured using the F-65 current clamp with the compensated F-65 current clamp measurement.

2.1. MEASUREMENT RESULTS FOR THE CONTROLLED SETUP

The measurement results for the controlled setup of 6 kV and 10 kV ESD gun voltage settings in contact mode discharge are shown in Figure 6. A spark gap of 0.8 mm

requires approximately 3.91 kV as the minimum breakdown voltage to result in secondary discharge. The breakdown voltage (also called "Paschen value") for a specific spark gap distance is calculated using the formula given in [9]. The time lag between primary and secondary events depends on the discharge voltage setting, gap length, surface materials, and humidity [1]. The higher the discharge voltage, the lower the time lag for the secondary discharge event. An example waveform for the occurrence of the secondary discharge at 10 and 6 kV as well as the influence on time lag is shown in Figure 6(b).



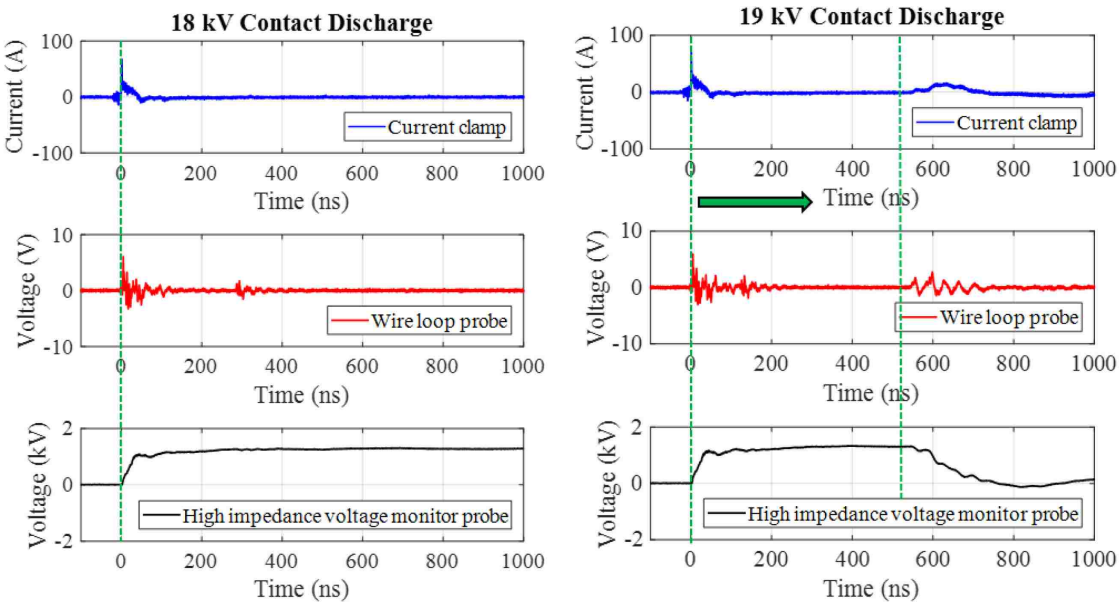
(a) (b)

Figure 6. Measured waveforms on the controlled setup. (a) Primary charging waveform measured using an F-65 current clamp, and secondary discharge waveform measured using a current target. (b) Secondary discharge due to 10 kV occurs approximately 6 ns before the secondary discharge due to 6 kV. The primary ESD event occurring at 0 ns is not included in this figure.

2.2. MEASUREMENT RESULTS FOR SECONDARY DISCHARGE INSIDE OF A TWO-WIRE POWER SUPPLY

The ESD gun was discharged in contact mode into the metal enclosure as shown in Figure 3. The waveforms were measured from 6 to 18 kV in steps of 2 kV, and the results

for the 18 kV ESD gun discharge are shown in Figure 7(a). The first vertical dashed line is a visual representation of the time at which the ESD gun was discharged into the DUT. There is no secondary discharge at 18 kV setting as shown in Figure 7(a). At a 19 kV setting, all three measurement monitors identify the occurrence of a secondary discharge event at approximately 545 ns as shown in Figure 7(b). The second vertical dashed line in Figure 7(b) represents the occurrence of the secondary discharge event. The stable voltage amplitude of the high impedance voltage monitor probe shown in Figure 7(a), and its collapsing amplitude approaching zero after approximately 545 ns in Figure 7(b), provide clear evidence of nonexistence and occurrence of a secondary discharge, respectively.



(a) (b)

Figure 7. Measured waveforms on the two-wire power supply setup using the F-65 current clamp placed at the tip of the ESD gun measuring the discharge current, the wire loop probe positioned near the two-wire power supply to monitor any disturbances inside of the two-wire power supply and the high impedance voltage probe to monitor the floating metal voltage. (a) 18 kV discharge. (b) 19 kV discharge with secondary ESD event occurring at 545 ns.

3. SOFTWARE-ASSISTED DETECTION

During ESD compliance testing, multiple test points are chosen for ESD injection. Often, an automated robotic system is tasked with executing a suite of tests, which determine the failure voltage or current levels [18]. While such a system can produce a pass/fail report, it does not help to determine the root cause of the failure due to ESD discharge or secondary discharge events. A software-assisted secondary ESD detection algorithm is proposed to identify the secondary ESD events during testing. To detect an event, the discharge current at the ESD gun tip using an F-65 current clamp and the charge delivered obtained from the current clamp waveform are analyzed.

For an algorithm to differentiate secondary events from primary events, pre- and post-pulses, and reignition events, the characteristics of the primary events must first be introduced to the algorithm during the learning sequence. Operator input to the software is also required to select the appropriate ESD gun voltage setting and the DUT configuration. The proposed testing sequence is illustrated in Figure 8. First, the operator needs to discharge the ESD gun onto a large ground plane and measure the discharge current using a current clamp. The tests should begin with a low voltage setting on the ESD gun, for example, 1 kV, where it is expected that there will be no secondary ESD events occurring inside of the DUT. The current clamp waveform is analyzed for the charge delivered into the DUT, the next rising edge after the primary event and the next fast changing *dI/dt* (slope) after the primary event. If the charge ratio criteria or the next rising and the next fast changing *dI/dt* criteria are met, then the algorithm concludes that the secondary ESD

has occurred. Otherwise, the algorithm suggests increasing the ESD gun discharge voltage to the next voltage increment and repeat the test procedure.

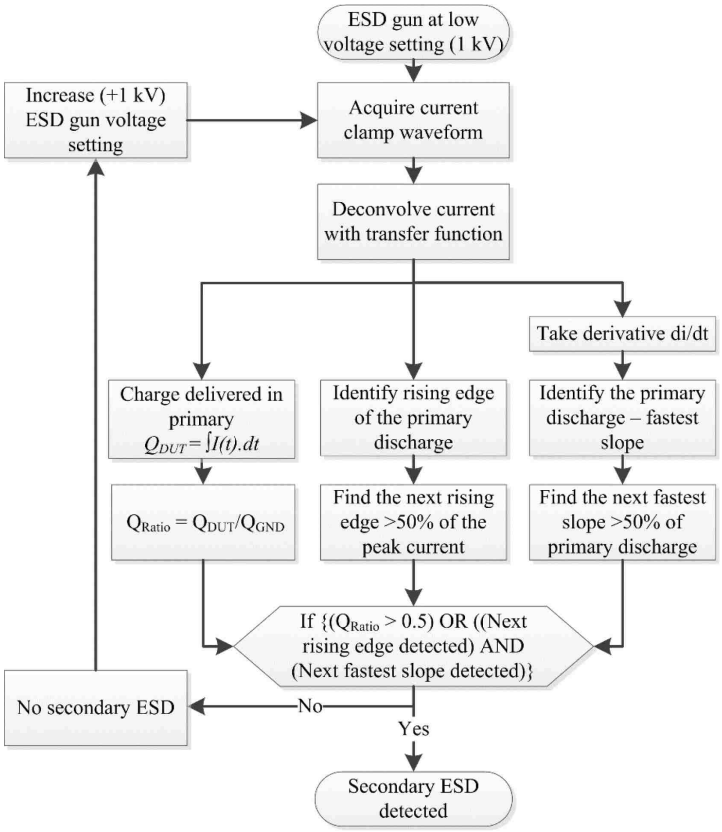


Figure 8. Flowchart of the suggested algorithm for secondary ESD detection based on the secondary ESD waveforms acquired using a current clamp.

3.1. CHARGE-BASED DETECTION

One method to detect the occurrence of a secondary ESD event would be to analyze the amount of charge delivered to the DUT. During an ESD test session, the test sequence begins with measuring the charge delivered to a large ground plane. For a low voltage setting of 1 kV, a secondary ESD event is not expected. Once the ground discharge Q_{GND} result is available to the operator, then the ESD gun is discharged with the same voltage

setting to the DUT. The charge delivered to HCP can also be used as a discharge reference value. However, the quantity of charge delivered to the HCP is less than the ground plane discharge. The HCP has a capacitance to the comparatively larger ground plane and it is also connected to the ground plane by two 470 kΩ resistors in series, thus the ESD gun delivers less quantity of charge to the ground plane.

$$Q(t) = \int I(t) \cdot dt \tag{1}$$

$$Q = C \cdot V \tag{2}$$

In (1), charge Q is the integration of measured current I with respect to time t. In (2), Q is equal to the product of capacitance C and voltage V. In our case, the large ground plane-based discharge is used as reference during the learning sequence while testing. First, the charge Q_{DUT_1kV} delivered using (1) is determined. The detection algorithm compares the Q_{DUT_1kV} with Q_{GND_1kV}, and the resulting ratio is $Q_{Ratio} = Q_{DUT\_1kV}/Q_{GND\_1kV}$. It is important to note that this detection method requires a time capture window which includes both events. In addition, the time corresponding to the charge calculation for the ground and the DUT discharge must be equal. If the Q_{Ratio} is less than 0.5, then this suggests that the test point is nongrounded (a capacitive load) with a possibility of spark gap structures existing within the DUT geometry causing secondary ESD occurrences at higher test voltages. For example, as shown in Table 1, the charge delivered into the DUT at 1 kV is 14 nC. Using the relation given in (2), where V is equal to the ESD gun voltage of 1 kV. The effective capacitance obtained is approximately 14 pF. If the discharge was injected into a grounded device, most of the ESD gun charge would be delivered into the DUT and $Q_{Ratio} = Q_{DUT\_1kV}/Q_{GND\_1kV}$ would be approaching unity. Since the Q_{DUT} is approximately 14 nC and the Q_{Ratio} is less than 0.5, with a capacitance of 14 pF, it strongly suggests that

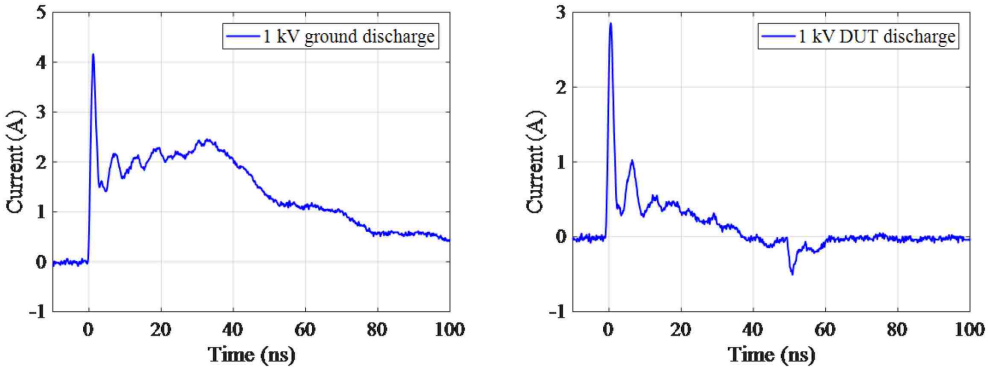
the DUT is a nongrounded device. This provides an indicator that a secondary ESD event may be possible if one of the spark-gap structures breaks down at a higher ESD voltage setting.

Since at 1 kV the charge ratio is not greater than 0.5, the operator is guided to increase the ESD gun voltage to 2 kV and the process is then repeated. If the Q_{Ratio} criteria for Q_{DUT_2kV} with Q_{GND_2kV} is similar to the previous discharge voltage, then the ESD testing is continued with higher ESD gun test voltages in +1 kV increments. It is important to note that Q_{Ratio} will remain the same at higher voltages, because contact mode ESD gun discharges are linearly proportional to the voltage setting. However, this holds true only when no secondary ESD occurs.

Table 1 provides the Q_{Ratio} values obtained during a learning sequence from 1 to 8 kV applied to the controlled setup. Figure 9 illustrates the current waveforms for the low voltage 1 kV in which no secondary ESD event occurred. In addition, it depicts the waveforms at 6 kV, when the secondary ESD occurred. A Q_{Ratio} plot is illustrated in Figure 9(e), which depicts the increase in the charge delivered into a DUT when a secondary ESD event occurs.

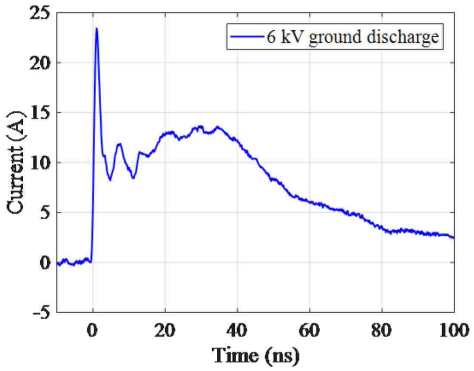
Table 1. Learning sequence and charge based analysis.

ESD gun Voltage	Charge delivered to ground Q_{GND}	Charge delivered to DUT Q_{DUT}	$Q_{Ratio} = Q_{DUT}/Q_{GND}$
1 kV	140 nC	14 nC	0.10
2 kV	250 nC	29 nC	0.12
3 kV	393 nC	48.4 nC	0.12
4 kV	475 nC	57.06 nC	0.12
5 kV	659.3 nC	98.62 nC	0.15
6 kV	825 nC	727.5 nC	0.88
7 kV	941 nC	856.9 nC	0.91
8 kV	1132 nC	991.6 nC	0.88



(a)

(b)



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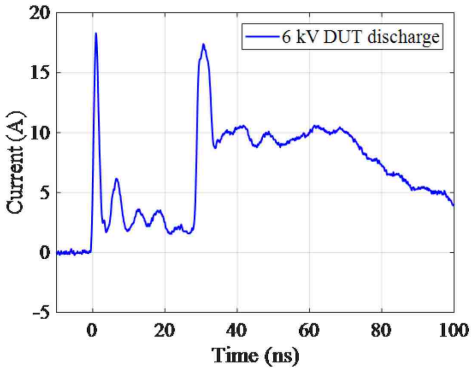
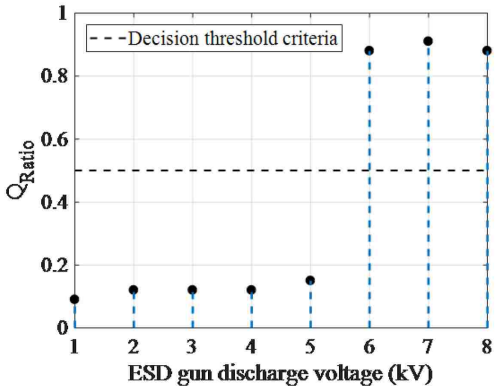


(d)



(e)

Figure 9. Measured F-65 current clamp waveforms. (a) Current waveform at 1 kV ESD gun discharge to ground plane. (b) Current delivered at 1 kV ESD gun discharge to DUT. (c) Current waveform at 6 kV ESD gun discharge to ground plane. (d) Current delivered at 6 kV ESD gun discharge to DUT, with a secondary ESD event. (e) Q_{Ratio} parameter for a test sequence from 1 to 8 kV based on the Table 1 data.

During the testing sequence with incrementally higher ESD gun voltage discharges, when Q_{Ratio} is higher than 0.5, the software identifies it as a secondary ESD event occurrence. For example, in the controlled setup geometry depicted in Figure 1, for a 6 kV ESD gun discharge setting, $Q_{Ratio} = Q_{DUT\_6kV}/Q_{GND\_6kV}$ is greater than 0.5. Thus, the quantity of charge delivered to the nongrounded metal produces sufficient overvoltage to break down the spark gap distance within the DUT geometry. The relationship between charge and voltage is given in (2), where C is the capacitance of the nongrounded metal to the grounded reference which is a constant based on DUT geometry. Therefore, as the ESD gun voltage level is increased, a higher amount of charge is delivered with each subsequent ESD discharge into the DUT. Since the nongrounded metal has a fixed capacitance, the amount of voltage generated across the spark gap in the nongrounded metal increases with each higher ESD gun voltage setting.

This detection methodology is based on a learning sequence which initiates with low test voltages and does not require the operator to have knowledge of the internal DUT geometry details, such as the nongrounded metal's capacitance, or the spark gap distances. As an example, if the maximum reliability level for testing is 8 kV, and a secondary ESD event has not yet occurred, then the DUT is considered immune to secondary ESD events for voltages up to 8 kV.

3.1.1. Total Charge in the Secondary and Primary ESD Event. Analyzing events using the concept of total charge delivered into the controlled setup is shown in Figure 6(a). It is observed that the charge associated with the secondary ESD event is more than the primary event. The F-65 current clamp measures the ESD gun discharge and the current target measures the secondary ESD. To understand the QDUT delivered, the

measured waveform is further analyzed in terms of Qprimary and Qsecondary ESD events. Here, the primary ESD event was defined from 0 ns to approximately 25 ns. The total charge delivered during this time window is approximately 130 nC.

The secondary ESD event begins at approximately 25 ns. The total charge contained in Qprimary from 0 to 25 ns is equal to total charge contained in Qsecondary from time 25 to 27 ns, due to the law of charge conservation. After 27 ns, the extra current measured by the current target is due to the residual charge delivered by the ESD gun. The charge delivered during the primary and secondary events is indicated by the shaded areas of Figure 10.

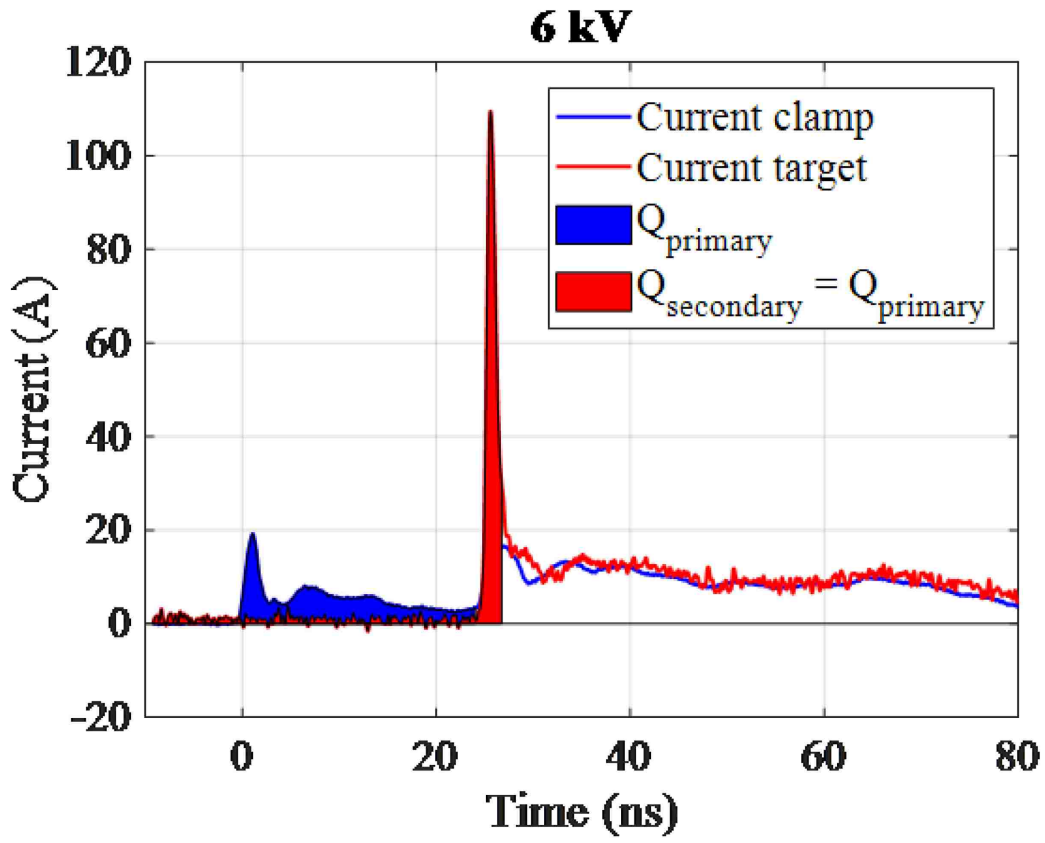
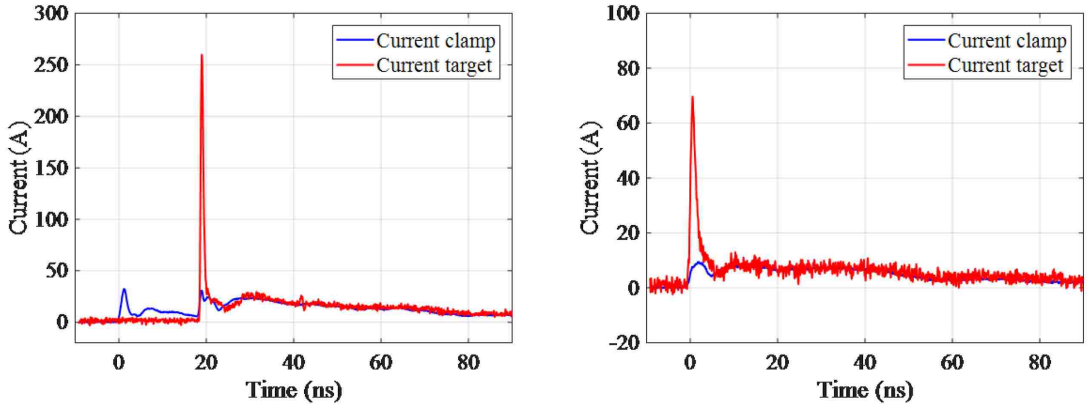


Figure 10. $Q_{primary}$ = $Q_{secondary}$ = approximately 130 nC. Charge delivered after 27 ns is due to residual current from the ESD gun.

The ESD gun in contact mode delivers charge to the nongrounded floating metal, but does not deliver complete charge into the floating structure until after the spark gap distance breaks down. At 25 ns, the spark gap distance of approximately 0.8 mm breaks down due to the overvoltage potential, causing the secondary ESD event. The spark resulting from the spark gap breakdown becomes a nonlinear resistive conductive path connecting the nongrounded metal with the ground reference. At this time, the ESD gun, still connected to the nongrounded plate in contact mode, has a residual charge current path to ground formed by the secondary ESD spark conductive channel which can be given by $Q_{DUT} = Q_{primary} + Q_{secondary} + Q_{residual\_ESD\_gun}$.

3.1.2. Events due to Residual Charge in the ESD Gun. After the primary and secondary discharge events occur, multiple secondary discharges, referred to as ESD gun reignition discharges, are possible due to residual charge buildup on the ESD gun tip. The software-based detection method can only identify multiple secondary events which occur within the same time capture window as the primary event. However, since these ESD gun reignition discharges have lower peak current than the secondary ESD event, they can be considered less important than the secondary ESD events for detection purposes.

In such situations, $Q_{primary}$ will be discharged during the secondary ESD event. The spark initiated by the secondary ESD allows residual charge to be delivered from the ESD gun tip after the occurrence of secondary ESD. The charge on the primary nongrounded metal must have sufficient overvoltage for the spark gap to break down for reignition events to occur. An example of reignition of the ESD gun after 5.8 ms after the first triggered event is shown in Figure 11.



(a) (b)

Figure 11. (a) First triggered event on the oscilloscope. (b) Reignition discharge event is 5.8 ms after the first triggered event with an ESD gun voltage setting of 10 kV.

3.2. DISCHARGE CURRENT WAVEFORM-BASED DETECTION

A detection method based on the rising edge and *dI/dt* is applied to the waveforms generated using the configuration shown in Figure 1. The detection results are determined for the two discharge cases of 6 and 10 kV, shown in Figure 12.

Waveform-based detection using the rising edges of the current waveform is depicted in Figure 12(a) and (c). The peak discharge amplitude is determined for the contact mode discharges using the transfer function 3.75 A/kV. As an example, an ESD gun voltage setting of 6 kV would be converted to 22.5 A. Using a 50% threshold of the peak amplitude, the primary event positive-polarity trigger threshold level is determined. The waveform sample points located above these threshold criteria are highlighted in Figure 12(a) and (c). A time gap separates the primary and secondary ESD events. In Figure 12(a), a time of 25 ns is detected by the suggested algorithm to be the start of the secondary ESD event.

The slope-based detection method calculates *dI/dt*. By applying a threshold crossing to the derivative function, the start time for primary or secondary discharge can be determined, as shown in Figure 12(b) and (d).

The secondary ESD event current can reach five times the amplitude of the primary current [1]–[4] and have faster rise times. If the secondary ESD event is not probed in close proximity to the source, a degradation in measured rise time and current amplitude will occur. This degradation of the acquired waveform can lead to missed detection using the rising edge and *dI/dt* (slope) based detection methods.

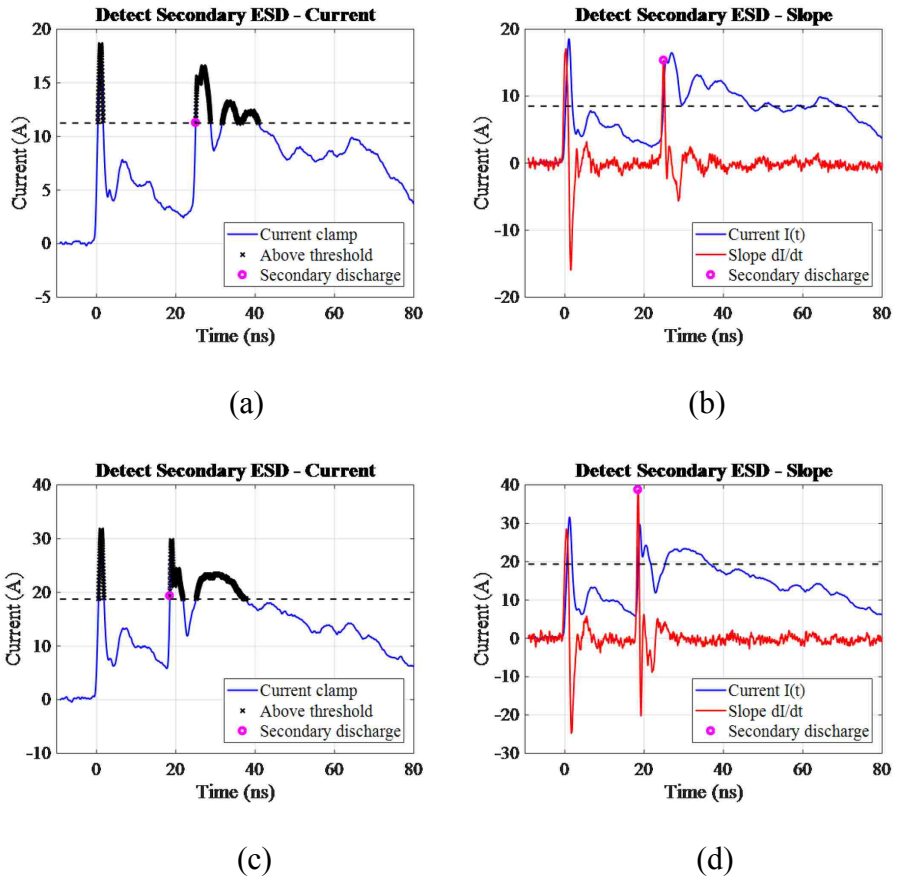


Figure 12. Secondary ESD detection using the rising edge and slope detection algorithm. (a) 6 kV rising edge-based detection. (b) 6 kV slope-based detection. (c) 10 kV rising edge-based detection. (d) 10 kV slope-based detection.

4. DISCUSSION

The suggested software-assisted detection of a secondary ESD event is based on measurable quantities such as current and charge. For system-level testing, it may be challenging to physically access all of the measurement test points. The use of a current clamp allows for current measurements to be performed from outside of the DUT. The acquired current waveform dataare used for secondary ESD detection based on the rising edge and slope-based algorithms.

However, these methods have two limitations based on the bandwidth of the measured data. First, since the F-65 current clamp is required to capture the current waveform, but also results in measurement system bandwidth reduction, highfrequency content such as fast transition times are reduced, which limits the software algorithm abilities to detect all occurrences of secondary discharge. Second, if the placement of the F-65 current clamp is relatively far from the occurrence of secondary discharge, then high-frequency content will be filtered by the transmission path, resulting in further system bandwidth reduction at the observation point. The charge-based method described in Section III resolves the bandwidth limitation problems, which impacted the accuracy of the rising edge and slope-based algorithms. An example in which the chargedbased method succeeds where the rising edge and slope based algorithms fail, is in a two-wire power supply setup, in which the F-65 current clamp did not capture the secondary ESD event rise time with high resolution. This leads to a missed detection using the rising edge and the slope method as shown in Figure 13.

In Figure 13, the charge-based method does detect the extra charge delivered during the secondary ESD event that ranges from approximately 550 to 800 ns. In order for the detection algorithm to work, the algorithm must be provided Q_{Ratio} values starting with a low-voltage case and then incrementing subsequently higher ESD gun voltages.

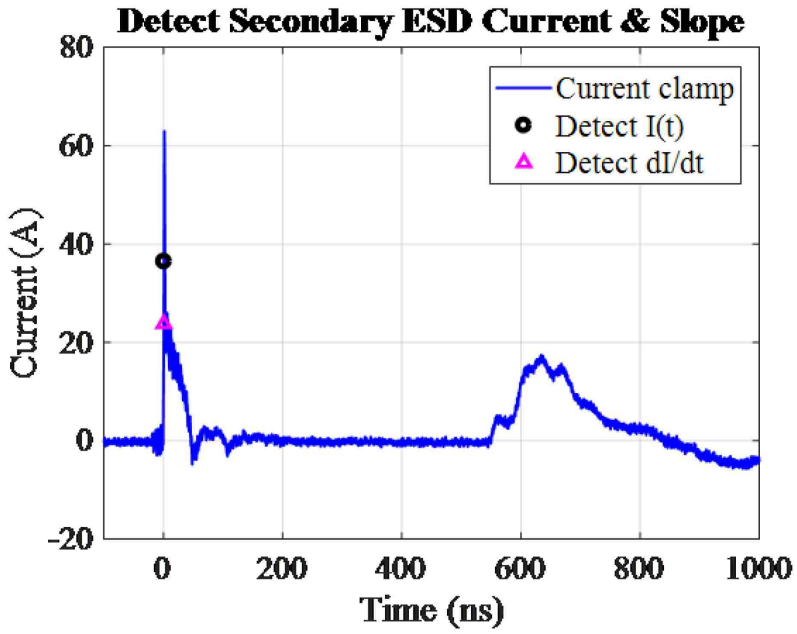


Figure 13. Detection based on the rising edge and the slope of the measured current for the two-wire power supply setup.

In order to determine if a device is floating, it should first be checked with low-voltage inputs. Once a low Q_{Ratio} value is computed for low-voltage inputs, this confirms a floating device which may be subject to spark gap breakdown at higher input voltages. The detection logic during the learning process is based on the sudden change in the Q_{Ratio} value during a secondary ESD event which did not previously occur for low-voltage inputs when the Q_{Ratio} value was low. To facilitate more rapid testing for secondary ESD, a smaller set of input voltages could be used. For example, the operator could first inject with a low

voltage of 1 kV to verify a floating device, then input a second high voltage at the maximum desired ESD reliability test level, for example, 8 kV. If the Q_{Ratio} at 8 kV and the Q_{Ratio} at 1 kV are both below 0.5, then a secondary ESD event did not occur. However, if the Q_{Ratio} at 8 kV is > 0.5 and the Q_{Ratio} at 1 kV < 0.5, then this indicates the presence of a secondary ESD event.

An additional advantage of the charge-based method is immunity to an overlapping primary and secondary discharge. In the case where overvoltage across the spark gap results in a secondary ESD event that overlaps with the primary event, the overlapping events may result in non-detection by the rising edge and slope-based methods, whereas this situation can be clearly detected using the charge-based method.

5. CONCLUSION

The purpose of this study was to analyze secondary discharge events acquired with various measurement setups, in order to identify waveform parameters for software-assisted algorithms, and to verify the occurrence and detection of secondary ESD events using current clamp-acquired waveforms. Multiple measurement setups and configurations were used, and several software algorithms were applied for detection. The use of software-assisted algorithms based on the acquired current waveforms can be flexible across multiple measurement setup scenarios, allowing secondary discharge events to be identified. The proposed detection methods were shown to work well across a range of configurations. As shown in Figure 8, multiple methods can also be combined to increase detection robustness.

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II. MEASUREMENT-BASED CHARACTERIZATION AND FULL-WAVE MODELING OF ESD TO DISPLAY TOUCHSCREEN SENSORS

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ABSTRACT

An electrostatic discharge (ESD) to display cover glass can damage touchscreen traces by sparkless corona discharges on the glass surface. The ESD induced currents are measured in an evaluation setup, which resembles the touch pattern. Each air discharge event leads to multiple waveforms, which are acquired using a fast-retrigger mode in the oscilloscope. The induced currents are analyzed using the peak value, and the total charge. The statistical behavior of the induced currents is determined for different parameters such as glass thickness, indium tin oxide layer equivalent resistance, sensor spacing to the ground plane, air discharge polarity and voltage, and ESD gun approach speed. The goal is to create a full-wave simulation model to predict the induced currents in the touchscreen sensors for various discharge parameters. Using the full-wave model, the source excitation current waveform is determined, which allows prediction of the displacement currents into

a single touchscreen sensor patch. The waveform then can be applied to different touchscreen sensor display geometries to determine if damage might occur.

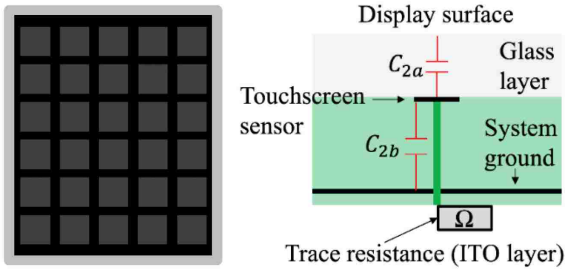
Keywords: Air discharge, corona discharge, displacement current, display, human metal model (HMM), surface discharge.

1. INTRODUCTION

Multiple mechanisms can damage a display if it is subjected to an Electrostatic Discharge (ESD) event. ESD events can lead to soft and hard-failures in display products [1]-[2]. A spark cannot penetrate through the display, but if the display is not well-insulated at the product edges, during an ESD event a spark can occur which can couple to the driving circuits of the display [3]. The spark may hit the flex cable or if the insulation undergoes an electrical breakdown [4], thus, leading to permanent damage to the insulation layer at the edges of the display. For well-designed displays products, the spark cannot occur, thus, leading to sparkless discharges. Even though there is no visual indication of the spark, a corona current charges the surface of the glass [5]-[6]. Displacement current flows through the display cover glass into the internal touchscreen structures.

Many consumer electronic products provide display and touchscreen functionality. The touchscreen sensors are typically positioned under the display cover glass. The users touch the display cover glass and the touchscreen sensors record the touch location from the user. The user can be charged and may discharge on the display cover glass. The ESD event on the glass surface leads to induced currents through the display cover glass into the touchscreen sensors. Figure 1 illustrates the simplified stackup of a touchscreen display

electronic product. Glass layer represents a display cover glass, which typically has the touchscreen sensors on the inner side of the display glass surface. The touchscreen sensor has a capacitance to its system ground. The indium tin oxide (ITO) layer which connects the sensor to the display IC has an equivalent series resistance whose value depends on the layout of trace connection between the sensor and the display IC.



(a) (b)

Figure 1. Typical touchscreen sensor geometry. (a) Typical display with touchscreen sensors. (b) Equivalent circuit capacitances and resistances of a single touchscreen sensor.

The sparkless discharge leads to deposition of charges on the glass surface, which can be visualized using the Lichtenberg's dust figure [7]. The visualization of the charges illustrated that the positive discharges led to a branching structure, while the negative discharges led to more concentrated, not branching like charge deposition [6], [8]. However, the dust figure only allows the visualization of the charges but does not show the time-domain waveforms. To address this problem, Muller [9]-[11] proposed a setup to measure the partial currents by using a segmented ground plane. In [6], a similar approach was used to capture the charge, streamer velocity, time, and displacement currents.

This paper builds on the work performed by Gan *et al.* [6] and focuses on quantifying the worst-case risk due to sparkless ESD discharges to the touchscreen sensors

underneath the display cover glass. Since the display is an insulator, air discharge testing is performed. An automated measurement setup was developed to control parameters such as ESD generator approach speed, the temperature, and relative humidity. For a given display geometry, the ESD generator total discharge current, and the ESD induced waveforms into the touchscreen sensor patches are monitored. A full-wave simulation modeling approach is presented to obtain the source excitation waveforms, which leads to the ESD induced waveform into a single touchscreen sensor patch.

2. MEASUREMENT SETUP

An evaluation geometry was designed and manufactured. The setup was automated to measure multiple waveforms for each test scenario. Since, the air discharge event has variations, having multiple discharges provides a statistical distribution of the induced currents into the touchscreen sensor patches. To control the parameters such as temperature and relative humidity, the setup was positioned in a climate chamber. The chamber held the temperature at 75°F (24°C) and relative humidity (RH) of 32% approximately. Human metal model (HMM) discharges were performed on the evaluation geometry to quantify the ESD risk, as the testing process of displays is performed using an ESD generator in air discharge mode with a rounded metal tip [12].

2.1. EVALUATION PRINTED CIRCUIT BOARD (PCB) GEOMETRY

An evaluation PCB is designed to analyze the influence of touchscreen sensor geometry parameters such as display glass thickness (C_{2a}), sensor-to-system-ground capacitance (C_{2b}), and the ITO layer equivalent resistance (R_{trace}) as shown in Figure 1. The

evaluation PCB is designed to match a typical touchscreen sensor geometry, as shown in Figure 2. Multiple squares are representative of the various touchscreen sensor patches below the display cover glass. These sensors are designed on the top layer of thee evaluation PCB. Vias connect each sensor to the bottom layer, where a surface mount metal electrode leadless face (MELF) resistor is connected in series. This resistance represents the equivalent Indium Tin Oxide (ITO) layer resistance in a display product. The third layer (inner layer) of the PCB is assigned the ground reference plane.

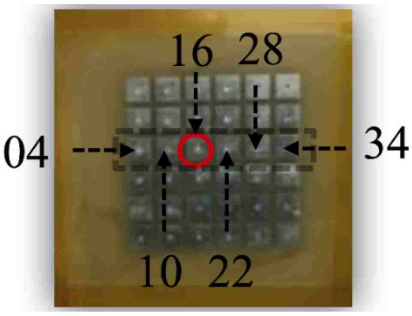


Figure 2. Designed evaluation PCB touchscreen sensor patch display geometry.

2.2. AUTOMATED HMM DISCHARGE SETUP

To enable acquisition of multiple discharges for measuring the statistical distribution of the ESD induced currents, the setup was automated. The block diagram of the full-automated setup is depicted in Figure 3.

2.2.1. ESD Generator Approach Speed Control. Guide-rods were used to guide the movement of the ESD generator. Two motors along with forward and return single pole double throw (SPDT) switches were installed to guide the movement of the ESD generator at a constant speed of approach toward the device under test (DUT). The

motor control board was designed to control the speed, direction, and movement of the motors.

2.2.2. ESD Generator Voltage and Polarity. A USB-to-Serial and Serial-to-Optical interfaces circuits were designed and implemented on the ESD generator control board. The control board allowed remote control setting of the ESD generator test voltage and polarity of the discharges.

2.2.3. Shielded Enclosure. The display cover glass and the evaluation PCB were installed vertically at the enclosure slot facing the ESD generator air discharge tip. The DUT was installed at the enclosure slot, to prevent any undesired field coupling from the ESD generator [6], [13]-[15] into the measured waveforms on the oscilloscope. The direct probing coax cables monitored the respective touchscreen sensor patch waveforms during an air discharge event. ESD attenuators and ESD protectors were connected between the coax cables and the individual oscilloscope channels to prevent any unintentional ESD stress damage to the oscilloscope channels.

2.2.4. Vacuum Pump. Air gaps are undesired, as the real product geometry typically has the touchscreen sensors on the inner side of the display cover glass. Thus, to mimic a real product geometry, the vacuum pump was added in the setup to remove any possible air gaps between the display cover glass and the touchscreen sensor patches on the evaluation PCB.

2.2.5. Ionizer. Each test scenario was measured at least five times. A single air discharge measurement deposited charge on the surface of the display cover glass. An ionizer was used to remove the charges deposited due to a single ESD generator air discharge event on the display cover glass. The removal of deposited charges was

necessary to prevent the accumulation of charge on the display cover glass before the initiation of the next test. The accumulation of charges may lead to higher induced currents, and may not be a realistic representation of the ESD stress due to a single test voltage (for example, +15 kV) of the ESD generator.

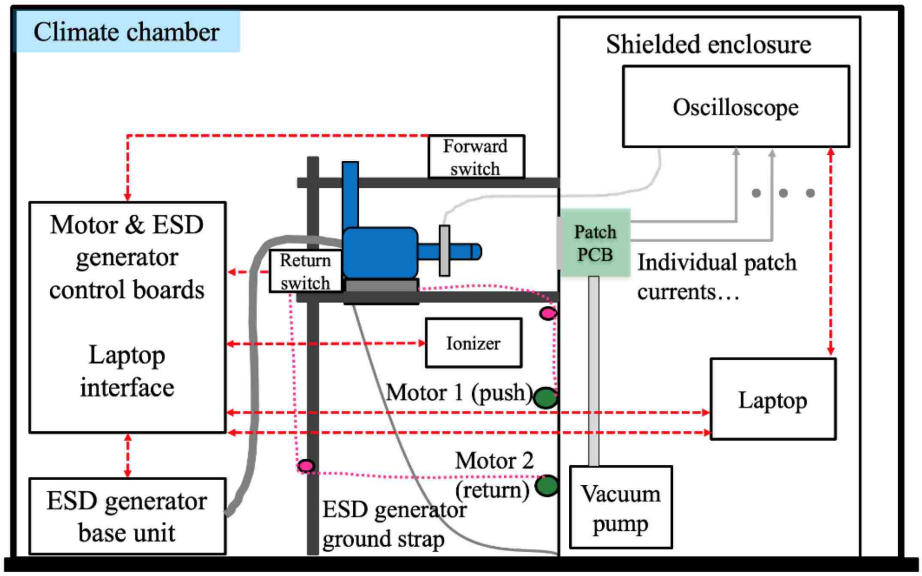
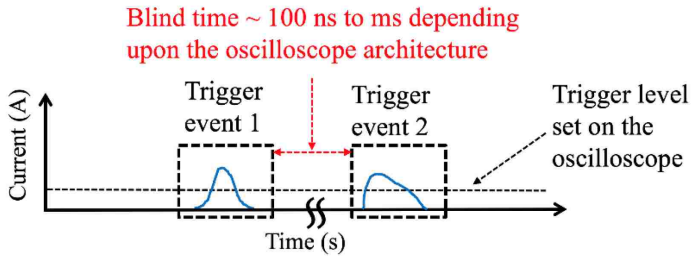


Figure 3. Automated measurement setup positioned in a climate chamber.

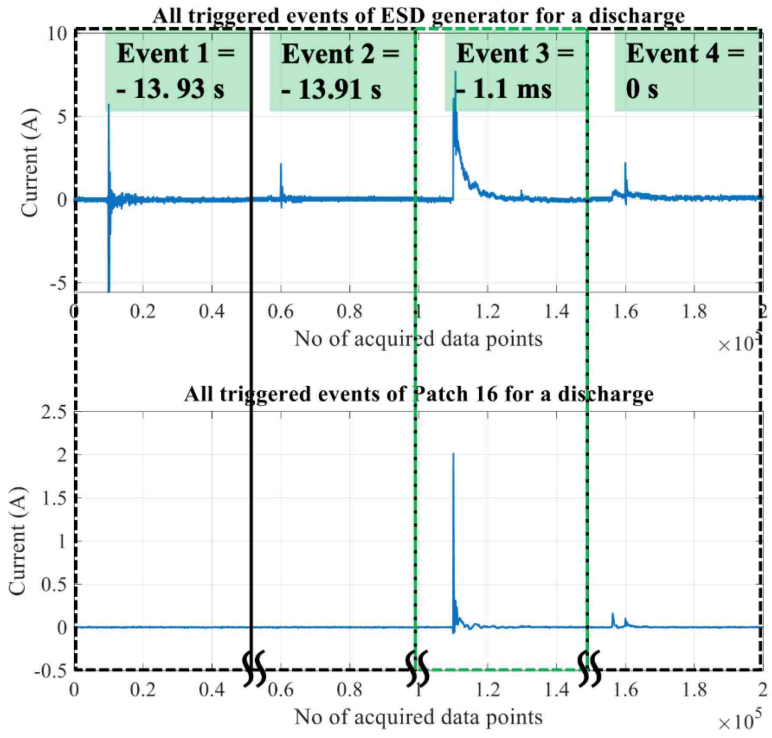
2.3. ULTRA-SEGMENTATION MODE OSCILLOSCOPE ACQUISITION

An approaching ESD generator to the DUT glass surface leads to multiple sparkless discharges. To determine the worst-case induced currents on the touchscreen sensor patches, all the discharges must be acquired. An F-65 current clamp [16] was positioned on the rounded tip of the ESD generator. The F-65 current clamp signal was used to trigger the oscilloscope. The fast-retrigger mode acquisition in the oscilloscope is useful in capturing multiple occurring waveforms [13]-[15] separated in time. ESD

generators are known to generate noise pulses apart from the desired discharge pulse [13]-[15]. It is important to distinguish the desired discharge pulses from the noise pulses. An example of multiple triggered events due to a single ESD generator discharge is illustrated in Figure 4.



(a)



(b)

Figure 4. Ultra-segmentation or fast-retrigger mode on the oscilloscope. (a) Qualitative explanation of the multiple triggered events during an air discharge event. (b) Selection of the worst-case ESD generator discharge waveform at the DUT surface.

As shown by this example, one approach of the ESD generator led to four triggered events on the oscilloscope. In Figure 4, two channel's data, one for the F-65 current clamp measuring the ESD generator discharge current and another channel monitoring the induced current into one of the multiple touchscreen sensor patches is depicted. It was observed that the first two events captured on the F-65 current clamp, did not have a corresponding waveform in the triggered events 1 and 2 of the touchscreen sensor patch 16. However, events 3 and 4 showed an induced waveform on the sensor due to the waveform captured at the ESD generator tip. Thus, the initial events 1 and 2 are noise pulses, which are caused by the internal switching of the relay, and cause no induced currents into the touchscreen sensors. When the ESD generator discharged at the surface of the glass, the events 3 and 4 were recorded later. Within the multiple discharge events that led to the induced currents, only the worst-case event was selected for risk analysis. It is important to note that from a hard-failure perspective, the worst-case induced current event will cause possible damage to the ITO layer within the product. Furthermore, each test is repeated at least five times to understand the variance in the measured worst-case event.

3. MEASUREMENT RESULTS

Table 1 illustrates the key geometry parameters within a display touchscreen sensor stackup. For each experiment, one geometry parameter was changed, and the other parameters were kept constant. The change in the induced ESD currents into the touchscreen sensor patches, as a function of change in the geometry parameters, was recorded.

Table 1. Design parameters of the display geometry.

Range of values	Glass capacitance (C_{2a})	Sensor to system ground capacitance (C_{2b})	ITO equivalent series resistance (R_{trace})
Minimum	430 fF	2.9 pF	100 Ω
Maximum	650 fF	2.9 pF	100 Ω

The measurement results for a particular geometry stackup selection of a 0.6 mm thick glass with a dielectric constant of about 7.3, which leads to an effective glass capacitance of 650 fF for a 2.5 mm x 2.5 mm sensor patch area. One of the evaluation PCBs were designed to have the ground plane in the third layer of the four-layer PCB. The top layer of this PCB consisted of the touchscreen sensor patches. Surface-mount resistors were mounted on the bottom layer of the PCB. The second layer of the PCB was not used, but a large ground layer was assigned to the third layer of the PCB. This geometry led to a sensor to system ground capacitance value of 2.9 fF, which was obtained via low-frequency electrostatics field solver using computer simulation technology (CST) full-wave software [17]. A surface mount pulse resistor of 50 Ω in series with the 50 Ω oscilloscope channel impedance leading to a total series resistance of 100 Ω.

As illustrated in Figure 4, during a single approach of the ESD generator toward the DUT multiple discharge events, are triggered on the oscilloscope. The worst-case event, which induced maximum ESD current into the touchscreen sensor patch, was selected. The test was performed five times, and the resulting worst-case event F-65, center sensor patch (directly underneath the ESD generator tip), 1st adjacent sensor patches, 2nd adjacent sensor patch, and 3rd adjacent patch time-domain waveforms are illustrated in Figure 5. For each plot, a zoom-in of the first few nanoseconds of the time-domain waveforms is depicted.

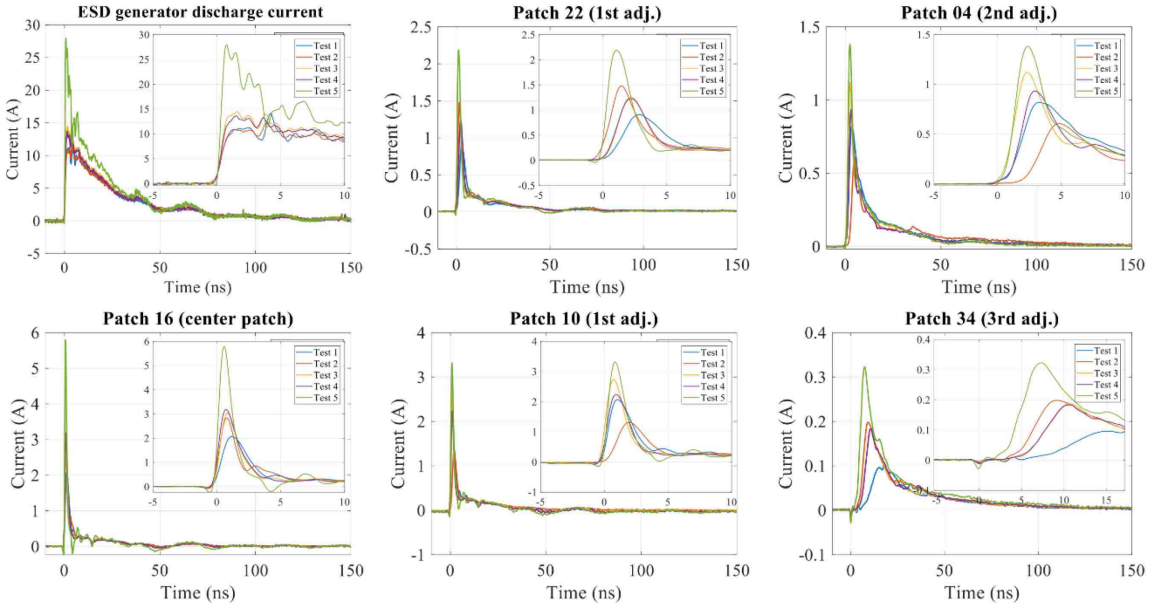


Figure 5. Measured data for 0.6 mm (thin glass, C2a = 650 fF), 3rd layer PCB ground (C2b = 2.9 pF), 100 Ω ITO series resistance (Rtrace), 0.3 m/s approach speed at +15 kV ESD generator air discharge setting.

The HMM discharge waveform acquired using the F-65, and the ESD induced waveform into the patch directly underneath the discharge location was quantified based on peak and charge delivered.

$$Q(t) = \int I(t) \cdot dt = C \cdot V(t) \quad (1)$$

$$E = I^2(t) \cdot R_{trace} \quad (2)$$

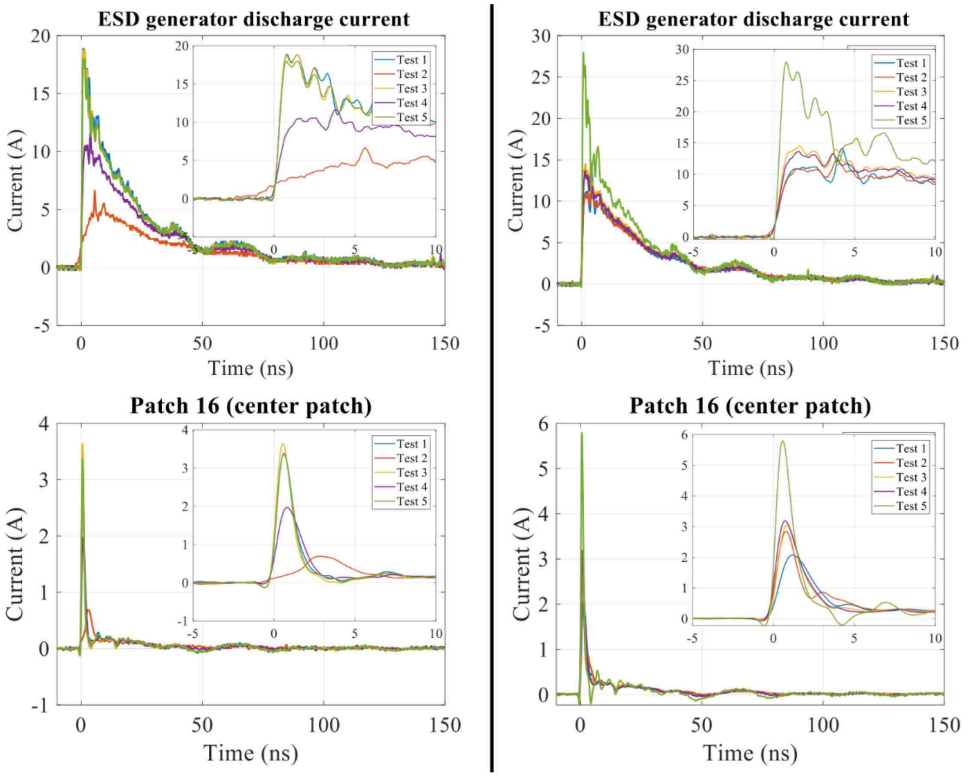
Where Q, is the charge delivered to the touchscreen sensor patch over a specific time interval from $t = 0$ ns to $t = 150$ ns. The charge delivered can also be estimated by the voltage V at the touchscreen sensor and its capacitance C relative to the DUT geometry ground. The energy E delivered is determined by taking the square of the current value for each instant of time, multiplied by the effective resistance (R_{trace}) seen by the touchscreen

sensor. The energy delivered is to the touchscreen sensor is a criterion used to determine hard-failure of the ITO traces inside the display geometry. It is a known failure mechanism, where the energy delivered leads to the heating of the metal interconnects [18]-[20], and based on the layout parameters such as thickness, width, shape, the material characteristics can lead to a burn-out.

Relative to the current at the glass surface (ESD generator discharge current), the induced currents into a single touchscreen sensor patch directly underneath the discharge location are smaller in peak, pulse width, and the charge delivered. For instance, a peak of 28 A, charge of 480 nC was recorded for the ESD generator current at the top of the glass. However, a peak of only 6 A and charge of 18 nC was induced in the touchscreens sensor as shown in Figures 5, 6, and 7. In addition, the peak and charge in the adjacent touchscreen sensors are lesser than the center patch, which is directly underneath the discharge point on the glass surface.

In terms of worst-case risk estimation, it was observed from the measurements that the center patch records the worst-case current waveform both in terms of peak current and the charge delivered (area under the current waveform). For all further testing, the emphasis was placed on the touchscreen sensor patch directly underneath the discharge location and was termed as the worst-case touchscreen sensor patch. Figure 6(a) illustrates the ESD generator discharge and center touchscreen sensor patch waveforms during a +15 kV HMM discharge when display cover glass capacitance (C_{2a}) was 430 fF. However, when the display cover glass was changed to thinner glass thickness, the effective C_{2a} was approximately 650 fF. The higher glass capacitance, led to higher induced ESD stress into the touchscreen sensor patch as depicted in Figure 6(b). The peak discharge current for

both the ESD generator and induced center touchscreen patch 16 was higher when higher capacitance glass was used. The thicker glass with lower capacitance (430 fF) led to smaller currents than the 650 fF glass capacitance case. For instance, a peak of 18 A and charge of 40 nC was recorded for the ESD generator current at the top of the thick glass with lower capacitance. However, a peak of 28 A and charge of 480 nC was recorded for the ESD generator current at the top of the thin glass with higher capacitance. Similarly, the effect of higher ESD stress due to higher display cover glass capacitance was observed in the peak and charge delivered into the touchscreens sensor, as shown in Figures 5, 6, and 7.



(a) (b)

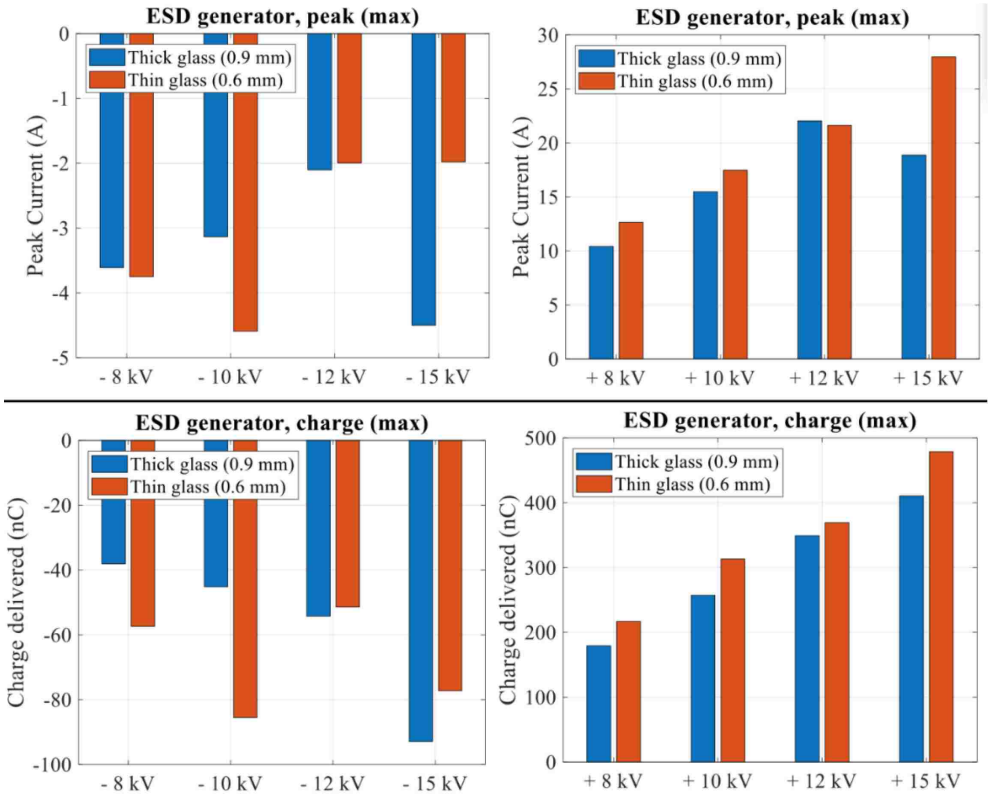
Figure 6. DUT geometry with 3rd layer PCB ground (C_{2b} = 2.9 pF), 100 Ω ITO series resistance (R_{trace}), 0.3 m/s approach speed at +15 kV ESD generator air discharge setting. (a) Measured data for 0.9 mm (thick glass, C_{2a} = 430 fF). (b) Measured data for 0.6 mm (thin glass, C_{2a} = 650 fF).

Five discharges were performed at each polarity and the test voltage of the ESD generator. The measurement-based characterization was performed from ±8 kV to ±15 kV. For each test case, one worst-case peak and the charge delivered (150 ns) was computed for the ESD generator discharge current and the center touchscreen sensor patch. The distribution of the peak and charge delivered as a function of polarity, test voltage, and the display cover glass thickness is shown in Figure 7(a) for the ESD generator discharge current waveform. Similarly, Figure 7(b) illustrates the distribution of the peak and charge delivered to the worst-case touchscreen sensor patch.

For the intended application of ESD testing of display products, ±15 kV is considered as the realistic maximum worst-case test voltage. It should be noted that, an increasing trend in the charge delivered is not observed for the negative polarity test voltages from – 8 kV to – 15 kV, for both the ESD generator discharge current and the worst-case touchscreen sensor patch. However, to quantify the realistic worst-case ESD induced risk, the positive polarity test voltages showed and an increasing trend for both ESD generator discharge current and the worst-case touchscreen sensor patch. Thus, from a realistic worst-case risk estimation perspective, the +15 kV testing provides the maximum peak and the charge delivered into a single touchscreen sensor patch. Considering the energy or charge delivered [21] into the touchscreen sensors as the main-failure mechanism for the burnout of the ITO traces, the +15 kV testing provides the measurement-based realistic worst-case risk parameters.

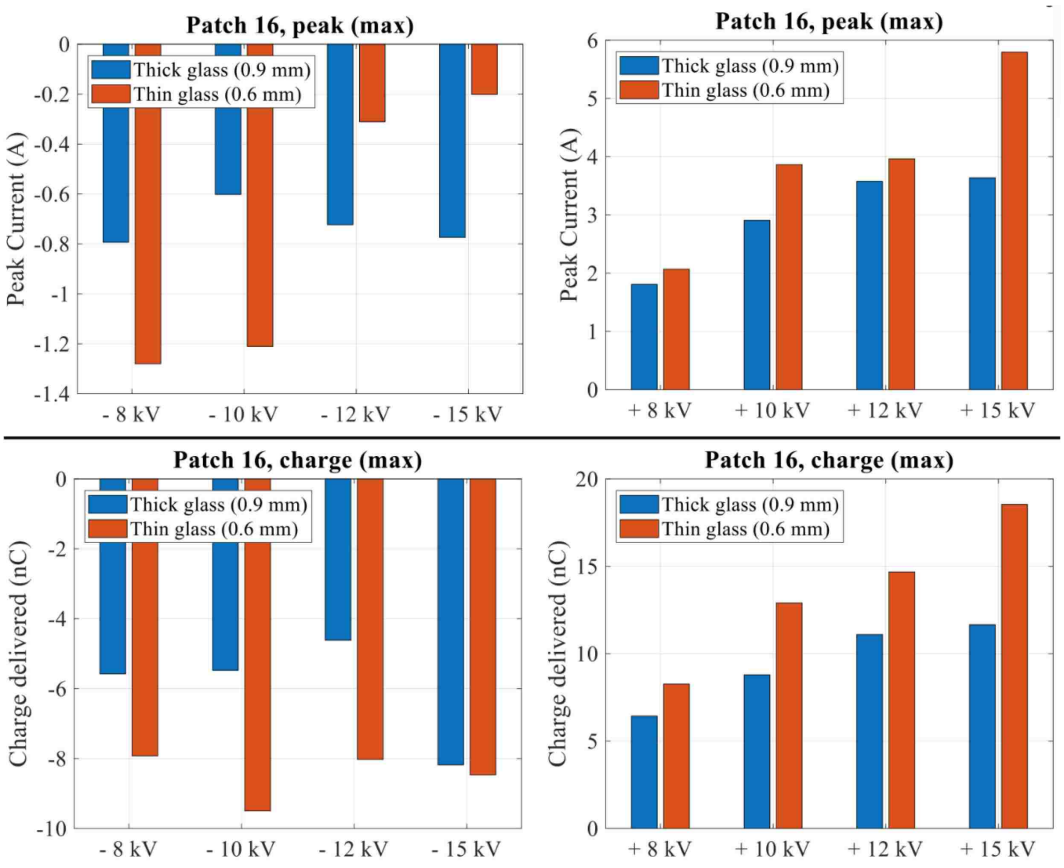
This evaluation geometry-based testing can be further applied to other display geometry parameters such as different values of C_{2a}, C_{2b}, and R_{trace}, and the risk parameters can be obtained. The general trends observed from measurement suggest that a higher

display cover glass capacitance (C_{2a}) leads to more ESD induced currents into the touchscreen structures. In the process of reducing product thickness, the display cover glass thickness may be reduced to attain a thinner product. However, this may lead to increased glass capacitance if the same dielectric constant glass is used. If the equivalent resistance (R_{trace}) is small, then higher induced currents are expected into the touchscreen structures. Careful estimation of the display geometry parameters C_{2a}, C_{2b}, and R_{trace}, are needed to assess the realistic worst-case ESD induced risk to the inner electronic structures of the display.



(a)

Figure 7. Measured data for 0.6 mm (thin glass) & 0.9 mm (thick glass), 3rd layer PCB ground, 100 Ω ITO series resistance, 0.3 m/s approach speed at +15 kV ESD generator air discharge setting.



(b)

Figure 7. Measured data for 0.6 mm (thin glass) & 0.9 mm (thick glass), 3rd layer PCB ground, 100 Ω ITO series resistance, 0.3 m/s approach speed at +15 kV ESD generator air discharge setting. (a) ESD generator discharge current measured using F-65. (b) Worst-case touchscreen sensor patch (cont.).

4. FULL-WAVE SIMULATION MODELING

The goal of the full-wave simulation model allows system-level EMC engineer to run simulations to analyze the impact of the ESD induced waveforms to the internal display structures, their dimensions, spacing to the neighboring traces or system ground to prevent arcing or secondary ESD discharges within the product.

The air discharge event on the glass surface leads to charge deposition. These charges can be visualized using Lichtenberg's dust figures [6]-[7]. The positive discharges show to distinguished zones, the corona discharge close to the ESD generator electrode, and the streamers, which lead to radial branching structures [6]. The current flows on the surface of the glass with a propagation velocity of about 0.3 to 1 mm/ns.

On the contrary, the negative polarity discharges lead to non-branching charge deposition, with the charge deposition being localized near the ESD generator electrode discharge location [6]. From a modeling perspective, the touch screen sensors are large. Thus they capture charge due to corona discharge and the multiple branches for positive polarity discharges. Similarly, for negative polarity discharges, the charge is captured from the localized charge deposition. From a realistic worst-case perspective, the touchscreen sensor patch directly underneath the discharge electrode is subjected to the maximum ESD induced displacement currents. Thus, the modeling of the propagation velocity and the corona current on the radially outward touchscreen sensor is not critical. The risk is determined only for the touchscreen sensor patch directly underneath the discharge location.

To perform early design stage simulations, a source excitation waveform is determined using simulation which models the measured touchscreen sensor patch waveform. By acquiring the ESD generator discharge current using F-65, the total waveform is determined, which gets deposits the charge on the glass surface during the air discharge event. However, the charge which is deposited directly over the touchscreen sensor patch area is the only relevant charge which causes displacement currents to flow through the display cover glass into sensors. Thus, using circuit simulation and full-wave

simulation, the exact source waveform is obtained. Once the source waveform of a single patch for a specific display geometry is known, this waveform can be used to excite a similar display geometry to estimate the early design stage ESD robustness using full-wave simulation.

The simulation workflow is illustrated in Figure 8. The evaluation PCB geometry design was imported to CST and was assigned the appropriate material properties, boundary condition, and the frequency range of evaluation was set up to 2 GHz. The measurement bandwidth for the ESD generator discharge current was limited to 1 GHz due to the frequency bandwidth of the F-65 current clamp. However, higher frequency bandwidth measurement up to 2 GHz was available for the touchscreen sensor patch currents.

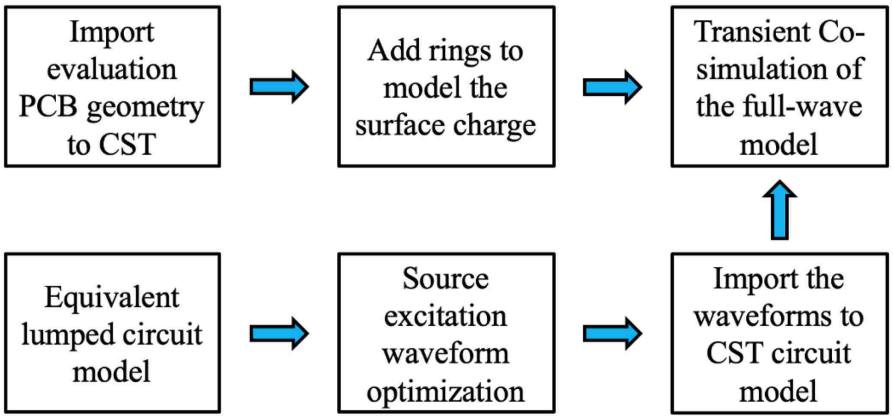


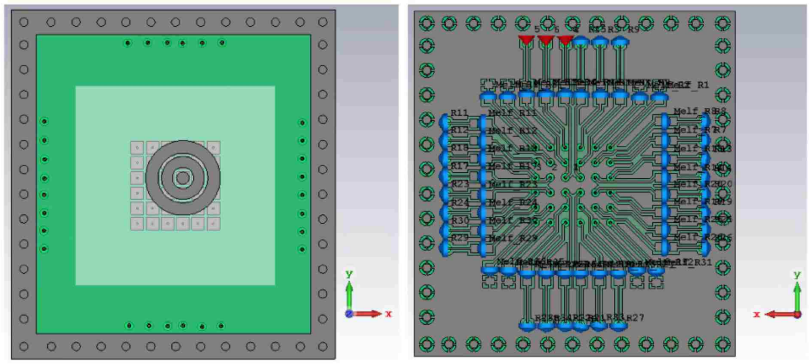
Figure 8. Simulation workflow.

Based on Lichtenberg dust figure visualization of the surface charge deposition study performed in [6], it is known that the diameter of the surface area is not a linear function of the test voltage and polarity. The surface discharge current was modeled using

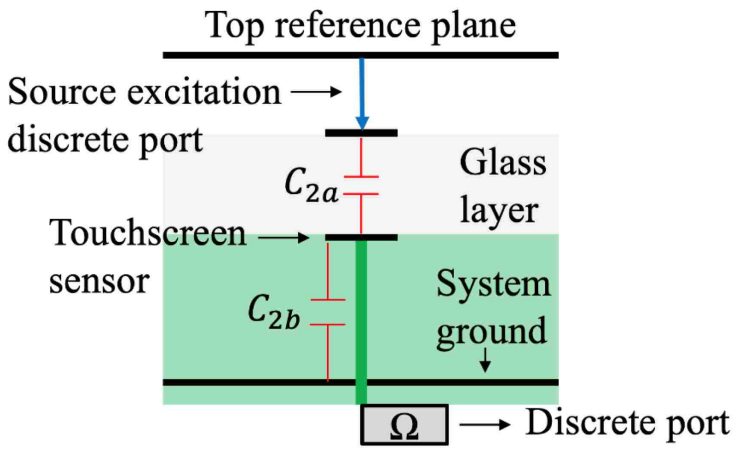
the proposed method of multiple annuluses by the authors in [6], and [11]. The glass was divided into several rings. The ring sizes were optimized to cover the respective touchscreen sensor patches. To provide an excitation waveform, a discrete port was placed per ring. The ring to ring spacing was adjusted to reduce the cross-coupling between the rings. A perfect electric conductor (PEC) reference plane was used as the reference for the discrete excitation ports, which only exists in the simulation model. The reference in measurement setup is based on the ESD generator ground strap and the parasitic return of the high-frequency components of the discharge waveform at the tip of the ESD generator. The ring structures are shown in Figure 9(a) and (c). Figure 9(b) illustrates the bottom view of evaluation PCB, which consists of lumped elements to model the SMD resistors. Additionally, discrete ports were only placed at the touchscreen sensor patches of interest to monitor the ESD induced displacement currents, while optimizing the total simulation time.

A circuit simulation approach was used to model the source excitation waveform. As a first step to the waveform optimization process, a simplified equivalent circuit for the display geometry was determined in terms of equivalent glass capacitance, touchscreen sensor capacitance to system ground, and the equivalent trace resistance. To identify the equivalent glass capacitance, a parallel plate capacitor method was employed. The copper tape was placed on both sides of the glass, and the capacitance was determined using the LCR meter and was additionally verified using Z_{11} measurement The touchscreen sensor capacitance to system ground was determined using a low-frequency solver (electrostatic solver) in the CST software. Additionally, the electrostatic solver was used to determine the capacitance of the ring to the reference ground in the simulation model. Two

exponential decay current sources were used to model the source excitation waveform, as shown in Figure 10(a). Parameters such as peak (I_high), the time constant (tau1) for the rising edge, the time constant (tau2) for the falling edge, and the delay parameter for tuning the separation between the two-time constants. The optimized waveform obtained from the circuit simulation model is shown in Figure 10(b). The optimization of the source excitation waveform is concluded once the waveform current waveform at the 50 Ω termination resistance matches the measured touchscreen sensor patch waveform.

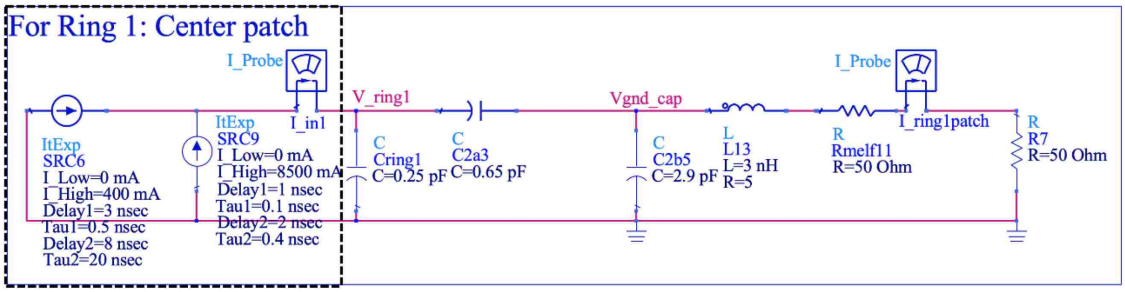


(a) (b)

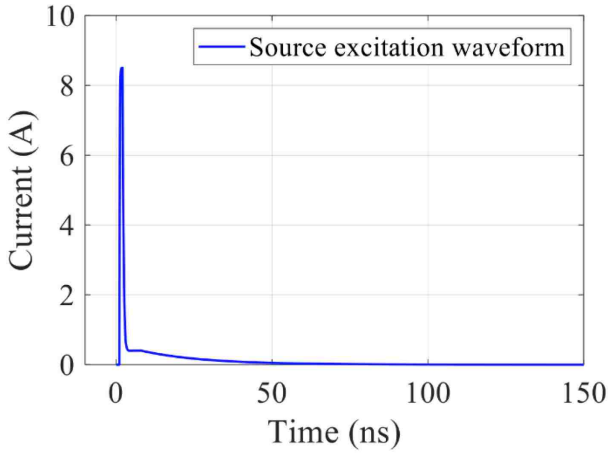


(c)

Figure 9. Simulation model illustrating the concentric ring structures.



(a)



(b)

Figure 10. DUT equivalent circuit geometry simulated using the advanced designed system (ADS) software.

The optimized source excitation waveform obtained only of the center patch is imported to the CST full-wave model as an excitation source to the transient co-simulation model. The same process can be repeated to identify the source excitation waveforms for the surrounding rings which cover the adjacent touchscreen sensor patches. However, to illustrate the worst-case risk to a single touchscreen sensor patch, only the simulation process is depicted for the center touchscreen sensor patch. However, it could be extended to other rings to have a more comprehensive model. The transient co-simulation block is illustrated in Figure 11. The simulation waveform at the current probe (P4) as illustrated in

Figure 11 is compared with the measured touchscreen sensor patch waveform in Figure 12. The two ESD induced waveforms are compared for peak, charge, energy delivered, and the rise time and the quantitative comparison is shown in Table 2.

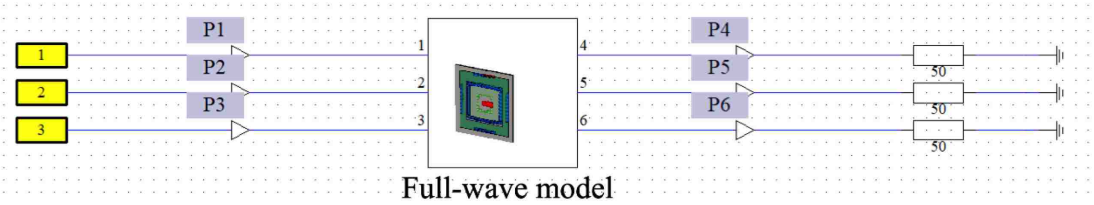


Figure 11. Transient co-simulation block diagram.

Table 2. Waveform parameters for the worst-case touchscreen sensor patch at +15 kV.

Parameters	Measurement	Simulation
Peak current	5.8 A	5.9 A
Charge	16 nC	15 nC
Energy	3.1 uJ	3.5 uJ
Rise time	0.53 ns	0.51 ns

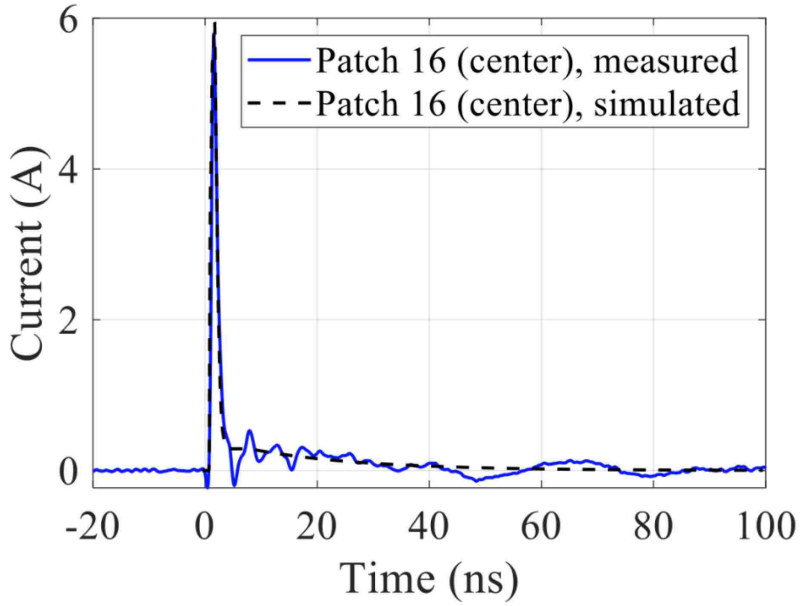


Figure 12. Comparison of the measured and simulated worst-case ESD induced waveform.

5. DISCUSSION

The focus of this work was to develop an ESD to display characterization method for early design stage robustness evaluation of touchscreen sensors. To this aim, an evaluation geometry was designed to mimic the touchscreen structures and quantify the measured ESD induced displacement currents. To assess the ESD risk, it might be late to wait for the physical hardware units to perform ESD risk analysis. To better design or define design guidelines for the layout of the ITO traces which connect the touchscreen sensors to the display driver ICs, a measurement-based approach was proposed. The evaluation PCB geometry parameter values such as the glass capacitance, sensor to system ground capacitance, and equivalent trace resistance were selected based on a real display geometry.

Characterization of the evaluation geometry was performed using HMM testing, with ±15 kV as the maximum test voltage for the intended application of compliance testing of displays within electronic products. A fast approach speed of 0.3 m/s was considered as a realistic worst-case approach speed for the ESD generator air discharge tests. It is known that slower approach speeds lead to lesser ESD induced risk [5]. Relative humidity was selected to be approximately close to 30 % to perform testing at the lower end (dry conditions) of the suggested range provided by IEC standard [12].

During an air discharge, the ESD generator current measured by the F-65 current clamp provides the total discharge current over the glass surface. However, this total current waveform may lead to over estimation. Using the measurement-based characterization of the display geometry, only the touchscreen patch directly underneath

the discharge location records the worst-case ESD induced displacement currents. The surrounding sensor patches are exposed to a lower induced risk. In reality, a user can touch and discharge into any part of the display. Thus, every touchscreen sensor patch for the display can be designed to withstand the ESD risk obtained from one touchscreen sensor patch.

A full-wave simulation model was provided to model the measured ESD induced waveforms into the touchscreen sensor patches. During an HMM discharge, the charge is deposited on the glass surface. The HMM discharge waveform is measured using an F-65 current clamp. However, it measures the total current discharged from the ESD generator to the entire glass surface. Thus, an ADS equivalent circuit model was used as the first step in the modeling process to obtain the exact source waveform, which is subjected to the single touchscreen sensor patch. The source waveform was obtained from the optimization of the two-exponential decay current sources. The optimized waveform was then applied as an excitation source to the virtual concentric rings in the full-wave model, to obtain the induced touchscreen sensor patch currents using transient co-simulation approach. In this simulation approach, only one simulation of the coupled circuit-EM problem is performed, with exactly the excitation signal, which is defined in the circuit model. Both the circuit and the EM problem are solved simultaneously. This transient co-simulation approach typically leads to a faster simulation time than the standard EM/circuit co-simulation, as no general s-parameters are needed to be calculated.

This approach provides a realistic worst-case excitation waveform for a single touchscreen sensor. Using this information, early design stage simulations can be performed by replacing the evaluation PCB geometry in the full-wave model with the

actual product display geometry. The simulation can highlight if the energy delivered into a single touchscreen sensor can damage the ITO trace. Typically, the layout of all touchscreen sensor ITO traces is concentrated at one location of the display edge, where they make a connection to the driver IC. In this region, the traces are routed close to each other and may have a thinner trace width or thickness to allow for multiple ITO traces to be routed in a small area. The layout of ITO traces in this region is highly susceptible to hard-failures due to the ESD induced energy. Here additional thermal simulations are needed to quantify further the possibility of a burnout using the ITO trace geometry parameters and using the induced ESD current waveform's energy as an excitation source. The goal of this work was only to quantify how much current can be induced into the touchscreen structures.

6. CONCLUSION

An evaluation geometry was designed to quantify the HMM discharge ESD risk to the touchscreen sensors in an electronic display. The measurement setup was automated to enable multiple measurements on the DUT. Positioning the setup inside the climate chamber provided a controlled temperature and humidity during air discharge testing. Characterization was performed on the DUT structure to identify the worst-case currents from the ESD generator and the induced currents into the touchscreen sensor patches. The currents were quantified by their peak, energy delivered, and rise time. The influence of test voltage, the polarity of test voltage, and display cover glass thickness was quantified. Currents up to 6 A, with hundreds of picosecond rise time, pulse-widths in the range of

tens of nanoseconds, and charges of about 16 nC, were induced into the touchscreen sensors. The currents induced into the touchscreen sensors will be much smaller than ESD generator currents on the top of the glass, as the sensors only capture a percentage of the ESD energy. The parameter values for worst-case sensor currents were found for a single touchscreen sensor for test voltages up to ±15 kV.

A full-wave model was developed to model the measured ESD induced risk to the touchscreen sensors. The goal of the full-wave model is to assist in the early design stage of a product cycle. It is expected that the typical display geometry, which has the same per-unit-area resistance of the ITO layer and per-unit-area capacitance of the touchscreen sensor, will observe waveforms similar to the evaluation PCB geometry used in this work. Thus, the system-level EMC engineer can run early design stage simulations for the touchscreen sensor display geometry to identify if the worst-case ESD induced waveform may lead to possible hard-failures in the ITO traces due to the amount of energy delivered into it.

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III. EFFECT OF INHOMOGENEOUS MEDIUM ON FIELDS ABOVE GCPW PCB FOR NEAR-FIELD SCANNING PROBE CALIBRATION APPLICATION

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ABSTRACT

In this paper, a method is proposed to calibrate a probe by placing it into a known field and referencing its output voltage to the known field. A transmission line is a convenient structure for creating such a known field. This paper presents the effect of the inhomogeneous medium on the near-field generated over a grounded coplanar waveguide (GCPW) printed circuit board (PCB) and reports the field pattern over the GCPW. GCPW PCBs are used to determine the probe factor for near-field scanning applications. A near-field scan is performed to visualize the near-field sources over a device under test (DUT). The near-field is measured by using E- and H-field electromagnetic interference probes. The output of these probes is a voltage and using the probe factor, the field present over the DUT can be determined. To calculate the probe factor, the near-field strength needs to be known using the 3-D simulation. GCPW creates a quasi-TEM field. The effect of non-

TEM modes is easily underestimated, such that non-TEM fields prevent the user from determining the unwanted field suppression of probes at higher frequencies.

Keywords: E-field probe, grounded coplanar waveguide (GCPW), H-field probe, near-field scanning, probe calibration.

1. INTRODUCTION

Near-field scanning is used to visualize the near-field sources present inside an electronic device. The nearfields are measured using near-field E and H probes. The probes can have a broadband frequency response or a resonant narrowband response. The resonant probes have a higher signal to noise ratio in the narrowband frequency range than the broadband probes. The near-field data obtained using the probes [1]–[3] are valuable; for example, identifying radio frequency interference in mobile devices. One of the applications of the near-field scanning technique is to generate models of ICs or emission sources on PCBs by obtaining the near-field data over the device under test (DUT). This data along the Huygens' surface can be utilized for far-field estimation [4], and for source reconstruction-based investigations [5]. The emission frequency spectrum may range from a few KHz up to 40 GHz and higher. Recent developments in 5G wireless communication and testing have introduced the usage of 20 GHz and higher frequency spectrums [6]–[8] which has created the need for high-frequency near-field scanning probes and their calibration. A few other applications include optical transceivers, harmonics generated from PCI-E on-board, etc., where scanning at 20 GHz and higher frequencies is desirable.

The concept of probe factor calibration refers to the calibration of the voltage at the probe output in a field that is disturbed by the probe, relative to the field that is present without the probe. This way, the effect of the probe on the field is taken into account. The probes usually do not measure the field when the probe is present, but the field which was there before the probe was inserted. Various probe calibration methods are published in literature, for example, a low-frequency probe calibration using the Helmholtz coil (typically from 9 KHz to 10 MHz) and the TEM cell (typically from 9 KHz to 1000 MHz) or the GTEM cell (typically from 9 KHz to 1 GHz) [9]–[11] or free-field calibration using horn antennas. A few other methods mentioned in the IEEE Std. 1309-2013 [11], also include open-ended waveguide (typically from 200 to 450 MHz) and the pyramidal horn antennas (typically from 450 MHz to 40 GHz). The goal of this work is to identify a single-probe calibration method, which can work for large frequency bandwidth. From the available choices, the grounded coplanar waveguide (GCPW) transmission line is selected as it supports wide frequency bandwidth and because of its convenience of measuring the field strength over small heights over the trace structure.

The probe factor calculation steps involve calculating the field strength (using 3-D simulation) above a microstrip or a GCPW PCB based on the desired frequency range of interest. Applying a source excitation to the microstrip or GCPW PCB and placing the near-field probe at the desired height over the PCB by using high-precision robot scanning system [12]. Measurement cables, amplifiers, and attenuators can be included in the calibration procedure. The voltage measured using vector network analyzer (VNA) will be referenced to the simulated field strength, and the probe factor or the system factor is calculated. Probe factor is called as the system factor when the measurement components

such as the cables, amplifiers, attenuators, etc., are included in the measurement set-up. The simulated fields obtained from the simulation model are important to accurately calculate the probe factor [13]. The probe factor for E- or H-field can be given by

$$PF = \frac{E\ or\ H_{simulated}(f, h_{eff})}{S_{21} . V_{simulated}} \tag{1}$$

where the E- or the H-field is obtained from simulation at a fixed frequency f, at an effective height h_{eff} above the surface of the trace. $V_{\text{simulated}}$ refers to the voltage applied at the trace in the simulation model, which generated the simulated E- or H-field above the trace. S_{21} is obtained from the measurement as shown in Figure 1. An accurate probe factor calibration leads to an accurate estimation of the measured field strength over the DUT. An illustration of the probe factor calibration measurement setup is shown in Figure 1.

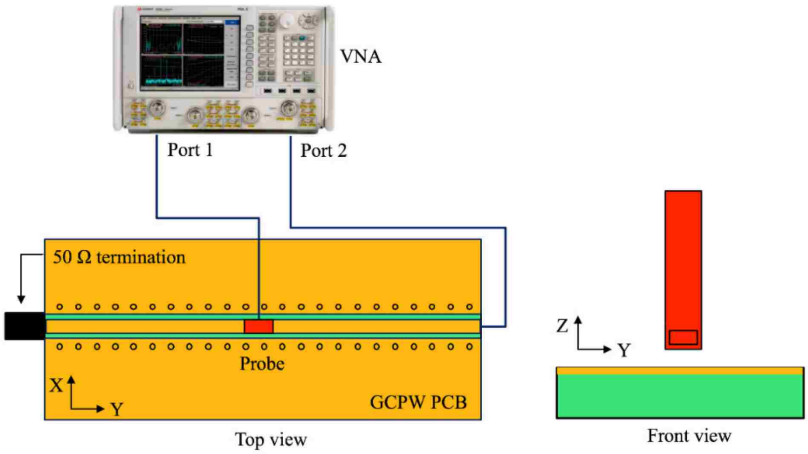


Figure 1. Measurement set-up for probe factor calculations using a GCPW PCB.

One of the applications of these calibration structures is to quantify the undesired field component suppression for a nearfield probe. For instance, for an H-field probe placed above the GCPW calibration structure shown in Figure 1, the desired (TEM) component is

the H_x field component and the H_y is the undesired (non-TEM) field component. The y-component is along the wave propagation direction and, hence, in a quasi-TEM wave geometry, the component is expected to be much smaller than the desired component. In such applications, if the fields generated by the calibration structure itself have stronger non-TEM or the undesired fields, then it makes the calibration structure unsuitable for probe undesirable field component suppression quantification measurements.

At first glance, one may believe that the field structure over a GCPW or microstrip is not a function of frequency as the structure supports a quasi-TEM wave. This paper discusses the effect of the inhomogeneous medium in GCPW PCB. At first, it was assumed that a GCPW transmission line would have TEM-dominated fields above the PCB for the desired frequency range. From the simulated near-field data, it was found that that this assumption does not hold true. A difference in the maximum field strength, asymmetric field variation on the two sides of the trace, and magnitude variation along the length of the trace were observed. One of the core findings is that the variation of the desired component (about 3–8 dB) along the length of the trace at about 30 GHz and higher frequencies suggests that the during the calibration process, the position of the near-field scanning probe becomes important. If the probe is not placed at the center of the length of the GCPW where the simulated field is determined, then the fields measured by the probe will not lead to an offset of 3–8 dB in the field strength calculation based on the probe factor (1) calculation using the simulation and the measurement. The variation in the desired component along the length of the trace can be reduced by reducing the PCB thickness [14], thus, by keeping the cross-sectional waveguide geometry electrically small for the highest frequency of interest.

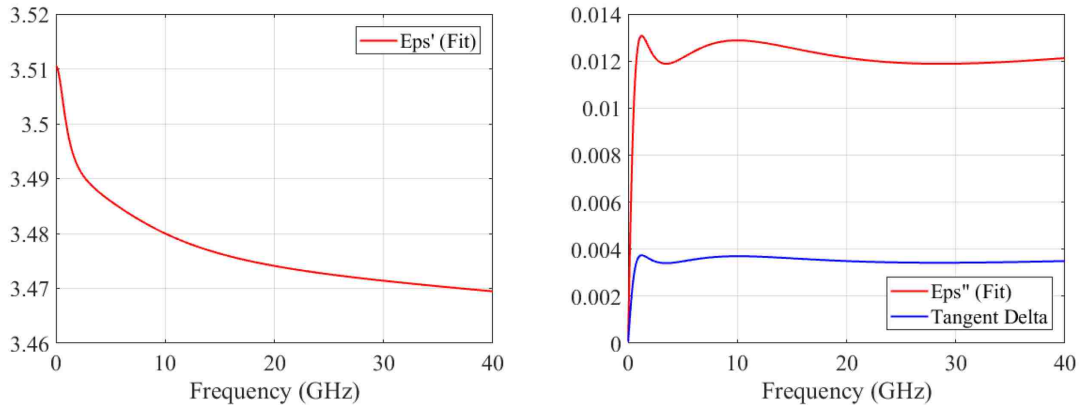
The GCPW PCB was simulated using CST MWS [15] and the effect of the inhomogeneous medium on the near-field x-component (perpendicular to the trace) of the E- and H-fields is reported. With the increase in frequency, the height above the GCPW PCB, which can be utilized for probe factor measurements, is restricted. The investigation in this paper was performed up to 40 GHz on an RO4350 dielectric-based GCPW PCB. To confirm the effect of the inhomogeneous medium, a GCPW PCB with air as the dielectric material was simulated and compared to the RO4350 dielectric material. Here, the comparisons are quantified using the ratio of the desired (TEM) and the undesired field (non-TEM) component at a particular frequency and at a fixed scanning height above the trace surface.

2. GCPW SIMULATION MODEL

The two simulation models were used to determine if the unwanted field variations were caused by the launch section (connector-PCB transition) or a result of the non-TEM field due to the inhomogeneous dielectric medium interface. First, a GCPW with RO4350 low-loss dielectric structure was investigated. Then, an only-air dielectric GCPW was simulated to observe the difference between the air–air interface and the RO4350–air interface in the RO4350-based GCPW PCB.

The 0.762-mm RO4350 dielectric material-based GCPW PCB available from Southwest Microwave [16] was used as a typical low-loss high-frequency board. These boards are typically used for signal integrity applications, which was not the focus of this study. In this application, it was used as an intentional near-field source for probe factor

calibration applications. For reducing the simulation time, the stitching ground vias are modeled as rectangular blocks in the CST MWS model. It is important to note that the frequency dependence of the RO4350 dielectric material was considered in the simulation model and is illustrated in Figure 2. The time domain solver based on finite integration technique was used for solving the model with a Gaussian excitation source applied at the waveguide ports placed at the GCPW connectors. The model has around 6 million hexahedral mesh cells and the time domain accuracy is increased to –60 dB to achieve better convergence in the simulated results.



(a) (b)

Figure 2. Frequency dependence of the RO4350 dielectric material properties used in the simulation model. For the electric dispersion, the Nth order model with $N = 3$ (constant tangent delta fit) is used in the simulation. (a) Eps′ or the dielectric constant. (b) Eps" and the tangent delta.

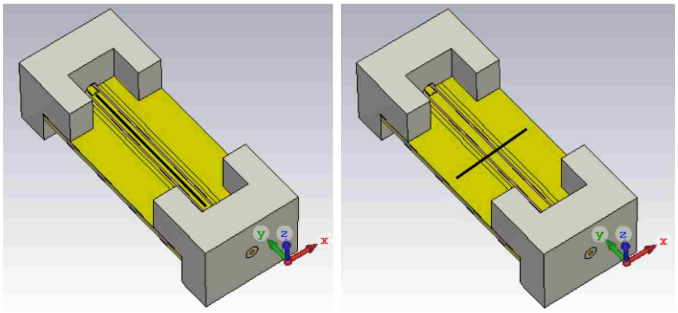
Another simulation model was designed for the same structure, but instead of the RO4350 dielectric, the PCB was designed using air dielectric. To maintain similarity to the RO4350 PCB, only the air dielectric substrate was changed to obtain the nominal 50 Ω

trace impedance in the simulation model. The substrate thickness was reduced from 0.762 mm to about 0.249 mm for air as the dielectric. Table 1 provides the design parameters of the two GCPW geometries considered for the desired near-field component investigation.

Table 1. Design parameters of the two GCPW models investigated using CST MWS simulation.

Design	PCB Length	PCB Width	Trace width	Top ground gap	Substrate	Substrate thickness
Rogers 4350-based GCPW	25.4 mm	12.7 mm	1.143 mm	0.241 mm	RO4350, $\varepsilon_r(f) = 3.48$	0.762 mm
Air dielectric GCPW	25.4 mm	12.7 mm	1.143 mm	0.241 mm	Air, $\varepsilon_r = 1$	0.249 mm

The E- and H-field monitors were defined for a volume in the CST models, and the field magnitude was determined for the frequency range from 0.1 to 40 GHz. The simulated results are analyzed by plotting the field magnitude at the center of the PCB width along the length of the PCB as shown in Figure 3(a). In addition, the near-fields are analyzed at the center of the PCB length, along the width of the PCB, respectively, as shown in Figure 3(b). The trace surface is considered as 0 mm reference height. The desired x-component is plotted over the solid line as shown in the Figure 3(a) and (b). The analysis was performed at different heights above the trace surface, such as 1, 2 mm above the trace, etc. It should be noted that, in Figure 3, the evaluation line is shown for 1 mm above the trace surface.



(a) (b)

Figure 3. Simulation model of the RO4350 dielectric-based GPCW PCB with a connector model. (a) Solid line represents the field plotted at the center of the width of the PCB but along the length of the PCB or the trace (y-direction). (b) Solid line represents the field plotted at the center of the PCB length but along the width of the PCB or the trace (x-direction).

3. SIMULATION RESULTS

The GCPW structure implemented in an RO4350 PCB dielectric and air on the trace top surface is expected to have quasi-TEM mode because the wave propagation velocity in dielectric and air is different, which leads to a quasi-TEM mode. The GCPW structure with air dielectric is expected to have the TEM mode because of the homogeneous medium for the wave propagation.

The y-direction is along the length of the trace, the x-direction is perpendicular to the trace. The x-component of the E- and H-fields is the desired field component for the probe factor calibration calculation. In this section, the field components are shown at different heights above the trace, frequency, along the width of the trace, and along the length of the trace. The main finding here is that as frequency increases, the desired E_x or the H_x field component has ripples or variations along the length of the trace, for example,

the 0.762-mm thick RO4350 GCPW. On the contrary, the PCB geometry with 0.249-mm thick air dielectric GCPW observes much less variation along the length of the trace. The variation along the length of the trace can be reduced by making the PCB thinner, thus, keeping the cross-sectional waveguide geometry electrically small for the highest frequency of interest.

The simulation results for the RO4350 dielectric and the air dielectric are compared for the desired H_x and the E_x component. The magnitude of the two components is plotted along the length of the PCB (y-direction) and along the width (x-direction) of the PCB at y equal to 0 mm (center position of the trace length). In the following plots, the effect of the frequency at a fixed height of z = 1 mm is observed. Later the effect of height will be considered. The desired H_x component at a height of z = 1 mm above the GCPW PCB for the RO4350 dielectric-based model is plotted in Figures 4 and 5.

Figure 5 shows about a 12 dB variation at the center of the trace width (5 mm) at 40 GHz for the H_x component at a height of z = 1 mm above the GCPW PCB. The desired H_x component at a height of z = 1 mm above the GCPW PCB for the air dielectric-based model is plotted in Figures 6 and 7.

Referencing the probe factor calibration application, it is observed that the magnitude component in Figure 4 has a large variation from 0.1 to 40 GHz when compared to the plots in Figure 6. The magnitude difference is within 1–2 dB up to 20 GHz, but there are about 14 dB variations at 40 GHz along the length of the PCB in Figure 4. Compared to the simulation results obtained using the air dielectric model, the magnitude variation along the length of the PCB is within 4 dB for the frequencies from 0.1 to 40 GHz in Figure 6. The variation in amplitude for the air dielectric is much less than the RO4350

dielectric, which suggests that the probe height over the PCB is important while performing the probe factor measurements using an RO4350 dielectric material GCPW. The peak magnitude value for the air dielectric simulation model varies only by 1.5 dB, as shown in Figure 7, confirming that this is a TEM wave. For the commercially available GCPW PCB's such as the RO4350 dielectric-based model, a variation of 12 dB is observed as shown in Figure 5.

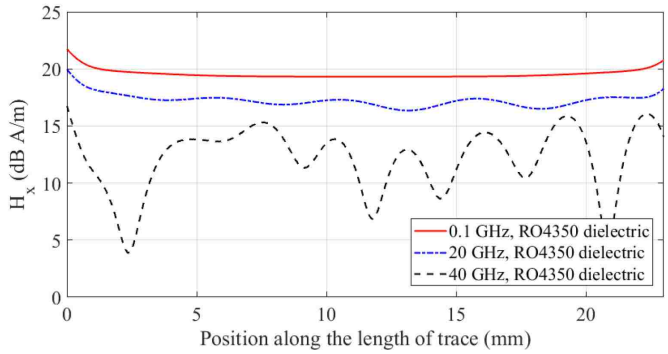


Figure 4. Desired H_x component over the RO4350 GCPW trace along the length (y-direction, parallel to the trace) of the PCB at 0.1, 20, and 40 GHz. Note the strong reduction of the field for 40 GHz compared to Figure 6.

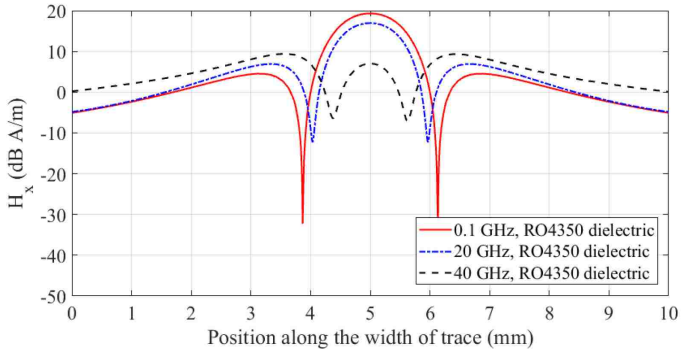


Figure 5. Desired H_x component over the RO4350 GCPW trace along the width (x-direction) of the PCB at 0.1, 20, and 40 GHz. The curve length of 5 mm represents the center position of the PCB trace width. Note the strong reduction of the field for 40 GHz compared to Figure 7.

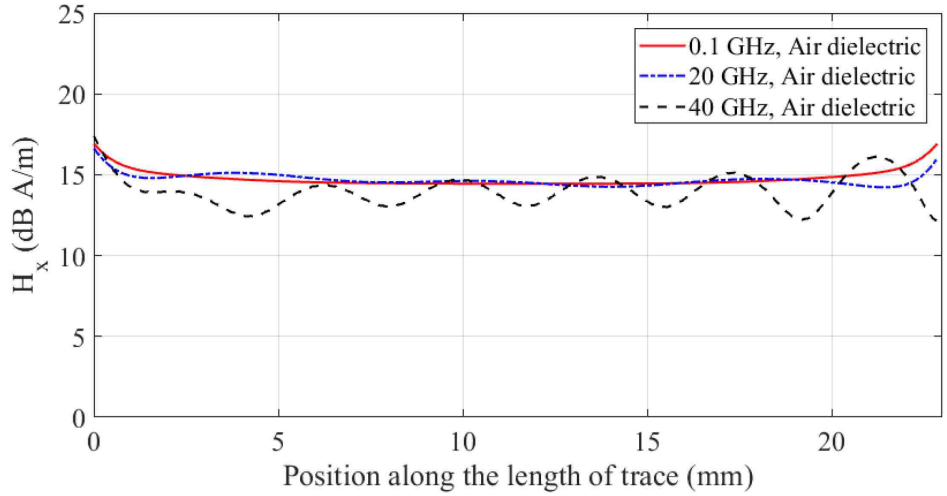


Figure 6. Desired H_x component over the air GCPW trace along the length (y-direction) of the PCB at 0.1, 20, and 40 GHz. The y-axis scale is kept to the same range as in Figure 4 for better comparison.

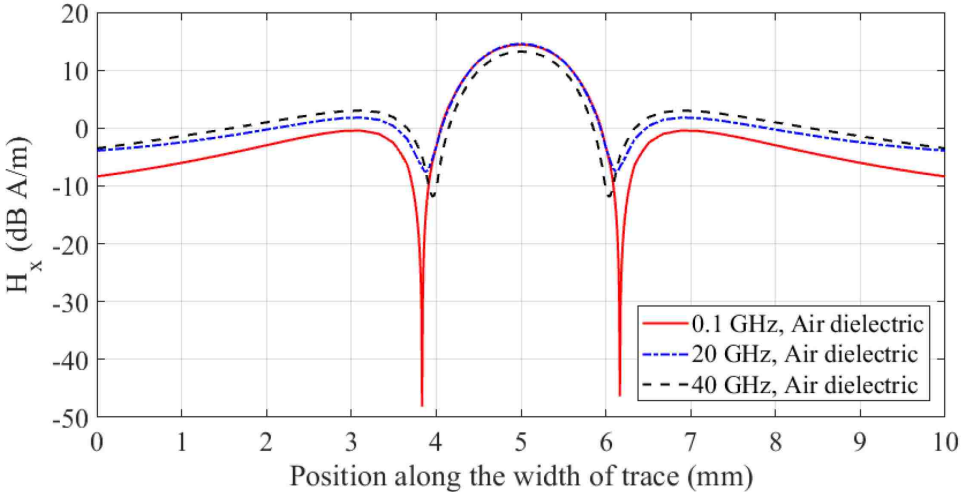


Figure 7. Desired H_x component over the air GCPW trace along the width (x-direction) of the PCB at 0.1, 20, and 40 GHz. The curve length at 5 mm represents the center position of the PCB trace width. Note that the field is only a weak function of frequency verifying the TEM behavior of the fields.

The near-field desired E_x component is analyzed similarly along the length and the width of the PCB. The E_x component at a height of z = 1 mm above the GCPW PCB for

the RO4350 dielectric-based model is plotted in Figures 8 and 9. In addition, the desired E_x components at a height of z = 1 mm above the GCPW PCB for the air dielectric-based model are plotted in Figures 10 and 11.

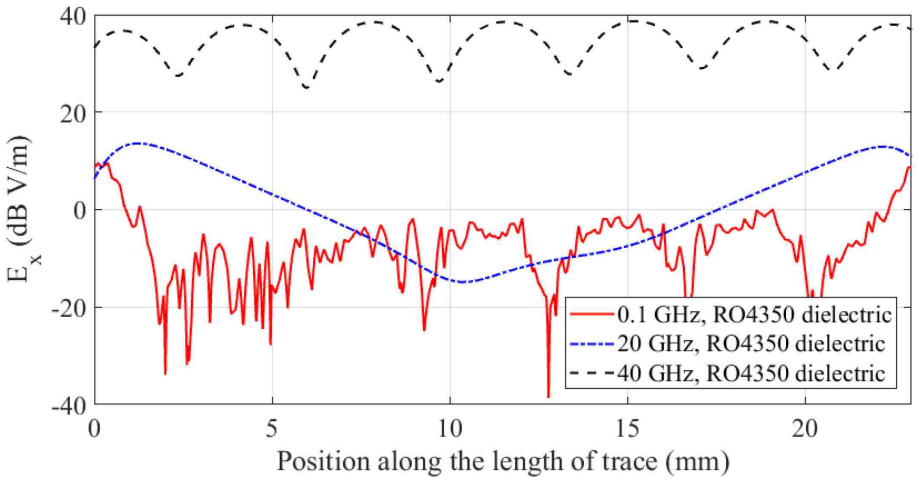


Figure 8. Desired E_x component over the GCPW trace along the length (y-direction) of the PCB at 0.1, 20, and 40 GHz but exactly in the middle where the component has a null. Note the strong values for 40 GHz compared to Figure 10.

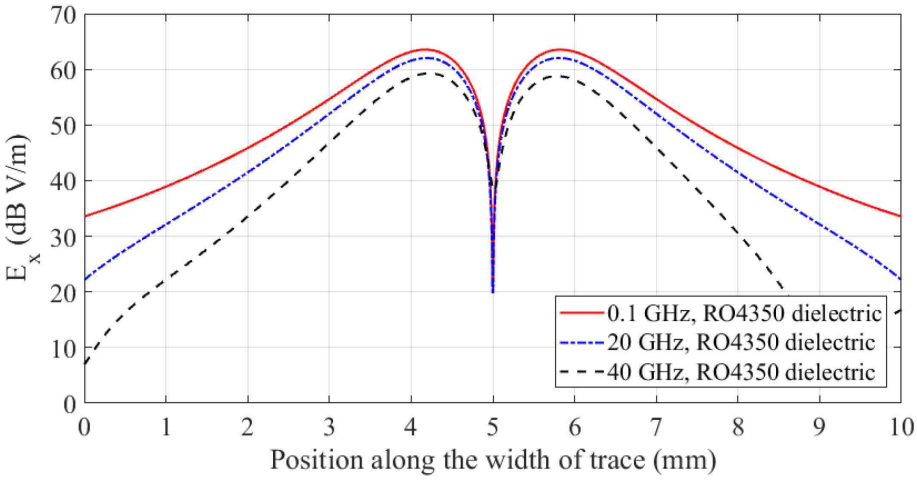


Figure 9. Desired E_x component over the GCPW trace along the width (x-direction) of the PCB at 0.1, 20, and 40 GHz. The curve length of 5 mm represents the center position of the PCB trace width.

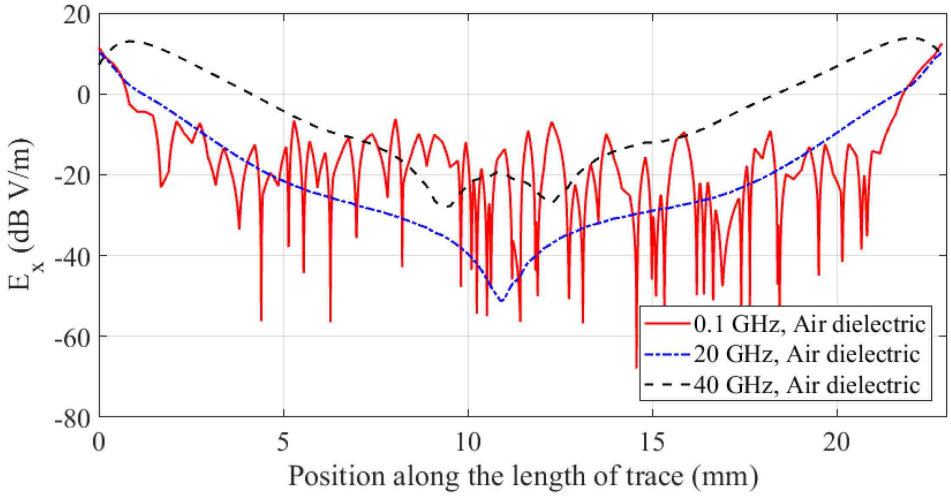


Figure 10. E_x component over the GCPW trace along the length (y-direction) of the PCB at 0.1, 20, and 40 GHz. Note that the unwanted longitudinal component is mainly excited at the connector transition.

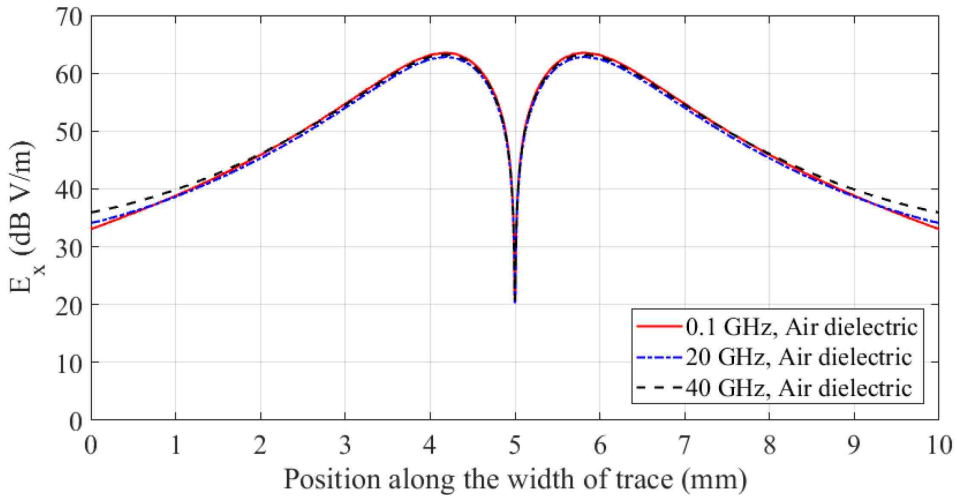


Figure 11. E_x component over the GCPW trace along the width (x-direction) of the PCB at 0.1, 20, and 40 GHz. The curve length of 5 mm represents the center position of the PCB trace width. Note that the frequency independence again is an indication for the dominance of the TEM mode.

Figure 10 shows the desired field at the center of the trace where the component has a null for the air GCPW; the field strength variation is about –10 to –40 dB. The desired

E_x component has the strongest magnitude around the edges of the PCB trace width, which is about 63 dB in Figure 11. Hence, the null field strength is much less than the peak magnitude field strength and the noise floor looking waveforms in Figures 8 and 10 can be considered acceptable based on the simulated near-field waveforms.

4. TESTING THE REJECTION RATIO OF A NEAR-FIELD PROBE

Every H-field probe is sensitive to E-field and vice versa, also an H_x probe cannot perfectly reject other magnetic field components. A typical way to determine the rejection ratio of an H_x probe would be to place the probe at first in the middle of the trace and rotate it to the desired field component (H_x) to obtain a reference reading. Then, the probe is rotated 90°, assuming that the desired component is perfectly rejected and that no longitudinal component exists (H_y), as one would expect in a TEM wave. In this case, the remaining signal picked up by the probe would only be caused by the electric field coupling.

This numerical simulation allows us to test the underlying assumption of not having a longitudinal H_y component. It is known that the magnetic field probes are sensitive to the E-field especially if they are offset to the side of the trace and rotated into an orientation in which they reject the TEM field. However, the conclusion could be wrong, if the non-TEM field is stronger on the side of the trace. In this case, the probe would couple to the non-TEM field, but the user may misinterpret this as a coupling to the E-field. To investigate this, the non-TEM fields were also plotted to the side of the trace and compared to the desired field component. It is important to note that the numerical simulation allows for

identifying the desired quasi-TEM or the TEM components (H_x , H_z , E_x , and E_z) and the non-TEM components (H_y and E_y). The following plots give an insight into the field rejection ratio, which is defined as follows:

$$H - Field\ Rejection\ Ratio = \frac{H_x(f, h_{eff})}{H_y(f, h_{eff})} \tag{2}$$

$$E - Field\ Rejection\ Ratio = \frac{E_x(f, h_{eff})}{E_y(f, h_{eff})} \tag{3}$$

In this rectangular co-ordinate system, the x- and z-components are the desired TEM field components and the y-component is the undesired non-TEM field component. The field rejection ratio is defined as the field strength of the desired component at an expected maximum location divided by the maximum field strength of the undesired field component. For instance, the expected maximum H_x field will be at the center of the trace width, and at the edge of the trace width for the E_x field component as shown in Figures 7 and 11, respectively. Using this definition, the field rejection ratios are determined and illustrated in Figures 12 to 15.

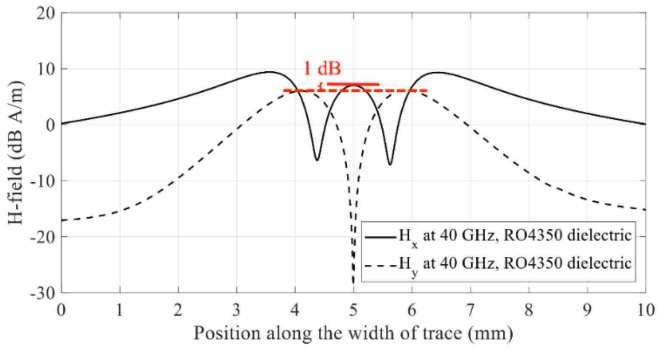


Figure 12. Side scan comparison of the desired H_x component (solid line) and the non-TEM H_y component (dashed line) over the RO4350 GCPW trace along the width (x-direction) of the PCB at z = 1 mm at 40 GHz. Note that at 1 mm the maximum of the non-TEM component is only 1 dB below the maximum of the desired component.

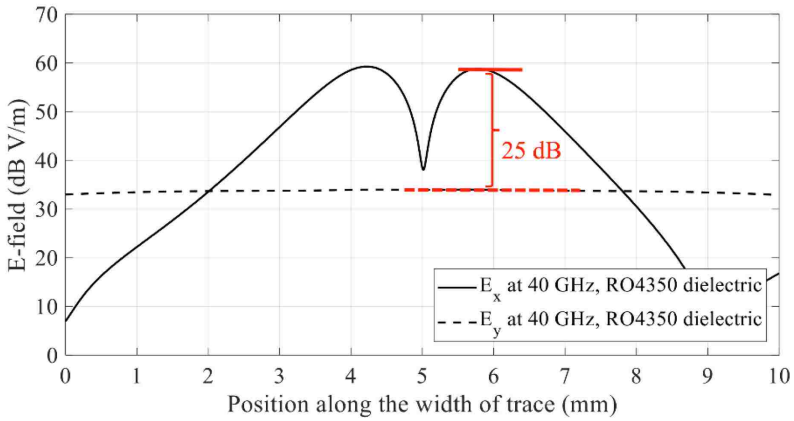


Figure 13. Side scan comparison of desired E_x component (solid line) and the E_y component (dashed line) over the RO4350 GCPW trace along the width (x-direction) of the PCB at z = 1 mm at 40 GHz.

4.1. COMPARISON BETWEEN THE TWO GCPW GENERATED FIELDS AT A FIXED HEIGHT AND FREQUENCY

In Figures 12 and 13, the rejection ratio of the RO4350 dielectric-based GCPW generated fields is compared. Figure 12 shows the plot of the quasi-TEM H_x and the non-TEM H_y along the width of the trace.

On comparing Figures 12 and 14, it is observed that the non-TEM component at 40 GHz in the RO4350 dielectric GCPW is only 1 dB weaker than the desired H_x field. This is a strong indication of the inhomogeneous medium effect on the near-field above the PCB geometry. In the case of the air dielectric GCPW as shown in Figure 14, the non-TEM component is 30 dB weaker than the desired field component. This quantification of the rejection ratio of the fields generated by the characterization PCB geometry is an important factor in determining the rejection ratio of a near-field scanning probe during probe characterization or evaluation measurements. Similarly, the behavior is seen in the E-field plots in Figures 13 and 15. The air-dielectric GCPW has effectively 35 dB weaker

non-TEM field component, as compared to the 25 dB suppression in the RO4350 dielectric GCPW at z = 1 mm at the highest frequency of interest.

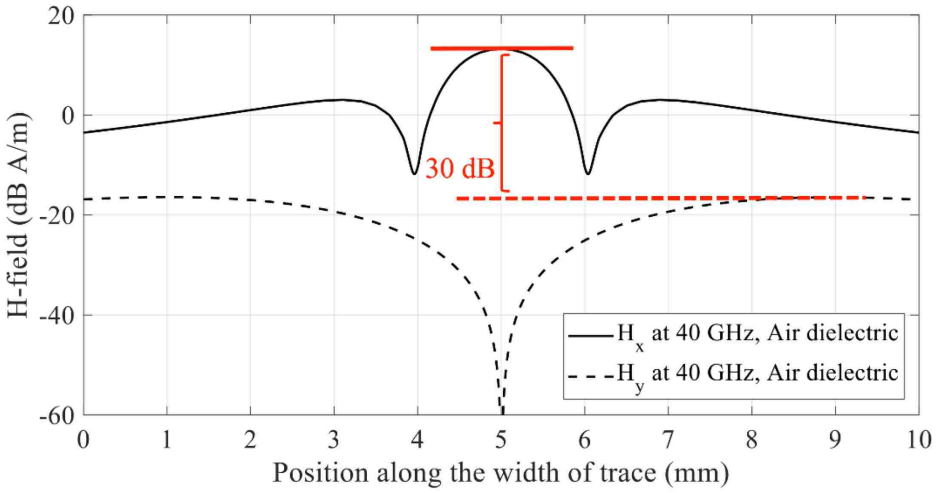


Figure 14. Side scan comparison of the desired H_x component (solid line) and the non-TEM H_y component (dashed line) over the air GCPW trace along the width (x-direction) of the PCB at z = 1 mm at 40 GHz. Note that at 1 mm the maximum of the non-TEM component is 30 dB below the maximum of the desired component.

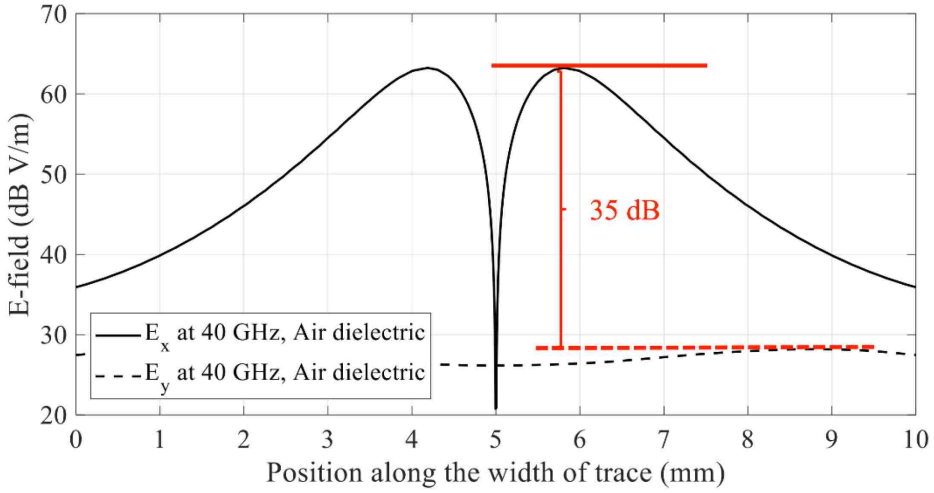


Figure 15. Side scan comparison of desired E_x component (solid line) and the E_y component (dashed line) over the air GCPW trace along the width (x-direction) of the PCB at z = 1 mm at 40 GHz. Note that at 1 mm the maximum of the non-TEM component is 35 dB below the maximum of the desired component.

4.2. COMPARISON BETWEEN THE TWO GCPW GENERATED FIELDS AT A FIXED FREQUENCY AND DIFFERENT HEIGHTS

In Figures 16 and 17, the desired H_x and the undesired (non-TEM) H_y components are plotted along the width of the trace at scanning heights of 1 and 2 mm at 40 GHz frequency. Figure 16 shows the results for the RO4350 GCPW trace, where it is seen that the H_y component changes with the scanning height. However, it is observed in Figure 17 for the air GCPW that the H_y (non-TEM) component does not increase in magnitude when the scanning height is changed from 1 to 2 mm. A similar effect is observed for the E-field in Figures 18 and 19; however, a small increase is observed in the E_y field component. The increase in the undesired y-component is shown by the red dashed lines in Figures 16–19.

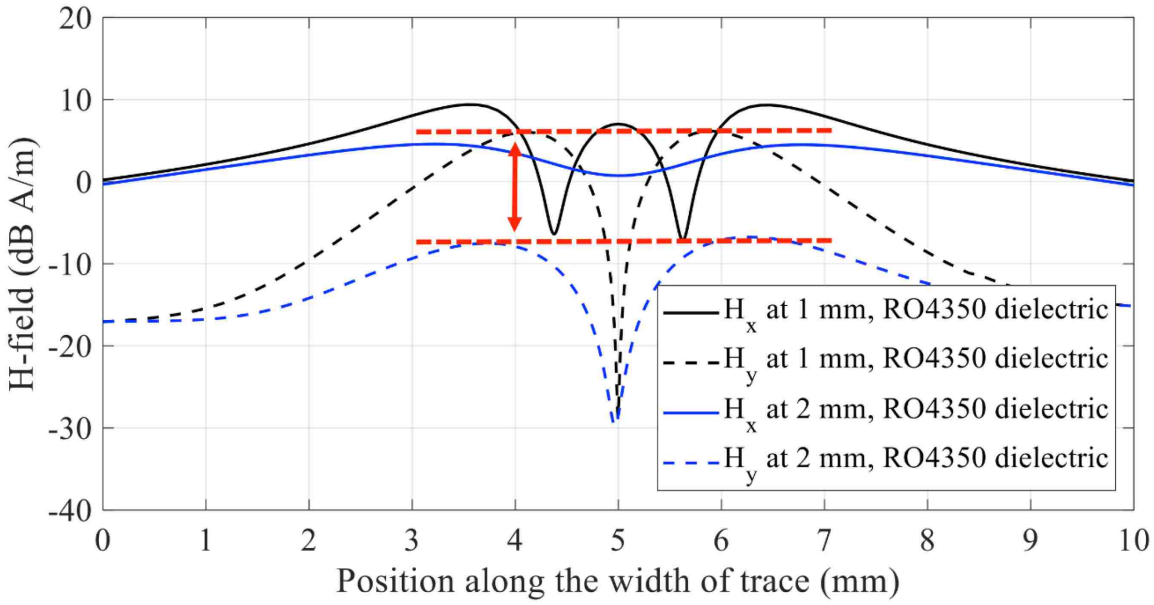


Figure 16. Side scan comparison of the desired H_x component (solid line) and the H_y component (dashed line) over the RO4350 GCPW trace along the width (x-direction) of the PCB at z = 1 and 2 mm at 40 GHz.

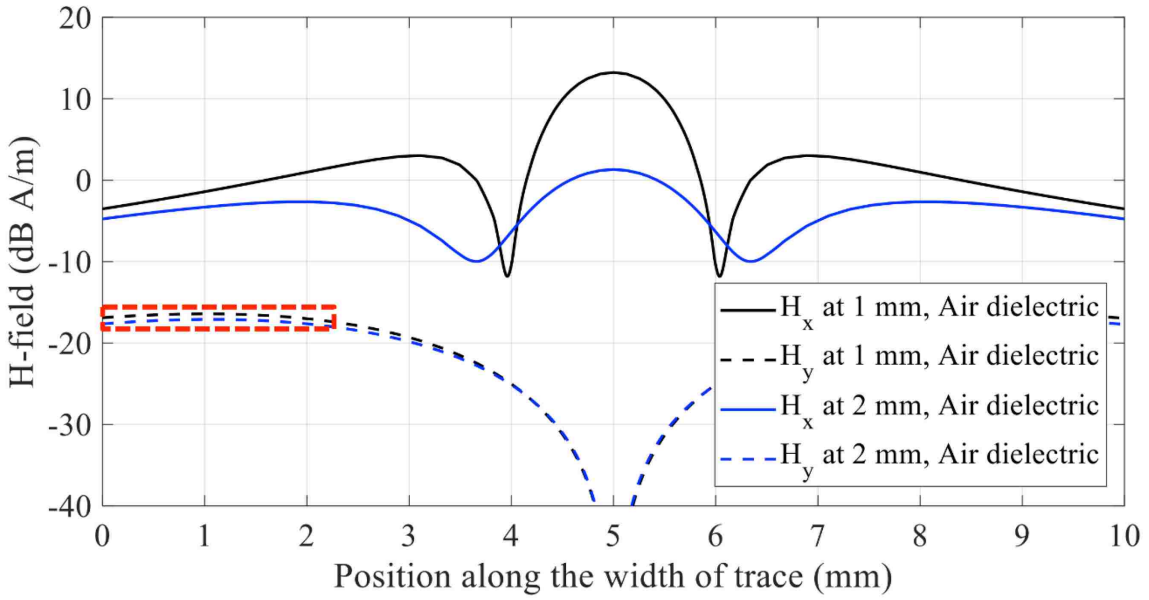


Figure 17. Side scan comparison of desired H_x component (solid line) and the H_y component (dashed line) over the air GCPW trace along the width (x-direction) of the PCB at z = 1 and 2 mm at 40 GHz.

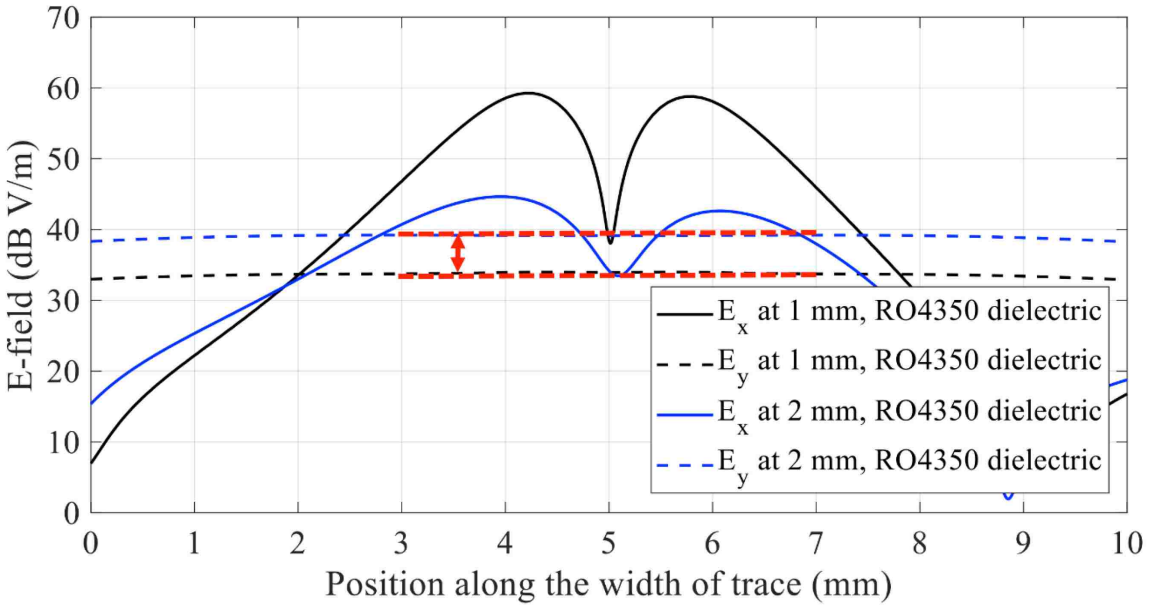


Figure 18. Side scan comparison of desired E_x component (solid line) and the undesired E_y component (dashed line) over the RO4350 GCPW trace along the width (x-direction) of the PCB at z = 1 and 2 mm at 40 GHz.

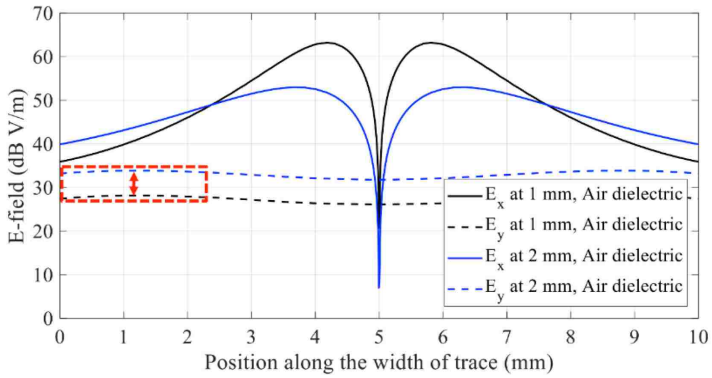


Figure 19. Side scan comparison of desired E_x component (solid line) and the undesired E_y component (dashed line) over the air GCPW trace along the width (x-direction) of the PCB at z = 1 and 2 mm at 40 GHz.

Table 2 lists the rejection ratios calculated using (2) and (3) for various frequencies. The table shows the trend that as the frequency of interest increases, the undesired (non-TEM) H_y field component magnitude becomes comparable to the desired H_x field strength. Referencing the near-field scanning applications at higher frequencies, the inhomogeneous dielectric-based GCPW is not suitable for generating the desired quasi-TEM waves. For instance, at 40 GHz frequency, the rejection ratio for the H-field (H_x/H_y) when using the RO4350 GCPW is only 1 dB. However, an air-dielectric GCPW provides about 30 dB non-TEM (H_y) component suppression.

5. DISCUSSION AND CONCLUSION

The CST MWS simulation was performed on the GCPW PCB designed using the RO4350 dielectric. At higher frequencies, stronger non-TEM field components were observed, such that the suppression between the quasi-TEM and the non-TEM is only about a few dB as shown in Table 2 for the 40 GHz frequency for the H-field.

Table 2. Field rejection ratio for various frequencies for RO4350 and air-dielectric GCPW at 1 mm above the trace.

Frequency	For RO4350 GCPW = H_x/H_y	For Air GCPW = H_x/H_y	For RO4350 GCPW = E_x/E_y	For Air GCPW = E_x/E_y
0.1 GHz	57 dB	54 dB	69 dB	62 dB
10 GHz	18 dB	44 dB	50 dB	43 dB
20 GHz	13 dB	49 dB	37 dB	38 dB
30 GHz	10 dB	42 dB	49 dB	45 dB
40 GHz	1 dB	30 dB	25 dB	35 dB

The desired x-component of the E- and H-fields was simulated over the RO4350 GCPW trace structure. The x-component of the E- or H-field is plotted on a line at a fixed height, along the length of the trace at 0.1, 20, and 40 GHz. In this RO4350 GCPW structure, the air and RO4350 dielectric are the two media through which the waves propagate. To verify the effect of the inhomogeneous medium on the field above the PCB, another set of simulations were performed by replacing the RO4350 dielectric with air as a dielectric medium.

These simulations revealed that while performing the nearfield probe calibration or calculating the probe factor of a nearfield probe, the effect of the inhomogeneous media needs to be taken into account to determine the effective height and the frequency range supported by the GCPW PCB; Figure 12 illustrates this effect. In addition, for the near-field probe rejection ratio calculation using (2) and (3), the near-field generating PCB must be well evaluated for the presence of the non-TEM field components at the desired height; for example, 1 mm above the surface. It is important that the rejection ratio of the near-

field generating source PCB should be more than the value obtained for a near-field scanning probe during its probe undesired field suppression measurements. This criterion ensures that, for example, an H-field probe's unwanted measured component was the E-field coupling and not the non-TEM component generated by the calibration PCB.

The simulation results reveal that using an air-dielectric GCPW geometry provides better field rejection ratio than the RO4350 dielectric-based GCPW. The field rejection values for the E- and H-field are provided in Table 2. An air dielectric structure generates the desired TEM fields, which are important for the near-field probe factor calibration measurement application.

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SECTION

2. SUMMARY AND CONCLUSIONS

In the first paper of this dissertation, the purpose of this study was to analyze secondary discharge events acquired with various measurement setups, in order to identify waveform parameters for software-assisted algorithms and to verify the occurrence and detection of secondary ESD events using current clamp-acquired waveforms. Using a non-intrusive measurement method, secondary ESD events generated due to contact mode primary ESD events can be detected by monitoring the discharge current at the ESD generator tip.

In the second paper, sparkless discharges to display electronic products are investigated. The statistical behavior of the induced currents is determined for different parameters, such as a change in display cover glass thickness, ITO layer equivalent resistance, sensor spacing to the ground plane, ESD generator air discharge polarity, and test voltage. In addition, a full-wave simulation model was developed to reproduce the worst case displacement current flowing through the glass into the display's inner electronic structures.

In the third paper, CST MWS simulation was performed on the GCPW PCB that was designed using the RO4350 dielectric. At higher frequencies, stronger non-TEM field components were observed, such that the suppression between the quasi-TEM and the non-TEM is only about a few dB for the 40 GHz frequency for the H-field. These simulations revealed that while performing the nearfield probe calibration or calculating the probe

factor of a nearfield probe, the effect of the inhomogeneous media needs to be taken into account to determine the effective height and the frequency range supported by the GCPW PCB. In addition, for the near-field probe rejection ratio calculation, the near-field generating PCB must be well evaluated for the presence of non-TEM field components at the desired height, for example, 1 mm above the surface. It is important that the rejection ratio of the near-field generating source PCB should be more than the value obtained for a near-field scanning probe. This criterion ensures that, an H-field probe's unwanted measured component was the E-field coupling and not the non-TEM component generated by the calibration PCB. The simulation results reveal that using an air-dielectric GCPW geometry provides better field rejection ratio than the RO4350 dielectric-based GCPW.

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