Fall 2019

Modeling strategies for estimating and suppressing electromagnetic interference and improving power integrity

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MODELING STRATEGIES FOR ESTIMATING AND SUPPRESSING ELECTROMAGNETIC INTERFERENCE AND IMPROVING POWER INTEGRITY

by

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A DISSERTATION

Presented to the Faculty of the Graduate School of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

DOCTOR OF PHILOSOPHY

in

ELECTRICAL ENGINEERING

2019

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PUBLICATION DISSERTATION OPTION

This dissertation consists of the following three articles, formatted in the style used by the Missouri University of Science and Technology:

Paper I: Pages 3-30 “Accurate Inductance Models of Mounted 2-Terminal Decoupling Capacitors.” are intended for submission to have been submitted to IEEE Transactions on Electromagnetic Compatibility Journal.

Paper II: Pages 31-57 “Simple Circuit Models of the Inductance of 8-Terminal Decoupling Capacitors.” are intended for submission to IEEE Transactions on Electromagnetic Compatibility Journal.

Paper III: Pages 58-84 “Determining Equivalent Material Properties for Shielding Effectiveness Based on a Low Frequency Dual-Loop Method.” are intended for submission to IEEE Transactions on Electromagnetic Compatibility Journal.

Paper IV: Pages 85-97 “Developing an Equivalent System-level Common-mode Current Model Based on Component Behavior.” are intended for submission to IEEE Transactions on Electromagnetic Compatibility Journal.

ABSTRACT

Decoupling capacitors are used to suppress high-frequency noise in power distribution networks. The inductance associated with a mounted decoupling capacitor can vary by 26% depending on characteristics of the printed circuit board. Here, simple and accurate inductance models of 2- and 8-terminal capacitors including connections to the power and return plane are developed. Circuit models of the capacitors and layout are created using the partial equivalent element circuit method which provide options for circuit-level simulations as well as analytic estimation of inductance. The circuit solution matches results from the full-wave simulation model within 9% for the 8-terminal capacitor and within 15% the for the 2-terminal capacitor.

System-level radiated emissions from a harness are primarily caused by common-mode currents on the harness. An approach is needed to predict system-level emissions early in the design process based on a relatively simple component-level measurements. A prediction technique estimates equivalent common-mode source voltages and impedances based on component-level measurements, which can be used to predict the common-mode current on a harness of arbitrary length or characteristic impedance.

Shielding the victim or isolating the noise source can suppress electromagnetic interference. Numerical and analytical methods can accurately estimate shielding effectiveness if the conductivity and permeability of the shielding material is known. A measurement process for obtaining equivalent material properties at low frequencies (from than 0.01-1 MHz) is proposed. Comparison of measured and simulated shielding estimated using material properties found with this process agree within 1.6 dB.

ACKNOWLEDGMENTS

I would like to express my gratitude to have such an outstanding professor and excellent advisor like Dr. Daryl G. Beetner. I would like to express my appreciation to him for his guidance, patience, support, and assistance throughout my projects. Special thanks to Dr. James Drewniak, Dr. Albert Ruehli, and Dr. Chulsoon Hwang for their insightful technical discussions and for guiding me in the completion of my dissertation. Many thanks to Dr. Victor Khilkevich for interesting classes that helped greatly with my research. I am also grateful to Dr. Daniel Stutts for his time and input during review of this document. I would like to thank Phil Berger for his help and valuable advice along the way I was pursuing my degree.

It is my pleasure to thank all the former and current members of the EMC Laboratory for their teamwork and friendship. Special thanks to my family members and friends who were a great support.

I am honored to dedicate this work to my parents, Nanuli Kharshiladze and Merab Makharashvili for their love, trust, and continuous support.

TABLE OF CONTENTS

Page

LIST OF ILLUSTRATIONS

PAPER I Page

PAPER II

PAPER IV

LIST OF TABLES

1. INTRODUCTION

Decoupling capacitors are used to reduce voltage ripples in power supply circuit while keeping the power distribution network's (PDN) impedance sufficiently low in packages and printed circuit board (PCB) design. The voltage ripples are caused by the simultaneous IC switching and could be propagated through power and reference planes. A target impedance of a PDN system has been developed to supposedly ensure a voltage fluctuation that is smaller than the allowable limit. The current path of the PDN must maintain impedances in the milliohms range from dc to several hundred megahertz for high performance designs. A contributor to the PDN impedance is the decoupling capacitors series inductance. The equivalent series inductance values provided by the manufacturer are based on measurements performed on a specific test fixture. Hence, the ESL values depend on the measurement fixture. Unfortunately, it is not possible to calculate the correct inductance without considering the layout impact on the mounted capacitor's inductance. The first paper in this dissertation proposes a method to estimate the overall inductance associated with a power bus 2-terminal decoupling capacitor and its connections to the power and return planes by partitioning the inductance into a portion associated with the connections to the power and return planes and a portion associated with the mounted capacitor. Partitioning allows the designer to make a single estimate of inductance for the capacitor and mounting pads and to pair this estimate with an estimate of inductance for the connecting traces and vias made for a variety of trace configurations.

An inductance model of the 8-terminal capacitor with its connections to the power and the return plane is developed in the second paper. A simplified circuit model of the capacitor is developed using the partial equivalent element circuit (PEEC) approach. The circuit models are such that an analytical evaluation of the inductance can be used the capacitor couplings and the layout circuit can be used to study the impact of changes in geometry on current path inductance.

The third paper is about investigating shielding properties of materials to protect victim device from aggressor. Conductivity and permeability are the properties of the materials contributing to their electromagnetic shielding performance. In the paper, material properties are determined for metals and magnetic material as well as for composed layers of materials. Equivalent material properties are further used to evaluate shielding effectiveness of the materials based on the military standard requirements.

The fourth paper of this dissertations addresses the electromagnetic emission problem by identifying the source. The system-level emissions from the vehicle does not correlate with component-level performance. Emissions are usually contributed by the common-mode current in the harness. Approach is proposed to predict system-level common-mode currents based on a relatively simple component-level common-mode current measurements by identifying common-mode sources. Numerical optimization is used to solve nonlinear equations derived from the multi-conductor transmission line theory. Solution of the optimization algorithm is equivalent common-mode impedances and voltages best fitted to measured currents. Common-mode sources are used to predict common-mode current on an arbitrary length or characteristics of the harness.

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PAPER

I. ACCURATE INDUCTANCE MODELS OF MOUNTED 2-TERMINAL DECOUPLING CAPACITORS

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ABSTRACT

The inductance associated with a decoupling capacitor is typically represented as a constant equivalent series inductance (ESL). In reality, this inductance depends on how the capacitor is mounted and on coupling to nearby structures, including the traces and vias connecting the capacitor to the power and return planes. Determining the effective inductance of every decoupling capacitor layout in a design with commercial electromagnetic solvers, however, is an overwhelming task. Here, a method is proposed to estimate the overall inductance associated with a power bus decoupling capacitor and its connections to the power and return planes by partitioning the inductance into a portion associated with the connections to the power and return planes and a portion associated with the mounted capacitor. The equivalent inductance associated with only the capacitor and pads must then only be estimated for a few configurations. The accuracy of the partitioning approach is demonstrated in simulation and experimentally using two common decoupling capacitor layouts. The partitioning approach estimates the

overall inductance associated with the decoupling capacitor and its connections to the power bus within 16% if the distance between the capacitor and reference plane (dielectric thickness) is not more than 6 mils. A simplified partial element equivalent circuit model was further developed which allows a user to estimate the inductance associated with the capacitor using closed-form expressions. This simplified model estimates the capacitor's inductance within 14% of values found using a commercial electromagnetic tool. These models should allow engineers to better estimate the power bus impedance and the impact of design changes than is possible using manufacturer estimates of ESL.

1. INTRODUCTION

Decoupling capacitors are a major contributor to the power delivery network (PDN) impedance [1], [2], [3]. They are usually represented in simulations as an equivalent series capacitance (ESC), inductance (ESL), and resistance (ESR) [4], [5], as a distributed circuit [6], [7], or as an S-parameter network block [8], [9]. These representations, however, often do not accurately represent the parasitic interactions between the capacitor and surrounding structures, including its mounting pads, the reference plane, and the traces and vias connecting the capacitor to the power buss. ESR and ESC values given by the manufacturer are typically correct within the specified tolerance [4], [10], but the ESL of the mounted decoupling capacitor can vary substantially depending on layout [11]. The equivalent inductance depends on the distance to the reference plane and capacitor's inner electrode architecture [11], [12].

Accurately modeling the inductance associated with decoupling capacitors can be critical to the design of the power delivery network (PDN), but it is not practical to estimate the inductance of the capacitor and its connections to the PDN using commercial electromagnetic (EM) tools, considering the many connection configurations that are possible.

Here, a method is proposed to partition the total loop inductance associated with a decoupling capacitor into sub-models for the capacitor and mounting pads and for the traces and vias connecting the capacitor to the power and return planes. The partitions are outlined in Figure 1. Partitioning allows the designer to make a single estimate of inductance for the capacitor and mounting pads and to pair this estimate with a estimate of inductance for the connecting traces and vias made for a variety of trace configurations.

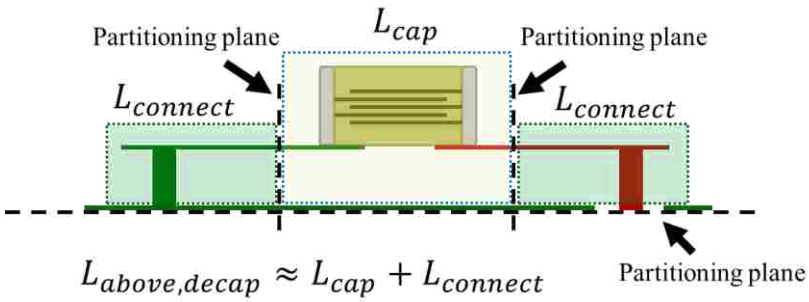


Figure 1. The total inductance associated with a decoupling capacitor, $L_{above,decap}$ can be partitioned into a portion associated with the capacitor and mounting pads, L_{cap}, and a portion associated with the connecting traces and vias, $L_{connect}$.

Not every user has access to a commercial EM tool to estimate the inductances shown in Figure 1. Estimates of these inductances, however, can be made using a simple

representation of the decoupling capacitor using the partial equivalent element circuit (PEEC) method [13]. PEEC allows representation of electromagnetic parasitics with electrical circuit elements whose values can be calculated using closed-form expressions. A method of approximating the inductance associated with the decoupling capacitor and pads using closed-form expressions is developed here using PEEC.

The following sections discuss the method used to partition inductance, studies performed to determine the internal geometries of several commercially available capacitors, experiments and simulations that demonstrate the accuracy of the partitioning approach, and the development of the simplified PEEC model and its associated closed-form solution for inductance

2. PARTITIONING APPROACH

Figure 1 shows the partitioning of the total inductance associated with a PDN decoupling capacitor, $L_{above,decap}$, into inductance associated only with the capacitor and pads, L_{cap}, and inductance associated only with the connecting traces and vias, $L_{connect}$. The inductance associated with the vias after penetrating the power/return plane does not have to be considered since $L_{above,decap}$ does not couple beyond this plane. Using this partitioning, the total capacitance can be approximated as

$$L_{above,decap} = L_{connect} + L_{cap} + error \quad (1)$$

where the error is caused by ignoring the mutual inductance between $L_{connect}$ and L_{cap}. This error is small, as will be demonstrated later.

With this partitioning, the value of L_{cap} can be estimated independent of the connections to the PDN. L_{cap} will depend on the internal geometry of the capacitor, the pads, and the distance to the power/return plane. The inductance of the connecting traces and pads, $L_{connect}$, can be estimated for a number of possible connections configurations and combined with the estimate or model for L_{cap} to find the total inductance.

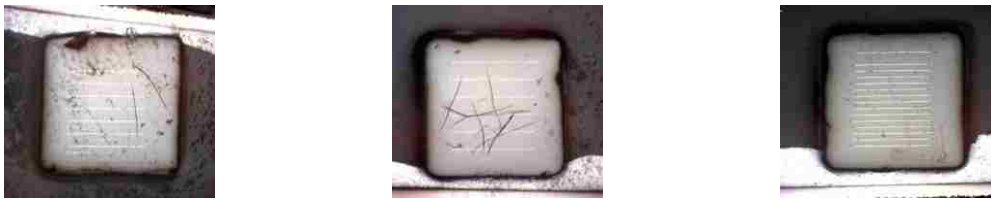
3. CAPACITORS AND CONNECTIONS

Estimating the inductance of the mounted capacitor requires knowledge of the capacitor's internal architecture [14]. The internal geometries of the several commonly used capacitors were studied. Capacitors with values of 22 μF, 100 nF, and 1 nF and in 0201, 0402, 0603, and 0805 sizes were studied because they are commonly used in the PDN designs. Measurements were made of capacitors from five different manufacturers.

3.1. CAPACITOR'S INTERNAL ARCHITECTURE

To measure the capacitors' internal dimensions, the capacitors were cut and viewed under a microscope. Cross-sections of two 0603 capacitors with values of 1 nF and 100 nF are shown in Figure 2 and Figure 3, respectively.

Figure 4 shows the internal dimensions that were measured during the study. The range of each dimension are given in Tables 1-5 for each capacitance value and package size. The distance between the reference plane and the closest electrode is particularly important to L_{cap}. The range of measured values are later used to estimate the expected range of the inductance associated with the mounted capacitors, L_{cap}.



(a) (b) (c)

Figure 2. The cross-section of 0603 capacitors with 1 nF nominal capacitance produced by (a) manufacturer A; (b) manufacturer B; (c) manufacturer C.

(a) (b) (c)

Figure 3. The cross-section of 0603 capacitors with 100 nF nominal capacitance produced by (a) manufacturer A; (b) manufacturer B; (c) manufacturer C.

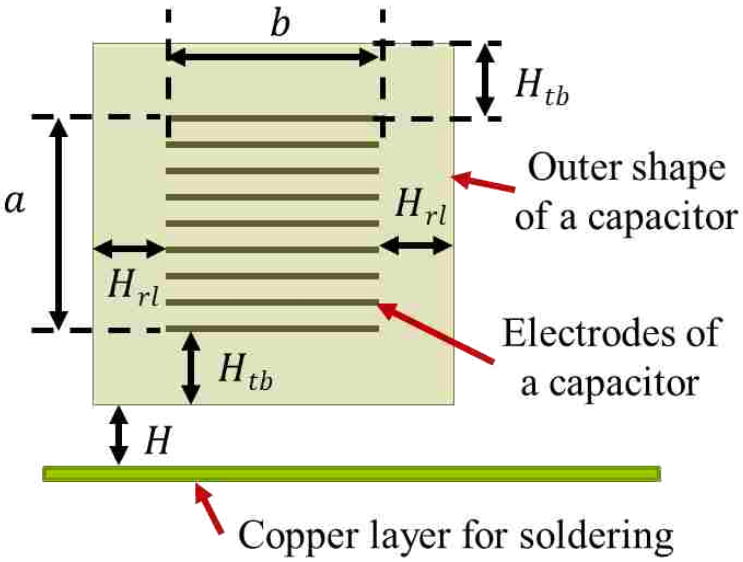


Figure 4. Dimensions of the capacitor's internal architecture.

Table 1. Dimensions in mils of 22 μF 0805 capacitor.

	a	b	H_{tb}	H_{rl}	H
Minimum	38	27	1.6	3.5	1
Average	41	35	3	3.7	2
Maximum	44	44	4.5	4	4

Table 2. Dimensions in mils of 1 nF 0603 capacitor.

	a	b	H_{tb}	H_{rl}	H
Minimum	16	13	4.8	4	1
Average	18	18	6	6	2
Maximum	20	20	7.7	12	4

Table 3. Dimensions in mils of 100 nF 0603 capacitor.

	a	b	H_{tb}	H_{rl}	H
Minimum	17.6	17.6	2.3	4.1	1
Average	19	19	5	5	2
Maximum	25	25	6.3	7	4

Table 4. Dimensions in mils of 100 nF 0402 capacitor.

	a	b	H_{tb}	H_{rl}	H
Minimum	13.8	7.7	2.4	3.5	1
Average	13	11	3.5	4.5	2
Maximum	9.7	11.1	4.4	6.2	4

Table 5. Dimensions in mils of 1 nF 0201 capacitor.

	a	b	H_{tb}	H_{rl}	H
Average	12.6	10	3	3.5	2

3.2. CAPACITOR'S CONNECTIONS

Capacitors may be connected to the PDN through a variety of connection layouts. A few of the more common layouts and their inductance are shown in Figure 5 [15]. Layouts #2 and #5 are studied in this paper. Design #2 will be referred to as the "straight" layout, and design #5 as the "L-shaped" layout. The dimensions of the studied layouts are shown in Figure 6. The layout was sized for an 0603 capacitor, though other sizes could easily be analyzed with the technique proposed here.

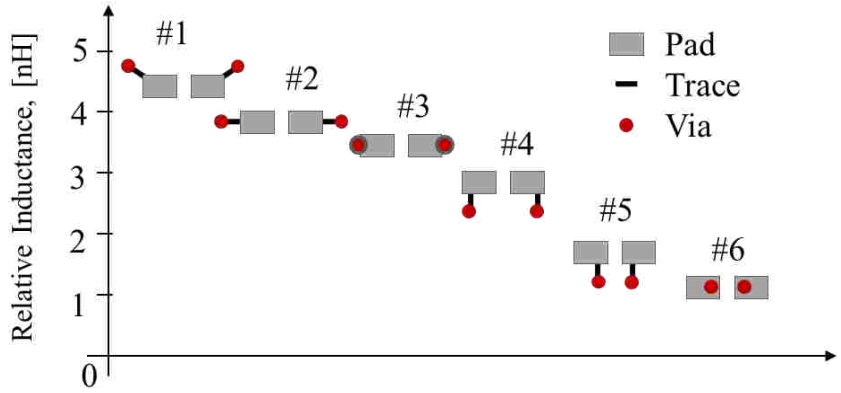
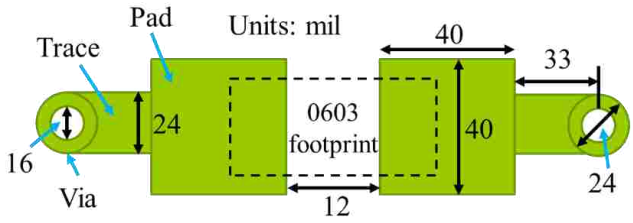


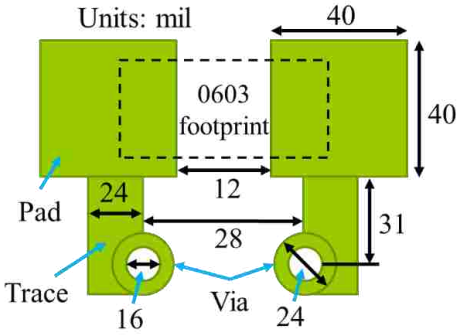
Figure 5. Typical decoupling capacitor connection techniques and their connection inductance (top view) [15].

Two designs, straight and L-shaped, were selected to demonstrate proposed partitioning approach. Initial designs of these two designs are shown in Figure 7. Layout dimensions are suitable for 0603 package capacitor's footprint. The partitioning approach

can be applied to any other layout designs. In this paper only two designs were selected to show and validate partitioning approach.



(a)



(b)

Figure 6. Layout dimensions of the (a) straight; (b) L-shaped layout designs [16].

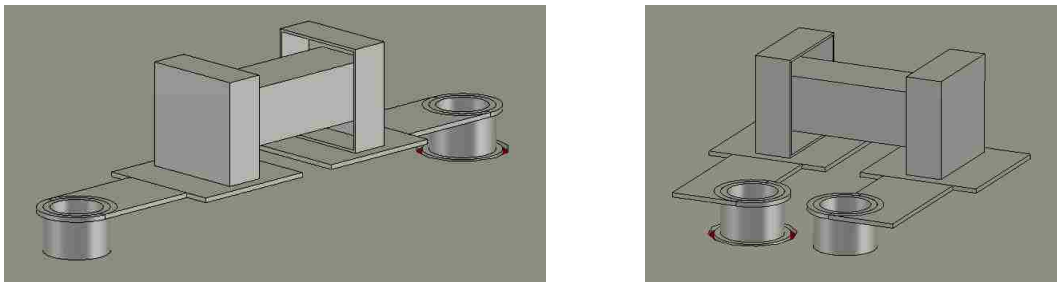
4. VALIDATION OF PARTITIONING APPROACH

The accuracy of the partitioning approach was validated by estimating the overall inductance of the mounted capacitor, $L_{above,decap}$, in simulation, demonstrating simulated values of inductance were correct by comparing them with measurements, then demonstrating that simulated values of inductance for the decoupling capacitor, L_{cap}, and its connections, $L_{connect}$, could be used to accurately estimate $L_{above,decap}$.

4.1. MODEL OF MOUNTED CAPACITOR

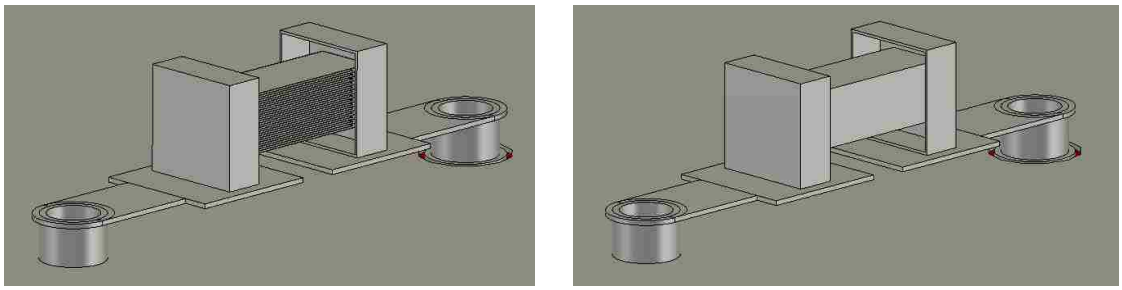
Examples of the CST simulation models of the mounted decoupling capacitors studied here are shown in Figure 7. The multiple electrode plates used to construct a decoupling capacitor do not necessarily have to be included in an electromagnetic model for inductance [17], [18]. Below a gigahertz, within the frequency range of interest here, the current is roughly uniform distributed among the plates, so the magnetic flux between the plates is close to zero. In this case, the plates can be modeled as a solid conductive block.

Figure 8a shows a simulation model of an 0603 100 nF decoupling capacitor and its connections to the PDN, where all 54 electrode plates were included in the model. Figure 8b shows a model where the capacitor's electrodes were approximated as a solid conductive block. These models were simulated in CST Microwave Studio. The loop inductance, $L_{above,decap}$, for the detailed capacitor model in Figure 8a was 1092 pH, and was 1179 pH for the approximate model in Figure 8b. The 87 pH (7%) difference between the models was deemed acceptable for this study.



(a) (b)

Figure 7. Models of 100 nF 0603 capacitor mounted on the (a) straight; (b) L-shaped layout.



(a) (b)

Figure 8. Full-wave simulation models of (a) the detailed capacitor with 54 electrode plates; (b) the approximated capacitor with a solid block conductor, while mounted on the straight layout.

4.2. VALIDATION OF SIMULATION MODEL

The simulation models in Figure 7 were validated through measurements of $L_{above,decap}$. Decoupling capacitors were mounted to a fixture which was a standard 4-layer PCB, with two SMA ports connected to the power and return planes from the top and the bottom of the board [19]. To obtain $L_{above,decap}$, a measurement of the transfer impedance between the two ports is used to estimate the entire inductance looking into the PDN, L_1, including the capacitor, pads, vias, and ground plane. The inductance, L_2, looking into an equivalent PDN was also measured, where the decoupling capacitor inductance is removed from the measurement by shorting the power via to the return plane. The inductance $L_{above,decap}$ created by the capacitor, pads, traces, vias, and reference plane is calculated by subtracting the two inductances, i.e.:

$$L_{above,decap} = L_1 - L_2 \tag{2}$$

The inductance associated with the mounted capacitor will vary between manufacturers and between tests, depending on the internal structure of the capacitor [14] or the soldering, which can cause variations in the distance between the capacitor and

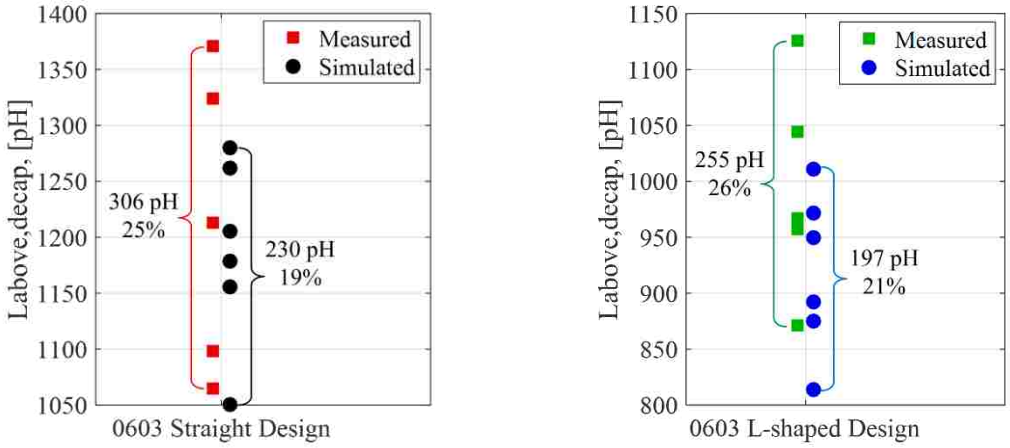
return plane or position of the capacitor on the pads. Since the precise geometries associated with the measured capacitors were not know, measurements of inductance were made using five 0603 100nF capacitors of the same capacitance but from different manufacturers and were compared to simulations of inductance for typical geometry variations shown in Table 3. Measured and simulated inductance, $L_{above,decap}$, for the straight and L-shaped layouts are shown in Figure 9. The measured values of inductance vary by about 26% for both layouts. Not surprisingly, the inductance for the straight layout was generally higher than for the L-shaped layout. Variations seen in the simulated values of inductance closely matched those seen in measurement. As shown in Table 6, the difference between the average inductance found in simulation and in measurement were within 8%, demonstrating the relatively good accuracy of the simulation models for $L_{above,decap}$.

Table 6. Average Values of $L_{above,decap}$.

	Straight Layout	L-shaped Layout
Simulated	1188 pH	919 pH
Measured	1214 pH	993 pH
Difference	2%	8%

The slightly higher values of inductance seen in measurements compared to simulation may have been caused by the solder tilting or rotating the capacitor slightly above the return plane in measurements. The solder can change relative angle between

reference plane and capacitor body. These changes in placement has not been accounted for in simulations.



(a) (b)

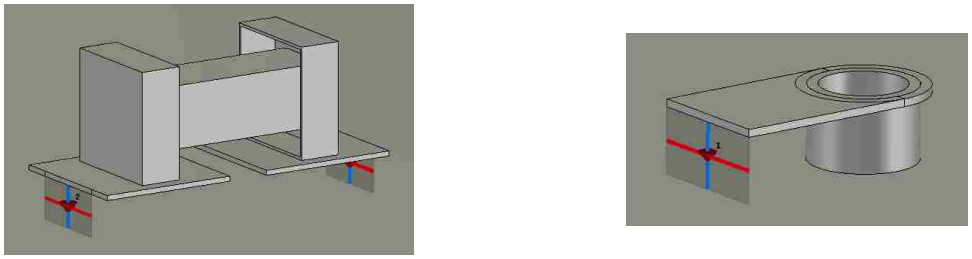
Figure 9. Variation is measured and simulated $L_{above,decap}$ while changing the 0603 capacitor's geometry and placement for (a) straight and (b) L-shaped layout designs.

4.3. PARTITIONING

As shown in Figure 1, the partitioning approach separates the inductance, $L_{above,decap}$, into a portion associated with the traces and vias, $L_{connect}$, and a portion associate with the capacitor and pads, L_{cap}. The partition could occur at multiple locations (e.g. within the pad or within the trace connecting the pad to the via). Here, the partition was made at the location the pad connected to the trace. This partitioning allows more variation in how the designer connects to the pad, for example at the ends as in the straight layout or at the sides as in the L-shaped layout. It is assumed that coupling

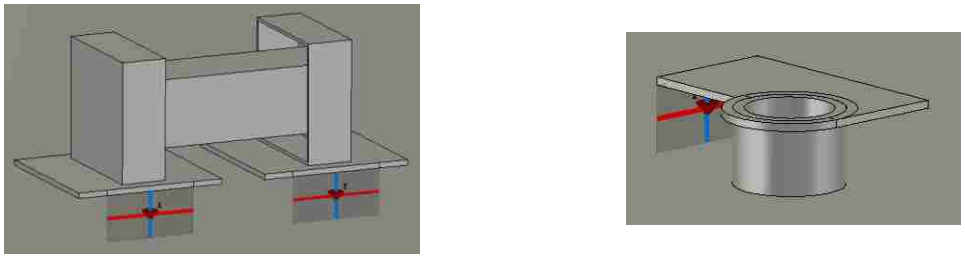
between the sub-models capacitor and for the traces and vias is small, so that their inductances can be simply added to estimate $L_{above,decap}$.

The models for each partition for the straight and L-shaped layout are shown in Figure 10 and Figure 11. The unpartitioned models are shown in Figure 7. The models were partitioned at the position where the trace and pad connect. The geometries for the capacitor are the same in Figure 10a and Figure 11a, but the port locations are different. The location of the connection port is shown.



(a) (b)

Figure 10. The straight layout shown in Figure 8a was partitioned into models of (a) L_{cap}, representing the pads, capacitor, and reference plane, and (b) $L_{connect}$, representing the connecting trace and via, and the reference plane.



(a) (b)

Figure 11. The L-shaped layout shown in Figure 8b was partitioned into models of (a) L_{cap}, representing the pads, capacitor, and reference plane, and (b) $L_{connect}$, representing the connecting trace and via, and the reference plane..

The partial inductances associated with each partition shown in Figure 10 and Figure 11 were simulated in CST Microwave studio and were used to estimate the total inductance of the mounted capacitor and traces, $L_{above,decap}$. The estimated values for L_{cap} and $L_{connect}$, as well as for $L_{above,decap}$ found using the partitioning approach and found using direct simulation of the entire structure, are listed in Table 7. While the capacitor and pad geometries did not change for the straight and L-shaped layouts, the values for L_{cap} differ between the designs because of the port locations. The current flow and associated flux changes when the port is moved from the end of the pad to the side.

The accuracy of the partitioning approach is a function of the thickness of the dielectric under the capacitor. As shown in Table 7, the thicker the dielectric the greater the error introduced by the partitioning approximation. This error likely results because of coupling between L_{cap} and $L_{connect}$, which increases with distance to the return plane. It should be noted, however, that the dielectric thickness in high-speed, multilayer PCBs do not typically exceed 6 mil. The expected error using the partitioning approach should not exceed 16% in these cases. The greater error observed in the partitioning approach for the L-shaped design than the straight design is also likely due to the greater coupling between the capacitor and the connecting traces for this design strategy.

5. THE MOUNTED CAPACITOR'S INDUCTANCE

The inductance associated with the capacitor alone, L_{cap}, is similar to the inductance parameter typically given by the manufacturer, ESL [20]. The single value of

ESL provided by the manufacturer, however, does not take into account how inductance changes with the distance between the capacitor and return plane.

Table 7. Partitioning error depending on the height between reference plane and pads.

Straight Design					
Height, h, [mil]	Partitioning Approach			Direct Sim.	error
	$L_{connect}$ [pH]	L_{cap} [pH]	$L_{above,decap} \approx L_{connect} + L_{cap}$, [pH]	$L_{above,decap}$ [pH]	
3	158	457	615	622	2%
5	246	547	793	769	3%
6	286	590	876	836	5%
10	438	748	1186	1073	11%
12	510	823	1333	1179	13%
L-shaped Design					
Height, h, [mil]	Partitioning Approach			Direct Sim.	error
	$L_{connect}$ [pH]	L_{cap} [pH]	$L_{above,decap} \approx L_{connect} + L_{cap}$, [pH]	$L_{above,decap}$ [pH]	
3	160	416	576	547	5%
5	246	481	727	645	13%
6	286	513	767	687	16%
10	436	629	1065	820	29%
12	508	684	1192	875	36%

Figure 12 shows the variations in L_{cap} for different capacitor sizes as the distance between the capacitor and reference plane changes from 3 to 6 mils. The ports were assigned at the ends of the pads, as in the straight layout shown in Figure 10a. Values are shown using the average dimensions of the 0201 1 nF capacitor, 0402 100 nF capacitor, 0603 100 nF capacitor, and 0804 22 uF capacitor shown in Tables 1-5. Different inductances would be expected for the L-shaped layout. Values for L_{cap} can vary by as much as 50% for 0201 and 23% for 0805 in a given package size over this relatively modest range of distances from the return plane. Even greater variations would be expected if changes in the location of the port connection were also taken into account. These variations in L_{cap} clearly demonstrate why a single value for ESL is often not sufficient to characterize the inductance associated with the capacitor in the final design.

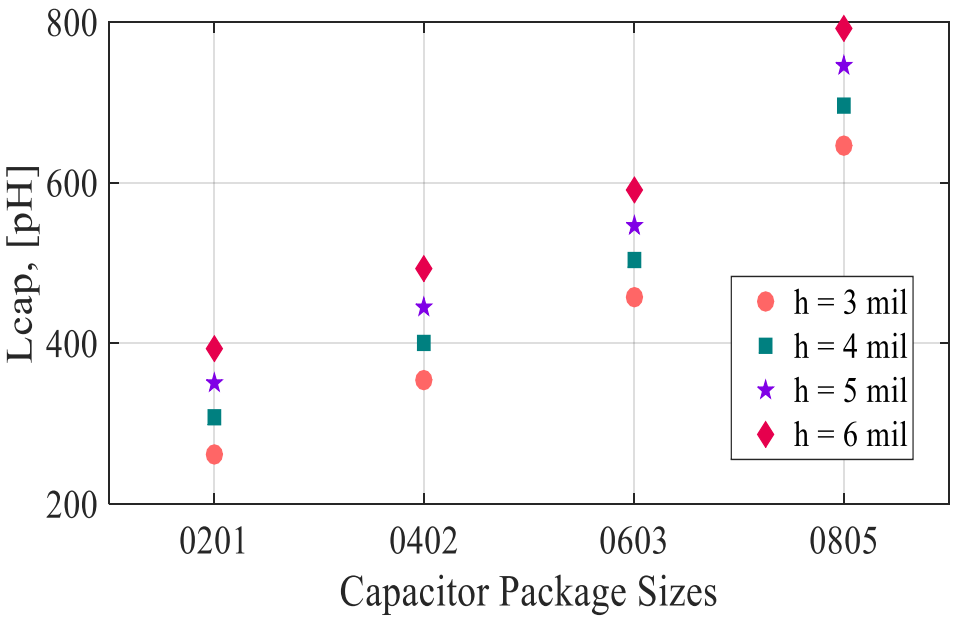


Figure 12. The mounted capacitor's inductances for different capacitor's package sizes depending on the distance between capacitor and reference plane.

5.1. THE PEEC INDUCTANCE MODEL

As shown in Table 7, the inductance associated with the capacitor, L_{cap}, depends on how the traces are connected to the pad. While the values of L_{cap} can be estimated using a solver like CST and varying the port locations, another option is to determine the values in PEEC. PEEC has the advantage the circuit parasitics are represented using circuit elements so that simulations can be performed using SPICE.

PEEC approach was used to apply circuit elements to the segments of the geometry and inductance cells are shown in Figure 13. Elements of the inductance circuit is calculated using analytical equations of the PEEC method [13]. Analytical solution does not require integral calculates and computation is time effective. Vertical and horizontal cells of the partial inductances are created according to Chapter 5 in [13]. Pads and capacitor's terminals are assumed to have zero thickness and partial self- and mutual inductances are calculated for rectangular sheets using (6) in Appendix A [13]. A solid block, representing capacitor's electrode, is treated as a finite thickness boxes, and partial self- and mutual inductances are calculated using (12) in Appendix A [13].

The inductance, L_{cap}, is highly influenced by the location of the port as shown in Table 7. A port is placed at the connection point of a pad and a trace. The port can be assigned at a different location of the PEEC model and represent L_{cap} models of the straight (Figure 10a), and L-shaped (Figure 11a) layouts. Figure 13 shows port assigned to the PEEC model similar to the model in Figure 10a. The detailed PEEC model (Figure 13) includes vertical and horizontal cells to account for an accurate current direction path.

The inductance of the capacitor, pads, and reference plane is calculated using PEEC and CST and results are compared in Table 8. The difference between CST and

PEEC solution is not more than 14%. Pads and terminals are assumed to have a zero thickness in PEEC model, which results into 69 pH difference for L-shaped layout model. However, PEEC model requires less than a minute to calculate capacitor's inductance, which is a significant benefit of the PEEC method compared to CST.

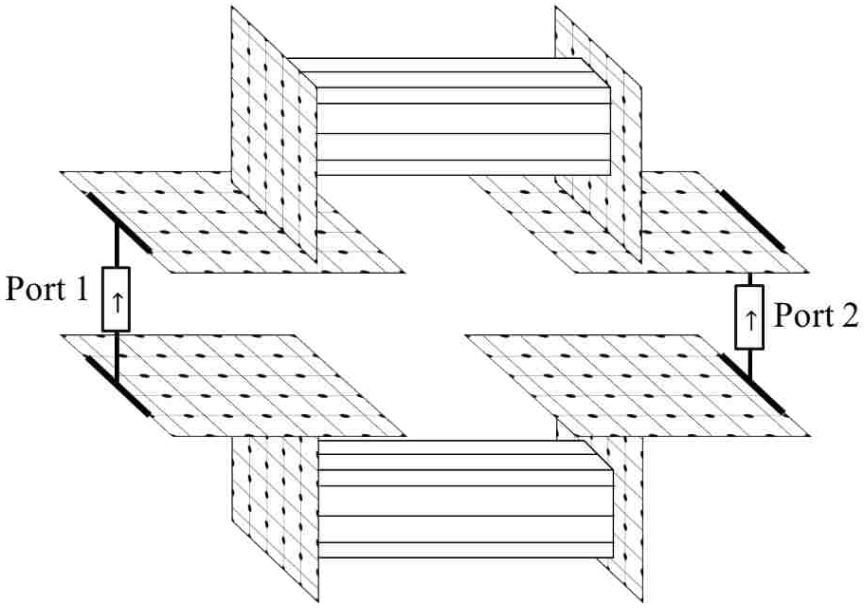


Figure 13. Inductances mesh cells of the mounted capacitor over reference plane, where reference plane was replaced with an image.

Table 8. Inductance of the capacitor calculated using PEEC and CST.

L_{cap} in [pH]; 100 nF 0603 Capacitor; h = 5 mil			
Design	CST	Detailed PEEC	Simplified PEEC
L_{cap} for straight layout (Figure 10a)	547	607	473
L_{cap} for L-shaped layout (Figure 11a)	481	550	N/A

Users without access to a commercial EM solver need a method for estimating L_{cap} using more commonly available tools like SPICE or Matlab. A simplified circuit model of L_{cap} was developed using PEEC whose elements can be determined using closed form expressions. The simplified circuit model representing the straight layout design is shown in Figure 14. The inductances in this model can be calculated using the formulas shown in Appendix A. Each structure in Figure 14a is represented as a single rectangular sheet with zero thickness or with a rectangular bar. The partial self- and mutual inductances for this circuit were calculated for an 0603 capacitor as shown in Table 9. Values in this table were calculated using the average 0603 dimensions shown in Table 3, using the pads dimensions shown in Figure 6, and using a capacitor height h of 5 mils. Mutual inductances in the table are given with respect to a structure's image in the return plane, as shown in Figure 14b. Other mutual inductances were ignored. Once these values are calculated, the total equivalent inductance, L_{cap}, for the capacitor model in Figure 14 can be found as:

$$L_{cap} = \frac{L_{p11} - L_{p12}}{2} \tag{4}$$

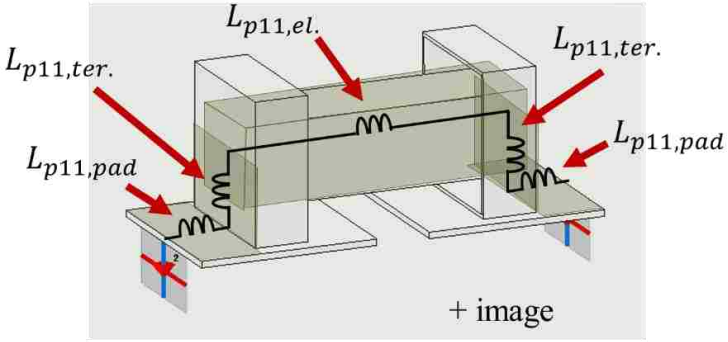
where

$$L_{p11} = 2\left(2L_{p11,pad} + 2L_{p11,ter.} + L_{p11,el.}\right) \tag{5}$$

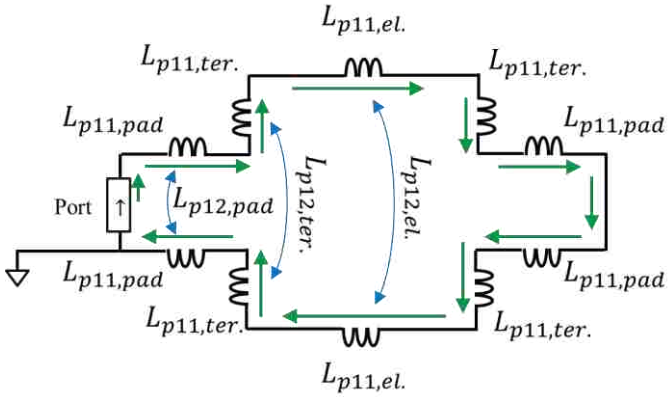
$$L_{p12} = 2\left(2L_{p12,pad} + 2L_{p12,ter.} + L_{p12,el.}\right) \tag{6}$$

Using the values in Table 9 along with (4)-(7), L_{cap} was estimated to be 473 pH. CST found L_{cap} to be 547 pH, a 14% difference. This difference should typically be within the acceptable range of error.

Analyzing the circuit elements in Table 9 demonstrates that conductor associated with the capacitor's electrodes is the main contributor to L_{cap}. The mutual coupling ($L_{p12,el.}$) between the capacitor and its image in the reference plane contributes substantially to the overall value of L_{cap} as well. In this case, the partial mutual inductance to the image is almost half the partial self-inductance of each component. The large contribution of this mutual inductance helps demonstrate the importance of considering the reference plane in L_{cap} calculations.



(a)



(b)

Figure 14. (a) The partial inductances identified on the geometry; (b) simplified PEEC model.

Table 9. Inductance of the capacitor calculated using PEEC and CST.

$L_{p11,pad}$, [pH]	$L_{p11,ter.}$, [pH]	$L_{p11,el.}$, [pH]
57.7	81.7	569.9
$L_{p12,pad}$, [pH]	$L_{p12,ter.}$, [pH]	$L_{p12,el.}$, [pH]
29.7	23.3	279.9

6. CONCLUSION

High-speed designs need increasingly accurate estimates of the power bus impedance. The ESL provided by capacitor manufacturers cannot be used to accurately estimate the inductance associated with a capacitor in a real design because it does not account for coupling to the reference plane and the impact of changes in height with respect to the plane. ESL also does not account for coupling to nearby traces, vias and other circuit elements. Determining the inductance associated with each decoupling capacitor layout in a printed circuit board design using commercial EM tools, however, is impractical given the number of possible layouts.

The partitioning approach proposed here allows the modeling problem to be separated into a portion associated with the capacitor and mounting pads and a portion associated with the traces and vias that connect the capacitor to the power and return planes. This approach was shown to find the overall inductance of the capacitor and its connections to the power bus within 16% of the inductance found by modeling the entire structure at once when the height of the capacitor above the reference plane was 6 mils or

less. This error results because the partitioning approach ignores the coupling between the partition for the capacitor and pads and the partition for the traces and vias. The error increases for larger heights, as the coupling becomes more significant, though most high-speed designs use heights in the 6-mil range.

The advantage of the partitioning approach is that the inductance of the portion associated with the capacitor and pads must be calculated for only a few configurations. The inductance associated with typical trace and via configurations can be calculated separately and then combined later when estimating the overall power bus impedance. Here, the problem was partitioned at the location where the trace connected to the pad. The inductance associated with the capacitor partition varied by 20% or more depending on where the pad connected to the trace, suggesting it is important to estimate this inductance for at least a few trace connection locations.

The simple PEEC model developed here allows users to estimate the equivalent inductance associated with the capacitor and pads without the use of a full wave modeling tool. The closed-form expressions associated with this model estimated the inductance of an 0603 capacitor within 14% of the inductance found using CST, which is within the error margin of the partitioning approach. This simple circuit model, however, can only be applied to the straight layout design.

Modeling of the capacitor in PEEC and in CST was simplified by approximating the electrode stack as a solid conductor block. The overall inductance found using the solid block approximation was within 87 pH (7%) of the value found when modeling the full electrode stack for a case studied here.

Results demonstrate the partitioning approach may be used to estimate values of inductance, and thus of power bus impedance, that are more accurate than using the manufacturer provided ESL, and that are nearly as accurate as using commercial EM simulations of the entire capacitor and its connections to the power bus. The partitioning approach also promises to be much faster and more practical than performing simulations of each decoupling structure used in a printed circuit board design.

APPENDIX A

The partial self- and mutual inductances associated with the simplified PEEC model in Figure 14 can be estimated using the following equations. PEEC defines the partial self-inductance, L_{pii}, for a conductor, i, from the equation $V_i = sL_{pii}I_i$, where V_i is the voltage along conductor i, I_i is the current in the conductor, $s = 2\pi f$, and f is a frequency. Similarly, the partial mutual inductance, L_{pij}, is defined between two conductors i and j as $V_i = sL_{pij}I_j$. The pads and terminals of the capacitor shown in Figure 14 can be approximated as rectangular sheets with zero thickness. The partial mutual inductances between two zero thickness rectangular sheets, like those shown in Figure 15, is given by [13]:

$$
\begin{aligned}
L_{p12} = \frac{\mu_0}{4\pi}\frac{1}{(y_{e1}-y_{s1})(y_{e2}-y_{s2})}\sum_{k=1}^{4}\sum_{m=1}^{4}(-1)^{m+k} \\
\cdot\left[\frac{b_m^2 - Z^2}{2}a_k \log(a_k + r_{km} + \epsilon)\right. \\
+\frac{a_k^2 - Z^2}{2}b_m \log(b_m + r_{km} + \epsilon) - \frac{1}{6}(b_m^2 - 2Z^2 + a_k^2)r_{km} \\
\left. - b_m Z a_k \tan^{-1}\left(\frac{a_k b_m}{r_{km} Z}\right)\right]
\end{aligned}
\tag{6}
$$

where

$$a_1 = x_{s2} - x_{e1}, \quad a_2 = x_{e2} - x_{e1} \tag{7}$$

$$a_3 = x_{e2} - x_{s1}, \quad a_4 = x_{s2} - x_{s1} \tag{8}$$

$$b_1 = y_{s2} - y_{e1}, \quad b_2 = y_{e2} - y_{e1} \tag{9}$$

$$b_3 = y_{e2} - y_{s1}, \quad b_4 = y_{s2} - y_{s1} \tag{10}$$

$$Z = z_2 - z_1 + \epsilon, \quad r_{km} = \sqrt{a_k^2 + b_m^2 + Z^2} \tag{11}$$

The partial self-inductance of the rectangular sheet is calculating using (6), with the assumption that $Z = \epsilon$. That is, the partial self-inductance can be solved by estimating the partial mutual-inductance for two sheets separated by an infinitesimally small value of ϵ [13].

The capacitor electrodes can be approximated as solid conductive rectangular bar, as shown in Figure 14 and Figure 16. The partial mutual inductance between two rectangular bars is given by [13]:

$$\begin{aligned} L_{p12} = {} & \frac{\mu_0}{4\pi}\frac{1}{\mathcal{A}_1\mathcal{A}_2}\sum_{k=1}^{4}\sum_{l=1}^{4}\sum_{m=1}^{4}(-1)^{k+l+m+1} \\ & \cdot\left[-\frac{b_l c_m a_k^3}{6}\tan^{-1}\left(\frac{b_l c_m}{a_k R}\right) - \frac{b_l c_m^3 a_k}{6}\tan^{-1}\left(\frac{b_l a_k}{c_m R}\right)\right. \\ & -\frac{b_l^3 c_m a_k}{6}\tan^{-1}\left(\frac{c_m a_k}{b_l R}\right) + a_k\left(\frac{b_l^2 c_m^2}{4} - \frac{b_l^4}{24} - \frac{c_m^4}{24}\right) \\ & \cdot\log\left(\frac{a_k + R}{\sqrt{b_l^2 + c_m^2}}\right) + b_l\left(\frac{c_m^2 a_k^2}{4} - \frac{c_m^4}{24} - \frac{a_k^4}{24}\right) \\ & \cdot\log\left(\frac{b_l + R}{\sqrt{c_m^2 + a_k^2}}\right) + c_m\left(\frac{b_l^2 a_k^2}{4} - \frac{b_l^4}{24} - \frac{a_k^4}{24}\right)\cdot\log\left(\frac{c_m + R}{\sqrt{a_k^2 + b_l^2}}\right) \\ & \left.+\frac{1}{60}(b_l^4 + c_m^4 + a_k^4 - 3b_l^2 c_m^2 - 3c_m^2 a_k^2 - 3a_k^2 b_l^2)R\right] \end{aligned} \tag{12}$$

where

$$a_1 = x_{s2} - x_{e1}, \quad a_2 = x_{e2} - x_{e1} \tag{13}$$

$$a_3 = x_{e2} - x_{s1}, \quad a_4 = x_{s2} - x_{s1} \tag{14}$$

$$b_1 = y_{s2} - y_{e1}, \quad b_2 = y_{e2} - y_{e1} \tag{15}$$

$$b_3 = y_{e2} - y_{s1}, \quad b_4 = y_{s2} - y_{s1} \tag{16}$$

$$c_1 = z_{s2} - z_{e1}, \quad c_2 = z_{e2} - z_{e1} \tag{17}$$

$$c_3 = z_{e2} - z_{s1}, \quad c_4 = z_{s2} - z_{s1} \tag{18}$$

$$\mathcal{A}_1 = (y_{e1} - y_{s1})(z_{e1} - z_{s1}) \tag{19}$$

$$\mathcal{A}_2 = (y_{e2} - y_{s2})(z_{e2} - z_{s2}) \tag{20}$$

$$R(a_k, b_l, c_m) = \sqrt{a_k^2 + b_l^2 + c_m^2} \tag{21}$$

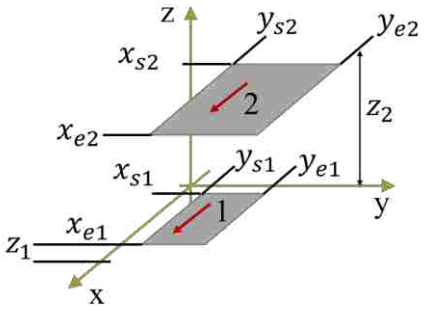


Figure A.1. Two parallel zero thickness conductors [13].

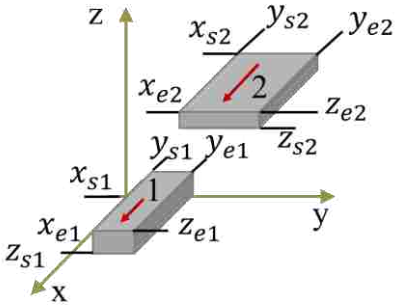


Figure A.2. Two parallel rectangular bar conductors [13].

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II. SIMPLE CIRCUIT MODELS OF THE INDUCTANCE OF 8-TERMINAL DECOUPLING CAPACITORS

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ABSTRACT

The series inductance associated with decoupling capacitors can contribute significantly to the power distribution network impedance. The 8-terminal capacitors considered in this work have a lower self-inductance than the 2-terminal capacitors which are commonly used in IC package. The equivalent series inductance (ESL) provided by manufacturers cannot accurately predict the inductance seen during use, however, because ESL cannot account for the coupling between the capacitor and nearby structures like the return plane. To accurately estimate the inductance of an 8-terminal capacitor, a model of the capacitor was developed in CST Microwave Studio. The partial equivalent element circuit (PEEC) method was used to construct simple models that could be simulated in SPICE. Accurate estimates of inductance were obtained by representing the body of the capacitor as a solid conductive block. This representation substantially reduced the compute time and resulted in a 3% (~1 pH) difference in the estimated inductance compared to the detailed models of the multi-layer ceramic capacitors. The PEEC models of the capacitors and layout provide options for circuit-level simulations and the analytic estimation of inductance. The CST and the circuit models agreed within

9% (~3 pH). With the partitioning we used, the circuit models are computed independent from the rest of the PDN circuit. Hence, the inductance can be pre-calculated to save PDN compute time. The models also allowed study of the impact of changes to the capacitor layout, like the impact of the distance to the return plane, and the symmetry of the via placement. These models will allow the IC-package designer to rapidly evaluate package layouts and fix potential problems.

1. INTRODUCTION

Decoupling capacitors (decaps) are used to keep the power distribution networks (PDN) impedance acceptably low in package and printed circuit board (PCB) designs [1], [2]. The capacitors reduce power supply noise and associated signal or power integrity issues [3], [4]. On-package decoupling capacitors may be used to reduce high frequency noise up to gigahertz frequencies. The PDN impedance is typically kept below a target impedance to ensure voltage fluctuations on the PDN are smaller than an allowable limit [2], [5]. The PDN impedance must be in the milliohms range up to several hundred megahertz for high performance designs [6].

A major contributor to the PDN impedance at higher frequencies is the series inductance to the decoupling capacitors [7], [8], [9]. Eight-terminal capacitors have up to an 80% lower inductance than similar 2-terminal capacitors [10], [11].

A good electrical model for a decoupling capacitor is a series RLC circuit, where R is the equivalent series resistance (ESR), L is the equivalent series inductance, and C is the capacitor's nominal value [6]. Manufacturers usually provide a single value for the

inductance in terms of its so-called “ESL” [2], [12]. The values for ESL are based on measurements performed on a specific test fixture [11], [15], [16], and depend on the measurement fixture characteristics [2], [15], [17]. Typical representations of ESL do not take into account the layout and associated coupling to structures in the surrounding environment, such as the ground plane and pads. Unfortunately, the actual inductance depends strongly on this coupling [5], [12], [18], [19]. More complicated models are available for modeling a capacitor’s behavior above the first RLC circuit resonance frequency [6], [13], [14], but these representations also do not take into account coupling within the local environment.

Full-wave modeling of the complete geometry, including the local environment, can give accurate inductance values [13]. The partial equivalent element circuit (PEEC) method allows development of full-wave models which can easily be incorporated into SPICE models of the rest of the PDN design [20], [21], [22], [23]. This circuit approach gives insight into behavior as well as allowing the engineer to quickly make changes within the SPICE model to incorporate changes made to the actual layout [23].

A typical package design with a flip-chip IC and decoupling capacitor is shown in Figure 1 [2], [8]. The decoupling capacitor is connected to the PDN through traces and vias. The connection to the topmost reference plane, usually a ground plane, is a good place to partition the inductance associated with the capacitor from the inductance associated with the package and PCB [5]. We call the inductance pointing into the capacitor from the via holes in the ground plane as $L_{above,decap}$, as shown in Figure 1. The total equivalent inductance of the PCB and package, L_{below}, is associated with the current loop below the partitioning ground plane through all the layers up to the IC [4].

These two inductances can be calculated separately, and the results combined after calculation to obtain the complete PDN impedance.

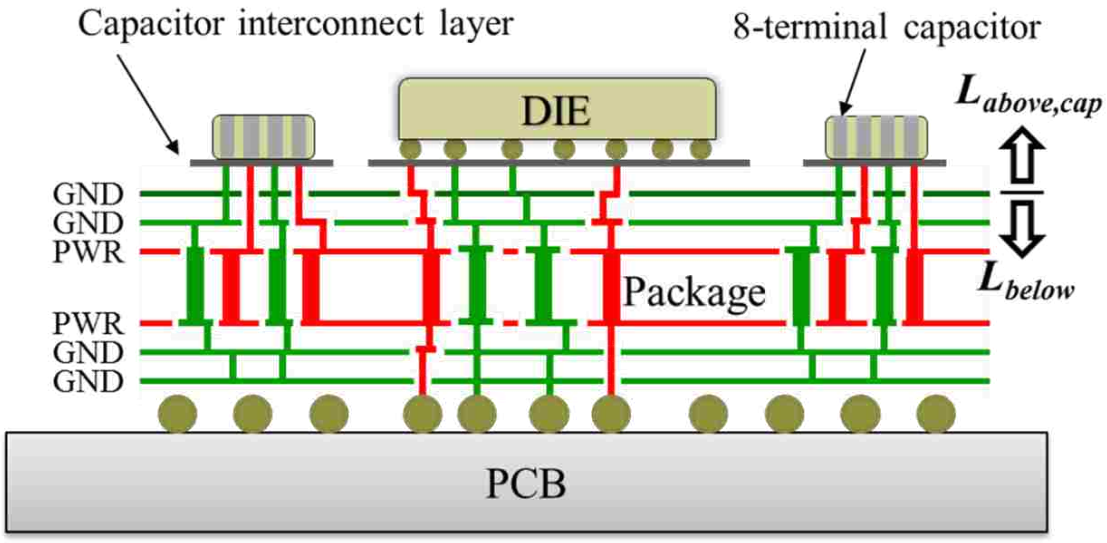


Figure 1. Cross-section of a typical power distribution network with decoupling capacitors [2], [8].

An inductance model of the 8-terminal capacitor and its connections to the power and the return plane is developed in this paper. A simplified model, which maintains most of the accuracy, is developed by representing the body of the capacitor as a solid block. A further simplified circuit model of the capacitor is developed using the PEEC method [22]. The next section considers the internal connections of the capacitors. Then a simple PEEC circuit-level model is given while equivalent circuit models are presented in Section 3. The circuit models are such that an analytical evaluation of the inductance can be used the capacitor couplings and the layout circuit can be used to study the impact of changes in geometry on current path inductance.

2. STRUCTURE UNDER TEST

Eight-terminal capacitors minimize the connection inductance through a variety of strategies. The distance between pins (terminals) is made small to reduce the size of the current path size and thus the inductance [11]. Alternating power and return pins further reduce the overall inductance by increasing the mutual inductance between internal capacitors [10], [11].

Currently, two manufacturers produce 8-terminal capacitors, AVX and TDK [11], [24]. The terminal connections and equivalent schematics, however, are different between them. Both 8-terminal capacitors are analyzed in the following sections.

2.1. AVX 8-TERMINAL CAPACITOR

AVX made the Inter-Digitated Capacitor (IDC) design to reduce the capacitor's internal inductance [11]. The internal architecture of AVX IDC capacitor is shown in Figure 2a. The AVX IDC will be referred to as the "consolidated" capacitor throughout the text, identifying that all positive pins (pins 2, 4, 5, and 7) are connected internally, as all are the return pins (pins 1, 3, 6, and 8). Effectively, there is a single capacitance between the positive pins (2, 4, 5, and 7) and negative pins (1, 3, 6, and 8) as shown in Figure 2b [11].

2.2. TDK 8-TERMINAL CAPACITOR

TDK produces the CLL series 8-terminal multilayer ceramic capacitors with a reduced internal inductance [24]. Reduced inductance is achieved in a similar manner as

the “consolidated” capacitor, but the capacitor configuration differs slightly. The architecture of the inner electrodes is shown in Figure 2c. A corresponding equivalent circuit is shown in Figure 2d [24]. The TDK CLL capacitor is made so there is a unique capacitance between each set of neighboring pins. The design from the TDK will be referred to as the “divided” capacitor, indicating that some pins are electrically isolated at dc. When used as a decoupling capacitor, pins 1, 3, 6, and 7 of the TDK CLL should be connected to one supply and pins 2, 4, 5, and 7 to the other [24]. Connected in this way the divided and consolidated capacitors perform very similarly. If the TDK CLL is used to decouple more than one supply, so that the pins are connected differently, the overall inductance may be much larger. In this paper, the TDK CLL capacitor is assumed to be used as a single decoupling capacitor with the positive supply connected to pins 1, 3, 6, and 8 and the negative supply to pins 2, 4, 5, and 7.

2.3. INDUCTANCE MODELS

To study the inductance, detailed models of the consolidated and divided capacitors with pads and vias connecting to power planes were built in CST Microwave Studio as shown in Figure 3. To accurately determine the internal structure, the AVX IDC and TDK CLL capacitors were cut, polished, and observed under a microscope as shown in Figure 4. The length and width of the electrode plates were measured. Further, the closest distance between the electrode and outside of capacitor was determined. The size of the plates and the distance between the inner plate and the outer shape boundary are critical parameters for determining the capacitor model inductance. The individual capacitors have 102 plates to achieve the large ESC. To avoid long compute times due to

the high dielectric constants (>1000), we placed discrete capacitors between the layers. The dimensions of the 8-terminal capacitor footprint [16], [24] are shown in Figure 5.

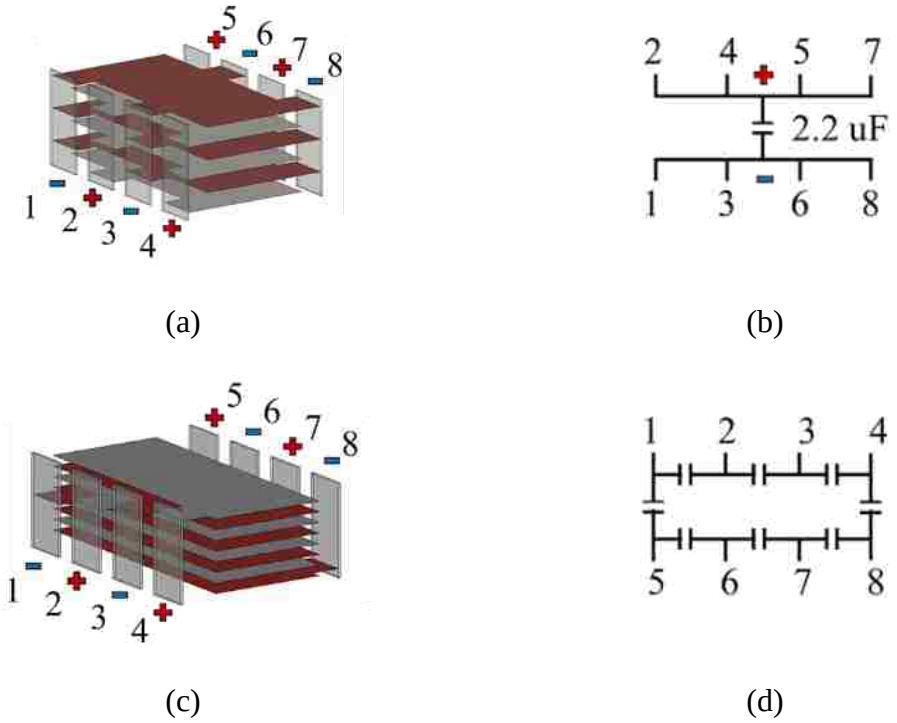


Figure 2. (a) An internal structure, and (b) an equivalent circuit of AVX's IDC "consolidated" capacitor [11], [20]; (c) an internal structure, and (d) an equivalent circuit of TDK's CLL "divided" capacitor [20], [24].

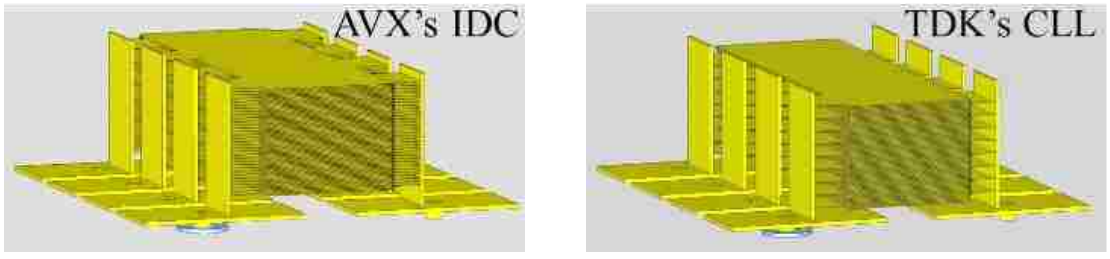


Figure 3. Detailed 3D models of (a) AVX IDC "consolidated" capacitor; (b) TDK CLL "divided" capacitor with interconnects [20].

Figure 4. Cross-section of the divided 0603 capacitor under a microscope with 5x magnification [20].

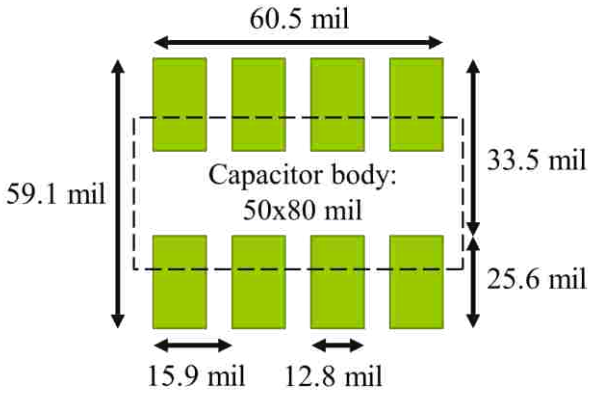


Figure 5. An 8-terminal capacitor footprint [16], [24].

Inductance was estimated among all power pins. Measurement ports were placed across the anti-pad at the point each power via penetrated the reference plane as shown in Figure 6. As there are four power and ground pins, the overall capacitor inductance can be characterized with a four-by-four inductance matrix.

The inductance matrices obtained from CST for the detailed models of the AVX IDC and TDK CLL capacitors are shown in Figure 7. These inductance matrices are calculated at the point where the power via passes through the return plane, and includes the traces, vias, and the capacitor package. The inductance matrix was extracted at 100 MHz.

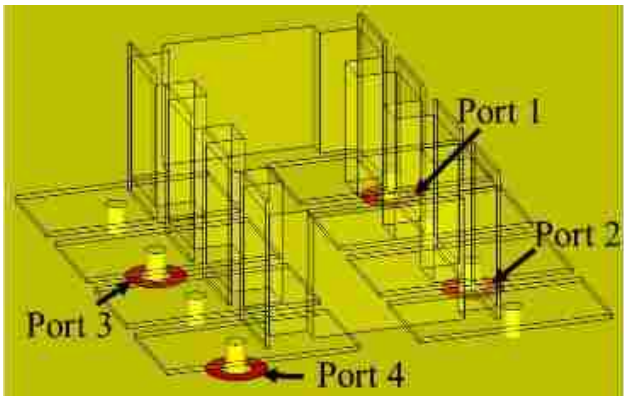


Figure 6. Port defined between power vias and top ground plane.

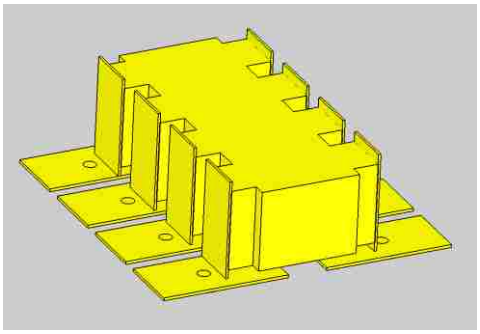
$$\begin{bmatrix} 130 & 8 & 11 & 4 \\ 8 & 99 & 7 & 11 \\ 11 & 7 & 99 & 8 \\ 4 & 11 & 8 & 130 \end{bmatrix} pH \qquad \begin{bmatrix} 133 & 9 & 11 & 4 \\ 9 & 102 & 7 & 11 \\ 11 & 7 & 101 & 9 \\ 4 & 11 & 9 & 132 \end{bmatrix} pH$$

(a) (b)

Figure 7. The inductance matrix calculated for the (a) AVX IDC consolidated; (b) TDK CLL divided capacitor.

Modeling all the electrode layers of the capacitor requires significant computational resources and large compute times. We found that the dense multi-layer geometry could be approximated as a solid conducting block for inductance calculations [20]. At the frequencies of interest, the conductive block approximation is valid since the current flows in the same direction through all the electrode plates. This approximation can be applied to both the AVX IDC consolidated and TDK CLL divided capacitors. The inductance matrix found using this approximation is shown in Figure 8. Approximating the capacitor body with a conductive block results in a maximum 3 pH difference in matrix elements compared to the more detailed models. The multi-terminal box

approximation maintains sufficient accuracy in the estimated inductance and substantially reduces the computational time.



(a)

$$\begin{bmatrix} 133 & 8 & 12 & 4 \\ 8 & 100 & 7 & 12 \\ 12 & 7 & 100 & 8 \\ 4 & 12 & 8 & 133 \end{bmatrix} pH$$

(b)

Figure 8. (a) 3D model and (b) solution of capacitor, when electrodes are represented as a solid block.

In practical designs the overall inductance can be represented with a single value, $L_{above,decap}$, rather than using a matrix [17]. The relation between the inductance matrix, the port voltage, and the port current is:

$$\begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} \\ L_{21} & L_{22} & L_{23} & L_{24} \\ L_{31} & L_{32} & L_{33} & L_{34} \\ L_{41} & L_{42} & L_{43} & L_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \quad (1)$$

A single value for inductance can be found from this relationship by assuming all ports are at the same voltage and the current through the single inductance is equal to the sum of currents through the individual inductances [20]:

$$I = I_1 + I_2 + I_3 + I_4 \quad (2)$$

$$V = V_1 = V_2 = V_3 = V_4 \quad (3)$$

and using the relation

$$L_{above,decap} = \frac{V}{I} \tag{4}$$

The relationship in (3) assumes the voltages at all four ports are the same, which is not necessarily true in the practical PDN designs. From PEEC modeling, we know that it is impossible to connect the four pins without adding inductances between the contacts. Hence, we can say that the combined result in (4) is a lower bound for the total inductance associated with the decoupling capacitor above the plane. While (1) is more accurate, this single value is useful for comparing results and evaluating relative behavior of designs.

The inductance matrices shown in Figure 7 and Figure 8b were converted into a single-value inductance, $L_{above,decap}$, using (4) and those results are las listed in Table 1. The difference between the capacitor approximated as a solid conductive block and the multi-layer detailed capacitor models is about 3% (~1 pH). These results will be further considered in Section 3 when discussing the PEEC models of the capacitors.

Table 1. PEEC and CST for consolidated and divided capacitors.

Solver	Model	Inductance
CST	Detailed AVX IDC model (Figure 3a)	35.2 pH
CST	Detailed TDK CLL model (Figure 3b)	36.0 pH
CST	A solid block approximation (Figure 8)	35.1 pH
PEEC	AVX IDC capacitor (Figure 10 and Figure 11a)	32.0 pH
PEEC	TDK CLL capacitor (Figure 10 and Figure 11b)	33.2 pH
PEEC	Simplified inductance circuit (Figure 12a)	31.4 pH

3. EQUIVALENT PEEC MODEL

The capacitors and their connections to the reference plane (pads, traces, vias, etc.) were modeled using the PEEC method to obtain an equivalent circuit representation of their inductance. Partial inductances for each portion of the design were found using analytical formulas available in the literature [19], [20], [21]. The solid conductive block representing the capacitor body was meshed using rectangular partial inductances as suggested in Figure 9. The pads and "pins" were represented with similar elements. The via partial inductance were modeled with an approximate partial inductance [20], [22]. To model the important impact of the ground-plane we used an image solution. The simplified model for the geometry at hand is shown in Figure 9 and the equivalent circuit is shown in Figure 10.

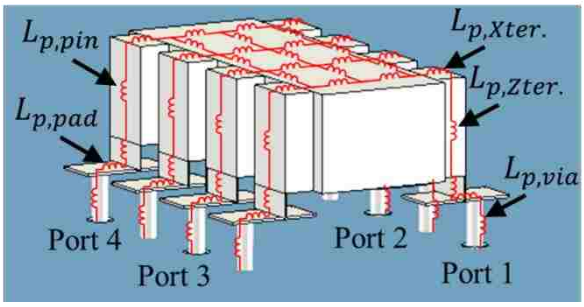


Figure 9. (a) 8-terminal capacitor with a layout subdivided into simple geometrical objects with the corresponding PEEC circuit.

The internal structure for the consolidated and the divided capacitors is different. Figure 10 shows the PEEC inductance circuit for a consolidated capacitor (Figure 11a). Since the current can only flow to neighboring pins in TDK's divided capacitor (Figure

2d), the mesh structure must change. The top view of the equivalent circuit for this mesh in Figure 11b reflects this restriction.

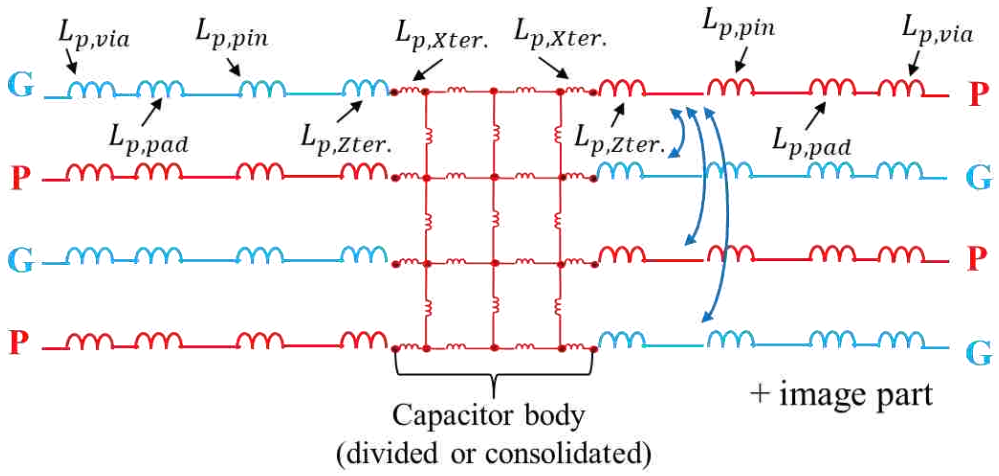


Figure 10. PEEC partial inductance circuit of 8-terminal capacitor and its layout.

(a) (b)

Figure 11. PEEC inductance circuit models of the internal structures of the (a) AVX IDC consolidated; (b) TDK CLL divided capacitors, corresponding to circuit models shown in Figure 2 b and Figure 2 d.

Again, the partial self- and mutual inductances for the simple geometrical cells are given in [23]. Values for finite or zero thickness rectangular prism objects were found using (C.8), (C.15), (C.26), (C.36), (C.40) in [22]. The partial self-inductance of the via is

referred to as $L_{p,via}$. All eight vias have the same partial self-inductance since the geometry is the same. The partial self-inductance of the pads, $L_{p,pad}$, is described using zero-thickness rectangular sheets. The partial self-inductance of the vertical pin that connects the capacitor's electrode to the pad, $L_{p,pin}$, is also described using a zero-thickness rectangular sheet.

The capacitor body was modeled using vertical and horizontal mesh cells. A capacitor body has eight protruding terminals attached to the solid rectangular box. Current in the protruding parts of the electrodes is flowing in the vertical and horizontal direction as well. Partial self-inductance, $L_{p,Xter.}$, is associated with the horizontal current flow and partial self-inductance, $L_{p,Zter.}$, is associated with the vertical current. The current in the terminal is reducing linearly with height as the current enters the main body of the capacitor. Integrating current over the full height of the pin shows the effective inductance can be accurately represented as half the inductance of the total inductance of the terminal.

Partial mutual inductances between the parallel objects were included in the overall model (i.e. between vertical and horizontal terminals, $M_{p,Zter.}$ and $M_{p,Xter.}$, between pins, $M_{p,pin}$, between pads, $M_{p,pad}$ between vias, $M_{p,via}$). Partial mutual terms between orthogonal inductances are equal to zero as they do not couple.

The reference plane was accounted for using an image of the capacitor and its connections. In order to include an image into the PEEC partial inductance model, the "source" circuit shown in Figure 10 was mirrored and corresponding ground pins were connected. Complete PEEC model includes partial mutual terms between source and

image geometries. Including mutual coupling between the sources and images is critical to accurately describe the total inductance of the structure.

The PEEC circuit was solved using modified nodal analysis. The inductance matrix has 104 partial self-inductances. Circuit construction and calculation takes less than a minute. The inductance circuit was solved using modified nodal analysis (MNA) [22].

Table 1 demonstrates $L_{above,decap}$ solutions using PEEC and CST for consolidated and divided capacitors. According to the PEEC calculations, $L_{above,decap}$ of TDK and AVX differ from each other by 1.2 pH, which is consistent with the CST simulations (Figure 7). The PEEC and CST result comparison in Table 1 shows that they differ by 3.1 pH (8.8%) or less.

3.1. ANALYTICAL PEEC SOLUTION

The complex PEEC circuit consists of 104 self-terms and a few hundreds of mutual terms. The circuit can be further simplified to obtain simple analytical solution. An analytical equation helps to identify main contributors to the inductance and quickly approximating $L_{above,decap}$ for different designs. A simplified model of the PEEC inductance circuit is shown in Figure 12a. The model was derived by combining series inductances, ignoring part of the mesh, and accounting for only the mutual inductance between neighboring object or to the return plane. The mesh of the capacitor's internal electrodes is neglected. This assumption is valid because the magnetic flux surrounding the rectangular box is close to zero due to alternating current directions. The circuit in

Figure 12a was determined using only 64 partial self-inductances and 56 partial mutual inductances. Error due to this simplification is analyzed at the end of this section.

As mentioned previously, the circuit in Figure 12a is symmetrical, so the left side of the circuit is simplified (Figure 12b) and then combined with right side to solve for $L_{above,decap}$. Figure 12b shows that partial self-inductances can be added to define L_{path} as in:

$$L_{path} = L_{p,via} + L_{p,pad} + L_{p,pin} + L_{p,Zter.} + L_{p,Xter.} \tag{5}$$

In the same manner, M_{path} and M_{image} are calculated as:

$$M_{path} = M_{p,via} + M_{p,pad} + M_{p,pin} + M_{p,Zter.} + M_{p,Xter.} \tag{6}$$

$$M_{image} = M_{p,image,via} + M_{p,image,pad} + M_{p,image,pin} + M_{p,image,Zter.} + M_{p,image,Xter.} \tag{7}$$

The circuit in Figure 12 b is further simplified as shown in Figure 12 c, where self- and mutual elements are calculated as:

$$L = 2(L_{path} + M_{image}) \tag{8}$$

$$M = 2M_{path} \tag{9}$$

Inductance, $L_{above,decap}$, is a solution of the circuit in Figure 12 c. and is calculated as:

$$L_{above,decap} = \frac{L^2 - LM - M^2}{2L + M} \tag{10}$$

Fifteen partial self-and mutual inductances must be calculated to estimate the model shown in Figure 12a. Equations for these elements can be in [22] (equations C.8, C.15, C.26, C.36, C.40). Values for these elements for the geometry studied here are shown in Table 2.

Table 2. Circuit inductances in pH for simplified circuit in Figure 16 a.

$L_{p,via}$	$L_{p,pad}$	$L_{p,pin}$	$L_{p,Zter.}$	$L_{p,Xter.}$
14.13	10.00	4.66	40.34	13.92

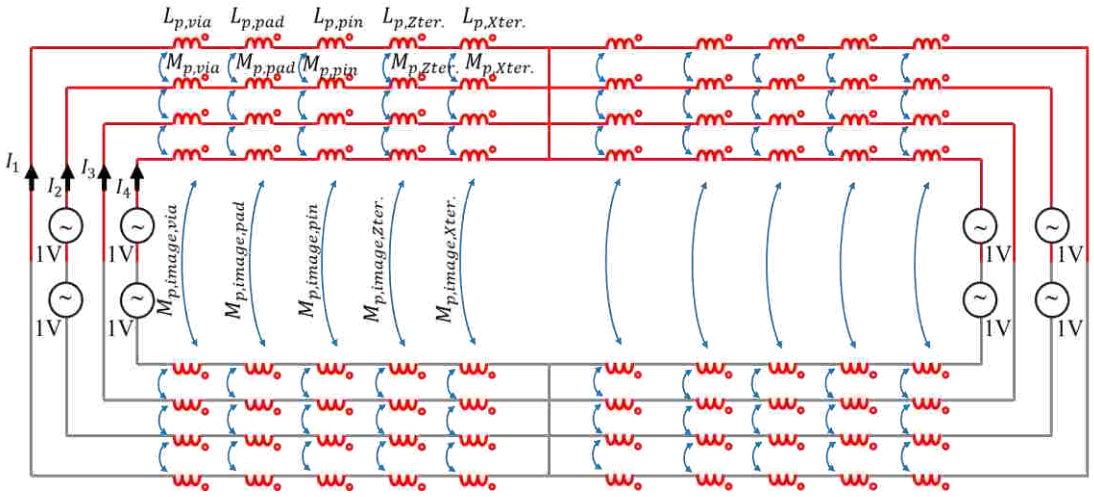
$M_{p,via}$	$M_{p,pad}$	$M_{p,pin}$	$M_{p,Zter.}$	$M_{p,Xter.}$
0.18	1.41	0.57	11.62	4.97

$M_{p,image,via}$	$M_{p,image,pad}$	$M_{p,image,pin}$	$M_{p,image,Zter.}$	$M_{p,image,Xter.}$
4.59	2.76	0.91	8.91	2.77

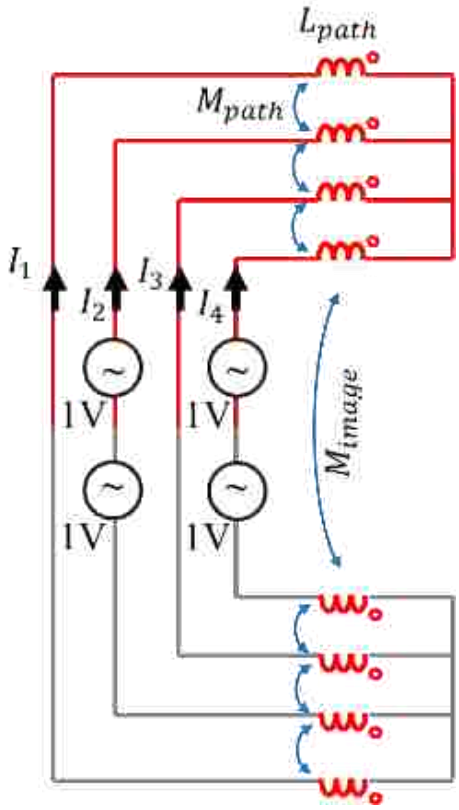
According to the values listed in Table 2 $L_{above,decap}$ is calculated using (10) and is equal to 31.4 pH. In Table 1, a simplified inductance circuit solution is compared with a complex PEEC circuit solution without ignoring the capacitor's body and mutual terms between far neighboring elements. The difference between complex and simplified PEEC solutions is 0.6 pH as shown in Table 1. This difference is so small, in part because the inductance of the mesh representing the capacitor body only contributes about 0.6 pH to overall inductance.

4. CONNECTIONS TO THE CAPACITORS

So far, we considered the modeling of the capacitor which we call $L_{above,decap}$. An important part of the design are the connections to the capacitor in the IC environment to determine the total $L_{above,decap}$ for the 8-terminal capacitor.



(a)



(b)

Figure 12. (a) Simplified inductance circuit including partial self-inductance of the vias, pads, pins, and protruding terminal of the capacitor electrodes and partial mutual inductances between the neighboring elements; (b) Left side of the circuit, which is symmetrical to the right side of the circuit in (a).

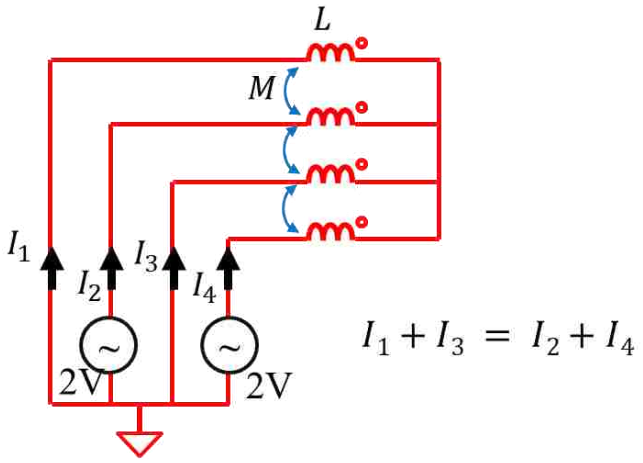


Figure 13. A simplified circuit to solve for $L_{above,cap}$ inductance.

In this section, design curves for determining $L_{above,decap}$ values for different contact situations are shown. Importantly, the distance between pads and ground plane is changing for different PCB designs as shown in Figure 14. The distance between the pads and the closest electrode also varies due to capacitor manufacturing details or the mounting processes. The distance between ground to pads (H), and distance from the pads to the closest internal capacitor plate (h) are shown in Figure 14. Dependence of $L_{above,decap}$ on H and h parameters are shown in Figure 15a and b, respectively. According to Figure 15 $L_{above,decap}$ value will not exceed 78 pH if the dielectric thickness of the first layer of the PCB is less than 10 mil.

Further, the total inductance, $L_{above,decap}$, is impacted by the design of the via connections. Intuitively, the closer the vias are to the capacitor electrodes the smaller the inductance will be. In Figure 16a, the dependence of $L_{above,decap}$ on the via locations is shown. The distance, D, between the via and capacitor terminals is varied from 2.77 mil to 12.77 mil as shown in Figure 17a.

As an example, we investigated the impact if the entire capacitor is not centered on the contacts as shown in Figure 16b. During the soldering process, a mounted capacitor might be shifted by S mils where the capacitors location is indicated by the dashed line in Figure 16b. The full-wave model of the model shown in Figure 8a was used to find the impact of the small shift on the $L_{above,decap}$ inductance. The results are as shown in Figure 17b.

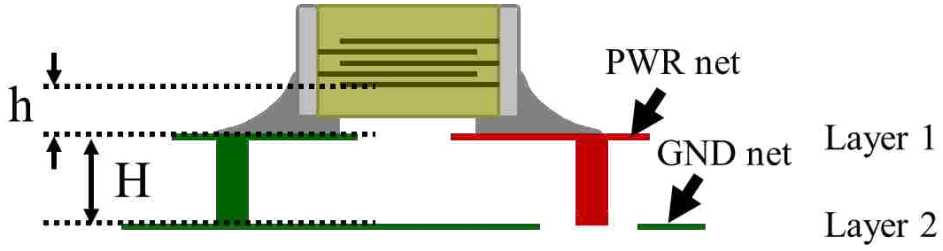


Figure 14. The geometry of the mounted 8-terminal capacitor. The distance between ground plane and the pad is H and the distance between pad and the closest capacitor's electrode is h.

Unfortunately, it is generally not well understood how much the strong mutual inductive coupling under the capacitor impacts the final result of total inductance. These couplings are a key for the low inductance value for the 8-terminal capacitor. Asymmetry can be introduced by shifting even one of the via connections. For example, the via connecting to the pin 3 was moved by 6.7 mils as shown in Figure 18a. The asymmetry introduced by moving this one via increased the $L_{above,decap}$ value by 3.9 pH (11.1%). Assuming the worst-case scenario, all vias could be shifted as is shown in Figure 18b. Again, the model shown in Figure 8 was selected to start with. The equivalent inductance values, $L_{above,decap}$, were modeled for five different randomly

placed vias. We found that the total inductance showed a large variation between 32 pH and 42 pH.

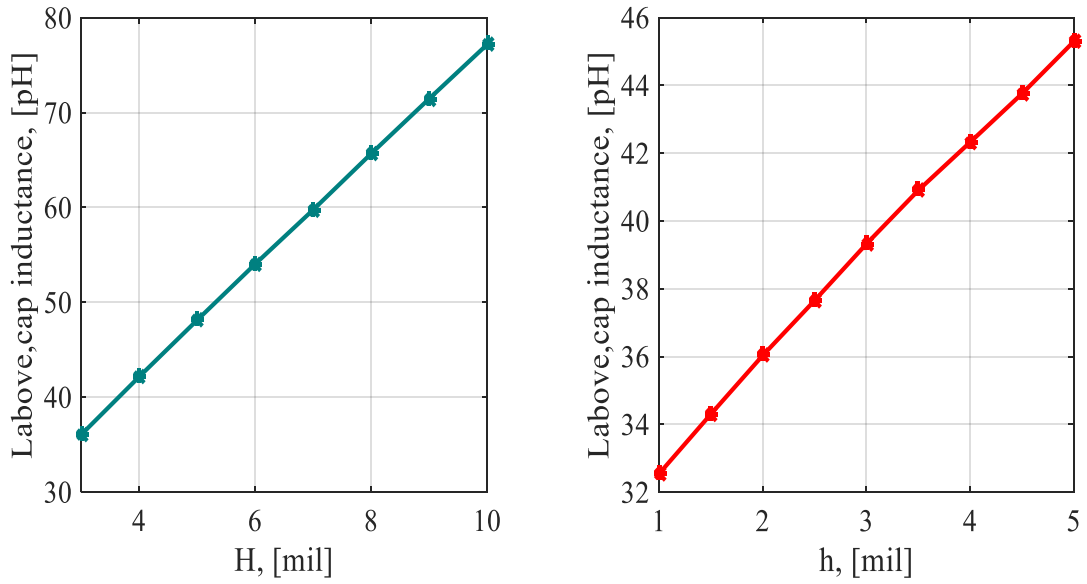
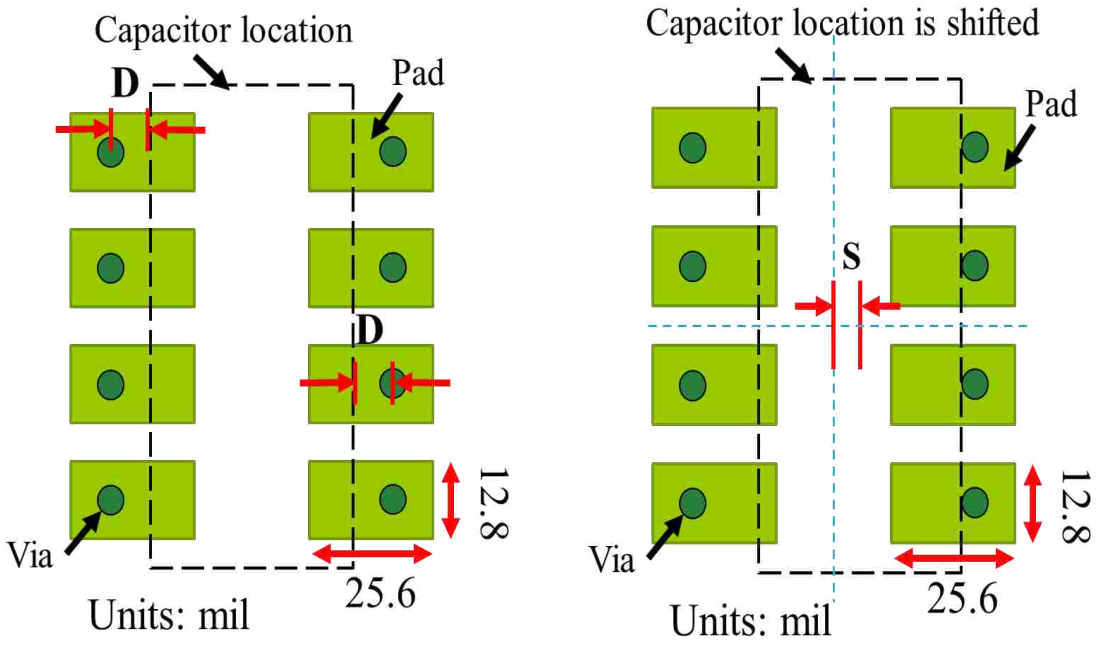


Figure 15. (a) Inductance dependence on the height, H, between the ground plane and pads, when h = 2 mil; (b) inductance dependence on the height, h, between the pads and capacitor's closest electrode, when H = 3 mil.

The result of this study shows that the low inductance value for the 8-terminal capacitor depends on several important factors. Of course, the distance of the capacitor plates to the ground plane and pads should be as small as possible. A more surprising result is that the alignment of the different locations of the via connections also has a strong influence.

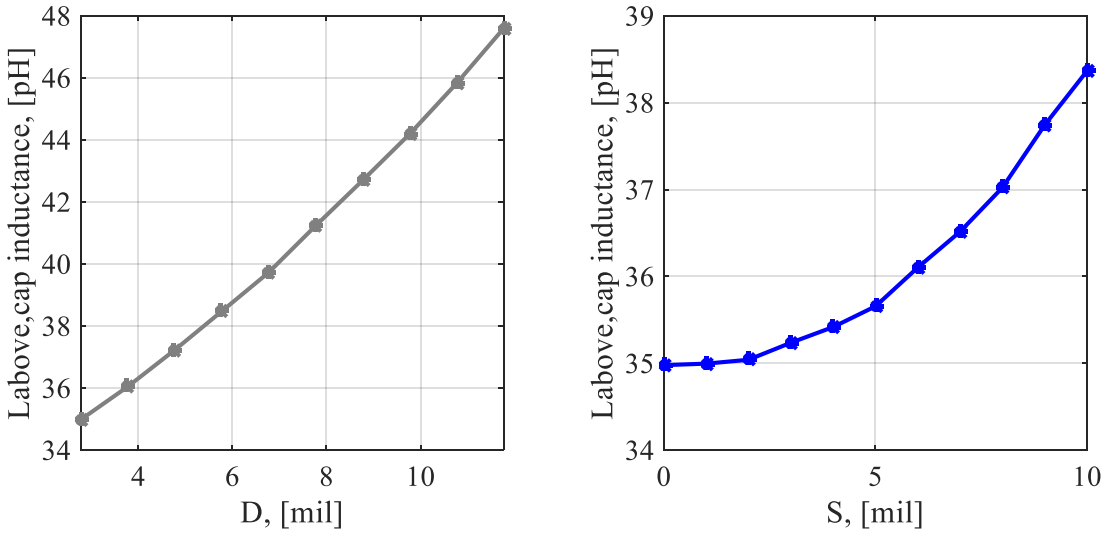
As a final study, we consider the case where the capacitor is directly mounted on the ground and power pads. This reduces the distance H = 0 as shown in Figure 14. An

example of such a design is shown in Figure 19a and Figure 19b. In this case, the closest distance between capacitor electrodes and the reference plane is h=1.75 mils as shown in Figure 14. To ensure that a loop created by a capacitor body and a reference plane is not coupled with the internal layers of the package, the anti-pad between the power pads and the ground plane should not exceed 3.1 mil [24]. Not surprisingly, the smallest inductance for the 8-terminal capacitor design shown in Figure 19b was calculated to be 21.5 pH. Importantly, we also give the inductance matrix for this case. As expected, the values for this case in Figure 19c are smaller for this direct connection in comparison the conventional connections shown in Figure 7.



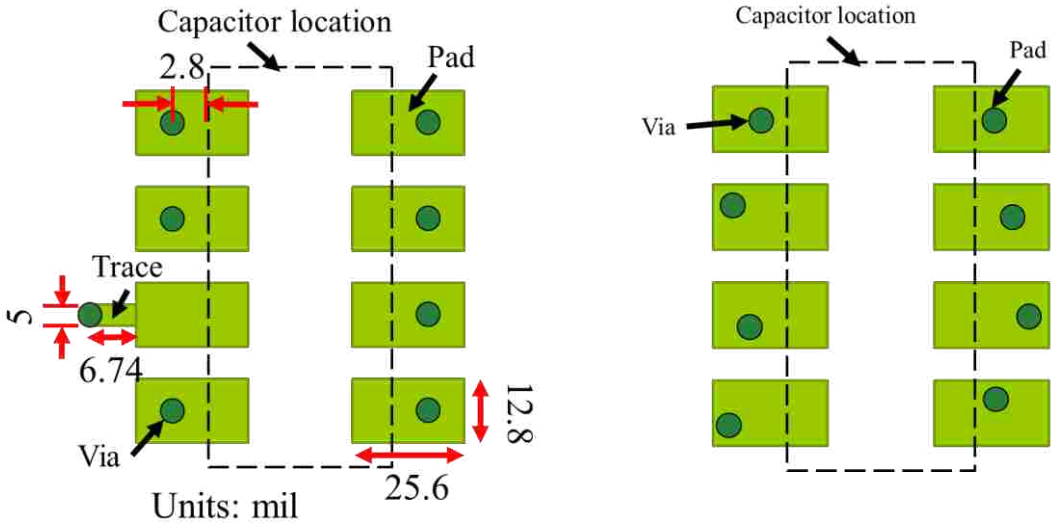
(a) (b)

Figure 16. (a) Distance, D, between center of the vias and the capacitor's terminal; (b) Mounted capacitor shifted by S distance from its footprint center.



(a) (b)

Figure 17. Effect of (a) shifting vias by D distance away from the capacitor body D; (b) shifting capacitor by S distance from the center of its footprint on the $L_{above,decap}$, when h = 1.75 mil, and H = 3 mil.



(a) (b)

Figure 18. (a) Asymmetrical layout with an additional trace connecting via and pad; (b) vias connecting pads to the planes are randomly placed, which creates an asymmetrical distribution.

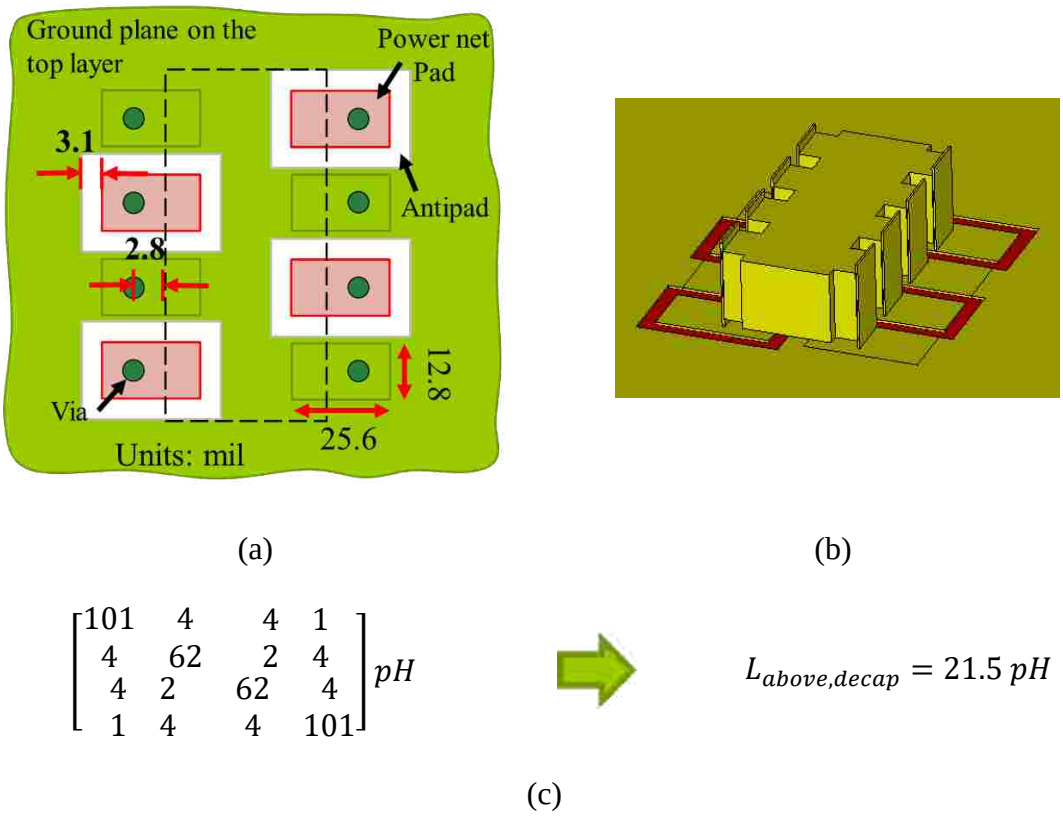


Figure 19. (a) Footprint and; (b) 3D model of the layout design with a ground plane placed on the first layer of the package or PCB.

5. CONCLUSION

The equivalent inductance associated with the 8-terminal decoupling capacitor mounted on the package or PCB is analyzed in this work. We found that the 8-terminal capacitor for practical applications should be characterized using a four-by-four inductance matrix instead of a single-value inductance suitable for practical applications in the complete package or PCB environment. Usually, a single-value inductance is given based on an assumption that the voltages at all ports are the same, or that the inductance

between the connections below the plane is zero. These inductances must be taken into account to get the inductance of the mounted capacitors.

We found that sufficiently accurate models can be found for the inductance computation if we replace the capacitor plates with a conductor block that is modeled with a multi-terminal PEEC model. CST full-wave models were used to validate the circuit models. We found for the 8-terminal capacitor model the circuit model was approximately within 9% of the CST muti-layer model.

We further considered the important issues in the tolerances and different connection arrangements to study its impact on the inductance. The results show that the distance to the return plane has the most impact. The total inductance of a mounted 8-terminal capacitor varies between 30 pH and 50 pH if dielectric thickness of the first layer of package is between 3 mils and 5 mils. Using shifted via positions of the pads can change inductance as much as 10 pH.

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III. DETERMINING EQUIVALENT MATERIAL PROPERTIES FOR SHIELDING EFFECTIVENESS BASED ON A LOW FREQUENCY DUAL-LOOP METHOD

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ABSTRACT

Shielding the victim or isolating the noise source can suppress electromagnetic interference between devices or systems. Selecting an appropriate material and shielding structure is challenging. Numerical simulation can be used to evaluate shielding performance. Often though, material properties, such as conductivity and permeability are unknown. Accurate representation of material properties is essential for modeling and simulation of shielding effectiveness, especially for low-frequency magnetic field shielding. This work details the process of obtaining equivalent material properties of an uniform material sheet. Material conductivity was measured using the van der Pauw method. The obtained conductivities of materials were within % of the tabulated values. Air-core dual-coil approach is proposed to measure shielding of various material sheets. Permeability of a material was fitted to match measured and simulated shielding. The fitted permeability values were within % of the tabulated values provided by manufacturers. The equivalent material properties were used to estimate the shielding effectiveness of different materials according to MIL-STD-188-125.

1. INTRODUCTION

Electromagnetic interference between a noise and a victim is undesirable [1]. Shielding a device from the electromagnetic interference is a common practice to increase the immunity to the surrounding electromagnetic noise.

Shielding enclosures protect electronic devices against external interference and can mitigate electromagnetic interference from noise sources [1]. The shielding effectiveness is a figure of merit to compare and characterize performances of the shield and shielding materials [2]. Shielding effectiveness is defined as the ratio of the field at the point that is intended to be shielded, in the absence and presence of the shield [2]. Shielding for electric and magnetic fields is not necessarily the same. Thus, electric- and magnetic-field shielding effectiveness are defined and measured independently [3]. Electric-field shielding effectiveness [4] is a ratio of the magnitude of the incident electric field without the shield, to the magnitude of the transmitted electric field through the shield as

$$SE_{E,dB} = 20\log_{10}\left|\frac{\vec{E}_i}{\vec{E}_t}\right| \tag{1}$$

Similarly, magnetic shielding effectiveness [4] is calculated as

$$SE_{E,dB} = 20\log_{10}\left|\frac{\vec{E}_i}{\vec{E}_t}\right| \tag{2}$$

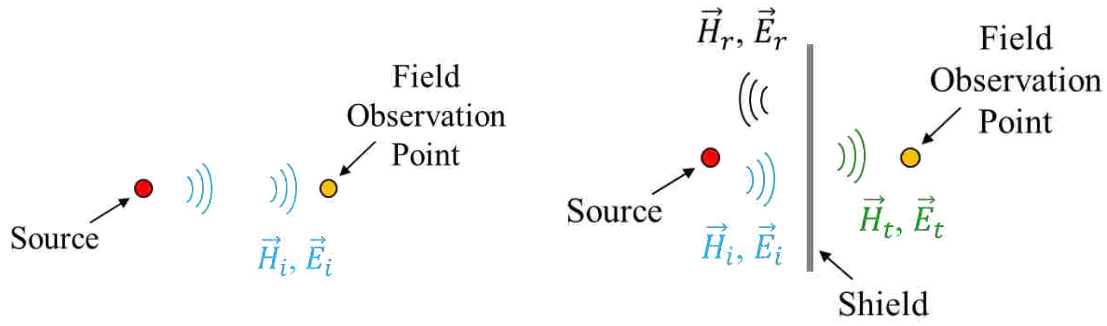
where $SE_{E,dB}$ and $SE_{E,dB}$ are the electric- and magnetic-field shielding effectiveness, respectively. $\vec{E}_i$ and $\vec{E}_t$ are the electric fields in the absence and presence of the shield, respectively. $\vec{H}_i$ and $\vec{H}_t$ are the magnetic fields in the absence and presence of the shield,

respectively as shown in Figure 1. Shielding effectiveness, $SE_{E,dB}$ and $SE_{E,dB}$, are usually expressed in decibels (dB) [4].

Shielding of equipment can be required over a wide frequency range from a few hertz, up to a few tens of gigahertz, depending on functioning frequencies of the noise source and victim [5]. Different aspects of the shielding are important depending on the frequency. At high frequencies (a few tens of megahertz and above), the enclosure shielding is mainly determined by the material conductivity and a geometry. Conductive metals easily achieve a high level of shielding at high frequencies [6]. However, openings in the enclosure can compromise the shielding effectiveness when apertures and penetrations are no longer electrically small. Magnetic-field shielding is an effective shielding mechanism against low-frequency external fields. As frequency increases, shielding is provided by eddy currents induced by the external field. The eddy currents produce a magnetic-field that opposes the external field. Below a few tens of kilohertz, the permeability of the material is essential [2]. Ferromagnetic materials have higher shielding effectiveness than pure metals at very low frequencies below few kilohertz [2]. This paper is focused on a frequency range of a few tens to hundreds of kilohertz, where conductivity and permeability are both contributors to the shieling effectiveness of a material.

The shielding effectiveness of a material sheet is influenced by the skin depth (thickness, frequency, permeability, conductivity) [6]. Conductivity and permeability are critical parameters for shielding characterization. Known material properties can be used in simulations, which helps in making design decisions. Simulation tools or analytical

formulations are very useful when evaluating different materials and their performances [3], [4].



(a) (b)

Figure 1. Shielding effectiveness with and without shield.

Various research had been conducted to evaluate shielding effectiveness based on analytical and numerical methods [1]. The closed-form expressions are mainly applied to structures with geometries that conform to separable coordinate systems so as to enable an analytical solution [5], [7], [8], [9]. However, powerful numerical methods and commercial simulation tools allow the shielding effectiveness of complicated structures to be assessed. Numerical approaches can be categorized into time-domain and frequency-domain methods [1]. Time domain methods such as the finite-difference time-domain (FDTD) [10], and transmission-line matrix [3] methods are suitable for wideband analysis. Frequency-domain methods are more accurate and suitable for narrowband analysis. The finite element method [11], [12] and method of moments [13] are the most commonly used frequency-domain methods for estimation of shielding effectiveness [2].

Numerical and analytical methods can be accurate and suitable to estimate shielding effectiveness; however, the solution depends on the material properties. Inaccurate material properties result in discrepancies between simulation and measurements. The material conductivity and permeability may not always be known. In [14] analytical procedure is developed to directly calculate the first-order Debye model parameters of the materials based on the shielding requirements. Although Debye models do not apply magnetic materials. In this paper, a procedure to determine material properties is proposed. An equivalent material property could be further used in numerical simulations.

Here, a methodology is proposed to develop equivalent material properties. Conductivity is measured according to the van der Pauw method [15], [16], and permeability is fitted to match measured and simulated shielding. To measure shielding of the materials simple air-core dual-coil setup was developed. Materials are required to be homogeneous in thickness and dimensions should be at least 15 cm by 15 cm to avoid edge effects. The procedure is applicable at kilohertz frequency range. Material properties further could be used in simulation, with different geometrical structures. The equivalent material property models can be obtained for single-layer fabric or solid, metal or magnetic materials.

2. SHIELDING MEASUREMENT

Measuring shielding-effectiveness can be challenging. Measured shielding is sensitive to the measurement setup, such as transmitter and receiver devices and their

placement, as well as material dimensions [5]. Standards define measurement test setup requirements to evaluate materials' shielding properties in a consistent and controlled environment.

2.1. STANDARDS

ASTM E1851 Standard [17] standard defines a procedure to measure shielding effectiveness of a large enclosure using two loop antennas (140 KHz - 500 MHz). An oscillator and spectrum analyzer are used to excite one antenna and record received power on the other antenna, respectively. Power and pre-amplifiers are required to increase the dynamic range of the measurement. The intended application of this test method is to define shielding properties of non-ideal enclosures to identify the potential points where the shielding room may be compromised in the process of assembly and at penetrations.

IEEE Std. 299-2006 [18] standard defines requirements to measure the effectiveness of electromagnetic shielding enclosures or planar sheets. The magnetic field is generated by a current in a loop antenna. A signal generator and amplifier are used to supply the loop current. The receiver loop is connected to a spectrum analyzer. Transmitting and receiving loops spaced by 30 cm should be placed perpendicularly to the material surface. Standard low-frequency measurements (9 kHz to 20 MHz) evaluate material performance when exposed to a near-field magnetic source. Measurement dynamic range and sensitivity depend on antenna type and distance from the shield sample.

Military Standard MIL-STD-188-125 [19] is like IEEE Std. 299, with small modifications to dimensions, distances, and frequency range. Similarly, this standard setup can be used to measure magnetic shielding effectiveness for the near excitation and observation points.

2.2. AIR-CORE DUAL-COIL MEASUREMENT SETUP

A simple shielding measurement setup is proposed in this paper to characterize material properties of a sheet materials. The proposed measurement setup is an air-core dual-coil (dual-loop) method. A dual-loop method is suitable for low-frequency magnetic-field shielding measurements. The air-core loops were constructed for the shielding measurements to achieve a dynamic range at least 85 dB at 10 kHz. Copper wire with a 10 mil diameter was wound around a non-conducting/non-magnetic cylinder of 25.4 mm diameter and 32 mm length. The length between the end of the wire turns and the cylinder end was 14 mm. Sixty-two turns of the 10 mil wire were wound on the air-core loops, and the wire connected to a Bayonet Neill-Concelman (BNC) connector. Air-core loops were used for magnetic field shielding evaluation as shown in Figure 2.

The air-core dual-loop test configuration is shown in Figure 3. A gap was left between the loops to accommodate the thickness of the materials under test. The gap between the air-core loops is 3.5 cm. The loops were mounted in a stand that was 76 mm above the table surface to allow a sample with a dimension of 15 cm by 15 cm to avoid the edge effects.

The test setup including the test instrument and the air-core loops with a material sample is shown in Figure 4. A Rohde-Schwarz FSV30 spectrum analyzer with a tracking

generator was used for the testing. The output power of the tracking generator was set to 0 dBm. The frequency range of the testing was 10 kHz - 200 kHz, and the resolution bandwidth was set at 100 Hz.

Receiving and transmitting loops were placed so that edge-to-edge loop distance was 3.5 cm. The received power P_i was recorded as a reference measurement. The transmitting and receiving antennas were placed in the open space, away from any scatterers. The air-core dual-loop setup with no material in between the loops is shown in Figure 3. Corresponding test results are also shown in Figure 5 together with the lowest measurable signal (measurement noise floor) for given setup, when 32 mil thick aluminum was placed in between the loops. Figure 5 shows that the proposed test configuration provides at least 85 dB dynamic range to determine shielding of the samples.

Locations of receiving and transmitting antennas remained the same, and test shield material sheet was placed in between the loops. The sample can be located anywhere in between the loops as long as the distance between the loops is unchanged [7]. The setup with test material and a spectrum analyzer is shown in Figure 4. The received power P_t was recorded.

The ratio of the test measurement to the reference measurement is the magnetic shielding of the sample material at a specified frequency and at source/observation point locations. The logarithm of this ratio expresses the shielding in decibels as

$$Shield_{H,dB} = 20\log_{10}\left|\frac{P_i}{P_t}\right|_{E,dB} \quad (3)$$

Power measured with and without sample in between the loops includes cable losses and antenna factors, but those losses are eliminated in shielding calculations due two ratio of the powers.

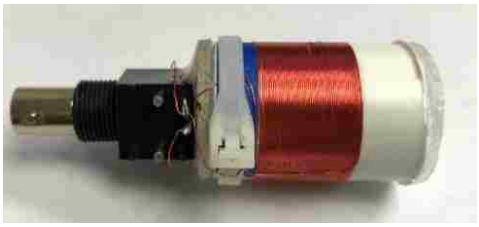


Figure 2. Air-core loop used in magnetic field shielding testing.

Figure 3. Air-core dual-loop magnetic field shielding test setup showing the air gap between the two loops used in the testing

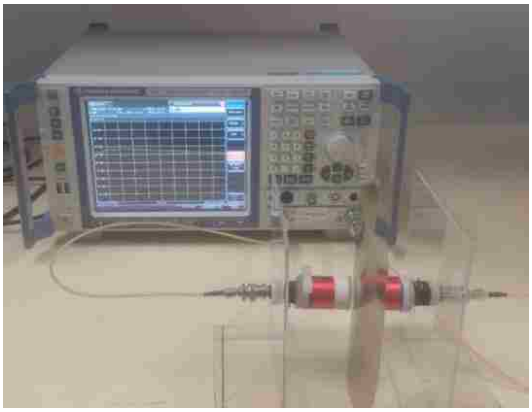


Figure 4. The spectrum analyzer with tracking generator connected to the dual-loop apparatus with a sample material between the loops.

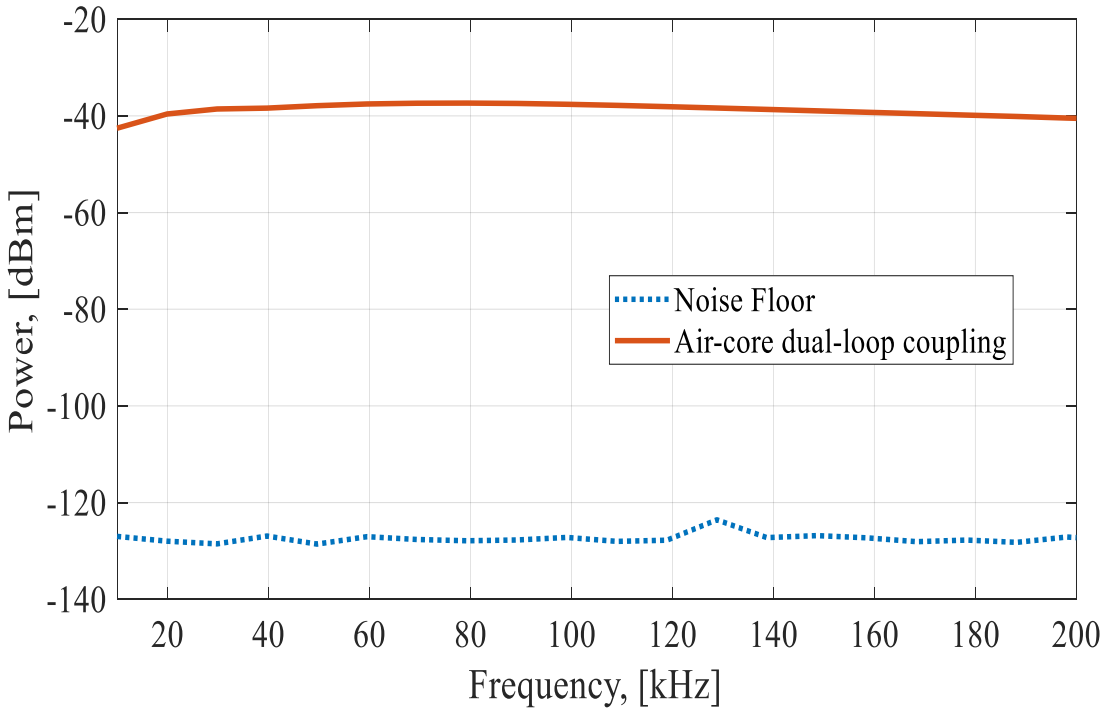
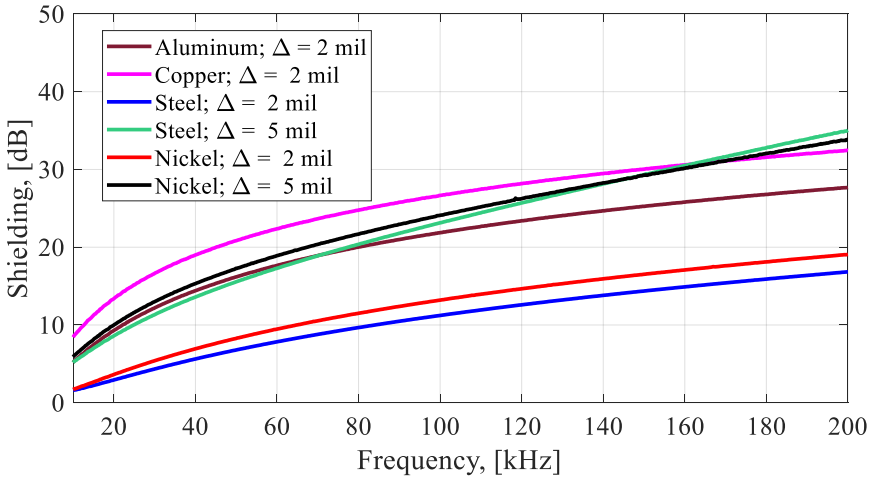


Figure 5. Dynamic range of the test setup.

2.3. MATERIALS

Thin sheets of copper, aluminum, nickel, and steel were selected to be evaluated in this paper. Properties of materials with trade names, Mu-Metal and Mu-Copper, were investigated as well. Mu-Metal is a nickel-iron soft ferromagnetic alloy with a high permeability. Mu-Copper is a nickel copper alloy. Laird 3027-532C is a fabric material. Its base layer is a metallized non-woven fabric plated with conductive copper and nickel for corrosion resistance. This is bonded to a thin layer of solid aluminum. A set of test materials is identified in Table 1. Each sample was tested according to the procedure described in Section 2.2. The measured shielding of the samples is shown in Figure 6.



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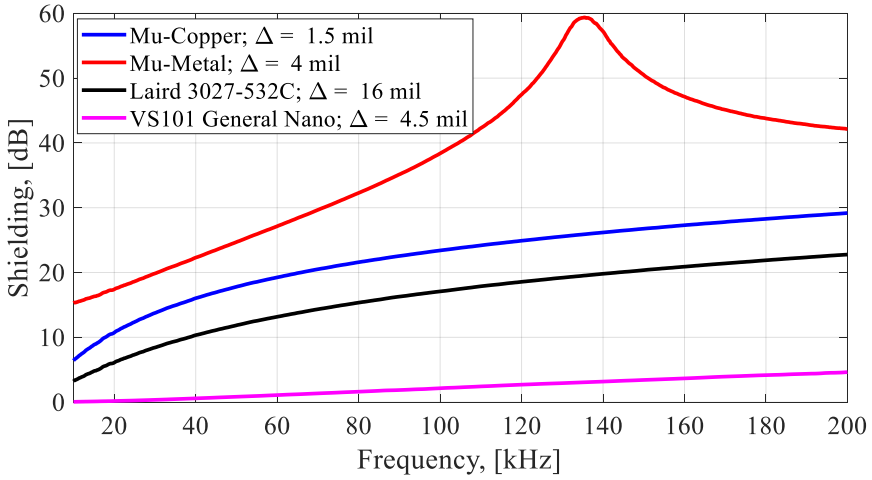


(b)

Figure 6. Shielding effectiveness of the materials identified in Table 1 using the air-core loops for frequency range from 10 kHz – 200 kHz.

3. CONDUCTIVITY MEASUREMENT

The van der Pauw method was used to measure electrical resistivity, which is the inverse of conductivity, the [15], [16]. This test method requires the sample to be free

from holes and be homogeneous in thickness, but can be arbitrary in shape. Figure 7a represents the concept of the method. Current is applied between two points of the sample, and voltage is measured for one of eight different testing permutations as required for the full van der Pauw method. These permutations allow for the evaluation of resistivity regardless of the sample shape and electrical contact positioning [16].

Two values of resistivity, ρ_A and ρ_B, are calculated as

$$\rho_A = \frac{1.1331 f_A t}{I}\left(V_{21,34} - V_{12,34} + V_{32,41} - V_{23,41}\right) \quad \Omega\cdot\text{cm} \tag{4}$$

$$\rho_B = \frac{1.1331 f_B t}{I}\left(V_{43,12} - V_{34,12} + V_{14,23} - V_{41,23}\right) \quad \Omega\cdot\text{cm} \tag{5}$$

where $V_{\text{ab,cb}}$ is voltage drop across the sample under a given current I for each permutation. The subscripts denote the positioning of the positive current terminal (a), negative current terminal (b), positive voltage terminal (c), and negative voltage terminal (d) on the numbered positions for the sample in Figure 7a [14], [16]. The voltages are given in volts, the specimen thickness, *t*, is in centimeters, and the current magnitude, *I*, is in amperes. The parameters f_A and f_B are an empirically derived shape factor f that can be solved as

$$\frac{Q-1}{Q+1} = \frac{f}{0.693}\operatorname{arcosh}\left(\frac{1}{2}e^{\frac{0.693}{f}}\right) \tag{6}$$

$$Q_A = \frac{V_{21,34} - V_{12,34}}{V_{32,41} - V_{23,41}} \tag{7}$$

$$Q_B = \frac{V_{43,12} - V_{34,12}}{V_{14,23} - V_{41,23}} \tag{8}$$

The average of ρ_A and ρ_B can then be calculated, giving a single resistivity ρ. A material is considered uniform and homogenous if ρ_A and ρ_B are within 10% [15]. The

preferred location for the terminal contacts is on the sample edge [16]. The conductivity σ in S/cm of the sample is the inverse of resistivity ρ as

$$\sigma = \frac{1}{\rho} \tag{9}$$

The conductivity for the materials from the Table 1 were tested as shown in Figure 7b. Conductivities for each material sample are listed in Table 1. Measured conductivity values were compared with tabulated values of the materials [3], [4], [20]. Expected and measured values of commonly-used materials were within 3%. Repeatability of the measurement is not more than 5%.

Table 1. Equivalent material properties.

Material	Thickness, [mil]	Conductivity $\times 10^6$, [S/m]	Permeability
Aluminum	2	34.7	1
Copper	2	58.6	1
1010 Steel	2	7.5	115
Steel	4	7.3	115
Nickel	2	10.5	40
Nickel	5	12.4	40
Mu-Copper	1.5	54.7	1
Mu-Metal	4	1.6	$\mu(f)^*$
Laird 3027-532C	16	2.5	1
VS101 General Nano	4.5	0.7	1

(a) (b)

Figure 7. Test setup (a) schematic [15] and (b) sample under test for conductivity measurements.

4. MATERIAL PROPERTIES

Simulations were used to reproduce measured shielding demonstrated in Section 2.3. The simulation configuration is shown in Figure 8 for the parallel air-core loop antenna polarization.

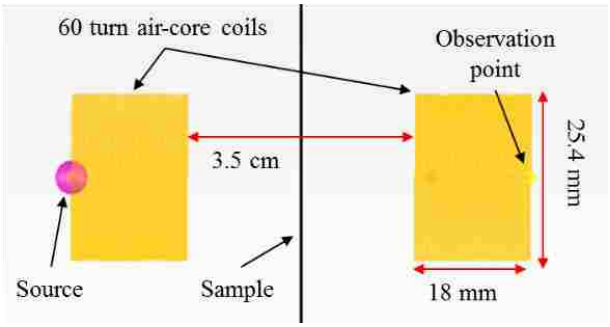
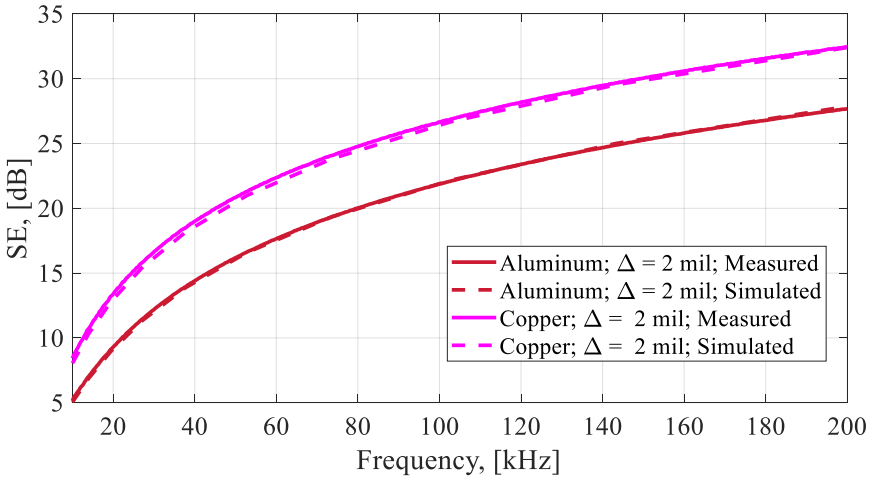


Figure 8. Simulation configuration according to measurement setup.

EMCoS Studio [21] was used to perform low-frequency magnetic field calculations. Conductivities of the material from Table 2 were used. Permeabilities were

swept to match with measurements. Figure 9 shows a comparison of measured and simulated shielding for each material. Approximated permeabilities of the test samples are listed in Table 2. As expected, permeability of the pure metals (aluminum, copper) is found to be one.



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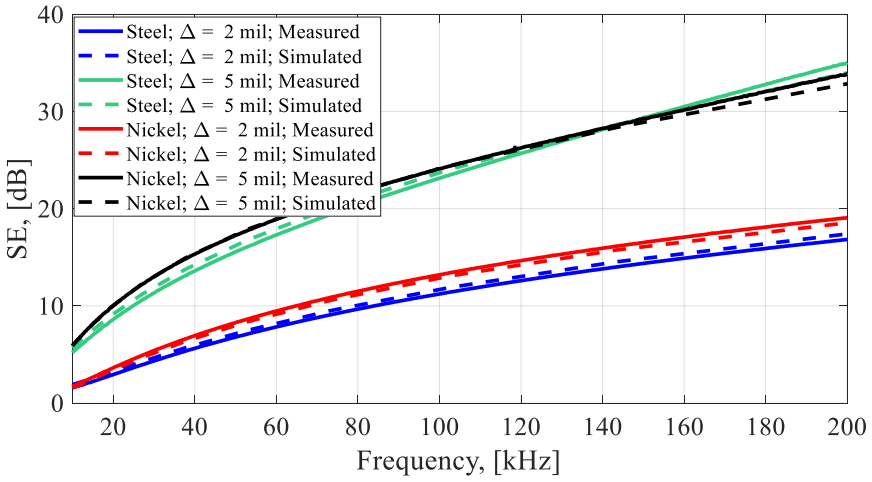

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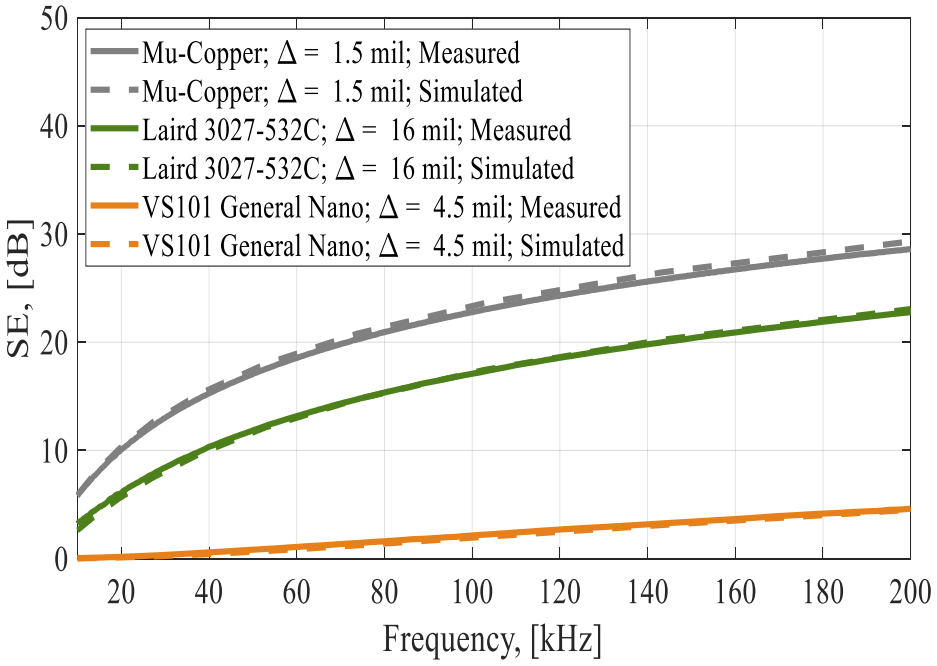
Figure 9. Comparison of simulated and measured shielding.



(c)

Figure 9. Comparison of simulated and measured shielding. (cont.)

Mu-metal is a soft ferromagnetic alloy. It has very high initial and maximum permeability with nominal hysteresis loss. High permeability mu-metal offers a low reluctance path for magnetic flux that provides high magnetic shielding at low frequencies. Permeability of the mu-metals are strongly dependent on the frequencies of the external fields in the frequency range studied here. On the other hand, conductivity of the mu-material can be approximated as constant value and measured according to van der Pauw method in Section 3. Permeability values of the mu-metal are fitted at the different frequency points. Frequency-dependent permeability of the mu-metal is shown in Figure 10. Simulated shielding of the mu-metal with the properties defined in Table 1 and Figure 10 is compared with measured shielding and shown in Figure 11.

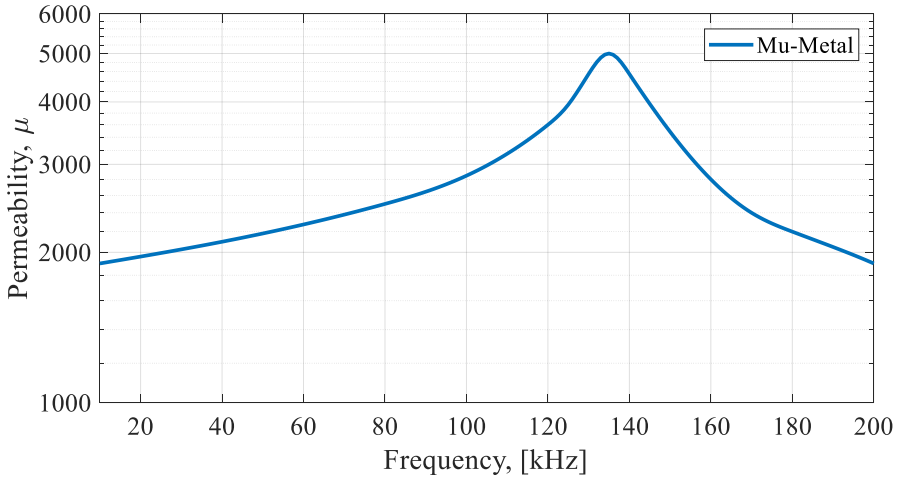


Figure 10. Frequency dependence of the mu-material permeability.

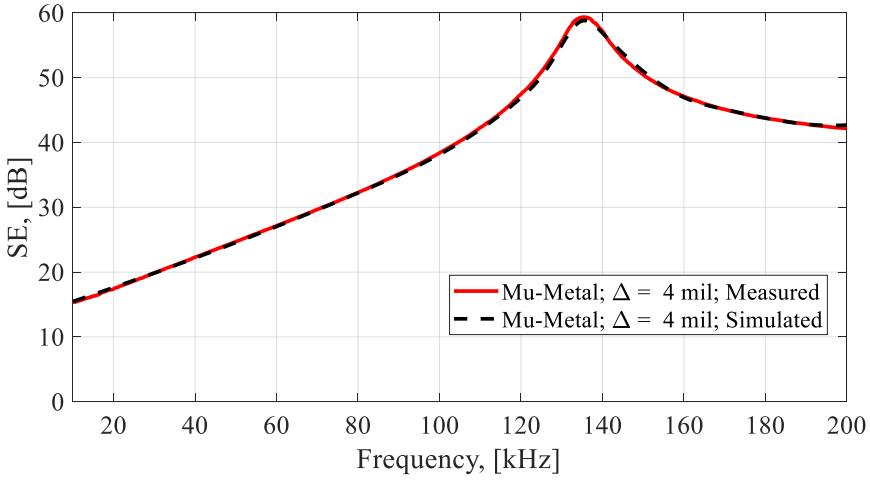


Figure 11. Measured and simulated shielding of the mu-metal.

To model shielding accurately, material dimensions, thickness, conductivity, and permeability are required to be known. Curve-fitted conductivity and permeability might match simulated and measured shielding of the material for the selected setup. In other words, there are multiple combinations of material properties that could fit the measured curve, but fitting does not guarantee accuracy when measurement conditions are changed.

An advantage of the proposed strategy is that conductivity is measured and fixed, which allows curve-fitting only permeability.

In order to check the validity of the obtained material properties, measurement and simulations setups were modified. Double sheets of the material samples with a 1 in. separation are placed in between air-core dual-loops, where they were separated by 5.5 cm. A modified setup is shown in Figure 12, and corresponding shielding results are shown in Figure 13. This indicates that equivalent material properties are realistic and further could be used in simulations to predict shielding effectiveness according to MIL-STD-188-125-2.

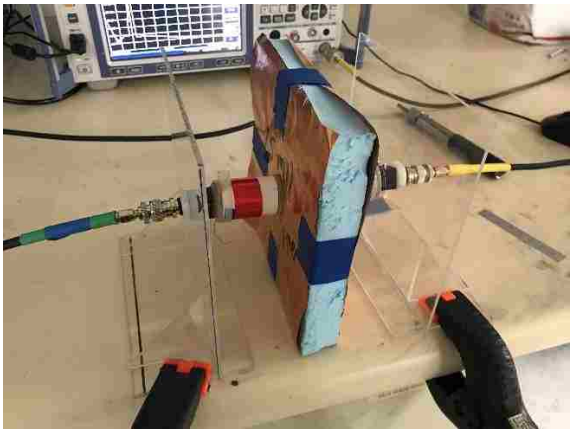


Figure 12. Double sheets of the material samples with a 1 in. separation are placed in between air-core dual-loops.

Edge effects due to electrically small length and width of the 6 in. by 6 in. mu-copper is observed in Figure 13. At 80 kHz shielding of the 6x6 in. mu-copper starts to decrease, because fields are leaked around the edges of the sample sheets. Figure 13 demonstrates a simulation of what shielding would look like if mu-copper samples were

infinitely large. Edge effects are not observed for Laid 532C material because its shielding is low, and the field leakage happens through material.

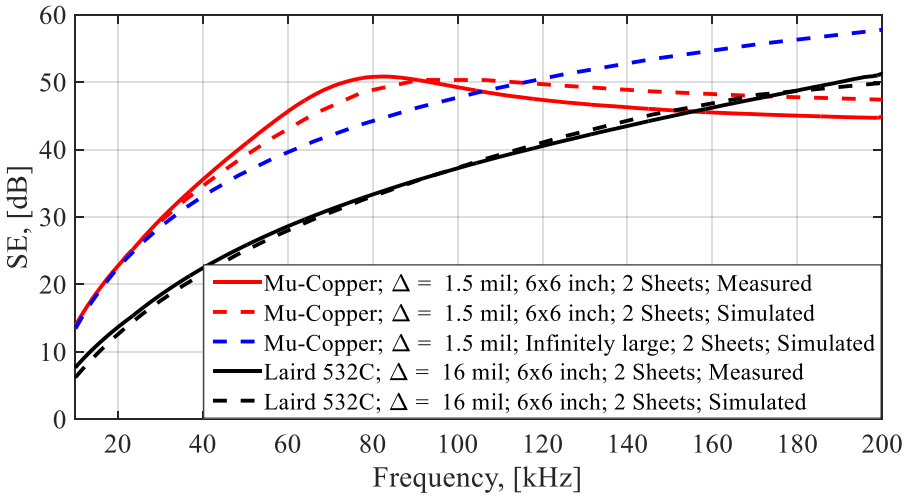


Figure 13. Comparison of simulated and measured shielding of the same two material sheets separated by 1 in..

5. SHIELDING EFFECTIVENESS

Equivalent material properties are obtained based on conductivity measurements and permeability fitting. As mentioned above, equivalent material properties can be used for evaluating shield effectiveness of materials according to MIL-STD-188-125-2. The industry standard requires systems to be shielded against high-altitude electromagnetic pulses, and the shield should provide at least the minimum shielding effectiveness as defined in (10) [19].

$$SE_{dB} = 20\log_{10} F - 60 \tag{10}$$

where F is the frequency range of the interest. In this study, F is from 10 KHz to 1 MHz.

The shield must be a continuous conductive enclosure, normally constructed of a metal such as steel, copper, or aluminum. The enclosure must be electromagnetically closed at all seams and joints between adjacent panels on all wall, ceiling, and floor surfaces [19]. Shielding effectiveness of the materials is measured according to the test configuration shown in Figure 14 [19].

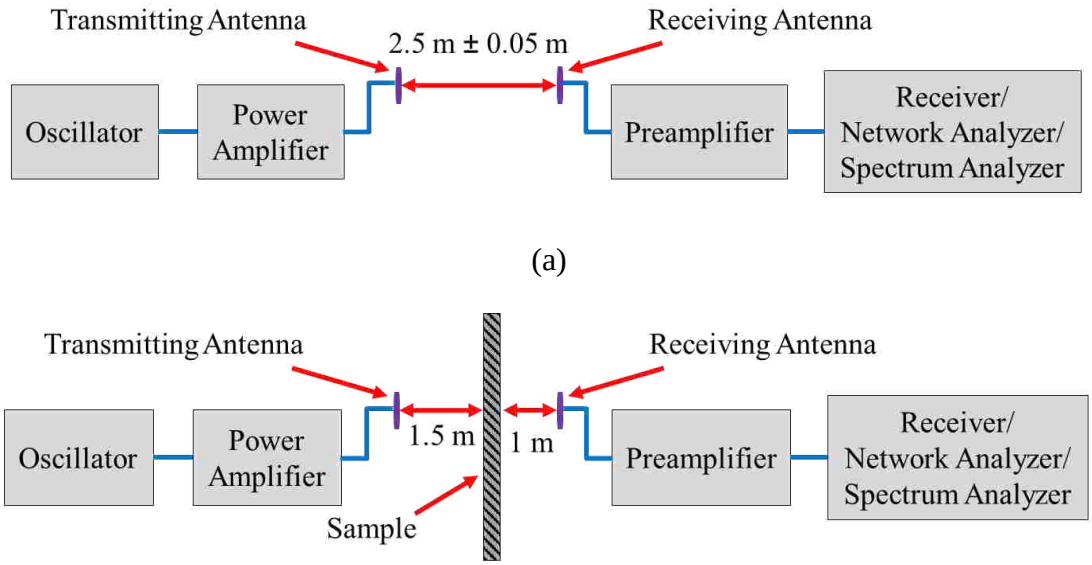
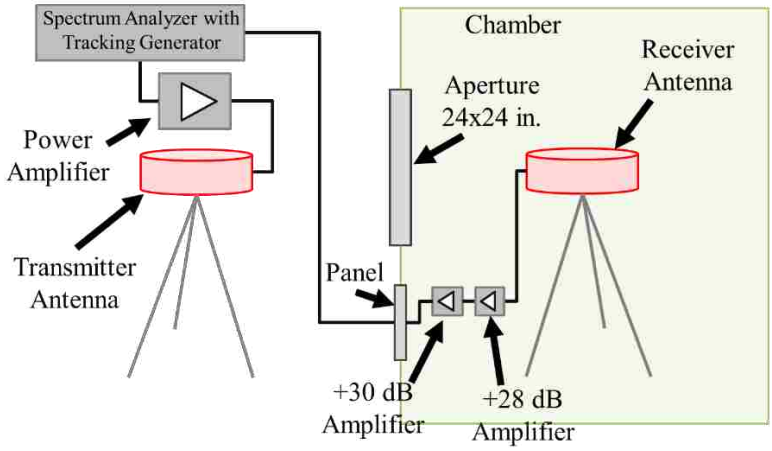


Figure 14. Shielding effectiveness (a) calibration and (b) measurement configurations according to MIL-STD-188-125-2.

Experimental setup as shown in Figure 15 was assembled to measure shielding effectiveness of the material samples according to MIL-STD-188-125-2. A transmitter antenna was placed outside a chamber and a receiver antenna was located inside the chamber [22]. The transmitter and the receiver antennas were identical 12 turn loop antennas with an 18 in. diameter. Power amplifier was used to amplify transmitted power

and two low-noise pre-amplifiers were used to amplify received power. Amplifiers are critical in this setup to obtain sufficient signal to noise ratio.



(a)

(b)

Figure 15. Schematic, and (b) pictures of the shielding effectiveness measurement setup according to MIL-STD-188-125-2.

A numerical model was constructed according to Figure 15 in EMCoS Studio as shown in Figure 16. Measured and simulated shielding effectiveness of mu-copper, Laird 532C, and aluminum were compared in Figure 17 to validate numerical solution and

material properties. According to Figure 17 measured and simulated shielding effectiveness curves agree with each other within 1.6 dB.

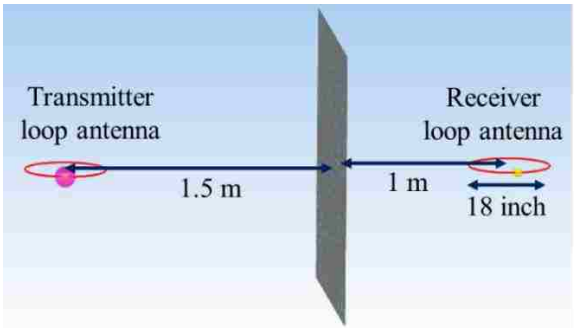


Figure 16. Shielding effectiveness simulation model according to MIL-STD-188-125-2.

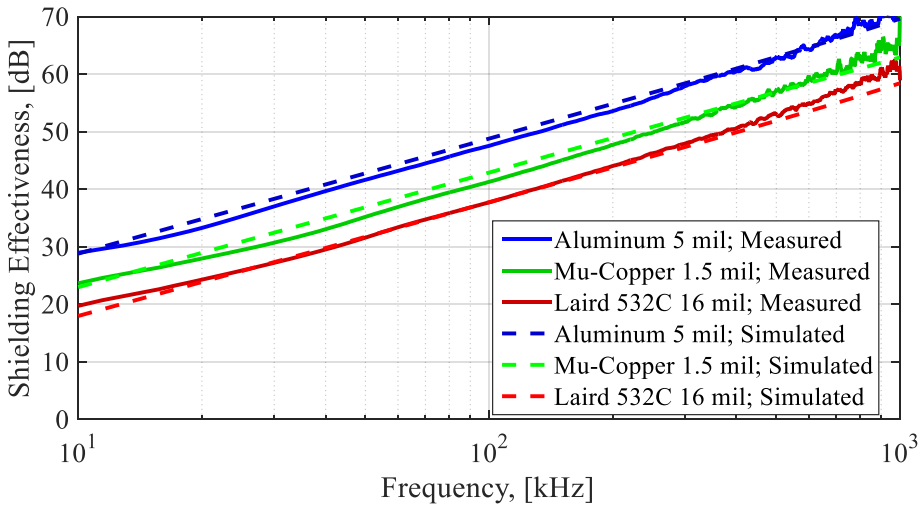


Figure 17. Measured and simulated shielding effectiveness of mu-copper, Laird 532C and aluminum.

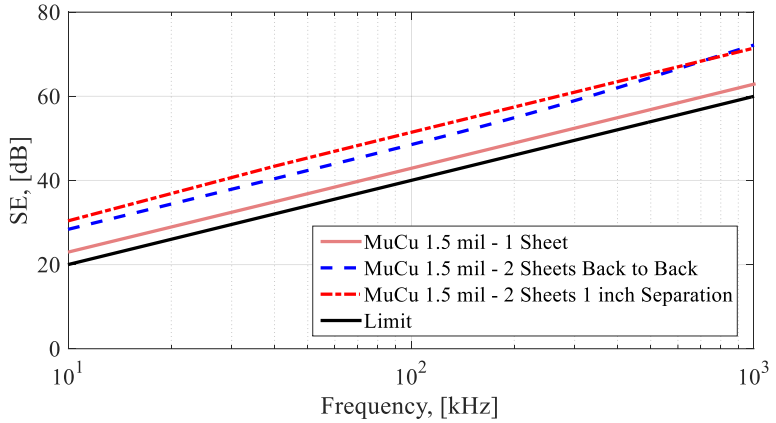
Simulations are used to determine material thicknesses which satisfies standard limit lines. Table 2 shows thicknesses of aluminum, mu-copper, and Laird 532C, in

which case shielding effectiveness is over the standard limit line by 0 dB, 6 dB, and 10 dB, respectively.

Table 2. Finding material thicknesses to satisfy standard requirements.

	0 dB over the limit	6 dB over the limit	10 dB over the limit
Aluminum	2 mil	4 mil	6 mil
Mu-Copper	1 mil	2.1 mil	3.5 mil
Laird 3027-532C	25 mil	48 mil	70 mil

Shielding effectiveness of the mu-copper and Laird 532C materials with 1.5 mil and 16 mil thickness respectively, was simulated. Figure 18 a demonstrates shielding effectiveness of a single sheet of mu-copper compared to cases where two sheets of mu-metals are separated by 1 in. or placed together. Figure 18 a shows that 1.5 mil mu-copper meets the standard requirements by about 2.8 dB. Two sheets of mu-copper could be placed back to back or separated by a distance. Figure 18 a demonstrates the benefit of using two sheets of mu-copper with a 1 in. separation. Difference in shielding effectiveness between using two sheets of mu-copper back to back or separated by 1 in. is about 3 dB below 200 KHz. Comparison between one sheet and two sheets of Laird 532C is demonstrated in Figure 18 b. One sheet of 16 mil Laird 532C fails to meet standard requirements by 2.3 dB. Shielding effectiveness of the shielding enclosure will be over a standard line by 6 dB if two sheets of Laird 532C with a 1 in. separation is used. Above 500 kHz, shielding of two sheets of material places back to back starts to dominate over two sheets of materials separated by a distance.



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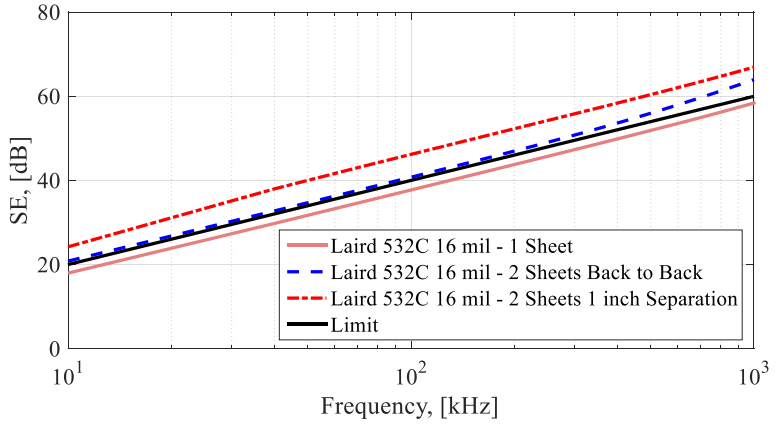

(b)

Figure 18. Shielding effectiveness (a) calibration and (b) measurement configurations according to MIL-STD-188-125-2.

It can be seen that the larger the air separation, the more effective the shield is. This is true only when the shield is electrically thin [3], [23]. When the shield is electrically thick, the two sheets with an air gap have considerably less shielding than the two sheets placed back to back. The multiple-reflection terms in shielding mechanism for two sheets consisting of the same material and of the same thickness increase by increasing the air gap between the sheets [3], [23]. Shielding is a combination of material

absorption, reflection, and multiple-reflection between the surfaces of the two mediums. Multiple-reflection loss is significant at low frequencies, where material is electrically thin, but negligible at high frequencies.

6. CONCLUSION

The methodology of obtaining equivalent material properties of magnetic or non-magnetic materials has been demonstrated in this work. The procedure is applicable at kilohertz frequency range. Sample materials are required to be homogeneous in thickness but could be arbitrary in shape. Dimensions of the samples are required to be at least 15 cm by 15 cm. The methodology is valid for solid or fabric materials. Demonstrated procedure was applied to magnetic materials with frequency-dependent permeability. In this case, frequency-dependent permeability was fitted in simulation at selected frequency points. The measurement setup is simple, and the simulation model runs within a few minutes. Obtained equivalent material properties are in the reasonable range as expected and results are validated.

ACKNOWLEDGMENT

This paper is based upon work supported in part by the National Science Foundation under Grant No. IIP-1440110.

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IV. DEVELOPING AN EQUIVALENT SYSTEM-LEVEL COMMON-MODE CURRENT MODEL BASED ON COMPONENT BEHAVIOR

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ABSTRACT

System-level radiated emission mostly is caused by the radiation from the common-mode current on the harness. Estimating system-level current distribution is complex. Here, an equivalent common-mode current model of the component is developed using relatively simple measurements of common-mode current on harness bundle. Prediction technique calculates equivalent common-mode source voltage and impedance, which can be used to predict current distribution on a harness with an arbitrary length or characteristic impedance, while excitation and termination on each wire are not known. The cables' terminations are assumed to be either open- or short-ended. Numerical optimization algorithms are used to predict common-mode current on a complex multi-wire harness connecting source with a load.

1. INTRODUCTION

Component behavior at the well-controlled test setup does not correlate with a complex system-level behavior. Component could pass component-level electromagnetic

emission test, but this does not guarantee that system will meet system-level standard requirements [1], [2]. Complexity and unpredictability of the system configuration makes difficult to predict failure at the early design stage [3]. Typically, component-level setup differs from system-level configuration, thus spectrum of the radiated emission is different [2], [4]. Failure to predict possible complications at the system waists financial and human resources. Developing an approach to predict system-level emissions based on a relatively simple component-level measurements is critical. Prediction method could help engineers to plan and build robust systems by detecting and fixing issues at the design stage [3], [5].

The objective of this paper is to demonstrate a methodology which uses relatively simple component-level measurements to estimate common-mode currents up to a few hundred megahertz on harnesses of arbitrary length and transmission line characteristics. Once common-mode current is accurately predicted radiated electromagnetic field could be numerically simulated [1], [6], [7], [8]. In this case assumption is that radiation is resulted only from common-mode current on the harness. Device under test (DUT) analyzed in this paper is a cable harness connecting engine control unit (ECU) with a load.

Previous work has demonstrated that the electromagnetic radiation from a cable harness can be obtained from the common-mode current distribution [1], [6], [9], [10]. To predict the system-level electromagnetic interference (EMI) resulting from a common-mode current on the cable harness currents are injected into a full-wave model as impressed current sources on small segments of the hardness [1], [6], [8]. Correlation between common-mode current and EMI is also established by determining transfer

function [2], [5]. These methods require common-mode currents to be known, either measured or estimated by numerical methods. Thus, prediction methods cannot predict EMI when current distribution changes while different placement of the harness.

In [1], [7], [9], [11] a generalized equivalent cable bundle method is presented for modeling EMI from a complex cable bundle terminated with arbitrary loads. Cable grouping method [1], [7], [11], assumes that source and termination information for each wire in a complex harness is known, which is rarely practical in real applications.

Proposed methodology can predict common-mode current distribution on a harness with an arbitrary length or characteristic impedance, while excitation on each wire are not known. With an assumption that cables' terminations are either open- or short-ended. Use an equivalent component model to evaluate system performance based on the numerical simulations. Numerical simulation tools are widely used to predict emissions [3], [7], [8].

Initial approach of the methodology was proposed in [12]. Common-mode current on a harness bundle is predicted by representing the bundle with two equivalent circuits, one terminated with a short and one terminated with an open. The common-mode current on each equivalent circuit is found from measurements of current at two locations along the harness [10]. Magnitude and relative phase of the common-mode current is required to determine the source voltages and impedances. Measuring relative phase between two setups with a different harness length is not practical and technique does not account for the error in phase. Formulation in [13] requires only magnitude values of the common-mode current and does not require the harness to be changed. However, technique in [13] does not account for coupling in the transmission line and shared impedance in the source

circuit. Proposed method in this paper accounts for coupling in the transmission line and does not limit complexity of the original source circuit. Here, to determine source voltage and impedance, nonlinear system of equations is analyzed. Optimization algorithms are used to minimize error with predicted and actual, measured currents. Three optimization solvers available in Matlab are evaluated. Optimal solutions of source voltage and impedance are used to predict the common-mode current on a harness of arbitrary length or arbitrary characteristic impedance.

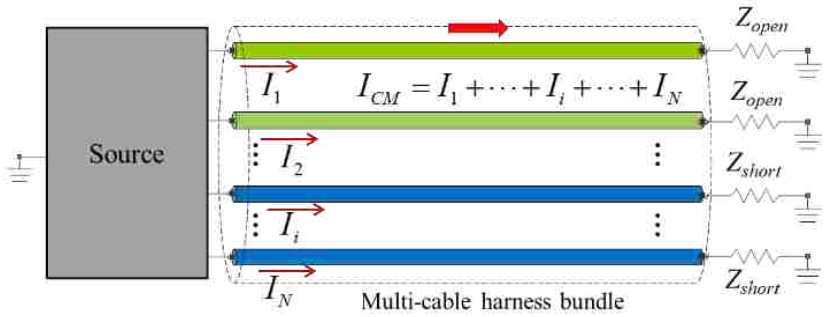
2. METHODOLOGY

Prediction technique makes possible to predict system-level common-mode current from a relatively simple component-level measurement. Alternatively, estimated common-mode current could be used to predict system-level emissions [8]. Proposed methodology assumes that overall common-mode current can be represented with two equivalent circuits terminated with an open and a short.

2.1. AN EQUIVALENT MODEL

A typical harness configuration [10] targeted by the method is shown in Figure 1(a). The harness can be approximated as a transmission line. In most of the practical situations source voltages and impedances are not known. Approach assumes loads can be approximated as shorts or opens. This assumption is valid for the capacitive or inductive terminations, when impedances are much smaller or larger than harness characteristic impedance.

Complex circuit [19], [7] shown in Figure 1(a) is simplified to an equivalent circuit as shown in Figure 1(b). An equivalent circuit consists of two wires, one wire is terminated with an ideal open and another wire is terminated with an ideal short. An equivalent source voltages and impedances for open- and short ended wires are found according the technique. Values of the equivalent source is selected so that common-mode currents in original and an equivalent harness are the same [16], [11].



(a)

(b)

Figure 1. (a) Multi-wire harness; (b) an equivalent two wire system [12].

2.2. CURRENT DISTRIBUTION IN THE MULTI-WIRE HARNESS

Equations describing current and voltage distribution on the transmission line were developed in [14]. The frequency-domain solution of the multi-conductor

transmission line equations for an $(n+1)$-conductors is based on the assumption that sources are sinusoids and voltages and currents are in steady state. The general solutions of the phasor multi-conductor transmission line equations are derived with additional constraint equations provided by the terminal conditions at the source and load locations. According to [14], current distribution on the transmission line can be described as

$$\hat{\mathbf{I}}(z) = \hat{\Phi}_{21}(z)\hat{\mathbf{V}}_s + \left(\hat{\Phi}_{22}(z) - \hat{\Phi}_{21}(z)\hat{\mathbf{Z}}_s\right) \cdot \left(\hat{\Phi}_1 + \hat{\Phi}_2\hat{\mathbf{Z}}_s\right)^{-1}\hat{\Phi}_2\hat{\mathbf{V}}_s \tag{1}$$

where

$$\hat{\Phi}_1 = \hat{\Phi}_{12}(\mathcal{L}) - \hat{\mathbf{Z}}_{\mathcal{L}}\hat{\Phi}_{22}(\mathcal{L}) \tag{2}$$

$$\hat{\Phi}_2 = \hat{\mathbf{Z}}_{\mathcal{L}}\hat{\Phi}_{21}(\mathcal{L}) - \hat{\Phi}_{11}(\mathcal{L}) \tag{3}$$

and $\mathcal{L}$ is a length of the transmission line, z is location along the transmission line ($0 < z < \mathcal{L}$), $\hat{\mathbf{I}}(z)$ is a $n \times 1$ column vector containing individual currents in n conductor lines. Source voltages and impedances are written in $\hat{\mathbf{V}}_s$ vector and $\hat{\mathbf{Z}}_s$ matrix, respectively. Termination impedances are listed in $\hat{\mathbf{Z}}_{\mathcal{L}}$ matrix. Coefficients $\hat{\Phi}_{ij}$ are chain-parameter matrices and are calculated as

$$\hat{\Phi}_{11}(z) = \frac{1}{2}\hat{\mathbf{Z}}_c\hat{\mathbf{T}}\left(\mathrm{e}^{\hat{\gamma}z} + \mathrm{e}^{-\hat{\gamma}z}\right)\hat{\mathbf{T}}^{-1}\hat{\mathbf{Y}}_c \tag{4}$$

$$\hat{\Phi}_{12}(z) = -\frac{1}{2}\hat{\mathbf{Z}}_c\hat{\mathbf{T}}\left(\mathrm{e}^{\hat{\gamma}z} - \mathrm{e}^{-\hat{\gamma}z}\right)\hat{\mathbf{T}}^{-1} \tag{5}$$

$$\hat{\Phi}_{21}(z) = -\frac{1}{2}\hat{\mathbf{T}}\left(\mathrm{e}^{\hat{\gamma}z} - \mathrm{e}^{-\hat{\gamma}z}\right)\hat{\mathbf{T}}^{-1}\hat{\mathbf{Y}}_c \tag{6}$$

$$\hat{\Phi}_{22}(z) = \frac{1}{2}\hat{\mathbf{T}}\left(\mathrm{e}^{\hat{\gamma}z} + \mathrm{e}^{-\hat{\gamma}z}\right)\hat{\mathbf{T}}^{-1} \tag{7}$$

where

$$\hat{\mathbf{Y}} = \mathbf{G} + j\omega\mathbf{C} \tag{8}$$

$$\hat{\mathbf{Z}} = \mathbf{R} + j\omega\mathbf{L} \tag{9}$$

where $\hat{\mathbf{R}}$, $\hat{\mathbf{L}}$, $\hat{\mathbf{G}}$ and $\hat{\mathbf{C}}$ are pre-unit length resistance, inductance, admittance, and capacitance of a transmission line, ω is the radian frequency of source where $\omega = 2\pi f$ and f is the cyclic frequency of excitation, $\hat{\mathbf{T}}$ are the eigenvectors of $\hat{\mathbf{Y}}\hat{\mathbf{Z}}$, and $\hat{\gamma}$ is propagation constant and is an $n \times n$ diagonal matrix calculates as

$$\hat{\mathbf{T}}^{-1}\,\hat{\mathbf{Y}}\hat{\mathbf{Z}}\,\hat{\mathbf{T}} = \hat{\gamma}^2 \tag{10}$$

Characteristic impedance is calculated as

$$\hat{\mathbf{Z}}_{\mathrm{C}} = \hat{\mathbf{Z}}\,\hat{\mathbf{T}}\hat{\gamma}^{-1}\hat{\mathbf{T}}^{-1} \tag{11}$$

and characteristic admittance matrix is calculated as

$$\hat{\mathbf{Y}}_{\mathrm{C}} = \hat{\mathbf{Z}}_{\mathrm{C}}{}^{-1} \tag{12}$$

More information regarding multi transmission line theory can be found in [14].

2.3. NUMERICAL OPTIMIZATION

According to multi-conductor transmission line theory, to find source voltages and impedances nonlinear system of equations (1) should be solved. Numerical optimization solution is needed to obtain the best fitted values of the unknowns while minimizing a cost function. In this case the cost function is an error between expected and fitted currents. Expected currents are obtained from 5-wire circuit simulations, which is an ideal imitation of the real measurements. Fitted currents in the equivalent harness are calculated based on the varying vector of the unknowns iteratively, until the minimization conditions for the cost function is satisfied. The cost function is defined as

$$Error(x) = \sum \left(I_{cm,exp.} - I_{cm,fitted}(x)\right)^2 \tag{13}$$

where $I_{cm,exp.}$ is expected current in 5-wire harness, $I_{cm,fitted}(x)$ is a fitted common-mode current in the equivalent harness, and vector of unknows are defined as

$$x = [V_{so}, V_{ss}, Z_{11}, Z_{12}, Z_{22}] \quad (14)$$

Unknows are complex numbers, thus real and imaginary parts are fitted. Additional constraints are defined for unknowns to ensure real part of the impedances are positive. A few numerical optimization solvers are available in Matlab. Function PatternSearch is applicable to be used to solve (1) and find global minimum of (13).

2.4. ESTIMATING COMMON-MODE EQUIVALENT SOURCE

Nonlinear system of equations can be solved using optimization tool as discussed in the previous section. Proposed technique is demonstrated on a test models in this section. Five-wire harness circuit was modeled as shown in Figure 2. Two wires in the harness are almost open due to higher resistance and three wires are approximately shorted compared to characteristic impedance of the transmission line. Multi-conductor transmission line is modeled using per-unit-length parameters which are obtained based on cross-sectional analysis using FEMAS tool.

Common-model current at least for three slightly different setups are needed. Different configuration of the circuit provides additional information so that optimization tool can have enough variation in data to converge and find acceptable values of the fitted common-mode currents. Four different length, 1.2 m, 1.5 m, 1.95 m and 2.1 m are used to obtain additional sets of nonlinear sets of equations. Different sets of configurations can also be obtained by lifting up load or source enclosure above the reference plane which

adds a capacitance between enclosure, and reference plane. Else by adding voltage source in-between the enclosure and the reference plane.

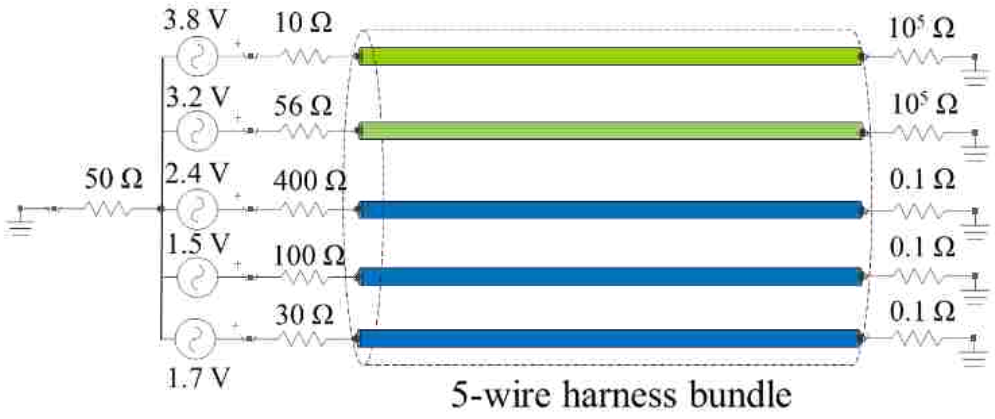
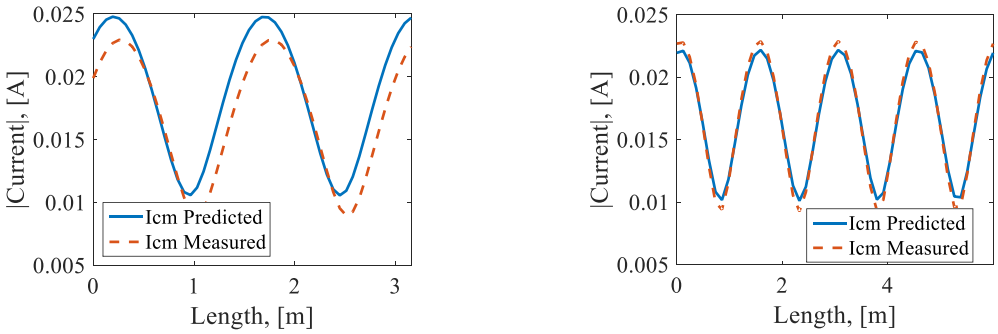


Figure 2. The circuit of the 5-wire harness.

The common-model current distribution along the 5-wires were input parameters of the PatternSearch optimization tool to find optimal values of the source voltages and impedances. Obtained source impedances and voltages were used to predict common-mode current on an arbitrary length using equivalent harness model as shown in Figure 1(b). Predicted common-mode current on the 3.2 m, and 6 m harnesses at 100 MHz were estimated and compared with the ideal, 5-wire circuit results as shown in Figure 3. Error of the prediction was calculated as

$$Error = dB\left(\frac{max\{|I_{cm,ideal}|\}}{max\{|I_{cm,fitted}|\}}\right) \quad (15)$$

Error was estimated for every possible length from a wavelength to two wavelengths. Expected errors are shown in Figure 4. For the given example, prediction error is less than a 1.8 dB for any arbitrary length of the hardness.



(a) (b)

Figure 3. Comparison of the ideal and predicted common-mode currents on the (a) 3.2 m; (b) 6 m long harness.

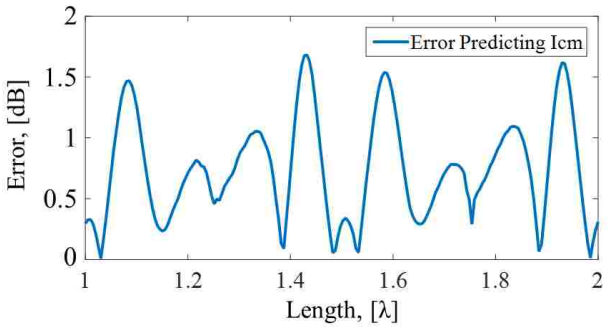


Figure 4. Error of the prediction for every possible length, when complex common-mode currents were used for optimization.

The same circuit (Figure 2), and configurations were used to obtain source information, but magnitude of the common-mode currents were used for optimizations. Predictions error was estimated as shown in Figure 5 when only magnitude of the common-mode current was used for optimization. Expected error for these given conditions is less than 3 dB for any arbitrary harness length. More number of the configurations are needed to reduce prediction error when magnitudes of the common-mode currents are given to optimization function.

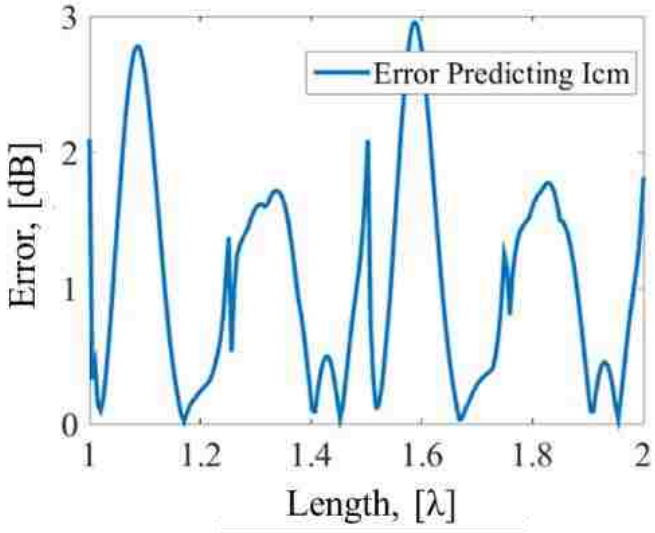


Figure 5. Error of the prediction for every possible length, when magnitudes of the common-mode currents were used for optimization.

3. CONCLUSION

Common-mode current prediction technique requires relatively simple common-mode current measurements at a component-level. Prediction requires magnitude values of the common-modes current, which makes measurement process relatively simple and fast. Harness at the component level is assumed to be a transmission line, so that the steady-state current distribution can be applied. The far-end terminations for each wire are assumed to be either open- or short-ended relative to characteristic impedance of the harness. Numerical solutions were used to solve nonlinear coupled harness problem. Direct search optimization was used to fit common-mode source unknowns while minimizing least-square error between expected and predicted common-mode currents.

Prediction error does not exceed 1.8 dB, if magnitude and phase of the common-mode current are known. In case only magnitude of the current is known, prediction error is below 3 dB. Prediction technique is shown to be a useful tool to predict common-mode current and further to estimate radiated emissions at the system-level, when length of the harness is different.

ACKNOWLEDGMENT

This paper is based upon work supported in part by the National Science Foundation under Grant No. IIP-1440110.

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SECTION

2. CONCLUSIONS

High-speed designs need increasingly accurate estimates of the power bus impedance. Decoupling capacitor representation as a series equivalent capacitance, inductance, and resistance is acceptable to model power distribution networked impedance below a few hundreds of megahertz. As shown in the first and second papers, the ESL value provided by the vendors are inaccurate. The key issue solved by the proposed partitioning approach is to efficiently model inductance when 2- or 8-terminal decoupling capacitors are mounted on the PCB. According to partitioning approach, inductance of the 2-terminal capacitor, pads, and reference plane can be calculated separately and added to the layout inductance to obtain complete PDN impedance. Accuracy of petitioning approach depends on how strong the inductive coupling is between the capacitor's body and the area under it. The equivalent inductance associated with the 8-terminal decoupling capacitor mounted on the package or PCB is analyzed in the second paper. Sufficiently accurate models can be found for the inductance computation if the capacitor plates are replaced with a conductor block. Further, the important issues in the tolerances and different connection arrangements has been studied. The results show that the distance to the return plane has the most impact. The total inductance of a mounted 8-terminal capacitor varies between 30 pH and 50 pH if dielectric thickness of the first layer of package is between 3 mils and 5 mils. Using shifted via positions of the pads can change inductance as much as 10 pH. The mounted

capacitor's inductance can be established before designing the overall PDN circuit details. The methodology of obtaining equivalent material properties of magnetic or non-magnetic composed materials is proposed in the third paper in this dissertation. Methodology is valid at kilohertz frequency range, and planer materials are required to be homogeneous in thickness but could be arbitrary in shape. Planer material should not be smaller than 15 cm by 15 cm rectangular. Equivalent material properties of solid or fabric composed materials are found and properties are used to estimate shielding with less than 1.6 dB certainty compared to measured shielding data.

In the fourth paper, common-mode current prediction technique is proposed, which requires relatively simple common-mode current measurements at a component-level. Harness at the component-level is assumed to be a transmission line, and multi-conductor transmission line theory is applied to model current distribution. The far-end terminations for each wire are assumed to be either open- or short-ended relative to characteristic impedance of the harness. Magnitude of the common-modes current on the harness is required to predict common-mode excitation circuit. Numerical optimization algorithms were used to solve nonlinear coupled harness problem. Prediction error does not exceed 1.8 dB, if magnitude and phase of the common-mode currents are known. Prediction error is below 3 dB for any given length of the harness, if magnitude of the current is given. Prediction technique is shown to be a useful tool to predict common-mode current when details about source and loads are not given.

VITA

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