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Advanced control architectures for grid connected and standalone converter systems

Subhajyoti Mukherjee

Department: Electrical and Computer Engineering

ADVANCED CONTROL ARCHITECTURES FOR GRID CONNECTED AND STANDALONE CONVERTER SYSTEMS

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SUBHAJYOTI MUKHERJEE

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Approved by

Mehdi Ferdowsi, Co-Advisor
Pourya Shamsi, Co-Advisor
Jonathan Kimball
Hamidreza Modares
Ali Rownaghi

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ABSTRACT

This dissertation proposes new control algorithms dedicated towards improving the reliability, computational burden and stability in grid-connected and stand-alone based power electronic converter systems applicable for ac microgrids.

Two voltage sensorless control architectures, one for stand-alone applications and the other for grid-connected application are established in this thesis. The output voltage of a standalone single-phase inverter is controlled directly by controlling the output filter capacitor current without using a dedicated output voltage sensor. A method to estimate the output filter capacitance is also presented. For the grid connected converter, a novel closed loop estimation is presented to estimate the grid voltage. In addition to the estimation of the grid voltage, the proposed method also generates the unit vectors and frequency information similar to a conventional phase-locked loop structure. The voltage sensorless algorithm is then extended to *LCL* filter based grid connected converters thereby proposing a new indirect method of controlling the grid current.

Furthermore, addressing the stability issues in current-controlled grid tied converters, this dissertation also analyzes the power angle synchronization control of grid-tied bidirectional converters for low voltage grids. The power flow equations for the low voltage grid are analyzed and compensators are designed to ensure the decoupled control of active and reactive power. It is demonstrated that the proposed compensators are immune to grid fluctuations and ensure stable operation controlling the desired power flow to and from the grid.

Detailed plant modeling, controller design, simulation and experimental results are presented for all of the proposed schemes.

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1. INTRODUCTION

1.1. REVIEW OF EXISTING CONTROL ARCHITECTURES FOR STAND-ALONE AND GRID-CONNECTED CONVERTER SYSTEMS

The single-phase and three-phase voltage source converter is the most commonly used power electronics converter for utility level stand-alone or grid-connected distributed generation units. With the focus on reducing emission due to power production by fossil fuels, renewable energy gained immense importance over the past few decades. Renewable energy being abundantly available with no cost, it can serve as an alternative for power production. Various renewable resources present offer their own advantages and disadvantages. The most commonly used renewable power sources are the wind energy and solar energy. Extraction of power from wind energy requires high initial cost for setting up of the wind power plant i.e. the wind turbine along with its mechanical and electrical control system for optimal usage. On the other hand solar energy requires the panels to be setup over along with its electrical and mechanical systems which also involve high initial cost. However, from the perspective of maintenance solar power plants are comparatively easier to maintain from the mechanical perspective as replacement of a wind turbine would involve replacing an old wind turbine with a newer one. On the contrary maintenance of solar power plants is easier from the mechanical perspective. However, it might get challenging to locate the exact point of problem in a solar power plant as generally mechanical failure of a solar panel is seldom observed. Despite all these advantages and disadvantages, due to the inherent intermittent nature of renewable power resources it becomes immensely challenging to connect these

sources to the grid/local load directly. The latter issue enabled researchers to come up with interfacing power converter topologies for successful grid integration of renewable power resources. A DC-AC converter serves as the interface for the renewable power source to connect to the grid. Pointing out some drawbacks in the existing control architecture, advanced control technique to successfully integrate renewable resources with the grid is the main focus of this thesis.

For grid-connected applications, the goal is to control the active and reactive power supplied to and from the grid. Since, the grid voltage is (generally) not dictated by the converter, this is achieved by controlling the current supplied by the converter to the grid. This control approach is known as the current control architecture [1]-[3], and is immensely popular due to its inherent simplicity and decoupled nature. Typical implementation with a *L* and *LCL* filters are shown in Figure 1.1 - Figure 1.3. The control scheme requires the accurate phase information of the fundamental component of the grid voltage. This information is obtained from a phase locked loop (PLL) which has the grid voltage as its input and generates the frequency and phase information (in the form of unit vectors) as its outputs. On the contrary, for stand-alone applications (see Figure 1.4) the goal is to control the output voltage. The output voltage requirement at the utility level is dictated as in [4] which clearly specifies the voltage rms to be within ±5% of the nominal voltage. General requirements necessitate a control architecture which needs to ensure a negligible steady-state error in the output voltage, a minimum total harmonic distortion (THD) under nonlinear loads, and a fast response during load transients. The popularly used control architecture to achieve these is the two-loop control [5], [6], with an inner current and outer voltage loop as shown in Figure 1.4.

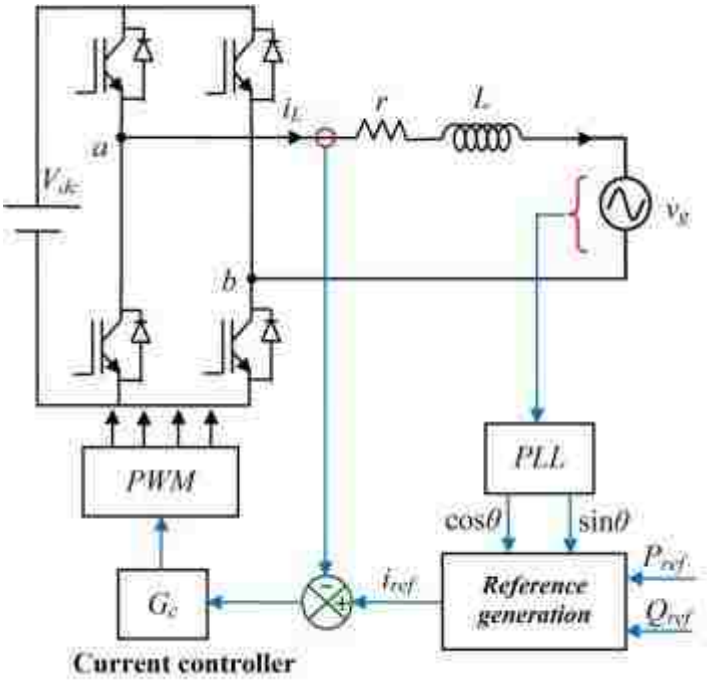

Figure 1.1. Current controlled architecture for single-phase grid-connected converter.

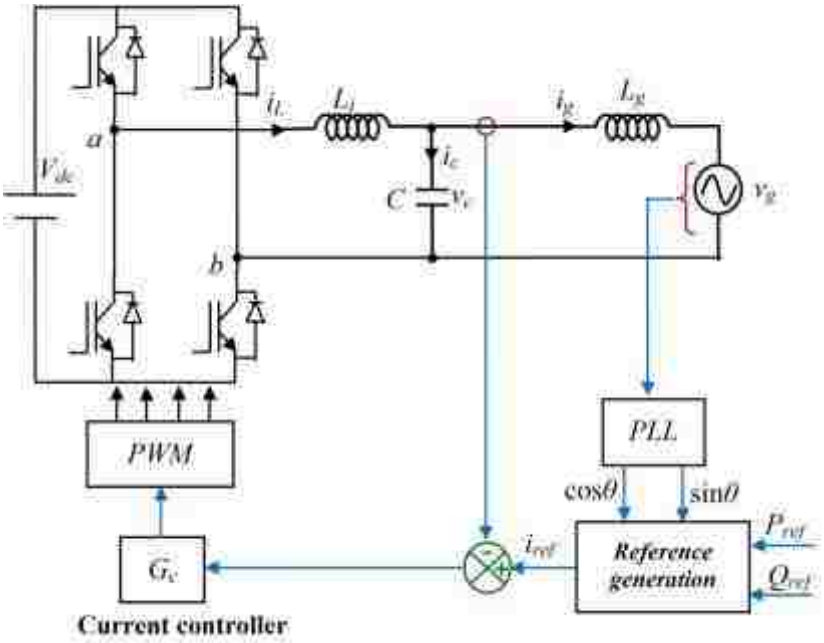

Figure 1.2. Direct grid current control architecture for *LCL* filter based single-phase grid-connected converter.

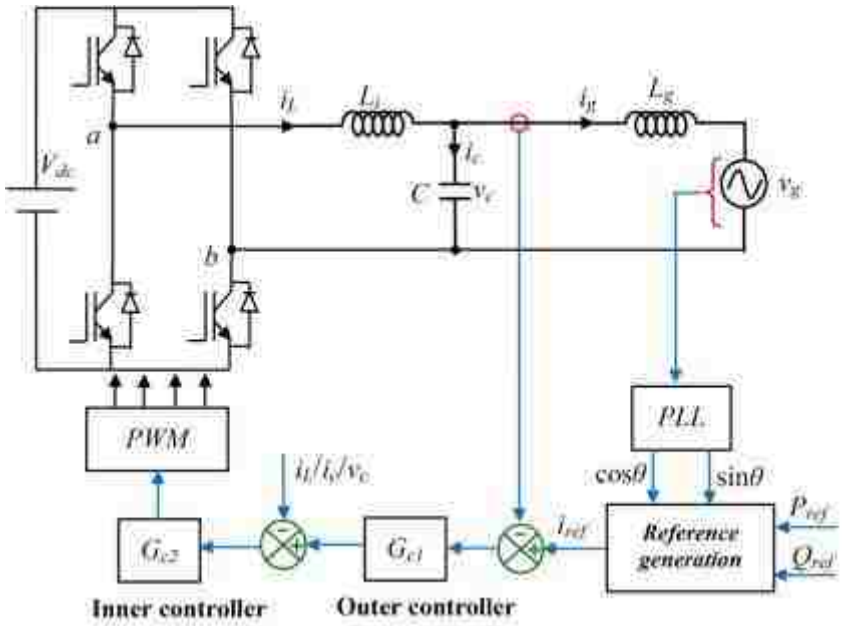

Figure 1.3. Multi-loop current control architecture for *LCL* filter based single-phase grid-connected converter.

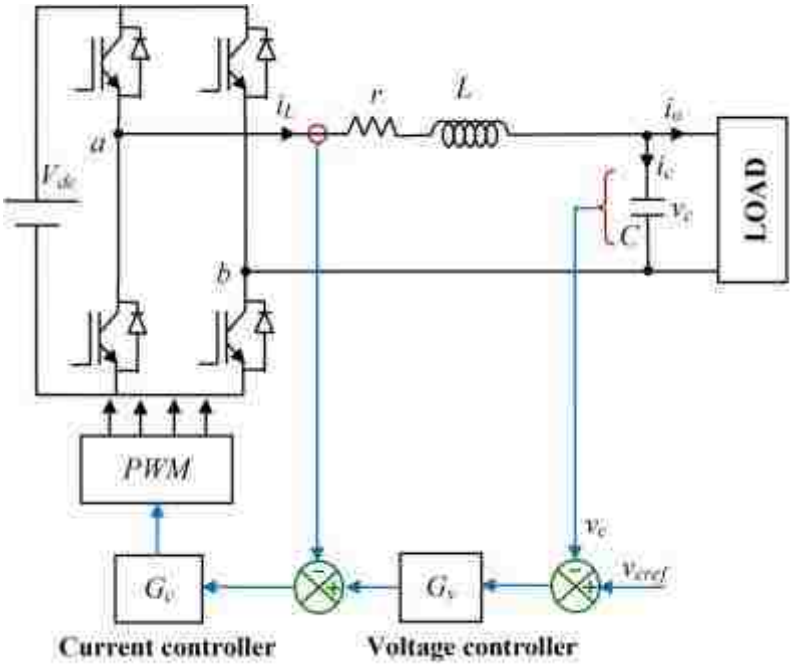

Figure 1.4. Conventional two-loop architecture for single-phase stand-alone converter.

The performances of the conventional control architectures have reported satisfactory performance. However, the following drawbacks are noted in the existing control architectures. The power electronic converter (stand-alone or grid connected) is crucial for utility applications. Hence it is important to ensure its reliable operation. As discussed above, it can be identified that the voltage and current sensors are extremely crucial in the control architecture and the smooth functioning of the converter. However, sensors are prone to failure. In situations where any sensor fails, the dedicated control system for the converter will be jeopardized and in worst case this may cause disconnection and complete shutdown of the corresponding power converter. So, for increased reliability, there is a need to look for possible sensorless control algorithms. A sensorless algorithm may act as a suitable backup and take over once a sensor failure is identified. From protection point of view, removing the current sensors is not advisable. However, possible sensorless control algorithms can be ventured to replace the voltage sensor. A sensorless algorithm also saves space and cost. This results in a more compact design.

The *LCL* filter based grid connected converter has reported excellent grid current quality. However, the controller itself is challenging to design. Direct control of the grid current implies designing a controller for a third order system. This is not straight forward and generally involves a complex controller structure [7]. Multiple control loops have also been proposed for *LCL* based grid connected converters, [8]-[15], for stability and resonance damping at the cost of increased sensors. In general, the grid side current is chosen as the variable for the outer loop while the inner loop variable is chosen as the capacitor current [8], [11], [12],or the converter current [13] or the filter capacitor voltage

[14], [15]. However design of a multi-loop control structure is not trivial and requires detailed mathematical analysis [8], [11]. Compared to controlling the grid current, control of the converter side current is simple. Hence, alternative approaches to control the grid current by controlling the converter side current can be ventured. Additionally, accurate and optimized controller design depends on knowledge of accurate plant parameters. The plant parameters change depending on the operating conditions, temperature and ageing. So an online estimation of the plant parameters can be done to get an accurate plant model and tune the control parameters accordingly.

Finally, the popularly used current controlled architecture for grid connected converters are reporting stability problems in weak grid conditions with multiple converters connected in parallel. The loss of stability is mainly due to unmodelled and simplified PLL dynamics [16]-[20]. While research is still being carried on to mathematically model the issue, there is a parallel need to come up with alternate control algorithms which eliminate the PLL structure but still retain the advantages of the current control architecture.

1.2. RESEARCH CONTRIBUTION

Addressing the above problems, this dissertation proposes the following solutions for grid connected and stand-alone converter systems. Some of the solutions are proposed for single-phase systems. However, they are equally applicable to corresponding three-phase architectures.

A methodology to control the output voltage of a standalone single-phase inverter without using a dedicated output voltage sensor (addressed in Paper I). The proposed control architecture aims to control the output voltage by controlling the output filter

capacitor current. In addition to eliminating the voltage sensor, the proposed control method achieved better total harmonic distortion (THD) in the output voltage compared to existing conventional control methods. The plant modeling and controller design for the proposed control technique are presented. The proposed method depends on having the value of the output filter capacitance. A method to estimate the output filter capacitance is also presented. Dependence of the system parameters on the proposed control is studied. Rigorous analysis is done to show that the proposed sensorless scheme ensures the output voltage is within specified regulations at utility level.

For grid connected applications, it is important to know the phase and frequency of the grid voltage. This dissertation (Paper II) presents an estimation algorithm to estimate the grid voltage and control a single-phase grid connected converter without a dedicated grid voltage sensor. The main focus is given to current controlled architectures which need phase locked loops (PLL) for their operation. The grid voltage estimation method is proposed based on the active and reactive power delivered by the converter to the grid. In addition to the estimation of the grid voltage, the proposed method also generates the unit vectors and frequency information similar to a conventional PLL structure. The effect of circuit non idealities and parameter variations are considered and analyzed in details, thereby establishing their effects on the proposed estimation scheme. The proposed estimation algorithm is equally applicable for three phase grid connected systems. The proposed estimation method is then applied to *LCL* based grid connected converter to develop an indirect grid current control algorithm (Paper III). The new control algorithm of *LCL* based grid connected converter system uses the same number of sensors as a conventional direct grid current control algorithm (one current and one

voltage sensor). However, compared to the direct grid current control, the proposed control structure is simple in design as it controls the converter side current which follows an equivalent first order system. Fundamental and harmonic components of the filter capacitor voltage are estimated and the corresponding filter capacitor currents are computed from these estimated values. The fundamental and harmonic filter capacitor currents are then compensated from the converter side thereby indirectly controlling the grid current.

Addressing the issue of parameter variations, this dissertation proposes an online estimation based on model reference adaptive control (MRAC) approach in obtaining an accurate model of a grid connected inverter system. Active and reactive power based MRAC approaches are used to estimate the equivalent resistance and reactance between the inverter and the grid. Detailed stability analysis of the MRAC approach is presented. The system models for the MRAC controller design are derived and guidelines on the controller parameters selection are proposed.

Addressing the stability issue in conventional current controlled grid connected converter systems, this dissertation analyzes the power angle synchronization control of a grid-tied bidirectional dc-ac converter is investigated for low voltage grids (Paper V). The concept of power angle synchronization based control is to replace the current controlled architecture with voltage controlled architecture. In other words, the active and reactive power delivered to and from the grid is now controlled by controlling the voltage at the output of the converter. The power flow equations for the low voltage grid are analyzed and compensators are designed to ensure the decoupled control of active and reactive power. The proposed control system operates without the need for a phase

locked loop during balanced and unbalanced grid conditions. The proposed power angle synchronization shows stable start-up, steady state and transient state operation during balanced grid conditions ensuring the desired power flow to and from the grid. It is also demonstrated that the compensators are immune to grid fluctuations and to a large extent can cater grid unbalanced conditions.

PAPER

I. CONTROL OF A SINGLE-PHASE STANDALONE INVERTER WITHOUT AN OUTPUT VOLTAGE SENSOR

ABSTRACT

This paper analyzes the possibility of controlling the output voltage of a standalone single-phase inverter by directly controlling the output filter capacitor current without using a dedicated output voltage sensor. The plant modeling and controller design are presented. The proposed method depends on having the value of the output filter capacitance. A method to estimate the output filter capacitance is also presented. Rigorous analysis is done to show that the proposed sensorless scheme is largely insensitive to parameter variations and ensure the output voltage is within specified regulations at utility level. It is also demonstrated in the paper that compared to the conventional voltage control scheme the proposed control scheme ensures an improved total harmonic distortion (THD) of the output voltage waveform. Experimental results presented validate the proposed scheme.

1. INTRODUCTION

The single-phase voltage source inverter is the most widely used power electronic converter for utility level standalone distributed generation units. The output voltage requirement at the utility level is dictated as in [1] which clearly specifies the voltage rms to be within ±5% of the nominal voltage. General requirements necessitate a control

architecture which needs to ensure a negligible steady-state error in the output voltage, a minimum total harmonic distortion (THD) under nonlinear loads, and a fast response during load transients. Thus the control of such inverters has become a topic of interest among researchers. Unlike a three-phase inverter, a single-phase inverter cannot be directly controlled in the synchronous frame of reference. Authors of [2], [3] proposed to do so by creating a fictitious quadrature axis. Though the modeling and control of the inverter becomes simple in the fictitious synchronous frame of reference, the conversion itself involves additional computations and inherently introduces delay in the system. Furthermore, additional controllers as shown in [4] are necessary to maintain the output voltage under nonlinear loads. Over the past years, several nonlinear, adaptive, hysteresis, repetitive and geometric based control structures have been proposed for controlling single-phase inverter systems [5]−[15]. However, each of these interesting control structures have their limitations namely modeling complexities, detailed mathematical derivations, unsatisfactory performances under nonlinear loads, parameter sensitivity etc. Among the proposed control structures for single-phase inverters in the literature, the proportional resonant (PR) controller is arguably the most popular. The PR controller in a stationary frame of reference is the equivalent counterpart of the proportional integral (PI) controller in the synchronous frame of reference. Initially proposed in [20], the PR controller has been successfully implemented to track linear and nonlinear currents in current controlled grid connected converters [16]−[18]. It has also been applied to standalone converters to control their output voltage [5], [21]. The controller has reported excellent steady state error tracking under linear loads. However, as shown in [19], the controller has stability issues under nonlinear loads. This is primarily because with the

addition of resonant peaks at the dominant harmonic frequencies, namely third, fifth and seventh, the phase margin of the control loop deteriorates. The system stability thereby puts a limit on the resonant gains at higher harmonic frequencies, thereby requiring additional measures to improve the phase margin and reduce the voltage THD under nonlinear loads [19].

All the previous control architectures discussed for single-phase inverters use an output voltage sensor. In this paper, we take a novel step by eliminating the output voltage sensor and investigate the possibility of controlling a standalone inverter without the voltage sensor. Sensorless control has been proposed for grid connected converter systems where the power flow between the converter and the grid is controlled without the need of dedicated grid voltage sensors [22]−[24]. However, to the best knowledge of the authors, sensorless voltage control approaches have not been discussed for standalone inverters in the literature. With a regulated dc bus voltage, faults in single-phase inverter systems are generally caused by overcurrents. Hence, eliminating the output voltage sensor does not compromise the system protection. In fact, the elimination of the voltage sensor saves cost and space. Additional circuitry and wiring requirements are also reduced. The inverter may have to operate in an environment where it is subjected to high temperature, electromagnetic interference (EMI), and noises. In such conditions, sensors are prone to errors and physical damage. One such example is the hybrid power train where the power electronics converters have to operate under high temperature, noise and vibrations. A damaged or inaccurate sensor will jeopardize the entire system. A sensorless control scheme thus adds to the reliability of the overall system. It actsas a backup during sensor failure thereby preventing complete shutdown of the system.

However, it must be ensured that the output voltage meets the desired specifications for utility applications [1]. Addressing this issue, the control methodology presented in this paper ensures that the output voltage is within the prescribed limits. The approach aims to control the output voltage by directly controlling the output capacitor current. An estimation of the output filter capacitance, required for this purpose is also discussed. It is demonstrated that the proposed control scheme ensures better THD of the output voltage under nonlinear loads compared to the conventional voltage control approach. A thorough analysis is done to show that such estimation along with the proposed control structure is largely immune to parameter fluctuations.

The rest of the paper is arranged as follows. The proposed control scheme is presented in Section 2. This section also includes the estimation of the output voltage and the output filter capacitance prediction. The modeling of the rms voltage control loop and the sensitivity of the output voltage to the parameter variations is shown in Section 3. The results are discussed in Section 4, while the conclusion presented in Section 5.

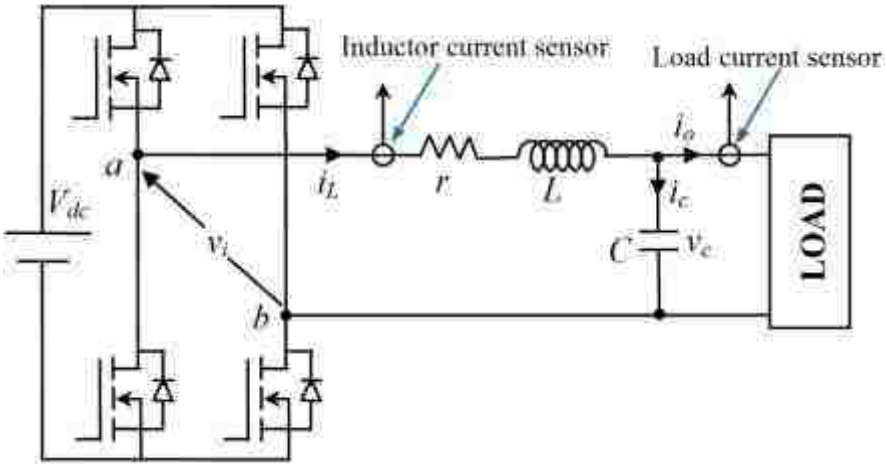

Figure 1. Circuit of a single-phase standalone inverter.

2. CONTROL ARCHITECTURE

The schematic of a standalone inverter is shown in Figure 1. In the figure, L is the filter inductance, r is the resistance representing the ohmic loss of the switches and the filter inductor, C is the filter capacitance, i_L is the filter inductor current, i_o is the load current, i_c is the capacitor current, v_c is the output voltage of the converter, and v_i is the output voltage of the bridge. The filter inductor and load current are measured. However, unlike conventional voltage control methods the output voltage is not measured for the proposed sensorless control scheme.

2.1 Review of the Conventional Voltage Control Method

The inductor current and output capacitor voltage dynamics for the circuit as shown in Figure 1 are given as

$$L\frac{di_L}{dt} + ri_L = v_i - v_c \tag{1}$$

$$C\frac{dv_c}{dt} = i_L - i_o \tag{2}$$

The inductor current, output capacitor current, and load current are related as

$$i_L = i_o + i_c \tag{3}$$

The multi loop structure with an outer voltage loop and an inner current loop [21] is generally used as the controller structure. The control structure introduces output impedance dependent on the load current. It has been reported that the choice of the capacitor current feedback in the inner current loop ensures much lower output impedance compared to the inductor current feedback approach [21]. The controller

structure is presented in Figure 2. The output voltage feedforward is also added to the control loop. With such a control structure, the open loop gain is given as [21]

$$G(s) = \frac{k_{pc} G_v(s)}{s^2 LC + (r + k_{pc}) sC} \tag{4}$$

where $G_v(s)$ is the voltage compensator and k_{pc} the proportional gain of the inner current loop. The system represented by (4) is a second order system. With an increase in the controller gain, especially at the higher harmonic frequencies, the phase margin of the system deteriorates. So there is a tradeoff between achieving a high bandwidth and stability in the open loop gain represented by (4). Often phase lead compensators are needed to improve the phase margin as reported in [19].

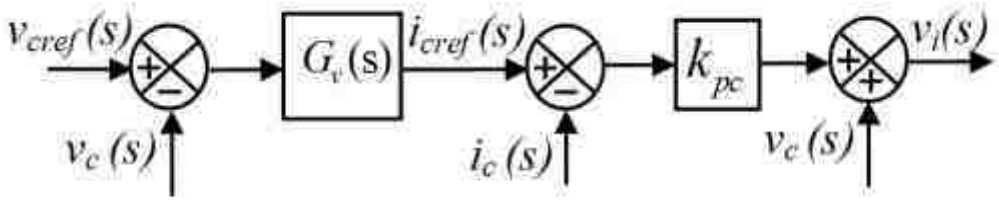

Figure 2. The conventional voltage control structure with capacitor current feedback.

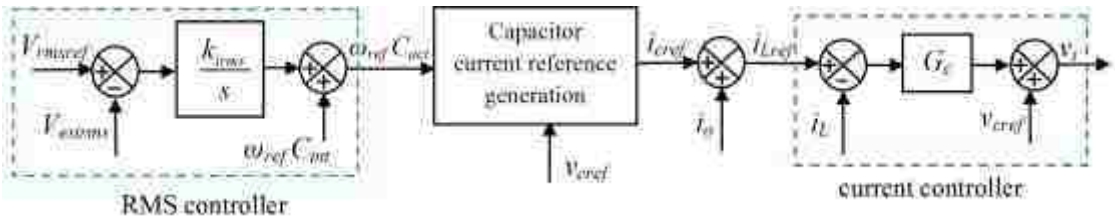

Figure 3. Overall block diagram of the proposed control scheme.

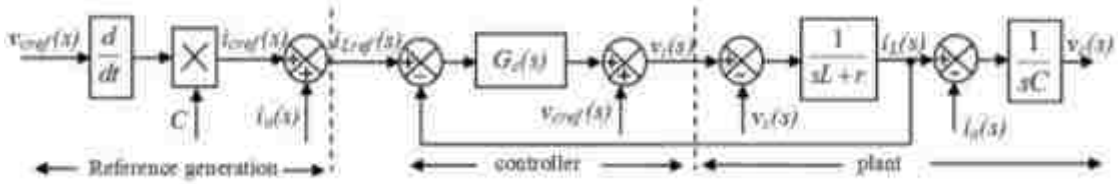

Figure 4. The current control loop with the corresponding plant.

2.2 Proposed Control Scheme

The overall block diagram of the proposed control scheme is shown in Figure 3. The control structure has three distinct parts, the voltage RMS controller, the filter capacitor current reference generator, and a current controller. Each of the section is sequentially described in details. The output voltage of a single-phase inverter can be controlled by controlling the capacitor current. To produce the desired output voltage vcref, an inductor current reference can be set as

$$i_{Lref} = i_o + i_{cref} \tag{5}$$

where,
$$i_{cref} = C\frac{dv_{cref}}{dt} \tag{6}$$

It is worth mentioning that metallized polypropylene film capacitors are the most common choice as filter capacitors. These capacitors have negligible equivalent series resistance (ESR). On the basis of this knowledge, the resistive drop across the output capacitor has been ignored in (6). It can be seen from (1) that inductor current i_L can be controlled by v_i, the output of the bridge, while the dynamics of output voltage v_c can be controlled by controlling inductor current i_L. Thus output voltage v_c can be indirectly controlled by controlling v_i. A properly designed controller will ensure that the output of the bridge (v_i) is able to maintain the inductor current at its desired reference i_{Lref} (as in

(5)) thereby ensuring that capacitor current i_c is maintained at i_{cref} as given in (6). This in turn will ensure that the output voltage is maintained at the desired reference value v_{cref}. However, it should be noted that an accurate knowledge of the value of the output filter capacitor is needed in (6). The rms voltage controller in Figure 3 gives an estimation of the filter capacitor which is used to calculate the capacitor reference current (as in (6)). The capacitor reference current generator in Figure 3 basically implements (6). The estimation of the capacitor and capacitor reference current generation will be addressed in details in the next section. Capacitor reference current icref is added to the load current to generate reference inductor current i_{Lref} as in (5). A well-designed current controller ensures that the actual inductor current i_L tracks i_{Lref}. The current controller structure is represented as

$$v_i(s) = (i_{Lref}(s) - i_L(s))G_c(s) + v_{cref}(s) \tag{7}$$

where $G_c(s)$ represents the current controller. Generally output voltage v_c is treated as a disturbance input in (1) and is used as the feedforward term in (7) [21]. However, as a voltage sensor is not being used, v_c is not available. So v_{cref} is used as the feedforward term. The control structure is shown in Figure 4.

The design of the controller needs the knowledge of the plant model. In other words, the open loop gain of the plant and controller must be known. The loop gain of the proposed control structure is derived next. Taking the Laplace transform of (2), (3), (5) and (6) and using them in (7) leads to

$$v_i(s) = \left(sCG_c(s) + 1\right)v_{cref}(s) - sCG_c(s)\,v_c(s) \tag{8}$$

Also, in the Laplace domain (1) and (2) can be combined as

$$\left(s^2LC + srC + 1\right)v_c(s) + \left(sL + r\right)i_o(s) = v_i(s) \tag{9}$$

Substituting $v_i(s)$ from (8) in (9) results in

$$\left(s^2LC + s(r + G_c(s))C + 1\right)v_c(s) = \left(sCG_c(s) + 1\right)v_{cref}(s) - \left(sL + r\right)i_o(s) \tag{10}$$

or,
$$v_c(s) = \frac{sCG_c(s) + 1}{s^2LC + s(r + G_c(s))C + 1}v_{cref}(s) - \frac{sL + r}{s^2LC + s(r + G_c(s))C + 1}i_o(s) \tag{11}$$

which can be rearranged in the standard form as

$$v_c(s) = \frac{\frac{sCG_c(s) + 1}{sC(sL + r)}}{1 + \frac{sCG_c(s) + 1}{sC(sL + r)}}v_{cref}(s) - \frac{\frac{1}{sC}}{1 + \frac{sCG_c(s) + 1}{sC(sL + r)}}i_o(s) \tag{12}$$

The block diagram representation of (12) is shown in Figure 5. The load current i_o is generally treated as an disturbance input. From (12), treating i_o as a disturbance input, the transfer function relating v_c and v_{cref} need sto be found. This transfer function will serve as the closed loop gain. The closed loop gain is obtained as

$$\frac{v_c(s)}{v_{cref}(s)} = G_{cl}(s) = \frac{\frac{sCG_c(s) + 1}{sC(sL + r)}}{1 + \frac{sCG_c(s) + 1}{sC(sL + r)}} \tag{13}$$

Equation (13) is in the standard form. The open loop gain is found by inspection of (13). From (13), the open loop gain is obtained as

$$G_{ol}(s) = \frac{sCG_c(s) + 1}{sC(sL + r)} \tag{14}$$

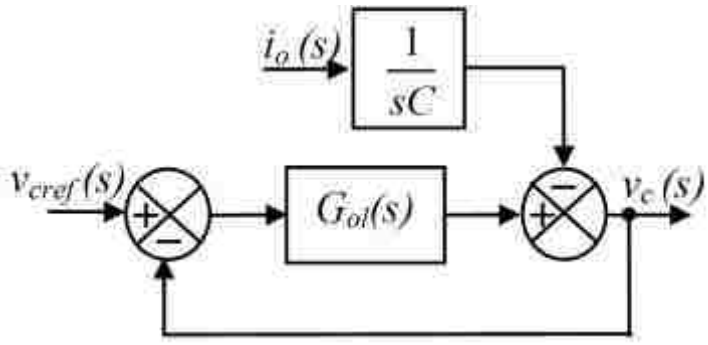

Figure 5. Closed loop equivalent representation of the controller structure.

The controller parameters will be selected based on the open loop gain in (14). Again, open loop gain $G_{ol}(s)$ can be simplified as

$$G_{ol}(s) = \frac{1}{sC(sL+r)} + \frac{G_c(s)}{sL+r} \tag{15}$$

or,
$$G_{ol}(s) = G_1(s) + G_2(s) \tag{16}$$

where,
$$G_1(s) = \frac{1}{sC(sL+r)} \text{ and } G_2(s) = \frac{G_c(s)}{sL+r}$$

It can be observed from (15) and (16) that the open loop gain at low frequencies is primarily dictated by $G_1(s)$. However, as frequency increases the influence of $G_1(s)$ decreases. So at higher frequencies the open loop gain is dictated by $G_2(s)$. Hence it can be asserted that the system bandwidth and response to harmonic frequencies can be controlled by $G_c(s)$. It should also be noted that similar to the voltage control architecture [19], [21], output impedance $Z_o(s)$ is also introduced in this case. From (12), $Z_o(s)$ can be found as

$$\frac{v_c(s)}{i_o(s)} = Z_o(s) = \frac{sL+r}{s^2LC + s(r+G_c(s))C + 1} \tag{17}$$

From (3) and (5) it is worth noting that

$$i_{Lref} - i_L = i_{cref} - i_c \tag{18}$$

So, unlike in voltage control structures, it can be concluded that the choice of the inductor current or the capacitor current as the control variable makes no difference to the performance of the control loop for the proposed scheme.

Since a single-phase system is expected to produce a sinusoidal output, a PR controller with the resonant peak at the fundamental frequency is sufficient as the current controller. However, since any standalone system must have the capability to cater nonlinear loads, the controller is augmented with resonant peaks at dominant harmonic frequencies, namely the third, fifth and seventh harmonic frequencies. Incorporating the additional resonant peaks, the controller structure is given as

$$G_c(s) = k_p + \sum_{n=1,3,5,7} \frac{k_{rn}\omega_{cutn}s}{s^2 + 2\omega_{cutn}s + \left(n\omega_o\right)^2} \tag{19}$$

In (19), k_p is the proportional gain, k_{rn} and ω_{cutn} are the resonant gain and cut off frequency at the n^{th} harmonic frequency. The proportional gain and resonant gains are chosen such that the bandwidth is about 3 kHz, while the gain at the fundamental and compensated harmonic frequencies is at least 40 dB. It should be noted that since the open loop system has a first order behavior, the phase margin at 3 kHz is sufficiently high (about 75 degrees). Such high phase margin and bandwidth cannot be simultaneously achieved with the conventional voltage control architecture. The different components used for the circuit in Figure 1 are listed in Table 1. It should be noted that in Table 1, r is taken as the summation of the winding resistance of the inductor and twice the on state resistance of each switch ($r = r_{dc}+2R_{ds}$). With the controller parameters represented in

Table 2, the open loop frequency response of the plant and the controller is shown in Figure 6. The corresponding close loop response is shown in Figure 7. For the chosen controller parameters, the output impedance Z_o is shown in Figure 8. It can be seen that the output impedance is very low at the fundamental and compensated harmonic frequencies. The effect of the delay introduced due to the sampling, computation and PWM update was not considered in the controller design. The delay adds an additional phase lag to the system [4]. Hence it is important to verify that the phase lag does not make the closed loop system unstable. The phase lag introduced due to the delay is approximated as

$$\phi_{del} = -tan^{-1}(\omega T_{del}) \tag{20}$$

For a switching frequency of 20 kHz, a double sample and update scheme in one switching cycle gives T_{del} of 25 micro seconds. Using (20), the phase lag at the cross over frequency of 3 kHz, is computed as 25 degrees. Hence the phase margin at the crossover frequency of 3 kHz decreases from 75 degrees to 50 degrees. This phase margin is still sufficient to ensure the stable operation of the closed loop system.

Table 1. System Parameters.

Part	Manufacturer	Specifications
Inductor(L)	Hammond (195G20)	L=5 mH, r_{dc} = 40 mΩ
Capacitor (C)	Epcos (B33364A5206J050)	20 μF, 440 V
Switches (S_1-S_4)	Infineon (IPP600N25N3)	V_{ds}=250 V, I_d =25 A, R_{ds} = 80 mΩ
Dc bus capacitor	Epcos (B43704B5338M)	450 V, 3300 μF
Loss resistance (r)	–	r_{dc}+2R_{ds} = 0.2 Ω

Table 2. Controller Parameters.

k_p (V/A)	80
k_{r1} (V/Asec)	2,000
k_{r3}(V/Asec)	2,500
k_{r5}(V/Asec)	3,000
k_{r7}(V/Asec)	4,000
ω_{cut1} (rad/sec)	10
ω_{cut3} (rad/sec)	20
ω_{cut5} (rad/sec)	30
ω_{cut7} (rad/sec)	40

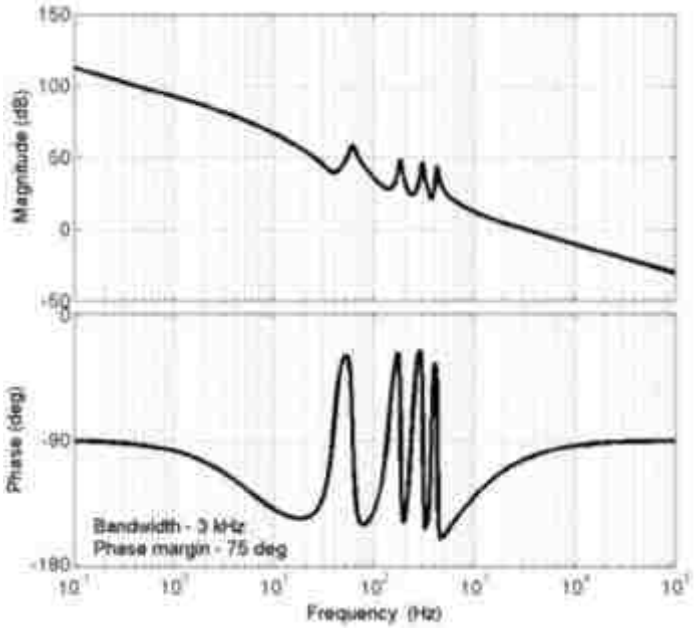

Figure 6. Open loop frequency response of the current controller and plant.

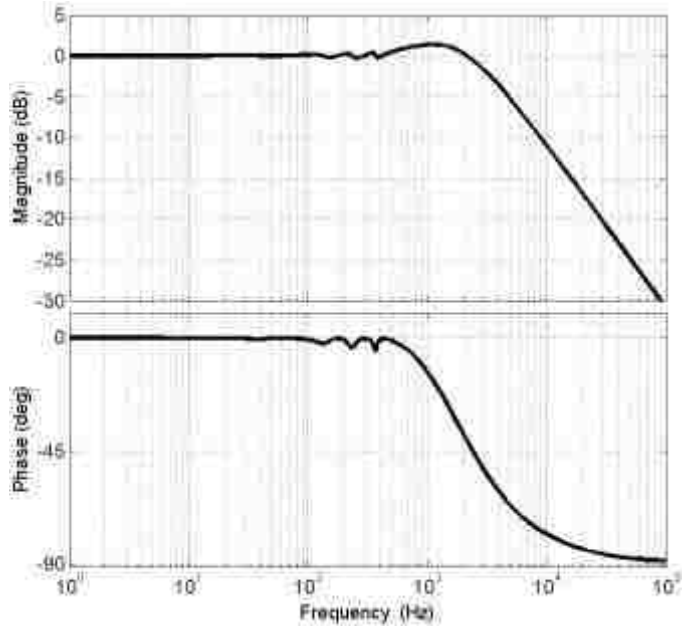

Figure 7. Closed loop frequency response of the current controller and plant.

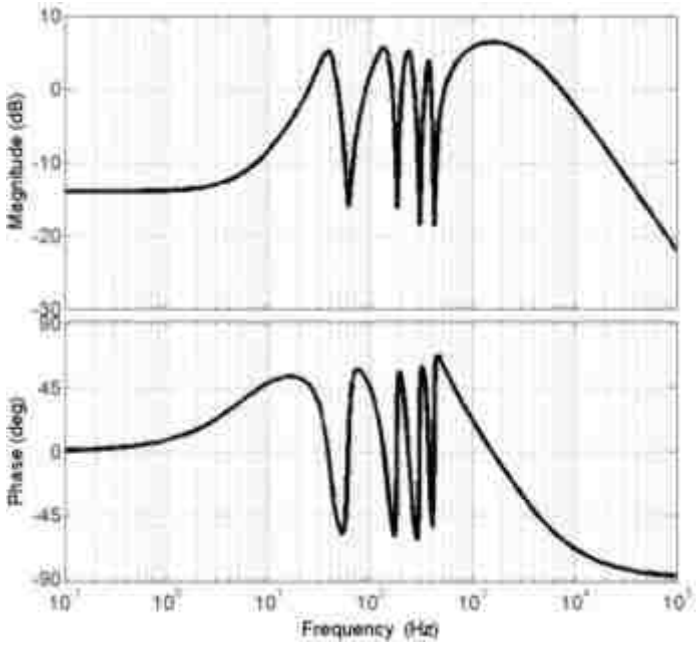

Figure 8. Frequency response of the output impedance.

2.3 Estimation of the Output Filter Capacitance

It can be seen from (6) that the value of i_{cref} is dependent on the value of output capacitance C. An inaccurate estimate of C will cause the output voltage to deviate from the desired reference value. An output voltage rms control loop is proposed to get an estimate of the filter capacitance (see Figure 3). To get the rms value of the output voltage, an estimation of the output voltage is needed. The output voltage estimation is done using the concept of virtual flux [22], [23] . The virtual flux is computed as

$$\psi_{vir} = \int \left(v_i - r_e i_L \right) - L_e i_L \tag{21}$$

where r_e and L_e are the assumed value of the resistance and inductance of the filter inductor. A pure integrator has dc drift problems. Hence the integration in (21) is generally performed by a low pass filter. However, low pass filtering
is always associated with phase lag and attenuation in the gain. A better alternative is to use the filter

$$G_{fil} = \frac{k\omega_{cut}}{s^2 + k\omega_{cut}s + \omega_{ref}{}^2} \tag{22}$$

The filter as shown in (22) is generally used for positive and negative sequence separation [25], [26] and has been used for virtual flux generation in [22]. The virtual flux is multiplied by ω_{ref} to generate the signal vest which is passed through an orthogonal signal generator (OSG) to generate the signal $v_{estquad}$. The OSG is realized using an all pass filter (APF) given as

$$G_{quad} = \frac{\omega_{ref} - s}{\omega_{ref} + s} \tag{23}$$

Thus if $v_{ref} = V_{rekpk}\cos\theta$, then $v_{est} = V_{estpk}\sin\theta_1$ and vestquad $= -V_{estpk}\cos\theta_1$. With the knowledge of vest and $v_{estquad}$, an instantaneous computation of the rms of the estimated voltage can be done. To do so, an operation similar to the scalar product between the reference and estimated voltage is performed. The operation is represented as

$$\langle v_{ref}, v_{est} \rangle = v_{quad} v_{est} - v_{ref} v_{estquad} \tag{24}$$

or,
$$\langle v_{ref}, v_{est} \rangle = V_{refpk} V_{estpk} cos\delta_{err} \tag{25}$$

Where, $v_{quad} = V_{refpk}\sin\theta$, V_{refpk} is the peak value of the reference voltage, V_{estpk} is the peak value of the estimated voltage and δ_{err} is the angle between them. The phase shift between the two voltages occurs if actual resistance r and inductance L in the circuit deviate from the assumed resistance r_e and inductance L_e respectively. However considering the phase shift to be small $\cos\delta_{err} \approx 1$. So (25) can be written as

$$\langle v_{ref}, v_{est} \rangle = V_{refpk} V_{estpk} \tag{26}$$

or,
$$V_{estpk} = \frac{\langle v_{ref}, v_{est} \rangle}{V_{refpk}} \tag{27}$$

With the peak of the estimated voltage known, the rms value of the estimated voltage can be calculated as

$$V_{estrms} = \frac{V_{estpk}}{\sqrt{2}} \tag{28}$$

The rms calculation shown in (28) is valid for sinusoidal waveforms. The calculated virtual flux, ψ_{vir}, in (21) involves an integration which is equivalent to low pass filtering. Hence ψ_{vir} has negligible higher order harmonics. The estimated voltage, vest which is

computed from the ψ_{vir} is thus sinusoidal and can be safely used in (28) to give accurate estimate of the rms component. The rms calculation is demonstrated in Figure 9.

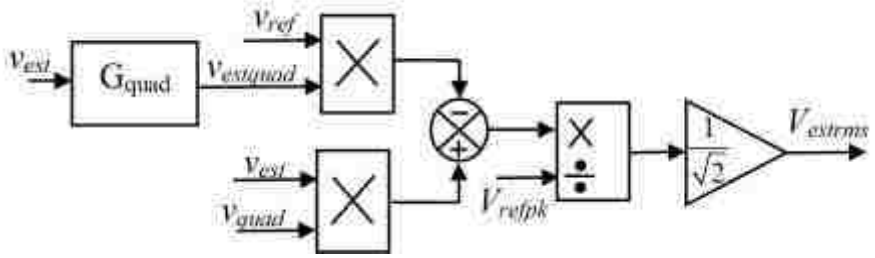

Figure 9. Computation of the rms value for the estimated filter capacitance.

The error between the reference rms value and the estimated rms value is processed by an integral controller as shown in Figure 3. The output of the rms control loop of Figure 3 serves as the additional capacitive susceptance required to converge the estimated rms value with the desired rms value. This output is added to the initial assumed capacitance susceptance. The actual capacitance is now modified to C_{act} to be used in the next cycle for the capacitor current reference generation. The reference capacitor current generation is shown in Figure 10.

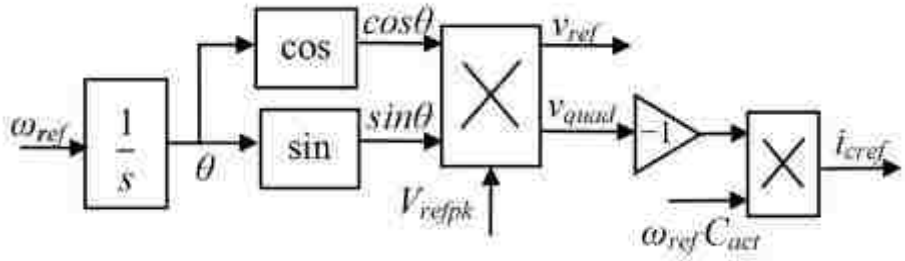

Figure 10. Generation of the reference value for the filter capacitor current.

3. DESIGN GUIDELINES FOR THE RMS CONTROLLER AND SENSITIVITY ANALYSIS

3.1 Modeling the RMS Control Loop

The selection of the parameters of the rms controller can only be done from the knowledge of the corresponding plant. Hence, it is important to have an idea of the plant to design the controller. The output of the rms controller serves as the estimated capacitive susceptance (see Figure 3). To have an idea of the plant, it is necessary to derive a transfer function relating the change in the output rms voltage to the change in the estimated capacitance. To compute the above mentioned transfer function, it is assumed that the current loop is much faster (at least ten times) than the rms voltage control loop and ensures exact tracking of the reference current without any steady state error. The peak value of the output voltage is given as

$$V_{cpk} = \frac{C_{est}}{C} V_{refpk} \tag{29}$$

Again neglecting any deviations in r and L ($r_e = r$, $L_e = L$)

$$V_{cestpk} = V_{cpk} \tag{30}$$

Using (29) and (30), the rms value of the estimated voltage is given as

$$V_{estrms} = \frac{C_{est}}{\sqrt{2}C} V_{refpk} \tag{31}$$

Considering V_{rmsref} to be the rms value of the desired output voltage, the error in the rms voltage is calculated as

$$V_{rmserr} = V_{rmsref} - V_{estrms} \tag{32}$$

or,
$$V_{rmserr} = \frac{V_{refpk}}{\sqrt{2}} - \frac{C_{est}}{\sqrt{2}C} V_{refpk} \tag{33}$$

or,
$$V_{rmserr} = \frac{V_{refpk}}{\sqrt{2}C} C_{err} \tag{34}$$

or,
$$\frac{V_{rmserr}}{C_{err}} = \frac{V_{refpk}}{\sqrt{2}C} \tag{35}$$

The transfer function relating the change in the output rms voltage to the change in the estimated capacitance is given in (35). Equation (35) serves as the plant transfer function for the rms controller. With this plant model, the closed loop representation of the rms controller estimating the capacitance is shown in Figure 11. The controller is taken as a simple integral controller. The frequency response of the loop is shown in Figure 12. Selecting k_{irms} to be 0.03 Ω-1/V the bandwidth is kept at 80 Hz, which is far less than the current control loop.

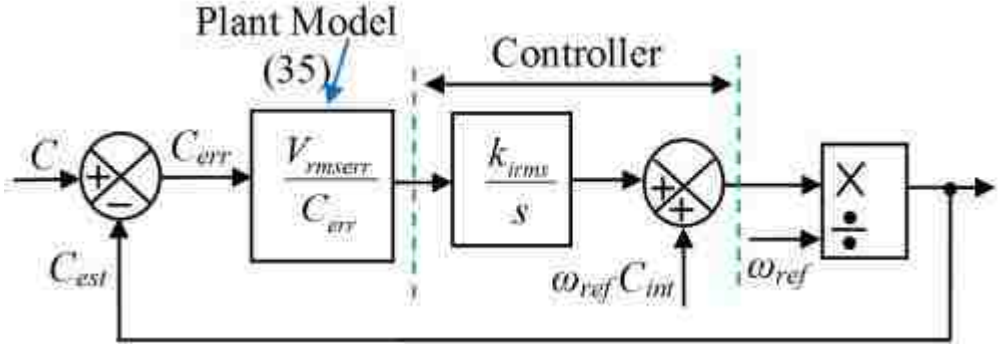

Figure 11. Closed loop representation of the RMS control loop for estimating the output filter capacitance.

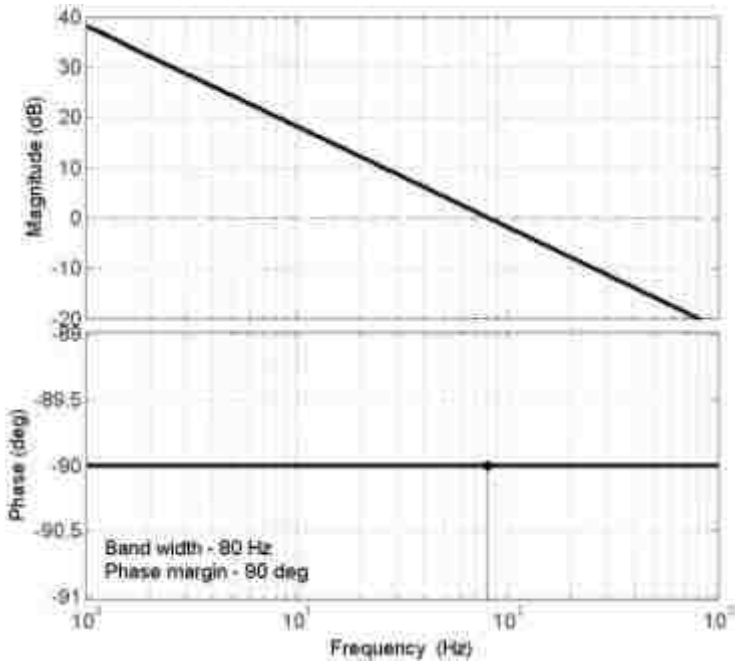

Figure 12. Open loop frequency response of the rms voltage controller and plant.

3.2 Parameter Sensitivity Analysis

It can be seen from (21), that the output voltage is estimated based on the initial assumed values of resistance r_e and inductance L_e of the filter inductor. These parameters change with the circuit operating conditions. The values of the parameters (re and Le) depend on temperature, time (ageing) and the ioperating condition of the converter. Hence, even an accurate initial estimate of the resistance and inductance will not be able to eliminate deviations in the estimated and actual output voltage. This section presents a sensitivity analysis of the actual output voltage rms value to the changes in the resistance and inductance for a 1 kVA inverter at full load conditions. For the analysis we consider the rms voltage control loop and the current control loop to be ideal ensuring no steady state errors. The rms value of the output voltage at steady state can be expressed as

$$V_{rms} = \frac{C_{est}}{C} V_{rmsref} \tag{36}$$

From (36), it can be understood that to find the actual output rms voltage, C_{est} has to be calculated under different load conditions. The detailed derivations are shown in the Appendix. Following the derivations in the Appendix the value of C_{est} is given as

$$\frac{1}{C_{est}} = \begin{bmatrix} \frac{1}{C} + r_{err}\left(\frac{R_L}{C\left(R_L^2 + X_L^2\right)}\right) \\ +\omega L_{err}\left(\frac{X_L}{C\left(R_L^2 + X_L^2\right)} - \omega\right) \end{bmatrix} \tag{37}$$

where, r_{err} is the deviation in the resistance, L_{err} is the deviation in the inductance, R_L is the load resistance and X_L the load reactance. The C_{est} under different loads are computed for variations in r and L. The estimated capacitance as shown in (37) is a function of r_{err} and L_{err}. It can also be observed from (37) that C_{est} depends on the load impedance. Having a knowledge of C_{est} under different loads (from (37)) helps compute the actual output rms V_{rms} (using (36)). The deviations in V_{rms} from the desired reference V_{rmsref} under different load conditions with variations in r and L can then be calculated. The actual rms output voltage under variation in r with L unchanged for different power factor loads is shown in Figure 13. The corresponding plot as obtained from simulations is shown in Figure 14. The plot of the actual rms voltage for variations in L with r unchanged is shown in Figure 15, while the corresponding plot obtained from simulations is shown in Figure 16. It can be observed from the plots that the deviation in the voltage with variations in the resistance increases with the power factor, while the deviation for the variations in the inductance decreases with the increase in the power factor. However in both cases the variations are well within the ±5% limits of the nominal rms voltage as

specified in [1]. The simulated figures (Figure 14 and Figure 16) show similar trajectory as the theoretical figures (Figure 13 and Figure 15). Small deviations are contributed to the fact that the theoretical plots were done assuming that the control loops ensures perfect tracking of reference values with no steady state error (see Appendix). However, in practice the current controller does not ensure perfect tracking of the reference value and will have small steady state error. In addition to the above mentioned assumption, δ_{err} being small, $\cos\delta_{err}$ in (25) was considered to be unity for the theoretical analysis. It should be noted that the plots in Figure 13 and Figure 15 are under rated load condition. Hence these plots present the worst case or maximum voltage deviation. Deviation in the output voltage under any other load is expected to be smaller than those presented in theoretical and simulate plots.

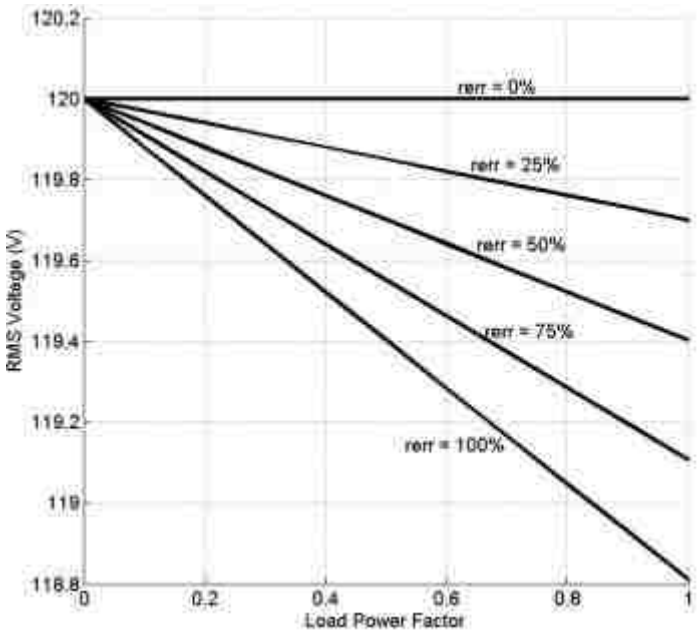

Figure 13. Theoretical rms output voltage with error in the assumed resistance at different load power factor.

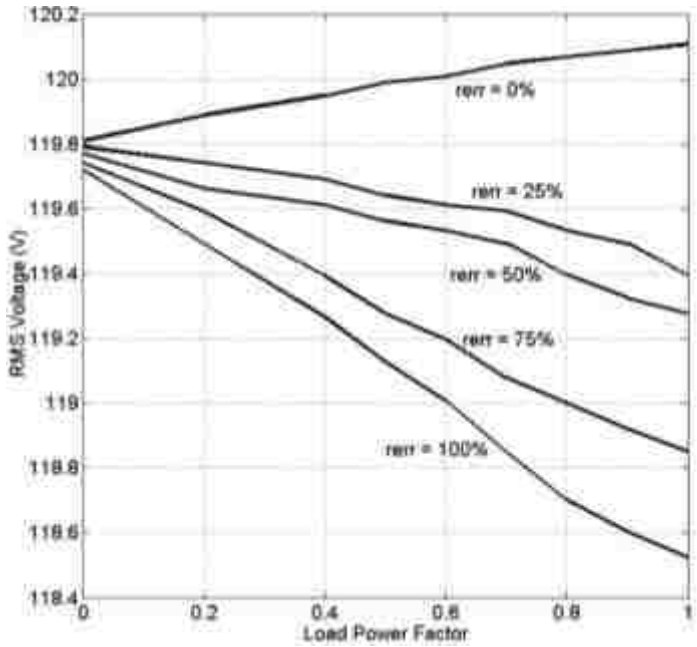

Figure 14. Simulated rms output voltage with error in the assumed resistance at different load power factor.

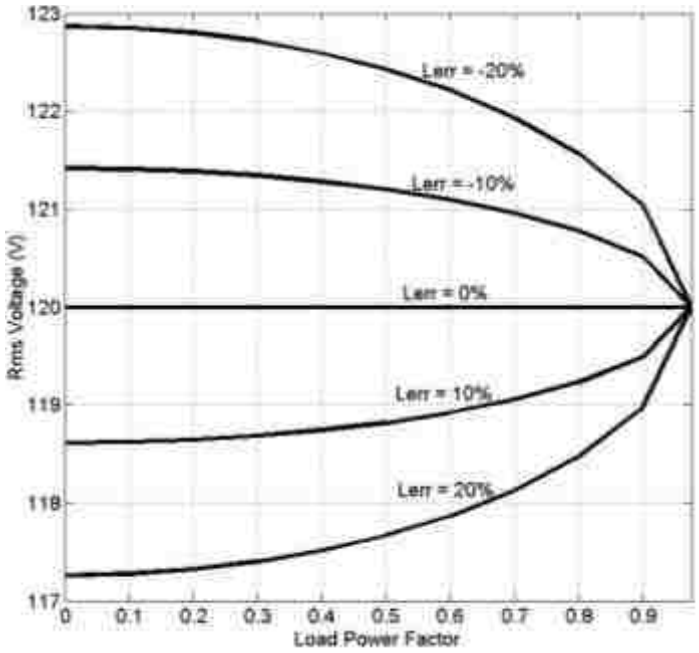

Figure 15. Theoretical rms output voltage with error in the assumed inductance at different load power factor.

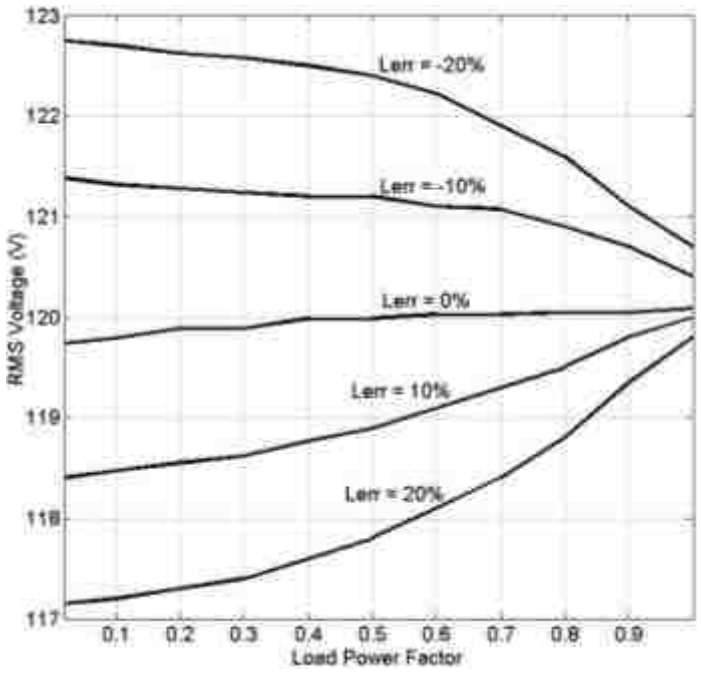

Figure 16. Simulated rms output voltage with error in the assumed inductance at different load power factor.

4. RESULTS AND DISCUSSIONS

4.1 Simulation Studies

The proposed control is verified through preliminary simulations on a on a 400 VA converter in the Simulink/PLECS platform. The power circuit and its load is kept similar to the experimental setup (discussed in the next section). The output voltage and the load current during a transition in linear load from 1 A to 5 A rms are shown in Figure 17, while those for change in nonlinear load are shown in Figure 18.

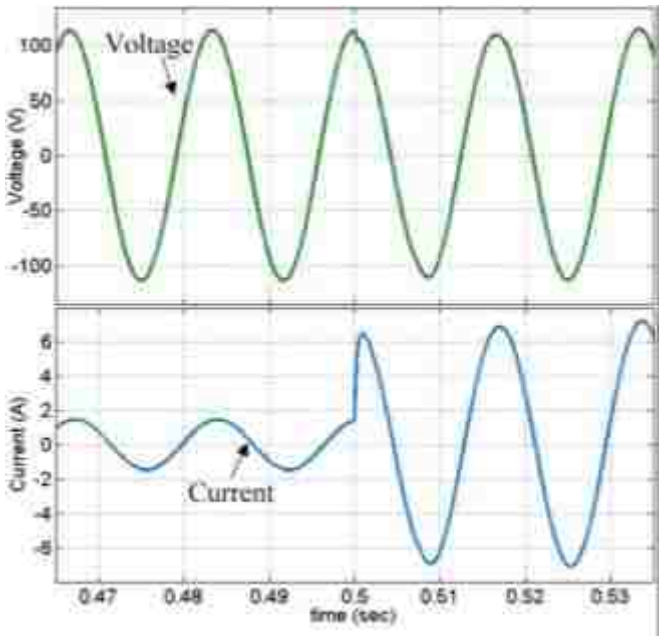

Figure 17. Simulated voltage and load current waveforms during change in linear load.

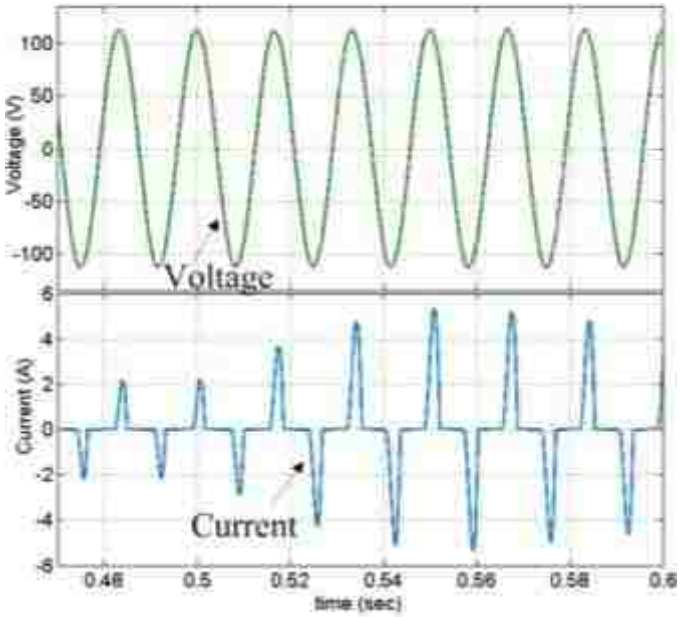

Figure 18. Simulated voltage and load current waveforms during change in nonlinear load.

The waveforms show a stable operation under linear and nonlinear loads with negligible distortions in the load voltage.

4.2 Experimental Verification

The proposed control algorithm is experimentally verified on a 400 VA laboratory prototype. Limitation of the dc power supply in the laboratory restricted the output voltage to 80 V rms value. The circuit parameters details are given in Table 1. Hall effect current sensors (LA-55P) were used to measure the filter inductor and load currents. The control algorithm is implemented in the TMS320F28335 digital signal controller from Texas Instruments. The details on the configuration of the linear and nonlinear loads used for the test are shown in Figure 19.

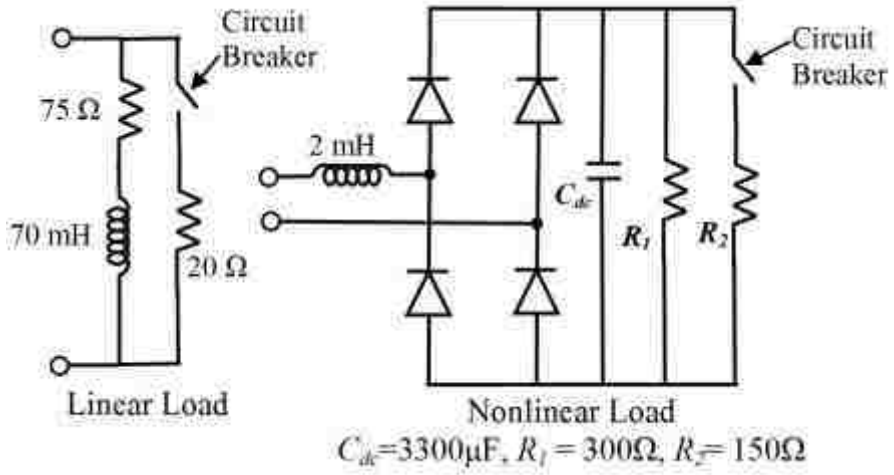

Figure 19. Configuration of the linear and nonlinear loads used for the experimental study.

The controller performance for a step change in the load current from 1 A to 5 A rms is reported in Figure 20. The voltage waveform during a change in nonlinear load is shown in Figure 21. To verify the improvement in the output voltage THD under nonlinear loads, a comparison of the voltage waveform with the proposed scheme and the conventional voltage control scheme is shown in Figure 22. The conventional voltage

control scheme has an outer voltage loop with an inner current loop as shown in Figure 2. The output voltage feed forward term was also added. The control scheme is similar to the one presented in [21]. For the same filter inductor and filter capacitor the values of the bandwidth of the voltage control loop was at 1.8 kHz to achieve the same phase margin of 50 degrees. It can be clearly seen from Figure 22 that the proposed control scheme ensures less distortions in the output voltage with a THD of 1.6% compared to the conventional voltage control scheme which reported a THD of 2.4%. In both cases, the THD results were captured on the spectrum analyzer build in the oscilloscope. The output voltage during the startup of the system with the proposed control scheme is shown in Figure 23. The output voltage shows slight overshoot before settling to its reference of 80 V rms. The load current and estimated capacitance are also shown in Figure 23. The waveforms show a stable startup of the system with the proposed controller. The performance of the controller for a change in the reference voltage (80 V rms to 100 V rms) is shown in Figure 24. The waveforms confirm stable operation with negligible change in the estimated capacitance. The performance of the rms controller in estimating the capacitance is demonstrated in Figure 25. With the inverter operating at steady state, the rms controller was this period the estimated capacitance value was forced to be 16 μF in the software. As seen from Figure 25, with the estimated value not equal to the actual capacitance value, the output voltage deviated from its nominal value of 80 V rms. However, with the rms controller enabled again, the correct value of the estimated capacitance is tracked and the output voltage is brought back to its desired value.

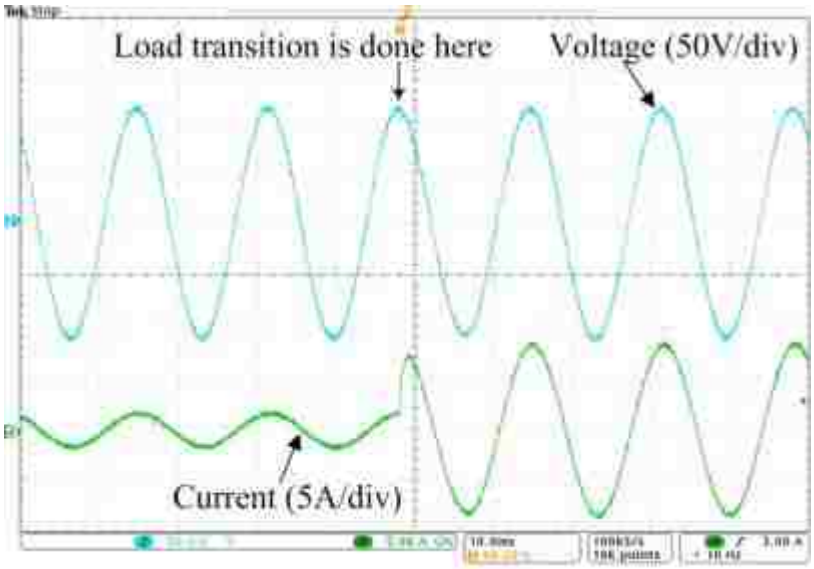

Figure 20. Output voltage and load current waveforms during change in linear load.

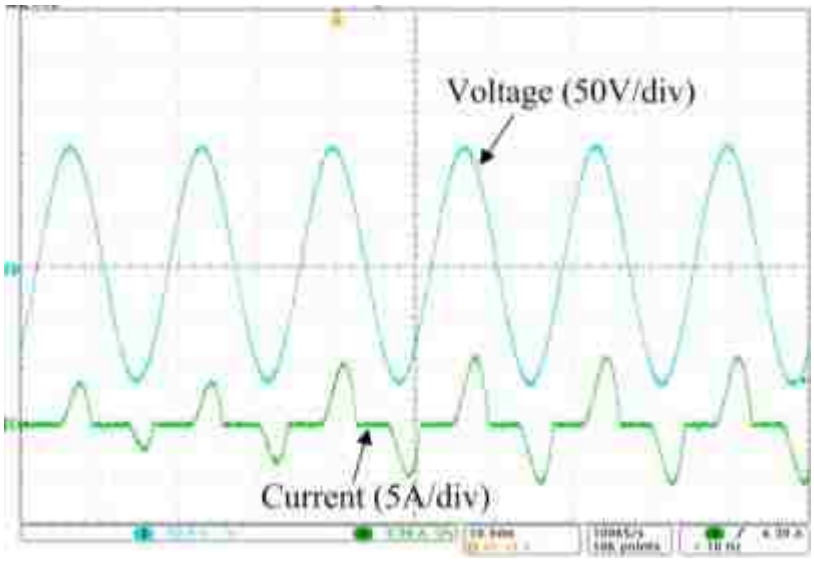

Figure 21. Output voltage and load current waveforms during change in nonlinear load.

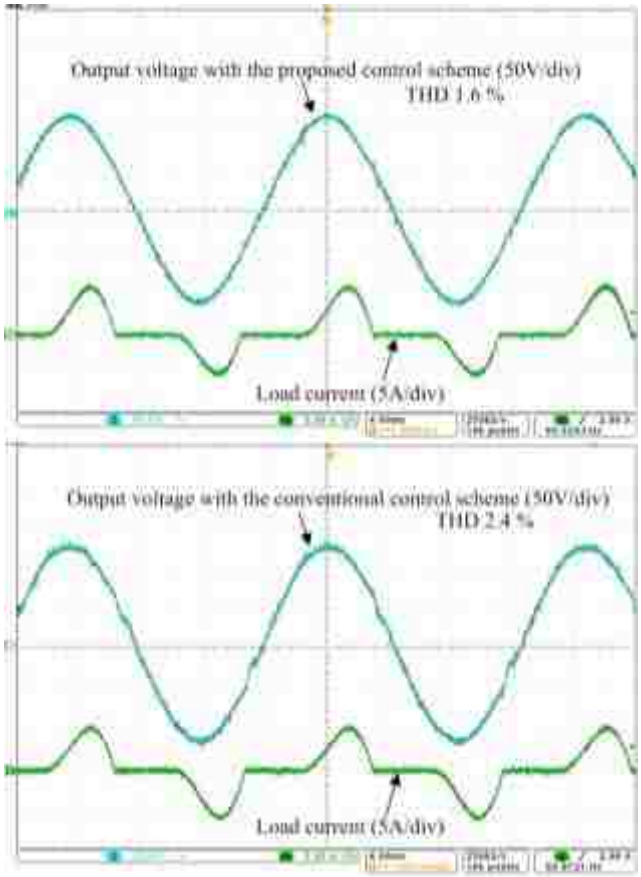

Figure 22. Output voltage under nonlinear load with proposed control scheme (top) and conventional voltage control scheme (bottom).

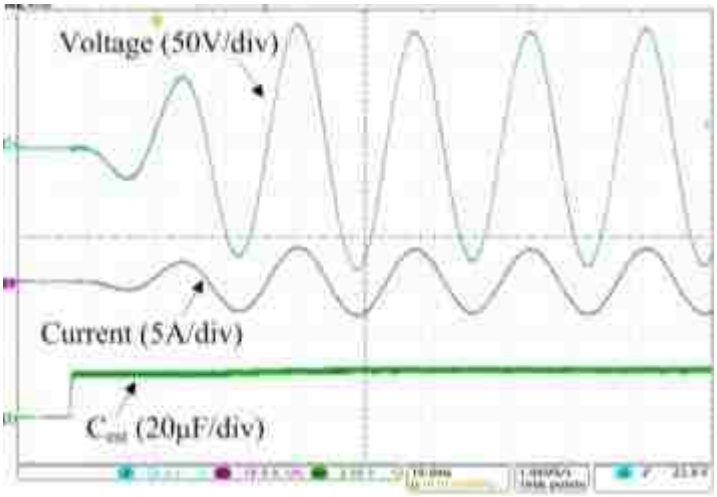

Figure 23. Output voltage, load current and estimated filter capacitance during a startup.

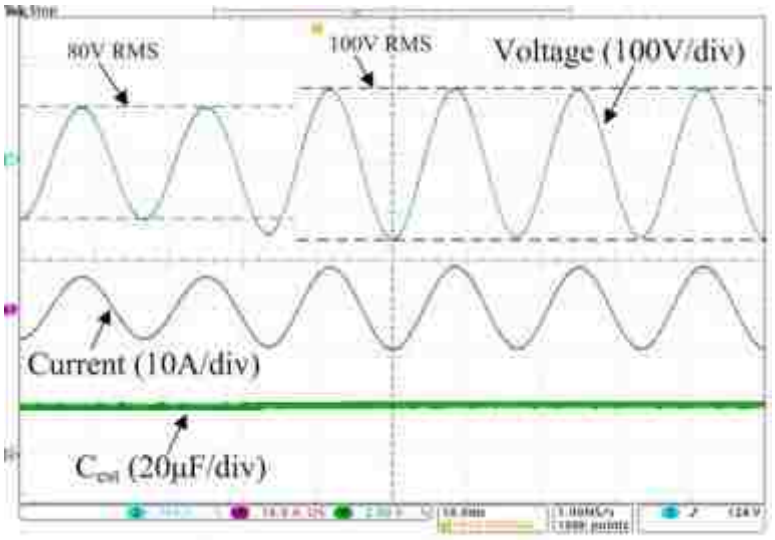

Figure 24. Output voltage, load current and estimated filter capacitance during a change in reference from 80 V rms to 100 V rms.

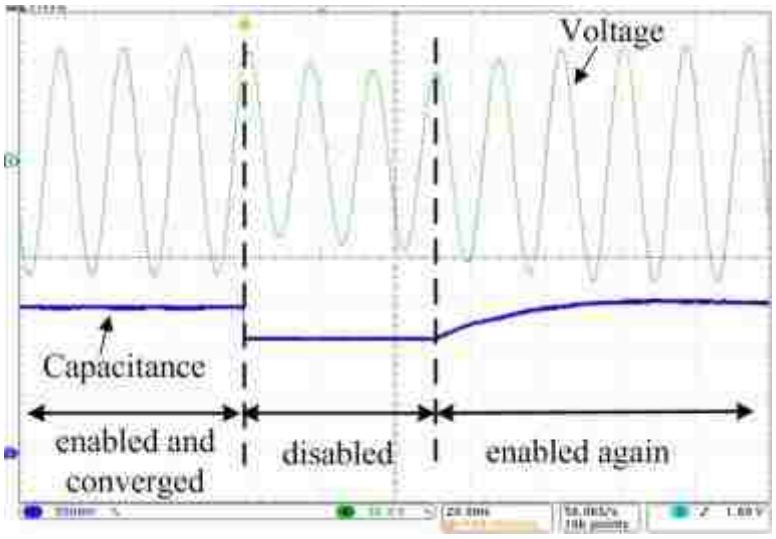

Figure 25. Output voltage and estimated filter capacitance with rms controller disabled for 3 cycles and enabled again (Voltage : 50 V/div, Capacitor : 6.67 μF/div).

Experimental results are also reported to demonstrate the effect of changes in r and L on the output voltage with the proposed control method. From the sensitivity analysis presented in Section 3.2, it is clear that the error in the initial assumed resistance

(r_e) creates maximum deviations in the output voltage near unity power factor operation (Figure 13 and Figure 14) while the error in the assumed filter inductance (L_e) creates maximum deviation near zero power factor operation (Figure 15 and Figure 16). Experiments were performed for these conditions and the results are reported in Figure 26 and Figure 27. Figure 26 shows the rms value of the actual output voltage and the estimated capacitance for error in the resistance at the unity power factor operation. To create the error in the resistance, the assumed resistance (r_e) in the software was changed. The graph of the rms value of the output voltage is similar to the theoretical and simulation results reported in Figure 13 and Figure 14, where near unity power operation the voltage deviations increase with increase in the error (r_{err}). The rms value of the actual output voltage and the estimated capacitance for error in the filter inductance under high inductive loads (power factor 0.1) is shown in Figure 27. The error in the inductance was created by manipulating the value of the assumed inductance (L_e) in the software. The plot of the rms value of the output voltage is similar to the theoretical and simulation results reported in Figure 15 and Figure 16, where at near zero power factor operation, the rms value of the output voltage is greater than the desired reference when L_{err} is negative. However, when the assumed inductance is more than the actual inductance (L_{err} is positive), the actual rms value is less than the desired reference. The estimated capacitance in both cases (Figure 26 and Figure 27) is maintained around the nominal value of 20 μF by the rms controller. Voltage deviations are within the acceptable range of ±5% of the nominal value of 80 V.

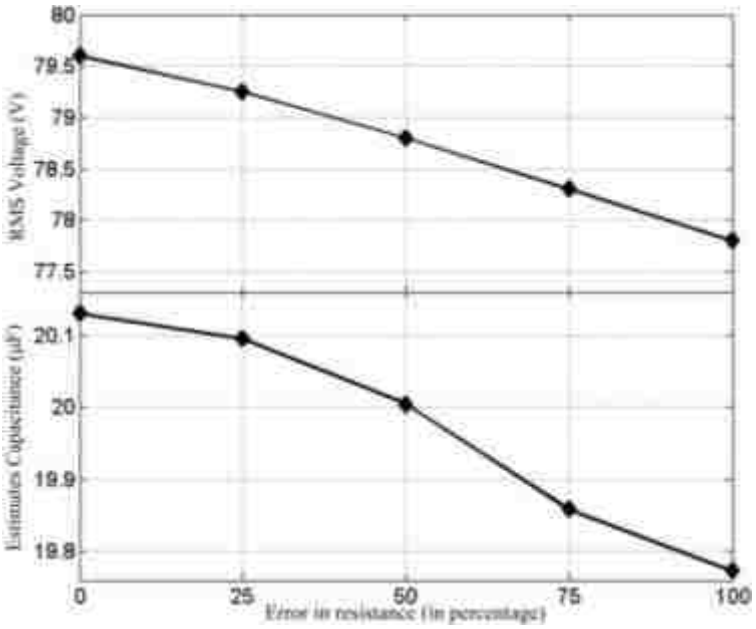

Figure 26. The actual rms voltage and estimated capacitance for different r_{err} (%) at unity power factor operation.

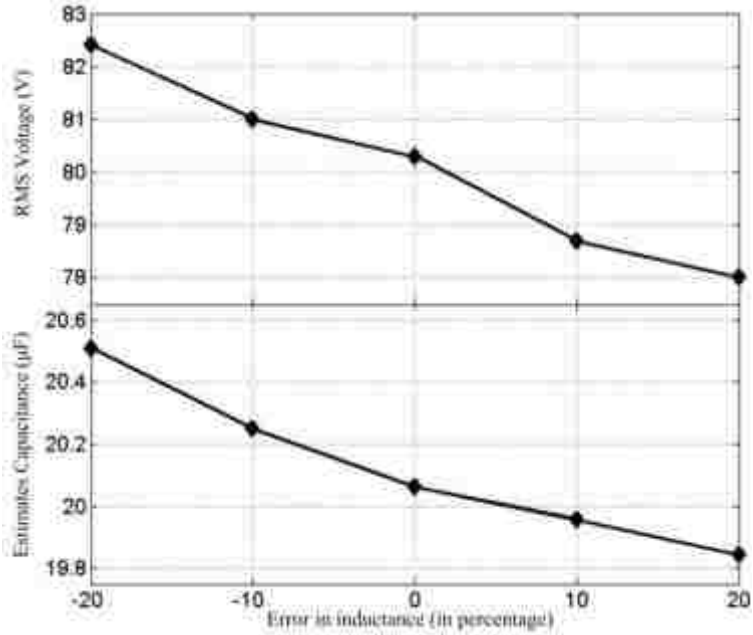

Figure 27. The actual rms voltage and estimated capacitance for different L_{err} (%) under highly inductive load (load power factor 0.1).

5. CONCLUSION

This paper presents a scheme to control a single-phase standalone inverter without an output voltage sensor. The control approach, mainly based on the output capacitor current control is analyzed thoroughly. The system modeling is presented and a controller structure is proposed and designed based on the model. It is demonstrated that the presented control approach ensures better THD of the output voltage under nonlinear load conditions compared to conventional voltage control approach achieving a THD as low as 1.6%. The estimation of the output filter capacitance based on the output voltage rms control loop is also discussed. The output voltage estimation is done based on the virtual flux method. It is shown that the method is largely insensitive to the filter inductor resistance and inductance variations, keeping the output voltage within regulation specifications. Experimental results presented support the validity of the proposed control scheme.

APPENDIX

The derivation of the estimated capacitance C_{est}, due to the variations in r and L is presented below. For simplicity the calculations are present in a fictitious synchronous (d-q) frame of reference attached to the output voltage considering that the rms voltage control loop and the current loop ensures perfect reference tracking. Since we are interested in finding the deviation in the steady state voltage under parameter fluctuations, all equations reported below are at steady state neglecting any dynamics. The subscripts d and q in the following equations represent the corresponding d axis and

q axis quantities.

For a given controller output voltage V_i, the steady state voltage across the filter capacitor, V_c in the *d-q* coordinates is given as

$$V_{id} = rI_{Ld} - \omega LI_{Lq} + V_{cd} \tag{A1}$$

$$V_{iq} = rI_{Lq} + \omega LI_{Ld} + V_{cq} \tag{A2}$$

whereas the corresponding estimated voltage V_{est} is given as

$$V_{id} = r_e I_{Ld} - \omega L_e I_{Lq} + V_{estd} \tag{A3}$$

$$V_{iq} = r_e I_{Lq} + \omega L_e I_{Ld} + V_{estq} \tag{A4}$$

Using (A1) and (A2) in (A3) and (A4) leads to

$$V_{estd} = r_{err} I_{Ld} - \omega L_{err} I_{Lq} + V_{cd} \tag{A5}$$

$$V_{estq} = r_{err} I_{Lq} + \omega L_{err} I_{Ld} + V_{cq} \tag{A6}$$

where, $$r_{err} = r - r_e \text{ and } L_{err} = L - L_e \tag{A7}$$

Now, for a given C_{est}, the reference of the output capacitor current in the *d-q* coordinates is given as

$$I_{cdref} = -\omega C_{est} V_{refq} \tag{A8}$$

$$I_{cqref} = \omega C_{est} V_{refd} \tag{A9}$$

While the output voltage is actually given as

$$V_{cd} = \frac{I_{cq}}{\omega C} \tag{A10}$$

$$V_{cq} = -\frac{I_{cd}}{\omega C} \tag{A11}$$

In the *d-q* coordinates $V_{dref} = V_{refpk}$, $V_{qref} = 0$. Considering the current controller is ensuring perfect tracking under steady state conditions, $I_{cd} = I_{cdref} = 0$, $I_{cq} = I_{cqref}$ and $V_{cq} = 0$.

$$V_{cd} = \frac{C_{est}}{C} V_{dref} \tag{A12}$$

$$V_{cq} = \frac{C_{est}}{C} V_{qref} \tag{A13}$$

For a load impedance of $Z = R_L + jX_L$, the load current I_o is given as

$$V_{cd} = R_L I_{od} - X_L I_{oq} \tag{A14}$$

$$V_{cq} = R_L I_{oq} + X_L I_{od} \tag{A15}$$

Solving (A14) and (A15), for I_{od} and I_{oq}

$$I_{od} = \frac{R_L V_{cd}}{R_L^2 + X_L^2} \tag{A16}$$

$$I_{oq} = \frac{-X_L V_{cd}}{R_L^2 + X_L^2} \tag{A17}$$

The inductor current I_L can now be found as

$$I_{Ld} = I_{od} + I_{cd} = \frac{R_L V_{cd}}{R_L^2 + X_L^2} \tag{A18}$$

$$I_{Lq} = I_{oq} + I_{cq} = \frac{-X_L V_{cd}}{R_L^2 + X_L^2} + \omega C_{est} V_{refd} \tag{A19}$$

The rms control loop ensures that $V_{estd} = V_{refpk}$. Using (A18), (A19), (A12) in (A5) C_{est} turns out as

$$\frac{1}{C_{est}} = \begin{bmatrix} \frac{1}{C} + r_{err}\left(\frac{R_L}{C\left(R_L^2 + X_L^2\right)}\right) \\ +\omega L_{err}\left(\frac{X_L}{C\left(R_L^2 + X_L^2\right)} - \omega\right) \end{bmatrix} \tag{A20}$$

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II. GRID VOLTAGE ESTIMATION AND CURRENT CONTROL OF A SINGLE PHASE GRID CONNECTED CONVERTER WITHOUT GRID VOLTAGE SENSOR

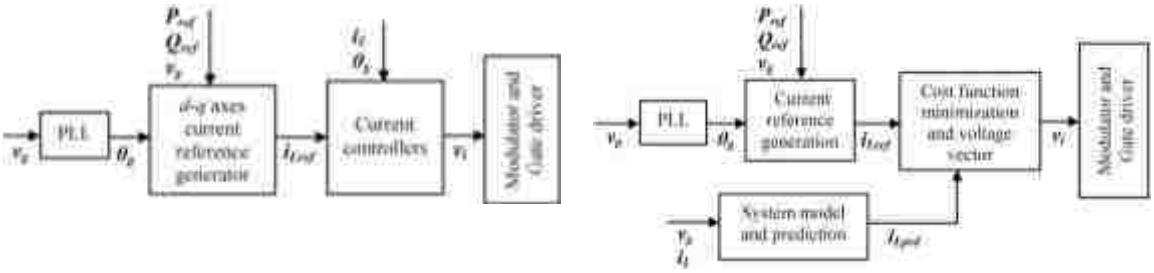
ABSTRACT

This paper investigates the possibility of estimating the grid voltage and controlling a single-phase grid connected converter without a dedicated grid voltage sensor. The main focus is given to current controlled architectures which need phase locked loops (PLL) for their operation. The grid voltage estimation method is proposed based on the active and reactive power delivered by the converter to the grid. In addition to the estimation of the grid voltage, the proposed method also generates the unit vectors and frequency information similar to a conventional PLL structure. The influence of various parameters like the dead-time, equivalent loss resistance, and the filter inductance on the proposed estimation method is studied in details. Experimental results validate the feasibility of the proposed scheme.

1. INTRODUCTION

With the widespread use of renewable energy sources, the application of single-phase grid connected power electronic converter is gaining popularity. The commonly used control approach for such converters is the current controlled method (see Figure 1(a)) which aims to control the active and reactive powers by controlling the current supplied to the grid [1]-[3]. The control scheme requires the accurate phase information of the fundamental component of the grid voltage [1]-[3]. This information is

obtained from a phase locked loop (PLL) which has the grid voltage as its input and generates the frequency and phase information (in the form of unit vectors) as its outputs [4]. Proposing accurate and improved PLL structures is a popular area of research and a few are reported in [4]-[9]. However, irrespective of the type of the PLL used, generally all PLLs use a voltage sensor to sense the grid voltage. Further, in the inverter mode of operation, the references for the output currents are generated from the knowledge of the grid voltage. So, the current controlled architecture is very much dependent on the accurate knowledge of the grid voltage for its operation. Similar to the current control approach, other popular control approaches for grid connected converter like the Model Predictive Control (MPC) approach [10]-[12] also needs the information of the grid voltage. MPC focuses on selecting the switching state which optimizes a desired cost function (see Figure 1(b)). The accuracy of the MPC approach relies on having an accurate plant model, which in the case of grid connected converters is dependent on the grid voltage.



(a) (b)

Figure 1. Control structure for (a) current controlled VSC, (b) VSC controlled by MPC.

Irrespective of the control structure used for the grid connected converter, it can be observed that knowledge of the grid voltage is essential for most of them. The grid

voltage is generally measured using a voltage sensor. The converter current is generally measured locally just after the converter bridge. However, in situations where the grid is physically far from the converter, installing the grid voltage sensor may not be feasible. In such cases elimination of the grid voltage sensor reduces additional circuitry and wiring requirements. From the hardware point of view elimination of the voltage sensor leads to a compact design and reduces the overall cost. Further, when the converter is physically distant from the grid, the cable connecting the sensor to the controller may be physically damaged. In such situations, sensorless operation adds to the reliability of the overall system. However, any control architecture without a voltage sensor must ensure very accurate and stable estimation of the grid voltage.

Grid voltage sensorless control approaches have been proposed in the literature [13]-[19]. The estimation method presented in [13] is only applicable for unity power factor operation. Further, stable operation is ensured only under certain load conditions. The estimated method presented in [14] involves a derivative operation on the current. However, the derivative operation is prone to noise which increases the distortions in the control loop. An improved estimation of the voltage vector is presented in [23] where the concept of virtual flux is used to estimate the grid voltage. Infact, the most common method of grid voltage estimation without a grid voltage sensor is the virtual flux based estimation [23]-[19]. The virtual flux based estimation method involves an integration operation. A pure integrator has dc drift problems. Hence the integration is generally performed by a low pass filter. However, low pass filtering is always associated with phase lag and attenuation in the gain. Moreover, all virtual flux based voltage estimators neglect the resistive drop in the circuit. The basis of this assumption is that the winding

resistance of the filter inductor is very small. However, it must be remembered that this resistance is the equivalent loss representing the total losses of the switches in the converter bridge, the winding resistance of the filter inductor, and the resistance of the connecting cables. Furthermore, virtual flux based estimation also neglects variations in the filter inductance. Virtual flux based voltage estimation has been limited to direct power control (DPC) or MPC which do not need a PLL. However, to the best knowledge of the authors, sensorless PLL generation and its impact on the current control approach for the control of grid-connected inverters has not been discussed in the literature.

Distinctly, this paper presents a grid voltage sensorless estimation method which estimates the fundamental component of the grid voltage as well as generates the information of phase, frequency, and unit vectors without the need of an additional PLL structure. As demonstrated with theory and supporting results, the proposed sensorless method gives accurate estimation of the phase (and unit vectors) even under distorted grid conditions. As with the virtual flux based estimation, the proposed estimation method depends on the inductance and equivalent loss resistance. Addressing this issue, the effect of the parameter variation on the proposed estimation method is studied in detail. Experimental results are provided which show the effective performance of the proposed grid voltage estimation scheme. The rest of the paper is arranged as follows. The proposed estimation with the corresponding system modeling and controller design is presented in Section 2. A detailed analysis on the effect of the dead time and variations of system parameters on the proposed estimation is presented in Section 3. Experimental results are discussed in Section 4, while the conclusion is presented in Section 5.

2. CONTROL ARCHITECTURE

2.1 Proposed Estimation of the Grid Voltage and Unit Vector Generation Without a Voltage Sensor

A grid connected inverter is shown in Figure 2. In this figure, L is the filter inductance, r is the equivalent loss resistance, i_L is the filter inductor current, v_g is the voltage of the grid. It should be noted that only the inductor current, i_L, is measured. The corresponding equivalent circuit of Figure 2 is shown in Figure 3. The values of the loss resistance and inductance used in the control algorithm may be different from the actual values in the circuit. Considering r_e and L_e as the expected values of the loss resistance and inductance, voltage v_{i1} is calculated as

$$v_{i1} = v_i - i_L r_e \tag{1}$$

In (1), loss resistance r_e represents the ohmic loss of the switches, the losses in the filter inductor and connecting cable, and the voltage drop due to the dead-time effect (modeled in the next section). The overall block diagram of the proposed control technique is shown in Figure 4. In the figure, P_{ref} is the active power reference, Q_{ref} is the reactive power reference, i_{Lref} is the reference value of the inductor current, G_c represents the current controller, v_i is the output of the current controller, V_g^1 is the peak values of the fundamental component of the estimated grid voltage, $\cos\theta$ and $\sin\theta$ are the unit vectors obtained from the proposed grid voltage estimation algorithm. The control diagram shown in Figure 4 is identical to conventional current control architectures except for the PLL being replaced with the proposed voltage sensorless estimation algorithm. The proposed estimation algorithm is discussed in details below.

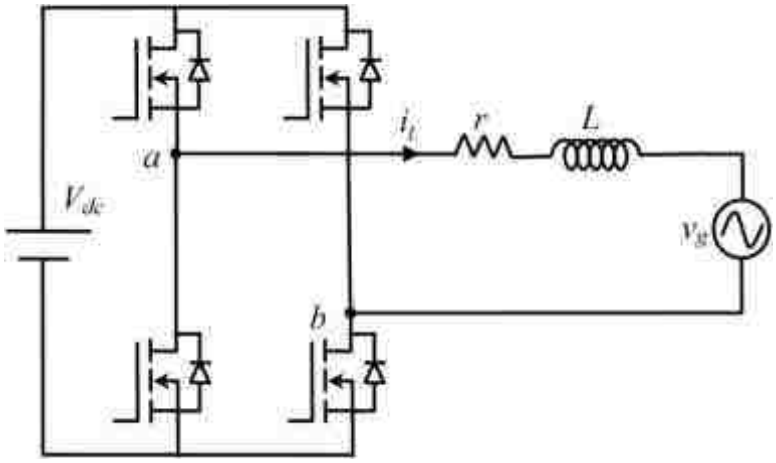


Figure 2. A single-phase grid connected inverter.

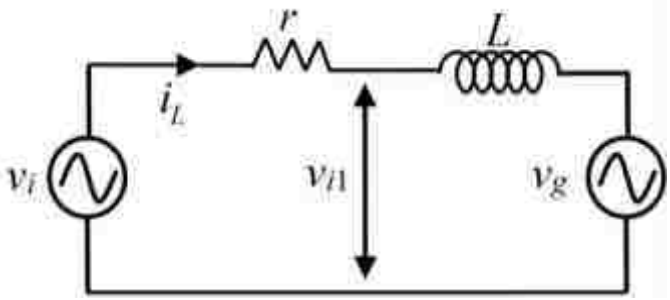


Figure 3. Single line equivalent diagram of the circuit in Figure 1.

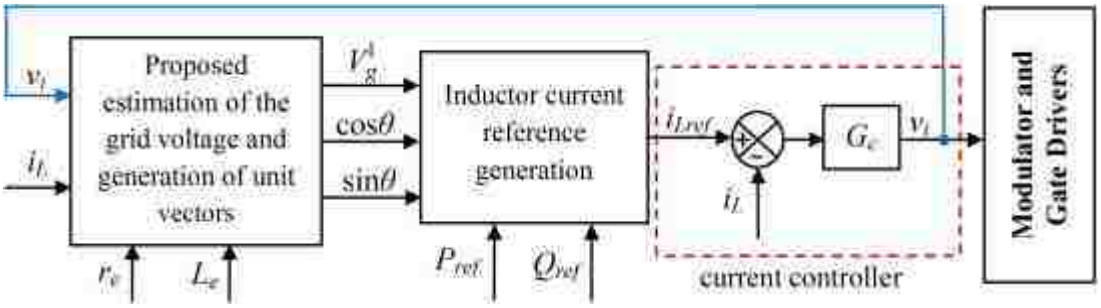


Figure 4. Overall control block diagram.

The proposed voltage estimation method is based on model reference adaptive control (MRAC) based estimation structure. The MRAC technique is popularly used for parameter estimations in control systems. In the field of power electronics, MRAC based estimators have been successfully used for estimating the speed in sensorless drive systems. The control structure is well established for cage rotor [20]-[23], doubly fed induction [24], [25] and permanent magnet machines [26], [27]. Recent examples of application of MRAC based parameter estimation for grid connected converters are found in [30], [31] where the technique is used to estimate the parameters of an inverter. Examples of application of MRAC approach for converter control are presented in [32], [33]. The concept of the classic MRAC based estimation is briefly discussed here. The typical schematic of a MRAC system is shown in Figure 5. The system consists of a reference system, an adjustable system, and a compensator. The fundamental concept of the MRAC scheme is to process the error between F_1 and F_2 to generate the unknown parameter, which is then fed back to the adjustable system. A properly designed controller will eventually converge the error between F_1 and F_2 to zero, thereby matching unknown parameter x with its actual value in the system.

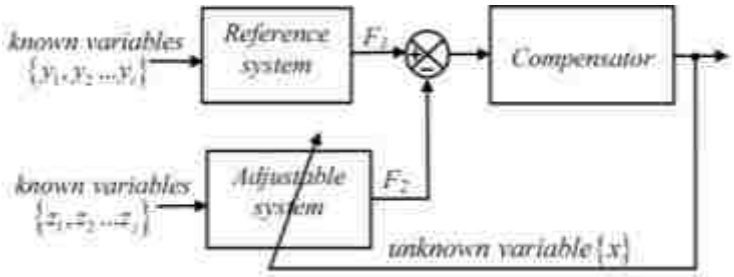


Figure 5. Basic structure of an MRAC system.

Active and reactive power based MRAC structures will be used to estimate the grid voltage. For the instantaneous computation of the average power in a single-phase system, the active and reactive powers are calculated in a fictitious two phase ($\alpha\beta$) frame of reference. The in-phase (α axis) and quadrature (β axis) signals are generated using second order generalized integrators (SOGI) [34], [35].The SOGI structure consists of two filters given as

$$G_{phase} = \frac{k\omega s}{s^2 + k\omega s + \omega^2} \tag{2}$$

$$G_{quad} = \frac{k\omega^2}{s^2 + k\omega s + \omega^2} \tag{3}$$

The SOGI structure implementing the transfer functions in (2) and (3) is shown in Figure 6 where X_{ph} and X_{quad} are the in-phase and quadrature components of any arbitrary input X. Each of the signals v_{i1} and i_L is passed through the SOGI structure tuned at the fundamental frequency (see Figure 7) to generate the corresponding in-phase and quadrature fundamental components $v^1_{i1\alpha}$, $v^1_{i1\beta}$, $i^1_{L\alpha}$, and $i^1_{L\beta}$, respectively. It should be noted that the SOGI structure also helps to extract the corresponding fundamental components.

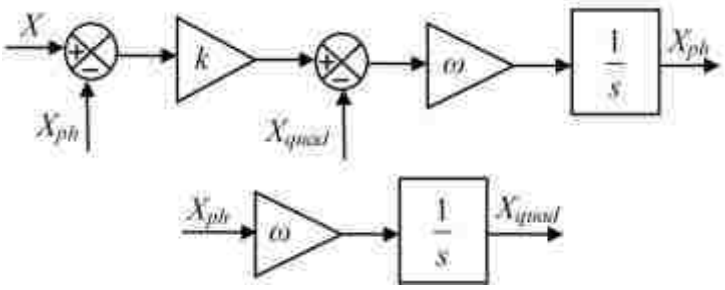


Figure 6. The SOGI structure.

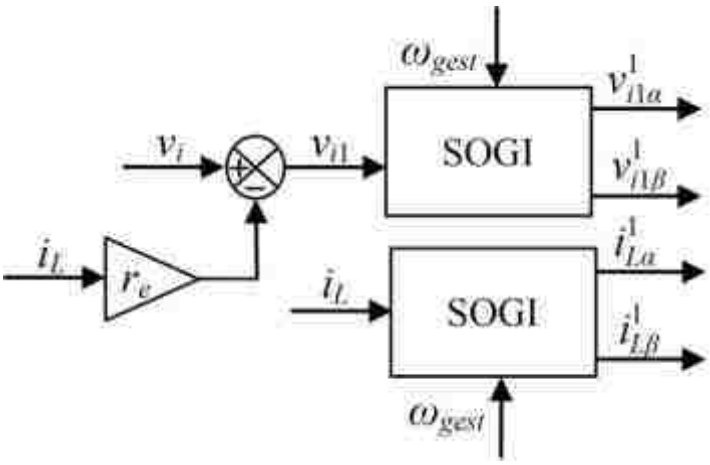


Figure 7. Generation of the in-phase (α) and quadrature (β) components.

Once the in-phase and quadrature components are known, the active and reactive power based MRAC estimation method is presented next. In the $\alpha\beta$ frame of reference active power P_1 and reactive power Q_1 delivered by the fundamental component of v_{i1} are given as

$$P_1 + jQ_1 = \frac{1}{2}\left[\left(v_{i1\alpha}^1 + jv_{i1\beta}^1\right)\times\left(i_{L\alpha}^1 - ji_{L\beta}^1\right)\right] \tag{4}$$

Separating the real and imaginary components

$$P_1 = \frac{1}{2}\left(v_{i1\alpha}^1 i_{L\alpha}^1 + v_{i1\beta}^1 i_{L\beta}^1\right) \tag{5}$$

and

$$Q_1 = \frac{1}{2}\left(v_{i1\beta}^1 i_{L\alpha}^1 - v_{i1\alpha}^1 i_{L\beta}^1\right) \tag{6}$$

The factor of 0.5 appearing in (4)-(6) is needed to keep the active and reactive power unchanged in both the frame of reference. At the same time, the active and reactive power supplied from source v_{i1} to v_g (considering fundamental components only) connected through a pure inductance L (see Figure 3) are given as [37]

$$P_2 = \frac{V_{i1}^1 V_g^1 \sin\delta}{2X_e} \tag{7}$$

$$Q_2 = \frac{V_{i1}^1}{2X_e}(V_{i1}^1 - V_g^1 \cos\delta) \tag{8}$$

where, $v_{i1}^1 = V_{i1}^1 \angle \varepsilon$, $v_g^1 = V_g^1 \angle \varepsilon - \delta$ and $X_e = \omega_{gest} L_e$

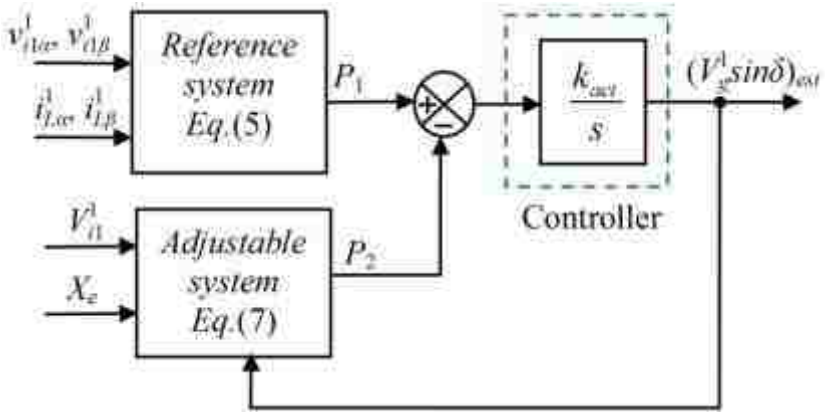


Figure 8. MRAC structure to estimate $V_g^1 \sin\delta$.

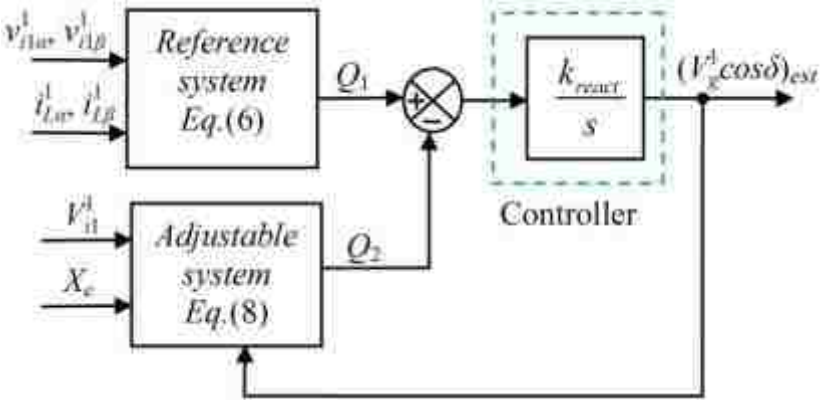


Figure 9. MRAC structure to estimate $V_g^1 \cos\delta$.

In (7) and (8) V_{i1}^1 and V_g^1 are the peak values of the fundamental component of voltage vectors v_{i1} and v_g, respectively while δ is the angle between the fundamental component of v_{i1} and v_g. Oberving (5), it can be seen that all the variables on the right side of the equation are known or can be computed. Similarly all variables in (7) are also known except the term $V_g^1\sin\delta$ (as the grid voltage is unknown). Using the concept of MRAC based estimation, $V_g^1\sin\delta$ can be estimated as shown in Figure 8, where P_1 forms the reference variable and P_2 the adjustable variable. The reference model is given by (5), while the adjustable model is given by (7). Exactly similar structure is used to estimate $V_g^1\cos\delta$, where Q_1 forms the reference variable and Q_2 the adjustable variable. Here, (6) serve as the reference model and (8) as the adjustable model. The estimation of $V_g^1\cos\delta$ is shown in Figure 9. An integral controller is chosen as the desired controller in each case.

The estimated values $(V_g^1\sin\delta)_{est}$ and $(V_g^1\cos\delta)_{est}$ help to give an estimate of the fundamental component of the grid voltage v_g as discussed below. It should be remembered that δ is the angle between v_g^1 and v_{i1}^1 (see Figure 10). Angle ε being known, angle θ can be easily computed. The unit vectors $\cos\varepsilon$ and $\sin\varepsilon$ can be found as

$$\cos\varepsilon = \frac{v_{i1\alpha}^1}{V_{i1}^1} \text{ and } \sin\varepsilon = \frac{v_{i1\beta}^1}{V_{i1}^1} \tag{9}$$

where
$$V_{i1}^1 = \sqrt{\left(v_{i1\alpha}^1\right)^2 + \left(v_{i1\beta}^1\right)^2} \tag{10}$$

Again, unit vectors $\cos\delta_{est}$ and $\sin\delta_{est}$ are found as

$$\cos\delta_{est} = \frac{\left(V_g^1\cos\delta\right)_{est}}{V_{gest}^1} \text{ and } \sin\delta_{est} = \frac{\left(V_g^1\sin\delta\right)_{est}}{V_{gest}^1} \tag{11}$$

where
$$V_{gest}^1 = \sqrt{\left((V_g^1\cos\delta)_{est}\right)^2 + \left((V_g^1\sin\delta)_{est}\right)^2} \tag{12}$$

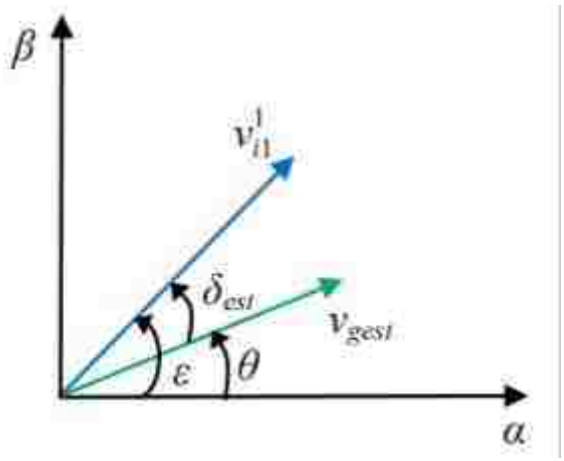


Figure 10. Representation of the different voltage vector in the α-β frame of reference.

Angle θ can be expressed as $\varepsilon - \delta_{est}$ (see Figure 10). Unit vectors $\cos\theta$ and $\sin\theta$ are then computed as

$$\cos\theta = \cos\varepsilon\cos\delta_{est} + \sin\varepsilon\sin\delta_{est} \tag{13}$$

$$\sin\theta = \sin\varepsilon\cos\delta_{est} - \cos\varepsilon\sin\delta_{est} \tag{14}$$

Unit vectors $\cos\theta$ and $\sin\theta$ as in (13) and (14) are same as the unit vectors generated from a conventional PLL structure. These unit vectors are needed to generate current references in current controlled architectures and to transform any quantity from the stationary frame of reference to the synchronous frame of reference attached to the grid voltage vector. The fundamental component of the grid voltage can now be found as

$$v_{gest} = V_{gest}^1\cos\theta \tag{15}$$

The grid frequency (in rad/sec) can be estimated from the unit vectors $\cos\theta$ and $\sin\theta$ as shown below

$$\omega_{gest} = \cos\theta\frac{d\sin\theta}{dt} - \sin\theta\frac{d\cos\theta}{dt} \tag{16}$$

The expression of ω_{gest} as obtained from (16) is passed through a low pass filter to remove any high frequency noise in it. The filtered value of ω_{gest} can be used to update the frequency in the SOGI structure (see Figure 6 and Figure 7) and to update the value of X_e in (7) and (8). From the theory and analysis presented in this section it can be concluded that the proposed estimation method gives an estimation of the fundamental component of the grid voltage, the unit vectors and the grid frequency.

The estimated grid voltage and unit vectors are used to generate the reference for the inductor current from the reference values of the active and reactive power (see Figure 4). Conventional feedback current control [2], [38]−[40] is used to control the current delivered by the converter to the grid. A well designed current controller ensures that the actual inductor current tracks the desired reference value. For a single-phase system, proportional resonant controller, with resonant peaks at the fundamental and dominant harmonic frequencies is employed to track current reference i_{Lref}. The current controller is given as

$$G_c = k_p + \sum_{n=1,3,5,7\ldots} \frac{k_{rn}\omega_{cutn}s}{s^2 + 2\omega_{cutn}s + (n\omega)^2} \tag{17}$$

In (17) k_p is the proportional gain, k_{rn} is the resonant gain and ω_{cutn} is the cutoff frequency of the resonant controller at the n^{th} harmonic frequency. The reference generation and details on the current controller is not the focus of this paper. The details can be found in [2], [38]−[40]. The important plant and current controller parameters are listed in Table 1. In Table 1, T_{sw} is the switching period, T_{del} is the dead-time used to prevent simultaneous switching of the switches in the same phase leg of the converter, and V_{dc} is the dc bus voltage. The frequency response of the current controller and the plant is shown in Figure 11. It is important for the controller to ensure sufficiently high gains at the fundamental

(60 Hz) and desired harmonic frequencies. It should be noted that in a single phase system the third, fifth and seventh harmonics are most dominant. The resonant gains are chosen such that the loop gain at the fundamental, third, fifth and seventh harmonic frequency is at least 40 dB. Such high gains ensure negligible steady state error. For the chosen controller parameters the crossover frequency was at 2 kHz with phase margin of 74 degrees. It can be also checked that the phase delay introduced by the sampling and hold effect for a switching frequency of 20 kHz is less at the crossover frequency of 2 kHz.

Table 1. System and Controller Parameters.

L (mH)	5
r (Ω)	0.4
T_{del} (μsec)	0.5
T_{sw} (μsec)	50
V_{dc} (V)	150
k_p (*V/A*)	50
k_{r1} *(V/Asec)*	1,000
k_{r3} *(V/Asec)*	1,500
k_{r5}*(V/Asec)*	2,000
k_{r7}*(V/Asec)*	3,000
ω_{cut1} (*rad/sec*)	10
ω_{cut3} (*rad/sec*)	20
ω_{cut5} (*rad/sec*)	40
ω_{cut7} (*rad/sec*)	50
k (in (2) and (3))	1.4

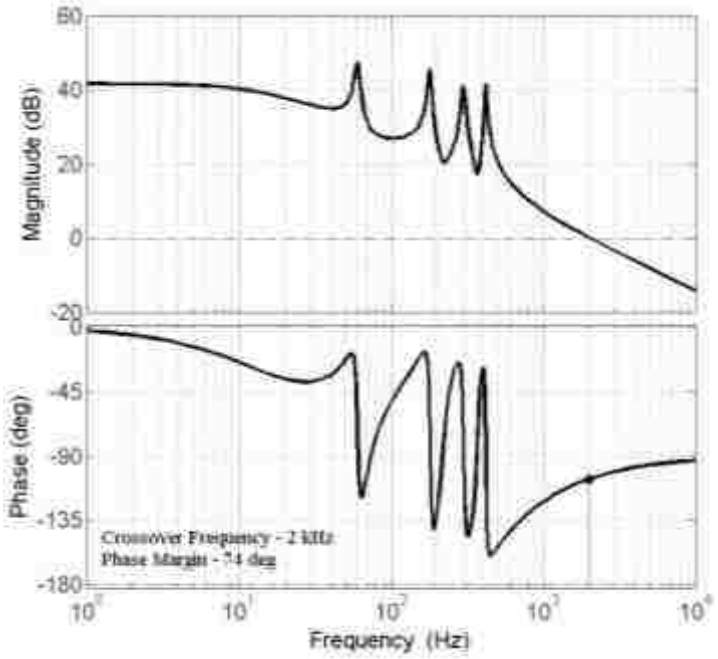


Figure 11. Loop gain plot of the current controller and plant.

2.2 System Modeling and Guidelines for Controller Parameter Selection

This section describes the system modeling for the proposed MRAC structures of Figure 8 and Figure 9. To design of the controller for the proposed MRAC based estimation structure in Figure 8, it is essential to know the corresponding plant model. This is not straightforward by directly looking at Figure 8. However, it should be remembered that the controller shown in the MRAC structure of Figure 8 has the error between P_1 and P_2 as inputs and produces the estimated value of $V_g^1 \sin\delta$ as an output. Thus, a system model relating the error in the active power ($P_1 - P_2$) to the error in the estimation of $V_g^1 \sin\delta$ is needed to design the controller of the MRAC structure as proposed in Figure 8. The model is derived considering that the accurate value of the inductance and resistance is known. The active power P_1 is given as

$$P_1 = \frac{1}{2}\left(v_{i1\alpha}^1 i_{L\alpha}^1 + v_{i1\beta}^1 i_{L\beta}^1\right) \tag{18}$$

or,
$$P_1 = \frac{1}{2}\mathrm{Re}(\vec{v}_{i1}^1 \mathrm{x}\, \vec{i}_L^{1*}) \tag{19}$$

From Figure 3, the fundamental component of current i_L can be represented as

$$\vec{i}_L^1 = \frac{\vec{v}_{i1}^1 - \vec{v}_g^1}{jX} \tag{20}$$

Using representation in phasor form, (20) results

$$\vec{i}_L^1 = \frac{V_{i1}^1 - V_g^1 \angle -\delta}{jX} \tag{21}$$

It should be remembered that in (20) and (21), X is the actual reactance. Using (21) in (19) one gets

$$P_1 = \frac{V_{i1}^1 V_g^1}{2X}\sin\delta \tag{22}$$

Defining P_{err} as $P_1 - P_2$, the input to the MRAC controller for estimating $V_g^1\sin\delta$ is given as

$$P_{err} = \frac{V_{i1}^1}{2X}\left(\left(V_g^1 \sin\delta\right) - \left(V_g^1 \sin\delta\right)_{est}\right) \tag{23}$$

Note that the expression of P_2 is substituted from (7) considering $X_e = X$. The system model relating the change in active power to the error in estimation of $V_g^1\sin\delta$ is given as

$$\frac{P_{err}}{\left(V_g^1 \sin\delta\right)_{err}} = \frac{V_{i1}^1}{2X} \tag{24}$$

where, $(V_g^1\sin\delta)_{err} = V_g^1\sin\delta - (V_g^1\sin\delta)_{est}$.

With the plant model as in (24), the closed loop representation of the MRAC estimator for the estimation of $V_g^1\sin\delta$ is shown in Figure 12.

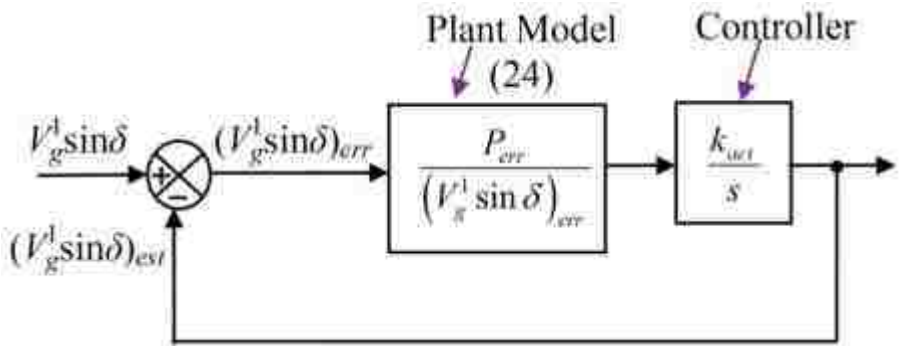


Figure 12. Closed loop representation of the MRAC structure for estimating $V_g^1\sin\delta$.

The system model relating the change in the reactive power ($Q_1 - Q_2$) to the error in the estimation of $V_g^1\cos\delta$ is derived next. This model will help design the controller parameters of the MRAC structure represented in Figure 9. The input to the MRAC controller for estimating $V_g^1\cos\delta$ is given as

$$Q_1 = \frac{1}{2}\left(v_{i1\beta}^1 i_{L\alpha}^1 - v_{i1\alpha}^1 i_{L\beta}^1\right) \tag{25}$$

or,

$$Q_1 = \frac{1}{2}\mathrm{Im}(\vec{v}_{i1}^1 \mathrm{x}\, \vec{i}_L^{1*}) \tag{26}$$

Substituting i_L from (21) in (26) results

$$Q_1 = \frac{V_{i1}^1(V_{i1}^1 - V_g^1\cos\delta)}{2X} \tag{27}$$

Defining Q_{err} as $Q_1 - Q_2$, the input to the MRAC for estimating $V_g^1\cos\delta$ is given as

$$Q_{err} = -\frac{V_{i1}^1}{2X}\left(\left(V_g^1 \cos\delta\right) - \left(V_g^1 \cos\delta\right)_{est}\right) \tag{28}$$

As in the previous case, the expression of Q_2 is substituted from (8) considering $X_e = X$. The system model relating the change in reactive power to the to the error in estimation of $V_g^1\cos\delta$ is given as

$$\frac{Q_{err}}{\left(V_g^1 \cos\delta\right)_{err}} = -\frac{V_{i1}^1}{2X} \tag{29}$$

where, $(V_g^1\cos\delta)_{err} = V_g^1\cos\delta - (V_g^1\cos\delta)_{est}$. The corresponding closed loop representation is shown in Figure 13. The system models given by (24) and (29) are identical in magnitude but opposite in phase. The magnitude is proportional to the peak value of the fundamental component of v_{i1}. It should be noted that the system model presented in (24) and (29) are varying in nature as V_{i1}^1 changes depending to the magnitude and power factor of the current i_L. For design simplification, the voltage drop in the filter inductor is considered to be sufficiently small (see Figure 3), and the magnitude of the fundamental component of v_{i1} can be taken equal to the nominal peak value of the grid voltage in (24) and (29). This converts the varying system models in (24) and (29) to fixed system models. The frequency response of the controller and plant estimating $V_g^1\sin\delta$ is shown in Figure 14. The value of k_{act} is taken as 10 W/V. This keeps the crossover frequency at 70 Hz. The value of k_{react} is taken same as k_{act} but opposite in sign. Alternately, a controller with adaptively changing gain can also be designed. Such varuations would depend on the magnitude of the fundamental component of the controller output V_i^1. However, this would lead to a complex control algorithm involving additional calculations. Hence such a controller design has been avoided in the present scenario.

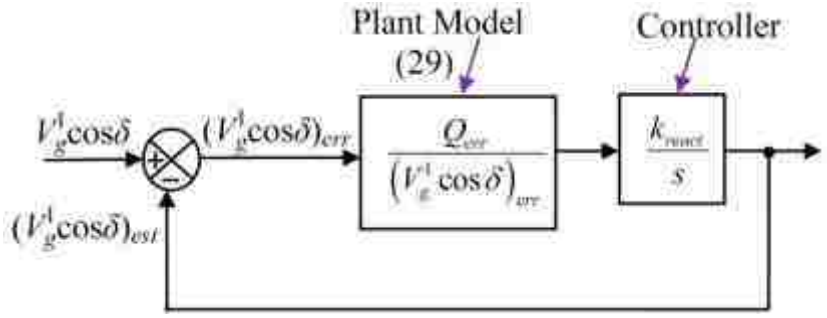


Figure 13. Closed loop representation of the MRAC structure for estimating $V_g^1\cos\delta$.

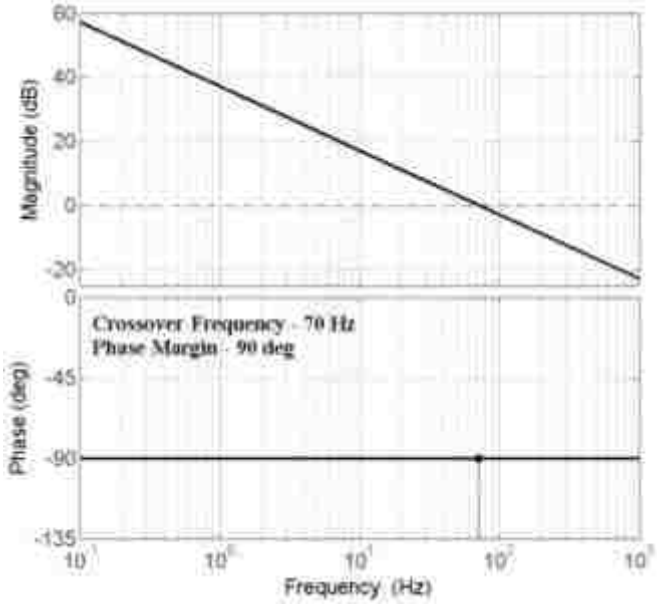


Figure 14. Open loop frequency response of the controller and plant estimating $V_g^1\sin\delta$.

3. EFFECT OF THE DEAD-TIME AND PARAMETER SENSITIVITY ANALYSIS

3.1 Modeling the Dead-Time

A turn on delay (dead time) is used to prevent short circuit between the switches of the same phase leg in a voltage source converter (as in Figure 2). The dead-time adds to a drop (loss) in the output voltage. However, this drop is not linear. Under low

switching frequencies, the effect of this drop can be significant. Hence, it is importane to analyse the effect of the dead-time on the proposed estimation algorithm and suggest suitable compensation techniques. The effect of the dead-time on the proposed estimation method is analyzed here. The dead time, T_{del}, creates a voltage drop given as [41]

$$v_{del1} = \frac{T_{del}}{T_{sw}} V_{dc} \operatorname{sign}(i_L) \tag{30}$$

It should be noted as the voltage drop v_{del1} depends on the direction of the current i_L, the sign function has been used in (30). Similarly, the voltage drop due to the dead-time in the other phase leg is given as

$$v_{del2} = \frac{T_{del}}{T_{sw}} V_{dc} \operatorname{sign}(-i_L) \tag{31}$$

The total voltage drop due to the dead-time can then be calculated as

$$v_{del} = v_{del1} - v_{del2} \tag{32}$$

or,

$$v_{del} = \frac{2T_{del}}{T_{sw}} V_{dc} \operatorname{sign}(i_L) \tag{33}$$

The proposed estimation method is based on the fundamental components of the voltage and currents. So it is important to consider the fundamental component of v_{del}. Considering the inductor current as $i_L = I_{Lpk} \cos(\omega t - \phi)$, the fundamental component of v_{del} is expressed as

$$v_{delfun} = \frac{4}{\pi}\left(\frac{2T_{del}}{T_{sw}} V_{dc} \cos(\omega t - \phi) \right) \tag{34}$$

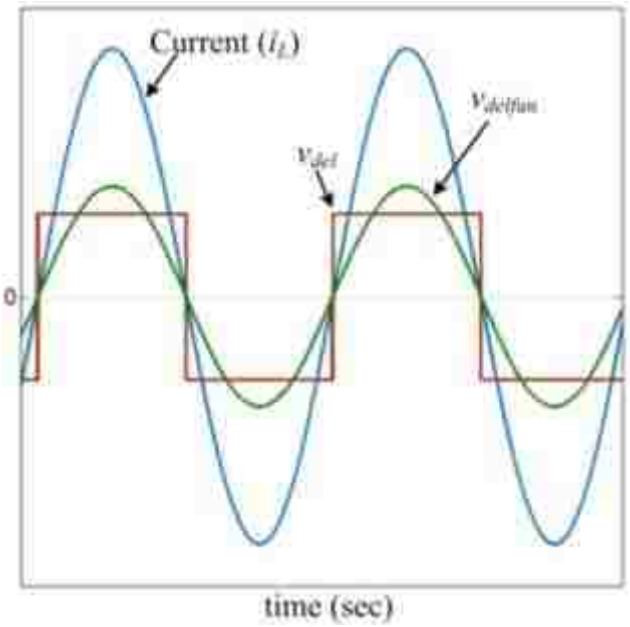


Figure 15. Qualitative representation of the inductor current (i_L), voltage drop due to dead time (v_{del}) and its fundamental component (v_{delfun}).

A typical example of the current waveform (i_L), the voltage drop due to the dead time (v_{del}) and its fundamental component (v_{delfun}) are shown in Figure 15. It can be seen from Figure 15, that v_{delfun} is in phase with i_L. Thus, it can be concluded that the fundamental component of the voltage drop due to the dead time can be modelled as a resistance (r_{del}) given as

$$r_{del} = \frac{v_{delfun}}{i_L} \tag{35}$$

or,

$$r_{del} = \frac{8T_{del}V_{dc}}{\pi T_{sw} I_{Lpk}} \tag{36}$$

In (36), I_{Lpk} is the peak value of inductor current i_L. Considering the inner current loop to be ideal and ensuring perfect tracking with no steady state error

$$I_{Lpk} = I_{refpk} \tag{37}$$

In (37), I_{refpk} is the peak value of inductor current i_L. Using (37) in (36), r_{del} can be expressed as

$$r_{del} = \frac{8T_{del}V_{dc}}{\pi T_{sw} I_{refpk}} \tag{38}$$

The resistance r_{del} will be included as a part of r_e in (1) (also shown in Figure 7).

3.2 Parameter Sensitivity Analysis

It is clearly evident from the discussions in the last section that the proposed estimation of the grid voltage depends on the assumed values of resistance r_e and inductance L_e of the filter inductor. It should be remembered that loss resistance r_e is a combination of the ohmic loss of the switches, the losses in the filter inductor and connecting cable, and the equivalent resistance (r_{del}) representing the voltage drop due to the dead-time effect. Resistance r_{del} can be accurately modeled (as discussed in the previous subsection). However, the winding resistance of the filter inductor, connecting cable and the ohmic losses of the switches change with the circuit operating conditions. Variation in the inductance value is also common. Hence, even an accurate initial estimate of the resistance and inductance will not be able to eliminate deviations in the estimated and actual output voltage. This section presents a sensitivity analysis of the estimated voltage to the changes in the resistance and inductance for a 1 kVA inverter at full load conditions. The detailed derivations are shown in the Appendix. The theoretical plot of the deviations in the magnitude and phase of the estimated grid voltage as obtained from the results in the Appendix for different conditions are shown in Figure 16 to Figure 19. The deviations when delivering rated active power for changes in the

resistance and inductance are shown in Figure 16 and Figure 17. While, the deviations when delivering rated reactive power for changes in the resistance and inductance are shown in Figure 18 and Figure 19. The corresponding results obtained from simulations are also included in each Figure The simulated plots show good concurrence with the theoretical plots.

It can be observed from Figure 16 that there is no deviation in the phase of the estimated voltage with changes in the resistance when supplying active power. Hence, it can be concluded that accurate unit vectors are obtained even with variations in the resistance when the inverter is delivering active power. Observing Figure 19, similar conclusions can be made for changes in the inductance when the converter is supplying reactive power. For the case when the converter is delivering reactive power, variations in the resistance causes errors in the phase of the estimated voltage (see Figure 18). In this case, the error in the magnitude of the estimated voltage is negligible. Similar observations are noted for variations in the inductance when the converter is delivering active power (see Figure 17). However, it should be noted that the deviations in the magnitude of the estimated voltage from the actual value with variations in inductance when supplying reactive power is much more compared to deviations in the magnitude of the estimated voltage with variations in resistance when supplying active power. Similarly, the deviations in the phase of the estimated voltage from the actual value with variations in inductance when supplying active power is much more compared to deviations in the phase of the estimated voltage with variations in resistance when supplying reactive power.

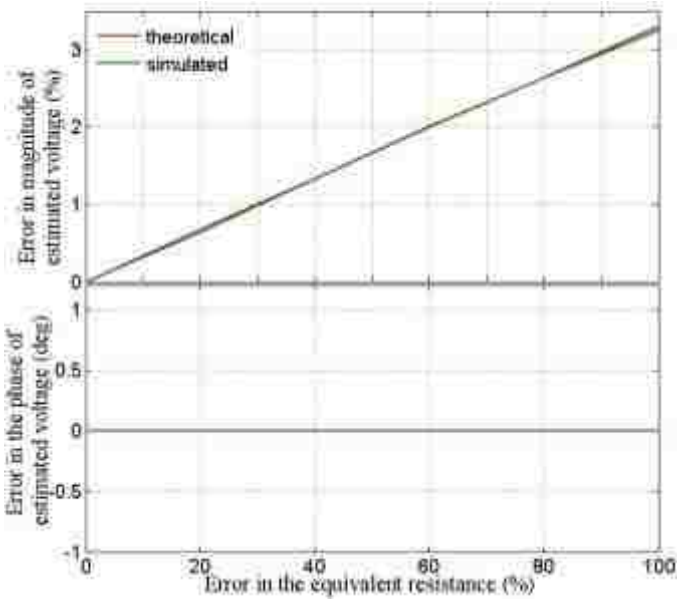


Figure 16. Error in the magnitude and phase of the estimated voltage with variation in the resistance when supplying rated active power.

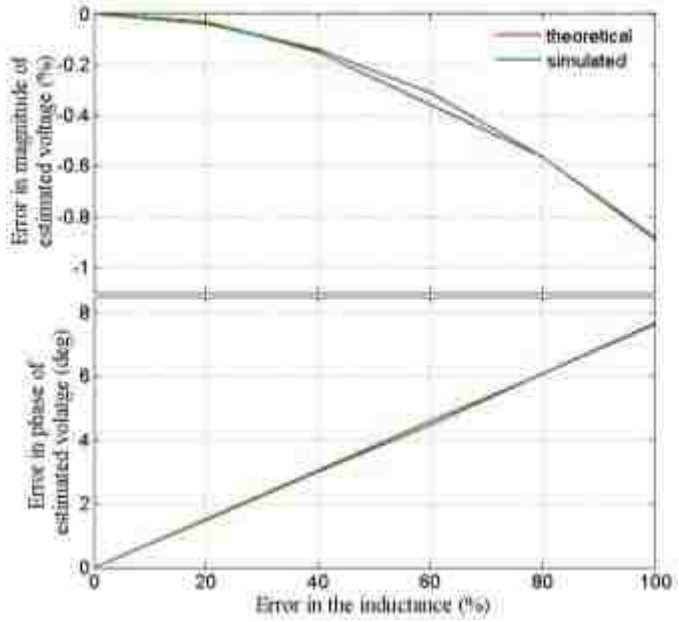


Figure 17. Error in the magnitude and phase of the estimated voltage with variation in the inductance when supplying rated active power.

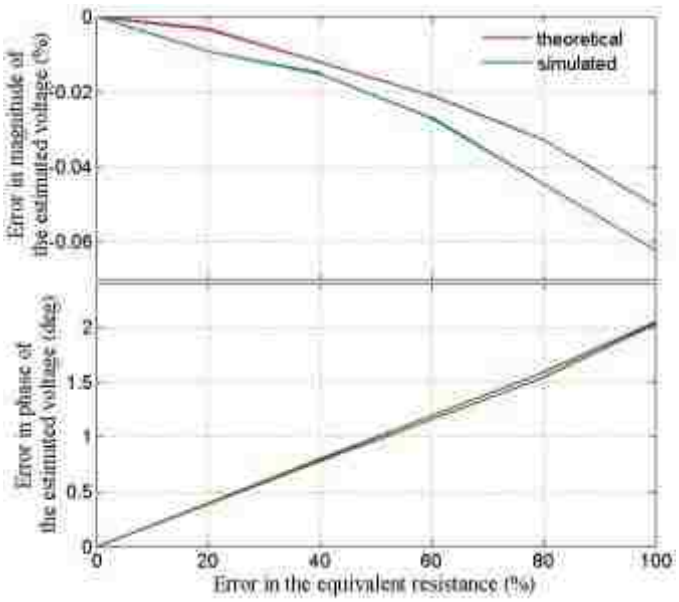


Figure 18. Error in the magnitude and phase of the estimated voltage with variation in the resistance when supplying rated reactive power.

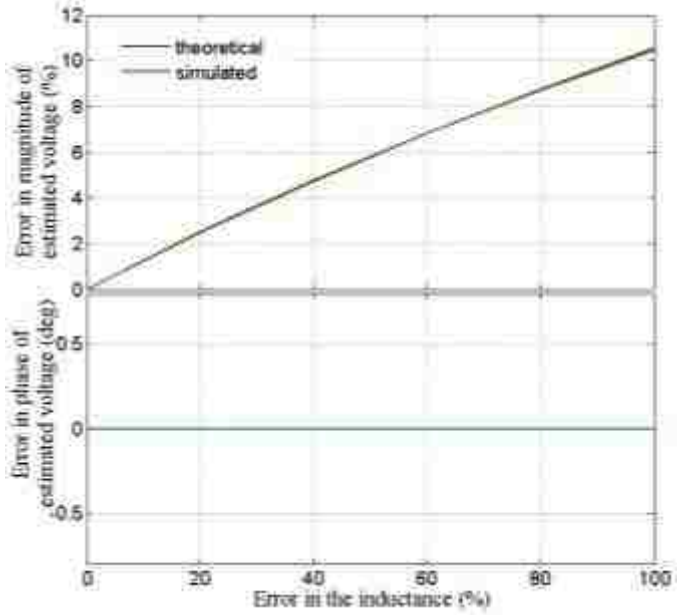


Figure 19. Error in the magnitude and phase of the estimated voltage with variation in the inductance when supplying rated reactive power.

4. RESULTS AND DISCUSSIONS

The proposed algorithm for the estimation of grid voltage without the voltage sensor was experimentally verified on a scaled down 400 VA laboratory prototype. The proposed estimation and control algorithm was implemented in the TMS320F28335 digital signal processor from Texas Instruments. IPP600N25N3 MOSFETs from Infineon were used as switches in the converter bridge. Hall effect current sensor (LA-55P) was used to measure the inductor current. The estimated grid voltage with the proposed estimation method during starting the system is shown in Figure 20. It can be observed that a stable startup is ensured by the proposed algorithm. The estimated voltage and the generated unit vectors for a purely sinusoidal grid voltage with no harmonics are shown in Figure 21. The grid voltage is then mixed with harmonics and the estimation under distorted grid voltage is reported in Figure 22. In this figure, the grid voltage had a THD of 7%. It can be seen the proposed voltage sensorless estimation technique is able to extract the fundamental voltage and generates distortion free unit vectors in both cases. The performance of the proposed method in estimating the grid voltage during changes in the grid is reported next. The estimated waveform during a voltage sag in the magnitude of the grid voltage by 50% is shown in Figure 23, while Figure 24 shows the estimated voltage when the phase of the grid voltage is changed by 45 degrees. The waveforms confirm that the proposed estimation is able to track the grid voltage during sudden changes in the grid.

A comparison of a conventional PLL structure and the proposed sensorless estimation technique is reported in Figure 25. The popularly used single phase SOGI PLL structure [4] was chosen as the conventional PLL structure. It can be seen from

Figure 25, that the proposed sensorless estimation technique reports the same frequency and same unit vectors as the SOGI PLL.

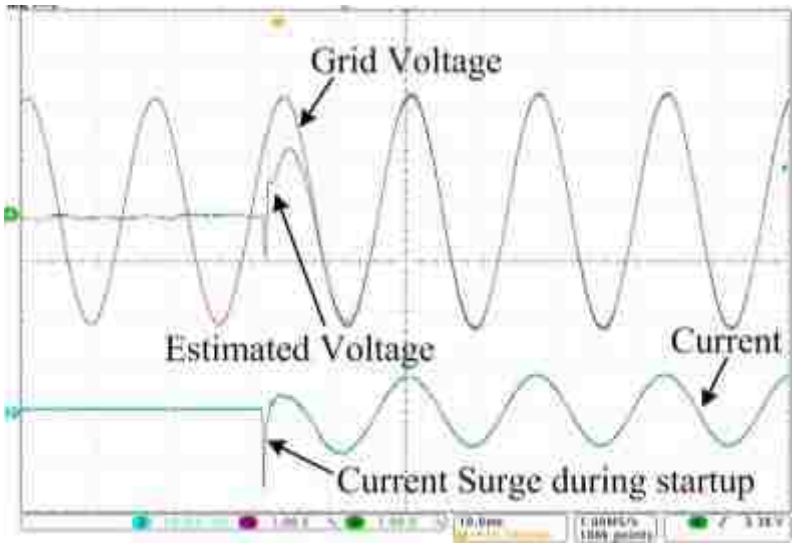


Figure 20. The estimated voltage during startup (Voltage scale:50V/div).

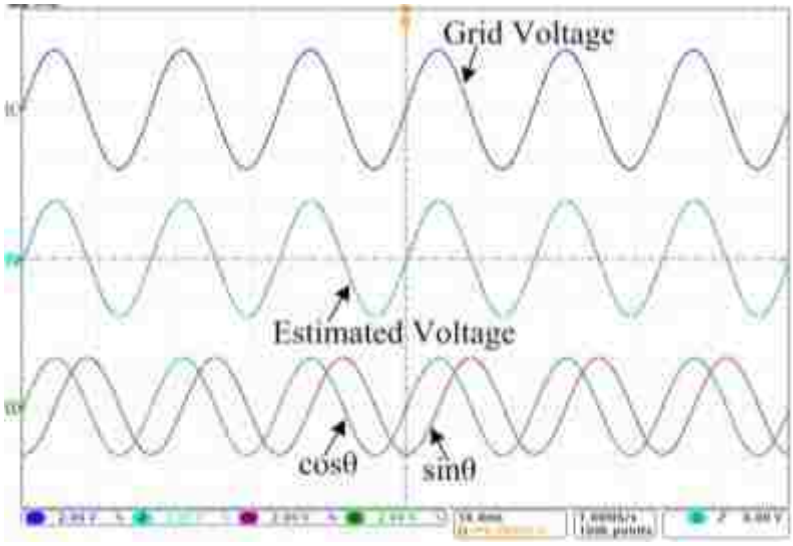


Figure 21. Estimated voltage and unit vectors under pure sinusoidal grid voltage (Voltage scale:100V/div).

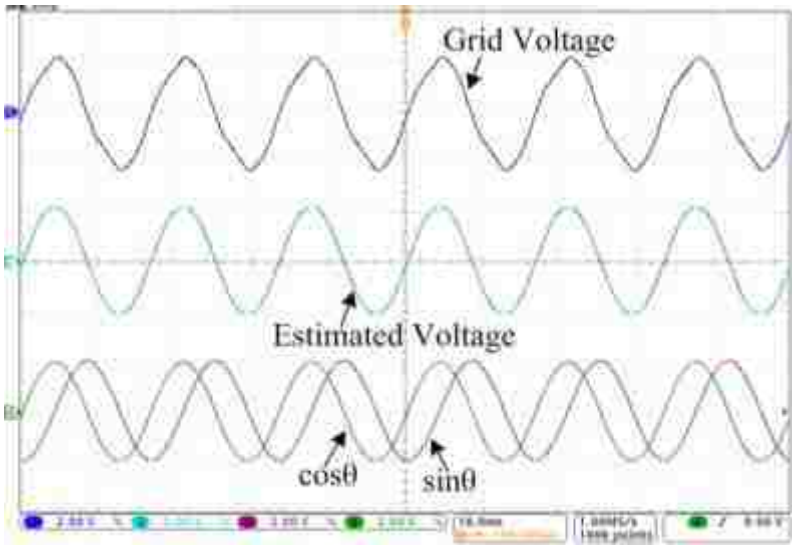


Figure 22. Estimated voltage and unit vectors under highly distorted grid voltage (Voltage scale:100V/div).

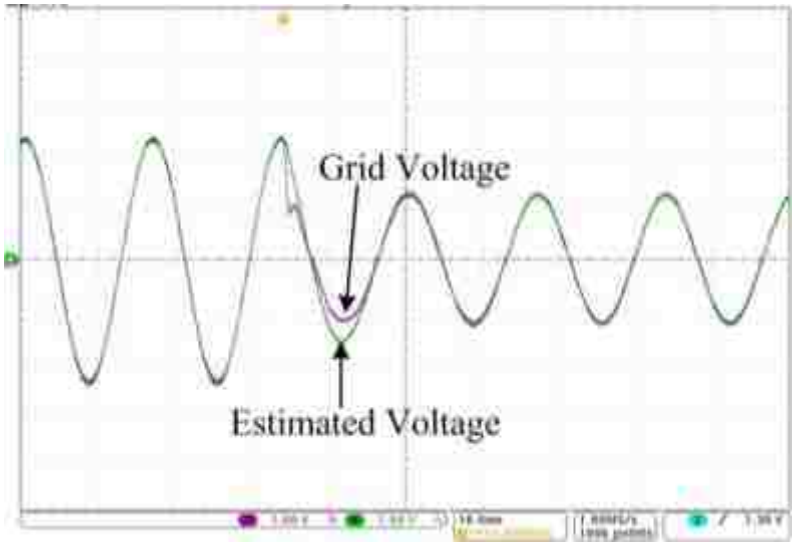


Figure 23. The estimated voltage during a decrease in the grid voltage by 50% (Voltage scale:50V/div).

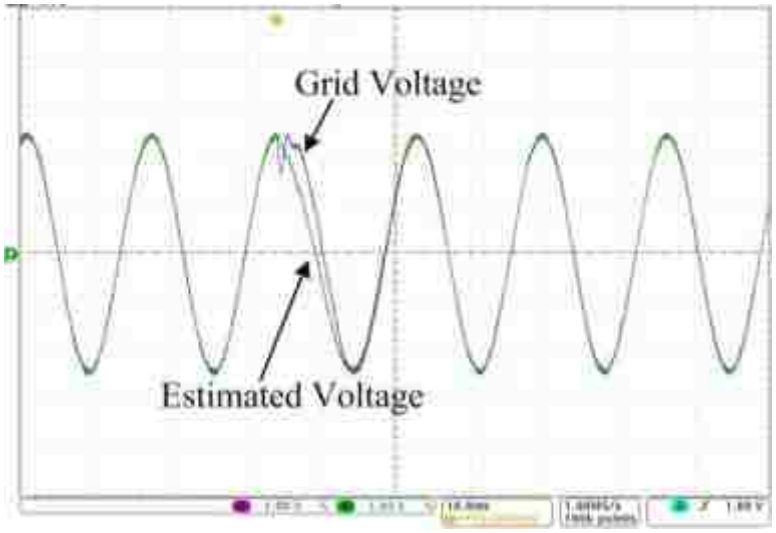


Figure 24. The estimated voltage during a change in the phase of grid voltage by 45 degrees (Voltage scale:50V/div).

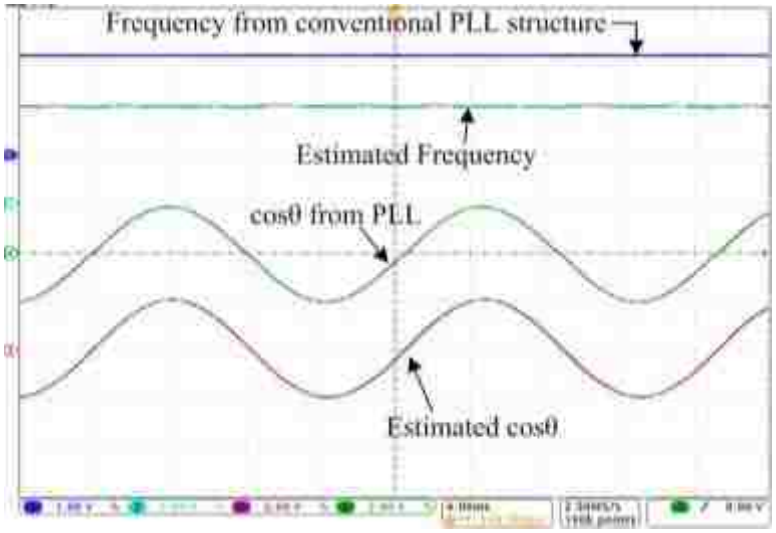


Figure 25. Comparison of the estimated frequency from the proposed scheme with the frequency generated from SOGI PLL structure. (Frequency scale: 30 Hz/div).

The performance of the proposed sensorless estimation scheme for the grid connected converter operating in current controlled mode of operation is reported next. The waveforms of the current, active and reactive power during a transient change in active power from zero to the rated value of 400 W are shown in Figure 26. The

waveforms confirm that the proposed estimation scheme ensures operation at unity power factor. The corresponding waveforms when the converter is delivering rated reactive power of 400 VA to the grid are shown in Figure 27. It can be observed from the figure that the operation is now at zero power factor. The waveforms in the rectifier mode of operation when rated active power is drawn from the grid are reported in Figure 28. The figure shows the grid current is now out of phase to the grid voltage. It should also be observed from Figure 26 − Figure 28, that the current waveforms were distorted for about half of the line cycle. The desired phase tracking was also absent. This is time the proposed algorithm needs for synchronization. In other words, the proposed algorithm is capable of tracking the grid voltage within half line cycle as a regular PLL structure.

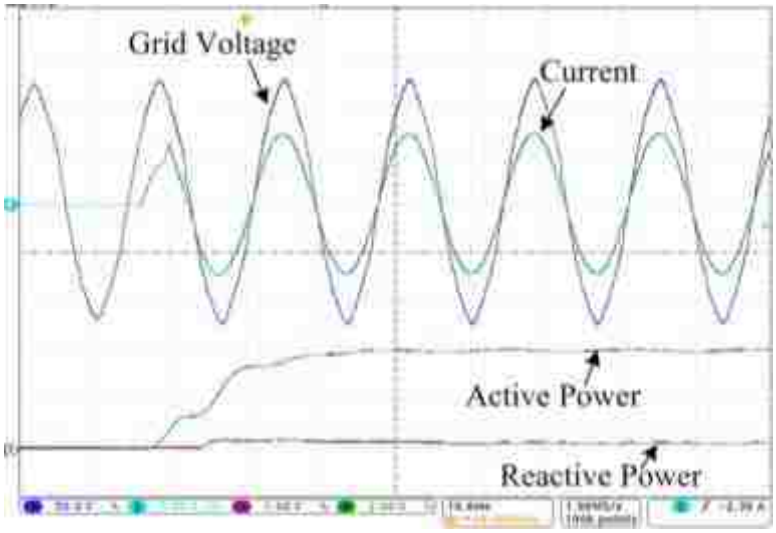


Figure 26. Grid voltage, current, active and reactive power when delivering rated active power (Active Power: 200W/div, Reactive Power: 200VAR/div).

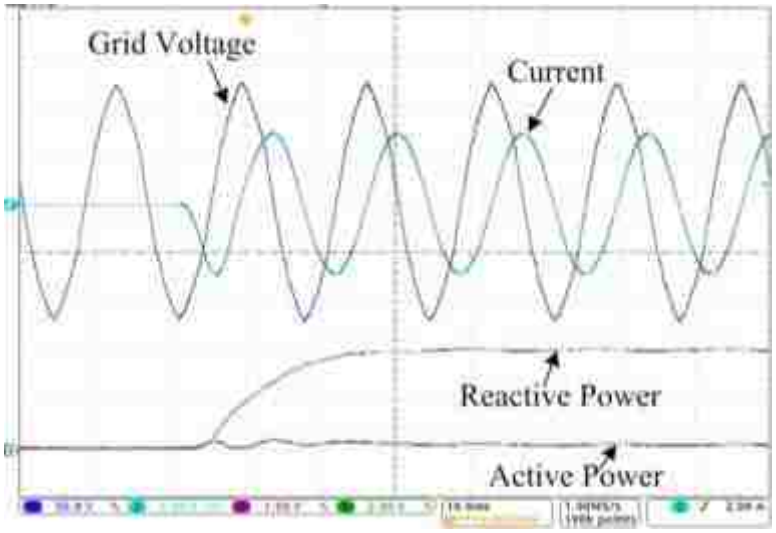


Figure 27. Grid voltage, current, active and reactive power when delivering rated reactive power (Active Power: 200W/div, Reactive Power: 200VAR/div).

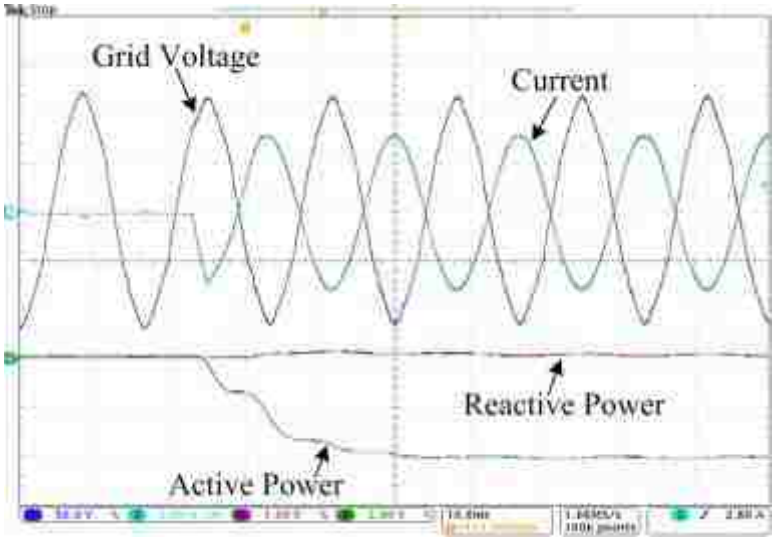


Figure 28. Grid voltage, current, active and reactive power when delivering rated active power in rectifier mode of operation (Active Power: 200W/div, Reactive Power: 200VAR/div).

5. CONCLUSION

This paper presented an estimation method of the grid voltage in single phase grid connected converter system without the need of a grid voltage sensor. The proposed method can be used as an alternative to conventional PLL structures which need a dedicated voltage sensor. The estimation algorithm was able to extract the fundamental component of the grid voltage under distorted grid conditions and generate the unit vectors from it. In addition, it gave an estimation of the grid frequency. The system model required for the controller design was presented. The effect of the dead-time on the proposed estimation method was studied and a model for the voltage drop due to the dead-time was developed. The effects of parameter mismatch, basically the filter inductor inductance and equivalent loss resistance, on the estimated voltage were also analyzed. Rigorous experiments were performed and the results showed that the performance of the proposed sensorless method was very similar to conventional PLL based control architectures. The results supported the validity of the proposed approach.

APPENDIX

The deviation of the estimated voltage from its actual value due to the variations in r and L is presented below. For simplicity the calculations are present in a fictitious synchronous (d-q) frame of reference attached to the estimated voltage considering that the inner current loop ensures perfect reference tracking. The deviations in the steady state voltage under parameter fluctuations being of main interest, all equations reported below are at steady state neglecting any dynamics. Further, as the fundamental

component is of main interest, the equations reported below mainly consider the fundamental components. The subscripts *d* and *q* in the following equations represent the corresponding *d* axis and *q* axis quantities, while superscript 1 refer to fundamental components.

Under steady state conditions, the output voltage V_i^1, the grid voltage, V_g^1 and the inductor current i_L^1 are related as

$$V_{id}^1 = rI_{Ld}^1 - \omega LI_{Lq}^1 + V_{gd}^1 \quad \text{(A1)}$$

$$V_{iq}^1 = rI_{Lq}^1 + \omega LI_{Ld}^1 + V_{gq}^1 \quad \text{(A2)}$$

whereas the output voltage V_i^1, the estimated voltage, V_{gest}^1 and the inductor current i_L^1 are related as

$$V_{id}^1 = r_e I_{Ld}^1 - \omega L_e I_{Lq}^1 + V_{gestd}^1 \quad \text{(A3)}$$

$$V_{iq}^1 = r_e I_{Lq}^1 + \omega L_e I_{Ld}^1 + V_{gestq}^1 \quad \text{(A4)}$$

Using (A1) and (A2) in (A3) and (A4) leads to

$$V_{gd}^1 = V_{gestd}^1 - r_{err} I_{Ld}^1 + \omega L_{err} I_{Lq}^1 \quad \text{(A5)}$$

$$V_{gq}^1 = V_{gestq}^1 - r_{err} I_{Lq}^1 - \omega L_{err} I_{Ld}^1 \quad \text{(A6)}$$

where, $r_{err} = r - r_e$ and $L_{err} = L - L_e$ (A7)

Now, as the fictitious *d-q* frame of reference attached to the estimated voltage

$$V_{gestq}^1 = 0 \quad \text{(A8)}$$

$$I_{dref}^1 = \frac{P_{ref}}{V_{gestd}^1} \text{ and } I_{qref}^1 = \frac{Q_{ref}}{V_{gestd}^1} \quad \text{(A9)}$$

Again as it is assumed that the current loop ensure perfect tracking, under steady state conditions, $I_{Ld}^1 = I_{dref}^1$, $I_{Lq}^1 = I_{qref}^1$.

$$V_{gd}^{1} = V_{gestd}^{1} - r_{err}\frac{P_{ref}}{V_{gestd}^{1}} + \omega L_{err}\frac{Q_{ref}}{V_{gestd}^{1}} \tag{A10}$$

$$V_{gq}^{1} = -r_{err}\frac{Q_{ref}}{V_{gestd}^{1}} - \omega L_{err}\frac{P_{ref}}{V_{gestd}^{1}} \tag{A11}$$

Equations (A10) and (A11) can be combined as

$$\left(V_{gestd}^{1} - r_{err}\frac{P_{ref}}{V_{gestd}^{1}} + \omega L_{err}\frac{Q_{ref}}{V_{gestd}^{1}}\right)^{2} + \left(-r_{err}\frac{Q_{ref}}{V_{gestd}^{1}} - \omega L_{err}\frac{P_{ref}}{V_{gestd}^{1}}\right)^{2} = \left(V_{gd}^{1}\right)^{2} + \left(V_{gq}^{1}\right)^{2} = \left(V_{gpk}^{1}\right)^{2} \tag{A12}$$

Equation (A12) is solved to find V_{gestd}^{1}. As V_{gestq}^{1}=0, so $V_{gest}^{1} = V_{gestd}^{1}$

The error in estimation (expressed as a fraction) is given as

$$V_{esterr} = \frac{V_{gpk}^{1} - V_{gest}^{1}}{V_{gpk}^{1}} \tag{A13}$$

The calculated V_{gestd}^{1} from (A12) is substituted in (A10) and (A11) to find the corresponding V_{gd}^{1} and V_{gq}^{1}. The error in the estimated phase is then calculated as

$$\delta_{err} = \tan^{-1}\left(\frac{V_{gq}^{1}}{V_{gd}^{1}}\right) \tag{A14}$$

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III. INDIRECT GRID CURRENT CONTROL OF AN *LCL* BASED GRID CONNECTED CONVERTER

ABSTRACT

This paper presents a method to indirectly control the grid current of a *LCL* filter based grid connected converter. The proposed method is based on estimating the fundamental and harmonic components of the current drawn by the filter capacitor. The estimated fundamental and harmonic components of the filter capacitor current are then compensated by injecting equal amount of current from the converter side using a well-designed current controller. This indirectly ensures the grid current to be at the desired power factor and immune to any distortions in the grid voltage. The proposed estimation and control scheme is verified by experimental results.

1. INTRODUCTION

Power electronic converters are generally interfaced to the grid using either an *L* filter or an *LCL* filter. Optimally designed *LCL* filters substantially reduce the switching harmonics in the grid side current compared to the *L* filter [2]. However, the control of the converter with an *LCL* filter is more challenging compared to a converter interfaced with only the *L* filter [3]. A single-phase grid connected converter with an *LCL* filter is shown in Figure 1. In the figure, L_i is the converter side filter inductance (with winding resistance r_i), C is the filter capacitance, L_g is the grid side filter inductance (with winding resistance r_g), i_L is the converter current, i_g is the grid current, i_c is the capacitor current,

v_c is the voltage across the filter capacitor, v_g is the grid voltage, and v_i is the output of the bridge. In such a configuration, the transfer function of the converter side current i_L to the output voltage of the bridge v_i, presents an equivalent first order system [3], [4] while the transfer function of the grid current, i_g, to v_i, presents a third order system [3], [4] (see Figure 2). Typical system parameters are given in Table 1.

Direct control of the grid current implies designing a controller for a third order system. This is not straight forward and generally involves multiple control loops [3], [5]−[9] for stability and resonance damping. In general, the grid side current is chosen as the variable for the outer loop while the inner loop variable is chosen as the capacitor current [3], [5], [6] or the converter current [7] or the filter capacitor voltage [8], [9]. Multi loop control structure for *LCL* filter was initially proposed in [3]. Details on the controller design with parameter selection for the two-loop structure in [3] is presented in [5]. However, the design is based on pole placement and pole zero cancellation which is practically difficult to realize. In addition to the problem of resonance oscillations (which is mitigated using active damping [10]−[12]), harmonics and distortions in the grid voltage often affect the quality of the grid current. Addressing this problem, grid voltage or the filter capacitor voltage feedforward is used to minimize the effect of distortions in the grid voltage on the grid current. The use of the capacitor voltage is suggested in [13]. A more detailed feedforward term based on the grid voltage is derived in [14]. However, this feedforward term depends on the system parameters. The variation of the system parameters and their effect on the feedforward term are not considered in [14]. A direct grid current control using resonant controllers to mitigate grid voltage disturbance has

been suggested in [15]. However, the proposed controller needs zero compensation for stability.

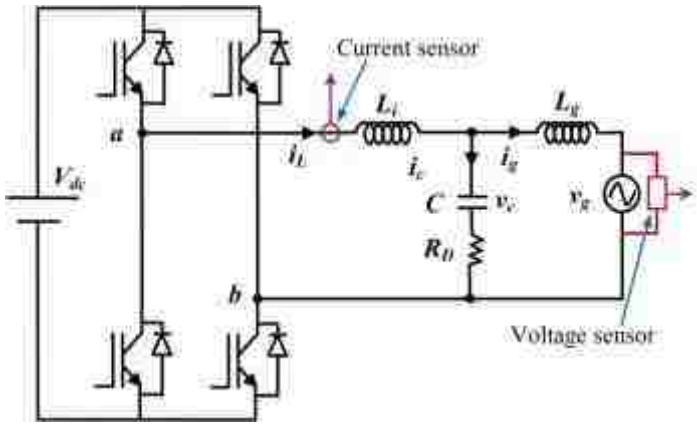

Figure 1. A single-phase grid connected inverter with *LCL* filter.

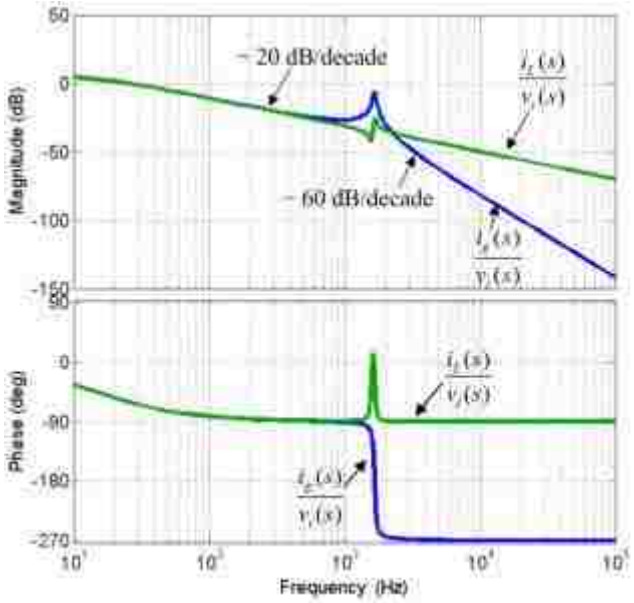

Figure 2. The frequency response of $\frac{i_L(s)}{v_i(s)}$ and $\frac{i_g(s)}{v_i(s)}$.

Table 1. System Parameters.

L_i (mH)	2.5
L_g (mH)	0.5
r_i (Ω)	0.04
r_g (Ω)	0.01
C (μF)	20

Compared to direct control of the grid current, controlling the converter current is simple as it presents an equivalent first order system [3], [4]. However, it is generally not preferred as the filter capacitor draws a reactive current which being unknown cannot be compensated by controlling the converter current [2]. This leads to a deviation in the desired power supplied to the grid, especially at low load conditions. Further, due to the presence of the capacitor branch, the grid current is affected by the harmonics and distortions in the grid voltage. Addressing this problem, this paper proposes to estimate the filter capacitor current and then control the grid side current by controlling the converter side current and supplying the required capacitive reactive power (both fundamental and harmonics) from the converter side. An estimation method based on simple algebraic equations is presented to estimate the filter capacitor current. The proposed scheme uses only one current sensor (to measure i_L) and one voltage sensor to measure the grid voltage, v_g, needed to generate the reference of the grid current.

The rest of the paper is arranged as follows. The estimation of the filter capacitor current and the proposed control structure is presented in Section 2. The detailed stability analysis and controller design guidelines of the proposed estimation is presented in Section 3. The results are discussed in Section 4 and the conclusion presented in Section 5.

2. CONTROL ARCHITECTURE

The overall control block diagram of the proposed control of the *LCL* filter based inverter is shown in Figure 3. The control structure can be categorized as − the estimation of the fundamental and harmonic components of the filter capacitor voltage, the computation of the filter capacitor current and a current controller. It should be noted that only i_L and v_g are measured. The idea is to estimate the filter capacitor current (fundamental and harmonic components) and then add it to the desired grid current reference to generate the converter current reference i_{Lref}. A current controller then ensures that the converter side current i_L tracks i_{Lref}. In Figure 3, v_i is the output of the current controller, P_{ref} and Q_{ref} are the reference values of the active and reactive power, cosθ and sinθ are the unit vectors generated from the phase locked loop (PLL) while ω_g is the grid frequency as obtained from the PLL structure. The estimation of the filter capacitor current is done from the estimated values of the filter capacitor voltage. The estimation of both fundamental and dominant harmonics of the capacitor voltage is done.

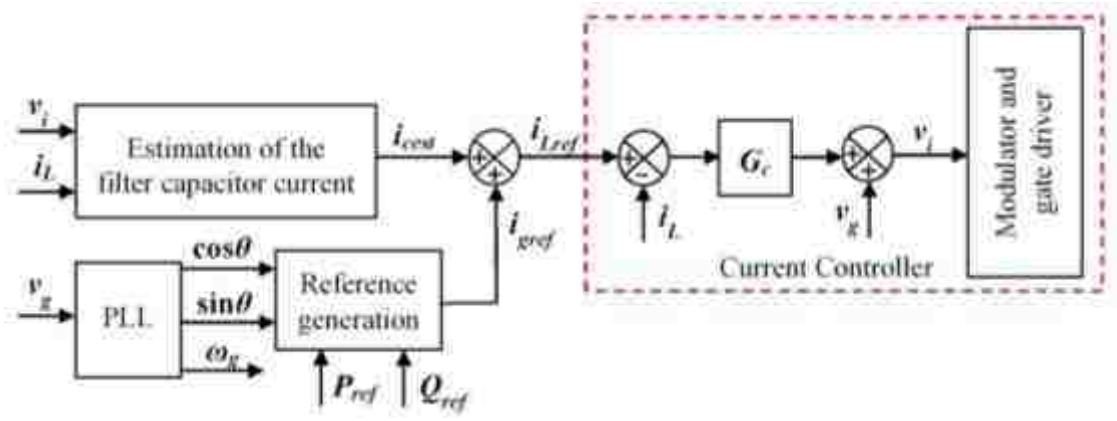

Figure 3. Overall block diagram of the proposed control scheme.

2.1 Estimation of the Filter Capacitor Voltage

The estimation of the filter capacitor current forms an important feature of the proposed control structure. The proposed voltage estimation is based on the active and reactive power transferred from the converter bridge to the filter capacitor. The basics of the estimation method are presented below. The generalized equivalent circuit relating v_i and v_c for the n^{th} harmonic is shown in Figure 4. The voltage drop across the switches, on-state resistance and resistive impedance of the cables being small have been neglected in the equivalent circuit of Figure 4. The superscript n denotes the n^{th} harmonic component in Figure 4.

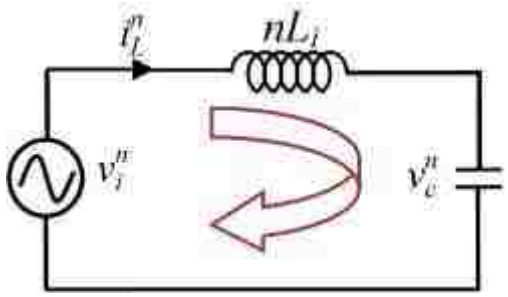

Figure 4. Equivalent circuit representation from the converter bridge to the filter capacitor of the circuit in Figure 1.

For the circuit shown in Figure 4, the power delivered by the source v_i^n to the source v_c^n is given as

$$P_{i1}^n = \frac{1}{2}\left(v_{i\alpha}^n i_{L\alpha}^n + v_{i\beta}^n i_{L\beta}^n\right) \tag{1}$$

and

$$Q_{i1}^n = \frac{1}{2}\left(v_{i\beta}^n i_{L\alpha}^n - v_{i\alpha}^n i_{L\beta}^n\right) \tag{2}$$

At the same time, for two sources (in this case v_i^n to v_c^n) connected through a pure inductance (in this case nL_i), the active and reactive power supplied from the source v_i^n to v_c^n are given as

$$P_{i2}^n = \frac{V_i^n V_c^n \sin\delta_i^n}{2nX_i} \tag{3}$$

$$Q_{i2}^n = \frac{V_i^n}{2nX_i}(V_i^n - V_c^n \cos\delta_i^n) \tag{4}$$

where, $v_i^n = V_i^n \angle \varepsilon_i^n$, $v_c^n = V_c^n \angle \varepsilon_i^n - \delta_i^n$ and $X_i = \omega_g L_i$

In (3) and (4) V_{i1}^n and V_c^n are the peak values of the voltage vectors v_{i1}^n and v_c^n respectively while δ_i^n is the angle v_i^n and v_c^n. It should be noted that the active power given by (1) and (3) should be identical. Observing (1), it can be seen that all the variables on the right side of the equation are known (measured or computed). Similarly, all variables in (3) are also known except the term $V_c^n \sin\delta_i^n$. Based on this knowledge, an estimation of $V_c^n \sin\delta_i^n$ can be proposed as shown in Figure 5. Similarly, the reactive power given by (2) and (4) are identical. Hence (2) and (4) can be used to estimate $V_c^n \cos\delta_i^n$. The estimation of $V_c^n \cos\delta_i^n$ is shown in Figure 6.

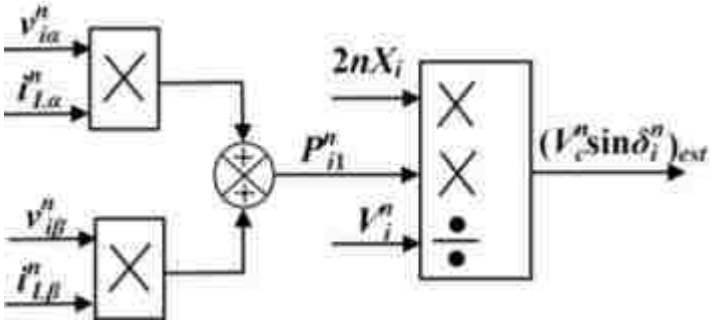

Figure 5. Proposed closed loop estimation structure to estimate $V_c^n \sin\delta_{in}$.

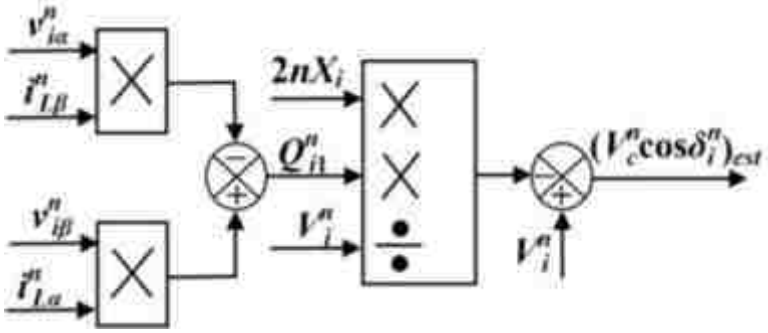

Figure 6. Proposed closed loop estimation structure to estimate $V_c^n\cos\delta_{in}$.

The estimated values $(V_c^n\sin\delta_i^n)_{est}$ and $(V_c^n\cos\delta_i^n)_{est}$ help to give an estimate of the voltage v_c^n as discussed below. A similar method to estimate only the fundamental component of the grid voltage was presented in [16]. It should be noted that the proposed method depends on the loss resistance and the inductance. However, as shown in [16], the dependence is extremely negligible. Hence parameter variations have minimal effect on the proposed estimation. The phasors v_i^n *and* v_c^n are represented in Figure 7. The unit vectors $\cos\varepsilon_i^n$ and $\sin\varepsilon_i^n$ can be found as

$$\cos\varepsilon_i^n = \frac{v_{i1\alpha}^n}{V_{i1}^n} \text{ and } \sin\varepsilon_i^n = \frac{v_{i1\beta}^n}{V_{i1}^n} \tag{5}$$

where
$$V_{i1}^n = \sqrt{\left(v_{i1\alpha}^n\right)^2 + \left(v_{i1\beta}^n\right)^2} \tag{6}$$

Again, unit vectors $\cos\delta_{iest}^n$ and $\sin\delta_{iest}^n$ are found as

$$\cos\delta_{iest}^n = \frac{\left(V_c^n\cos\delta_i^n\right)_{est}}{V_{cest}^n} \text{ and } \sin\delta_{iest}^n = \frac{\left(V_c^n\sin\delta_i^n\right)_{est}}{V_{cest}^n} \tag{7}$$

where
$$V_{cest}^n = \sqrt{\left((V_c^n\cos\delta_i^n)_{est}\right)^2 + \left((V_c^n\sin\delta_i^n)_{est}\right)^2} \tag{8}$$

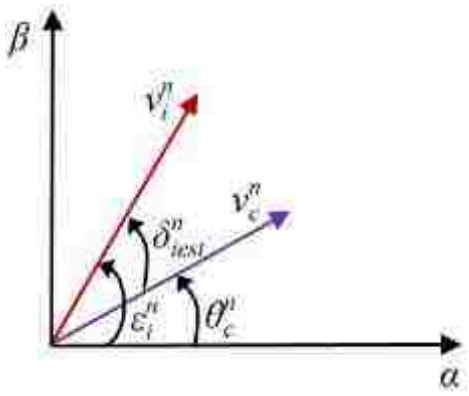

Figure 7. Representation of the different voltage vector in the α-β frame of reference.

Angle θ_c^n can be expressed as $\varepsilon_i^n - \delta_{iest}^n$ (see Figure 7). Unit vectors $\cos\theta_c^n$ and $\sin\theta_c^n$ are then computed as

$$\cos\theta_c^n = \cos\varepsilon_i^n \cos\delta_{iest}^n + \sin\varepsilon_i^n \sin\delta_{iest}^n \tag{9}$$

$$\sin\theta_c^n = \sin\varepsilon_i^n \cos\delta_{iest}^n - \cos\varepsilon_i^n \sin\delta_{iest}^n \tag{10}$$

Unit vectors $\cos\theta_c^n$ and $\sin\theta_c^n$ as in (9) and (10) are used to compute the α-axis and β-axis fundamental component of the filter capacitor voltage as given below

$$v_{cest\alpha}^n = V_{cest}^n \cos\theta_c^n \tag{11}$$

$$v_{cest\beta}^n = V_{cest}^n \sin\theta_c^n \tag{12}$$

It should be noted that all ohmic drops were neglected in the equivalent circuit as in Figure 4. These drops are generally small and create negligible deviations between the actual and estimated values [16]. Further, it can also be argued that the proposed estimation depends on the value of the inductor L_i, which is also subject to variations. However, it should be noted that the inductance L_i is the converter side inductor and is generally accurately known. Deviations in the inductance due to variation of the current i_L is generally negligible.

2.2 Estimation of the Filter Capacitor Current and Proposed Control Structure

Once the β-axis component of the capacitor voltage is estimated, the proposed controller uses the estimated capacitor value to compensate the reactive current drawn by the capacitor (see Figure 3). The fundamental component of the filter capacitor current can be found as

$$i_{cest} = C\frac{dv_{cest}^{1}}{dt} \tag{13}$$

or,
$$i_{cest} = -\omega_g C v_{cest\beta}^{1} \tag{14}$$

Generally metallized polypropylene film capacitors are chosen as the filter capacitor of the *LCL* filter. These capacitors are show negligible deviations in the capacitance value over temperature and time. In addition, these capacitors have negligible equivalent series resistance (ESR). So any resistive drop has been ignored in (13). Compensating the capacitor current as in (14) is sufficient to ensure the desired power factor of the grid current. However, generally the grid voltage is contaminated with harmonics. So to reduce the distortions in the grid current, in addition to the fundamental component of the capacitor current, harmonics of the capacitor current need to be compensated. Including the effect of the harmonics, the capacitor current as in (14) is modified and given as

$$i_{cest} = -\sum_{n=1,3,5,7\ldots}\left(n\omega_g C\right)v_{cest\beta}^{n} \tag{15}$$

The estimation of the filter capacitor current is shown in Figure 8. It should be noted that the fundamental as well as the dominant harmonics are estimated and used to replicate the filter capacitor current.

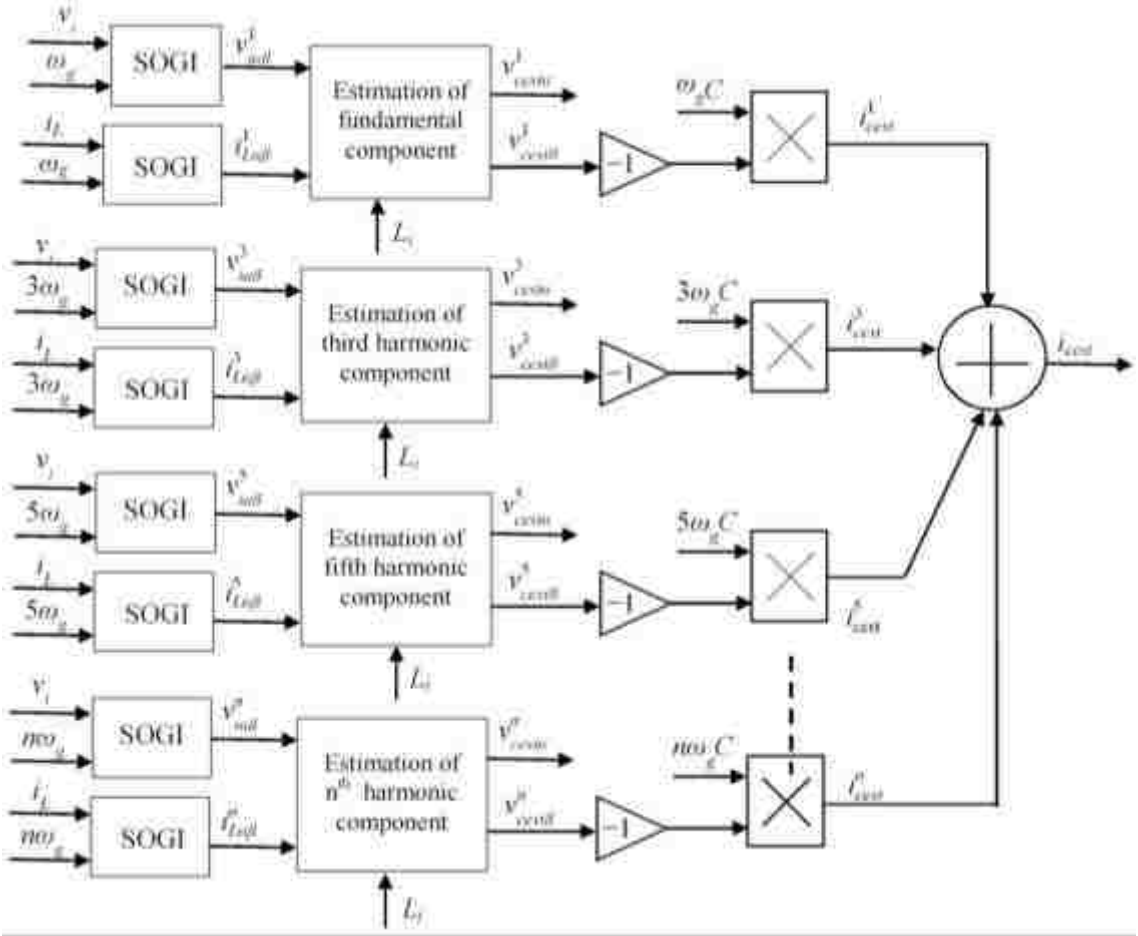

Figure 8. Estimation of the filter capacitor current.

As depicted in Figure 3, i_{cest} as in (15) is added to the grid current reference (i_{gref}) to generate the converter current reference i_{Lref}.

$$i_{Lref} = i_{gref} + i_{cest} \tag{16}$$

A proportional resonant controller, with resonant peaks at the fundamental and dominant harmonic frequencies is then employed to track current reference i_{Lref}. The control law is defined as

$$v_i(s) = \left(i_{Lref}(s) - i_L(s)\right) G_c(s) + v_g(s) \tag{17}$$

where,
$$G_c = k_p + \sum_{n=1,3,5,7\ldots} \frac{k_{rn}\omega_{cutn} s}{s^2 + 2\omega_{cutn} s + (n\omega)^2} \tag{18}$$

The control structure given as in (18) is known as the proportional resonant controller [38]−[39]. With the control law as in (17), response of i_L to i_{Lref} is given as (derivation shown in Appendix)

$$i_L(s) = \frac{(1+H_2H_3)G_c(s)}{((1+H_2H_3)(H_1+G_c(s))+H_2)} i_{Lref}(s) + \frac{H_2H_3}{((1+H_2H_3)(H_1+G_c(s))+H_2)} v_g(s) \tag{19}$$

From (19) the loop gain of the current controller is given as

$$G_{ol}(s) = \frac{(1+H_2H_3)G_c(s)}{H_1+H_2+H_1H_2H_3} \tag{20}$$

The response of the grid current is then given as

$$\begin{aligned} i_g(s) = {} & \frac{(1+H_2H_3)G_c(s)}{D(s)} i_{gref}(s) + \left(\frac{(1+H_2H_3)G_c(s)}{D(s)} - 1 \right) i_{cest}(s) \\ & - i'_{cest}(s) + \frac{H_2H_3}{D(s)} v_g(s) \end{aligned} \tag{21}$$

Equations (19)-(21) are derived in details in the Appendix. The frequency response of the current controller and the plant (the loop gain as in (20)) for the controller parameters as listed in Table 2 are shown in Figure 9. The response of the controller to the estimated components of the capacitor current is shown in Figure 10. It is seen that the gain at the fundamental and compensated harmonic frequencies is very less. The uncompensated capacitor current cannot be attenuated. Its effect is reflected in the grid current. The grid voltage also has an effect on the grid current. The frequency response of the output admittance relating the effect of the grid voltage to the grid current is shown in Figure 11. The admittance is sufficiently attenuated at the harmonic and high frequencies. It should be noted that as with other control structures for *LCL* filter based grid connected

converters, damping of the resonance oscillations in the grid side current is also needed in this case. However, since only the converter side current is measured in this case, active damping cannot be directly implemented. Passive damping technique by connecting a resistor R_D in series with the filter capacitor (see Figure 1) was used to damp out the resonant oscillations. The value of R_D was chosen as 1Ω, which is very negligible compared to the capacitive impedance of the filter capacitor. Hence (13)−(15) are still unchanged. It can also be argued that passive damping increases the losses of the system. However, for a filter capacitor of 20 μF, a damping resistor of 1Ω creates a power loss of less than 1W at utility level grids. Design and choice of an optimal damping resistor is a problem by itself. This paper did not focus on that and hence the chosen damping resistor may not be the optimal one.

Table 2. Controller Parameters.

k_p (V/A)	40
k_{r1} (V/Asec)	1,000
k_{r3} (V/Asec)	1,500
k_{r5} (V/Asec)	2,000
k_{r7} (V/Asec)	3,000
ω_{cut1} (rad/sec)	10
ω_{cut3} (rad/sec)	15
ω_{cut5} (rad/sec)	20
ω_{cut7} (rad/sec)	30
Switching frequency (kHz)	20

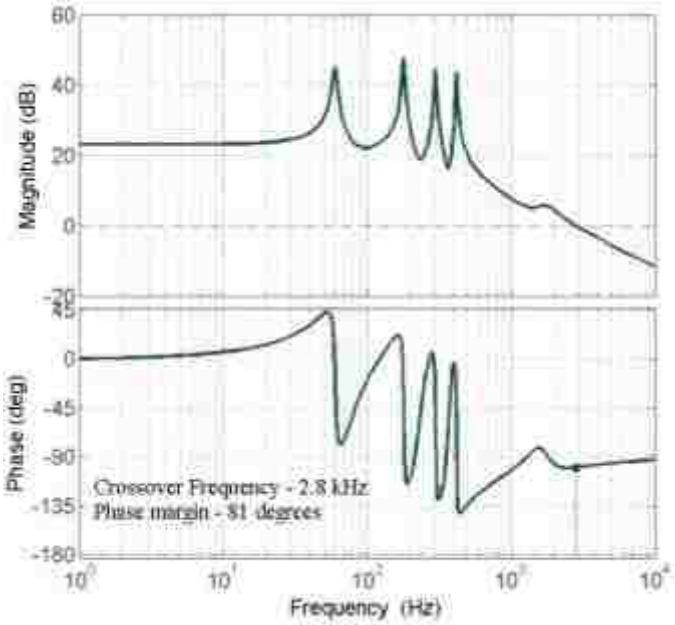

Figure 9. Loop gain plot of the current controller and plant.

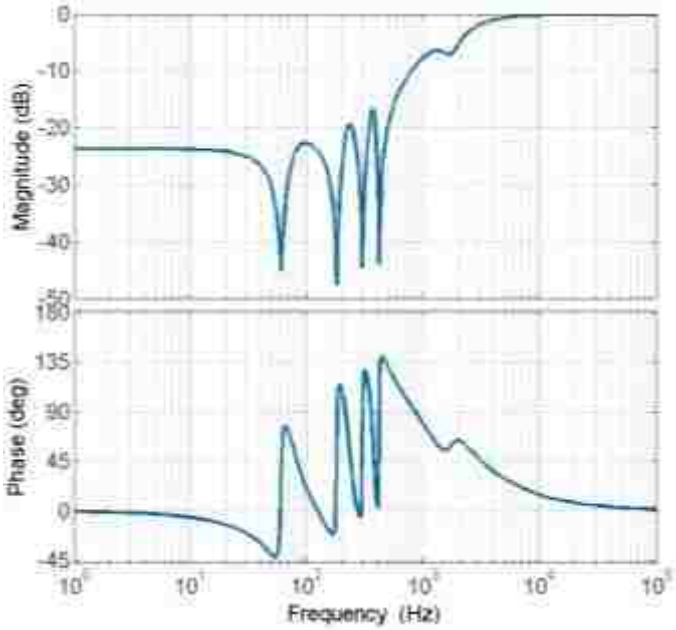

Figure 10. Frequency response showing the effect of the filter capacitor current on the grid current.

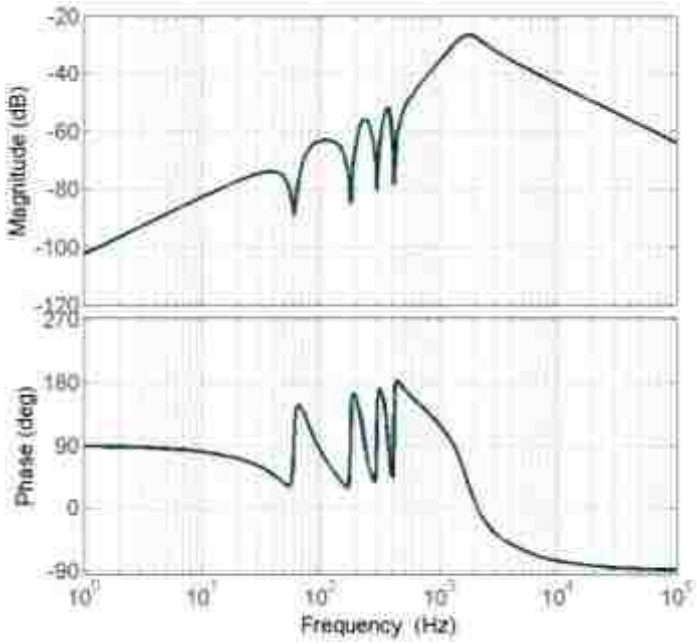

Figure 11. Frequency response of the output admittance.

3. RESULTS

The proposed control scheme was experimentally verified on a scaled down prototype of 400 VA converter. The grid voltage was maintained at 100 V rms. The parameters of the *LCL* filter were as listed in Table. I. IRGP50B60PD1PbF IGBTs from Infineon Technologies were used as the power switches of the converter bridge. The dc bus was supplied from a regulated dc voltage source in the laboratory. The control algorithm was implemented in the TMS320F28335 digital signal processor from Texas Instruments. Hall effect current (LA-55P) and voltage (LV-20P) sensors were used to measure the converter side current and grid voltage. Experimental results are reported for a reference of 0.5 p.u. active power (corresponding to 2 A grid current) and 0 p.u. of reactive power, respectively. The proposed capacitor current compensation was enabled

after a delay. The grid voltage, converter current and grid current waveforms are shown in Figure 12. It can be observed from the figure that while the capacitor current compensation was disabled, unity power factor operation was not ensured. The grid is supplying about 75 VAR of reactive power. However, as soon as the proposed capacitor current compensation is enabled the grid current becomes in phase with the grid voltage ensuring unity power factor operation. No instability with the proposed control is noted during the transition.

The grid voltage is now mixed with 5% of fifth harmonic and 3% seventh harmonic voltage. The waveforms without compensation of the filter capacitor current are shown in Figure 13. It is observed from the figure that the grid current is not in phase with the grid voltage. Additionally, as the harmonic components of the capacitor current are not compensated, the grid current is distorted. The waveforms with the compensation of the fundamental component of the filter capacitor current are shown in Figure 14. It can be seen from the figure that with the compensation of the fundamental capacitor current unity power factor operation is ensured, but the grid current waveform has harmonic components. Measurements reported a THD of 6.8%. The fundamental and harmonic compensation of the capacitor current is implemented next. The corresponding waveforms are shown in Figure 15. It can be seen from Fig. 15 that with the proposed harmonic compensation the grid current has less distortion (THD of 2.3%) compared to the grid current waveform in Figure 14. The actual filter capacitor voltage and the estimated fundamental, fifth and seventh harmonic components are shown in Figure 16.

The waveforms with the proposed control architecture during a transition in active power from 0.25 p.u to 1 p.u are shown in Figure 17. It can be seen from the figure that

the entire system was stable and the proposed controller ensures good tracking of the grid current during the transition. The waveforms during a sag in the grid voltage by 20% are reported in Figure 18. The waveforms show that the proposed control was able to ensure satisfactory performance during sudden change in the grid voltage with negligible distortions in the grid current.

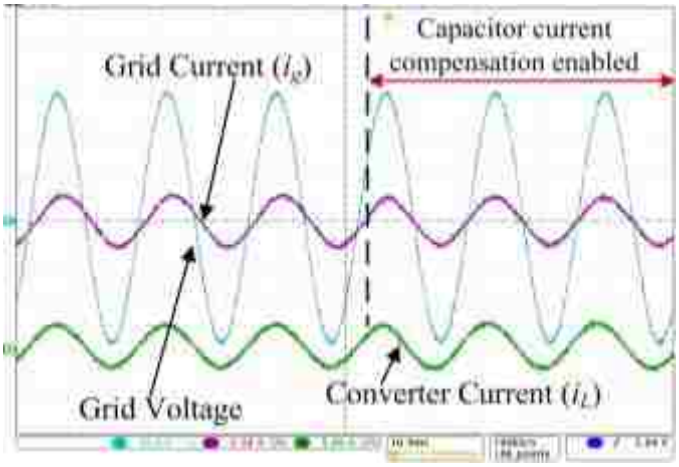

Figure 12. Grid voltage, grid current and converter current with and without the proposed capacitor current compensation under normal grid conditions.

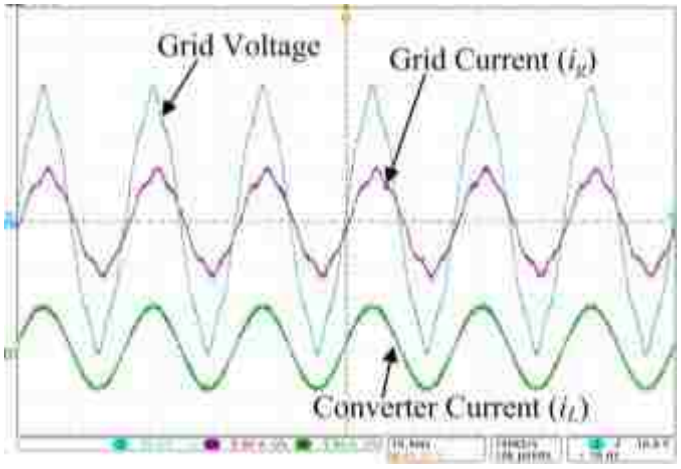

Figure 13. Grid voltage, grid current and converter current without compensation of the capacitor current under distorted grid conditions.

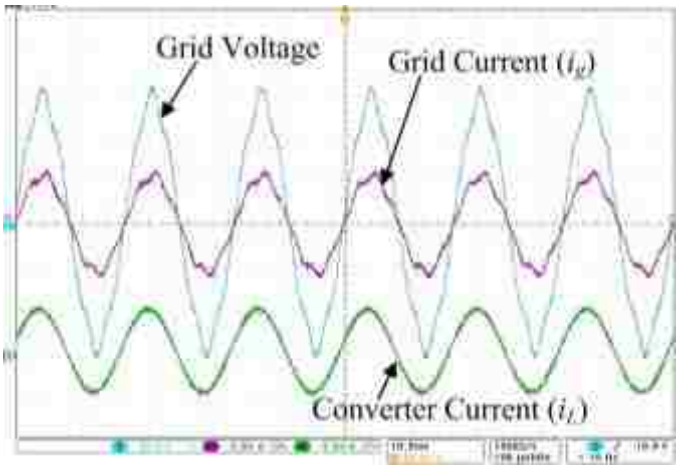

Figure 14. Grid voltage, grid current and converter current with proposed compensation of the capacitor current (only the fundamental) under distorted grid conditions.

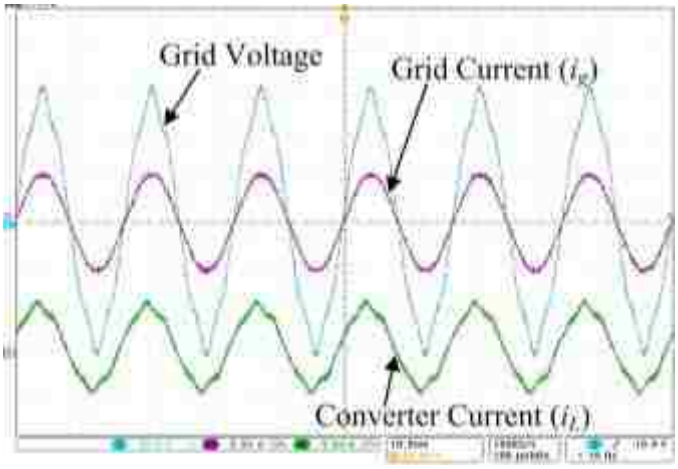

Figure 15. Grid voltage, grid current and converter current with proposed compensation of the fundamental and harmonic capacitor current under distorted grid conditions.

4. CONCLUSION

This paper presented a control architecture to control the grid side current of a grid connected converter with *LCL* filter by estimating the filter capacitor current. The filter capacitor voltage was first estimated using simple algebraic identities. The filter

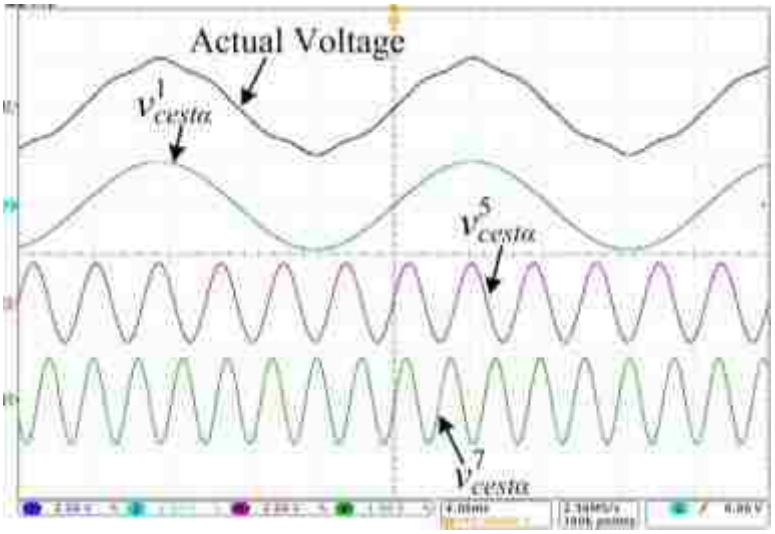

Figure 16. The actual capacitor voltage, estimated fundamental (v^1_{cesta}), fifth harmonic (v^5_{cesta}) and seventh harmonic (v^7_{cesta}) components.

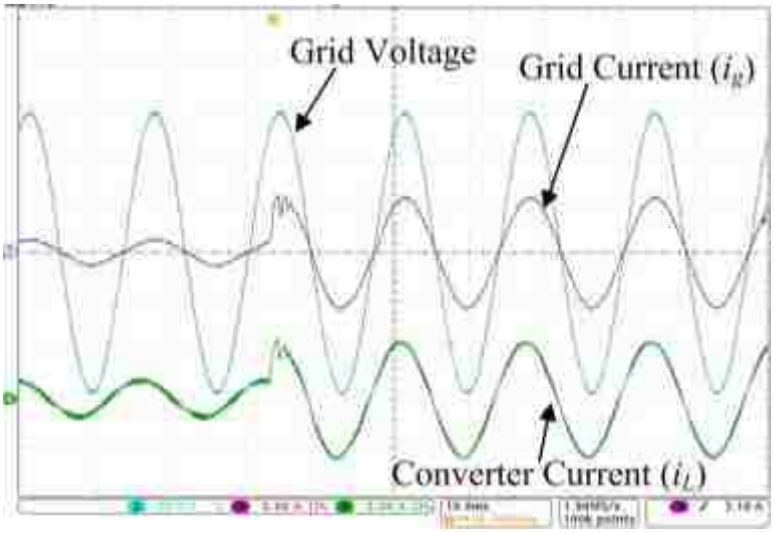

Figure 17. Grid voltage, grid current and converter current during a transition from 0.25 p.u to 1 p.u of active power.

capacitor current was computed from the estimated filter capacitor voltage. The estimated fundamental and harmonic components of the filter capacitor current were then compensated from the converter side, thereby maintaining a sinusoidal grid current at the

desired power factor. Experimental results showed the efficacy of the proposed estimation and control scheme in controlling the current supplied to the grid.

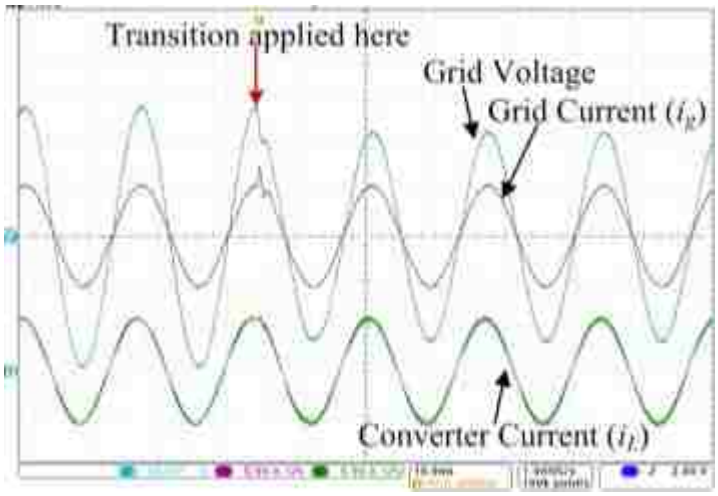

Figure 18. Grid voltage, grid current and converter current during a transition of 20% in the grid voltage.

APPENDIX

The following transfer functions are derived in reference to the circuit in Figure 1 and the control architecture in Figure 3. In the Laplace domain inductor current, capacitor voltage and grid current dynamics are given as

$$\left(sL_i + r_i\right) i_L(s) = v_i(s) - v_c(s) \tag{A1}$$

$$\left(sL_g + r_g\right) i_g(s) = v_c(s) - v_g(s) \tag{A2}$$

$$sCv_c(s) = i_L(s) - i_g(s) \tag{A3}$$

Let $H_1 = (sL_i+r_i)$, $H_2 = (sL_g+r_g)$ and $H_3 = sC/(1+sCR_D)$. Using (A1) in the controller structure as in (17) yields

$$\left(i_{Lref}(s)-i_L(s)\right)G_c(s)+v_g(s)=H_1 i_L(s)+v_c(s) \tag{A4}$$

Using (A3) in (A2) to eliminate i_g one gets

$$v_c(s)=\frac{H_2 i_L(s)+v_g(s)}{1+H_2H_3} \tag{A5}$$

Using (A5) in (A4) yields

$$\left(i_{Lref}(s)-i_L(s)\right)G_c(s)+v_g(s)=H_1 i_L(s)+\frac{H_2 i_L(s)+v_g(s)}{1+H_2H_3} \tag{A6}$$

$$\begin{aligned} i_L(s)=&\frac{\left(1+H_2H_3\right)G_c(s)}{\left(\left(1+H_2H_3\right)(H_1+G_c(s))+H_2\right)}i_{Lref}(s)\\ &+\frac{H_2H_3}{\left(\left(1+H_2H_3\right)(H_1+G_c(s))+H_2\right)}v_g(s)\end{aligned} \tag{A7}$$

From (A7), the closed loop transfer function relating i_L and i_{Lref} is given as

$$G_{cl}(s)=\frac{\left(1+H_2H_3\right)G_c(s)}{\left(\left(1+H_2H_3\right)(H_1+G_c(s))+H_2\right)} \tag{A8}$$

Arranging (A8) in the standard form one gets

$$G_{cl}(s)=\frac{\dfrac{\left(1+H_2H_3\right)G_c(s)}{H_1+H_2+H_1H_2H_3}}{1+\left(\dfrac{\left(1+H_2H_3\right)G_c(s)}{H_1+H_2+H_1H_2H_3}\right)} \tag{A9}$$

From (A9) the open loop transfer function is given as

$$G_{ol}(s)=\frac{\left(1+H_2H_3\right)G_c(s)}{H_1+H_2+H_1H_2H_3} \tag{A10}$$

Observing (A10) the plant transfer function is obtained as

$$G_p(s)=\frac{1+H_2H_3}{H_1+H_2+H_1H_2H_3} \tag{A11}$$

The response of the grid current is found next. i_L and i_{Lref} can be represented as

$$i_L(s) = i_g(s) + i_c(s) \tag{A12}$$

$$i_{Lref}(s) = i_{gref}(s) + i_{cest}(s) \tag{A13}$$

Using (A12) and (A13) in (A7) yields

$$i_g(s) + i_c(s) = \frac{(1 + H_2H_3)G_c(s)}{D(s)}\left(i_{gref}(s) + i_{cest}(s)\right) + \frac{H_2H_3}{D(s)}v_g(s) \tag{A14}$$

where,
$$D(s) = (1 + H_2H_3)(H_1 + G_c(s)) + H_2 \tag{A15}$$

Considering i_c to be combined of n harmonics, out of which k harmonics are compensated by i_{cest}

$$i_c = \sum_{j=1}^{n} i_{cj} \tag{A16}$$

$$i_{cest} = \sum_{j=1}^{k} i_{cj} \tag{A17}$$

Using (A16) and (A17) in (A14) yields

$$\begin{aligned} i_g(s) = \frac{(1 + H_2H_3)G_c(s)}{D(s)} i_{gref}(s) + \left(\frac{(1 + H_2H_3)G_c(s)}{D(s)} - 1\right) i_{cest}(s) \\ -i'_{cest}(s) + \frac{H_2H_3}{D(s)}v_g(s) \end{aligned} \tag{A18}$$

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IV. MODEL REFERENCE ADAPTIVE CONTROL BASED ESTIMATION OF EQUIVALENT RESISTANCE AND REACTANCE IN GRID-CONNECTED INVERTERS

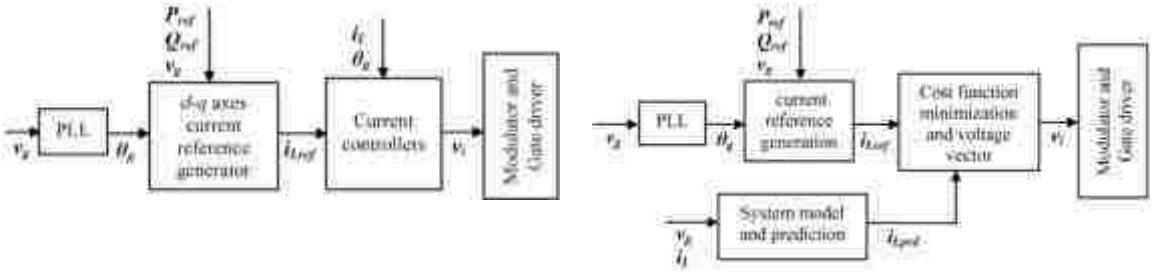
ABSTRACT

The model of a grid connected inverter used for the corresponding controller design depends on the equivalent resistance and inductance between the inverter and the grid. These parameters are not fixed and change with operating conditions, temperature, and age. This paper analyses the effectiveness of the application of the model reference adaptive control (MRAC) approach in obtaining an accurate model of a grid connected inverter system. Active and reactive power based MRAC approaches are used to estimate the equivalent resistance and reactance between the inverter and the grid. Detailed stability analysis of the MRAC approach is presented. The system models for the MRAC controller design are derived and guidelines on the controller parameters selection are proposed. Experimental results validate the feasibility of the proposed scheme.

1. INTRODUCTION

The control of grid-connected inverters has been a very attractive field of research over the past few years. Arguably the current controlled method is the simplest and most popular control scheme for grid-connected inverter control [1]-[3]. The control architecture is shown in Figure 1(a) where the active and reactive powers are controlled by controlling the current supplied to the grid [1]-[3]. However, the design of the current

controllers depends on the plant model which requires the knowledge of the equivalent reactance and resistance between the inverter and the grid [4]-[6]. These parameters are not fixed and change with the circuit operation thereby varying the initially assumed model of the plant. Additionally, the parameters are prone to change by temperature and aging. Therefore, for optimal performance it becomes imperative to estimate the plant parameters and use them to tune the controller parameters. Another popular control approach for grid connected systems is the model predictive control (MPC) scheme [9]-[12]. MPC focuses on selecting the switching state which optimizes a desired cost function (see Figure 1(b)). The cost function is generally dependent on the plant model and similar to the current controlled architecture, the accuracy of the MPC approach relies on the plant parameters.



(a) (b)

Figure 1. Control structure for of a grid-tied inverter using (a) current controlled architecture and (b) MPC.

Addressing the above, authors of [28]-[31] have proposed to estimate the equivalent resistance and reactance between the inverter and the grid. The estimation method presented in [28], [29] uses neural networks to estimate the parameters. However, the proposed algorithm is not verified on a physical hardware system. Furthermore, it can

be understood that estimation and online parameter tuning using neural networks increase the computation burden and complexity of the overall control structure. Authors in [30] and [31] use the concept of model reference adaptive control (MRAC) method for parameter estimation. The MRAC technique is a very simple but powerful control structure which is popularly used for parameter estimations in control systems. In the field of power electronics, MRAC based estimators have been successfully used for estimating the speed in sensorless drive systems. The control structure is well established for cage rotor [20]-[18], doubly fed induction machines [19]-[25] and permanent magnet machines [26], [27]. However, studies on the applications of MRAC approaches in control of grid connected inverters are limited in the literature. Some recent examples are found in [30], [31]. Authors in [30] use the MRAC estimation technique to estimate only the equivalent resistance between the inverter and the grid while in [31] the authors use the technique to estimate both the resistance and inductance. The values are then used to tune the current controller parameters to achieve the desired transient response. The MRAC structures are proposed based on the closed loop current response. However, the MRAC based estimation in [30], [31] is highly iterative. Additionally, the estimations under unbalanced grid conditions are not verified.

In this paper, it is proposed to use active and reactive power based MRAC approaches to estimate the equivalent resistance and reactance between the inverter and the grid. Compared to the estimation methods presented in [28]-[31], the proposed MRAC based estimation is simpler and involves less calculations. Additionally, it gives accurate estimation under both balanced and unbalanced grid conditions. The rest of the paper is arranged as follows. The estimation of the equivalent resistance and reactance

are presented in Section 2. A detailed stability analysis and small signal modeling of the proposed MRAC estimation is presented in Section 3. Experimental results are discussed in Section 4, while the conclusion is presented in Section 5.

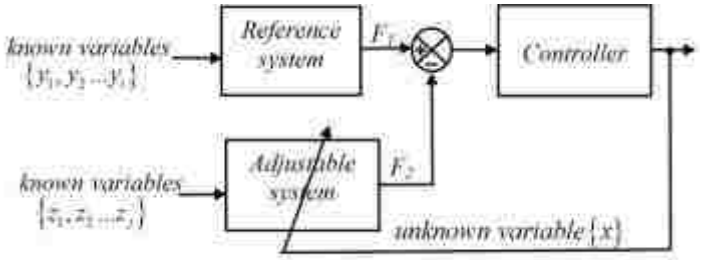


Figure 2. Basic structure of an MRAC system.

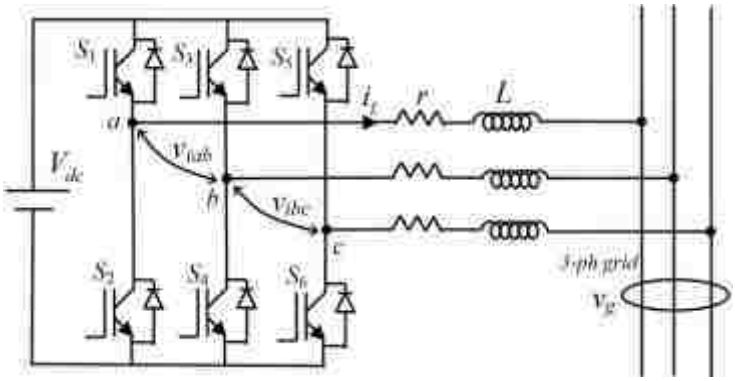


Figure 3. A 3-phase grid connected inverter.

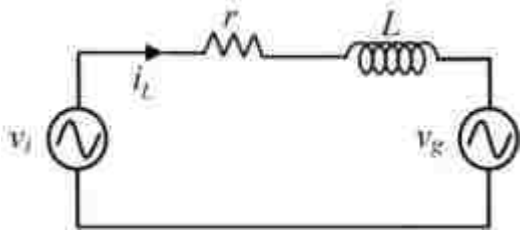


Figure 4. Per-phase equivalent circuit of the grid connected inverter in Figure 3.

2. CONTROL ARCHITECTURE

2.1 Concept of Model Reference Adaptive Control (MRAC)

An MRAC system is shown in Figure 2. The control structure consists of a reference system, an adjustable system, and a compensator (or controller) [26]. The reference system takes *i* known or measurable variables as inputs to generate an output F_1. The adjustable system takes *j* known variable and one unknown variable, which is intended to be estimated, as inputs to generate another output F_2, such that if the unknown parameter is equal to its actual value, then $F_1 = F_2$. However, if the unknown parameter is not the same as its actual value, then $F_1 \neq F_2$. The fundamental concept of the MRAC scheme is to process the error between F_1 and F_2 to generate the unknown parameter, *x*, which is then fed back to the adjustable system. A properly designed controller will eventually converge the error between F_1 and F_2 to zero, thereby matching unknown parameter *x* with its actual value in the system.

2.2 Application of the MRAC Approach for Estimating the Equivalent Resistance and Reactance in a Grid-Connected Inverter

A grid connected inverter is shown in Figure 3. In this figure, *L* is the per phase filter inductance, *r* is the per phase loss resistance, i_L is the filter inductor current, v_g is the per phase voltage of the grid, and v_i is the per phase output voltage of the converter bridge. The per phase equivalent circuit of the grid connected inverter in Figure 3 is shown in Figure 4. It is intended to estimate the equivalent resistance, r_{est}, and reactance, X_{est}, between the inverter bridge and the grid using active and reactive power based MRAC estimators. Further, the estimations should be valid for both balanced and unbalanced grid conditions. From the symmetrical component theory [37], it is known

that an unbalanced system can be decomposed in positive, negative, and zero sequence components. In a three wire system, zero sequence is absent and the positive and negative sequence impedances are identical [37]. Using this advantage, the estimation of the equivalent resistance and reactance is proposed based on positive sequence components. The determination of positive sequence components is discussed next followed by the description of the proposed estimation method.

Using the power invariant transformation any vector in the three-phase (*abc*) stationary coordinates can be transformed to the two phase ($\alpha\beta$) stationary coordinates [15]. The transformation is given as

$$T = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{1}$$

It should be noted that the transformation as in (1) increases the magnitude of each transformed variable by a factor of $\sqrt{3/2}$. In the $\alpha\beta$ frame of reference, the positive sequence components can be determined by using the second order generalized integrator (SOGI) structure as in [34], [35].The SOGI structure consists of two filters given as

$$G_{phase} = \frac{k\omega_{ref} s}{s^2 + k\omega_{ref} s + \omega_{ref}^2} \tag{2}$$

$$G_{quad} = \frac{k\omega_{ref}^2}{s^2 + k\omega_{ref} s + \omega_{ref}^2} \tag{3}$$

The transfer function in (2) creates the in-phase component and (3) creates the quadrature component. The SOGI structure implementing the transfer functions in (2) and (3) is shown in Figure 5 where X_{ph} and X_{quad} are the in-phase and quadrature components of

any arbitrary input X. The positive sequence calculation taking the grid voltage v_g as an example is demonstrated. The 3-phase grid voltage v_{ga}, v_{gb} and v_{gc} are first converted to corresponding 2-phase quantities $v_{g\alpha}$ and $v_{g\beta}$ using the transformation as in (1). Each of the signals $v_{g\alpha}$ and $v_{g\beta}$ is then passed through the SOGI structure (see Figure 5) to generate the corresponding in phase and quadrature components $v_{g\alpha ph}$, $v_{g\alpha quad}$, $v_{g\beta ph}$, and $v_{g\beta quad}$, respectively.

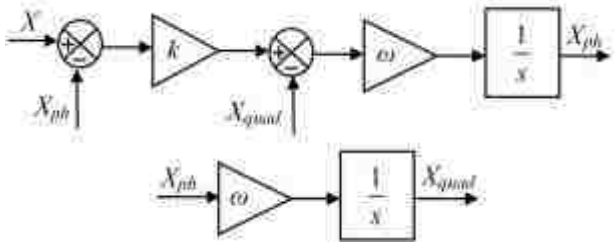


Figure 5. The SOGI structure.

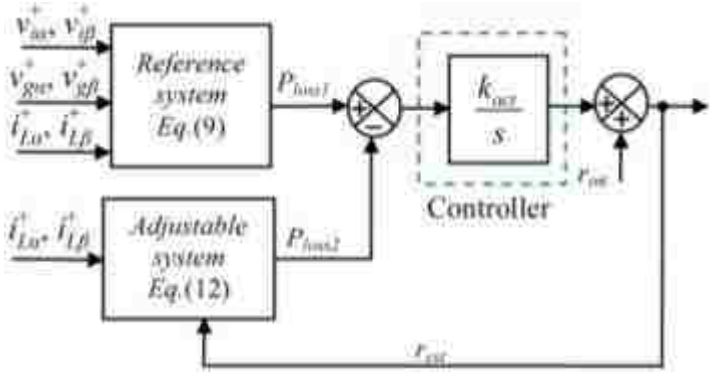


Figure 6. MRAC structure to estimate the equivalent resistance.

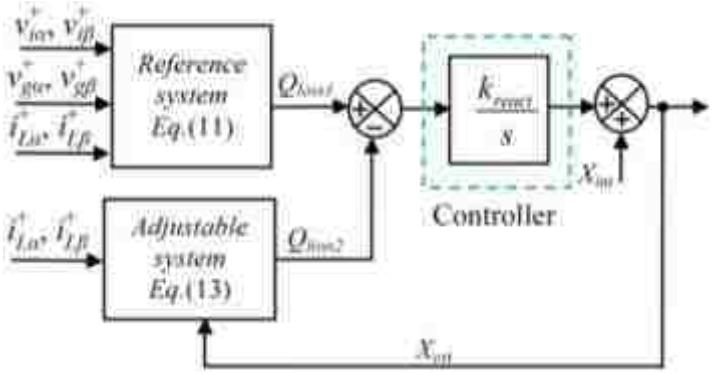


Figure 7. MRAC structure to estimate the equivalent reactance.

Following [36], the positive sequence components are then determined as

$$v_{g\alpha}^{+} = 0.5(v_{g\alpha ph} + v_{g\beta quad}) \tag{4}$$

$$v_{g\beta}^{+} = 0.5(-v_{g\alpha quad} + v_{g\beta ph}) \tag{5}$$

Exactly similar steps are taken to extract the positive sequence components from i_L, and v_i. It should be noted that the filter generating the in-phase component (as in (2)) is band-pass in nature, while the filter generating the quadrature component (as in (3)) is low pass in nature [34], [35]. Both the filters are tuned to the fundamental grid frequency. This eliminates higher order harmonics in the extracted positive sequence components.

The positive sequence components being known, the active and reactive power based MRAC estimation method is presented next. The per phase positive sequence active power P_i^+ and reactive power Q_i^+ generated by the inverter are given as

$$P_i^+ + jQ_i^+ = \frac{1}{3}\left[\left(v_{i\alpha}^+ + jv_{i\beta}^+\right)\times\left(i_{L\alpha}^+ - ji_{L\beta}^+\right)\right] \tag{6}$$

Per phase positive sequence active power P_g^+ and reactive power Q_g^+ delivered to the grid are given as

$$P_g^+ + jQ_g^+ = \frac{1}{3}\left[\left(v_{g\alpha}^+ + jv_{g\beta}^+\right)\times\left(i_{L\alpha}^+ - ji_{L\beta}^+\right)\right] \tag{7}$$

The difference between the two is the active and reactive power loss in the switches, filter inductor, and the connecting cable. The per phase active and reactive power loss, P_{loss1}, and Q_{loss1} are computed as

$$P_{loss1} = P_i^+ - P_g^+ \tag{8}$$

or,
$$P_{loss1} = \frac{1}{3}\left[\left(v_{i\alpha}^+ i_{L\alpha}^+ + v_{i\beta}^+ i_{L\beta}^+\right) - \left(v_{g\alpha}^+ i_{L\alpha}^+ + v_{g\beta}^+ i_{L\beta}^+\right)\right] \tag{9}$$

$$Q_{loss1} = Q_i - Q_g \tag{10}$$

or,
$$Q_{loss1} = \frac{1}{3}\left[\left(v_{i\beta}^+ i_{L\alpha}^+ - v_{i\alpha}^+ i_{L\beta}^+\right) - \left(v_{g\beta}^+ i_{L\alpha}^+ - v_{g\alpha}^+ i_{L\beta}^+\right)\right] \tag{11}$$

It is desired to use the active and reactive power as obtained in (9) and (11) as the reference variables (see Figure 2) of the MRAC systems estimating the equivalent resistance and reactance, respectively. The adjustable systems are proposed next. If r_{est} and X_{est} represent the equivalent resistance and reactance between the inverter bridge and the grid, then the per phase active and reactive power loss, P_{loss2} and Q_{loss2} are given as

$$P_{loss2} = i_{Lrms}^2 \, r_{est} \tag{12}$$

$$Q_{loss2} = i_{Lrms}^2 \, X_{est} \tag{13}$$

where,
$$i_{Lrms}^2 = \frac{1}{3}\left(\left(i_{L\alpha}^+\right)^2 + \left(i_{L\beta}^+\right)^2\right) \tag{14}$$

Resistance r_{est} is the sum total of the resistance of the filter inductor, connecting cable, and the resistance depicting the power loss in the switches. Using the concept of MRAC based estimation, r_{est} can be estimated as shown in Figure 5, where P_{loss1} forms

the reference variable and P_{loss2} the adaptive variable. Correspondingly, the reference model is given by (9), while the adjustable model is given by (12). Exactly a similar structure is used to estimate X_{est}, where Q_{loss1} forms the reference variable and Q_{loss2} the adaptive variable. In this case, (11) forms the reference model and (13) is the adjustable model. The MRAC structure is shown in Figure 7. An integral controller is chosen as the compensator in each case. It should be noted that in both the controller structures depicted in Figure 6 and Figure 7, the system starts with an initial assumed value of resistance r_{int} and reactance X_{int}, respectively. These values can be easily obtained from the datasheet of the inductor.

The proposed MRAC based estimation is not iterative in nature. It is a closed loop controlled estimation method. The convergence of the proposed estimation method thus does not depend on the number of iterations, but on the bandwidth of the control loop. Additionally, it should be noted that an iterative based estimation method generally requires space (memory) to store past values for comparison purposes. However, the MRAC based estimation approach presented in this paper uses integral (see Figure 6 and Figure 7) controllers which need to store a maximum of two past values for its digital implementation.

3. STABILITY ANALYSIS OF THE PROPOSED MRAC METHOD

3.1 Global Stability

The rules for determining the global asymptotic stability of an MRAC estimator are established in the literature [20], [22], [26]. The key is to rearrange the MRAC

structure in a form comprising of a linear time invariant forward path and a nonlinear time varying feedback path. The required conditions are summarized below

a) The forward path time invariant transfer function must be positive real.

b) The nonlinear feedback path with input ε and output w must satisfy the Popov criterion

$$\int_0^{t_1} \varepsilon^T w dt \geq -\gamma^2 \tag{15}$$

with γ^2 being a finite positive constant. The modified representation of the MRAC structure estimating the resistance is shown in Figure 8. It can be observed that the forward path gain is unity. Again, from Figure 7

$$\varepsilon_1 = -w_1 \tag{16}$$

Using (16) it is obvious that

$$\int_0^{t_1} \varepsilon_1^T w_1 dt = -\int_0^{t_1} w_1^2 dt \tag{17}$$

For any real w_1, w_1^2 is always positive. Hence

$$\int_0^{t_1} w_1^2 dt \geq 0 \tag{18}$$

or,
$$\int_0^{t_1} \varepsilon_1^T w_1 dt \geq -\gamma^2 \tag{19}$$

This satisfies the Popov criterion. Hence the MRAC estimator is globally asymptotically stable. Exactly similar derivations for the MRAC estimating the reactance show that the corresponding MRAC as in Figure 7 (which is modified as in Figure 9) is globally asymptotically stable.

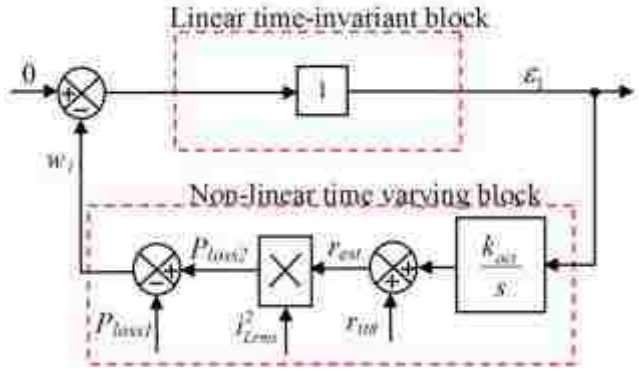


Figure 8. Equivalent structure of the MRAS in Figure 6.

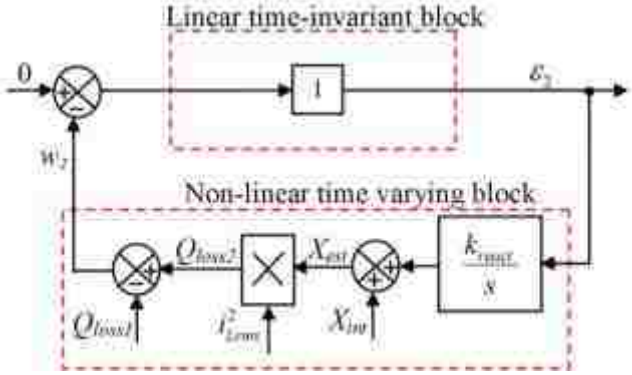


Figure 9. Equivalent structure of the MRAS in Figure 7.

3.2 System Modeling and Controller Parameter Selection

The global stability analysis ensures the stability of the overall system with a generalized controller (shown as an integrator in Figure 5, 6, 7 and 8) structure. However, to ensure proper transient and steady-state response, the controller needs to be designed based on the plant model. The active power based MRAC structure of Figure 5 estimates the equivalent loss resistance. Thus, a system model relating the error in the active power ($P_{loss1} - P_{loss2}$) to the error in the estimation of the equivalent resistance is needed to

design the controller of the MRAC structure as proposed in Figure 5. The model is presented in the $\alpha\beta$ frame of reference. In this frame of reference, the dynamics of the filter inductor current are given as

$$L\frac{di_{L\alpha}^{+}}{dt}+ri_{L\alpha}^{+}+v_{g\alpha}^{+}=v_{i\alpha}^{+} \tag{20}$$

$$L\frac{di_{L\beta}^{+}}{dt}+ri_{L\beta}^{+}+v_{g\beta}^{+}=v_{i\beta}^{+} \tag{21}$$

In the $\alpha\beta$ frame of reference $i_{L\alpha}^{+}$ and $i_{L\beta}^{+}$ are in quadrature to each other. So,

$$\frac{di_{L\alpha}^{+}}{dt}=-\omega i_{L\beta}^{+} \tag{22}$$

$$\frac{di_{L\beta}^{+}}{dt}=\omega i_{L\alpha}^{+} \tag{23}$$

The mathematical proof of (22) and (23) is presented in the Appendix. Using (22) and (23) in (20) and (21) results

$$v_{i\alpha}^{+}=ri_{L\alpha}^{+}-Xi_{L\beta}^{+}+v_{g\alpha}^{+} \tag{24}$$

$$v_{i\beta}^{+}=ri_{L\beta}^{+}+Xi_{L\alpha}^{+}+v_{g\beta}^{+} \tag{25}$$

In (24) and (25), X is the actual reactance. The input to the MRAC controller for estimating the resistance is given as

$$P_{err}=\frac{1}{3}\left[\left(v_{i\alpha}^{+}i_{L\alpha}^{+}+v_{i\beta}^{+}i_{L\beta}^{+}\right)-\left(v_{g\alpha}^{+}i_{L\alpha}^{+}+v_{g\beta}^{+}i_{L\beta}^{+}\right)\right]-i_{L\,rms}^{2}r_{est} \tag{26}$$

Substituting $v_{i\alpha}^{+}$ and $v_{i\beta}^{+}$ from (24) and (25) in (26) one gets

$$P_{err}=r\left(\frac{i_{L\alpha}^{+2}+i_{L\beta}^{+2}}{3}\right)-i_{L\,rms}^{2}r_{est} \tag{27}$$

Using (14) in (27) leads to

$$P_{err} = \frac{i_{Lpk}^{+2}}{3} r_{err} \tag{28}$$

where, $i_{Lpk}^{+2} = i_{L\alpha}^{+2} + i_{L\beta}^{+2}$, and $r_{err} = r - r_{est}$.

The system model relating the change in active power loss to the change in resistance is given as

$$\frac{P_{err}}{r_{err}} = \frac{i_{Lpk}^{+2}}{3} \tag{29}$$

With the plant model as in (29), the closed loop representation of the MRAC estimator for the estimation of the equivalent resistance is shown in Figure 10.

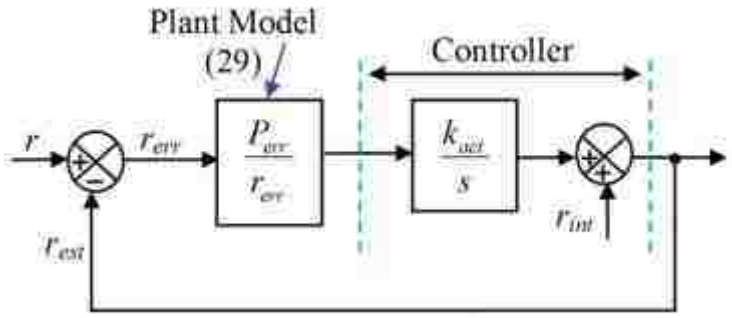


Figure 10. Closed loop representation of the MRAS for estimating the resistance.

The system model relating the change in the reactive power ($Q_{loss1} - Q_{loss2}$) to the estimated reactance is derived next. This model will help design the controller parameters of the MRAC structure represented in Figure 6. The input to the MRAC controller for estimating the reactance is given as

$$Q_{err} = \frac{1}{3}\left[\left(v_{i\beta}^{+} i_{L\alpha}^{+} - v_{i\alpha}^{+} i_{L\beta}^{+}\right) - \left(v_{g\beta}^{+} i_{L\alpha}^{+} - v_{g\alpha}^{+} i_{L\beta}^{+}\right)\right] - i_{L\,rms}^{2} X_{est} \tag{30}$$

Substituting $v_{i\alpha}^{+}$ and $v_{i\beta}^{+}$ from (24), (25) in (30)

$$Q_{err} = X\left(\frac{i_{L\alpha}^{+2} + i_{L\beta}^{+2}}{3}\right) - i_{L\,rms}^{2} X_{est} \tag{31}$$

Using (14) in (31),

$$Q_{err} = \frac{i_{Lpk}^{+2}}{3} X_{err} \tag{32}$$

where, $X_{err} = X - X_{est}$.

The system model relating the change in reactive power loss to the change in reactance is given as

$$\frac{Q_{err}}{X_{err}} = \frac{i_{Lpk}^{+2}}{3} \tag{33}$$

The corresponding closed loop representation is shown Figure 11. It should be noted that both the transfer functions given by (29) and (33) are identical.

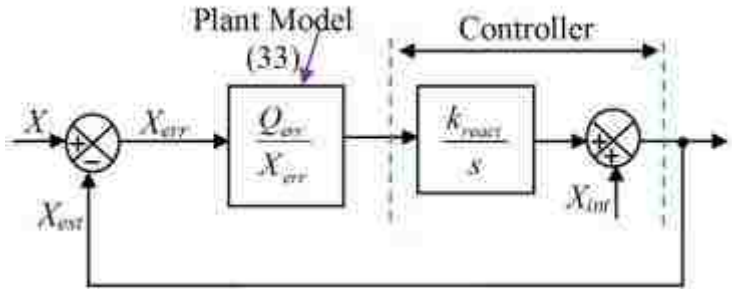


Figure 11. Closed loop representation of the MRAS for estimating the inductive impedance.

The transfer functions are dependent on the peak value of the current delivered to the grid. In fact the dc gain is proportional to the square of the peak current. The controller is designed at the rated power output corresponding to the rated current ($I_{ratedpk}$). To keep the bandwidth of the control loop unchanged, the controller gain is changed proportionally to the square of the peak of the delivered current to the grid. The frequency response of the controller and plant estimating the equivalent resistance at rated load condition is shown in Figure 12. The controller gain at this operating condition is designated as k_{act0}. With the knowledge of the peak value of the reference current (I_{refpk}), the controller gain is modified as

$$k_{act} = k_{act0} \frac{I_{ratedpk}^2}{I_{refpk}^2} \tag{34}$$

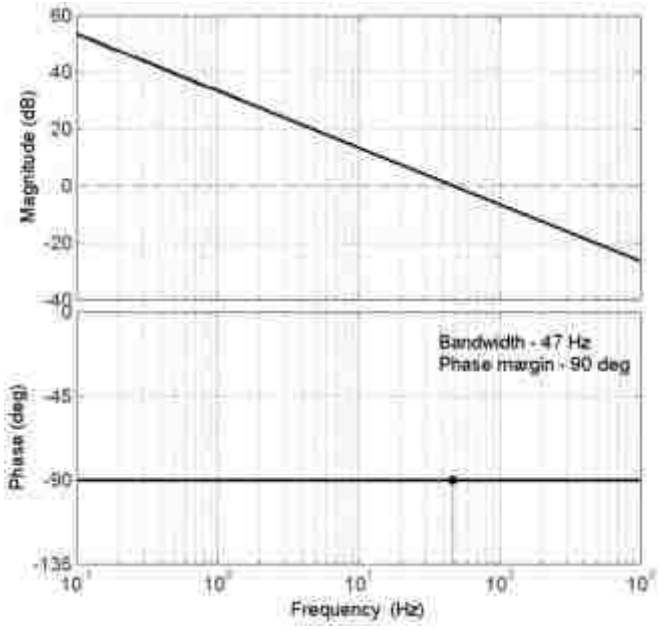


Figure 12. Frequency response of the controller and plant estimating the resistance.

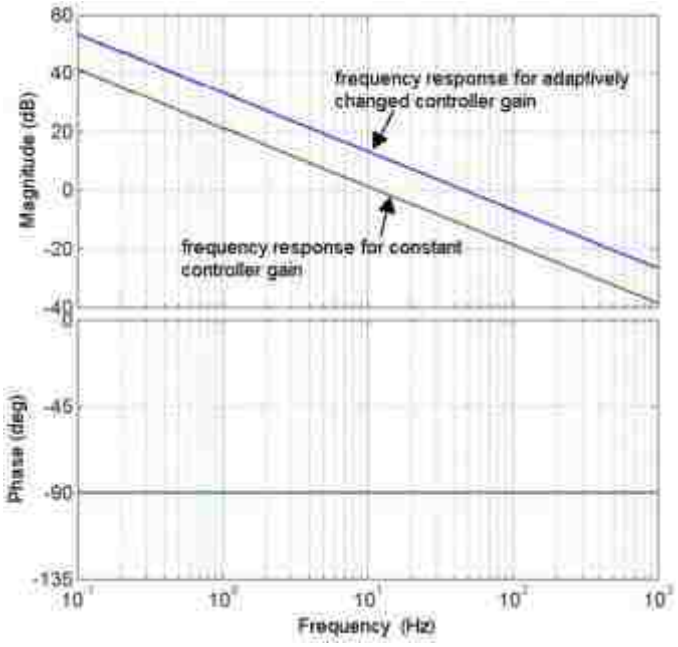


Figure 13. Frequency response of the controller and plant estimating the resistance delivering half the rated power with and without the adaptive change in controller gain as in (34).

Similarly, the controller gain for the equivalent reactance is modified as

$$k_{react} = k_{react0} \frac{I_{ratedpk}^2}{I_{refpk}^2} \tag{35}$$

where, k_{react0} is the controller gain at rated load conditions. It should be noted that $k_{act0} = k_{react0}$. A comparison of the frequency responses of the controller and plant estimating the equivalent resistance at half the rated load condition with constant controller gain as k_{act0}, and the gain varied as in (34) are shown in Figure 13. The system and controller parameters are shown in Table 1, while the adaptive variation in the controller gain is shown in Figure 14.

Table 1. System and Controller Parameters.

L	5.5 mH
r	0.4 Ω
k_{act0}	9 Ω/W
k_{react0}	9 Ω/VAR
f_s	20 kHz

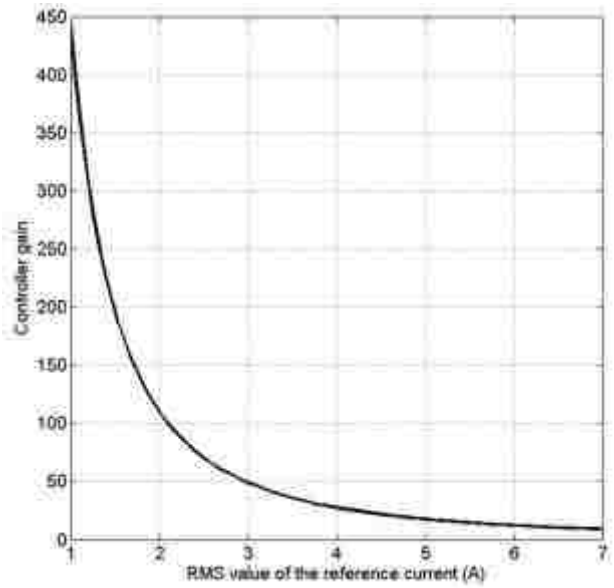


Figure 14. Variation in the controller gain with change in the reference current.

4. RESULTS AND DISCUSSIONS

The proposed MRAC estimator was experimentally verified on a scaled down 750 VA laboratory prototype. The grid voltage was maintained at 65V. The control algorithm was implemented in the TMS320F28335 digital signal processor from Texas Instruments. IRGP50B60PD1PbF IGBTs [32] from International Rectifiers were used as switches in the converter bridge. Hall effect current (LA-55P) and voltage (LV-20P) sensors were

used to measure the currents and voltages. The details of the hardware setup are given in Table 2. The picture of the hardware setup is presented in Figure 15.

The estimated values of the resistance and reactance under balanced grid voltage are shown in Figure 16. It can be seen that the estimated resistance which represents the equivalent loss resistance is about 1.3 Ω. This is more than the dc winding resistance of the inductor. The corresponding values during unbalanced and distorted grid conditions are shown in Figure 17. The estimated resistance and reactance now represent the corresponding positive sequence components, which in a three wire system are the same as the negative sequence components. From Figure 16 and Figure 17, it can be seen that the estimated resistance and reactance are the same under both balanced and unbalanced grid conditions. Hence the proposed estimation algorithm ensures accurate estimation under both balanced and unbalanced grid conditions.

Table 2. Hardware Components.

Part	Manufacturer	Specifications
Switches (S_1-S_6)	International Rectifiers (IRGP50B60PD1PbF)	V_{ds}=600 V, I_d =30 A
Inductor(L)	-	L=5.5 mH, r_{dc} = 0.4 Ω
Dc bus capacitor	Epcos (B43704B5338M)	450 V, 3300 μF
Current Sensors	LA-55P	
Voltage Sensors	LV-25P	

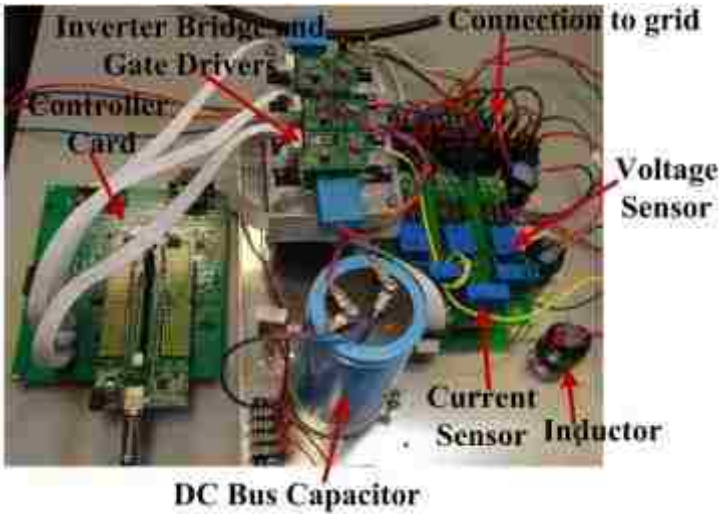


Figure 15. Picture of the hardware setup.

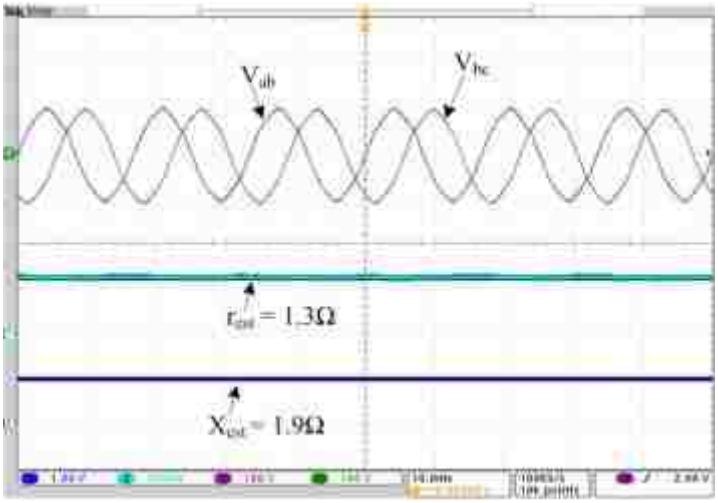


Figure 16. Estimated resistance and reactance under balanced grid voltage (r_{est} : 1 Ω/div, X_{est} : 2 Ω/div).

The estimated values of the resistance and reactance during a change in active power from 375 W to 750 W are shown in Figure 18. The corresponding values during a change in reactive power from 375 VAR to 750 VAR are shown in Figure 19.

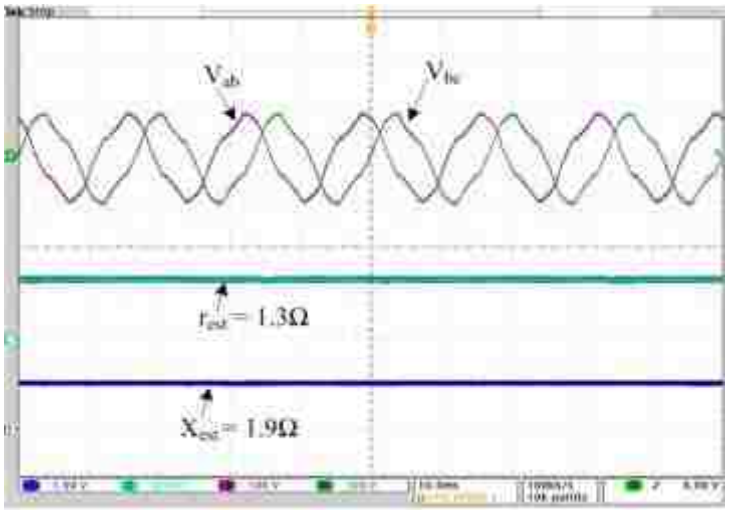


Figure 17. Estimated resistance and reactance under unbalanced and distorted grid voltage (r_{est} : 1 Ω/div, X_{est} : 2 Ω/div).

It can easily be observed from Figure 18 and Figure 19 that due to the adaptive nature of the control, the estimated resistance and reactance have some reasonable variations. The values actually vary with the delivered active and reactive power. The estimated values for the different conditions are tabulated in Table 3. It can be observed that the equivalent resistance when supplying reactive power is slightly more than the equivalent resistance while supplying active power. While supplying reactive power, the current is leading or lagging at about 90 degrees. So, the conduction time of the anti-parallel diode across each switch is much more when supplying reactive power compared to when active power is supplied by the inverter. As the voltage drop across the anti-parallel diode is more than the drop across the active switch [32], the conduction losses of the anti-parallel diodes are more than the active switches. The equivalent resistance represents the active power loss and hence is slightly more when supplying reactive power. Observations of Figure 18 and Figure 19 show that the estimated resistance decreases with the increase in the current. This can be explained by considering the on state characteristic of the switch. The switch

being an IGBT can be represented as a voltage drop during its on state. This voltage drop does not change in the same proportion as the current [32]. Hence with the increase in the current, the equivalent resistance decreases. Again, with the increase in current, the inductor slowly goes into saturation. This justifies the slight decrease in the estimated reactance with the increase in the current as can be seen in Figure 18 and Figure 19. The performance of the MRAC approach in estimating the equivalent resistance and reactance is demonstrated in Figure 20. With the inverter supplying 600 W of active power, an additional external resistance of 0.85 Ω was added to each of the phases. The results are shown in Figure 20. It is seen that the estimated resistance tracks and converges to the new value of 2.25 Ω, while the estimated reactance remains unchanged. During the transient period when the estimated resistance is not equal to the actual resistance the phase current deviates from its reference value, but the error is negligible as soon as the estimated resistance converges with the actual value as in the circuit. However, during this sudden addition of resistance no unstable operation is observed. It should also be noted that the addition of the resistance caused no change in the estimated reactance, which was maintained at 1.9 Ω

Table 3. Estimated Values of Resistance and Reactance.

	Active Power (W)		Reactive Power (VAR)	
	375	750	375	750
Equivalent Resistance (Ω)	1.3	1.17	1.6	1.3
Equivalent Reactance (Ω)	1.9	1.78	1.8	1.6

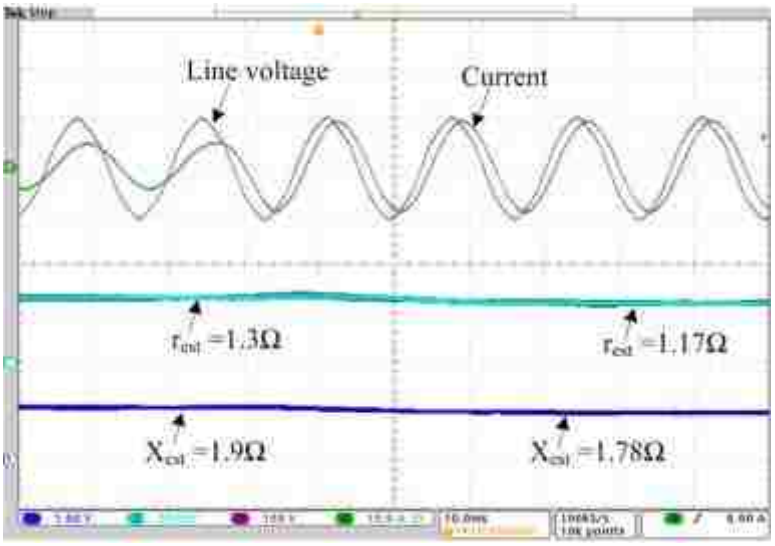


Figure 18. Line voltage and current waveform during transition from P = 375 W to P = 750 W (r_{est} : 1 Ω/div, X_{est} : 2 Ω/div).

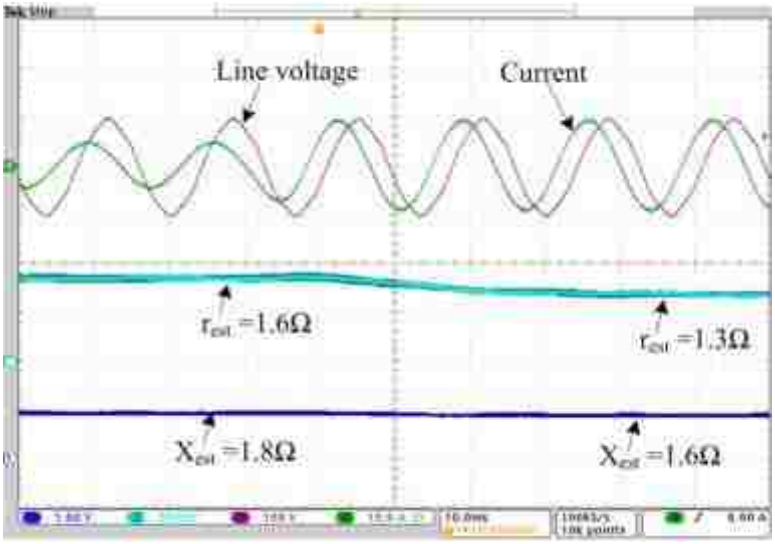


Figure 19. Line voltage and current waveform during transition from Q = 375 VAR to Q = 750 VAR (r_{est} : 1 Ω/div, X_{est} : 2 Ω/div).

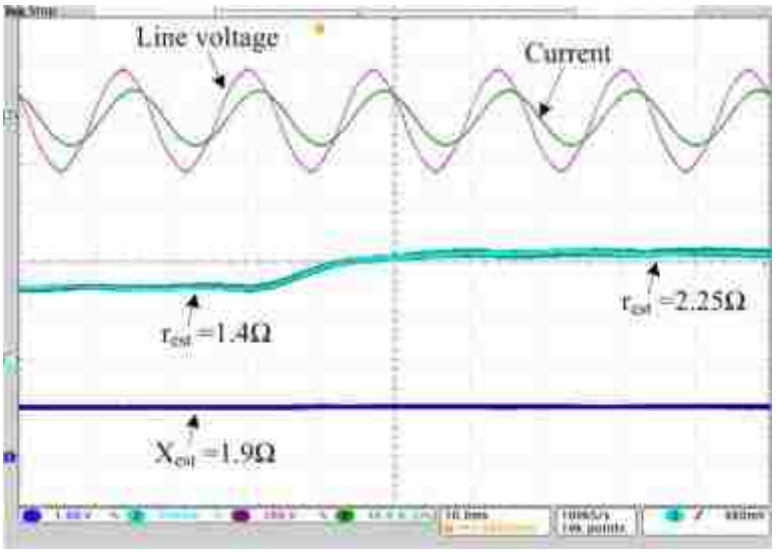
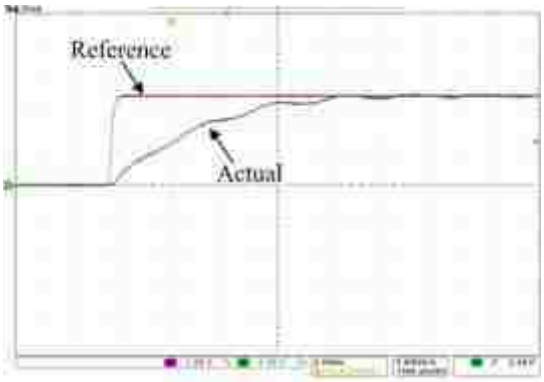


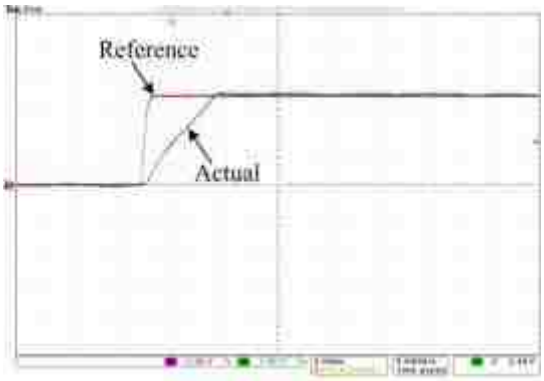
Figure 20. Line voltage, current, estimated resistance and estimated reactance during an addition of 0.85 Ω (r_{est} : 1 Ω/div, X_{est} : 2 Ω/div).

The utility of the proposed estimated method to tune the parameters of the current controller is demonstrated. A 3-phase grid connected converter is generally controlled in the synchronous (*dq*) frame of reference fixed to the grid voltage vector. Typical responses to the *d*-axis reference current are shown in Figure 21. Figure 21a and Figure 21b show responses for non-optimally tuned controller, where the parameters of the plant model (the equivalent loss resistance and inductance) were not accurately known. In such cases the response may be underdamped exhibiting overshoot (Figure 21a) or may be overdamped exhibiting (Figure 21b) long settling time. However with the correct knowledge of the plant parameters (as obtained with the proposed algorithm in this paper) the controller parameters can be tuned to get the optimal response as in Figure 21c.

(a)



(b)



(c)

Figure 21. Reference and actual *d*-axis current in current controlled grid connected converter (a) Response exhibiting overshoot, (b) Overdamped response exhibiting long settling time, (c) Response with optimally tuned controller parameters.

5. CONCLUSION

This paper presented the control architecture of a grid connected inverter using the MRAC approach. The MRAC estimators were used to estimate the equivalent loss resistance and reactance between the inverter and the grid. The small signal model of the system required for the MRAC based controller design was presented and the global asymptotic stability was ensured. The MRAC controller design, based on the presented small signal plant model was discussed. The estimated values will be helpful to determine accurate plant model which will in turn help design accurate control parameters for the current controllers. Experimental results were presented supporting the proposed approach.

APPENDIX

The mathematical proof of (22) and (23) is presented below. Consider a set of positive sequence current given as

$$\begin{bmatrix} i_a^+ \\ i_b^+ \\ i_c^+ \end{bmatrix} = \begin{bmatrix} I^+ \cos(\omega t - \phi) \\ I^+ \cos(\omega t - \phi - 2*\pi/3) \\ I^+ \cos(\omega t - \phi - 4*\pi/3) \end{bmatrix} \quad \text{(A1)}$$

Using the transformation T as in (1), the corresponding components in the 2-phase stationary frame of reference can be found as

$$\begin{bmatrix} i_\alpha^+ \\ i_\beta^+ \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a^+ \\ i_b^+ \\ i_c^+ \end{bmatrix} \tag{A2}$$

Substituting i_a^+, i_b^+, i_c^+ from (A1) in (A2)

$$\begin{bmatrix} i_\alpha^+ \\ i_\beta^+ \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I^+ \cos(\omega t - \phi) \\ I^+ \cos(\omega t - \phi - 2*\pi/3) \\ I^+ \cos(\omega t - \phi - 4*\pi/3) \end{bmatrix} \tag{A3}$$

or,

$$\begin{bmatrix} i_\alpha^+ \\ i_\beta^+ \end{bmatrix} = \begin{bmatrix} I^+ \cos(\omega t - \phi) \\ I^+ \sin(\omega t - \phi) \end{bmatrix} \tag{A4}$$

Let us now consider the derivative of i_α^+

$$\frac{di_\alpha^+}{dt} = I^+ \frac{d\cos(\omega t - \phi)}{dt} \tag{A5}$$

$$\frac{di_\alpha^+}{dt} = -\omega I^+ \sin(\omega t - \phi) \tag{A6}$$

However, from (A4) it can be noted that

$$i_\beta^+ = I^+ \sin(\omega t - \phi) \tag{A7}$$

Using (A4) in (A6)

$$\frac{di_\alpha^+}{dt} = -\omega i_\beta^+ \tag{A8}$$

Similarly if we consider the derivative of i_β^+

$$\frac{di_{\beta}^{+}}{dt} = I^{+}\frac{d\sin(\omega t-\phi)}{dt} \tag{A9}$$

$$\frac{di_{\beta}^{+}}{dt} = \omega I^{+}\cos(\omega t-\phi) \tag{A10}$$

Again, from (A4) it can be noted that

$$i_{\alpha}^{+} = I^{+}\cos(\omega t-\phi) \tag{A11}$$

Using (A4) in (A9)

$$\frac{di_{\beta}^{+}}{dt} = \omega i_{\alpha}^{+} \tag{A12}$$

Equations (A8) and (A12) prove the equations (22) and (23) in the main text.

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V. POWER-ANGLE SYNCHRONIZATION FOR GRID-CONNECTED CONVERTER WITH FAULT RIDE-THROUGH CAPABILITY FOR LOW VOLTAGE GRIDS

ABSTRACT

In this paper, the power angle synchronization control of a grid-tied bidirectional dc-ac converter is investigated for low voltage grids. The power flow equations for the low voltage grid are analyzed and compensators are designed to ensure the decoupled control of active and reactive power. The proposed control system operates without the need for a phase locked loop during balanced and unbalanced grid conditions. It is shown that during balanced conditions the compensators ensure stable operation controlling the desired power flow to and from the grid. It is also demonstrated that the compensators are immune to grid fluctuations and to a large extent can cater grid unbalanced conditions. Experimental results verify the performance of the proposed control scheme.

1. INTRODUCTION

With the increased use of renewable energy resources more and more voltage source power electronic converters (VSC) are being interfaced to the grid [1]. Usually, the active and reactive power flow between the converter and grid is controlled by controlling the converter current (see Figure 1). In such cases, they are referred to as current-controlled converters [2]. The controller is usually implemented in the synchronous (*d-q*) frame of reference attached to the grid voltage. This control method is immensely popular as it enables the decoupled control of active and reactive power.

However, this approach requires a phase-locked loop (PLL) [3]-[10] to accurately estimate the phase angle of the grid voltages and generate unit vectors in phase with them. However, PLLs are nonlinear and challenging to model [9]−[14]. Furthermore, a PLL can lead to unstable operations in weak grids where a number of converters are connected to the grid each having their own PLL [14]-[16]. The authors in [10] present a flexible PLL structure applicable to single phase and 3-phase systems. However, the analysis is limited to balanced grid conditions. A detailed mathematical analysis of the drawbacks of PLLs is beyond the scope of this paper. Such details are dealt in [11]-[16].

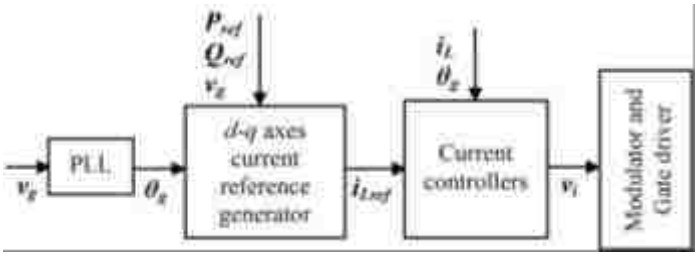

Figure 1. Control structure for current controlled VSC.

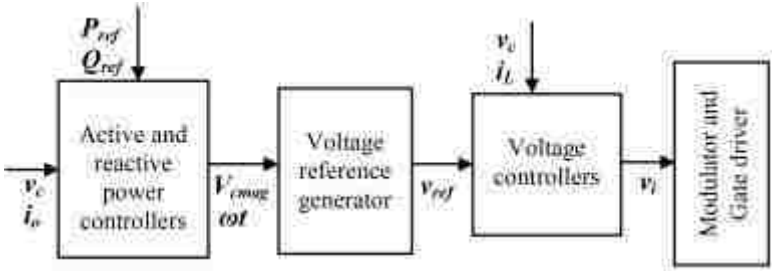

Figure 2. Control structure for voltage controlled grid connected VSC.

To eliminate the drawbacks of the PLL, alternate approaches like virtual synchronous machine [17] or synchroverter [18], [19] have been proposed forcontrolling grid tied VSCs where the inverter connected to the grid represents a virtual synchronous

machine. However, all these approaches (except [19]) require a PLL for the start-up. Furthermore, during grid unbalanced conditions, the phase currents exhibit large magnitudes which in practical systems will cause the protection circuit to trip thereby disconnecting the converter from the grid. The control presented in [19] avoids the initial PLL but still has the problem of large currents (as seen from the results presented in the paper) during grid unbalanced conditions.

A grid-connected VSC can also be controlled as a voltage controlled converter, where the output voltage of the converter is adjusted to deliver the desired active and reactive power to the grid. A typical control structure is represented in Figure 2. In such control architectures, active and reactive power controllers generate the desired voltage reference. Suitably designed voltage compensators will then track the generated voltage references to ensure the desired power is transferred to the grid. Such a control approach is known as the power-angle synchronization in the existing literature and can be implemented based on the power flow equations and does not require a PLL. At the same time, it retains the main advantage of the conventional current control technique, namely the decoupled control of the active and reactive power. The control of a grid-tied VSC as voltage controlled converter has been studied for high voltage grids [20], where the power transmission line is mainly inductive. However, during grid unbalanced conditions, the controller structure is switched to conventional current control scheme to limit the fault currents. Improved power-angle synchronization with a nonlinear damper to improve the stability is presented in [21]. However, the effects of grid frequency variations are not reported. Moreover, the control scheme is verified only through simulations and restricted to inductive grids.

Existing work on power-angle synchronization is limited to medium or high voltage grids [20]−[24]. Distinctively, this paper focuses on low voltage grids. An example of such a grid is a community microgrid, where renewable energy sources supply few local loads and the utility grid [25]. Ample examples of application of droop control in low voltage grid exist in literature, a few are cited in [27]-[28]. However, to the best knowledge of the authors the study of power-angle synchronization for low voltage grid has not been done in literature. A low voltage level grid, unlike the high voltage grid, is more resistive (see Table 1 in [26]) and so the power flow equations in a low voltage grid are fundamentally different from those in the high voltage grid [27], [28]. The power flow equations being different; the corresponding system model for the power-angle synchronization will change. This will ultimately change the design of the controller and lead to a new controller structure. The main contributions of this paper are i) establishing that the power-angle synchronization in a low voltage grid is different from an inductive grid, ii) proposing a control structure based on resonant controllers that ensures the converter has safe ride through during grid unbalanced conditions with the phase currents within reasonable limits; and iii) validating the proposed control structure through experimental results. The proposed control structure for voltage controlled grid connected converter can be used as an alternative to the droop control architecture [27], [28] when only one converter is connected to the grid. This eliminates the drop in terminal voltage and frequency caused by the droop controller.

The rest of the paper is arranged as follows. Section 2 reviews the power flow equations and establishes that the system model required for power-angle synchronization in low voltage grids is different from high voltage grids. The necessary system model

required to design the active and reactive power controllers is also discussed in this section. Based on this model, the controller design is presented in Section 3. Additional issues like startup procedure are also addressed in this section. Results are demonstrated in Section 4, and the conclusions are presented in Section 5.

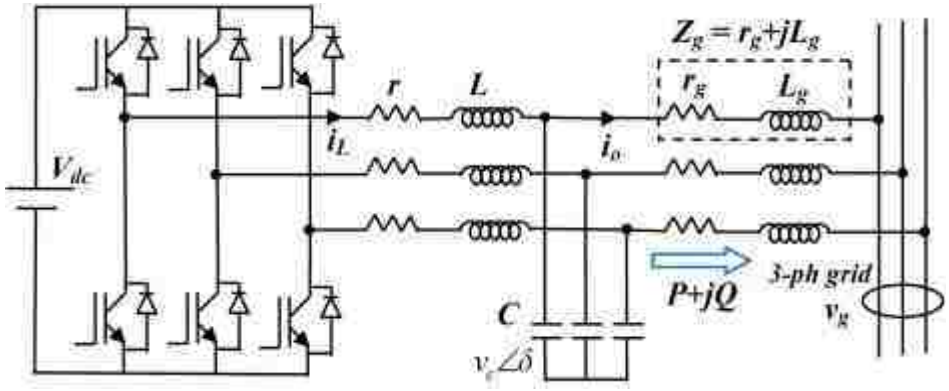

Figure 3. 3-phase grid-connected VSC.

2. POWER FLOW EQUATIONS AND SYSTEM MODELLING FOR LOW VOLTAGE GRIDS

A 3-phase grid-connected converter configured as a voltage controlled converter is shown in Figure 3. In the figure, L is the per phase filter inductance, r is the per phase winding resistance of the filter inductor, C is the per phase filter capacitance, $Z_g = r_g + j\omega_g L_g$, is the per phase impedance of the cable connecting the converter to the grid, ω_g is the angular frequency of the grid, i_L is the per phase filter inductor current, i_o is the per phase load current and v_c is the per phase output voltage of the converter. It should be noted that in such a configuration the active and reactive power transfer from the output

of the converter (after the capacitor) to the grid is of main interest. The per phase active and reactive power delivered by the converter to the grid can be expressed as

$$P = \frac{1}{2}\left[(\frac{V_c^2}{Z_g^2} - \frac{V_c V_g \cos\delta}{Z_g^2}) r_g + \frac{V_c V_g}{Z_g^2} X_g \sin\delta \right] \quad (1)$$

$$Q = \frac{1}{2}\left[(\frac{V_c^2}{Z_g^2} - \frac{V_c V_g \cos\delta}{Z_g^2}) X_g - \frac{V_c V_g}{Z_g^2} r_g \sin\delta \right] \quad (2)$$

where, P and Q are the per phase delivered active and reactive power, V_g is the peak value of the phase voltage of the grid, V_c is the peak value of the output voltage of the converter (after the capacitor) and δ is the phase angle between grid voltage and inverter output voltage which is also termed as the power angle.

As demonstrated in [20]-[26], [30], the per phase active power and reactive power delivered by the converter to an inductive grid where $X_g >> r_g$ is given as

$$P \approx \frac{V_c V_g}{2X_g} \sin\delta \quad (3)$$

$$Q \approx \frac{V_c}{2X_g} (V_c - V_g \cos\delta) \quad (4)$$

Generally, power angle δ is small, hence, (3) and (4) suggest that the active and reactive power injected to the grid can be independently controlled by controlling power angle δ and the magnitude of the converter output voltage V_c respectively. For designing the active and reactive power compensators, the small signal transfer function of $\Delta P/\Delta\delta$ and $\Delta Q/\Delta V_c$ must be known. These are derived in [20] and are reported below

$$\frac{\Delta P}{\Delta\delta} = \frac{V_{c0}}{\omega_g L_g}\left[\frac{(V_g \cos\delta - V_c)s^2 + \omega_g^2 V_g \cos\delta}{(s + r_g / L_g)^2 + \omega_g^2} \right] \quad (5)$$

$$\frac{\Delta Q}{\Delta V_c} = \frac{1}{\omega_g L_g}\left[\frac{(V_c - V_g\cos\delta)s^2 + \omega_g^2(2V_c - V_g\cos\delta)}{(s + r_g / L_g)^2 + \omega_g^2}\right] \quad (6)$$

The corresponding active and reactive power controller structure as given in [20] is such that the active power controller generates the reference for the load angle while the reactive controller generates the reference for the magnitude of the output voltage. This controller shows satisfactory performance for inductive grids. However, for a low voltage grid with a typical line impedance of $Z_g = 0.03+j0.02$, the performance of the controller is reported in Figure 4. It is seen that the actual values of the active and reactive power do not converge to the corresponding reference values. This motivates to take a fresh look at power-angle synchronization in low voltage grids.

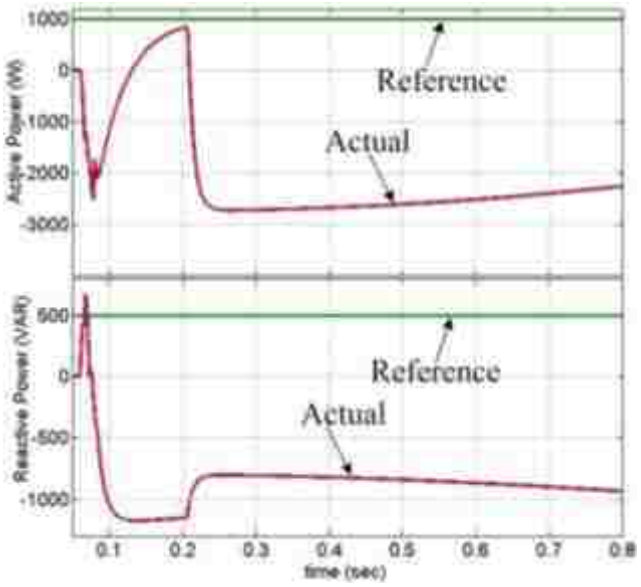

Figure 4. Performance of the power-angle synchronization controller of high voltage (inductive) grids [20] when applied to low voltage grids.

A low voltage grid, unlike the high voltage grid, is more resistive [26]. Hence (1) and (2) cannot be simplified to (3) and (4). Thus, *P* and *Q* are coupled and unique

relationships among P, Q, V_c and δ cannot be defined. The problem can be solved by adding inductor or resistor with the connecting cable. However, addition of inductors or resistors makes the system bulky and increases the losses. An alternative mean to solve by problem is by implementing virtual inductance or resistance at the output of the converter in series with the impedance of the connecting cable. Implementing a virtual inductance requires a differentiator or a high pass filter [30], which increases the complexity of the system. However, implementing virtual resistor is far simpler. A suitably selected virtual resistance, r_{vir}, makes the net output impedance, r_{eff}, more resistive than reactive. Equations (1) and (2) are now modified as

$$P \approx \frac{V_c}{2r_{eff}}(V_c - V_g) \tag{7}$$

$$Q \approx -\frac{V_c V_g}{2r_{eff}}\delta \tag{8}$$

In (7) and (8) r_{eff} is the sum of r_g and r_{vir}.

Equations (7) and (8) suggest that contrary to the inductive grid, the active and reactive power injected to the grid can be independently controlled by controlling the magnitude of the converter output voltage V_c and the power angle δ, respectively [27], [28]. As the active power P is controlled by V_c, the active power compensator will now generate the reference for the required voltage magnitude. On the other hand, as the reactive power Q is controlled by δ, the reactive power compensator will generate the reference for load angle δ and frequency. To design the controllers, the small signal transfer functions of $\Delta P/\Delta V_c$, $\Delta Q/\Delta\delta$ need to be derived for a low voltage grid. It should be remembered, this is opposite to as in medium or high voltage grid. The small signal modeling was introduced in [29] and is presented here for completeness of the article.

The modeling is done in the synchronous (*d-q*) frame of reference attached to the grid voltage where the active and reactive power delivered by the converter is given by

$$P = v_{cd} i_{od} + v_{cq} i_{oq} \tag{9}$$

$$Q = v_{cq} i_{od} - v_{cd} i_{oq} \tag{10}$$

The power equations as in (9) and (10) are nonlinear. It is desired to use linear control structure to control the active and reactive power. Hence, a small signal linearized plant model has to be derived from (9) and (10). Linearizing (9) and (10) results

$$\Delta P = V_{cd} \Delta I_{od} + V_{cq} \Delta I_{oq} + \Delta V_{cd} I_{od} + \Delta V_{cq} I_{oq} \tag{11}$$

$$\Delta Q = V_{cq} \Delta I_{od} - V_{cd} \Delta I_{oq} + \Delta V_{cq} I_{od} - \Delta V_{cd} I_{oq} \tag{12}$$

where, ΔI_{od} and ΔI_{oq} are small perturbations in the *d*-axis and *q*-axis load currents. Similarly, ΔV_{cd} and ΔV_{cq} are small perturbations in the *d*-axis and *q*-axis output voltages. The corresponding steady state values of the currents and voltages being I_{od}, I_{oq}, V_{cd} and V_{cq} respectively. ΔP and ΔQ are the resulting changes in the active and reactive power.

While connected to the grid, the output current dynamics represented in the *d-q* frame of reference are given as

$$L_g \frac{di_{od}}{dt} + r_{eff} i_{od} - \omega_g L_g i_{oq} = V_c \cos\delta - V_g \tag{13}$$

$$L_g \frac{di_{oq}}{dt} + r_{eff} i_{oq} + \omega_g L_g i_{od} = V_c \sin\delta \tag{14}$$

Equations (13) and (14) can be solved for the steady state value I_{od} and I_{oq}. At steady state all differential terms in (13) and (14) converge to zero. Using this and solving (13) and (14) for the steady state value I_{od} and I_{oq} yields

$$I_{od} = \frac{r_{eff}(V_{c0}\cos\delta - V_g) + \omega_g L_g V_{c0}\sin\delta}{r_{eff}^2 + (\omega_g L_g)^2} \tag{15}$$

$$I_{oq} = \frac{r_{eff}V_{c0}\sin\delta - (V_{c0}\cos\delta - V_g)\omega_g L_g}{r_{eff}^2 + (\omega_g L_g)^2} \tag{16}$$

where, V_{c0} is the steady state value of V_c.

To determine the transfer function $\Delta P/\Delta V_c$, (13) and (14) should be linearized with respect to V_c, neglecting any perturbations in load angle δ. Taking the Laplace transform of the linearized versions of (15) and (16) about an operating point results

$$(sL_g + r_{eff})\Delta I_{od} - \omega_g L_g \Delta I_{oq} = \Delta V_c \cos\delta \tag{17}$$

$$(sL_g + r_{eff})\Delta I_{oq} + \omega_g L_g \Delta I_{od} = \Delta V_c \sin\delta \tag{18}$$

where, ΔV_c is small perturbations in V_c about its steady state value V_{c0}. Solving (17) and (18) for ΔI_{od} and ΔI_{oq}

$$\Delta I_{od} = \frac{(sL_g + r_{eff})\cos\delta + \omega_g L_g \sin\delta}{(sL_g + r_{eff})^2 + (\omega_g L_g)^2}\Delta V_c \tag{19}$$

$$\Delta I_{oq} = \frac{(sL_g + r_{eff})\sin\delta - \omega_g L_g \cos\delta}{(sL_g + r_{eff})^2 + (\omega_g L_g)^2}\Delta V_c \tag{20}$$

By substituting (15), (16), (19) and (20) in (11), one can get

$$\frac{\Delta P}{\Delta V_c} = V_{c0}\left[\frac{(s + \frac{r_{eff}}{L_g})}{(s + \frac{r_{eff}}{L_g})^2 + \omega_g^2} + x\right] \tag{21}$$

Where,

$$x = \frac{\left(r_{eff}V_{c0} - V_g(r_{eff}\cos\delta - \omega L_g \sin\delta)\right)}{\left(V_{c0}{r_{eff}}^2 + V_{c0}(\omega_g L_g)^2\right)} \tag{22}$$

Simplifying (21) results

$$\frac{\Delta P}{\Delta V_c} = V_{c0}\left[\frac{s^2 + s(\frac{1+2r_{eff}x}{xL_g}) + \frac{r_{eff} + x(r_{eff}^2 + (\omega_g L_g)^2)}{xL_g^2}}{(s+\frac{r_{eff}}{L_g})^2 + \omega_g^2}\right] \tag{23}$$

Considering $\omega_g L_g << r_{eff}$, one can write

$$\frac{\Delta P}{\Delta V_c} = V_{c0}\left[\frac{(s+\frac{r_{eff}}{L_g})(s+\frac{1+xr_{eff}}{xL_g})}{(s+\frac{r_{eff}}{L_g})^2 + \omega_g^2}\right] \tag{24}$$

Similarly, to obtain small signal transfer functions $\Delta Q/\Delta\delta$, (13) and (14) have to be linearized with respect to δ, neglecting perturbations in V_c. The transfer function is represented as

$$\frac{\Delta Q}{\Delta \delta} = V_{c0}^2\left[\frac{(s+\frac{r_{eff}}{L_g})(s+\frac{xr_{eff}-1}{xL_g})}{(s+\frac{r_{eff}}{L_g})^2 + \omega_g^2}\right] \tag{25}$$

Equations (5) and (24) describe the small signal plant model for the active power controller in an inductive and resistive (low voltage) grid respectively. A comparison between the transfer functions of (5) and (24) is shown in Figure 5. It is seen that the system transfer function for an inductive grid is less damped and prone to instability compared to the system transfer function for a low voltage grid. However, compared to the inductive grid, a low voltage grid with virtual resistance (r_{vir}) is sufficiently stable. To implement the virtual resistance, a voltage proportional to the output current is calculated for each of the three phases (see Figure 6). An initial estimate of Z_g can be found using a LCR meter tuned at the line frequency (60 Hz) or from the datasheet of the cable.

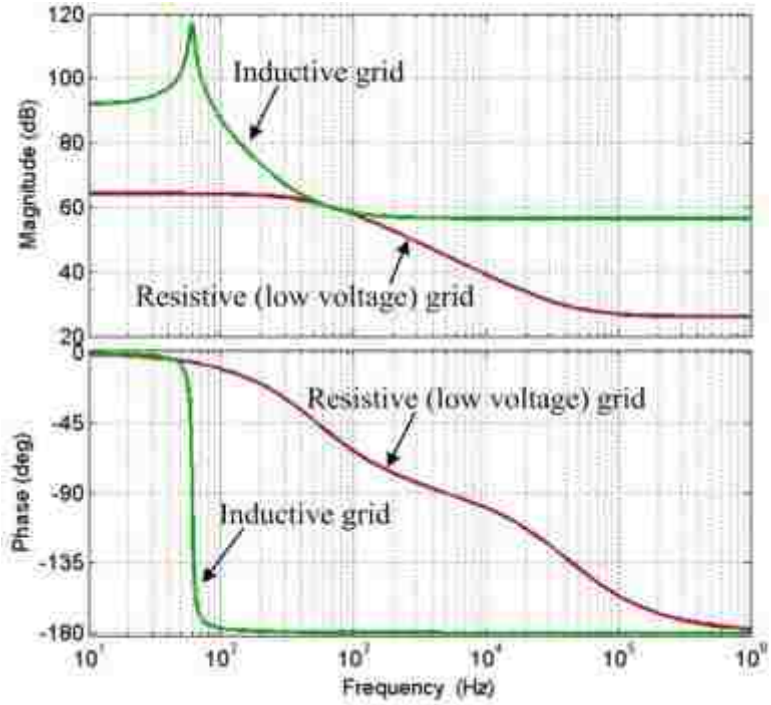

Figure 5. Comparison of the frequency response of the small signal model in (5) and (24).

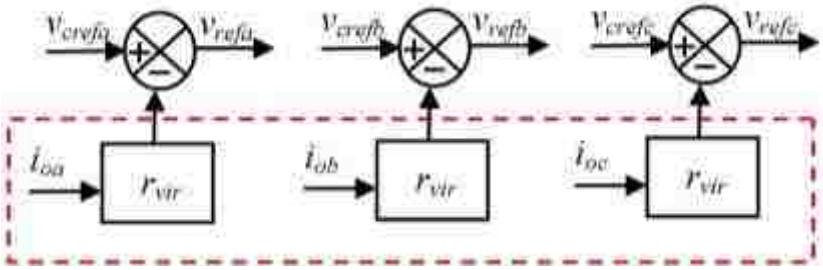

Figure 6. Implementing the virtual resistance for better decoupling between active and reactive power.

3. CONTROLLER STRUCTURE

3.1 Active and Reactive Power Compensators

The active and reactive power controllers constitute an integral part of the controller structure shown in Figure 2. The required transfer functions for the active and

reactive compensator design are given by (24) and (25). For 3-phase balanced systems, the instantaneous active and reactive powers are dc quantities. Hence for balanced systems as reported in [29] a simple proportional integral (PI) controller is sufficient to ensure satisfactory controller performance. However, unbalances in the grid voltage give rise to oscillations in the active and reactive power. The frequency of the oscillation is at double the fundamental frequency of the line voltage. To ensure satisfactory performance during both balanced and unbalanced grid conditions, proportional-integral-resonant (PIR) controller is proposed as the active and reactive power controllers. The controller is easily achieved by augmenting the PI controller with a resonant peak. The integral part tracks the dc references while the proportional gain achieves the bandwidth for the desired transient response. The resonant peak is tuned at the second harmonic frequency. It helps to limit the ripple in the active and reactive power during unbalanced voltage conditions thereby keeping the line currents within safe limits. It is known that perfectly ripple free power (both active and reactive) and sinusoidal currents cannot be simultaneously achieved in unbalanced 3-wire grid systems [31], [32]. To attenuate the oscillations in the power, distortions must be allowed in the currents. This is acceptable since the main purpose of the controller is to ensure safe ride through during a fault condition without the converter being disconnected from the grid. The proposed structure for active and reactive power controllers is shown in Figure 7. In this figure, ω_{ref} is the nominal angular frequency of the grid and V_{cnom} is the nominal magnitude of the phase voltage.

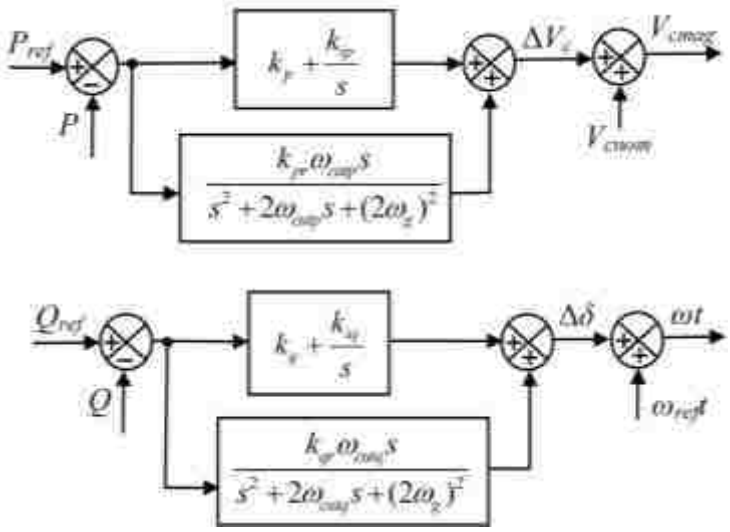

Figure 7. Proposed control structure of the active and reactive power compensators.

The controller parameters are selected based on the small signal transfer functions as obtained in (24) and (25). The active and reactive power compensators are followed by voltage control loops. The overall structure thus shapes as a cascaded or multi-loop control structure. In a multi-loop structure, the bandwidth of the outer loop is kept much smaller than the bandwidth of the inner loop. This ensures that the dynamics of the outer loop is not influenced by the dynamics of the inner loop. Typically, choosing a bandwidth of 2 kHz for the voltage controllers, the parameters of the power compensators are so chosen that the maximum bandwidth of each of the power control loops is allowed to be 600 Hz with a minimum gain of 40 dB at the resonant frequency. The active power compensator is given as

$$G_{\Delta V_c(\mathbf{s})} = \left(k_p + \frac{k_{ip}}{s} + \frac{k_{pr}\omega_{cutp}s}{s^2 + 2\omega_{cutp}s + (2\omega_g)^2} \right) \tag{26}$$

where, k_p is the proportional gain, k_{ip} is the integral gain, k_{pr} is the resonant gain, and ω_{cutp} is the cutoff frequency. The reactive power compensator generating reference for the

change in load angle is similar in structure and is given as

$$G_{\Delta\delta(s)} = \left(k_q + \frac{k_{iq}}{s} + \frac{k_{qr}\omega_{cutq}s}{s^2 + 2\omega_{cutq}s + (2\omega_g)^2} \right) \tag{27}$$

The frequency response of the loop gain of plant and compensator for the active power controller is shown in Figure 8, while that for the reactive power compensator generating reference of the load angle and frequency is shown in Figure 9. The controller parameters are listed in Table 1.

The derivation of the small signal transfer functions and the corresponding controller design was done based on the knowledge of the grid impedance Z_g. It can be argued that such a design is not very prudent as the grid impedance may change. However, it should be noted that a virtual resistor was added to make the output impedance resistive. This virtual resistor solves the problem of variation in the grid impedance. As shown in Figure 10, three different loop gains of the active power controller and plant are plotted for different grid impedance (Z_g, $2Z_g$ and $0.5Z_g$) keeping the virtual resistance unchanged. It can be clearly seen that in the frequency range of interest (the gain cross over frequency) all three plots are almost identical. Thus it can be concluded that the virtual resistance serves a threefold purpose. In addition to decoupling the power flow equations and making the system more stable, it neutralizes the effect of grid impedance variations on the controller structure.

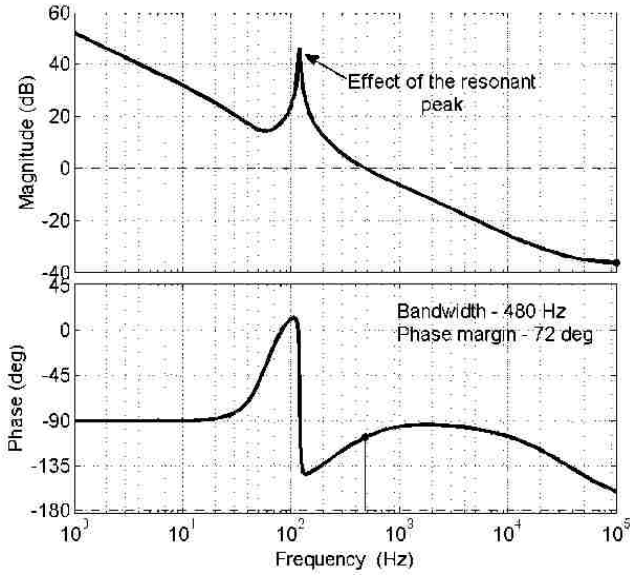

Figure 8. Bode plot of the active power controller and plant when consuming rated active power.

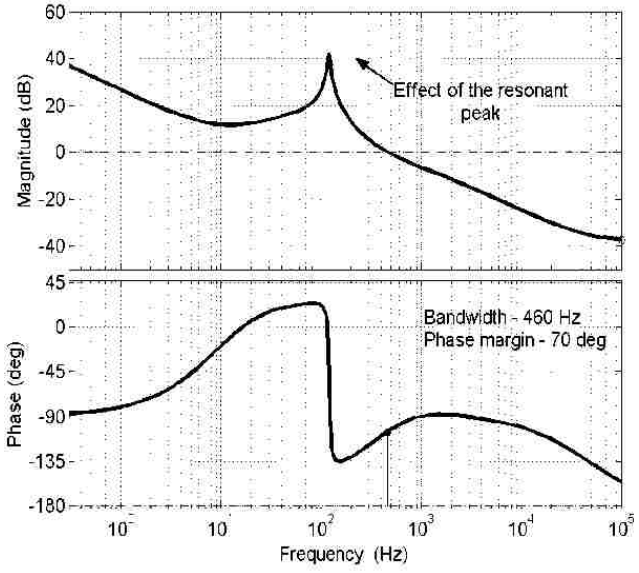

Figure 9. Bode plot of the reactive power controller and plant generating load angle reference when consuming rated active power.

Table 1. Parameters of the power Controllers.

Control output	Plant T.F.	Controller parameters
ΔV_c	$\Delta P(s)/\Delta V_c$ (s)	k_p= 0.045V/W, k_{ip}= 333V/Wsec, k_{pr}= 3V/Wsec, ω_{cutp} = 20 rad/sec
$\Delta\delta$	$\Delta Q(s)/\Delta\delta(s)$	k_q = 0.001rad/VAR, k_{iq}= 33.33rad/VARsec, k_{qr} = 0.05 rad/VARsec, ω_{cutq} = 20 rad/sec

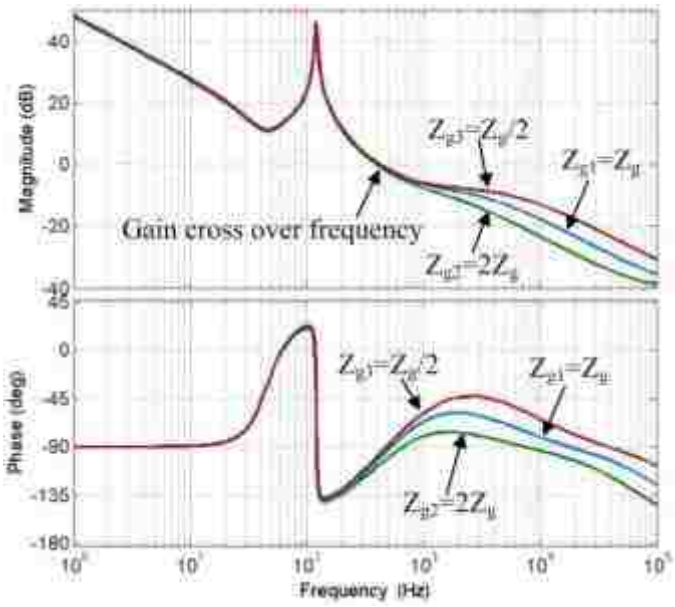

Figure 10. Bode plot of the active power controller and plant for different grid impedance.

3.2 Start-up Procedure

The controller structure as discussed in the previous section is developed based on a small signal model of the system. The controller thus needs the information of the initial phase of the grid voltage for stable operation. The exact information of the phase is not needed, only an approximate estimate is sufficient. Thus, a phase-locked loop (PLL)

is not necessary for the startup process. It is sufficient to determine the initial phase in an open-loop manner. One of the phase voltages, in this case v_{ca}, is passed through a band-pass filter to extract its fundamental component. The transfer function of the band pass filter is given by

$$G_{bandpass} = \frac{k\omega_{cut}s}{s^2 + k\omega_{cut}s + \omega_g^2} \tag{28}$$

As shown in Figure 11, the positive zero crossing of the output of the band pass filter is detected by a zero-crossing detecting (ZCD) algorithm and a unit sine wave is generated synchronized with this zero crossing. This initial zero crossing detection is called as the start-up bit. The other two 120-degree-phase-shifted sine waves are also generated inside the microcontroller. The controller is started with this initial estimate of the phase. The startup algorithm (the band pass filter and ZCD) needs to run only for one cycle until one zero crossing is detected after which it is bypassed. A properly designed controller can ensure stable operation delivering the desired active and reactive power to the grid, without the need for a PLL.

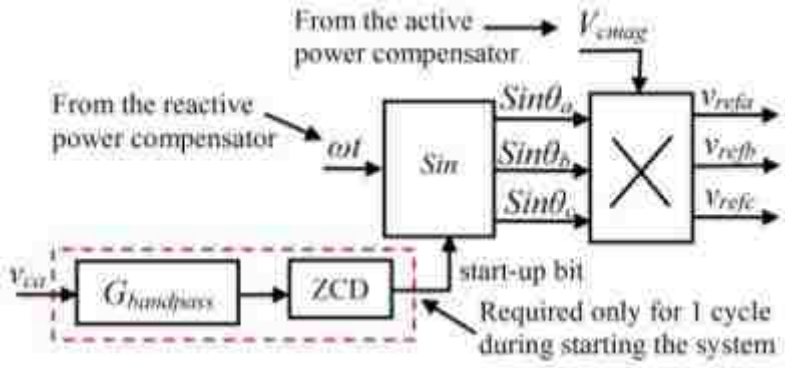

Figure 11. 3-phase voltage reference generation with the start-up circuit.

3.3 Voltage Controller

As depicted in Figure 2, the active and reactive power controllers are followed by voltage controllers. The voltage controller is implemented in the 2-phase stationary ($\alpha\beta$) frame of reference. The overall voltage controller structure is shown in Figure 12. A proportional−resonant (PR) controller with the resonant peak at the fundamental frequency is used as the voltage controller. An inner current loop is also added to improve the stability and phase margin of the controller. The inner current controller is generally taken as a proportional controller, the proportional gain being represented by k_{ci}. The voltage controller based on the PR structure has been studied in great details in the literature [33]−[35] and hence not discussed in details here. The α-axis voltage controller is represented as

$$G_v(s) = \left(k_{pv} + \frac{k_{vr}\omega_{cut}s}{s^2 + 2\omega_{cut}s + \omega_g{}^2} \right) \tag{29}$$

where, k_{pv} is the proportional gain, k_{vr} is the resonant gain, ω_{cut} is the cutoff frequency of the resonant controller. The entire α-axis controller structure with the inner current loop is shown in Figure 13. The β-axis controller is identical in structure. The system and voltage controller parameters are shown in Table 2. For the controller parameters as in Table 2, the frequency response of the voltage controller is shown in Figure 14.

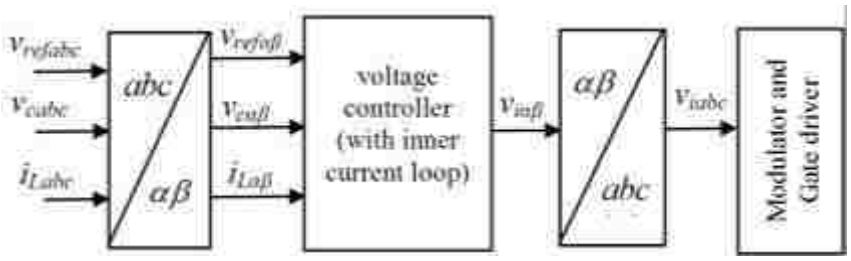

Figure 12. Inner voltage controller structure.

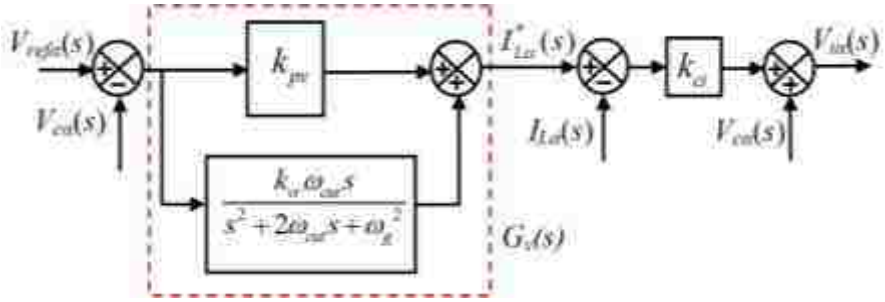

Figure 13. α-axis voltage controller with inner current loop.

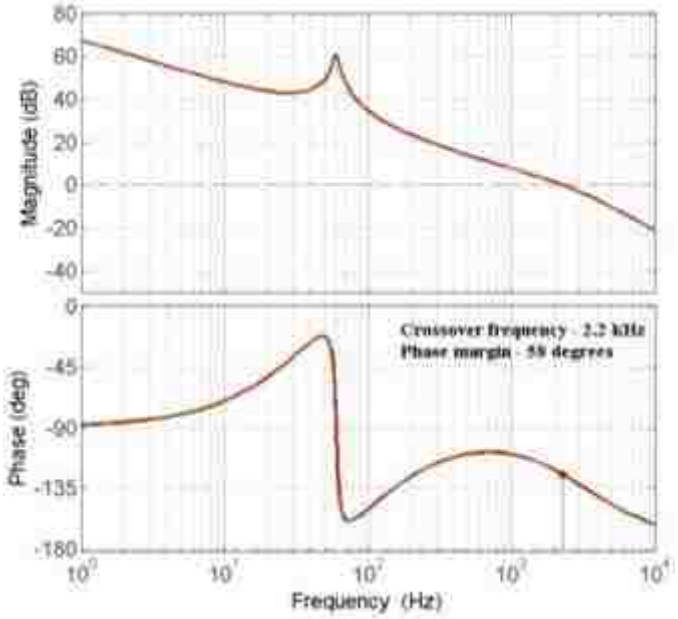

Figure 14. Frequency response of the loop gain of the voltage controller and plant.

Table 2. System Parameters and Voltage Controller Parameters.

L	5 mH
r	0.2 Ω
C	10 μF
Switching Frequency	20 kHz
Z_g	0.03+j0.02 Ω
r_{vir}	0.3 Ω
k_{pv}	0.3 A/V
ω_{cut}	30 rad/sec
k_{vr}	4 A/V
k_{ci}	60 V/A

Table 3. Hardware Components.

Part	Manufacturer	Specifications
Switches (S_1-S_6)	International Rectifiers (IRGP50B60PD1PbF)	V_{ds}=600 V, I_d =30 A
Filter Inductor(L)	-	L=5 mH, r_{dc} = 0.2 Ω
Filter Capacitor (C)	Epcos (B32678G8106K)	10 μF, 400 V
Dc bus capacitor	Epcos (B43704B5338M)	450 V, 3300 μF
Current Sensors	LA-55P	
Voltage Sensors	LV-20P	

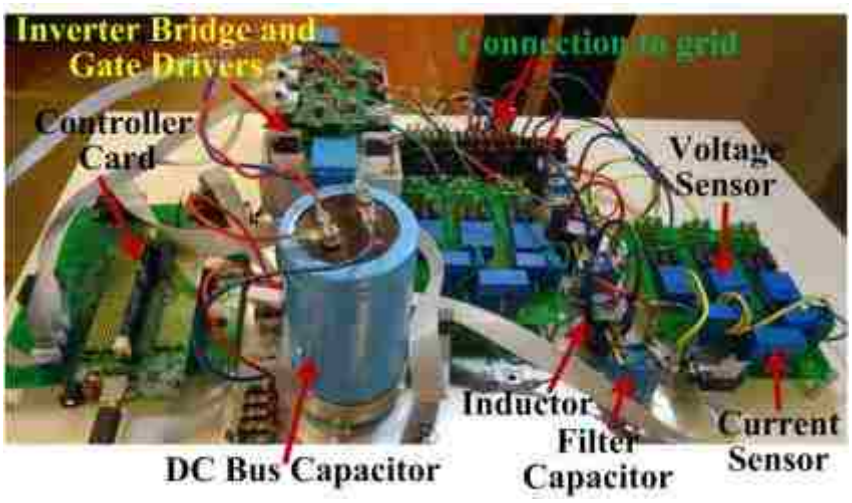

Figure 15. Picture of the hardware setup.

4. RESULTS AND DISCUSSIONS

Experimental results are reported for a 1 kVA laboratory prototype. The grid voltage was maintained at 135V line to line rms. The details of the components used for the hardware is given in Table 3. The picture of the hardware setup is presented in Figure 15. IRGP50B60PD1PbF IGBTs from International Rectifiers were used as the power switches of the converter bridge. Hall effect current (LA-55P) and voltage (LV-20P) sensors were used to measure the currents and voltages. The control algorithm was implemented in the TMS320F28335 digital signal processor from Texas Instruments. The start-up process with the earlier discussed start-up bit is shown in Figure 16. The same figure also shows the line voltage and phase current waveforms during the transient in active power from 0 W to 1 kW. It should be noted that the line voltage and phase current is shown in the Figure Hence the current lags the voltage by 30 degrees.

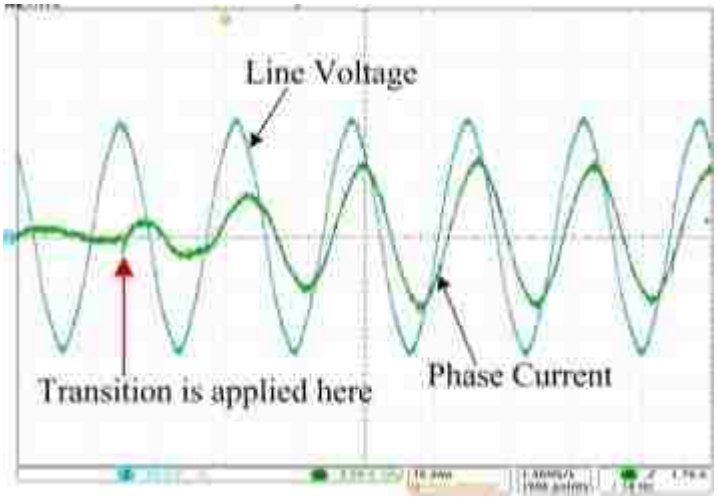

Figure 16. Line voltage and current waveform during transition from P = 0 W to P = 1 kW (Voltage : 80 V/div, Current : 5 A/div).

The decoupled nature of the controller is demonstrated in Figure 17 and Figure 18. P_{ref} was changed from 500 W to 1 kW and then back to 500 W with Q_{ref} kept constant at 500 VAR. The actual active and reactive powers are shown in Figure 17. As observed from Figure 17, a change in the active power from 500 W to 1 kW and from 1 kW back to 500 W was successfully achieved with negligible changes in the reactive power. This is because the active power is controlled by the magnitude of the voltage in low voltage grids which has negligible effect on the reactive power. The value of Q_{ref} was changed next with P_{ref} kept constant at 625 W. The corresponding changes in the actual active and reactive power are shown in Figure 18. Observing Figure 18, it can be concluded that changes in the reactive power (which is controlled by δ in low voltage grids) had no effect on the active power.

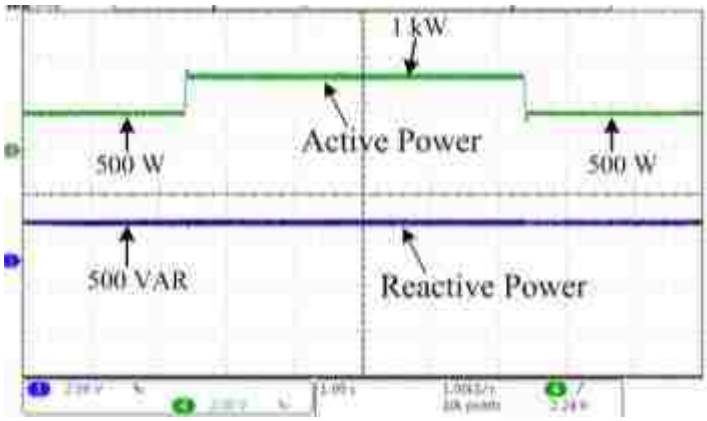

Figure 17. Change in active power with reactive power kept constant. (Active Power : 625 W/div, Reactive Power : 625 VAR/div).

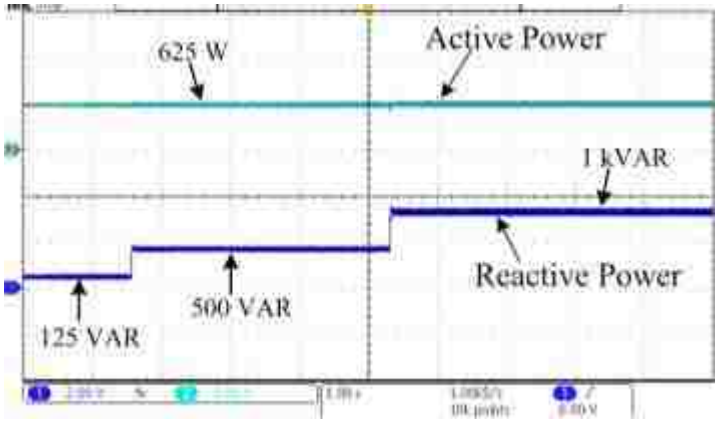

Figure 18. Change in reactive power with active power kept constant. (Active Power : 625 W/div, Reactive Power : 625 VAR/div).

Line voltage and phase current waveforms during the transition in active power from 0 W to −1 kW are shown in Figure 19. Results during transition in reactive power from 800 VAR to −1 kVAR are shown in Figure 20. The waveforms confirm stable operation during the transitions in active and reactive power.

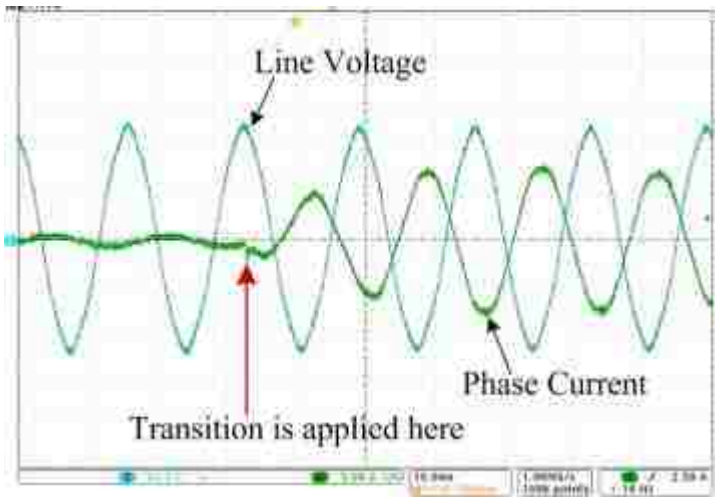

Figure 19. Line voltage and current waveform during transition from P = 0 W to P = −1 kW (Voltage : 80 V/div, Current : 5 A/div).

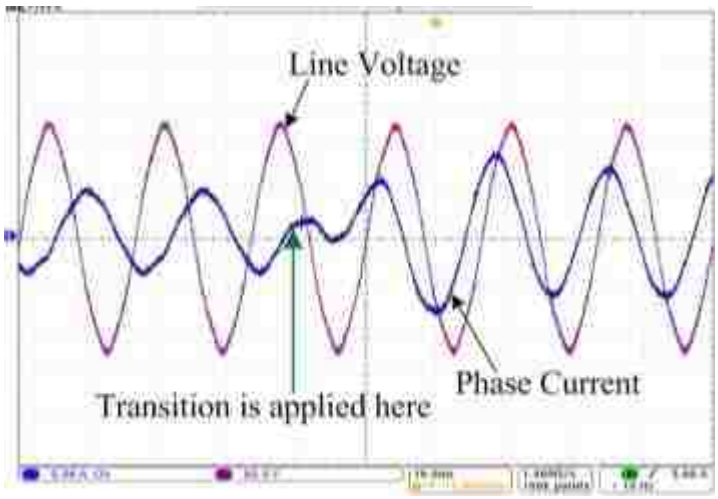

Figure 20. Line voltage and phase current during transition from Q = 0.8 kVAR to Q = −1 kVAR (Voltage : 80 V/div, Current : 5 A/div).

The experimental results for unbalanced grid voltage are presented next. It should be noted that the control objective was to minimize the ripple in the active and reactive power. The phase currents, active and reactive power delivered for 30 percent voltage sag in one of the phase voltage (here phase ‘a’ voltage) are shown in Fig. 21. The peak value

of the current is observed as 6.5 A with a ripple of 160 W (and 160 VAR) in the active and reactive power. Fig. 22 shows the same waveforms for 50 percent voltage sag. The peak value of the current is observed as 8.5 A with a ripple of 320 W (and 320 VAR) in the active and reactive power. It can be clearly seen that the grid currents are distorted and the active and reactive power supplied to the grid are contaminated with some ac ripple which increases with the increase in the magnitude of the voltage sag. However, the magnitude of the current is within limits. So it is possible for the controller to ensure safe ride through during unbalanced conditions without the converter being disconnected from the grid. This is an advantage over the controller proposed in [20] where the controller shifts to the conventional current controlled structure during a fault condition. The ripple in the active and reactive power is mainly contributed due to the harmonics in the grid voltage (the grid voltage available in the laboratory shows 3% fifth harmonic and 1.8% seventh harmonic components).

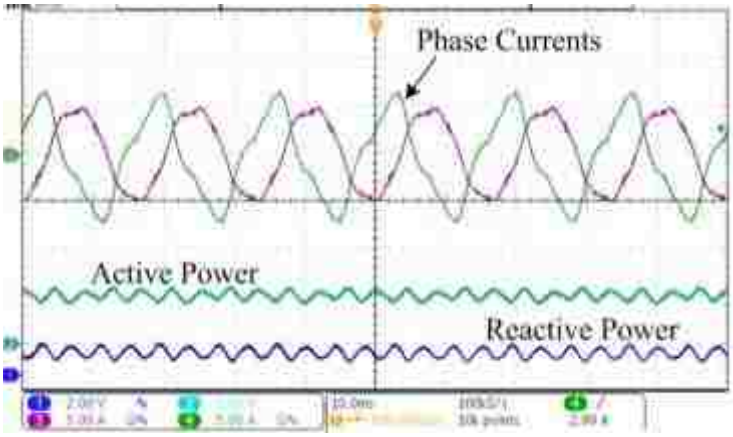

Figure 21. Line currents and power delivered during a 30% sag in voltage. (Active Power : 0.8 kW/div, Reactive Power : 0.8 kVAR/div).

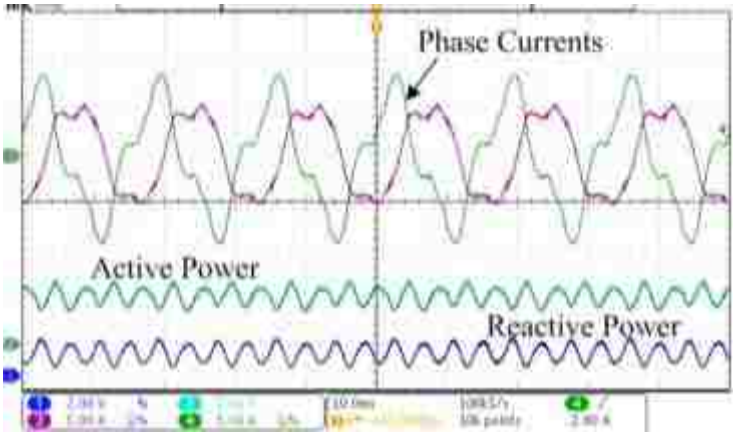

Figure 22. Line currents and power delivered during a 50% sag in voltage (Active Power : 0.8 kW/div, Reactive Power : 0.8 kVAR/div).

The proposed control architecture (as shown in Fig. 7) has resonant peaks at the second harmonic frequency to attenuate oscillations in the active and reactive power under unbalanced grid conditions. The performance of the resonant peaks added at twice the fundamental frequency during grid unbalanced conditions is demonstrated from Fig. 23. With the converter delivering 800 W of active power and 350 VAR of reactive power, the resonant portions of the compensators were disabled for five cycles and the enabled again. As seen from Fig. 23, the double-line frequency oscillations in the active and reactive power as well as the peak phase current are drastically increased during the period when the compensators were disabled. With the resonant controllers disabled, the oscillations in the active power reported a peak to peak value of 1000 W, while oscillations in the reactive power reported peak to peak value of 500 VAR. The peak value of the current increased from 5 A to 8.75 A. However, the oscillations in the active and reactive power as well as the peak current were highly attenuated as soon as the resonant controllers were enabled again.

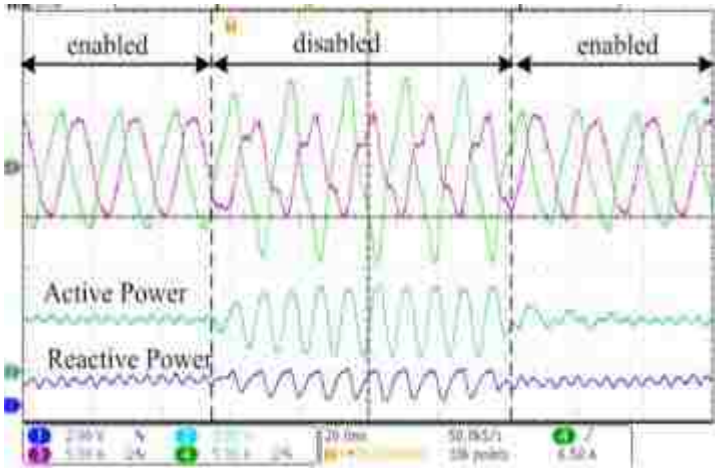

Figure 23. Line Currents, active and reactive power waveforms with the resonant portion of the active and reactive power compensators disabled for 5 cycles and enabled again (Active Power : 0.8 kW/div, Reactive Power : 0.8 kVAR/div).

5. CONCLUSION

This paper presented the power-angle synchronization to control a grid-connected VSC as a voltage-controlled voltage-source converter for low voltage grids. A virtual resistance based control scheme was used to ensure decoupled control of active and reactive power. Furthermore, the operation of the system did not require a PLL which reduces sensitivity to grid voltage unbalances and harmonics. The small signal modelling was discussed and the active and reactive power compensators were designed based on this model. The proposed controller could limit oscillations in the delivered power and the magnitude of the current during grid unbalanced conditions. Experimental results confirmed the stable operation of the converter with the proposed control scheme with its ability to deliver required active and reactive power to and from the grid under balanced and unbalanced grid conditions.

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2. CONCLUSION

This dissertation proposed new control algorithms dedicated towards improving the reliability, computational burden and stability in grid-connected and stand-alone based power electronic converter systems applicable for ac microgrids.

Addressing issues with the voltage sensor, two voltage sensorless control algorithms were proposed. The sensorless control algorithm for the standalone inverter was focused towards controlling the output voltage. The control approach, mainly based on the output capacitor current control was analyzed thoroughly. The system modeling was presented and a controller structure was proposed and designed based on the model. The proposed approach ensures better THD of the output voltage under nonlinear load conditions compared to conventional two loop voltage control approach achieving a THD as low as 1.6%. The estimation of the output filter capacitance based on the output voltage rms control loop was also discussed. It is shown that the method is largely insensitive to the filter inductor resistance and inductance variations, keeping the output voltage within regulation specifications.

The sensorless control algorithm for the grid-connected converter was focused towards estimating the fundamental component of the grid voltage. The proposed method can be used as an alternative to conventional PLL structures which need a dedicated voltage sensor. The estimation algorithm was able to extract the fundamental component of the grid voltage under distorted grid conditions and generate the unit vectors from it. In addition, it gave an estimation of the grid frequency. A simplified system model required for the controller design was presented. The effect of the dead-time on the proposed estimation method was studied and a model for the voltage drop due to the dead-time was

developed. The effects of parameter mismatch, basically the filter inductor inductance and equivalent loss resistance, on the estimated voltage were also analyzed.

The voltage estimation technique proposed for the grid connected converter was then extended to *LCL* based grid connected converter to establish an indirect control approach of the grid current. The grid current was controlled by estimating the filter capacitor current and then compensating the same from the converter side. The filter capacitor current was computed from the estimated filter capacitor voltage. The estimated fundamental and harmonic components of the filter capacitor current were then compensated from the converter side, thereby maintaining a sinusoidal grid current at the desired power factor.

This thesis presented an estimation method using the MRAC approach to get accurate online estimation of the system parameters in a grid connected inverter. The MRAC based estimators were used to estimate the equivalent loss resistance and reactance between the inverter and the grid. The small signal model of the system required for the MRAC based controller design was presented and the global asymptotic stability was ensured. The MRAC controller design, based on the presented small signal plant model was discussed. The estimated values will be helpful to determine accurate plant model which will in turn help design accurate control parameters for the current controllers. Experimental results were presented supporting the proposed approach.

Finally, this dissertation presented the power-angle synchronization to control a grid-connected VSC as a voltage-controlled voltage-source converter for low voltage grids. A virtual resistance based control scheme was used to ensure decoupled control of active and reactive power. Furthermore, the operation of the system did not require a PLL

which reduces sensitivity to grid voltage unbalances and harmonics. The small signal modelling was discussed and the active and reactive power compensators were designed based on this model. The proposed controller could limit oscillations in the delivered power and the magnitude of the current during grid unbalanced conditions.

Rigorous simulations and experiments were performed to verify the performance of each on the proposed control scheme.

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VITA

Subhajyoti Mukherjee completed the Bachelor of Engineering (B.E) degree in Electrical Engineering from Jadavpur University in 2007 and the Master of Technology (M.Tech) degree in Electrical Engineering from Indian Institute of Technology, Kharagpur in 2010. From July 2007 to June 2008 he worked in Siemens Limited, Kolkata as a Graduate Trainee Engineer working on programmable logic controller (PLC) based automation architectures. After completing the M.Tech degree, he worked for three years in several power electronics companies including Honeywell Technology Solutions Lab, Bangalore. During this time, he had the opportunity of working on different dc-dc isolated and non-isolated converter topologies, single phase and three phase bidirectional converters, working both on the design and control. In August 2013, he joined the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, as a full-time PhD student but transferred to Missouri University of Science and Technology in August 2014. In December 2017, he received the Ph.D. degree in Electrical Engineering from Missouri University of Science and Technology.