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FAR-FIELD PREDICTION USING ONLY MAGNETIC NEAR-FIELD SCANNING
AND MODELING DELAY VARIATIONS IN CMOS DIGITAL LOGIC CIRCUITS
DUE TO ELECTRICAL DISTURBANCES IN THE POWER SUPPLY

by

XU GAO

A DISSERTATION

Presented to the Faculty of the Graduate School of the
MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

DOCTOR OF PHILOSOPHY

in

ELECTRICAL ENGINEERING

2014

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PUBLICATION DISSERTATION OPTION

This dissertation consists of the following three articles that have been submitted for publications as follows:

Pages 4-34 have been accepted in IEEE TRANSCCTIONS ON
ELECTROMAGNETIC COMPATIBILITY

Pages 35-62 have been submitted to in IEEE TRANSCCTIONS ON
ELECTROMAGNETIC COMPATIBILITY

Pages 63-86 will be submitted to IEEE TRANSCCTIONS ON
ELECTROMAGNETIC COMPATIBILITY

ABSTRACT

This dissertation discusses two topics. In the first paper, a novel method to predict the far-field using only magnetic near-field on a Huygens surface is proposed. The electrical field on the Huygens surface was calculated from the magnetic near-field using the finite element method (FEM). Two examples were used to verify the proposed method. The validity of this method when the near-field is high-impedance field was verified as well. Sensitivity of the far-field to noise in both magnitude and phase in the near-field data was also investigated. The results indicate that the proposed method is very robust to the random variation of both. The effect of using only four sides of the Huygens box was investigated as well, revealing that, in some instances, the incomplete Huygens's box can be used to predict the far-field well. The second topic is discussed in the second and third papers. Soft errors can occur in digital integrated circuits (ICs) as a result of an electromagnetic disturbance. Many soft errors come from changes in propagation delays through digital logic which are caused by changes in the on-die power supply voltage. In the second paper, an analytical model was developed to predict timing variations in digital logic as a result of variations in the power supply voltage. In the third paper the delay model developed in second paper was extended into dynamic delay models, which is used to predict the clock period variation due to the disturbances in the power supply.

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1. INTRODUCTION

The first topic of this dissertation is far-field prediction using only magnetic near-field scanning. Near-field scanning has been used extensively for the far-field estimation of antennas. Applied to electromagnetic compatibility (EMC) problems, near-field scanning has been used to estimate emissions from both integrated circuits (ICs) and printed circuit boards (PCBs). Interest in applying far-field predictions using near-field to EMI/EMC problems has recently grown. To predict the far-field emissions from a PCB in the top half space, the near-field data on a planar surface above PCB usually is sufficient. However, near-field measurement on only one planar surface may not be enough to predict the far-field radiation of three-dimensional structures. The near-field on an enclosed Huygens's surface may be preferred for near-field scanning when predicting the far-field radiation associated with the EMI problems of some complex structures. Based on the equivalence theorem (Huygens's principle), both equivalent electric current obtained from the tangential magnetic field and equivalent magnetic current obtained from the tangential electric field are needed to perform far-field transformation from near-field data. However, designing electric field probes for tangential components is more difficult than designing magnetic field probes. As a result and in the interest of reducing scan time, far-field transformation based only on magnetic field near-field measurements is preferred. In the first paper, a novel method is proposed to predict the far-field radiation using only the magnetic near-field component on a Huygens's box. The proposed method was verified with two simulated examples and one measurement case. The effect of inaccuracy of magnetic field and the incompleteness of the Huygens's box on far-field results is investigated in this paper. The proposed method can be applied for arbitrary shapes of closed Huygens's surfaces. Only the tangential magnetic field needs to be measured. And it also shows good accuracy and robustness in use. Measuring only the magnetic field cuts the scan time in half.

The second topic of this dissertation is modeling delay variations in CMOS digital logic circuits due to electrical disturbances in the power supply. Electronic designers go to considerable effort to minimize the susceptibility of electronic systems against electromagnetic interference. For many systems, the component which fails is an

integrated circuit (IC). Susceptibilities are typically found through testing, which is expensive, time consuming, and does not always uncover problems that are encountered in the field. While IC-level testing helps to establish the operational limits of an IC, testing rarely ensures the IC can withstand all interferences, even within the specified limits. Even when a problem is found, the engineer often does not know why a problem was caused or the best way to prevent the problem in the future. Solving problems through trial and error cannot be done as it is at the system level, because of the prohibitive cost of manufacturing and testing multiple versions of the IC. The IC engineer must build the IC to be robust on the first design cycle. IC failures may be caused by a “hard” failure of the IC, for example, due to latch-up or permanent damage to an I/O pin, or may be caused by a “soft” failure, where incorrect data is read from I/O, internal logic, and/or memory. Soft errors that occur within the logic and/or memory components of the IC can be particularly difficult to deal with since errors associated with these components are much more diverse and complex than those associated with I/O. One common reason for soft errors is that a change in the power supply voltage causes a change in the propagation delay through internal logic or the clock tree, so that the clock edge arrives at a register before valid data and an incorrect logic value is stored at the register. While methods are available to predict the level of voltage fluctuation within the IC from an external electromagnetic event, predicting when a failure will occur as a result of the event is challenging. Methods are developed in the second paper and third paper to help predict these soft failures, by predicting the change in the propagation delay through logic during an electromagnetic disturbance of the power supply.

In the second paper, an analytical delay model was developed to predict propagation delay variations in logic circuits when the power supply is disturbed by an electromagnetic event. Simulated and measured results demonstrate the accuracy of the approach. Four different types of logic circuits were tested, verifying that the proposed delay model can be applied to a wide range of logic circuits and process technologies.

Analytical formulas were developed to predict the clock period variation in integrate circuit when the power supply is disturbed by an electromagnetic event in the third paper. The proposed formulas can be seen as a clock jitter model. The clock jitter due to the power supply variation can be estimated by the proposed propagation delay

model. It is more meaningful, however, to estimate the clock period variation rather than the delay variation for one clock edge, because it is clock period which affects if a soft error will happen or not. Simulated results using Cadence Virtuoso demonstrate the validity and accuracy of the proposed approach. Three different types of noise were used to disturb the power supply voltage, verifying that the proposed model can be applied to a wide range of disturbance of power supply. Many electromagnetic events cause soft errors in ICs by momentarily disturbing the power supply voltage. The proposed model can be helpful for predicting and understanding the soft errors caused by these timing changes within the logic.

PAPER 1**FAR-FIELD PREDICTION USING ONLY MAGNETIC NEAR-FIELD
SCANNING FOR EMI TEST****Xu Gao, Jun Fan, *Senior Member, IEEE*, Yaojiang Zhang,****David Pommerenke, *Senior Member, IEEE*****Electrical Engineering****Missouri University of Science and Technology, Missouri, U. S. A. 65401****Email: xg2z7@mst.edu, davidjp@mst.edu****ABSTRACT**

Far-field prediction for EMI testing was achieved using only magnetic near-field on a Huygens surface. The electrical field on the Huygens surface was calculated from the magnetic near-field using the finite element method (FEM). Two examples were used to verify the proposed method. The first example used the field radiated by an infinitesimal electric dipole. The calculated results were compared with the analytical solution. In the second example, the calculated results were compared with full-wave simulation results for the radiation of a print circuit board (PCB). The validity of this method when the near-field is high-impedance field was verified as well. Sensitivity of the far-field to noise in both magnitude and phase in the near-field data was also investigated. The results indicate that the proposed method is very robust to the random variation of both. The effect of using only four sides of the Huygens box was investigated as well, revealing that, in some instances, the incomplete Huygens's box can be used to predict the far-field well. The proposed method was validated using near-field

measurement data taken from a sleeve dipole antenna. The error for the maximum far field value was in only 1.3 dB.

Index Terms

Near-field far-field transformation, Equivalence theorem, Magnetic fields, Finite element methods, Electromagnetic interference.

I. INTRODUCTION

Near-field scanning has been used extensively for the far-field estimation of antennas [1]-[5]. Applied to electromagnetic compatibility (EMC) problems, near-field scanning has been used to estimate emissions from both integrated circuits (ICs) and printed circuit boards (PCBs) [6]-[13]. Interest in applying far-field predictions using near-field to EMI/EMC problems has recently grown. To predict the far-field emissions from a PCB in the top half space, the near-field data on a planar surface above PCB usually is sufficient [6]-[8]. However, near-field measurement on only one planar surface may not be enough to predict the far-field radiation of three-dimensional structures. The near-field on an enclosed Huygens's surface may be preferred for near-field scanning when predicting the far-field radiation associated with the EMI problems of some complex structures.

Two principle approaches are typically used for near-field far-field transformation. One method relies on expanding the field by a superposition of modes [14]. The other is based on equivalent electric current sources [1] [7] and/or equivalent magnetic current sources [2]. In [1], only the equivalent electric current is used for the near-field far-field transformation using a horn antenna as an example. The electric current is obtained from the magnetic near-field on the planar surface at outlet of a horn. In this case, the electric near-field is not needed due to two reasons. The first reason is that the equivalence principle [19](also described in Section II.) is applied here. The second one is that the image theory for infinite-large planar perfect magnetic conductor (PMC) boundary is also used. Similar reasoning was applied in [2]. The authors of [7], use a planar surface of equivalent sources above PCB to predict the far-field emission

from the PCB. Image theory allows to use only one class of equivalent sources. However, the usage of only one type of equivalent sources combined with image theory requires a large planar Huygens's surface that covers area beyond the PCB size. The planar Huygens's surface is usually used to calculate far-field in half space above the surface. For more general cases, for example, a Huygens's box enclosing all sources, the simplification resulting from applying image theory cannot be used, because image theory can be only used for either infinite-large perfect electric conductor (PEC) plane or infinite-large PMC plane. Thus, both equivalent electric current obtained from the tangential magnetic field and equivalent magnetic current obtained from the tangential electric field are needed to perform far-field transformation from near-field data [19].

Designing electric field probes for tangential components is more difficult than designing magnetic field probes. As a result and in the interest of reducing scan time, far-field transformation based only on magnetic field near-field measurements is preferred. Since electric near-field is required to calculate the far field, methods to extract electric field from magnetic field were proposed in [15][16] based on the principle of plan wave spectrum. However, the method discussed in [15] and [16] is constrained to planar near-field scanning and cannot be used on an arbitrarily shaped Huygens's surface. In [4], a good method is proposed to reconstruct equivalent currents on arbitrary three dimensional Huygens's surface based on the integral equation algorithms and the Conjugated Gradient (CG) method.

This paper proposes a novel method to extract the electric field from the tangential magnetic field on an arbitrary shaped Huygens's surface. It does not rely on image theory. For EMC applications the near field is used to predict the maximum far-

field. The robustness of the method against input data errors is investigated and shown using measured data.

Several practical issues need to be considered for near-field scanning to be successful. Due to obstruction by structures that hold the DUT, and a limited ability to robotically place the probe at any location in the desired tangential orientation it is difficult to obtain near-field data on all sides of a 6-sided Huygens box. The effect of incompleteness of Huygens's surface is investigated in this paper. These results indicate that the maximum of the far-field, radiated to the side of the Huygens's box can still be retrieved if the bottom and the top surfaces are missing. The effect of measurement inaccuracy on the far-field is also investigated.

This paper is organized into seven sections. The theoretical basis and procedure of the proposed method are described in Section II and Section III, respectively. Two examples are used in Section IV to verify the proposed method. In Section V, both the effect of inaccuracy of magnetic near-field and the effect of using incomplete Huygens's box on the far-field result are investigated. In Section VI, the proposed method is validated using real near-field scanning data for a sleeve dipole. Final, discussions and conclusions are reported in Section VII.

II. BRIEF REVIEW OF THEORY

The equivalence theorem (Huygens's principle) is well known and widely used in the electromagnetic area [19]. Fig. 1 depicts the equivalence theorem. The actual radiating sources (J_1 and M_1) are enclosed inside surface S , as shown in Fig. 1 (a). If the electromagnetic field outside the enclosed surface S is the only field of interest, one can substitute the sources with equivalent electric and magnetic currents placed on the surface of S , as shown in Fig. 1 (b). Love's equivalence principle is used to move from the situation in Fig.1 (a) to the situation in Fig. 1 (b). The fields within the surface S are set to zeros, and the equivalent sources become:

$$\overline{J}_s = \hat{n} \times \overline{H}_2 \Big|_S \quad (1)$$

$$\overline{M}_s = -\hat{n} \times \overline{E}_2 \Big|_S \quad (2)$$

Based on the equivalent problem shown in Fig. 1 (b), the fields \overline{E}_2 and \overline{H}_2 outside the surface S can be determined by using (3-6).

$$\overline{A} = \frac{\mu}{4\pi} \iint_S \overline{J}_s \frac{e^{-j\beta R}}{R} ds' \quad (3)$$

$$\overline{F} = \frac{\varepsilon}{4\pi} \iint_S \overline{M}_s \frac{e^{-j\beta R}}{R} ds' \quad (4)$$

$$\overline{E} = -j\omega\overline{A} - j\frac{1}{\omega\mu\varepsilon} \nabla(\nabla \cdot \overline{A}) - \frac{1}{\varepsilon} \nabla \times \overline{F} \quad (5)$$

$$\overline{H} = \frac{1}{\mu} \nabla \times \overline{A} - j\omega\overline{F} - j\frac{1}{\omega\mu\varepsilon} \nabla(\nabla \cdot \overline{F}) \quad (6)$$

where $R = |\overline{r} - \overline{r}'|$, \overline{r} is the observation point, and \overline{r}' is the source point.

In the equivalent problem given in Fig. 1 (b), both the tangential magnetic field and the electric fields on the surface S are used to establish the equivalent source. However, based on the electromagnetic uniqueness theorem, the tangential components of only magnetic or electric field on surface S is needed to determine the field outside surface S . This allows considering the problem as show in Fig. 1 (c). Because both the E and the H field are zero within the surface S , fields cannot be disturbed if the properties of the medium within S are changed.

A further simplification can be obtained by filling the volume V_1 with perfect magnetic material (PMC). The PMC boundary prohibits the radiation from the equivalent magnetic current source [19]. The equivalent magnetic current is considered to be zero. In this case, only the tangential magnetic field is used to determine all equivalent sources. The equivalent problem translates to the radiation of electric current sources on a PMC boundary. The advantage of this equivalence is that only the tangential magnetic field on the surface S is needed, but the difficulty of it is that (3-6) cannot be used anymore, because the current sources do not radiate into unbounded medium.

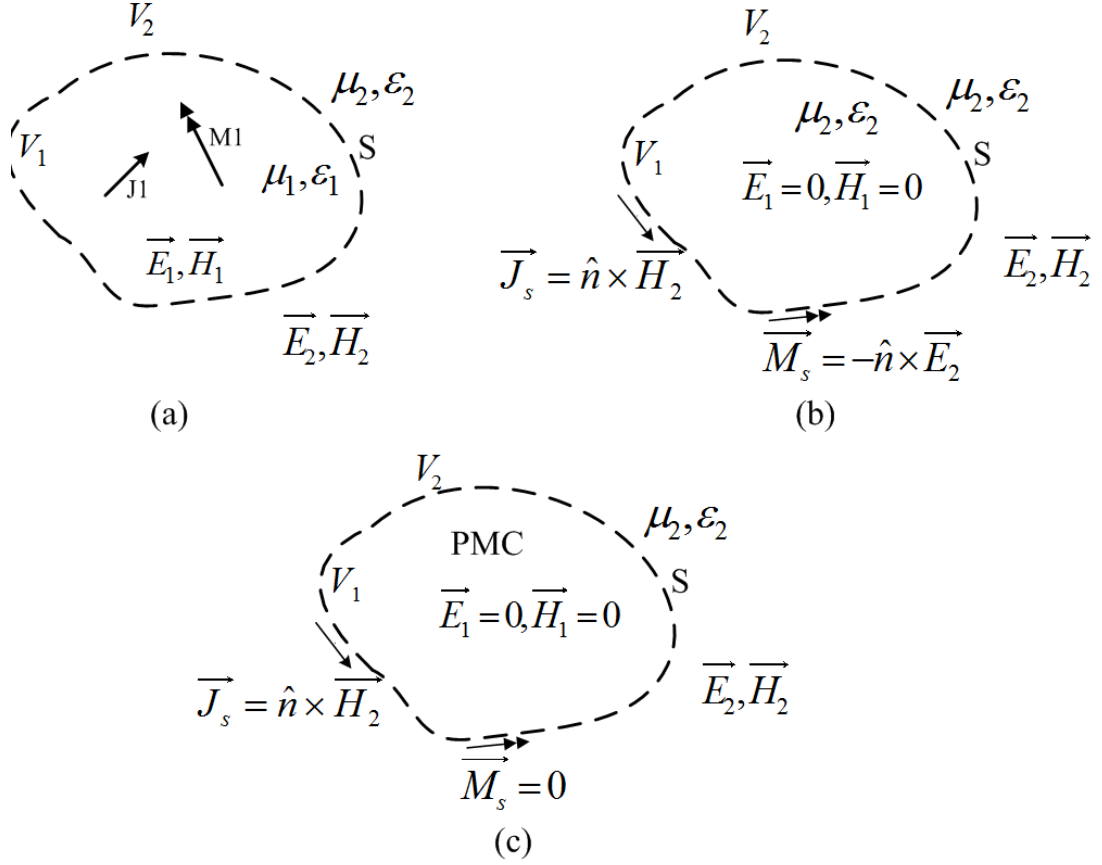


Fig. 1. Equivalence principle models. (a) Original problem. (b) Love's equivalent problem. (c) Equivalent problem when PMC is filled.

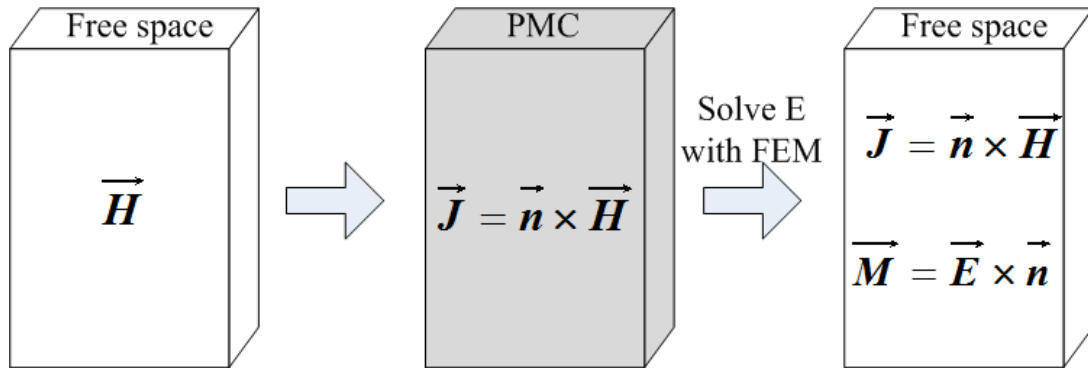
In the EMC testing, the equivalence principle could be used to predict the far-field radiation from near-field scanning. However, to perform the near-field-far-field transformation using the equivalence in Fig. 1 (b), the tangential components of both electric and magnetic fields on the complete Huygens's surface are needed theoretically. As previously mentioned, fabricating an electric field probe for the tangential field is relatively difficult. Consequently, a method that uses only magnetic fields would be helpful.

In real near-field scanning, several types of geometries are used as an enclosed Huygens's surface (i.e., sphere and box). The rectangle Huygens's box is used in this

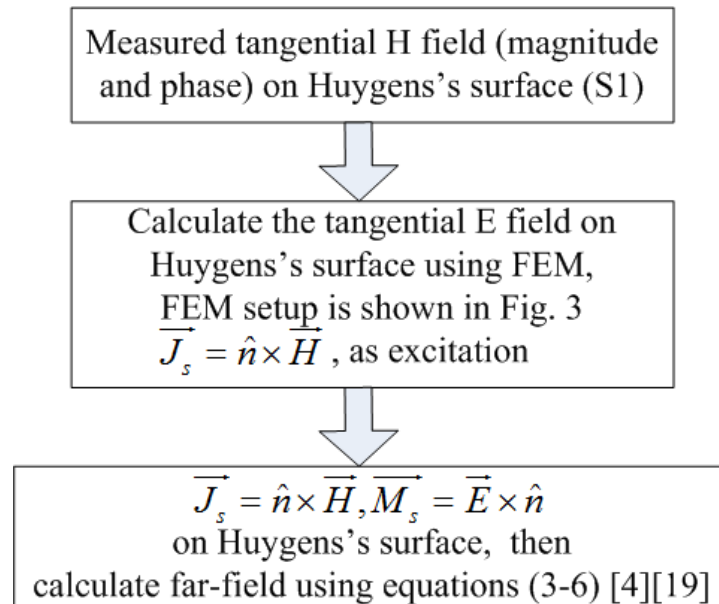
paper. However, the proposed method is not only suitable for the rectangle Huygens's box, but also for other geometries.

III. DESCRIPTION OF THE PROPOSED METHOD

Fig. 2 illustrates the main steps of the method. The method starts with having only the tangential magnetic field in phase and magnitude for six sides as input data. As the method used for the phase measurement is not relevant to the post processing, different phase measurement techniques can be applied [7],[17],[18]-[22]. The middle box shows the method to retrieve the missing tangential magnetic field. The tangential magnetic field, converted into equivalent electric currents, is applied as excitation on a PMC box. This is solved by finite element method (FEM) [20]. The FEM calculation determines the missing tangential electric field. After the tangential electric field is obtained Huygens's principle (Fig. 1(b)) is used to determine the far field using equations (3-6) which have been implemented based on [4] and [19]. Fig. 2(b) gives a flow diagram of the proposed method. The setup of FEM implementation is shown in Fig. 3.



(a)



(b)

Fig. 2. Procedure of the proposed method. (a) The left box shows the original problem. The middle box shows the equivalent problem. FEM was used to solve the equivalent problem to obtain the tangential electric on the surface of the Huygens's box. The right box shows the equivalence to calculate the far- field. (b) The flow diagram of the proposed method.

The equivalent electric current sources were determined using (1). The PMC boundary condition was then assigned to the surface of the Huygens's box (the surface

S1 in Fig. 3). A larger radiation box was implemented outside the Huygens's box to terminate the FEM domain. Here, the absorbing boundary conditions were implemented on the inside surface (S2) of the radiation box. The volume between surfaces S1 and S2 was the calculation region. This region needed to be meshed. The wave equation in (7) was solved using FEM to obtain the tangential electric field on the surface S1.

$$\nabla \times \left(\frac{1}{\mu_r} \nabla \times \bar{E} \right) - k_0^2 \epsilon_r \bar{E} = -jk_0 Z_0 \bar{J} \quad (7)$$

where k_0 is the free-space wave number and Z_0 is the wave impedance in free space.

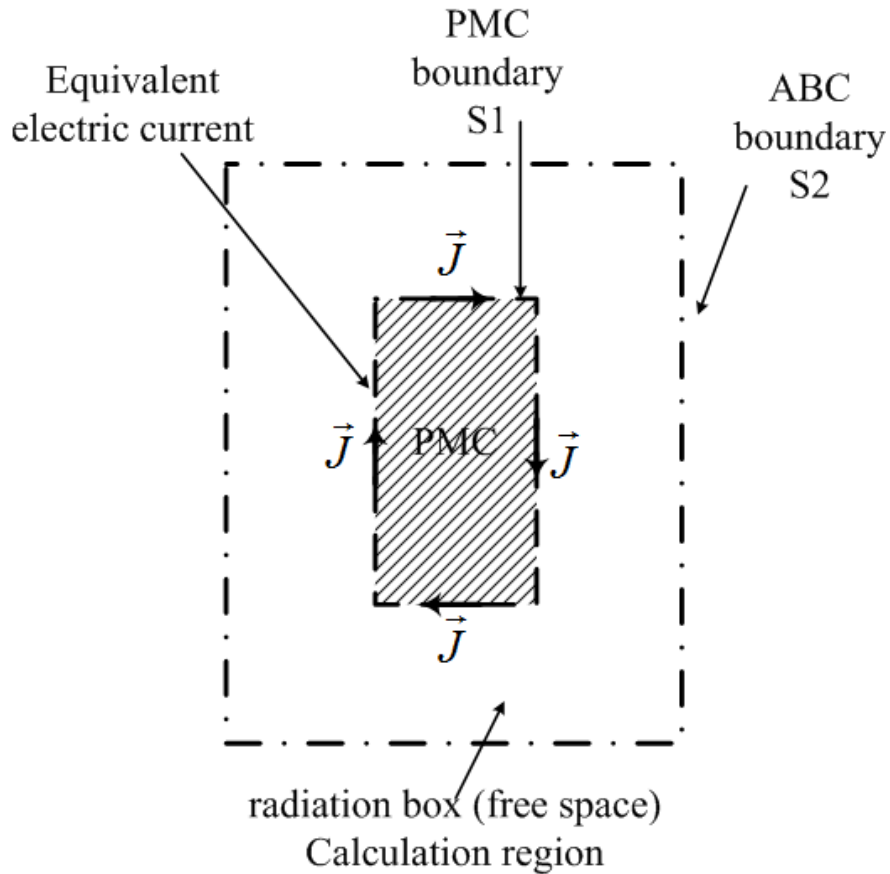


Fig. 3. FEM implementation for determining the electric field on the Huygens's box.

IV. VERIFICATION OF THE PROPOSED METHOD

A. Example Using An Infinitesimal Dipole

For simplicity, the first example used to test the proposed method was an infinitesimal electric dipole along the z-direction, as shown in Fig. 4. This dipole was placed at the center of the Huygens's box. The magnetic field on the surface of the Huygens's box was obtained from the analytical solution of the fields for a dipole. The electric field was then calculated using the proposed method. The calculated electric field was compared with the analytical solution. Finally, the far field was determined using (1-6). These results were compared to the analytical solution for the far-field of an infinitesimal dipole. Since there are six faces in the Huygens's box, for clarity, in the following text, face z1 and face z2 denotes the two faces perpendicular to z-axis, and the z-coordinates of face z2 is larger than that of face z1. For example, in Fig. 4, face z1 is the bottom face of the Huygens's box. Face z2 is the top face. The similar meaning for face x1 and face x2, face y1 and face y2 was used in the following text.

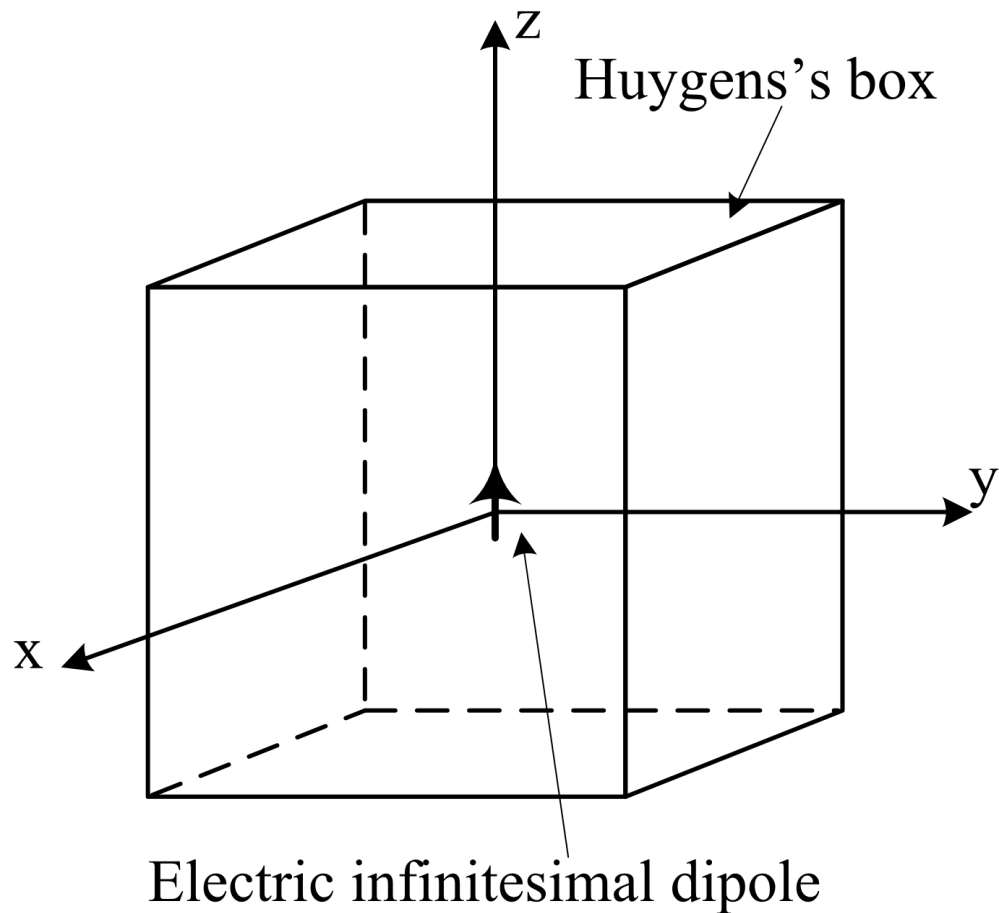


Fig. 4. A test example using an infinitesimal electric dipole

The dimension of the Huygens's box shown in Fig. 4 was $100 \times 100 \times 100$ mm; 500 MHz was selected as the test frequency. The equivalent electric currents on the surface of the Huygens's surface were obtained analytically. These currents were used as sources to calculate the electric field on the surface of the Huygens's box. A FEM solver implemented in Matlab was used to calculate the electric field. The calculated tangential electric fields on face x2 are given in Fig. 5. These fields were compared with the analytical solution. The comparison of electric fields on other faces reveals a similar behavior. Both the calculated results agree well with the analytical results. Although

some numerical noise was present in the calculated results, these noises had little effect on the accuracy of the far field calculation.

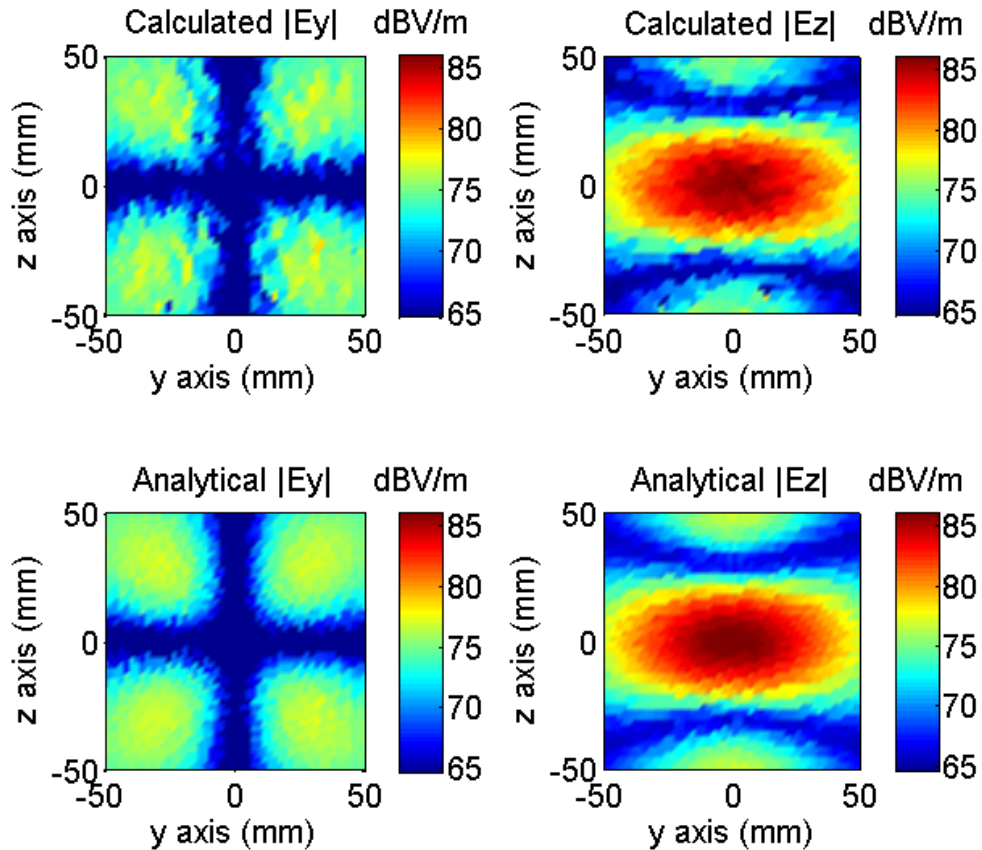


Fig. 5. Comparison of calculated and analytical electric field on the surface of Huygens's box: face x2.

Fig.6 shows the far-field calculation result on the XZ plane. This far-field was calculated using (1-6) with the calculated electric field. This result was compared to the analytical results. The Root Mean Square (RMS) error was less than 0.01, providing evidence that the proposed method was correctly implemented. Next, the same method was applied to a PCB, mounted on a metallic box, without symmetry.

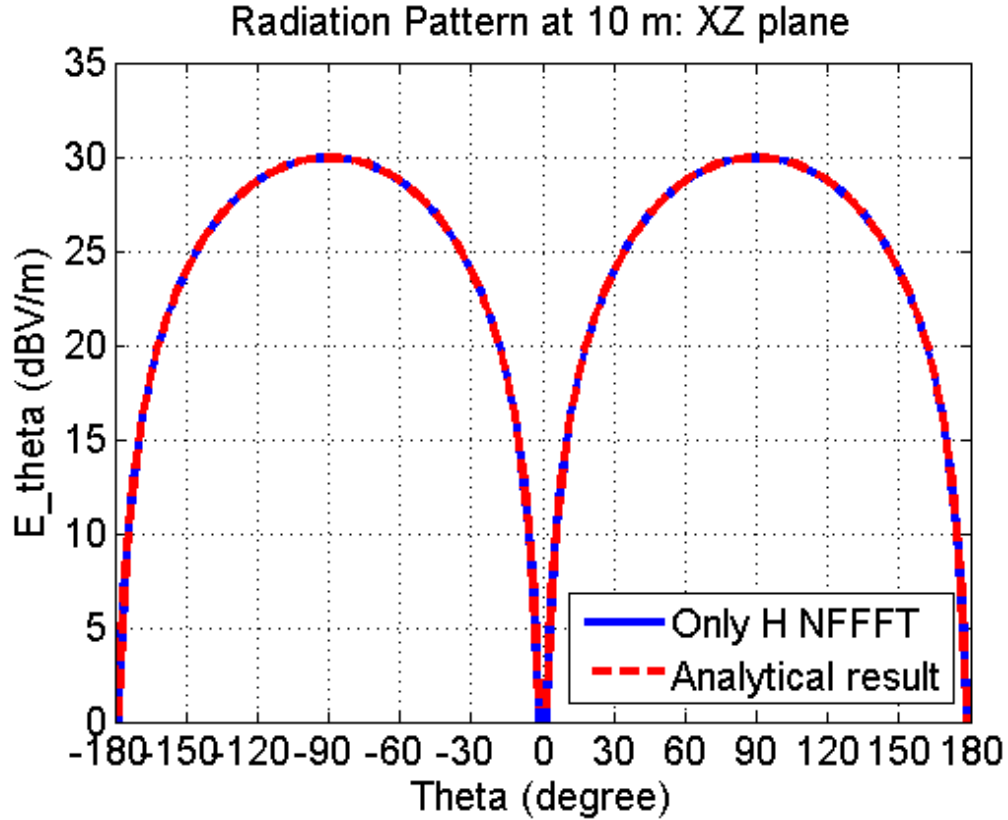


Fig. 6. Comparison of calculated electric field radiation pattern with analytical result on the XZ cutting-plane.

B. Example of A PCB Board on A Metal Box

The geometry, shown in Fig. 7, consisted of a 50 Ω load terminated trace with a patch added to it. The Huygens's box has a distance of 2 cm to the box. The dimensions of the Huygens's box were 80 \times 50 \times 130 mm. 500 MHz was again selected as the test frequency. A references solution was obtained using EMC-Studio [21]. The simulated magnetic field on the Huygens's box was exported from EMC-Studio and used as input for the proposed method. For the compactness of the paper, only the final far-field calculation results are presented here. Fig. 8 compares the far-field at 3 m in the XY plane. The calculated results (using the proposed method) closely matched the

simulation results. The RMS errors were 0.02 and 0.01 for theta component and phi component, respectively.

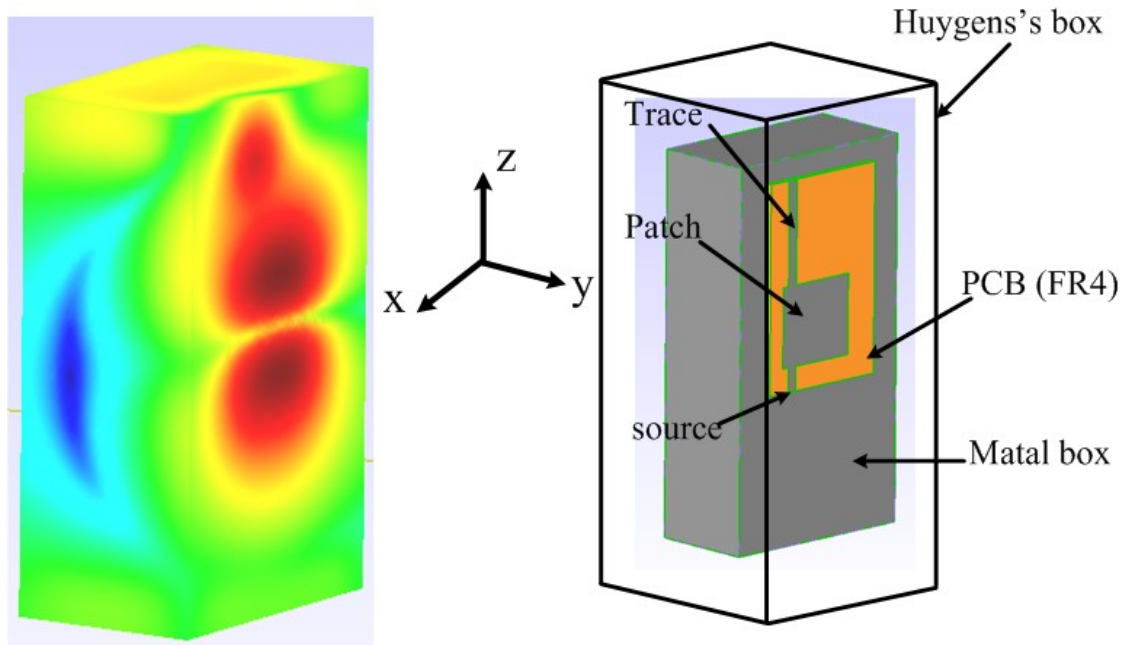


Fig. 7. Simulation model in EMC studio.

The situation in which the electric field dominates in near-field must be investigated, because the proposed method use only magnetic field on Huygens's box. In that situation, the field impedance on Huygens's surface was higher than the wave impedance in air (377Ω). Thus, the same PCB example without termination at the end of the trace was tested at 50 MHz. The field impedance in near-field in this situation was high, due to the open end of trace and the low frequency. Fig. 9 is a histogram of the field impedance at the sampling points on face y2 for two cases. Fig.9 (a) is the case at 500 MHz with termination and Fig. 9 (b) is the case at 50 MHz without termination. These histograms clearly show that, for the case at 50 MHz without termination, the average field impedance on Huygens's box was much higher than 377Ω .

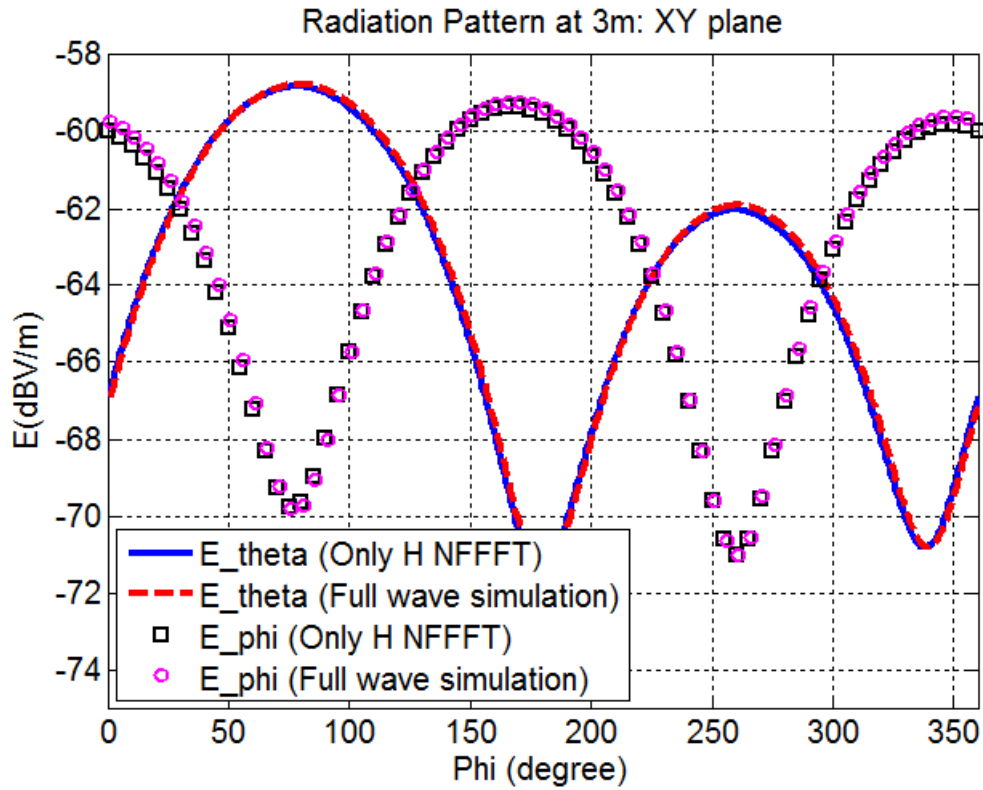


Fig. 8. Comparison of the calculated far-field results of the PCB example using the proposed method with the full wave simulation results at 500 MHz, E_{θ} and E_{ϕ} in XY plane.

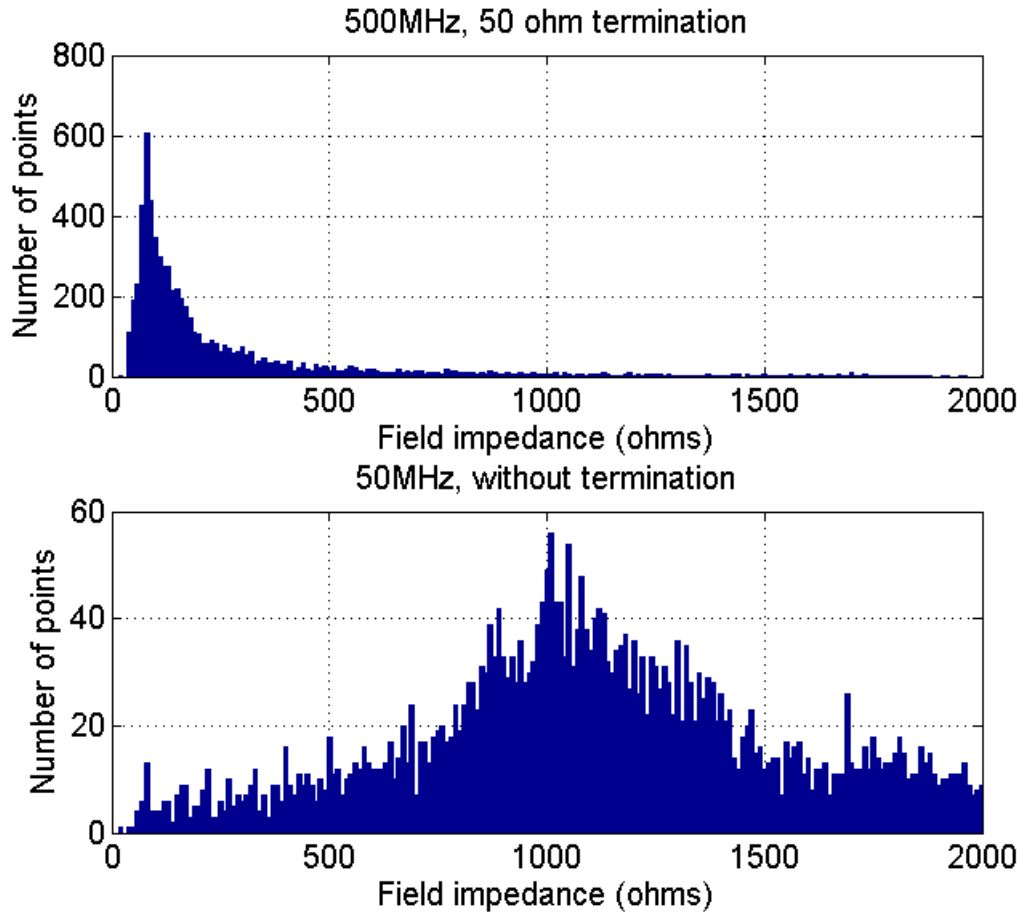


Fig. 9. Histogram for field impedance on face y2. (a) 500 MHz with termination. (b) 50 MHz without termination.

Fig. 10 shows the far-field calculation for the second case. Again, the proposed method worked very well, indicating that it can be used for the case with high field impedance in near-field.

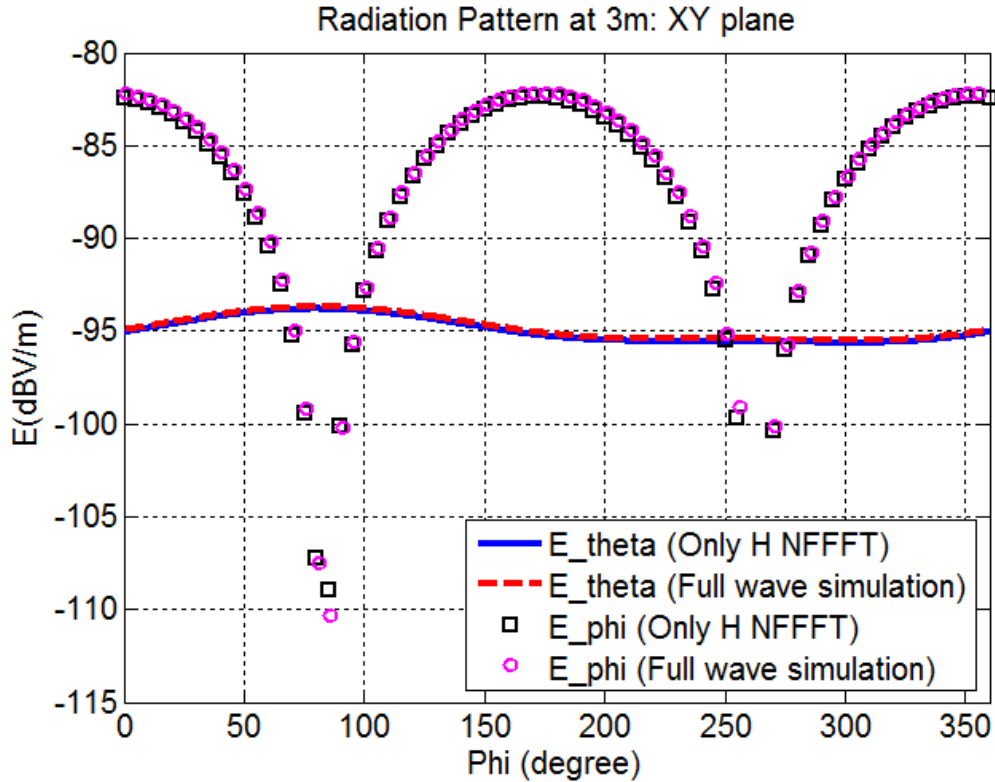


Fig. 10. Calculation results of far-field at 50 MHz for the case without termination, E_{θ} and E_{ϕ} in XY plane.

V. INVESTIGATION ON ISSUES IN PRACTICAL SCANNING

Near-field scanning results are affected by thermal noise, positioning errors, the coupling of insufficiently suppressed field components, phase measurement errors and amplitude measurement errors. In this section, inaccuracies were introduced to the magnetic field to investigate the propagation of noise from the initial magnetic field to the far field result. The same PCB board example at 500 MHz was used in this section.

A. *Magnitude Error in Scanning Magnetic Field*

The randomly distributed magnitude error was added to the simulated magnetic field on the Huygens's box to investigate the noise effect on the proposed method. The amplitude of the noise was ± 5 dB. This value means the magnetic field strength varied

by multiplying factors. These factors were randomly distributed between 0.6 and 1.8. Fig. 11 illustrates the equivalent electric current. This current was obtained from the magnetic field using (1), both with and without the magnitude noise on face y2. The magnitude error was added for all faces of the Huygens's box. Here, only the z component of the equivalent electric current on face y2 is shown. The other faces show similar behavior.

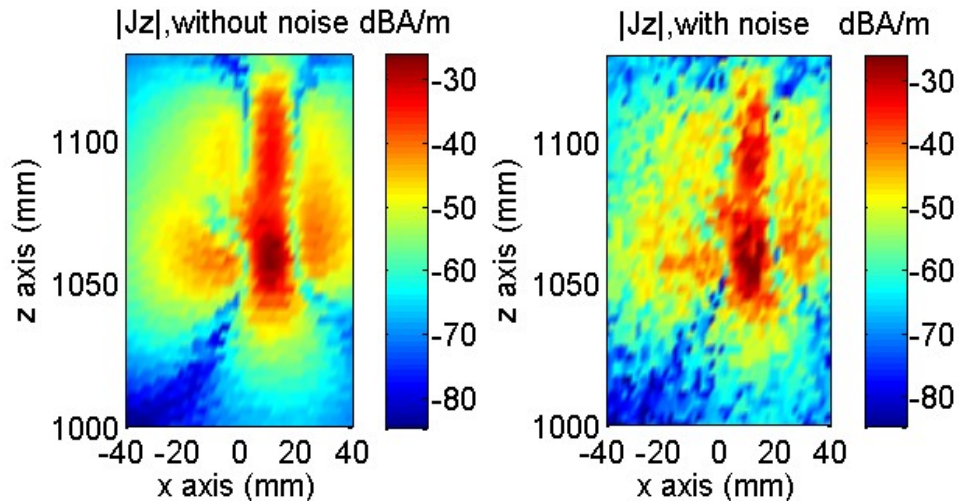


Fig. 11. The equivalent electric currents, both with and without magnitude noise, on face y2. The amplitude of noise is +/- 5 dB and randomly distributed.

The resulting far-field is illustrated in Fig. 12. Although the noise has some effects on the calculated results, these results still agree with the simulation results using the full wave simulation tool. EMI testing is primarily focused on the maximal field. Here, the differences between the calculated maximal E-field and the maximal E-field of full wave simulation are 1.2 dB and 0.1 dB for vertical polarization and horizontal polarization, respectively. This suggests that the proposed method is relatively robust to randomly distributed magnitude noise typically present in scanned near-field data.

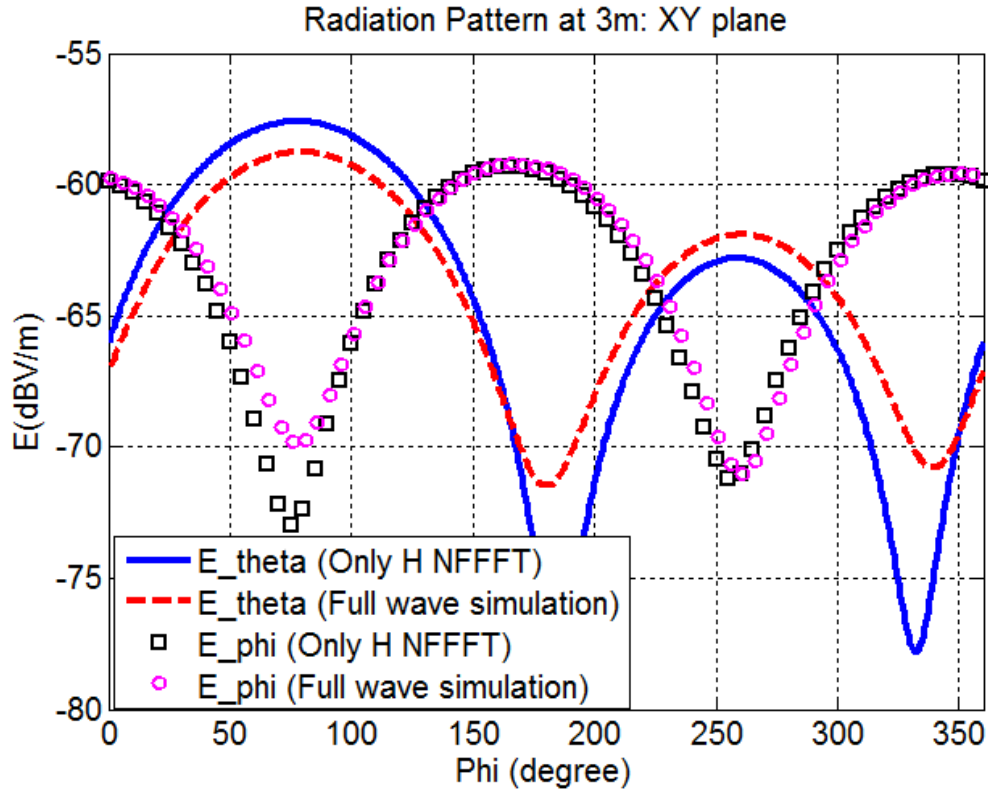


Fig. 12. The effect of magnitude error (± 5 dB) in the scanning H field to the far-field results, E_{θ} and E_{ϕ} in XY plane.

B. Random Variations in The Phase of Scanning Magnetic Field

A random phase deviation of ± 30 degree was introduced to investigate the effect of random deviations of the phase from the real phase value, as shown in Fig. 13. Again, only the phase of equivalent electric current on face y2 is presented. For other faces, the effect of the random phase noise on the equivalent current was similar.

The far-field results (illustrated in Fig. 14) indicate that the random phase variations of the magnetic field did not greatly affect the final far-field calculation results. For the maximum electric field, the differences between the calculated results and full wave simulation result are 0.9 dB and 0.2 dB for vertical polarization and horizontal

polarization, respectively. This suggests that the proposed method is also relatively robust to randomly distributed phase deviations typically present in scanned near-field data.

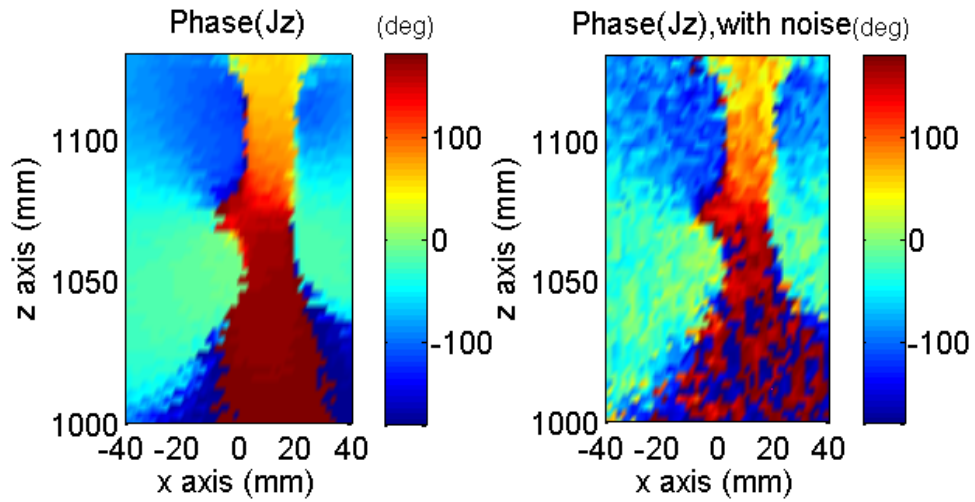


Fig. 13. The equivalent electric currents, both with and without phase variation, on face y_2 . The amplitude of noise was ± 30 degree and randomly distributed.

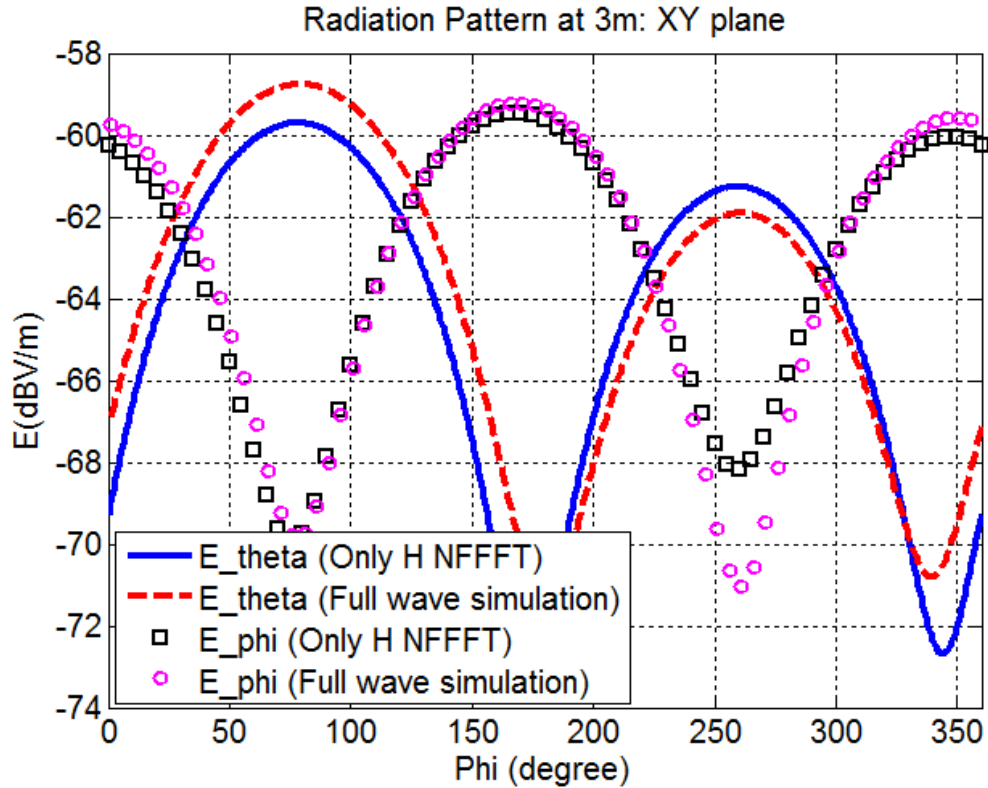


Fig. 14. The effect of phase variation (± 30 degree) in the scanning H field on the far-field results using the proposed method, E_{θ} and E_{ϕ} in XY plane.

C. Calibration Error

Uncertainties in the probe calibration can lead to errors in the near field data. As long as the probe calibration error is not a function of the probe location during scanning, a linear relationship exists between the probe calibration error and the resulting error in the far field. This fact is illustrated in Fig. 15, a 3dB error was observed in the far-field resulted as a result of a 3dB error in the input H-field data. This linear relationship is mainly due to the linear property of FEM method.

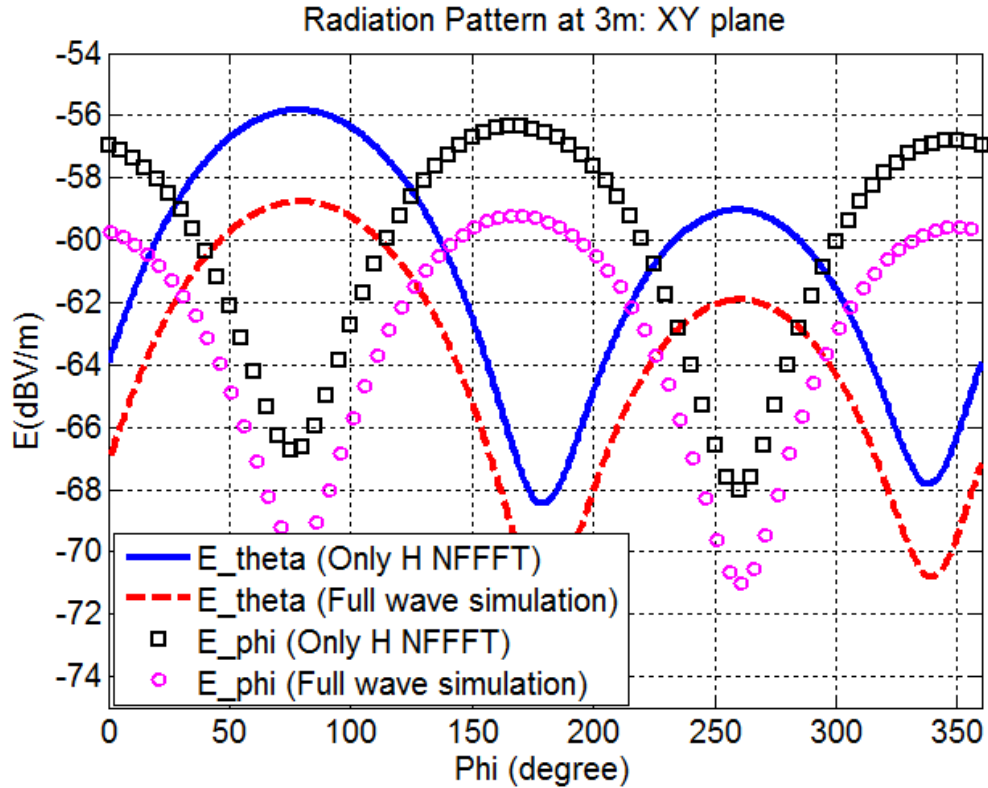


Fig. 15. The effect of 3 dB calibration error in H-field on the far-field results using the proposed method, E_θ and E_ϕ in XY plane.

D. Incomplete Huygens's Box

In real near-field scanning, measuring the magnetic field on all of the faces of the Huygens's box may be difficult. This difficulty may be due to DUT holders and limited reach of the robotic scanner. The effect of incomplete Huygens's boxes on the far-field was investigated therefore. The main radiation of the PCB example board was in the XY plane. The far-field was also analyzed in the XY plane. The magnetic fields on face z1 and face z2 were assumed unknown and set to zero in the proposed method. In this calculation, only magnetic fields on the four side faces (face x1, face x2, face y1 and face y2) were used, which means an incomplete Huygens's box is used. The far-field calculation results using the proposed method are presented in Fig. 16. Although the

incompleteness of the Huygens's box slightly deteriorates the far-field calculation results, the error is small. For the maximum E field, the differences between the calculated results and the full wave simulation results are 0.3 dB and 2.6 dB for vertical polarization and horizontal polarization, respectively. This test result confirms that neither the top surface nor the bottom surface of the Huygens's box contribute significantly to the far-field in XY plane, in which the main radiation direction is included, so they can be set to zeros. Of course, the top and bottom surfaces of the Huygens's box will have an effect on the far field in the top and bottom direction, however, in this PCB example, they are not main radiating directions.

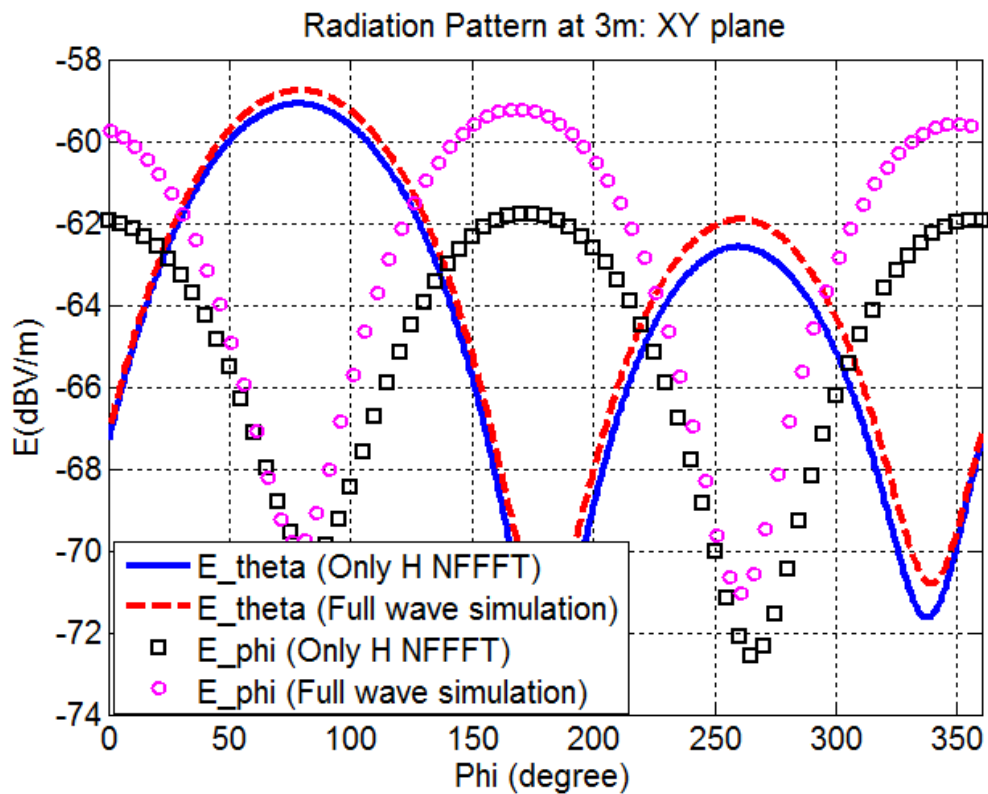


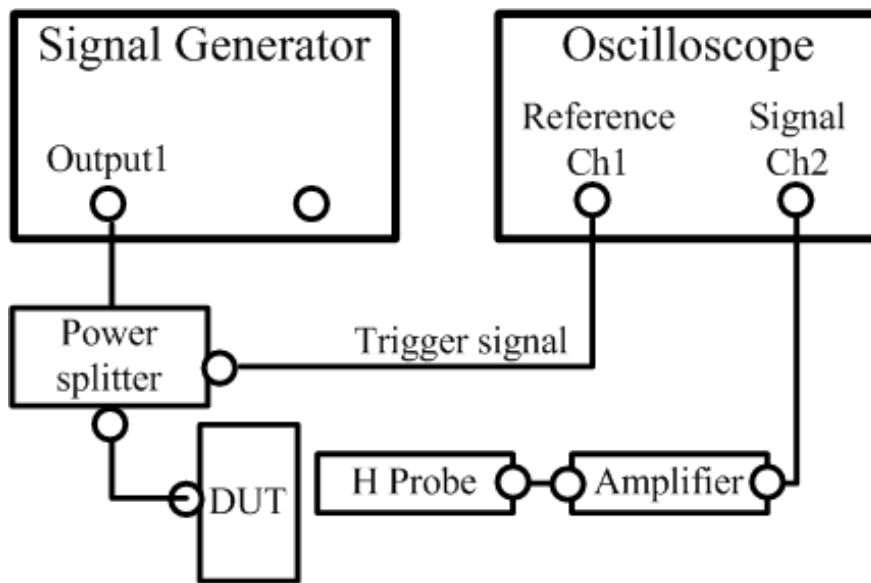
Fig. 16. The effect of incompleteness of Huygens's box on the far-field results using the proposed method, E_{θ} and E_{ϕ} in XY plane.

VI. MEASUREMENT VALIDATION

A 922 MHz sleeve dipole antenna was constructed to test the performance of the proposed method. The magnetic field was measured. Fig. 17(a) shows the measurement setup. An oscilloscope measured both the magnitude and the phase of magnetic fields. The phase information was obtained by comparing the measured signal and the reference signal. The characteristics of the amplifier and cable were calibrated using a network analyzer. A 5-mm H-field probe was used. The calibration method is described in [22]. Due to the rotational symmetry of the antenna, only the magnetic near-field on face x2 was scanned. The magnetic fields on the bottom face were not scanned because of the feeding cable. The fields on the top face were omitted as well. The calculation was based on both one measured side face and the assumption of symmetry. The length of the dipole antenna was 150 mm. The dimension of the scanning area (on face x2) was 80×190 mm, and the scanning face was 20 mm away from the sleeve dipole antenna. Fig. 18 illustrates the measured equivalent electric current on face x2 after conversion from the measured magnetic field. Theoretically, for dipole, the y-component of the equivalent electric current should be zero, however in real measurement it is not zero due to the non-ideal fabrication of dipole and probe coupling. The ratio of the magnitude of J_z to the magnitude of J_y is also shown in Fig. 18 to give feeling of the rejection to J_y in measurement.

The calculated electric field in the X-Z cutting plane is shown in Fig. 19. The calculation result was compared with analytical result for the dipole antenna. The maximal far-field was calculated and compared with the same input power applied during measurement (see Table I). A good agreement was obtained for the maximum electric

field. The difference was only 1.3 dB. The incomplete Huygens's box was used for the sleeve dipole antenna, because in this case the contribution of the equivalent sources on the top and bottom faces to the far-field radiating field are not important compared with that on other faces.



(a)



(b)

Fig. 17. Near-field scanning for a sleeve dipole antenna. (a) Measurement Setup. (b) photograph of probe and DUT.

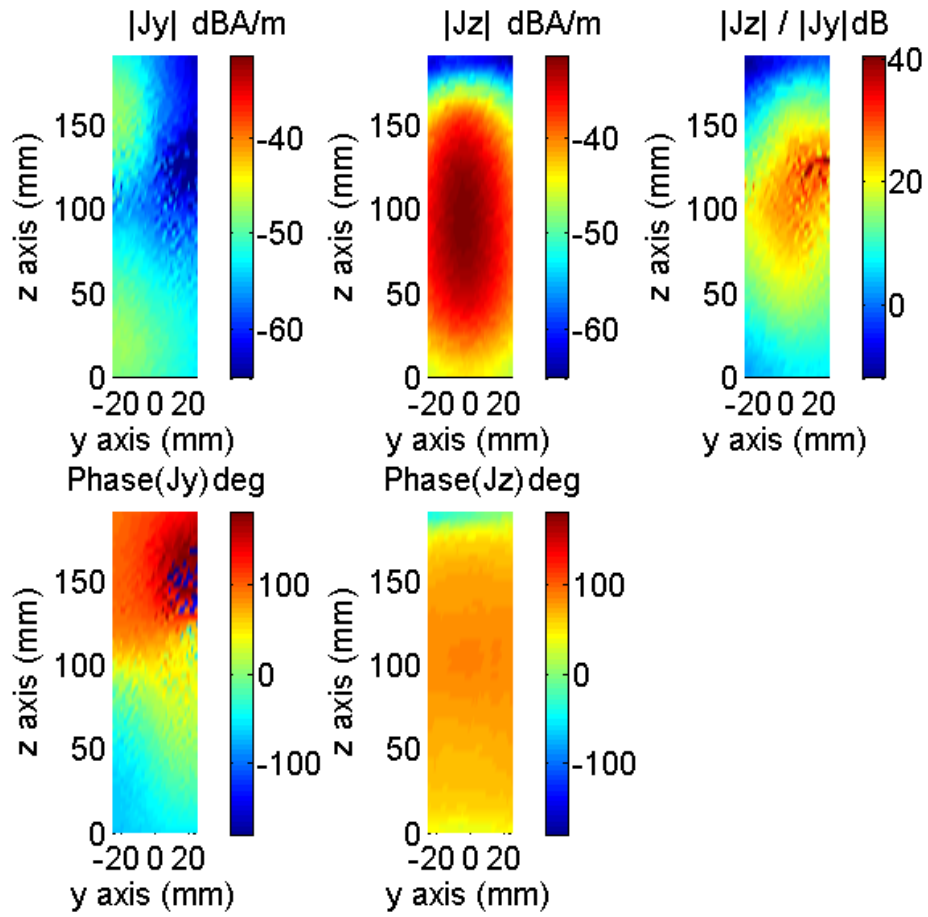


Fig. 18. The measured equivalent electric current of the sleeve dipole on face x2 of the Huygens's box

TABLE I. The Maximum E Field at 10 m

| | Only H NFFFT | Analytical solution |
|---------------------------------------|-----------------|------------------------|
| Maximum E field at 10 m (dBV/m) | -33.2 | -31.9 |

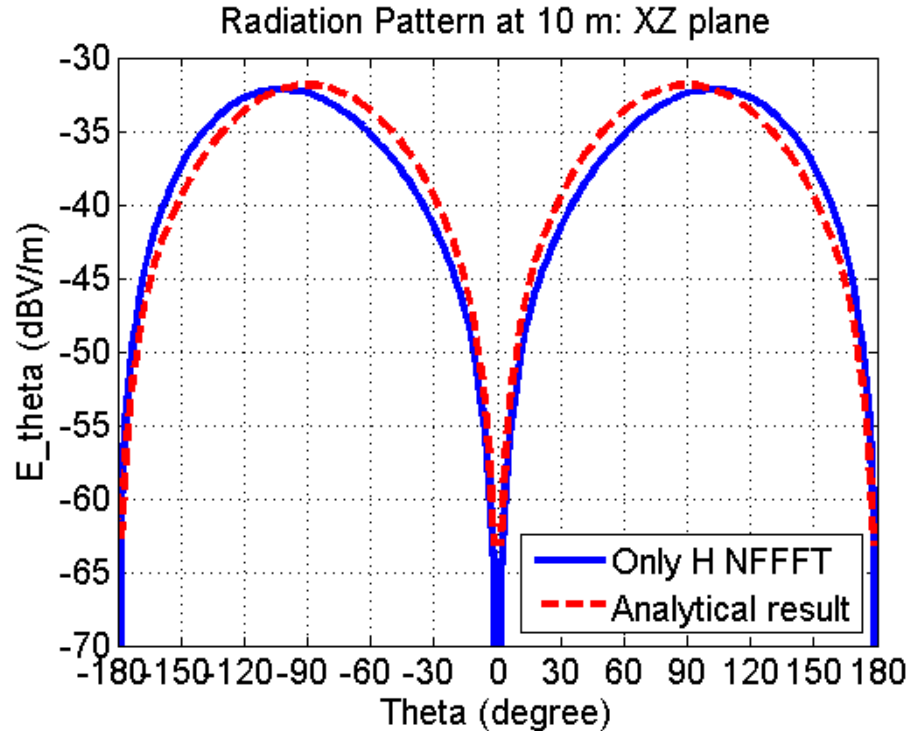


Fig. 19. Calculated electric field radiation pattern of the sleeve dipole using the proposed method. Comparison with analytical result on XZ cutting-plane.

VII. DISCUSSIONS AND CONCLUSIONS

When using a Huygens's box, both the tangential electric and the magnetic field are needed. In this paper, a novel method is proposed to predict the far-field radiation using only the magnetic near-field component on a Huygens's box. The proposed method was verified with two simulated examples and one measurement case. The effect of inaccuracy of magnetic field and the incompleteness of the Huygens's box on far-field results is investigated in this paper. The proposed method can be applied for arbitrary shapes of closed Huygens's surfaces. Only the tangential magnetic field needs to be measured. And it also shows good accuracy and robustness in use. Measuring only the magnetic field cuts the scan time in half. However, there are also several limitations or

disadvantage with this method. At first, the proposed method needs to measure a closed Huygens's surface. In some cases, measuring on a close surface may be difficult. This difficulty may be due to DUT holders and limited reach of the robotic scanner. Therefore as shown in this paper, in some cases, an incomplete Huygens's box can be also used for the proposed method. However, if lots of energy goes through the eliminated side, this method will fail probably. Secondly, the proposed method is a narrow-band method because that FEM is frequency-domain method, while wide-band method is preferred for EMI/EMC application. However, this problem can be mitigated by dividing the wide-band into several smaller bands.

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PAPER 2**MODELING DELAY VARIATIONS IN CMOS DIGITAL LOGIC CIRCUITS
DUE TO ELECTRICAL DISTURBANCES IN THE POWER SUPPLY**

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ABSTRACT

Soft errors can occur in digital integrated circuits (ICs) as a result of an electromagnetic disturbance, such as might result from an electrical fast transient (EFT). Many soft errors come from changes in propagation delays through digital logic which are caused by changes in the on-die power supply voltage. An analytical model was developed to predict timing variations in digital logic as a result of variations in the power supply voltage. The derivation of the analytical delay model is reported. The model was validated experimentally by applying EFTs to a ring oscillator built in a test IC. The predicted and measured ring oscillator frequencies (or periods) agreed within a relative error of less than 2.0%. To further validate the approach, the model was applied to test the response of more complex circuits consisting of NAND/NOR logic gates, binary adders, dynamic logic gates, and transmission gates. The circuits were built using two different process technologies (0.18 and 0.5 micron). The model performed well in each case with a maximum relative error of 3.0%, verifying the applicability of the model

for analyzing complex logic circuits within a variety of process technologies. The proposed delay model can be used by IC design engineers to predict and understand soft errors due to timing changes in ICs caused by disturbance of the power supply.

Index Terms

CMOS integrated circuits, delay effects, electromagnetic interference, electromagnetic transients, modeling, immunity.

I. INTRODUCTION

Electronic designers go to considerable effort to minimize the susceptibility of electronic systems against electromagnetic interference. For many systems, the component which fails is an integrated circuit (IC). Susceptibilities are typically found through testing, which is expensive, time consuming, and does not always uncover problems that are encountered in the field. While IC-level testing helps to establish the operational limits of an IC, testing rarely ensures the IC can withstand all interferences, even within the specified limits. Even when a problem is found, the engineer often does not know why a problem was caused or the best way to prevent the problem in the future. Solving problems through trial and error cannot be done as it is at the system level, because of the prohibitive cost of manufacturing and testing multiple versions of the IC. The IC engineer must build the IC to be robust on the first design cycle.

IC failures may be caused by a “hard” failure of the IC, for example, due to latch-up or permanent damage to an I/O pin [1][2], or may be caused by a “soft” failure, where incorrect data is read from I/O, internal logic, and/or memory. Soft errors that occur within the logic and/or memory components of the IC can be particularly difficult to deal with since errors associated with these components are much more diverse and complex than those associated with I/O. One common reason for soft errors is that a change in the power supply voltage causes a change in the propagation delay through internal logic or the clock tree, so that the clock edge arrives at a register before valid data and an incorrect logic value is stored at the register [6]. While methods are available to predict the level of voltage fluctuation within the IC from an external electromagnetic event [3]-[5], predicting when a failure will occur as a result of the event is challenging. Methods

are developed in the following paper to help predict these soft failures, by predicting the change in the propagation delay through logic during an electromagnetic disturbance of the power supply.

The power supply can be disturbed in a variety of ways. The following paper focuses on disturbances caused by electrical fast transients (EFTs). EFTs are usually caused by switching of inductive loads connected to the power distribution network [4]. An EFT has a rise time of several nanoseconds and a pulse width of tens of nanoseconds [7]. An EFT can directly couple energy to the power supply, or the energy can be coupled to the power supply through I/O protection structures. Although electrical fast transient (EFTs) were used as the source of power supply noise in this paper, the proposed model should be applicable to many other disturbances.

Several models are present in the literature that can be used to estimate delay through logic gates. A delay model for a CMOS inverter was proposed by Sakurai [8], and was extended by Dutta [9]. These models were used to estimate the delay through clock buffers in the presence of simultaneous switching noise in the on-die power supply [10], [11]. Ideally, an immunity model can be applied even to an IC where the engineer does not have detailed information about the internal operation of the IC, such as the circuit structure, FET size and load capacitance. These analytical delay models, however, were developed only for an inverter or buffer and cannot be used directly for a generic IC.

More generic delay models were developed in [12]-[14]. An empirical delay model proposed in [12] shows a good estimation of delay for generic logic circuits. However, this delay model was only validated for a small variation of power supply. The

delay model reported in [13] works for large variation of power supply. The reported accuracy is reasonable but not satisfactory, and not consistent for different logic circuits. A novel and accurate delay model was proposed for generic logic circuit, which can account for the large power supply variations that may occur during an electromagnetic disturbance. The proposed delay model was applied in the immunity test to predict the delay variation when the power supply was disturbed by EFT noise. The accuracy of the model was validated through tests on a variety of typical digital logic circuits. The model performed well in all tests, indicating its potential usefulness for understanding and preventing soft errors in digital ICs.

The paper is presented in five sections. The delay model is derived in Section II. Validation of the delay model is presented in Section III, where modeling results are compared with measurements of a ring oscillator in a test IC. In Section IV, the model is applied to four different types of logic circuits and two different process technologies. Discussion and conclusions are given in Section V.

II. DELAY MODEL FOR GENERIC LOGIC CIRCUITS

The propagation delay through a CMOS inverter, like the one in Fig. 1, is given by [8]:

$$t_{pHL}, t_{pLH} = \left(\frac{1}{2} - \frac{1 - v_T}{1 + \alpha} \right) t_T + \frac{C_L V_{dd}}{2I_{D0}} \quad (1)$$

where $v_T = V_{th} / V_{dd}$, V_{dd} is the power supply voltage, V_{th} is the threshold voltage, α is the velocity saturation index for a MOSFET (typically from 1 to 2), t_T is the rise or fall time of the input signal, I_{D0} is the drain current when $V_{GS} = V_{DS} = V_{dd}$, and C_L is the output

capacitance driven by the gate. The propagation delay is defined as the time between the input signal reaching $V_{dd} / 2$ to the output signal reaching $V_{dd} / 2$. High-to-low propagation delay times, t_{pHL} , are dependent on the parameters for nFETs (i.e. on $V_{th,n}$ and α_n). Low-to-high propagation delay, t_{pLH} , are dependent on pFETs (i.e. on $V_{th,p}$ and α_p). Both the threshold voltage, V_{th} , and the velocity saturation index, α , are technology dependent. The rise or fall time, t_T , is a property of the input signal and is often unknown in the propagation delay calculation. If the input signal is generated inside the IC, however, this parameter can be approximated by assuming the input transition time is similar to the output transition time. Thus, t_T can be expressed as follows [8]:

$$t_T = \frac{C_L V_{dd}}{I_{D0}} \left(\frac{0.9}{0.8} + \frac{V_{D0}}{0.8 V_{dd}} \ln \frac{10 V_{D0}}{e V_{dd}} \right) \quad (2)$$

where V_{D0} is the drain saturation voltage at $V_{GS} = V_{dd}$.

The drain current, I_{D0} , and drain saturation voltage, V_{D0} , are given by [8]:

$$I_{D0} = \left(\frac{V_{dd} - V_{th}}{V_{dd,ref} - V_{th}} \right)^\alpha I_{D0,ref} \quad (3)$$

$$V_{D0} = \left(\frac{V_{dd} - V_{th}}{V_{dd,ref} - V_{th}} \right)^{\alpha/2} V_{D0,ref} \quad (4)$$

where $I_{D0,ref}$ is the drain current when $V_{GS} = V_{DS} = V_{dd,ref}$, and $V_{D0,ref}$ is drain saturation voltage when $V_{GS} = V_{dd,ref}$.

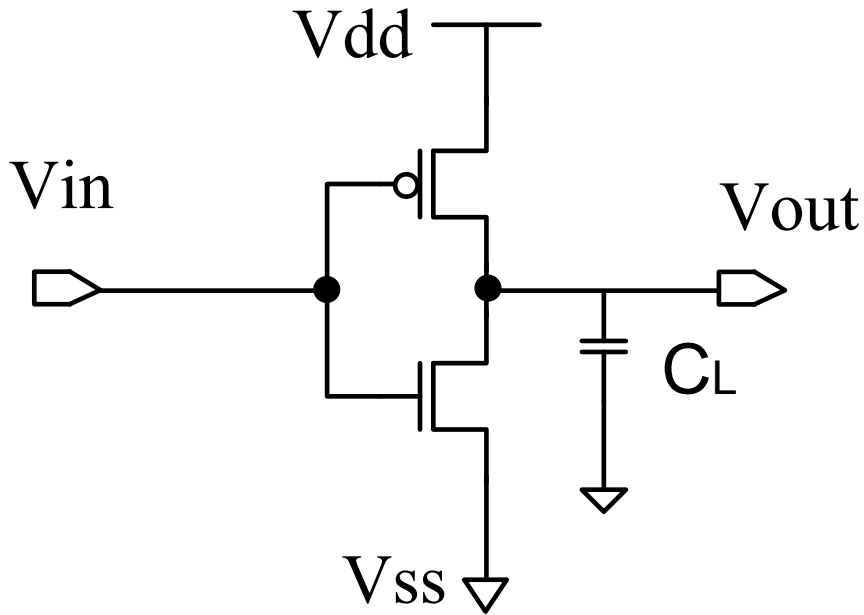


Fig. 1. A MOSFET inverter.

This model for an inverter can be extended to generic logic circuits containing multiple components. Based on (1)-(4), a new delay model that works for generic logic circuits and has higher accuracy than the delay model in [13] is proposed.

Consider the delay through an inverter chain as shown in Fig. 2. The low-to-high delay and high-to-low delays through the i th inverter are given by:

$$t_{pLH,i} = \frac{C_{Li}V_{dd}}{2I_{D0,p,i}} + \left(\frac{1}{2} - \frac{1-v_{T,p}}{1+\alpha_p}\right) \cdot \left(\frac{0.9}{0.8} + \frac{V_{D0,n,i-1}}{0.8V_{dd}} \ln \frac{10V_{D0,n,i-1}}{eV_{dd}}\right) \frac{C_{L(i-1)}V_{dd}}{I_{D0,n,i-1}} \quad (5)$$

$$t_{pHL,i} = \frac{C_{Li}V_{dd}}{2I_{D0,n,i}} + \left(\frac{1}{2} - \frac{1-v_{T,n}}{1+\alpha_n}\right) \cdot \left(\frac{0.9}{0.8} + \frac{V_{D0,p,i-1}}{0.8V_{dd}} \ln \frac{10V_{D0,p,i-1}}{eV_{dd}}\right) \frac{C_{L(i-1)}V_{dd}}{I_{D0,p,i-1}} \quad (6)$$

where the subscript i indicates the inverter number and the subscripts n and p indicate whether the parameters apply to an nFET or pFET, respectively.

Equations (5) and (6) can be simplified by recognizing that portions of the equations are constant with respect to power supply disturbances:

$$\frac{V_{D0,i}}{V_{dd}} = \frac{V_{D0,ref}}{(V_{dd,ref} - V_{th})^{\alpha/2}} \frac{(V_{dd} - V_{th})^{\alpha/2}}{V_{dd}} = D \cdot \frac{(V_{dd} - V_{th})^{\alpha/2}}{V_{dd}} \quad (7)$$

and

$$\frac{C_{Li} V_{dd}}{I_{D0,i}} = \frac{C_{Li} (V_{dd,ref} - V_{th})^{\alpha}}{I_{D0,i,ref}} \frac{V_{dd}}{(V_{dd} - V_{th})^{\alpha}} = A_i \cdot \frac{V_{dd}}{(V_{dd} - V_{th})^{\alpha}} \quad (8)$$

where $D = \frac{V_{D0,ref}}{(V_{dd,ref} - V_{th})^{\alpha/2}}$ and $A_i = \frac{C_{Li} (V_{dd,ref} - V_{th})^{\alpha}}{I_{D0,i,ref}}$. D is a technology dependent

parameter while A_i depends on the size of the MOSFET and the load capacitance driven by the MOSFET.

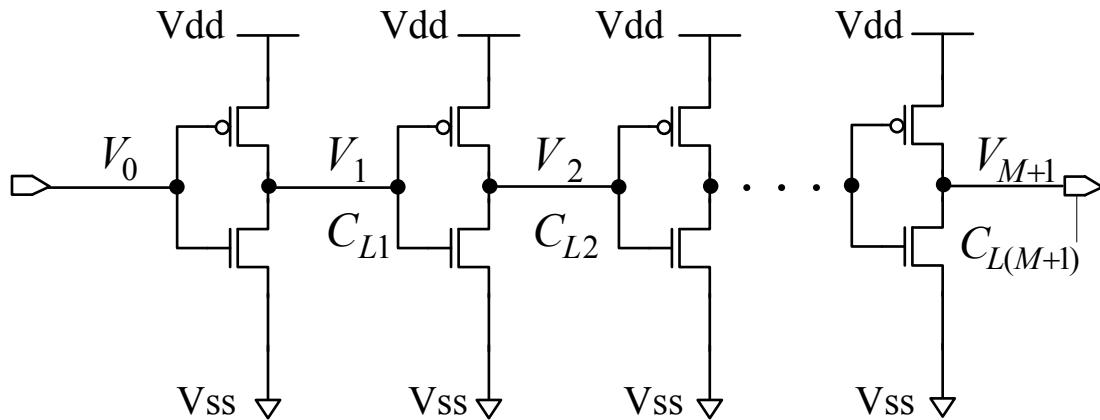


Fig. 2. An inverter chain.

Using the simplifications given in (7) and (8), the delay through the i th inverter is given by:

$$t_{pLH,i} = \frac{A_{i,p}V_{dd}}{2(V_{dd} - V_{th,p})^{\alpha_p}} + f(V_{th,p}, \alpha_p) \cdot g(V_{dd}, V_{th,n}, \alpha_n, D_n) \frac{A_{i-1,n}V_{dd}}{(V_{dd} - V_{th,n})^{\alpha_n}} \quad (9)$$

$$t_{pHL,i} = \frac{A_i^n V_{dd}}{2(V_{dd} - V_{th}^n)^{\alpha_n}} + f(V_{th,n}, \alpha_n) \cdot g(V_{dd}, V_{th,p}, \alpha_p, D_p) \frac{A_{i-1,p}V_{dd}}{(V_{dd} - V_{th,p})^{\alpha_p}} \quad (10)$$

where

$$f(V_{th}, \alpha) = \left(\frac{1}{2} - \frac{1 - v_T}{1 + \alpha} \right) \quad (11)$$

and

$$g(V_{dd}, V_{th}, \alpha, D) = \frac{0.9}{0.8} + \frac{D(V_{dd} - V_{th})^{\alpha/2}}{0.8V_{dd}} \cdot \ln \frac{10D(V_{dd} - V_{th})^{\alpha/2}}{eV_{dd}} \quad (12)$$

The total propagation delay through the inverter chain from V_1 to V_{M+1} , that is

$t_{pLH,tot}$ and $t_{pHL,tot}$ (assuming for brevity that M is an even number), is given by:

$$t_{pLH,tot} = t_{pLH,2} + t_{pHL,3} + t_{pLH,4} + \dots + t_{pLH,M+1} \quad (13)$$

$$t_{pHL,tot} = t_{pHL,2} + t_{pLH,3} + t_{pHL,4} + \dots + t_{pHL,M+1} \quad (14)$$

By substituting (9) and (10) into (13) and (14), and using the approximations

$\alpha = (\alpha_n + \alpha_p) / 2$, $V_{th} = (V_{th,n} + |V_{th,p}|) / 2$ and $D = (D_n + |D_p|) / 2$, a simplified delay model

can be obtained as

$$t_{pLH,tot}, t_{pHL,tot} \approx \frac{V_{dd}}{(V_{dd} - V_{th})^\alpha} \cdot [S1 \cdot f(V_{th}, \alpha) g(V_{dd}, V_{th}, \alpha, D) + S2] \quad (15)$$

where $S1 = \sum_{i=1}^M A_i$ and $S2 = \frac{1}{2} \sum_{i=2}^{M+1} A_i$. $S1$ and $S2$ are constants which depend on the sizes and output capacitances of the MOSFETs in the logic circuit.

Although the delay model in (15) is derived for an inverter chain, it can easily be applied to generic push-pull logic by simply treating $S1$ and $S2$ as constants dependent on the logic circuit. While $S1$ and $S2$ can be determined analytically, they may be difficult to determine for complex circuits. In this case, or when detailed information about the circuit structure is not known, they can be found through experiments or simulations. It should be noted that the values of $S1$ and $S2$ are different when the output is switched from low-to-high than when switched from high-to-low.

Because $S1$ and $S2$ are independent of the power supply voltage, their values can be calculated from the propagation delays, $t_{p,1}$ and $t_{p,2}$, at two different power supply voltages, $V_{dd,1}$ and $V_{dd,2}$. The value of the constants can be found by solving the equation:

$$\begin{bmatrix} N_1 & P_1 \\ N_2 & P_2 \end{bmatrix} \begin{bmatrix} S1 \\ S2 \end{bmatrix} = \begin{bmatrix} t_{p,1} \\ t_{p,2} \end{bmatrix} \quad (16)$$

where

$$N_j = f(V_{th}, \alpha) g(V_{dd,j}, V_{th}, \alpha, D) \frac{V_{dd,j}}{(V_{dd,j} - V_{th})^\alpha} \quad (17)$$

and

$$P_j = \frac{V_{dd,j}}{(V_{dd,j} - V_{th})^\alpha} \quad (18)$$

where $j = 1, 2$. The only required circuit information is the threshold voltage, the velocity saturation index, and the drain saturation voltage, in addition to the delays $t_{p,1}$ and $t_{p,2}$.

III. VALIDATION ON A TEST IC

The delay model in (15) was validated through experiments on a test IC implemented in 0.5 micron technology. While the 0.5 micron technology is relatively old, the equations should apply to both older and newer technologies.

A. Predicting The Frequency (Period) of A Ring Oscillator

A ring oscillator with 11 inverters was implemented in the test IC, as shown in Fig. 3. The frequency of oscillation was measured while applying EFTs to the power supply. Equation (15) can be used to predict changes in the delay through the inverter chain, and thus changes in the oscillation frequency of the ring oscillator. This structure is used generically to demonstrate the ability to predict changes in delay through logic circuits.

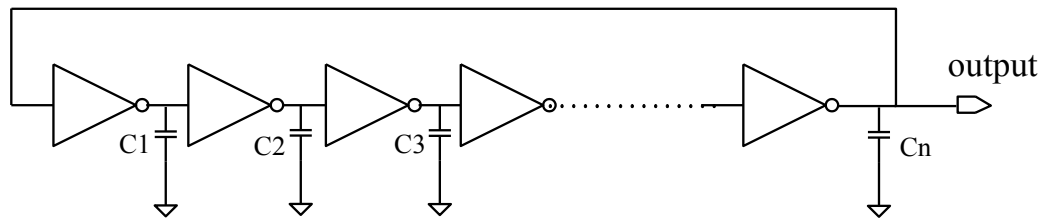


Fig. 3. A ring oscillator.

The period of the output oscillation can be calculated as

$$T = t_{pHL,tot} + t_{pLH,tot} \quad (19)$$

where $t_{pLH,tot}$ and $t_{pHL,tot}$ are the total low-to-high and high-to-low propagation delay through the entire inverter chain. Equation (15) can be used to predict the period of the oscillation of the ring oscillator using the following constants:

$$S1_T = S1_{HL} + S1_{LH} \quad (20)$$

$$S2_T = S2_{HL} + S2_{LH} \quad (21)$$

where $S1_T$ and $S2_T$ are constant in (15) for the period, and Si_{LH} and Si_{HL} ($i = 1, 2$) are constants for $t_{pLH,tot}$ and $t_{pHL,tot}$, respectively. Equations (16) to (18) can also be used to obtain $S1_T$ and $S2_T$ by replacing the delays, $t_{p,1}$ and $t_{p,2}$, with two values of the periods, T_1 and T_2 , that occur at two different power supply voltages, $V_{dd,1}$ and $V_{dd,2}$.

B. Immunity Test Setup

Fig. 4 shows the test setup. An EFT generator was connected to the IC V_{dd} pin through a 40 dB attenuator and a 33 nF capacitor. The 40 dB attenuator was used to avoid physical damage to the IC. A 4.7 nF off-chip decoupling capacitor was mounted near to the V_{dd} pin of the test IC to minimize switching noise from the IC itself. A DC power supply was connected to the V_{dd} pin through a ferrite and inductor to decouple the power supply from the EFT test. The V_{dd} pin and the output of the ring oscillator were monitored using a 1 kohm resistive probe.

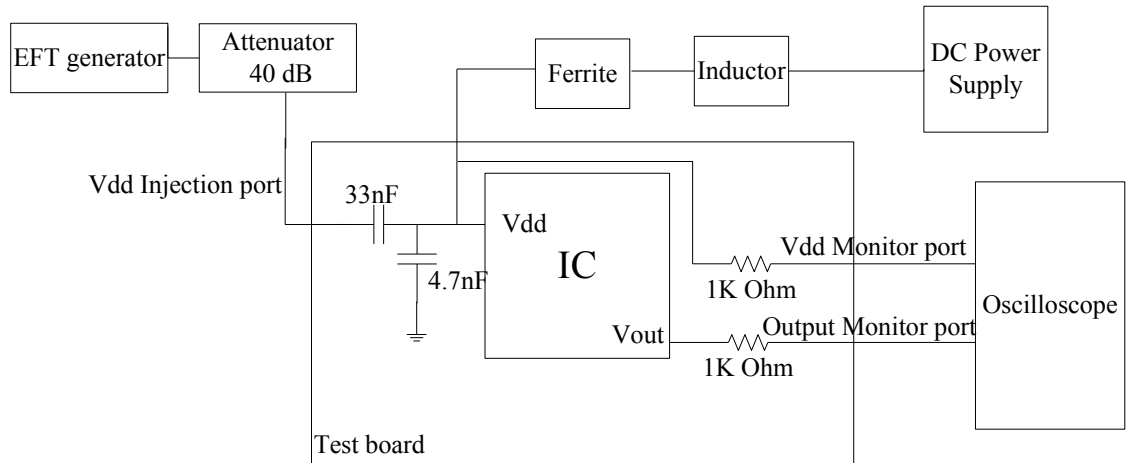


Fig. 4. EFT immunity test setup for the ring oscillator.

Fig. 5 shows one test result when the EFT generator was set to negative 600 V. The top plot shows the voltage waveform at the V_{dd} pin of the IC. The middle plot shows the waveform at the output pin of the ring oscillator. The oscillations in the output waveform are too fast to show at this timescale, so the bottom plot shows the frequency of the output oscillation. The voltage on V_{dd} dropped during the EFT injection. As V_{dd} dropped, the frequency of the oscillation also decreased, which means that the propagation delay in the inverter chain increased. This increasing propagation delay through the logic gates of the IC could cause timing errors.

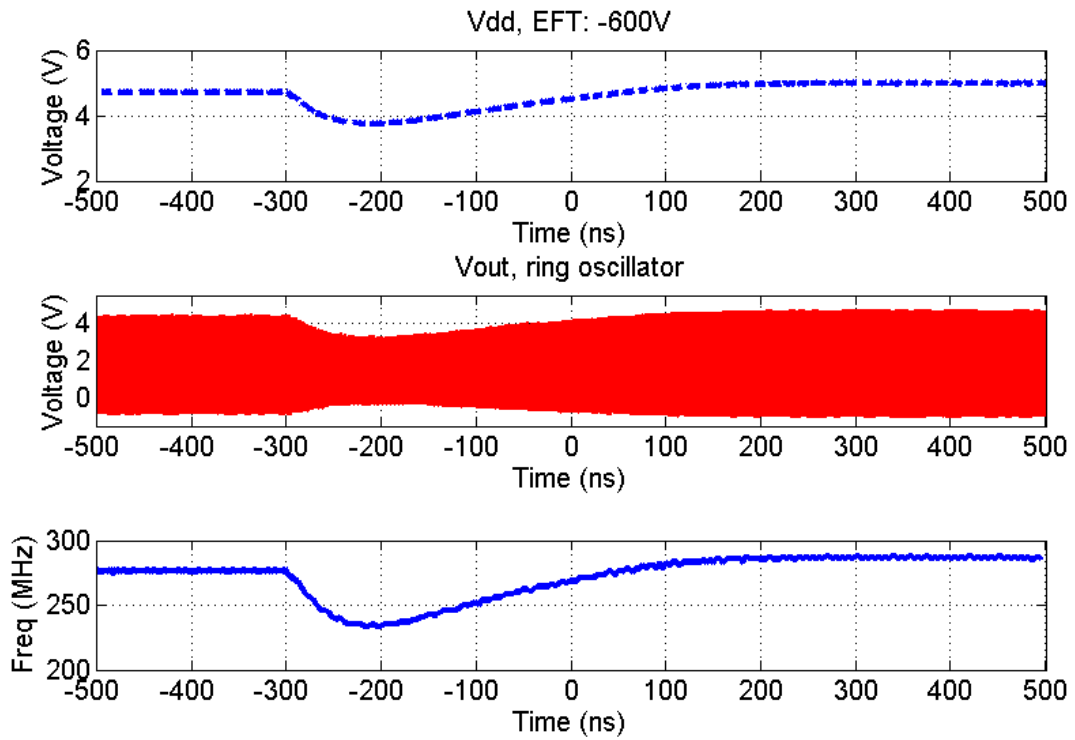


Fig. 5. Test results during a negative 600V EFT.

C. Results

To find values of $S1_T$ and $S2_T$ for the ring oscillator, values of periods T_1 and T_2 were found for two different values of V_{dd} . These values of the period and supply voltage were then used in (16)-(18) to calculate N_i and P_i and $S1_T$ and $S2_T$. Once $S1_T$ and $S2_T$ were determined, they were used to predict delays in the EFT immunity tests.

The measured power supply voltage was used in (15) to predict the period and/or frequency of the ring oscillator during an EFT event. Fig. 6 shows a comparison of the predicted and measured results during a negative 600 V EFT. The predicted and measured frequency matched well, within a maximum relative error of 1.5%.

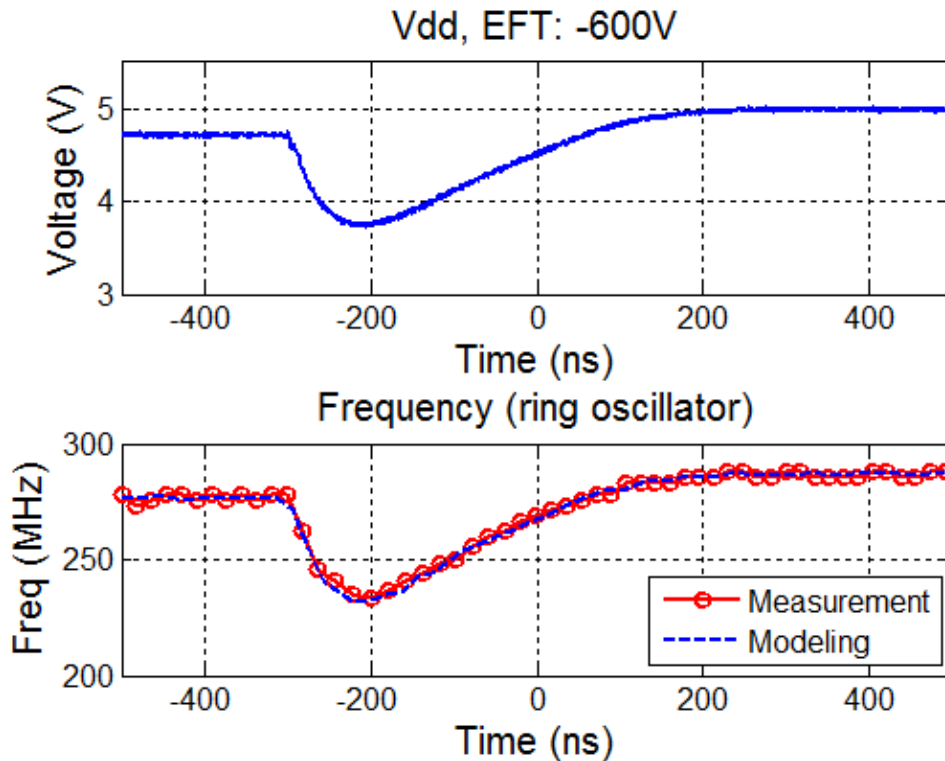


Fig. 6. Waveform on Vdd during a negative 600 V EFT and the corresponding frequency of the ring oscillator.

Additional testing was performed with EFTs of different amplitudes and polarities. Table I shows the maximum relative error of predicted oscillation frequencies compared with measurement results for EFT injections at 400 V, 600 V and 800 V. The testing results in Table I demonstrate that the proposed model can accurately predict the propagation delay through an inverter chain during an EFT immunity test, given the correct voltage on V_{dd} . Later results will be shown using predicted values of the waveform on V_{dd} .

TABLE I. Maximum Relative Error for Ring Oscillator

| Case | EFT Noise | Maximum relative error |
|------|-----------|------------------------|
| 1 | +400 V | 1.2% |
| 2 | +600 V | 1.4% |
| 3 | +800 V | 1.9% |
| 4 | -400 V | 1.2% |
| 5 | -600 V | 1.5% |
| 6 | -800 V | 2.0% |

D. Power Supply Waveform Modeling

In the previous section, the measured waveform on V_{dd} was used to predict the delay through the inverter chain. More generally, however, one would like to predict the V_{dd} waveform without the requirement of a measurement. The circuit model in Fig. 7 was developed to predict the waveform on the V_{dd} bus during an EFT test when the EFT was injected into the V_{dd} pin of the test IC. The circuit includes a model of the EFT generator,

models of lumped components on the PCB and a simple model for the IC. The EFT generator was modeled using a voltage source. The voltage source creates a waveform measured from an actual EFT generator. The lumped components on the PCB include a 47 μH inductor and ferrite used to decouple the DC power supply from the EFT test, and a 4.7 nF on-board decoupling capacitor. The model of the IC includes a simple model of the package and the on-die power delivery network. A non-linear resistor was used to represent the nonlinear relationship between V_{dd} and the switching current consumed by the test IC.

Measured and predicted voltage waveforms of the on-board V_{dd} are shown in Fig. 8 when the EFT generator was set to positive or negative 600 or 800 V. The results demonstrate that the V_{dd} waveform can be accurately predicted using this model. These predicted waveforms for Vdd should yield similarly accurate predictions of delay, as shown in Fig. 6.

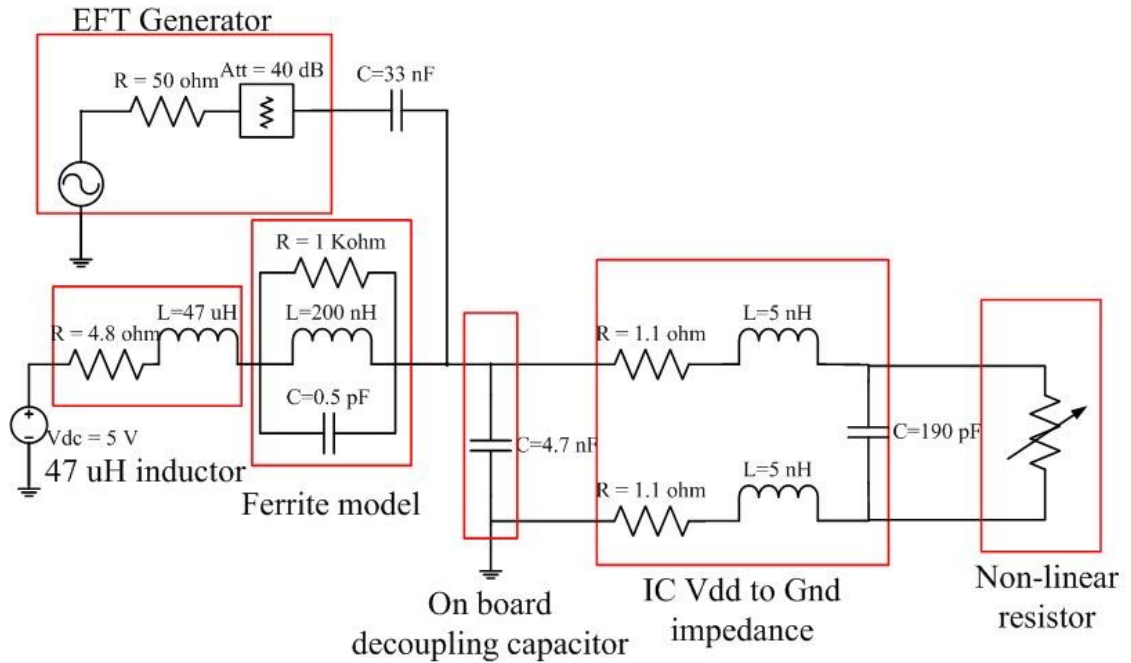


Fig. 7. Circuit model to predict the waveform on the Vdd bus during an EFT test.

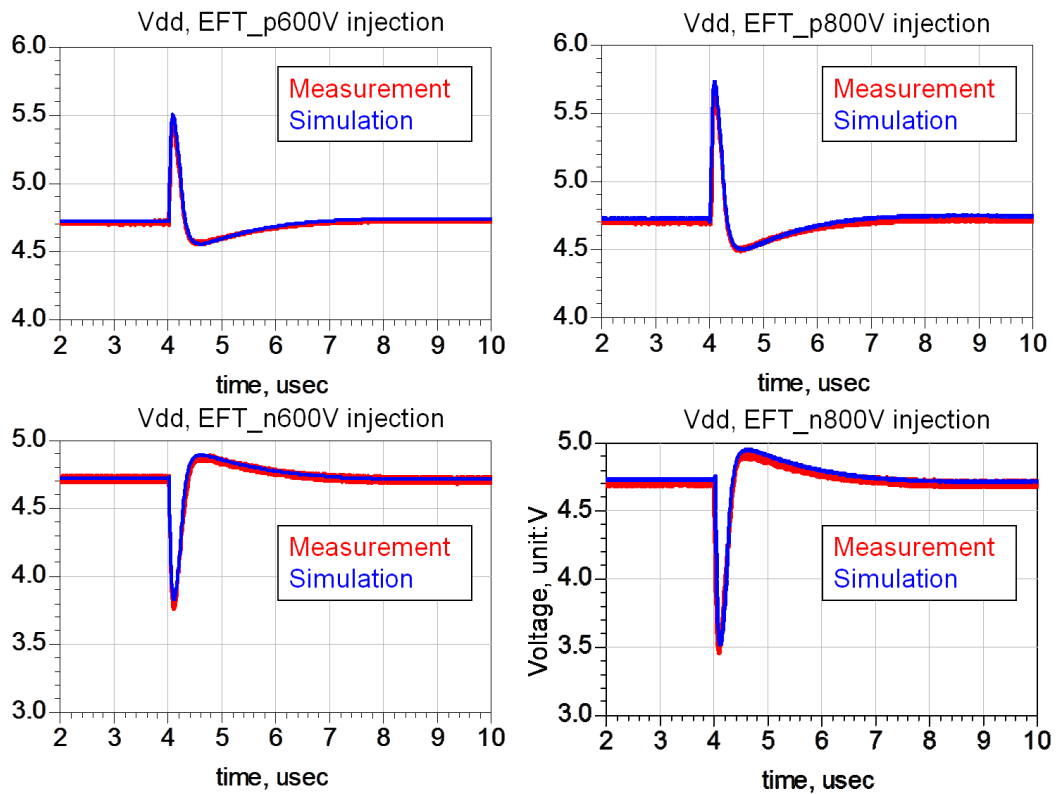


Fig. 8. Predicted and measured Vdd waveform during an EFT.

IV. DELAY PREDICTION FOR GENERIC LOGIC GATES

To verify that the delay model will work well with more complex logic circuits, four different logic circuits were tested through simulation in Cadence Virtuoso, and tests were performed using different process technologies. An EFT pulse was injected into the power pin of the IC by capacitive coupling using the same method as shown in Fig. 4. The propagation delays through the logic circuits were predicted using the proposed delay model according to the predicted power supply voltage waveform on V_{dd} . The delays predicted by (15) were compared with delays predicted through simulation in Cadence. Two different technologies, (0.5 micron and 0.18 micron), were used in the simulations.

A. NAND -NOR Gate Logic Block Using 0.5 Micron Technology

A logic block containing NAND and NOR gates was used to test the performance of the proposed delay model with a “generic” logic circuit. Fig. 9 shows the circuit diagram of the logic block. The NAND gates and NOR gates used conventional CMOS push-pull structures. Gates with different drive strengths were used. For example, a gate with 3 times the driving strength of a minimum sized inverter is marked with an “X3”. The normal power supply voltage was 5 V. A negative 5 V (without the 40 dB attenuator in Fig. 4) EFT pulse was injected on to the power pin of this circuit. The resulting waveform on V_{dd} is shown in Fig. 10. This logic block was set to a propagate mode by setting the “unused” inputs of NAND gates and NOR gates to logic ‘1’ or ‘0’, respectively, so the signal at V_{in} will propagate to V_{out} . The delay from V_{in} to V_{out} was measured.

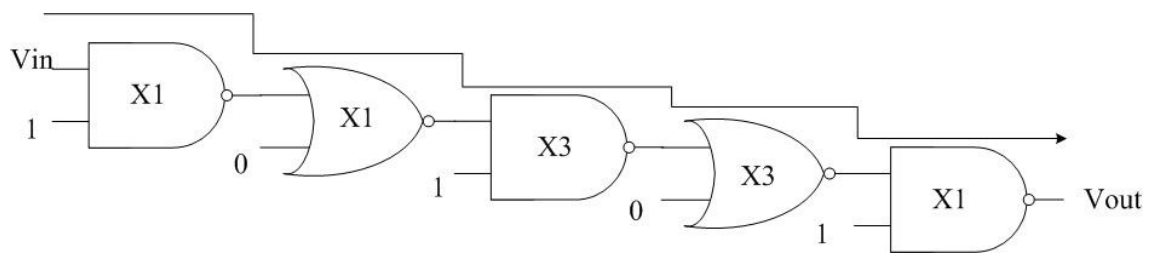


Fig. 9. A logic block with NAND and NOR gates.

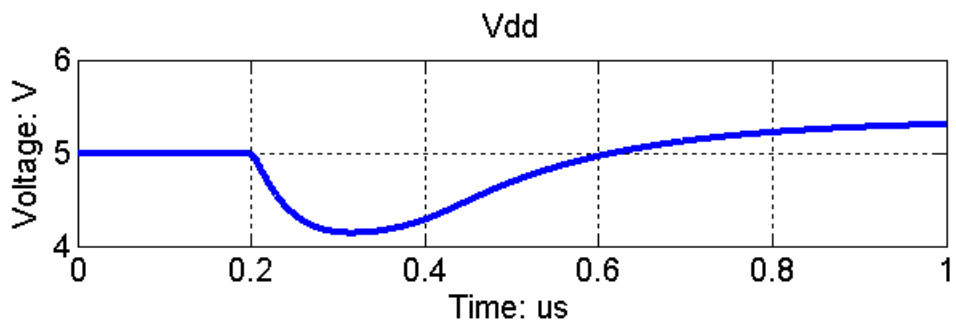


Fig. 10. Waveform on Vdd when a negative 5 V EFT pulse was injected on the Vdd pin of the NAND-NOR circuit.

The predicted and simulated delays are shown in Fig. 11. A good agreement between predicted and simulated delays was achieved. The maximum relative errors were 1.0% and 0.4% for t_{pLH} and t_{pHL} , respectively.

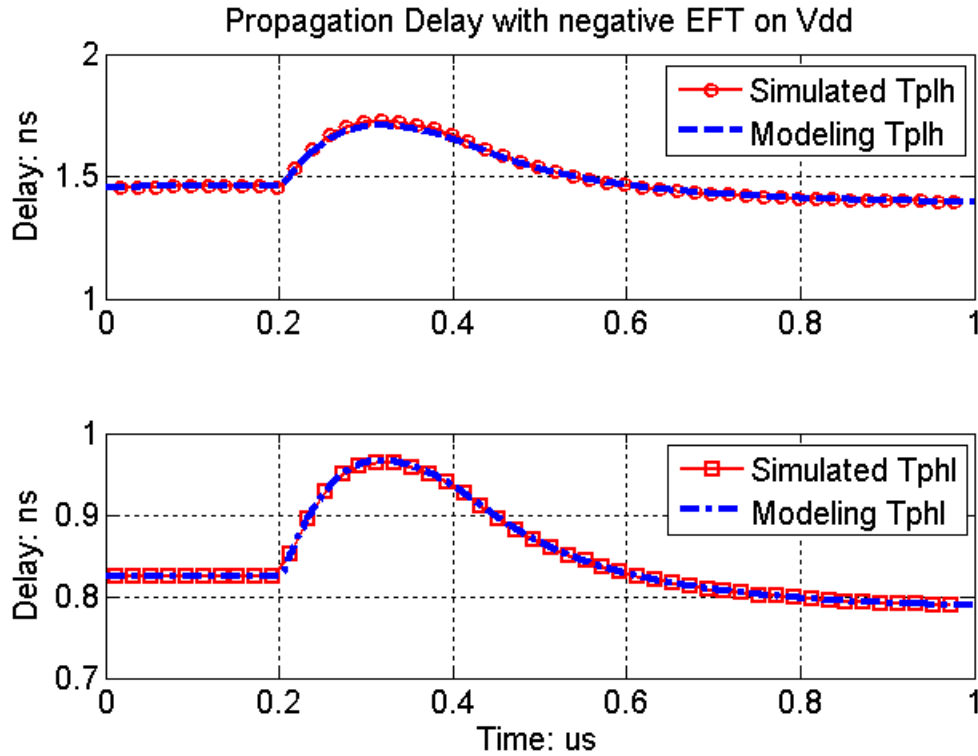


Fig. 11. Simulated and estimated delays through a logic block containing NAND and NOR gates. Top: Tplh; Bottom: Tphl.

B. 4-bit Full Adder Using 0.18 Micron Technology

Tests were performed on a 4-bit full adder implemented using 0.18 micron technology to further test the methodology. The circuit diagram of the 4-bit full adder is shown in Fig. 12. The 4-bit full adder was composed of four 1-bit full adders. Each 1-bit adder had three inputs, A and B , the two digits to be summed, and C_i , the carry input, and had 2 outputs, the sum, S and the carry out, C_o . A conventional logic structure was used for the 1-bit adder as shown in [12].

For a 1-bit full adder, if the two input digits $A \neq B$, then $C_o = C_i$, and in this case, the full adder is said to be in the propagate mode. For the 4-bit full adder, the two 4-bit

digits A and B were set to '1111' and '0000', respectively, so that all 1-bit full adders were in propagate mode. In this case, the carry out $C_{out} = C_{in}$. The propagation delay from C_{in} to C_{out} was tested.

The normal power supply voltage was 3.3 V. A negative 3 V EFT pulse was injected on the V_{dd} pin of the IC in simulation resulting in the waveform on V_{dd} shown in Fig. 13. The predicted and simulated delays are shown in Fig. 14. The maximum relative errors were 0.5% and 0.3% for t_{pLH} and t_{pHL} , respectively.

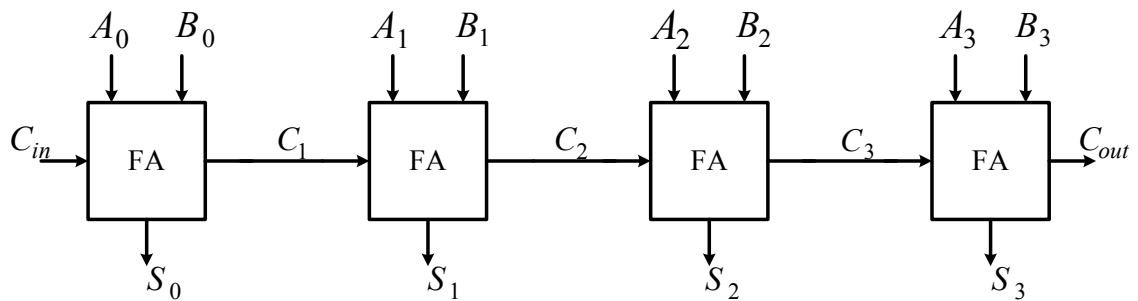


Fig. 12. Circuit diagram of a 4-bit full adder.

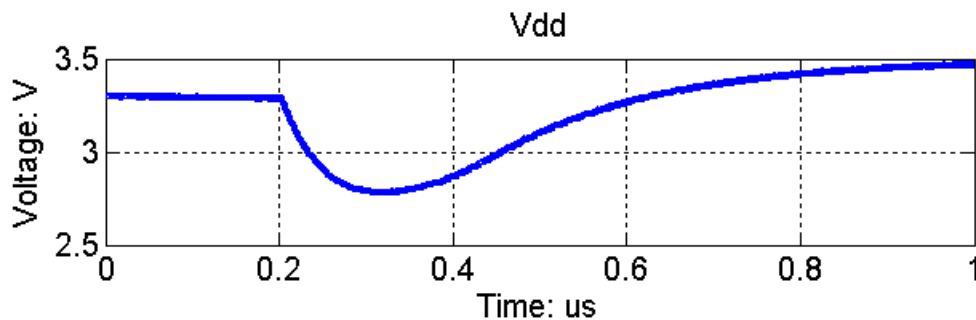


Fig. 13. Waveform on V_{dd} when a negative 3 V EFT pulse was injected on the V_{dd} pin.

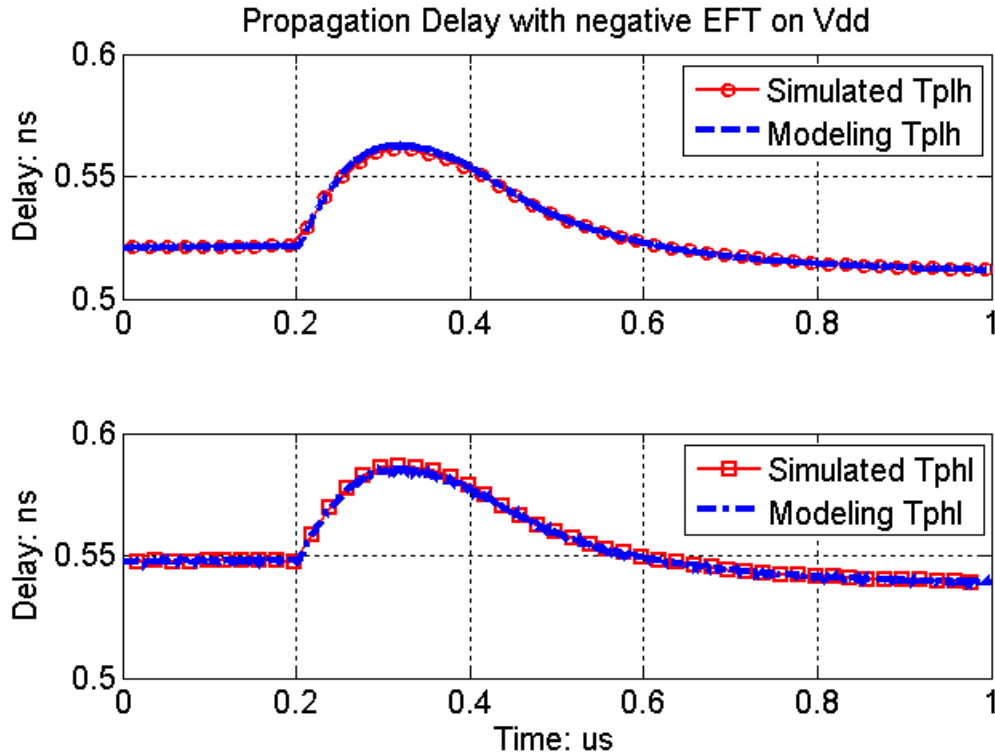


Fig. 14. Simulated and estimated delays through the 4-bit full adder. Top: Tplh; Bottom: Tphl.

C. *Dynamic Logic Circuit Using 0.18 Micron Technology*

The performance of the proposed delay model was also tested on a dynamic logic circuit. The circuit consisted of a chain of dynamic logic buffers, as shown in Fig. 15.

The complete dynamic logic circuit consisted of 10 dynamic logic buffers in series. For this dynamic logic circuit, $V_{out} = V_{in}$ only when clk becomes logic high, and V_{out} remains at a logic low when clk is logic low. Therefore, the propagation delay for the dynamic logic circuit was from clk to V_{out} . Only low to high delay was tested, since the V_{out} high to low transition occurs when the clk signal becomes a logic low, and no signal is propagated through the circuit (i.e. the output is “don’t care”).

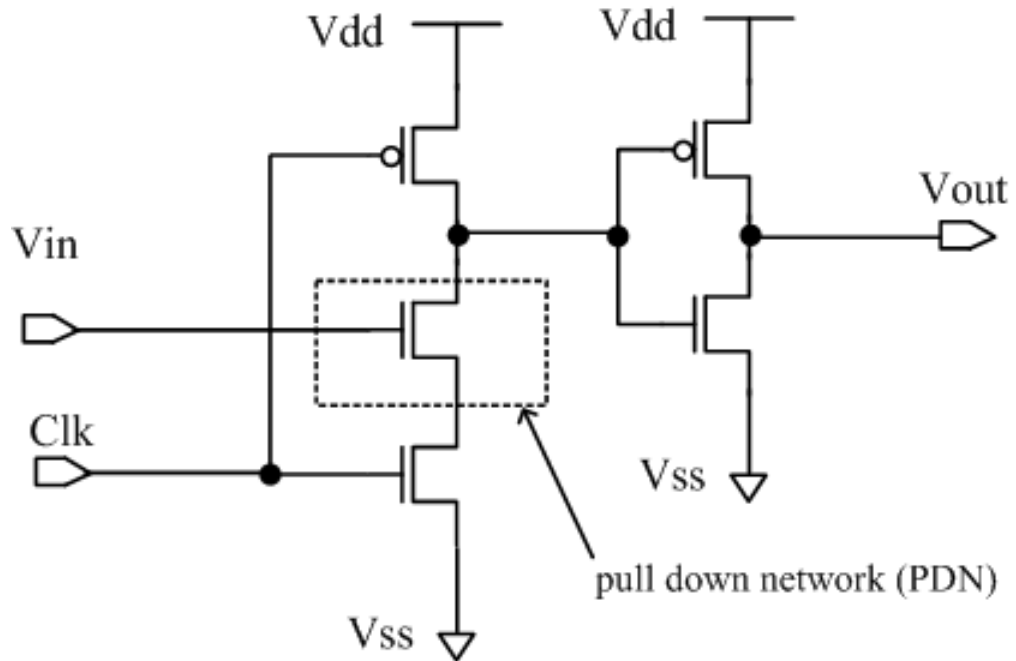


Fig. 15. The dynamic logic buffer.

The normal power supply voltage was 3.3 V. A negative 3 V EFT pulse was injected on the V_{dd} pin of the IC resulting in the waveform on V_{dd} shown in Fig. 13. The predicted and simulated delays are shown in Fig.16. The maximum relative error was 0.5%.

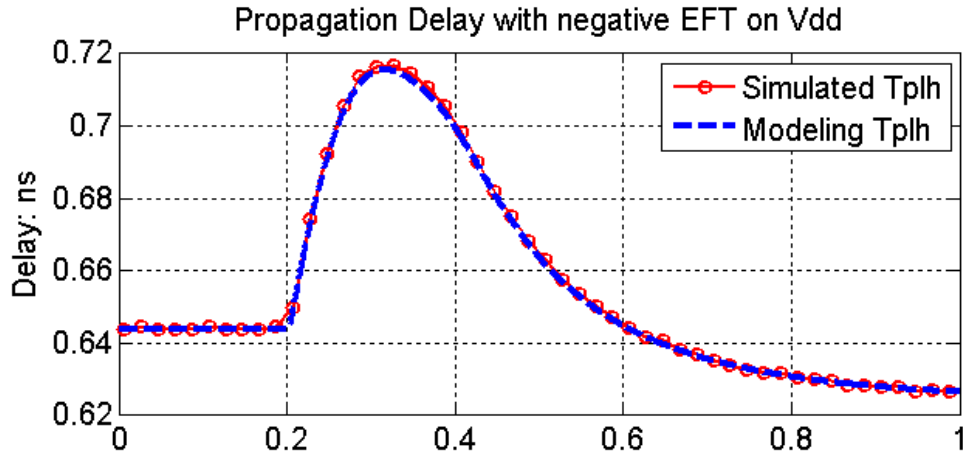


Fig. 16. Simulated and estimated delays through the dynamic logic circuit.

D. Transmission Gates Using 0.18 Micron Technology

Many logic circuit employ transmission gates as well as push-pull circuits. The circuit shown in Fig.17 was used to test the performance of the proposed delay model for transmission gates. Ten transmission gates were connected in series, and configured in transmission mode. The normal power supply voltage was 3.3 V. A negative 3 V EFT pulse was injected on the V_{dd} pin of the IC resulting in the waveform on V_{dd} shown in Fig. 13. The predicted and simulated delays are shown in Fig. 18. The maximum relative errors were 2.6% and 2.5% for t_{pLH} and t_{pHL} , respectively.

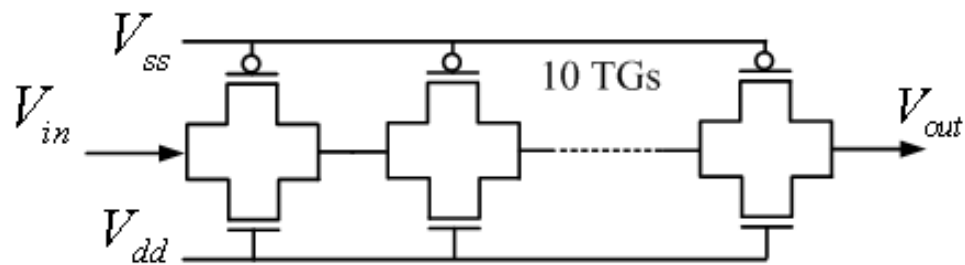


Fig. 17. Ten transmission gates in series.

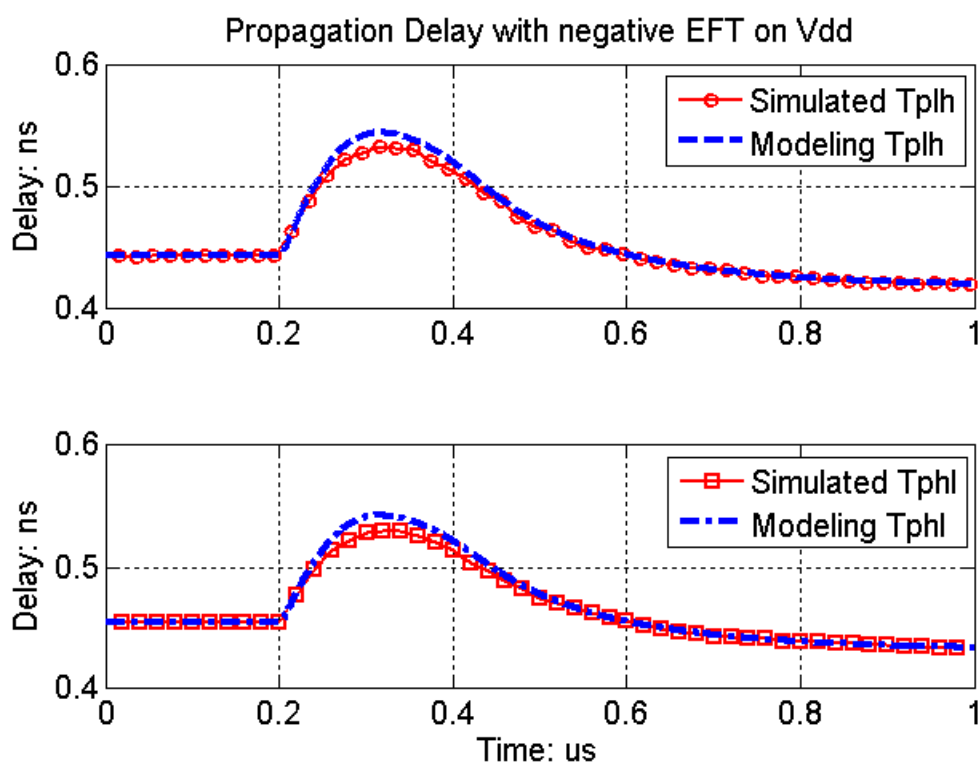


Fig. 18. Simulated and estimated delays through the transmission gate circuit. Top: Tplh; Bottom: Tphl.

V. DISCUSSION AND CONCLUSIONS

An analytical delay model was developed to predict propagation delay variations in logic circuits when the power supply is disturbed by an electromagnetic event. Simulated and measured results demonstrate the accuracy of the approach. Four different types of logic circuits were tested, verifying that the proposed delay model can be applied to a wide range of logic circuits and process technologies. There are some limitations, however, to the delay model. First, since the proposed delay model was derived based on a traditional push-pull logic structure, its accuracy might be lower when it is applied to other logic structures, such as those based on transmission gates. Second, the proposed delay model is a static delay model, which assumes the power supply voltage is constant during the logic transition of the output. Fortunately, this delay model can be extended by using integration methods to solve this problem. The authors are working on this problem and will report the results in the future.

Many electromagnetic events cause soft errors in ICs by momentarily disturbing the power supply voltage. The proposed model can be helpful for predicting and understanding the soft errors caused by these timing changes within the logic. Commercial logic circuits are much more complex than the circuit presented here. Accurate characterization of the susceptibility of such logic circuits should include statistics related to the magnitude of the electromagnetic event and the probability of a particular logic path being active when the event occurs.

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PAPER 3**CLOCK JITTER MODEL FOR SINGLE-ENDED BUFFER DUE TO
DISTURBANCES IN THE POWER SUPPLY**

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ABSTRACT

Soft errors can occur in digital integrated circuits (ICs) as a result of an electromagnetic disturbance, such as might result from an electrical fast transient (EFT), Radio Frequency (RF) noise. Many soft errors come from changes in propagation delays through clock tree or digital logic which are caused by changes in the on-die power supply voltage. Analytical formulas were developed to predict the clock period variation in ICs when the power supply is disturbed by an electromagnetic event. The model was validated by comparison with simulation in Cadence Virtuoso. Three different types of noise, EFT, pulsed RF and narrow pulse, were used to disturb the power supply for testing the proposed model. The period of clock signal at the output of a CMOS buffer was modeled using the analytical formulas proposed in this paper. The predicted variations of clock period agreed with the simulation results. The maximum relative error among all tests is 11.5%.

Index Terms

CMOS integrated circuits, delay effects, jitter, electromagnetic interference, modeling, immunity.

I. INTRODUCTION

Errors can occur in digital integrated circuits (ICs) as a result of an electromagnetic disturbance. IC failures may be caused by a “hard” failure of the IC, for example, due to latch-up or permanent damage to an I/O pin[1][2], or may be caused by a “soft” failure, where incorrect data is read from I/O, internal logic, and/or memory. One common reason for soft errors is that a change in the power supply voltage causes a change in the propagation delay through internal logic or the clock tree, so that the clock edge arrives at a register before valid data and an incorrect logic value is stored at the register [3]. As shown in Fig. 1, for a typical synchronous circuit, when timing criteria $T_{clk} > t_p + t_{co} + t_{su}$ is met, where T_{clk} is the period of the clock, t_p is the propagation delay through the logic gates, the t_{co} and t_{su} are clock to output time and setup time of the D-flip-flop, correct data can be stored. However, the supply voltage variation can cause both T_{clk} and t_p change, thus a timing error might happen due to the disturbance in the power supply.

One main reason for the clock period T_{clk} variation is the delay change through the clock tree circuit. Fig. 2 shows the clock signal propagation through a clock tree. The clock tree circuit is generally a chain of inverters. The uncertainty of the clock period is known as clock jitter [4]. Among the root causes of the clock jitter, the power supply voltage fluctuation is one of the main causes of deterministic jitter (DJ) [5].

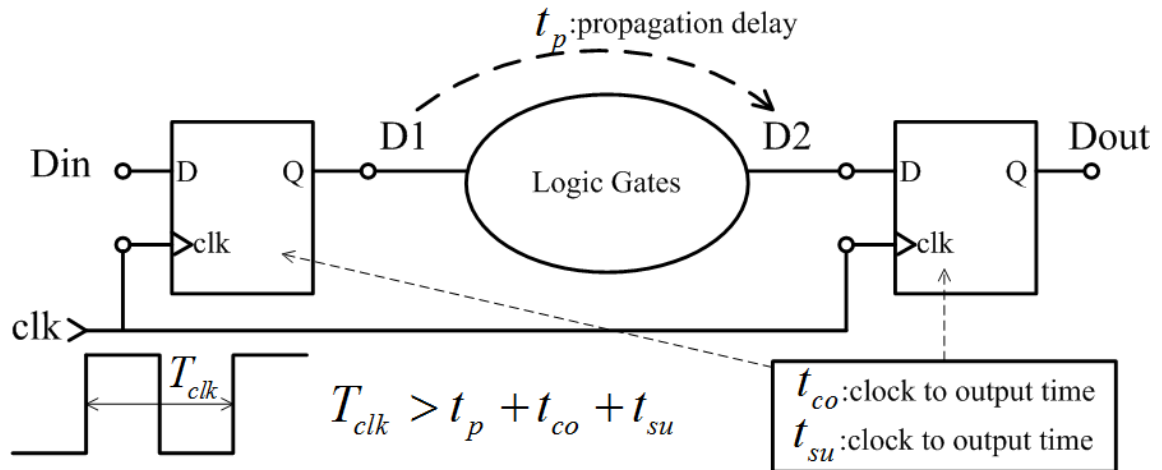


Fig. 1. The typical synchronous circuit.

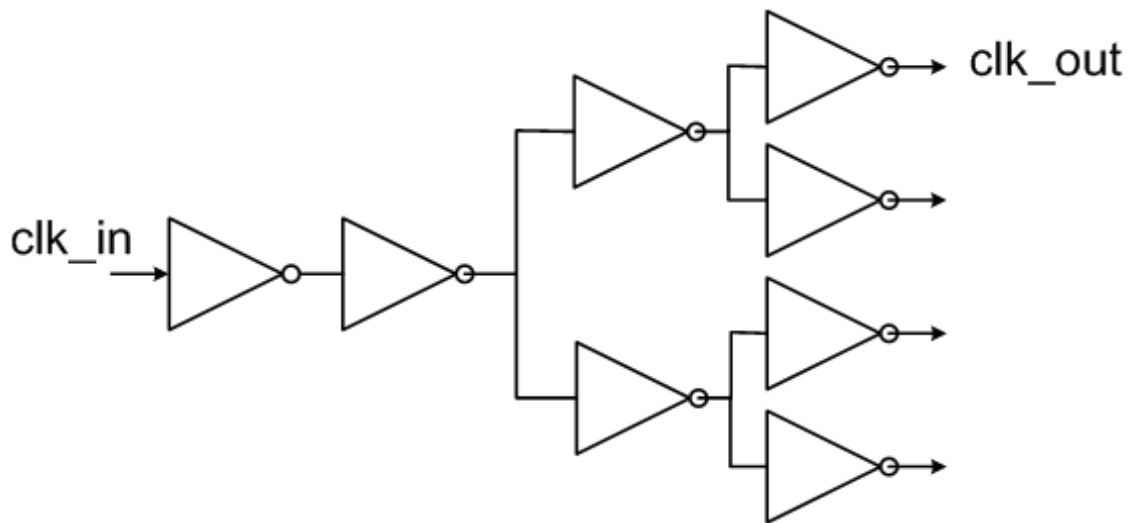


Fig. 2. Clock signal propagation through a clock tree.

Jitter due to supply voltage fluctuation has been studied recently. Several delay models were proposed in the literature that can be used to estimate jitter due to supply voltage variation. The delay change due to a DC level shift of power supply can be analytical calculated by using delay models in [6]-[14]. However the dynamic effect of the supply voltage fluctuation during the buffer transition is not considered. Analytical

closed-form expressions for the transfer functions relating the supply voltage fluctuations to jitter were proposed in [5][15], which could be very useful in jitter estimation.

However, these transfer functions were derived only for one inverter, and detail information about inverter are needed. Although the delay model in [14] is a static model, it can be used for generic logic circuit with less circuit information needed.

In this paper, the delay model developed in [14] was extended into dynamic delay models, in which the dynamic effect of the power supply variation on the propagation delay is considered. The clock period variation due to disturbed the power supply can be calculated using the proposed analytical delay models. The proposed analytical formulas were validated by comparison with Cadence Virtuoso simulations. Three different types of noise sources were simulated to generate different types of power supply voltage variations.

The paper is presented in five sections. The analytical delay model in [14] was briefly described in Section II. The proposed clock jitter model is derived in Section III. In Section IV, the clock jitter model is validated by comparison with simulated results. Discussion and conclusions are given in Section V.

II. THE DELAY MODEL

An analytical delay model for generic logic gates was developed in [14] by the same authors, in which the propagation delay through a logic gates is given by:

$$t_{pLH}, t_{pHL} \approx \frac{V_{dd}}{(V_{dd} - V_{th})^\alpha} \cdot [S1 \cdot f(V_{th}, \alpha) g(V_{dd}, V_{th}, \alpha, D) + S2] \quad (1)$$

where

$$f(V_{th}, \alpha) = \left(\frac{1}{2} - \frac{1 - v_T}{1 + \alpha} \right) \quad (2)$$

$$g(V_{dd}, V_{th}, \alpha, D) = \frac{0.9}{0.8} + \frac{D(V_{dd} - V_{th})^{\alpha/2}}{0.8V_{dd}} \cdot \ln \frac{10D(V_{dd} - V_{th})^{\alpha/2}}{eV_{dd}} \quad (3)$$

$$v_T = V_{th} / V_{dd} \quad (4)$$

$$D = \frac{V_{D0,ref}}{(V_{dd,ref} - V_{th})^{\alpha/2}} \quad (5)$$

$S1$ and $S2$ are two unknown constant which are independent on the power supply voltage. They can be either analytically calculated when detailed information (FET size, capacitance etc.) about the circuit structure is known or be found through experiments or simulations without detailed information about the circuit structure [14]. V_{dd} is the power supply voltage, V_{th} is the threshold voltage, α is the velocity saturation index for a MOSFET, and $V_{D0,ref}$ is drain saturation voltage when $V_{GS} = V_{dd,ref}$.

III. THE CLOCK JITTER MODEL

The delay model described in section II can be used to estimate the delay variation through clock tree due to the supply voltage fluctuation. As shown in Fig. 3, the period of the i th clock cycle is defined from the i th rising edge to $(i+1)$ th rising edge of the clock signal ($i = 1, 2, 3, \dots$). The period, T , of the i th cycle of the clk_out signal is given by:

$$T = T_0 + (t_{pLH,i+1} - t_{pLH,i}) \quad (6)$$

where $t_{pLH,i}$ is the low to high propagation delay through the clock tree, for the i th clock rising edge and T_0 is the normal clock period. In this paper, the rising edge was used to calculate the period of clock, however, the same methodology can be used for the falling edge. The value of $t_{pLH,i}$ depends on the power supply voltage during the time the i th rising edge of clk_in propagates through the clock tree:

$$t_{pLH,i} = t_{pLH}(V_{dd,i}) \quad (7)$$

where the function $t_{pLH}(\bullet)$ represents the delay model given by (1) and $V_{dd,i}$ is the power supply voltage during the i th rising edge. Because the power supply voltage may change between the time of the i th rising edge of clk_in, t_1^i , and the time the edge is seen at clk_out, t_2^i , dynamic effect of power supply on propagation delay should be considered. It is shown in [16] that when power supply varies during the transition of the signal, the averaged power supply voltage determines the propagation delay. Therefore, two methods were proposed in this paper to deal with the dynamic effect of power supply on

propagation delay. The first method is to use the averaged power supply voltage in (7), as given by:

$$t_{pLH,i} = t_{pLH} \left(\frac{1}{(t_2^i - t_1^i)} \int_{t_1^i}^{t_2^i} V_{dd}(t) \cdot dt \right) \quad (8)$$

The other method is to calculate the averaged propagation delay value during the transition, as given by:

$$t_{pLH,i} = \frac{1}{(t_2^i - t_1^i)} \int_{t_1^i}^{t_2^i} t_{pLH}(V_{dd}(t)) \cdot dt \quad (9)$$

The value of t_2^i , however, is unknown without knowledge of $t_{pLH,i}$. If the change in the power supply voltage between t_1^i and t_2^i is negligible, then

$$t_{pLH,i} \approx t_{pLH}(V_{dd}(t_1^i)) \quad (10)$$

If the change in the power supply voltage between t_1^i and t_2^i is not negligible, then the equation (8) can be approximated by using:

$$t_{pLH,i} \approx t_{pLH} \left(\frac{1}{\Delta t} \int_{t_1^i}^{t_1^i + \Delta t} V_{dd}(t) \cdot dt \right) \quad (11)$$

And equation (9) can be approximated by using:

$$t_{pLH,i} \approx \frac{1}{\Delta t} \int_{t_1^i}^{t_1^i + \Delta t} t_{pLH}(V_{dd}(t)) \cdot dt \quad (12)$$

where Δt is the delay through the clock tree when the power supply voltage is at the normal value:

$$\Delta t = t_{pLH}(V_{dd} = V_{dd,normal}) \quad (13)$$

Here, three equations (10), (11) and (12) can be used to estimate the propagation delay through the clock tree. Equation (10) is suitable for the case that power

supply is close to static during propagation of the signal, while equation (11) or (12) can handle the dynamic effect of power supply variation during the propagation.

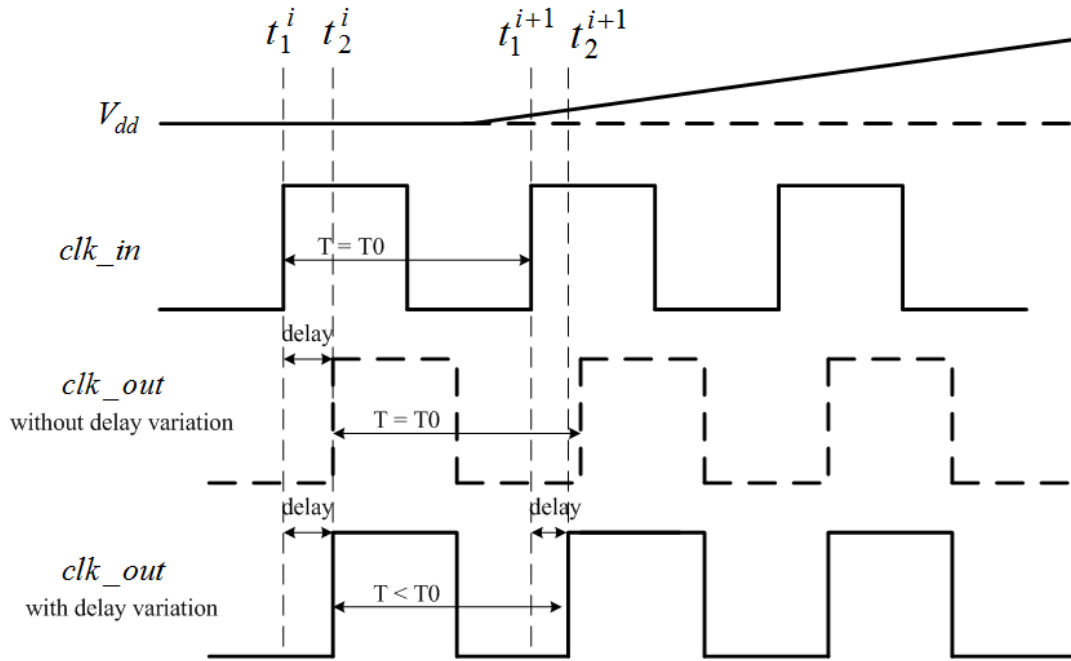


Fig. 3. Clock tree jitter due to the variation of delay through the clock tree.

IV. MODELING RESULTS

The validity of the proposed jitter model was tested in this section. As shown in Fig. 4, an inverter chain was used to represent a clock tree. The number of inverters is 60. The inverter chain was simulated in Cadence Virtuoso using 0.18 micron technology. As demonstrated in [14], the delay model in (1) is independent of technology, so the proposed clock jitter model should apply to both older and newer technologies. In the following test cases, the clk_in signal is a 200 MHz square clock signal. The normal V_{dd} value is 3.3 V. The V_{dd} was disturbed by noise, causing the clock jitter in the clk_out

signal. The jitter of the clk_out signal was estimated by using equations (6-13). Three different types of noise were used to validate the proposed clock jitter model.

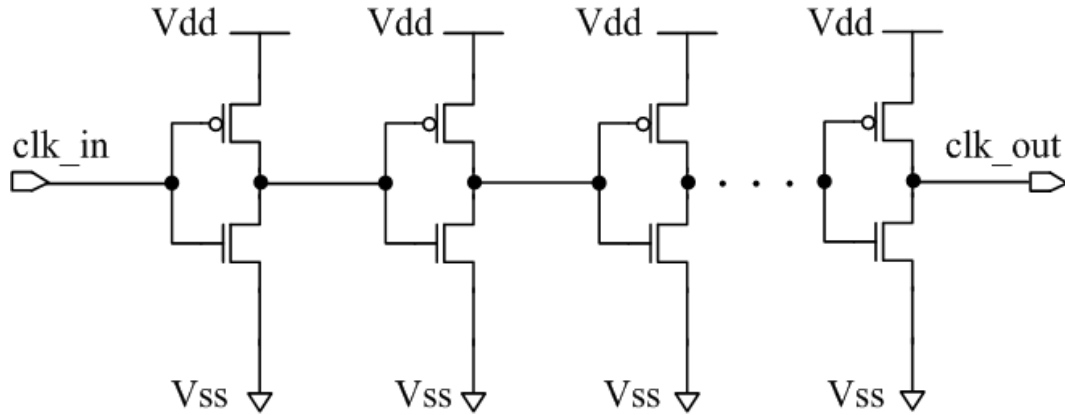
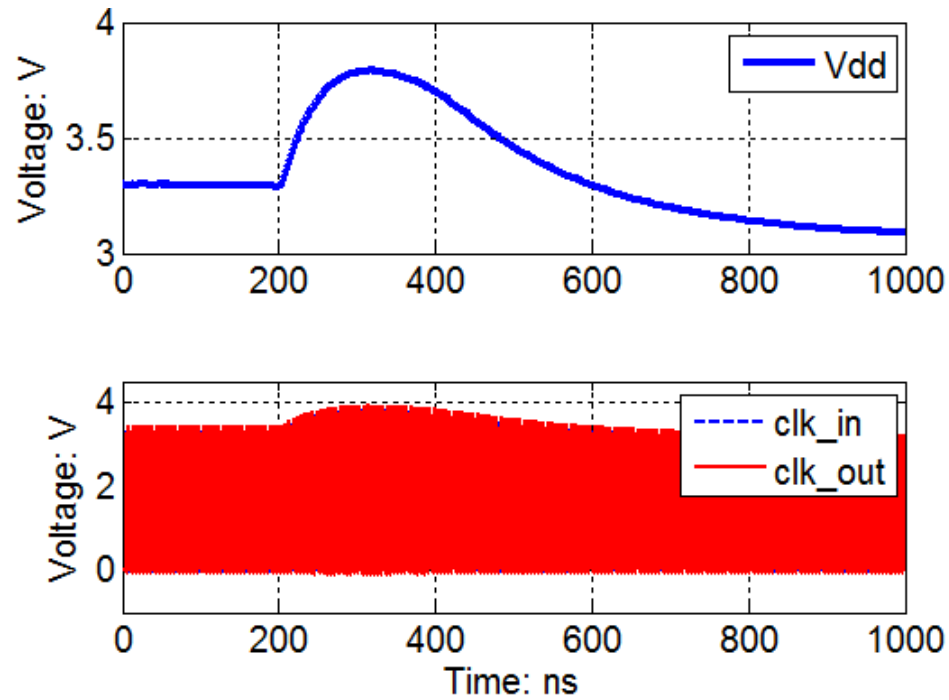


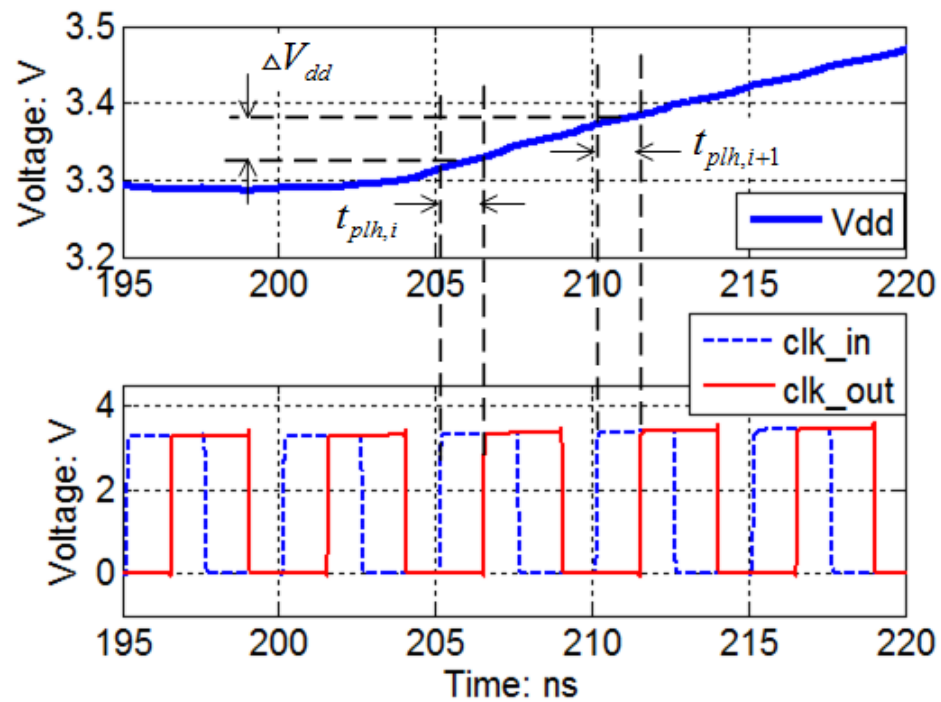
Fig. 4. An inverter chain.

A. Electrical Fast Transients (EFT) Noise on Vdd

In this test case, the electrical fast transient (EFT) [17][18] pulse was injected into the V_{dd} . Fig. 5 shows the disturbed V_{dd} waveform, clk_in and clk_out waveform. In this case, because the change of V_{dd} during the propagation of the signal is small, equation (10) was used to estimate the propagation delay through the clock tree.



(a)



(b)

Fig. 5. Vdd waveform and clock signal in the case of a positive EFT pulse is injected on Vdd. (a) 1 μ s view. (b) Zoom in view.

The jitter was caused by the delay variation through the inverter chain. The modeling propagation delay of the clock rising edge using delay model in (1) is shown in Fig. 6, and compared with the simulated delay result. The modeling result agrees well with the simulated delay. The estimated jitter, which is difference between the maximum delay and minimum delay, is 97 ps, close to the simulated jitter value, 104 ps.

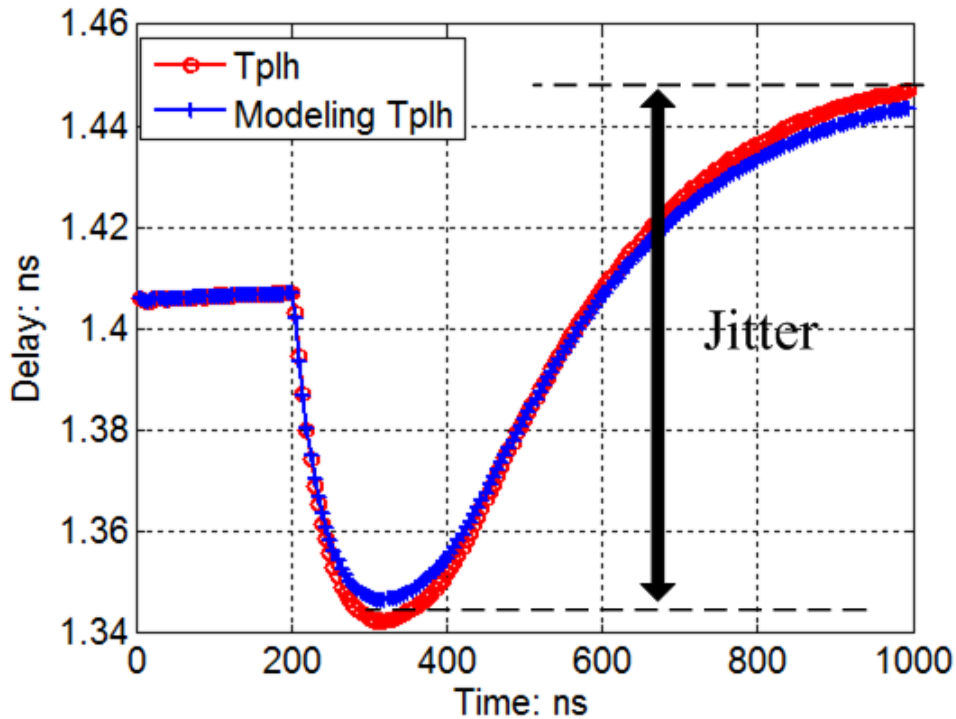


Fig. 6. Propagation delay variation due to EFT pulse on Vdd.

Although the V_{dd} variation causes the jitter in the clock rising edge, it is the variation of the period of clock that could cause a soft error inside the IC. Therefore, it is more meaningful to model the clock period variation rather than the jitter of one clock edge. Clock period was calculated using equation (6). Fig. 7 shows the estimated clock period using the proposed clock jitter model, which is close to the simulated result. There is some numerical noise shown in the simulation results due to the very small scale of

vertical axis. By comparing Fig. 6 and Fig. 7, it is easily found that although for this type of V_{dd} variation cause a relatively big delay variation in clock tree, the clock period variation is very small. This is because that the ΔV_{dd} for two successive edges is relatively small in this case, as shown in Fig. 5(b), resulting in the small variation of propagation delay for two successive clock rising edge $t_{pLH,i}$, $t_{pLH,i+1}$.

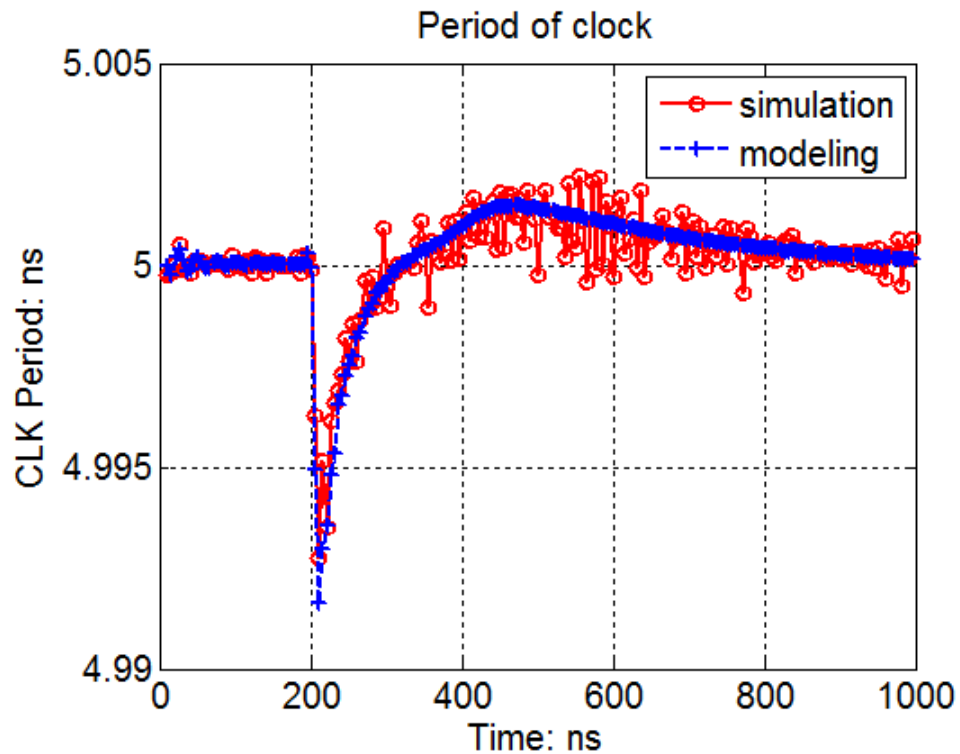


Fig. 7. Modeling result for the period variation of clk_out signal caused by the EFT noise on Vdd.

B. Pulsed RF Noise on V_{dd}

In the case of EFT noise, the power supply voltage variation was relatively slow compared with the clock signal, thus a constant V_{dd} value can be used to evaluate the propagation delay for one transition edge and equation (10) can be used to predict the delay value. When the power supply voltage has a big variation during the propagation time, however, the dynamic effect of the power supply on propagation delay should be considered. As shown in Fig. 8, the V_{dd} was disturbed by a pulsed RF noise. The frequency of RF signal is 900 MHz. Fig. 8 (a) shows the overall waveforms for 600 ns, and Fig. 8 (b) shows a zoom-in view for the waveforms from 195 ns to 220 ns. In the simulation, the parasitic inductance and capacitance of the bonding wire and pad of IC were considered, therefore, overshooting happens on the V_{dd} at the beginning and end of the pulsed RF signal. As shown in Fig. 8(b), the RF signal is coupled into the V_{dd} signal, causing V_{dd} swing from 2.55 V to 4 V at frequency of 900 MHz. The V_{dd} variation is big and fast during the propagation time of the clock signal. For this type of power supply variation, the equation (11) or (12) can be used to estimate the propagation delay through the clock tree.

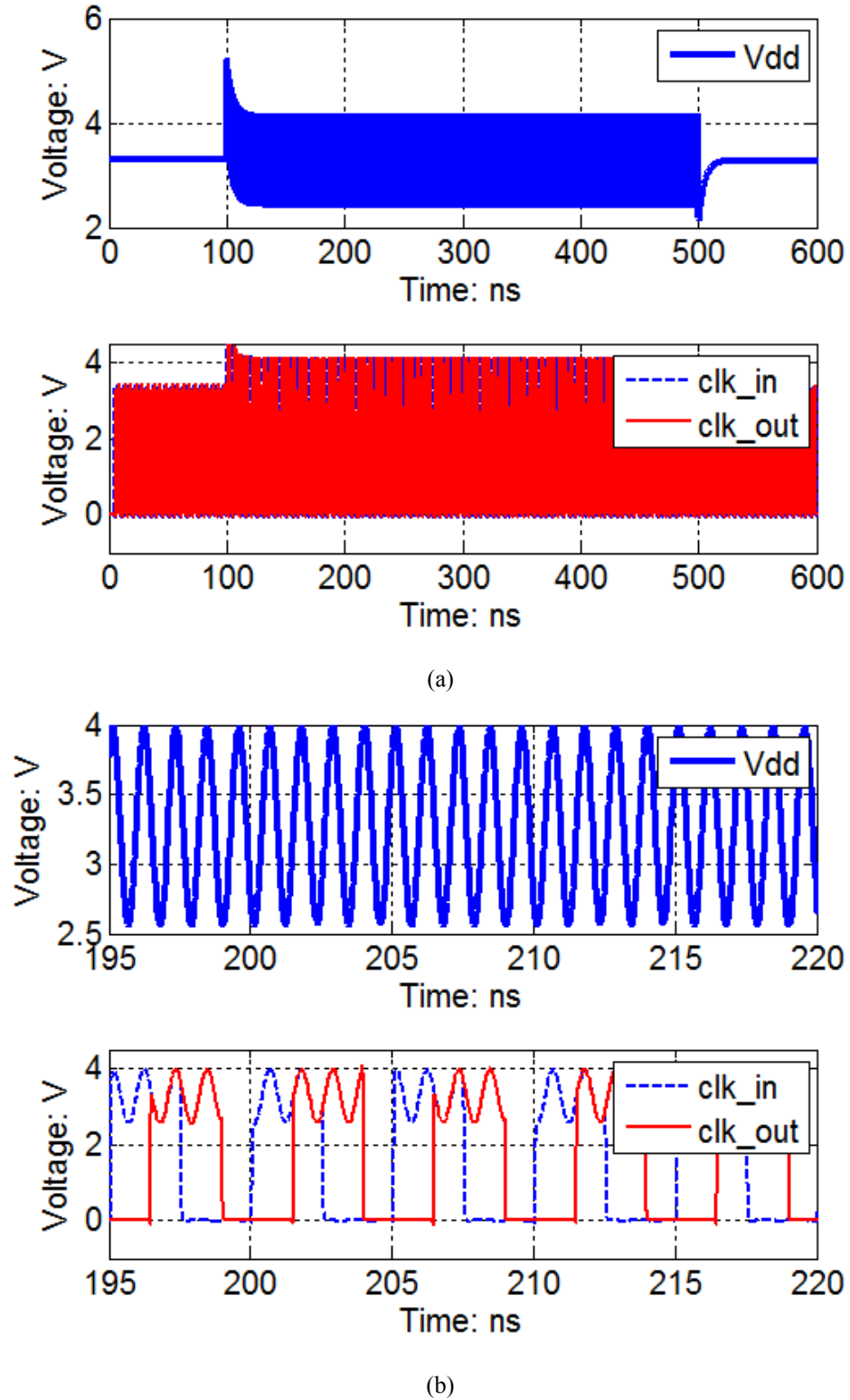


Fig. 8. Vdd waveform and clock signal in the case of 900 MHz pulsed RF signal is injected on Vdd. (a) overall view. (b) Zoom in view.

The modeling result for the period of clk_out signal using equation (6) and (11) is shown in Fig. 9 and compared with the simulation result in Cadence Virtuoso. The modeling result agrees well with the simulation result. Using the relative error defined in (14), the maximum relative error is 11.5%.

$$Error = \frac{|T_{model} - T_{simulation}|}{|T_{simulation} - T_0|} \times 100\% \quad (14)$$

In this modeling result, the equation (11) was used to estimate the propagation delay through the clock tree. The performance of equation (12) was tested as well. The comparison of modeling results using equation (11) and (12) is shown in Fig. 10. It shows that the equation (11) and (12) has similar performance, both of them works well with equation (6) to predict the clock period change caused by the power supply variation. For compactness, only the modeling results using equation (11) are shown in the following paper.

It can be seen from Fig. 9 that the period variation caused by the 900 MHz pulsed RF signal fluctuates at frequency of 100 MHz (period 10 ns). This is because the frequency of the clk_in signal is 200MHz, and then 10 ns is the minimum common multiple number of clk_in period and the period of the RF signal. This frequency value (100 MHz) can be seen as the minimum mixed frequency of RF noise frequency and clock frequency, which is $5 \times f_{clk} - f_{RF}$.

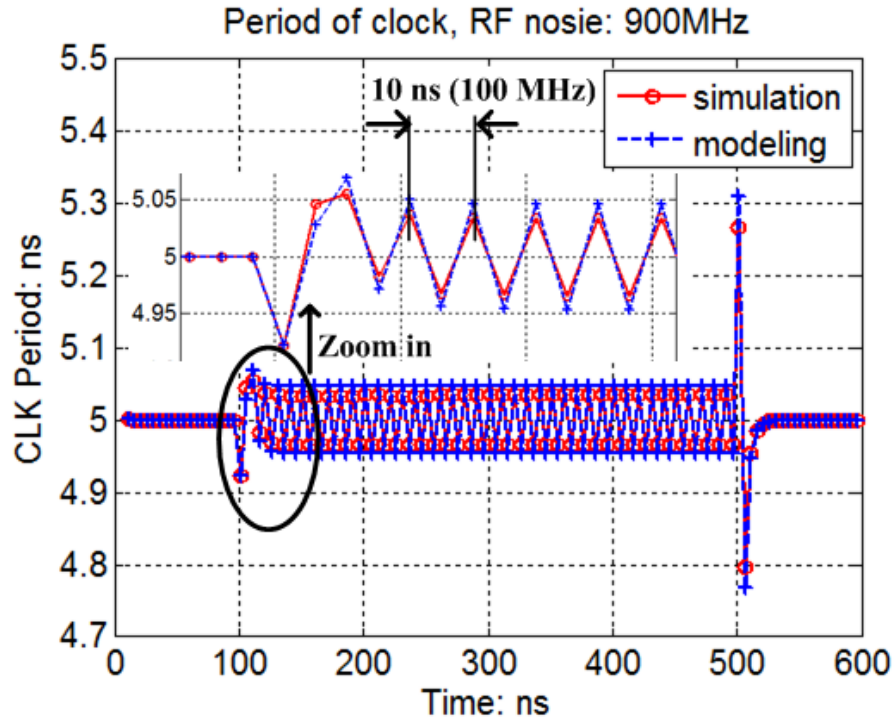


Fig. 9. Modeling period result (using equation (11)) for the case that 900 MHz pulsed RF noise is injected on Vdd.

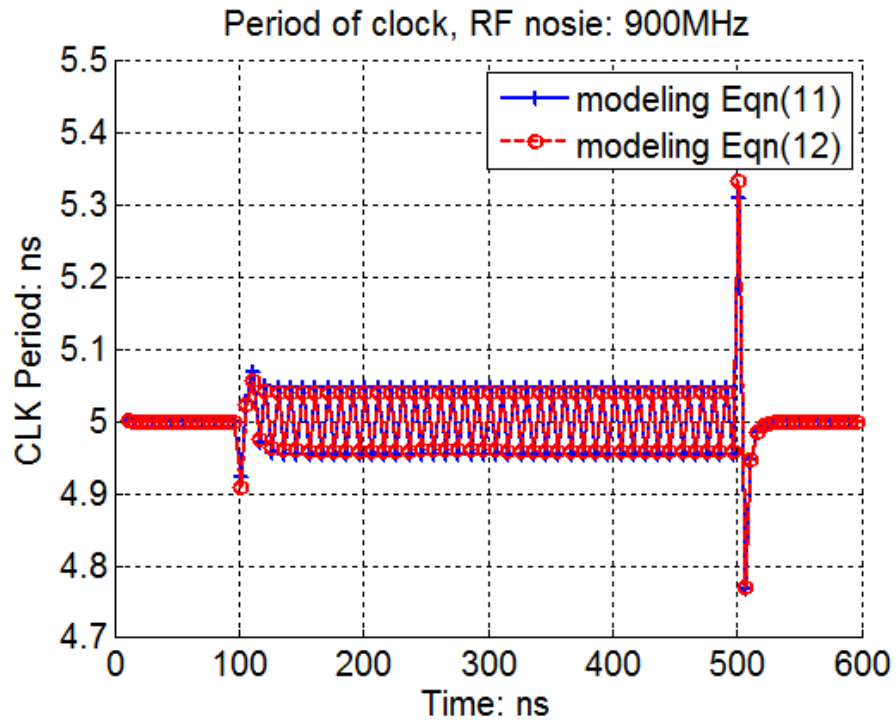


Fig. 10. Comparison between the modeling period result using equation (11) and result using equation (12).

The 800 MHz and 960 MHz pulsed RF noises were also tested to further verify the proposed method. The V_{dd} waveforms for 800 MHz and 960 MHz pulsed RF noise are similar with the V_{dd} waveform shown in Fig. 8 except the different frequency. The modeling period results for 800 MHz and 960 MHz RF noise are shown in Fig. 11 and Fig. 12, respectively. Both the modeling results agree well with the simulation results in Cadence Virtuoso. The maximum relative errors are 7% and 4% for 800 MHz and 960 MHz noise, respectively. For 800 MHz RF noise, since the period of the clock signal (5 ns) is 4 times of the period of the RF noise signal (1.25 ns), $4 \times f_{clk} = f_{RF}$, the V_{dd} waveform has the same variation at every clk_in rising edge. Although the propagation delay through clock tree may changes due to the RF noise, the delay values are same for every clock rising edge during the stable stage of the V_{dd} waveform. Therefore, except the beginning and end of the RF signal, the period of clk_out signal will has no variation. While for the 960 MHz RF noise case, the period of clk_out signal fluctuates at the frequency of 40 MHz, which is $5 \times f_{clk} - f_{RF}$.

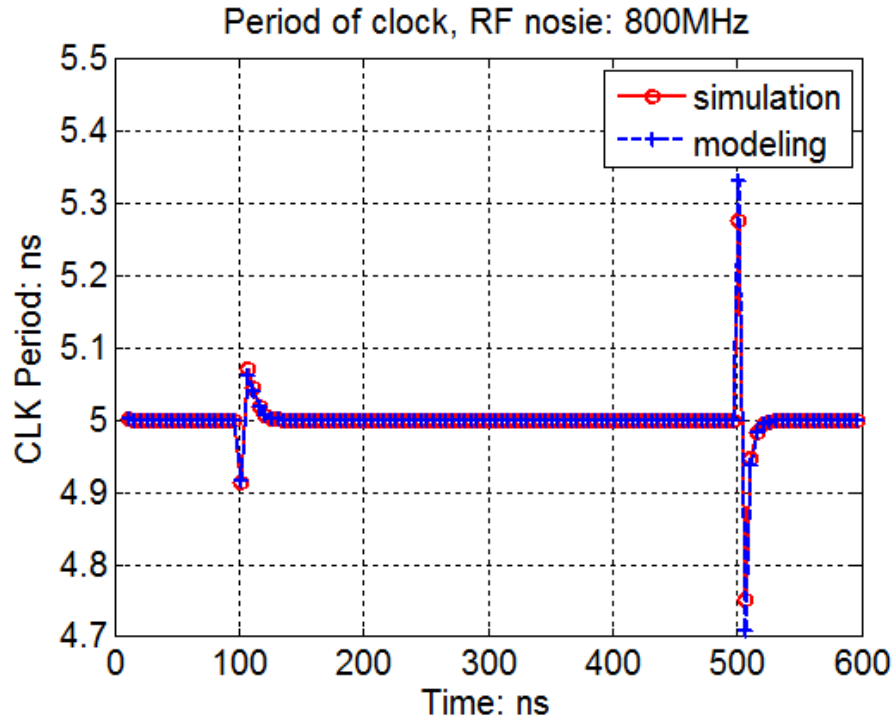


Fig. 11. Modeling period result for the case that 800 MHz pulsed RF noise is injected on Vdd.

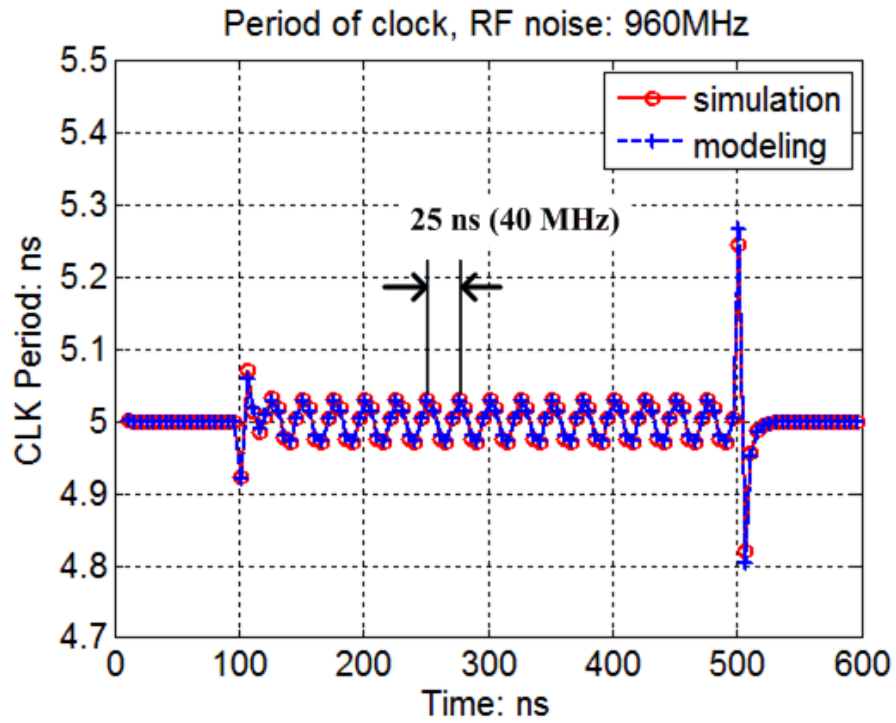


Fig. 12. Modeling period result for the case that 960 MHz pulsed RF noise is injected on Vdd.

C. *Narrow Pulse Noise on Vdd*

The narrow pulse noise with fast rising or falling time is another type of noise which is usually used in IC immunity test. Fig. 13 shows the V_{dd} waveform when a negative pulse, with 1 ns falling time, 1 ns pulse width and 1 ns rising time, was injected into the V_{dd} of IC. The ringing of the V_{dd} is caused by the parasitic inductance associated with bonding wire and the on-die decoupling capacitor. The modeling period variation of the clk_out signal is shown in Fig. 14, which agrees well with the simulation results. The maximum relative error is 10.6 %.

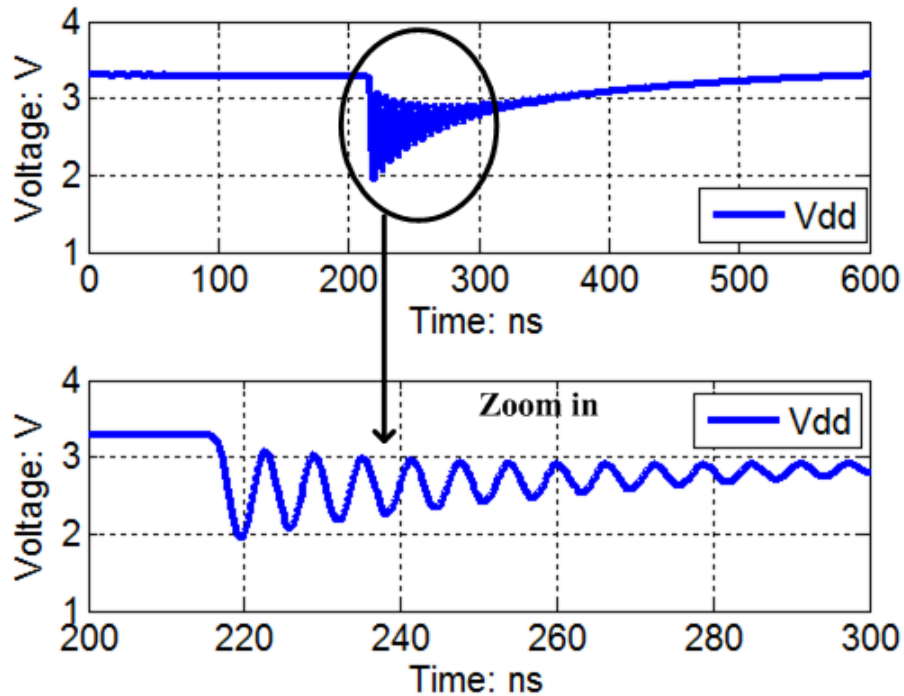


Fig. 13. Vdd waveform and clock signal in the case of a negative narrow pulse is injected on Vdd. (a) 1 us view. (b) Zoom in view.

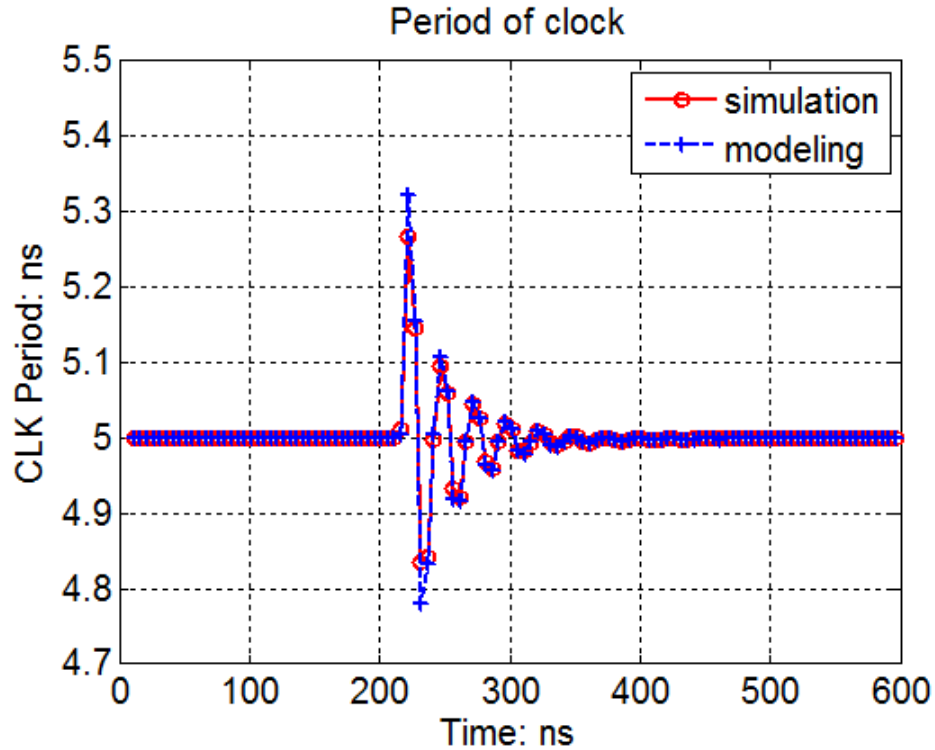


Fig. 14. Modeling period result for the case that a negative narrow pulse noise is injected on Vdd.

V. CONCLUSION AND DISCUSSION

Analytical formulas were developed to predict the clock period variation in integrate circuit when the power supply is disturbed by an electromagnetic event. The proposed formulas can be seen as a clock jitter model. The clock jitter due to the power supply variation can be estimated by the proposed propagation delay model in this paper. It is more meaningful, however, to estimate the clock period variation rather than the delay variation for one clock edge, because it is clock period which affects if a soft error will happen or not. Simulated results using Cadence Virtuoso demonstrate the validity and accuracy of the proposed approach. Three different types of noise were used to

disturb the power supply voltage, verifying that the proposed model can be applied to a wide range of disturbance of power supply. Many electromagnetic events cause soft errors in ICs by momentarily disturbing the power supply voltage. The proposed model can be helpful for predicting and understanding the soft errors caused by these timing changes within the logic.

The proposed formulas in this paper were based on the analytical delay model developed in [14], which can predict propagation delay variations in generic logic circuits when the power supply is disturbed by an electromagnetic event. The delay model in [14], however, is a static delay model, which assumes the power supply voltage is constant during the logic transition of the output. The developed delay formulas in this paper are extension versions of the model in [14]. The dynamic effect of power supply variation on propagation delay is considered in the developed formulas. Therefore the proposed delay model can be used to estimate the propagation delay even when the power supply has fast variation during the propagation of signal. Although in this paper, the developed delay model was only used on the clock tree circuit, which is a simple inverter chain, it can be used for other type of logic circuits as well. This is because the delay model in [14], which is the basis of the proposed model in this paper, can be applied generic logic circuit.

There are also some limitations for the proposed approach. The main limitation is that the timing relation between the power supply voltage waveform and the clock input signal is needed to estimate the clock period variation of the clock output. When the timing relationship between power supply and clock input signal is not known, the

proposed model can be used to predict the maximum clock period variation by sweeping the timing relationship.

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SECTION

2. CONCLUSIONS

The first topic of this dissertation is far-field prediction using only magnetic near-field scanning. When using a Huygens's box, both the tangential electric and the magnetic field are needed. In the first paper of this dissertation, a novel method is proposed to predict the far-field radiation using only the magnetic near-field component on a Huygens's box. The proposed method was verified with two simulated examples and one measurement case. The effect of inaccuracy of magnetic field and the incompleteness of the Huygens's box on far-field results is investigated in this paper. The proposed method can be applied for arbitrary shapes of closed Huygens's surfaces. Only the tangential magnetic field needs to be measured. And it also shows good accuracy and robustness in use. Measuring only the magnetic field cuts the scan time in half.

The second topic of this dissertation is modeling delay variations in CMOS digital logic circuits due to electrical disturbances in the power supply. In the second paper of this dissertation, an analytical delay model was developed to predict propagation delay variations in logic circuits when the power supply is disturbed by an electromagnetic event. Simulated and measured results demonstrate the accuracy of the approach. Four different types of logic circuits were tested, verifying that the proposed delay model can be applied to a wide range of logic circuits and process technologies. Many electromagnetic events cause soft errors in ICs by momentarily disturbing the power supply voltage. The proposed model can be helpful for predicting and understanding the soft errors caused by these timing changes within the logic. Commercial logic circuits are

much more complex than the circuit presented here. Accurate characterization of the susceptibility of such logic circuits should include statistics related to the magnitude of the electromagnetic event and the probability of a particular logic path being active when the event occurs. In the third paper, analytical formulas were developed to predict the clock period variation in integrate circuit when the power supply is disturbed by an electromagnetic event. The proposed formulas can be seen as a clock jitter model. The clock jitter due to the power supply variation can be estimated by the proposed propagation delay model in third paper. It is more meaningful, however, to estimate the clock period variation rather than the delay variation for one clock edge, because it is clock period which affects if a soft error will happen or not. Simulated results using Cadence Virtuoso demonstrate the validity and accuracy of the proposed approach. Three different types of noise were used to disturb the power supply voltage, verifying that the proposed model can be applied to a wide range of disturbance of power supply. Many electromagnetic events cause soft errors in ICs by momentarily disturbing the power supply voltage. The proposed model can be helpful for predicting and understanding the soft errors caused by these timing changes within the logic.

VITA

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