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Two new families of high-gain DC-DC power electronic converters for DC-microgrids

Venkata Anand Kishore Prabhala

Department: Electrical and Computer Engineering

TWO NEW FAMILIES OF HIGH-GAIN DC-DC POWER ELECTRONIC CONVERTERS FOR DC-MICROGRIDS

by

VENKATA ANAND KISHORE PRABHALA

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Approved by

Mehdi Ferdowsi, Advisor
Mariesa L. Crow
Jonathan W. Kimball
Yahong Rosa Zheng
Akim Adekpedjou

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Paper I, Pages 11-30, "DC Distribution Systems – An Overview," to be submitted in *IEEE Power and Energy Magazine*.

Paper II, Pages 31-66, "A Multiport DC-DC Converter with High Voltage Gain," submitted to *IEEE Transactions on Power Electronics*.

Paper III, Pages 67-106, "A High Voltage Gain Bidirectional DC-DC Converter," submitted to *IEEE Transactions on Power Electronics*.

ABSTRACT

Distributing the electric power in dc form is an appealing solution in many applications such as telecommunications, data centers, commercial buildings, and microgrids. A high gain dc-dc power electronic converter can be used to individually link low-voltage elements such as solar panels, fuel cells, and batteries to the dc voltage bus which is usually 400 volts. This way, it is not required to put such elements in a series string to build up their voltages. Consequently, each element can function at it optimal operating point regardless of the other elements in the system. In this dissertation, first a comparative study of dc microgrid architectures and their advantages over their ac counterparts is presented. Voltage level selection of dc distribution systems is discussed from the cost, reliability, efficiency, and safety standpoints. Next, a new family of non-isolated high-voltage-gain dc-dc power electronic converters with unidirectional power flow is introduced. This family of converters benefits from a low voltage stress across its switches. The proposed topologies are versatile as they can be utilized as single-input or double-input power converters. In either case, they draw continuous currents from their sources. Lastly, a bidirectional high-voltage-gain dc-dc power electronic converter is proposed. This converter is comprised of a bidirectional boost converter which feeds a switched-capacitor architecture. The switched-capacitor stage suggested here has several advantages over the existing approaches. For example, it benefits from a higher voltage gain while it uses less number of capacitors. The proposed converters are highly efficient and modular. The operating modes, dc voltage gain, and design procedure for each converter are discussed in details. Hardware prototypes have been developed in the lab. The results obtained from the hardware agree with those of the simulation models.

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I dedicate my dissertation to my father Prabhala Narasimham Murty and mother Prabhala Vijaya Lakshmi and my late grandparents Prabhala Venkata Narasimham and Prabhala Kameswari. They have taught me the importance of education and supported all my endeavors. I would like to thank my wife Deepti for being a constant source of support and encouragement. I would also like to thank my brother Prabhala Ravi Prasad and sister Prabhala Ratna Kameswari for being part of my support system. I would like to thank all my friends and well-wishers for their love and blessings.

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1. INTRODUCTION

With increasing costs of energy from traditional fossil fuel and conventional energy sources, it is becoming imperative to integrate distributed energy resources (DERs) (renewable energy sources like solar, wind, etc.) and distributed energy storage systems (DESS). There are many advantages of renewable energy sources as they provide a much cleaner alternative to fossil fuels with low or no carbon footprint and they are not depleted. However, these sources are intermittent and unreliable thus limiting the optimal utilization of these sources. The concept of microgrid (shown in Figure 1.1) was introduced to help integrate DERs and DESS, therefore, improving the resilience, reliability, and efficiency of the electric grid to any contingencies. The U.S. Department of Energy (DOE) defines a microgrid as, "A microgrid is a group of interconnected loads and distributed energy resources within clearly defined electrical boundaries that acts as a single controllable entity with respect to the grid and that connects and disconnects from such grid to enable it to operate in both grid-connected or 'island' mode".

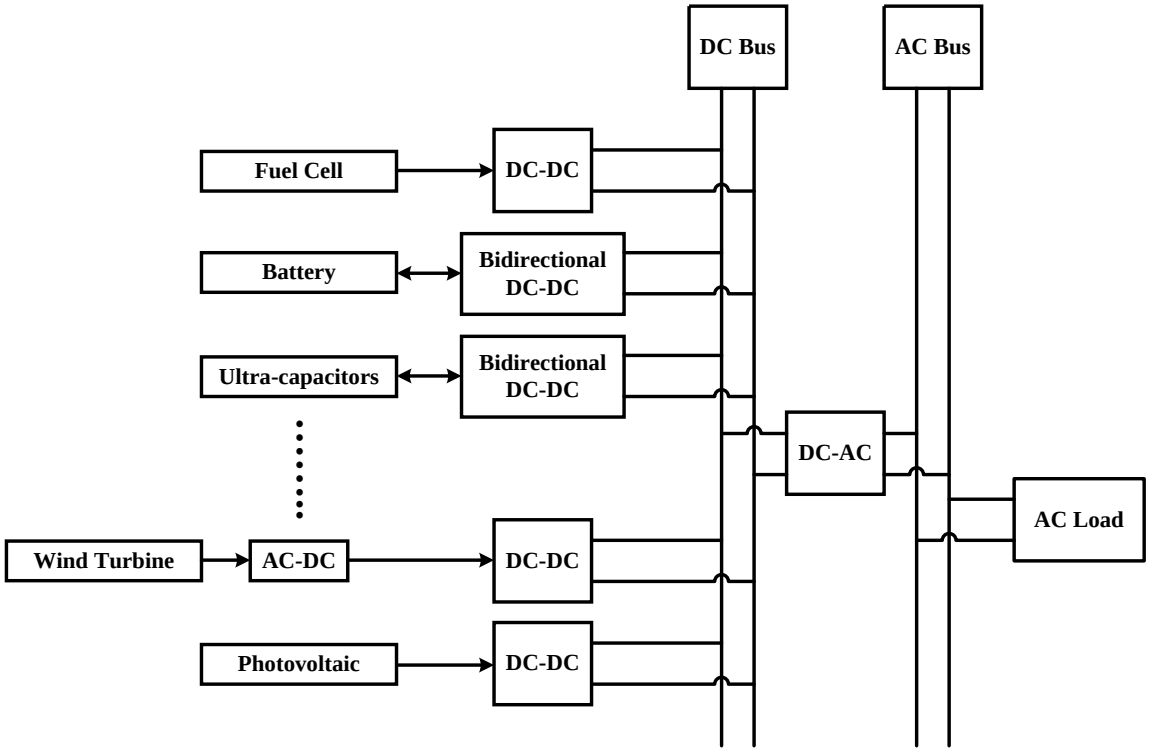

Figure 1.1. Microgrids for interfacing multiple energy sources.

Microgrids can have economic benefits as costs can be reduced by increasing the efficiency of the system. Generally, in dc microgrid systems, renewable energy sources like solar and energy storage systems such as battery systems are low voltage sources which are interfaced with a 400-Vdc bus using dc-dc power electronic converters. High-voltage-gain dc-dc converters can be used to link these renewable energy sources and energy storage systems to the dc bus efficiently thus improving the overall system efficiency. Since solar panels and battery cells have low output voltage, in the conventional approach, several panels/cells have to be connected in series to get higher voltages. Therefore, mismatch in any solar panel or battery cell would affect the output power of the whole string and failure of any one panel/cell would result in the failure of

the entire string. Furthermore, system reliability is improved by individually linking the solar panel or battery cell with the 400-Vdc bus.

1.1. REVIEW OF EXISTING DC-DC TOPOLOGIES

1.1.1. Conventional Non-Isolated Converters. Non-isolated dc-dc converters like buck-boost and boost converters, as shown in Figures 1.2 and 1.3 respectively, are generally used to get output voltages greater than the input source voltage. From (1.1) and (1.2), it can be observed that large duty ratios are required for achieving high voltage gains. Therefore, converter efficiency gets affected due to large input current and high output voltage. Large input currents are due to low input voltage and would result in higher conduction losses in the switch. Therefore, MOSFETs with low $R_{DS(on)}$ should be used. Since the peak blocking voltage of the switch is equal to the high output voltage, MOSFETs sustaining such high voltages have high $R_{DS(on)}$. Therefore, the conduction losses in the MOSFETs are also high. Furthermore, there is a severe reverse recovery problem in the output diode of these converters due to the high output voltage and large pulse currents due to large switch duty ratios. Therefore, conventional non-isolated converters are not an efficient solution for achieving high voltage gains. Moreover, cascading these converters to achieve high gains would decrease the efficiency and increase the cost.

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-d} \tag{1.1}$$

$$\frac{V_{out}}{V_{in}} = \frac{d}{1-d} \tag{1.2}$$

where *d* is the duty ratio of switch *S*.

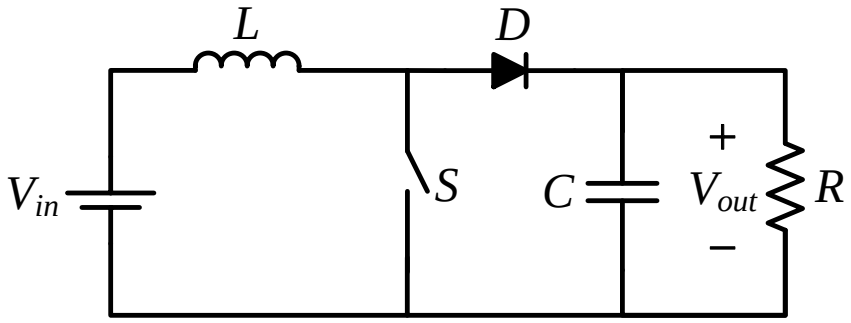

Figure 1.2. Conventional boost converter.

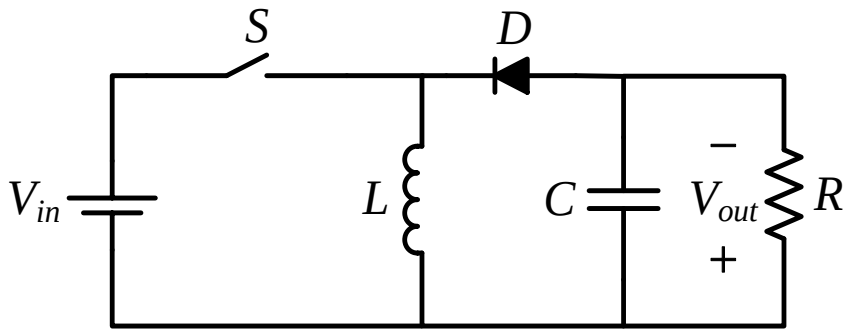

Figure 1.3. Conventional buck-boost converter.

1.1.2. Conventional Isolated Converters. Isolated converters like flyback converters, as shown in Figure 1.4, can be used to achieve large voltage conversion ratios. In a flyback converter, coupled inductors are used to transfer energy to the output and large voltage gains given by (1.3) which can be achieved by selecting higher turns ratio. Leakage inductance increases with increasing winding turns resulting in increased voltage stresses across the switch. Therefore, active clamping techniques are required which makes the design complicated. Moreover, the input current is not continuous, which is not ideal for solar applications.

$$\frac{V_{out}}{V_{in}} = \frac{N_2}{N_1}\frac{d}{1-d} \tag{1.3}$$

where d is the duty ratio of switch S and N_2/N_1 is secondary to primary turns ratio.

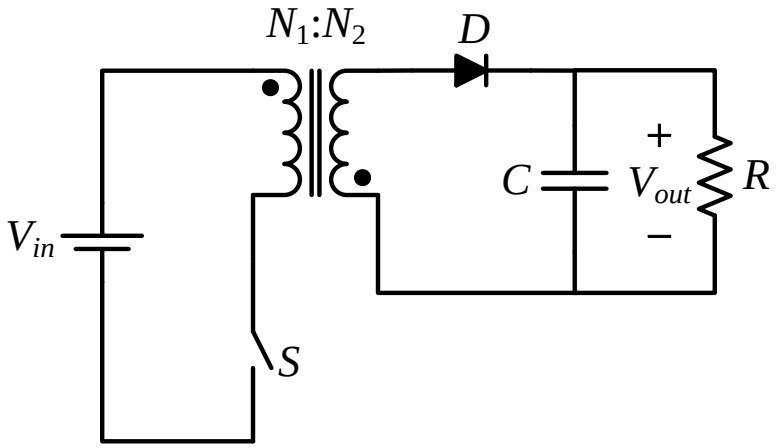

Figure 1.4. Flyback converter.

1.1.3. Tapped-Inductor Boost Converter. The tapped-inductor boost converter shown in Figure 1.5 is an extension to the normal boost converter [1]. Similar to the flyback converter, a coupled inductor is used to transfer energy from the input to the output. High voltage gains given by (1.4) can be achieved by using appropriate turns ratio. However, voltage spikes appear across the switch due to the leakage inductance, hence clamping techniques are used to reduce the voltage stresses across the switch. Furthermore, the input current is not smooth and has large input current ripple which is unsuitable for solar applications.

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-d} + \frac{N_2}{N_1}\frac{d}{1-d} \tag{1.4}$$

where d is the duty ratio of switch S and N_2/N_1 is secondary to primary turns ratio.

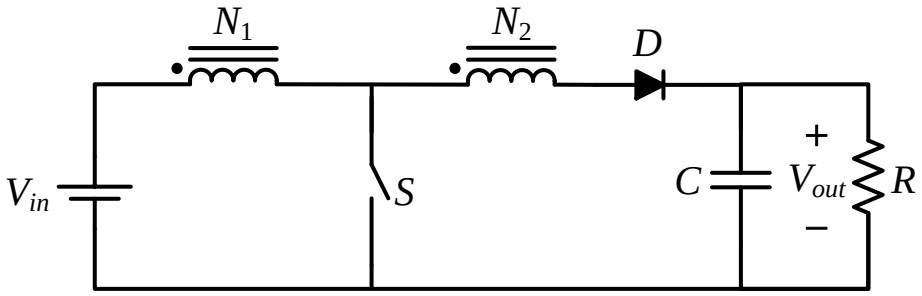

Figure 1.5. Tapped inductor boost converter.

1.1.4. Interleaved Coupled Inductor Boost Converter. Dc-dc converters derived from boost topologies have continuous input currents which are particularly useful for renewable energy applications such as solar. Several interleaved coupled inductor boost topologies have been proposed in [2-19], which have continuous input current. From Figures 1.6 and 1.7, it can be seen that high gains given by (1.5) can be achieved by keeping the coupled inductors in backward polarity and voltage multiplier cells can be used to achieve higher gains given by (1.6). The main disadvantage of these topologies is that there are voltage spikes across the switches due to the leakage inductance. Therefore, several active clamping techniques have been suggested which makes the design complicated.

$$\frac{V_{out}}{V_{in}} = \left(\frac{N_2}{N_1} + 1\right)\frac{1}{1-d} \tag{1.5}$$

$$\frac{V_{out}}{V_{in}} = \left(2\frac{N_2}{N_1} + 1\right)\frac{1}{1-d} \tag{1.6}$$

where d is the duty ratio of switch S and N_2/N_1 is secondary to primary turns ratio.

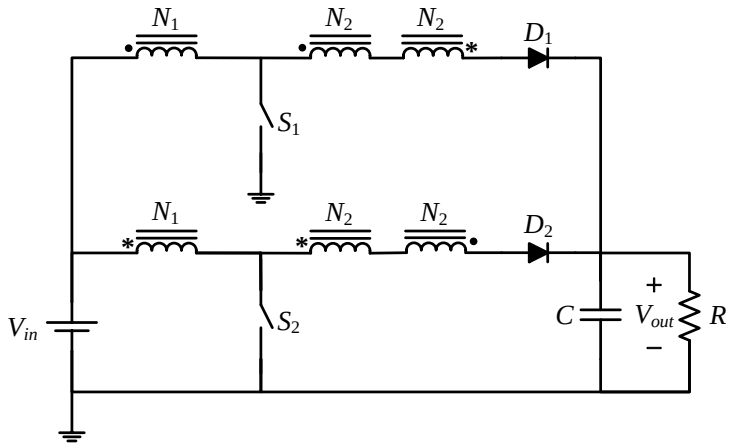

Figure 1.6. Interleaved coupled inductor boost converter.

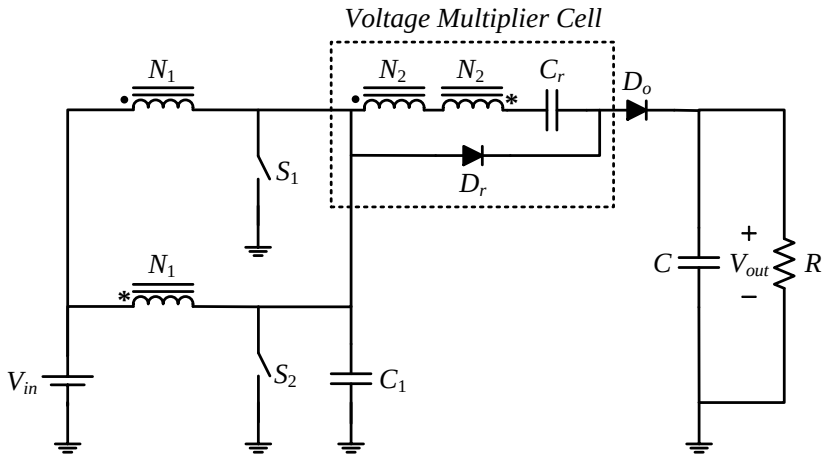

Figure 1.7. Interleaved coupled inductor boost converter with voltage multiplier.

1.1.5. Interleaved Boost Converter with Diode-Capacitor Voltage Multipliers. Interleaved boost converters with several diode-capacitor voltage multiplier stages cascaded together to boost up the voltage have been proposed in [20-25]. They have low input current ripple and have low voltage stresses across the switches. Figure 1.8 shows the interleaved boost converter with Cockcroft-Walton voltage multiplier. The output impedance of the Cockcroft-Walton based converters increases rapidly with the number of multiplying stages [23, 24, 26]. The efficiency and the output voltage regulation depend on the output impedance; therefore, for high gains the converter efficiency would be reduced.

Similarly, a multiphase converter is introduced in [20-22] based on integrating the diode-capacitor voltage multiplier cells (shown in Figure 1.9) with the interleaved boost converter. The static gain of the converter is determined by the number of multiplier stages and duty ratio of the switches of the interleaved boost stage. The voltage conversion ratio for both the topologies for *N* number of multiplier stages is given by

$$\frac{V_{out}}{V_{in}} = \frac{(2N+1)}{1-d} \tag{1.7}$$

where *d* is the duty ratio of switch *S*. It can be observed that this topology has more number of diodes and capacitors which can affect the efficiency of the power stage. Therefore, it is important to have voltage multiplier stages with reduced number of diodes and capacitors. Moreover, it is also important to have voltage multiplier stages that have lower output impedance which would improve the efficiency and the output voltage regulation of the converter.

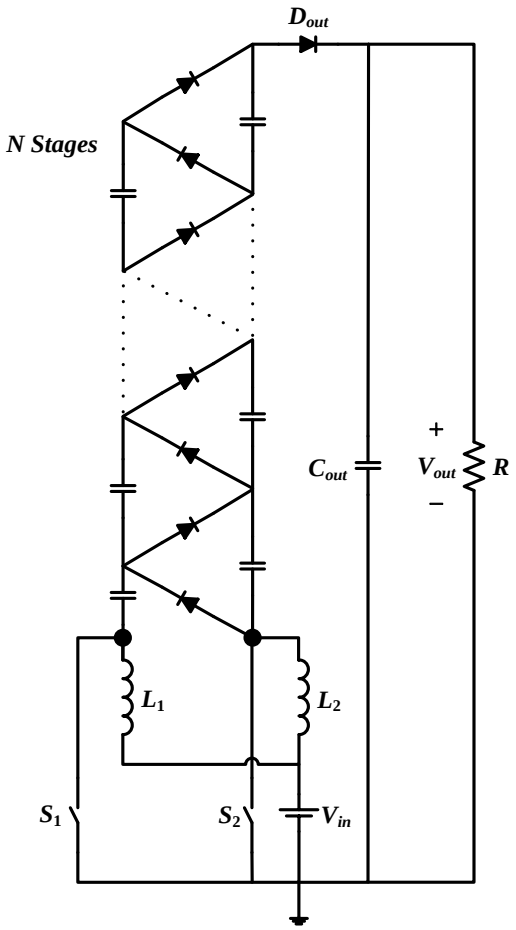

Figure 1.8. Interleaved boost with Cockcroft-Walton voltage multiplier.

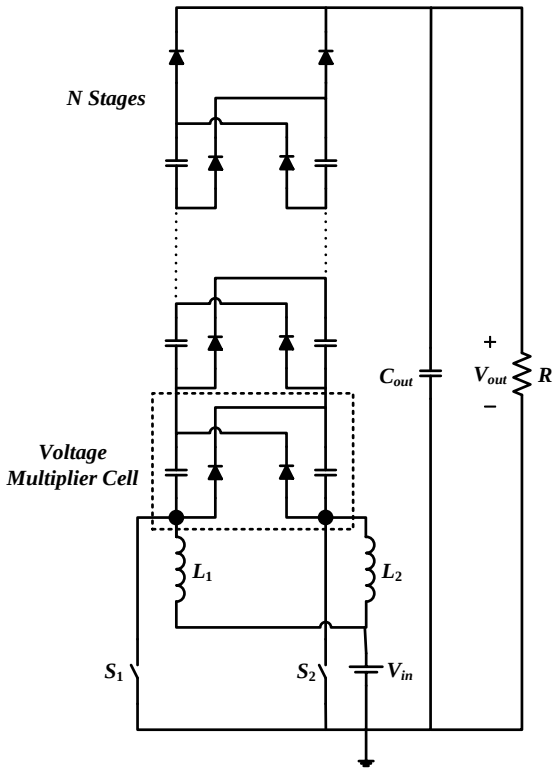

Figure 1.9. Multiphase converter with diode-capacitor voltage multiplier cells.

1.2. RESEARCH CONTRIBUTION

In this dissertation, paper I gives a brief overview of different power distribution architectures which include both ac and dc distribution systems for different voltage levels. Dc bus voltage level selection has also been discussed. Furthermore, it discusses the reliability and cost, safety and protection, and efficiency of dc distribution systems.

In paper II, a multiport unidirectional high-voltage-gain dc-dc converter topology is proposed which can easily achieve a gain of 20 while benefiting from a continuous input current. Such a converter can individually link a PV panel to a 400-Vdc bus. Different modes of operation have been explained and the voltage gain of the converter is derived. An alternative topology along with its combined variant has also been introduced. Furthermore, current and voltage stresses required for component selection and loss calculations along with simulation results are provided. Experimental results validating the converter operation are also provided.

Finally in paper III, a novel SC converter with multiphase switching scheme is introduced and different modes of operation are explained. The output impedance of the proposed SC converter is derived. Switch realization for bidirectional operation and design guidelines for component selection has also been provided. A bidirectional dc-dc converter for dc microgrid applications has been proposed. The experimental results for the prototype converter are provided for both directions of power flow.

PAPER

I. DC DISTRIBUTION SYSTEMS - AN OVERVIEW

***Abstract*—**This paper examines the existing and future dc distribution systems which has wide range of applications in data centers, telecommunication systems, residential homes, space crafts, electric vehicles, and aircrafts. The advantages and disadvantages of a dc distribution system are compared against their ac counterpart. Several dc distribution architectures are presented. Dc distribution systems are discussed from the cost, reliability, efficiency, and safety standpoints.

I. INTRODUCTION

The growing need for highly reliable power supply for critical applications like in hospitals, data centers, telecommunication systems, and semiconductor industry necessitated extensive use of power electronic converters (PEC). These converters improve the system reliability, controllability, efficiency, cost, safety and size of the system. PECs have been extensively incorporated in the power system of electric cars, aircrafts, ships, and space stations [1-8]. Also, interfacing different sources of energy (renewable energy sources like wind and solar) and energy storage systems (batteries and ultra-capacitors) is done with PECs. So the power distribution system should be designed in a way to have all the aforementioned characteristics. The system architecture, energy flow control, protection, and power quality become very important.

Recent developments in the renewable energy technology and increased penetration of the distributed energy sources are prompting renewed interest in the dc distribution systems. The dc power distribution system was first proposed for lighting purposes and patented by Edison [9] in 1883. Sprague proposed an ac distribution system in 1886 [10] that eventually became popular and universally adopted for electric power distribution. Telecommunication systems and datacenters are one of the few surviving examples of dc distribution systems. They are low voltage (48 Vdc) and low load power systems that have characteristics similar to a conventional dc distribution system. Increased load levels would entail increased voltage levels for better system efficiency, reliability, and cost. In addition, the system should be able to fully utilize all the energy sources and should have the flexibility for future expansion.

In case of residential applications, a dc microgrid (or nanogrid) structure is used for dc buildings which are higher voltage dc systems. In this paper, a comparative study has been presented for selecting an optimum dc bus voltage level that would improve the system efficiency and reliability. Authors in [11-17], show different power delivery architectures for both ac and dc systems with different voltage levels. Ideally, power delivery architecture should provide power at low cost and should maximize the efficiency. It should also be reliable to supply critical and sensitive loads as uninterrupted power is necessary for applications such as data centers. Moreover, there should be room for further expansion as and when necessary. In [18-24], authors propose new topologies for power electronic converters with high efficiency and high power density that can be used to improve the overall efficiency of the distribution system.

II. Power Architecture and Voltage Levels

The factors that affect the selection of power delivery architectures are mainly voltage levels, energy, quality of power required by the load, overall life, utility ratio, overall costs, and efficiency. For example, telecommunication loads require low voltage and high quality power supplied reliably to them. Moreover, it should be flexible enough to expand and integrate new sources of energy. Low voltage dc systems for telecom and datacenter applications operate at 48 Vdc. It has at least three conversion stages from the ac input to the load and hence results in lower system efficiency. In [25-33], different voltage levels for the dc bus have been proposed based on efficiency, reliability, and cost considerations.

In [11] and [12], three different power architectures namely conventional ac architecture, rack-level dc architecture, and facility-level dc architecture used in data and telecom centers have been described. Conventional dc system architecture for datacenter applications has a medium voltage transformer that steps down the utility voltage to 480 Vac (shown in Figure 1). The uninterruptible power supply (UPS) unit supplies power to the power distribution unit (PDU) which steps down the voltage to 208 Vac. The voltage is stepped down to keep it in the input range of the power supply unit (PSU) of the server. It can be observed that there are several conversion stages which include the double conversion stage of the UPS where the input ac voltage is converted to dc where the energy storage system is connected, again it is converted back to ac which is stepped down to 208 Vac using a transformer. This ac voltage is converted to a dc voltage in the range of 380V-400V in the PSU. Isolated dc-dc converters are used to step down voltages for further distribution to loads. The overall system efficiency without any

redundancy when operated in high load condition is typically around 50%. The system efficiency can be increased to 70% by using high efficiency and high power density components with increase in component costs.

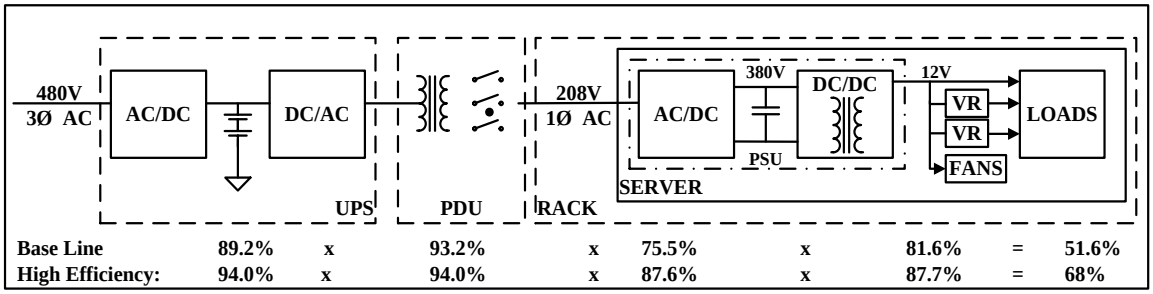

Figure 1. Conventional 480Vac architecture.

In the rack-level dc architecture (shown in Figure 2) the ac-dc converter is moved from the PSU of the server to the rack, thus reducing the cooling requirement for the servers. The server volume is thus reduced and the whole consolidated rack has higher power density and improved light load efficiency. Since the number of conversion stages is the same as the conventional ac architecture, the overall system efficiency is not expected to improve any further. If the dc voltage is increased from 48V to 380-400V, then the system efficiency can be slightly increased by using non-isolated and more efficient ac-dc converter.

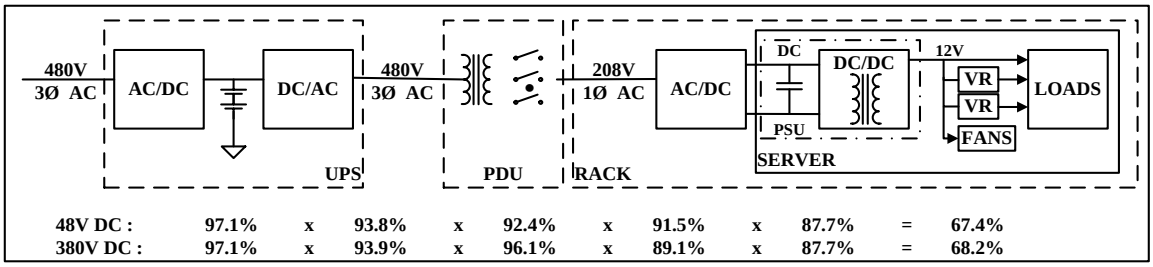

Figure 2. Rack-level dc architecture.

In the facility-level dc architecture as shown in Figure 3, the dc-ac conversion stage in the UPS and the ac-dc conversion stage in the PSU of the server are removed. Again the transformer in the PDU is also not required . Since the number of conversion stages are reduced, the power delivery efficiency is increased significantly. The efficiency can be further increased by using higher dc voltages. The copper losses are higher for a 48Vdc system compared to 380V/400V dc system. Low voltage systems have to distribute power at high currents which limit the efficiency of the system.

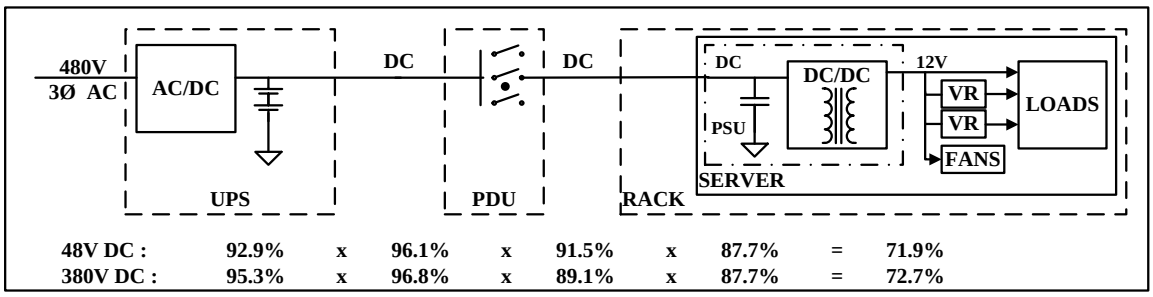

Figure 3. Facility-level dc architecture.

For residential buildings and homes, the so called ac and dc nanogrid architectures can be used where the renewable energy sources and storage systems are integrated along with the existing power grid [14]. It has been envisioned that future homes would be self-sustainable with a mix of renewable and alternative energy sources like wind, solar, generators, micro-turbines, and batteries along with the utility grid. Figure 4 shows one such ac nanogrid architecture for residential applications where plug in hybrid electric vehicles (PHEVs) are also going to be part of the scheme in the near future. It will have an energy control center (ECC) that would monitor the power flow and would communicate with the utility grid for energy trading that would eventually reduce the cost of energy by reducing the energy consumption from the utility grid during peak hours. It will also have smart metering and can remotely control the breakers.

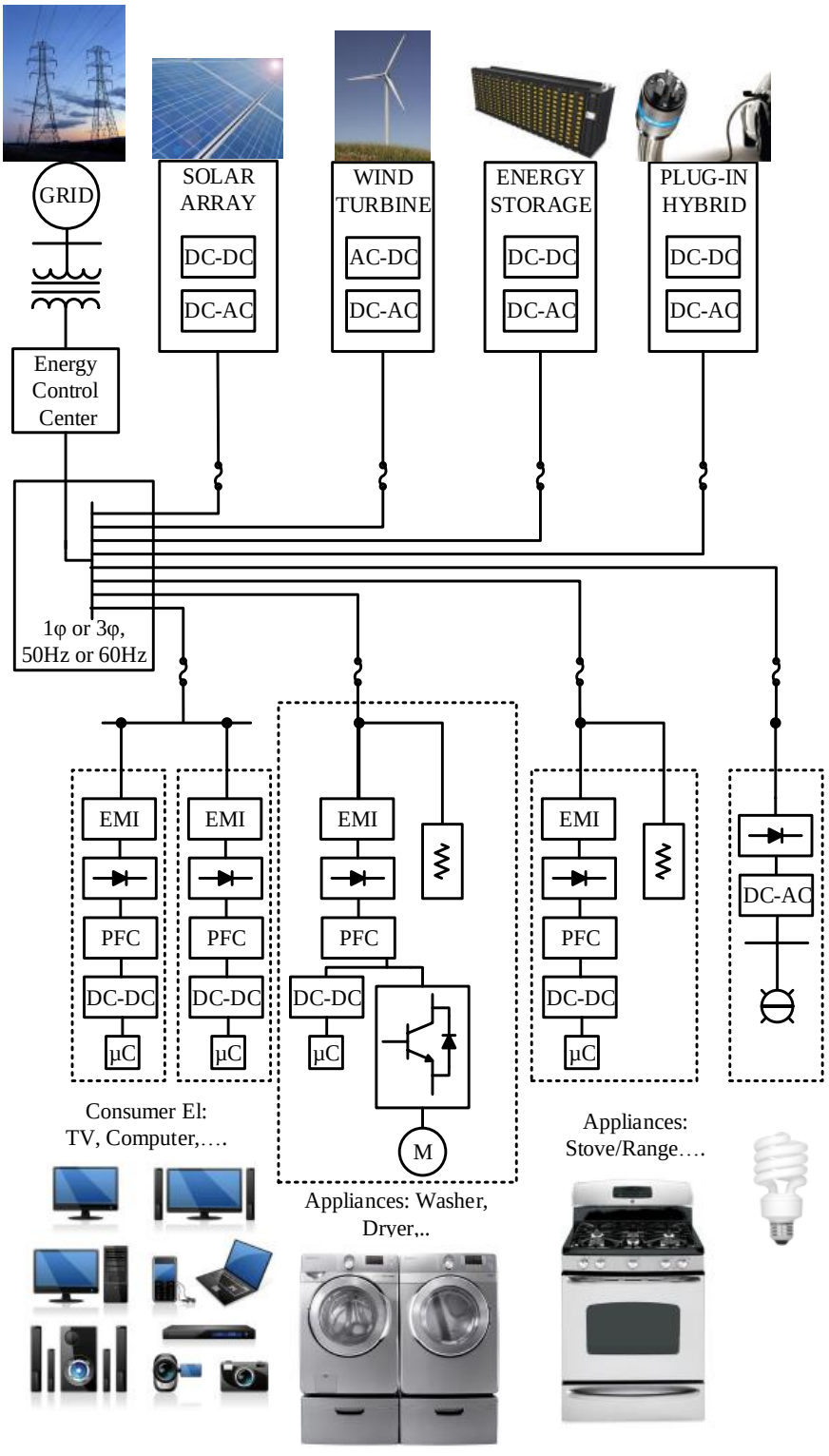

Figure 4. Ac nano grid for residential homes.

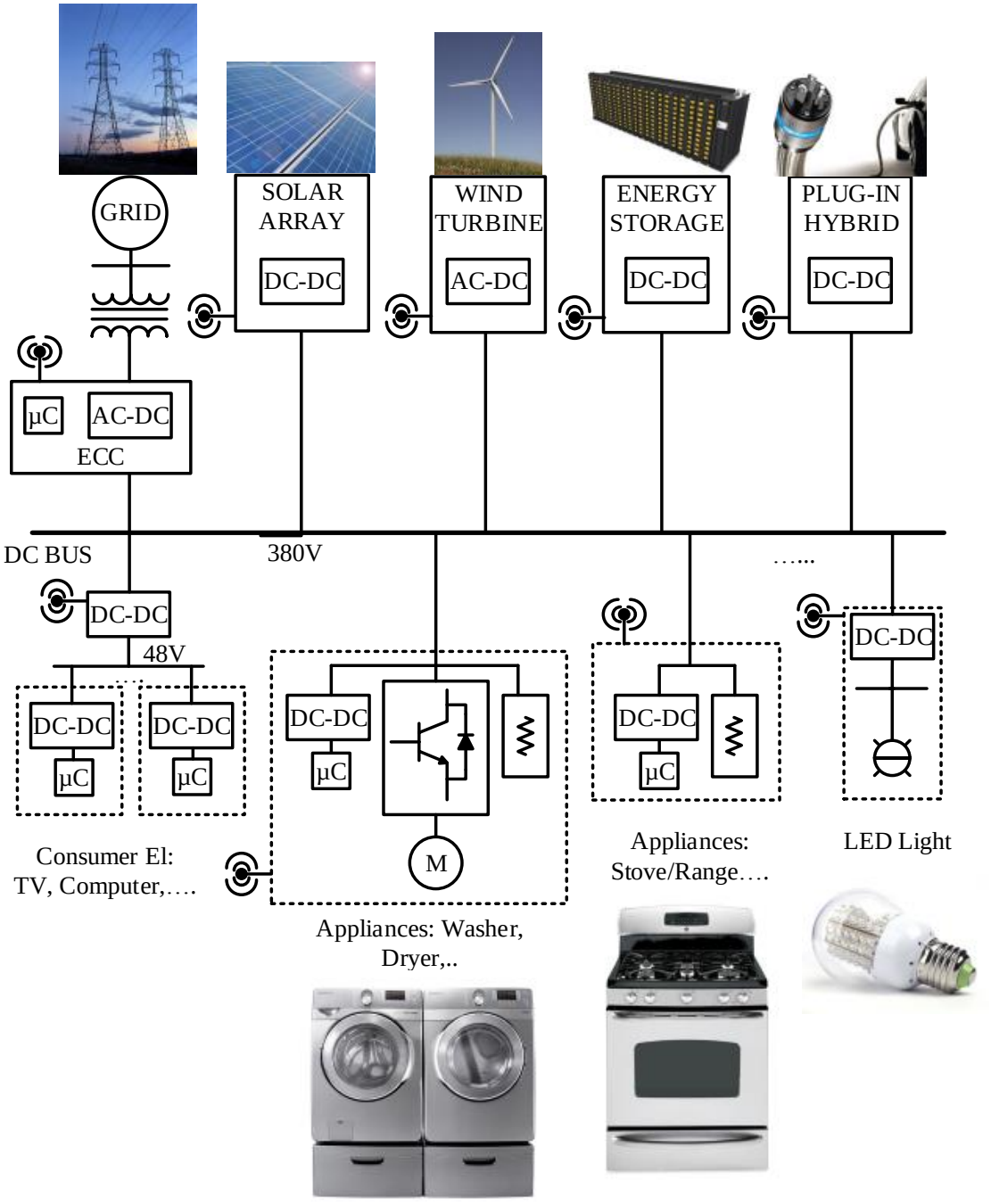

Figure 5. Dc nano grid for residential homes.

Another architecture that has been reported extensively is the dc nanogrid (shown in Figure 5) architecture for homes and future buildings [14]. Dc systems have inherent advantages over ac system like high overall efficiency, easier integration of renewable energy sources and energy storage systems. Moreover there is no reactive power and frequency stabilization issues which results in reduced copper losses. Many loads like LED lighting systems, consumer electronics, and appliances using variable speed motor drives can be easily powered by dc distribution systems.

In dc distribution systems, the dc voltage level should be selected to maximize the efficiency and reliability and to reduce the costs and increase the flexibility of the system for future expansion. Conventional dc distribution systems for telecom and data centers operate at 48 Vdc. Higher system voltages is preferred for the aforementioned factors but there are challenges like safety and protection that can lead to fire hazards. Again reliability of system is also affected as the voltage and current stresses are increased on the components as it increases the risk of component failure.

In [27], it has been reported that Telecom New Zealand deployed a 220 Vdc system to replace the existing 50 Vdc system for increased power capacity. The new system has reportedly reduced the installation costs and copper costs. The proposed system uses 30-40% smaller batteries and maximizes available floor space. In [32], for a 220 V single-phase supply or 380 V three-phase system, the dc bus is chosen ±110 V with a grounded center tap as shown in Figure 6. The dc bus voltages are selected such that the existing electric appliances can be used in the proposed dc system with little modifications.

In [33], the $(DC)^2$ concept has been introduced for dc integrated data centers which has higher efficiency and reliability compared to ac systems. The distribution bus voltage of the proposed system is in the range of 500-550 Vdc with distributed energy sources that increase the reliability of the system. The improved efficiency decreases the power required for the cooling systems and hence there is 21% savings in total energy consumption compared to ac systems.

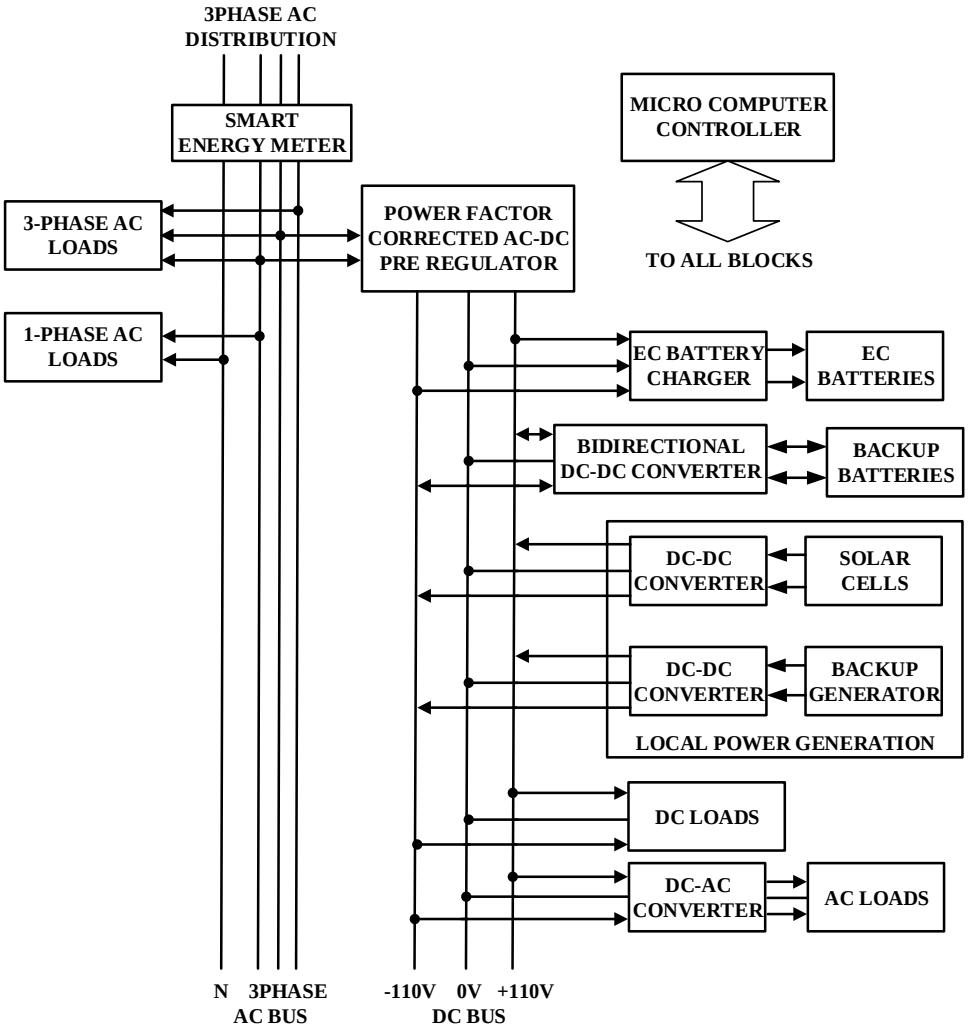

Figure 6. ±110V dc power system for residential homes.

Studies show that the dc voltage level of 380 V is an ideal voltage considering the number of battery cells that are required to be connected for energy storage system, availability of components with suitable ratings, and in terms of safety (see Figure 7). Electric Power Research Institute (EPRI) demonstrated a prototype 380 Vdc system that has 7% improved efficiency compared to the state-of-the-art ac power distribution [34].

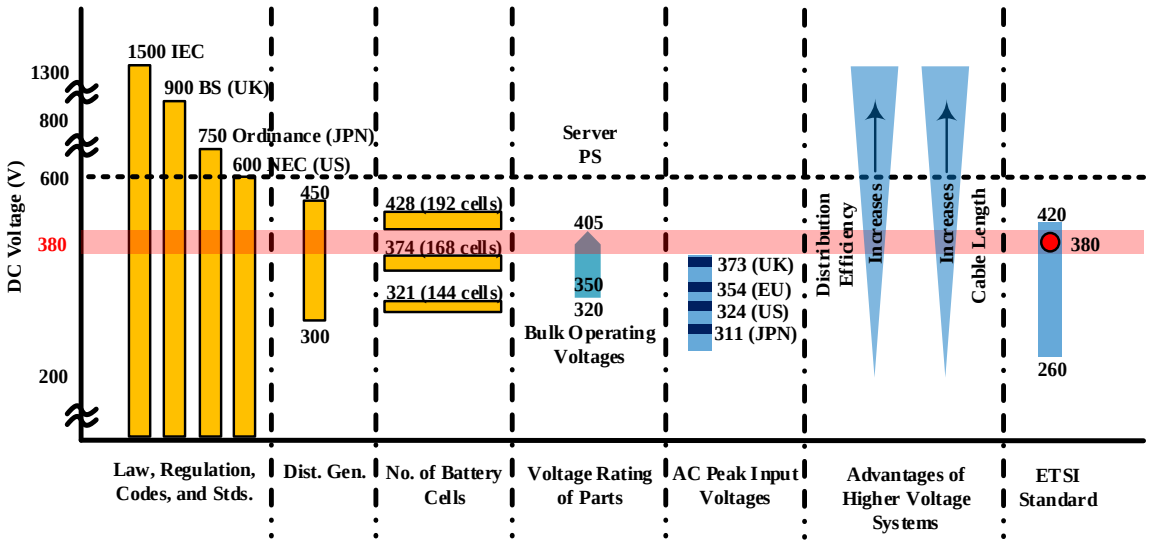

Figure 7. DC bus voltage level selection.

III. Reliability

The reliability of a dc system depends on its system architecture and redundancies resulting in component failure. Increasing the system voltage adversely affects the voltage and current stresses experienced by the switching components and thereby reducing the reliability of the system. Switching components like MOSFETs and diodes should always be operated within their safe operating area. Hence they are selected

considering a factor of safety so that there are enough margins to take care of the voltage and current transients, which may result in the failure of these components. If the operating voltages/currents are more than its rating during transients, the electrical stress on the component will lead to breakdown and result in its failure.

It has been observed that an increase in the main bus voltage reduces the life of the capacitors [35]. The lifetime of electrolytic capacitors is calculated using

$$L = L_0 \times M_v \times 2^{\left(\frac{T_{core,\max} - T_{core}}{10}\right)} \quad (1)$$

where, L is the lifetime (hours), L_0 is the base lifetime at maximum core temperature (hours), T_{core} and $T_{core,max}$ are the normal and maximum operating temperatures of the core respectively ($^{\circ}C$), and M_v is the voltage multiplier, which is the ratio of applied dc voltage to the rated dc voltage. When capacitors are subjected to higher stress levels, the core temperature is close to its maximum temperature which causes degradation and results in reduced life of the capacitor. DC systems with higher voltages require smaller capacitances because for the same amount of power the capacitance is inversely proportional to the square of voltage. Thus capacitors are selected with sufficient voltage ratings to account for increase in the dc bus voltage without reducing the reliability of the system. Also, series-parallel combination of capacitors can be employed to improve system reliability.

If batteries are used for energy storage system, a more number of battery cells is required to be connected in series to attain the required voltage. This leads to reduced system reliability as failure in any one cell in the string of cells would result in failure of the whole battery pack.

IV. COST

Higher dc bus voltage improves the system efficiency thus reducing the operational costs of the system. The amount of copper required to limit the copper losses decreases with increasing voltage, and is inversely proportional to the square of the voltage. Thus the copper costs are reduced as conductors with smaller cross-sectional areas can be used. The cabling and installation costs are reduced as the conductors are flexible and easy to lay. Conductor costs may be between 10 to 15% of the total hardware cost and the savings associated by increasing the dc bus voltage can represent less than 5% of the total hardware costs [28]. Higher voltages require elaborate protection schemes which require costly fusing, wiring and non-standard connectors that can offset the savings. Again the capacitors required should also have higher voltage ratings which are expensive. Thus these design factors cause some offset in the savings.

In [28], it has been shown that the cost of a 270 Vdc system is 15% lower than that of a 48 Vdc system. Due to lower number of conversion stages, the equipment cost is reduced. Again, the cabling costs are also lower compared to the 48 Vdc system since smaller diameter wires are used. The battery cost is higher for the 270 Vdc system since more number of cells are connected in series. The cost breakdown for a 30 kW 270 Vdc and a 48 V dc system is shown in Figure 8.

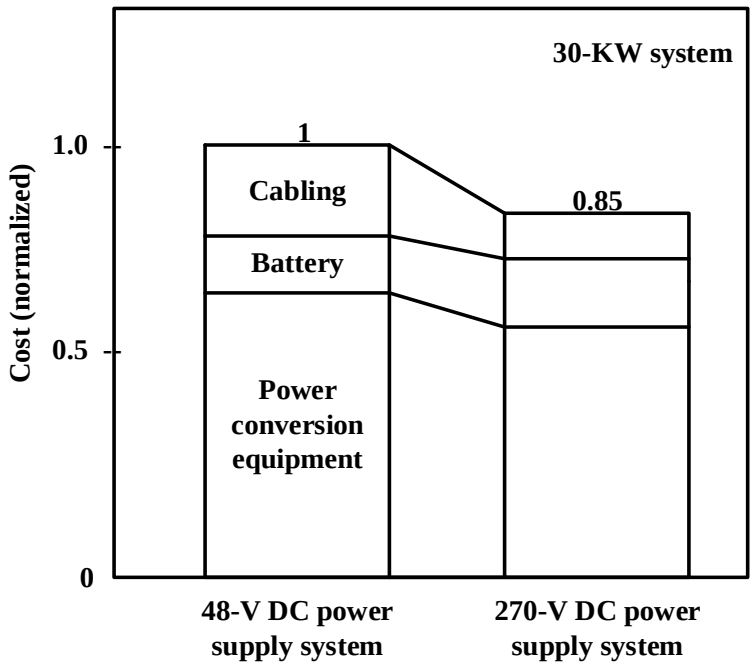

Figure 8. Cost breakdown of 48 Vdc and 270Vdc systems.

V. Safety and Protection

Dc distribution system protection is different from that of an ac system as it is difficult to break a dc current compared to an ac current. Protection devices like circuit breakers and fuses for both the ac and dc systems are similar. In case of dc systems, they have to withstand more stresses because of the persistent nature of the arc while breaking a dc current. For dc buildings and residential applications, circuit breakers can be used instead of fuses as it can be reset when the fault is cleared. Again the voltage and current rating of the circuit breaker is lower for a dc system compared to an ac system. Same components can be used for protection both on the ac and the dc side. In addition, in the event of short circuits, individual converters will have the short circuit protection and can

be easily detected by observing the dc bus voltage. If the dc bus voltage is below a certain threshold, the controller can signal a short circuit and shut down the system.

Dc distribution systems for data centers and commercial buildings require special plug and socket which should provide arc extinction, prevent electric shocks, and mechanical locks for human safety. The Nippon Telegraph and Telephone Corporation and Fujitsu Component Limited have developed a 400 Vdc, 10 A plug and socket (shown in Figure 9) that can be used for integration with the dc distribution system [36]. When a dc current is cut off, then there is an arc generated that can damage the equipment or can be lead to fatal injuries. To prevent that, the plug should not be taken from the socket when the power supply is on, but there can be instances when the plug is removed from the socket accidentally or during emergencies when the power in still on. During those cases, arc extension and shock prevention should be done by the plug and socket.

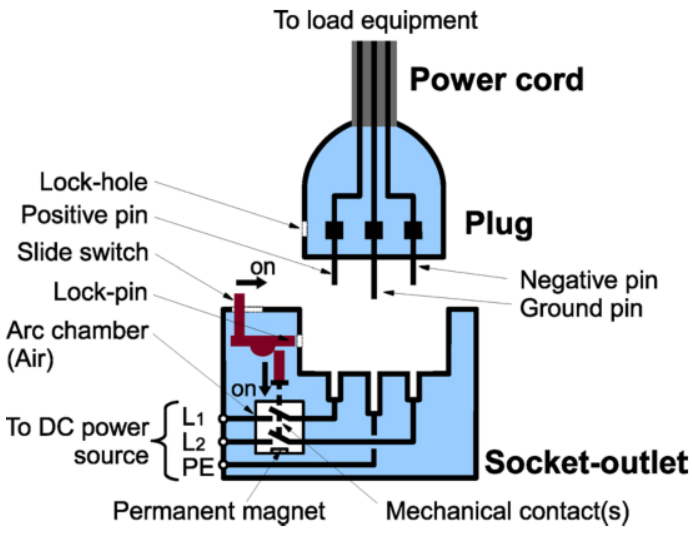

Figure 9. Configuration of plug and socket outlet for a dc system [36].

VI. Efficiency Improvement

In [18], a 380 Vdc modified power delivery architecture (shown in Figure 10) for server applications has been proposed which is more efficient than the conventional 48 Vdc system. In the modified power delivery architecture, the efficiency is increased by reducing the number of power conversion stages and placing isolated dc-dc converters close to the load. High efficiency resonant topologies such as the LLC resonant topology is used for the dc-dc conversion stage with high power densities. Also in [23-24], several multi-input dc-dc converter topologies have been introduced where various storage systems and energy sources such as renewable sources can be integrated to achieve high power density and efficiency.

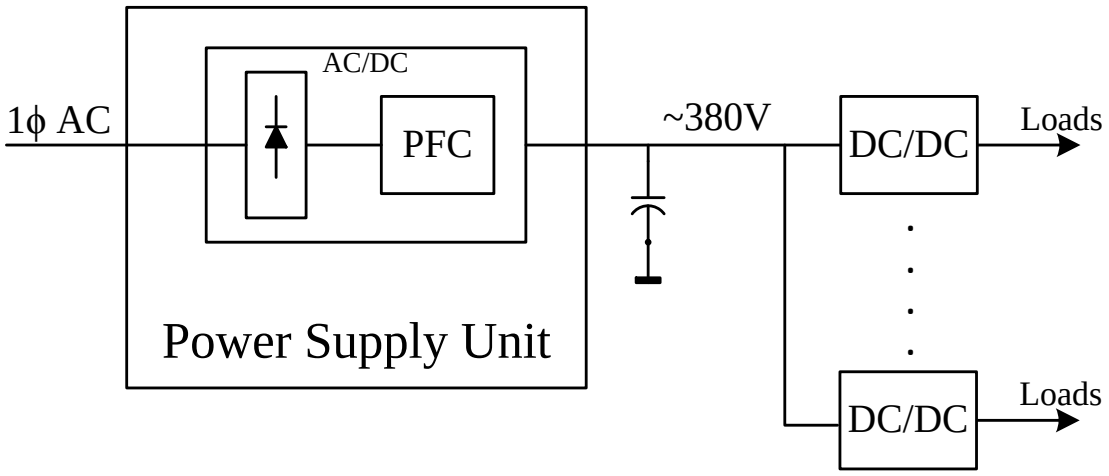

Figure 10. 380 Vdc power delivery architecture for server applications.

VII. Conclusion

Dc distribution has advantages like improved efficiency and reduced costs compared to ac distribution. Major applications of dc distribution systems are in the field of telecommunications, data centers, dc buildings, and microgrids. In current scenario, several challenges exist that need to be addressed before the dc distribution system can be used for commercial purposes. One major challenge is selecting a suitable voltage level that makes the system more efficient and reliable. Studies till date propose that a 380 Vdc system has both higher reliability and efficiency. Another critical challenge is the advancement in safety and protection technology for dc systems. Therefore, a suitable industry standard is needed to be developed to make such systems more compatible and ready to integrate with existing power systems.

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II. A MULTIPORT DC-DC CONVERTER WITH HIGH VOLTAGE GAIN

***Abstract*—**A family of non-isolated high-voltage-gain dc-dc power electronic converters is proposed. The suggested topologies can be used as multiport converters and draw continuous current from two input sources. They can also draw continuous current from a single source in an interleaved manner. This versatility makes them appealing in renewable applications such as solar farms. The proposed converters can easily achieve a gain of 20 while benefiting from a continuous input current. Such a converter can individually link a PV panel to a 400-Vdc bus. The design and component selection procedures are presented. A 400-W prototype of the proposed converter with V_{in} = 20 V and V_{out} = 400 V has been developed to validate analytical results.

I. INTRODUCTION

With increased penetration of renewable energy sources and energy storage, high gain dc-dc power electronic converters find increased applications in green energy systems. They can be used to interface low voltage sources like fuel cells, photovoltaic (PV) panels, batteries, etc. to the 400-V bus in a dc microgrid system (shown in Figure 1) [1-3]. They also find applications in different types of electronic equipment such as high-intensity-discharge (HID) lamps for automobile headlamps, servo-motor drives, X-ray power generators, computer periphery power supplies, and uninterruptible power supplies (UPS) [4].

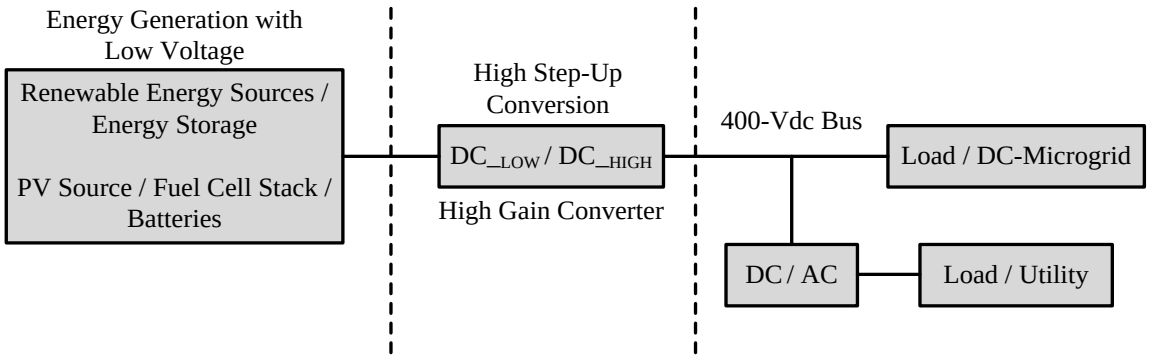

Figure 1. High gain dc-dc converter in dc-microgrid system.

To achieve high voltage gains, classical boost and buck-boost converters require large switch duty ratios. Large duty cycles result in high current stress in the boost switch. The maximum voltage gain that can be achieved is constrained by the parasitic resistive components in the circuit and the efficiency is drastically reduced for large duty ratios. There are diode reverse recovery problems because the diode conducts for a short period of time. Also the high current and output voltage along with large current ripples would further degrade the efficiency of the converter [5]. Typically high frequency transformers or coupled inductors are used to achieve high voltage conversion ratios [6-15]. The transformer design is complicated and the leakage inductances increase for achieving larger gains, as it requires higher number of winding turns. This leads to voltage spikes across the switches and voltage clamping techniques are required to limit voltage stresses on the switches. Consequently, it makes the design more complicated.

To achieve high voltage conversion ratios, a new family of high gain dc-dc power electronic converters has been introduced. The proposed converter can be used to draw power from two independent dc sources as a multiport converter [16, 17] or one source in an interleaved manner. They draw continuous input current from both the input sources

with low current ripple which is required in many applications, e.g., solar. Several diode-capacitor stages are cascaded together to boost up the voltage which limits the voltage stresses on the switches, diodes and capacitors. Due to advantages listed above theses converters are good solutions to integrate solar panels into a dc microgrid. In conventional approaches as the output voltage of PV panel is low, several panels are connected in series when connecting the PV array to the 400-Vdc bus through conventional step-up converters. This results in reduced system reliability which can be addressed by connecting high gain converter to each individual PV panel. Moreover, since it is a multi-port converter with a high voltage gain, independent sources can be connected and power sharing, MPPT algorithms etc. can be implemented independently at each input port.

Similar converters with interleaved boost input have been proposed earlier using the Cockcroft-Walton (CW) voltage multiplier [18, 19]. Current fed converters are superior in comparison to the voltage fed counterparts as they have lower input current ripple [19]. The limitation with the CW based converters is that the output impedance increases rapidly with the number of multiplying stages [20]. The efficiency and the output voltage regulation of these converters depend on the output impedance, thus for high gains the converter efficiency would be affected.

In this paper, a topology is proposed which can easily achieve a gain of 20 while benefiting from a continuous input current. Such a converter can individually link a PV panel to a 400-Vdc bus. In Section II the proposed converter topology is introduced and different modes of operation are explained. In Section III the voltage gain of the converter is derived and an alternative topology is also explained. In Section IV current

and voltage stresses required for component selection and loss calculations along with simulation results are provided. In Section V experimental results for the prototype converter is provided and Section VI concludes the paper.

II. Topology Introduction and Modes of Operation

The proposed converter is inspired by a Dickson charge pump [20]. Diode-capacitor voltage multiplier (VM) stages are integrated with two boost stages at the input. The VM stages are used to help the boost stage achieve a higher overall voltage gain. The voltage conversion ratio depends on the number of VM stages and the switch duty ratios of the input boost stages. Figure 2 shows the proposed converter with four VM stages. For simplicity and better understanding the operation of the converter with four multiplier stages has been explained here. Similar analysis can be expanded for a converter with N stages.

For normal operation of the proposed converter, there should be some overlapping time when both the switches are ON and also one of the switches should be ON at any given time (as shown in Figure 3). Therefore, the converter has three modes of operation.

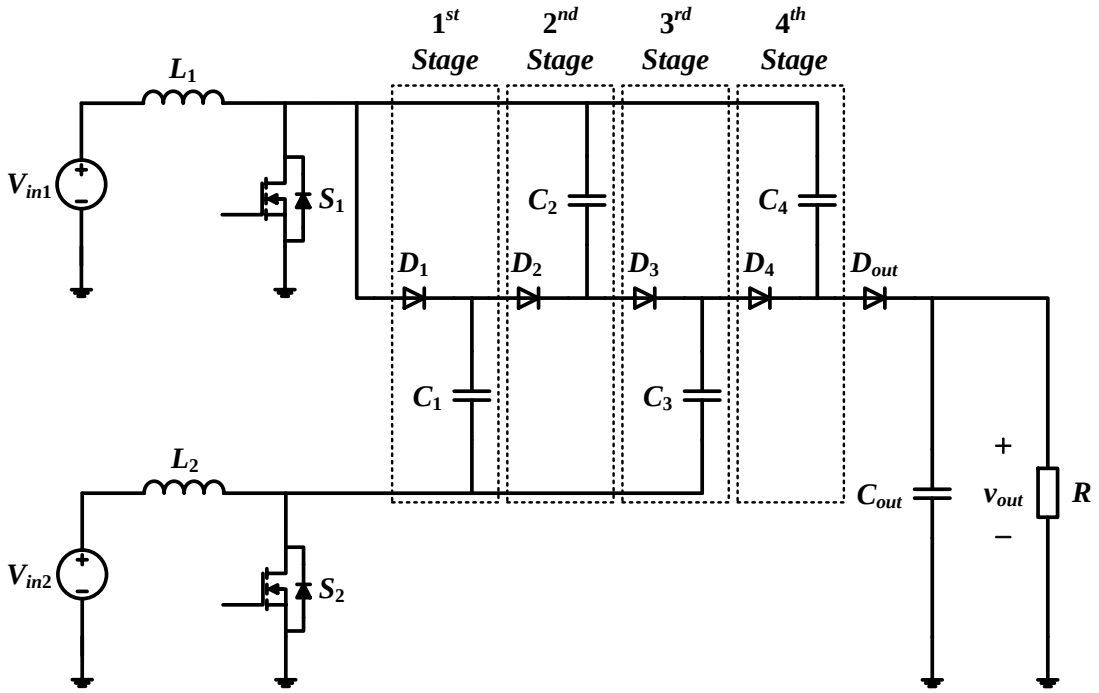

Figure 2. Proposed high gain dc-dc converter with four VM stages.

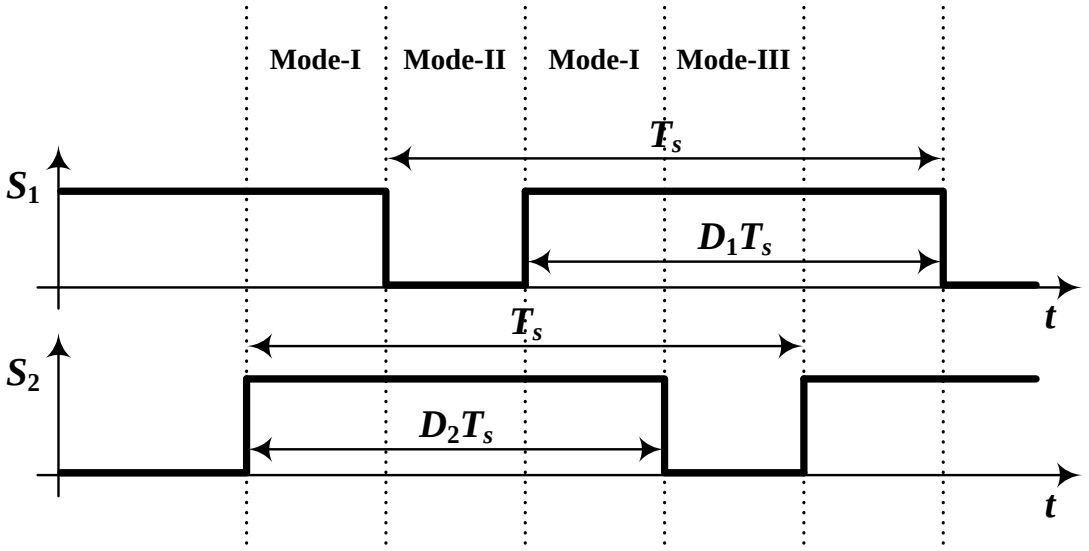

Figure 3. Switching signals for the input boost stage for the proposed converter.

A. Mode-I:

In this mode both switches S_1 and S_2 are ON. Both the inductors are charged from their input sources V_{in1} and V_{in2}. The current in both the inductors rise linearly. The diodes in different VM stages are reverse biased and do not conduct. The VM capacitor voltages remain unchanged and the output diode D_{out} is reverse biased (as shown in Figure 4), thus the load is supplied by the output capacitor C_{out}.

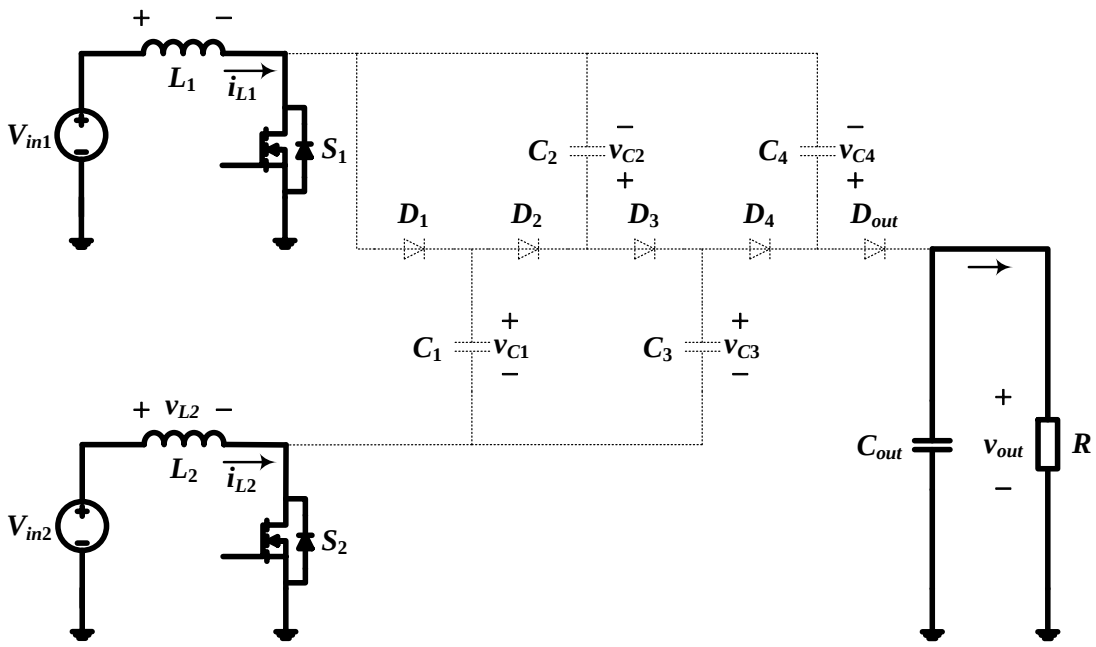

Figure 4. Mode-I of operation for the proposed converter with four VM stages.

B. Mode-II:

In this mode switch S_1 is OFF and S_2 is ON (shown in Figure 5). All the odd numbered diodes are forward biased and the inductor current I_{L1} flows through the VM capacitors charging the odd numbered capacitors (C_1, C_3, …) and discharging the even numbered capacitors (C_2, C_4, …). If the number of VM stages is odd, then the output diode D_{out} is reverse biased and the load is supplied by the output capacitor. However, if the number of VM stages is even, then the output diode is forward biased charging the output capacitor and supplying the load. In the particular case considered here, since there are four VM stages, the output diode is forward biased.

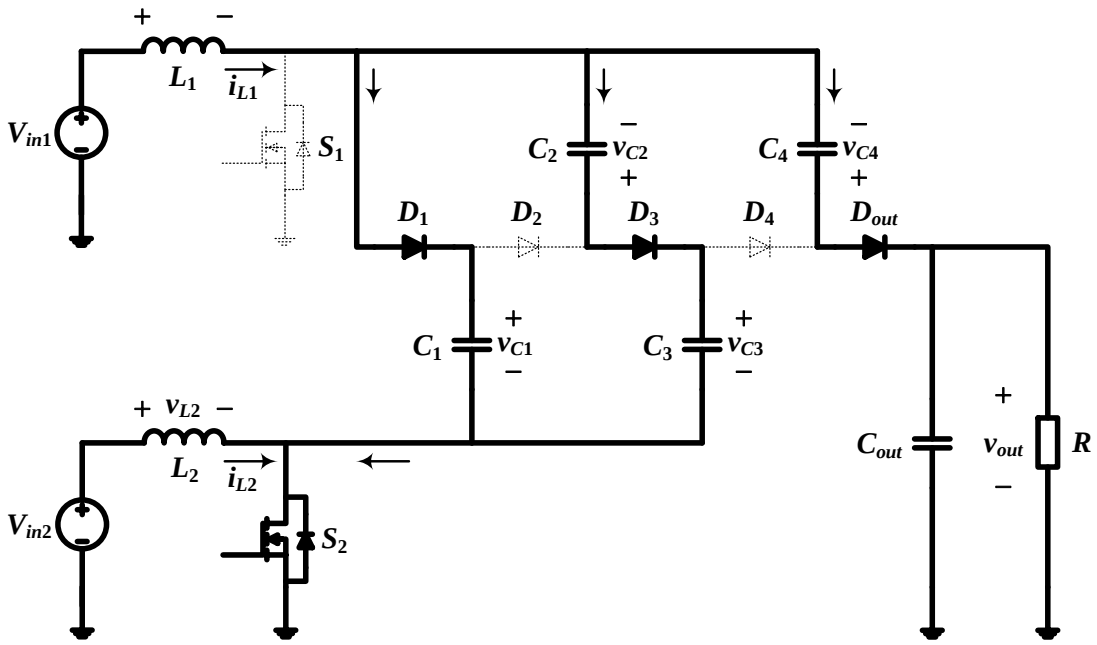

Figure 5. Mode-II of operation for the proposed converter with four VM stages.

C. Mode-III:

In this mode switch S_1 is ON and S_2 is OFF (shown in Figure 6). Now the even numbered diodes are forward biased and the inductor current I_{L2} flows through the VM capacitors charging the even numbered capacitors and discharging the odd numbered capacitors. If the number of VM stages is odd, then the output diode D_{out} is forward biased charging the output capacitor and supplying the load. However, if the number of VM stages is even, then the output diode is reverse biased and the load is supplied by the output capacitor.

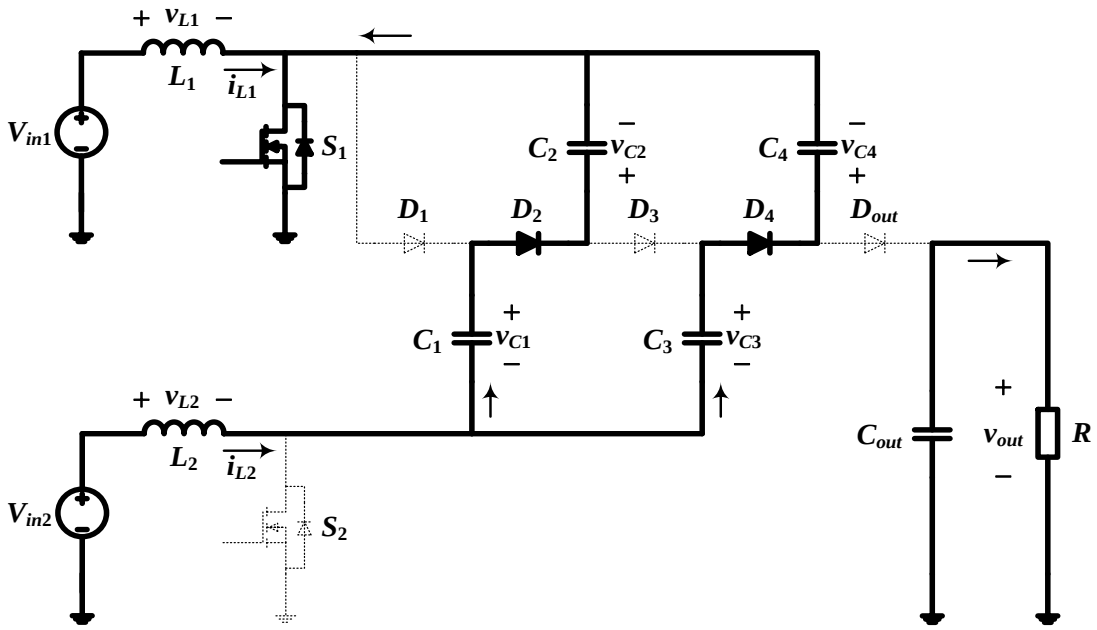

Figure 6. Mode-III of operation for the proposed converter with four VM stages.

III. Voltage Gain of the Converter

The charge is transferred progressively from input to the output by charging the VM stage capacitors. For a converter with four stages of VM (shown in Figure 2), the voltage gain can be derived from the volt-sec balance of the boost inductors. For L_1 one can write

$$\langle v_{L1} \rangle = 0 \tag{1}$$

Therefore from Figure 5, it can be observed that the capacitor voltages can be written in terms of upper boost switching node voltage as

$$V_{C1} = V_{C3} - V_{C2} = V_{out} - V_{C4} = \frac{V_{in1}}{(1-d_1)} \tag{2}$$

where d_1 is the switching duty cycle for S_1.

Similarly, from the volt-sec balance of the lower leg boost inductor L_2, one can write the capacitor voltages (shown in Figure 6) in terms of lower boost switching node voltage as

$$V_{C2} - V_{C1} = V_{C4} - V_{C3} = \frac{V_{in2}}{(1-d_2)} \tag{3}$$

where d_2 is the switching duty cycle for S_2.

From (2) and (3), the capacitor voltages for the proposed converter with four VM stages can be derived as

$$
\begin{aligned}
V_{C1} &= \frac{V_{in1}}{(1-d_1)} \\
V_{C2} &= \frac{V_{in1}}{(1-d_1)} + \frac{V_{in2}}{(1-d_2)} \\
V_{C3} &= \frac{2V_{in1}}{(1-d_1)} + \frac{V_{in2}}{(1-d_2)} \\
V_{C4} &= \frac{2V_{in1}}{(1-d_1)} + \frac{2V_{in2}}{(1-d_2)}
\end{aligned} \tag{4}
$$

The output voltage is derived from (2), which is given by

$$
\begin{aligned}
V_{out} &= V_{C4} + \frac{V_{in1}}{(1-d_1)} \\
&= \frac{3V_{in1}}{(1-d_1)} + \frac{2V_{in2}}{(1-d_2)}
\end{aligned} \tag{5}
$$

Similar analysis can be extended to a converter with *N* number of VM stages (shown in Figure 7). Thus the VM stage capacitor voltages are given by

$$
\begin{aligned}
V_{Cn} &= \left(\frac{n+1}{2}\right)\frac{V_{in1}}{(1-d_1)} + \left(\frac{n-1}{2}\right)\frac{V_{in2}}{(1-d_2)} && \text{if } n \text{ is odd} \,\&\, n \le N \\
V_{Cn} &= \left(\frac{n}{2}\right)\frac{V_{in1}}{(1-d_1)} + \left(\frac{n}{2}\right)\frac{V_{in2}}{(1-d_2)} && \text{if } n \text{ is even} \,\&\, n \le N
\end{aligned} \tag{6}
$$

The output voltage equation of the converter with *N* number of VM stages depends on whether *N* is odd or even and is given by

$$
\begin{aligned}
V_{out} &= V_{CN} + \frac{V_{in2}}{(1-d_2)} \\
&= \left(\frac{N+1}{2}\right)\frac{V_{in1}}{(1-d_1)} + \left(\frac{N+1}{2}\right)\frac{V_{in2}}{(1-d_2)}
\end{aligned} \qquad \text{if } N \text{ is odd} \tag{7}
$$

$$
\begin{aligned}
V_{out} &= V_{CN} + \frac{V_{in1}}{(1-d_1)} \\
&= \left(\frac{N+2}{2}\right)\frac{V_{in1}}{(1-d_1)} + \left(\frac{N}{2}\right)\frac{V_{in2}}{(1-d_2)}
\end{aligned} \qquad \text{if } N \text{ is even} \tag{8}
$$

When the converter operates in an interleaved manner with single input source, if d_1 and d_2 are also chosen to be identical, i.e., $d_1 = d_2 = d$, then the output voltage is given by

$$V_{out} = (N+1)\frac{V_{in}}{(1-d)} \tag{9}$$

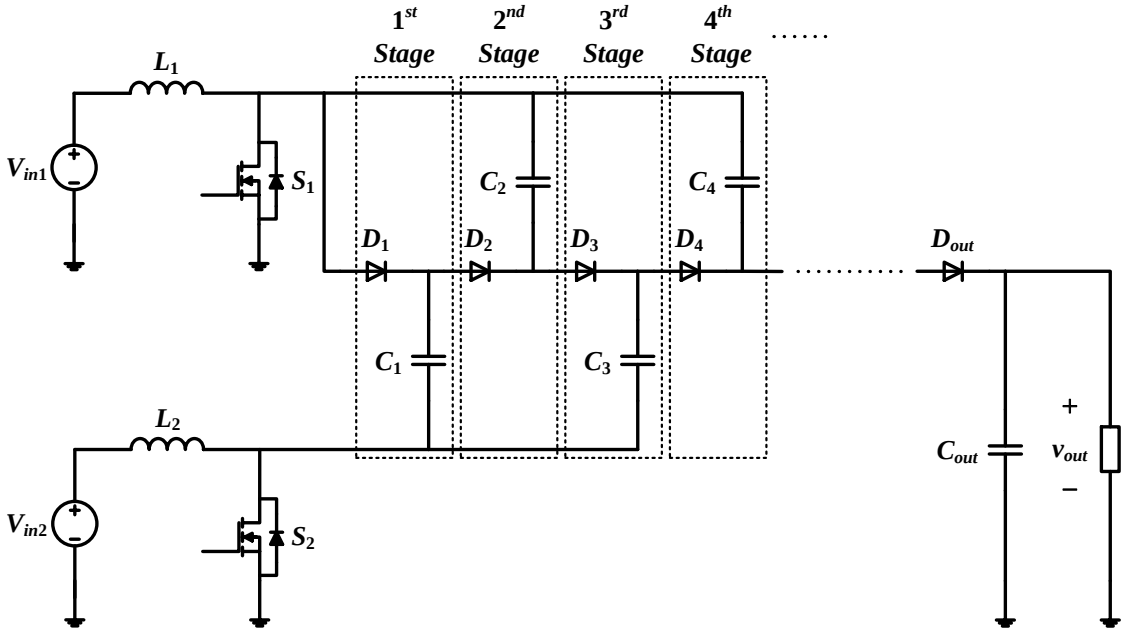

Figure 7. Proposed converter with *N* number of VM stages.

In [21], an interleaved boost power factor corrected converter with voltage-doubler characteristics is introduced. It can be observed that it is a special case of the proposed converter with a single VM stage ($N = 1$).

It is worth noting that there is an alternative to the proposed converter (shown in Figure 8) where diode D_1 of the first VM stage is connected to the lower boost switching

node and capacitor C_1 is connected to the upper boost switching node (compare with Figure 7).

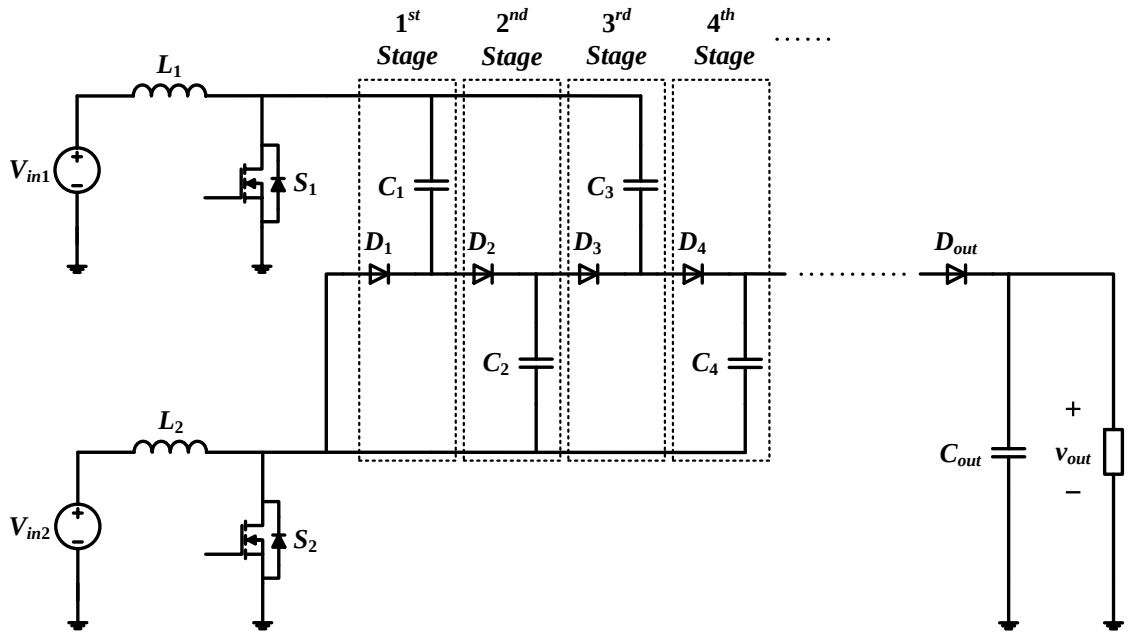

Figure 8. Alternative to the proposed converter with *N* number of VM stages.

The output voltage equation for this alternative topology is given by

$$V_{out} = \left(\frac{N+1}{2}\right)\frac{V_{in1}}{(1-d_1)} + \left(\frac{N+1}{2}\right)\frac{V_{in2}}{(1-d_2)} \qquad \text{if } N \text{ is odd} \tag{10}$$

$$V_{out} = \left(\frac{N}{2}\right)\frac{V_{in1}}{(1-d_1)} + \left(\frac{N+2}{2}\right)\frac{V_{in2}}{(1-d_2)} \qquad \text{if } N \text{ is even} \tag{11}$$

For $N = 1$, if one combines the topology depicted in Figure 7 with its alternative (see Figure 8), then the resulting converter in Figure 9 is similar to the multiphase converter introduced in [22].

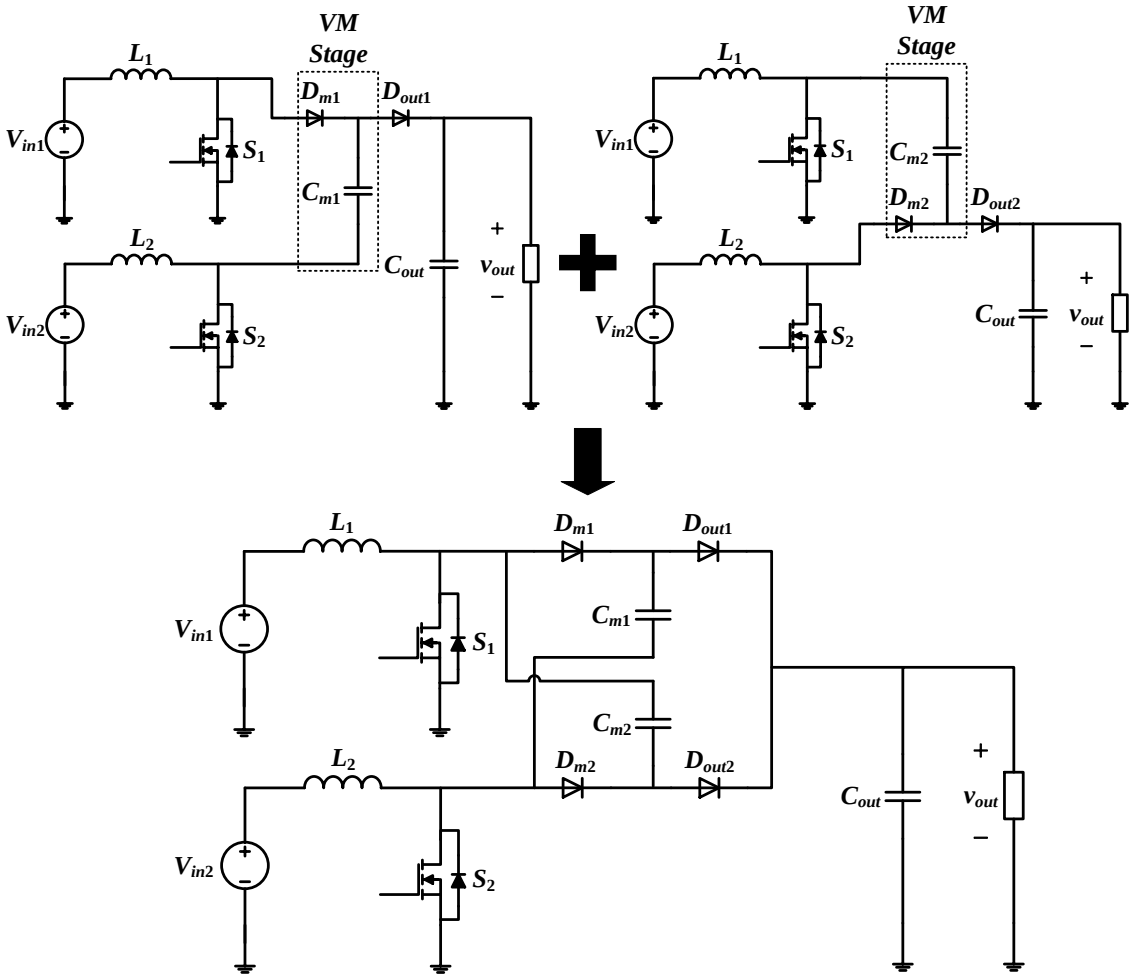

Figure 9. Combined topology with single VM stage.

In general, when both topologies with N number of VM stages are combined, then the resulting converter is shown in Figure 10. When N is odd, then from (7) and (10), the voltage gain of the combined topology is given by

$$V_{out} = \left(\frac{N+1}{2}\right)\frac{V_{in1}}{(1-d_1)} + \left(\frac{N+1}{2}\right)\frac{V_{in2}}{(1-d_2)} \quad \text{if } N \text{ is odd} \tag{12}$$

In this case, the original topology and its alternative each process half of the output power. In other words, the average currents of D_{out1} and D_{out2} are equal.

When N is even, the output voltage of the combined topology would be either (8) or (11) and will be dictated by the topology that provides a higher output voltage. Both legs (shown in Figure 10) would compete with each other and only one of the output diodes (D_{out1} and D_{out2}) would process the entire power while the other will be reverse biased. When N is even, putting the converters in parallel only makes sense if there is only one source used and $d_1 = d_2$. In that case both (8) and (11) determine the output voltage to be

$$V_{out} = (N+1)\frac{V_{in}}{(1-d)} \quad \text{if } N \text{ is even} \tag{13}$$

For the combined topology with a single input source and identical duty ratios d_1 and d_2, i.e., $d_1 = d_2 = d$, both the boost stages will always have symmetrical inductor and switch currents irrespective of the number of VM stages.

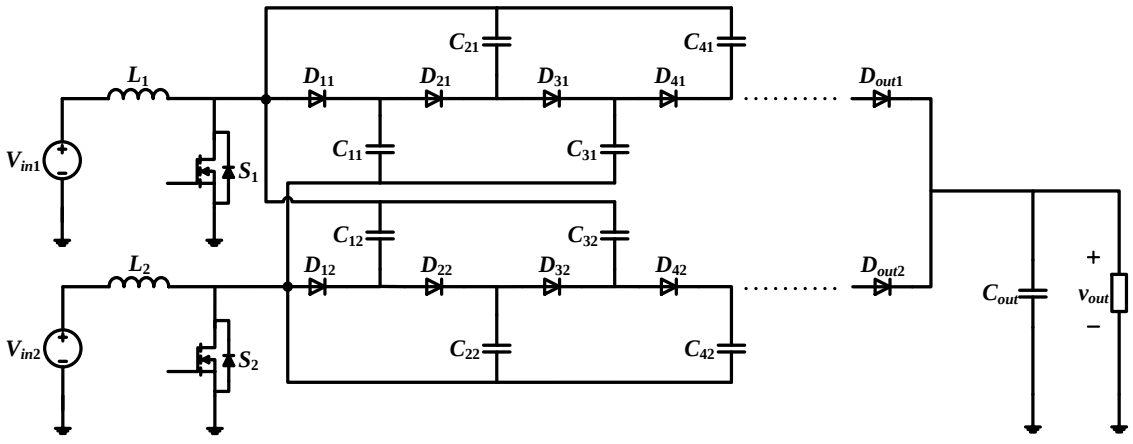

Figure 10. Combined topology with N number of VM stages.

IV. Component Selection and Simulation Results

A. Inductor Selection

The inductor currents in both the boost stages depend on the number of VM stages connected to each leg. The average inductor current in each boost stage (shown in Figure 2) is given by

$$I_{L1,avg} = \left(\frac{N+1}{2}\right)\frac{I_{out}}{(1-d_1)} \qquad \text{if } N \text{ is odd} \qquad (14)$$
$$I_{L2,avg} = \left(\frac{N+1}{2}\right)\frac{I_{out}}{(1-d_2)}$$

$$I_{L1,avg} = \left(\frac{N+2}{2}\right)\frac{I_{out}}{(1-d_1)} \qquad \text{if } N \text{ is even} \qquad (15)$$
$$I_{L2,avg} = \left(\frac{N}{2}\right)\frac{I_{out}}{(1-d_2)}$$

It can be observed from (14) and (15) that for a converter with single input source and identical duty ratios d_1 and d_2, when N is odd, then both boost stages have equal average inductor currents (shown in Figure 11(a)). Whereas when the N is even, then $I_{L1,avg}$ is larger than $I_{L2,avg}$ as observed in Figure 11(b).

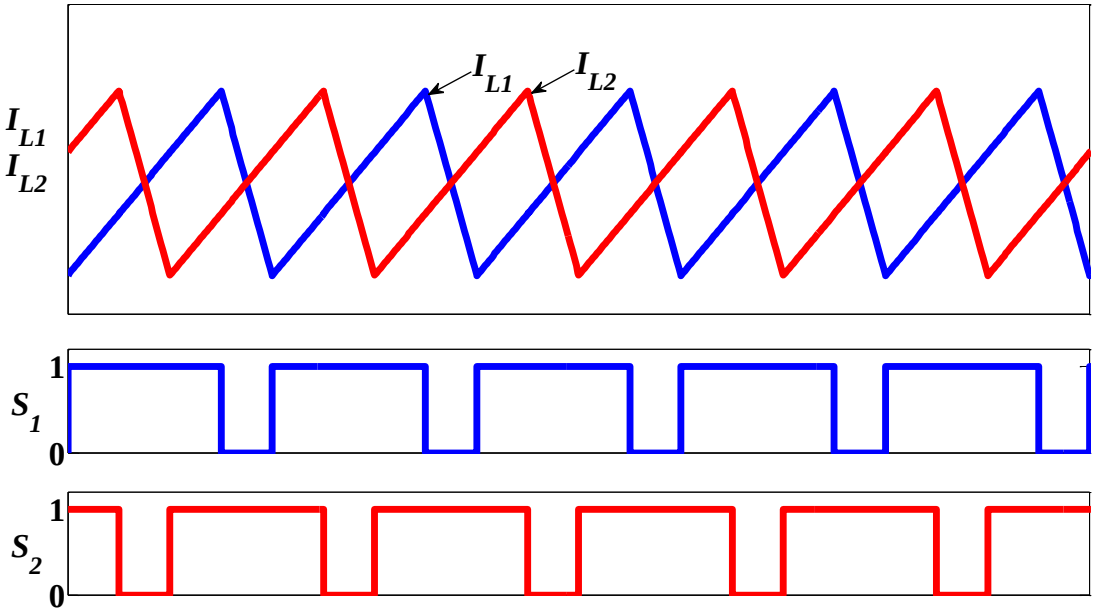

Figure 11(a). Inductors currents for odd number of VM stages.

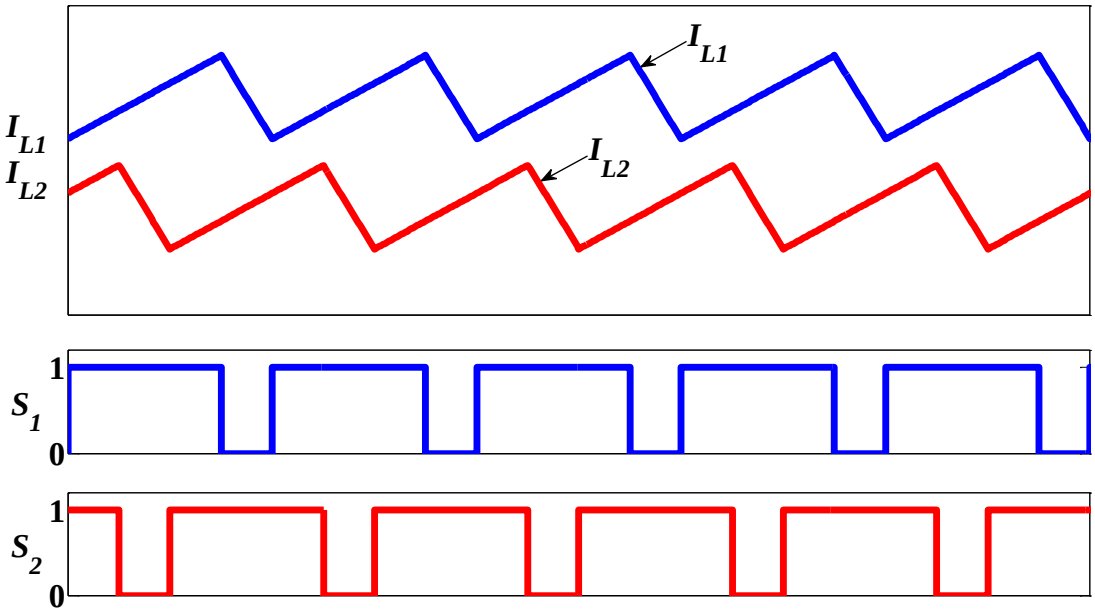

Figure 11(b). Inductors currents for even number of VM stages.

The inductor design is similar to that of the normal boost converter. The inductor value is selected such that both the boost stages operate in continuous conduction mode (CCM). The minimum inductor value for the CCM operation of both the boost stages is given by

$$L_{1,crit} = \frac{V_{in1} d_1 (1-d_1)}{(N+1) I_{out} f_{sw}} \qquad \text{if } N \text{ is odd} \qquad (16)$$
$$L_{2,crit} = \frac{V_{in2} d_2 (1-d_2)}{(N+1) I_{out} f_{sw}}$$

$$L_{1,crit} = \frac{V_{in1} d_1 (1-d_1)}{(N+2) I_{out} f_{sw}} \qquad \text{if } N \text{ is even} \qquad (17)$$
$$L_{2,crit} = \frac{V_{in2} d_2 (1-d_2)}{N I_{out} f_{sw}}$$

The inductor values selected for the assumed ripple current is

$$L_1 = \frac{V_{in1} d_1}{\Delta I_{L1} f_{sw}} \qquad (18)$$

$$L_2 = \frac{V_{in2} d_2}{\Delta I_{L2} f_{sw}} \qquad (19)$$

The peak value of the inductor currents is given by

$$I_{L1,pk} = \frac{(N+1) I_{out}}{2(1-d_1)} + \frac{V_{in1} d_1}{2 L_1 f_{sw}} \qquad \text{if } N \text{ is odd} \qquad (20)$$
$$I_{L2,pk} = \frac{(N+1) I_{out}}{2(1-d_2)} + \frac{V_{in2} d_2}{2 L_2 f_{sw}}$$

$$I_{L1,pk} = \frac{(N+2) I_{out}}{2(1-d_1)} + \frac{V_{in1} d_1}{2 L_1 f_{sw}} \qquad \text{if } N \text{ is even} \qquad (21)$$
$$I_{L2,pk} = \frac{N I_{out}}{2(1-d_2)} + \frac{V_{in2} d_2}{2 L_2 f_{sw}}$$

For inductor copper loss calculation, it is important to know the rms value of the inductor currents, which can be calculated as

$$I_{L1,rms} = \sqrt{\left(\frac{(N+1)I_{out}}{2(1-d_1)}\right)^2 + \left(\frac{V_{in1}d_1}{2\sqrt{3}L_1 f_{sw}}\right)^2}$$
$$I_{L2,rms} = \sqrt{\left(\frac{(N+1)I_{out}}{2(1-d_2)}\right)^2 + \left(\frac{V_{in2}d_2}{2\sqrt{3}L_2 f_{sw}}\right)^2} \quad \text{if } N \text{ is odd} \tag{22}$$

$$I_{L1,rms} = \sqrt{\left(\frac{(N+2)I_{out}}{2(1-d_1)}\right)^2 + \left(\frac{V_{in1}d_1}{2\sqrt{3}L_1 f_{sw}}\right)^2}$$
$$I_{L2,rms} = \sqrt{\left(\frac{NI_{out}}{2(1-d_2)}\right)^2 + \left(\frac{V_{in2}d_2}{2\sqrt{3}L_2 f_{sw}}\right)^2} \quad \text{if } N \text{ is even} \tag{23}$$

B. MOSFET Selection

The peak blocking voltage of both the switches is similar to that of the normal boost converter (shown in Figure 2) which is given by

$$V_{S1} = \frac{V_{in1}}{(1-d_1)} \tag{24}$$

$$V_{S2} = \frac{V_{in2}}{(1-d_2)} \tag{25}$$

The current stresses on both the switches depend on the number of VM stages. The average current through the switches is given by

$$I_{S1,avg} = \left(\frac{(N+1)d_1}{2(1-d_1)} + \frac{(N-1)}{2} \right) I_{out}$$
$$I_{S2,avg} = \left(\frac{(N+1)d_2}{2(1-d_2)} + \frac{(N+1)}{2} \right) I_{out} \quad \text{if } N \text{ is odd} \tag{26}$$

$$I_{S1,avg} = \left(\frac{(N+2)d_1}{2(1-d_1)} + \frac{N}{2} \right) I_{out}$$
$$I_{S2,avg} = \left(\frac{Nd_2}{2(1-d_2)} + \frac{N}{2} \right) I_{out} \quad \text{if } N \text{ is even} \tag{27}$$

From (26) and (27), for a converter with single input source and identical duty ratios d_1 and d_2, it can be observed that when N is odd, the average current through S_2 is greater than S_1 (seen in Figure 12(a)). When N is even, the average current through S_1 is greater than S_2 (as can be seen in Figure 12(b)).

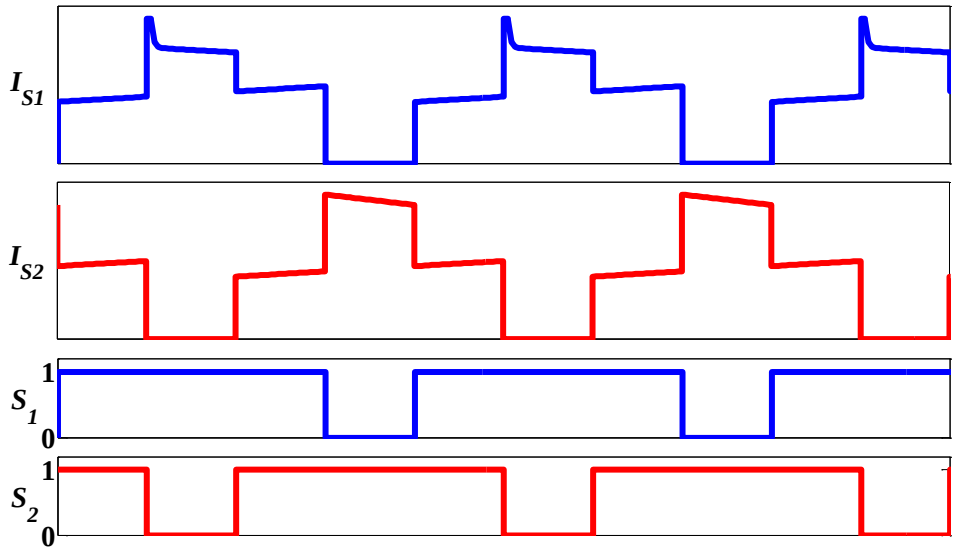

Figure 12(a). Switch current for odd number of VM stages.

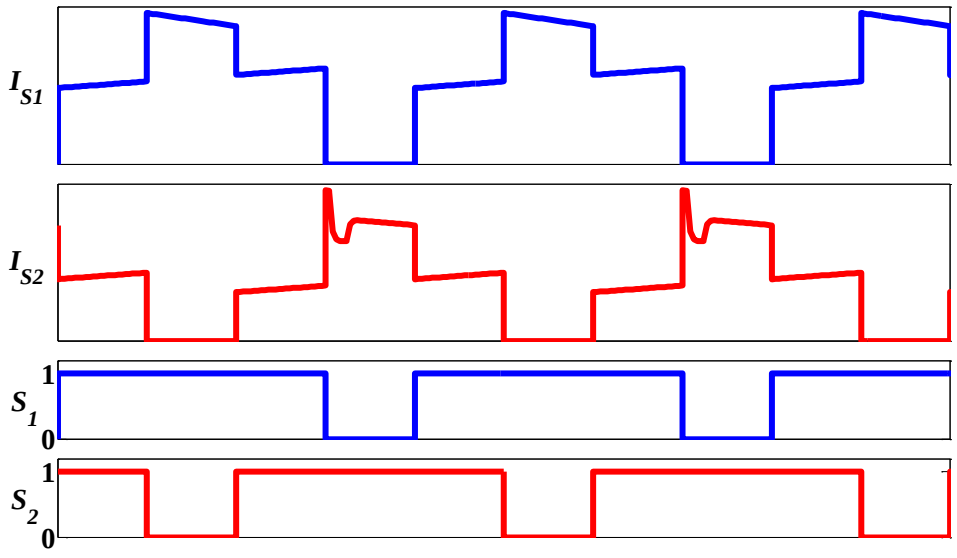

Figure 12(b). Switch current for even number of VM stages.

Also, the rms values of switch currents required for loss calculations are given by

$$I_{S1,rms} = \left(\sqrt{\left(\frac{(N+1)}{2(1-d_1)} \right)^2 (d_1 + d_2 - 1) + \left\{ \frac{(N-1)}{2(1-d_2)} + \frac{(N+1)}{2(1-d_1)} \right\}^2 (1-d_2)} \right) I_{out}$$

$$I_{S2,rms} = \left(\sqrt{\left(\frac{(N+1)}{2(1-d_2)} \right)^2 (d_2 + d_1 - 1) + \left\{ \frac{(N+1)}{2(1-d_1)} + \frac{(N+1)}{2(1-d_2)} \right\}^2 (1-d_1)} \right) I_{out}$$

if N is odd (28)

$$I_{S1,rms} = \left(\sqrt{\left(\frac{(N+2)}{2(1-d_1)} \right)^2 (d_1 + d_2 - 1) + \left\{ \frac{N}{2(1-d_2)} + \frac{(N+2)}{2(1-d_1)} \right\}^2 (1-d_2)} \right) I_{out}$$

$$I_{S2,rms} = \left(\sqrt{\left(\frac{N}{2(1-d_2)} \right)^2 (d_2 + d_1 - 1) + \left\{ \frac{N}{2(1-d_1)} + \frac{N}{2(1-d_2)} \right\}^2 (1-d_1)} \right) I_{out}$$

if N is even (29)

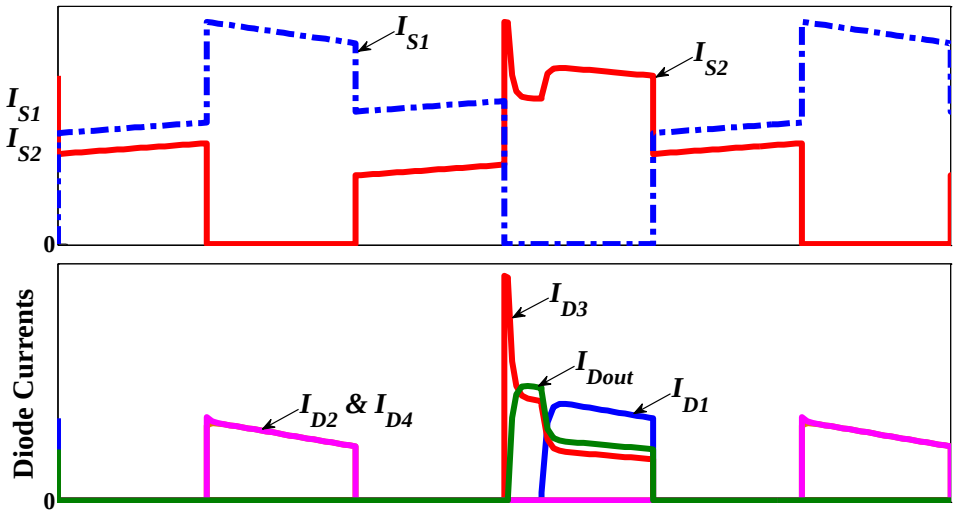

Figure 13. Switch and diode currents for the proposed converter with four VM stages.

It is observed that there is a distortion and spike in the switch current waveforms (as seen in Figs. 12(a), 12(b), and 13). The spike is observed in I_{S1} when the number of VM stages are odd. However, when the number of VM stages are even, the spike is observed in I_{S2}. The spike in switch currents is due to the voltage imbalance between VM stage capcitors. Figure 13 shows the switch and diode currents for the conveter with four VM stages (shown in Figure 2). The spike in I_{S2} appears during mode-II of operation of the converter (see Figure 5). Initially diode D_3 conducts the total inductor current I_{L1}, since v_{C3}-v_{C2} is less than v_{C1} and v_{out}-v_{C4}. When v_{C3}-v_{C2} and v_{out}-v_{C4} are both balanced, then diodes D_3 and D_{out} start conducting and share almost equal inductor current I_{L1}/2. Diode D_1 starts conducting when v_{C1}, v_{C3}-v_{C2}, and v_{out}-v_{C4} are all balanced. During this period diode current I_{D1} is greater than I_{D3} and I_{Dout} since the impedance seen by the current path is lower. The ratio between the currents is dependent on the values chosen for the VM stage capacitors. Switch current I_{S2} during this period is the sum of I_{L2}, I_{D1},

and I_{D3} and hence there is spike and distortion of the switch current. The magnitude of spike is equal to the sum of both the inductor currents I_{L1} and I_{L2}. It can be observed that the currents exhibit characteristics similar to charging/discharging of a RC circuit which is because of the parasictic resistances of the circuit such as switch $R_{DS(on)}$, inductor *DCR* and VM stage capacitor *ESR*.

C. Diode Selection

The voltage stresses across the diodes depend on the capacitor voltages as it is connected between two VM stage capacitors (shown in Figure 2). It can be observed that in mode-II of operation, when S_1 is OFF and S_2 is ON, the odd numbered diodes are forward biased and even numbered diodes are in blocking mode. Similarly, the odd numbered diodes are in blocking mode in the mode-III of operation, when S_1 is ON and S_2 is OFF (shown in Figure 14). The maximum blocking voltage of the VM stage diodes is given by

$$V_{Dn} = \frac{V_{in1}}{(1-d_1)} + \frac{V_{in2}}{(1-d_2)} \tag{30}$$

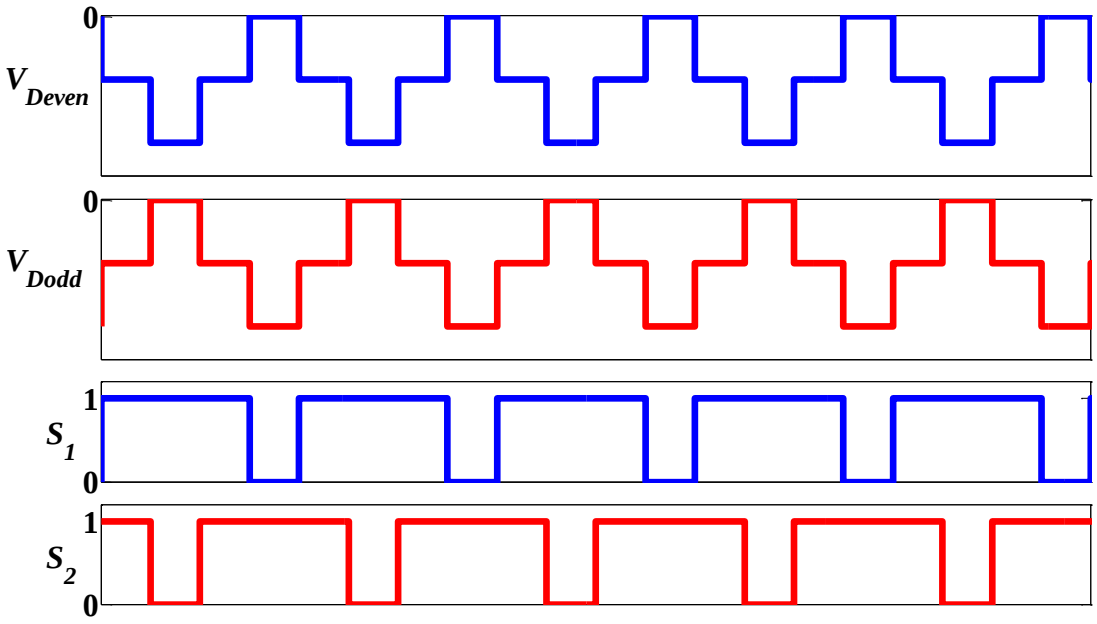

Figure 14. Diode voltages for odd and even number of VM stages.

However, the output diode conducts during mode-III of operation when there is odd number of VM stages as shown in Figure 15(a) and conducts during mode-II of operation when there is even number of VM stages as shown in Figure 15(b). The peak blocking voltage of the output diode is given by

$$V_{Dout} = \frac{V_{in2}}{(1-d_2)} \qquad \text{if } N \text{ is odd} \tag{31}$$

$$V_{Dout} = \frac{V_{in1}}{(1-d_1)} \qquad \text{if } N \text{ is even} \tag{32}$$

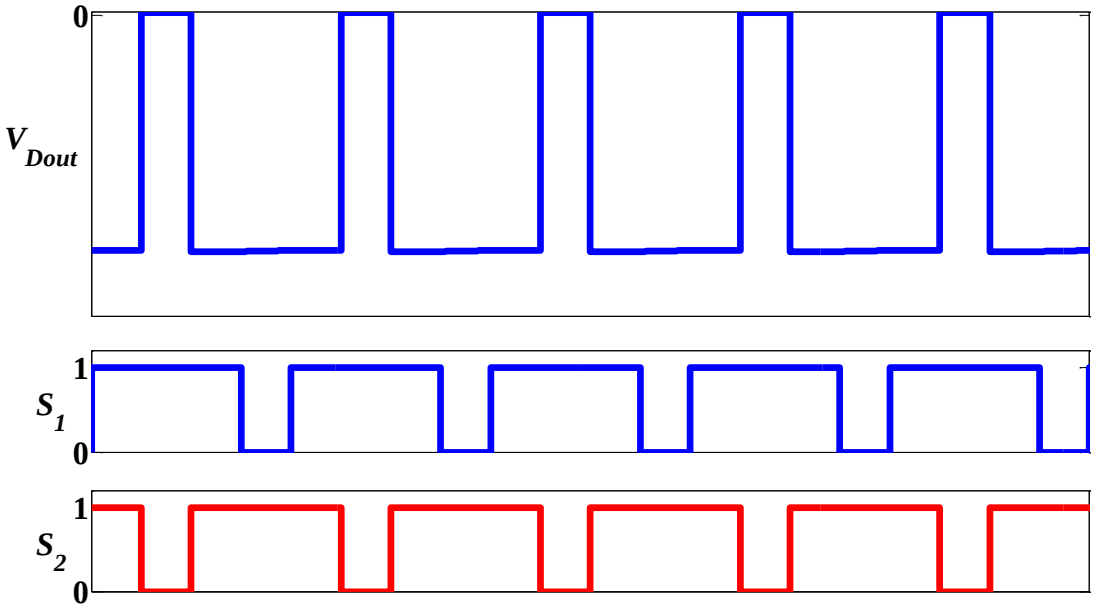

Figure 15(a). Output diode voltage for odd number of VM stages.

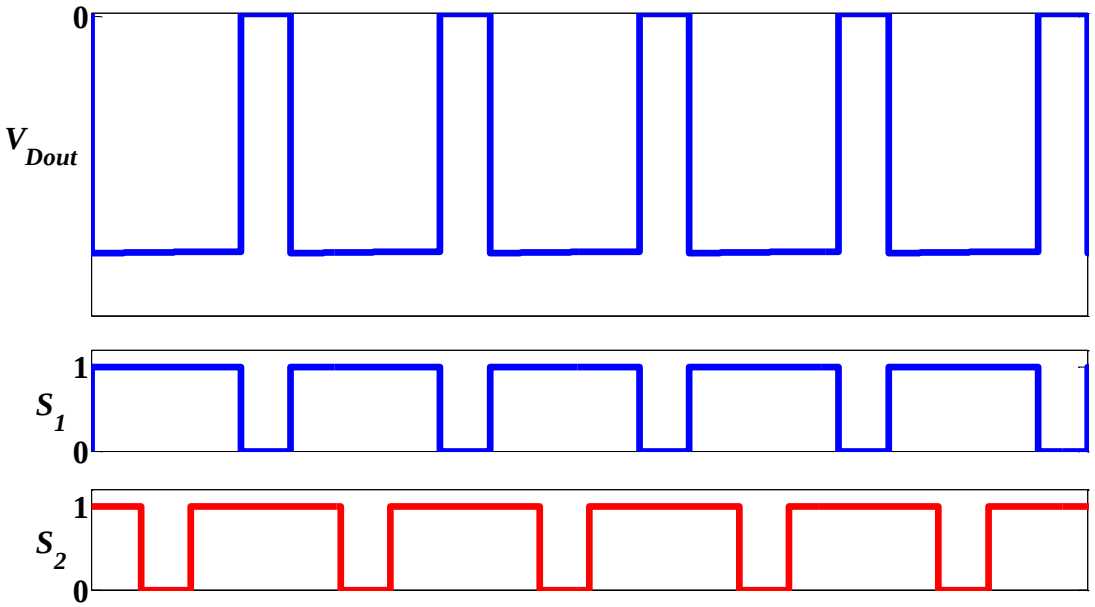

Figure 15(b). Output diode voltage for even number of VM stages.

As explained earlier, the odd numbered diodes conduct during mode-II of operation and the even numbered diodes conduct during mode-III of operation. The average and rms diode currents required for diode selection and loss calculation is given by

$$I_{Dodd,avg} = I_{Deven,avg} = I_{Dout,avg} = I_{out} \tag{33}$$

$$I_{Dodd,rms} = \sqrt{\frac{1}{1-d_1}} I_{out} \tag{34}$$

$$I_{Deven,rms} = \sqrt{\frac{1}{1-d_2}} I_{out} \tag{35}$$

$$I_{Dout,rms} = \sqrt{\frac{1}{1-d_2}} I_{out} \qquad \text{if } N \text{ is odd} \tag{36}$$

$$I_{Dout,rms} = \sqrt{\frac{1}{1-d_1}} I_{out} \qquad \text{if } N \text{ is even} \tag{37}$$

V. Experimental Results

The laboratory prototype with four VM stages and with interleaved boost input stage with a single source was built to test and validate the proposed converter operation. The components used for building the prototype is given in Table I. The converter is rated at 400 W with input voltage of 20 V and output voltage of 400 V. The switching frequency of the converter is 100 kHz.

Table I. Component List for the Experimental Prototype

Item	**Reference**	**Rating**	**Part No**
Inductor	L_1, L_2	100µH DCR = 11mΩ	CTX100-10-52LP
MOSFET	S_1, S_2	150V, 43A $R_{DS(on)}$ = 7.5mΩ	IPA075N15N3G
Diode	D_1, D_2, D_3, D_4, D_{out}	250V, 40A V_D = 0.97V	MBR40250T
Capacitor	C_1, C_2, C_3, C_4	20µF, 450V ESR = 2.2mΩ	C4ATGBW5200A3MJ
Capacitor	C_{out}	22µF, 450V	B32774D4226

The component selection is critical as it determines the output voltage regulation and the efficiency of the converter. The output capacitor is selected based on the amount of charge that is transferred to the output for desired output voltage ripple given by

$$q_{out} = C_{out}\Delta V_{out} = \frac{I_{out}}{f_{sw}}(1-d) \tag{38}$$

where d is either d_1 or d_2 based on whether the number of VM stages is even or odd. The same amount of charge q_{out} is transferred progressively by the VM stage capacitors. The VM stage capacitors for desired ripple voltage is given by

$$C_n\Delta V_{Cn} = \frac{I_{out}}{f_{sw}}(1-d) \tag{39}$$

The component selection is critical as it determines the output voltage regulation and the efficiency of the converter. The VM stage capacitors are selected such that the equivalent series output resistance due to the charging/discharging of the capacitors is reduced keeping the total capacitance to reasonable levels thus improving the efficiency and output voltage regulation. It is important to select VM stage capacitors with low *ESR* to minimize the losses, for that purpose thin film capacitors are selected as they have low *ESR* values. Furthermore, the VM stage capacitors and the output capacitor are selected based on the ripple current ratings of the capacitors. For the VM stage capacitors, the ripple current will be higher, therefore capacitor C4ATGBW5200A3MJ (20 µF, 450 V) is selected which has a ripple current rating of 29 A. Since the output capacitor has lower ripple currents, capacitor B32774D4226 (22 µF, 450 V) is selected which has a ripple current rating of 9 A. The output voltage gain and efficiency also depends on the inductor *DCR*, forward voltage drop of the diode, and the MOSFET $R_{DS(on)}$.

The losses in the proposed converter can be easily calculated based on the average and rms currents calculated in the previous section. The conduction losses in the

proposed converter have been enumerated in Table II. The switching losses in both the MOSFETs are calculated by a commonly used formula given by

$$P_{sw} = \frac{1}{2} \times I_{L,avg} \times V_S \times (t_{off} + t_{on}) + \frac{1}{2} \times f_{sw} \times C_{oss} \times V_S^2 \quad (40)$$

where $I_{L,avg}$, V_S, and f_{sw} are the inductor current, switch voltage and switching frequency respectively. While t_{on} and t_{off} are the MOSFET turn-on and turn-off switching times.

Table II. Conduction Losses for the Proposed Converter at 400 W Output Power

Description	**Loss Calculation**	**Losses (W)**
Copper Losses in L_1	$I_{L1,rms}^2 \times R_{L1}$	1.6745
Copper Losses in L_2	$I_{L2,rms}^2 \times R_{L2}$	0.7454
Conduction Losses in S_1	$I_{S1,rms}^2 \times R_{S1}$	1.3561
Conduction Losses in S_2	$I_{S2,rms}^2 \times R_{S2}$	0.7534
Diode Conduction Losses	$(N+1) \times V_f \times I_{D,avg}$	6.5029

The power loss associated with the charging/discharging of the VM stage capacitors can be calculated by calculating the series equivalent resistance [20]. When all the VM stage capacitors are assumed to be same, then the power loss is given by

$$P_C = I_{out}^2 \times \frac{N}{C \times f_{sw}} \quad (41)$$

where C is the value of the VM stage capacitors. The total power loss in the proposed converter is given by

$$P_{Loss} = P_{L1} + P_{L2} + P_{S1} + P_{S2} + P_{SW1} + P_{SW2} + P_D + P_C \quad (42)$$

The efficiency of the proposed converter calculated for 400 W output power based on the loss breakdown comes out to be 96.95% with total power loss being 12.54 W. The efficiency of the prototype was measured to be 91.4%. Figure 16 shows the efficiency of the converter at different load levels. Maximum efficiency of 94.24% is observed at the output power of 162 W. Since the simulation model only has conduction losses, in the end the switching losses calculated from (40) where added to the simulated efficiency. From (15), the average inductor currents $I_{L1,avg}$ and $I_{L2,avg}$ are calculated as 6.125 A and 4.083 A respectively. Figure 17 shows the inductor current waveforms and the average values measured for I_{L1} and I_{L2} are 6.461 A and 4.210 A respectively. Figure 18 shows the voltage stresses across the switches which can be calculated from (24) and (25). The measured peak blocking voltage of the switches is 83.5 V. Figs. 19 and 20 show the voltages across diodes D_4 and D_{out} respectively. The peak blocking voltage of VM stage diodes is given by (30) and is measured as 165 V. Similarly the peak blocking voltage of the output diode for even number of VM stages is given by (32) and is measured as 83.5 V. The measured waveforms shown in Figs. 17 to 20 match the simulated waveforms and thus validate the operation of the converter.

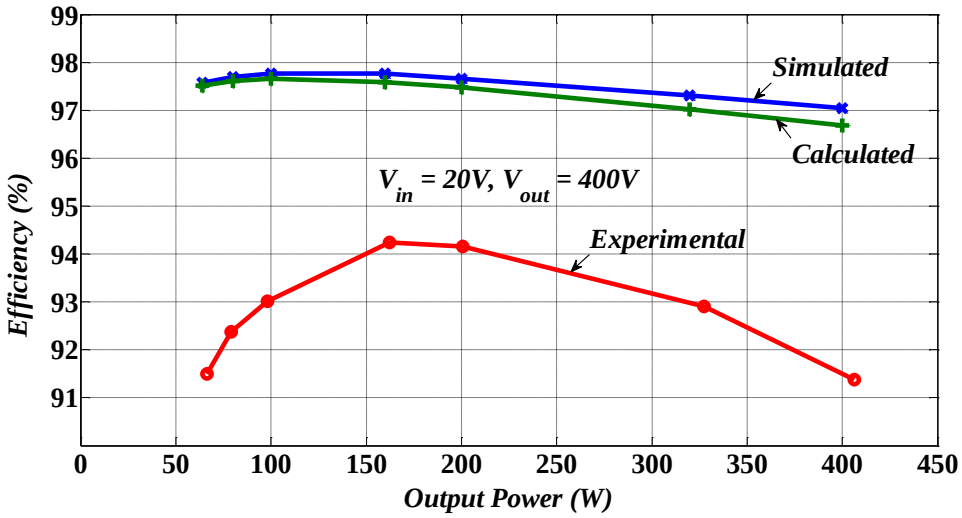

Figure 16. Efficiency of the proposed converter with interleaved input and four VM stages.

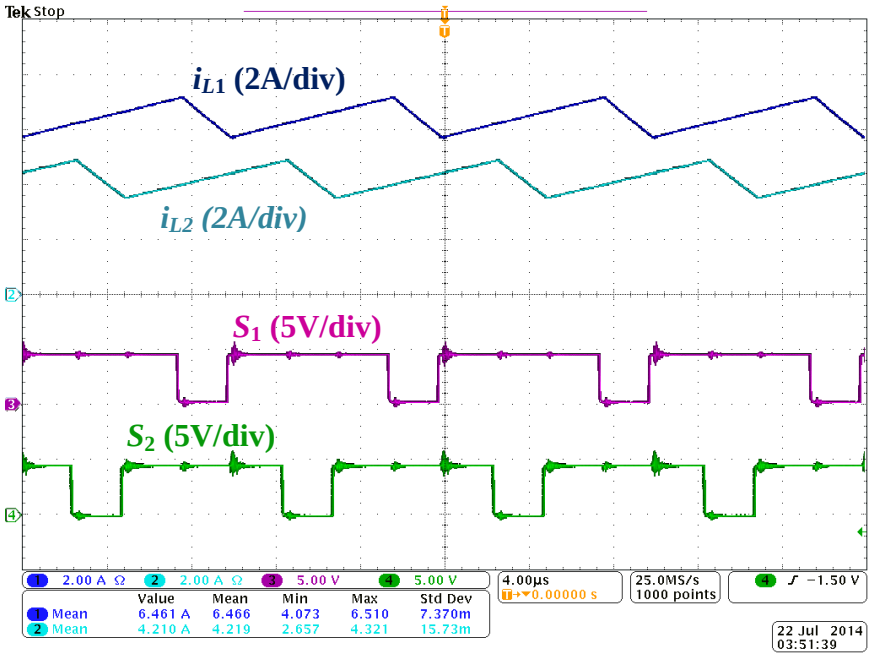

Figure 17. Inductor current waveforms at 200 W output power.

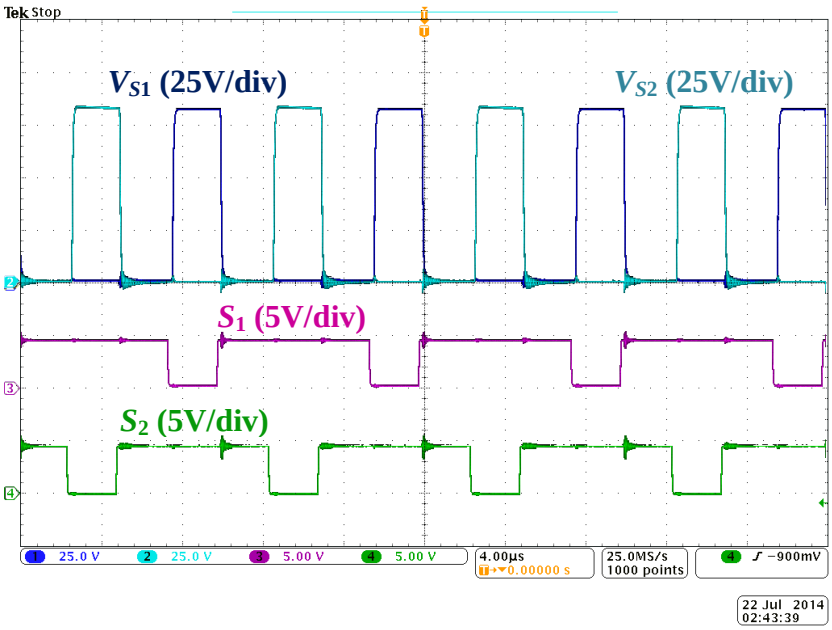

Figure 18. Voltage stresses on the boost switches.

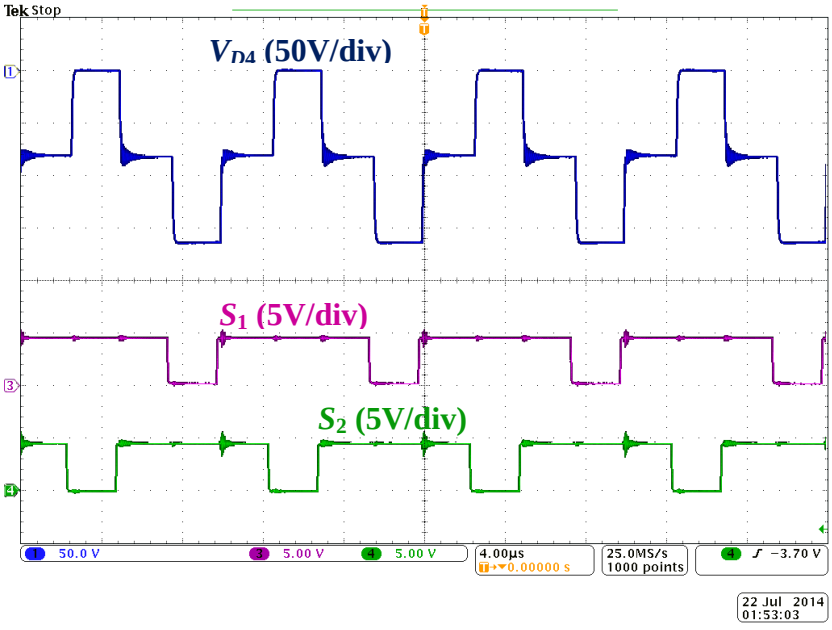

Figure 19. Voltage waveform across diode D_4.

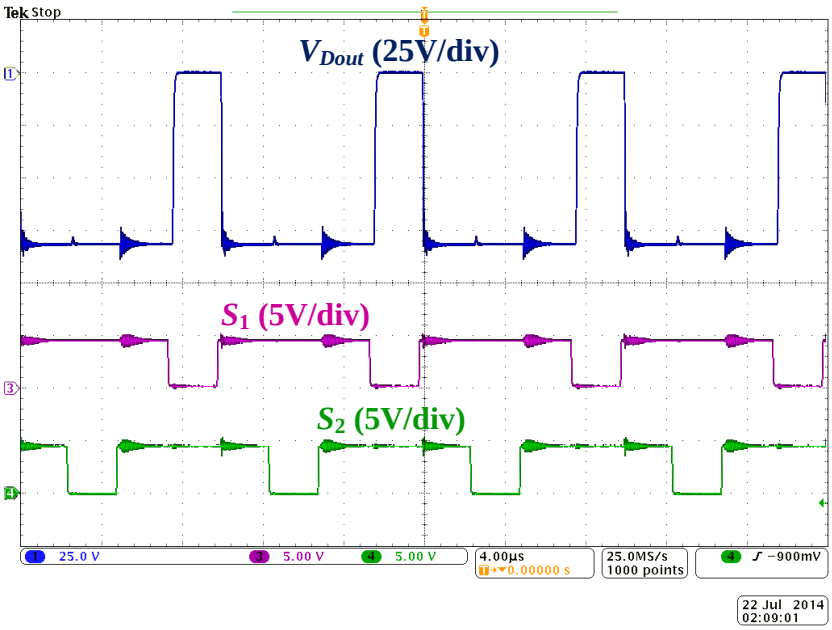

Figure 20. Voltage waveform across output diode D_{out}.

VI. Conclusion

In this paper, a family of novel high gain dc-dc converters with two boost stages at the input has been proposed. The proposed converter is based on diode-capacitor VM stages and the voltage gain is increased by increasing the number of VM stages. It can draw power from two input sources like a multiport converter or operate in an interleaved manner when connected to a single source. One of the advantages of the proposed converter is, since it is a multi-port converter with high voltage gain, independent sources can be connected and power sharing, MPPT algorithms etc. can be implemented independently at each input port. Furthermore, an alternative topology of the proposed converter has been presented and combining them both would result in a new converter topology. The proposed converter can be used for solar applications where each panel can be individually linked to the 400-Vdc bus. The experimental prototype is built to validate

the operation of the converter.

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III. A HIGH VOLTAGE GAIN BIDIRECTIONAL DC-DC CONVERTER

***Abstract*—**A high-voltage-gain bi-directional dc-dc power electronic converter is proposed. The proposed converter can easily achieve high step-up/step-down voltage gains while benefitting from a continuous input/output current. The proposed converter is composed of a bidirectional boost converter cascaded with a bidirectional switched capacitor (SC) converter. The SC converter with the proposed multiphase switching scheme achieves higher gains with a low component count. Therefore, it benefits from higher power density and efficiency. In addition, it can achieve various voltage gains which makes it appealing for a variety of renewable and energy storage applications. A 200-W prototype of the proposed converter with V_{in}=24 V and V_{out}=400 V has been developed to validate the analytical results.

I. INTRODUCTION

Recent growth in energy storage and battery powered applications has resulted in the requirement of high-voltage-gain bidirectional dc-dc converters. Moreover, bidirectional dc-dc converters are widely used in applications such as renewable energy systems, telecommunication systems, hybrid electric vehicles, uninterrupted power supplies, dc microgrids, etc. [1-5]. Such converters can be used for interfacing renewable energy sources and energy storage systems to the 400V-dc bus (shown in Figure 1) [6, 7]. These applications require converters with high-voltage-gain and high efficiency with reduced weight, volume, and cost. In order to link solar panels or battery cells to a 400V-dc bus, a number of solar panels or battery cells are required to be connected in series to

attain the required voltage. This leads to reduced system reliability as failure in any one panel/cell in the string of panels/cells would result in failure of the whole string. Thus having a bidirectional dc-dc converter with high step-up/step-down voltage gains would improve the system reliability as several of these panels/cells can be linked individually to the 400-Vdc bus. Furthermore, mismatch between individual panels/cells would not affect the output power.

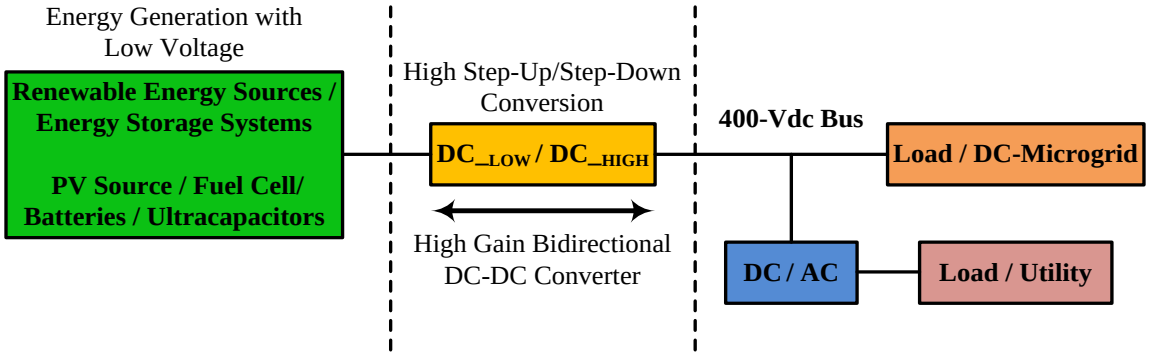

Figure 1. High gain bidirectional dc-dc converter in dc-microgrid system.

A bidirectional dc-dc converter has been proposed in this paper which has a bidirectional boost converter cascaded with a novel bidirectional switched capacitor (SC) converter. The proposed converter can easily achieve high step-up/step-down voltage gains while benefitting from a continuous input/output current. The proposed converter has low voltage stresses across the components and requires a simple controller. Conventional voltage and current mode control schemes can be easily implemented for the proposed converter.

SC dc-dc converters are fast gaining popularity as their power density is high and they have high efficiencies even at light load conditions while maintaining good no-load output voltage regulation [8-16]. There are several limitations of SC converters like large number of switching devices with pulsating input and device currents. Additional inductors have been used in resonant switched capacitor converters to mitigate the pulsating current and reduce the switching losses [17, 18]. Moreover, combinations of SC converters and inductors have been proposed to achieve large voltage conversion ratios [19-21]. This paper proposes a SC converter with a multiphase switching scheme. The proposed SC converter has several advantages like – a) less number of switching devices, b) higher gains for lower parts count, c) variable gains can be achieved by multiphase operation, d) low component stresses, e) higher efficiency, f) reduced weight, volume and cost, hence higher power density, g) bidirectional power flow achieved by minimal switch realization.

In Section II the proposed SC converter with multiphase switching scheme is introduced and different modes of operation are explained. In Section III, the output impedance of the proposed SC converter is derived. Sections IV and V discuss the switch realization for bidirectional operation and component selection. Section VI introduces the bidirectional dc-dc converter for energy storage applications. In Section VII experimental results for the prototype converter are provided and Section VIII concludes the paper.

II. Modified Multiphase Voltage Doublers

The basic two phase switched capacitor (TPSC) voltage doubler is shown in Figure 2 [9, 10, 22-26]. It has two modes of operation. In mode I, capacitor C_1 is charged

to input voltage V_{in} and C_{out} transfers charge to the next stage. In mode II, input voltage source V_{in} is placed in series with C_1 and transfer charge to output capacitor C_{out}. The output voltage V_{out} is 2 V_{in} which is the sum of the input voltage and the voltage due to the final charge in C_1. In order to achieve gains greater than 2, several voltage doublers can be cascaded. Figure 3 shows n TPSC voltage doublers cascaded to achieve a voltage gain of 2^n. It requires 4n switches and 2n capacitors (including the output capacitor).

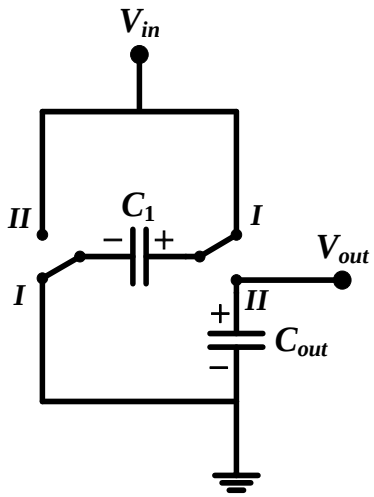

Figure 2. TPSC voltage doubler.

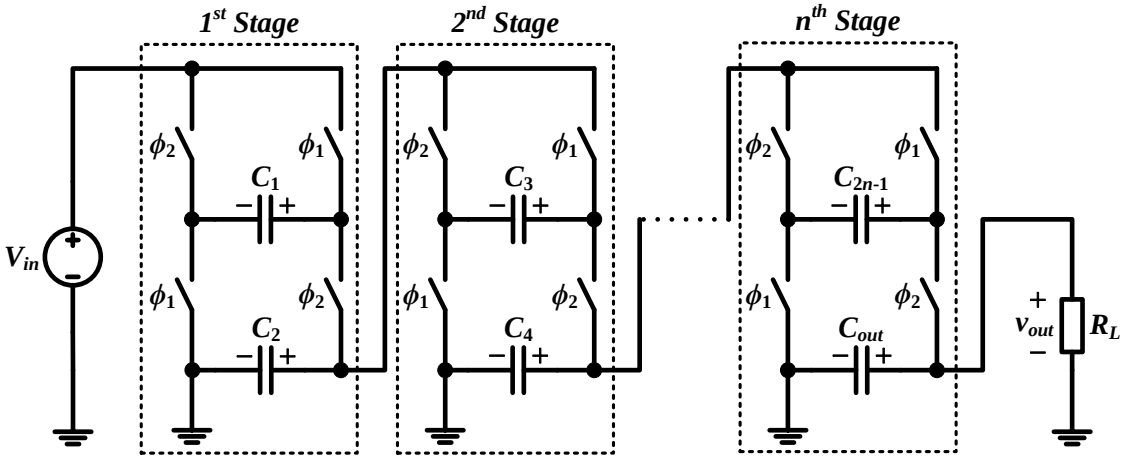

Figure 3. *n*-stage TPSC voltage doubler.

Many power electronic converter applications require higher efficiencies, lower volume, lower weight and lower production costs [27]. The power density of a converter can be increased by reducing the component count. As capacitors consume larger volume and area compared to switches, reducing the number of capacitors will significantly increase the power density of SC converters. Multiphase voltage doublers (MPVDs) were proposed which require 4*n* switches and *n*+1 capacitors (including the output capacitor) to achieve a voltage gain of 2^n (shown in Figure 4) [10, 25, 28-31]. They require 2*n* switching signals which can be easily generated by frequency division. They have a lower number of capacitors compared to *n*-stage TPSC voltage doublers. Therefore, they use lesser footprint and achieve higher power density.

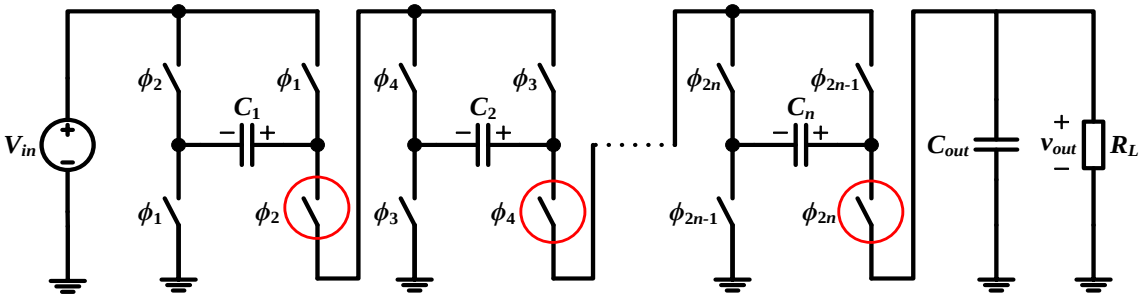

Figure 4. *n*-stage multiphase voltage doubler.

Furthermore, it can be observed that the multiphase switching scheme makes the right-hand-side bottom leg switch of each stage (as shown in Figure 4) in series with the upper leg switches of the next stage. Therefore, the component count can be further reduced by removing the redundant switches in the bottom legs (shown in Figure 5). Lower number of switches would reduce the switching and conduction losses in the converter. Moreover, it would require lesser switch driver circuitry and hence would improve the efficiency and power density of the SC converter.

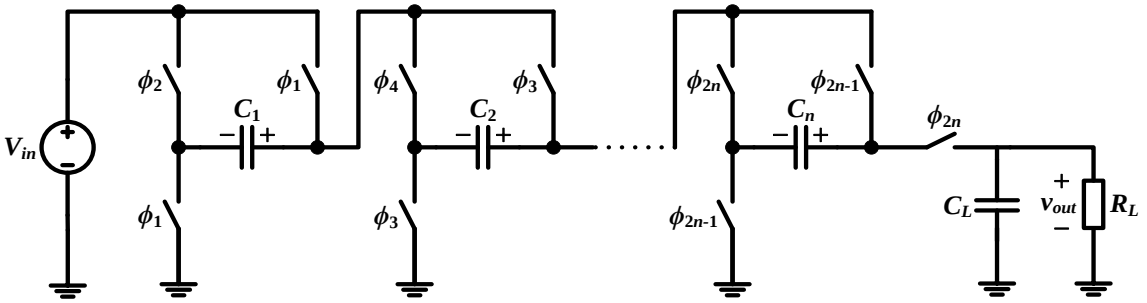

Figure 5. Proposed *n*-stage modified multiphase voltage doubler (MMPVD).

An *n*-stage modified multiphase voltage doubler (MMPVD) with reduced number of switches has been proposed. It has a voltage gain of 2^n (shown in Figure 5) and

requires $3n+1$ switches and $n+1$ capacitors (including the output capacitor). Similar to MPVD, it also requires $2n$ switching signals based on frequency division. It can be observed that the MMPVD circuit structure shown in Figure 5 is similar to that of an n-stage Fibonacci converter [10-12, 32-35]. However, the proposed SC converter can be used to achieve gains greater than that of a Fibonacci converter by just changing the switching scheme for the same parts count (as shown in Figure 6).

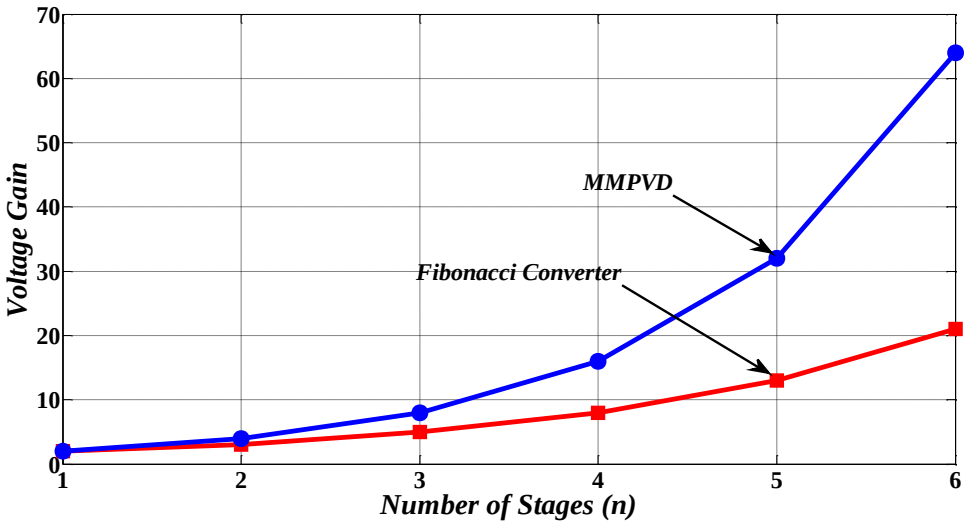

Figure 6. Voltage gain of MMPVD and Fibonacci converters.

To achieve a voltage gain of $M_V = 8$, a 3-stage MMPVD (shown in Figure 7) is used which requires 10 switches, 6 switching signals, and 4 capacitors. Figure 8 shows the switching scheme for the 3-stage MMPVD circuit based on frequency division. It can be observed from Figure 8, that the switching signals for any stage have a frequency half of the preceding stage with the same pulse width.

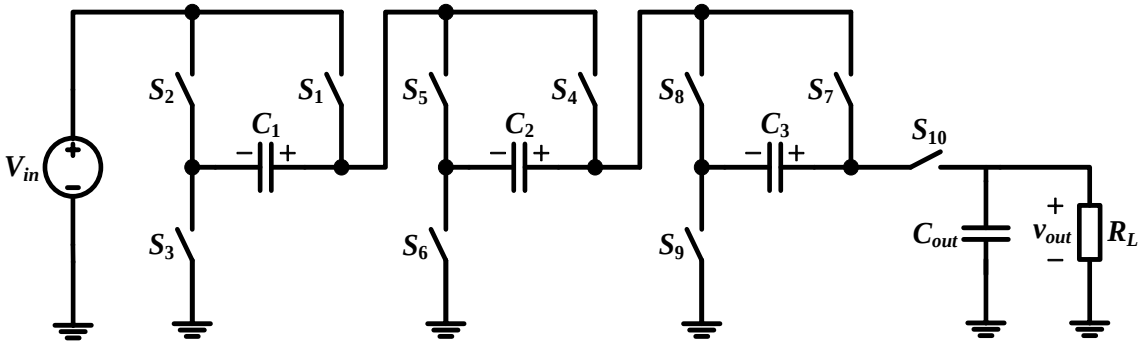

Figure 7. 3-stage MMPVD circuit.

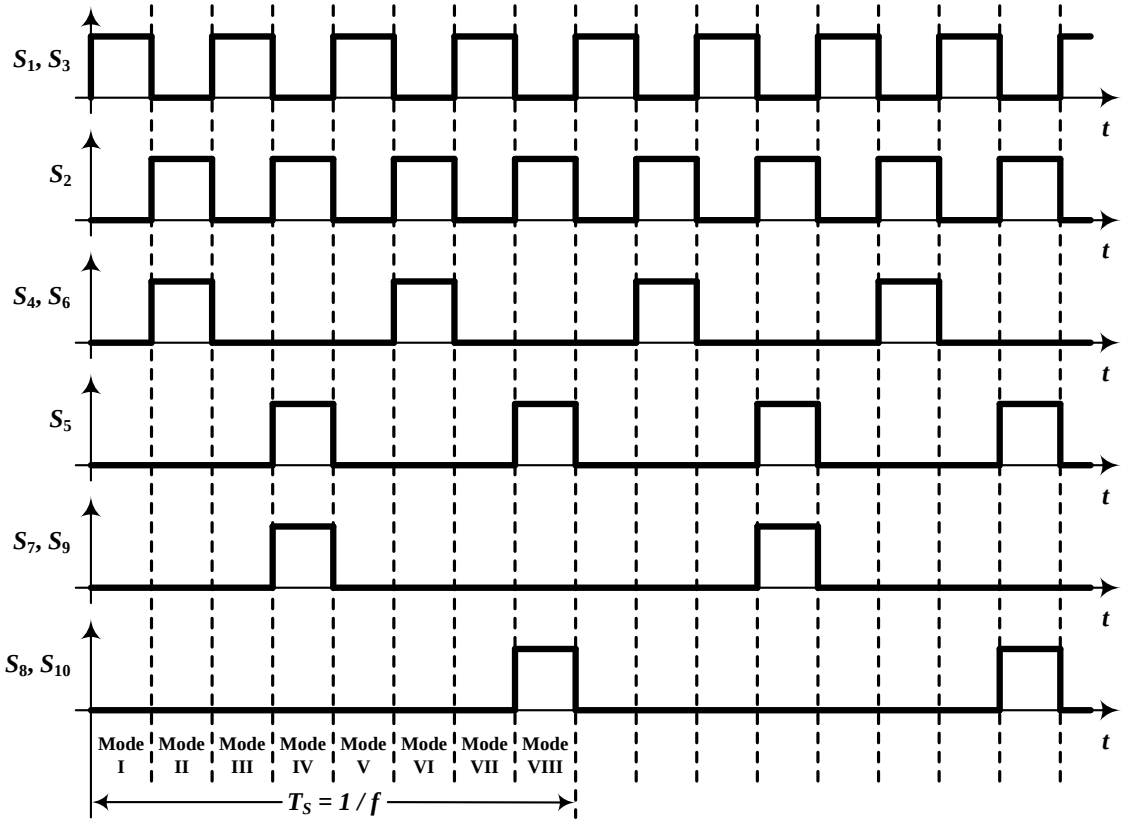

Figure 8. Switching scheme for 3-stage MMPVD.

Table I compares the component count of different topologies for a voltage gain M_V = 8. It can be observed that MMPVD has lower number of switches compared to MPVDs proposed in [10] (compare Figs. 4 and 5). The operation of the proposed SC converter with 3-stages can be explained in eight different modes (shown in Figure 8). The charge is transferred to the output by charging the capacitors in different modes of operation by turning ON appropriate switches and then discharging into the load.

Table I. Number of Devices Required for Voltage Gain M_V = 8

	TPVD	**Fibonacci**	**MPVD**	**MMPVD**
***n* (number of stages)**	**3**	**4**	**3**	**3**
Switches	**12**	**12**	**12**	**10**
Capacitors	**6**	**5**	**4**	**4**

A. Mode-I, III, V, VII

In these modes of operation, switches S_1 and S_3 are turned ON and capacitor C_1 is connected to the input voltage source and is charged to V_{in} (shown in Figure 9).

$$V_{C1} = V_{in} \tag{1}$$

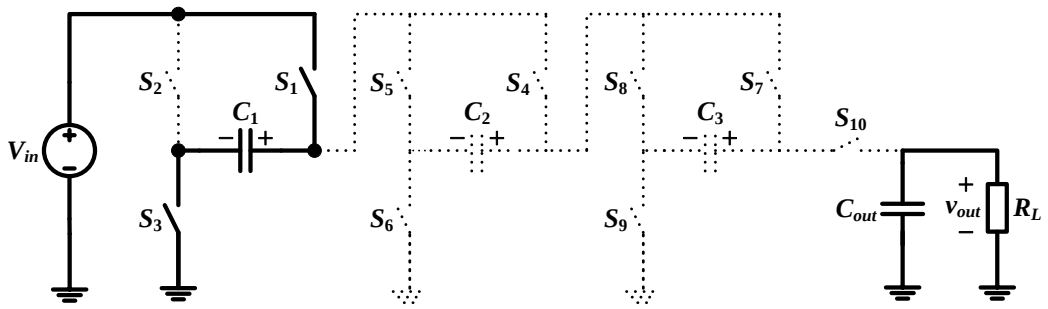

Figure 9. Equivalent circuit for modes-I, III, V, VII of MMPVD operation.

B. Mode-II, VI

In these modes, switches S_2, S_4, and S_6 are turned ON (shown in Figure 10). During this mode capacitor C_2 is connected to the input source in series with capacitor C_1. The charge stored in C_1 is transferred to capacitor C_2 which is charged to a voltage equal to the sum of the input voltage and the voltage due to the charge in C_1 and is given by

$$V_{C2} = V_{in} + V_{C1} = 2V_{in} \tag{2}$$

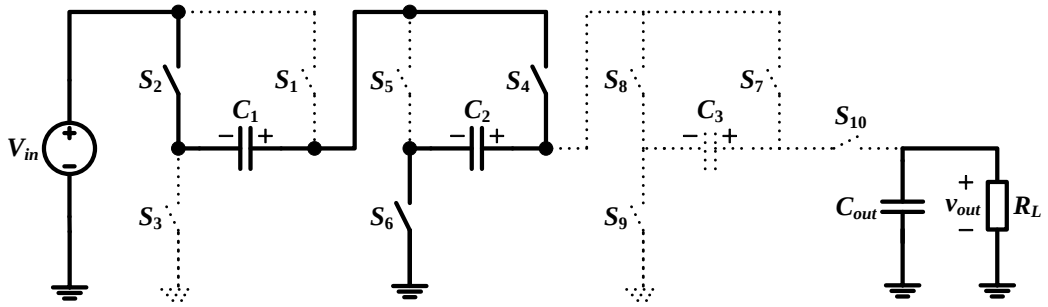

Figure 10. Equivalent circuit for modes-II, VI of MMPVD operation.

C. Mode-IV

In mode IV of operation, switches S_2, S_5, S_7, and S_9 are ON (shown in Figure 11). Capacitor C_3 is connected to the input source in series with capacitors C_1 and C_2. The charge is transferred to C_3 and is charged to a voltage equal to the sum of the input voltage and the voltages due to the charges in C_1 and C_2 and is given by

$$V_{C3} = V_{in} + V_{C1} + V_{C2} = 4V_{in} \tag{3}$$

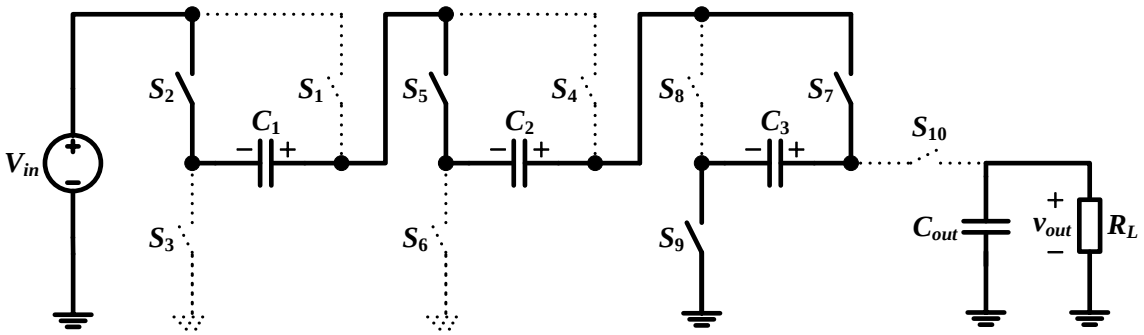

Figure 11. Equivalent circuit for mode-IV of MMPVD operation.

D. Mode-VIII

In mode VIII, switches S_2, S_5, S_8, and S_{10} are turned ON (shown in Figure 12). The load is connected to the source in series with capacitors C_1, C_2, and C_3 and the charge stored in these capacitors is discharged into the load. The output voltage is the sum of the input voltage and the capacitor voltages due to the final charges in C_1, C_2, and C_3, which is given by

$$V_{out} = V_{in} + V_{C1} + V_{C2} + V_{C3} = 8V_{in} \quad (4)$$

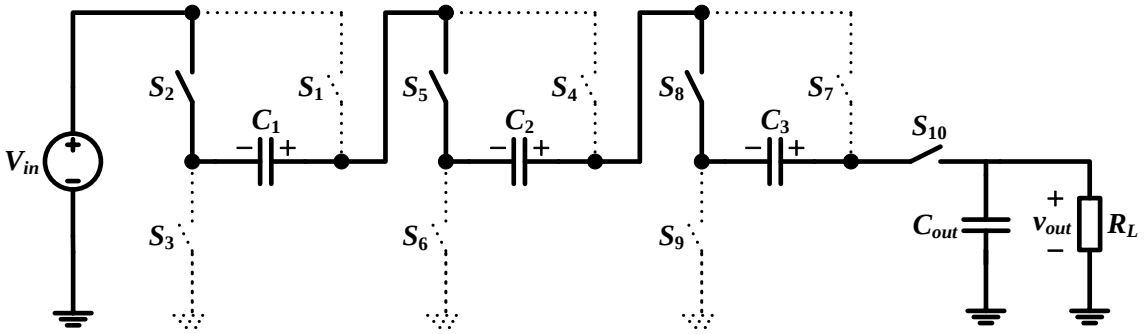

Figure 12. Equivalent circuit for mode-VIII of MMPVD operation.

The proposed SC converter can achieve different gains by changing the switching scheme as shown in Table II below. Moreover, it can also achieve gains similar to that of a Fibonacci converter. Thus the capability of the proposed SC converter to achieve variable gains makes it very versatile and useful for many applications.

Table II. Different Gains of MMPVD

3-Stage	Mode I	Mode II	Mode III	Mode IV	Mode V	Mode VI	Mode VII	Mode VIII
8x-Gain	S_1, S_3	S_2, S_4, S_6	S_1, S_3	S_2, S_5, S_7, S_9	S_1, S_3	S_2, S_4, S_6	S_1, S_3	S_2, S_5, S_8, S_{10}
7x-Gain	S_1, S_3	S_2, S_4, S_6	S_1, S_3	S_2, S_5, S_7, S_9	S_1, S_3	S_2, S_4, S_6	S_1, S_5, S_8, S_{10}	
6x-Gain	S_1, S_3	S_2, S_4, S_6	S_1, S_3	S_2, S_5, S_7, S_9	S_1, S_3	S_2, S_4, S_8, S_{10}		
5x-Gain	S_1, S_3	S_2, S_4, S_6	S_1, S_3	S_2, S_5, S_7, S_9	S_1, S_4, S_8, S_{10}			
4x-Gain	S_1, S_3	S_2, S_4, S_6	S_1, S_3	S_2, S_5, S_7, S_{10}				
3x-Gain	S_1, S_3	S_2, S_4, S_6	S_1, S_5, S_7, S_{10}					
2x-Gain	S_1, S_3	S_2, S_4, S_7, S_{10}						
1x-Gain	S_1, S_4, S_7, S_{10}							
Fibonacci	S_1, S_3, S_5, S_7, S_9	S_2, S_4, S_6, S_8, S_{10}						

III. Output Impedance of MMPVDs

SC converters achieve ideal voltage conversion ratios under no load conditions. Under load conditions, the output voltage is always lower than the no load output voltage [11, 12, 33]. This is because of the energy lost in periodically charging and discharging the capacitors in order to transfer charge from input to the load. The energy loss depends on the ac ripple voltage component in the capacitor voltages. Energy is also lost in the network parasitics like capacitor ESRs and switch on time resistances during charging/discharging process of the capacitors.

In [12], it has been shown that network parasitics play an important role in the performance of the SC converters. The parasitic time constants τ_i with respect to

switching period T_S is necessary to analyze and estimate the converter power losses and efficiency. If $\tau_i >> T_S$, the capacitor voltage ripple can be approximated to be linear and state-space averaging techniques can be used to determine the steady state and dynamic behavior of the converter. If τ_i is close to T_S, then the non-linearity in capacitor voltage ripples cannot be neglected and modified state space averaging techniques are used to analyze the converter. When $\tau_i << T_S$, the charge and discharge cycles of the capacitors are completed within the switching period and the exact knowledge of the parasitics in the network is not required.

Figure 13 shows the ideal SC converter model. The turns ratio gives the ideal no load voltage gain of the converter and R_{out} is the equivalent output resistance of the SC converter. The two asymptotic limits of the output impedance of SC converters related to the switching frequency are given by slow switching limit (SSL) and fast switching limit (FSL) impedance. These performance limits are required for design, analysis, and component selection for SC converters. They can also be used for comparing and selecting different SC converter topologies.

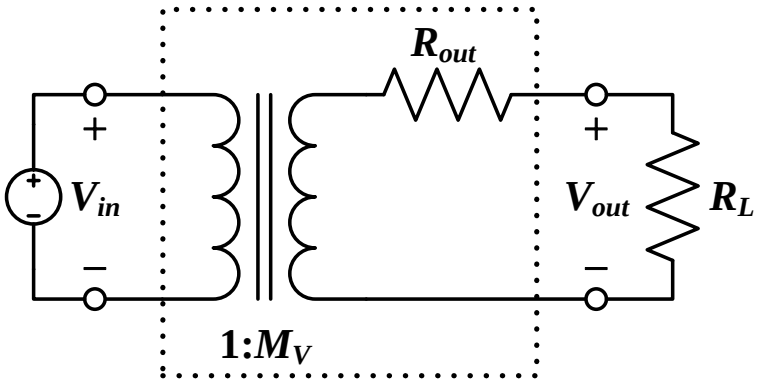

Figure 13. Ideal SC converter model.

The SSL impedance is calculated by assuming switches, capacitors and other conductive interconnects are ideal by neglecting the parasitics in the network [11, 33]. The energy loss is only due to the charging/discharging of the capacitors. In order to determine the output impedance, charge vectors are derived for the all modes of the SC converter operation using network analysis. It corresponds to the amount of charge flowing into each capacitor or an independent voltage source and is normalized with respect to the output charge. Charge vectors are calculated by having independent voltage sources V_{in} and V_{out} at the input and output respectively. They can be partitioned into charge flowing into the output, capacitor, and input components in each mode and can be shown as,

$$\boldsymbol{a}^{\boldsymbol{j}} = \left[q_{out}^{j} \quad \boldsymbol{a}_{\boldsymbol{C}}^{\boldsymbol{j}} \quad q_{in}^{j} \right]^{T} / q_{out} \tag{5}$$

where $\boldsymbol{a}_{\boldsymbol{C}}^{\boldsymbol{j}}$ is the vector of charge flowing into each capacitor in the j^{th} mode and is given by,

$$\boldsymbol{a}_{\boldsymbol{C}}^{\boldsymbol{j}} = \left[q_{C1}^{j} \quad q_{C2}^{j} \quad ..... \quad q_{Cn}^{j} \right]^{T} / q_{out} \tag{6}$$

As described earlier, there are 8 topological modes of operation for the 3-stage MMPVD. Similarly, an n-stage MMPVD has $2n$ switching signals and will have 2^n topological modes of operation. For a 3-stage MMPVD, the charge vectors for different modes can be described as,

$$\left[\boldsymbol{a}^1\middle|\boldsymbol{a}^2\middle|\boldsymbol{a}^3\middle|\boldsymbol{a}^4\middle|\boldsymbol{a}^5\middle|\boldsymbol{a}^6\middle|\boldsymbol{a}^7\middle|\boldsymbol{a}^8\right]=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 \\ 0 & 1 & 0 & -1 & 0 & 1 & 0 & -1 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 \\ -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \end{bmatrix} \quad (7)$$

In [11], the SSL impedance R_{SSL} describing only the energy loss due to charging/discharging of capacitors has been derived based on the charge vectors. For the 3-stage MMPVD, R_{SSL} is given by,

$$R_{SSL}=\sum_{i=1}^{3}\sum_{j=1}^{8}\frac{\left(a_{Ci}^{j}\right)^2}{2C_i f}=\frac{4}{C_1 f}+\frac{2}{C_2 f}+\frac{1}{C_3 f} \quad (8)$$

where C_i is the capacitor in the i^{th} stage, f is the switching frequency of the last stage. Similarly, for an n-stage MMPVD, R_{SSL} can be derived as,

$$R_{SSL}=\sum_{i=1}^{n}\sum_{j=1}^{2^n}\frac{\left(a_{Ci}^{j}\right)^2}{2C_i f}=\frac{2^{n-1}}{C_1 f}+\frac{2^{n-2}}{C_2 f}+.....+\frac{1}{C_n f} \quad (9)$$

Both MPVDs and MMPVDs are similar in terms of operation with the only difference that MMPVDs have lower number of switches. Therefore, R_{SSL} would be the same for both of the SC converter topologies.

When the switching frequencies increase, the parasitic time constants τ_i can no longer be neglected and the network parasitics like switch on-time resistances and capacitor ESRs would start dominating. The capacitors are charged/discharged by constant current flows and they do not approach equilibrium. The FSL impedance is calculated by modeling the capacitor voltages as constant and is only due to the conduction losses in the network parasitics. Normalized charge vectors for the switches

in each mode of operation is calculated based on the charge flowing into the switches by simple network analysis and can be given by,

$$\boldsymbol{a}_r^j = \left[q_{S1}^j \quad q_{S2}^j \quad ..... \quad q_{S(3n+1)}^j \right]^T / q_{out} \tag{10}$$

It can be observed that for an *n*-stage MMPVD, there are $3n+1$ switches and 2^n modes of operation. Therefore, for a 3-stage MMPVD there are 10 switches and 8 modes of operation. The charge vectors for the switches for different modes of operation are given by,

$$\left[\boldsymbol{a}_r^1 \middle| \boldsymbol{a}_r^2 \middle| \boldsymbol{a}_r^3 \middle| \boldsymbol{a}_r^4 \middle| \boldsymbol{a}_r^5 \middle| \boldsymbol{a}_r^6 \middle| \boldsymbol{a}_r^7 \middle| \boldsymbol{a}_r^8 \right] = \begin{bmatrix} 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{11}$$

The FSL impedance R_{FSL} for 3-stage MMPVD describing the conduction losses due to the switch on-time resistances and capacitor ESRs is given by,

$$R_{FSL} = 8\left(\sum_{i=1}^{10} \sum_{j=1}^{8} r_{Ti} (a_{ri}^j)^2 + \sum_{k=1}^{3} \sum_{m=1}^{8} r_{Ck} (a_{Ck}^m)^2 \right) = 176 r_T + 112 r_C \tag{12}$$

where r_T is the switch on time resistance and r_C is the capacitor ESR. Generally, thin film capacitors have low ESR values; therefore R_{FSL} is dominated by switch on time resistances. Similarly, for an *n*-stage MMPVD, R_{FSL} can be derived as,

$$R_{FSL}(MMPVD) = 2^n\left(\sum_{i=1}^{3n+1}\sum_{j=1}^{2^n} r_{Ti}(a_{ri}^{j})^2 + \sum_{k=1}^{n}\sum_{m=1}^{2^n} r_{Ck}(a_{Ck}^{m})^2\right) = \left(3\times 2^{2n} - 2^{n+1}\right)r_T + \left(2^{2n+1} - 2^{n+1}\right)r_C \quad (13)$$

The R_{FSL} for an n-stage MPVD proposed in [10] is given by,

$$R_{FSL}(MPVD) = \left(4\times 2^{2n} - 2^{n+2}\right)r_T + \left(2^{2n+1} - 2^{n+1}\right)r_C \quad (14)$$

The approximate output impedance for the SC converters is given by [33],

$$R_{out} \approx \sqrt[2.545]{\sqrt{\left(R_{SSL}\right)^{2.545} + \left(R_{FSL}\right)^{2.545}}} \quad (15)$$

It can be observed from Figs. 4 and 5 that MMPVDs have lower number of switches compared to MPVDs and hence R_{FSL} of MMPVD is less than that of MPVD (see Figure 14). Simulated R_{out} of the proposed MMPVD (blue stars in Figure 14) was compared with the R_{out} derived analytically in (9), (13), and (15).

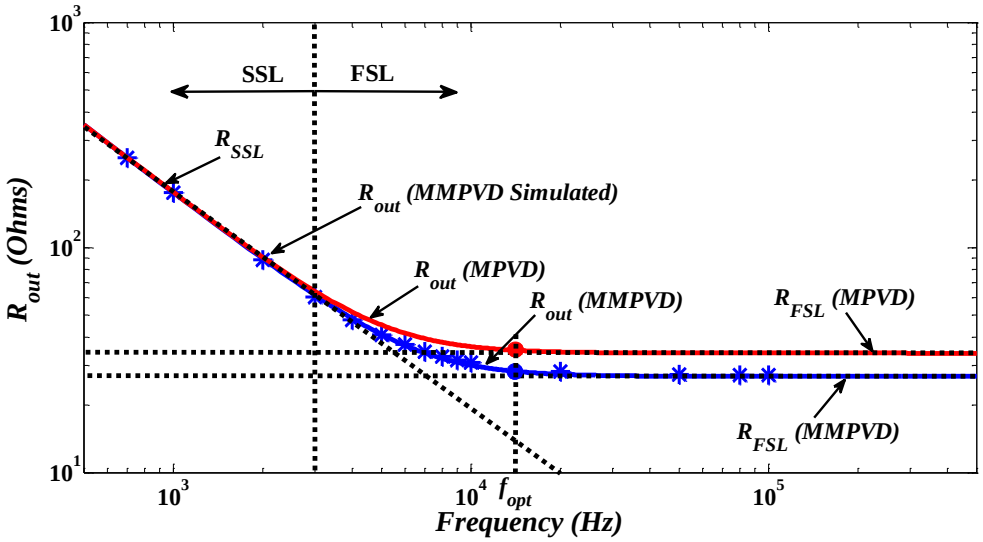

Figure 14. Output impedance of the proposed MMPVD.

The non-ideal voltage gain M and the efficiency of the SC converters η depend on the output impedance R_{out} of the converter and are given by

$$M = \frac{M_V}{1 + R_{out}/R_L} \tag{16}$$

$$\eta = \frac{1}{1 + R_{out}/R_L} \tag{17}$$

It can be observed that the SC converter voltage gain and efficiency decreases with increasing load current.

IV. BIDIRECTIONAL MMPVDS

The proposed SC converter can have bidirectional capabilities by having appropriate switch realization. It is important to realize switches in a manner to minimize the number of switches in order to improve the efficiency and power density of the SC converter. The switches should have two quadrant current bidirectional operation, i.e., always blocking the positive voltage and conducting currents in both directions. Power MOSFETs can be used to realize the switches as they have reverse conduction capabilities (as shown in Figure 15). Figure 16 shows the bidirectional MMPVD, it can be observed that the anti-parallel diodes of the power MOSFETs are always reverse biased and the switches have reverse conduction capabilities for reverse power flow.

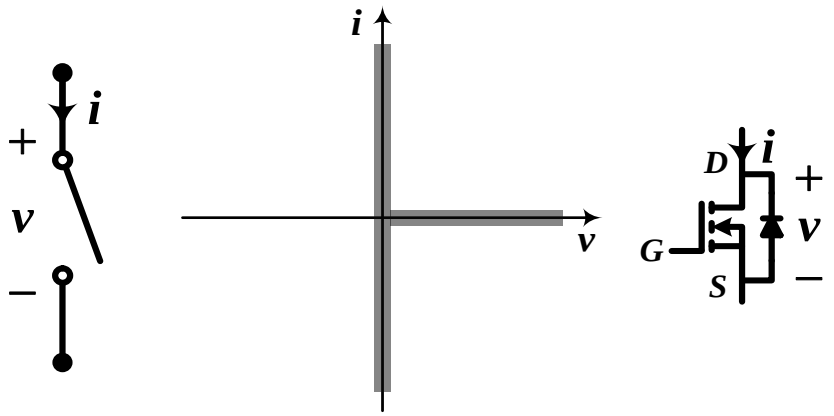

Figure 15. Two quadrant current bidirectional switch.

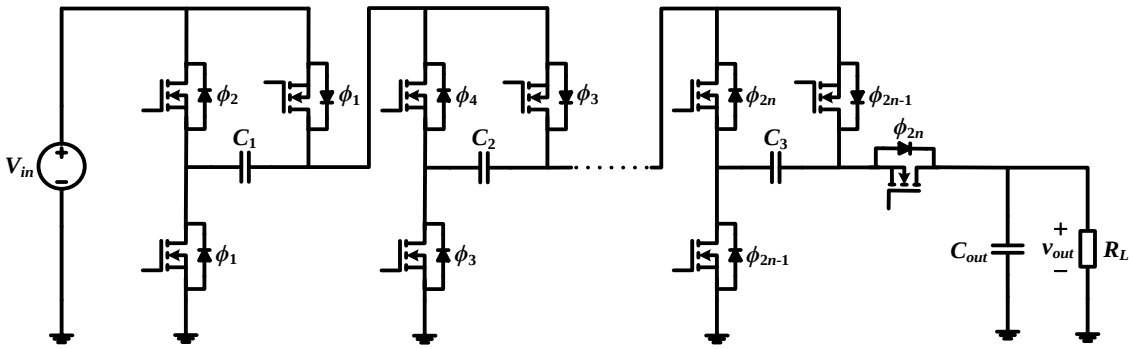

Figure 16. Bidirectional MMPVD.

V. Component Selection for MMPVDs

A. Frequency Selection

The SC converter operating frequency is important as its output impedance is frequency dependent. The converter efficiency, voltage gain, and output voltage regulation depends on the output impedance of the converter. From Figure 14, it can be observed that low output impedance for the SC converters happen in the FSL mode,

when R_{FSL} dominates the output impedance. Thus from (9) and (13), the optimal switching frequency is given by,

$$f_{opt} > \left(\frac{2^{n-1}}{C_1} + \frac{2^{n-2}}{C_2} + ... + \frac{1}{C_n} \right) \Big/ \left[\left(3 \times 2^{2n} - 2^{n+1}\right) r_T + \left(2^{2n+1} - 2^{n+1}\right) r_C \right] \tag{18}$$

B. Capacitor Selection

If the all capacitors are assumed to be similar, i.e., $C_1 = C_2 \ldots = C_n = C$, then the optimum value of the capacitors for which the converter would have efficient operation with low output impedance is when it operates in FSL mode and R_{FSL} would be dominating (shown in Figure 17). Thus from (9) and (13), the optimal value of the capacitors can be derived as,

$$C_1 = C_2 \ldots = C_n = C > \frac{\left(2^n - 1\right)}{f\left[\left(3 \times 2^{2n} - 2^{n+1}\right) r_T + \left(2^{2n+1} - 2^{n+1}\right) r_C\right]} \tag{19}$$

It can be observed that, increasing the capacitance beyond this value would not improve the performance of the converter and would only increase the size and cost of the converter. Moreover, the voltage across MMPVD capacitors is given by,

$$V_{Ci} = 2^{i-1} V_{in} \qquad \text{for } i = 1, 2, \ldots, n \tag{20}$$

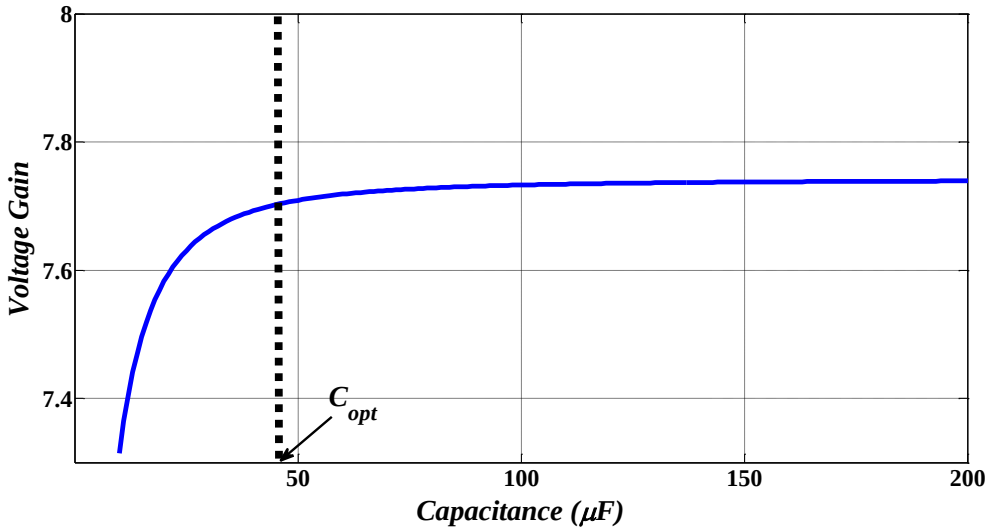

Figure 17. MMPVD voltage gain vs capacitance.

Therefore, the total energy delivered by the capacitors can be given by,

$$E_{tot} = \sum_{i=1}^{n} \frac{1}{2} C_i V_{Ci}^2 = \frac{\left(2^{2n} - 1\right)}{6} C V_{in}^2 \tag{21}$$

Since the size and cost of the SC converter is dominated by the capacitor sizing, the total energy delivered by the capacitors becomes a very important factor. From Figure 18, it can be observed that the total energy (normalized with respect to the total energy delivered by the capacitor in the first stage) delivered by the capacitors in the Fibonacci converter is greater than the proposed MMPVD. Therefore, the Fibonacci converter will have larger capacitor sizes, hence higher costs and lower power density compared to the proposed MMPVD topology.

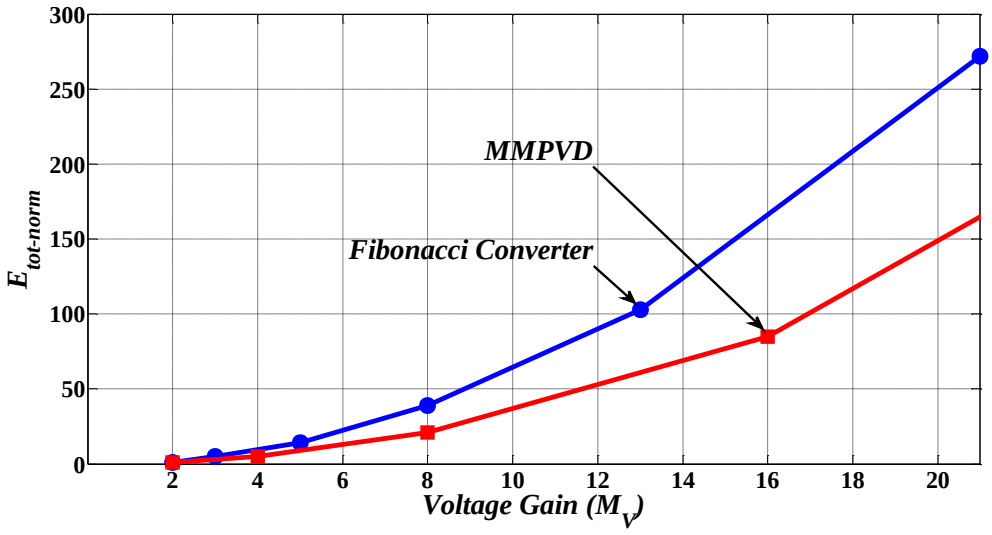

Figure 18. Normalized total energy $E_{tot\text{-}norm}$ delivered by the capacitors vs voltage gain.

The energy storage capability of the capacitors depends on their voltage ratings [11]. The size and cost of the capacitors can be further optimized by minimizing the SSL impedance (scaled by switching frequency) subject to the energy constraint. The Lagrange function for the above optimization problem is given by,

$$L = \sum_{i=1}^{n} \sum_{j=1}^{2^n} \frac{\left(a_{Ci}^{j}\right)^2}{2C_i} + \lambda \left(\sum_{i=1}^{n} \frac{1}{2} C_i V_{Ci(rated)}^2 - E_{tot} \right) \tag{22}$$

After evaluating the partial derivatives of L with respect to C_i and λ, the optimized value for each capacitor is given by,

$$C_i = \frac{\sqrt{\sum_{j=1}^{2^n} \left(a_{Ci}^{j}\right)^2}}{V_{Ci(rated)}} \frac{2E_{tot}}{\sum_{k=1}^{n} V_{Ck(rated)} \sqrt{\sum_{j=1}^{2^n} \left(a_{Ck}^{j}\right)^2}} \tag{23}$$

Moreover, from (13) it can be observed that capacitor's ESR increases R_{FSL}, thus affecting the converter efficiency and gain of the converter. Therefore, it is important to select capacitors with low ESRs.

C. MOSFET Selection

The peak blocking voltage and average current of the MOSFET depends on the stage it is connected to. It can be observed from Figure 19 that the peak blocking voltage of switch S_2 (connected to stage-1 of MMPVD) is $V_{out}/8$. The peak blocking voltages for switches S_5 (connected to stage-2) and S_8 (connected to stage-3) are $V_{out}/4$ and $V_{out}/2$ respectively. The voltage stress on the switches increases with each stage and the maximum voltage stress is experienced by switches in the last stage i.e., n^{th} stage, which is half of the output voltage and is given by (24). The current stress on the switches also depends on the stage they are connected to and the average current of the switches in the i^{th} stage is given by (25). The current stresses on the switches decrease with each stage.

$$V_S^i = \frac{V_{out}}{2^{n-i+1}} \qquad \text{for } i = 1, 2, \ldots, n \tag{24}$$

$$I_{S,avg}^i = 2^{n-i} I_{out} \qquad \text{for } i = 1, 2, \ldots, n \tag{25}$$

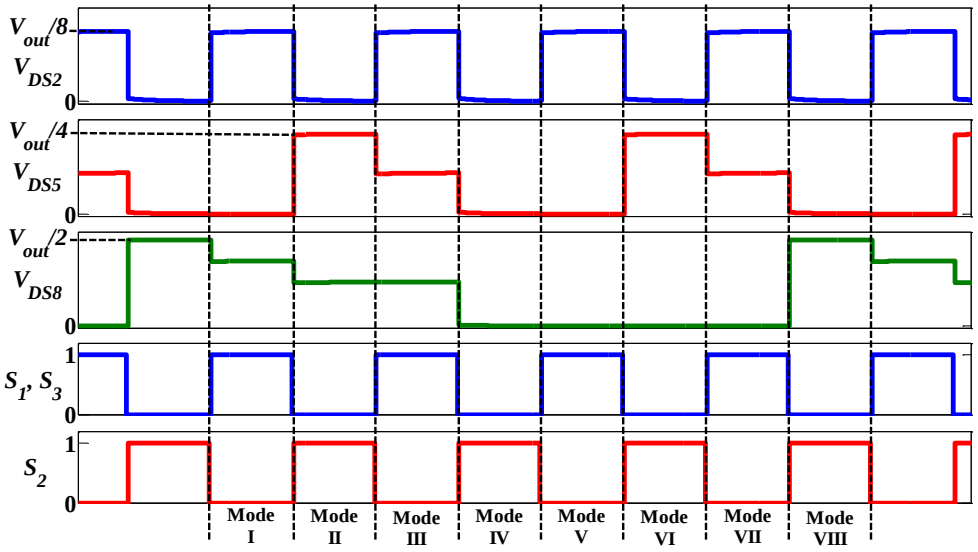

Figure 19. Voltage across switches S_2, S_5, and S_8 of 3-stage MMPVD.

From (13) it can be observed that R_{FSL} is directly proportional to switch on time resistance R_{on}. Figure 20 shows the converter gain vs. R_{on}. It can be observed that R_{on} adversely affects the converter efficiency and output voltage regulation. Therefore it is very important to select MOSFETs with low $R_{DS(on)}$.

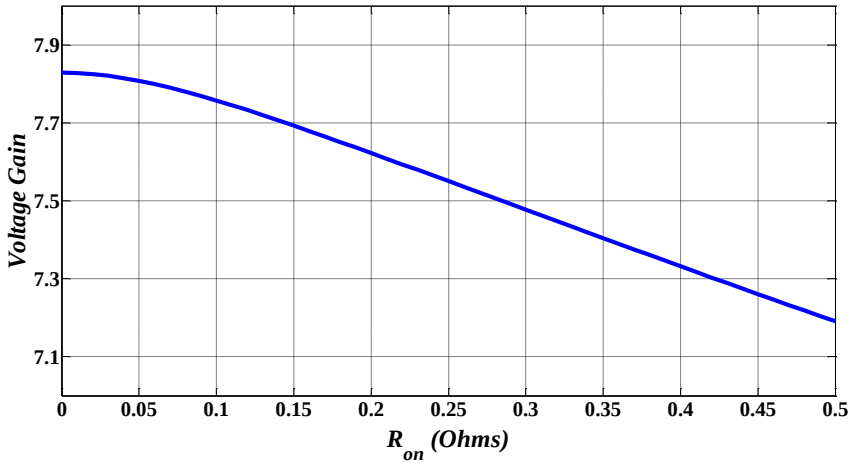

Figure 20. MMPVD voltage gain vs switch on time resistance R_{on}.

VI. Bidirectional Converter for Microgrid Applications

The proposed converter is based on cascading bidirectional boost converter with the proposed bidirectional MMPVD stages. MMPVD stages can boost the voltage up to 2^n times, where n is the number of voltage doubler stages cascaded together. In the reverse power flow direction the voltage doubler stages have a high step-down voltage gain of $1/2^n$. Thus we get both high step-up and step-down gains with the same conversion ratio in either direction of power flow. The first stage which is a bidirectional boost converter switches between boost and buck mode depending on the power flow direction. Moreover the bidirectional boost stage at the input further increases/decreases the gain of the converter.

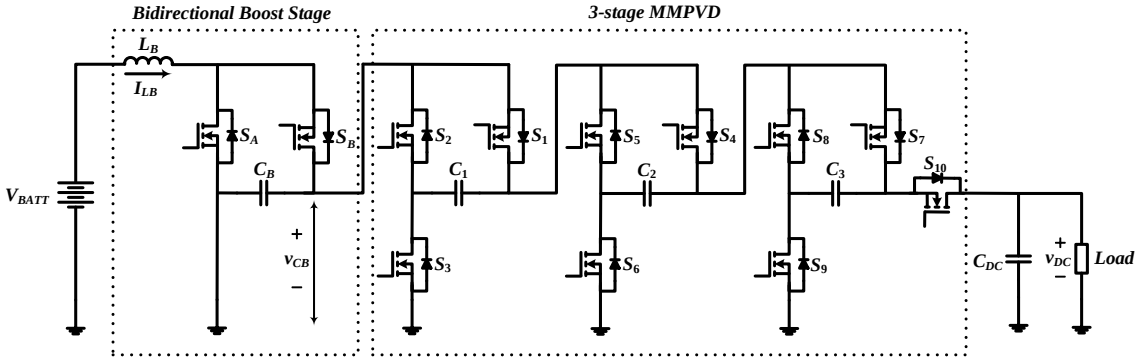

Figure 21. Proposed bidirectional converter.

In forward power flow, the output of the bidirectional boost stage is controlled by controlling the duty ratio d of switch S_A. The output of the boost stage is given by,

$$V_{CB} = \frac{V_{BATT}}{(1-d)} \tag{26}$$

Thus the input to the MMPVD stages is controlled by varying the duty cycle of the boost stage. The MMPVD stages are used to help the boost stage achieve higher gains. If an *n*-stage MMPVD is cascaded with the boost stage, then the overall gain of the proposed converter is given by,

$$V_{DC} = 2^n V_{CB} = \frac{2^n V_{BATT}}{(1-d)} \tag{27}$$

The MMPVD stages are operated at fixed duty ratios, so the only way to vary the converter output voltage is by varying the duty ratio of the boost converter switch. The desired gain at the output can be achieved by selecting appropriate number of MMPVD stages.

In reverse power flow, the bidirectional boost converter operates in buck mode and the voltage is stepped down by the same factor given by,

$$V_{CB} = \frac{V_{DC}}{2^n} \tag{28}$$

$$V_{BATT} = (1-d)V_{CB} = \frac{(1-d)V_{DC}}{2^n} \tag{29}$$

VII. Experimental Results

A laboratory prototype with a 3-stage MMPVD and the bidirectional boost input stage (shown in Figure 21) is built to test and validate the proposed converter operation. The components used for building the prototype are listed in Table III. The converter is rated at 200 W with an input voltage of 24 V and an output voltage of 400 V. The control for the prototype is implemented using the TMS320F28335 digital signal processor

(DSP). The switching frequency for the bidirectional boost stage is 100 kHz with a dead time of 100 ns between complementary duty cycles for switches S_A and S_B.

Table III. Component List for the Experimental Prototype

Item	**Reference**	**Rating**	**Part No**
Inductor	L_B	100µH DCR = 11mΩ	CTX100-10-52LP
MOSFET	S_A, S_B	150V, 43A $R_{DS(on)}$ = 7.5mΩ	IPA075N15N3G
MOSFET	S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8, S_9, S_{10}	500V, 29A $R_{DS(on)}$ = 150mΩ	AOT29S50L
Capacitor (Electrolytic)	C_B	800µF, 63V	B41607A8807M2
Capacitor (Thin Film)	C_1, C_2, C_3	40µF, 400V ESR = 1.4mΩ	C4ATFBW5400A3NJ
Capacitor (Electrolytic)	C_{DC}	1000µF, 500V	LNC2H102MSEF

As discussed earlier, component selection is important for the output voltage regulation and efficiency of SC converters. The capacitors for the MMPVD stages are selected based on (19). Moreover, it is important to select capacitors with low *ESR* values to reduce the output impedance of the proposed SC converter. For that purpose, thin film capacitors are selected for the MMPVD stages as they have high ripple current rating and low *ESRs*. Electrolytic capacitors with ripple current rating of 10.3 A are used at the

output of the bidirectional boost stage and the output of the proposed bidirectional converter. The output voltage gain and efficiency of the MMPVD stage also depends on the MOSFET $R_{DS(on)}$ (as shown in Figure 20). Therefore, it is critical to select MOSFETs with low $R_{DS(on)}$.

Since the MMPVD topology has a multiphase operation, the optimal switching frequencies for the stages are selected such that the output impedance is minimized. Consequently, the voltage gain and efficiency of the MMPVD stage is maximized. From Figure 22, it can be observed that the voltage gain for the MMPVD stage for selected capacitors increases with frequency and the optimal frequency for the efficient operation of MMPVD is f = 10 kHz, i.e., the frequency of the first, second and third stages are 40 kHz, 20 kHz, and 10 kHz respectively. Therefore, increasing the frequency further would not increase the voltage gain by much. Furthermore, switch duty ratios for switches S_1 and S_2 are 45% with the same pulse width for all the MOSFETs.

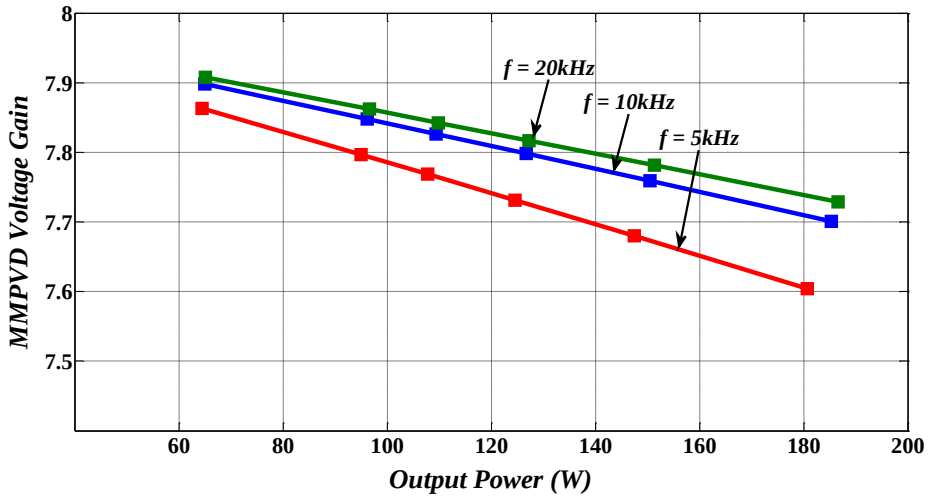

Figure 22. Simulated voltage gains of the MMPVD stage for different frequencies.

Figure 23 shows the measured voltage gain of the MMPVD stage for different frequencies at different loads. Figs. 24, 25 and 26 show the voltage across the MOSFETs in the first, second and third MMPVD stages respectively. It can be observed that the peak blocking voltages for the MOSFETs increases with each stage and is given by (24). The spikes in the voltage across the switches is due to the interconnect ESLs.

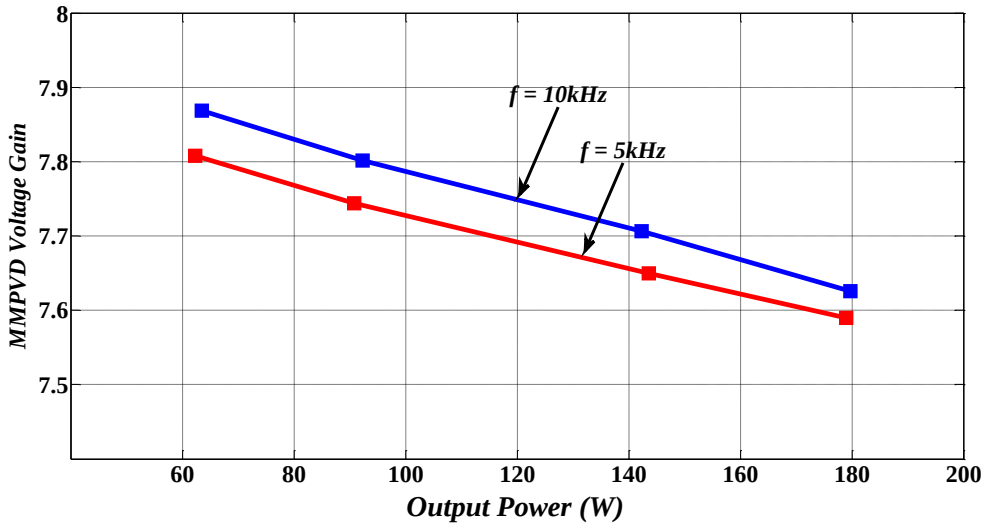

Figure 23. Measured voltage gain of the MMPVD stage.

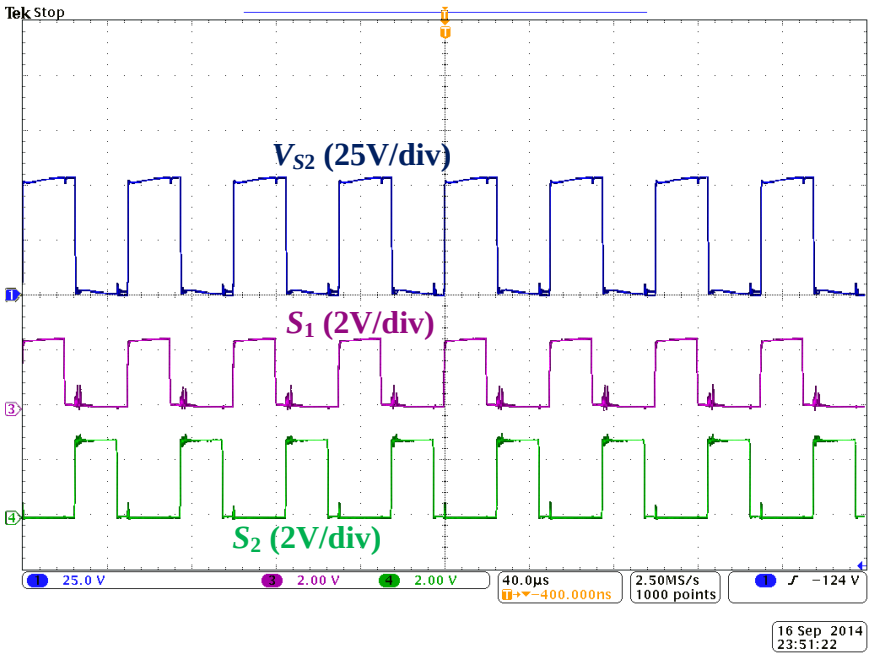

Figure 24. Voltage waveform across switch S_2.

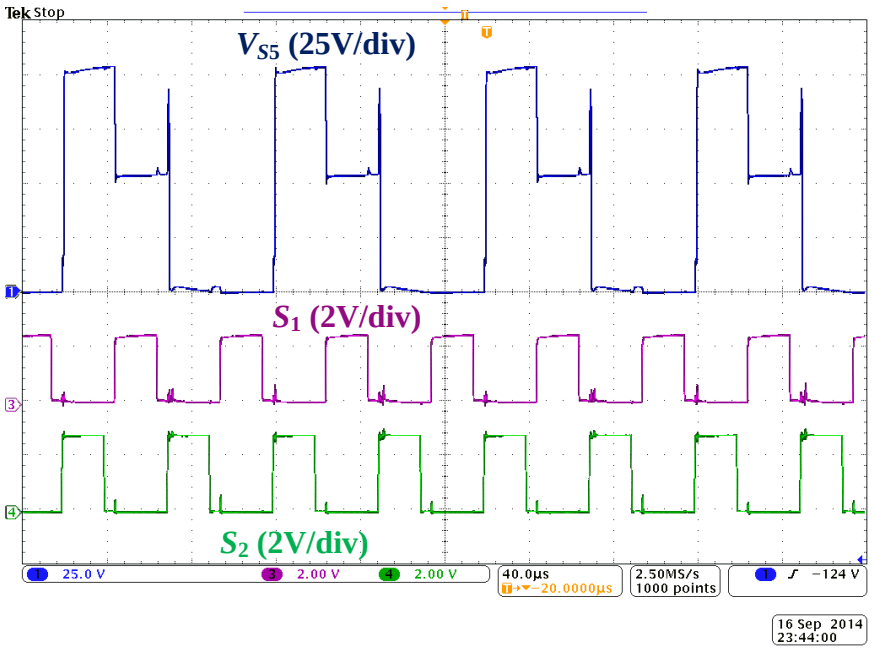

Figure 25. Voltage waveform across switch S_5.

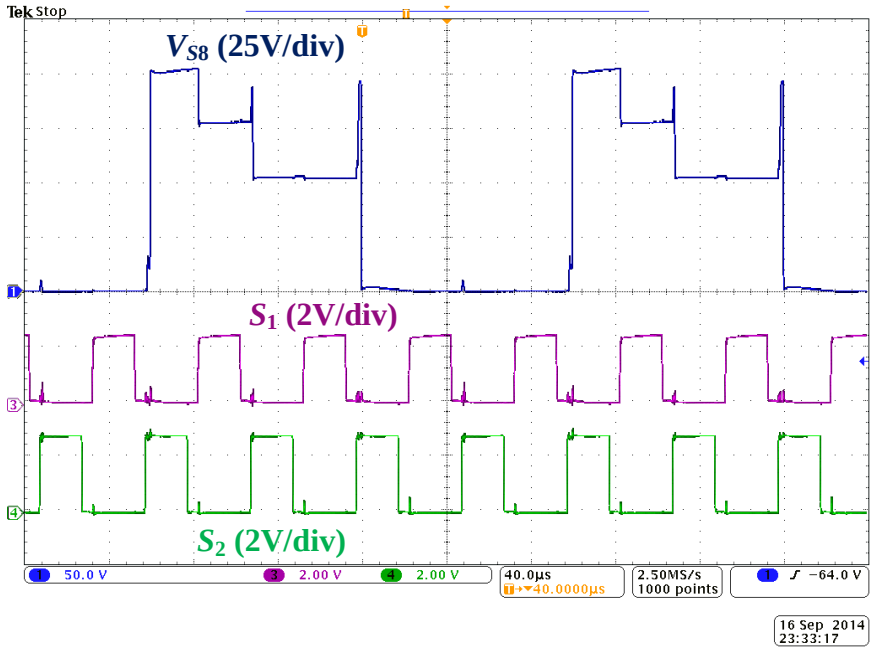

Figure 26. Voltage waveform across switch S_8.

In the forward power flow, the input source is connected to the bidirectional boost stage of the proposed converter and it operates in the boost mode. Moreover, a load of 800 Ω is connected at the output of the MMPVD stage (shown in Figure 21). From Figure 27, for input voltage V_{BATT} of 24 V, the voltage at the output of the proposed converter V_{DC} is maintained at 400 V by varying the duty cycle of switch S_A of the boost stage. Figure 28 shows the capacitor voltages of the MMPVD stage which is given by (20).

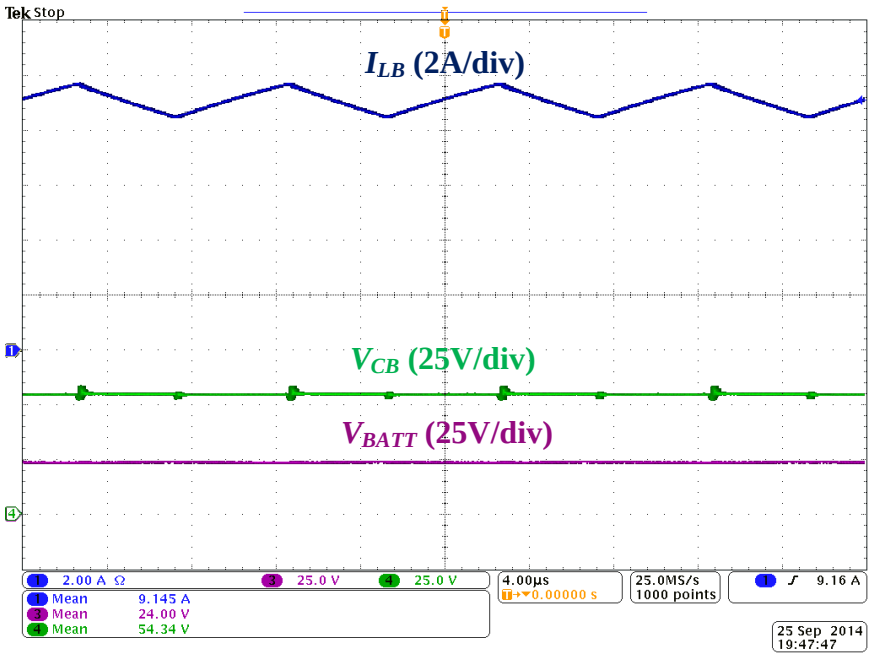

Figure 27. Boost stage inductor current i_{LB}, input voltage v_{BATT}, and output voltage v_{CB} waveforms in forward power flow.

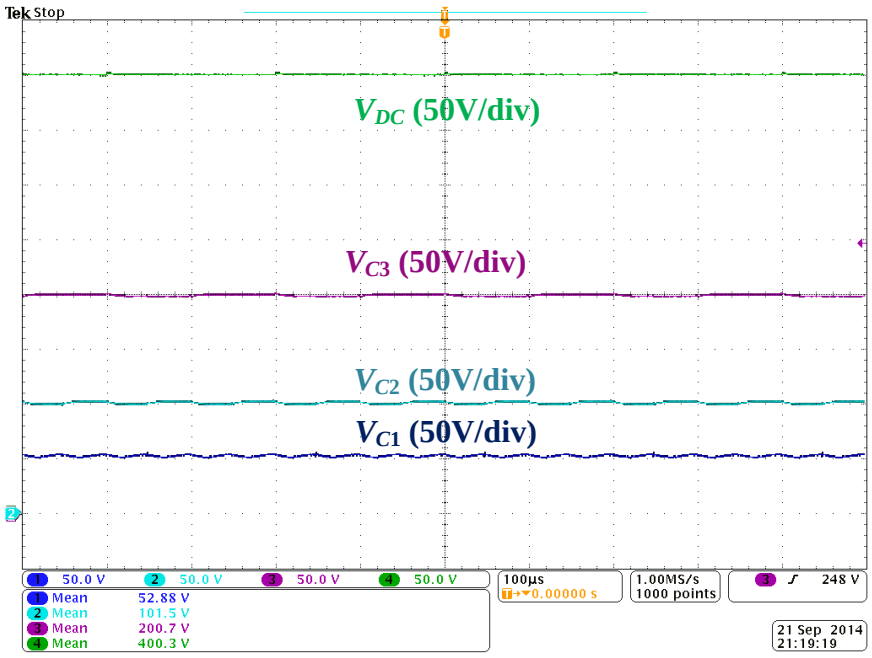

Figure 28. MMPVD input voltage v_{CB} and capacitor voltages v_{C1}, v_{C2}, and v_{C3} waveforms in forward power flow.

In the reversed power flow, the input source is connected to the MMPVD stage of the proposed converter and a load of 3.1 Ω is connected at the output of the bidirectional boost stage and it operates in the buck mode. For an input voltage V_{DC} of 400 V, the output voltage V_{BATT} is maintained at 24 V by varying the duty cycle of switch S_A of the buck stage. Figs. 29 and 30 show the capacitor and output voltages of the MMPVD stage and the buck stage respectively.

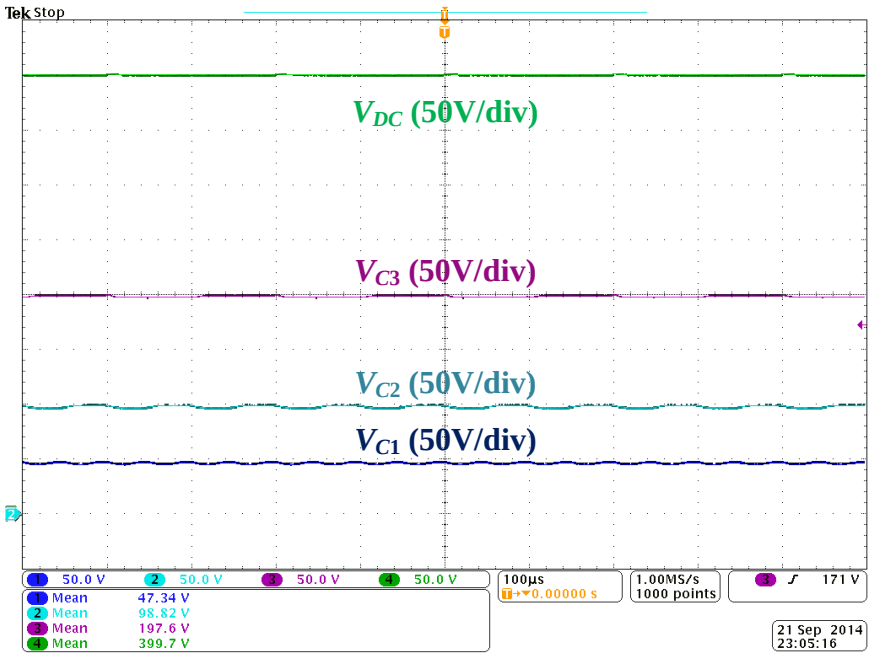

Figure 29. MMPVD input voltage v_{DC} and capacitor voltages v_{C1}, v_{C2}, and v_{C3} waveforms in reverse power flow.

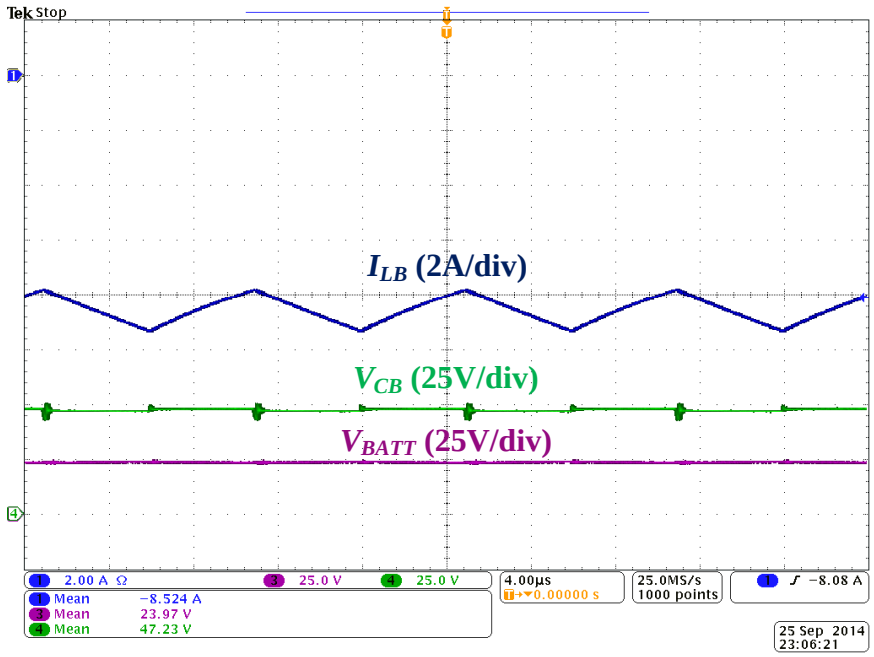

Figure 30. Buck stage inductor current i_{LB}, input voltage v_{CB}, and output voltage v_{BATT} waveforms in reverse power flow.

Figure 31 shows the efficiency of the proposed converter at different load levels. The measured efficiency of the proposed bidirectional converter for 200 W of output power is 90.5%. The maximum efficiency of the prototype is measured to be 92.9% at the output power of 133.6 W (shown in Figure 31).

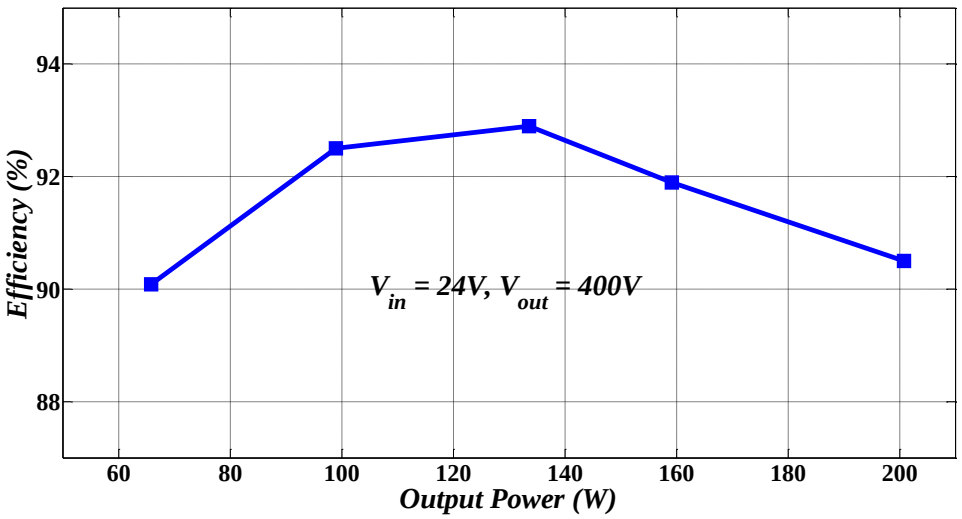

Figure 31. Measured efficiency of the proposed bidirectional converter.

VIII. Conclusion

In this paper, a high-voltage-gain bidirectional dc-dc converter has been proposed for energy storage and renewable energy applications. Such bidirectional dc-dc converters with high step-up/step-down voltage gains would improve the system reliability and are particularly useful for telecommunication and dc-microgrid applications. The proposed converter has a bidirectional boost stage cascaded with a 3-stage MMPVD for achieving higher voltage conversion ratios. The proposed MMPVD can achieve higher gains for lower parts count. The proposed switched capacitor converter has higher efficiency and power density with low component stresses. Moreover, bidirectional power flow can be achieved by minimal switch realization. The experimental prototype is built to validate the operation of the proposed converter.

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SECTION

2. CONCLUSION

In this dissertation, the advantages of dc distribution systems and their applications in the field of telecommunications, data centers, buildings, and microgrids has been reviewed. Selection of suitable voltage levels from system efficiency, cost, safety, and reliability standpoint has been discussed. Studies propose 380-Vdc to be the most suitable. Challenges regarding safety and protection system technology and suitable industry standard development have also been discussed. Secondly, a family of novel high gain dc-dc converters for dc microgrid applications has been introduced. The proposed converter has two boost stages at the input and is based on diode-capacitor VM stages. It can draw power from two input sources like a multiport converter or operate in an interleaved manner when connected to a single source. The voltage gain of the proposed converter is increased by increasing the number of VM stages. Since it is a dual input converter, power sharing and MPPT algorithms can be implemented independently at each input port. The experimental prototype is built to validate the operation of the proposed converter and an efficiency of 94.1% was achieved. Finally, a high-voltage-gain bidirectional dc-dc converter has been introduced which has high step-up/step-down voltage gains with continuous input/output current. The proposed converter has a bidirectional boost stage cascaded with a novel SC converter for achieving higher voltage conversion ratios. The proposed SC converter has the same circuit structure as that of a Fibonacci converter; however, it can achieve higher gains for a lower parts count due to

the multiphase switching scheme. Furthermore, bidirectional power flow can be achieved by minimal switch realization. The experimental prototype is built to validate the operation of the proposed converter and maximum efficiency of 92.9% was achieved for this converter. The proposed high gain dc-dc converters can be used for renewable energy and energy storage applications where each solar panel or battery cell can be individually linked to the 400-Vdc bus of a dc microgrid.

Future work can be done on developing average and small signal models for designing controllers for the proposed converters. Moreover, control strategies can be developed for implementing MPPT and power sharing algorithms for the proposed multiport converters with two independent sources. Integration of these converters in dc microgrid systems and their effects on the overall system stability and reliability can also be explored. Furthermore, efficiency of the proposed converters can be further improved by better design and PCB layout.

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VITA

Venkata Anand Kishore Prabhala was born on 12th October, 1981. He graduated from National Institute of Technology, Warangal (India) with a BSEE degree in 2005. He worked as a Project Engineer at Larsen & Toubro Ltd., India from 2005 to 2008. He completed his MSEE degree from Missouri University of Science and Technology (Rolla) in July 2010. He started his Ph.D. degree in January 2011 and graduated in December 2014 from Missouri University of Science and Technology (Rolla). His main research interests are design and control of multi-input and high-voltage-gain dc-dc power electronic converters and their application in dc microgrids. His other research interests include electric drives and application of power electronics in power systems.