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Advanced control of grid-connected multilevel power electronic rectifiers

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ADVANCED CONTROL OF GRID−CONNECTED MULTILEVEL POWER ELECTRONIC RECTIFIERS

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This dissertation consists of the following three articles:

Paper I, Pages 14−37, "Phase-Shifting Reference Strategy for Voltage Balancing in Neutral-Point Clamped Converter," to be summited in *IEEE Transactions on Power Electronics*.

Paper II, Pages 38−53, "Capacitor Voltage Regulation and Pre-Charge Routine for a Hybrid Multilevel Rectifier," to be summited in *IEEE Transactions on Power Electronics*.

Paper III, Pages 54−70, "Multiple Reference Frame-Based Harmonic Compensation for Grid Currents in the Three Phase Hybrid Multilevel Rectifier," to be summited in *IEEE Transactions on Power Electronics*.

ABSTRACT

Multilevel power electronic converters have been gaining attention due to their ability to supply high amounts of power and to handle high voltage levels. In this dissertation, grid connected AC−DC rectifier application is investigated with different topologies and control scheme.

At first, neutral point clamped (NPC) rectifier is employed to transfer power from the grid to the load. The NPC rectifier has two capacitors in order to build multilevel output voltage. However, it causes voltage unbalancing problem. Therefore, the new method has been proposed to regulate each capacitor voltage at the same voltage level. Experimental results show that it is effective to balance capacitor voltages of the NPC and it can improve total harmonic distortion (THD) of the grid current as a result.

Furthermore, 7 voltage levels can be achieved by using hybrid multilevel rectifier which consists of an NPC and cascaded H-bridges (CHB). Because the hybrid multilevel rectifier has total 8 capacitors which are completely discharged at first, large inrush currents from the grid might cause hazards. Therefore, the paper develops a pre-charge routine for building it up to steady state operation in which unity power factor control (PFC) and load voltage control are achieved.

Finally, multiple reference frame theory (MRF) is used to improve THD of the grid currents when the hybrid multilevel rectifier is connected with distorted grid voltage source. After calculating 5th harmonic of the grid current in real time, the voltage reference for the hybrid multilevel rectifier will be compensated in a feedback loop. Experimental results show validity in improving THD of the grid currents.

ACKNOWLEDGEMENTS

I would never have been able to finish my dissertation without the guidance of my committee members, help from friends, and support from my family. Especially for my advisor Dr. Mehdi Ferdowsi, I cannot express enough thanks to him for his continued support and encouragement. He has suggested not only solutions when I encountered problems during building up the experimental set, but also research topics that need me to develop new knowledge and technology. That made me study hard and finally gave me an opportunity to achieve better results. I would like to express my deepest gratitude to my advisor, Dr. Mehdi Ferdowsi, for his excellent guidance, caring, patience, and providing me with an excellent atmosphere for doing research.

I would like to thank Dr. Keith Corzine, who taught me the basic knowledge of power electronics and motor drives. Especially, I learned the concept of the multiple reference frame theory experience in the class. Therefore, it finally helped me apply the theory on grid current harmonic compensation. I would also like to thank Dr. Crow, Dr. Kimball, Dr. Sarangapani and Dr. Balakrishnan for guiding my research for the past several years and helping me to develop my background in power system engineering and optimal theory.

I would also like to thank my parents. They were always supporting and encouraging me with their best wishes and trying to rescue me from my deep loneliness. Also, I would like to appreciate encouragement and positivity from my brother, sister-in-law, my sister and brother-in-law.

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1. INTRODUCTION

Because of technical limitations on producing high-voltage semiconductor devices with fast switching capabilities, multilevel topologies using low switching frequency schemes have been accepted as the dominant approach in high power applications. However, output current distortion and physically heavy filters have been continuously reported as serious problems associated with these converters. Keeping the pace with the progress in producing semiconductor devices with medium voltage ratings and fast switching characteristics, various high frequency switching schemes for multilevel power conversion systems have been suggested in order to satisfy total harmonic distortion (THD) regulations on grid currents and to reduce overall weight of the system in high power multilevel applications [1]−[3].

1.1. APPLICATIONS

Renewable energy sources have been considered as alternative resources for electric power generation. Well-known two-level converters achieve good performance in medium power applications for providing power from the renewable source to utility grid or electric motors. On the other hand, in high power application in which switches should handle high voltage and the power circuit should produce low total harmonic distortion (THD) of grid currents, multilevel power converter topologies are more attractive. Figure 1.1. that is captured from [4] shows multilevel converters application. Multilevel converters can be used in utility interfacing applications because its multilevel output

voltages help improve THD of grid currents in applications such as static synchronous compensators (STATCOM), Active Filters and flexible alternating current transmission

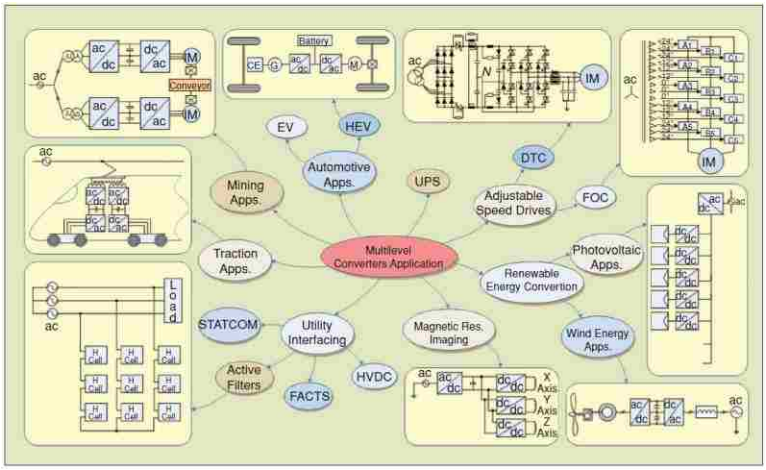


Figure 1.1. Multilevel converter application overview

systems (FACTS). Electric locomotive uses high voltage to provide high power to AC motors. Therefore, recently multilevel converters have been applied instead of using low frequency switching scheme with semiconductor switches like Thyristors. In PV application, multiple numbers of panels will be placed in arrays. Then each panel will have power converters to provide power to the utility grid in a way depicted in Figure 1.2. [5]. With this application, multilevel power conversion topologies will be more useful to combine all the electric energy and to provide it to the utility. The low-speed permanent-magnet generator is designed to have a large number of poles with multiple wounds as depicted in Figure 1.3. [6]. In this case, the power-electronic building block (PEBB) can be placed between the grid and the wind turbine. Increasing the nominal power of wind-

turbines is the current trend on the market. This makes the multilevel converter suitable for modern high-power wind-turbine applications. Recently along with the smart grid system in which the price of electricity is determined based on supply and demand in real time, energy storage system (ESS) has been gaining attention in peak-shaving application. Thus, electrical power will be stored in batteries at night time from the grid when the price of electricity is low because the overall demand is low. Then, the electrical energy stored in the battery can be used at daytime when the price of electricity is high. Therefore, factories or large buildings that consume large electricity everyday might prefer to equip with the ESS to save cost on electricity in long term. In the perspective of the electrical power provider, the ESS can be helpful to increase power security by doing peak-shaving and valley-filling [7] as described in Figure 1.4. In these high power applications, multilevel power conversion system will offer practical solutions.

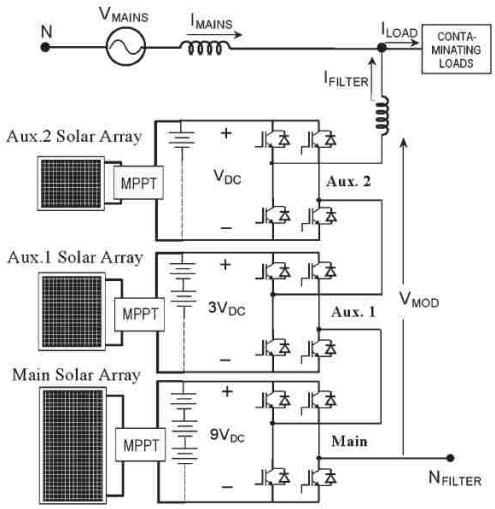


Figure 1.2. Multilevel converter in PV application

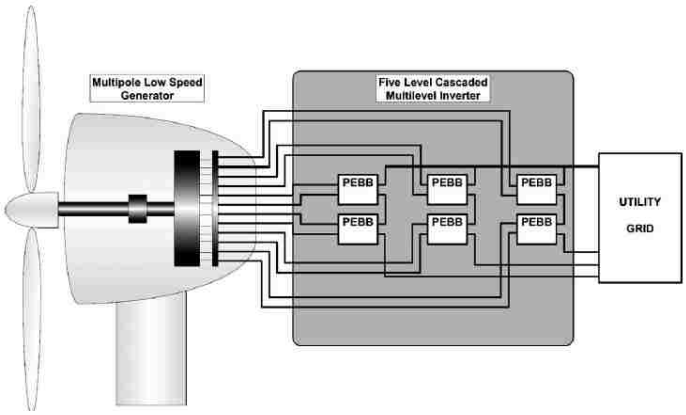


Figure 1.3. Five-level cascaded multilevel converter connected to a multiple pole low-speed wind-turbine generator

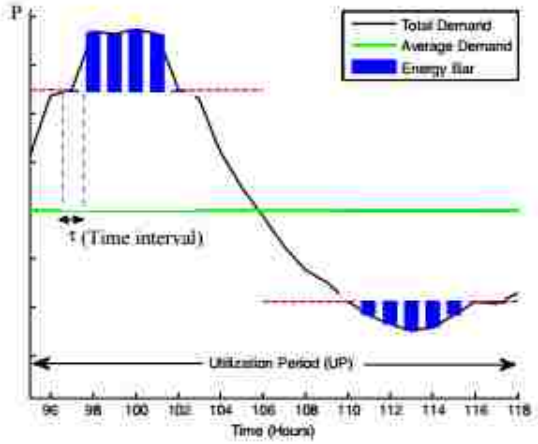


Figure 1.4. Peak shaving and valley filling

1.2. MULTILEVEL CONVERTER TOPOLOGIES

Multilevel topologies can be largely categorized into neutral point clamped (NPC or diode clamped) [8]−[11] as described in Figure 1.5., flying capacitors (capacitor clamped) [12]−[16] shown in Figure 1.6., cascaded H-bridges (CHB) [18]−[19] depicted

in Figure 1.7., and hybrid [20], [21] as represented in Figure 1.8. Recently, hybrid topologies have been suggested to combine an NPC and cascaded H-bridges in series.

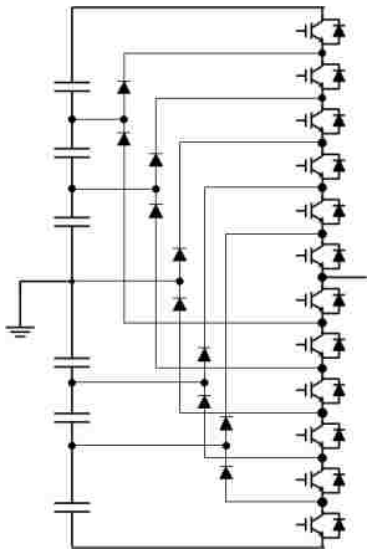


Figure 1.5. Neutral point clamped multilevel topology

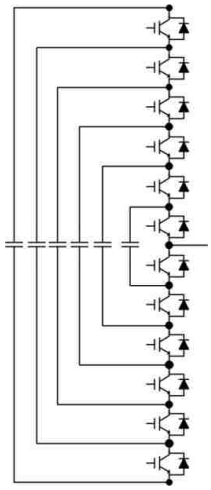


Figure 1.6. Flying capacitor multilevel topology

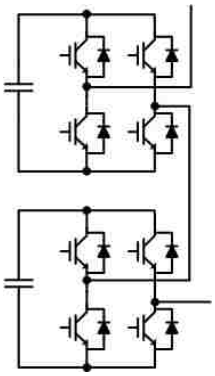


Figure 1.7. Cascaded H-bridge multilevel topology

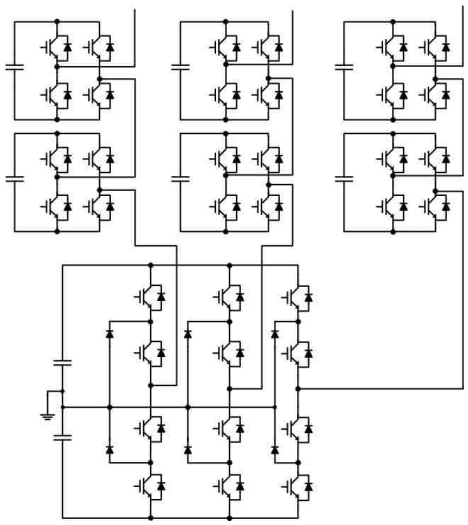


Figure 1.8. Hybrid multilevel topology

1.3. MODULATION METHODS FOR MULTILEVEL CONVERTERS

Various modulation methods have been suggested and developed including selective harmonic elimination [22]−[26], selective harmonic elimination pulse width modulation (PWM) [27]−[32], asymmetric modulation [33], asymmetric PWM [34], sub-harmonic elimination PWM [35]−[37], and hybrid modulation [38]−[40]. The selective harmonic elimination as shown in Figure 1.9. is called stepped waveform modulation. Main and series cells are operating with stacked square waveforms in a way that a group of switching angles of θ according to a reference eliminates a specific low harmonic. Therefore, it usually has a look-up table formed by calculation with a Fourier series equation in advance of an experiment. In Figure 1.10., selective harmonic elimination PWM is a similar method but it chops down a square waveform several times so that it removes several low harmonics. Asymmetric modulation in Figure 1.11. and asymmetric modulation PWM in Figure 1.12. are similar methods except that the strategy to make

voltages in each cell is different. The methods described in Figure 1.9.-1.12. are all based on low switching frequency. Sub-harmonic elimination modulation uses high switching frequency so that an output voltage of a multilevel inverter has no low frequency harmonics except switching frequency harmonics.

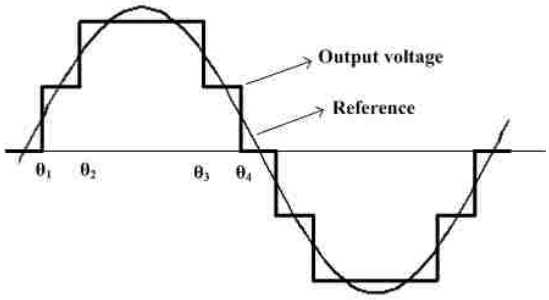


Figure 1.9. Selective harmonic elimination method

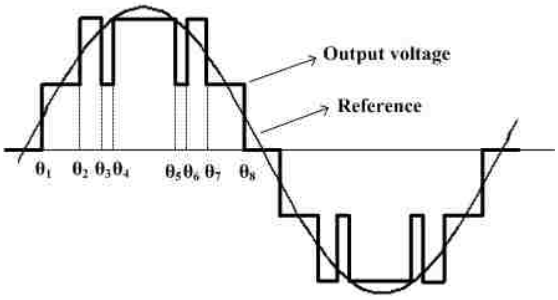


Figure 1.10. Selective harmonic elimination PWM method

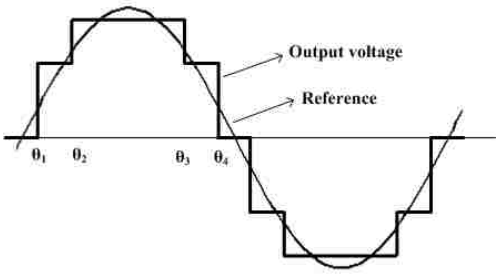


Figure 1.11. Asymmetric modulation method

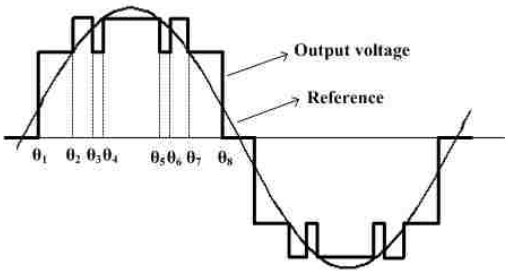


Figure 1.12. Asymmetric PWM method

1.4. NEW VOLTAGE BALANCING METHOD FOR NPC

In paper I, the three phase NPC topology is used in a grid connected rectifier. In the three-level NPC topology, there are two dc link capacitors which equally split the dc voltage. The two dc link capacitors are charged by the grid current coming from the grid. Therefore, with distorted grid currents, the NPC topology may suffer from capacitor voltage differences since the average neutral current flowing into and out of the neutral point of the dc link may not be zero, especially, during transients. The proposed voltage balancing method separates one sinusoidal reference into upper and lower references. Then, the upper and lower references are shifted to opposite directions. By charging the two NPC capacitors with different amount of grid currents, it balances them effectively. Simulation and experimental results verify the proposed voltage balancing method.

1.5. PRE-CHARGE ROUTINE FOR HYBRID MULTILEVEL RECTIFIER

In the paper II, a three phase hybrid multilevel topology is employed to provide power from the grid to the resistive load. The hybrid multilevel topology has an NPC and CHBs which are modulated with a hybrid modulation method. Selective harmonic elimination method will modulate the NPC with 60Hz switching frequency. Then semiconductor devices of CHBs will be switched with high switching frequencies. Since the hybrid multilevel rectifier has many capacitors that are completely discharged at the beginning of the operation, large inrush currents will come from the grid at start-up. Therefore, this paper proposes a start-up routine for the hybrid multilevel rectifier to be landed safely on a steady state condition. Along with the start-up procedure, this paper

also considers the three main goals in a grid connected rectifier application: 1) unity power factor control (PFC), 2) load voltage regulation and 3) capacitor voltage regulation of CHBs which are connected in series with the NPC. Control block diagrams and phasor diagrams explain not only the pre-charge routine but also control methods for the three main goals with details. Simulation and experimental results show the verification of the proposed method.

1.6. GRID CURRENT HARMONIC COMPENSATION BY USING MRF

Grid current harmonic compensation by using MRF for the hybrid multilevel rectifier is discussed in the paper III. In a practical application of grid connected power converters, grid voltage sources are a little bit distorted for various reasons. Thus with distorted grid voltage sources, grid connected rectifier might draw distorted grid currents from the grid to the converter. Therefore, this paper suggests a method for compensating the 5th harmonic of grid currents by using multiple reference frame theory for the hybrid multilevel rectifier. The grid currents resulted by the rectifier are analyzed with the multiple reference frame theory to extract only 5th harmonic. Then, magnitude and phase value at 5th harmonic frequency in a Bode plot will be used to convert the calculated 5th harmonic to the voltage references which modulate the hybrid multilevel rectifier. The feedback control loop for accomplishing load voltage control and unity PFC is explained with block diagrams. Simulations and experimental results show the verification of the suggested method.

PAPER

I. PHASE-SHIFTING REFERENCE STRATEGY FOR VOLTAGE BALANCING IN NEUTRAL-POINT CLAMPED CONVERTER

***Abstract*— This paper suggests a new method to balance two capacitor voltages in the three-level neutral-point clamped (NPC) converter. Usually, a carrier-based PWM method using a sinusoidal reference and two carriers is employed to run a three-level NPC converter. In this paper, the single reference is separated into upper and lower references. By creating a slight phase shift between these two references, the proposed method is able to balance two NPC capacitor voltages. In most conventional approaches, capacitor charging time is controlled in a way of manipulating pulse width in NPC output voltages. However, in the proposed method, capacitor charge/discharge is achieved by moving the upper and lower portions of the NPC output voltage toward/away from the grid peak current. The new voltage balancing technique is compared with the existing traditional methods and verified by simulation and experimental results.**

I. INTRODUCTION

In high power applications, it is difficult to use two-level converters because of the limited voltage rating on IGBTs or MOSFETs. Therefore, multilevel converters have been considered as an alternative topology in such applications [1]. Neutral point clamped (NPC) and cascaded H-bridge (CHB) converters are preferred to flying capacitor (FC) topologies as there is a difficulty in balancing flying capacitor voltages [2].

Also, in a three phase rectifier application, CHB needs isolated DC/DC converters to create each floating voltage that feeds the H-bridges. This is more expensive and bulky. On the other hand, in the three-level NPC topology, there are two dc link capacitors which equally split the dc voltage. The NPC topology may suffer from capacitor voltage differences. NPC converters have inherent unbalanced capacitor voltage problems since the average neutral current flowing into and out of the neutral point of the dc link may not be zero, especially, during transients [3], [4]. Also, distorted ac currents (linear imbalance) and a nonlinear load can cause voltage imbalance on the NPC inverter in motor drive application [31]. In addition, aging parameter variations and temperature may cause a drift in the value of the capacitors. Unequal values for capacitors will aggravate the voltage imbalance issue. As a result, many literatures have suggested methods to resolve this problem.

One of the suggested methods is to place additional circuits between dc link capacitors and the load [5]–[8]. With this method, the control strategy for the NPC is simple and easy to implement. However, it requires additional semiconductor switches and inductors. Therefore, it increases the overall costs and power losses. Another suggested method is to use the SVPWM (space vector pulse width modulation) strategy [9]–[16]. With SVPWM, one can use redundant switch states in order to make the average neutral current zero. So the SVPWM strategy allows balancing the two capacitor voltages effectively. However, this method requires some time to analyze every switching situation. Only after rigorous analysis on every switching state, one can apply SVPWM on balancing the two capacitor voltages. Also, many methods have been recommended based on SPWM (sinusoidal PWM) [17]–[24]. Although each method is

processed based on difference information, conceptual approach is same. There, voltage balancing is accomplished by injecting offset signal to a reference signal. Additionally, a different concept called multicarrier PWM strategy has been suggested [25]–[27]. There, triangular carriers are changed in ways of level-shifted carrier PWM or phase-shifted carrier PWM. In [26], the amplitudes of the triangular carriers are variable through a feed−forward compensation loop but the carriers have fixed phase differences. On the other hand, the phase difference between carriers will be determined by a pre-calculation while they have fixed peak amplitude [25], [27]. The common strategy of the offset injection method and the feed−forward compensated multicarrier PWM is to control the charging time of the target capacitors based on the severity of voltage imbalance. In these cases, the voltage unbalance problem is resolved by generating narrower or wider pulses depending on how the voltages are unbalanced.

In a situation operating near over-modulation region with the two conventional methods, a system might experience over−modulation because they manipulate pulse width by adding an offset to a reference or changing the magnitude of carriers. Rather than changing the width of the PWM pulses, the phase-shifting reference (PSR) method overcomes the voltage unbalance problem by moving the PWM pulses toward or away from the peak of grid currents. So it can naturally avoid over-modulation. Also, THD of the grid current gets slightly better since the balanced voltage by the proposed method increased the magnitude of the NPC output voltage at fundamental frequency.

The remainder of this paper is organized as follows. Section II explains why two reference signals are necessary to balance two capacitor voltages in the NPC. Then, simple simulation results describe a strategy of the PSR method in section III. Then

section IV explains an overlap and gap period which occurs in the PSR method. Section V shows a feedback control block diagram which output adjusts phase angle of two reference signals. In section V, experiment and simulation setting is explained and listed with details. It contains pictures and block diagrams which indicates the whole procedure of the experiment. Then waveforms from simulation and experiments prove the validity of the PSR method.

II. SWITCHING SCHEME AND TWO REFERENCE SIGNALS OF THE NPC TOPOLOGY

Figure 1. shows a three-phase neutral-point clamped AC/DC rectifier that is used in this paper. $S_{a1}, \overline{S_{a1}}$ and $S_{a2}, \overline{S_{a2}}$ are switch pairs in phase A. Table 1. demonstrates the relationship between the switch states and output voltage V_{u0}. If switches $\{ S_{a1}, S_{a2}, \overline{S_{a1}}, \overline{S_{a2}} \}$ are {On On Off Off}, then node u will be connected to node 2. In this case, V_{u0} would equal to V_{dc1}. The circuit of this switch state is described as mode (a) in Figure 2-(a). In mode (b) described in Figure 2-(b)., V_{u0} becomes 0. Similarly, the output voltage V_{u0} voltage would be $-V_{dc2}$ in the event of {Off Off On On} for switches $\{ S_{a1}, S_{a2}, \overline{S_{a1}}, \overline{S_{a2}} \}$ which relates to mode (c) of Figure 2-(c). With the assumption that V_{dc1} and V_{dc2} are constant, the switching scheme can be explained easily using Figure 3. There are upper and lower reference signals that are compared with carriers. Then on-off status of switches $\{ S_{a1}, S_{a1}, \overline{S_{a1}}, \overline{S_{a1}} \}$ are determined by

$$
\begin{aligned}
&\text{if } V_{upper\_r} > V_{upper\_tri} \quad \text{then } s_{a1},\ \overline{s_{a1}} \Rightarrow \{\text{On Off}\},\\
&\quad V_{upper\_r} < V_{upper\_tri} \quad \text{then } s_{a1},\ \overline{s_{a1}} \Rightarrow \{\text{Off On}\},\\
&\text{if } V_{lower\_r} > V_{lower\_tri} \quad \text{then } s_{a2}, \overline{s_{a2}} \Rightarrow \{\text{On Off}\},\\
&\quad V_{lower\_r} < V_{lower\_tri} \quad \text{then } s_{a2}, \overline{s_{a2}} \Rightarrow \{\text{Off On}\}
\end{aligned}
\tag{1}
$$

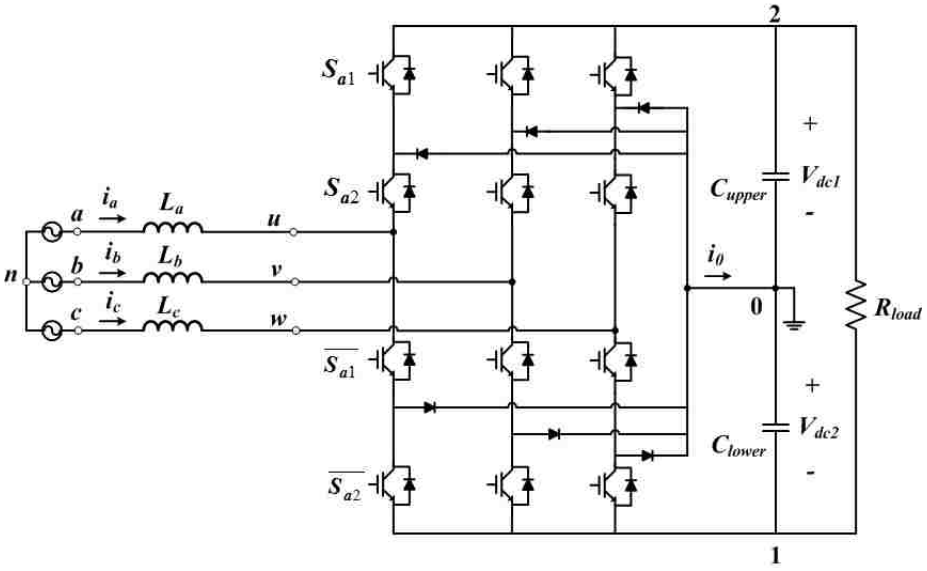
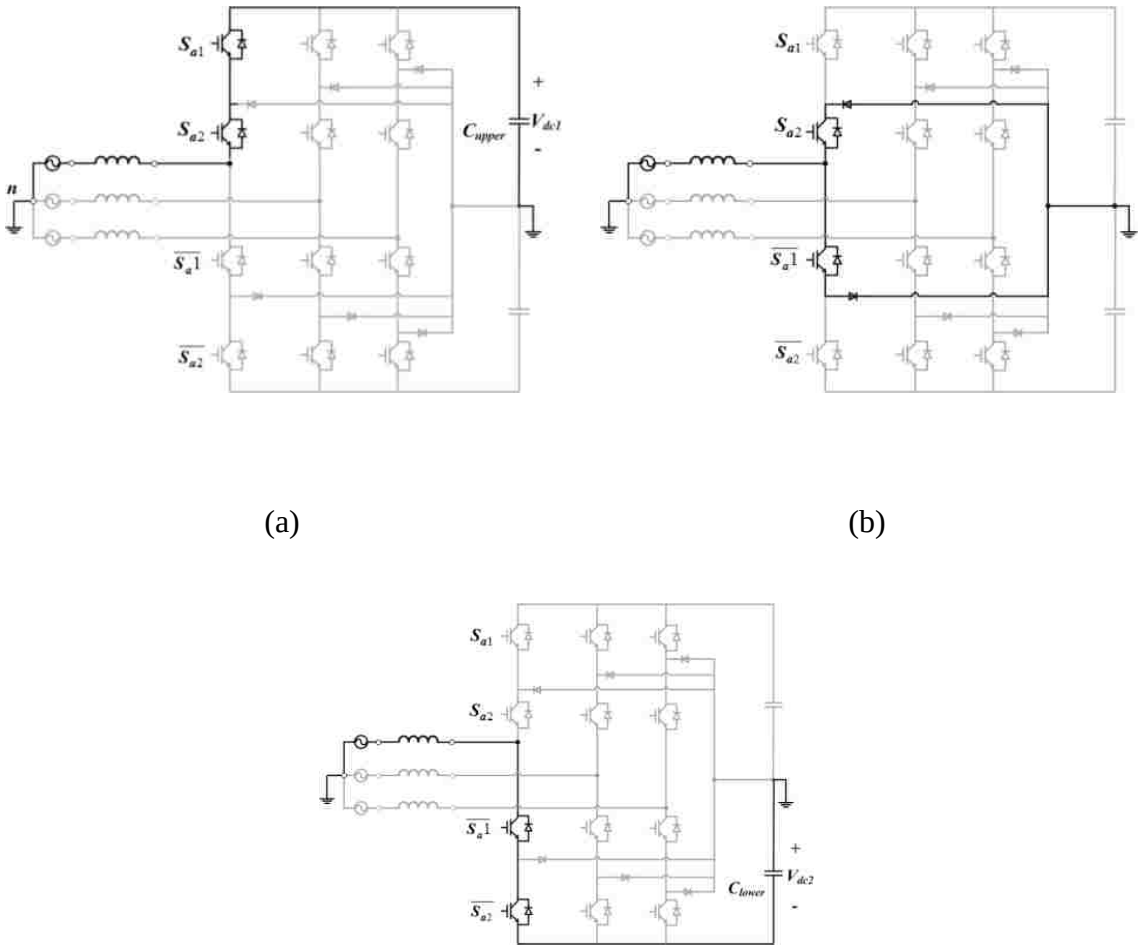


Figure 1. Three-phase neutral-point clamped AC/DC rectifier

Table 1. Three Level of Output Voltage According to Switch State

Switch State $\{ s_{a1}, s_{a2}, \overline{s_{a1}}, \overline{s_{a2}} \}$	**Output V_{u0}**	**Connection**	**Mode**
{On On Off Off}	V_{dc1}	2	(a)
{Off On On Off}	0	0	(b)
{Off Off On On}	$-V_{dc2}$	1	(c)



(a) (b)

(c)

Figure 2. Three modes of switching in a case of phase A : (a) when { s_{a1}, s_{a2}, $\overline{s_{a1}}$,$\overline{s_{a2}}$ } are {On On Off Off}, (b) when { s_{a1}, s_{a2}, $\overline{s_{a1}}$,$\overline{s_{a2}}$ } are {Off On On Off}, (c) when { s_{a1}, s_{a2}, $\overline{s_{a1}}$,$\overline{s_{a2}}$ } are {Off Off On On}

Figure 3. also shows a typical output voltage V_{u0} which has 3 levels. It can be seen that mode (a) and (b) are alternating during the first half cycle, which is related to the upper capacitor voltage V_{dc1}. As a result, if modes (a) and (b) are managed during the first half cycle, V_{dc0} can be controlled. Similarly, one can control V_{dc2} by managing

modes (b) and (c) during the second half of the cycle. Therefore, two separate reference signals are needed to balance both capacitor voltages.

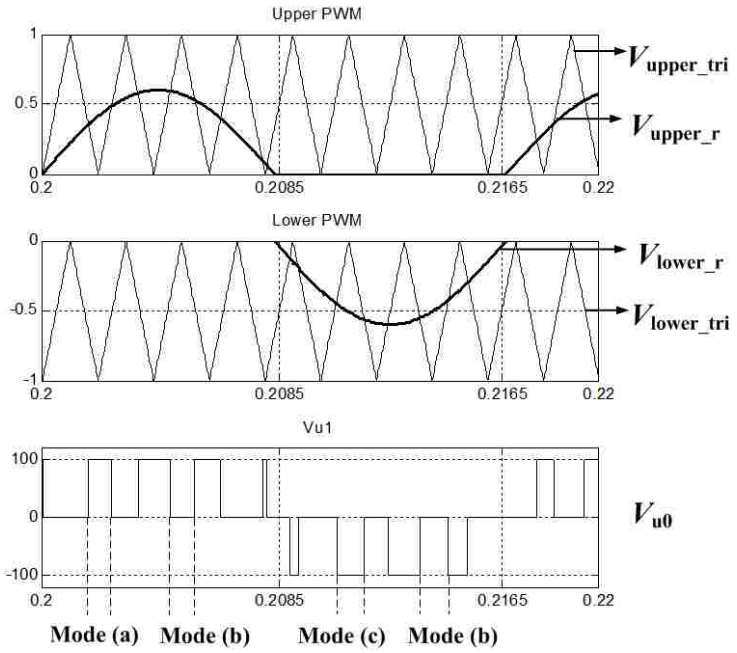


Figure 3. Two reference signals and the output V_{u0}

III. PHASE-SHIFTING REFERENCE STRATEGY

Figure 4. describes the PSR strategy for balancing the two NPC capacitor voltages. The solid sinusoidal waveforms are the original reference signals while the dotted waveforms are phase-shifted reference signals. With the proposed PSR strategy, the upper and lower references move to the right or the left based on the *phase_compensation* value by using (2) and (3). The *phase_compensation* value is an outcome of a closed loop, which is explained with block diagrams and codes in section V.

$$
\begin{aligned}
\boldsymbol{upper\_m_a} &= \boldsymbol{m} \times \cos(\theta \quad \mp \boldsymbol{phase\_compensation}) \\
\boldsymbol{upper\_m_b} &= \boldsymbol{m} \times \cos(\theta - \frac{2}{3}\pi \ \mp \boldsymbol{phase\_compensation}) \\
\boldsymbol{upper\_m_c} &= \boldsymbol{m} \times \cos(\theta + \frac{2}{3}\pi \ \mp \boldsymbol{phase\_compensation})
\end{aligned} \tag{2}
$$

$$
\begin{aligned}
\boldsymbol{lower\_m_a} &= \boldsymbol{m} \times \cos(\theta \quad \pm \boldsymbol{phase\_compensation}) \\
\boldsymbol{lower\_m_b} &= \boldsymbol{m} \times \cos(\theta - \frac{2}{3}\pi \ \pm \boldsymbol{phase\_compensation}) \\
\boldsymbol{lower\_m_c} &= \boldsymbol{m} \times \cos(\theta + \frac{2}{3}\pi \ \pm \boldsymbol{phase\_compensation})
\end{aligned} \tag{3}
$$

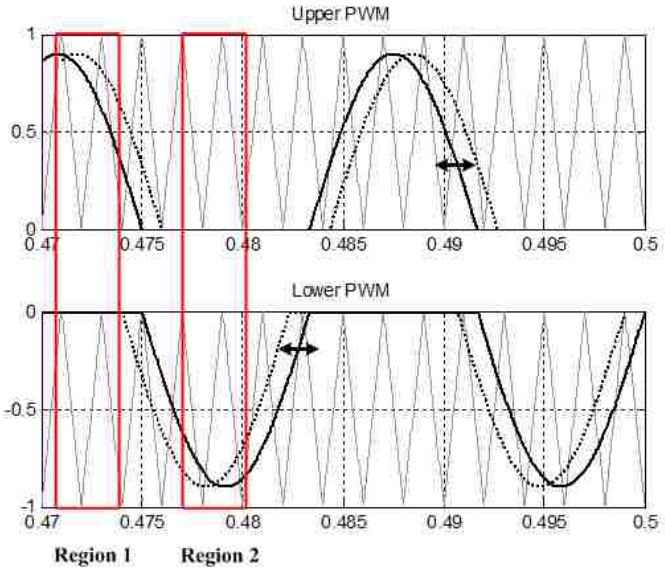


Figure 4. PSR strategy with upper and lower reference signals

The plus and minus signs in front of *phase_compensation* in (2) and (3) can be changed according to inverter or rectifier application. To show the concept of controlling target voltages using the proposed method, a simulation is carried out using only one phase of the NPC rectifier. The simulation circuit has an ideal current source i_a replacing the inductor for the purpose of removing the effect of the distorted grid current on the two capacitor voltages. Also, the switching frequency is chosen to be 500 Hz for the simulation to show better graphical PWM action. As a starting point before applying any

voltage balancing method, simulation conditions are intentionally selected for V_{dc1} and V_{dc2} to have the same average value in Figure 5.

After applying +0.2/−0.2 rad. (11.5°) of *phase_compensation*, the upper reference signal moves toward/away from the upper peak of the grid current I_a while the lower reference signal is shifted away from / toward the bottom peak of the grid current I_a as shown in Figure 6. / Figure 7. It is worth mentioning that the angle 0.2 rad. is much larger than practical cases. Since the charging current delivered to the C_{upper}/C_{lower} has been increased/ decreased, V_{dc1} goes higher than V_{dc2} as depicted in Figure 6. This explanation also applies on the result in Figure 7. Since the PSR method shifts the two references to right or left, not up or down, it can naturally avoid over-modulation. Over-modulation can degrade grid current THD [30].

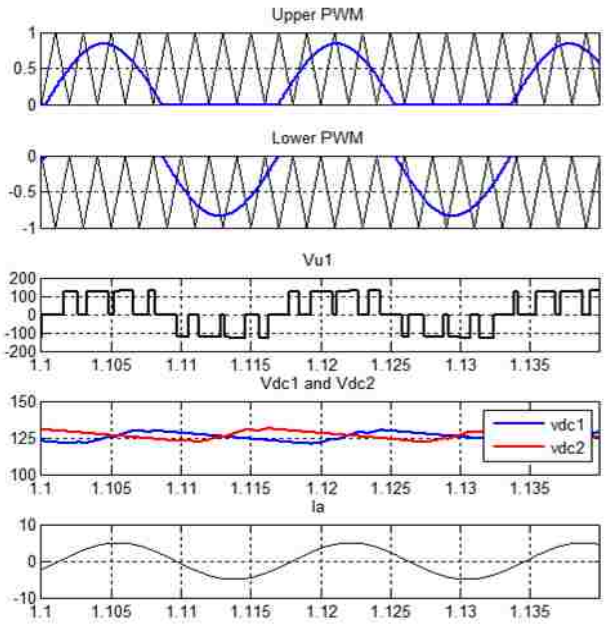


Figure 5. Simulation result when applying no voltage balancing method

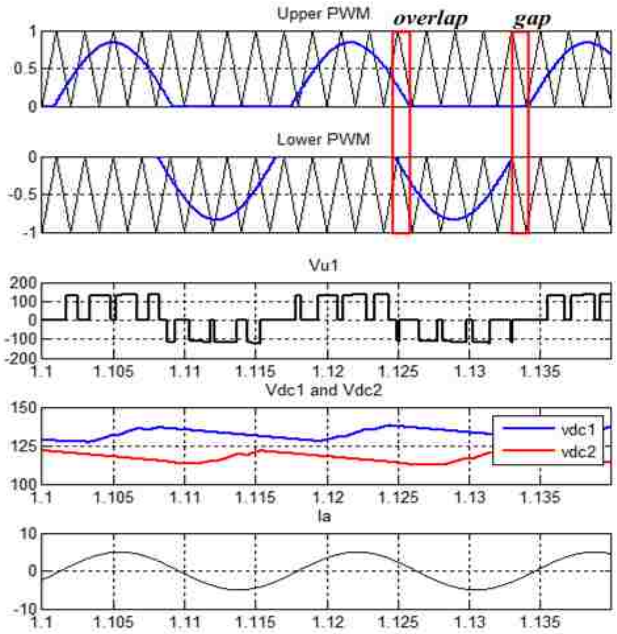


Figure 6. Two capacitor voltages when applying +0.2 rad. (+11.5°) as *phase_compensation* on (2) and (3)

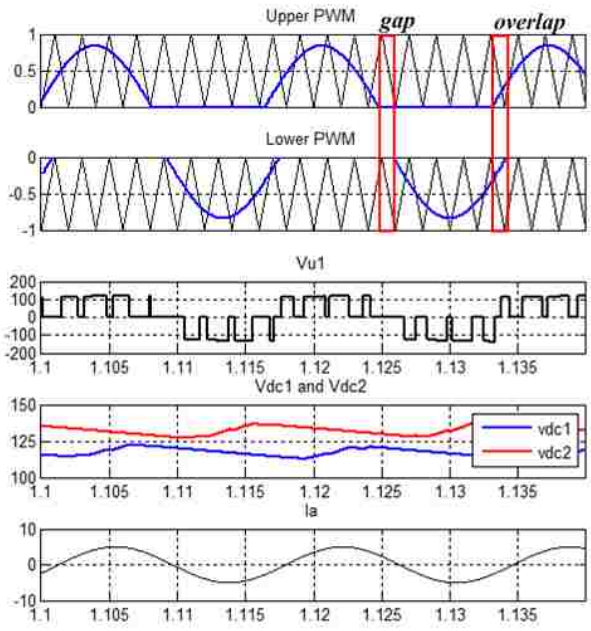


Figure 7. Two capacitor voltages when applying −0.2 rad. (−11.5°) as *phase_compensation* on (2) and (3)

IV. OVERLAP PERIOD HAPPENING IN PHASE-SHIFTING REFERENCE

As the upper and lower references shift to right or left, an overlap and a gap period will be occurred as shown in red rectangles in Figures 6.-7. In order to show switch state during the overlap period, a simple simulation is conducted with the same conditions except an actual switching frequency of 6 kHz. Figure 8. shows the switch state transition during the overlap period that is indicated in the red rectangle in Figure 7.

Normally, as described in Figures 3.-4., switching mode alternates between two modes. However, during the overlap period, switch mode will be changing between three modes. When the *phase_compensation* value becomes −0.7 rad. (−40°) for an impractical case as presented in Figure 9., switch state should transit from mode (a) to mode (c) instantly. Therefore, an arm short hazard may occur because it requires all of the four switches to turn on or off simultaneously. As long as the *phase_compensation* value is within ± 0.53 rad. (±30°) as a worst case when the peak reference is 1, the system will be safe from the hazard. In order to avoid extreme cases, the *phase_compensation* value is limited within ±0.06 rad. (3.44°) in the DSP code. In a practical case during a steady state, the *phase_compensation* is usually smaller than 0.01 rad. (0.57°). Therefore, the gap and overlap period do not persist for a long time.

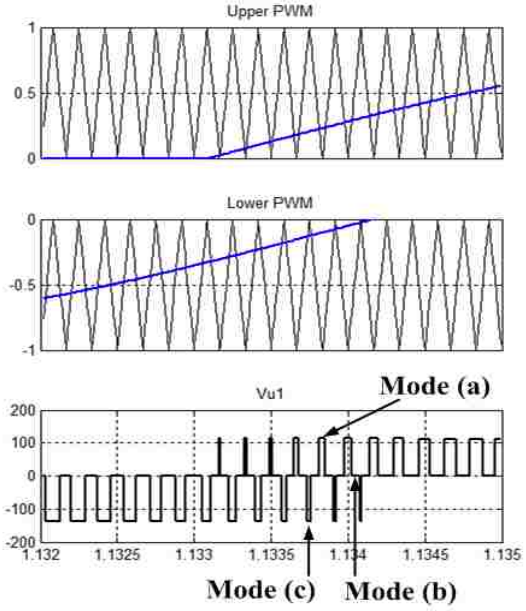


Figure 8. Overlap period when applying −0.2 rad. (−11.5°) as *phase_compensation* on (2) and (3)

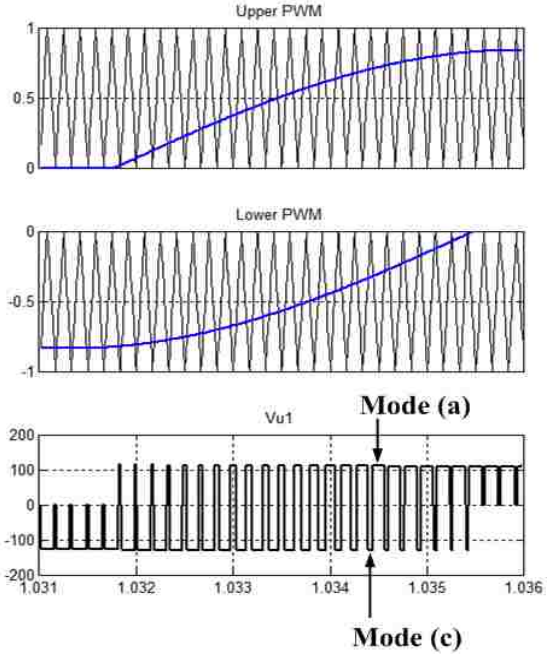


Figure 9. An impractical case of the overlap period with −0.7 rad. (−40°) of the *phase_compensation*.

V. PHASE COMPENSATION CONTROL LOOP

Figure 10. shows the feedback control loop in which *phase_compensation* is generated. For balancing V_{dc1} and V_{dc2} equally, the reference of the control loop is zero. Voltage difference between V_{dc1} and V_{dc2} is fed back to the loop. In the feedback loop an anti-windup PI controller is adopted, which can achieve lower overshoot response during transients. However, the anti-windup PI controller degrades the settling time. Generally, the voltage unba lance has a slow time response compared to other voltage and current control loops in the system. Among many types of anti-windup PI controllers, the anti-windup PI conditioned is a good alternative to reduce the overshoot [28], [29]. In Figure 10., the output of the anti-windup PI controller is limited by a certain value ($\pm 0.01 \times 2\pi$).

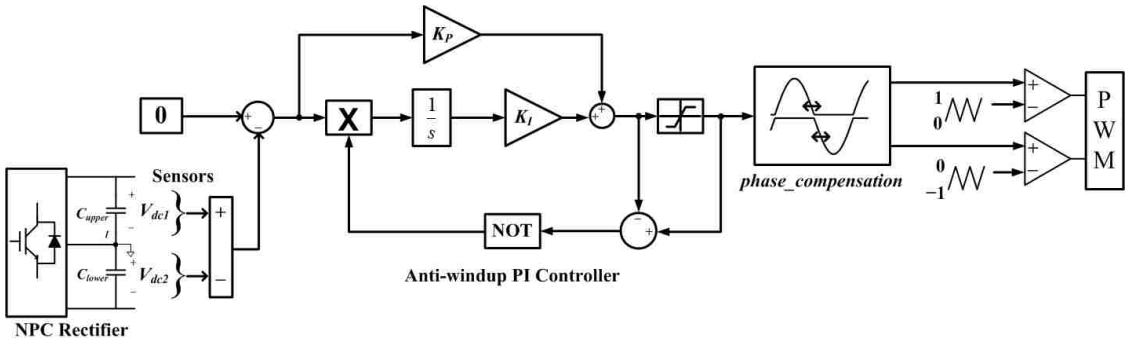


Figure 10. Feedback control block diagram for PSR strategy

When the limitation occurs, the input of the integrator becomes zero, but the previous value of the integrator in the digital PI controller will be held. Otherwise, the anti-windup PI controller will show same characteristics with a conventional PI controller.

Referring to the design of the anti-windup controller, K_P and K_I should be small enough so that a system can reduce overshoot of *phase_compensation* during transients. Thus in this paper, K_P and K_I are selected as 0.001 and 1, respectively. Since this topology is a rectifier, the plus-minus signs in (2) and (3) are selected as a minus in (2) and a plus in (3). The *phase_compensation* shifts the upper and lower references in an opposite direction. Then they are compared with each triangular carrier.

VI. SIMULATION AND EXPERIMENTAL RESULTS

The specifications of the simulation model as well as the hardware setup are as follows: phase voltage V_{grid_peak} = 100 V, grid frequency=60 Hz, switching frequency = 6 kHz, L = 6 mH, C_{upper} = 7.8 mF, C_{lower} = 11.7 mF for experimental set, C_{upper} = 800 µF, C_{lower} = 1 mF for MATALB/Simulink simulation, $R_{load} \approx 90\ \Omega$. In order to make the simulation fast, upper and lower capacitances are decreased. Figure 11. displays an overview of the experimental setup and the control block diagram. The sampling and switching frequencies are the same. The PLL block is designed based on a synchronous reference frame [32] and forms a closed loop control which will detect the angle of the grid phase voltage V_{an}. The DSP board has a push button so that a signal from 'Star/Stop' can trigger or stop the suggested method in the DSP. The experimental setup uses damping resistors ($R_{damping} \approx 15\ \Omega$) for reducing the inrush current from the grid at startup. After the capacitors are charged at a certain level, the damping resistors are removed by using magnetic switches. There are pictures displaying NPC rectifier prototype for the test in Figures 12. and 13. The white colored capacitors in the NPC rectifier are film

capacitors placed in parallel with the electrolytic capacitors. They filter noise and reduce stray inductance. For safety reasons, a tapped transformer provides magnetic isolation between the set and the grid. The voltage information measured by LV 25-P is transferred to the AIB board described in Figure 13. Then the DSP generates the PWM signals that are transformed to optic signals and consequently sent to the gate driver boards.

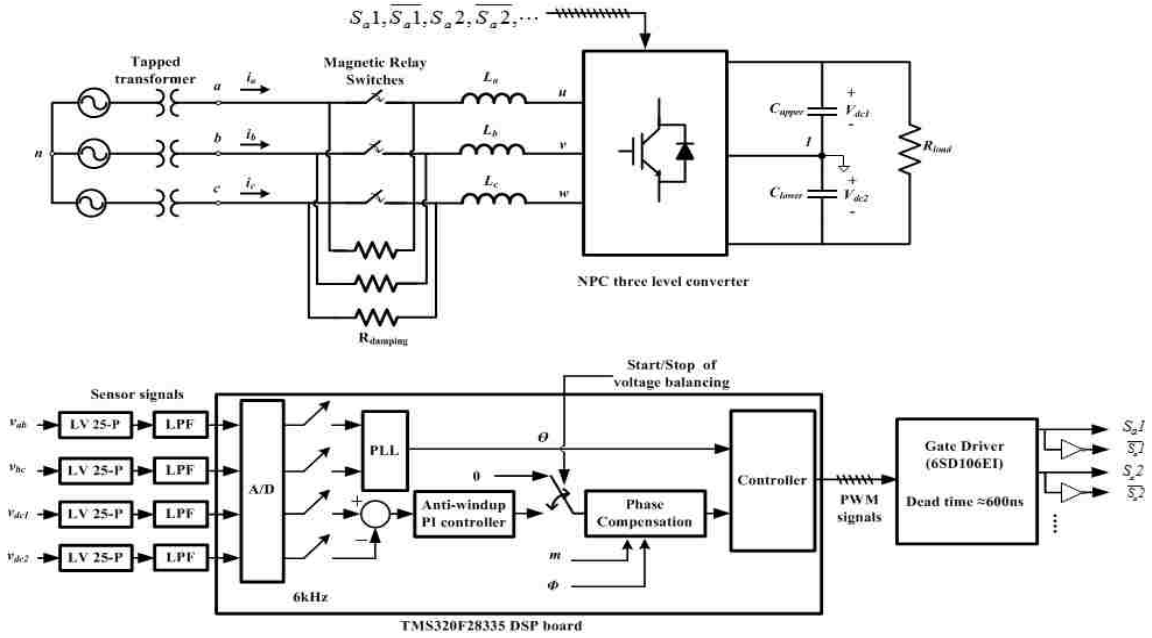


Figure 11. Experimental set configuration and control block diagram

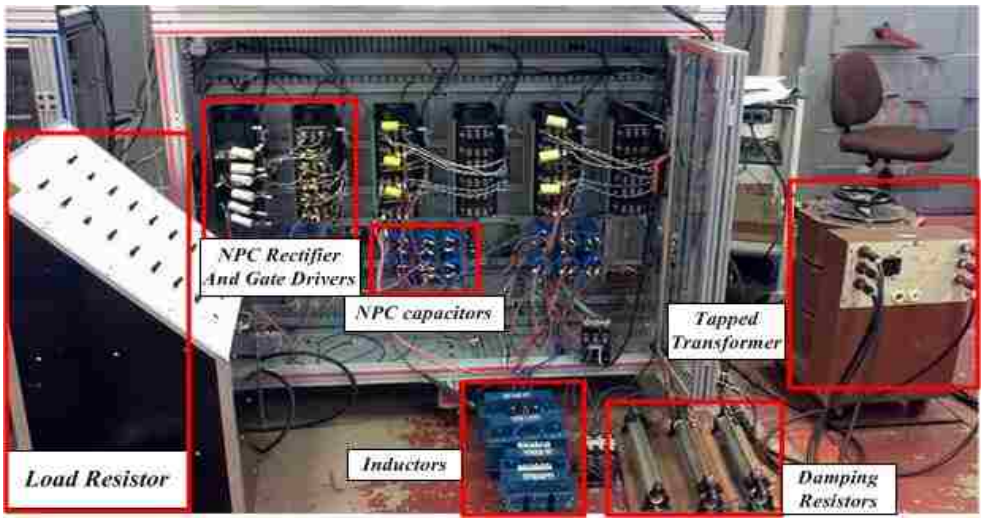


Figure 12. Experimental set configuration

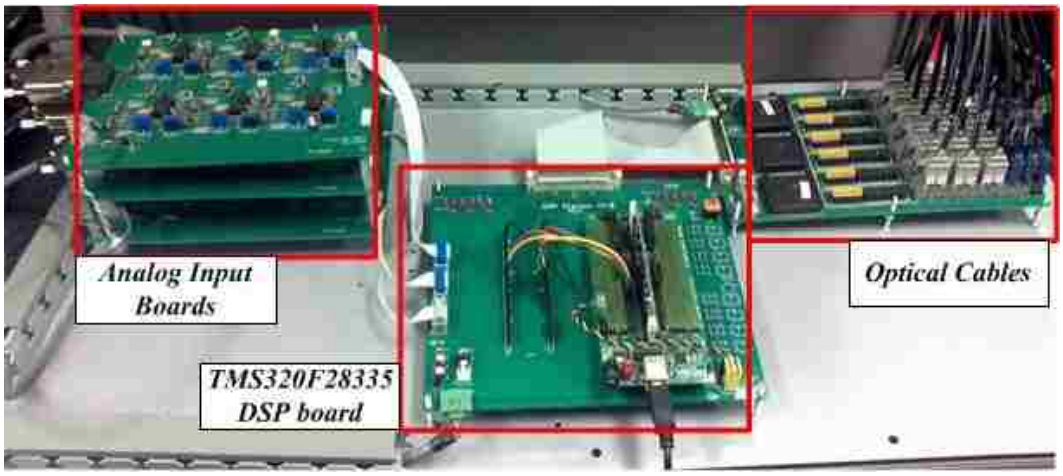


Figure 13. TMS320F28335 DSP, analog input board (AIB) and optical signal transmission board

Figure 14. shows the transient response of the two capacitor voltages and the *phase_compensation* value in simulation. From time 1.5s to 2s, the voltage balancing method is not applied. After time 2s, the PSR method is activated. Two capacitor voltages are well balanced with zero steady state error in the simulation. Again, the PSR

method is deactivated at 3 s. It looks like the two voltages are diverging unboundedly. However, it will be actually saturated at some point. The waveform in Figure 15. is the *phase_compensation* value during the steady state. The sinusoidal waveform has 180 Hz which is same with oscillation frequency of the two capacitor voltages. Figures 16. and 17. describe steady state waveforms with and without the PSR method in the simulation.

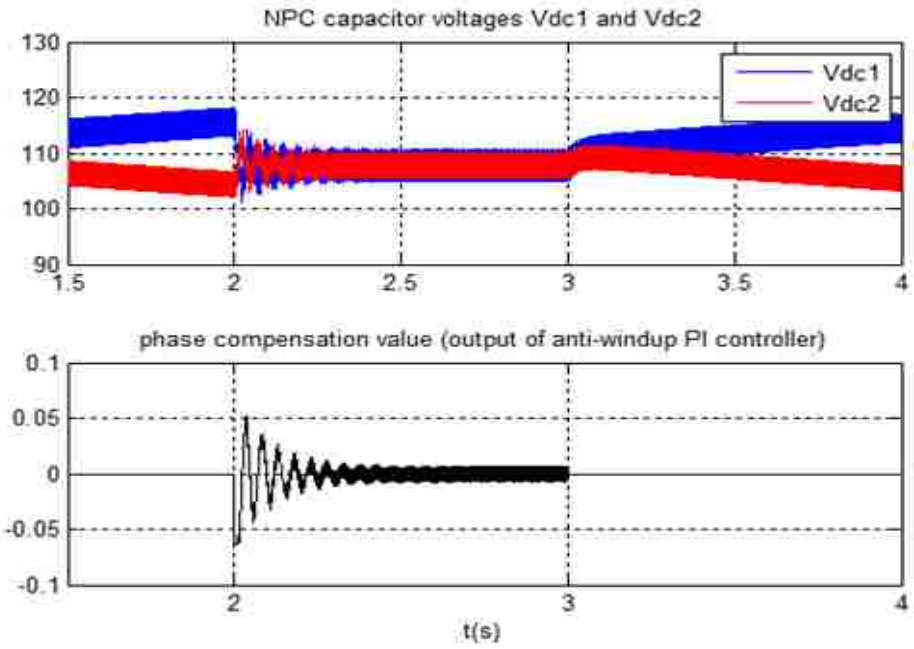


Figure 14. Transient response of the two capacitor voltages and *phase_compensation* value

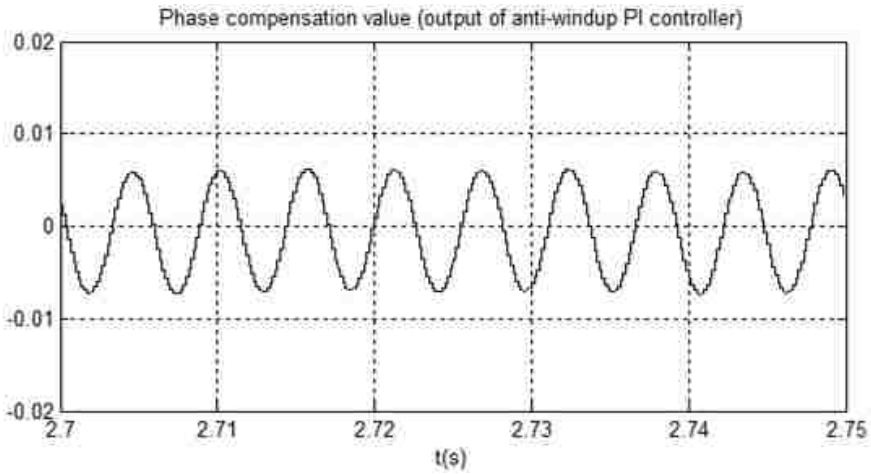


Figure 15. *Phase_compensation* value of (2) and (3) in a steady state in Figure 14. from 2.7 sec to 2.75 sec

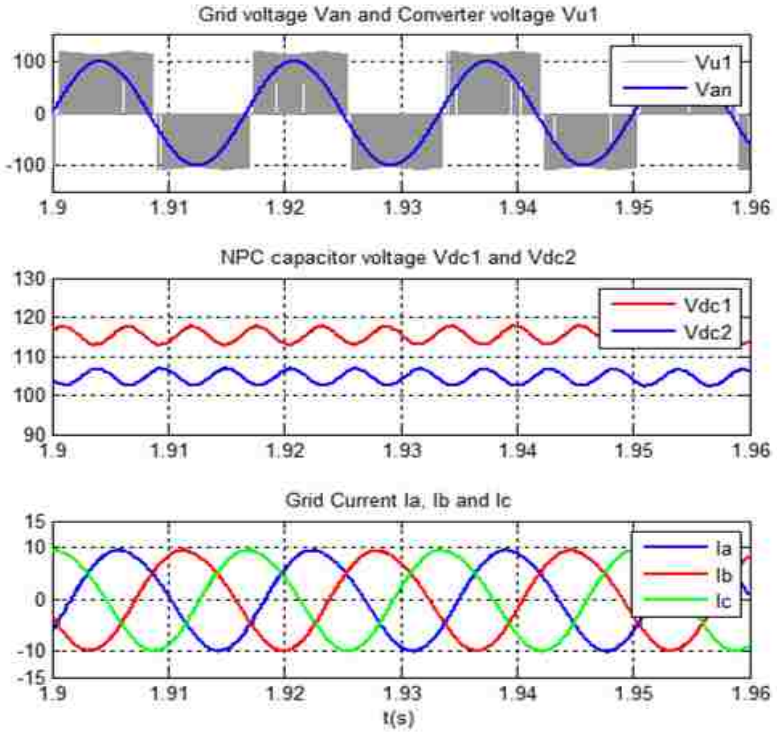


Figure 16. Simulation result in a steady state without a voltage balancing method

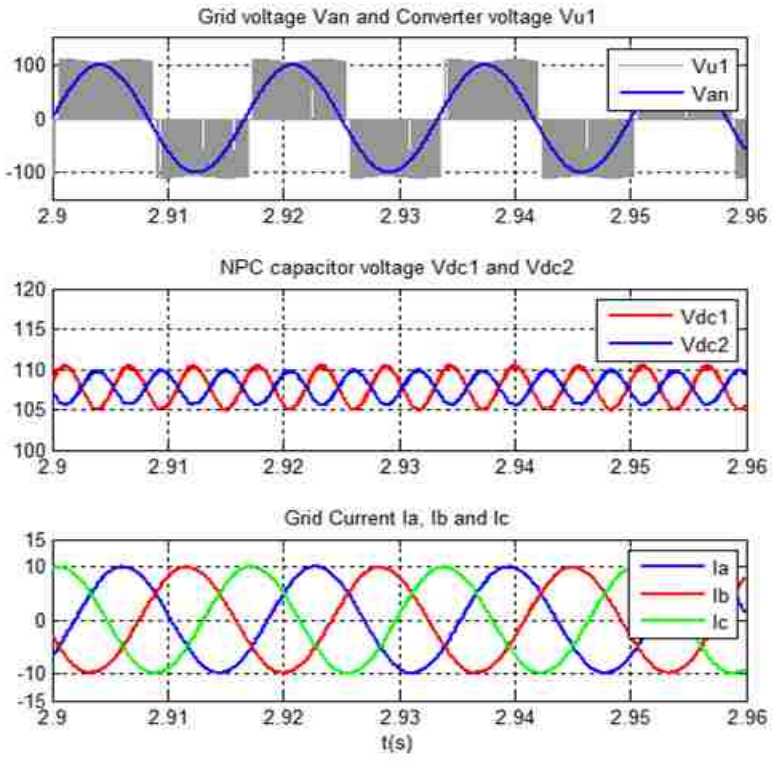


Figure 17. Simulation result in a steady state using the PSR method

Figure 18. depicts the steady state waveforms showing upper and lower capacitor voltages V_{dc1} and V_{dc2}, line−line grid voltage V_{ab} and the grid current I_a. The upper capacitor voltage is 114 V and the lower capacitor voltage is 107 V. So the voltage difference is approximately 7 V during the steady state without any voltage balancing technique. After applying the PSR method, the two capacitor voltages become 110.5 V as shown in Figure 19. The grid current waveforms in Figure 18. and Figure 19. look same. In order to figure out the difference between the two current waveforms precisely, Fast Fourier Transform (FFT) needs to be applied. Fig 21 shows the result after applying FFT

on the two currents in Figure 18. and Figure 19. THD of the grid current has been improved a little with the suggested PSR method because the fundamental magnitude of

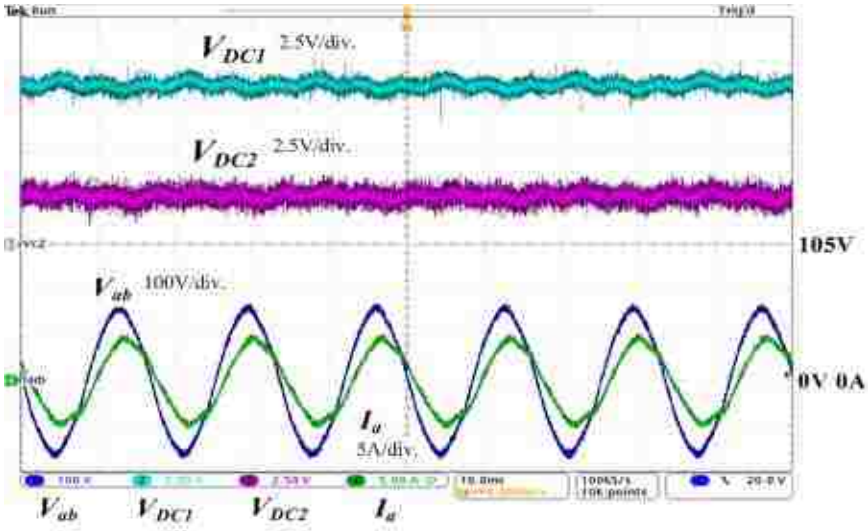


Figure 18. Experimental results in a steady state without a voltage balancing method

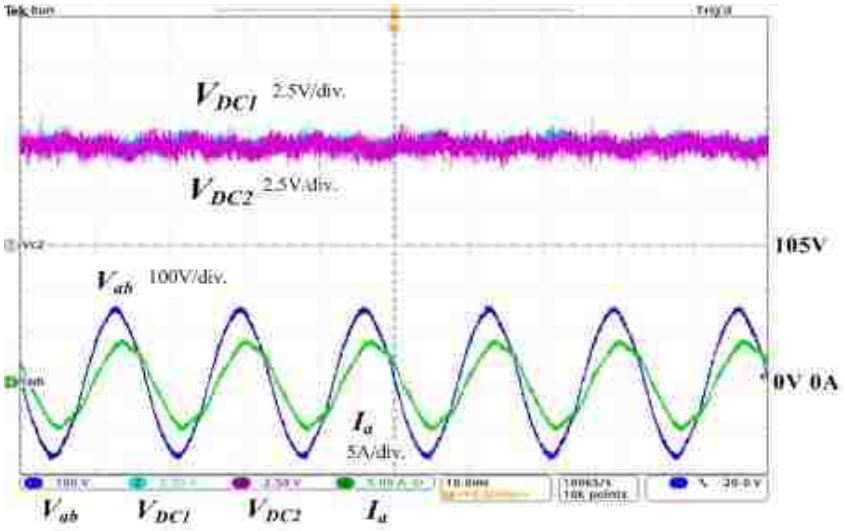


Figure 19. Experimental results in a steady state using the PSR method

the grid current becomes slightly larger from 4.53 to 4.58 and overall harmonics are reduced a little. The equally balanced capacitor voltages improved the output PWM voltage, which lead to make the fundamental output grid current a little larger. The transient response can be found in Figure 20. with 2 sec/div on the time axis. The DSP board has an external button to give a trigger signal to the DSP chip. When the button is pushed, the voltage balancing method will be activated. As described in the Figure 20., the close loop using PSR method produces low overshoot during transients and zero steady state error as similar with simulation results described in Figure 14.

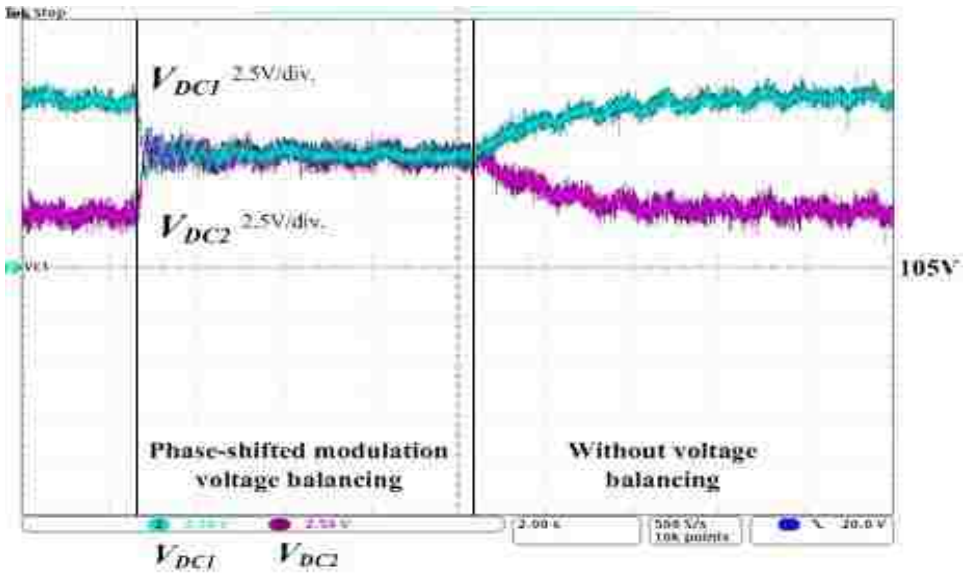


Figure 20. Transient response of the two capacitor voltages

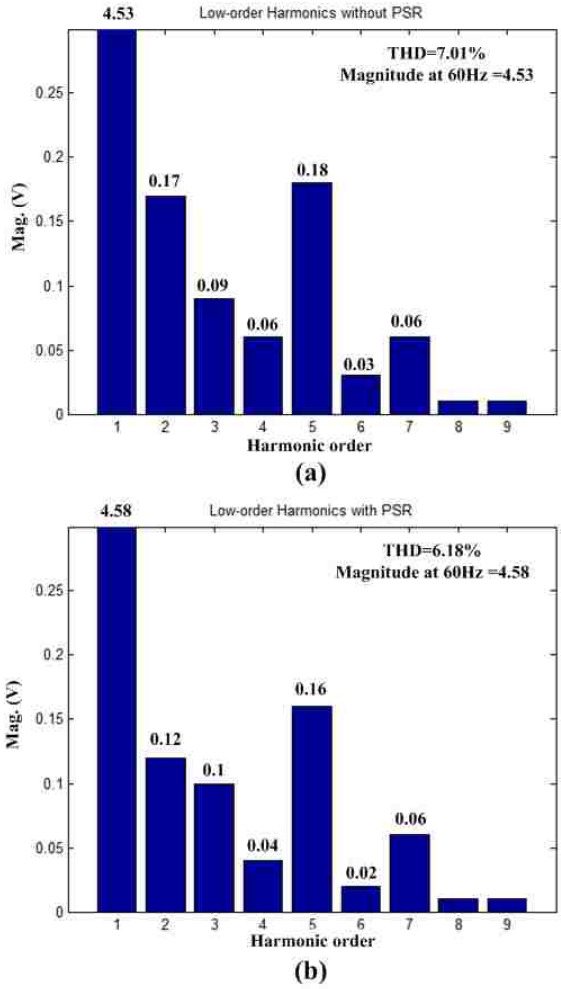


Figure 21. Magnitude spectrum of the grid current and THD comparison (a) using the grid current I_a in Figure 18., (b) using the grid current I_a in Figure 19.

VII. CONCLUSION

Having conceptually different approach from the offset injection method and a feed−forward compensated multicarrier PWM for balancing voltages in a NPC, this paper suggests the phase-shifting reference (PSR) method to balance capacitor voltages. With the PSR method, a system balances target voltages by moving the upper and lower reference in an opposite way. Eventually the compensated NPC output pulses charge the

two capacitors with different amount of grid currents. On the other hand, the conventional methods control charging time by injecting offsets. Also, the PSR method does not require to develop a model or to calculate rigorous equations. The controller design using the PSR is simple and straightforward. Over−modulation situation can be naturally prevented since it moves the upper and lower references to right or left. Also, switch states and a possible hazard during the overlap period are analyzed and explained. The transient response on the two capacitors shows stable transition and less overshoot with zero steady state error. The THD comparison brings a conclusion that the proposed method can effect slightly on the grid current THD. Therefore, the PSR method for 3-level NPC is verified with experimental and simulation results.

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II. CAPACITOR VOLTAGE REGULATION AND PRE-CHARGE ROUTINE FOR A HYBRID MULTILEVEL RECTIFIER

***Abstract*—This paper investigated a routine for the three phase hybrid multilevel rectifier to be landed safely on a steady state. The three-phase hybrid multilevel rectifier consists of a neutral point clamped (NPC) and cascaded H-bridges (CHBs). The NPC has 2 capacitors and CHBs have 9 capacitors. If they are completely discharged and the system is connected with the grid, the rectifier might experience large inrush currents which can destroy the experimental set if components have current rating lower than the inrush current. Experiment had conducted with different voltage references under load resistance change. Load voltage regulation control scheme is described with block diagrams. Unity power factor control (PFC) is also achieved and explained with details. The system regulates 6 capacitor voltages in CHBs without using independent DC power sources. Experimental results show a pre-charge routine after connection with the grid as well as load voltage control and unity PFC for steady state.**

I. INTRODUCTION

Multilevel power conversion has been gaining a lot of attention in recent years due to the pressure of satisfying better power quality, efficiency and low cost simultaneously in high power application [1] [2]. Largely, three types of multilevel topology have been widely studied and researched, which are neutral-point clamped (NPC) [3], flying capacitor [4] and cascaded H-bridge [5]. Each type of topologies has different advantages

and disadvantages among various applications. So far, research has been mainly focusing on one single switching strategy which will govern all switching devices in the topology. It can be sinusoidal pulse width modulation (SPWM), space-vector modulation (SVM) or staircase modulation at fundamental switching frequency. Recently, papers have been published with an effort of trying to use two different types of semiconductor devices. Normally, thyristor such as Integrated Gate Commutated Thyristor (IGCT) or Gate Turn-Off (GTO) thyristor can be characterized with high voltage blocking capability and large current rating, but with slow switching speed. On the other hand, popularity of Insulated Gate Bipolar Transistors (IGBTs) and Metal-Oxide Semiconductor Field Effect Transistors (MOSFETs) is based on their medium voltage blocking capability and medium current rating with fast switching speed. So, hybrid multilevel topology is based on hybrid usage of the two kinds of devices [6]−[19]. At first, the hybrid multilevel topology has been researched with a strategy using independent DC power supplies on each CHBs [6]–[12]. In order to save cost of DC power supplies, many methods that regulate CHB capacitor voltages have been suggested [13]−[19].

In an active rectifier application, a pre-charge routine is needed to protect the set from inrush currents [22]. The three-phase hybrid multilevel rectifier has 2 capacitors on the NPC and 9 capacitors on the CHBs. Therefore, large inrush currents can cause hazards on the set if they are completely discharged and components of the set have low current rating than the inrush current. Thus the 11 capacitor voltages need to be charged before unity PFC and load voltage control are activated in a feedback control. The pre-charge routine has several steps including 1) grid connection, 2) removing damping resistors, 3) open loop control and 4) closed loop control. Regarding the open loop

control, a reference for the hybrid multilevel rectifier is calculated based on a vector diagram.

There are three main goals in a grid−connected rectifier application: 1) unity PF generating grid line currents in phase with phase voltages, 2) load voltage regulation even under load change circumstances and 3) capacitor voltage regulation of CHBs which are connected in series with a NPC. Experiment had been conducted with a TMS320F28335 DSP board. The multilevel converter has totally 36 switching devices excluding diodes. This paper is also describing how to generate 36 switching signals with only one DSP.

II. HYBRID MULTILEVEL RECTIFIER

Figure 1. is the hybrid multilevel rectifier which consists of three phase NPC and 6 CHBs. The main NPC operates with square waveforms at fundamental frequency. So, the NPC provides most power to the load R. Figure 2. shows the modulation strategy that governs the hybrid multilevel rectifier. The NPC phase voltage V_{x0} forms a square voltage waveform. In order to make the grid current sinusoidal, the 6 CHBs generates harmonics for the output voltage V_{ag}. So, the rectifier output voltage V_{u0} builds 7-level PWM voltage waveform by summing $V_{x0}+V_{1a}+V_{2a}$. As the main NPC provides power to the load R, the output of the CHBs is not connected to any resistive load. They are just floating voltage regulated by a closed loop which is discussed in section IV with details.

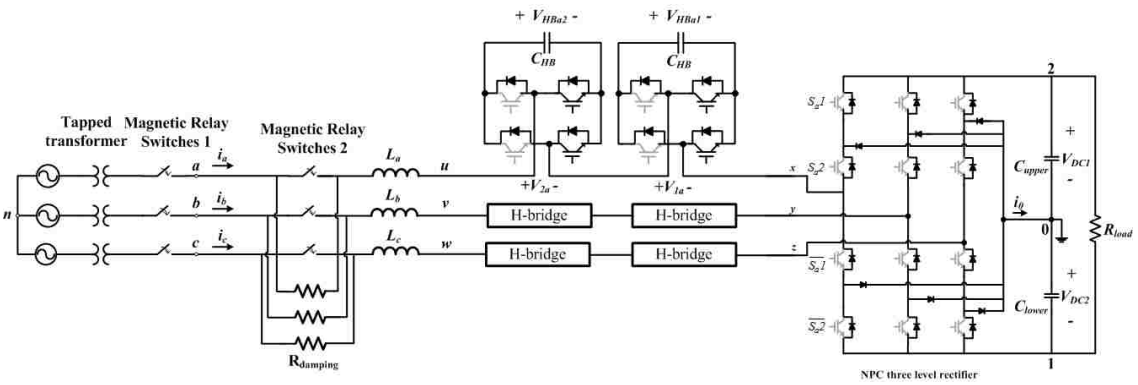

Figure 1. Hybrid multilevel rectifier consisting of the NPC and the CHBs

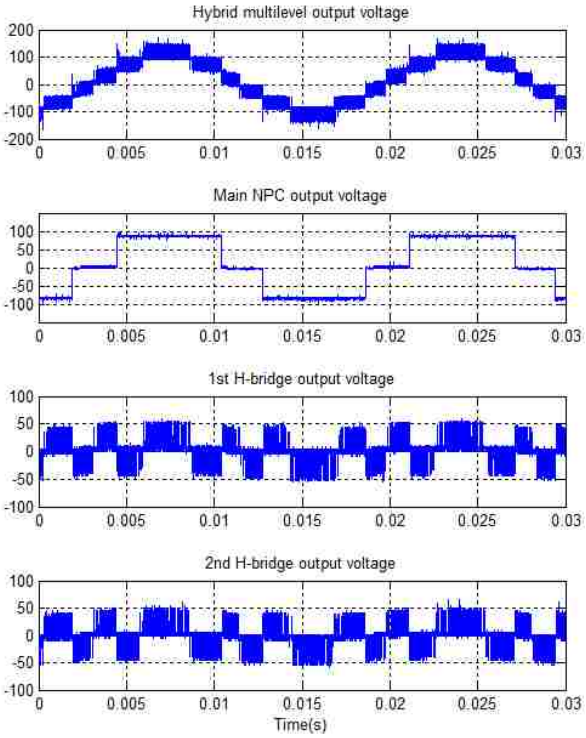

Figure 2. Experimental results explaining hybrid modulation method
(a) V_{u0}, the hybrid multilevel rectifier output voltage,
(b) V_{x0}, square waveform for the NPC,
(c) V_{1a}, output voltage of the 1st H-bridge
(d) V_{2a}, output voltage of the 2nd H-bridge

III. REGULATING H-BRIDGE VOLTAGES

Since the hybrid multilevel rectifier does not use independent voltage sources on the CHB capacitors, feedback loops for regulating CHB voltages are required. Figure 3. shows a feedback loop block diagram. The V_{HBDC}_ref is DC value calculated by simply using $(V_{DC1}+V_{DC2})\times 0.25$ and V_{HBDC}_sensing is information from voltage sensors. The V_{HB}_ref can be calculated by subtracting the square waveform in Figure 2. from a sinusoidal reference. There are two stages of H-bridges after NPC, thus V_{HB}_ref would be divided by 2. The signal $\cos(\theta)$ is just for phase A, so it can be $\cos(\theta \pm 2\pi/3)$ for phase B and C. The result V_{HB}_PWM is compared with triangular waveforms of ePWM channels in a DSP. When V_{HBDC}_sensing on phase A went higher than the desired V_{HBDC}_ref, output of the PI controller multiplied with $\cos(\theta)$ will be subtracted from V_{HB}_ref. That process causes PWM pulses of the CHB on phase A narrower so that a capacitor on phase A is charging less. As a result, the feedback loop of Figure 3. regulates CHB voltages as well as it creates the CHB output voltage similar with 1st and 2nd CHB output voltages as depicted in Figure 2.

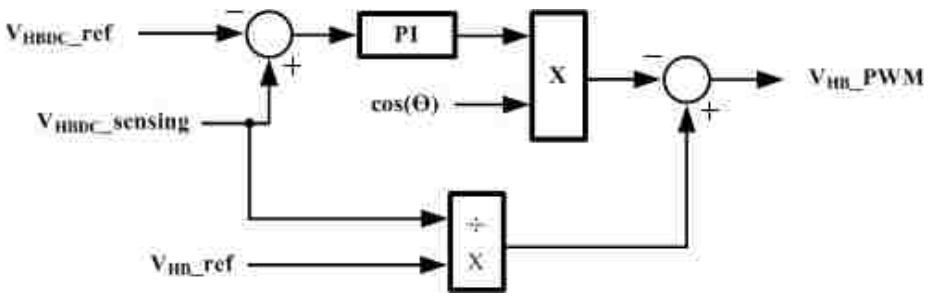

Figure 3. Feedback loop block diagram for regulating H-bridge voltage

IV. UNITY POWER FACTOR CONTROL AND LOAD VOLTAGE CONTROL

Unlike SPWM or SVPWM strategy, hybrid multilevel uses low frequency switching for the NPC and high switching frequency for CHBs. So the output of a closed loop should be V_m (maximum modulation index) and three phase sinusoidal waveform with amplitude ± 1. Figure 4. displays feedback loop for unity PFC and load voltage control. The V_{DC_ref} is the reference for the NPC capacitor voltages ($V_{DC1}+V_{DC2}$). The sensing information of $V_{DC1}+V_{DC2}$ is fed back to the loop and is compared with the V_{DC_ref}. The outputs of the PI controller for the load voltage control are I_q_ref and I_d_ref. It needs to be limited by a certain value depending on the grid current rating of the system. The three grid currents I_a, I_b and I_c are transformed to dq-axis with grid voltage angle θ, which is the result of PLL. Because this control is for achieving unity PFC, the I_q_ref is zero.

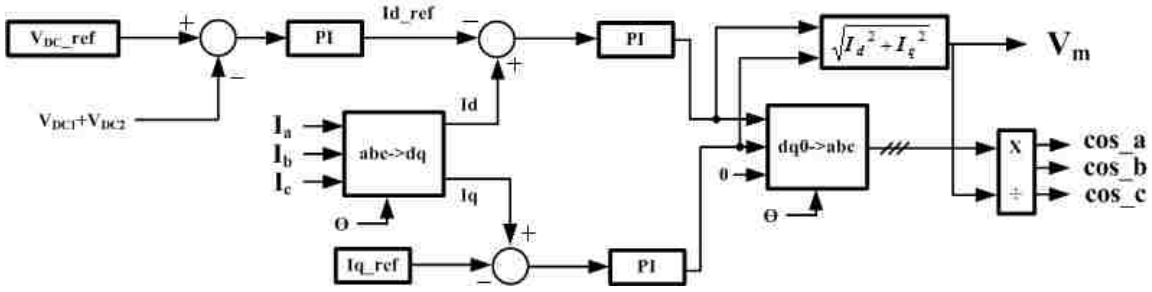

Figure 4. Feedback loop block diagram for unity displacement power factor control and load voltage control.

V. PRE-CHARGE ROUTINE

Before achieving regulation of CHB voltages (section III), unity PFC and load voltage control (section IV), the hybrid multilevel rectifier should pre-charge capacitors for preventing large inrush current from the grid. Table I represents operation modes for starting up the hybrid multilevel rectifier. In mode 0, the rectifier is completely disconnected from the grid. In mode 1, the experimental set is connected by turning on the magnetic relay switch 1 with damping resistors as described in Figure 1. The damping resistors is removed from the set by using the magnetic relay switch 2 as defined in mode 2. Therefore, the two NPC capacitors are charged to certain level during mode 1 and mode 2. Also, the on/off states of the all switches in the rectifier are shown in Figure 1. The grayed switches in Figure 1. are off so that CHBs are by-passed and the NPC acts like a diode rectifier. During the mode 3, the switching action for the NPC and HBs is activated and 6 HB capacitors are charged. The critical difference between mode 3 and 4 is the feedback control loop described in Figure 4. Mode 3 uses fixed voltage reference for the rectifier, which is explained in section VI. Figure 5. shows the simulation result that describes large inrush current from the grid when damping resistors are not used. Figure 6. represents acceptable grid currents with damping resistors.

Table 1. Operation Modes for Starting up the Hybrid Multilevel Rectifier

Mode	Grid connection	Damping resistors	Charging CHB caps	Charging NPC caps	Unity PFC Load voltage
0	X	O	X	X	X
1	O	O	X	O (low level)	X
2	O	X	X	O (high level)	X
3	O	X	O	O	X
4	O	X	O	O	O

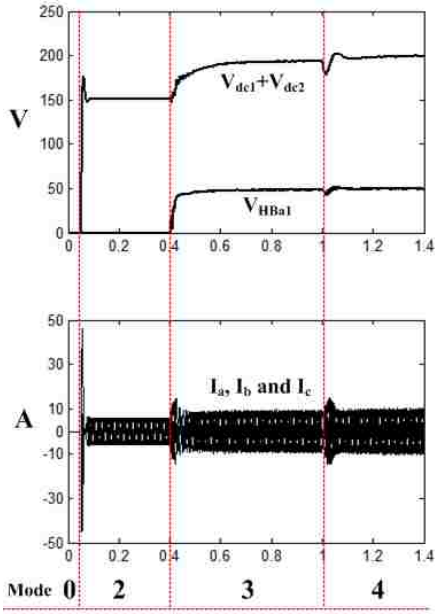

Figure 5. Large inrush currents without damping resistors

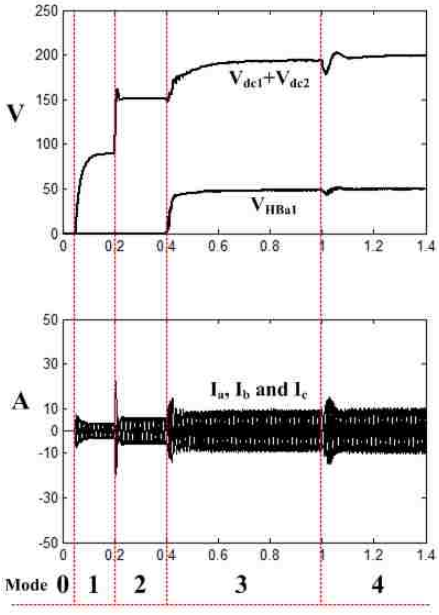

Figure 6. Acceptable grid currents with damping resistors

VI. OPEN LOOP CONTROL OF THE HYBRID MULTILEVEL RECTIFIER

Figure 7. explains how the value V_m and ϕ are calculated and used during the mode 3. Figure 7-(a). is a simplified circuit with only phase A. The resistor R is parasitic resistance in the filter inductor L. The circuit can be expressed by (1). In turn, (1) gives phasor representation. From Figure 7-(b)., the value V_m and ϕ can be calculated by using (2). With conditions of Ia_peak=10 A, R=0.2Ω, V_m=100.5765 and cos_a= cos(θ+ϕ)=cos(θ-0.2268). Therefore, during the mode 3, the rectifier voltage reference is fixed withV_m, cos_a, cos_b and cos_c. Otherwise during the mode 4, V_m, cos_a, cos_b and cos_c are determined by the feedback loop depicted in Figure 4.

$$-V_{an} + (R + j\omega L)I_a + V_{un} = 0 \tag{1}$$

$$\phi = -\tan^{-1}\frac{\omega L \cdot I_a}{V_{an} - R \cdot I_a}, \quad |V_{un}| = V_m = \sqrt{(V_{an} - R \cdot I_a)^2 + (\omega L \cdot I_a)^2} \tag{2}$$

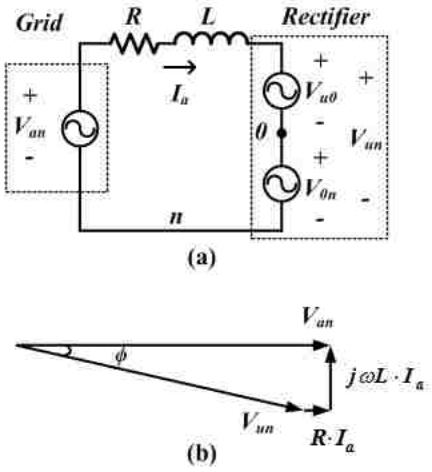

Figure 7. Calculation of the value V_m and ϕ (a) simplified power circuit only with phase A ,(b) Phasor representation that makes the rectifier achieve unity PF

VII. EXPERIMENTAL RESULTS

The specifications of the system are as follows: phase voltage V_{grid_peak} = 100 V, grid frequency=60 Hz, switching frequency for CHBs = 6 kHz, sampling frequency = 6kHz, L = 6 mH, $C_{upper} = C_{lower}$ = 11.7 mF, C_{HB} = 3.9mF, $R_{damping} \approx 15\ \Omega$, $R_{load} \approx 24\ \Omega$. This experiment was conducted with one TMS320F28335 DSP board. Voltage sensors are LV 25-P and current sensors are LA 55-P. Since this system acts as a rectifier, the grid current's direction is set from the grid to the rectifier. The actual angle of the grid voltage will be calculated by using PLL after the rectifier is connected with the grid. The PLL is designed based on synchronous reference frame and it forms feedback loop [20]. TMS320F28335 DSP has 6 ePWM modules and each module can generate 2 PWM signals. So 12 PWM channel are set to generate switching signals for 6 CHBs. The 1st and 2nd stage of CHB has 90 degree difference in triangular waveforms [21]. Figure 8. shows the acceptable grid currents with damping resistors after mode transition from mode 0 to mode 1. Figure 9. represents grid currents after removing damping resistors. Regarding the transition from mode 2 to mode 3, three grid currents and the hybrid multilevel rectifier output voltage V_{u0} are described in Figure 10. Figures 11.−13. display transient responses of grid currents, rectifier output voltage, NPC voltages and CHB voltages for mode transition from mode 3 to mode 4. From Figures 12. and 13., the load voltage control described in Figure 4. works well by observing the NPC voltage=202 V and CHB voltage 49 V with V_{dc}_ref=200V.

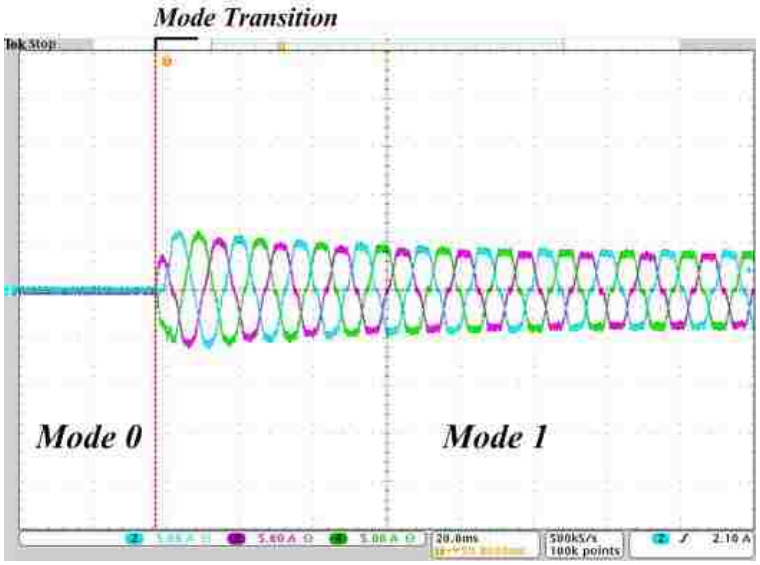

Figure 8. Acceptable grid currents with damping resistors after connecting with the grid (from mode 0 to mode 1)

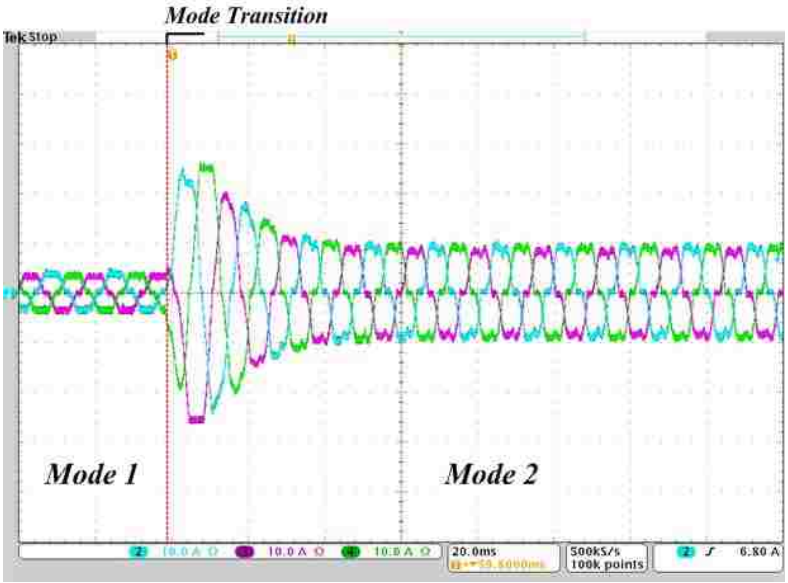

Figure 9. Acceptable grid currents after removing damping resistors (from mode 1 to mode 2)

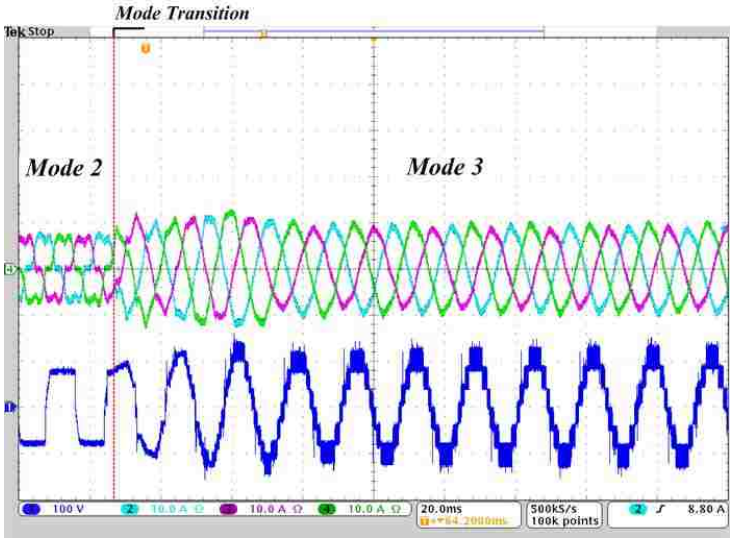

Figure 10. Grid currents and the rectifier output voltage V_{u0} after activating NPC and CHB switching (from mode 2 to mode 3)

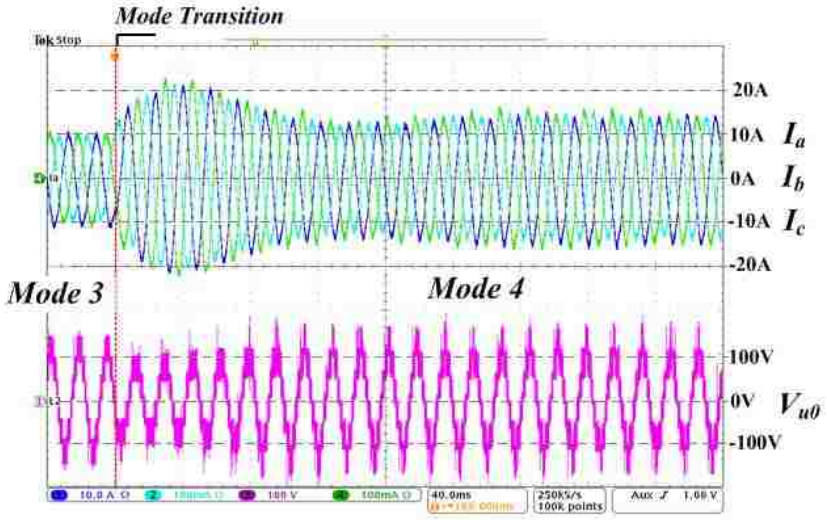

Figure 11. Transient responses of grid current and hybrid multilevel phase voltage output when voltage feedback loop is activated with V_{DC}_ref=200V (from mode 3 to mode 4).

Figure 14.−16. demonstrates that the unity PFC achieves the grid current I_a in phase with the grid phase voltage V_{an} which is calculated by using $(V_{ab}-V_{ca})/3$ in the oscilloscope during mode 4 with three different V_{DC}_ref.

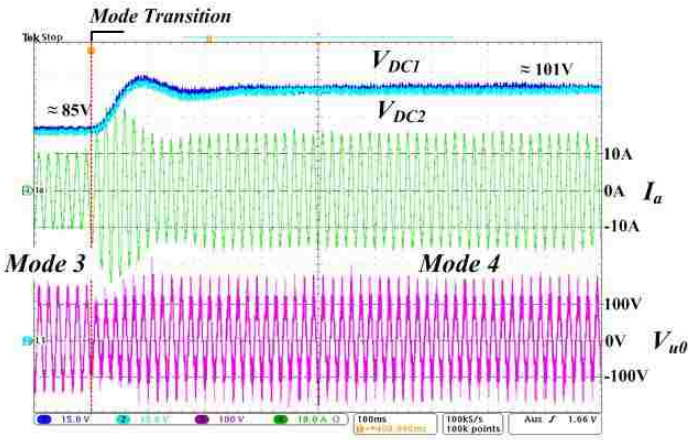

Figure 12. Transient responses of NPC voltages V_{DC1} and V_{DC2} when voltage feedback loop is activated with V_{DC}_ref=200 (from mode 3 to mode 4).

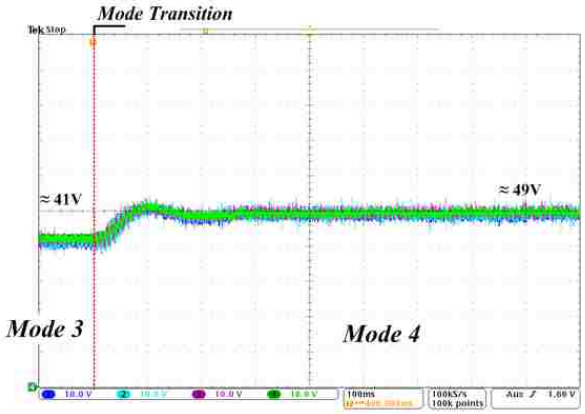

Figure 13. Transient responses of H-bridge voltages VHBa2, VHBa1, VHBb1 and VHBc1 when voltage feedback loop is activated with V_{DC}_ref=200 (from mode 3 to mode 4).

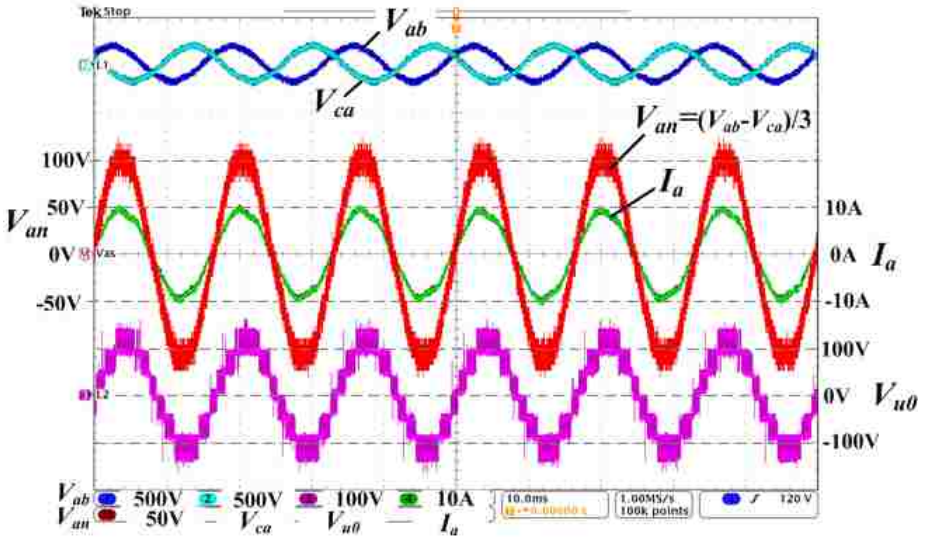

Figure 14. Steady state waveforms of grid current I_a and hybrid multilevel output V_{u0} with V_{DC}_ref=165 (mode 4).

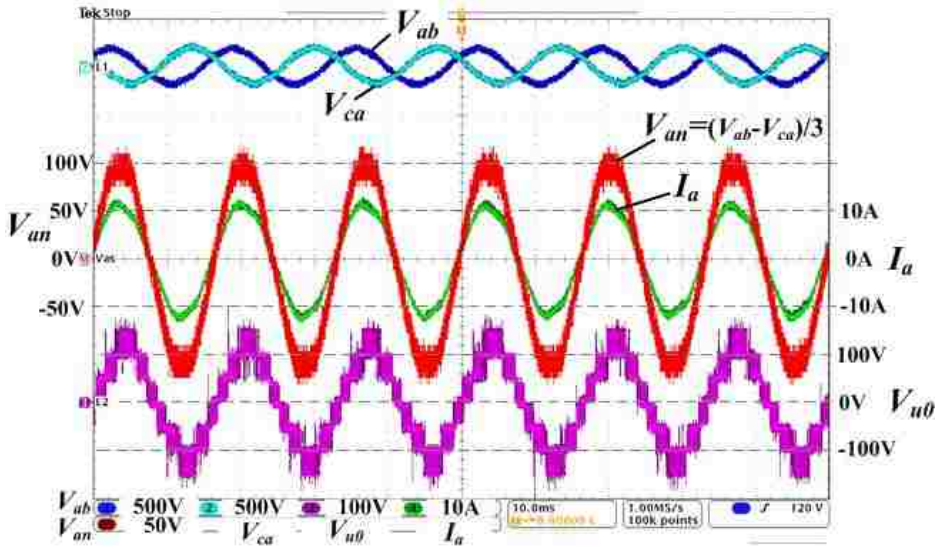

Figure 15. Steady state waveforms of grid current I_a and hybrid multilevel output V_{u0} with V_{DC}_ref=180 (mode 4).

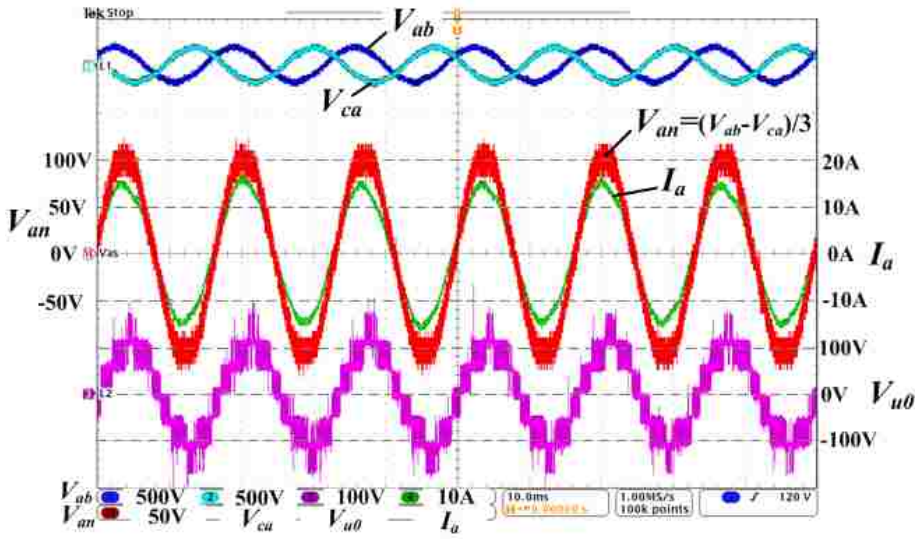

Figure 16. Steady state waveforms of grid current I_a and hybrid multilevel output V_{u0} with V_{DC}_ref=200 (mode 4).

VIII. CONCLUSION

This paper has presented complete procedure of start-up routine to run the hybrid multilevel rectifier which consists of the NPC and the CHBs. The hybrid multilevel has total 11 capacitors that need to be charged before achieving unity PFC and load voltage regulation. In a worst case of completely discharged capacitors, large inrush grid currents can destroy devices in the set. Therefore, a safe start-up routine is essential. This paper suggests the start-up routine from a situation that the rectifier is disconnected with the grid, to steady state responses that achieve CHB voltage regulation, load voltage regulation and unity PFC step by step. The experimental results have verified the start-up routine and steady state operation of the hybrid multilevel rectifier.

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III. MULTIPLE REFERENCE FRAME-BASED HARMONIC COMPENSATION FOR GRID CURRENTS IN THE THREE PHASE HYBRID MULTILEVEL RECTIFIER

***Abstract*—This paper suggests a method for compensating the 5th harmonic of grid currents by using multiple reference frame theory in the hybrid multilevel rectifier. The grid-connected AC/DC hybrid multilevel rectifier has a voltage source which is distorted slightly. Therefore, low order harmonics are contained in the grid currents coming from the voltage source to the load of the hybrid multilevel rectifier. In this paper, the grid currents are analyzed using the multiple reference frame theory to extract their 5th harmonic content. Magnitude and phase values at the 5th harmonic frequency in a bode plot will be used to convert the calculated 5th harmonic as an output to voltage reference compensation as an input. The feedback control loop for accomplishing load voltage control and unity power factor control is explained with block diagrams. Simulations and experimental results show the verification of the suggested method.**

I. INTRODUCTION

The power quality of grid connected power converter systems has become a serious issue with the increasing number of distributed generation systems and nonlinear loads. At the point of connection between the power conversion systems and the utility grid, low THD of the grid currents and a high power factor have been regarded as important requirement to fulfill. Among different topologies, multilevel converters are considered to be an effective way in achieving better THD of grid currents. Besides three different

multilevel topologies including the neutral point clamped (NPC) [1], cascaded H-bridge (CHB) [2], and flying capacitor [3], hybrid topologies have been suggested and researched. They take advantage of using two types of semiconductors such as thyristors and IGBTs [4]−[10]. Also, several control methods to reduce current harmonics have been suggested. Closed-loop selective harmonic compensation methods suppress harmonics by obtaining high loop gain at low frequencies [11]−[13]. As another method, repetitive control (RC) uses internal model control theory to track periodical and highly complex reference waveforms after designing phase-locked loops (PLL) which estimates phase-angle after rejecting harmonic disturbances [14]−[16].

PLLs have been widely used to extract the phase angle and magnitude of the fundamental frequency from a distorted grid voltage. Various methods have been suggested to reduce distortion and improve tracking performance of PLLs [17]–[24]. Also, multiple reference frame (MRF) theory can be employed to analyze a distorted or unbalanced grid voltage source. In [21]–[24], a PLL is designed to extract only sinusoidal angle at the fundamental frequency after filtering low order harmonics using MRF. In [22], after analyzing distorted grid voltage, the fundamental grid voltage signal with no harmonics advances to a hysteresis current controller. Therefore, the boost rectifier can improve the THD of the grid currents under distorted and unbalanced grid voltage conditions.

In this paper, the hybrid multilevel rectifier is built to generate grid currents with low THD while it is connected to a distorted grid voltage source. The hybrid multilevel rectifier consists of an NPC and CHBs connected in series with each phase of the NPC. To save the cost of using independent DC power supplies, the floating capacitor voltages

of CHBs are regulated in each feedback loop that is implemented in a DSP. Unity power factor control and load voltage control are achieved in a closed loop where voltage reference will be changed to achieve the two goals. Three grid currents are sensed and analyzed with the MRF theory to extract the 5th harmonic from the grid currents. Then, the calculated 5th harmonic is converted to voltage reference compensation in order to reduce the 5th harmonic of the grid current.

Simulation is conducted based on MATALB/SIMULINK and power circuit is created in PLECS. The simulation uses real grid voltage information from oscilloscope as grid voltage sources to mimic the real situation. Experiment is carried out with TMS320F28335 DSP board. The multilevel converter has totally 36 switching devices excluding diodes. This paper is also describing how to generate 36 switching signals with only one DSP. The simulation and experimental results have verified the validity of the proposed method to reduce low order harmonics of the grid current using MRF.

II. HYBRID MULTI-LEVEL RECTIFIER

In Figure 1., the hybrid multilevel rectifier consists of a three phase NPC and 6 CHBs. The NPC provides most power to the R_{load} and switches with square waveforms at the fundamental frequency. The 6 CHBs do not deliver power to any loads but they create high frequency output voltages to compensate for the harmonics that are created by the NPC square output voltage. Figure 2. describes the hybrid modulation strategy that has square waveforms for the NPC and high frequency PWMs for the CHBs. In order to compensate harmonics that are contained in the NPC phase voltage V_{x0} which operates

with square waveforms, the 6 CHBs are modulated with high switching frequency by using the reference after the square waveform is subtracted from the sinusoidal waveform. So, the rectifier output voltage V_{u0} builds a 7-level PWM voltage waveform by summing $V_{x0}+V_{1a}+V_{2a}$. CHB voltage V_{HBa1} should be regulated by a closed loop otherwise it needs to be supplied by an independent DC power supply.

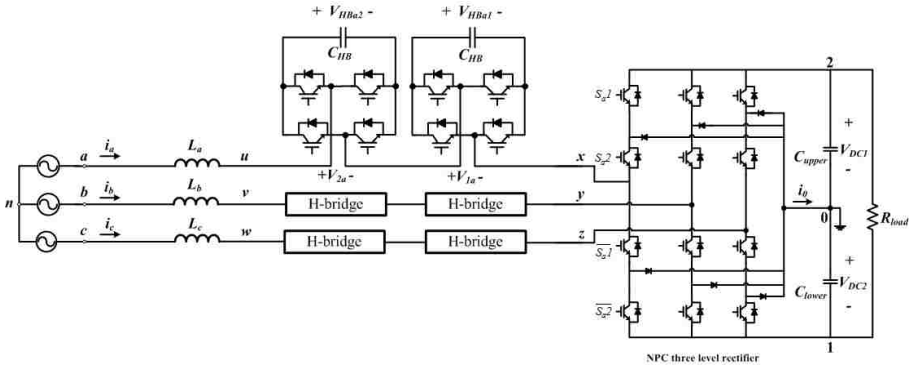


Figure 1. Hybrid multilevel rectifier consisting of the NPC and the CHBs

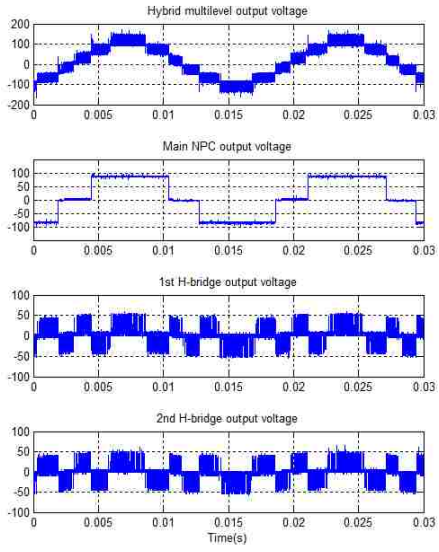


Figure 2. Experimental results explaining hybrid modulation method (a) V_{u0}, the hybrid multilevel rectifier output voltage, (b) V_{x0}, square waveform for the NPC, (c) V_{1a}, output voltage of the 1st H-bridge (d) V_{2a}, output voltage of the 2nd H-bridge

III. MULTIPLE REFERENCE FRAME THEORY

If the grid voltage is distorted, the grid current will also contain low order harmonics for the rectifier depicted in Figure 1. In turn, THD of the grid current will be worse. In order to improve THD, multiple reference frame theory can be employed to extract the 5th harmonic of the grid current. Then the calculated 5th harmonic current can be used to compensate the voltage reference for the grid connected hybrid multilevel rectifier shown in Figure 1. Finally, the actual grid current will include less 5th harmonic. Figure 3. displays the stationary multiple frames that possess 1) $i_{\beta\alpha}\_1p$: the vector rotating counter clockwise at the fundamental frequency on the stationary reference frame, 2) $i_{\beta\alpha}\_1n$: the vector rotating clockwise at the fundamental frequency on the stationary reference frame, 3) $i_{\beta\alpha}\_5p$: the vector rotating counter clockwise at the 5th harmonic frequency on the stationary reference frame. The abc axis can be transformed to the stationary βα axis by using (1). Then the βα axis is transformed to multiple rotating reference frames which consist of i_{dq}_1p, i_{dq}_1n and i_{dq}_5p by using (2)−(4).

$$i_{\beta\alpha} = \underbrace{\frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix}}_{K_{\beta\alpha}} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} i_\beta \\ i_\alpha \end{bmatrix} \tag{1}$$

$$i_{dq}\_1p = \underbrace{\begin{bmatrix} \cos(\hat{\theta}) & -\sin(\hat{\theta}) \\ \sin(\hat{\theta}) & \cos(\hat{\theta}) \end{bmatrix}}_{K_{1p}} \begin{bmatrix} i_\beta \\ i_\alpha \end{bmatrix} = \begin{bmatrix} i_{d_{1p}} \\ i_{q_{1p}} \end{bmatrix}, \quad {K_{1p}}^{-1}\, i_{dq}\_1p = i_{\beta\alpha}\_1p \tag{2}$$

$$i_{dq}\_1n = \underbrace{\begin{bmatrix} \cos(\hat{\theta}) & \sin(\hat{\theta}) \\ \sin(\hat{\theta}) & -\cos(\hat{\theta}) \end{bmatrix}}_{K_{1n}} \begin{bmatrix} i_\beta \\ i_\alpha \end{bmatrix} = \begin{bmatrix} i_d\_1n \\ i_q\_1n \end{bmatrix}, \quad {K_{1n}}^{-1}\, i_{dq}\_1n = i_{\beta\alpha}\_1n \tag{3}$$

$$i_{dq}\_5p = \begin{bmatrix} \cos(5\hat{\theta}) & -\sin(5\hat{\theta}) \\ \sin(5\hat{\theta}) & \cos(5\hat{\theta}) \end{bmatrix} \begin{bmatrix} i_\beta \\ i_\alpha \end{bmatrix} = \begin{bmatrix} i_d\_5p \\ i_q\_5p \end{bmatrix}, \quad {K_{5p}}^{-1}\, i_{dq}\_5p = i_{\beta\alpha}\_5p \tag{4}$$
K_{5p}

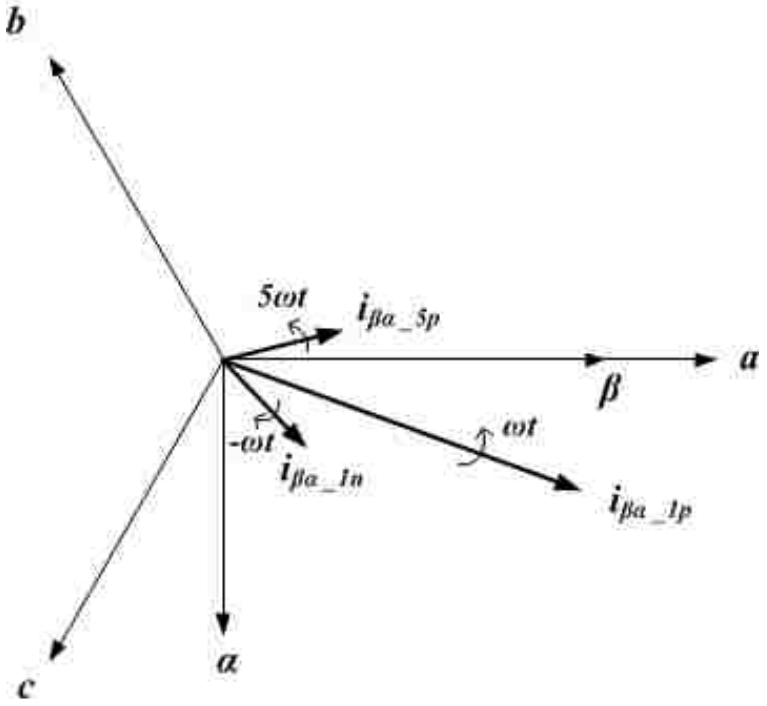


Figure 3. Grid current vectors and axes of the multiple reference frame

IV. CONTROL LOOP FOR GRID CURRENT COMPENSATION

This paper only compensates the 5th harmonic because the magnitudes of other harmonics such as the 7th and 11th contain large noises so that they cannot be filtered with the low pass filters. Figure 4. displays a block diagram for showing the method to compensate the grid currents based on MRF theory. As shown in Figure 4., the three grid currents are sent to the loop. Then they are transformed to the stationary reference frame by using (1). Then the fundamental positive and negative sequences are decoupled from

the grid currents in order to extract each $i_{\beta\alpha}\_1p$ and $i_{\beta\alpha}\_1n$. The output of the K_{5p} and LPF becomes the 5th harmonic positive sequence i_{qd}_5p. It is the 5th harmonic that is contained in the grid currents. Figure 5. shows a bode plot where 11.3 (abs) and 88.9 (degree) can be found at 300 Hz, the 5th harmonic frequency. In the transfer function of the bode plot, the input is grid currents and the output is the hybrid multilevel converter output voltages. Therefore, (5) can be used to calculate C5th_abc. Because direction of the grid current is set from the grid side to the load side, (5) should have minus in front of 11.3(abs).

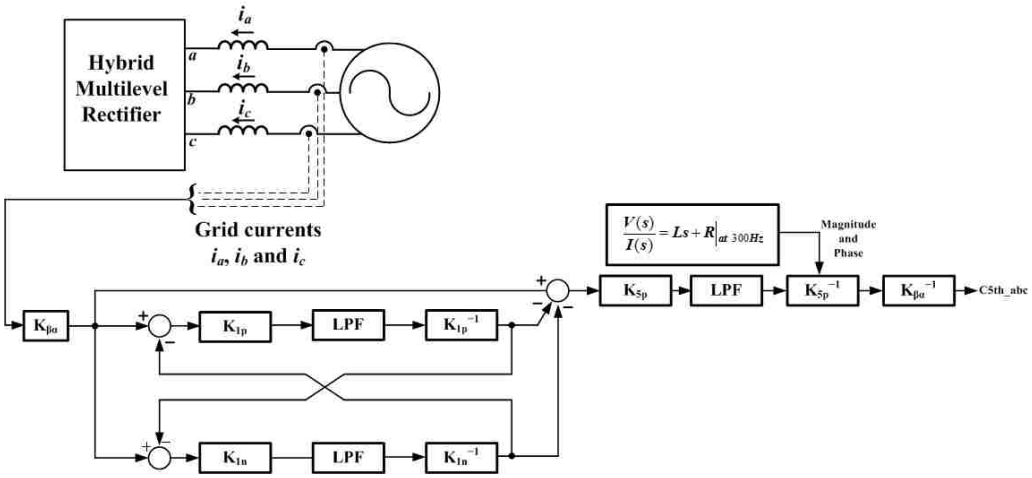
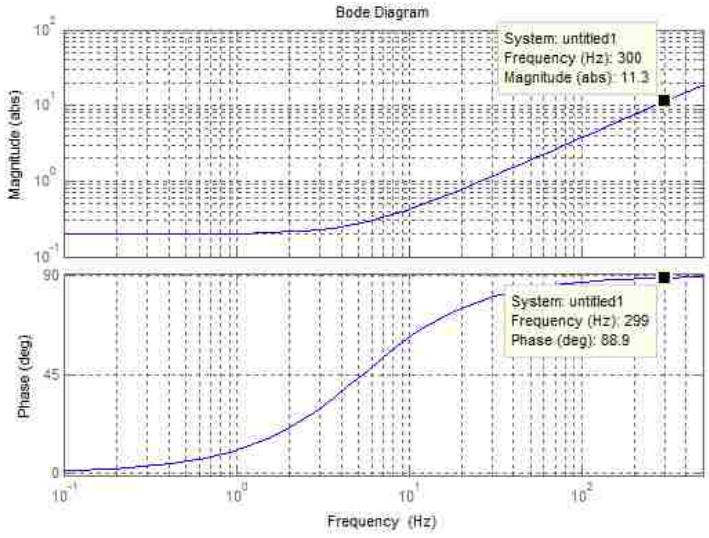


Figure 4. Extraction and conversion of 5th harmonic



$$\frac{V(s)}{I(s)} = Ls + R\Big|_{at\ 300Hz}$$

Figure 5. Magnitude and phase at 5th harmonic frequency on the bode plot

$$C5th\_abc = -11.3\begin{bmatrix} \cos(5\hat{\theta} + 88.9°) & \sin(5\hat{\theta} + 88.9°) \\ \cos\left(5\left(\hat{\theta} - \frac{2}{3}\pi\right) + 88.9°\right) & \sin\left(5(\hat{\theta} - \frac{2}{3}\pi) + 88.9°\right) \\ \cos\left(5\left(\hat{\theta} + \frac{2}{3}\pi\right) + 88.9°\right) & \sin\left(5(\hat{\theta} + \frac{2}{3}\pi) + 88.9°\right) \end{bmatrix}\begin{bmatrix} d \\ q \end{bmatrix} \quad (5)$$

Finally, the signal C5th_abc is delivered to the block diagram depicted in Figure 6. It represents the closed loop that achieves unity power factor and load voltage control. The feedback loop regulates the voltage of load R_{load} in Figure 1. and controls the grid current in phase with the grid voltage source. The voltage reference created by the loop will be compensated with C5th_abc signals. In other words, originally *cos_abc* signals are purely sinusoidal but they will become distorted after *cos_abc* are subtracted by the C5th_abc.

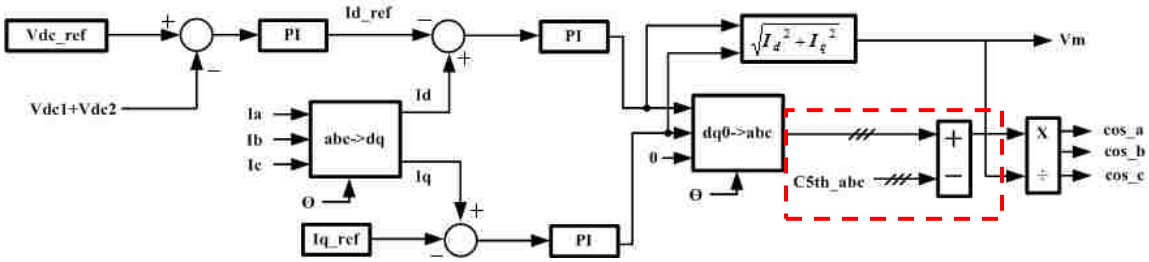


Figure 6. Voltage reference compensation in the feedback loop

V. SIMULATION

The experimental conditions are not ideal in the laboratory. So, the line-to-line grid voltages are a little bit distorted as shown in Figure 7. The simulation employs the signals of Figure 7. as grid voltage sources in order to simulate more accurately. The simulation is conducted based on MATLAB/SIMULINK and the power circuit is formed with PLECS. Figure 8. displays the normalized voltage reference for the hybrid multilevel rectifier after C5th_abc is subtracted from the sinusoidal voltage reference as explained in Figure 6. Now the voltage reference for the hybrid multilevel rectifier becomes a little bit distorted as shown in Figure 8. Figures 9.-10. depict the fundamental and the 5th grid current harmonic on stationary βα plane after applying MRF. The amplitude of the 5th harmonic is approximately 0.2 and it contains noises. In Figure 4., low pass filters are used to extract only DC terms. If the low pass filters are designed to have narrow bandwidth, the noise can be reduced but the simulation time will be longer.

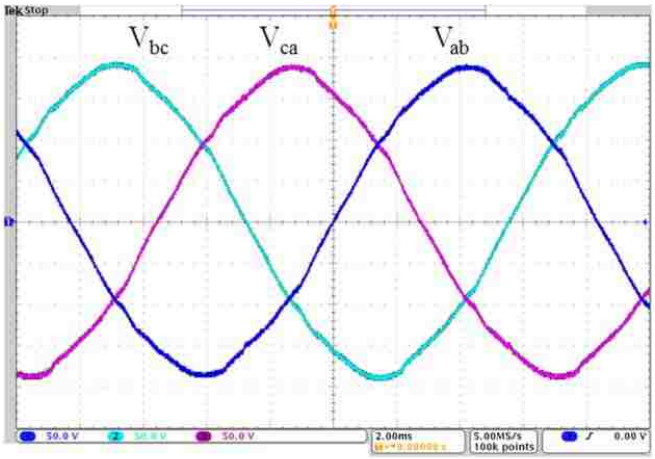


Figure 7. Grid voltage source waveforms that are used in simulation

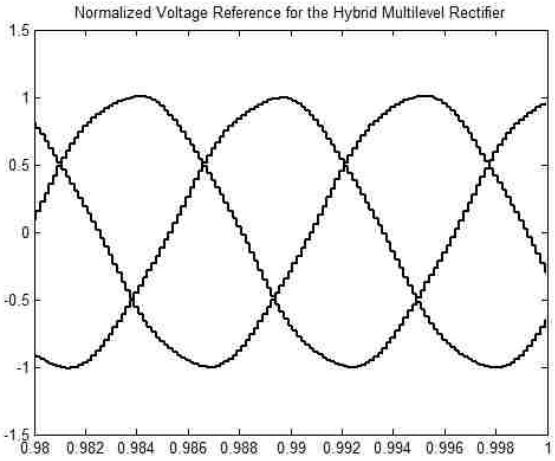


Figure 8. Normalized voltage reference for the hybrid multilevel rectifier after voltage reference compensation

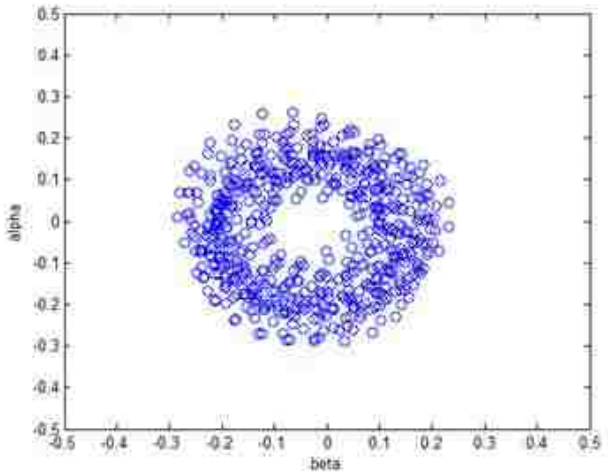


Figure 9. 5th grid current harmonic on βα plane after applying MRF

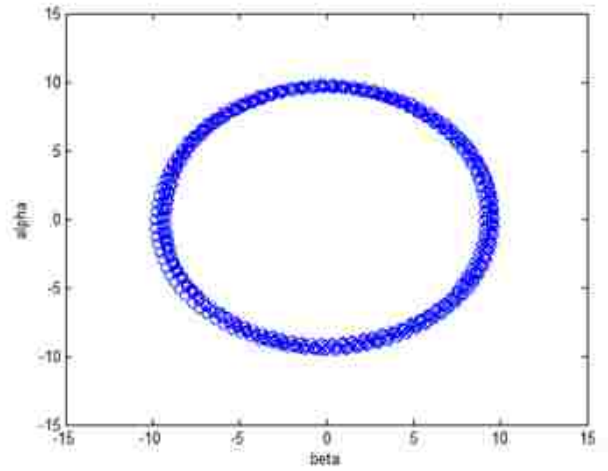


Figure 10. Grid current at fundamental frequency on βα plane after applying MRF

In the simulation results illustrated in Figures 11.-12., grid phase voltage V_{an}, grid current I_a, and hybrid multilevel rectifier output voltage V_{u0} are compared before and after the grid current compensation. In Figure 11., the grid current is distorted because the

voltage reference for the hybrid multilevel rectifier is purely sinusoidal although the grid voltage source is a little bit distorted. When grid current compensation using MRF is not activated, the THD of the grid current in Figure 11. is 4.07%. After applying MRF to calculate C5th_abc which are subtracted from purely sinusoidal voltage reference in Figure 6., the THD of the grid current has been improved to 3.18% in Figure 12.

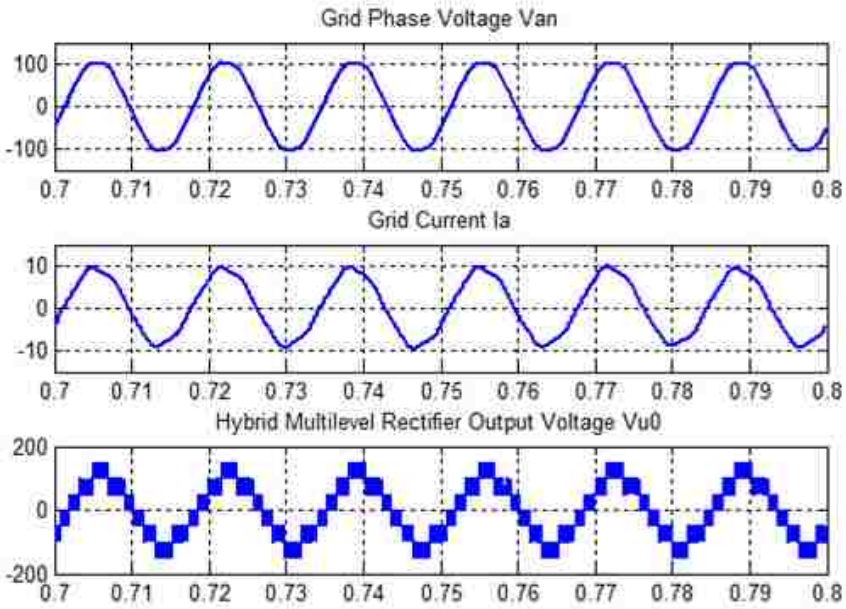


Figure 11. Simulation results representing V_{an}, I_a and V_{u0} before grid current compensation

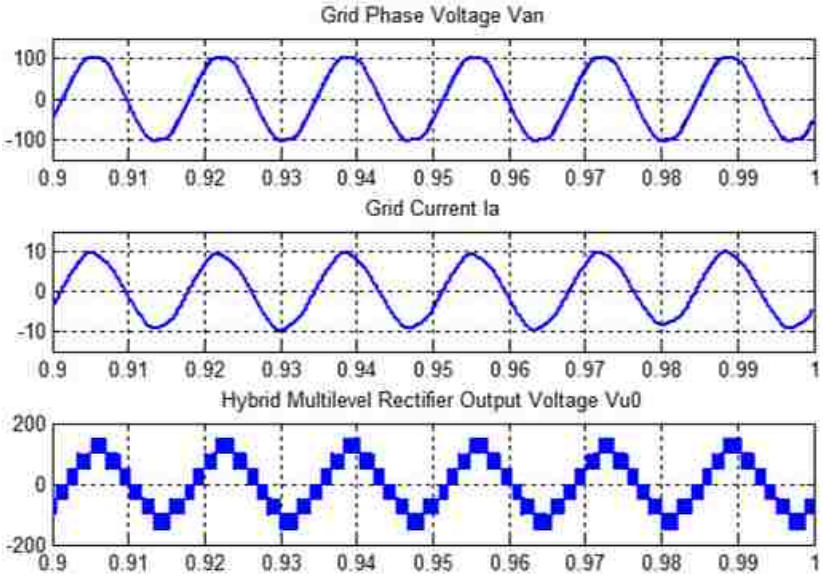


Figure 12. Simulation results representing V_{an}, I_a and V_{u0} after grid current compensation

VI. EXPERIMENTAL RESULTS

The specifications of the system are as follows: phase voltage V_{an} = 71 V_{rms}, grid frequency=60 Hz, switching frequency for CHBs = 6 kHz, sampling frequency = 6kHz, L = 6 mH, C_{upper} = C_{lower} = 11.7 mF, C_{HB} = 3.9mF, Rload ≈ 24 Ω. One TMS320F28335 DSP board which carries out operations on floating point numbers is used to send PWM signals to gate drivers. Voltage sensors are LV 25-P and current sensors are LA 55-P. The grid current's direction is set from the grid to the rectifier, since this system acts as a rectifier. The actual angle of the grid voltage will be calculated by using PLL which is designed based on synchronous reference frame in a form of a feedback loop [20]. NPC switches operate with a square waveform at 60Hz switching frequency. The DSP generates the PWM signals for the NPC through GPIO pins. Although there is a delay

between the GPIO pins and switching signals cannot be updated at the same time, GPIO pins can be used because 60Hz switching frequency is applied on GPIO pins. Figures 13.-14. show calculated grid phase voltage V_{an}, grid current I_a and the hybrid multilevel rectifier output voltage V_{u0} before and after applying the grid current compensation. As shown in Figure 13., the THD of the grid current can be calculated to 4.07% under distorted grid voltage source. In this case, the voltage reference for the hybrid multilevel rectifier is purely sinusoidal. However, after applying grid current compensation by using MRF, the THD of the grid current is improved to 3.18% in Figure 14. Since the voltage reference for the hybrid multilevel rectifier builds waveforms similar with Figure 8., the PWM at the peak of V_{u0} has been moved a little bit toward right in order to counterbalance the grid current depicted in Figure 13. Finally after the grid current compensation, I_a becomes more sinusoidal and has improved THD in Figure 14.

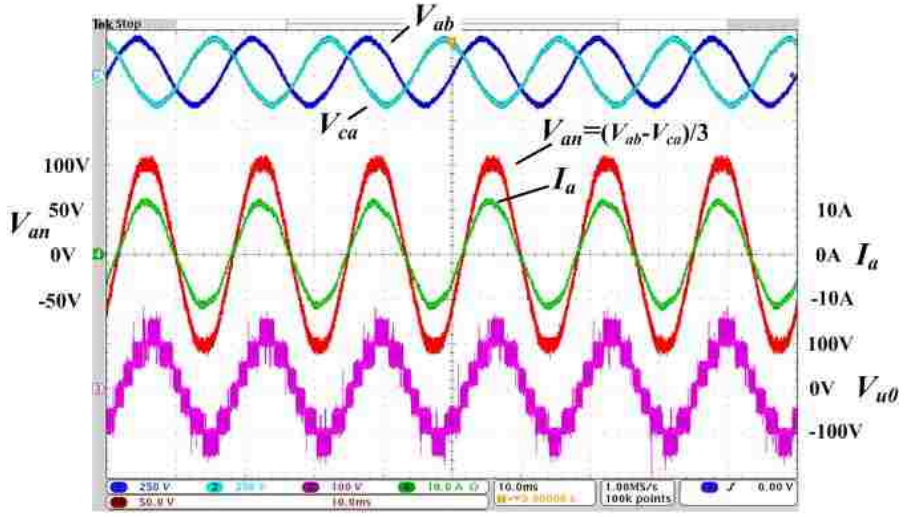


Figure 13. Experimental result without compensating the grid currents
(Grid current THD : 4.07%)

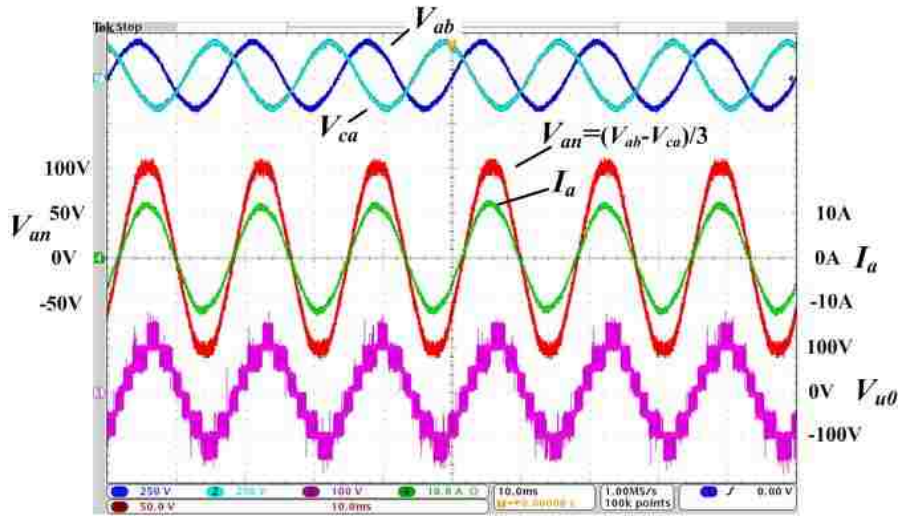


Figure 14. Experimental result after compensating the 5th harmonic on the grid currents (Grid current THD : 3.18%)

VII. CONCLUSION

The hybrid multilevel rectifier uses voltage reference to run the system. It also achieves unity power factor control and load voltage control. If the grid voltage sources are distorted, the grid current will possess low order harmonics. In order to improve the grid currents, 5th harmonic is calculated and compensated to the voltage reference by using the multiple reference theory. The control block diagram explains the process to calculate the 5th harmonic of the grid current and to compensate it to the voltage reference. Simulation reflects distorted grid voltage source condition and the results display vector trajectories on the fundamental reference frame and 5th harmonic reference frame. Experimental results represent the improved THD of the grid currents after applying the grid current compensation.

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SECTION

2. SUMMARY

In this dissertation, controlling two different multilevel topologies were investigated in grid connected rectifier application. The NPC topology has voltage unbalance problem because the neutral current flowing into and out of the neutral point of the dc link is not averagely zero. Also, with the hybrid multilevel topology having 8 capacitors which are discharged at first, large inrush currents coming from the grid might destroy the experimental set when it is connected with the grid. Furthermore, grid currents will contain low frequency harmonics when grid voltage source is distorted. In this case, a pure sinusoidal voltage reference for the rectifier cannot reduce low frequency harmonics that are contained in grid currents.

As a solution for the voltage unbalance problem on the NPC topology, paper I suggests a phase-shifting reference strategy. At first, it creates upper and lower references from one sinusoidal reference. Then, the two references are shifted in opposite directions. The degree of the phase shifting is determined by the outcome of the PI controllers. The design of the feedback loop for voltage balancing is explained with a block diagram and equations. Also, the gap and overlap situation that are occurred when the two references are shifted are examined and explained with simulation results. As a result of the proposed method, THD of the grid currents is improved a little from 7.01% to 6.18%. Experimental and simulation results verified the proposed phase-shifting reference strategy for solving the voltage unbalance problem.

Paper II suggests a pre-charge routine for a hybrid multilevel rectifier. The three phase hybrid multilevel rectifier consists of an NPC and CHBs. Therefore, it has total 8 capacitors. If they are completely discharged and the set is connected with the grid voltage source, large inrush currents from the grid might cause hazardous incidents. Moreover, the hybrid multilevel rectifier regulates each H-bridge capacitor voltages with a DSP without using independent DC power supplies. Thus, 6 H-bridge capacitor voltages should be charged before it lands on steady states which includes unity power factor control and load voltage control. The proposed pre-charge routine is comprised of several modes which accomplishes different goals. Simulation and experimental results verified the effectiveness of the pre-charge routine that lands the hybrid multilevel rectifier on steady states.

In grid connected applications, the grid currents contain low frequency harmonics if the grid voltage source is distorted. Thus, in order to reduce low frequency harmonics in the grid currents, voltage reference for the hybrid multilevel rectifier should be adjusted. Therefore, the new method to compensate the 5th grid current harmonic is proposed in the paper III. By using multiple reference frame theory, the control block diagram explains the process to calculate 5th harmonic that is contained in the grid currents. Then the calculated 5th harmonics will be extracted from the original sinusoidal voltage reference that runs the hybrid multilevel rectifier. Simulation and experimental results show the improved THD of the grid currents after applying the proposed method. Therefore, the propose method is effective to improve THD of grid currents when grid voltage source is distorted in grid connected applications.

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