Summer 2015

Stability design criteria and volt var control for distribution system with single phase solid state transformers

Darshit Girishchandra Shah

Department: Electrical and Computer Engineering

STABILITY DESIGN CRITERIA AND VOLT VAR CONTROL FOR DISTRIBUTION SYSTEM WITH SINGLE PHASE SOLID STATE TRANSFORMERS

by

DARSHIT GIRISHCHANDRA SHAH

A DISSERTATION

Presented to the Faculty of the Graduate School of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

in Partial Fulfillment of the Requirements for the Degree

DOCTOR OF PHILOSOPHY

in

ELECTRICAL ENGINEERING

2015

Dr. Mariesa Crow, Advisor
Dr. Mehdi Ferdowsi
Dr. Jonathan Kimball
Dr. Maciej Zawodniok
Dr. Bruce McMillin

PUBLICATION DISSERTATION OPTION

This dissertation consists of three articles prepared in the style according to university specifications:

Pages 3 to 27, “Stability Design Criteria for Distribution Systems With Solid State Transformers,” *IEEE Transactions on Power Delivery*, vol. 29, no. 6, pp. 2588–2595, December 2014.

Pages 28 to 36, “Stability Assessment Extensions for Single Phase Solid State Transformers,” has been accepted for future publication in Letters section of *IEEE Transactions on Power Delivery*.

Pages 37 to 58, “Volt-Var Control for Distribution System With Solid State Transformers”, was submitted to *IEEE Transactions on Power Delivery*.

ABSTRACT

Due to recent advancements in semiconductor technology, power electronic converters for high voltage, high power, and high frequency applications will soon be commercially available. Conventional single phase distribution transformers are replaced by solid state transformers (SST) in a distribution test system to investigate their interactive dynamics. Under certain circumstances, instabilities due to harmonic resonance are observed. A design criterion for solid state transformer during no load conditions has been proposed in order to avoid instability using an impedance-based analysis. Stability assessment is also extended to include the impact of distribution system voltages and system wide impedance analysis. It is shown that if the SST filters throughout the system are designed with regards to the proposed stability criterion, then system stability is guaranteed regardless of configuration. This leads to two resulting applications: (1) the order in which the SSTs are connected to the system will not generate instability if the criterion is satisfied, and (2) a system configuration change due to a fault will not produce instability. In distribution power systems, feeder voltages can be very sensitive to changes in load and/or distributed generation. A solid-state-transformer-based local voltage control strategy is introduced to reduce variability distribution system bus voltages. An on-line dynamic volt-var control (VVC) algorithm is proposed to regulate bus voltages by injecting or absorbing reactive power through a solid state transformer. The main goal of the algorithm is to enforce strict voltage constraints on the system voltages. The proposed control algorithm is validated in both a radial and meshed distribution system.

ACKNOWLEDGEMENT

First and foremost I offer my sincerest gratitude to my advisor, Dr. Mariesa Crow, who has supported me throughout my thesis with her patience and knowledge. It has been a great experience to work under her guidance and I attribute the level of my PhD degree to her encouragement and effort. I also gratefully acknowledge the support of the National Science Foundation through award number EEC-08212121 under the Engineering Research Centers program. This work is part of the Future Renewable Electric Energy Delivery and Management (FREEDM) Center. I would also like to thank Dr. Steve Glover of Sandia National Laboratories for his input.

I would also like to thank Dr. Mehdi Ferdowsi, Dr. Jonathan Kimball, Dr. Maciej Zawodniok and Dr. Bruce McMillin for serving on my committee. Especially, I would like to thank Dr. Kimball and Dr. Ferdowsi for all the guidance and help they provided during my thesis work and FREEDM LSSS project.

I would also like to thank power group students Fanjun Meng, Maigha, Tu Nguyen, Xin Qin, Venkata Anand and Bhanu Baddipadiga for their constant support and advice during my thesis work. Especially, I would like to thank Maigha for having very helpful discussions with Indian chai on various thesis topics and difficulties faced during PhD life. I would also like to thank my childhood friend Kuntal Shah for supporting me during my career.

I would like to dedicate my thesis to my family members Girishchandra Shah (Father), Chhaya Shah (Mother) and Joyal Shah (Brother). Without their support and motivation, I would not be in United States of America. I would also like to thank Shri Krishna for giving very important lessons in the form of “Bhagawad Gita”. I would like to thank all my cousins residing in USA.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1. INTRODUCTION

Distribution transformers are one of the important components of power system and are responsible for changing voltage levels while allowing power to flow through them very efficiently. Magnetically coupled transformers have been used for more than 100 years. They are a mature industrial product in terms of reliability, cost, lifetime, maintenance, stability, and efficiency. Voltage regulators are transformers with a tap and play an active role in boosting the voltages of nodes located along the feeder in radial distribution system. Transformers are inherently inductive in nature and in addition, power system loads, transmission and distribution lines are largely inductive as well. Hence, power system operates normally in with a lagging power factor. If conventional transformers could be upgraded to have the features of a voltage regulator and maintain unity power factor on the ac grid, utilities would benefit from such a device. The solid state transformer (SST) is a power electronic device that can maintain unity power factor on the ac grid and also play the role of a voltage regulator.

SSTs have been proposed as a powerful, highly flexible alternative to conventional transformers. Recent developments in semiconductor technology can make SST a reality, although the concept of the SST is not new. Multilevel converters employing IGBTs are already in use in the power system. Silicon carbide MOSFETS are being developed for use in power electronic switches for high voltage, high power, and high switching frequency applications. These switches support the development of the solid state transformer. SSTs have several attractive features: (1) SSTs can provide active compensation at the point of common coupling, (2) SSTs can provide user side voltage regulation, (3) SSTs may act as an active filter for loads, (4) SSTs provide a low voltage dc link that can be used for integrating renewable energy sources, and (5) SSTs allow bidirectional power flow. These features make the SST an attractive device for the future smart grid infrastructure.

A number of technical issues in the area of control and stability arises due to inclusion of large number of power electronic devices in a traditional ac grid. SST interactions may cause instability and harmonic resonance. The high voltage side of the SST may appear as constant power load to the ac grid, leading to voltage collapse due to negative impedance characteristics. Paper I addresses the instability caused by SST interactions and provides a stability design criteria for SST to avoid harmonic resonance during no load conditions. Paper II extends the application of stability design criteria for SSTs operating under loaded conditions.

SSTs may be used to maintain unity power factor on the ac grid. During high solar power generation, the bus voltages of the distribution system may exceed 1.05 pu. Additionally, during peak load conditions, the bus voltages may drop below 0.95 pu. The SSTs may be used to enforce strict limits for bus voltages. Paper III introduces an online dynamic DQDV algorithm to control the SST to maintain voltage in a limited range in the distribution system. The DQDV algorithm uses the bus voltage and active power flowing through SST as its inputs and generates a reactive power command for the active rectifier of the SST. If the upper voltage limit is violated, the control algorithm will direct the SST to absorb reactive power from the ac grid. Conversely, if the lower limit is violated, the SST will inject reactive power into the ac grid. The proposed DQDV algorithm performance is validated for both radial and meshed distribution systems.

PAPER

I. STABILITY DESIGN CRITERIA FOR DISTRIBUTION SYSTEMS WITH SOLID STATE TRANSFORMERS

D. G. Shah, *Student Member, IEEE* and M. L. Crow, *IEEE Fellow*

Department of Electrical and Computer Engineering,

Missouri University of Science and Technology, Rolla, Missouri 65401

1. INTRODUCTION

Distribution transformers are an integral component in the delivery of electrical power to the end customer. The distribution transformer provides voltage transformation by stepping down the voltage from the distribution circuit to the voltage level used by the customer. Conventional distribution transformers are passive components and without additional capabilities cannot provide voltage regulation, reactive power support, or power quality improvement. Solid state transformers (SST) have been proposed as a powerful, highly flexible alternative to conventional transformers [1]-[4]. SSTs are insensitive to harmonics or user-side faults, can perform power factor correction and voltage regulation, and do not use potentially toxic coolant oils.

A solid state transformers consists of three stages: an active rectifier, and bi-directional dc-to-dc dual active bridge converter, and an inverter as shown in Figure 1. These three stages together provide the key attractive features of the SST. The solid state transformer can provide active compensation to the point of grid coupling; therefore it can draw unity power factor or provide reactive compensation for voltage regulation. Additionally, it can provide active filtering to the load side such that the load is isolated from momentary sags, swells, and harmonics on the ac grid. Furthermore, the low voltage dc link can provide a dc bus to which photovoltaic panels, energy storage devices, or electric vehicle chargers can be connected. These additional features and flexibility provide a platform with which to build the future smart grid infrastructure.

The inclusion of a high number of power electronic converters in a traditionally ac grid introduces a number of technical issues in control and stability that have not previously been encountered. One area of concern is the potential for instability caused by SST interactions. This instability may take the form of a harmonic resonance induced by the interaction of the input impedance and the source output impedance [5]. Regardless of the

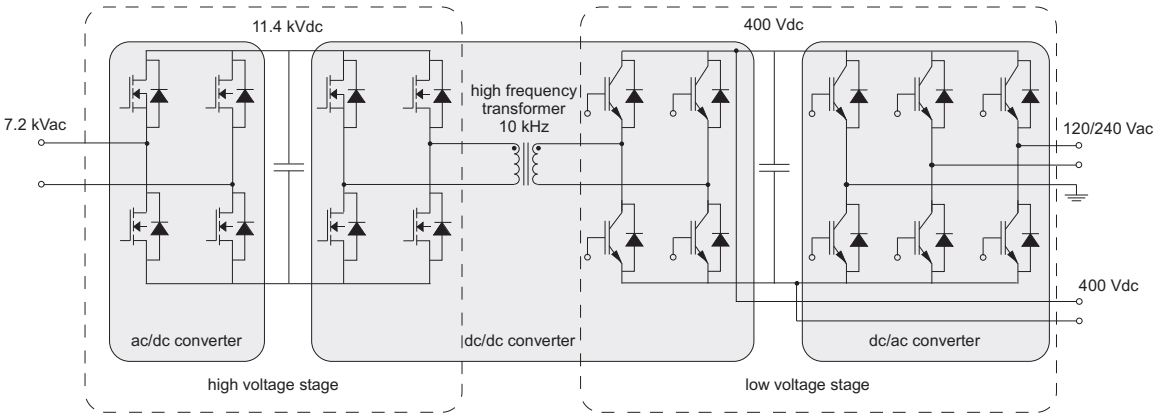


Figure 1 Solid state transformer

load composition on the customer side, the active front end of the SST (the high-voltage rectifier) will appear to the ac grid as a constant power load [5]. Constant impedance loads are generally considered to be self-correcting loads in that as the voltage decreases, the power consumption will also decrease. Constant power loads however, draw the same power and are sometimes referred to as "negative impedances" and can destabilize dc networks if not properly designed [4]. This type of instability is not frequently experienced in ac distribution systems, but may become increasingly prevalent with the advent of SSTs. It is anticipated that SSTs will replace many, if not all, conventional transformers and the ability to "plug-and-play" without additional design considerations is desirable. In this paper, we analyze the circumstances that may lead to SST interaction and instability and propose a design approach to avoid this problematic behavior.

Similar harmonic behavior is reported to have been generated by high frequency converters used for railway locomotives during low load conditions [8]. A theory of resonance stability analysis of railway systems is proposed in [9] based on the energy exchange principles between infrastructure and locomotive converters. A proof of an empirical input admittance criterion as a special case of results is provided by [9]. The concept of input admittance criterion and its application to the stability of railway systems is also discussed

in [10]. The shaping of the input admittance of the converter is discussed in [11] to achieve a positive real part of the admittance for a certain frequency range. It is shown that oscillations of a certain frequency will not occur if, for that frequency, the input admittance has positive conductance (i.e. is passive). Passivity helps to improve stability of systems in which interactions between the power system infrastructure and the converters occurs. A similar approach for improving stability by making the system passive for the entire frequency region is proposed in [12].

2. SST INTERACTIONS

To illustrate the impact of multiple SSTs in a distribution system, three (out of the total of 16 SSTs) are placed on the *b* phase of a modified IEEE 34 bus distribution test system (see Figure 2). The IEEE 34 bus distribution system was selected as the benchmark test case due to several attractive features: (1) it is a three-phase system with moderately unbalanced loads by phase; (2) the feeder requires voltage regulation (capacitors and tap changers); and (3) the system data was developed by the IEEE PES Distribution System Analysis Subcommittee's Distribution Test Feeder Working Group and is publicly available [12]. This case study is used to demonstrate instability occurring in the distribution system with multiple solid state transformers.

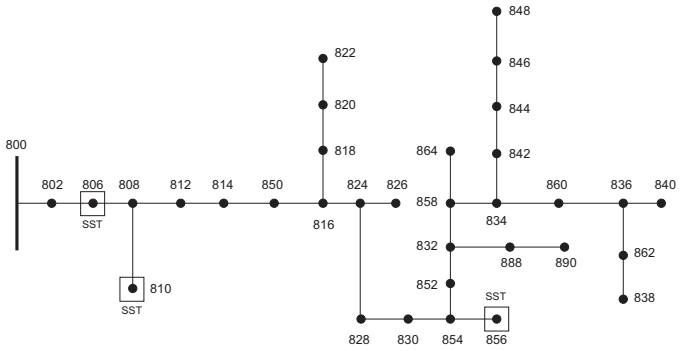


Figure 2 IEEE 34 bus distribution test system with 3 SSTs

The following assumptions are made:

- The SSTs are all single-phase to better accomodate the single-phase feeder laterals
- The SSTs are energized under no-load
- The substation is modeled as a constant voltage source

- An RL filter is placed at the first stage active rectifier
- The SSTs are aggregated to provide a 200 kVA power rating at each bus (for consistency with the IEEE 34 bus distribution system)
- The rated phase (line) input high-side voltage is 7.2 (12.47) kV
- The regulated output voltage of the SST is 120V/240V
- The SSTs provide voltage regulation to the system, therefore all capacitor banks and voltage regulators are removed from the test system
- The SSTs use DQ control [13] (see Appendix)

Topologies for three phase SSTs are still in the development stage and as a result will likely follow single-phase SSTs to market, therefore this study is restricted to single-phase SSTs.

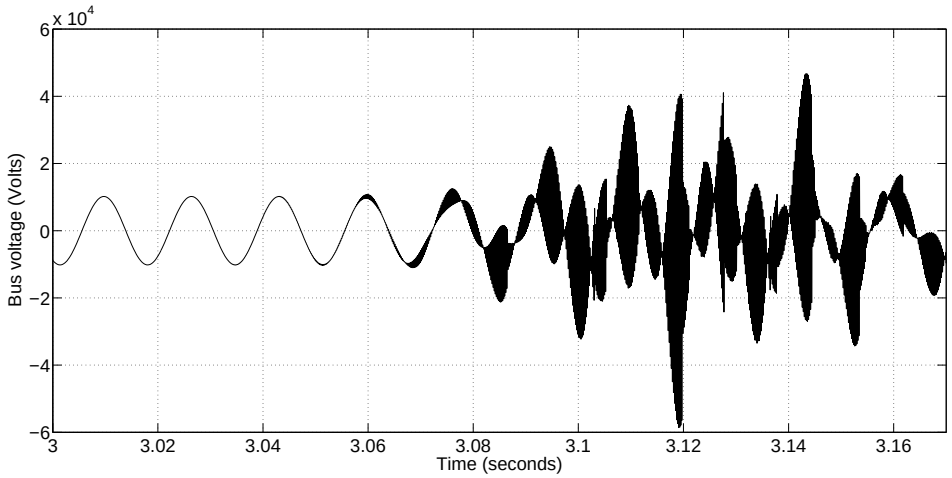
The three stages of the SST are connected in cascade, as shown in Figure 1. The active rectifier stage of the SST is connected to the high voltage capacitor and regulates the high voltage dc link at 10 kV. The actual topology of the active rectifier consists of three series connected H-bridge rectifiers. Each H-bridge rectifier is connected to the high voltage dc link and a dual active bridge converter. The output of each dual active bridge converter is connected in parallel. These dual active bridge converters regulate the low voltage dc link to 400 V. A split phase inverter is connected to the low voltage dc link and regulates the output voltage. The topology shown in Figure 1 is a simplified representation of the actual SST topology. The SST is energized at no load and brought to a stable operating point before it is connected to the distribution system.

The three solid state transformers are connected sequentially from the substation down the feeder. The SST at bus 806 is connected at 1 second, the SST at bus 810 is connected at 2 seconds, and the SST at bus 856 is connected at 3 seconds. Figs. 3(a), 3(b), and 3(c) show the bus 856 ac voltage, ac current, and SST high-side dc link voltage from

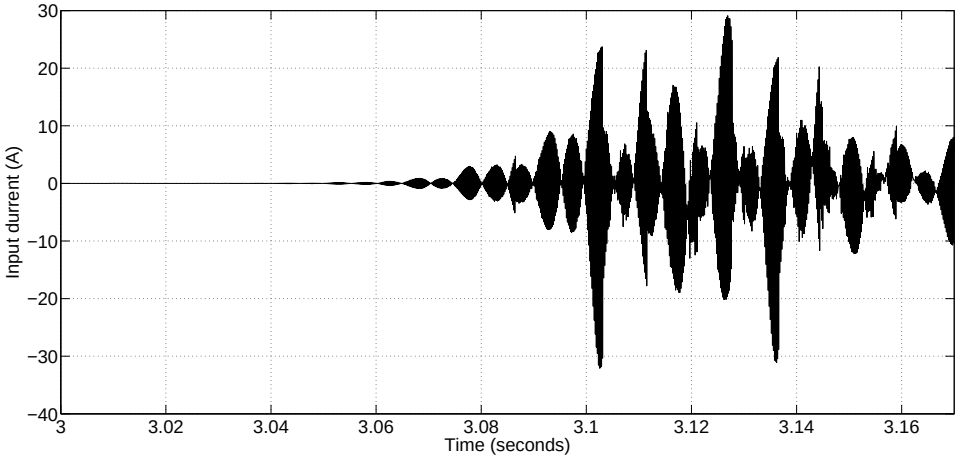
the time SST 856 is connected at no load. Note that the dc link voltage is uncontrolled and the SST bus voltage and current become increasingly erratic. We hypothesize the primary reason behind this behavior is the violation of an impedance-based (similar to the Middlebrook) stability criterion.

According to this impedance-based stability criterion, the source impedance for any system must be less than the load impedance at all frequencies to ensure stability. Therefore it is not surprising that the SST node (electrically) farthest from the substation should cause the instability when connected, since the source output impedance increases along the feeder. For this reason, an impedance-based stability criterion is used.

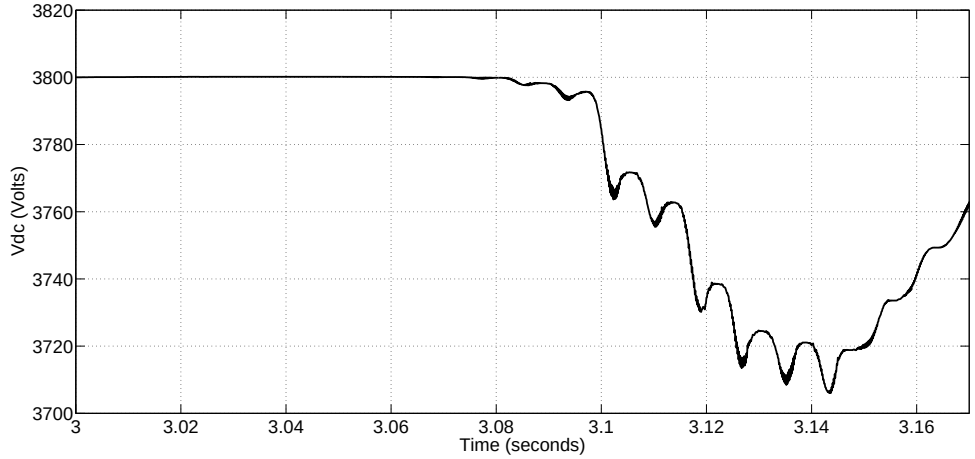
In this paper, the system is simulated in PSCAD using average value models of the active rectifier, dual active bridge converter and inverter to accurately replicate the behavior of the SSTs. Full switch-level models are not used due to the limitations of the simulation complexity and computational time. The average value models were developed directly from the switching models and validated experimentally [13]. A linear time invariant model is required to apply any stability criteria. To fulfill this requirement, the voltage and current controllers of active rectifier are tuned using state space analysis explained in [15]. Proportional and integral gains of controllers are present as variables in the system matrix derived using state space analysis. For a given set of gains, elements of the state matrix are independent of time. Thus, the model of the active rectifier used in the simulation is linear time invariant. The average value model of the dual active bridge converter and inverter also use linear proportional integral regulators for regulating their respective voltages. Their respective controls are summarized in the Appendix.



(a) ac voltage



(b) ac current



(c) dc link voltage

Figure 3 Bus 856 SST responses

3. IMPEDANCE-BASED STABILITY

It has been shown that distribution systems with a high penetration of photovoltaics may have sustained harmonic resonance or other erratic behavior due to interference with inverter current control loop [16]. The application of existing impedance-based stability criteria to grid-connected converters is problematic because, depending on the frame of reference, either the inverter or the grid can be modeled as the source. This can lead to contradictory stability considerations. Since the distance from the substation is a contributing factor in the SST stability, we take the approach that the grid is the source. To apply an impedance-based stability criterion to the SST-deployed system, the system to be analyzed is modeled as a source and a load subsystem. The source subsystem consists of a voltage source (V_s) in series with the Thevenin equivalent source impedance (Z_s). The load subsystem consists of the input impedance of the converter (Z_{in}) in series with source subsystem, as shown in Figure 4. It should be noted that this simple linear system representation is only valid for small-signal analysis.

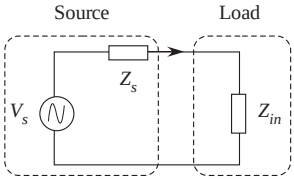


Figure 4 Voltage source with source impedance and input load impedance

The SST is connected to the distribution system through an *RL* filter with filter resistance R_f and filter inductance L_f as shown in Figure 5. The high-side ac source voltage is denoted by V_{hs} whereas the input to the active rectifier is V_{in}. The magnitude and phase of the sinusoidal input voltage V_s is controlled with four quadrant DQ control, therefore it

is represented as a controllable voltage source [13]. During energization, the SST is not loaded, therefore the input impedance is dominated by the filter impedance.

The direction of the active power flow depends on the relative phase difference between the source voltage and the input voltage. The direction of the reactive power flow depends on the relative phase difference between the source voltage and current. In the absence of voltage regulation commands, the active rectifier will have unity power factor operation. The input impedance $Z_{in}(s)$ is the impedance looking into the active rectifier. Its transfer function is comprised of the filter impedance, the controller impedance, and the load impedance. The source impedance $Z_S(s)$ is the impedance looking from the SST towards the substation and is calculated for each bus at which an SST is connected.

The load current transfer function can be expressed

$$I(s) = H(s)\frac{V_s(s)}{Z_{in}(s)} \tag{1}$$

where

$$H(s) = \frac{1}{1 + Z_s(s)/Z_{in}(s)} \tag{2}$$

Assuming that the source voltage $V_s(s)$ and $Z_{in}(s)$ are stable, then the stability of the load depends on $H(s)$. The Nyquist Criterion states that a necessary and sufficient condition for stability of the system is that the $H(s)$ does not encircle the $(-1,0)$ point in complex space. The Middlebrook Criterion was proposed specifically to provide input filter specifications to ensure that the converter dynamics are not adversely impacted. The Middlebrook Criteria states that the system is stable if $\|Z_s(s)/Z_{in}(s)\| < 1$. This states that the transfer function $H(s)$ must remain within the unit circle.

The Nyquist plot of $\frac{Z_s(s)}{Z_{in}}$ at bus 856 is shown in Figure 6. Clearly the Nyquist contour does not encircle the $(-1,0)$ point nor does any part of the contour lie outside the unit circle (the Middlebrook criterion), yet the system is displaying instability. This indicates that there are factors to be considered which are not captured by these basic criteria. We

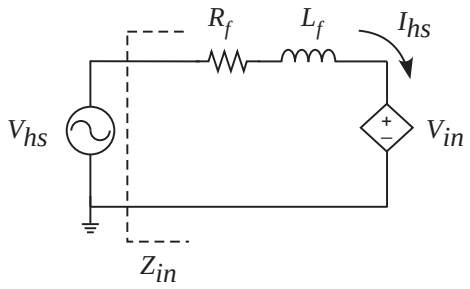


Figure 5 Equivalent circuit of active rectifier

propose an alternative stability design consideration in the following section.

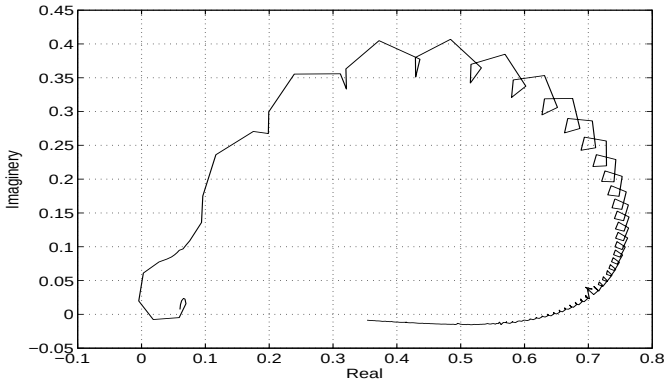


Figure 6 Nyquist plot of $\frac{Z_s(s)}{Z_{in}}$ at bus 856 (filter = 5.8%)

4. STABILITY-BASED DESIGN

The SST farthest electrically from the substation will see the largest source impedance. In a radial system, this impedance is calculated as the sum of the impedances of the laterals and feeder from the SST to the substation. For a looped system, however, the source impedance must be obtained either through an impedance calculation by injecting a nominal current and voltage at the SST bus, or from the bus impedance matrix. In the bus impedance matrix, the Thevenin equivalent for each bus in the system can be obtained from the diagonal of the bus impedance matrix that corresponds with the SST bus. One significant issue to consider is that all capacitor banks were removed from the system because the SSTs can provide voltage regulation. This has the additional impact of increasing the system impedance which further exacerbates the input impedance-source impedance mismatch.

The input impedance of the SST is difficult to calculate analytically due to the multiple stages and controls. Therefore a harmonic perturbation technique is used to numerically extract the input impedance from the SST model. To calculate the impedance at each frequency, a sinusoidal voltage harmonic having a peak magnitude of 3.36% of the fundamental component of the phase voltage is injected into the circuit model of the active rectifier (shown in Figure 5). The resulting current is measured and the respective current harmonic peak magnitude and phase are calculated using a discrete Fourier transform. The input impedance is the ratio of the voltage phasor to the current phasor. This process is repeated to extract the input impedance for frequencies ranging from 10 Hz to 15 kHz. The resulting gain and phase of the source impedance and input impedance at bus 856 are shown in Figs. 7 and 8.

The effect of the phase-locked-loop (PLL) is taken into account while calculating the input impedance using the harmonic perturbation method. To validate the accuracy of the

PLL, the results were repeated with two different approaches. In the first approach, the voltage angle was measured directly in the simulation using a multimeter. In the second approach, a single-phase PLL was used to calculate the angle. Both approaches yielded identical results.

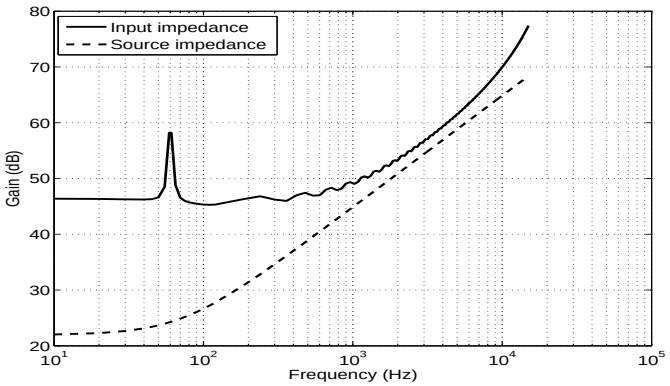


Figure 7 Bus 856 source and input impedance magnitudes (filter = 5.8%)

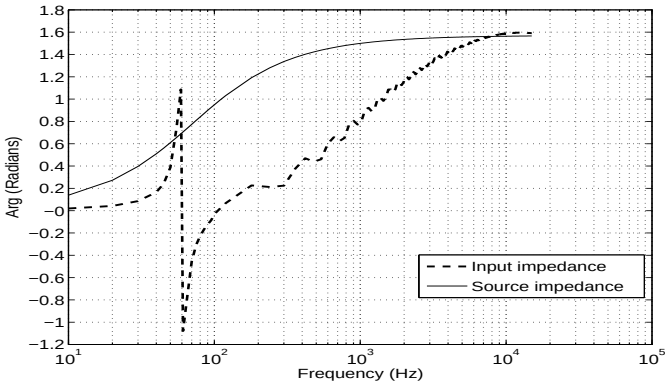


Figure 8 Bus 856 source and input impedance phases (filter = 5.8%)

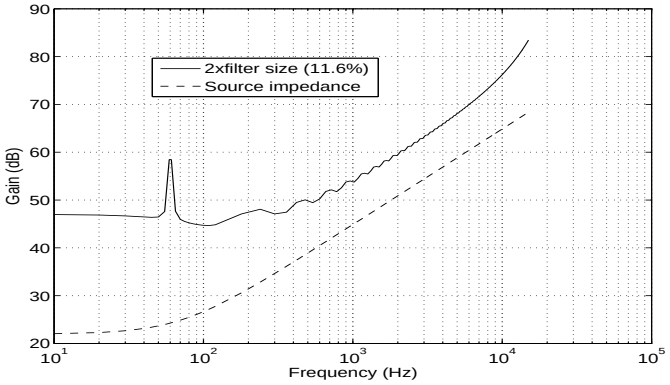


Figure 9 Source and input impedances at bus 856 (filter = 11.6%)

One possible explanation for the observed instability is the proximity of the source and input magnitudes indicating that the ratio is approaching 1.0 at higher frequencies. A good design practice requires that the gain margin of 6dB be maintained [17]; this margin is violated in Figure 7 explaining the exhibited instability. This is not a design issue that occurs with conventional transformers and is therefore seldom experienced in a distribution system. Therefore care must be taken with the deployment of SSTs. We propose a design criterion that provides guidance to size the input filter such that harmonic instability can be avoided. Specifically, we propose that system stability can be assured if the input filter is chosen such that the input impedance magnitude exceeds the source impedance. Now, using the stability criterion, it stands to reason that if the SST filters were selected such that the input impedance magnitude exceeded the source impedance, then the system would remain stable.

This condition is similar to Middlebrook criterion. This criterion (as with other similar criterion) is conservative and should be considered a sufficient condition and purely empirical in nature. If the condition is not satisfied, then it does not imply instability. The important application of empirical criterion lies in improving overall system stability by mitigating harmonics while integrating SSTs into the distribution system.

To test this hypothesis, the filter impedance at SST 856 is doubled. The resulting source and input impedances at bus 856 are shown in Figure 9. In this case with the larger filter size, the source impedance lies significantly below the input impedance of the SST, implying that the system should now be stable. The corresponding current and voltages are shown in Figs. 10(a)-10(c) for when the SST at 856 is energized at 3 seconds. These results are much improved over the original responses shown in Figs. 3(a)-3(c) and indicate that the system can be stabilized by appropriately sizing the SST input filter with respect to the source impedance.

The next step is to extend this hypothesis to encompass the entire system and all SSTs. To explore this behavior, all 16 SSTs are placed in the phase *b* of IEEE 34 bus testsystem. The electrically farthest SST in phase b is at bus 890 as indicated by the circle in Figure 11. The source and input impedances at bus 890 are shown in Figure 12. Note that in this case the input impedance magnitude is exceeded by the source impedance for a wide range of frequencies. Applying the proposed stability criterion indicates that this system will most likely exhibit instabilities, which indeed the system does. The left side of Figure 14 shows the ac voltage, ac current, and dc voltage of the SST located at node 890. The SST is connected to the system under no-load at 3 seconds. Note that all states exhibit considerable erratic behavior.

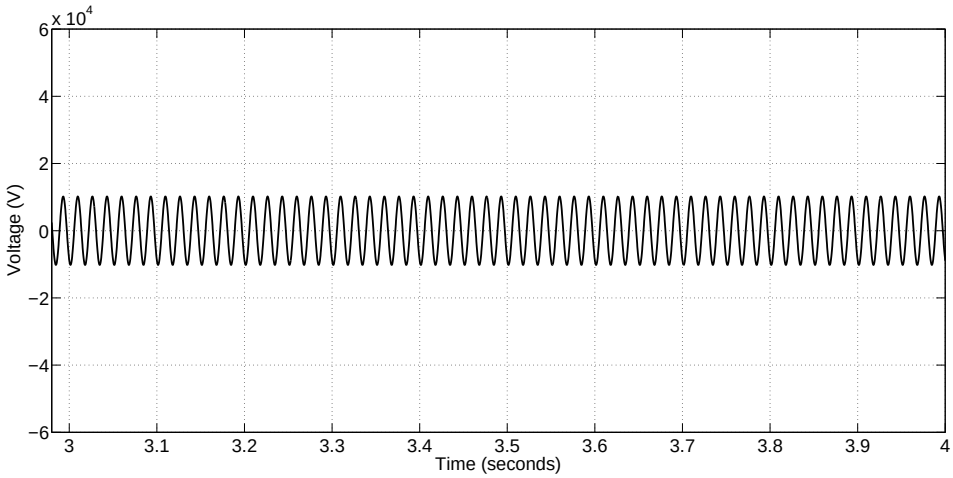
The design approach will now be extended to the SST at bus 890. Figure 13 shows the source impedance at SST 890 against several input impedances having filter sizes ranging from the original filter size (5.8%) up to three times the original filter size. This figure includes the trace for the original filter size shown in Figure 12. In addition, traces for twice ($2\times$) and three times ($3\times$) the original filter size. The source impedance crosses both the original and double filter sizes but not the $3\times$ trace. The proposed criterion indicates that if the filter size at 890 is selected to meet or exceed $3\times$ the original filter size, then the system will be stable. This design approach is validated with the simulation results shown in Figure 14. These results are obtained for a filter size of $3\times$ the original filter size at

all SSTs. The waveforms in Figure 14 compare the system responses for the original and resized filters. It is apparent that the system can be stabilized with appropriate filter sizing.

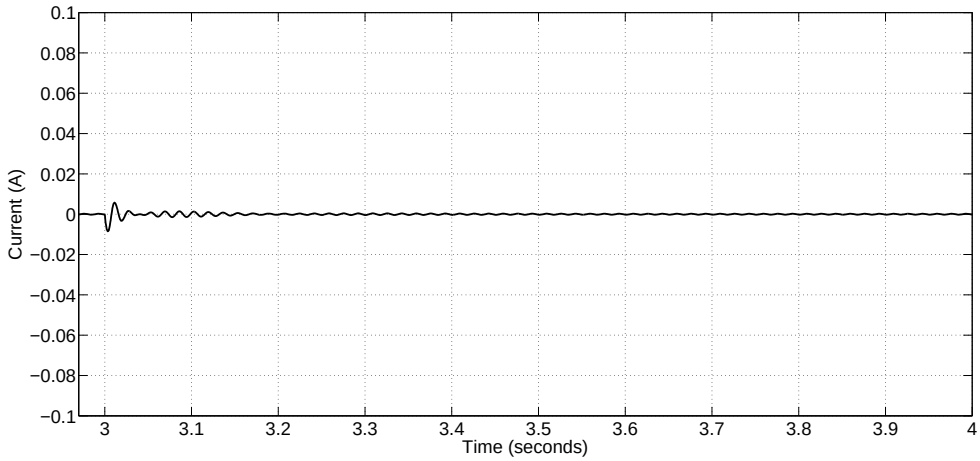
There is a qualitative synergy between the proposed approach and input admittance passivity. A purely passive system acts like a first order system for all frequencies [12]. For a system to be passive, the real part of the impedance or admittance must be positive for all frequencies. Similarly, the phase of the impedance must lie between between $-\pi/2$ and $\pi/2$. References [9]-[11] explain the role of an empirical input admittance criterion for improving the stability of converters. It can be inferred from the definition of passivity that for a particular frequency, if the impedance is active (i.e. not passive), then oscillations of this particular frequency can become amplified. Furthermore, due to limitations in control bandwidth it is not possible to have a passive impedance over all frequencies. However, control strategies can be designed to shape the impedance to be passive for a desired range of frequencies at which oscillations in the system can occur. Thus, the choice of filter size can move the impedance phase into regions which are more easily controllable.

Increased filter size may adversely affect efficiency due to changes in current. In our experience, the resulting decrease in efficiency was usually less than 0.1%. This result is based on simulation trials and may differ from actual performance. The decrease in efficiency must be weighed against the improvement in system stability.

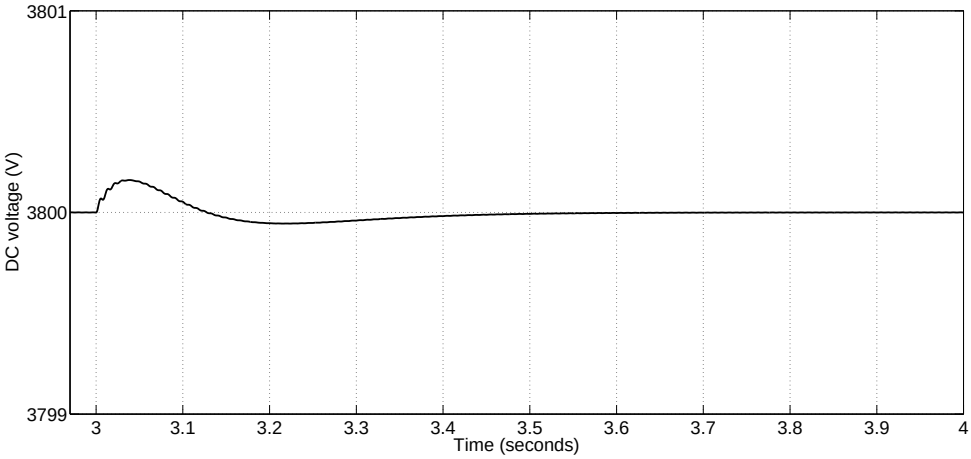
As a final note, different filter sizes may have an impact on the dynamic operation of the SST, but this effect is limited due to the number of frequency changes and control from SST input to output. There are two dc links (high voltage and low voltage) and a high frequency transformer (see Figure 1) thus limiting most filter size effects to the feeder side of the SST.



(a) ac voltage



(b) ac current



(c) dc link voltage

Figure 10 Bus 856 SST responses with resized filter

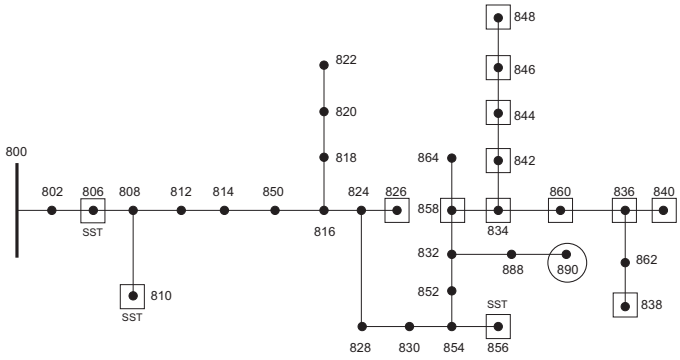


Figure 11 IEEE 34 test system with electrically farthest SST

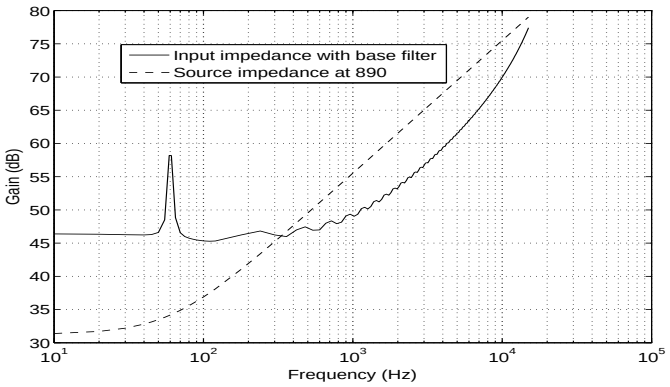


Figure 12 Source and input impedances at bus 890, base filter size

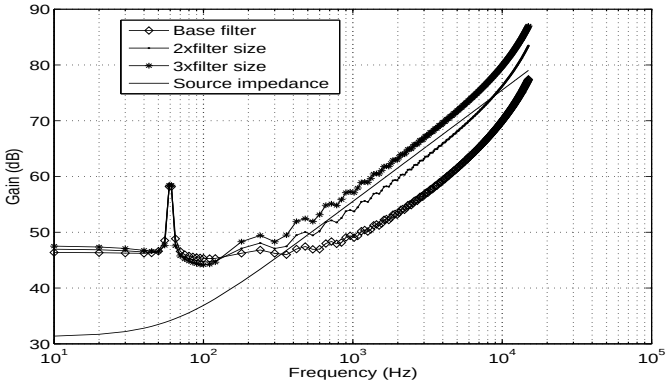
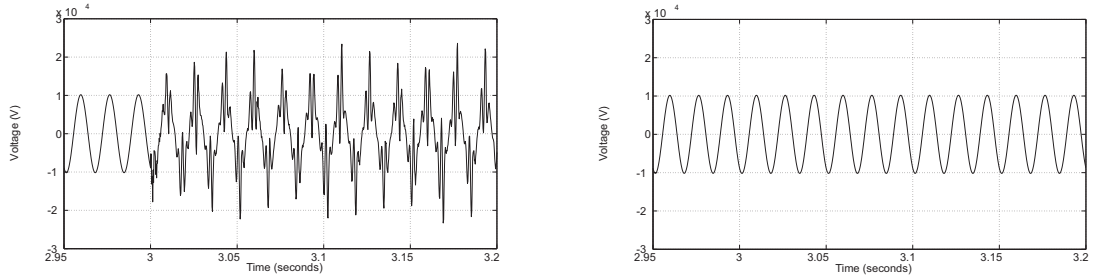
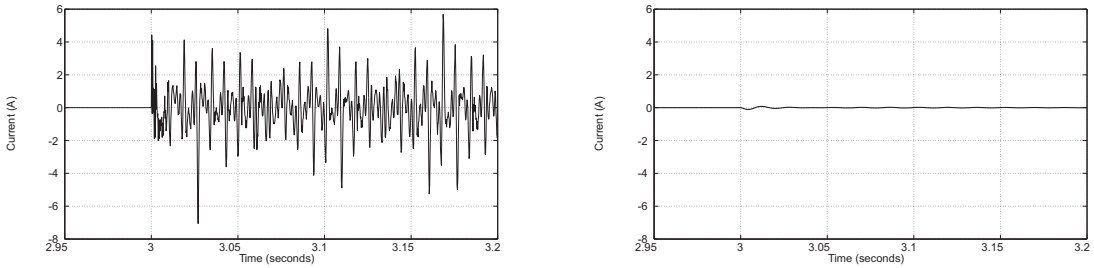


Figure 13 Source and input impedances at bus 890, multiple filter sizes



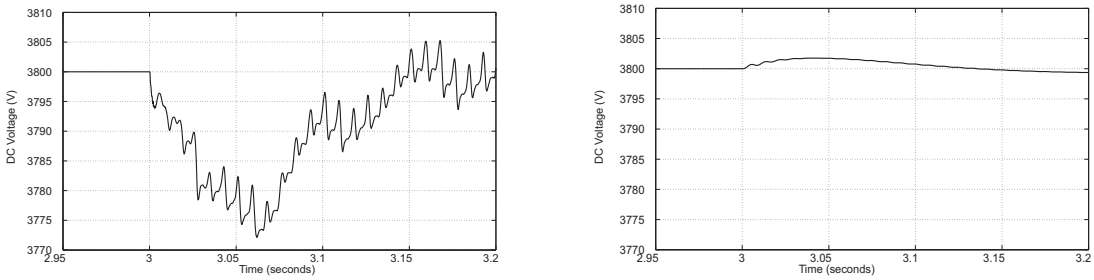
original filter resized filter

(a) ac voltage



original filter resized filter

(b) ac current



original filter resized filter

(c) dc voltage

Figure 14 Bus 890 SST responses with all 16 SSTs on system

5. CONCLUSIONS AND FUTURE WORK

In this paper, we establish the potential for instability when SSTs are energized in a distribution system. This type of "harmonic resonance" or "negative impedance" is seldom experienced in legacy power systems, but may become increasingly prevalent in systems with high penetrations of power electronics-based components that are connected directly to the AC grid. We have proposed a design criterion for the SST input filter to mitigate instabilities in the system. This design approach was validated through simulation on the IEEE 34 bus distribution system testbed.

In this paper, we concentrated on the energization of the SSTs. This is under SST no-load conditions. Furthermore, we considered each phase of the distribution system individually. Future work will focus on the impact of various load types on stability. Furthermore, we will expand this analysis to a three-phase system in which mutual coupling may impact the "per-phase" analysis we've presented.

6. SST CONTROL

The stability discussion presented in the previous sections tacitly assumed that all of the internal SST controllers are stable and that all instability occurred due to the mismatch in the source and input impedances. The SST is designed to be stable as a standalone device (this can be validated by observing that the system remains stable when only one SST is energized close to the substation). However, for completeness, we include the models of the SST controllers in this appendix.

6.1. ACTIVE RECTIFIER

The control of the active rectifier is a DQ vector controller with cross coupling terms. A phase-locked-loop (PLL) is used to calculate the frequency (ω_e) and phase (θ_e) of the source voltage (V_{hs}). The DQ vector controller is shown in Figure 15 where the starred values ($*$) indicate commanded values. If unity power factor is desired, then the commanded value of I_q^* is set to zero. The PI gains are tuned using the method presented in [15]. The input voltage V_{in} is calculated

$$V_{in} = \sqrt{V_{dd}^2 + V_{qq}^2 \sin(\omega_e t + \phi)} \tag{3}$$

where

$$\phi = \tan^{-1} \frac{V_{qq}}{V_{dd}}$$

where V_{hdc} is the high voltage dc voltage.

A correction factor of π radians is added or subtracted from ϕ depending on the sign of V_{dd}. If V_{dd} is positive, the ϕ is not corrected. If V_{dd} is negative and V_{qq} is positive, then π radians are added to ϕ. Similarly, if V_{dd} is negative and V_{qq} is negative, then π radians are

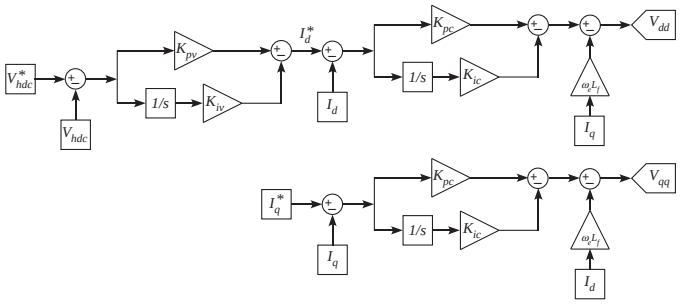


Figure 15 DQ vector controller

subtracted from ϕ.

6.2. DUAL ACTIVE BRIDGE AND INVERTER

The dual active bridge converter (DAB) consists of a high voltage H-bridge, a high frequency transformer, and a low voltage H-bridge. The low voltage dc link voltage V_{ldc} is regulated by the dual active bridge converter. The DAB is bi-directional. The active power flows across the DAB:

$$P_{DAB} = \frac{V_{hdc} V_{ldc} d_{dc} (1 - d_{dc})}{2 L_l f_h} \tag{4}$$

where d_{dc} is the ratio of the time delay between the high and low bridges to one half of a switching period. L_l is the leakage inductance and f_h is the switching frequency. The control is shown in Figure 16.

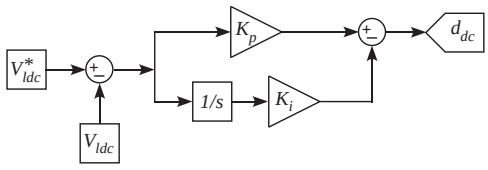


Figure 16 DAB controller

The DC/AC split phase inverter is shown in Figure 17. Each phase consists of a controlled voltage source with an LC filter and load. The positive (V_p) and negative (V_n) output voltages have a 180° phase shift. The output voltages are regulated at an RMS voltage of 120 V at 60 Hz. The duty cycle control for D_1 and D_2 is shown in Figure 18.

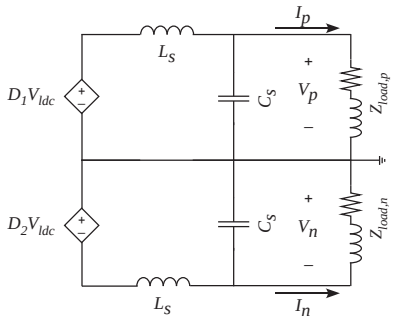


Figure 17 Inverter

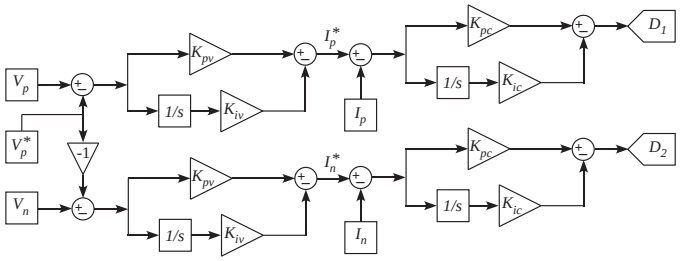


Figure 18 Inverter control

BIBLIOGRAPHY

[1] E. R. Ronan, S. D. Sudhoff, S. F. Glover, and D. L. Galloway, "A power electronic-based distribution transformer," *IEEE Transactions on Power Delivery*, vol, 17, no. 2, pp 537–547, April 2002.

[2] X. She, A. Q. Huang, and R. Burgos, "Review of the solid state transformer technologies and its application in power distribution system," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, early access, 2013.

[3] H. Qin and J. W. Kimball, "Solid-state transformer architecture using ac-ac dual-active-bridge converter," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 9, pp. 3720-3730, 2013.

[4] X. She, A. Q. Huang, S. Kukic, and M. E. Baran, "On integration of solid-state transformer with zonal dc microgrid," *IEEE Transactions on Smart Grid*, vol. 3, no. 2, pp. 975–985, 2012.

[5] J. Sun, M. Chen, and K. J. Karimi, "Analysis and mitigation of system interactions involving single-phase PFC converters," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 44, no. 1, pp. 217–226, 2008.

[6] N. Bottrell, M. Prodanovic, and T. C. Green, "Dynamic stability of a microgrid with an active load," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 5107–5119, November 2013.

[7] A. Kwasinski and C. Onwuchekwa, "Dynamic behavior and stabilization of dc microgrids with instantaneous constant-power loads," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 822âĂŞ-834, March 2011.

[8] E. Meollerstedt, B. Bernhardsson, "Out of control because of harmonics-An analysis of the harmonic response of an inverter locomotive," *IEEE Control Syst. Mag.*, vol. 20, no. 4, pp. 70-81, August 2000.

[9] I. Pendharkar, "Resonance stability in electrical railway systems-A dissipativity approach," *European Control Coneference (ECC)*, vol. 4574, no. 4579, pp. 17-19, July 2013.

[10] A. Paice, M. Meyer, "Rail network modeling and stability: the input admittance criterion," *The 14th Int. Symp. Math. Theory Netw. Syst.*, Perpignan, France, 2000.

[11] L. Harnefors, M. Bongiorno, S. Lundberg, "Input-admittance calculation and shaping for controlled voltage-source converters," *IEEE Trans. Ind. Electron.*, December 2007.

[12] M. Jansson, A. Danielsson, J. GaliÂt'c, K. PietilÃd'inen, L. Harnefors, "Stable and passive traction drives," *European Power Electronics and Drives Association (NORPIE)*, Trondheim, Norway, 2004.

[13] IEEE PES Distribution System Analysis Subcommittee's Distribution Test Feeder Working Group, "Distribution Test Feeders," [Online] `http://ewh.ieee.org/soc/pes/dsacom/testfeeders/`

[14] T. Zhao, J. Zeng, S. Bhattacharya, M. Baran, A. Q. Huang, "An Average model of solid state transformer for dynamic system simulation," *Proc IEEE Power & Energy Society Meeting*, Calgary, AB, July 2009.

[15] N. Bottrell, M. Prodanovic, T. C. Green, "Analysed small signal state-space model of an active rectifier," *Universities Power Engineering Conference (UPEC)*, Cardiff, Wales, September 2010.

[16] J. Sun, "Impedance-based stability criterion for grid-connected inverters," *IEEE Trans on Power Electronics*, vol. 26, no. 11, Nov. 2011.

[17] A. Riccobono, E. Santi, "Comprehensive review of stability criteria for DC distribution systems," in *Proc. IEEE ECCE*, pp.3917-3925, 2012.

II. STABILITY ASSESSMENT EXTENSIONS FOR SINGLE PHASE SOLID STATE TRANSFORMERS

D. G. Shah, *Student Member, IEEE* and M. L. Crow, *IEEE Fellow*

Department of Electrical and Computer Engineering,

Missouri University of Science and Technology, Rolla, Missouri 65401

1. INTRODUCTION

An empirical design criterion for solid state transformers (SST) is proposed in [1] for ensuring steady-state stability by shaping the input impedance of the SST under no load operating conditions. This letter extends the proposed design criterion for full load conditions and provides a method for stability assessment of distribution system with solid state transformers under loaded conditions. This design criterion is similar to the Middlebrook criterion. Regardless of the type of load connected to the SST, the front end of the SST (the high voltage active rectifier shown in Figure 1) will appear as a constant power load to the ac grid [5]. It is well known that these loads have negative impedance characteristics and can reduce damping and create steady-state instabilities [3] [4].

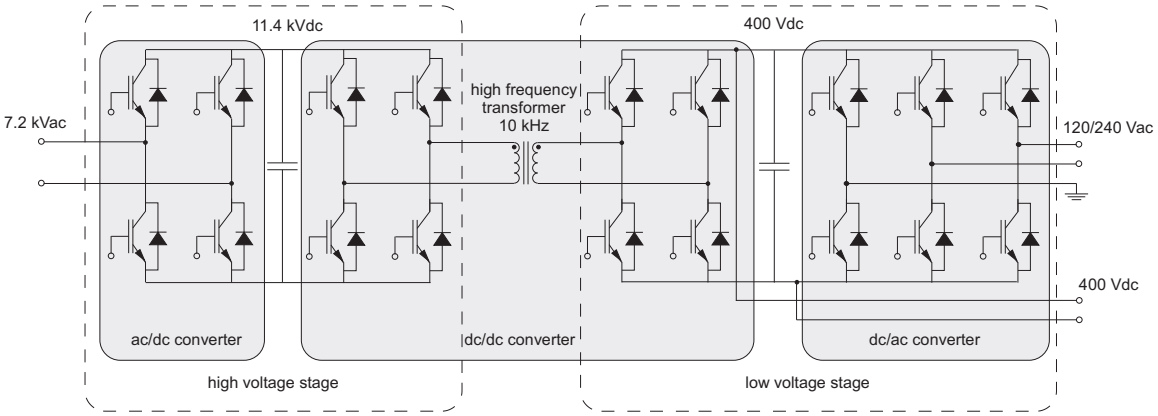


Figure 1 Solid state transformer

This letter extends the no load design criterion based on the SST input impedance [1] to full load conditions.

A modified method is introduced for calculating the source impedance seen by the solid state transformer and a stability assessment is performed for each SST in the system.

The principal goal of the assessment method is to predict steady-state instabilities due to each SST by using line and load data, the location of SSTs, and the input impedance of each SST.

To illustrate the full load design process, SSTs are placed at 16 locations in the IEEE 34 bus test system [12]. SSTs operate at unity power factor and thus absorb only active power from the distribution system, but may supply reactive power to the load through the secondary voltage-source converter. The voltages at the secondary are held to 1.0 per unit, whereas the primary side voltages are functions of the voltage drops along the distribution line. The primary side node voltages have a significant impact on the SST source impedance.

2. STABILITY ASSESSMENT AND DESIGN

The principal goal of the letter is to provide a general filter design procedure to avoid instabilities in the system with SSTs. Since the design process accounts for SST loading, several modifications are required during the calculations of the impedances to accurately reflect the node voltages.

The source impedance is the impedance looking from the SST towards the substation and is calculated for each bus at which an SST is connected. Since all SSTs are connected in shunt, the Thevenin equivalent source impedance seen by a SST is a parallel combination of other SST impedances and line impedances. The input impedance of the SST is difficult to calculate analytically due to the multiple stages and controls, therefore a harmonic perturbation technique is used to numerically extract the input impedance from the SST model. To calculate the impedance at each frequency, a sinusoidal voltage harmonic having a peak magnitude of 3.36% of the fundamental component of the phase voltage is injected into the circuit model of the active rectifier. The resulting current is measured and the respective current harmonic peak magnitude and phase are calculated using a discrete Fourier transform. The input impedance is the ratio of the voltage phasor to the current phasor. This process is repeated to extract the input impedance for frequencies ranging from 10 Hz to 15 kHz.

Figure 2 shows the source impedances and input impedance of the SST at node 890 with multiple filter sizes. An RL filter is typically placed at the input of the SST to mitigate harmonics. The base filter impedance is $5.8\angle 89.62^{\circ}\%$ on a 7.2kV/200kVA base. To vary the filter size, the percent impedance was varied; the impedance angle remained constant. Note that at high frequencies, the inductance will dominate the filter impedance. In [1], it was determined that to maintain stability, the input filter must be sized such that input impedance exceeded the source impedance over all frequency ranges. At the base filter

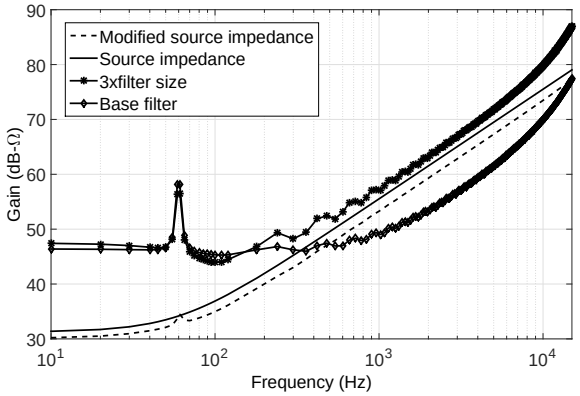


Figure 2 Source and input impedances at bus 890, multiple filter sizes

impedance, this stability criterion is violated. However, by increasing the filter size (3× in this example), the criterion is satisfied and stability is guaranteed.

The "modified source impedance" shown in Figure 2 is the input impedance of the SST calculated from the updated procedure that accounts for load and voltage conditions, whereas "source impedance" denotes the no-load case. Note that the modified source impedance provides a less conservative prediction of stability, allowing smaller filter sizes to be used while maintaining the stability margin stated by the criterion.

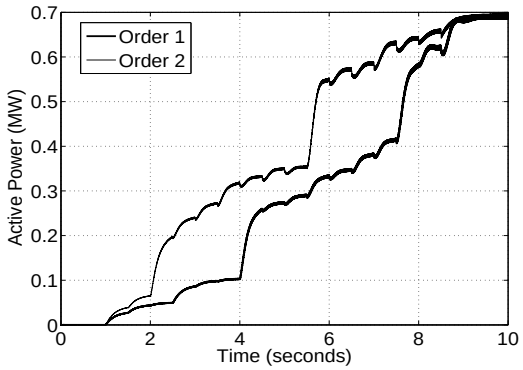


Figure 3 16 SSTs connected to IEEE 34 in different order

3. SYSTEM TOPOLOGY CHANGES

One of the resulting benefits from the assessment process is that if the stability requirements are satisfied, then there will be no impact on the stability due to order in which the SSTs are connected to the distribution system. To illustrate this, Figure 3 shows the active power measured at the substation for two different connection orders of 16 SSTs in the IEEE 34 bus test system. Note that the system reaches a stable operating point after each SST added regardless of configuration.

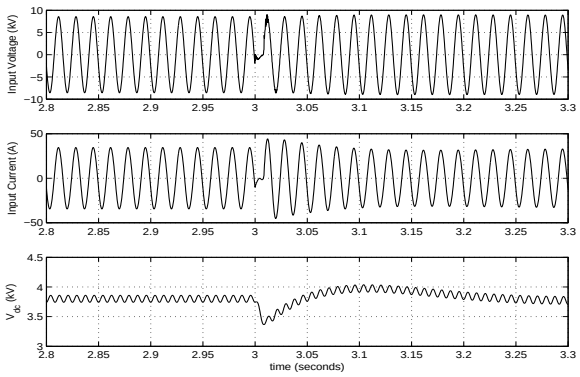


Figure 4 Bus 890 SST responses during pre-fault and post-fault condition

Another important result based on the assessment procedure is that a system configuration change after a fault will not cause instability. For example, a single phase fault occurs at bus 834 at 3 seconds and is cleared in 4 ms. The radial feeder downstream from node 858 is disconnected from the system and the 8 SSTs on the disconnected feeder are disengaged. Figure 4 shows the pre- and post-fault voltage, current and dc link voltage of the SST at node 890. At three seconds, a dip in the dc link voltage can be seen due to fault. Since the fault is cleared within 4 ms, the dc link voltage returns to the pre-fault voltage

even though the system configuration has changed. Similar results are observed for other SSTs after the change in system configuration. As the system configuration changes, the equivalent impedance seen by each SST varies between the boundaries of maximum source impedance and modified source impedance accordingly. Therefore, if the input impedance of each SST is designed such that it does not overlap these boundaries, then instabilities due to system configuration change can be avoided.

Note however, that the fault current profile on a SST dominated distribution feeder is considerably different than that of a conventional feeder [6]. When a fault occurs on the feeder, the SST is designed to disengage from the system if the ac bus voltage drops below 0.7 pu or above 1.2 pu and will continue to draw active power otherwise. For this reason, the impact of the filter size is only one of many considerations a protection scheme must consider and the long-term implications are not known at this time.

4. CONCLUSIONS

In this letter, we extended the application of the impedance-based stability criterion to the distribution system with SSTs during loaded conditions. For a given filter size, this criterion provides a stability guarantee for the system. Furthermore, if the SST filters throughout the system are designed with regards to the stability criterion, then system stability is guaranteed regardless of configuration. This leads to two resulting applications: (1) the order of connection of SSTs will not generate instability if the criterion is satisfied, and (2) a system configuration change due to a fault will not produce instability.

BIBLIOGRAPHY

[1] D. Shah and M. Crow, "Stability Design Criteria for Distribution System with Solid State Transformers," *IEEE Trans on Power Delivery*, in press.

[2] N. Bottrell, M. Prodanovic, and T. C. Green, "Dynamic stability of a microgrid with an active load," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 5107–5119, November 2013.

[3] M. H. Kent, W. R. Schmus, F. A. Mccrackin, and L. M. Wheeler, "Dynamic Modeling of Loads in Stability Studies," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-88, no. 5, May 1969.

[4] A. Kwasinski and C. Onwuchekwa, "Dynamic behavior and stabilization of dc microgrids with instantaneous constant-power loads," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 822âĂŞ-834, March 2011.

[5] IEEE PES Distribution System Analysis Subcommittee's Distribution Test Feeder Working Group, "Distribution Test Feeders," [Online] `http://ewh.ieee.org/soc/pes/dsacom/testfeeders/`

[6] H. Hooshyar and M. Baran, "Fault Analysis on Distribution Feeders Employing Solid State Transformers," *Proceedings of the 2014 IEEE Power & Energy Society General Meeting*, Washington, DC, 2014.

III. VOLT-VAR CONTROL FOR DISTRIBUTION SYSTEMS WITH SOLID STATE TRANSFORMERS

D. G. Shah, *Student Member, IEEE* and M. L. Crow, *IEEE Fellow*

Department of Electrical and Computer Engineering,

Missouri University of Science and Technology, Rolla, Missouri 65401

1. INTRODUCTION

The concept of "smart-grid" is predicated on the ability to implement localized control in power systems. The current trend in power system is to move away from centralized control and develop demand side controls to improve system response and reliability. Local voltage control is one of the examples of decentralization in power systems. This paper proposes a DQDV algorithm that is integrated with suitable power electronic devices such as an SST to reduce the voltage variation along the feeder. Local voltage control has several advantages that include (1) voltage regulation independent of load profile, (2) fast response time, (3) no centralized calculations, and (4) no communication requirement between the SSTs and the substation. The main strategy of the local voltage control is to enforce strict voltage constraints for the bus voltage by injecting or absorbing reactive power through the SST. The amount of reactive power required is computed by the proposed DQDV algorithm and injected or absorbed via the SST power electronic interface with the system.

Solid state transformers (SST) are powerful alternatives to conventional distribution transformers [1]-[4]. As shown in Figure 1, a solid state transformer has three stages: the active rectifier, the bidirectional dual active bridge dc/dc converter, and the split phase inverter. The ability to provide load side voltage regulation is a key feature of the SST. Additionally, due to the active rectifier, the SST can provide simultaneous active compensation at the point of feeder coupling, therefore it can easily contribute reactive power support for voltage regulation. The feeder side of the SST is an active rectifier and as a result, appears as a constant power load to the ac grid, irrespective of the load connected on the low voltage side [5]. The SST has the capability to regulate the user side voltage to 1.0 per unit even if ac grid voltage is much higher or lower. Furthermore, the SST has the ability to reflect any desired power factor, within the limits of the SST rating. For example, it may be desired for each SST to operate at unity power factor, or to compensate for reactive line losses such

that the substation operates at unity power factor. Another approach is to provide sufficient control to maintain all system voltages within a pre-specified range.

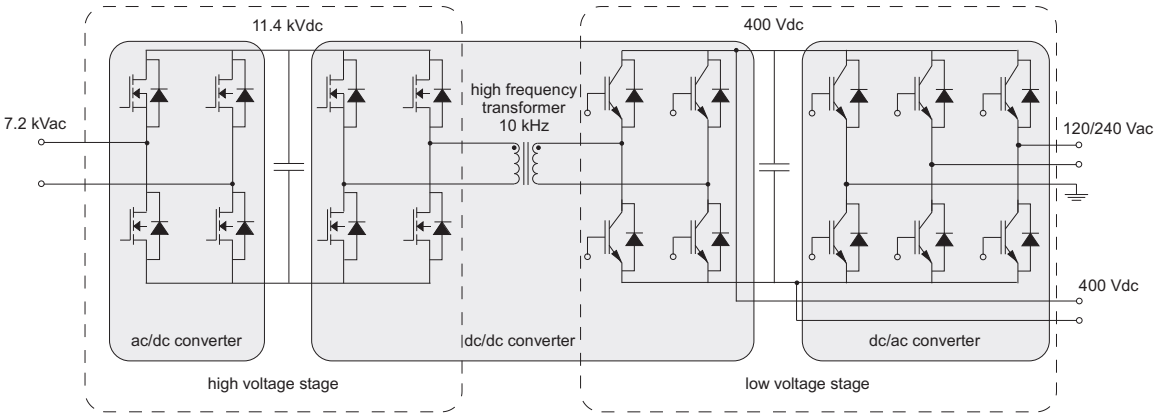


Figure 1 Solid state transformer

SST-based volt-var control was first introduced in [6]. The primary goal of the control strategy in [6] is to minimize system power losses while enforcing voltage limits across the system. The method proposed in [6] is a centralized approach that assumed that all SSTs participate in the volt-var control. Furthermore, implementation of the volt-var control requires communication of all bus voltages to the central controller. The concept of local voltage control that we introduce in this paper is in sharp contrast to the strategy introduced in [6] in that our proposed method does not require centralized computation nor is it applied at every SST. Only a subset of SSTs at particular “pilot” nodes participate in the volt-var control, leaving the remaining SSTs available for other functions. In the absence of voltage control, the SSTs in this paper operate in unity power factor mode by default.

2. ONLINE DQDV ALGORITHM FOR LOCAL VOLT-VAR CONTROL

The SST can perform voltage regulation on the high voltage ac side as well as the low voltage ac side. The proposed volt-var control is used to control the voltage at the high voltage ac side. In this work, it is assumed that all magnetic transformers in the distribution system have been replaced by solid state transformers. This is a generalization and in practice, not all transformers are required to be SSTs, only the transformers at the pilot buses. In the absence of voltage control, the SSTs operate in unity power factor mode. The main goal of the algorithm is to enforce strict real time voltage constraints for sensitive buses with the help of reactive power compensation from the SSTs. The VVC proposed in this paper is accomplished in two steps. In the first step, the pilot buses are identified. In the second step, the proposed voltage control algorithm is implemented to enforce strict voltage constraints.

Voltage and line current sensitivities can be used to identify sensitive buses in a radial distribution system. As the distance from the substation increases, the voltage sensitivity of the buses also increases [7]. Efficient calculation of voltage and current sensitivities is necessary for properly estimating sensitive buses. A new approach of calculating voltage and current sensitivities is proposed in [8]. Although we adopt the method of [7], there are a variety of ways to locate sensitive buses and it is plausible that other methods may be effective. Sensitivity in relation to location can also be used to locate sensitive buses in a distribution system [9]. Loss sensitivity factors can also be used to locate sensitive buses in radial distribution system. The loss sensitivity factor is able to predict which bus or buses will have the biggest loss reduction when reactive power is injected through that bus [10]. A reactive power margin can also be used to identify the weakest bus in the distribution system [11]. Any of these methods are suitable for determining the pilot buses for SST-based volt-var control. The pilot SSTs are typically selected to be electrically distant from

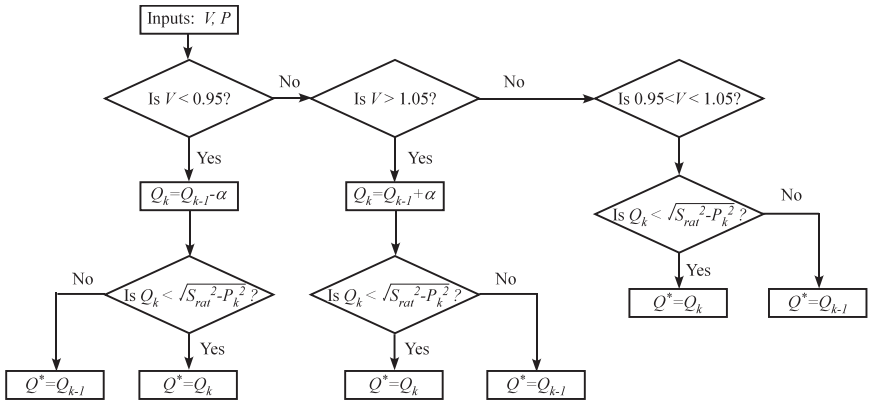


Figure 2 DQDV algorithm flowchart

one another such that their volt-var control effects are localized and do not cause “ringing” in control efforts between SSTs.

Figure 2 shows the flowchart of the proposed DQDV algorithm. The bus voltage and load power are the inputs and the reactive power command is the output. The core concept of algorithm is to determine the required reactive power injection/absorption to maintain the bus voltage within strict limits. The lower voltage constraint is set to be 0.95 pu and the upper voltage constraint of 1.05 pu are selected as strict voltage limits for buses where local voltage control is performed. There are three parallel paths in the algorithm, as shown in Figure 2. These paths are as follows:

- If the current bus voltage is below 0.95 per unit, the algorithm will command the active rectifier to inject reactive power into ac grid at the next time step. The injection of reactive power increases by a rate defined by α.

- If the current bus voltage is above 1.05 per unit, the algorithm will command the active rectifier to absorb reactive power into ac grid at the next time step. The absorption of reactive power increases by a rate defined by α.

- If the current bus voltage is between 0.95 and 1.05 per unit, the algorithm maintains

the previous reactive power command

The rate α can be defined as amount of reactive power injected or absorbed per time interval. The magnitude of α is a variable and can be tuned as per the operating speed requirement. In real time, the algorithm behaves as linear discrete integrator and integrates Q with respect to time with gain equal to α.

The algorithm also enforces a power constraint on the reactive power command. The power constraint states that reactive power command and current real power measurement should not exceed the apparent power rating of the SST. If the limit is violated, then the previously stored reactive power command should override the calculated reactive power command. The power constraint is applied for both the injection and absorption processes. The reactive power command is translated to the current command I_q^* and is input to the DQ vector control of the front end active rectifier as described in Section 5.

3. THE DQDV ALGORITHM IN A RADIAL SYSTEM

The IEEE 34 bus test system is selected as the test system for the implementation of the DQDV algorithm. The IEEE 34 system one-line diagram is shown in Figure 3. The IEEE 34 bus test system has several attractive features for use as a test bed case: (1) it is an unbalanced three phase system, (2) without SST volt-var control, voltage regulators are required to maintain the feeder voltages, and (3) the system data is publicly available [12]. Since the voltage rating of the single phase SST is 7.2 kV, the voltage rating of the original IEEE 34 has been changed from 24.9 kV L-L to 12.47 kV L-L. All parameters, including line impedances, have been converted to a consistent base. SSTs are placed at all load buses and unless they are a pilot SST, they will hold unity power factor. Pilot SSTs are located at bus 890 (all phases) and bus 822 (*a* phase - denoted by a circle), bus 810 (*b* phase - denoted by a square), and 806 (*c* phase - denoted by a diamond). Since the phases are not balanced and are not all three-phase, the pilot SSTs are located on different phases.

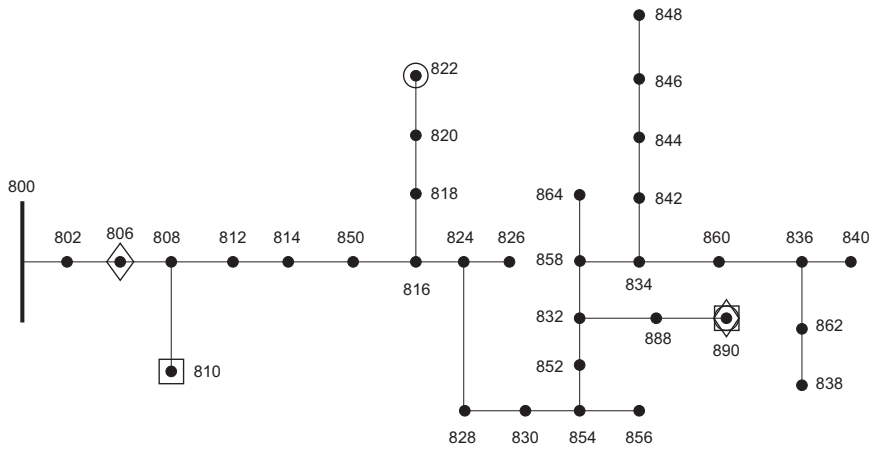


Figure 3 The IEEE 34 bus distribution test system

The following assumptions are made regarding the test system:

- The substation is modeled as a constant voltage source
- The substation voltage is set to 1.05 per unit
- The rated phase (line) input high-side voltage is 7.2 (12.47) kV
- The regulated output voltage of the SST is 120V/240V
- The SSTs are aggregated to provide a 200 kVA power rating at each bus
- The SSTs are all single-phase
- All loads are converted to wye-connected RL loads
- The SSTs are energized under no load conditions and then connected to distribution system

The peak load data is given in Table 1. The load varies throughout the day in accordance with the normalized load curve shown in Figure 4, which represents a typical residential load. The solar insolation at each pilot bus is shown in Figure 5.

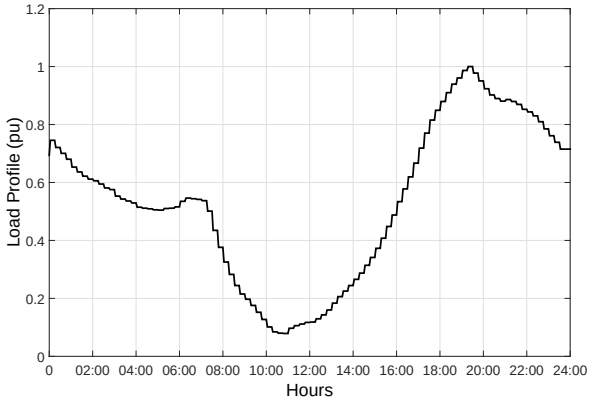


Figure 4 Daily load profile

Table 1: Peak Load data of IEEE 34

$Node$	kW_A	$kVAr_A$	kW_B	$kVAr_B$	kW_C	$kVAr_C$
806	0	0	30	15	25	14
810	0	0	16	8	0	0
820	34	17	0	0	0	0
822	135	70	0	0	0	0
824	0	0	5	2	0	0
826	0	0	40	20	0	0
828	0	0	0	0	4	2
830	17	8	10	5	25	10
856	0	0	4	2	0	0
858	7	3	2	1	6	3
864	2	1	0	0	0	0
834	4	2	15	8	13	7
860	36	24	40	26	130	71
836	30	15	10	6	42	22
840	27	16	31	18	9	7
838	0	0	28	14	0	0
844	144	110	135	105	135	105
846	0	0	25	12	20	11
848	20	16	43	27	20	16
890	130	75	130	75	130	75

Figs. 6-8 show the results of the algorithm on the voltage magnitude at bus 890. Note that without volt-var control, the competing effects of the diurnal load and the solar insolation cause the uncontrolled voltages to violate both the minimum and maximum voltage limits. However, once the VVC algorithm is implemented, the voltages are maintained within the operational boundaries.

To see the impact of the proposed volt-var control at the substation, the active and reactive power measured at the substation with and without control is shown in Figure 9. Note that due to the high penetration of solar power, the active power at the substation goes negative indicating that the distribution feeder is supplying active power through the substation to the remainder of the network. Note that without VVC, the power factor at

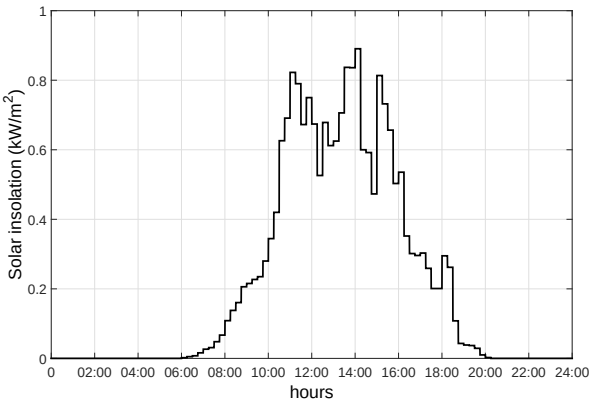


Figure 5 Daily solar profile

the substation is maintained at near unity as a design feature of the SSTs. However, as the SST pilot buses assume volt-var control, the reactive power changes to accommodate the commanded controls. However, even with the proposed VVC, the power factor is still near unity.

Lastly, it is important to also note that the load side voltage is unaffected by the variation in voltages at the feeder side. Figure 10 shows the corresponding load side voltage (phase *a*) at bus 890. The other phases have similar profiles.

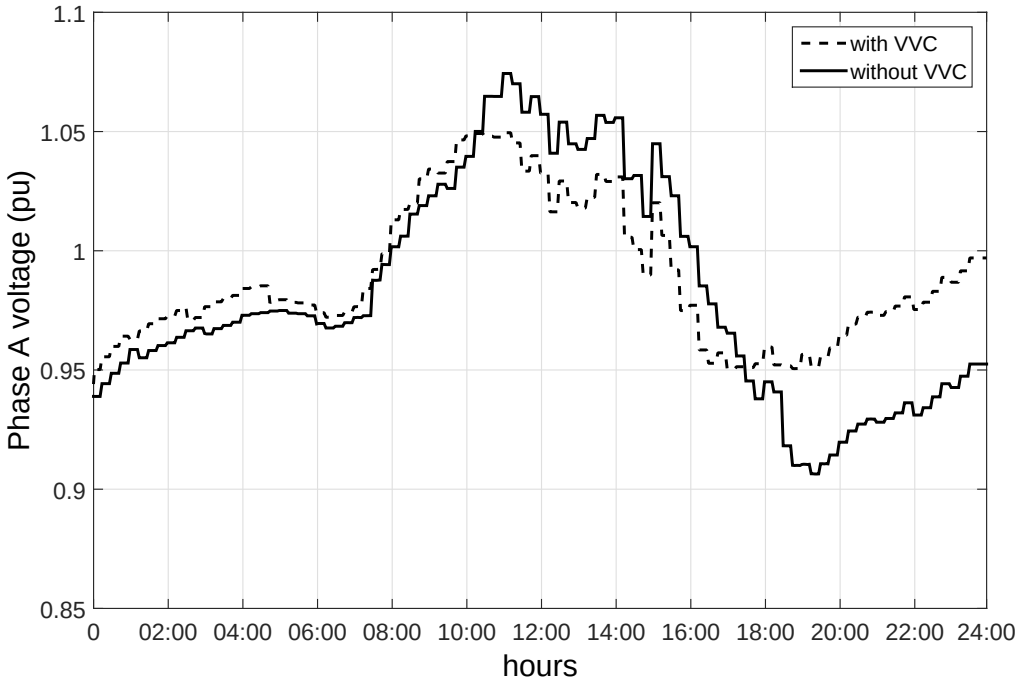


Figure 6 Node voltage of phase A at SST 890 – radial system

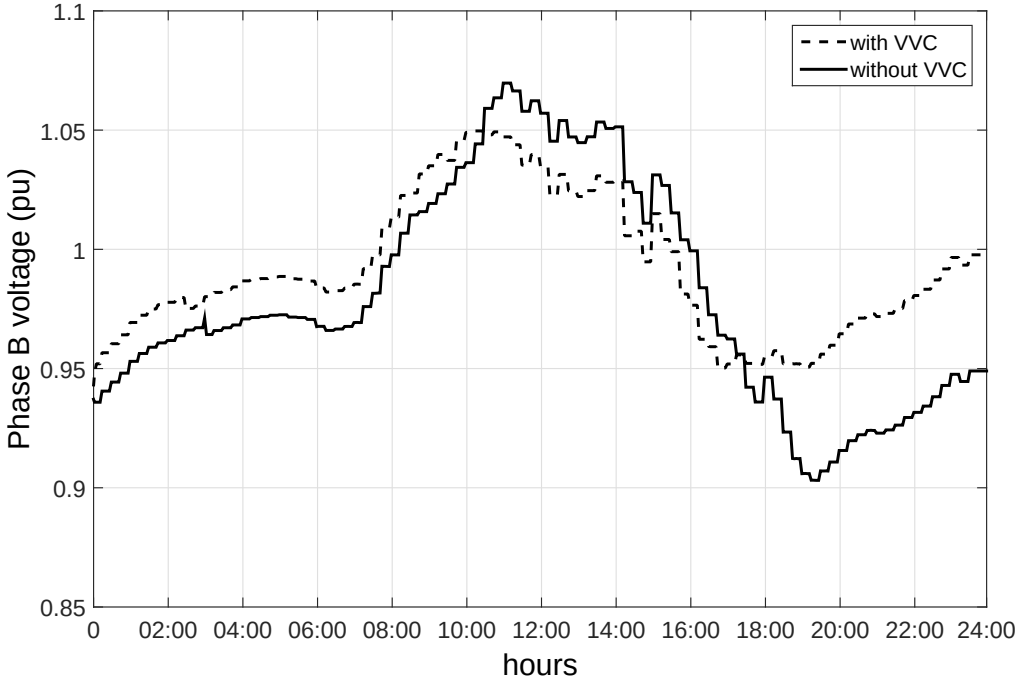


Figure 7 Node voltage of phase B at SST 890 – radial system

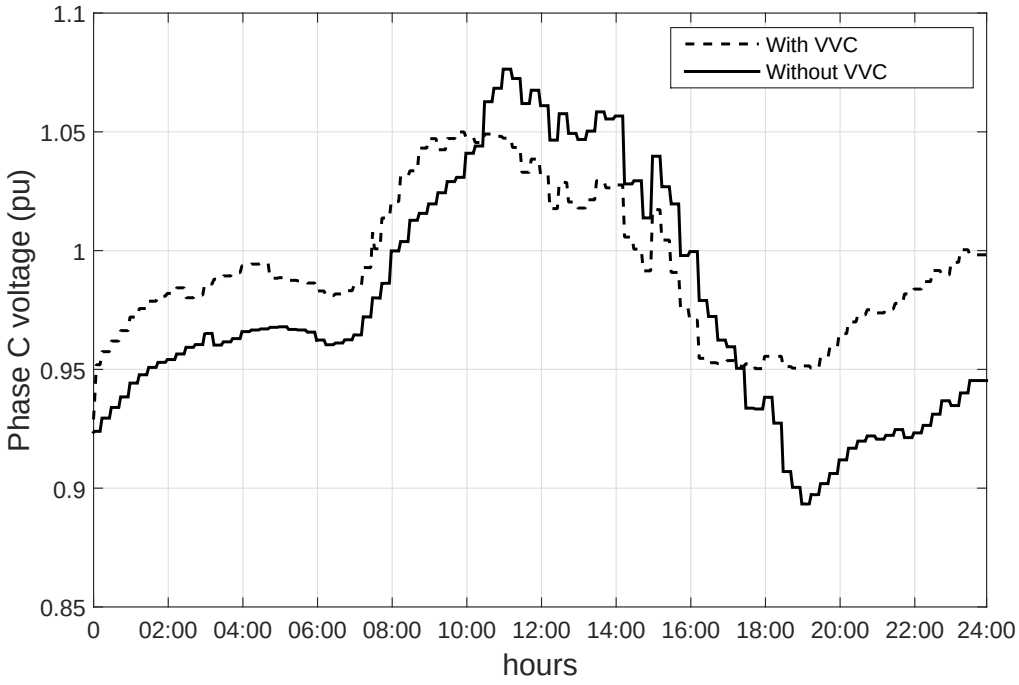


Figure 8 Node voltage of phase C at SST 890 – radial system

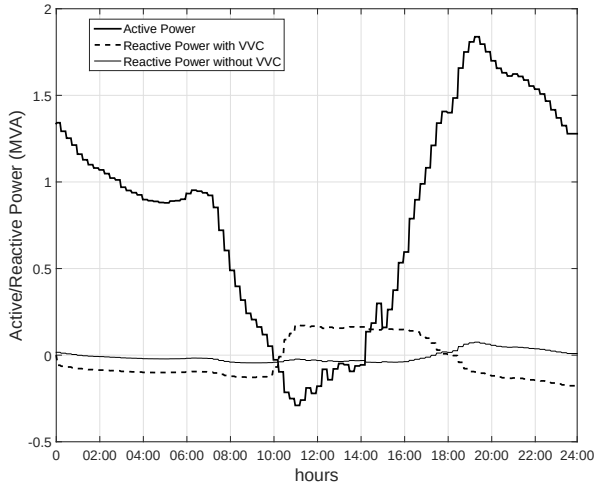


Figure 9 Substation P and Q with and without volt-var control

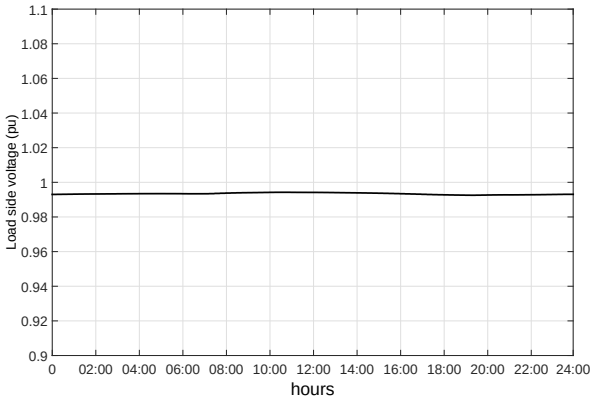


Figure 10 Load side voltage of SST 890

4. THE DQDV ALGORITHM IN A MESHED SYSTEM

To validate that the proposed algorithm also works in a meshed system, the IEEE 34 bus test system is modified to a meshed topology as shown in Figure 11. Each parallel connecting line is 6 miles long. The second feeder is a three phase balanced feeder and has four additional SST buses. The distance between any two buses is 9 miles. The line impedance per mile used for the second feeder is based on the line data of the IEEE 34 system. The peak load magnitude of these loads per phase are 75 kW and 38 kVAr. The pilot SSTs are the same as in the original system. The results of the proposed volt-var control for the meshed system is shown in Figure 12-14. As in the radial system, the proposed volt-var control is able to effectively maintain the bus voltages within the desired range.

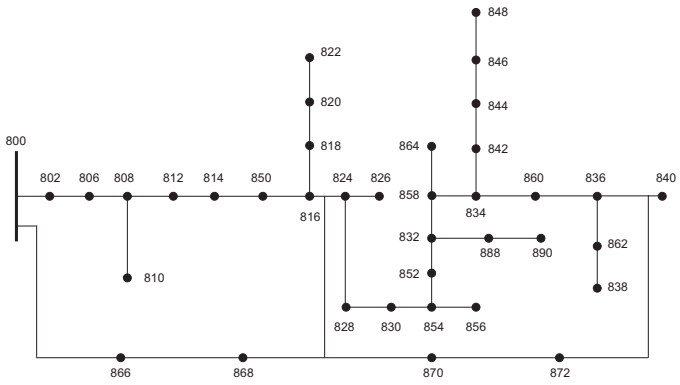


Figure 11 The meshed 34 bus distribution system

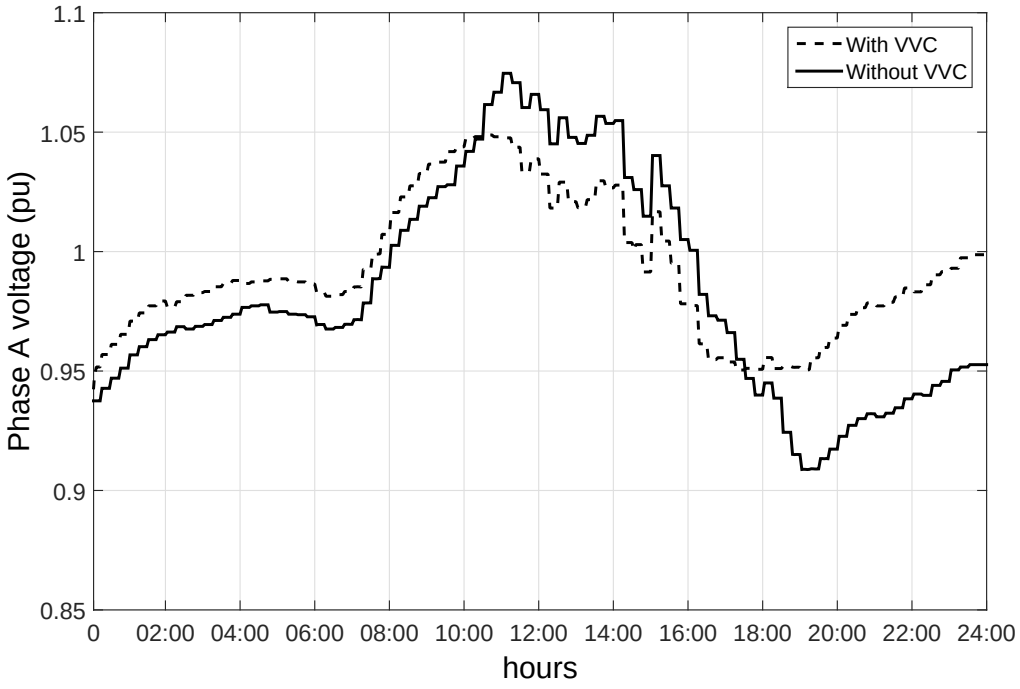


Figure 12 Node voltage of phase A at SST 890 – meshed system

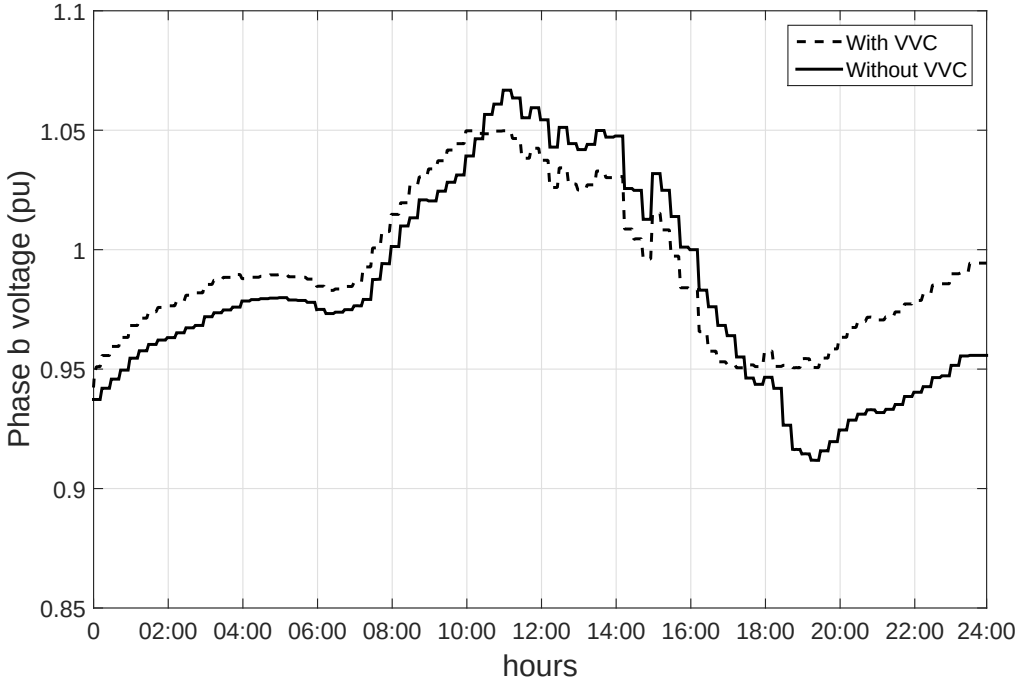


Figure 13 Node voltage of phase B at SST 890 – meshed system

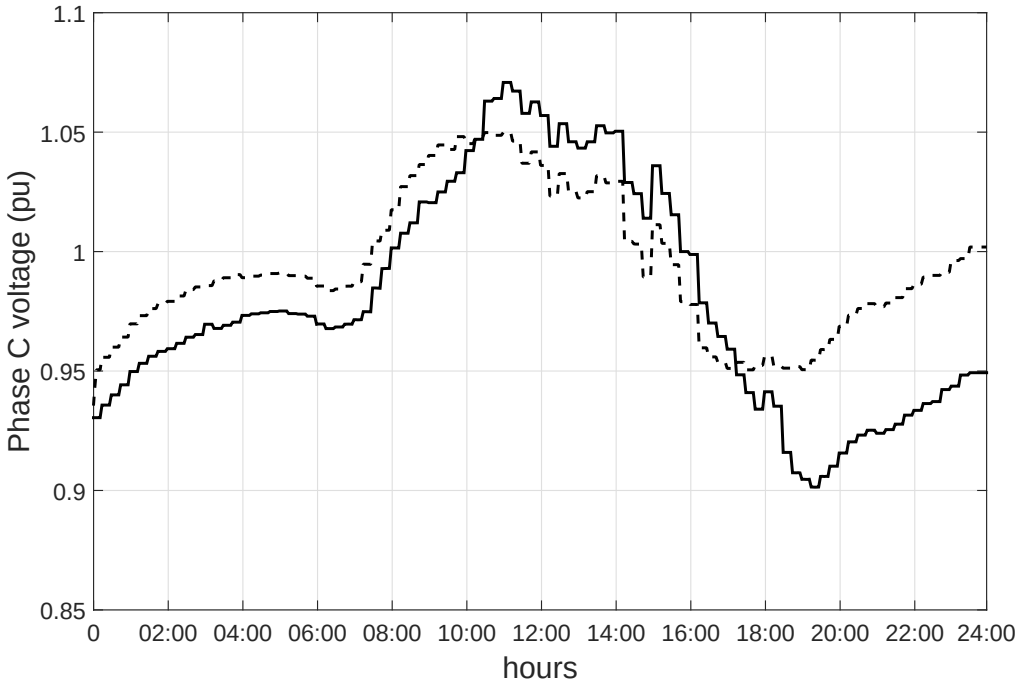


Figure 14 Node voltage of phase C at SST 890 – meshed system

5. SST CONTROL

The proposed volt-var control is a high-level control in that it determines the commanded reactive power. The SST is responsible for converting the commanded reactive power into the appropriate output voltage in a timely manner. Figure 1 shows a simplified representation of the actual topology of a single phase solid state transformer. The actual topology of an SST can be found in [13]. Throughout this paper, the SST was simulated in PSCAD using an average value model of the SST. The average value models were developed directly from the switching models and validated experimentally [13]. Each SST is rated at 20 kVA and 7.2 kV respectively [13]. Ten SSTs are aggregated to achieve a power rating of 200 kVA in order to supply power to large loads. The SST model consists of two regulated dc link voltages. The high voltage dc link is regulated at 11.4 kV by the active rectifier and the low voltage dc link is regulated at 400 V by the dual active bridge converter. The split phase inverter regulates the ac output voltage at the load side to 120/240 V.

A DQ vector controller with cross coupling terms, shown in Figure 15, is used for control of the active rectifier. Frequency (ω_e) and phase (θ_e) of the source voltage (V_{hs}) are calculated using a phase-locked-loop (PLL). The starred values shown in Figure 15 indicate the commanded values. For unity factor operation, the commanded value of I_q^* is set to zero. I_q^* is positive for reactive power injection into the distribution system and negative for reactive power absorption.

For voltage regulation, the commanded value of I_q^* is calculated and its magnitude depends on the amount of reactive power to be injected into, or absorbed from, the ac grid. Since the rating of SST is 200 kVA, Q is allowed to vary from from -200 kVAr to 200 kVAr. The gain α is selected such that 2 kVArs are injected every 0.1 seconds, but α can be adjusted to provide faster or slower response as needed. This update speed is well

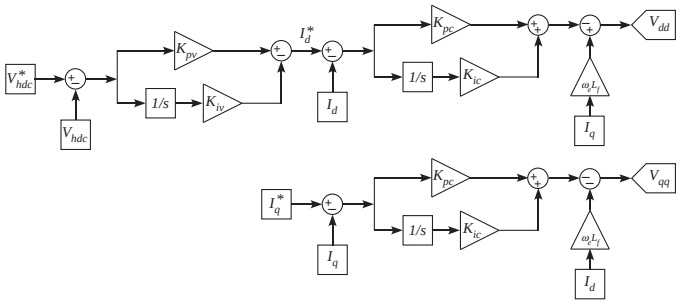


Figure 15 DQ vector controller

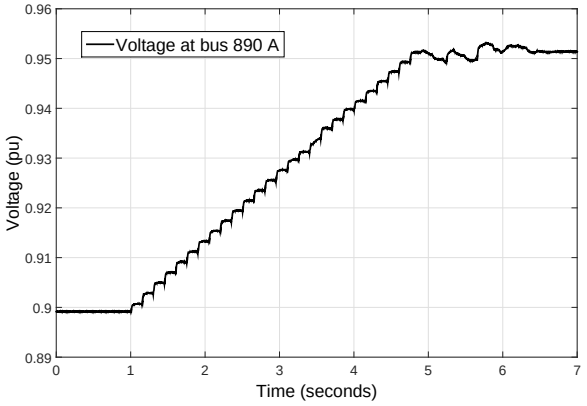


Figure 16 SST Voltage at 890

within the computational speed of the microprocessor allowing straightforward real-time implementation. An example of the SST response is shown in Figs. 16 and 17. The control is started at 1.0 second at which time the voltage is below the 0.95 minimum voltage level. Every 0.1 seconds, the reactive power injection is increased by 2 kVAr until the required voltage limit is reached, after which the voltage is maintained at a constant value. Figure 17 shows the response of the high voltage DC link of the active rectifier. Note that the voltage is stable at the desired DC voltage of 3800 V. The small oscillations in the DC link voltage are normal and can be mitigated by filters (which are not included in the average value model used in this study).

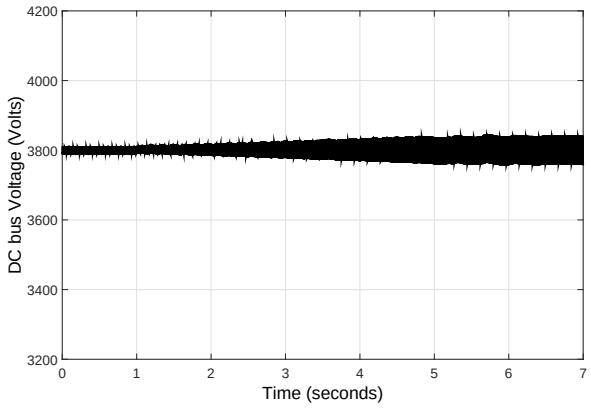


Figure 17 Active Rectifier DC link voltage

6. CONCLUSION

A local DQDV algorithm is proposed to perform voltage control in distribution systems with SSTs. Pilot buses for voltage control are identified in the distribution system and an SST is used to regulate bus voltage. Other power electronic devices such as PV array inverters can perform the same function. The main goal of the integrated algorithm and SST package is to enforce strict voltage constraints at the bus to which the SST is connected. Voltage regulation is maintained independent of the load and solar generation profile. Since the computations are performed locally, there is no required communication between the SSTs and the substation. The proposed algorithm is validated on both a radial and meshed distribution system. Furthermore, the results are verified via a time response appropriate model of the SST to validate that the SST is able to perform the commanded control.

BIBLIOGRAPHY

[1] E. R. Ronan, S. D. Sudhoff, S. F. Glover, and D. L. Galloway, "A power electronic-based distribution transformer," *IEEE Transactions on Power Delivery*, vol, 17, no. 2, pp 537–547, April 2002.

[2] X. She, A. Q. Huang, and R. Burgos, "Review of the solid state transformer technologies and its application in power distribution system," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, early access, 2013.

[3] H. Qin and J. W. Kimball, "Solid-state transformer architecture using ac-ac dual-active-bridge converter," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 9, pp. 3720-3730, 2013.

[4] X. She, A. Q. Huang, S. Kukic, and M. E. Baran, "On integration of solid-state transformer with zonal dc microgrid," *IEEE Transactions on Smart Grid*, vol. 3, no. 2, pp. 975–985, 2012.

[5] N. Bottrell, M. Prodanovic, and T. C. Green, "Dynamic stability of a microgrid with an active load," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 5107–5119, November 2013.

[6] Z. Shen, M. E. Baran, "Gradient based centralized optimal Volt/Var control strategy for smart distribution system," *Innovative Smart Grid Technologies (ISGT), 2013 IEEE PES* vol., no., pp.1-6, February 2013.

[7] K. Christakou, J. LeBoudec, M. Paolone, D.-C. Tomozei, "Efficient Computation of Sensitivity Coefficients of Node Voltages and Line Currents in Unbalanced Radial Electrical Distribution Networks," *IEEE Trans on Smart Grid*, vol. 4, no. 2, pp. 741-750, June 2013.

[8] V. Kumar, I. Gupta, H. O. Gupta, C. P. Agarwal, "Voltage and current sensitivities of radial distribution network: a new approach," *IEE Proceedings Generation, Transmission and Distribution*, vol. 152, no. 6, pp. 813-818, Nov. 2005.

[9] A. Sundhararajan, A. Pahwa, "Optimal selection of capacitors for radial distribution systems using a genetic algorithm," *IEEE Trans on Power Systems*, vol. 9, no. 3, pp. 1499-1507, Aug. 1994.

[10] K. Prakash, M. Sydulu, "Particle Swarm Optimization Based Capacitor Placement on Radial Distribution Systems," *Proceedings of the 2007 Power Engineering Society General Meeting*, June 2007.

[11] T. Aziz, T. K. Saha, N. Mithulananthan, "Identification of the weakest bus in a distribution system with load uncertainties using reactive power margin," *Proceedings of the 2010 Universities Power Engineering Conference (AUPEC)*, Dec. 2010.

[12] IEEE PES Distribution System Analysis Subcommittee's Distribution Test Feeder Working Group, "Distribution Test Feeders," [Online] `http://ewh.ieee.org/soc/pes/dsacom/testfeeders/`

[13] T. Zhao, J. Zeng, S. Bhattacharya, M. Baran, A. Q. Huang, "An Average model of solid state transformer for dynamic system simulation," *Proc IEEE Power & Energy Society Meeting*, Calgary, AB, July 2009.

SECTION

2. CONCLUSION

In Paper I, we demonstrated an instability caused by deploying SSTs in the distribution systems. Harmonic resonance is caused by an impedance mismatch of the distribution system with the SSTs. We have proposed a design criterion for the SST input filter to avoid harmonic resonance and mitigate the instabilities in the system under no load conditions. A stability analysis was performed for each phase in the distribution system individually.

In Paper II, we extended the application of the impedance based stability criterion to the distribution system with SSTs under loaded conditions. For a given filter size, this criterion provides a stability guarantee for the system. If the SST filters are designed according to stability criterion, then system stability is guaranteed regardless of configuration. This leads to two important implications: (1) the order of connection of the SSTs will not generate any instability if the criterion is satisfied, and (2) a system configuration change will not generate instability. This stability assessment can be applied to each of the three phases independently.

In Paper III, a local DQDV algorithm is proposed to perform voltage control in the distribution system. Pilot buses for voltage control are identified in the distribution system and an SST is used to regulate the bus voltage. SSTs at non-pilot buses maintain unity power factor. The main goal of the algorithm is to enforce strict voltage constraints during high solar power generation and peak load conditions. Since the computations are performed locally, there is no need for communication between the SSTs and the substation. The proposed algorithm is validated for both radial and meshed distribution system.

VITA

Darshit Shah got B.Tech in Electrical Engineering from Nirma University, Ahmedabad, India in May 2007. He received MS in Electrical Engineering from Georgia Institute of Technology, Atlanta, Georgia in May 2009. He received PhD in Electrical Engineering from Missouri University of Science and Technology, Rolla, Missouri in August 2015. His research interests include solid state transformers, smart grid and power system stability.