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# Advanced control techniques for doubly fed induction generator-based wind turbine converters to improve low voltage ride-through during system imbalances

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# ADVANCED CONTROL TECHNIQUES FOR DOUBLY FED INDUCTION GENERATOR - BASED WIND TURBINE CONVERTERS TO IMPROVE LOW VOLTAGE RIDE-THROUGH DURING SYSTEM IMBALANCES

by

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## ABSTRACT

A doubly-fed induction generator (DFIG) applied to wind power generation is under study for low voltage ride-through application during system disturbances. Conventional dq axis current control using voltage source converters for both the grid side and the rotor side of the DFIG are analyzed and simulated. DFIG operation is investigated under balanced and unbalanced system disturbances. A conventional d-axis and q-axis control applied to a voltage source converter (VSC) during a system imbalance exhibits oscillations in the stiff DC link voltage as well as in the real and reactive powers of the converter. Multiple advanced control methods are explored and compared for imbalance operations. An advanced control technique utilizing both positive and negative sequence domain is evaluated. The approach demonstrates the stabilization of the DC link voltage to a greater extent during a disturbance but is more sluggish than the conventional control. An innovative control strategy that employs the technique of direct power control (DPC) is also investigated. This control achieves real and reactive power stability with simple active and reactive power control variables replacing the current control loops in the conventional case. A modified DPC algorithm is proposed to eliminate the current harmonics created by DPC during system disturbances. The DPC is further extended to the rotor-side converter of the DFIG thus controlling the complete system using this technique. The DPC is implemented using a three-phase converter designed on a PCB using Eagle®. A Texas Instruments® TMS320F2812 DSP is used to implement the control algorithm. The converter is tested for ride through capability using an industrial power corruptor. The results are compared to the simulation results for compliance with standard grid codes.

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# NOMENCLATURE

| Symbol | Description |
|---|---|
| $I_{or}$ | Rotor side current |
| $I_{os}$ | Stator side current |
| E | DC link voltage |
| R | Series line resistance |
| L | Series line inductance |
| $v_a$ | A phase line to neutral voltage |
| $v_b$ | B phase line to neutral voltage |
| $v_c$ | C phase line to neutral voltage |
| $I_a$ | A phase line current |
| $I_b$ | B phase line current |
| $I_c$ | C phase line current |
| $v_{al}$ | A phase line to neutral converter voltage |
| $v_{bl}$ | B phase line to neutral converter voltage |
| $v_{cl}$ | C phase line to neutral converter voltage |
| n | Neutral point |
| $v_d$ | d-axis voltage |
| $v_q$ | q-axis voltage |
| $i_d$ | d-axis current |
| $i_q$ | q-axis current |
| $\omega_e$ | Electrical synchronous speed |
| $\omega_r$ | Electrical rotor speed |

| | |
|---|---|
| $\omega_{slip}$ | Electrical slip speed |
| $\theta_e$ | Angular position of the voltage |
| $v_\alpha$ | Stationary reference frame alpha voltage |
| $v_\beta$ | Stationary reference frame beta voltage |
| $\lambda_s$ | Stator flux linkages |
| $\lambda_{ds}$ | Stator d-axis flux linkages |
| $L_o$ | Mutual inductance per phase |
| $L_s$ | Stator leakage inductance per phase |
| $L_r$ | Rotor leakage inductance per phase |
| $L_m$ | Magnetizing inductance per phase |
| $i_{ms}$ | Stator magnetizing current |
| $i_{ds}$ | Stator d-axis current |
| $i_{dr}$ | Rotor d-axis current |
| $i_{qs}$ | Stator q-axis current |
| $i_{qr}$ | Rotor q-axis current |
| $v_{dr}$ | Rotor d-axis voltage |
| $v_{qr}$ | Rotor q-axis voltage |
| $\sigma$ | Leakage coefficient of induction machine |
| $R_s$ | Stator resistance |
| $R_r$ | Rotor resistance |
| $T_e$ | Air gap or electromechanical torque |
| $\lambda_{\alpha s}$ | Flux linkage of alpha phase in stationary reference frame |
| $\lambda_{\beta s}$ | Flux linkage of beta phase in stationary reference frame |

| | |
|---|---|
| $v_{\alpha s}$ | Stator alpha voltage in stationary reference frame |
| $v_{\beta s}$ | Stator beta voltage in stationary reference frame |
| $i_{\alpha s}$ | Stator alpha phase current |
| $i_{\beta s}$ | Stator beta phase current |
| $X_a$ | A phase components (voltage/current) |
| $X_b$ | B phase components (voltage/current) |
| $X_c$ | C phase components (voltage/current) |
| $x_{mp}$ | Positive sequence components (voltage/current) |
| $x_{mn}$ | Negative sequence component (voltage/current) |
| $x_{mo}$ | Zero sequence component (Voltage/current) |
| $\alpha_p$ | Positive sequence angle |
| $\alpha_n$ | Negative sequence angle |
| $\alpha_0$ | Zero sequence angle |
| $X_{de}$ | d-axis component synchronous reference frame |
| $X_{qe}$ | q-axis component synchronous reference frame |
| $X_{dpe}$ | Positive sequence d-axis component synchronous reference frame |
| $X_{qpe}$ | Positive sequence q-axis component synchronous reference frame |
| $X_{dne}$ | Negative sequence d-axis component synchronous reference frame |
| $X_{qne}$ | Negative sequence q-axis component synchronous reference frame |
| $T_{32}$ | A, B and C phase to dq transformation |
| $X_{abc}$ | A, B and C phase components |
| $X_{qdpe}$ | q-axis sequence components in positive synchronous reference frame |
| $X_{qdne}$ | d-axis sequence components in negative synchronous reference frame |

| | |
|---|---|
| $R(\omega t)$ | Reference frame transformation |
| $v_{dpe}$ | Positive sequence d-axis synchronous reference frame voltage |
| $v_{qpe}$ | Positive sequence q-axis synchronous reference frame voltage |
| $v_{dne}$ | Negative sequence d-axis synchronous reference frame voltage |
| $v_{qne}$ | Negative sequence q-axis synchronous reference frame voltage |
| $i_{dpe}$ | Positive sequence d-axis synchronous reference frame current |
| $i_{qpe}$ | Positive sequence q-axis synchronous reference frame current |
| $i_{dne}$ | Negative sequence d-axis synchronous reference frame current |
| $i_{qne}$ | Negative sequence q-axis synchronous reference frame current |
| $P$ | Real power |
| $P_0$ | Average real power |
| $P_{c2}$ | Real power cosine term coefficient |
| $P_{s2}$ | Real power sine term coefficient |
| $Q$ | Reactive power |
| $Q_0$ | Average reactive power |
| $Q_{c2}$ | Reactive power cosine coefficient |
| $Q_{s2}$ | Reactive power sine coefficient |
| $v_{a1b1c1}$ | Converter A, B and C phase to neutral voltage |
| $i_{abc}$ | A, B and C phase source currents |
| $v_{abc}$ | A, B and C phase to neutral voltages |
| $U_0$ to $U_7$ | space vectors |
| $V$ | source phase voltage |
| $v_1$ | converter phase voltage |
| $X_L$ | Line inductance |

| | |
|---|---|
| $\delta$ | Angle between source voltage and converter voltage |
| $P_{imb}$ | Real power due to system imbalance |
| $Q_{imb}$ | Reactive power due to system imbalance |
| $d_p$ | digitalized real power output |
| $d_q$ | digitalized reactive power output |
| $p_{ref}$ | Real power reference |
| $q_{ref}$ | Reactive power reference |
| Theta, θ | vector position |

# 1. INTRODUCTION

## 1.1 INTRODUCTION

Wind energy has gained popularity in recent years all over the world, mainly because wind energy is renewable and eco-friendly. There are, however, many challenges associated with harnessing this type of energy for grid application mostly due to its intermittent nature. This dissertation addresses some of the problems associated with the grid integration aspect of wind energy.

Generally, wind power generation uses either fixed speed or variable speed turbines which are classified in to four major types by the Western Electricity Coordinating Council (WECC) to develop industry-standard wind turbine models [1]. These types are briefly described below:

1. Pitch regulated squirrel cage induction generator directly coupled to the grid.
2. Variable slip squirrel cage induction generator directly coupled to the grid.
3. Wound rotor induction generator with an AC/DC/AC power converter connected between the rotor terminals and grid and is pitch regulated.
4. Synchronous or asynchronous machine connected to the grid using full rated AC/DC/AC power converter and is pitch regulated.

Type I and II use the simplest topology where the turbine is directly connected to the grid. This type of machine needs a switch to prevent motoring operation during low wind speeds and also suffers a major drawback of reactive power consumption as there is no reactive power control. Type II uses an electronically modulated rotor resistance to effect dynamic changes in the machine torque speed characteristics. Type III is the most common for high power grid applications. This topology allows the complete control of reactive power using rotor and grid side converters and around 25% of the

speed control using rotor side converter. The converters used for this topology need to be rated at only 25% to 30% of overall machine rating as they are used on the rotor side to supply the slip power which is 25% to 30% of the overall machine power. Type IV topology uses a full rated converter with either a synchronous or an asynchronous machine. This type of topology has full control of the reactive power and speed.

The major advantages associated with Type III wind turbines is that it has four quadrant active and reactive power flow capabilities, with constant frequency power output and low power converter ratings making it the most widely used topology. Hence this dissertation focuses attention on the integration of Doubly Fed Induction Generator (DFIG) – Type III based wind turbines to the power grid.

The major issues concerning integration of DFIG wind turbines are that the best wind regimes are located in rural areas and the power grid in these areas is often weak and prone to voltage sags, faults and unbalances. Unbalanced grid voltages can cause many problems for DFIG wind turbines such as torque pulsations, unbalanced currents, and reactive power pulsations. These problems may be attributed to the instability in the power converter's DC link voltage during system disturbances. This issue with the DC link voltage is mainly due to the distorted control in the back to back PWM converters during system unbalance. A review of the pertinent literature reveals several papers addressing the effect of unbalance associated with the DFIG and rotor side converter. This is discussed later in the literature review. The effect of unbalance on the grid side converter is studied in detail in this dissertation and possible remedies for voltage ride through during disturbances are addressed.

## 1.2 DISSERTATION OUTLINE

The later part of this section deals with major codes followed by US and European grid networks during grid disturbances. A brief literature review of the existing remedies associated with the PWM converters that can be possibly adapted for DFIG based wind turbine generators is also presented in this section.

The detailed operation of DFIG control using the conventional current control techniques are discussed in section two using a mathematical model in Matlab Simulink® and also with a more detailed model in DIgSILENT®. The effect of grid imbalances are also analyzed using these models.

The effect of unbalance on the grid side converter is analyzed in detail in section three. An advanced control technique using sequence controllers to stabilize the operation of the grid-side converter during grid imbalance is also presented in detail in this section.

A novel control technique using direct active and reactive power control called Direct Power Control (DPC) is discussed in section four. This controller eliminates the conventional current loops and uses delta modulation comparators, hence has faster response. The switching of the converter is done using a simple optimum switching table. A Grid-side controller is simulated and the results are compared with the conventional and sequence controllers. A complete DFIG including the rotor side and grid-side converters is simulated using DPC and is tested for ride through during system and grid disturbances.

Section five discusses the hardware implementation of a grid side converter using DPC. A 2kW converter is designed using Eagle® for PCB design. The control is coded in C and implemented in TMS320F2812 DSP. The converter using DPC is tested

for system unbalance conditions created by an Industrial Power Corruptor (IPC) [2] in the laboratory. The laboratory results are compared with the simulation results for accuracy errors and verification.

The concluding remarks and summary of the work along with some future developments are discussed in section six. The Appendix presents the system parameters, circuit diagrams and the C code used for hardware implementation.

## 1.3 GRID CODES

Grid codes determine the requirement of the wind power systems to stay connected to the grid during grid disturbances. The codes are typically described on a time voltage diagram as in Figure 1.1, Figure 1.2 and Figure 1.3. These diagrams contain safe limits or the border of operation of wind power plants. The system should remain connected during the fault inception and post fault recovery time according to the border limits and the times mentioned in the grid code diagrams.

According to the Low Voltage Ride Through (LVRT) requirement for wind generation facilities per Federal Energy Regulatory Commission (FERC) order No. 661 [3] the grid code standard requires that the machine stay connected for emergency low voltages at the terminals for as low as 15% of nominal per unit voltage for approximately 0.6 seconds. This time increases as the terminal voltage requirement increases. For example during the post-fault recovery, the wind power system should be able to withstand a low voltage of 60% at the terminal for a time period of two seconds as shown in Figure 1.1. In practice, the high voltage drop during grid disturbance gives rise to rotor protection which acts to short circuit the dc link capacitor (via a crowbar) in order to protect the converter and the associated components from high currents [4].

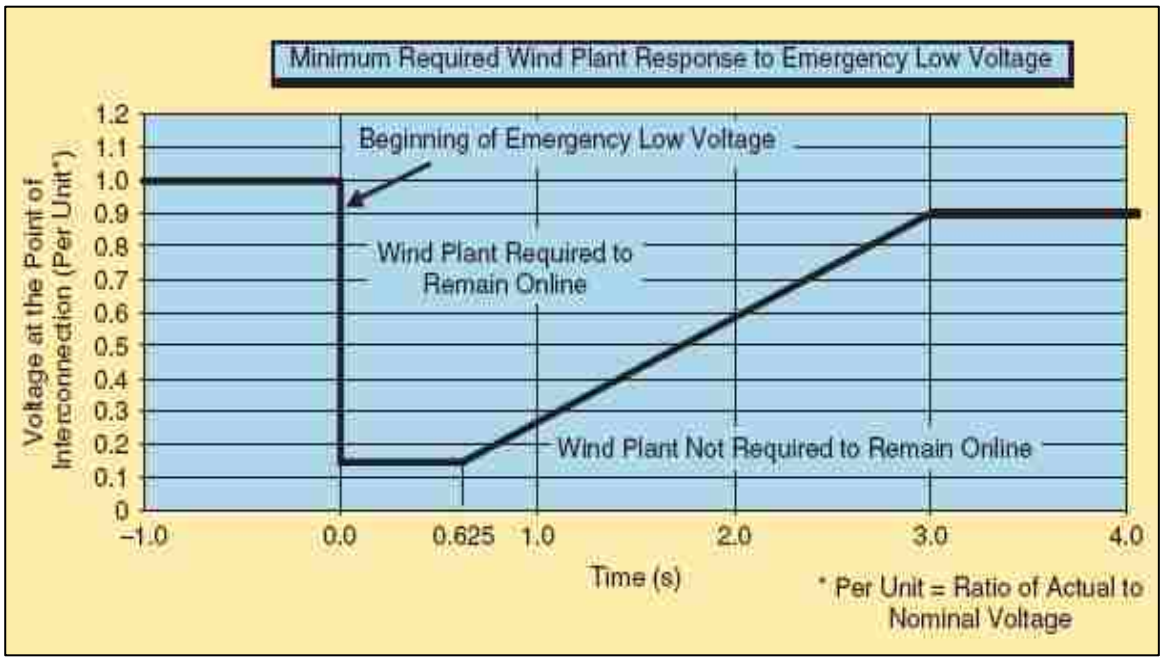


Figure 1.1. LVRT requirements for emergency low voltage per FERC order No. 661 [3]

The North American Electrical Reliability Corporation (NERC) and American Wind Energy Association on behalf of FERC had discussions to resolve the issues with FERC order 661 [5]. According to these discussion, *"the new language stated that wind generating plants are required to remain in service during three phase faults with normal clearing (which is a time period of approximately four to nine cycles) and single line to ground faults with delayed clearing, and subsequent postfault voltage recovery to prefault voltage unless clearing the fault effectively disconnects the generator from the system"* [5]. According to this new practice the old voltage versus time curve is no longer applied and the code is to go with post-fault clearing time as show in Figure 1.2.

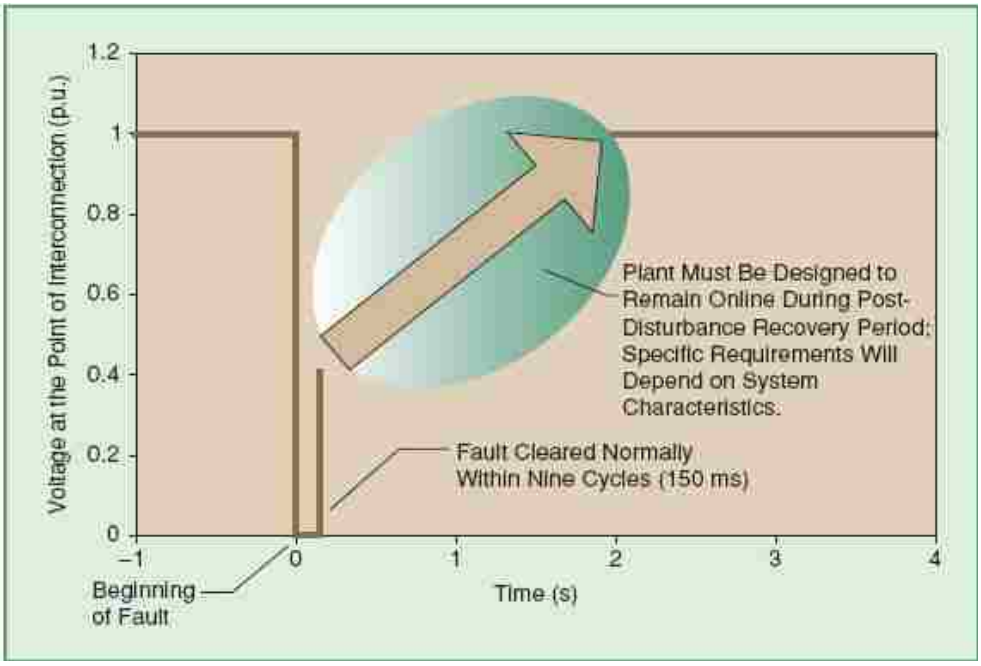


Figure 1.2. LVRT requirements at the point of intersection FERC Order 661 A [5]

Fault Ride Through (FRT) requirements of Germany are based on the time voltage diagram shown in Figure 1.3 [6]. These requirements state that the wind turbine has to connect to the grid within areas 1 and 2. Possible Short Term Interruption (STI) of less than 2 seconds can occur within area two due to over load or stability concerns or other kinds of technical problems. Short disconnection of the turbine is allowed in area 3 whereas resynchronization of the turbine is necessary after two seconds. Step wise tripping of the wind turbine is allowed in area 4.

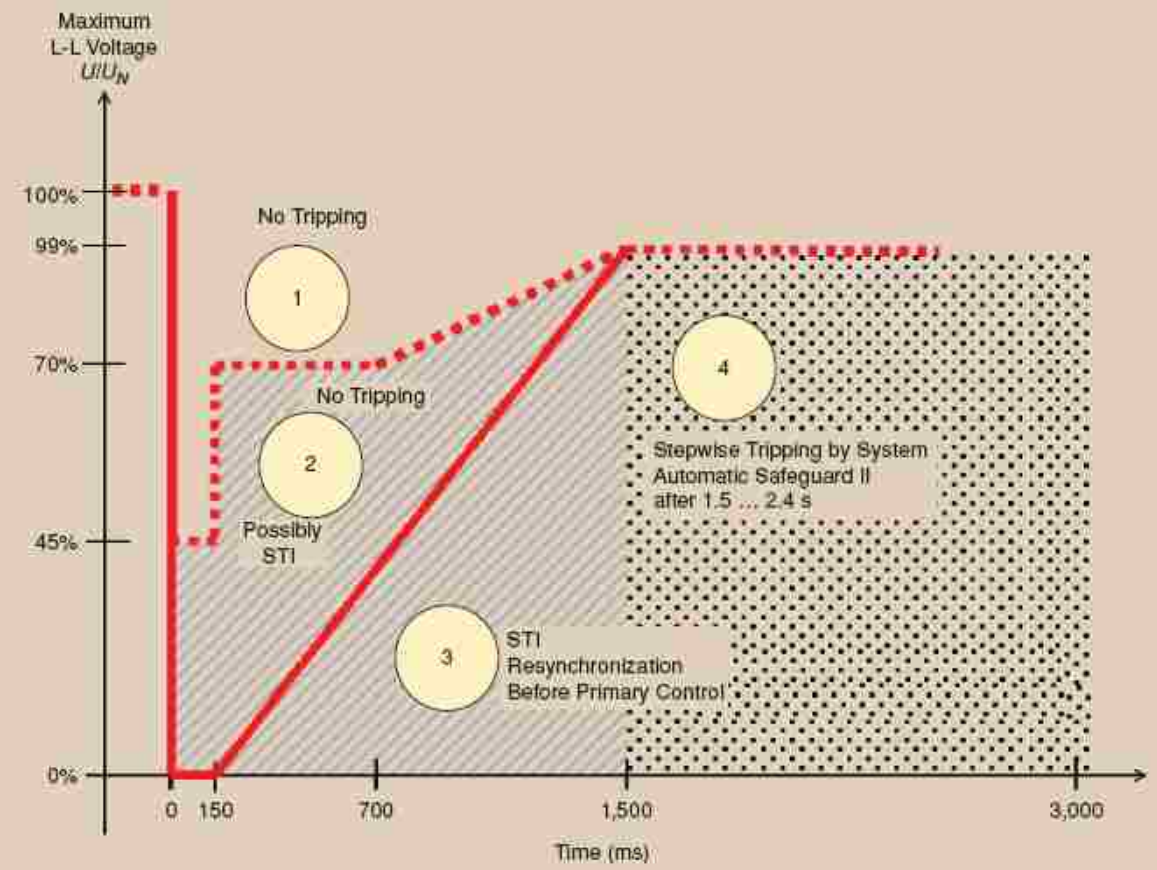


Figure 1.3. Definition of Fault ride through (FRT) requirement in Germany [6]

Looking at different grid codes, it can be concluded that DFIG controllers should be capable of overcoming temporary voltage disturbances. Hence, this work deals with the design of controllers that would keep the wind turbine in stable operation during a fault causing a low voltage of up to 40% for two seconds. This type of fault is of importance because the rotor need not be protected by crowbar during this time and the back-to-back PWM converters work normally even with the unbalance. The proposed controllers are tested for different fault conditions for ride through on the grid side as well as the turbine side.

## 1.4 LITERATURE REVIEW

Advanced control techniques for power converter control are reviewed in this literature review. Some of the controllers are adopted for implementation with DFIG to counter system imbalances. The control techniques are broadly divided into three major methods based on their operation. The first type is based on decomposing the system voltage and currents into symmetrical components and using different controllers in positive and negative sequence components [7] through [13].

Enjeti and Choudhury [7] propose a technique which counter balances the gating signals so that the imbalance in the supply is rectified. The technique is a feed-forward approach where the sequence components of the unbalanced input supply are calculated and are used to counter-unbalance the PWM gating signals of the converter switches to cancel the generated abnormal harmonics. This method is suitable for high power GTO-type PWM ac to dc converters.

Rioual et al. [8] propose a cascade regulation of PWM rectifier in the Park's d-q frame. The system is distributed with unbalanced voltage; the regulation is calculated with a positive sequence network voltage as well as a negative sequence network voltage separately. This control achieves desired positive and negative sequence current commands for a constant dc link voltage and average reactive power.

Kim et al. [9] propose a PWM converter where decomposition into symmetrical components of input voltage is needed. The negative sequence current component is commanded to be zero. It is observed that negative sequence is transformed into the second harmonic component on the synchronous reference frame and the positive sequence can be detected using a band pass filter with center frequency of 120 Hz.

Seok and Nam [10] propose a dual converter scheme where two reference frames are used for measuring the positive sequence in the positive synchronous reference frame (SRF) by eliminating the negative sequence with the 120 Hz and negative sequence in negative SRF. Separately measured currents are used for two feedback PI controllers called as the dual current controller. One regulates the positive sequence current and the other regulates the negative sequence current thus allowing the control of the negative sequence in its own frame.

Giuseppe et al. [11] propose two different controllers to deal with unbalanced conditions. The first controller is implemented in the positive synchronous reference frame. Active and reactive currents are controlled independently of each other with a high bandwidth. The second controller uses a feed forward approach for sequence separation. The DC link voltage controller used in this case is the same as that for the first controller. A third controller similar to the one proposed in [10] is considered; however the transient performance of the controller is not analyzed in [10].

Lie Xu et al. [12] proposed the use of a main controller using decoupled control without positive and negative sequence decomposition and an auxiliary controller in negative sequence with inclusion of cross coupling for negative sequence components. Lie Xu [13] Proposed complete modeling of the DFIG in positive and negative sequence to deal with network disturbances.

The second method proposed by Slavomir et al. [14-15] discusses a finite element modeling (FEM) of the magnetic field in the generator in two dimensions. This model takes into account magnetic saturation of the stator and the rotor leakage inductances. The large difference from the conventional model is that, during an

unsymmetrical fault, the FEM model represents unsymmetrical magnetic saturation better than the conventional analytical models.

The third method is based on a novel control technique that directly controls the active and reactive power of the systems. This method more suits the controllers used to connect the utility as this directly achieves the unity power factor requirement of the utility. References [16] to [18] discuss the concept as applied to the grid side and rotor side converters of the DFIG. In references [19] and [20], the authors modify the control and the switching table to accommodate for system disturbance and include the power due to imbalance.

Noguchi et al. [16] propose direct power of a three-phase Pulse Width Modulated (PWM) converter without line voltage sensors. In this control the real and reactive powers are calculated as the sum of power consumed by the inductance and the converter. The voltage angle is calculated from the powers and the currents.

Mariusz et al. [17] propose direct power control of three-phase pulse width-modulated rectifiers without line voltage sensors. The control is based on assuming the three phase grid as a virtual induction machine and the flux in the virtual machine is defined as virtual flux (VF). It is shown that the VF-DPC exhibits several advantages, particularly providing sinusoidal line current when the supply voltage is not ideal.

Rajib Datta et al. [18] proposed a method of direct decoupled control of active and reactive powers. The algorithm extends the switching logic of Direct Torque Control (DTC) to the rotor side of a doubly-fed wound rotor induction machine. The direct power control algorithm uses only stator quantities for active and reactive power measurements and is inherently position-sensorless. It is computationally simple and

does not incorporate any machine parameter. The algorithm can start on the fly and operate stably at synchronous speed.

Geardo Escobar et al. [19] proposed a direct power control where the controller builds upon the ideas of the well-known direct torque control technique for induction motors. The active and reactive powers replace the torque and flux amplitude using the controlled outputs in DPC. A simple modification of the original algorithm utilizing the concept of output regulation subspaces was formalized. A modification was added to the basic controller to deal with disturbances such as unbalance and distortion in the source voltage.

Santos-Martin et al. [20] presented a novel control strategy for a DFIG machine based on direct power control (DPC+) that includes power due imbalance. This method enables DFIG to work under perturbed conditions and achieve optimum results.

## 1.5 SUMMARY

Sequence controllers and direct power controller techniques would be suitable solutions to address the issue of voltage unbalances for low voltage or fault ride through situations. Sequence controllers are adopted for system stability during disturbances and they are further analyzed in the next two sections. The DPC for wind turbines have been mostly applied to the rotor side converter and the DFIG machine. Hence a similar idea is investigated in this dissertation for grid side converter during disturbances.

# 2. CONVENTIONAL DFIG CONTROL AND OPERATION DURING GRID DISTURBANCES

## 2.1 INTRODUCTION

The general operation of a DFIG is discussed in brief by S Muller et al. [21] and a detailed analysis of the control system is discussed by R Pena et al. [22], Vladislav et al. [23] and Nicholas et al. [24]. The DFIG model is shown in Figure. 2.1.

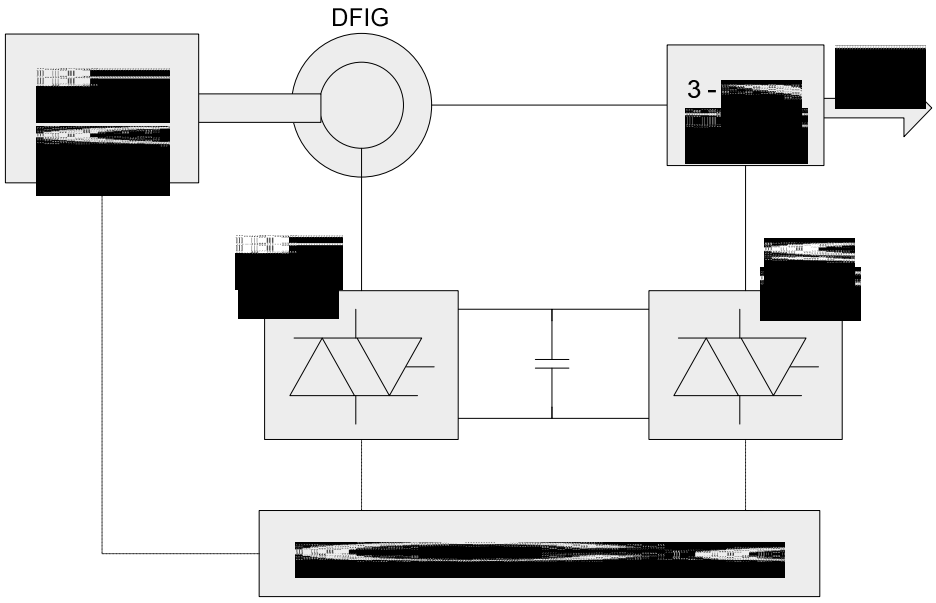


Figure 2.1. DFIG model

The prime mover utilizes a pitch angle controlled wind turbine where the shaft and gear box drive a doubly-fed induction machine. The stator of the machine is connected to the grid. The rotor of the induction machine is fed by self-commutated pulse width modulated converters which control the rotor voltage and angle, thus allowing active and reactive power control.

The voltage or the reactive power at the grid terminals, which is dependent on stator flux, is controlled by the reactive power generated or absorbed by the rotor side converter. Hence the current controller operates in a stator-flux oriented reference frame. In this reference frame, the q-axis component of the rotor current directly influences the torque and, hence, is used for active power control. The d-axis component of the rotor current directly influences the reactive power and hence can be used for reactive power control.

The active power dispatch of the wind turbine is by a look-up from power versus mechanical speed graphs or maximum power tracking (MPT) characteristics [22]. Alternatively, the induction machine operates using a reverse control scheme where the mechanical speed is calculated by inverse MPT characteristics.

The grid side controller uses a global reference frame which rotates at reference speed. The direct axis reference of this converter is set by the commanded DC voltage. The model allows using a grid converter to generate or absorb reactive power using a quadrature axis reference. Generally, this reference is kept constant.

## 2.2 CONVENTIONAL DECOUPLED CONTROL

Controllers used for three-phase PWM converters are generally designed on the assumption that the input voltage is balanced. They are implemented in the synchronous reference frame (SRF) as it eliminates steady state error and the control is decoupled. These controllers do not behave as expected when the input is unbalanced like in the case of voltage sags, Single Line to Ground (SLG) faults, Double Line to Ground (DLG) faults, etc.

A conventional control scheme based on [22] is implemented first in Matlab Simulink® and tested for different unbalanced conditions. The objective of this converter is to regulate the DC link voltage to a constant value irrespective of the disturbances due to the rotor-side converter. A standard design technique used by Pena [22] is used to regulate the DC-link voltage and reactive power. Predictably, the converter does not function well during the imbalance in the system. The PWM converter under analysis for the above schemes is shown in Figure 2.2.

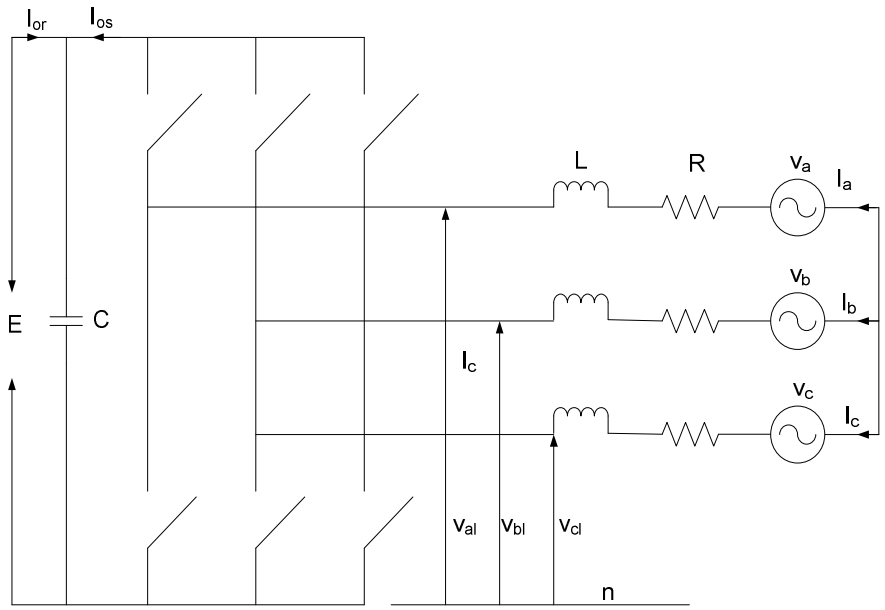


Figure 2.2. PWM converter

In this converter, a stator voltage vector-oriented reference frame is used. This allows the PWM converter to be current regulated; with the direct axis current regulating the DC-link voltage and the quadrature axis current regulating the reactive power. The voltage balance across the inductor is:

$$\begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} = R \cdot \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} + L \cdot \frac{d}{dt} \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} + \begin{pmatrix} v_{a1} \\ v_{b1} \\ v_{c1} \end{pmatrix} \tag{1}$$

L and R are the line parameters. Using the dq transformation rotating at synchronous speed, d-axis and q-axis voltage are:

$$v_d = R \cdot i_d + L \cdot \frac{d}{dt} i_d - \omega_e \cdot L \cdot i_q + v_{d1} \tag{2}$$

$$v_q = R \cdot i_q + L \cdot \frac{d}{dt} i_q + \omega_e \cdot L \cdot i_d + v_{q1} \tag{3}$$

The angular position of the voltage is calculated by (4).

$$\theta_e = \int \omega_e \, dt = atan\left(\frac{v_\beta}{v_\alpha}\right) \tag{4}$$

$V_\alpha$ and $V_\beta$ are the $\alpha, \beta$ (stationary 2-axis) stator voltage components. Aligning the d-axis along the stator-voltage vector position given by (3) gives $V_q = 0$ and a constant $V_d$. The active and reactive powers are proportional to the d-axis and q-axis current, respectively. Two current loops with PI controllers are independently implemented in these reference frames. The control strategy implemented in Matlab Simulink® using PLECS® tool box is shown in Figure 2.3 and the circuit is shown in Figure 2.4. The parameters used in the circuit are tabulated in Table A.1 of Appendix A.

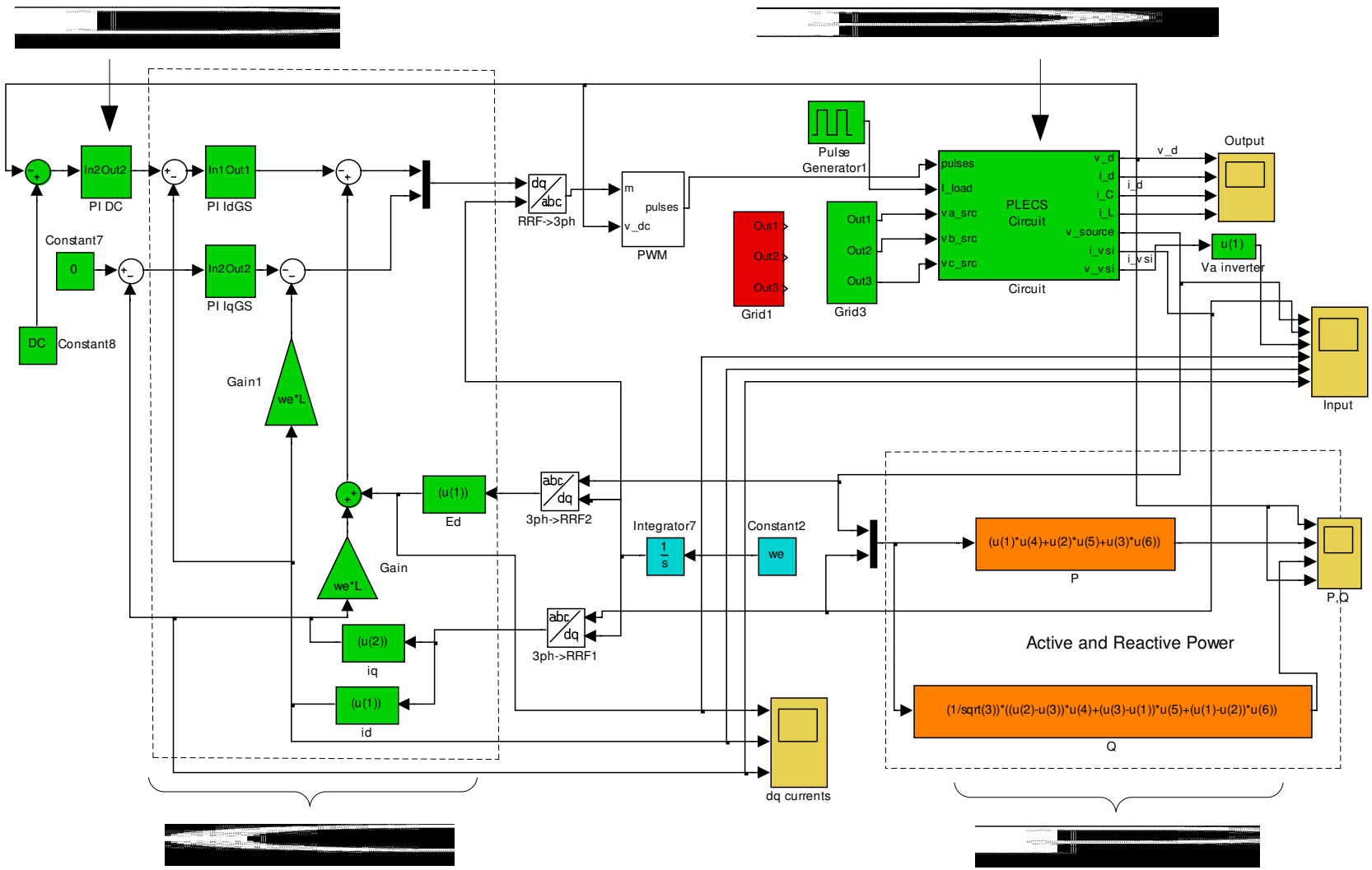


Figure 2.3. Conventional current control block diagram for grid-side converter

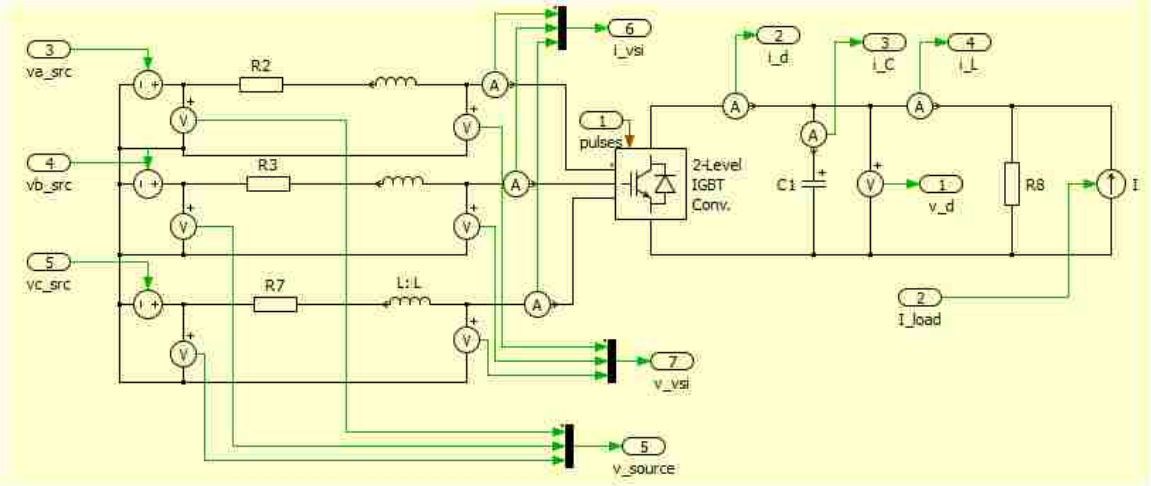


Figure 2.4. PLECS® Circuit diagram for grid-side converter

The discrete domain controllers designed by Pena [22] are implemented in the simulation by converting them to the continuous domain equivalent. The simulation is run for two different disturbances - one a three phase fault, shown in Figure 2.5 and Figure 2.6, which is a balanced disturbance, and the other a single line to ground fault, shown in Figure 2.7 and Figure 2.8, which is an unbalanced disturbance.

In the three phase fault case (Figure 2.5 and Figure 2.6), as the three phases are balanced, there is no negative sequence in the input voltage; hence, the disturbance does not affect the conventional control technique based on Park's transforms but the capacitor voltage decays with a time constant of RC circuit due to the load resistance and the dc link capacitance.

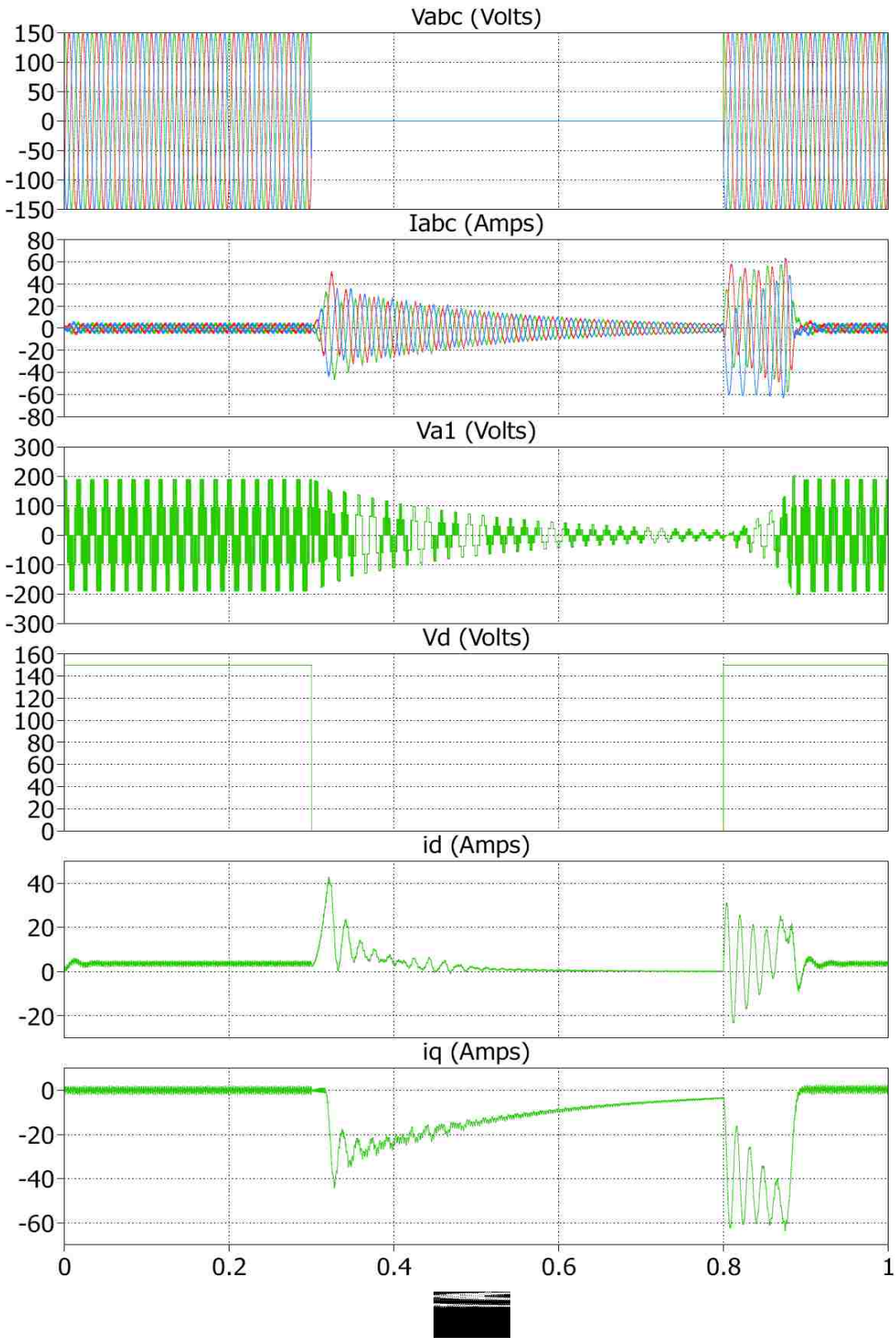


Figure 2.5. Simulation of a three phase fault (from top source voltage, source currents, converter voltage, d-axis voltage, d-axis current and q-axis current)

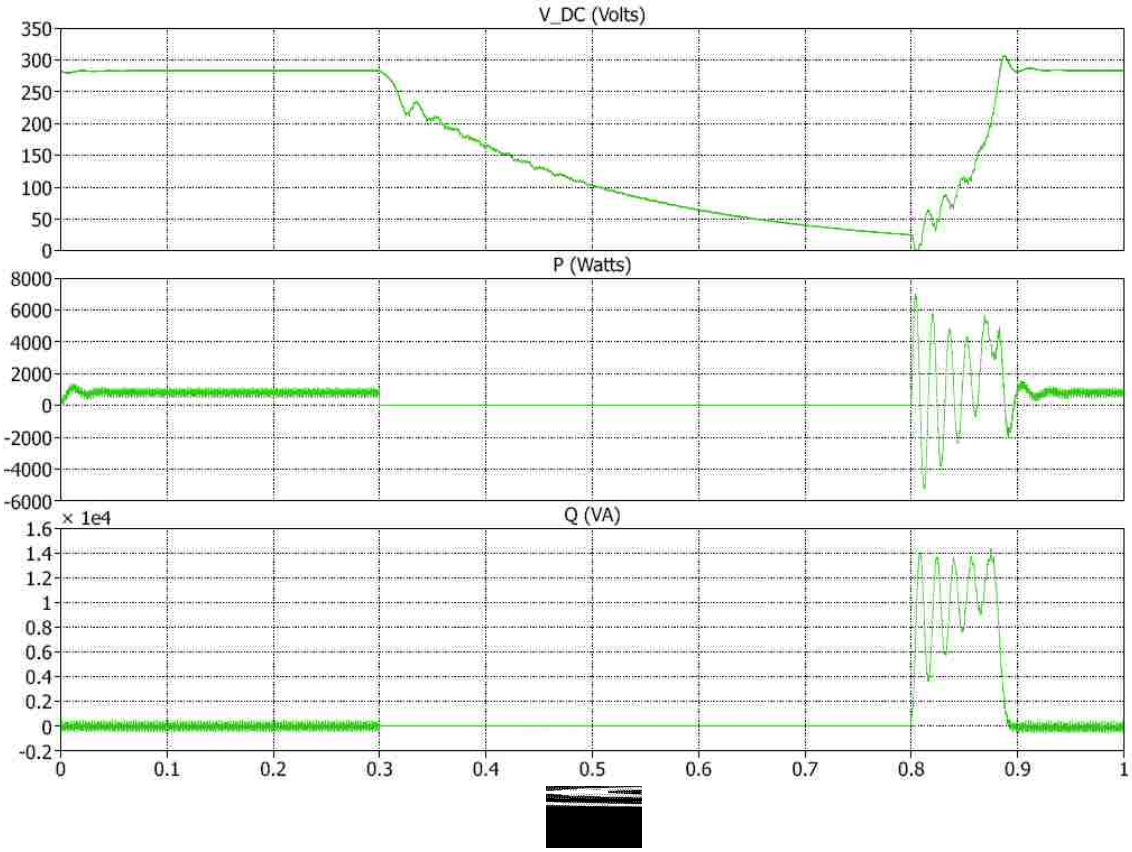


Figure 2.6. Simulation of a three phase fault (from top DC link voltage, real power, reactive power and DC link voltage)

In the single line to ground fault case (Figure 2.7 and Figure 2.8), the source voltage has a negative sequence component and hence there is a ripple in the dc link voltage. A double frequency ripple carries over to the d-axis voltage as well as in real and reactive power. The source currents are also distorted as the commanded voltages are perturbed due to the system disturbance.

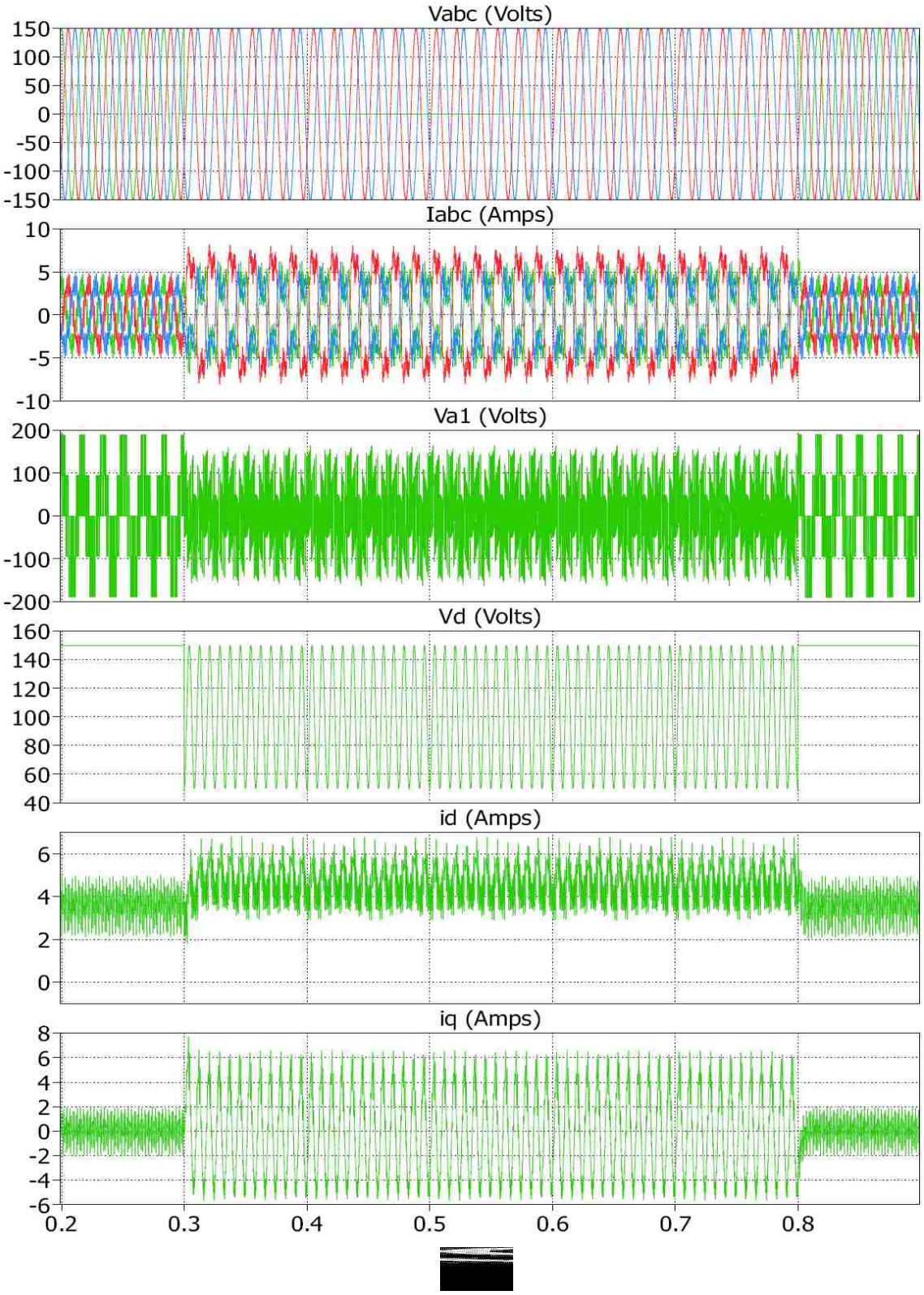


Figure 2.7. Simulation of a single line to ground fault (from top source voltage, source currents, converter voltage, d-axis voltage, d-axis current and q-axis current)

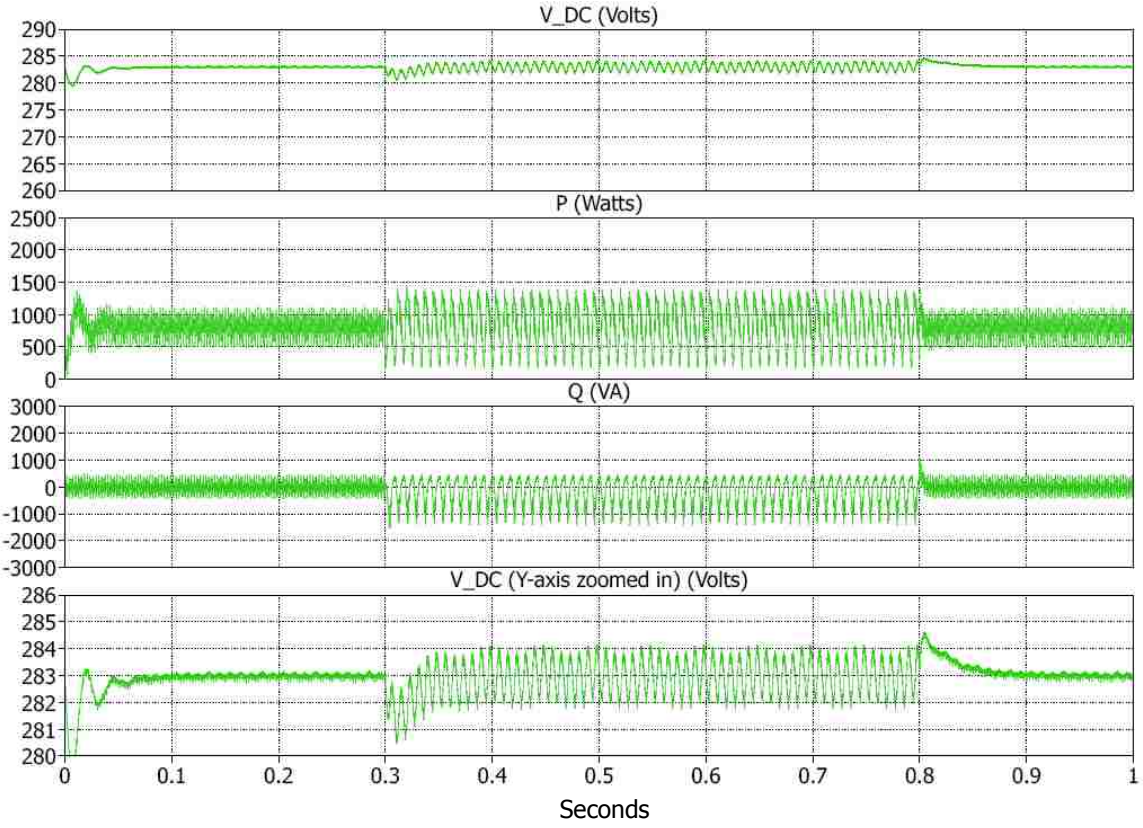


Figure 2.8. Simulation of a single line to ground fault (from top DC link voltage, real power, reactive power and DC link voltage Y-axis zoomed)

## 2.3 DFIG AND ROTOR-SIDE CONVERTER CONTROL

The objective of the rotor-side converter is to supply currents to the rotor-side part of the induction machine such that the grid-side active and reactive power is maintained according to the power tracking and desired power factor. The equations associated with the machine are from Leohard [25] and Chellapilla [26]. This converter is controlled in a dq axis reference frame with d-axis oriented along the stator-flux vector position. This reference frame allows a decoupled control between electric torque and rotor excitation. Since the stator is connected to an infinite grid and stator

resistance is small, the stator magnetizing current is assumed to be constant. The associated equations are (5)-(14).

$$\lambda_s = \lambda_{ds} = L_o i_{ms} = L_s i_{ds} + L_o i_{dr} \tag{5}$$

$$\lambda_{qr} = \sigma L_r i_{qr} \tag{6}$$

$$\lambda_{dr} = \frac{(L_o)^2}{L_s} i_{ms} + \sigma L_r i_{dr} \tag{7}$$

$$i_{qs} = \frac{-L_o}{L_s} i_{qr} \tag{8}$$

$$v_{dr} = R_r i_{dr} + \sigma L_r \frac{d}{dr} i_{dr} - \omega_{slip} \sigma L_r i_{qr} \tag{9}$$

$$\omega_{slip} = \omega_e - \omega_r \tag{10}$$

$$v_{qr} = R_r i_{qr} + \sigma L_r \frac{d}{dr} i_{qr} - \omega_{slip} (\sigma L_r i_{dr} + L_m i_{ms}) \tag{11}$$

$$T_e = -3 \frac{P}{2} L_m i_{ms} i_{qr} \tag{12}$$

$$L_m = \frac{(L_o)^2}{L_s} \tag{13}$$

$$\sigma = 1 - \frac{(L_o)^2}{L_s L_r} \tag{14}$$

The reference frame angle is calculated using (4) and (15)-(16). The stator flux speed is obtained from the derivative of the stator flux position ($\theta_s$). Stator flux speed is calculated using the differentiation of the rotor angle. The differentiator function in math

packages like Simulink® amplifies the error in the signal to a greater extent. Hence the differentiation is carried by applying the formula of arc tangent as shown in (17).

$$\lambda_{\alpha s} = \int (v_{\alpha s} - R_s i_{\alpha s}) dt \tag{15}$$

$$\lambda_{\beta s} = \int (v_{\beta s} - R_s i_{\beta s}) dt \tag{16}$$

$$\frac{d\theta}{dt} = \frac{\lambda_{\alpha s}(v_{\alpha s} - R_s i_{\alpha s}) - \lambda_{\beta s}(v_{\beta s} - R_s i_{\beta s})}{\lambda_{\alpha s}{}^2 + \lambda_{\beta s}{}^2} \tag{17}$$

The induction machine is simulated in the stationary reference frame. The control diagram for the induction machine is shown in Figure 2.9. Figure 2.10. shows simulation of induction machine above rated speed (Input - 400 rad/sec). It can be observed that the machine is demanding negative torque which means it is producing power. The second simulation is carried out on the complete DFIG at rated speed demanding zero torque as in Figure 2.11. It can be seen that the rotor torque has an average value of zero but with perceivable oscillations. These are due to approximations and errors in calculating the stator flux speed and reference angle.

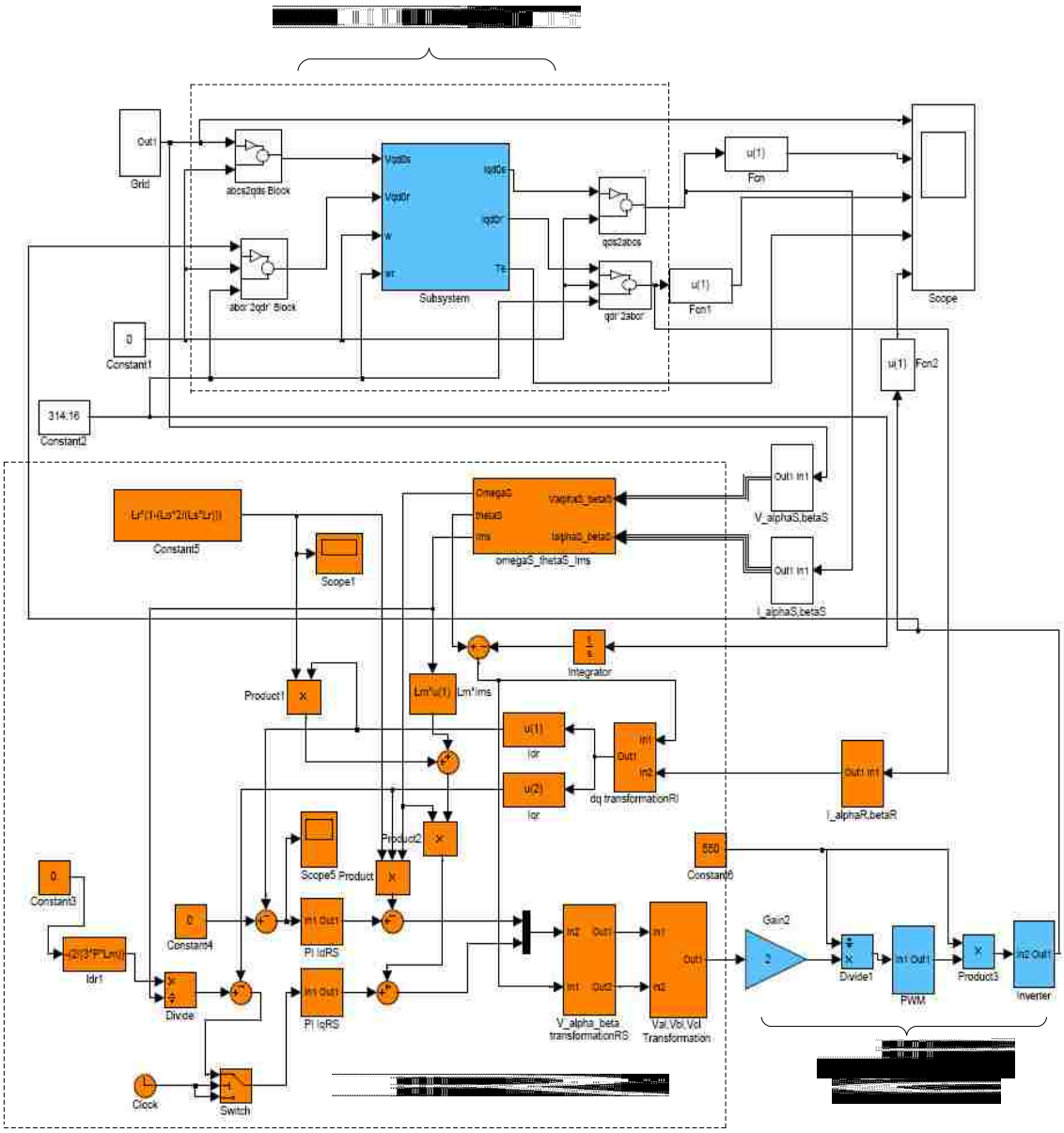


Figure 2.9. Rotor side converter and induction machine implementation

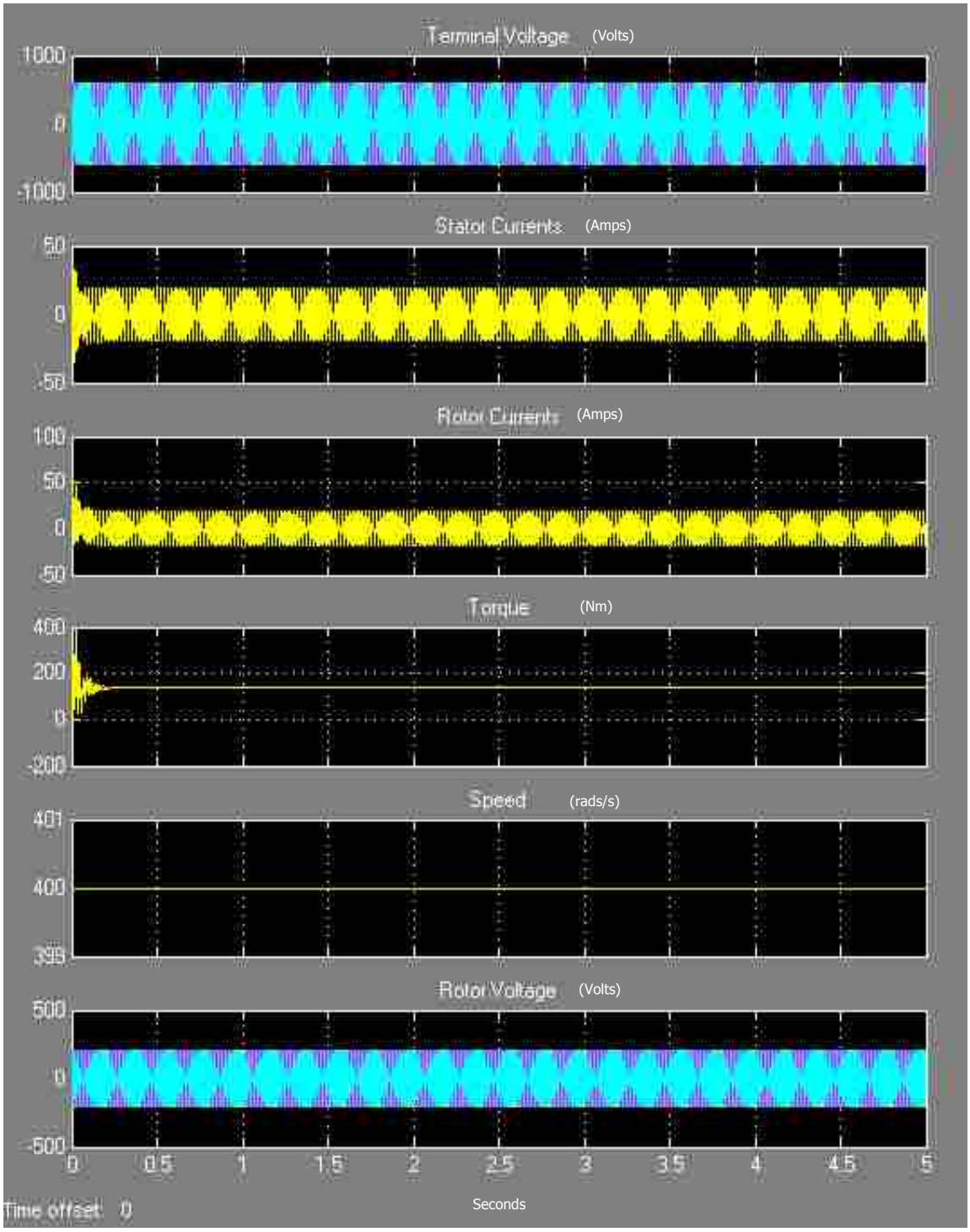


Figure 2.10. DFIG operation above rated speed

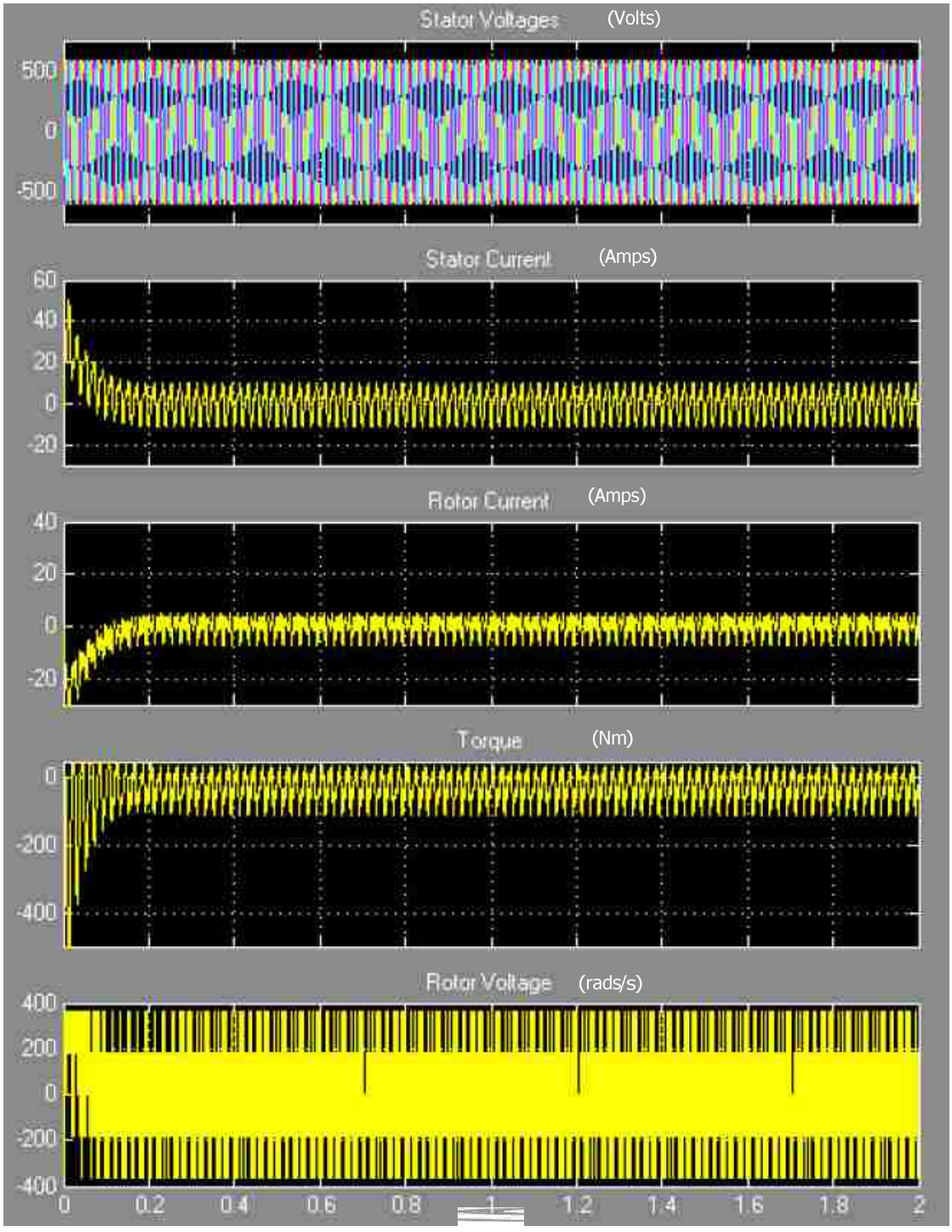


Figure 2.11. Rotor Side converter at rated speed

## 2.4 DFIG MODEL USING DIgSILENT®

A more robust model needs to be used to simulate the faults on the complete system. Review of various wind turbine models in different platforms are discussed in [27]. DIgSILENT® PowerFactory has dynamic models for wind turbine applications as discussed in [28]. Interactions between electric grid phenomena and the wind turbine using these models are discussed in [29]. Hence a dynamic DFIG-based wind turbine model [30] in DIgSILENT® mainly intended for stability analysis of large power systems is used in this study. Preliminary simulation with this model for different grid and system disturbances are discussed in [31].

The wind turbine model and power system are initially simulated for typical transient analysis for the rated values of the machine without any disturbance. The setup of the machine along with load flow is shown in Figure 2.12. Typical quantities versus time are shown in Figure 2.13. The simulation is executed for 5 seconds. The wind speed (vw) is assumed to be constant at 13.8 m/s and the output rated power of the wind turbine is 5 MW.

The simulation achieved its steady state after approximately a second. The wind speed (vw) is assumed to be constant at 13.8 m/s and the output rated power of the wind turbine is 5 MW. The simulation achieved its steady state after approximately a second. The real power commanded is 4.5 MW, reactive power is 0.2 MVar, the rotor side dc voltage commanded is 132.25V (1.15 per unit) and the reactive power commanded is -0.3 MVar.

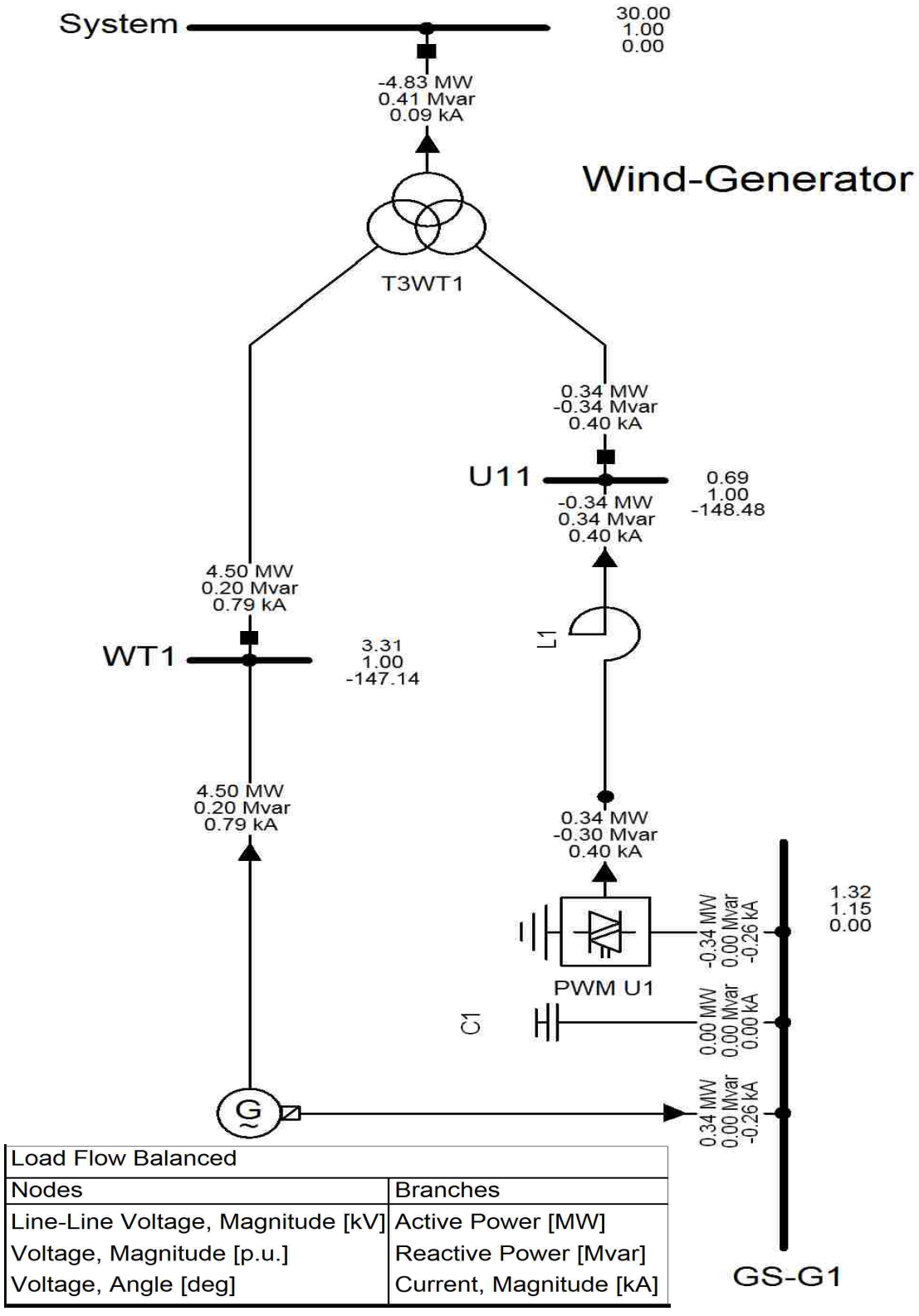


Figure 2.12. DFIG Model in DIgSILENT®

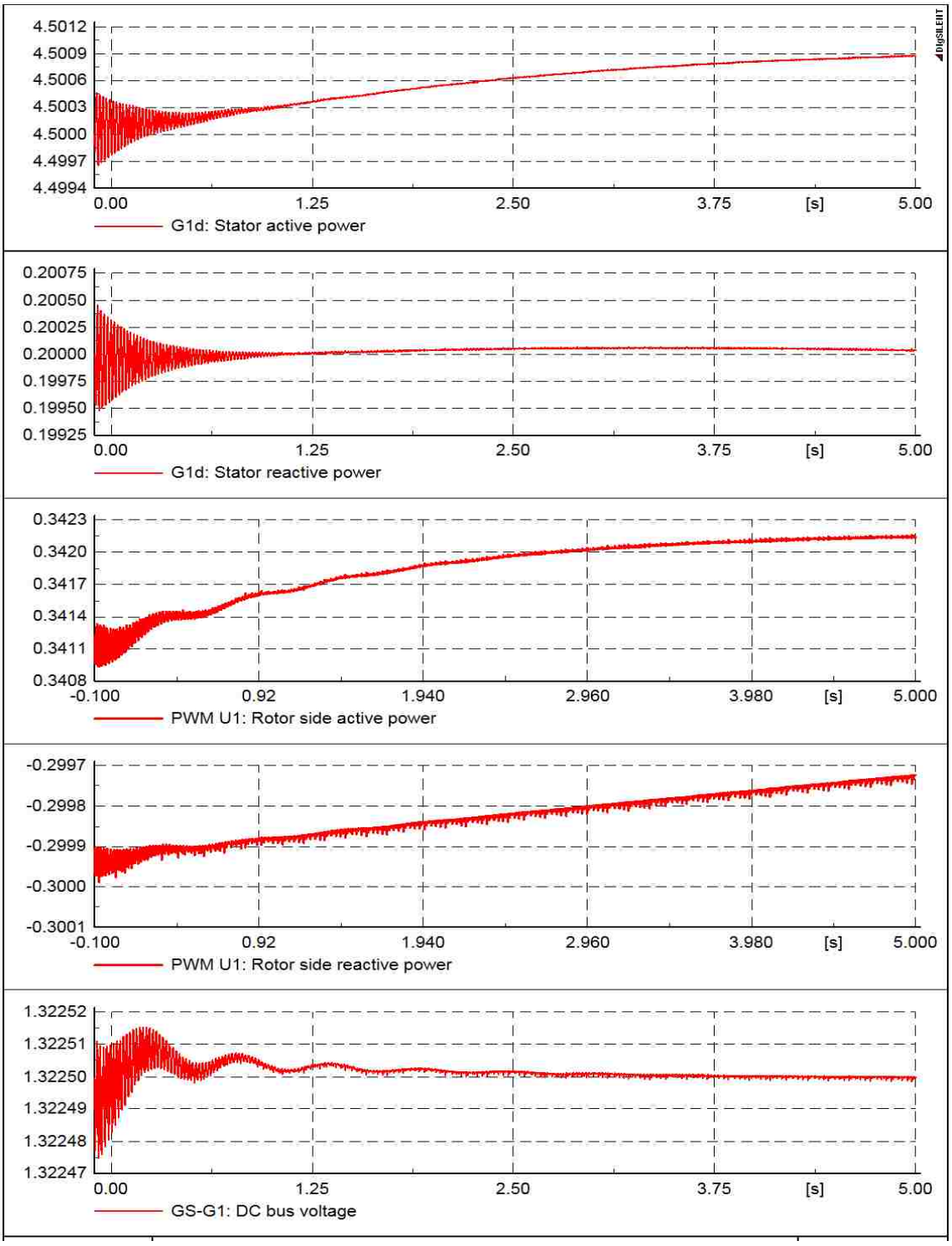


Figure 2.13. Normal Operation (Y-axis in pu)

A single line to ground fault is simulated for 600 ms. This fault causes a total voltage depression due to under voltage. The system is simulated for 10 seconds. Figure 2.14 shows the simulation results. It can be observed that the voltage of the dc bus is drastically increased to nine times the nominal voltage. Since this is undesirable, the rotor side system is short circuited during the inception if a fault.

A three phase fault is simulated near the system for 200 ms causing a full voltage collapse. The simulation results are shown in Figure 2.15. In this case it takes a longer time for the simulation to settle back after the fault event. The real power and reactive power takes much longer time to settle back compared the remaining quantities

As in the case of the single line to ground fault, the DC bus voltage increases drastically due to the fault to a value approximately 18 times the nominal voltage value (twice that of the single line to ground fault case). From the above cases it can be concluded that if there was a protection for rotor currents the rotor side converter would be disconnected during the event and the generator speed would increase. The rise in the dc link voltage is attributed to magnetic coupling between stator and rotor. The rise in the stator current induces high current in the rotor that flows through the rotor side converter [32]. The additional energy goes into charging the dc bus capacitor and thus the dc bus voltage rises rapidly, depending on the design of the converter, it is possible to limit the current by current-control on the rotor side of the converter; however this will lead to high voltages at the converter terminals that might also damage the converter. Normal practice is to equip the rotor side converter with crowbar protection during faults and voltage dips [33].

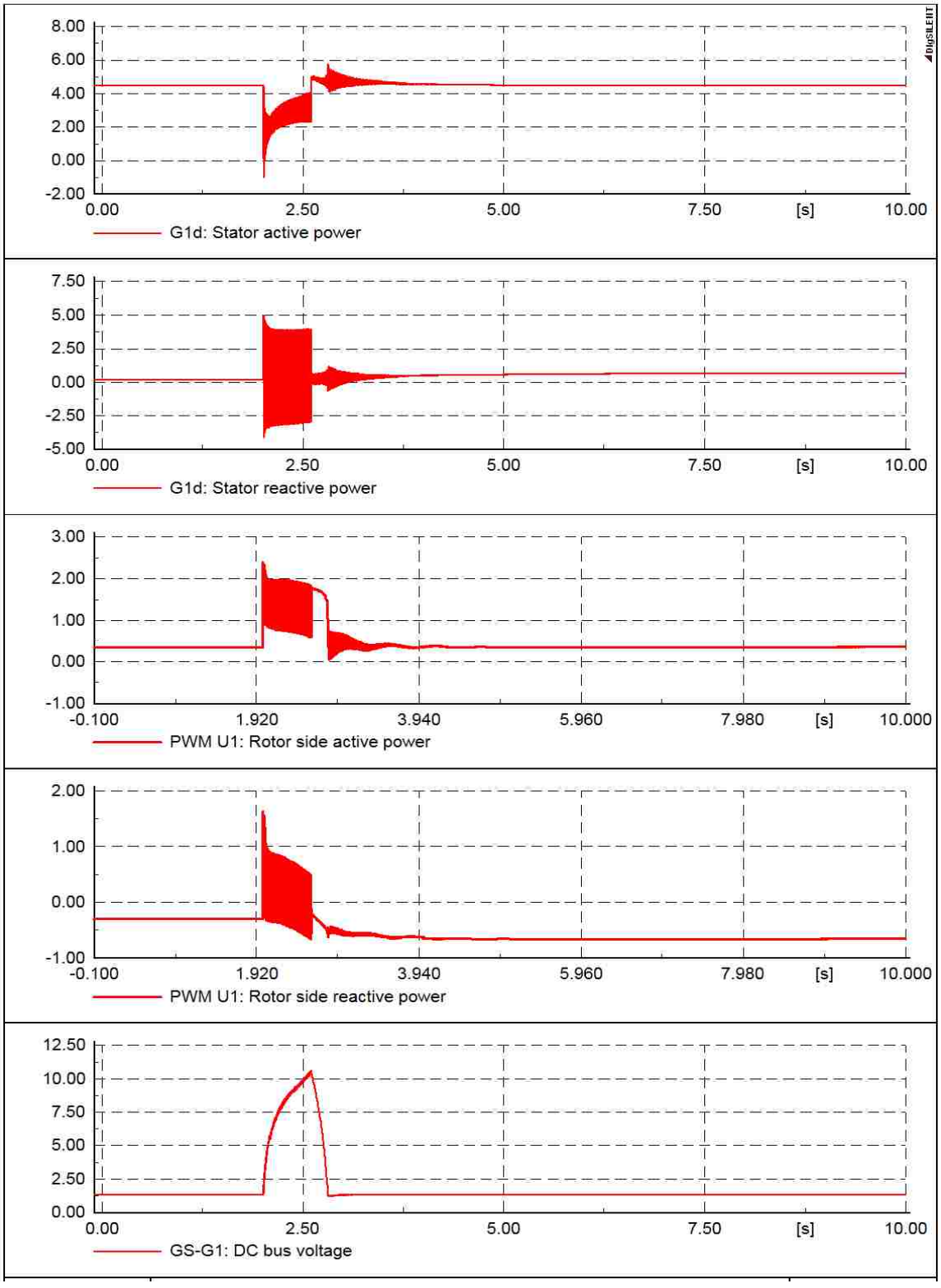


Figure 2.14. Simulation of a SLG fault (Y-axis in pu)

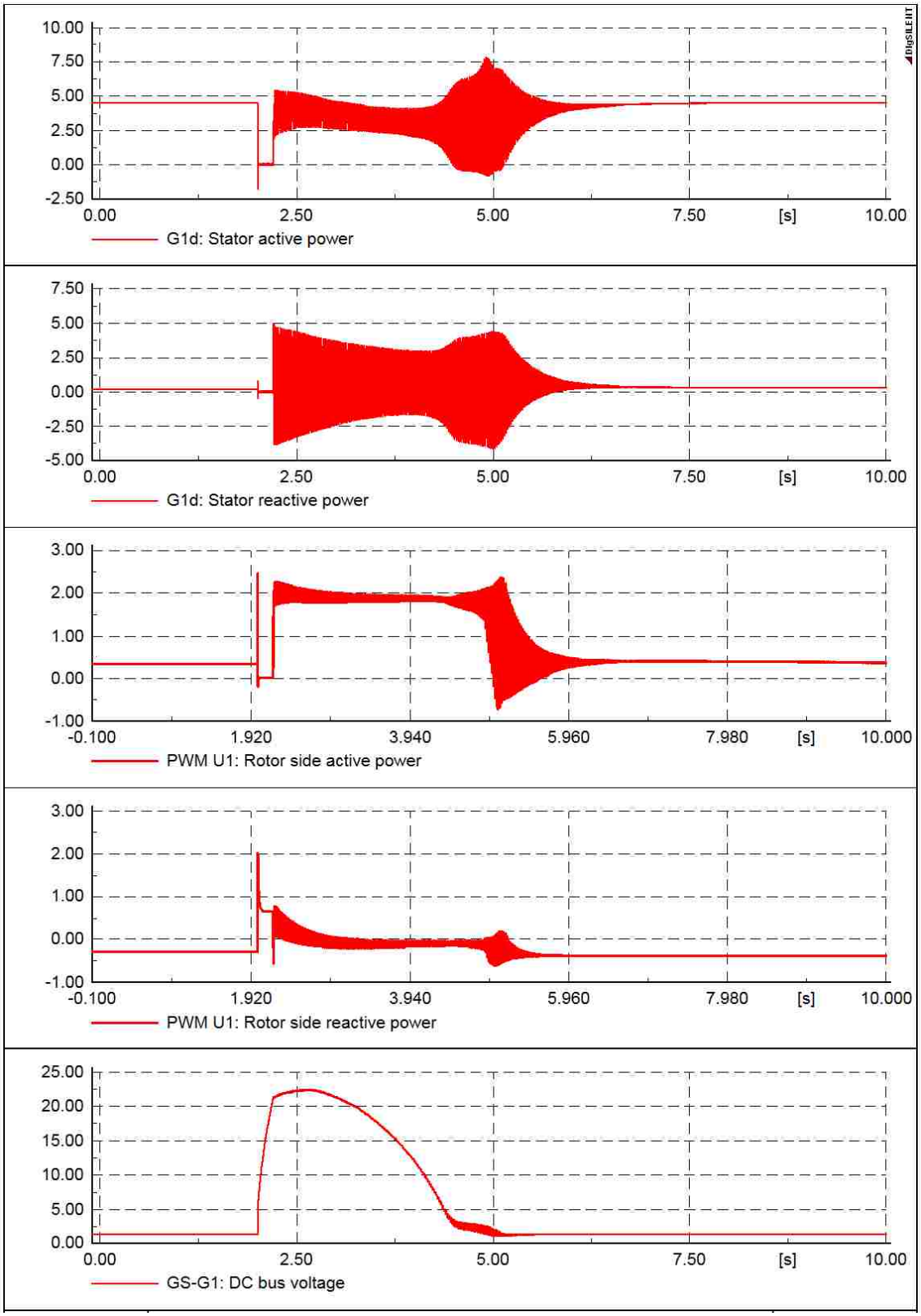


Figure 2.15. Simulation of a three phase fault (Y-axis in pu)

## 2.5 SUMMARY

This section described the operation of conventional back-to-back PWM converters for DFIG based wind turbines. In the operation, the grid side controller uses stationary dq reference frame current loops to control the dc link voltage and the reactive power. The rotor side controller uses stator flux orientation reference frame to control the real and reactive power from the stator according to the speed and wind efficiency curves. Different fault scenarios are analyzed to test the operation of the controllers during disturbances. The Conventional control technique creates oscillations in the DC link voltage and distortion in the source currents during system disturbances.

# 3. ANALYSIS OF UNBALANCED INPUTS AND SEQUENCE CONTROLLERS

## 3.1 INTRODUCTION

A disturbance on the grid voltage is generally characterized by an imbalance in the voltage or the current, either in magnitude or phase. The nature of the disturbance may be analyzed using symmetrical components theory. Hence, the control of a voltage source converter during a grid disturbance is studied using symmetrical components and multiple reference frame theory. The present work integrates several control and modeling techniques to develop a grid-side controller suitable for low voltage ride through of a DFIG. The change in the voltage dq components during a disturbance is discussed using a simple simulation using Matlab Simulink ® as shown in Figure 3.1.

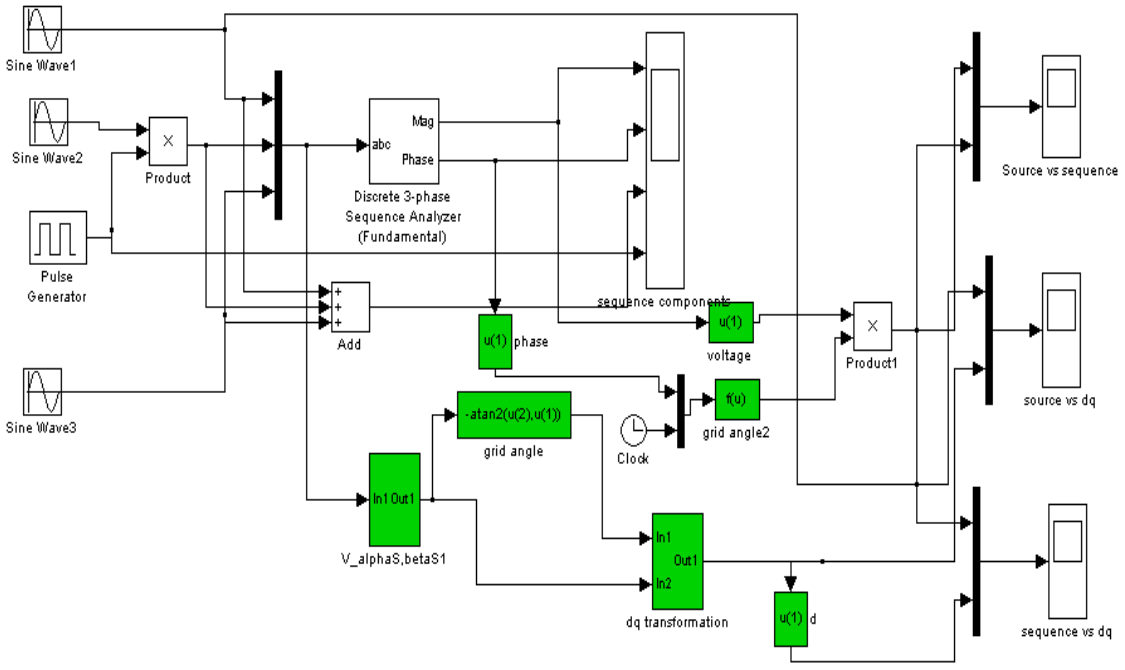


Figure 3.1. Sequence components and park's co-ordinates during a voltage imbalance

In the simulation, a line to ground fault is simulated in a balanced set of voltages after 0.5 sec. The simulation is run for 1 second. The simulation of the sequence components shows that the decoupled control during the imbalance gives rise to a negative sequence component in the output which is twice the source frequency. The simulation results are shown in Figure. 3.2. As expected, the negative sequence component appears as a second harmonic component in the synchronous reference frame.

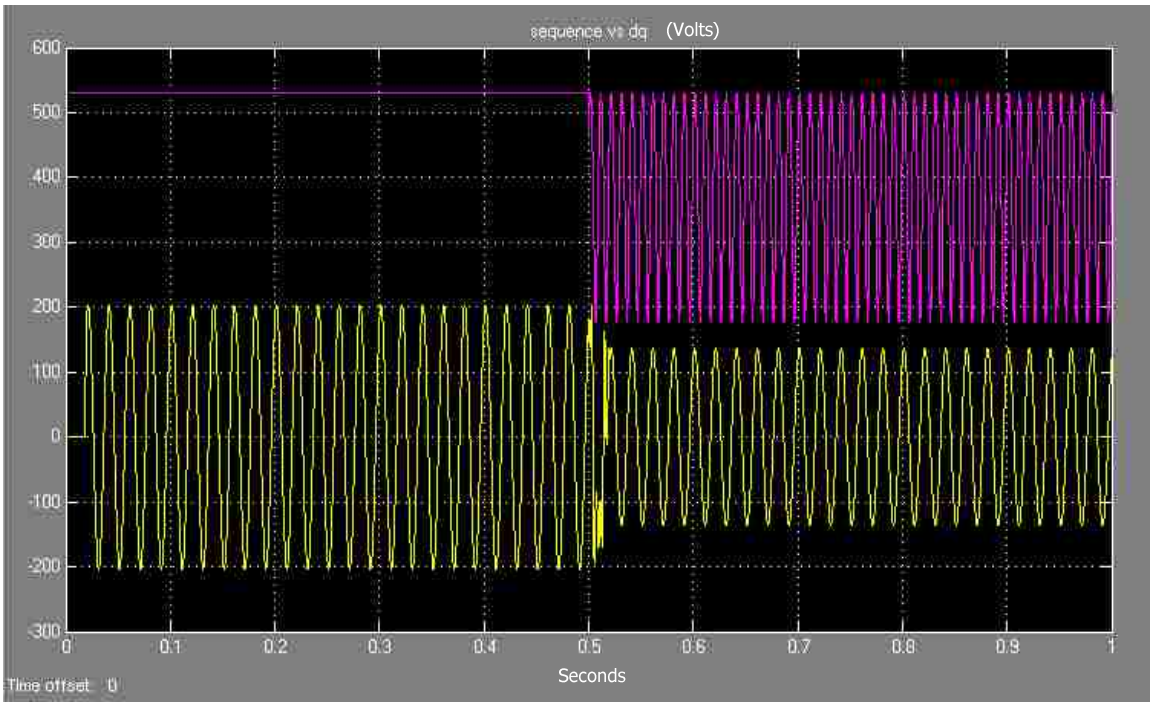


Figure 3.2. Voltage vs. dq components for a voltage disturbance

### 3.2 SEQUENCE COMPONENTS D-Q ANALYSIS

Any three phase quantities may be represented in sequence components using (18) [9].

$$\begin{pmatrix} X_a \\ X_b \\ X_c \end{pmatrix} = x_{mp}\cdot\begin{pmatrix} \cos(\omega t + \alpha_p) \\ \cos\left(\omega t + \alpha_p - \frac{2\cdot\pi}{3}\right) \\ \cos\left(\omega t + \alpha_p + \frac{2\cdot\pi}{3}\right) \end{pmatrix} + x_{mn}\cdot\begin{pmatrix} \cos(\omega t + \alpha_n) \\ \cos\left(\omega t + \alpha_n + \frac{2\cdot\pi}{3}\right) \\ \cos\left(\omega t + \alpha_n - \frac{2\cdot\pi}{3}\right) \end{pmatrix} + x_{m0}\cdot\begin{pmatrix} \cos(\omega t + \alpha_0) \\ \cos(\omega t + \alpha_0) \\ \cos(\omega t + \alpha_0) \end{pmatrix} \tag{18}$$

$x_a$, $x_b$, $x_c$ are transformed into synchronous d-q axis using (19) and (20).

$$\begin{pmatrix} X_{qe} \\ X_{de} \end{pmatrix} = \frac{2}{3}\begin{pmatrix} \cos(\omega\cdot t) & -\sin(\omega\cdot t) \\ \sin(\omega\cdot t) & \cos(\omega\cdot t) \end{pmatrix}\cdot\begin{pmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{-\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{pmatrix}\cdot\begin{pmatrix} X_a \\ X_b \\ X_c \end{pmatrix} \tag{19}$$

$$T_{32}{}^T = \begin{pmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{-\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{pmatrix} \tag{20}$$

The simplification of the equation is shown in (21) through (26).

$$\frac{2}{3}\cdot\begin{pmatrix} \cos(\omega\cdot t) & -\sin(\omega\cdot t) \\ \sin(\omega\cdot t) & \cos(\omega\cdot t) \end{pmatrix}\cdot T_{32}{}^T = \begin{bmatrix} \frac{2}{3}\cdot\cos(\omega\cdot t) & \left(\frac{-1}{3}\cdot\cos(\omega\cdot t)\ \ldots \right. \\ & \left. +\frac{1}{3}\cdot\sin(\omega\cdot t)\cdot\sqrt{3}\right) \\ \frac{2}{3}\cdot\sin(\omega\cdot t) & -\left(\frac{1}{3}\cdot\sin(\omega\cdot t)\ \ldots \right. \\ & \left. +\frac{1}{3}\cdot\cos(\omega\cdot t)\cdot\sqrt{3}\right) \end{bmatrix} \begin{bmatrix} -\left(\frac{1}{3}\cdot\cos(\omega\cdot t)\ \ldots \right. \\ \left. +\frac{1}{3}\cdot\sin(\omega\cdot t)\cdot\sqrt{3}\right) \\ \left(\frac{-1}{3}\cdot\sin(\omega\cdot t)\ \ldots \right. \\ \left. +\frac{1}{3}\cdot\cos(\omega\cdot t)\cdot\sqrt{3}\right) \end{bmatrix} \tag{21}$$

$$\frac{2}{3}\cdot\begin{pmatrix} cos(\omega\cdot t) & -sin(\omega\cdot t) \\ sin(\omega\cdot t) & cos(\omega\cdot t) \end{pmatrix}\cdot\begin{pmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{-\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{pmatrix} = \frac{2}{3}\cdot\begin{pmatrix} cos(\omega\cdot t) & cos\left(\omega\cdot t - \frac{2\pi}{3}\right) & cos\left(\omega\cdot t + \frac{2\pi}{3}\right) \\ sin(\omega\cdot t) & sin\left(\omega\cdot t - \frac{2\pi}{3}\right) & sin\left(\omega\cdot t + \frac{2\pi}{3}\right) \end{pmatrix} \tag{22}$$

$$\begin{pmatrix} X_{qe} \\ X_{de} \end{pmatrix} = \frac{2}{3}\cdot\begin{pmatrix} cos(\omega\cdot t) & cos\left(\omega\cdot t - \frac{2\pi}{3}\right) & cos\left(\omega\cdot t + \frac{2\pi}{3}\right) \\ sin(\omega\cdot t) & sin\left(\omega\cdot t - \frac{2\pi}{3}\right) & sin\left(\omega\cdot t + \frac{2\pi}{3}\right) \end{pmatrix}\cdot\begin{pmatrix} X_a \\ X_b \\ X_c \end{pmatrix} \tag{23}$$

$$\frac{2}{3}\cdot\begin{pmatrix} cos(\omega\cdot t) & cos\left(\omega\cdot t - \frac{2\pi}{3}\right) & cos\left(\omega\cdot t + \frac{2\pi}{3}\right) \\ sin(\omega\cdot t) & sin\left(\omega\cdot t - \frac{2\pi}{3}\right) & sin\left(\omega\cdot t + \frac{2\pi}{3}\right) \end{pmatrix}\cdot\left[\begin{array}{l} x_{mp}\cdot\begin{pmatrix} cos(\omega\cdot t + \alpha_p) \\ cos\left(\omega\cdot t + \alpha_p - \frac{2\cdot\pi}{3}\right) \\ cos\left(\omega\cdot t + \alpha_p + \frac{2\cdot\pi}{3}\right) \end{pmatrix} \dots \\ + x_{mn}\cdot\begin{pmatrix} cos(\omega\cdot t + \alpha_n) \\ cos\left(\omega\cdot t + \alpha_n + \frac{2\cdot\pi}{3}\right) \\ cos\left(\omega\cdot t + \alpha_n - \frac{2\cdot\pi}{3}\right) \end{pmatrix} + x_{m0}\cdot\begin{pmatrix} cos(\omega\cdot t + \alpha_0) \\ cos(\omega\cdot t + \alpha_0) \\ cos(\omega\cdot t + \alpha_0) \end{pmatrix} \end{array}\right] \tag{24}$$

$$\frac{2}{3}\cdot\begin{pmatrix} cos(\omega\cdot t) & cos\left(\omega\cdot t - \frac{2\pi}{3}\right) & cos\left(\omega\cdot t + \frac{2\pi}{3}\right) \\ sin(\omega\cdot t) & sin\left(\omega\cdot t - \frac{2\pi}{3}\right) & sin\left(\omega\cdot t + \frac{2\pi}{3}\right) \end{pmatrix}\cdot\begin{pmatrix} cos(\omega\cdot t + \alpha_p) \\ cos\left(\omega\cdot t + \alpha_p - \frac{2\cdot\pi}{3}\right) \\ cos\left(\omega\cdot t + \alpha_p + \frac{2\cdot\pi}{3}\right) \end{pmatrix} = \begin{pmatrix} cos(\alpha_p) \\ -sin(\alpha_p) \end{pmatrix} \tag{25}$$

$$\frac{2}{3}\cdot\begin{pmatrix} cos(\omega\cdot t) & cos\left(\omega\cdot t-\frac{2\pi}{3}\right) & cos\left(\omega\cdot t+\frac{2\pi}{3}\right) \\ sin(\omega\cdot t) & sin\left(\omega\cdot t-\frac{2\pi}{3}\right) & sin\left(\omega\cdot t+\frac{2\pi}{3}\right) \end{pmatrix}\cdot\begin{pmatrix} cos\left(\omega\cdot t+\alpha_n\right) \\ cos\left(\omega\cdot t+\alpha_n+\frac{2\cdot\pi}{3}\right) \\ cos\left(\omega\cdot t+\alpha_n-\frac{2\cdot\pi}{3}\right) \end{pmatrix}=\begin{pmatrix} cos(2\omega\cdot t) & -sin(2\omega\cdot t) \\ sin(2\omega\cdot t) & cos(2\omega\cdot t) \end{pmatrix}\cdot\begin{pmatrix} cos\left(\alpha_n\right) \\ sin\left(\alpha_n\right) \end{pmatrix} \tag{26}$$

Simplification of the expression yields (27)

$$\begin{pmatrix} X_{qe} \\ X_{de} \end{pmatrix}=\left[X_{mp}\cdot\begin{pmatrix} cos\left(\alpha_p\right) \\ -sin\left(\alpha_p\right) \end{pmatrix}+X_{mn}\cdot\begin{pmatrix} cos(2\omega\cdot t) & -sin(2\omega\cdot t) \\ sin(2\omega\cdot t) & cos(2\omega\cdot t) \end{pmatrix}\cdot\begin{pmatrix} cos\left(\alpha_n\right) \\ sin\left(\alpha_n\right) \end{pmatrix}\right]=\begin{pmatrix} X_{qpe} \\ X_{dpe} \end{pmatrix}+R(2\omega\cdot t)\cdot\begin{pmatrix} X_{qne} \\ X_{dne} \end{pmatrix} \tag{27}$$

It can be seen from the equation (27) that the positive sequence is expressed as a DC component and the negative sequence as a second harmonic component where *R* is the reference frame transformation matrix. The inverse notion of the above equation is shown as (28) and (29)

$$\begin{pmatrix} X_a \\ X_b \\ X_c \end{pmatrix}=T_{32}R(\omega t)\begin{pmatrix} X_{qpe} \\ X_{dpe} \end{pmatrix}+T_{32}R(-\omega t)\begin{pmatrix} X_{qne} \\ X_{dne} \end{pmatrix} \tag{28}$$

$$X_{abc}=T_{32}\cdot R(\omega\cdot t)\cdot X_{qdpe}+T_{32}\cdot R(-\omega\cdot t)\cdot X_{qdne} \tag{29}$$

In these cases, the current reference is distorted by a second harmonic voltage due to the presence of the negative sequence component. Hence, a more detailed control which takes into account this imbalance needs to be investigated.

### 3.3 SEQUENCE CONTROLLERS SIMULATION AND SYSTEM IMBALANCE

The first approach of solving imbalances in source voltages is to use two different reference frames for the positive and the negative sequence components [7-11]. This would decouple the control in the respective sequence frames. A dual control scheme similar to that reported in ref [10] is simulated. Here, the positive sequence is simulated in the positive SRF and the negative sequence is simulated in the negative SRF. A low pass filter or second order notch filter of 120 Hz frequency need to be used to separate the components from the real values. As the imbalance is seen as a 120Hz wave, it is eliminated using the notch filter. As a choice, a low pass filter is excluded due to instability issues with the simulation [10].

The d-q controllers in the positive and negative sequence are commanded based on the real and reactive power equations as shown in (30-32). Equation (30) gives the real power of the system during the presence of both positive and negative sequence components. Equation (31) gives the short form of (30) where the constant terms are the coefficients of average, sine and cosine terms as represented by the subscripts.

$$\begin{aligned} E\cdot i_{os} = {} & \frac{3}{2}\cdot\left(V_{qpe}\cdot i_{qpe} + V_{dpe}\cdot i_{dpe} + V_{qne}\cdot i_{qne} + V_{dne}\cdot i_{dne}\right) \cdots \\ & + \frac{3}{2}\cdot cos(2\cdot\omega\cdot t)\cdot\left(V_{qne}\cdot i_{qpe} + V_{dne}\cdot i_{dpe} + V_{qpe}\cdot i_{qne} + V_{dpe}\cdot i_{dne}\right) \cdots \\ & + \frac{3}{2}\cdot sin(2\cdot\omega\cdot t)\cdot\left(-V_{dne}\cdot i_{qpe} + V_{qne}\cdot i_{dpe} + V_{dpe}\cdot i_{qne} + V_{qde}\cdot i_{dne}\right) \end{aligned} \tag{30}$$

$$P = E\cdot i_{os} = P_0 + P_{c2}\cdot cos(2\cdot\omega\cdot t) + P_{s2}\cdot sin(2\cdot\omega\cdot t) \tag{31}$$

$$Q = Q_0 + Q_{c2}\cdot cos(2\cdot\omega\cdot t) + Q_{s2}\cdot sin(2\cdot\omega\cdot t) \tag{32}$$

The DC controller commands the DC link voltage to a constant value thus producing the command for average DC voltage. The q and d controllers in the positive

and negative sequence domain control the average real power component, average reactive power component, real power cosine component and real power sine component coefficients to zero [12],[32]. In general the negative sequence current controllers can be commanded to zero [9], [34] but this does not achieve the desired reactive power output. The simulation is done in Matlab Simulink® using the PLECS® block set. The block diagram is show in Figure 3.3. The circuit diagram is the same as shown earlier in Figure 2.4.

The behavior of the DC link voltage is observed by applying unbalanced voltages to the VSC with conventional control and with the sequence controllers separately. These results are compared with simulation results obtained by the conventional current control technique. It is observed from Figure 3.4 and Figure 3.5 that in steady state the oscillations in the DC link voltage and thus in real and reactive power are less than that obtained by the conventional control. However, the sequence controller takes a longer time to achieve steady state compared to the conventional controller.

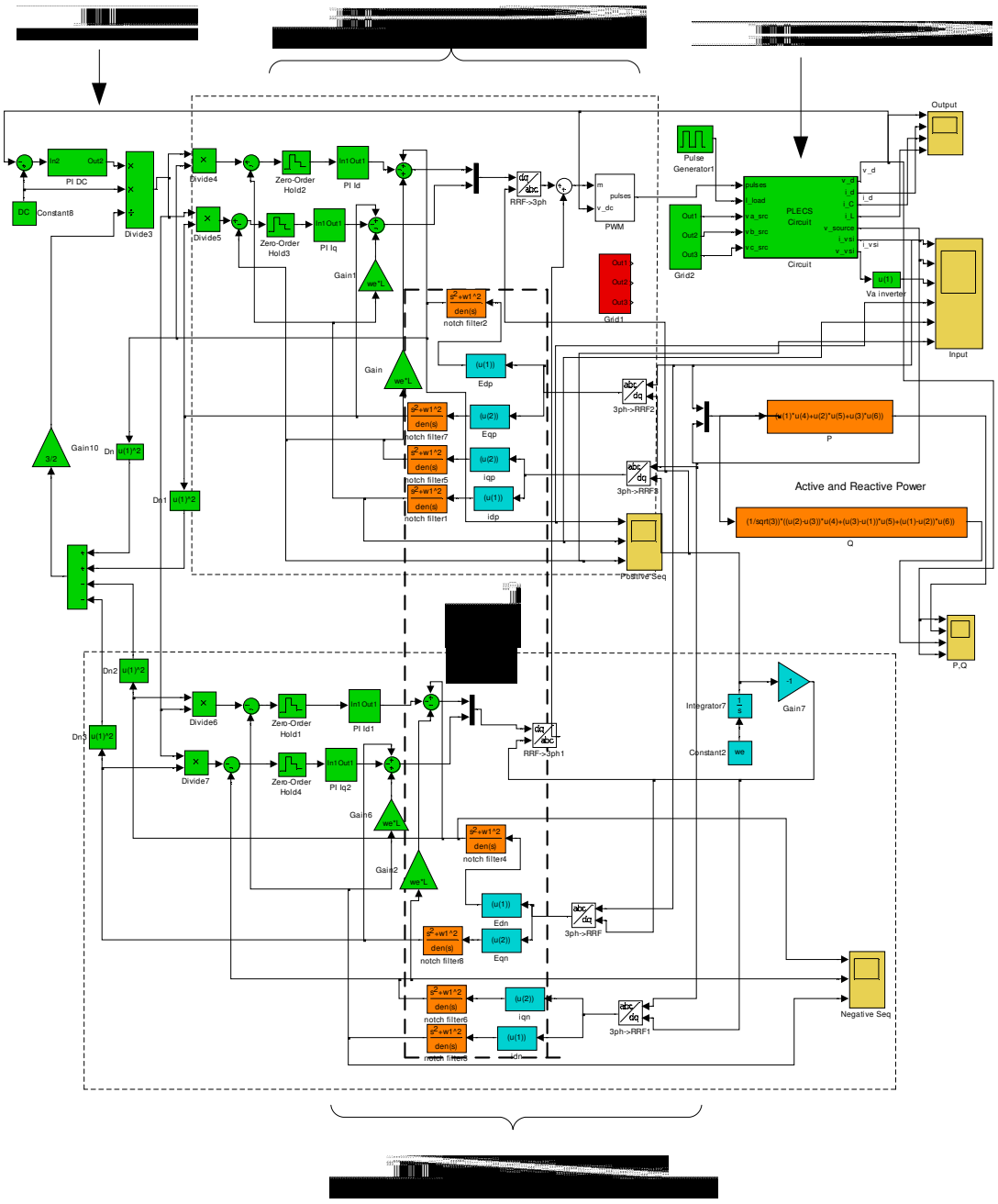


Figure. 3.3. Block diagram of the VSC controller using sequence controllers

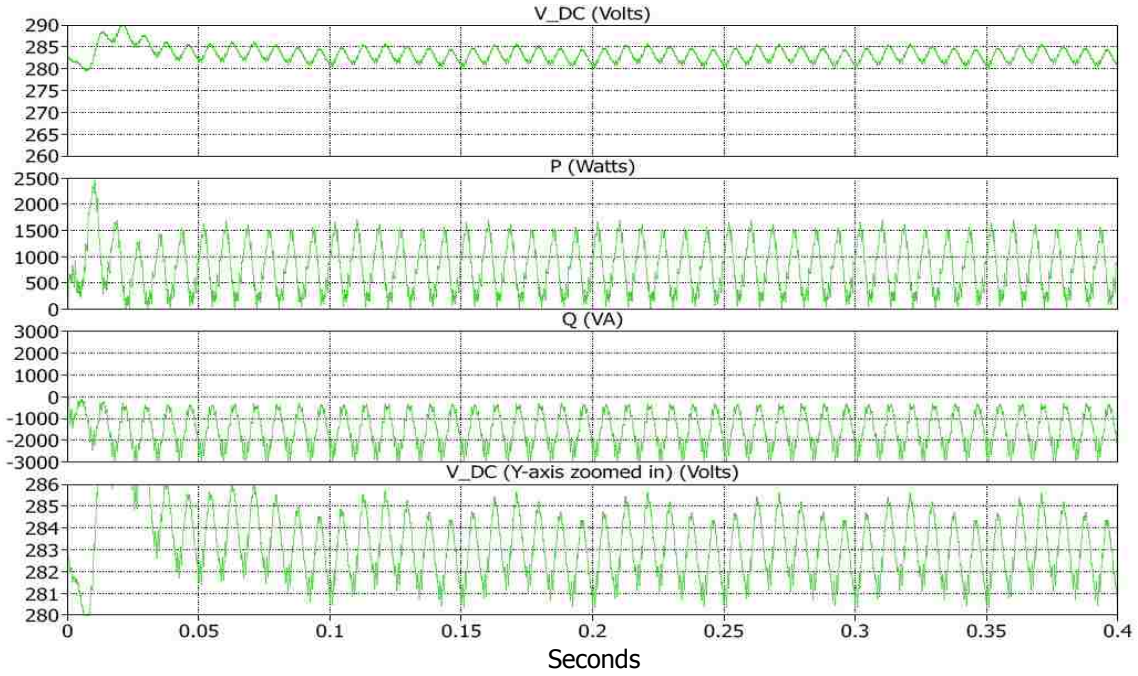


Figure 3.4. Voltage imbalance simulation for conventional controller (from top DC link voltage, real power, reactive power and DC link voltage Y-axis zoomed)

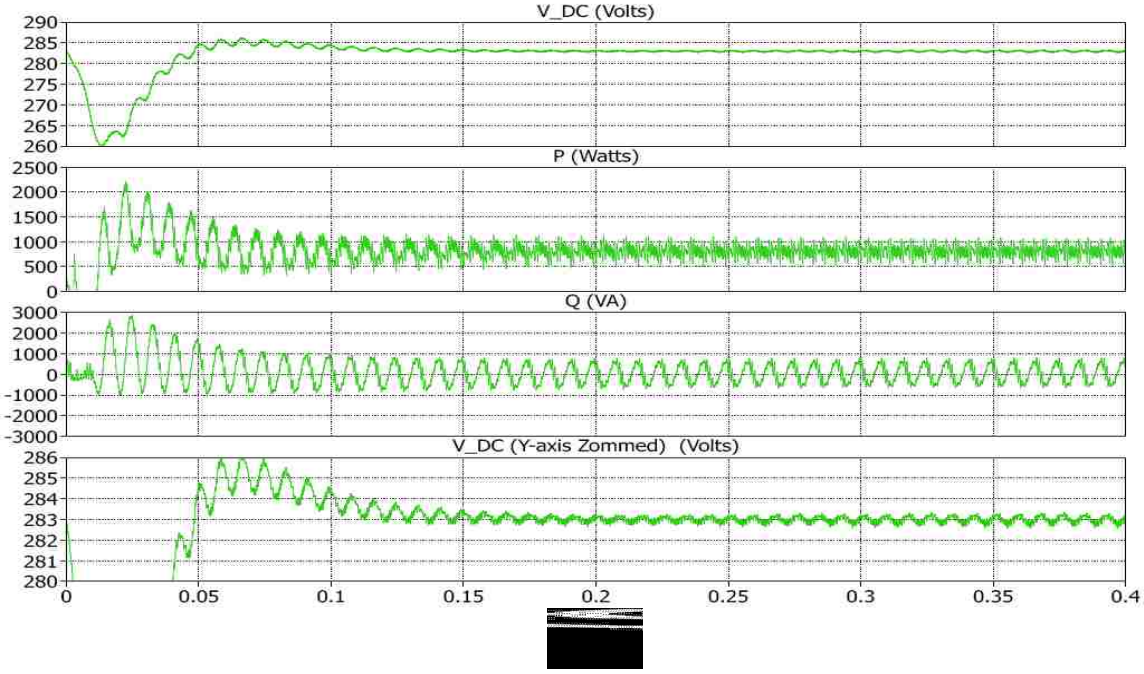


Figure 3.5. Voltage imbalance simulation for sequence controllers (from top DC link voltage, real power, reactive power and DC link voltage Y-axis zoomed)

Figure 3.6 and Figure 3.7 compare the dq components of the sequence controller and the conventional controller respectively. In the conventional controller, the d axis voltage is proportional to DC link voltage and is supposed to be a straight line for normal operation. During voltage imbalance, the dc link voltage exhibits double frequency oscillations. In the sequence controller positive d-axis voltage and negative d-axis voltage are approximately straight lines with oscillation of much smaller magnitude. The currents of the sequence controller are smooth compared to the conventional control. The q-axis currents of the conventional controller have an average value. In the general case the q-axis currents should have an average value of zero. This is achieved by the sequence controllers.

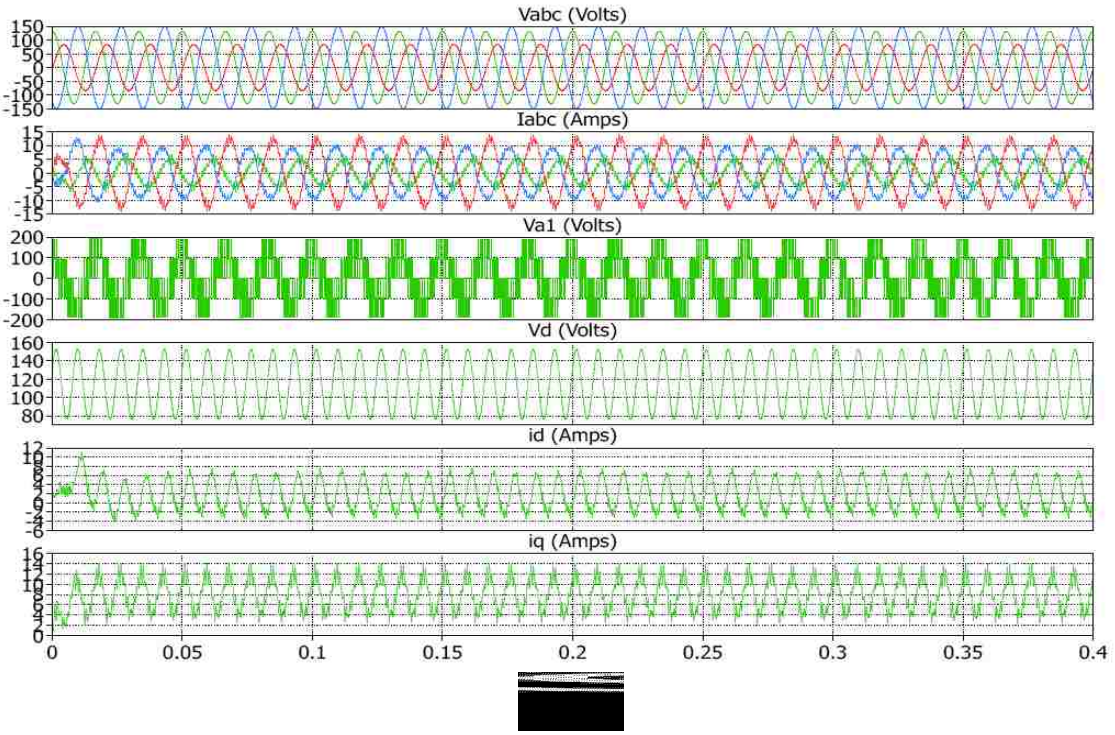


Figure 3.6. Voltage imbalance simulation for conventional controller (from top source voltages, source currents, converter voltage, d-axis voltage, d-axis current and q-axis current)

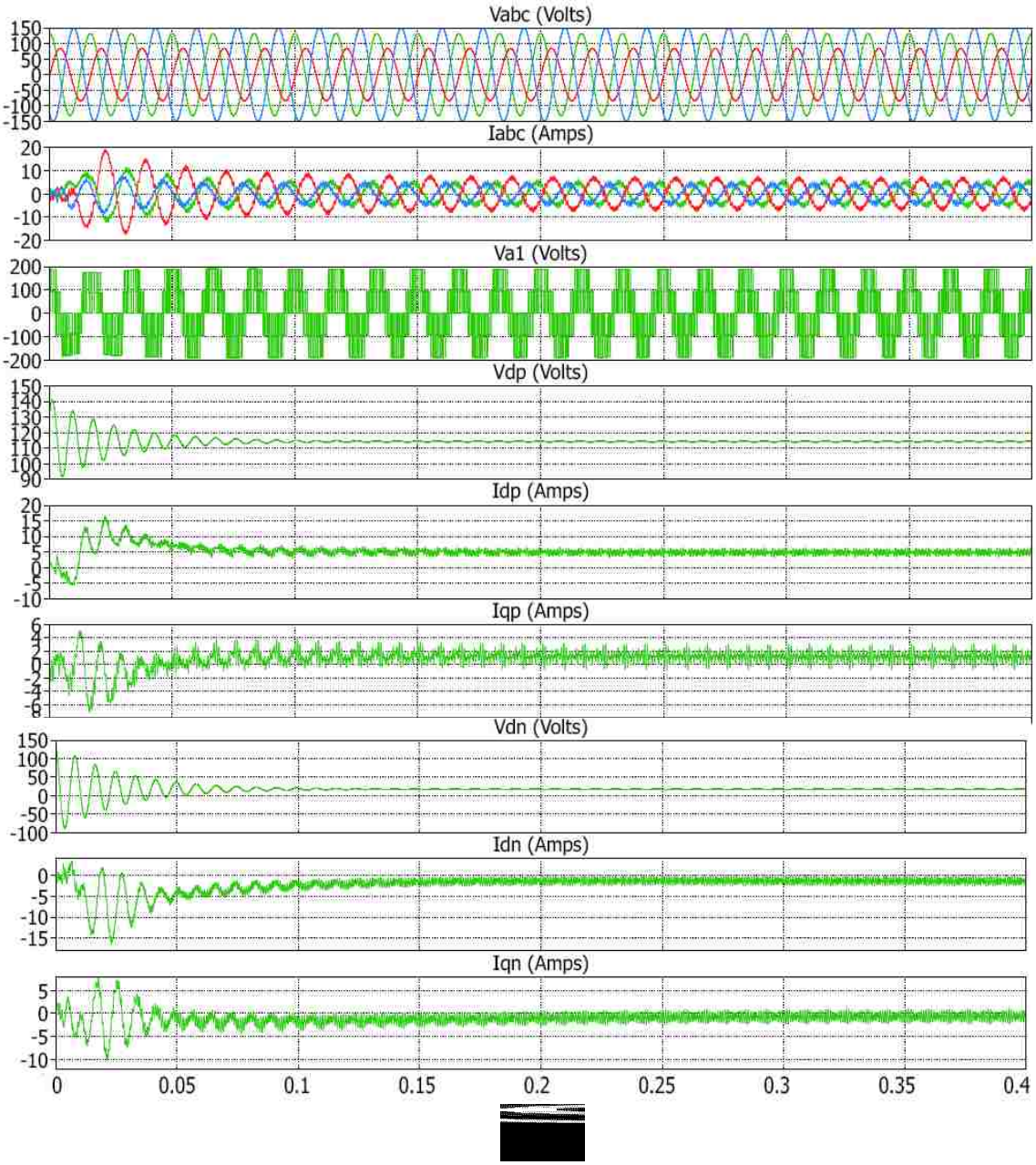


Figure 3.7. Voltage imbalance simulation for sequence controller (from top source voltages, source currents, converter voltage, positive sequence d-axis voltage, positive sequence d-axis current, positive sequence q-axis current, negative sequence d-axis voltage, negative sequence d-axis current, negative sequence q-axis current)

The sequence controllers are tested for a sudden change in the grid condition using a single line to ground (SLG) fault on one of the phases as shown in Figure 3.8 and Figure 3.9. The simulations are run for one second. The fault is applied at 0.3 seconds and removed at 0.8 seconds. The DC link voltage and thus P and Q have lesser oscillations than the conventional controller. It can be observed that the system with sequence controllers have high peak overshoot and their response is more sluggish than with conventional controller. The sluggish response of this control is due to the larger number of PI control loops (five compared to three in conventional control). Hence reducing the number of control loops would make the system respond faster.

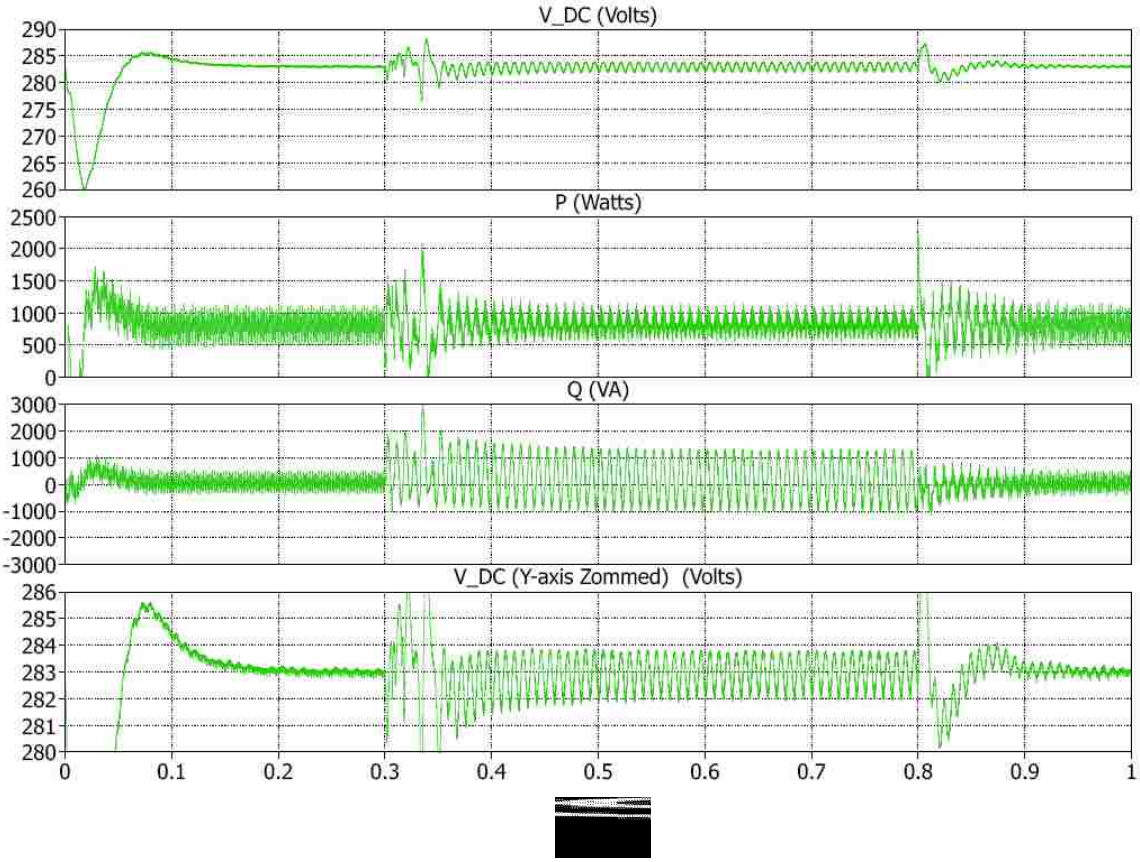


Figure 3.8. Single line fault simulation for sequence controllers (DC link voltage, real power, reactive power and DC link voltage Y-axis zoomed)

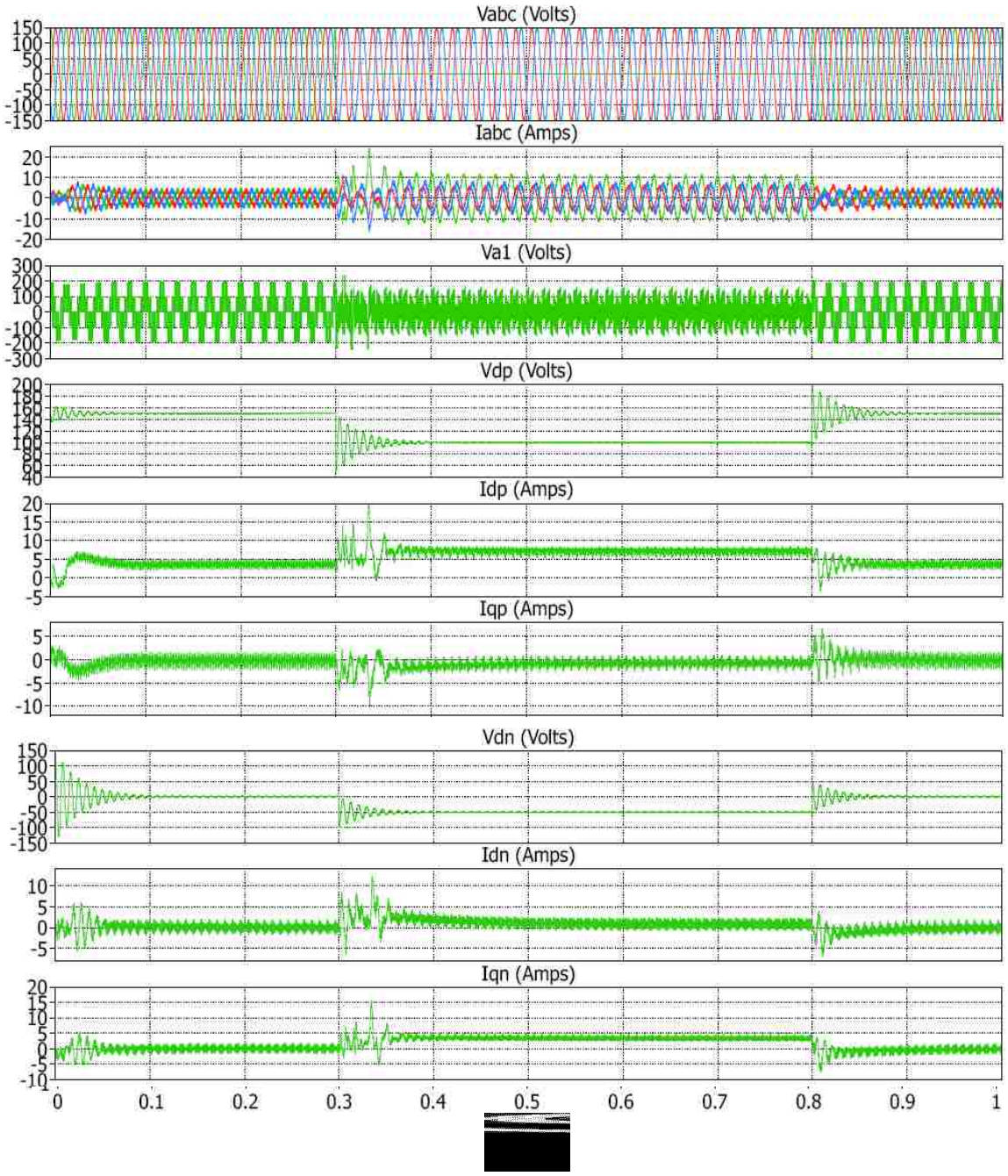


Figure 3.9. Single line fault simulation for sequence controller (from top source voltages, source currents, converter voltage, positive sequence d-axis voltage, positive sequence d-axis current, positive sequence q-axis current, negative sequence d-axis voltage, negative sequence d-axis current, negative sequence q-axis current)

Sequence controllers were also used on the rotor side converter of the DFIG by Lie et al. [13]. For rotor side converter analysis a rotor current control strategy based on positive and negative (dq) reference frames was used to provide precise control of the rotor positive and negative sequence currents. Sequence controllers for rotor side uses two PI controllers as well as band trap filters to separate the positive and negative sequence components, increasing the complexity of implementation. It was found that the overall converter ratings of the rotor side converter needed to be increased.

### 3.4 SUMMARY

Sequence control of the VSC acts as a good choice for a prolonged disturbance in the power system as in the case of a weak grid. It achieves stable voltages and currents even in the presence of a disturbance. This technique employs two different PI loops in both positive synchronous and negative synchronous reference frames (one PI loop in the d-axis and the other PI loop in the q-axis). The separation of voltage and currents in these frames is done using two notch filters in each reference frame. There are a total of five PI controllers including the dc link voltage and four notch filters which should be fine-tuned according to the system parameters, thus increasing the complexity of the system implementation. A larger number of controllers makes the system sluggish when compared to the performance of a conventional controller. Hence a fast acting control technique which uses fewer control loops, such as the direct power control technique, is employed for further analysis. This technique is discussed in detail in the next section.

# 4. DIRECT POWER CONTROL FOR DFIG-BASED WIND TURBINES

## 4.1 INTRODUCTION

A fast acting controller that gets rid of the conventional current control and acts directly upon the real and reactive power of the system is proposed by [14]. As this control acts directly according to the error in the real and reactive powers, this control is called Direct Power Control (DPC). In this control, the power required for the converters are commanded using the instantaneous voltages and currents whether they are balanced or not. The Sequence controller uses more complicated control and is more sluggish than the conventional current control approach. In the present section, DPC is adapted from motor drive applications to grid-side control of a DFIG and integrated with a DPC-based rotor-side converter to achieve fast response. Also, a modified DPC algorithm is derived to reduce current harmonics that occur in the grid-side converter during disturbances.

Figure 4.1 shows the single line diagram of the PWM converter shown earlier in Figure 2.2. $v_{abc}$ represents the source or the line voltage and $v_{a1b1c1}$ represents the voltage of the converter that can be controlled by the DC link. The voltage of the converter depends upon the switching sequence of the converter and the magnitude of the DC voltage. The series inductance of the line and the dc bus capacitance provides boost characteristics for the converter from the AC to the DC side. The flow of current from the source to the load is governed by the difference between the source voltage and the converter voltage. The line inductance provides stiff current characteristics to the source whereas the bus capacitance provides stiff voltage characteristics to the dc link. Typically the source voltage is assumed to be constant although this may not be

true in case of system imbalance. Hence the flow of the current in the circuit is governed by the magnitude and angle of the converter voltage.

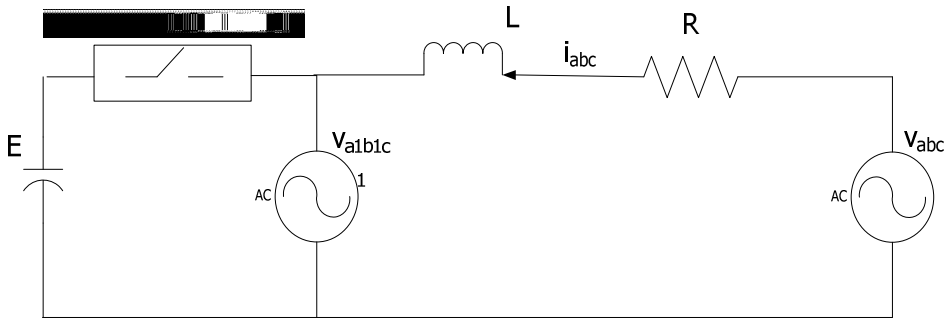


Figure 4.1. Single line diagram of the PWM converter

## 4.2 DPC SWITCHING STATES AND DELTA MODULATION

The switching states of a voltage source inverter are based on the space vector modulation approach presented in [35] and discussed in detail in [36]. In this approach, the converter voltages are referred to as space vectors in an α-β reference frame (stationary reference frame). There are eight possible states for these vectors depending on the converter switching possibilities as shown in Figure 4.2. The eight possible vectors are represented on an α-β reference frame as shown in Figure 4.3. Two of the eight cases are zero vectors and hence represented near the origin. An average vector is defined during a switching period. The average vector is assumed to be constant during the switching period and it defines the fundamental nature of the angle and phase of the three converter voltages. A high rate of switching frequency of the vectors is generally necessary to obtain the desired power transfer mechanism; hence the area between the vectors is broadly divided into twelve sectors.

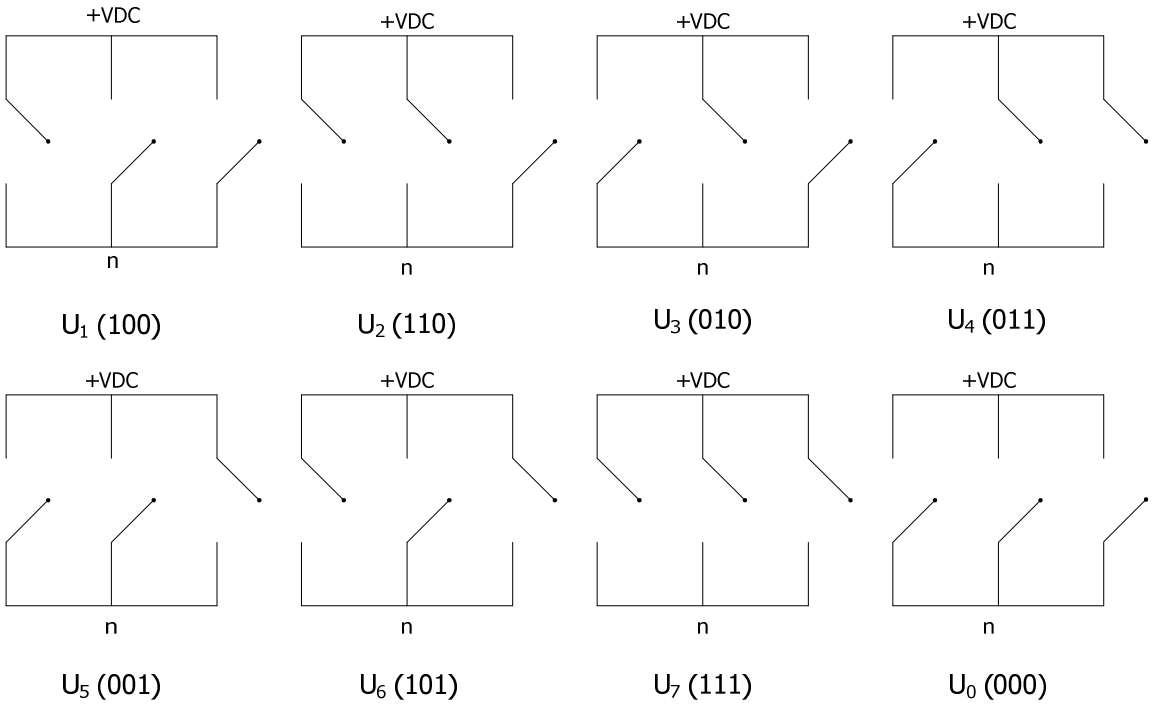


Figure 4.2. PWM Converter switching states

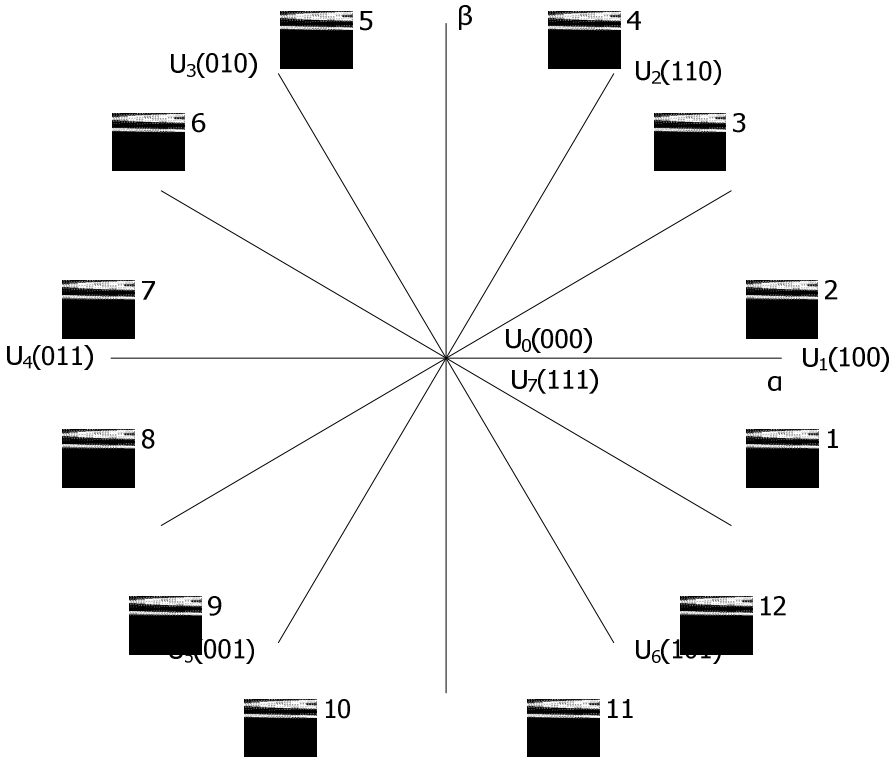


Figure 4.3. Voltage vector plane divided into 12 sectors

The magnitude and angle of the voltage vector can either be increased or decreased by applying appropriate vectors in the α-β plane. Consider for example that the average value of the converter voltage vector falls in sector 2 in a given time period. The magnitude of the vector in this sector can be increased by applying vectors $U_6$, $U_2$ and $U_1$ and can be decreased by applying vectors $U_3$, $U_4$ and $U_5$. Similarly the angle of the voltage can be changed by either advancing the vector in clockwise direction by applying $U_1$, $U_6$ and $U_5$ or in anticlockwise direction by applying $U_2$, $U_3$ and $U_4$. Zero vectors $U_0$ and $U_7$ neither change the magnitude nor angle but hold the vector at the same position in real time. Hence an appropriate selection of the vector in a given sector is necessary to change the magnitude and angle of the converter voltage.

The instantaneous real and reactive power, under the assumption of negligible series resistance, flowing between the source or line bus and the converter bus in Figure 4.3, is given in (33) and (34).

$$p = \frac{|v| * |v_1|}{X_L} \sin(\delta) \tag{33}$$

$$q = \frac{|v_1|}{X_L} (|v| * \cos(\delta) - |v_1|) \tag{34}$$

$\delta$ is the angle between the line and the converter voltages. As the line voltage is predetermined, the power flow can be varied using the converter voltage. From (33) it is observed that the real power can be increased or decreased either by increasing or decreasing $\delta$ or the magnitude of the converter voltage. It is important to consider that the effect of change in the angle would be significantly more than the change in the magnitude as the former is a sinusoidal function whereas the latter is just a linear function. Hence appropriate application of zero vectors also change the angle $\delta$. The

reactive power is predominantly determined by the magnitude of the converter voltage as it is proportional to the square of the magnitude.

An optimal switching table based on the above analysis as employed by [14] and [15] is used for the instantaneous control of real and reactive power. The switching vectors for different sectors are shown in Table 4.1. While applying the zero vector a choice between $U_0$ (000) or $U_7$ (111) depends on the converter legs switching during change of states.

Table 4.1. Optimal switching table for voltage source converter (↑ increase, ↓ decrease)

| P / Q | ↑ / ↓ | ↑ / ↑ | ↓ / ↓ | ↓ / ↑ |
|---|---|---|---|---|
| Sector 1 | $U_6$ (101) | $U_7$ (111) | $U_6$ (101) | $U_1$ (100) |
| Sector 2 | $U_7$ (111) | $U_7$ (111) | $U_1$ (100) | $U_2$ (110) |
| Sector 3 | $U_1$ (100) | $U_0$ (000) | $U_1$ (100) | $U_2$ (110) |
| Sector 4 | $U_0$ (000) | $U_0$ (000) | $U_2$ (110) | $U_3$ (010) |
| Sector 5 | $U_2$ (110) | $U_7$ (111) | $U_2$ (110) | $U_3$ (010) |
| Sector 6 | $U_7$ (111) | $U_7$ (111) | $U_3$ (010) | $U_4$ (011) |
| Sector 7 | $U_3$ (010) | $U_0$ (000) | $U_3$ (010) | $U_4$ (011) |
| Sector 8 | $U_0$ (000) | $U_0$ (000) | $U_4$ (011) | $U_5$ (001) |
| Sector 9 | $U_4$ (011) | $U_7$ (111) | $U_4$ (011) | $U_5$ (001) |
| Sector 10 | $U_7$ (111) | $U_7$ (111) | $U_5$ (001) | $U_6$ (101) |
| Sector 11 | $U_5$ (001) | $U_0$ (000) | $U_5$ (001) | $U_6$ (101) |
| Sector 12 | $U_0$ (000) | $U_0$ (000) | $U_6$ (101) | $U_1$ (100) |

Alternative to (33) and (34) the three phase instantaneous real and reactive power is estimated by the scalar and vector product of the instantaneous voltages and currents as in (35) and (36), respectively.

$$p = \left(v_a i_a + v_b i_b + v_c i_c\right) \tag{35}$$

$$q = \frac{1}{\sqrt{3}}\left\{i_a\left(v_b - v_c\right) + i_b\left(v_c - v_a\right) + i_c\left(v_a - v_b\right)\right\} \tag{36}$$

The commanded real and reactive powers are compared with the estimated power as in (35) and (36). The difference or error is digitized using a delta modulation as follows:

For reactive power: $d_q = 1$ for $q < q_{ref}$ $d_q = 0$ for $q > q_{ref}$

Similarly for active power: $d_p = 1$ for $p < p_{ref}$ $d_p = 0$ for $p > p_{ref}$

The vector position is estimated using the angle of the source voltage in the stationary reference frame (37). A voltage sensorless approach of similar topology is discussed by [14], [15], [35] and [36]. These digitized outputs along with the vector position as in (37) are fed to the optimum switching table. The vector position ($\theta$) is calculated in the range of – 180º to 180º and the situation of $V_\alpha = 0$ is eliminated by using the abc to αβ reference frame block in PLECS® block set.

$$\theta = \tan^{-1}\left(\frac{V_\beta}{V_\alpha}\right) \tag{37}$$

## 4.3 SIMULATION OF VOLTAGE SOURCE CONVERTER USING DPC

The simulation of the DPC for the voltage source converter is carried out in Matlab Simulink® using PLECS blockset similar to that of the conventional converter as in Figure 2.4 except the control is replaced by DPC. The simulation control diagram is shown in Figure 4.4.

To test the general operation as well as a ride-through for a voltage dip, the simulation was carried out for a second with a voltage dip in phase A from 0.3 s to 0.8 s. Figures 4.5 and 4.6 show the simulation results of the DPC strategy and Figure 3.7 shows the same for the conventional controller.

Under normal conditions, the DPC behaves similarly to that of the conventional controller. Comparing the DC link voltage, real and reactive powers produced by the two controllers, it may be observed that the DPC has lesser DC link voltage and power oscillations in normal operation as well as during the voltage dip. In the conventional controller, the oscillations in reactive power increase to two-fold during the fault whereas in DPC there is no variation, hence the stiff control. The DPC acts faster to a sudden disturbance with less overshoot compared to the conventional control and maintains a smooth control even in case of a disturbance.

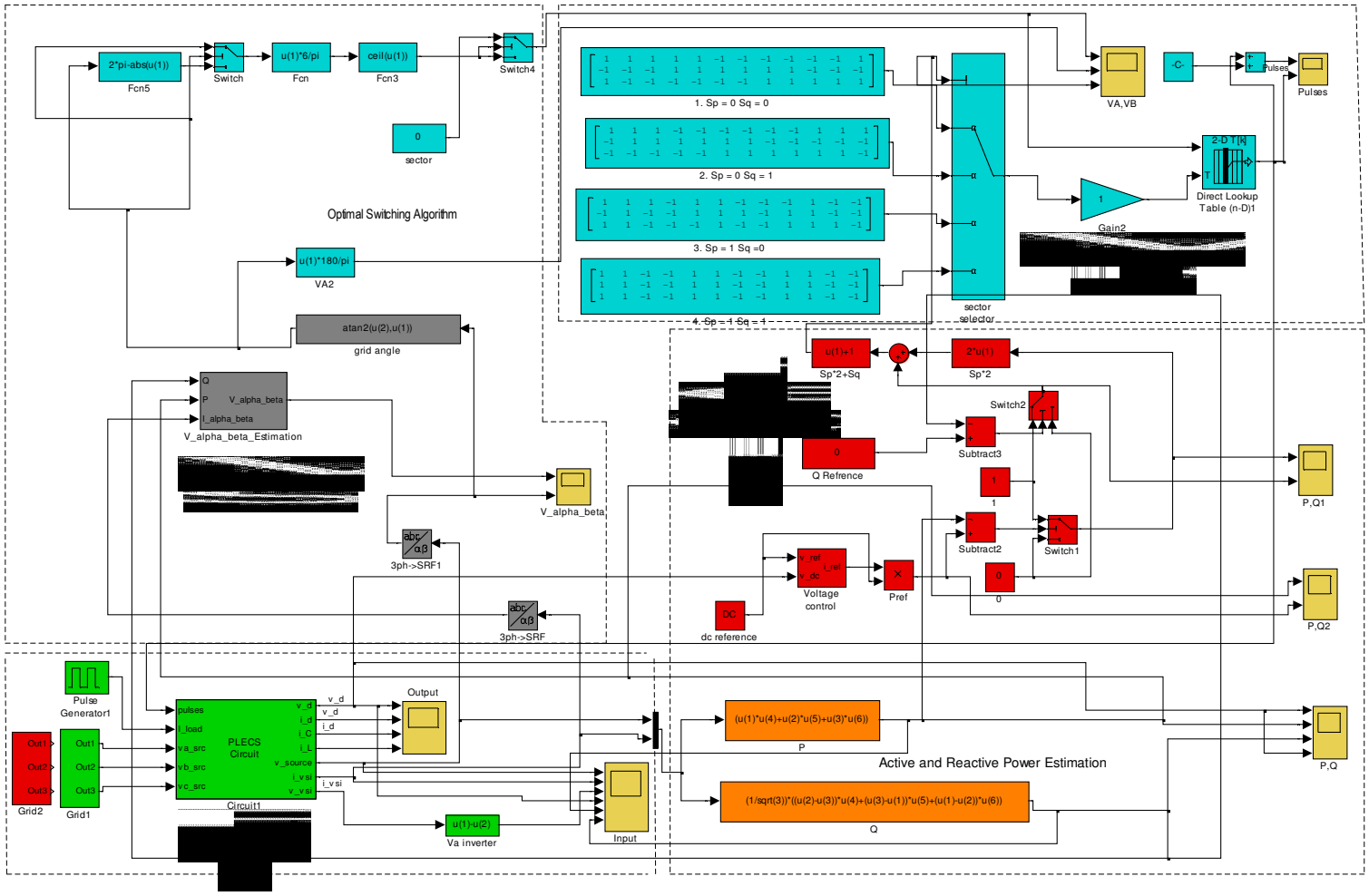


Figure 4.4. DPC structure for voltage source converter

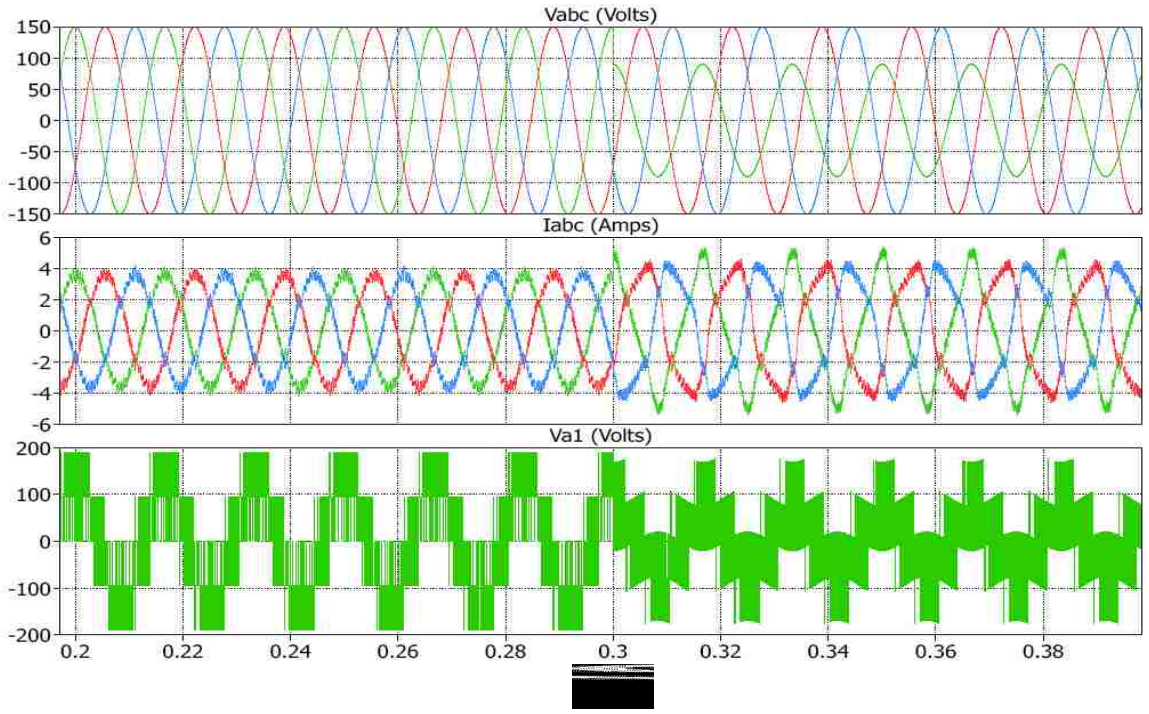


Figure 4.5. VSC using DPC for a voltage dip of 60% (from top source voltages, source currents and converter voltage) - zoomed between 0.2 s to 0.4 s

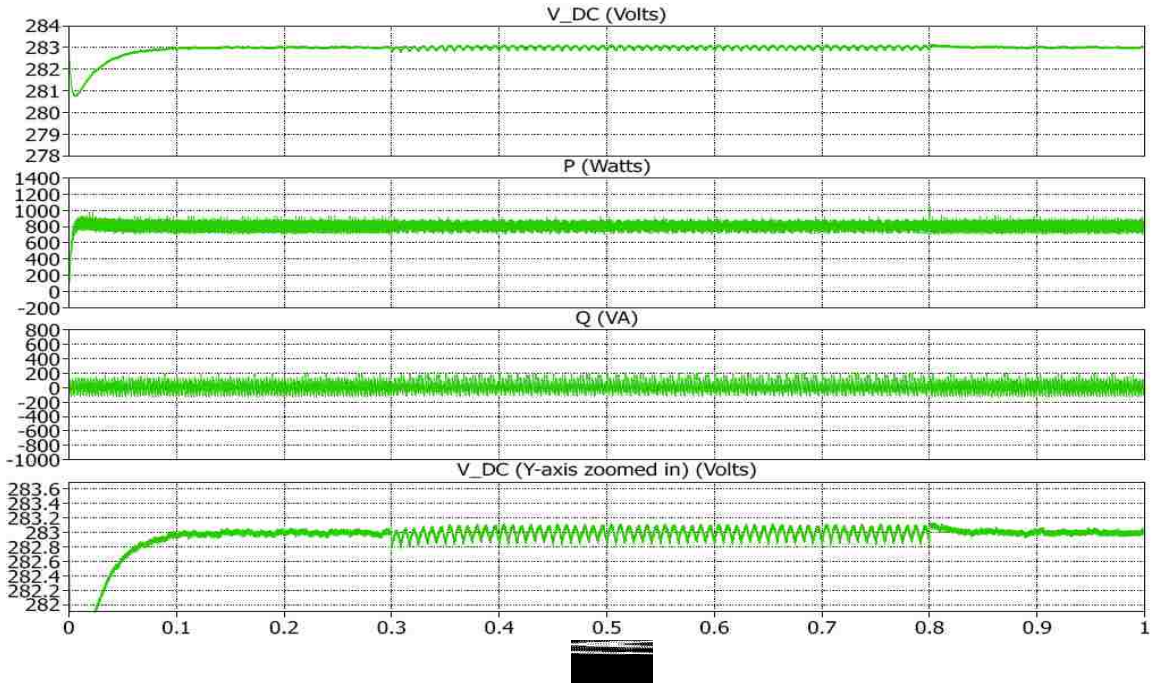


Figure 4.6. Simulation of the VSC using DPC for a voltage dip of 60% (from top DC-link voltage real power, reactive power DC-link voltage Y-axis zoomed)

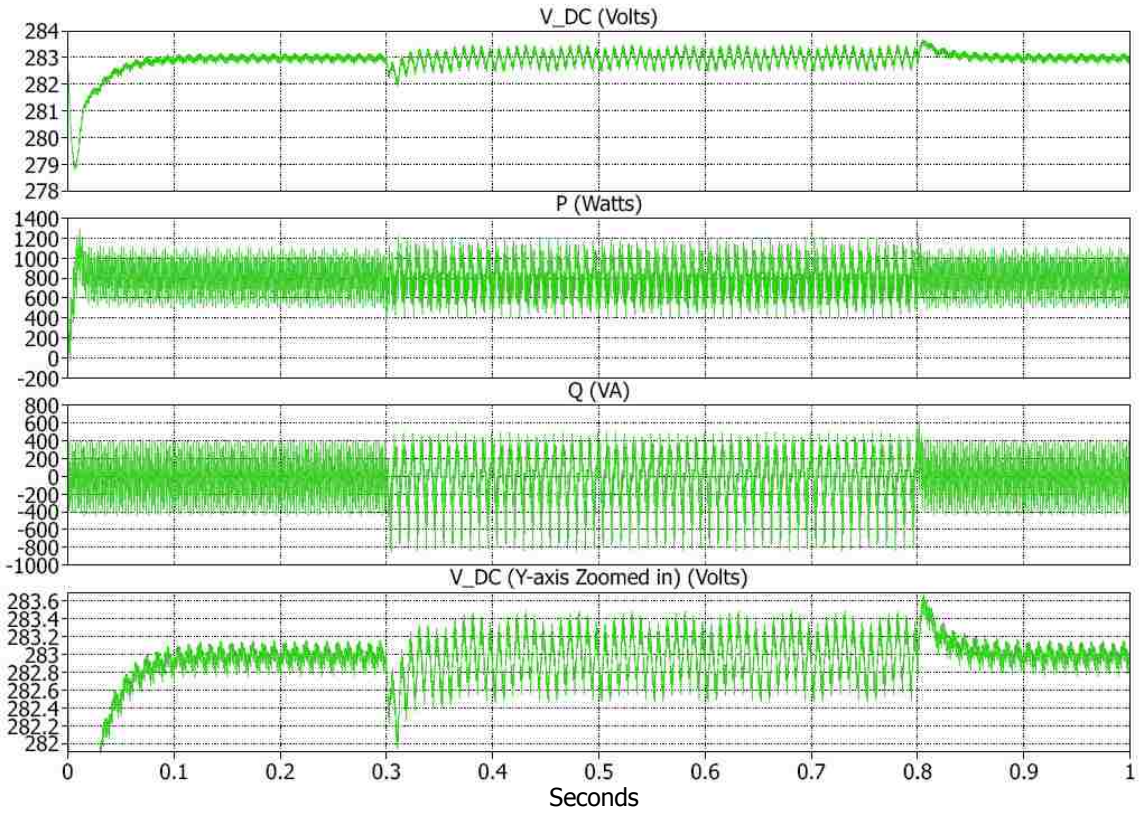


Figure 4.7. Simulation of conventional controller for voltage dip of 60% (from top DC-link voltage real power, reactive power DC-link voltage Y-axis zoomed)

To compare the conventional controller, sequence controller and the DPC, a simulation for imbalance in the system that lasts all the time is carried out in Figures 4.8 and 4.9. The real and reactive powers and the initial transient are the least in the case of the DPC. Initial settling time and peak overshoot of the DPC and conventional controller are almost the same and less than those for the sequence controllers. DPC lacks direct control over the current during imbalance. Hence, in DPC the currents are characterized by high distortion as seen in Figure 4.9 whereas sequence controllers offer smooth currents. A modified DPC approach is used to reduce the current harmonics and is discussed in the next section.

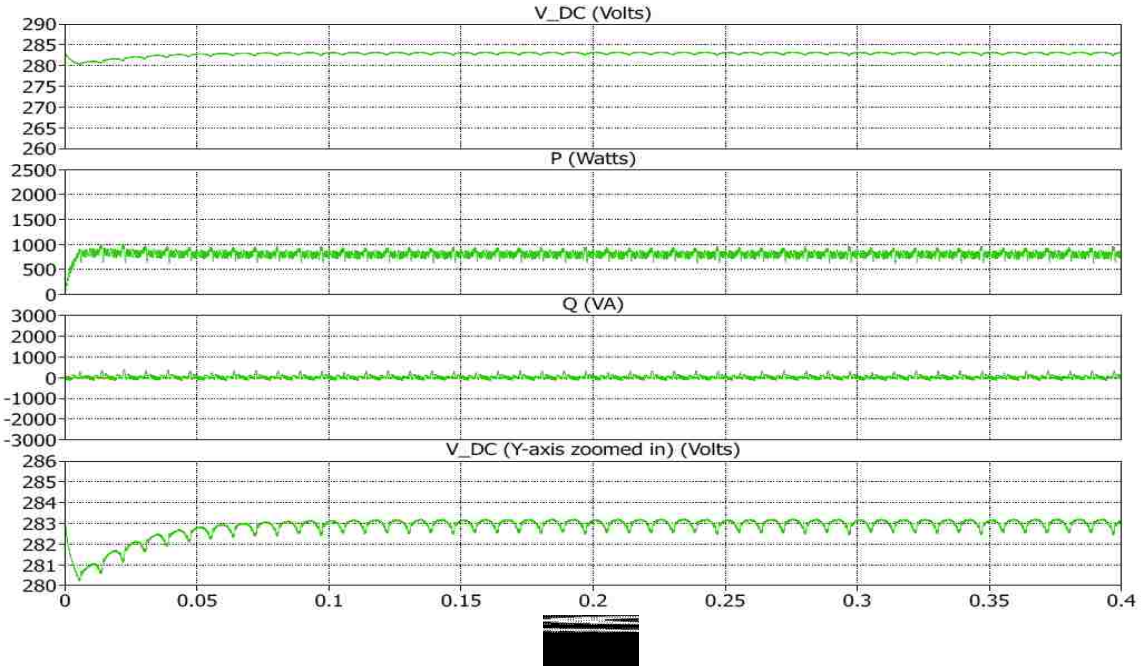


Figure 4.8. Voltage imbalance simulation of VSC for DPC (from top DC link voltage, real power, reactive power and DC link voltage Y-axis zoomed)

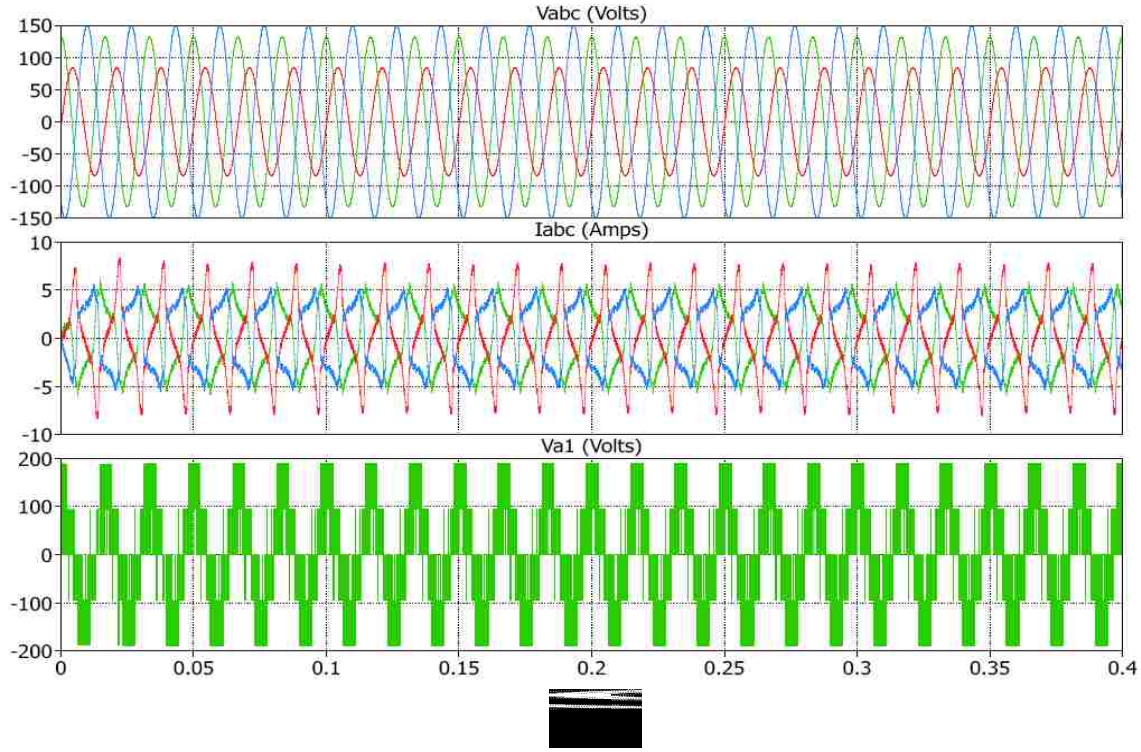


Figure 4.9. Voltage imbalance simulation of VSC using DPC (from top source voltage, source currents and converter voltage)

Table 4.2 shows the comparison of peak-to-peak ripple in DC link voltage, real power and reactive power of the conventional controller, sequence controller and the DPC. The DPC has similar oscillation in the DC link voltage but lesser oscillations in the real and reactive powers compared to that of the sequence controller. Hence DPC offers the advantages of sequence controller with fairly faster response and simple control algorithm.

Table 4.2. Comparison of ripple in DC link Voltage, real power and reactive power for voltage imbalance

| Control<br>Min/Max | DC Link Voltage<br>(283V) | Real Power<br>(800 Watts) | Reactive Power<br>(0VA) |
|---|---|---|---|
| Conventional | 281/285 | 0/1600 | -500/-3000 |
| Sequence | 282.6/283.2 | 500/1100 | -500/500 |
| DPC | 282.4/283.2 | 750/850 | -100/100 |

The DPC is dependent mainly on the sampling and actuation frequency as the comparators update the real and reactive powers once in a time period. Hence, an optimal frequency needs to be chosen so that the DPC maintains the control of real and reactive powers. Figure 4.10 shows the simulation of the DPC in normal operation at 5 kHz sampling frequency compared to the 20 kHz frequency with which the earlier simulations are carried out. It can be seen that the DC link voltage, the real power and the reactive power have very high oscillations than the simulation at higher frequency. Choosing very high frequency poses limitations on implementation as it consumes more

processing time due to more calculations. Hence, an optimal frequency needs to be considered while designing the controller.

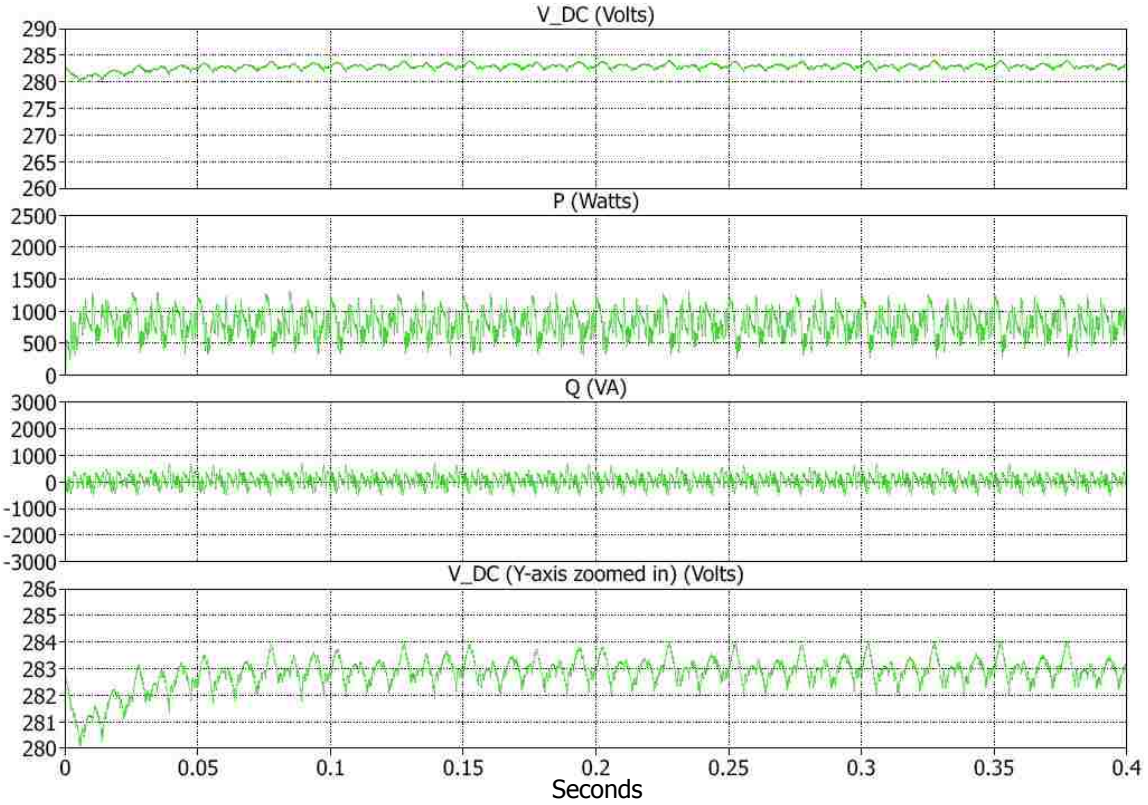


Figure 4.10. Simulation of the voltage source converter using DPC for at 5 KHz (from top DC-link voltage, real power and reactive power)

## 4.4 MODIFIED DIRECT POWER CONTROL

In order to decrease the distortion in the currents of the DPC, a hybrid approach similar to that presented in [39] is proposed. In this approach the real and reactive power references for the DPC are appended with powers due to the unbalance as discussed in section three (30)-(33). Neglecting the negative sequence current

components as they contribute for higher oscillation in power, the real and reactive power equations due to the imbalance are modified as in (38) and (39)

$$P_{imb} = v_{dne} i_{dpe} + v_{qne} i_{qpe} \tag{38}$$

$$Q_{imb} = v_{dne} i_{qpe} - v_{qne} i_{dpe} \tag{39}$$

The partial simulation diagram showing the addition of unbalanced power commands is shown in Figure 4.11. The voltage and current imbalances are calculated using notch filters for positive and negative sequence separation as in section 3. The modified DPC is simulated for the same 60% voltage dip in the input as for the normal DPC. The simulation results are shown in Figure 4.12. and 4.13. Table 4.3 shows the comparison of peak-to-peak ripple DC link voltage, real power and reactive powers of the 60% voltage dip. The source currents are less distorted than the normal DPC due to added unbalance in real and reactive power compensation. The trade-off is that the DC link voltage, real power and reactive power have slightly higher oscillations than the normal DPC but have lesser oscillations than the conventional current control technique. Imbalance power compensation retains the same settling time and overshoot as that of the normal DPC as there is no addition of new controllers. Four new notch filters are added to the circuit which adds computational complexity. Hence a compromise between current distortion and power oscillations need to be considered while choosing a normal DPC or a modified DPC.

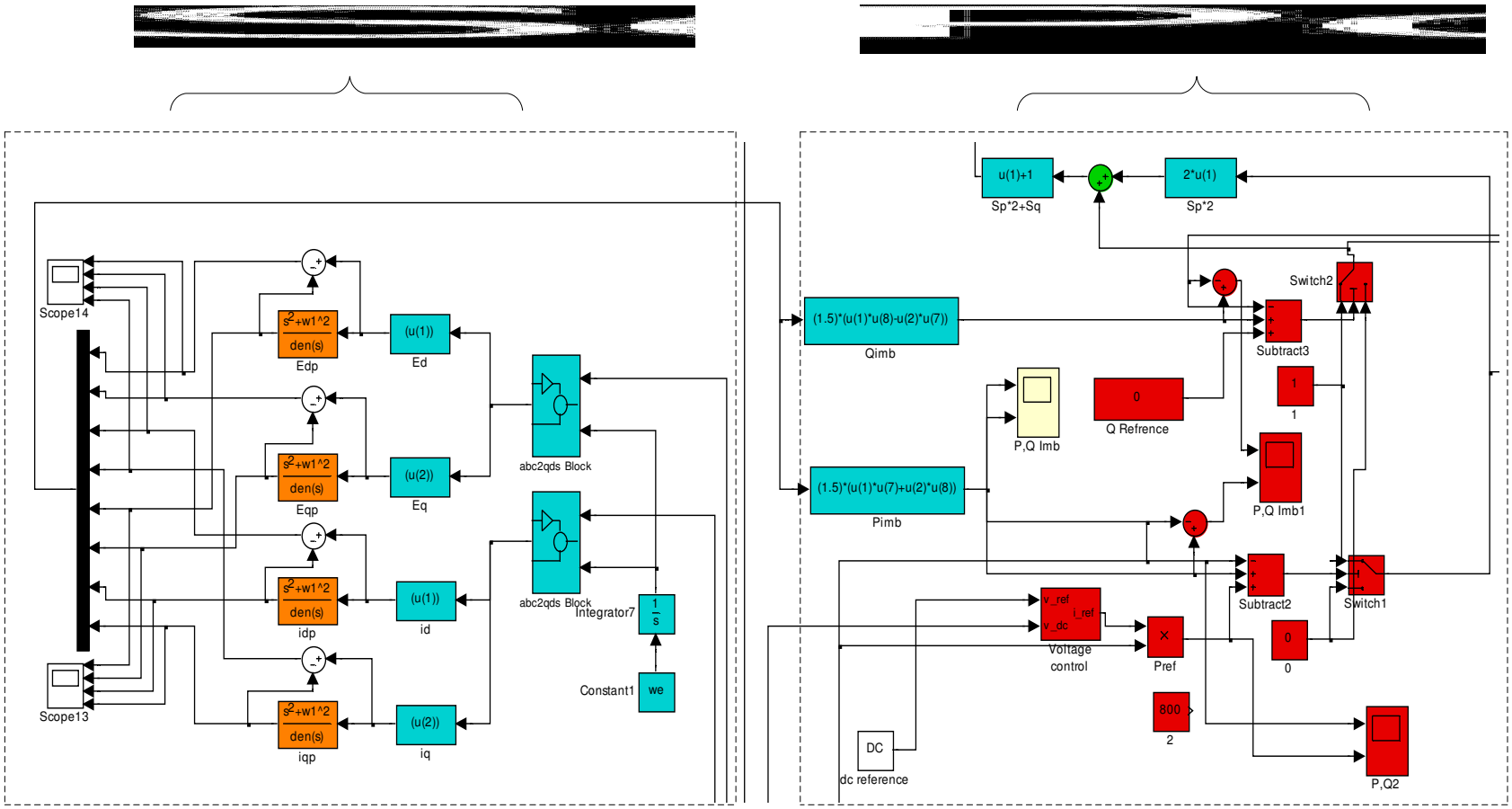


Figure 4.11. Partial simulation diagram for the modified DPC showing unbalanced powers

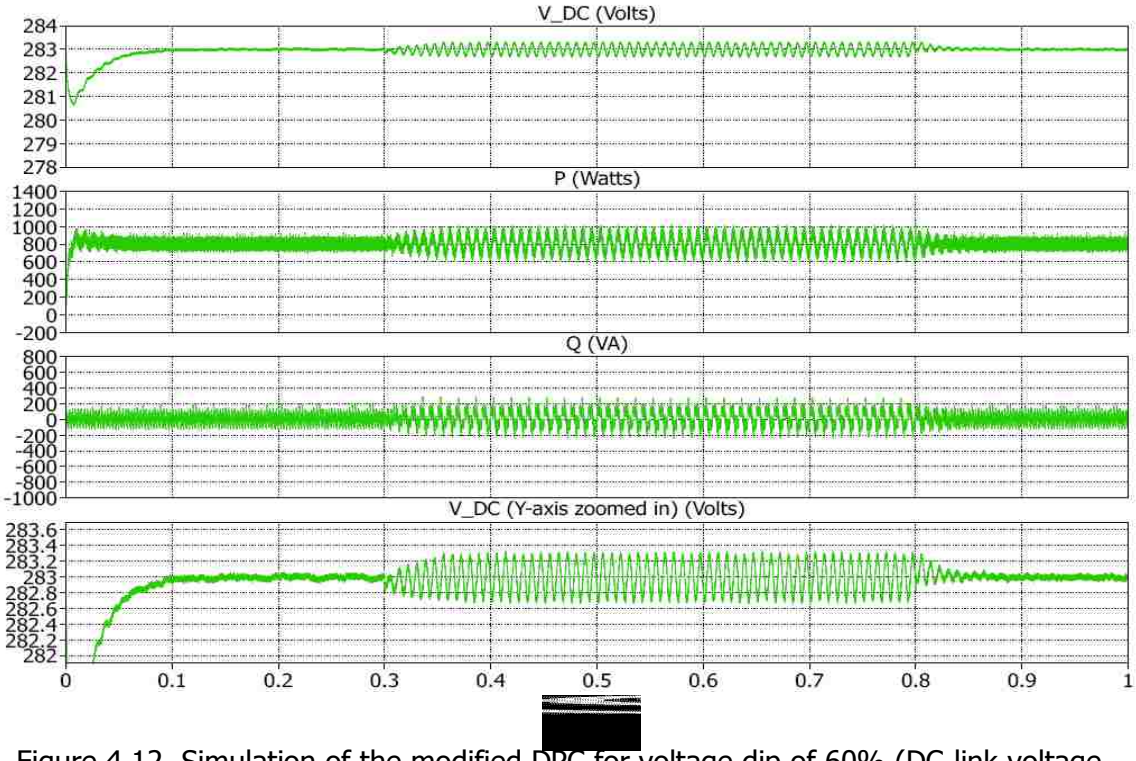


Figure 4.12. Simulation of the modified DPC for voltage dip of 60% (DC-link voltage - Vm1, real power (P) - Signal and reactive power (Q) - Signal)

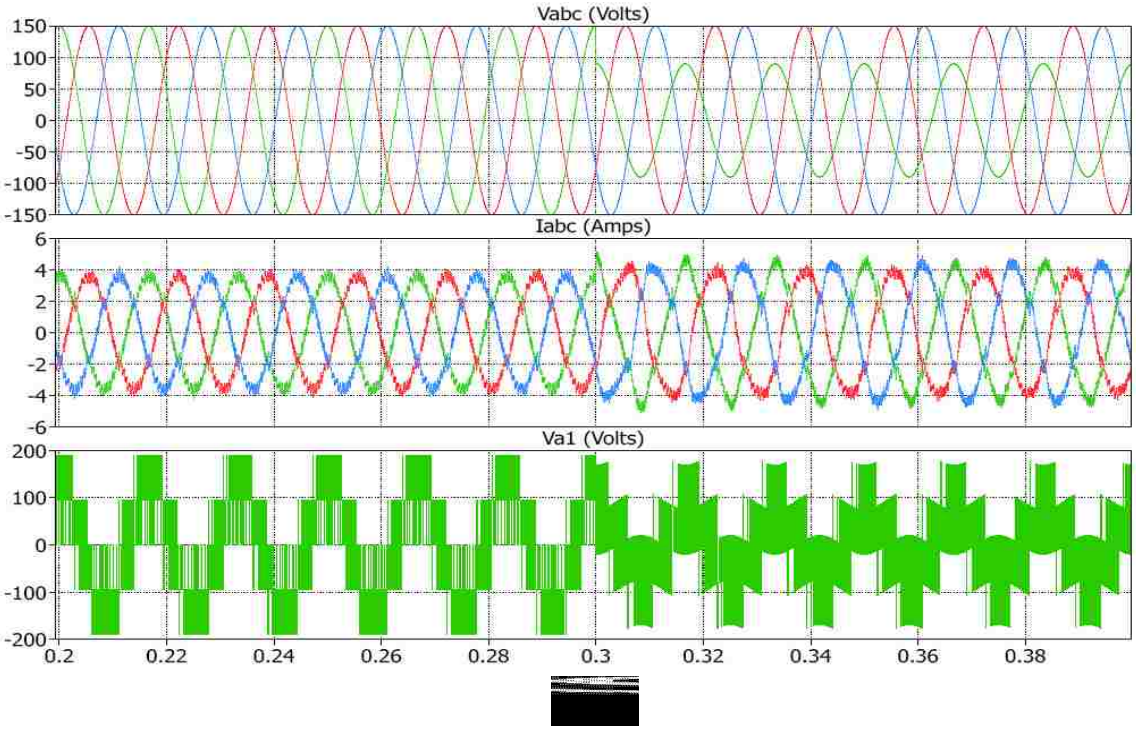


Figure 4.13. Simulation of the modified DPC for voltage dip of 60% (from top source voltage, source currents and converter voltage). - zoomed between 0.2 s to 0.4 s

Table 4.3. Comparison of ripple in DC link Voltage, real power and reactive power for 60% voltage dip

| Control Min/Max | DC Link Voltage (283V) | Real Power (800 Watts) | Reactive Power (0VA) |
|---|---|---|---|
| Conventional | 282.4/283.4 | 500/1100 | -800/400 |
| DPC | 282.8/283.1 | 730/870 | -100/100 |
| MDPC | 282.4/283.2 | 600/1000 | -200/200 |

## 4.5 DPC BASED ROTOR SIDE CONTROL

Conventional stator flux orientation control of the rotor side converter depends upon the accuracy of computing the stator flux vector and the rotor position, which in turn needs the parameters of the induction machine. A similar approach used for the grid side converter is also employed for control of the rotor side converter. This method is a modification of Direct Self Control (DSC) [40] or Direct Torque Control (DTC) [41-43] which uses a hexagonal or a circular trajectory for the stator flux.

DSC or DTC uses two delta modulation controllers - one for the torque control and the other for the flux control to command the switching states of the inverter. This method is computationally simple and does not need all the machine parameters. In DPC the flux and torque loops are replaced by the stator active power and reactive power loops, thus enabling the direct control of stator active and reactive powers.

Conventional current control employs a stator flux orientation reference frame as it offers a decoupled control over rotor torque and excitation which are directly dependent on active and reactive powers respectively. Hence a direct power control scheme using stator flux vector position [44] for selecting voltage vectors is employed.

The value of the stator flux is estimated first and is then referred to the rotor reference frame using reference frame transformation and rotor speed. Proper selection of the voltage vectors determines the magnitude and angle of rotor voltage. Neglecting rotor resistance, the rotor flux vector is a direct integral of rotor voltage.

By varying the angle (between the stator and rotor flux) and magnitude of the rotor flux, the real and reactive powers of the DFIG can be controlled directly [18]. This method eliminates the difficulties associated with measuring the rotor flux as stator flux estimation is only necessary. The only machine parameters needed for stator flux estimation are stator resistance; hence, this control is independent of most of the machine parameters.

The effect of zero vectors for the rotor side converter is indeterminate and hence is excluded. The vector plane is divided into six sectors rather than twelve because zero vectors are not taken into account. Each sector span $\pm$ 30 deg from each flux vector, thus covering 360 degrees with the six sectors as shown in Figure 4.14. A simple two level delta modulation as discussed for VSC is used for obtaining the digitized power error commands.

The selection of the vectors is similar to that employed for the voltage source converter where the rotor flux is varied instead of voltage to control real and reactive powers. The zero vectors have slightly different behavior depending on subsynchronous or supersynchronous modes [18]. Hence the use of zero vectors is eliminated while selecting the optimal switching vectors shown in Table 4.4.

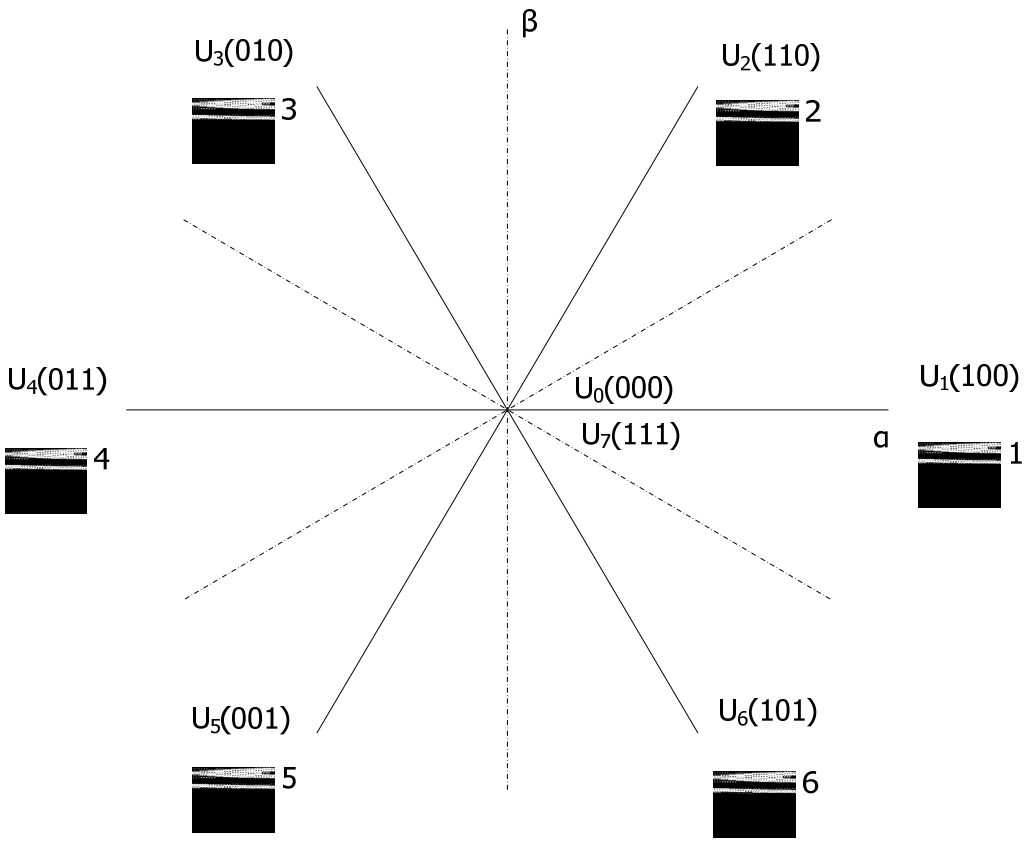


Figure 4.14. Stator flux vector plane divided into six sectors

Table 4.4. Optimal switching table for rotor side converter of DFIG (↑increase, ↓ decrease)

| P / Q | ↑ / ↓ | ↑ / ↑ | ↓ / ↓ | ↓ / ↑ |
|---|---|---|---|---|
| Sector 1 | $U_6$ (101) | $U_5$ (001) | $U_2$ (110) | $U_3$ (010) |
| Sector 2 | $U_1$ (100) | $U_6$ (101) | $U_3$ (010) | $U_4$ (011) |
| Sector 3 | $U_2$ (110) | $U_1$ (100) | $U_4$ (011) | $U_5$ (001) |
| Sector 4 | $U_3$ (010) | $U_2$ (110) | $U_5$ (001) | $U_6$ (101) |
| Sector 5 | $U_4$ (011) | $U_3$ (010) | $U_6$ (101) | $U_1$ (100) |
| Sector 6 | $U_5$ (001) | $U_4$ (011) | $U_1$ (100) | $U_2$ (110) |

The complete DFIG model using both rotor side and grid side converters are now simulated using DPC. The DFIG circuit model including the back-to back converters are simulated using the PLECS block set as shown in Figure 4.15. The grid side converter uses the same control discussed earlier in this section. The stator and rotor side converter control diagram using DPC in Matlab Simulink® is shown in Figure 4.16.

The DFIG is modeled to take mechanical speed as its input rather than mechanical torque, as DFIGs are wind-speed driven for wind turbine applications. DPC offers the advantage of simple and fast control as this operates directly on the stator active and reactive powers. This system is simple and is easily tune as it uses only one PI controller – that for controlling the DC link voltage.

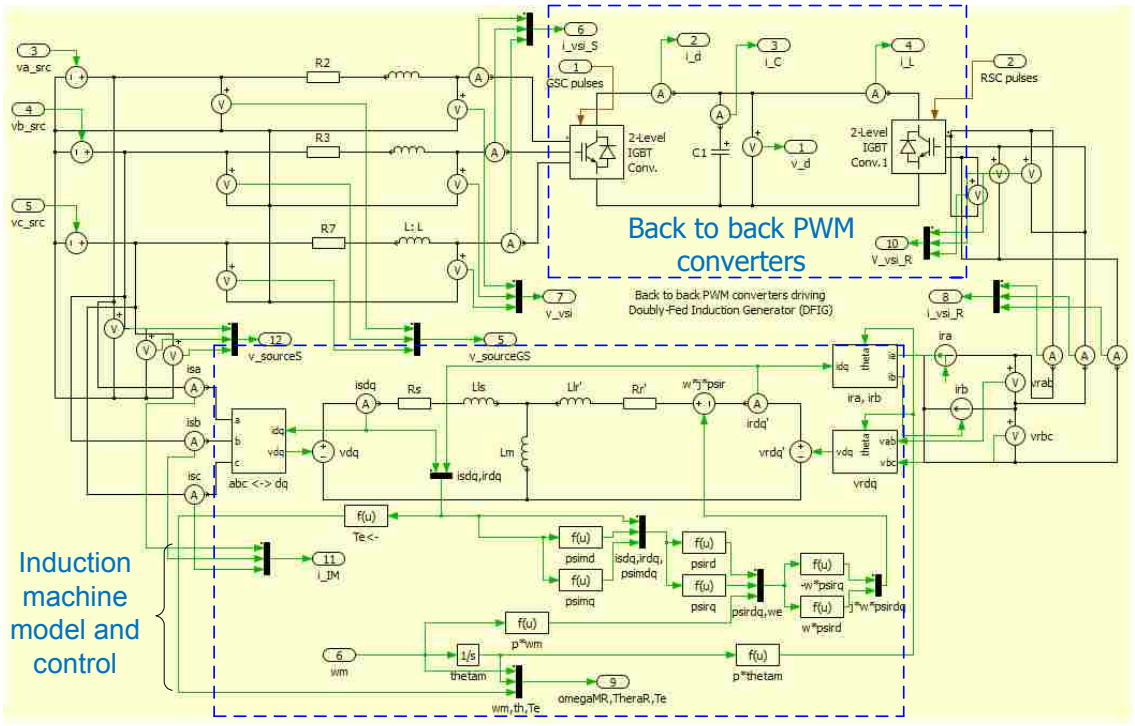


Figure 4.15. DFIG circuit diagram including the back-to-back converters

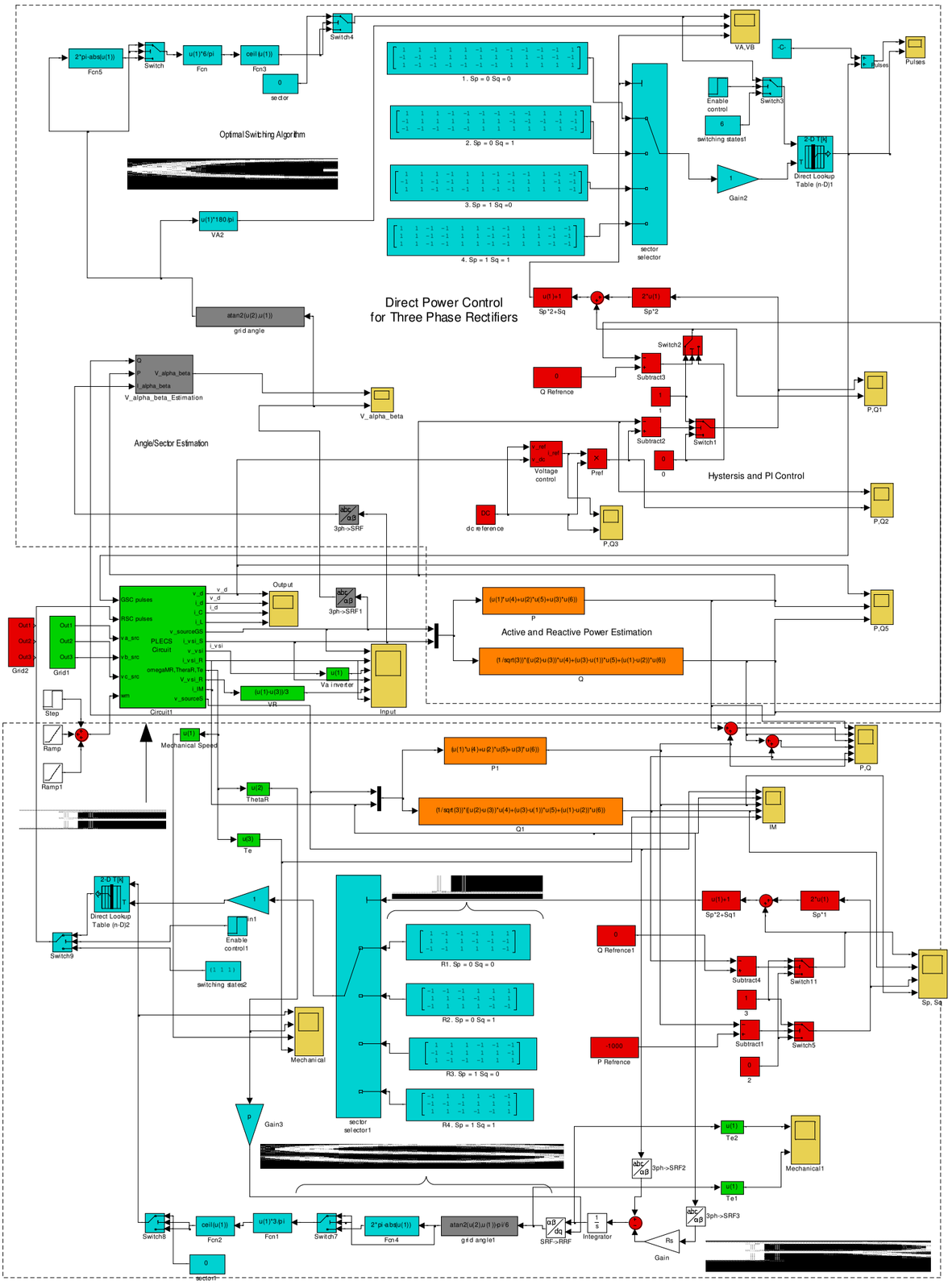


Figure 4.16. DPC structure of the grid side and rotor side converter of DFIG

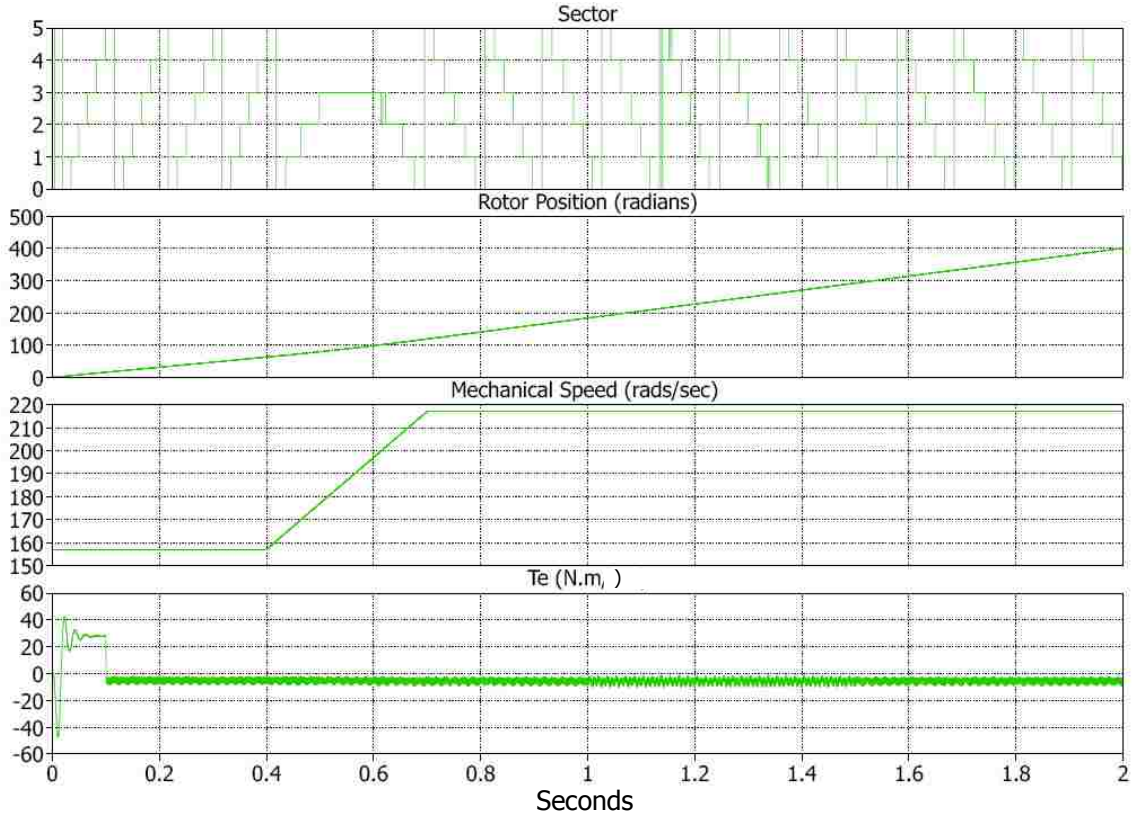


Figure 4.17. DFIG simulation results (from top sector, rotor position, mechanical speed and electrical torque)

In supersynchronous operation, both the stator and the rotor of the DFIG produce real power; hence during the speed change the rotor side power (Figure 4.18 and Figure 4.19) and the dc link current through the grid side converter shifted from positive to a negative value signifying the power change as seen in Figure 4.20. The total power produced by the DFIG increases as the mechanical input increased; this is observed from the total powers shown in Figure 4.19. Hence the DPC is capable of handling the speed change with smooth transition. The power scenario form the subsynchronous to supersynchronous operation is shown in Table 4.5

A voltage dip of 0.6 in 'A' phase is simulated from 1 s to 1.5 s. Fewer oscillations are seen in DC link voltage, currents and real power of the grid. There is not a considerable amount of change in the total power (Figure 4.18) delivered by the system. The rotor side currents (Figures 4.21 and 4.22) have oscillations of higher harmonics whereas the grid side currents have some distortion. The reactive power of the system stays as commanded even during the disturbance.

The DPC is capable of handling the system and grid disturbances. The controllers have fast response to change in speed and grid voltage. The real power through the rotor side of the converter can be limited according to the system rating by commanding the correct amount of stator power on the rotor side converter.

Table 4.5. Stator, rotor and total real and reactive powers for subsynchronous and supersynchronous operations

| Speed | subsynchronous | supersynchronous |
|---|---|---|
| Stator(P) | -1000 | -1000 |
| Rotor (P) | 200 | -200 |
| Total (P) | -800 | -1200 |
| Stator(Q) | 0 | 0 |
| Rotor (Q) | 0 | 0 |
| Total (Q) | 0 | 0 |

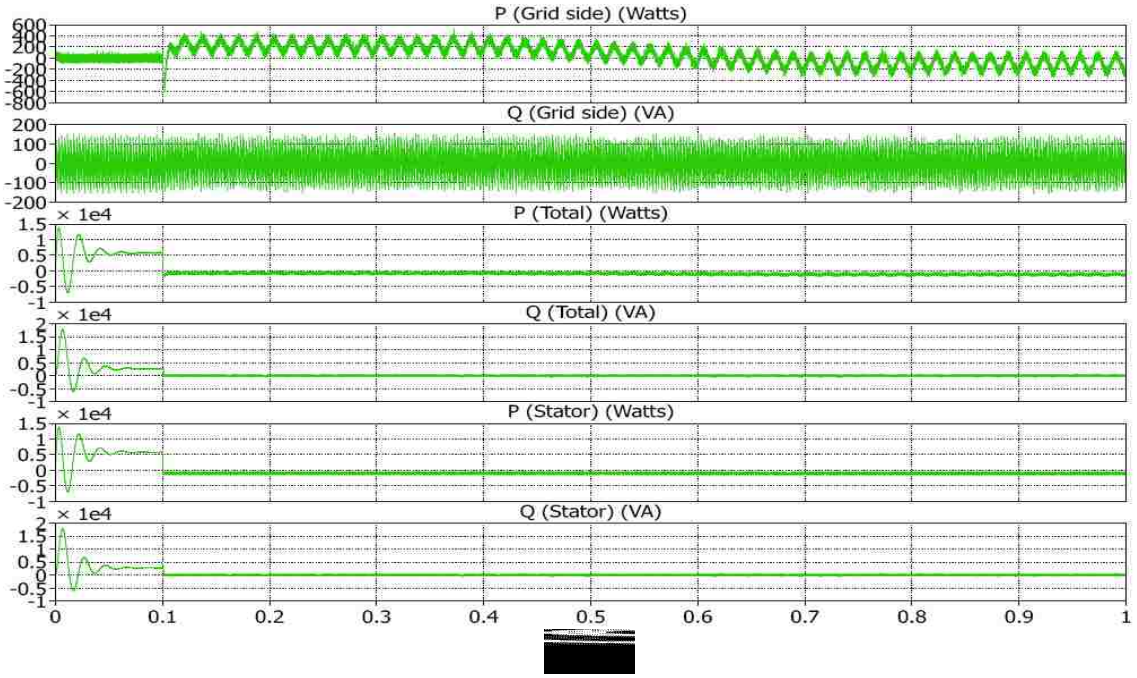


Figure 4.18. DFIG simulation results (from top grid side, total and stator side real and reactive powers)

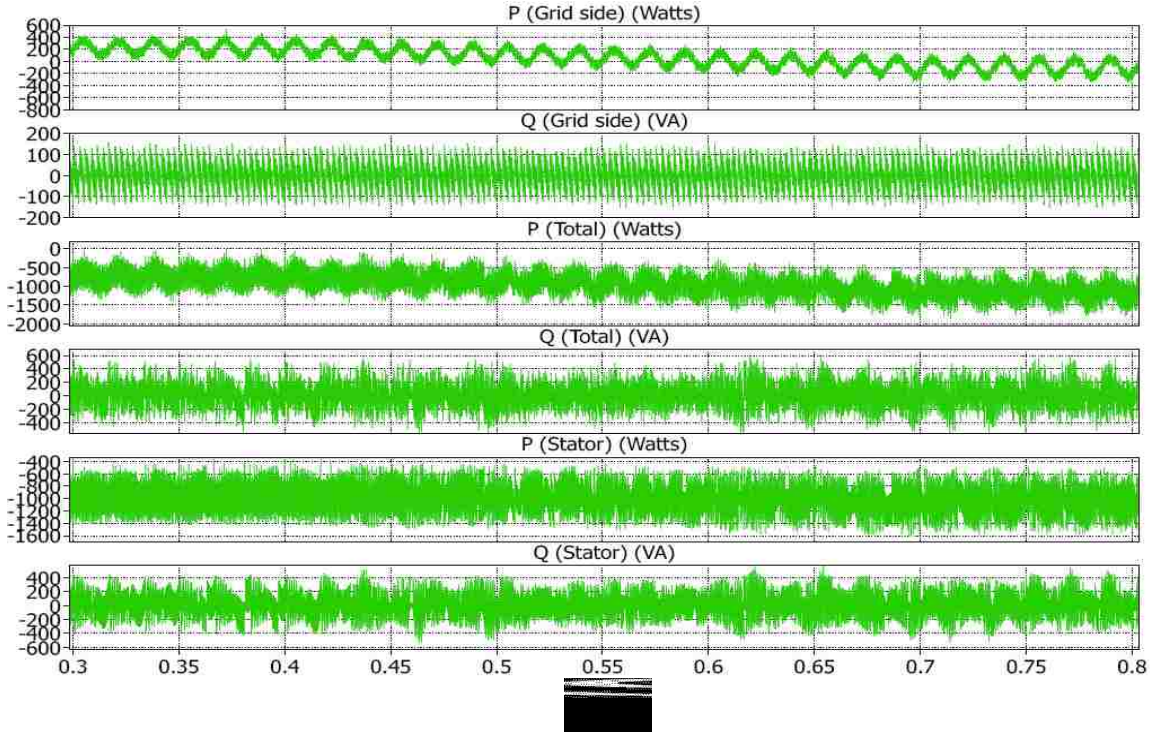


Figure 4.19. DFIG simulation results (from top grid side, total and stator side real and reactive powers)- zoomed in during ramp change in speed (0.3 s to 0.8 s)

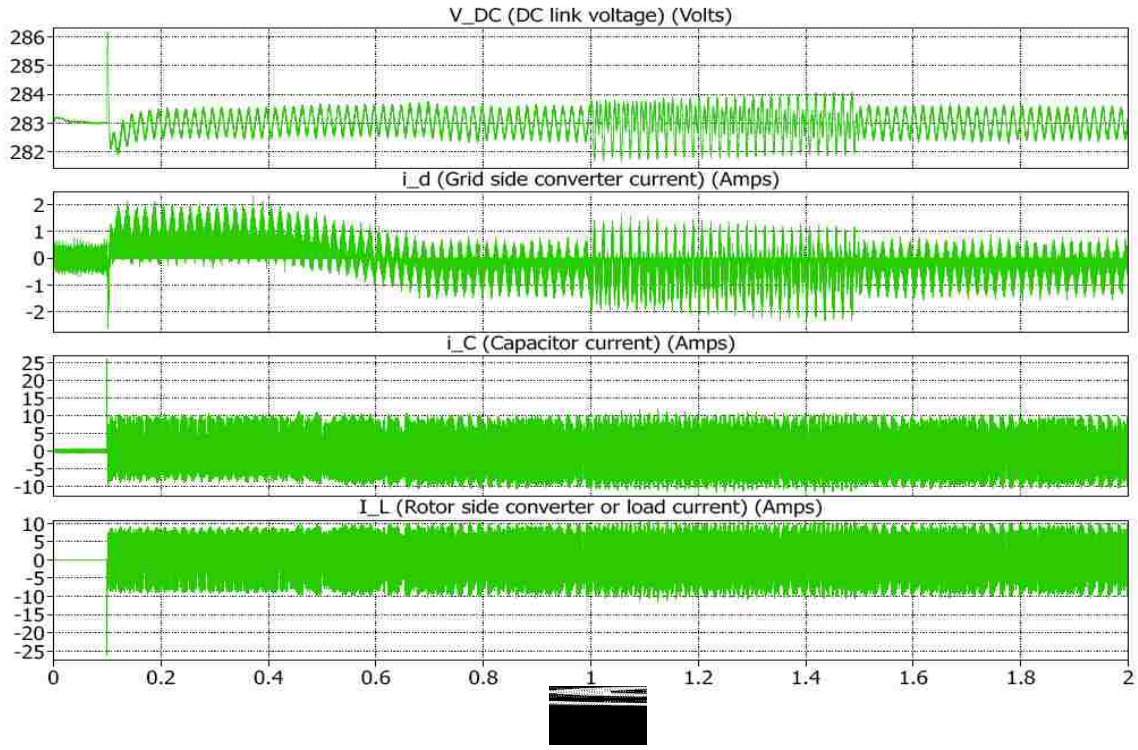


Figure 4.20. DFIG simulation results (from top DC link voltage, grid side converter current, capacitor current, rotor side converter current)

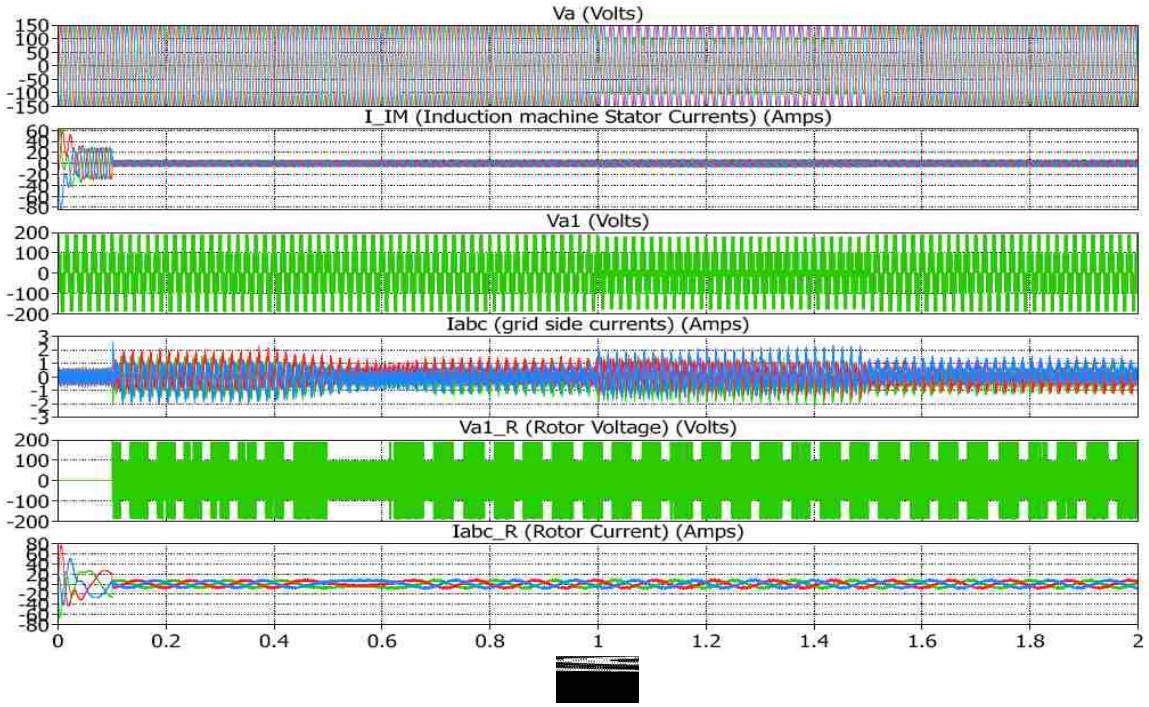


Figure 4.21. DFIG simulation results (from top source voltages, stator currents, grid side converter voltage, grid side converter currents, rotor voltage, rotor currents)

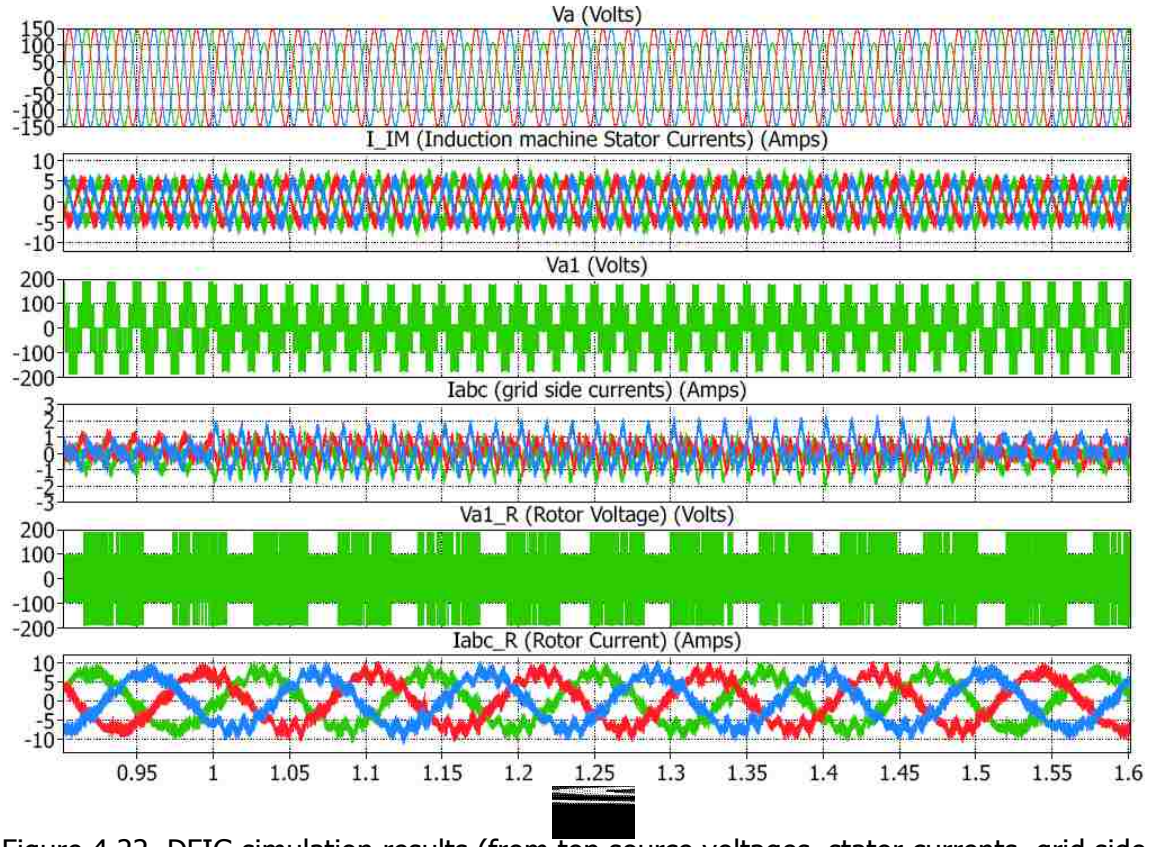


Figure 4.22. DFIG simulation results (from top source voltages, stator currents, grid side converter voltage, grid side converter currents, rotor voltage, rotor currents). - zoomed in during voltage dip (0.9 s to 1.6 s)

DPC requires high frequency of operation to update the real and reactive powers and the converters do not have a constant switching frequency due to delta type of control. During grid disturbances, high frequency oscillations and distortion crop up in the rotor and grid side converter currents. The rotor side converter which controls the power on the stator suffer less compared to the grid side converter that handles the power going through the rotor. As the rotor power is hardly 30% or less, this will not affect the overall system. The rotor side converter in the DPC does not have constant switching frequency as the switching states change according to the real and reactive power errors. A DPC scheme with constant switching frequency and improved transient

performance is proposed by [45]. In this method, the rotor voltage in a time period is estimated based on the stator flux, rotor position, active power and reactive power. Constant switching frequency is achieved using this voltage. A method to limit the rotor voltage is also proposed to improve the rotor transient performance. Modified DPC approaches as studied for the grid side converter are also developed for the rotor side converter in [46]. In this reference, a DPC+ algorithm is proposed in which the regular DPC power commands are appended with a variable factor of imbalance. This control achieves sinusoidal stator currents or constant active and reactive powers. The factor of imbalance is varied to achieve different control objectives from small steady state unbalances to temporary high unbalance factors created during sags.

## 4.6 SUMMARY

A novel technique called direct power control has been presented in detail for the back-to-back converters of the DFIG. It was shown that the DPC offers all the advantages of both conventional current controller and sequence controller using a simple control algorithm. The controllers used by the DPC are fast acting; hence they are suitable for sudden grid and wind disturbances. The DPC used only one PI controller to control DFIG compared to five PI controllers that is need for the conventional controller and seven or more PI controllers for the sequence controller, thus making it easy to set up and fine tune. DPC has less dependence on system parameters as it uses direct controllers using output powers. The drawback of the DPC is that it needs high switching frequencies to lower the harmonics and oscillations in the powers that increases the computational burden. The DPC turns out to be a viable solution for ride-through applications of DFIG-based wind turbines.

# 5. HARDWARE IMPLEMENTATION OF DPC

## 5.1 INTRODUCTION

The grid side converter using DPC was implemented on a printed circuit board (PCB) and is controlled by a Texas Instruments family Digital Signal Processor (DSP) TMS320F2812. The Line inductance and dc link capacitance were provided externally to the PCB. A three phase supply was fed through the circuit using an IPC [2]. The IPC was used to create sags in the input voltage to mimic actual conditions on the grid during disturbances. The purpose of the converter was to drive a resistive load on the DC side and maintain a stiff DC voltage. The DC capacitance is pre-charged using a DC power supply before the converter circuit is triggered. Over-voltage and over-current protection is provided to the circuit using MOV's and snubber capacitances. A schematic of the experimental setup is shown in Figure 5.1. The parameters used for practical implementation are tabulated in Table A.3 of Appendix A.

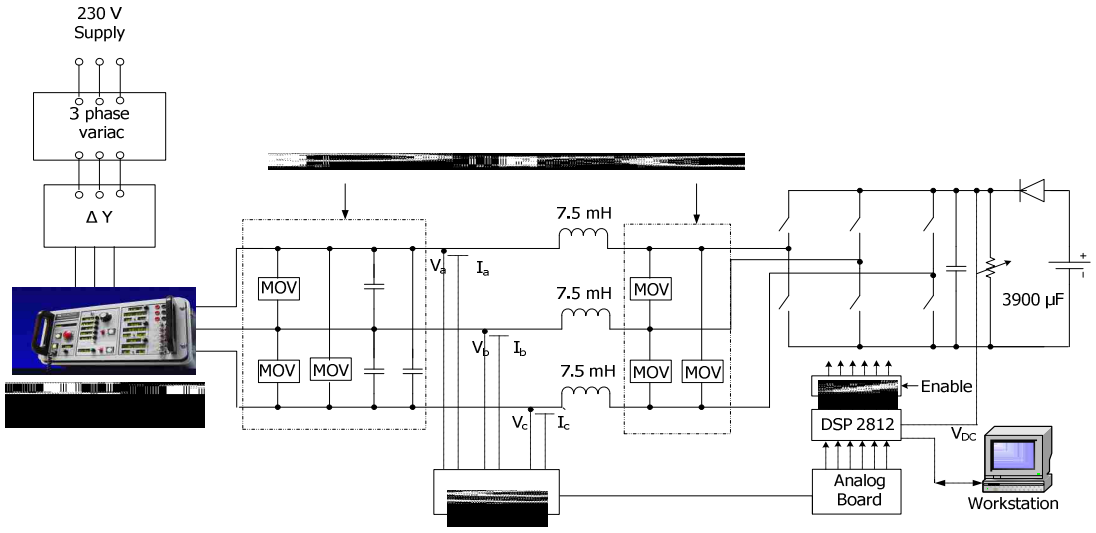


Figure 5.1. Circuit diagram of the converter for practical implementation

## 5.2 PCB DESIGN

The PCB consisting of an IGBT module, gate drivers, line current and dc voltage sensors was designed using Eagle® software. A six bridge IGBT SIP module CPV364MU was used for the main inverters. This IGBT Bridge was optimized for high operating frequency over 5kHz and was a fully isolated printed board mount package. The whole design is rated according to the IGBT module for a maximum of 600V across the collector and emitter of individual IGBT and a maximum continuous collector current of 6.8A at 100º C. The schematic of the six bridge IGBT module is shown in Figure 5.2.

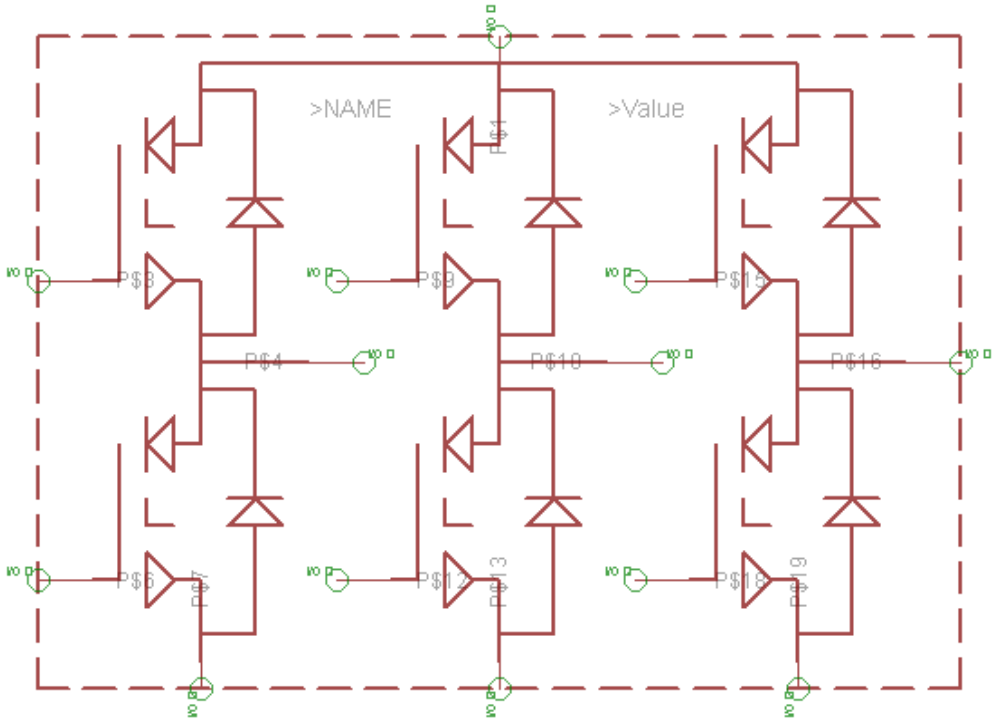


Figure 5.2. Schematic for the IGBT bridge module using Eagle®

Optocouplers HCPL - 3140 are used to drive the IGBT gates. These devices consist of a LED optically coupled to an integrated circuit with a power output stage. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by HCPL 3140 is ideally suited for directly driving small and medium power IGBTs like the CPV364MU. In the PCB design the HCPL – 3140 was configured for an open collector configuration on the input side so that the DSP can drive these optocouplers at 3.3 V. The output side of the optocouplers were provided with a 15 volts supply that was fed to the IGBT drive corresponding to a control input.

Isolation amplifier HCPL – 7840 was used for the measurement of DC link voltage. HCPL – 7840 is a current sensor in electronic motor drives. A differential output voltage was created on the outside of the optical isolation barrier. This differential output voltage is proportional to the motor current and could be converted to a single – ended signal by an op-amp.

Current transducer LTS 25 – NP was used to sense the line currents. LTS 25 – NP is a closed loop multi range current transducer using Hall Effect and has a compact design for PCB mounting. The LTS 25 – NP outputs a 0 V to 5 V scaled signal that needed to be further scaled to 0 V-3 V to input into a DSP.

Care is taken for proper isolation and while designing the IC position on the layout. Coupling capacitances are used for the supply voltages and buses. The schematic of the converter is shown in Figure 5.3 different component values used for the PCB are tabulated in Table A.4 of Appendix A and the board layout is shown Figure B.1 of Appendix B. The mounted converter is shown in Figure 5.4.

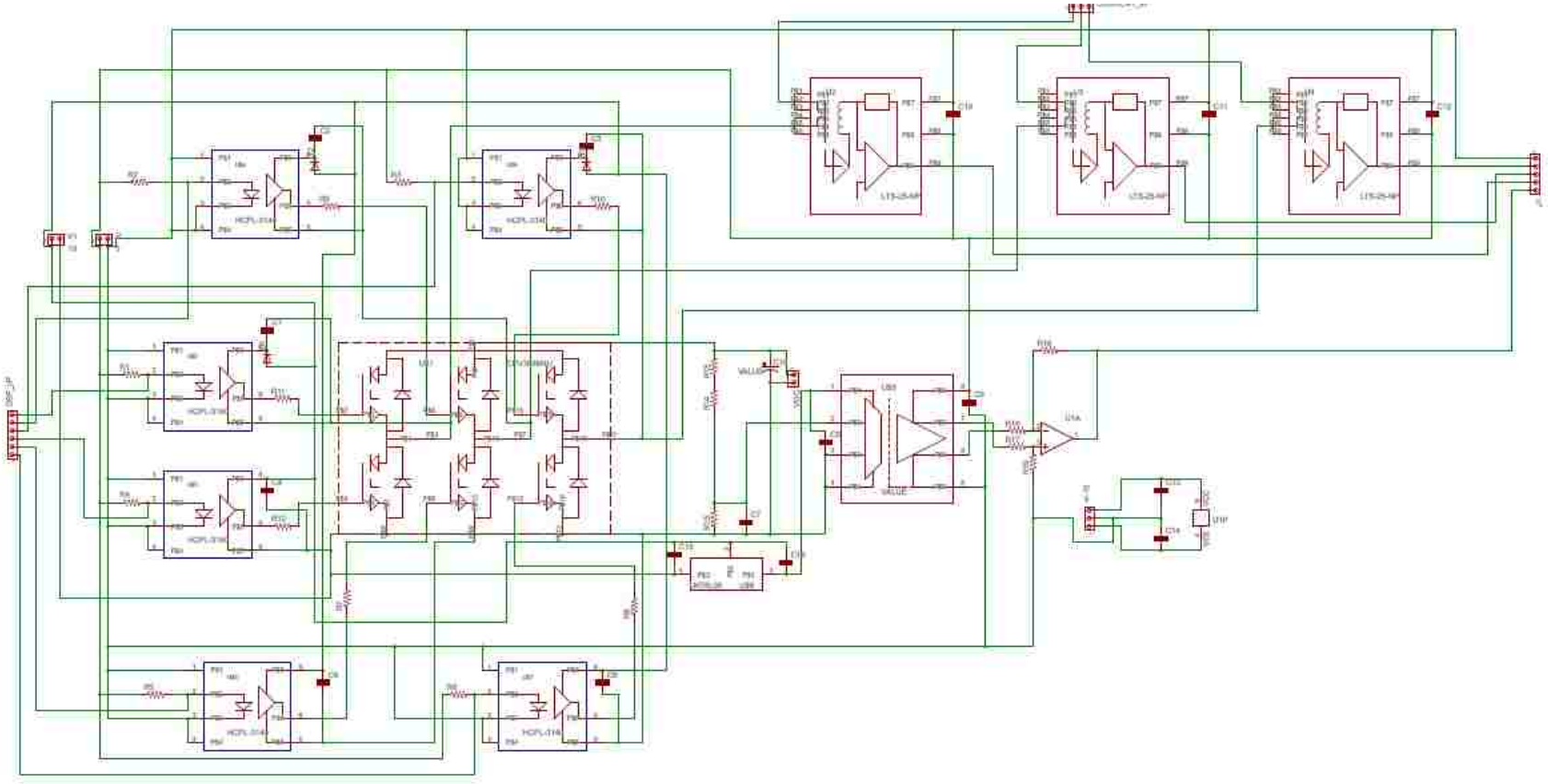

Figure 5.3. Schematic of the converter designed in Eagle®

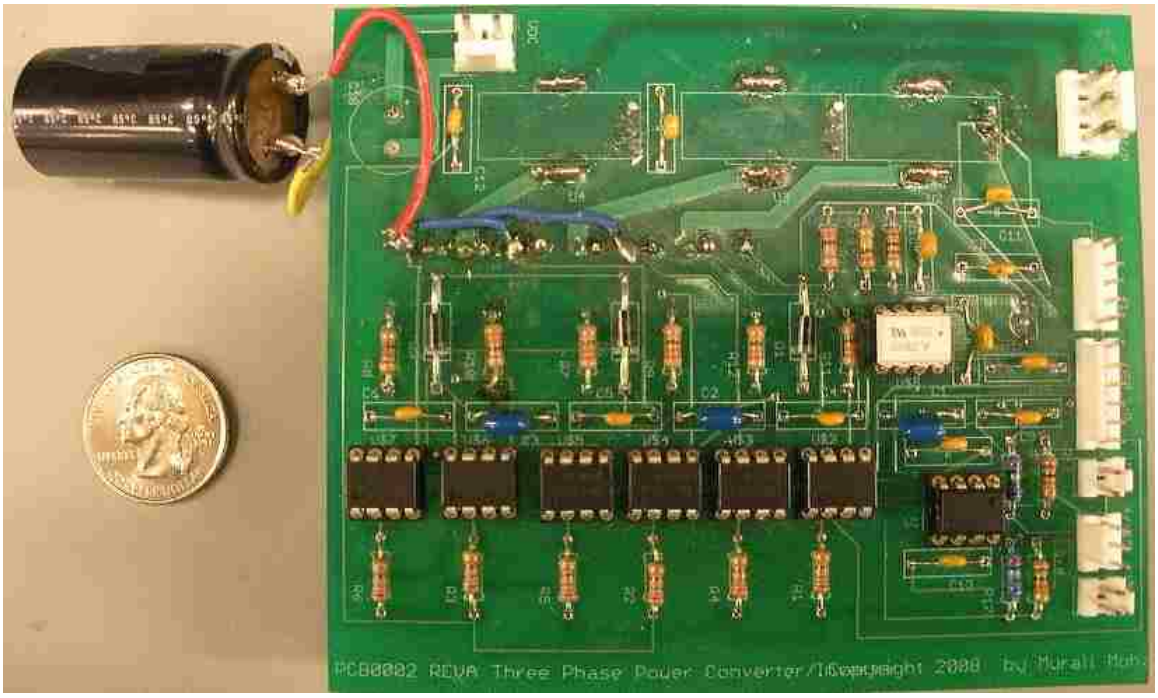


Figure 5.4. Mounted PCB of the three phase converter

LTS 25 – NP is rated for a 5 V output, whereas the DSP takes an external input of 3 V. The current range configured for this current output on the PCB board is +/- 25 A range which is too high compared to the normal operating range of the converter. Hence an external sensor board consisting of three voltage sensors (LV25-P) and three current sensors (LA55-P) was used to sense the line voltages and currents. An analog board was used to scale the outputs between 0 V and 3 V so that they were suitable to feed to DSP. As an alternative the IPC has dedicated voltage and current sensors with fixed sampling frequency and a maximum output of 10 V that had to be scaled between 0 – 3 V to input to a DSP. The attenuation factors for the DC link voltage, line voltage and current sensors are tabulated in Table A.5 in Appendix A. The circuit diagram for the sensor board and analog board are shown in Figures B.2 and B.3, respectively, in Appendix B.

Based on experiences of the present PCB design, some modifications are proposed for the next version to resolve the existing issues. The modifications are as follows.

1. Append the driver circuit on the input with a transistor and a NAND gate as shown in Figure 5.5 so that DSP outputs can be changed to open collector outputs.

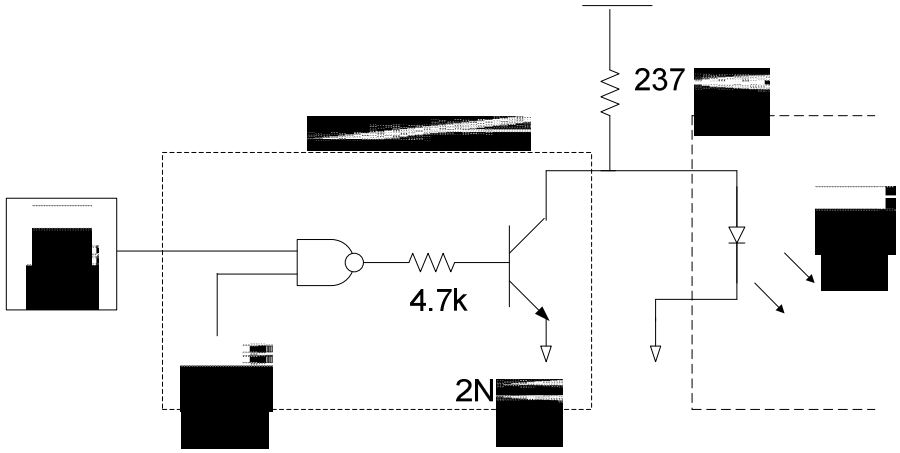


Figure 5.5. Circuit to convert gate outputs to open collector configuration

2. Addition of NAND gates between the DSP and driver circuitry to enable or disable the PWM outputs as in idling mode, the DSP produces 1's for the two IGBT's on the same leg shorting the DC source.
3. Change the input sensing range of current sensors +/- 12 A
4. Change the foot print of the current sensors as the present board has the bottom view rather than the top view.
5. The footprints of the DC bus capacitor need to be changed as the present one is not big enough to mount the capacitor.

6. Include a voltage divider that scales the outputs of the current sensors to a 3 V range to accommodate a direct input to DSP.
7. Swap the 1, 2 and 3 pins of the voltage regulator LM78LXX to 3, 1 and 2.
8. The nets connecting the negative terminal of the capacitor to the bottom terminals of the IGBT module need to be thicker as they carry higher currents coming from the line.

## 5.3 2812 DSP ARCHITECTURE AND PROGRAMMING

Technosoft® basic motion control kit consisting of DSP controller TMS320F2812PGFA and a software package DMC Developer-Pro® is used to control the fabricated converter. A realtime RS-232 serial communication provides communication between the PC and the DSP. The DSP features 32-bit data storage with fixed point operation at a speed of 150 MHz, 16 Analog to Digital Converter (ADC) input channels and two six pulse PWM channels distributed among two event managers - EVA and EVB. In this project, only one event manager is used for the grid side application of the DSP and the second one could be utilized in the future for the rotor side converter.

The line voltages, line currents and the DC link voltages are sensed using the seven channels of the ADC of the Event Manager A (EVA). A detailed explanation of the ADC is discussed in ADC reference manual SPRU060 [47]. The ADC is initialized using the DSP general purpose timer at 37.5 MHz and the values are updated using an interrupt service routine which calls back at a frequency of 20 kHz. The sensed values are scaled back to normal and the real and reactive powers are calculated using IQ Math Library [48], a virtual floating point engine. Digitized outputs for p and q commands are obtained using the sensed values. The interrupt service routine code is presented in

Appendix C. The internal values of the DSP are plotted using the inbuilt logger routine of the DMC Developer Pro® software [49]. Figure 5.6 shows the sensed phase a voltage and the dc bus voltage. The calculated voltage vector position theta and the sector values from the sensed data are shown in Figure 5.7.

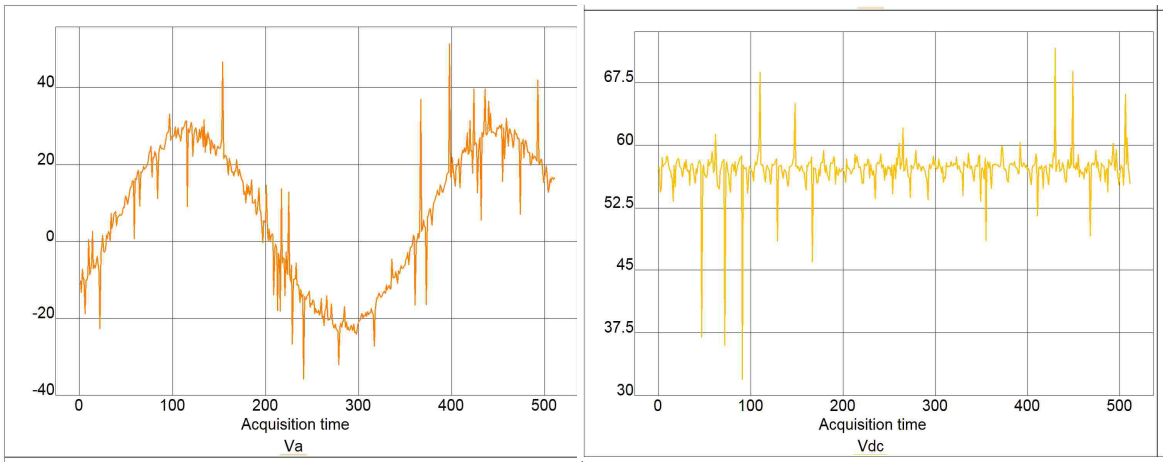


Figure 5.6. Phase A voltage and DC link voltage sensed by the ADC

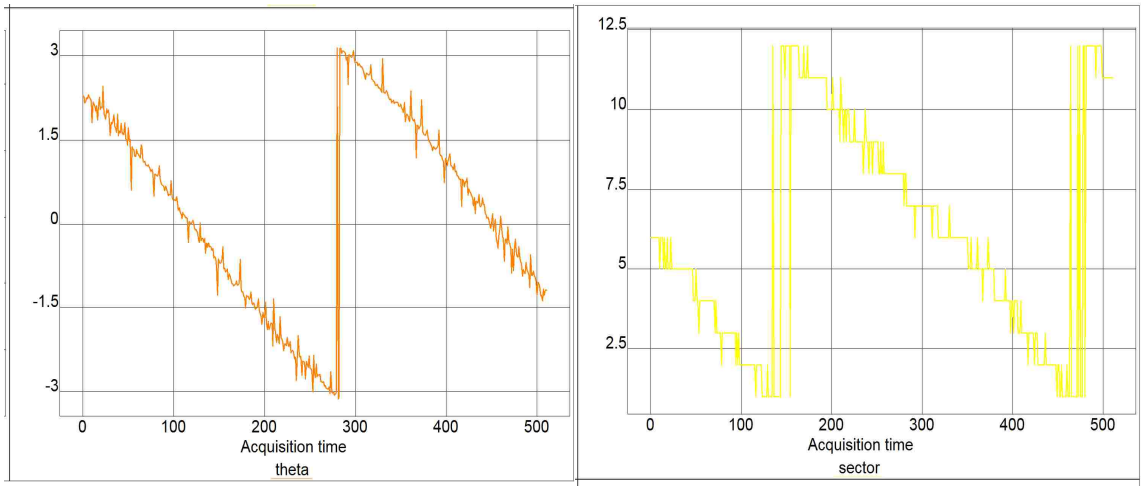


Figure 5.7. Theta and sector values calculated by the ADC

The PWM circuit associated with each event manager of the DSP is capable of producing six PWM output channels triggered by compare units. The function of the PWM circuit includes generation of asymmetric/symmetric waveforms, dead band and space vector PWM. All these generators take a voltage input and produce the PWM outputs and hence are not directly applicable to the DPC algorithm. Space vector PWM is the nearest applicable algorithm for DPC and hence is modified to be applied for DPC. In space vector PWM the algorithm applies two adjacent vectors to generate the intermediate vector for certain time desired by the compare units along with the zero vector. The PWM switches the zero vectors to either (000) or (111), whichever differs from the previous state by one, hence is not directly controllable. The Rest of the six vectors of the vector plane discussed in Figure 4.3 are applied by using a complete time period in the compare registers thus allowing the application of the one vector for most of the time.

Table 5.1 show a list of control registers values and compare register time periods for the eight possible vectors during a PWM time period of 50 microseconds (0x03A9). The values are coded in the main program of the DSP which are executed in a while loop depending on the sector, digitized P and Q commands. A detailed register setup and initialization of the DSP PWM circuit for space vector approach is discussed in the event manager manual [50].

A dead band time of one microsecond is preset so that the transients during the switching of the two IGBT's in a leg can be ignored. The code used in the DSP for DPC is given in Appendix C.

Table 5.1. Compare registers values of voltage vectors.

| Vector | Action control register | Compare register 1 | Compare register 2 |
|---|---|---|---|
| 000/111 | 0666 | 0x03A8 (49.9467 µs) | 0x03A8 (49.9467 µs) |
| 100 | 1666 | 0x03A8 (49.9467 µs) | 0x03A8 (49.9467 µs) |
| 010 | 2666 | 0x03A8 (49.9467 µs) | 0x03A8 (49.9467 µs) |
| 110 | 3666 | 0x03A7(49.893 µs) | 0x03A8 (49.9467 µs) |
| 001 | 4666 | 0x03A8 (49.9467 µs) | 0x03A8 (49.9467 µs) |
| 101 | 5666 | 0x03A7(49.893 µs) | 0x03A8 (49.9467 µs) |
| 011 | 6666 | 0x03A7(49.893 µs) | 0x03A8 (49.9467 µs) |
| 111/000 | 7666 | 0x03A7 (49.893 µs) | 0x03A8 (49.9467 µs) |

## 5.4 INDUSTRIAL POWER CORRUPTOR (IPC)

The converter with the DPC control algorithm was tested for Low Voltage Ride Through (LVRT) applications using the IPC [1]. The IPC adds sags, swells and interruptions reliably and repeatedly to a healthy system voltage to test sensitive electronic equipment. The IPC works on a transformer-based principle that contains an autotransformer with multiple taps and IGBT based switches. Correct tap selection and switching pattern creates the desired disturbances on the equipment. The IPC is also used to record and diagnose the disturbances in an easier way. The IPC has an inbuilt current limiting capability which trips the integrated circuit breaker with an internal setting determined by the maximum current of the IPC. Alternatively, this current can be set according to the circuit to be tested. An error message is displayed for each

automatic trip event occurred during the execution. The front view consisting of different controls to create disturbances and meters and channels to display and record real time data is shown in Figure 5.8.

Figure 5.8. Front view of the IPC

## 5.5 DPC IMPLEMENTATION AND RESULTS

The picture of the whole hardware setup is shown in Figure 5.9. The source voltage is tapped from a 230 V supply through a three phase variac. The three phase variac steps down the voltage of the source to the desired level. A delta-wye transformer was connected in between the variac and the power corruptor to provide a neutral current loop in the source. The converter was connected to the load side of the IPC using a series inductance. Protection was provided using Metal Oxide Varistors (MOV) and snubber capacitances to the line to line voltages of the power corruptor

output and converter input to suppress the surges in the source due to a sudden circuit breaker tripping. A system enable was provided by the NAND gates to enable the DSP inputs to the power converter. The power corruptor was set to a predetermined current limit on the basis of the load and the experiment. A switched variable load box was used as a load. The converter is started with a light load and later loaded to the desired value. The power on sequence of the circuit is given in the steps below.

1. Make sure the switch/NAND gate is disabled and then power on the control circuit. Download the DSP program.
2. Apply light load on the load box and turn on the DC power supply to charge the DC capacitance.
3. Make sure the circuit breaker of the power corruptor is off (circuit is disconnected) and power on the power corruptor and connect it to the PC.
4. Check if the three phase voltages are as desired; if not adjust them on the Variac and then turn on the circuit breaker.
5. Execute the DSP program and enable the switch/NAND gates immediately.
6. Turn off the DC power supply and decrease the voltage to zero and increase the load to the desired value.

The power off sequence of the circuit is given in the steps below.

1. Disable the switch/NAND gates and turn off the circuit breaker of the power corruptor.
2. Stop executing the program and save the results on the IPC, oscilloscopes and DMC Developer Pro® software.
3. Disconnect the IPC from the PC and turn off the IPC and turn off the control circuit.

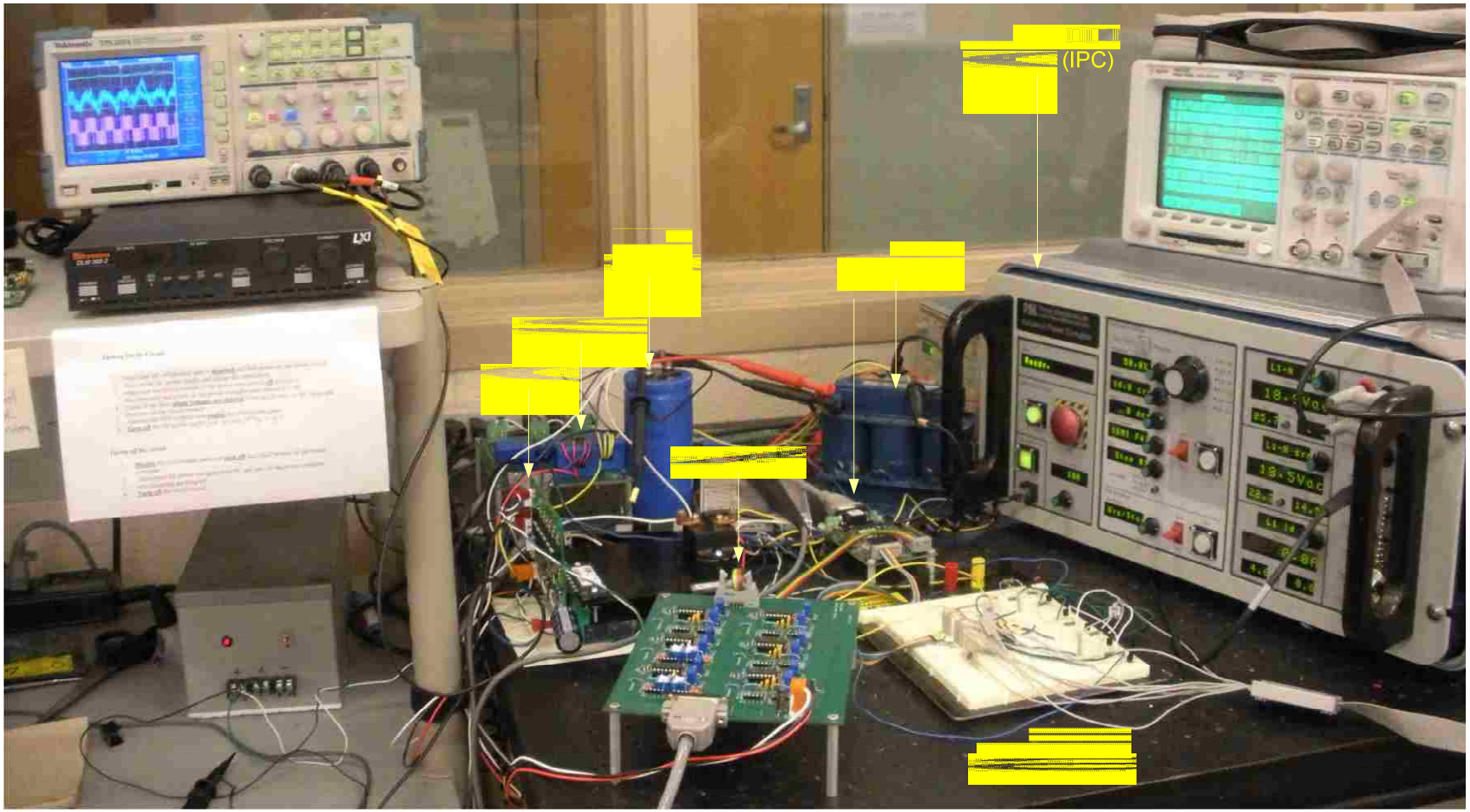


Figure 5.9. Picture of the experimental setup

Due to the limitations associated with the protection circuitry, the DPC was tested for 60V on the DC side with a 35V line to line voltage on the AC side. The system was initially loaded to a light load of 115 ohms before initiating the PWM circuit and later switched to a medium load of 90 ohms for disturbances and a higher load of 65 ohms for normal operation. The circuit was initially run to test the normal operation of the DPC. Figure 5.10 shows the DC voltage (vdc), line to line converter voltage (vab1) and line current (ia) readings of the oscilloscope; Figure 5.11 shows the line voltage and line current tapped from the IPC; Figure 5.12 shows the calculated P and Q from the acquired data and Figure 5.13 shows the simulated results. From the experimental results, it can be seen that the coded algorithm is capable of maintaining the dc link voltage with a ripple of four volts which is much higher compared to the simulated results. The currents are more distorted in the experimental results and the powers have greater oscillations, but it can be observed that the real and reactive powers are controlled by the DPC.

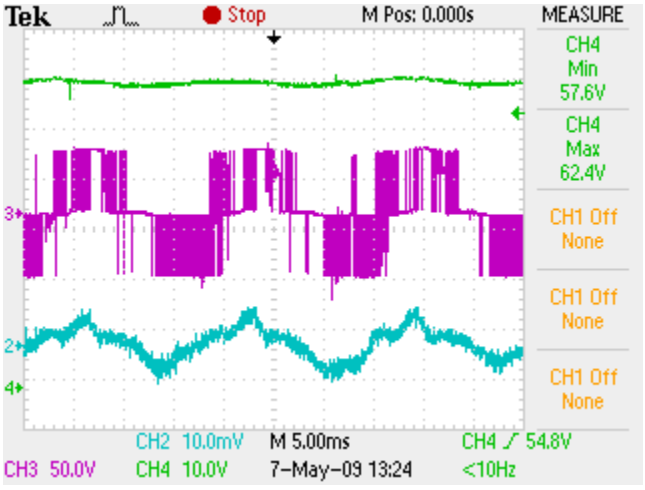


Figure 5.10. Experimental results for normal operation. (DC link voltage (vdc) – CH4, Converter line to line voltage (vab1) - CH3, line current (ia) - CH2)

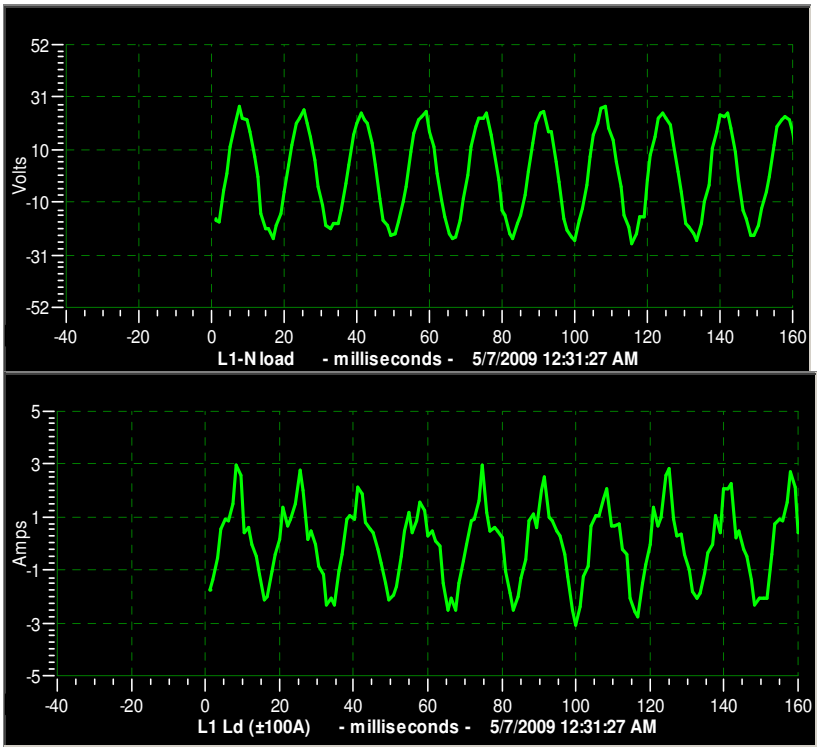


Figure 5.11. Experimental results for normal operation (from top source voltage (va) - L1-N load, source current (ia) - L1 Ld)

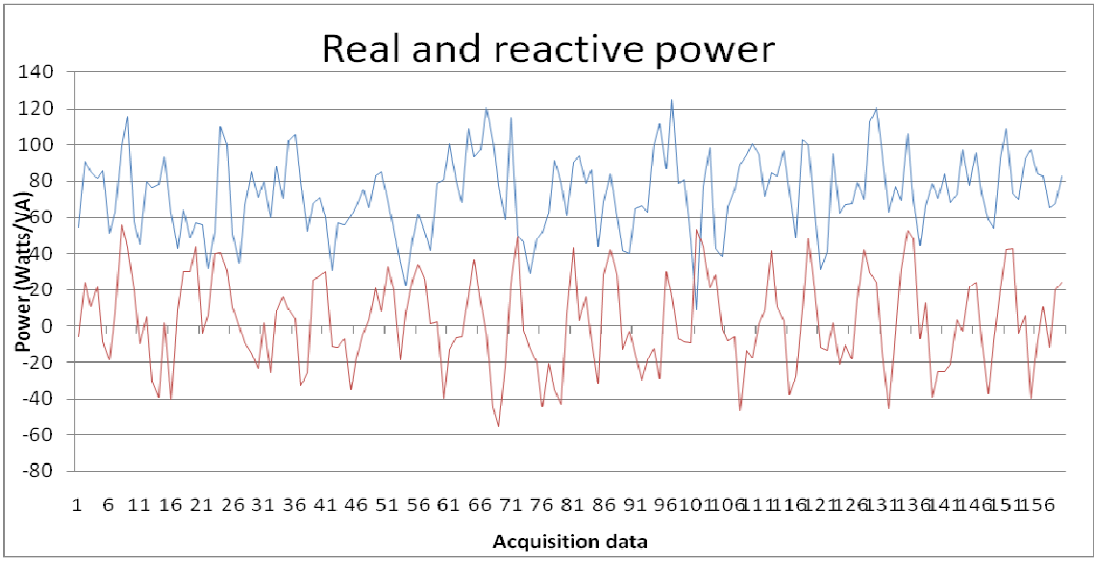


Figure 5.12. Real and reactive powers for normal operation (real power - blue, reactive power - red)

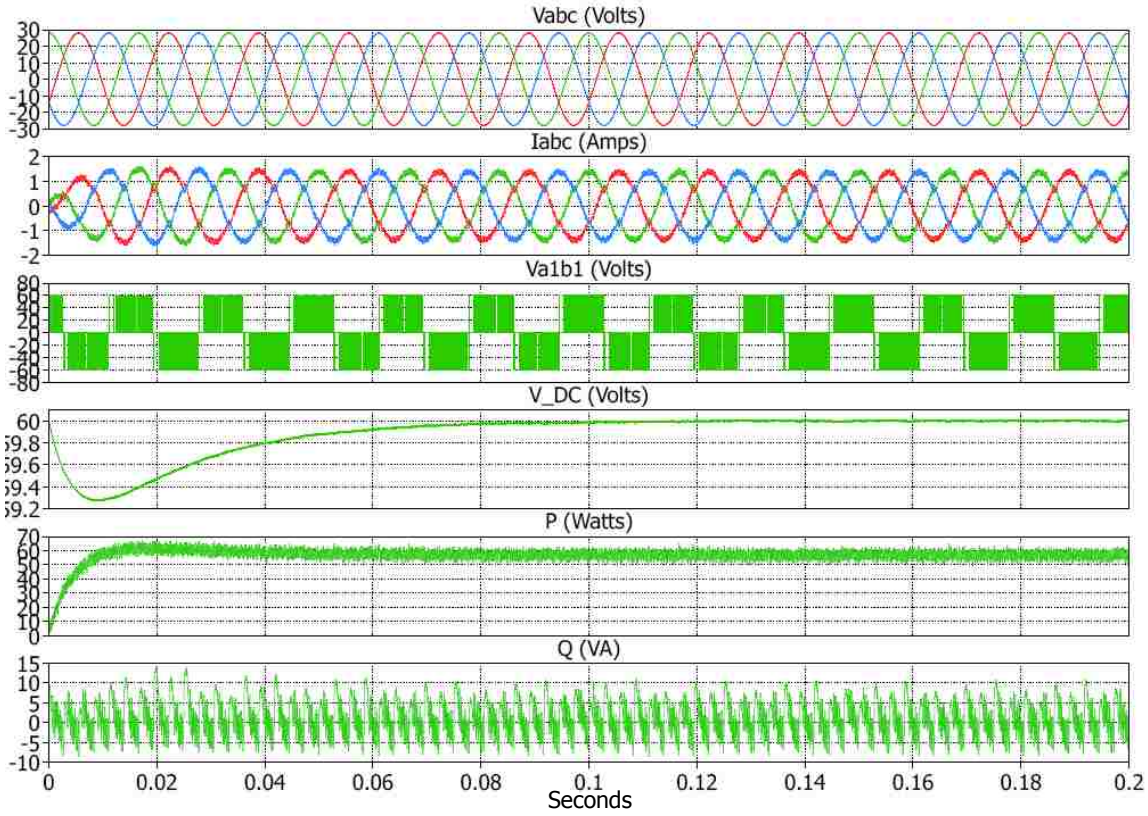


Figure 5.13. Simulated result for normal operation (from top source voltages, source currents, converter line to line voltage, DC link voltage, real power and reactive power)

The DPC hardware was tested for the grid code disturbances by implementing voltage sags and dips as discussed in the modern grid code requirements for wind turbines according to FERC 661a [5]. Four scenarios were simulated:

1. 70% input voltage for two seconds (120 cycles). – Figures 5.14 – 5.17
2. 50% input voltage for twelve cycles. – Figures 5.18 - 5.21
3. 30% input voltage for three cycles. – Figures 5.22 – 5.25
4. 50% input voltage for 1 sec. – Figure 5.26

For the 70% voltage the fault is applied at 0 ms in Figure 5.14 and 5.15, there is no variation in the DC link (Figure 5.14) voltage and the real and reactive powers in the experimental results as well as the simulation. Hence the DPC is capable of sustaining 70% voltage according to the grid code requirements.

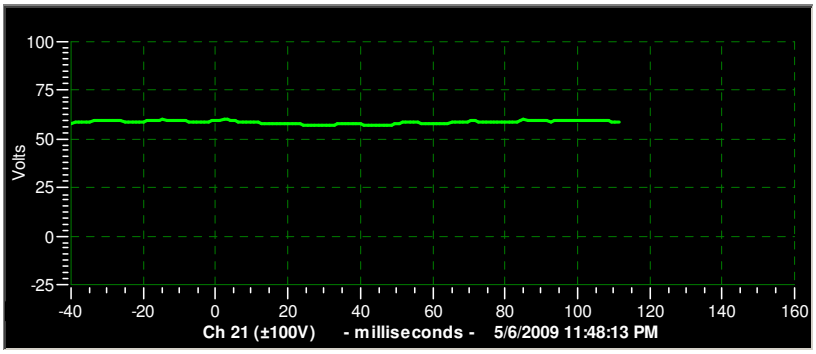


Figure 5.14. Experimental result for 70% voltage for 2 seconds (DC link voltage (VDC) – Ch 21)

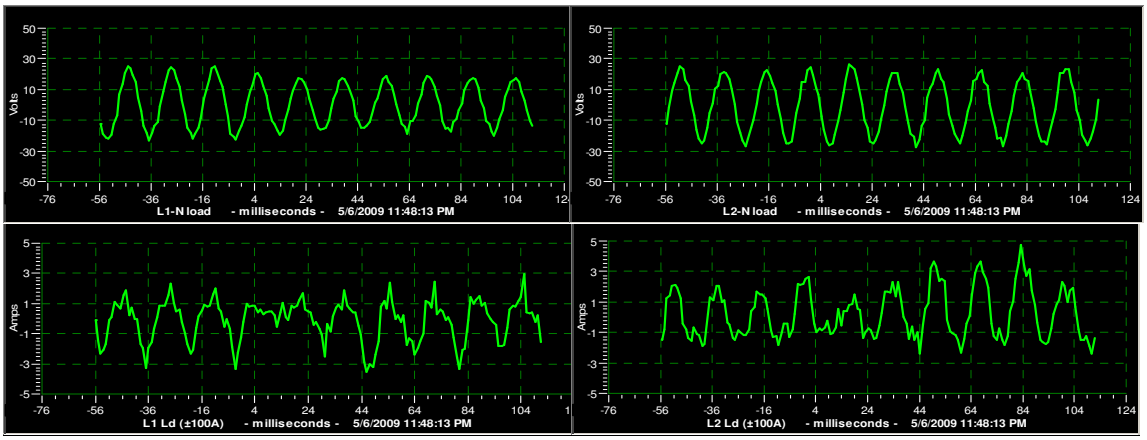


Figure 5.15. Experimental results for 70% voltage for 2 seconds. (clockwise - Source voltages (va, vb) – L2-N, L1-N load, source currents (ib, ia) – L2 Ld, L1 Ld)

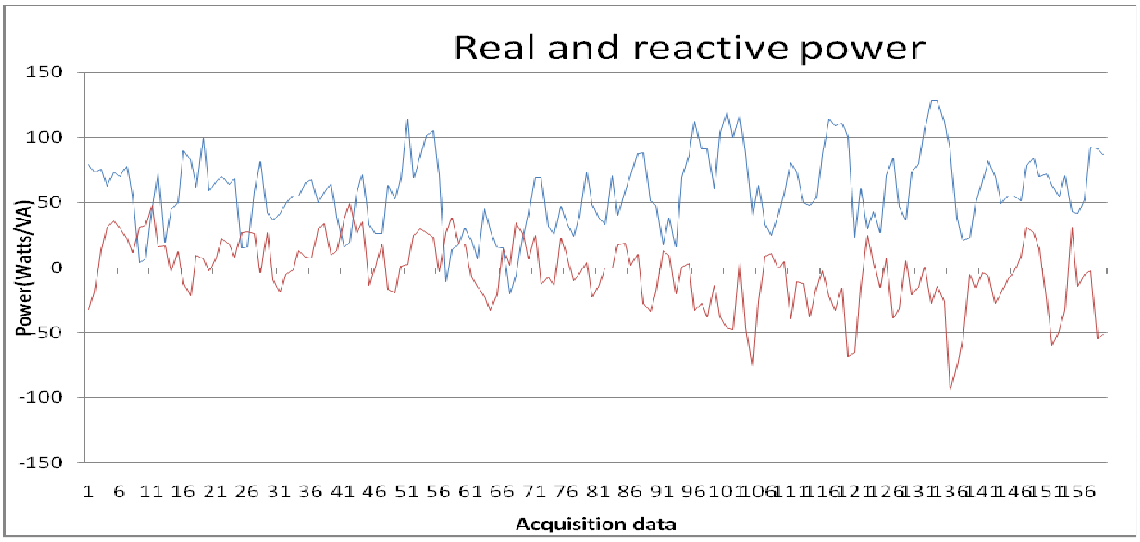


Figure 5.16. Real and reactive powers for 70% voltage for 2 seconds (real power - blue, reactive power - red)

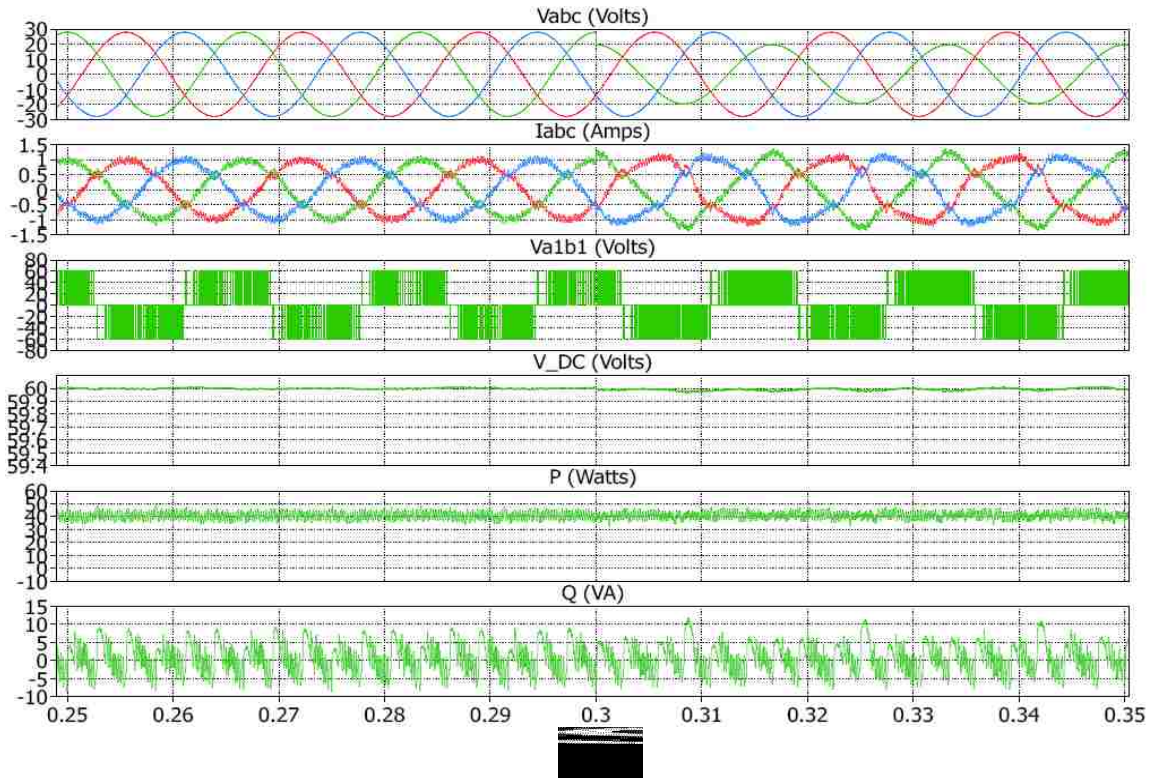


Figure 5.17. Simulated result for 70% voltage starting at 0.3 s (from top source voltages, source currents, converter line to line voltage, DC link voltage, real power and reactive power)

The other experiments conducted on the converter include deeper voltage sags. For these cases, there is a perceivable dip in the DC link voltage to a maximum of 10 V, but the voltage returns to the normal value after the sag is taken off from the power system. Hence the DPC is capable of holding these post fault recovery sags and operates normally for voltages greater than 70%.

During the sag, the oscillation in the real and reactive power increases but comes back to normal after the sag is removed. The oscillations in case of the experimental results are higher than those resulting from the software simulations as seen in the case of normal operation. The currents suffer in case of DPC as there is distortion during the disturbance event. The faulted phase currents increase during the fault as observed on the oscilloscope and the simulation results. The IPC recordings are not clear due to smaller sampling frequency. The 50% voltage applied is for 12 cycles; hence after the dip, the DC link voltage has an overshoot when it recovers back to the normal operation as seen in Figure 5.18.

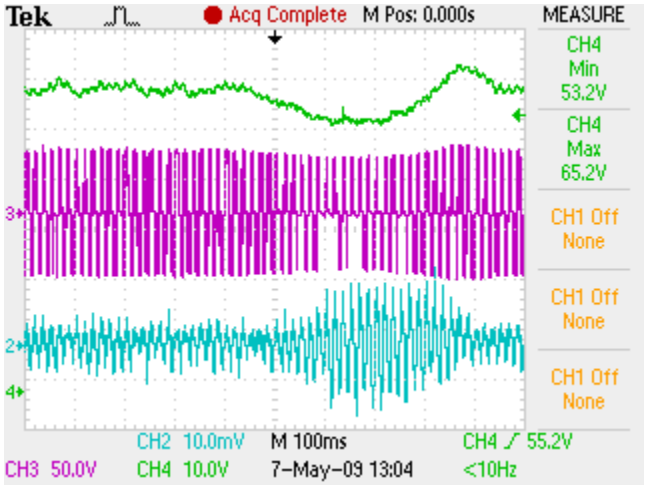


Figure 5.18. Experimental result of 50% voltage for 12 cycles - (DC link voltage (vdc) – CH4, Converter line to line voltage (vab1) - CH3, line current (ia) - CH2)

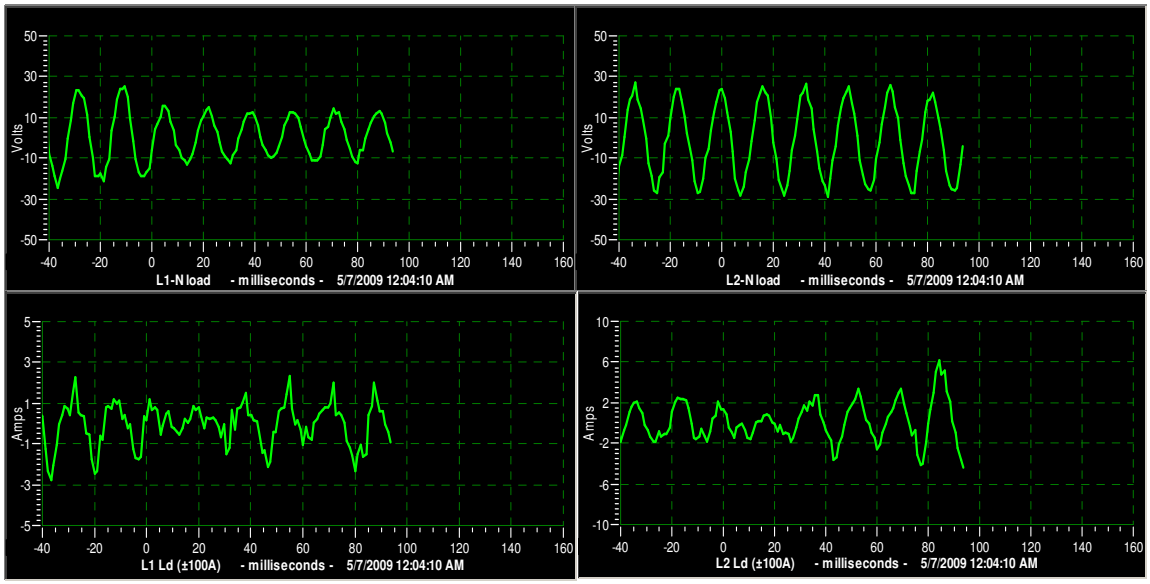


Figure 5.19. Experimental results for 50% voltage for 12 cycle starting at 0 s. (clockwise - Source voltages (va, vb) – L2-N, L1-N load, source currents (ib, ia) – L2 Ld, L1 Ld)

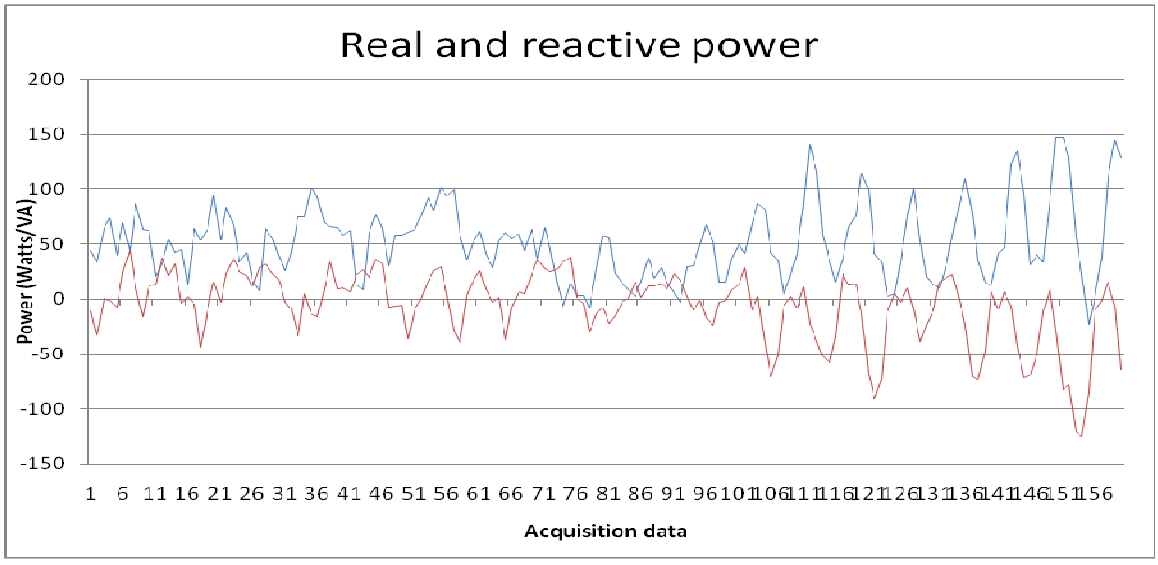


Figure 5.20. Real and reactive powers for 50% voltage for 12 cycles (Real power - blue, reactive power - red)

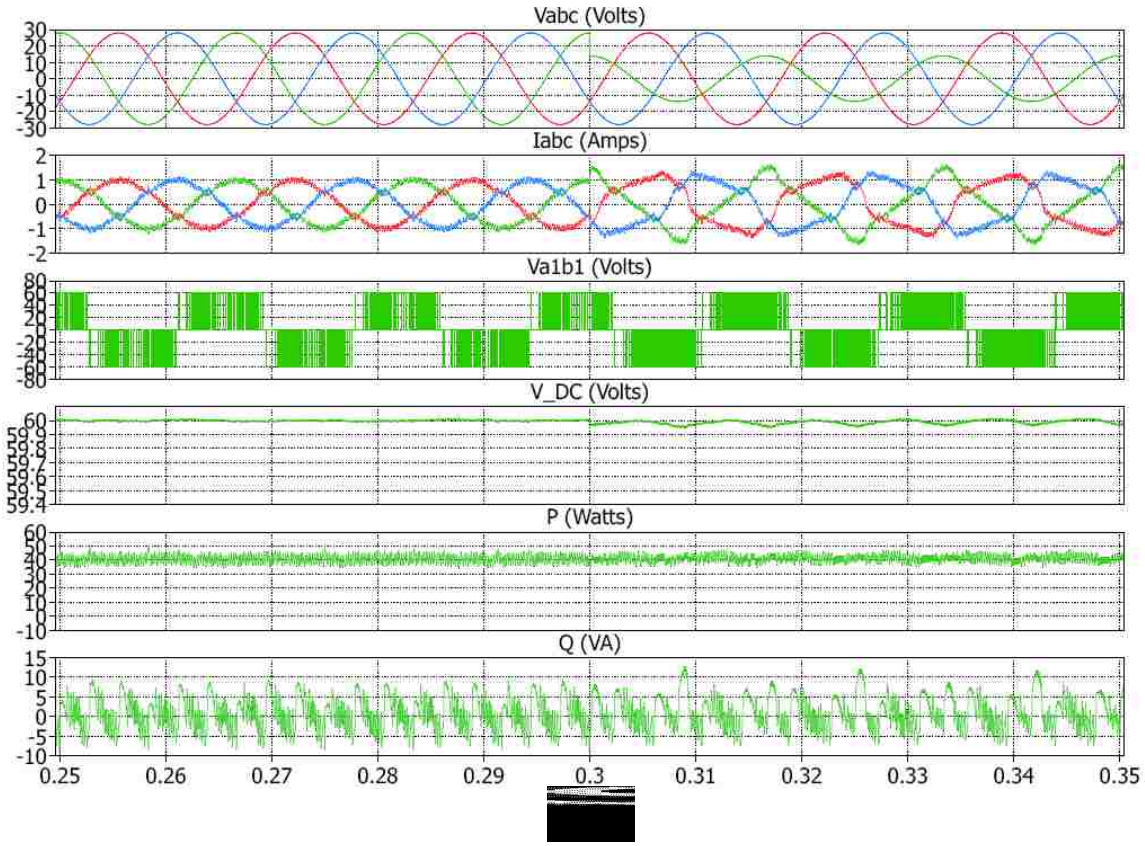


Figure 5.21. Simulated result for 50% voltage starting at 0.3 s. (from top source voltages, source currents, converter line to line voltage, DC link voltage, real power and reactive power)

A 30% voltage was applied for short durations as these occur during a very high faulted condition. The dip and overshoots in this condition are small when compared to the 50% dip for 12 cycles (Figure 5.22) as these are applied for a short duration. Hence, the duration of the fault also plays an important role in the performance of the converter along with the depth of the sag.

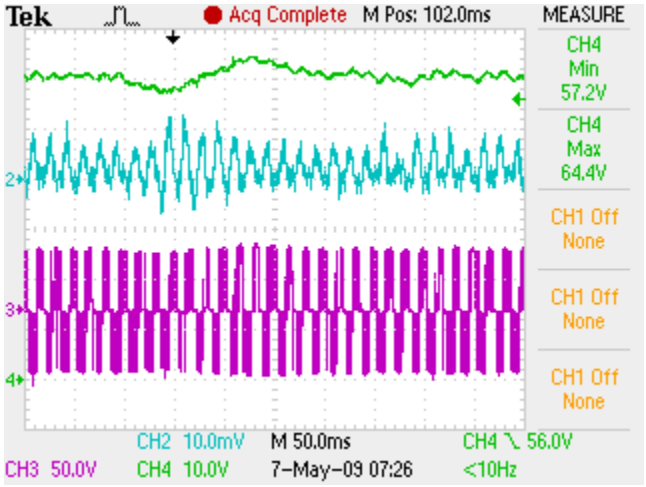


Figure 5.22. Experimental result of 30% voltage for 3 cycles. (DC link voltage (vdc) – CH4, Converter line to line voltage (vab1) - CH3, line current (ia) - CH2)

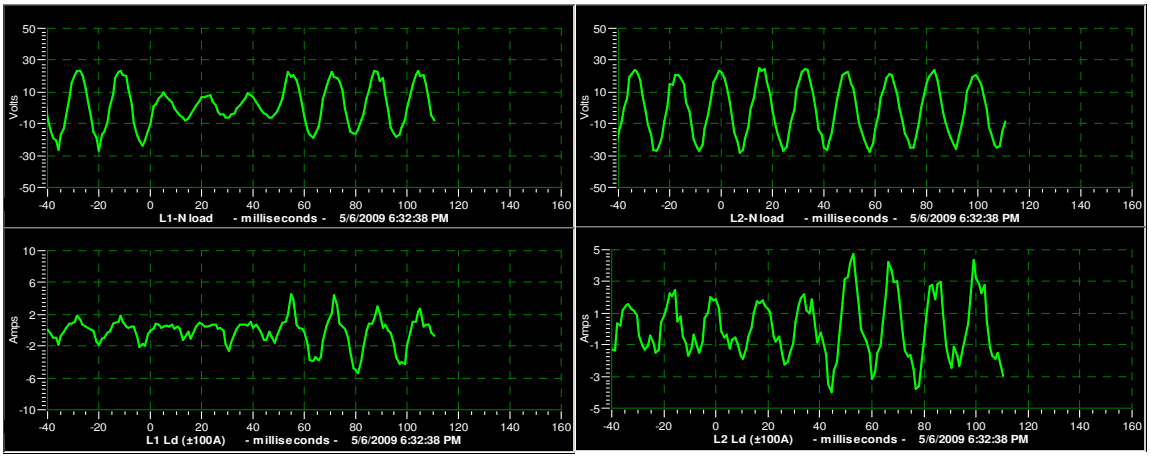


Figure 5.23. Experimental results for 30% voltage for 3 cycles starting at 0 s. (clockwise - Source voltages (va, vb) – L2-N, L1-N load, source currents (ib, ia) – L2 Ld, L1 Ld)

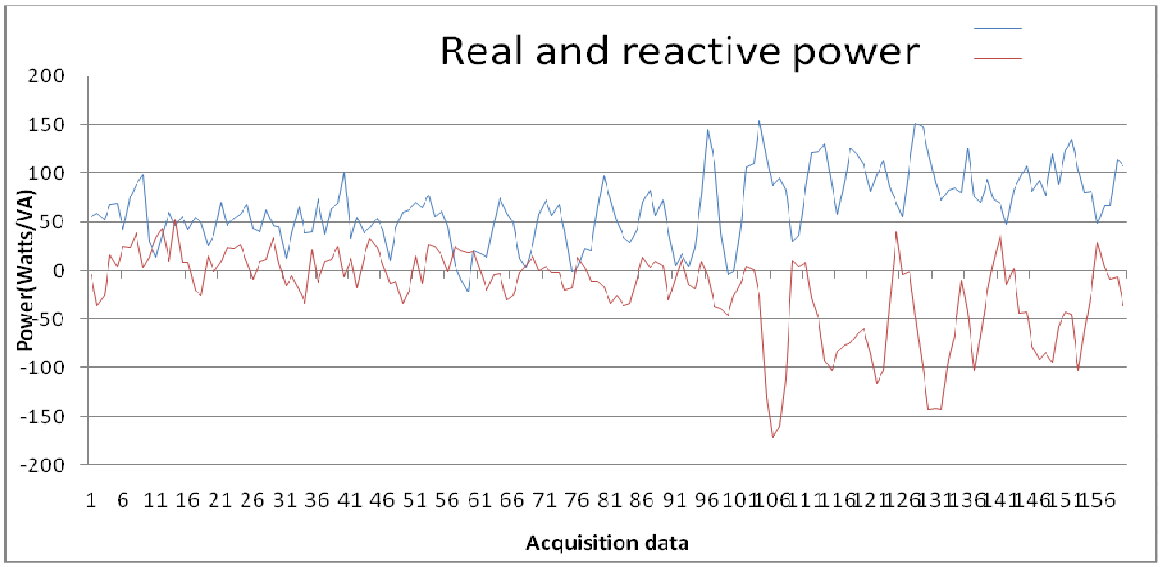


Figure 5.24. Real and reactive powers for 30% voltage for 3 cycles (Real power - blue, reactive power - red)

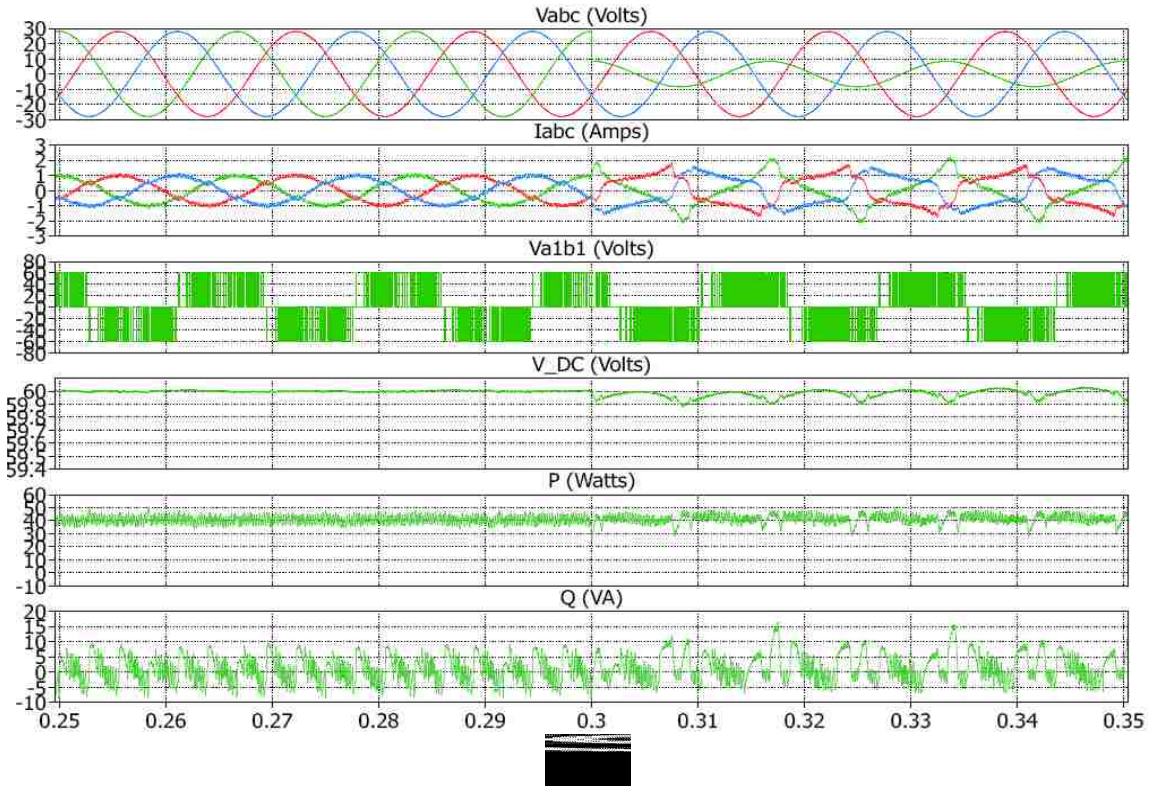


Figure 5.25. Simulated result for 30% voltage starting at 0.3 s. (from top source voltages, source currents, converter line to line voltage, DC link voltage, real power and reactive power)

Table 5.2 gives a comparison of the ripple in DC link voltage, real power and reactive power. The oscillations increase in case of the system disturbances and the sag depth increases compared to the general operation. The ripples are high compared to the simulation results as the sampling of the input signal of the DSP is not accurate. Hence an accurate sampling method needs to be adopted.

Table 5.2 Comparison of ripple in DC link Voltage, real power and reactive power for different grid code events.

| Control Min/Max | Load | DC Link Voltage (60V) | Real Power | Reactive Power (0 VA) |
|---|---|---|---|---|
| Normal operation | 65 ohms | 57.6/62.4 | 20/120 | -50/50 |
| 70% voltage for 2 seconds | 90 ohms | 57.6/62.4 | -10/120 | -90/50 |
| 50% voltage for 12 cycles | 90 ohms | 53.2/65.2 | -25/150 | -125/25 |
| 30% voltage for 3 cycles | 90 ohms | 53.2/65.2 | -10/150 | -170/25 |

To test the limitation of the DPC technique, a 50% voltage was applied on the system for one second more than that required by the grid code. The DPC controller could sustain the sag for 18 cycles (300 ms) and created a huge dip in the DC link voltage to 14.4V as see in Figure 5.26. After the dip the controller could return to its normal operation in an exponential way. Hence the controllers are highly dependent on the duration of the fault. Several other cases were run for higher loads for sags less that 50%. The DC link voltage settled to a new value around 30 V limiting the control

capability of the controller. Hence, the DPC has limitation with regard to the load and the duration of the disturbance on the system. There is not a considerable amount of change in the response of the DPC during load switching as it is done after initializing the circuit.

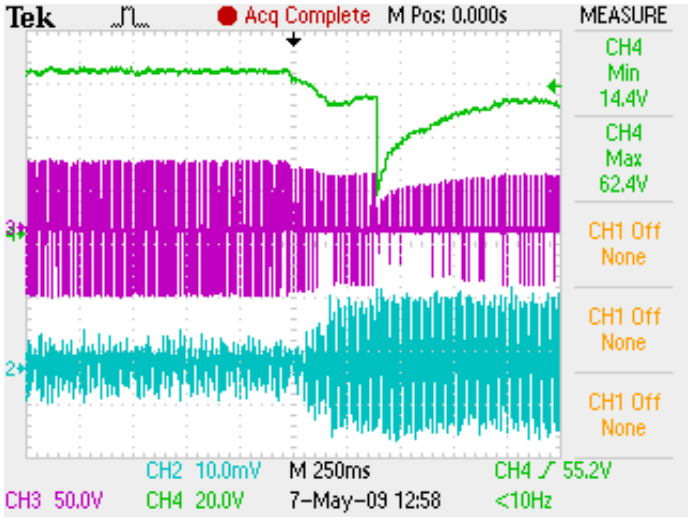


Figure 5.26. Experimental result of 50% voltage for 1 second. (DC link voltage (vdc) – CH4, Converter line to line voltage (vab1) - CH3, line current (ia) - CH2)

The current waveforms of the DPC are distorted to a greater extent during the application of disturbance thus including more oscillations in the real and reactive power. Hence higher level delta modulation as well as compensation of power during imbalance in the system need to be considered.

## 5.6 SUMMARY

This section discussed the hardware implementation of the DPC in detail. The converter was designed on a PCB using Eagle®. External voltage sensors and current sensors are provided to the circuit. The circuit was tested for LVRT applications using the power corruptor and different voltage dips are experimented and compared with the simulation results. Experimental results had more oscillations in the DC link voltage, real and reactive powers as compared to the simulation results due to the ideal nature of the simulation results and noise in the ADC inputs. The behavior of the voltages and currents was similar to the simulated results. The DPC was capable of sustaining its control during the disturbance according to grid code requirements. Higher dips cause a disturbance in the system which is characterized by an overshoot during the post disturbance recovery. For voltages deeper than 60% operating outside the grid requirements, the control was limited by time of the disturbance to regain its normal operation. The practically implemented DPC algorithm needs to include filters for tapping the ADC values to eliminate the transients created while sensing the parameters as this helps in smoothing the control. A direct register write algorithm needs to replace the existing space vector PWM algorithm to eliminate unwanted switching and the end of the periods due to the present indirect algorithm and thus the harmonics in the line currents.

# 6. CONCLUSIONS AND FUTURE WORK

## 6.1 SUMMARY AND CONCLUSIONS

This Dissertation discusses multiple control techniques for DFIG based wind turbine converters. Low voltage disturbances were conducted to test the performance of these techniques. Initially, conventional current control of DFIG-based wind turbines was analyzed in detail and tested for disturbances on the system using the widely-used software DIgSILENT®. The inability of the DFIG for system disturbances was further analyzed using sequence controllers.

A sequence controller was mathematically analyzed and simulated using PLECS® block set of Matlab Simulink®. The simulation results show that the d-axis voltage is smooth both in positive and negative reference frames. The current waveforms have fewer amounts of higher order harmonics. The DC link voltage and the real and reactive powers have fewer oscillations compared to the conventional controller. The currents show a significant improvement over the conventional controller. The technique uses more current loops leading to a sluggish response of the controller and hence the controller is unable to respond to sudden changes in the system disturbances. This controller has five PI loops and four notch filters; hence it needs more fine tuning of the controllers and more complex hardware implementation.

A novel control technique called the Direct Power Control technique was investigated. This control utilizes delta modulation-based direct control of active and reactive powers. The grid side converter of the DFIG was simulated using the DPC and compared with the conventional current controller and the sequence controllers. The DPC offers the same advantages as the sequence controllers with faster response compared to the conventional controller. The DPC suffers the disadvantage of distorted

currents during system disturbances. A modified DPC was then derived and analyzed to modify the commanded real and reactive powers during disturbances

The rotor side converter using the DPC was capable of controlling the stator side real and reactive power without using system parameters. The complete DFIG based system was simulated with DPC control and tested for voltage sags on the system. The system was capable of sustaining the disturbances and commanded the real and reactive powers accordingly. The DPC utilizes only one PI loop for DC bus voltage control and a simple control algorithm. Therefore, this controller was selected for implementation on hardware.

A three phase converter was designed in Eagle® for this purpose. A DSP TMS320F2812 was used to generate control inputs. The converter was tested using an industrial power corruptor for different voltage disturbances. The converter was capable of sustaining the disturbance pertinent to grid code requirements. A disturbance of longer duration cause a high voltage dip on the dc bus voltage and higher real and reactive power oscillations. The experimental results have higher oscillation in the DC link voltage, and also in the real and reactive powers compared to the simulated results. The currents generated by the converter have more harmonics due to the indirect space vector control algorithm utilized in the hardware. The load capability of the converter is high during normal operation whereas this decreased during the disturbance event.

A summary of the different controllers describing different performance aspects for low voltage ride through of each controller is given in Table 6.1.

Table 6.1. Summary of the performance of different controllers during system disturbance

| Control technique | DC-link voltage, real and reactive power oscillations | Line current distortion | Response of the algorithm and practical implementation |
|---|---|---|---|
| Conventional current control | Twice the source frequency oscillations appear in the output and reactive power does not average to zero. | Less distortion in line currents | Utilizes three PI controllers and has moderate response time and overshoot. Constant and lower switching frequency. |
| Sequence controllers | Oscillations during a system disturbance reduced to a greater extent with a slow settling time. (50% of the conventional) and reactive power averages to zero. | Smooth line currents | Utilizes five PI controllers and four notch filters with sluggish response. Complex to implement and fine tune. Constant and lower switching frequency. |
| Direct power control (DPC) | Less oscillation than the sequence controllers with a fast settling time. (50% of the conventional) and reactive power averages to zero. | Highly distorted line currents | Utilizes one PI controller, easy to implement and has fast response but does not have constant switching frequency |
| Modified direct power control | More oscillations than the regular DPC but less compared to sequence controllers and zero average reactive power. | Better line currents than the regular DPC | Utilizes one PI controller and four notch filters moderate to implement and has fast response and does not have constant switching frequency |

## 6.2 AUTHOR'S CONTRIBUTION

The author contributed to the state of art wind energy technology for the low voltage ride through applications. The author successfully compared different advanced control techniques, namely sequence controllers and DPC, to identify the best control technique suitable for low voltage ride through applications of DFIG-based wind system converters. Both the sequence controller and DPC were adapted from conventional motor drives and applied to the grid side converter for a DFIG.

A modified DPC algorithm was implemented on his own to overcome the disadvantages of the sequence controllers and DPC. The proposed modified controller uses a hybrid approach of the power control used in sequence controllers and the delta modulation and look up table algorithm of DPC.

The author simulated the DPC algorithm for the back-to-back converters of the DFIG-based wind turbine converters to improve the overall low voltage ride through of the system. This demonstrated the compatibility between the grid-side and rotor-side converters with the DPC algorithm.

DPC was practically tested by the author in the laboratory by an indirect space vector modulation algorithm in DSP 2812 under low voltage conditions. A three phase converter was designed and fabricated by the author for this purpose.

## 6.3 FUTURE WORK

The DPC was tested experimentally for ride-through application using the grid side converter. A complete DFIG system using the back-to-back PWM converters controlled by the DPC would extend the scope of application for low voltage ride

through. The DPC utilizes the same control algorithm for both grid side and rotor side converters. In the rotor side converter, the stator voltages are directly controlled instead of the converter source voltages. The need for DC link voltage PI controller was eliminated for the rotor side converter and thus one can simply modify the code to accommodate delta modulation only. The zero voltage vectors also needs to be eliminated as they do not have direct control over the real and reactive powers thus reducing the algorithm to utilize six sectors rather than twelve sectors as in the case of the grid side controller.

The experimental setup should be equipped with protection to accommodate a direct startup and eliminate manual errors caused during startup. A software enable would get rid of most of the manual steps as this can be done during the execution of the DSP code.

A modification of the DPC using a higher level delta modulation bands and imbalance compensation need to be considered to address the issues with oscillations in the real and reactive power and harmonics in line currents. A direct write algorithm could be developed rather than the indirect space vector algorithm used.

The generators used in wind power production are connected directly using a back-to-back converter to the grid. It works mainly on the principle of real and reactive power flow. As the DPC offers direct control of the real and reactive powers, this algorithm can be extended to PMSM and BDC generators utilized for wind power application.

The voltage dips caused in the dc link voltage during very low voltages can be eliminated by the use of storage at the DC link bus. This storage should be fast acting, such as superconducting magnetic energy storage or ultra capacitors to pull out high

amounts of power during the system disturbance and charge during the normal operation. Storage can also provide reserve power to the system during intermittent turbine speeds to maintain the real and reactive power of the grid.

A rapid increase in wind penetration in the utility makes it important to look after the temporary over voltages caused in the utility. These over voltages may reverse the current flow in the voltage source converter thus increasing the DC link voltage [51] Hence the DPC needs to be tested for high voltage ride through requirements in the system to keep the wind turbine operating during the disturbances.

# APPENDIX A.

# SIMULATION AND PRACTICAL IMPLEMENTATION PARAMETERS

Tables A.1 to A.5 lists the different parameters used throughout the dissertation.

Table A.1 VSC simulation parameters

| | | | |
|---|---|---|---|
| DC link capacitance | 2400 μF | DC Loop proportional gain | 1 |
| System frequency | 60 Hz | DC Loop Integral gain | 40 |
| Line inductance | 12 mH | Current loop proportional gain | 4.5312 |
| Line resistance | 0.1 ohms | Current loop integral gain | 0.1888 |
| Source peak voltage | 150V | Sampling frequency | 20 kHz |
| Dc link voltage | 283V | Notch filter Q | 10 |
| Load resistance | 100 ohms | Notch filter $\omega_o$ | 753.6 |

Table A.2 Induction machine parameters

| | | | |
|---|---|---|---|
| Stator resistance (Rs) | 0.4 ohms | Stator leakage inductance (Lls) | 0.002 H |
| Rotor resistance (Rr') | 0.8 ohms | Rotor leakage inductance (Llr') | 0.002 H |
| Pole pairs (p) | 2 | Mutual inductance (Lm) | 0.07 H |

Table A.3 Parameters for practical implementation

| | | | |
|---|---|---|---|
| DC link capacitance | 3900 μF | DC Loop proportional gain | 1 |
| System frequency | 60 Hz | DC Loop Integral gain | 40 |
| Line inductance | 7.5 mH | Dc link voltage | 60V |
| Line resistance | 0.5 ohms | Load resistance | 90 ohms/65 ohms |
| Source peak voltage | 28V | Sampling frequency | 20 kHz |

Table A.4 Converter PCB circuit parameters

| | |
|---|---|
| C1, C2, C3 | 10uF/ 25 V |
| C4, C5, C6, C8 C9, C10, C11, C12, C13, C14, C15, C 16 | 0.1uF/25V |
| C7 | 0.01uF/25 |
| C18 | 100uF/400V |
| R1, R2, R3, R4, R5, R6 | 270 ohms |
| R6, R7, R8, R9, R10, R11, R12 | 33 ohms |
| R13, R14 | 200K ohms |
| R15 | 100 ohms |
| R16, R17 | 2K ohms |
| R18, R19 | 10K ohms |

Table A.5 Sensor board and analog board attenuation factors

| | |
|---|---|
| Line voltage attenuation (LV25-P) | $(V_{DSP}$ -1.5)*153.044 |
| Line current attenuation (LA55-P) | $(I_{DSP}$ -1.5)*6.37681 |
| DC voltage attenuation (HCPL 7840) | $V_{DC\text{-}DSP}$*137.034 |
| DC voltage attenuation (LV25-P) | $V_{DC\text{-}DSP}$*(116.814 adjusted to 112.92) |

# APPENDIX B.

# DESIGN LAYOUT AND CIRCUIT DIAGRAMS

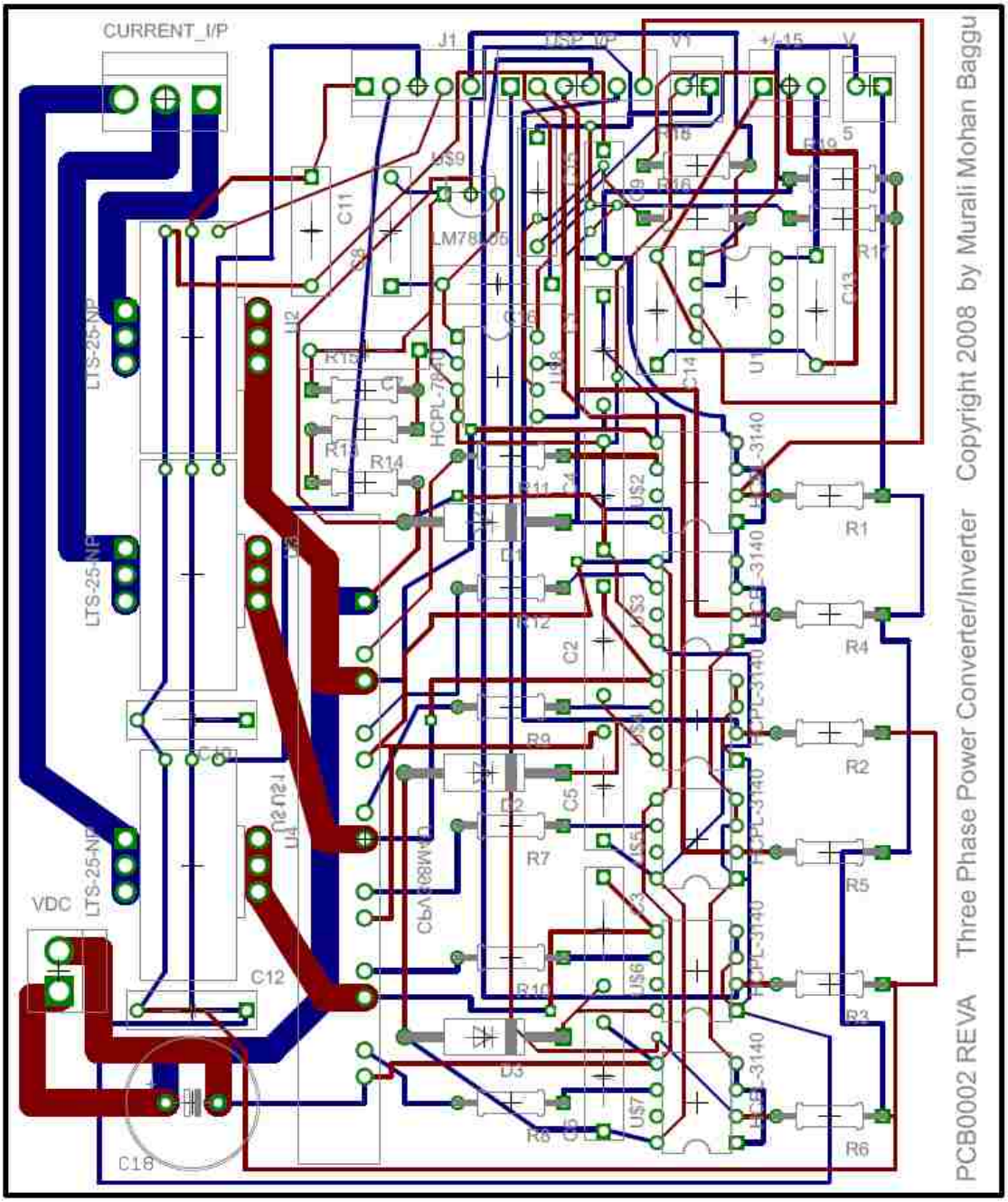


Figure B.1. Layout of the converter board designed in Eagle®

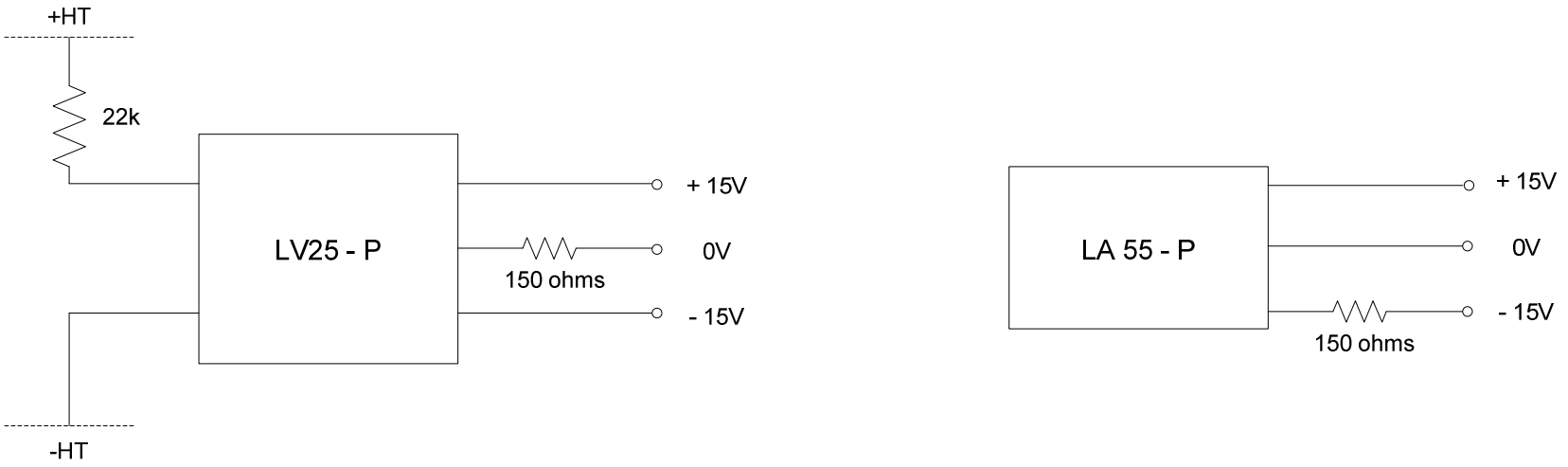


Figure B.2. Sensor board for tapping line voltage and line currents

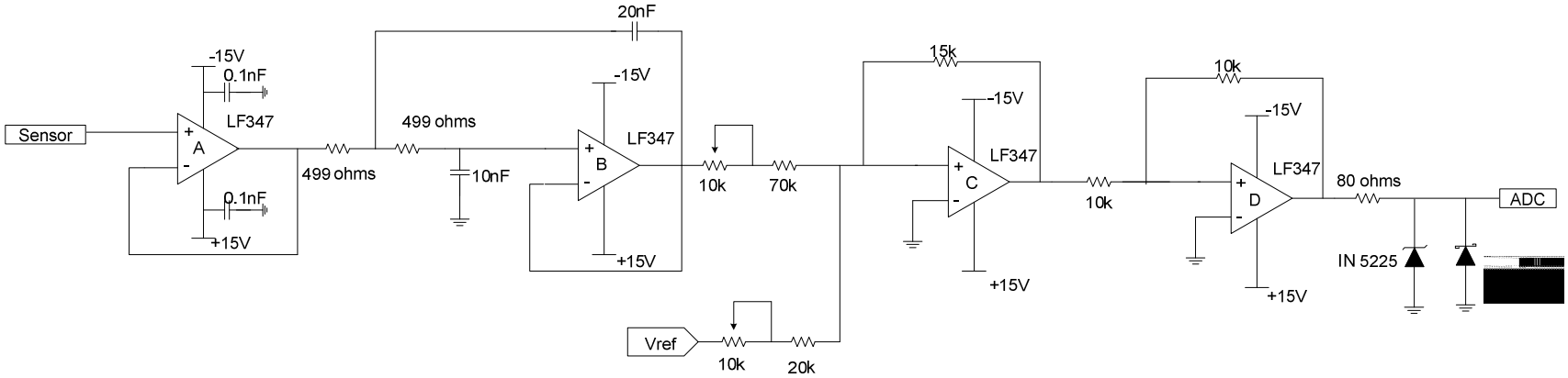


Figure B.3. Analog board circuit

# APPENDIX C.

# DSP CODE FOR PRACTICAL IMPLEMENTATION OF DPC

## MAIN C FILE

```
//*****************************************************************************************************
//Murali Mohan Baggu
//DPC Control Algorithm main.c
//Main consists of ADC call back and PWM Programming for EVA
//April 30 2009

#include "..\include\LF2812_Regs.h"
#include "..\include\RegDef.h"
#include "dpc.h"


void main(void)
{ Init_function();

        // initial App setting: stop, ret_val_mon, Sysclock, ....

        App.init(&App);

        //initialize adc setting
        adc.init(&adc);

        init_logger(); //initialize the data logger module

//====================================
// Space Vector PWM demo for EVA
//====================================

// Enable PWM pins
        EALLOW;
   GpioMuxRegs.GPAMUX.all = 0x003F; // EVA PWM 1-6  pins
   EDIS;

// Enable EVA clock
        SysCtrlRegs.PCLKCR.bit.EVAENCLK=1;

// Set HSPCLK to SYSCLKOUT = 150MHz
        EALLOW;
        SysCtrlRegs.HISPCP.all = 0;    // HSPCLK = SYSCLKOUT / 1 = 150MHz
        EDIS;

// Setup Timer 1 Registers (EV A)
   EvaRegs.GPTCONA.bit.T1TOADC = 0;            // configure GPTCONA not to start ADC on GPT1 Event
   EvaRegs.T1PR = 0x03A9;              // set GPT1 timer period (for 20kHz)
```

```
   EvaRegs.T1CNT = 0x0000;                    // reset GPT1 counter register

// set dead-band parameters
          EvaRegs.DBTCONA.all =  0x0AE4;      //          enable dead-band and set dead-time to 1us

// set Action Control Register.
  EvaRegs.ACTRA.all = 0x0666;                 // set initial vector in Action Control Register

// set value for compare units 1,2 register
          EvaRegs.CMPR1 = 0x03A8;
          EvaRegs.CMPR2 = 0x03A8;

// set GPT1 configuration register
          EvaRegs.T1CON.all = 0x0800; // timer in continuous up/down mode for symmetric PWM
          EvaRegs.T1CON.bit.TPS = 2;                  // Set clock prescaler to x/4 (T1 clock = 37.5MHz)

// set FCU control register
  EvaRegs.COMCONA.all = 0x1000;

// start PWM generation
          EvaRegs.COMCONA.bit.CENABLE = 1;    // enable compare operation
          EvaRegs.COMCONA.bit.FCOMPOE = 1;   // enable compare output pins
          EvaRegs.T1CON.bit.TENABLE = 1;              // Start GPT1 counter

  // Enable global Interrupts and higher priority real-time debug events:
          EINT;                                                       // Enable Global interrupt INTM
          ERTM;                                                            // Enable Global realtime
interrupt DBGM

          //Start timer to start ADC
          adc.start(&adc);

          EvaRegs.T2CON.bit.TENABLE = 1;              // Start GPT2 counter for ADC

 while (!App.stop)// test if user press Esc
          {

//Selection of Switching Vector by updating action control register and value for compare units 4,5 register
// 0666 = 000/111, 1666 = 100, 2666 = 010, 4666 = 001 and EvaRegs.CMPR1 = 0x03A8; EvaRegs.CMPR2 = 0x03A8;
// 3666 = 110, 5666 = 101, 6666 = 011, 7666 = 111/000 and EvaRegs.CMPR1 = 0x03A7; EvaRegs.CMPR2 = 0x03A8;

          if ((sector == 1)  & (Sp == 0) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x5666; EvaRegs.CMPR1 = 0x03A7;}
          if ((sector == 1)  & (Sp == 0) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x1666; EvaRegs.CMPR1 = 0x03A8;}
          if ((sector == 1)  & (Sp == 1) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x5666; EvaRegs.CMPR1 = 0x03A7;}
          if ((sector == 1)  & (Sp == 1) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x7666; EvaRegs.CMPR1 = 0x03A7;}
```

```
if ((sector == 2)  & (Sp == 0) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x1666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 2)  & (Sp == 0) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x3666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 2)  & (Sp == 1) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x7666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 2)  & (Sp == 1) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x7666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 3)  & (Sp == 0) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x1666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 3)  & (Sp == 0) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x3666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 3)  & (Sp == 1) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x1666; EvaRegs.CMPR1 = 0x03A8;}
 if ((sector == 3)  & (Sp == 1) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x0666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 4)  & (Sp == 0) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x3666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 4)  & (Sp == 0) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x2666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 4)  & (Sp == 1) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x0666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 4)  & (Sp == 1) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x0666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 5)  & (Sp == 0) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x3666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 5)  & (Sp == 0) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x2666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 5)  & (Sp == 1) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x3666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 5)  & (Sp == 1) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x7666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 6)  & (Sp == 0) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x2666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 6)  & (Sp == 0) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x6666; EvaRegs.CMPR1 = 0x03A7;}
 if ((sector == 6)  & (Sp == 1) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x7666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 6)  & (Sp == 1) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x7666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 7)  & (Sp == 0) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x2666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 7)  & (Sp == 0) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x6666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 7)  & (Sp == 1) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x2666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 7)  & (Sp == 1) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x0666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 8)  & (Sp == 0) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x6666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 8)  & (Sp == 0) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x4666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 8)  & (Sp == 1) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x0666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 8)  & (Sp == 1) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x0666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 9)  & (Sp == 0) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x6666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 9)  & (Sp == 0) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x4666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 9)  & (Sp == 1) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x6666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 9)  & (Sp == 1) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x7666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 10) & (Sp == 0) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x4666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 10) & (Sp == 0) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x5666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 10) & (Sp == 1) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x7666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 10) & (Sp == 1) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x7666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 11) & (Sp == 0) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x4666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 11) & (Sp == 0) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x5666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 11) & (Sp == 1) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x4666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 11) & (Sp == 1) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x0666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 12) & (Sp == 0) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x5666; EvaRegs.CMPR1 = 0x03A7;}
if ((sector == 12) & (Sp == 0) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x1666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 12) & (Sp == 1) & (Sq == 0)) {EvaRegs.ACTRA.all = 0x0666; EvaRegs.CMPR1 = 0x03A8;}
if ((sector == 12) & (Sp == 1) & (Sq == 1)) {EvaRegs.ACTRA.all = 0x0666; EvaRegs.CMPR1 = 0x03A8;}
```

```
            // call monitor
                        App.ret_val_mon = (*callmon2812)();
 }

            App.reset();
}

void Init_function()
{
            App.init=(void (*)(long))App_Init;
            App.reset=(void (*)(long))App_Reset;

            adc.init=(void (*)(long))ADC_Init;
            adc.start=(void (*)(long))ADC_Start;
}

void App_Init(MSK_APP* pApp)
{
            pApp->stop = 0;
            pApp->ret_val_mon = 1;

            adc.control.count_adc = 0;
            adc.control.count_saved = 0;
            adc.control.timer_period = 0x0753; //timer2 for adc sampling= 37.5M/20K= 1875 = x0753  count-up(write
error in EPC side after updaing)
            adc.control.ch_sel1 = 0x3210;
            adc.control.ch_sel2 = 0x0654;
            adc.control.ch_sel3 = 0;
            adc.control.ch_sel4 = 0;
            adc.control.max_ch = 6;        //16 total
}
void App_Reset()
{
// Generate system reset
            DINT;
            EALLOW;
            SysCtrlRegs.SCSR.bit.WDOVERRIDE =1; // Set WDOVERRIDE bit to allow the Watchdog enable
            SysCtrlRegs.WDCR = 0x000F;                        // Enable Watchdog and write incorrect WD Check Bits
                                                              // (001 in lieu of 101) to force a system reset
            EDIS;
}
//end of code
//***************************************************************************************************
```

## ADC C FILE

```
//*****************************************************************************************************
//Murali Mohan Baggu
//adc.c for Six channels on EVA
//April 29 2009

#include "dpc.h"

_iq18 IA, IB, IC, VDC, VA, VB, VC, delta_VDC, VDC_REF,Q_REF,P_REF, Tp, Iint,I_REF;
_iq18 Kp, Ki,Theta,P, Q, Valpha, Vbeta, Ialpha, Ibeta;
_iq18 pi, f2by3, f1bysqrt3, fpiby6, fpiby3,          fpiby2,f2piby3, f5piby6;
float Ia, Ib, Ic, Va, Vb, Vc, Vdc, p, q, theta, valpha, vbeta;
float thetaWatch[100], VaWatch[100], sectorWatch[100], P_ref, Q_ref;
int loop1;
Uint16 va,vb,vc,ia,ib,ic,vdc, counter, counter1, n_samples;
int Temp;

void ADC_Init(ADC_SET* pADC)
{
        Iint = _IQ18(0);
        Tp = _IQ18(0.00005); //50 us corresponding to 20kHz - time Period of the ADC controller.
        Kp = _IQ18(1);
        Ki = _IQ18(40);
        Sp = 0;
        Sq = 0;
        VDC_REF = _IQ18(60); // Check if the three phase voltages are corresponding to the command !!!
        Q_REF = _IQ18(0);
        sector = 0;
  pi = _IQ18(3.14159265358979);
  f2by3 = _IQ18(0.6666666667);
  f1bysqrt3 = _IQ18(.57735);
  fpiby6 = _IQ18(0.523599);
  fpiby3 = _IQ18(1.0462);
  fpiby2 = _IQ18(1.5708);
  f2piby3 = _IQ18(2.0944);
  f5piby6 =_IQ18(2.61799);


        // Enable ADC clock
        EALLOW;
  SysCtrlRegs.PCLKCR.bit.ADCENCLK=1;
  EDIS;

        AdcRegs.ADCTRL3.bit.ADCCLKPS = 3;    // ADCCLK = HSPCLK/6
```

```
        AdcRegs.ADCTRL1.bit.CPS = 0;                    // ADCCLK = HSPCLK/6
// Power up the reference and bandgap circuits
        AdcRegs.ADCTRL3.bit.ADCBGRFDN = 0x3;        // Power up bandgap/reference circuitry
        DELAY_US(DELAY8000);              // Delay before powering up rest of ADC
        AdcRegs.ADCTRL3.bit.ADCPWDN = 1;            // Power up rest of ADC
        DELAY_US(DELAY30);                // Delay after powering up ADC

// set Maximum Conversion Channels Register

        AdcRegs.MAXCONV.all = pADC->control.max_ch;  // Setup the number of conv's on SEQ1

// Setup stimultaneous sampling mode by Keyou
//        AdcRegs.ADCTRL3.bit.SMODE_SEL=1;

// Select Cascaded mode
        AdcRegs.ADCTRL1.bit.SEQ_CASC = 1;           // Cascaded mode

// Initialize ADC Input Channel Select Sequencing Control Register


        AdcRegs.CHSELSEQ1.all = pADC->control.ch_sel1; // Setup the 1st to 4th SEQ1 conv.
        AdcRegs.CHSELSEQ2.all = pADC->control.ch_sel2; // Setup the 5th to 8th SEQ1 conv.
        AdcRegs.CHSELSEQ3.all = pADC->control.ch_sel3; // Setup the 9th to 12th SEQ1 conv.
        AdcRegs.CHSELSEQ4.all = pADC->control.ch_sel4; // Setup the 13th to 16th SEQ1 conv.
        AdcRegs.ADCTRL2.bit.EVA_SOC_SEQ1 = 1;  // Enable EVASOC to start SEQ1
        AdcRegs.ADCTRL2.bit.INT_ENA_SEQ1 = 1;  // Enable SEQ1 interrupt (every EOS)
        AdcRegs.ADCTRL2.bit.INT_MOD_SEQ1 = 0;
}

void ADC_Start(ADC_SET* pADC)
{
// Assign ADC Interrupt Service Routine

        EALLOW; // This is needed to write to EALLOW protected registers
        PieVectTable.ADCINT = &adc_isr;
        EDIS;   // This is needed to disable write to EALLOW protected registers

// Enable ADCINT in PIE
  PieCtrlRegs.PIEIER1.bit.INTx6 = 1;

// Enable CPU Interrupt 1
   IER |= M_INT1;                       //Enable Global INT1

// Enable global Interrupts and higher priority real-time debug events:
//        EINT;                 // Enable Global interrupt INTM
```

```
//          ERTM;               // Enable Global realtime interrupt DBGM

// Configure EVA
// Assumes EVA Clock is already enabled
          EvaRegs.GPTCONA.bit.T2TOADC = 1;      // Enable EVASOC in EVA
          EvaRegs.T2PR = pADC->control.timer_period; // Setup period register
          EvaRegs.T2CNT = 0x0000;                         // reset GPT2 counter register
          EvaRegs.T2CON.all = TIM_CONT_UP; // timer in continuous up mode
          EvaRegs.T2CON.bit.TPS = 2;                      // Set clock prescaler to x/4 (T1 clock = 37.5MHz)
//          EvaRegs.T2CON.bit.TENABLE = 1;                  // Start GPT4 counter

}


//===========================================
// Timer 2 period interrupt service routine
//===========================================
interrupt void adc_isr(void)
{

          // disable all interrupt
          DINT;
          DRTM;

          vdc = AdcRegs.RESULT6 >>4;
          VDC = _IQ18(vdc);
          VDC = _IQ18mpy((_IQ18div(VDC, _IQ18(1365))), _IQ18(112.92));
          Vdc= _IQ18toF(VDC);

          vc = AdcRegs.RESULT5 >>4;
          VC = _IQ18(vc);
          VC = _IQ18mpy((_IQ18div(VC, _IQ18(1365)) - _IQ18(1.5)), _IQ18(153.044));
          Vc = _IQ18toF(VC);

          ia = AdcRegs.RESULT4 >>4;
          IA = _IQ18(ia);
          IA = _IQ18mpy((_IQ18div(IA, _IQ18(1365)) - _IQ18(1.5)), _IQ18(6.37681));
          Ia = _IQ18toF(IA);

          vb = AdcRegs.RESULT3 >>4;
          VB = _IQ18(vb);
          VB = _IQ18mpy((_IQ18div(VB, _IQ18(1365)) - _IQ18(1.5)), _IQ18(153.044));
          Vb= _IQ18toF(VB);

          ib = AdcRegs.RESULT2 >>4;
```

```
            IB = _IQ18(ib);
            IB = _IQ18mpy((_IQ18div(IB, _IQ18(1365)) - _IQ18(1.5)), _IQ18(6.37681));
            Ib = _IQ18toF(IB);

            va = AdcRegs.RESULT1 >>4;
            VA = _IQ18(va);
            VA = _IQ18mpy((_IQ18div(VA, _IQ18(1365)) - _IQ18(1.5)), _IQ18(153.044));
            Va = _IQ18toF(VA);

            ic = AdcRegs.RESULT0>>4;
            IC = _IQ18(ic);
            IC = _IQ18mpy((_IQ18div(IC, _IQ18(1365)) - _IQ18(1.5)), _IQ18(6.37681));
            Ic = _IQ18toF(IC);

 // Caluclation of P.Q, Valpha, Vbeta, Ialpha, I beta and Theta.
            P = _IQmpy(VA,IA)+_IQmpy(VB,IB)+_IQmpy(VC,IC);
            p = _IQtoF(P);
            Q = _IQdiv(_IQmpy((VB-VC),IA)+_IQmpy((VC-VA),IB)+_IQmpy((VA-VB),IC), _IQsqrt(_IQ(3)));
             q = _IQtoF(Q);
            Valpha = _IQ18mpy(f2by3,(VA-_IQ18div(VB,_IQ18(2))-_IQ18div(VC,_IQ18(2))));
            valpha = _IQ18toF(Valpha);
            Vbeta = _IQ18mpy(f1bysqrt3,(VB-VC));
            vbeta = _IQ18toF(Vbeta);
            Ialpha = _IQ18mpy(f2by3,(IA-_IQ18div(IB,_IQ18(2))-_IQ18div(IC,_IQ18(2))));
            Ibeta =  _IQ18mpy(f1bysqrt3,(IB-IC));

            Theta = _IQ18atan2(Vbeta,Valpha);
            theta = _IQ18toF(Theta);

//Sector Selection according tho the value of Theta.
   if ((_IQ18(0) <= Theta) & (Theta < fpiby6)){sector = 2;}
   if ((fpiby6 < Theta) & (Theta < fpiby3)){sector = 3;}
   if ((fpiby3 <= Theta) & (Theta < fpiby2)){sector = 4;}
   if ((fpiby2 <= Theta) & (Theta < f2piby3)){sector = 5;}
   if ((f2piby3 <= Theta) & (Theta < f5piby6)){sector = 6;}
   if ((f5piby6 <= Theta) & (Theta < pi)){sector = 7;}
   if ((-pi <= Theta) & (Theta < -f5piby6)){sector = 8;}
   if ((-f5piby6 <= Theta) & (Theta < -f2piby3)){sector = 9;}
   if ((-f2piby3 <= Theta) & (Theta < -fpiby2)){sector = 10;}
   if ((-fpiby2 <= Theta) & (Theta < -fpiby3)){sector = 11;}
   if ((-fpiby3 <= Theta) & (Theta < -fpiby6)){sector = 12;}
   if ((-fpiby6 <= Theta) & (Theta < _IQ18(0))){sector = 1;}

// DC Link Voltage control - PI Controller
  delta_VDC = VDC_REF-VDC;
```

```
  Iint = Iint + _IQ18mpy(_IQ18mpy(Ki,Tp), delta_VDC);
  if (Iint > _IQ18(10)){Iint = _IQ18(10);}
  if (Iint < _IQ18(-10)){Iint = _IQ18(-10);}
  I_REF = Iint+_IQ18mpy(Kp,delta_VDC);
  if (I_REF > _IQ18(7)){I_REF = _IQ18(7);}
  if (I_REF < _IQ18(-7)){I_REF = _IQ18(-7);}
  P_REF = _IQmpy(I_REF, VDC);
  P_ref = _IQtoF(P_REF);
  Q_ref = _IQtoF(Q_REF);

//Histeres Control
  if (P_REF > P) Sp = 1;
  if (P_REF < P) Sp = 0;
  if (Q_REF > Q) Sq = 1;
  if (Q_REF < Q) Sq = 0;

  if (counter1 < 100)
  {
   thetaWatch[counter1] = theta;
   sectorWatch[counter1] = sector;
   VaWatch[counter1] = Va;
            counter1++;
  }
            logger();

// Reinitialize for next ADC sequence
            AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;                       // Reset SEQ1
            AdcRegs.ADC_ST_FLAG.bit.INT_SEQ1_CLR = 1;    // Clear INT SEQ1 bit
            PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;                 // Acknowledge interrupt to PIE

            EINT;                // Enable Global interrupt INTM
            ERTM;                // Enable Global realtime interrupt DBGM
}


/*=====================================================================
==
 Delay Function
---------------------------------------------------------------------

 There is a 18/19 cycle overhead and each loop takes 14 cycles.
 The LoopCount is given by the following formula:

  DELAY_CPU_CYLES = 18 + 14*LoopCnt
```

```
 LoopCnt = (DELAY_CPU_CYCLES - 18) / 14

=============================================================================
*/
void Delay(unsigned long LoopCnt)
{
	unsigned long i;

	for (i = 0; i < LoopCnt; i++){}
//***************************************************************************************************
```

## GLOBAL DEFINITIONS C FILE

```
//***************************************************************************************************
//Murali Mohan Baggu
//GlobalVariableDef.c - Global Definitions for ADC and Main

#include "dpc.h"

MSK_APP App		;//= MSK_APP_DEFAULTS;
SPWM_SET	spwm	;//= SPWM_SET_DEFAULTS;
ADC_SET adc	;//=ADC_SET_DEFAULTS;

Uint16 sector;
Uint16 Sp;
Uint16 Sq;
//***************************************************************************************************
```

## DPC HEADER FILE

```
//***************************************************************************************************
/Murali Mohan Baggu
//dpc.h - Common Header File

#ifndef _DPC_H_
#define _DPC_H_

#include "..\include\LF2812_Regs.h"

#define	GLOBAL_Q		18
#include "..\include\IQMathLib.h"

#include "..\include\logger.h"

#define callmon2812 (int(*)(void)) 0x003f4000 // monitor's command interpreter
```

```
//define about timer
#define TIM_CONT_UP_DN          0x0800   //      timer in continuous up/down mode for symmetric PWM
#define TIM_CONT_UP             0x1000   //      timer in continuous up mode for asymmetric PWM

//-------------------------------------------------------------------------
// Used for calculating delays in micro-seconds:

#define CPU_CLOCK_SPEED      6.6667L   // ns/cycle for a 150MHz CPU clock speed
#define DELAY_US(A)  Delay(((((long double) A * 1000.0L) / (long double)CPU_CLOCK_SPEED) - 18.0L) / 14.0L)

//#define DELAY5000  5000L                  // Delay constant for 5 ms
//#define DELAY20 20L                       // Delay constant for 20 us
#define DELAY8000  8000L                    // Delay constant for 8 ms
#define DELAY30 30L                         // Delay constant for 30 us

void (*init)();
void (*start)();
void (*update)();
} PWMV_SET;

ADC_DATA;

typedef volatile struct {
Uint16 ch_sel1;                                     // Channel Select Control Register
Uint16 ch_sel2;                                     // Channel Select Control Register
Uint16 ch_sel3;                                     // Channel Select Control Register
Uint16 ch_sel4;                                     // Channel Select Control Register
Uint16 max_ch;                                      // Maximum Conversion Channels Register
Uint16 timer_period;                            // T2PR Register value
Uint16 count_adc;                               // counter of A/D made conversions
Uint16 count_saved;                                 // counter of A/D saved results
}ADC_CONTROL;

typedef volatile struct {
//Uint16                sampling_period;                        //T4PR Register value
ADC_CONTROL             control;
ADC_DATA                statcom;
ADC_DATA                sssc;
void (*init)();
void (*start)();
}ADC_SET;

typedef volatile struct{
Uint16     stop;                                                    // stop index (1 = stop)
```

```
Uint16     ret_val_mon;
void (*init)();
void (*reset)();
} MSK_APP;

//Program variables

/*---------------------------------------------------------------------------
 Extern Variables and function
---------------------------------------------------------------------------*/
// declaration
extern MSK_APP      App;
extern PWMV_SET pwmv;
extern ADC_SET      adc;
extern Uint16 res_buf[0x0100];                                          // A/D results
extern Uint16   sector;
extern Uint16   Sp;
extern Uint16   Sq;

void Init_function();// connect fun point to gobal variable

void App_Init(MSK_APP* pApp);
void App_Reset();

void PWMV_Init(PWMV_SET* pPWMV);
void PWMV_Start(PWMV_SET* pPWMV);
void PWMV_Update(PWMV_SET* pPWMV);

void ADC_Init(ADC_SET* pADC);
void ADC_Start(ADC_SET* pADC);

interrupt void adc_isr(void);
void Delay(unsigned long Count);
#endif     /* end of _DPC_H */
//*****************************************************************************************************
```

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