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SYSTEM AND IC LEVEL ANALYSIS OF ELECTROSTATIC DISCHARGE (ESD) AND ELECTRICAL FAST TRANSIENT (EFT) IMMUNITY AND ASSOCIATED COUPLING MECHANISMS

by

JA YONG KOO

A DISSERTATION

Presented to the Faculty of the Graduate School of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

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IN
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PUBLICATION DISSERTATION OPTION

This dissertation consists of the following three articles that have been submitted for publication as follows:

Pages 3-48 have been accepted in IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY

Pages 49-75 have been published in IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY*

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J. Koo, Q. Cai, G. Muchaidze, A. Martwick, K. Wang, and D. Pommerenke, "Frequency-Domain Measurement Method for the Analysis of ESD Generators and Coupling," *IEEE Trans. Electromagn. Compat.*, vol. 49, no. 3, pp. 504 – 511, Aug. 2007.

ABSTRACT

The exposure of electronic circuits to lightning, electrostatic discharge (ESD), electrical fast transients (EFT) or sine wave signals can reveal RF immunity problems. Typical problems include temporary malfunctions or permanent damage of integrated circuits (ICs). In an effort to reproduce those disturbances, a series of electromagnetic compatibility standards has been developed. However, a complete understanding of the root cause of the immunity problems has yet to be established. This dissertation discusses immunity problems in three papers, starting at the system level, via the coupling path into the IC. The first paper analyzes system level ESD testing, wherein a Round Robin test was conducted at three different locations to investigate ESD test repeatability. It allowed a correlation of parameters that describe the severity of an ESD generator with respect to failure levels observed in equipments under test (EUTs). The results demonstrate the importance of the transient field generated by ESD generators for obtaining test result repeatability and indicate narrowband coupling between the ESD generator and the EUT. The second paper presents and analysis of the coupling path. This method analyzes the coupling path under the assumption of linearity in the frequency domain. Further, it shows the limitations of the small signal assumption caused by the non-linear effects of active devices. The third paper analyzes the immunity of ICs against the noise generated from EFTs with emphasis on the power delivery network (PDN). A methodology for obtaining and analyzing a circuit model of PDN inside an IC is provided. The model includes the ESD protection diodes as well as passive elements between power and ground pins. This allows estimating the current sharing of different branches within the IC and an analysis of the reaction of ESD power rail clamp to overvoltage conditions.

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1. INTRODUCTION

Immunity problems arise when electronic circuits are exposed to a variety of disturbance sources, in particular, lightning, ESD, and EFT. Typical symptoms include temporary malfunctions or permanent damages on the ICs. As technology evolves towards higher density electronics and low-voltage operation, immunity problems are becoming more frequent with the same disturbance severity. Further, immunity plays a critical role in automotive electronics and motor control as well as the hand-held consumer electronics, which are all fast-growing electronics industries.

Traditionally EMC standards regulate the system level EMC performance, which led to traditional EMC approaches such as grounding and shielding. However, the demanding requirements of immunity performance, as mentioned before, can be difficult to fulfill by traditional EMC approaches. In the recent years, test standards have been expanded such that the IC level EMC performance can be quantified. Now a set of IC immunity test standards are available in the form of either a draft or a publication. However, these standards primarily deal with the artificial reproduction of the specific disturbing environments, i.e. ESD or EFT, while the research on logical analysis of the immunity problems is still premature.

This dissertation discusses immunity problems in three papers from different points of view. The first paper approaches immunity problems at the system level ESD testing from the macroscopic point of view. The Round Robin test, a world-wide experimental research project on ESD test repeatability, demonstrated that the transient field generated by ESD generators has a significant influence over the failure level for various equipments under test (EUTs). The correlation coefficient employed in the analysis of lab measurement results quantifies the correlation between ESD parameters and EUT failure levels.

The importance of the transient field is investigated in the second paper. The estimation of transient field coupling from an ESD generator to the susceptible components in a given EUTs can be achieved using a vector network analyzer. The method presented evaluates the linear field coupling in a frequency domain small-signal analysis. As the usual disturbance sources have large magnitudes in their instantaneous

power, the non-linear characteristics of active devices also need to be considered. The primary concern would be the ESD protection scheme, wherein the clamping against a severe disturbance occurs, in the IC.

A circuit model of the power delivery network in an IC is introduced in the third paper. The model includes the ESD protection diodes as well as passive elements between power and ground pins. The nodes in the model properly separate the internal transient current into different branches. The current flowing to the ESD power rail clamp is estimated as an application of the model.

PAPER 1

CORRELATION BETWEEN EUT FAILURE LEVELS AND ESD GENERATOR PARAMETERS

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ABSTRACT

Some system level ESD tests repeat badly if different ESD generators are used. For improving repeatability, ESD generator specifications have been changed and modified generators have been compared in a worldwide Round Robin test. The test showed up to 1:3 variations of failure levels. Multiple parameters that characterize ESD generators have been measured. This paper correlates the parameters to test result variations trying to distinguish between important and non relevant parameters. The transient fields show large variations among different ESD generators. The voltage induced in a semi-circular loop and the ringing after the first discharge current peak show the best correlation to failure levels. The regulation on the transient field is expected to improve the test repeatability.

Keywords

Correlations, electrostatic discharge, failure levels, Round Robin test

I. INTRODUCTION

The objective of system level ESD testing is two fold: ensuring adequate robustness of electronic systems against real world ESD and passing a standardized test as this is often a legal or company's internal requirement for selling a product. When passing a legal requirement an unambiguous pass/fail determination is required. However, it is well known that all EMC tests suffer from reproducibility problems. This is especially true for ESD testing [1]-[4]. When measuring emissions a test result uncertainty can be calculated, however, the standardization groups have only attempted to determine a calibration uncertainty for ESD testing, and have shied away from attempting to establish methods for test result uncertainties for ESD testing.

Owing to the large variation nature of the natural ESD phenomena, a reference ESD event has been introduced in the standard, IEC 61000-4-2 [5]. This document describes the discharge current waveform. In the early 1990's testing has been moved from air discharge to contact mode testing to avoid the effect of arc length variations in air discharge [6] and to improve reproducibility. In spite of this and other steps taken to improve the reproducibility of test results, variations as much as by a factor of 2 in passing test voltage are common. Thus, the site-to-site variation of test result often leads to regulatory problems and may cause redesigns for improving the product's immunity if an EUT turns out to be especially sensitive to a specific model of ESD generators used at that test site.

A standard needs to regulate the parameters that determine the severity of the tests. However, there has been and still is considerable confusion about which parameters determine the severity of ESD testing. Traditionally the effort to improve the test

repeatability has been focused on defining the right discharge current [7]-[8]. This thought guided the standard formulation in its early stage, resulting in the four parameters that define the discharge current specification [5]: rise time, peak current, current at 30 ns and current at 60 ns. Two reasons may have turned the focus to the current, while paying little attention to the fields: The current can be measured with high precision [9] and the belief that the rise time is directly related to the probability of system failure [10]-[11].

Questioning the parameters that determine the severity of system level ESD led to multiple studies having inconsistent and even partially contradicting results. In [11] it was shown that the coupled energy is related to the rise time. The authors of [3] concluded that the high frequency components or the current derivatives dominate simulator severity while our own previous study claimed that the voltage induced in a small loop predicts the severity level for upset type failures [12]. Many studies have indicated that the transient fields of ESD strongly influence the EUT response. However, an often met misunderstanding is that the transient fields of the ESD generator are determined by the discharge current. If this is the case, a well written specification of the discharge current would define the transient fields.

A simple dipole model [13]-[14] often assumes a short line current which carries the current of a human-metal ESD. According to this model it can be used to calculate the transient fields. The limitations of the model have been shown to originate from omitting the field contributions from the complete geometry and not taking into account that within the ESD generator much shorter rise time currents are present [15].

However, an ESD event by an ESD generator has critically different characteristics from the human ESD model.

- The ESD energy is stored in a small discrete capacitor.
- A ground strap is used for the current return path.
- The pulse shaping network is used to smooth the discharge current.

It is true that the transient field variation is partially due to the discharge current variation, however, the differences listed above also cause other uncertainties in the transient field. Therefore, even if all ESD generators could have identical discharge current, the transient fields may be significantly different. Then what would be the correct way to represent the field radiation?

It has been known that the transient fields are different among ESD generators from different manufacturers [2], [6]. The voltage induced in a small loop was used as a simple indicator of the transient field and a correlation to the failure levels was found in some limited conditions [16]-[17]. However, if the field distribution is not uniform over the revolution angle [3], [18]-[19], then the transient field coupling to the EUT depends not only on the manufacturing but also on the revolution angle that faces the EUT, which leads to a clear failure level variation with respect to the revolution angle (see Section II).

In spite of numerous factors that would possibly affect the severity of ESD generators, TC77B, the technical group in charge of IEC 64000-4-2, investigated adding another discharge current specification as can be seen in Fig. 1. The specification states that the width is measured at 60% of the first discharge current peak and should be 1.5 to 3.5 ns.

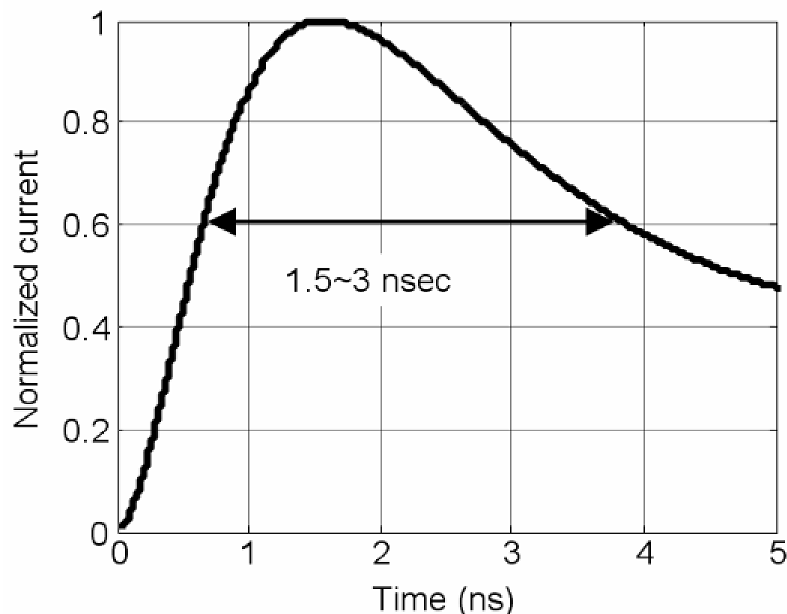


Fig. 1. New specification suggested for discharge current waveform. The width measured at 60% of the first discharge current peak should be 1.5 to 3 ns.

A Round Robin test was initiated to test the effect of this change on different EUTs, at three locations (EHC Tokushima lab. in Japan, Missouri University of Science and Technology in Rolla, and IBM in Minnesota) using the same ESD generators. Various EUTs, such as desk top computers, laptop computers, printers, wireless routers, and projectors, were used. The measurements were performed in accordance with the standards [5]. The contact mode using direct discharge was used to minimize test uncertainty. The detailed test methods are described in [4].

The Round Robin test results showed that the proposed regulation shown in Fig. 1 improved little on the test repeatability. Consequently the IEC 77b MT12 ESD standard setting working group decided not to include this specification into the standard IEC 61000-4-2. Besides the test repeatability evaluation, we characterized the ESD generators with respect to their discharge current and fields. These parameters can be used to study the correlation of the failure levels to the ESD parameters.

Section II introduces the failure levels and the variations of various EUTs. Section III presents the measured ESD parameters, including the discharge currents and voltages induced in a semi-circular loop. Section IV discusses the frequency selective immunity of the EUTs and the general correlation between the ESD parameters and the failure levels over all EUTs and Section V compares the modified and unmodified ESD generators.

II. EUT FAILURE LEVELS

The failure levels of desktop and laptop computers, servers, routers, etc. were determined using the contact mode.

Analyzing a complex set of partially imperfect data requires a set of assumptions that are discussed in this section. We have tested the stability of our results and conclusions against these and other reasonable assumptions and found them to be consistent with our assumptions.

Some EUTs had multiple test points spaced far from each other. In this case we assumed that the coupling path and failure cause was different, allowing us to regard each new test point as an independent EUT. A charge voltage of 10 kV was the maximum for most ESD generators. A few EUTs didn't fail up to 10 kV. In this case we assumed a failure level of 12kV.

Each of the recorded failure levels for an EUT using eight different ESD generators was normalized to the lowest failure level such that the relative failure level variations could be seen. Fig. 2. Normalized failure levels for fourteen EUTs while (a) positive voltage discharges and (b) negative voltage discharges were performed using eight ESD generators. The lowest failure level for each EUT was used for normalization. EUT 10 (rarely failed up to 10kV) and EUT 13 (indirect discharge) were excluded.

shows the normalized failure level for the positive and negative voltage discharge respectively. The variations were strongly dependent on the EUT, ranging from 1:3 down to 1:1.5. The data is sorted such that the EUTs having large variations in the failure level are shown on the left side.

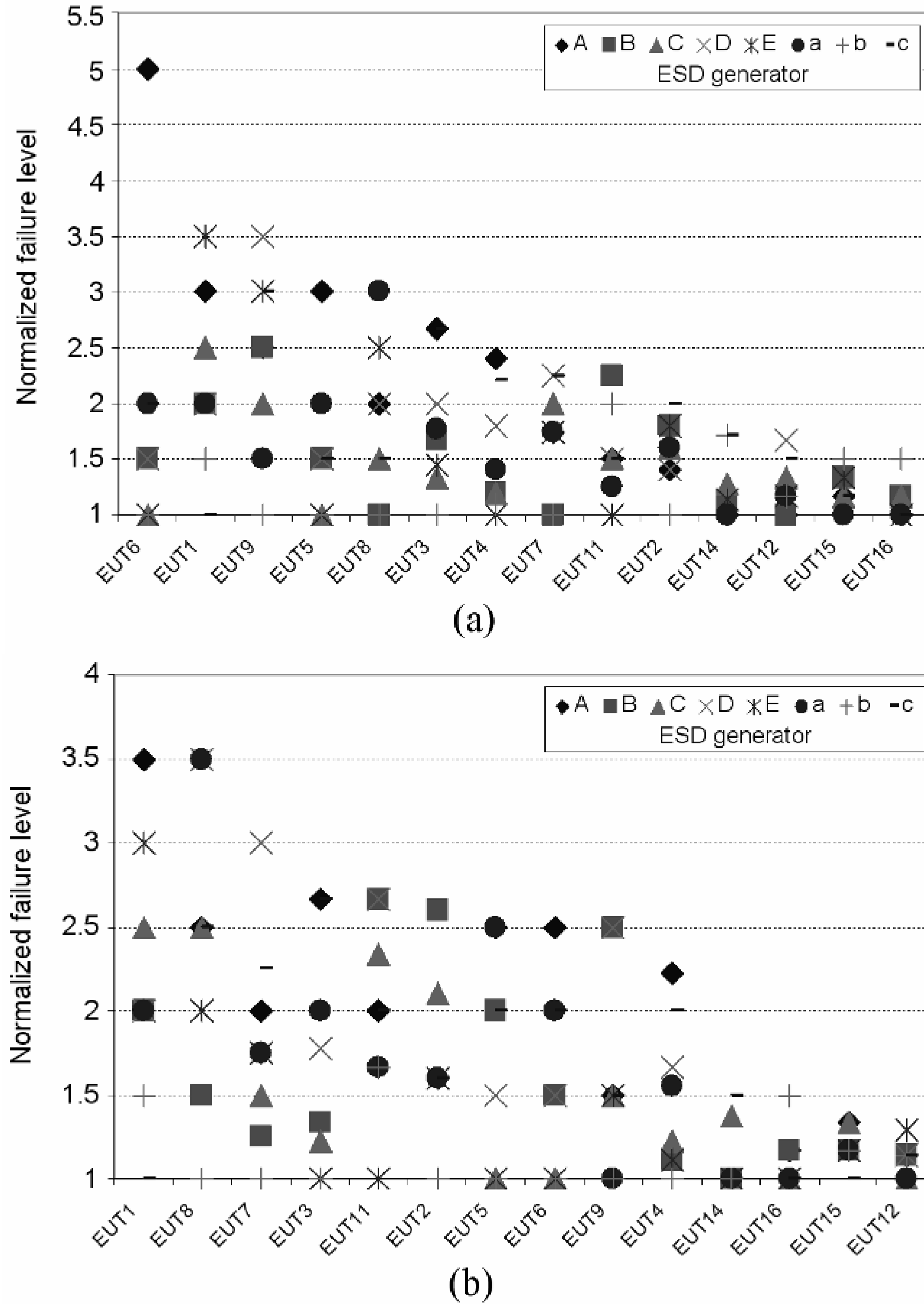


Fig. 2. Normalized failure levels for fourteen EUTs while (a) positive voltage discharges and (b) negative voltage discharges were performed using eight ESD generators. The lowest failure level for each EUT was used for normalization. EUT 10 (rarely failed up to 10kV) and EUT 13 (indirect discharge) were excluded.

ESD generators are not bodies of revolution. To observe if a non-uniform transient field distribution around the ESD generator causes a failure level variation, the

ESD generators were held at four different angles while the failure levels of the EUT were recorded. TABLE I shows examples of the variations of failure levels at four different revolution-angles of the ESD generator. A failure level variation of 1 : 1.5 was observed for EUT 4 while discharging with 'generator a'. Rotation was only performed on a very few number of EUTs and only using few ESD generators, as it was not part of the Round Robin test protocol.

The injected current remains unchanged if the generator is rotated, however the fields will change. The variation indicates the importance of the transient fields and shows that even when using one generator there can be repeatability problems.

TABLE I

Measured Failure Levels at Different revolution-Angles of the ESD Generator

	Failure levels at each revolution-angle of ESD generator (kV)				Variation (max. failure level : min. failure level)
	0 deg.	90 deg.	180 deg.	270 deg.	
Generator a / EUT 3	8	8	8	7	1 : 1.1
	-8	-8	-10	-10	1 : 1.3
Generator a / EUT 4	7	9	7	6	1 : 1.5
	-8	-8	-10	-8	1 : 1.3

III. MEASUREMENTS OF ESD PARAMETERS

Five of the ESD generator manufacturers supported the Round Robin test by providing ESD generators which meet the proposed new current requirement specifying the width of first discharge current. These generators are denoted by capital letters,

'Generator A' to 'Generator E', in the measurement results. Three of these manufacturers also provided their old versions, which didn't meet the new current requirement, 'Generator a' to 'Generator c'. 'Generator D' and 'Generator E' don't have corresponding old versions because they have already met the new current specifications. We measured the parameters to characterize the ESD generators and to correlate the parameters to failure levels. The general measurement methods and results are introduced in this section. A full wave ESD generator model for discharge current and field coupling estimation is shown in [20].

A. Discharge Currents

The discharge current from each ESD generator was measured in accordance with the standards [5] with the time span of 200 nanoseconds. As shown in Fig. 3, the measured discharge currents meet the four parameters of the discharge current specification in general. However, the current waveforms after the first peak deviate significantly. The spectra differ by more than +/- 6 dB below 2.5 GHz, as can be seen in [4].

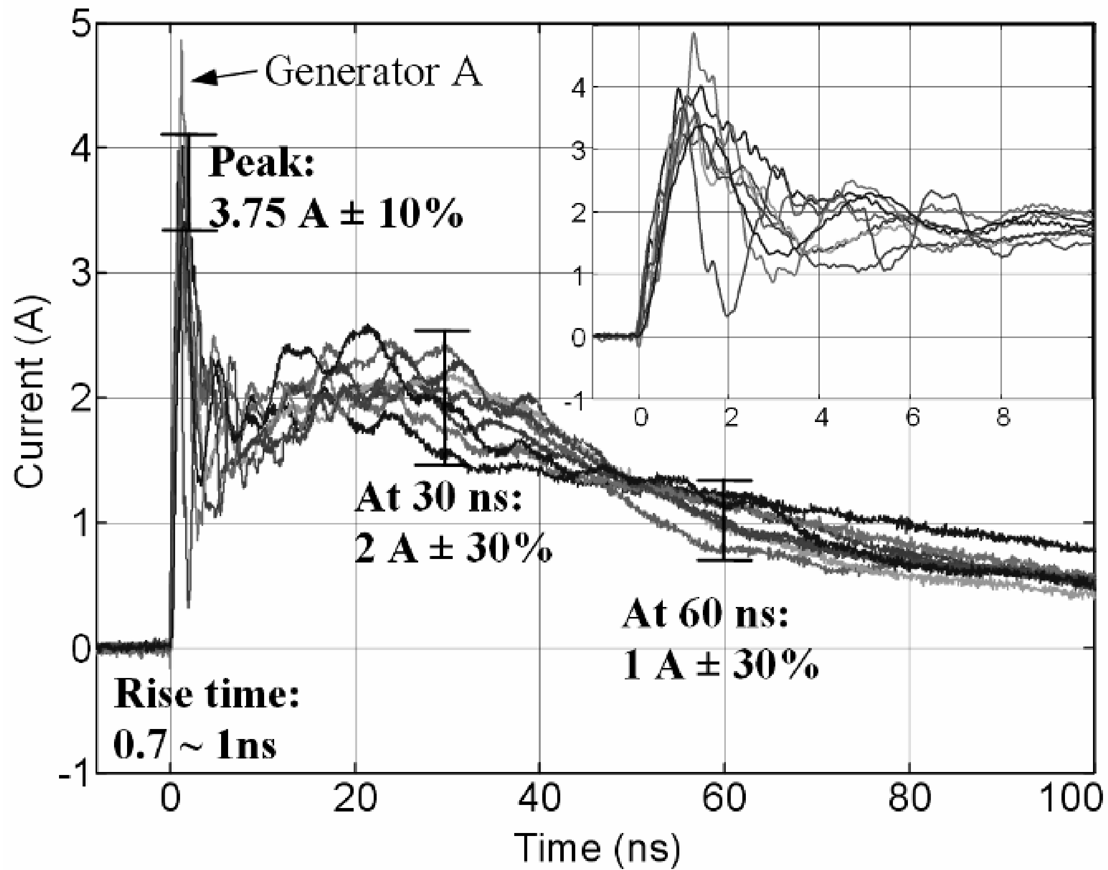


Fig. 3. Discharge currents measured for the Round Robin test. Eight different ESD generators were used. The four parameters of the discharge current specifications are indicated. The upper-right plot shows the first 10 ns.

B. Induced Voltages in a Semi-Circular Loop

To observe the transient field from the ESD generators during discharge, the induced voltages in a small loop have been measured with the time span of 50 nanoseconds. The measurement setup is depicted in Fig. 4.

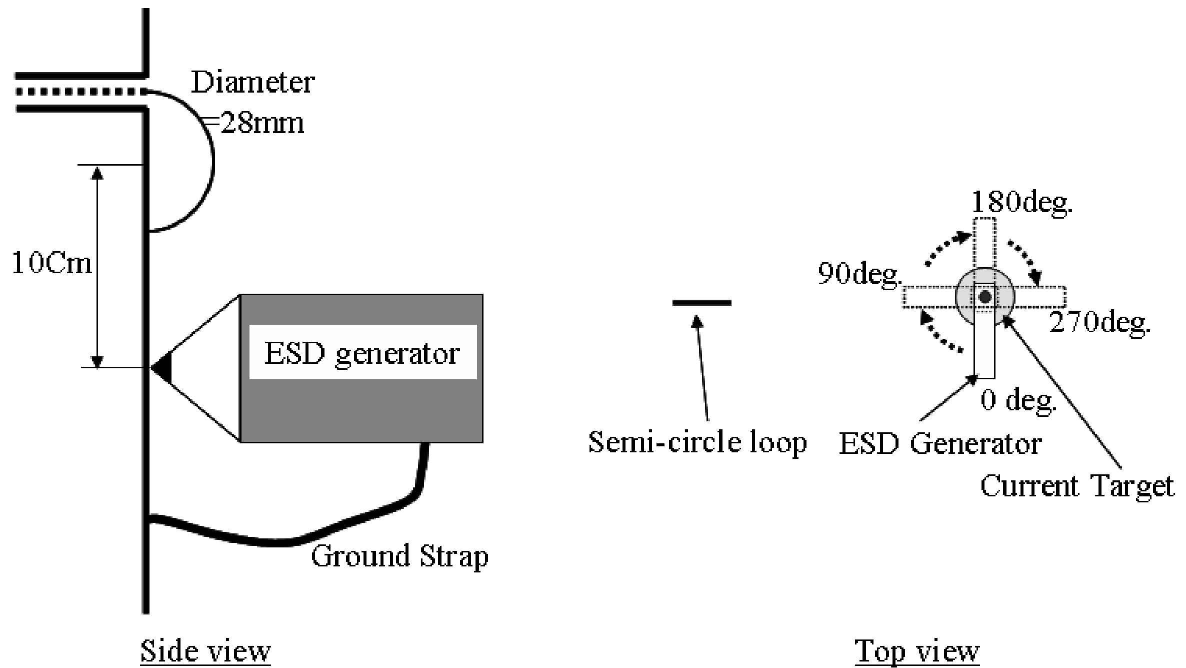


Fig. 4. Measurement setup for the induced voltages in a semi-circular loop. The ESD generators that were used were rotated around the discharge tip. The induced loop voltage was measured at four angles.

A semi-circular loop (28 mm diameter, 0.7 mm wire diameter) was placed on a ground plane (approximately 4 m by 2.5 m) and connected to an oscilloscope (6 GHz, 20 Gs/sec). The discharge location is 10 cm from the center of the semi-circular loop. A distance of 10 cm was selected as the IEC 61000-4-2 standard requires the same distance for indirect ESD testing. Full-wave simulations of the voltage induced in a semi-circular loop by an incident plane wave were conducted. The frequency responses are shown in Fig. 5.

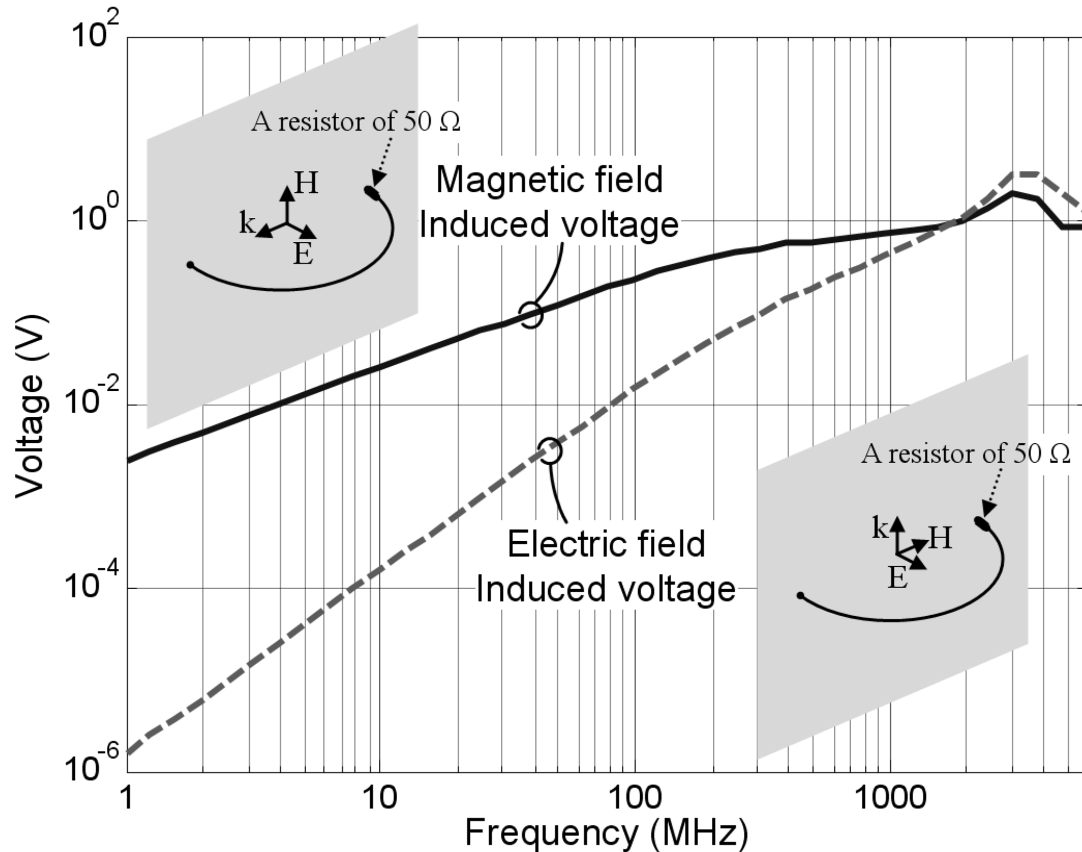
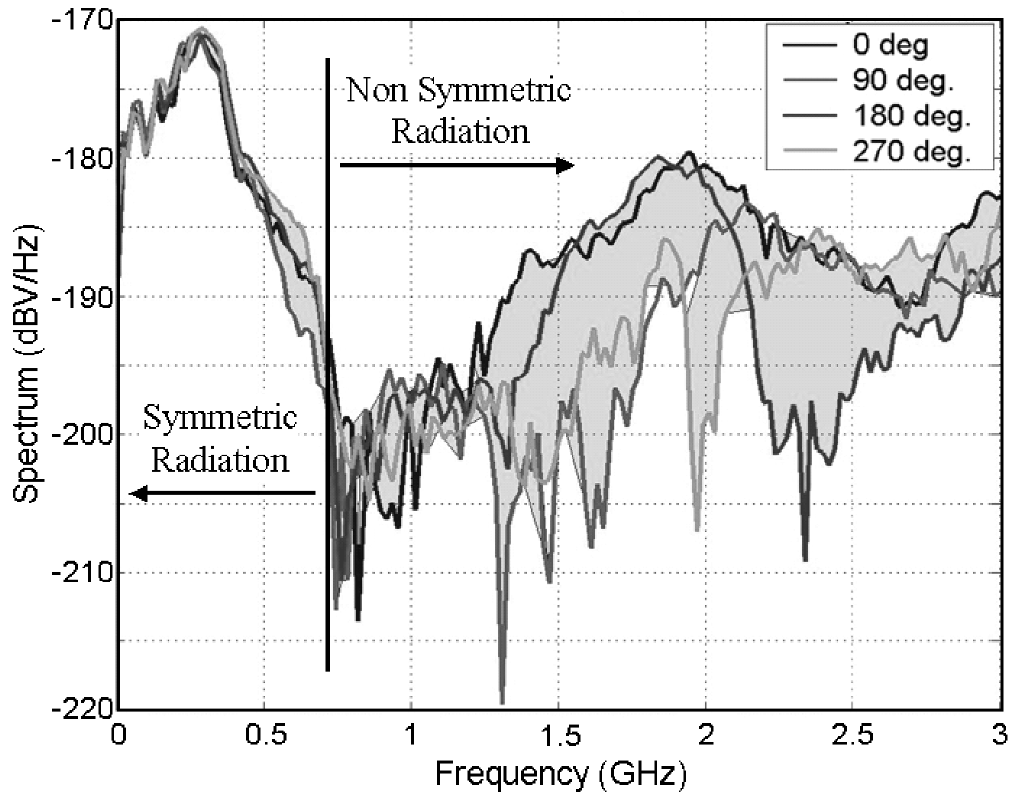
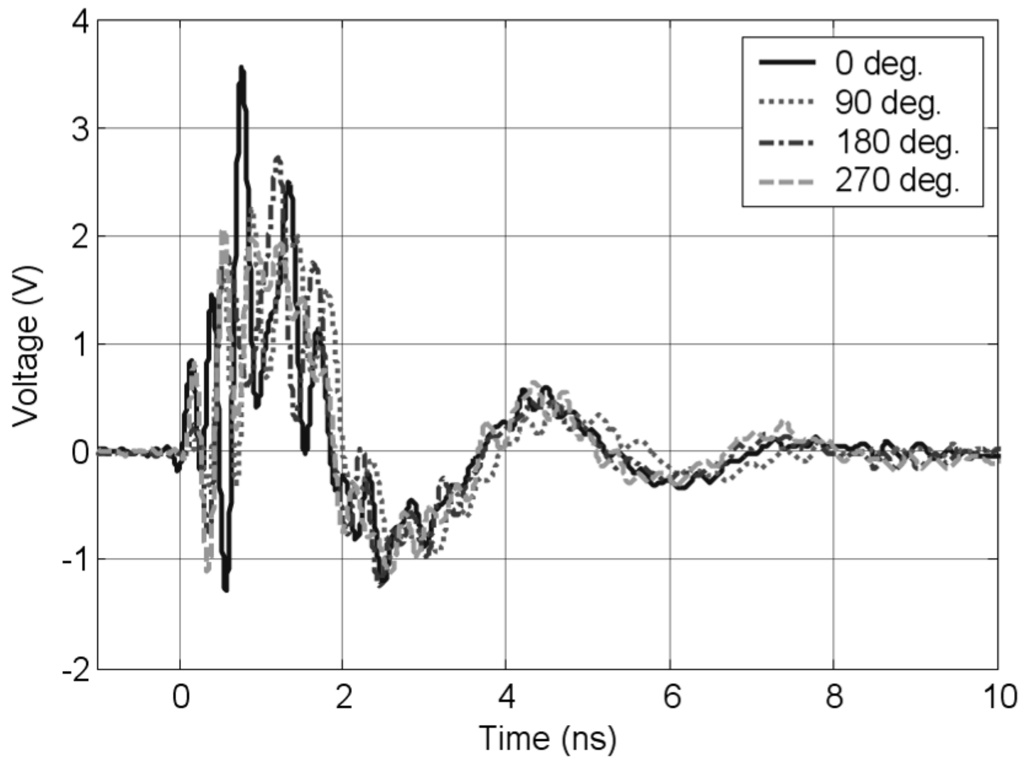


Fig. 5. Frequency responses of the voltage induced in a semi-circular loop by an incident plane wave (E = 377 V/m, H = 1 A/m). Two polarizations were used in each of full-wave simulations.

The ground strap, which is about 3 m long in general, was pulled back to its midpoint. The ESD generators that were used were rotated around the discharge tip, as can be seen in the right side of Fig. 4, maintaining the overall shape of the ground strap. The current of the ESD generator is hardly affected by rotating it. However, the transient fields are, as most ESD generators do not form bodies of revolution. For capturing the effect of these asymmetries we recorded the induced loop voltage for four orientations of the ESD generators. For example, the spectra and the time domain waveform of the measured induced voltages in a semi-circular loop for 'Generator a' are shown in Fig. 6.



(a)

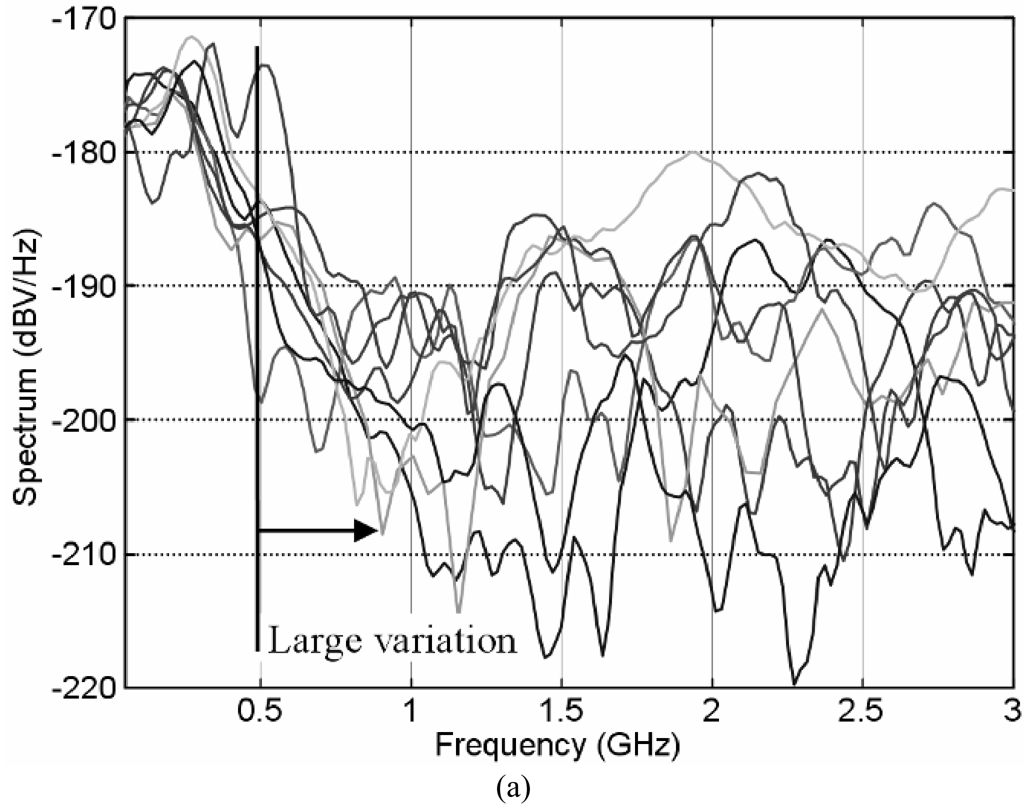


(b)

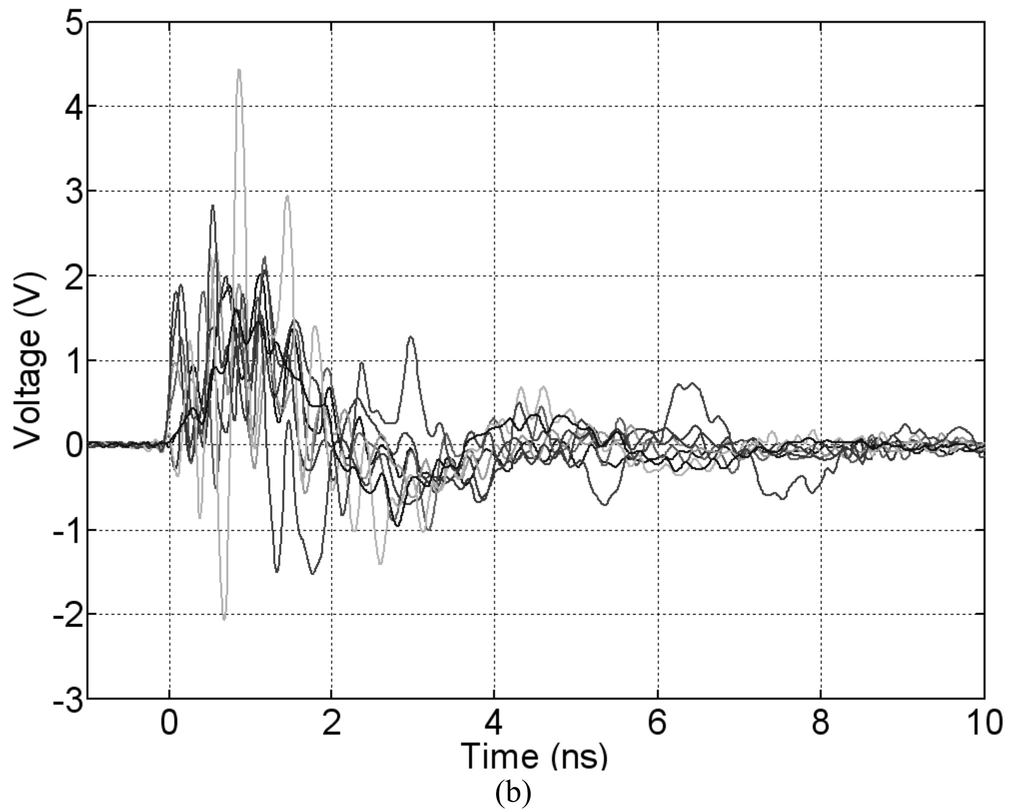
Fig. 6. A set of (a) spectra and (b) time domain waveforms of measured induced voltages in a semi-circular loop for 'Generator a'.

Within the spectrum of the induced voltage in a semi-circular loop one can distinguish two regions. In the lower frequency ranges, the rotation effects are less seen in the spectrum. In the higher frequency ranges, we observe strong variations due to the angle of the rotations. For 'Generator a' and a 10 cm loop distance, the transition occurred at about 700 MHz, other generators showed transition frequencies between 250 MHz and 800 MHz.

This can be explained as follows: In the lower frequency ranges the induced loop voltage is dominated by the fields from the discharge current which is not affected by rotating the ESD generator. The higher frequency components are caused by the relay that initiates the ESD pulse in the contact mode. The voltage collapse time in the relay is less than 100 ps. Thus, a pulse forming network is needed to shape the discharge current into a standard waveform [16]. The currents flowing on this pulse forming network, the relay and the metallic structures in proximity, are not symmetric. Therefore, the currents within the ESD generator will generate non-symmetric transient fields, while the discharge current flowing through the discharge tip generates the symmetric transient field around the ESD generator. This is observed as 'Symmetric radiation' indicated in Fig. 6 (a) in low frequency range. Fig. 7 shows how strong the spectra and the time domain waveform of the induced voltage vary among different ESD generators. As expected, the variation is larger in the high frequency ranges.



(a)



(b)

Fig. 7. (a) Spectra and (b) time domain waveforms of measured induced voltages in a semi-circular loop for eight ESD generators at 0 degree of revolution-angle.

C. Electric Fields

A broad-band electric field sensor [21] was placed on the ground plane at a distance of 0.1 m from the discharge point and the transient electric fields were measured with the time span of 1 microsecond. The electric field sensor has a high pass nature with the cutoff frequency of 4 MHz. The ESD generators were held at 4 different angles, the same as was measured for the induced voltage in the semi-circular loop. The transient electric fields also show a variation over rotation angles, but the variation is not as strong as that of the voltage induced in a semi-circular loop. The E-field sensor has a flat frequency response from about 2 MHz – 2 GHz, while the loop emphasizes the stronger varying high frequency content. Typical waveforms of the transient electric field are shown in [16].

IV. Correlation analysis

Multiple parameters describe an ESD event; starting from electrostatic parameters like charge up to the GHz spectral components. Only the parameters that determine the severity need to be regulated by an ESD standard. However, which parameters should be regulated? During the Round Robin we observed the failure levels for a diverse set of EUTs and recorded parameters that characterize the ESD generators. It is a logical step to investigate the correlation between the failure levels and the parameters. We attempted to extract as much general information as possible using a large, but far from perfect data set.

A. Method

To illustrate the principle, let us assume an EUT is selectively sensitive to only one ESD parameter and let it be the peak current. If this EUT is tested using a set of ESD generators that differ in their peak current, then we would observe a disproportional relationship between the peak current and the failure level. The correlation analysis searches for a linear relationship between the severity of an ESD generator and the reciprocal failure level. We quantify this using the correlation coefficient ($-1 \leq \rho \leq 1$), where a 1 indicates the strongest correlation [22]. Please see the appendix for the details about these methods.

In reality matters are more complex. A weighted combination of these parameters determines the failure level of an EUT. However, the weighting factors are EUT dependent. For example, one EUT may not react at all to spectral components higher than 100 MHz, but another may have a shield that can only be penetrated by spectral contents higher than 2 GHz. Also, the parameters are not mutually independent. For example the distributed current derivative over all conducting parts of an ESD generator causes the transient magnetic field. The current derivative at the tip of the generator contains only a fraction of the transient field greater than 1 GHz. But, this derivative is certainly part of those currents that cause the transient field. Thus, both parameters are related. A similar argument is valid for other parameters.

B. Extracting ESD Parameters

The underlying disturbance model assumes that a EUT fails if the peak noise level induced into some circuit exceeds a certain threshold level. The noise is caused by one or a combination of many ESD generator parameters. For the correlation analysis, various

peak-to-peak values of ESD parameters were extracted from the measured data; discharge currents, induced voltages in a semi-circular loop, and electric fields.

Another simplification is we assume that there are no cumulative effects. These effects could be of an electrical nature, e.g., heating, or from the lack of charge removal from previous pulses or software related, like the accumulation of bit errors.

Obvious parameters are the peak current and the discharge current derivative. The ESD generator current waveforms often differ in a highly visible fashion during the decay after the initial peak [3]. The currents may fall very rapidly or ring. The ringing is often caused by structural resonances leading to frequencies in the middle range from 200 to 800 MHz. Enforcing a smooth current decay after the first discharge current peak has been introduced into the discussion of the standardization as a measure of improving test result repeatability. To test if this frequency range of the current correlates to failure levels we defined the peak-to-peak of a band-passed current (200-800 MHz) as a parameter.

The transient fields will induce noise in the loop or monopole like structures. Based on this and previous publications [16], the standardization committee introduced the voltage in a ground plane mounted semi-circular loop as a way to characterize the transient fields of ESD generators [5]. Besides the simplicity of the test setup, other arguments for including this specification had been the availability of the data not only on ESD generators, but on the human-metal ESD event, which forms the event that the standard tries to reproduce.

Transient field magnitudes have also been selected as a parameter. However, they do not describe the nature of the induction process as well as the voltage induced in a loop.

The problem of the large variation of ESD test results had been known prior to the Round Robin and it initiated the maintenance work on IEC 61000-4-2 that eventually led to the Round Robin testing. If we assume a linear relationship between parameters and the reciprocal failure levels it is logical to search for parameters that differ strongly between ESD generators. For example, test result variations of 1:3 had been observed previously [4], but the peak currents of different ESD generators that fulfill the standard vary only by +/-10%. Thus, the peak current is not a suitable parameter to explain the observed variation ratio of 1:3.

The spectrum of the discharge current derivatives, the electric fields, and the induced voltages in a semi-circular loop show larger variation in the higher frequency range than in the low frequency range (<500 MHz). Therefore we created high and low-pass filtered parameters to search for a correlation.

The peak-to-peak values taken from the various ESD parameters explained above are summarized in Table II. Table III describes the symbols that describe the ESD parameters and data processing. Also, Fig. 8 explains how measured data were processed to obtain the ESD parameters used in the correlation analysis.

TABLE II

ESD parameters measured at 1 kV

ESD generator	Discharge current related		Transient field related		
	I_p (A)	$I_{BP,\ p\text{-}p}$ (A)	$(di/dt)_{p\text{-}p}$ (A/ns)	$V_{Loop,\ p\text{-}p}$ (V)	$E_{p\text{-}p}$ (V/m)
A	4	1.8	10.7	2.8	512.6
B	3.6	1.5*	9	3.2	684.5**
C	3.2*	1.5	6.8*	2.5	428.7*
D	3.6	1.6	12	3	514.6
E	3.9	1.8	8.3	3.7	567.4
a	4.9**	2.3**	14.7**	5.2**	554.4
b	3.7	2.1	13.3	4.1	637.9
c	3.5	1.6	8.1	2.3*	549.7
Variation Ratio (max./min.)	1.5	1.5	2.2	2.3	1.6

** maximum value, * minimum value

- Average values over 4 different angles were taken for V_{Loop} and E
- variation ratio: max(values over all ESD generators) / min(values over all ESD generators)

Note: The ‘Generator a’ in Table II has exceeding values in most parameters while not always causing low failure levels. This effect is also considered in part D.

TABLE III

Glossary for ESD parameters used in correlation analysis

ESD parameter symbols	
I	Discharge current
(di/dt)	Discharge current derivative
V_{Loop}	Induced voltage in a semi-circular loop
E	Transient electric field
Data processing symbols (subscripts after ESD parameter symbols)	
LP	Low-pass filtering (<500 MHz)
HP	High-pass filtering (>500 MHz)
BP	Band-pass filtering (200~800 MHz)
p	Peak detection
p-p	Peak to peak detection
BP(*)	Band-pass filtering at sweeping center frequency from 50 MHz to 3 GHz with a Q factor of 5 %. A 3rd order Butterworth filter was used.
BP(*freq.*)	Band-pass filtering at center frequency of *freq.* with Q factor of 5 %. Butterworth filter of order of 3 was used

- A 1st order Butterworth filter was used for LP, HP and BP filtering process in MATLAB.
- Examples (also see Fig. 8)
  - $(di/dt)_{HP,\ p\text{-}p}$: A column vector of peak to peak values of high-pass filtered (> 500 MHz) discharge current derivatives. Each row corresponds to a specific ESD generator.
  - $I_{BP(500MHz),\ p\text{-}p}$: A column vector of peak to peak values of band-pass filtered discharge currents at the center frequency of 500 MHz with Q factor of 5%. Each row corresponds to a specific ESD generator. Butterworth filter of 3rd were used.
  - $I_{BP(*),\ p\text{-}p}$: A matrix whose columns indicate peak to peak values of band-pass filtered discharge currents with a Q factor of 5 % at a certain center frequency between 50 MHz and 3 GHz. Each column corresponds to a center frequency. Each row corresponds to a specific ESD generator. 3rd order Butterworth filter was used.

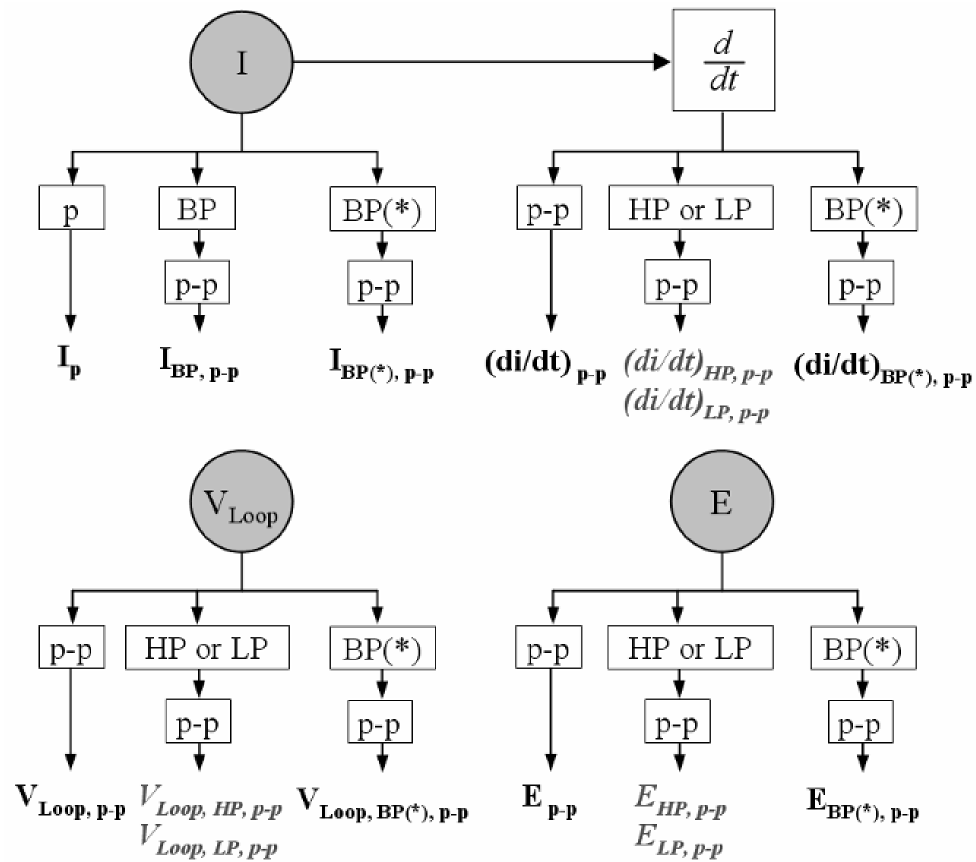


Fig. 8. ESD parameter trees. The shaded circles indicate unfiltered raw data and the rectangles indicate the data processing introduced in Table III.

Italic fonts used in Fig. 8 indicate high or low-pass filtered parameters. The parameters are not independent of each other. For example, the peak to peak values of the current derivative strongly correlate to the peak to peak values of the high-passed current derivatives. This is caused by GHz ringing in the current. For other parameters the correlations and possible physical mechanism are shown in Table IV.

TABLE IV

Correlations between ESD parameters

Filtered parameter	Parameter that correlates with	Reason for correlation of parameters
$V_{Loop, LP, p\text{-}p}$	I_p	The discharge current induces a voltage in the semi-circular loop.
$(di/dt)_{LP, p\text{-}p}$	$I_{BP, p\text{-}p}$	A low-pass and a derivative applied to a signal act together as a band-pass
$(di/dt)_{HP, p\text{-}p}$	$(di/dt)_{p\text{-}p}$	Strong high frequency ringing dominates the peak to peak voltage
$V_{Loop, HP, p\text{-}p}$	$V_{Loop, p\text{-}p}$	
$E_{HP, p\text{-}p}$	$V_{Loop, p\text{-}p}$	The loop is not shielded. It detects the electric field strongly at high frequencies.
$E_{LP, p\text{-}p}$	$E_{p\text{-}p}$	Strong electrostatic field is captured by both parameters.

Consequently, the correlations between failure levels and the ‘filtered parameter’ are very similar to the correlations between failure levels and the corresponding ‘parameter that correlates with’.

Immunity problems often occur over very narrow frequency ranges. This is due to resonances that enhance the coupling between the field and the circuits. One might expect that the resonances will increase the sensitivity of the EUTs at specific frequencies. Such behavior is known from radiated immunity testing. Is it possible to see indication of the resonant behavior? At first glance this does not seem to be easy as pulse testing was performed. However, the following is possible: each generator has different frequency content and the ranking from strongest to weakest varies with frequency. If, at a selected frequency the ranking of generator spectral content matches the EUT failure level ranking, then this can be understood as an indication of frequency selective behavior. It is

even better if not only the non-quantified ranking matches, but the variation trends of parameters and the EUT failure levels correlate with each other.

To search for resonance enhanced correlation we created a set of parameters by band-pass filtering. Four sets of such parameters were created by sweeping the center frequency and recording the peak to peak values at each: $I_{BP(*), p\text{-}p}$, $(di/dt)_{BP(*), p\text{-}p}$, $V_{LOOP, BP(*), p\text{-}p}$, and $E_{BP(*), p\text{-}p}$, (see Table III). Fig. 9 illustrates the dramatic variations of $V_{LOOP, BP(*), p\text{-}p}$, while the center frequency of the band-pass filter is sweeping. At first glance it may look surprising because the values for most ESD generators are higher in the high frequency ranges (>1.5 GHz) than in the low frequency. Owing to the strong high frequency oscillations for the first few nanoseconds of discharging, the high frequency peak becomes significant after band-pass filtering.

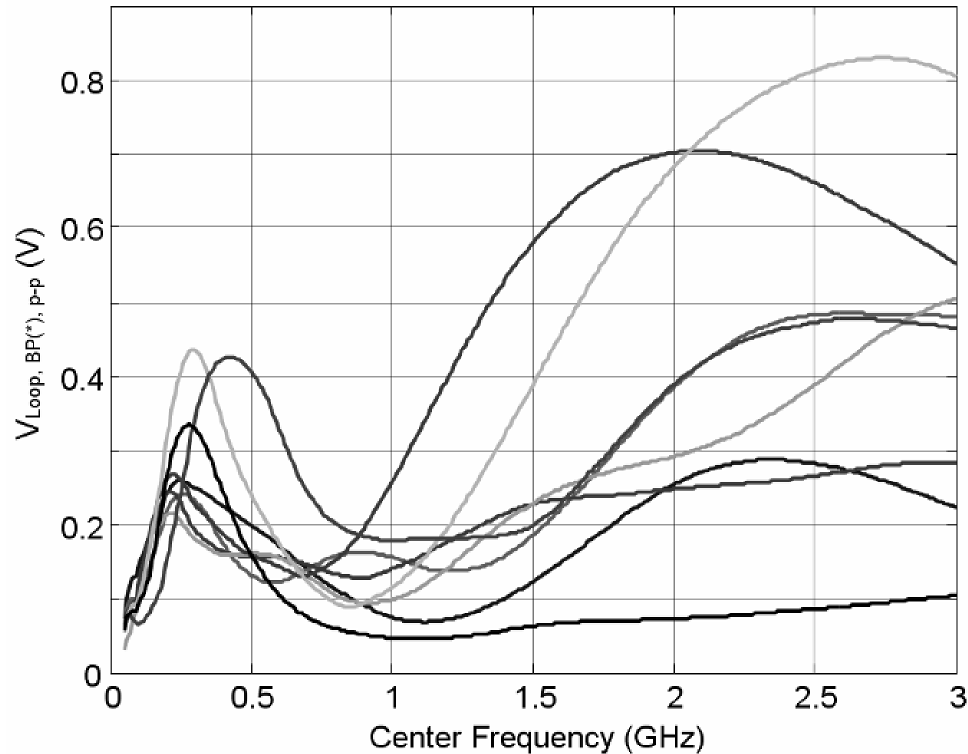


Fig. 9. Peak to peak values of band-pass filtered induced voltage in a semi-circular loop, $V_{Loop,\ BP(*),\ p\text{-}p}$, using eight different ESD generators. See Table III for ESD parameter symbols.

C. Frequency Selective Immunity of EUTs

The correlation between the reciprocal failure levels and the four sets of band-pass filtered parameters, $I_{BP(*),\ p\text{-}p}$, $(di/dt)_{BP(*),\ p\text{-}p}$, $V_{LOOP,\ BP(*),\ p\text{-}p}$, and $E_{BP(*),\ p\text{-}p}$ was investigated for each EUT. To illustrate the results the two data sets were compared and are shown in Fig. 10. The correlation between the failure levels and $V_{Loop,\ BP(630MHz)}$ is shown in Fig. 10 (a) while Fig. 10 (b) shows the non-correlation between the failure levels and $V_{Loop,\ BP(80MHz),\ p\text{-}p}$ for EUT2. The positive voltage discharges were performed for both cases. At 630 MHz a strong correlation is visible, while there is no correlation at 80 MHz between the failure level and the induced loop voltage. This indicates that a resonance within EUT2 strongly influences the robustness of the EUT.

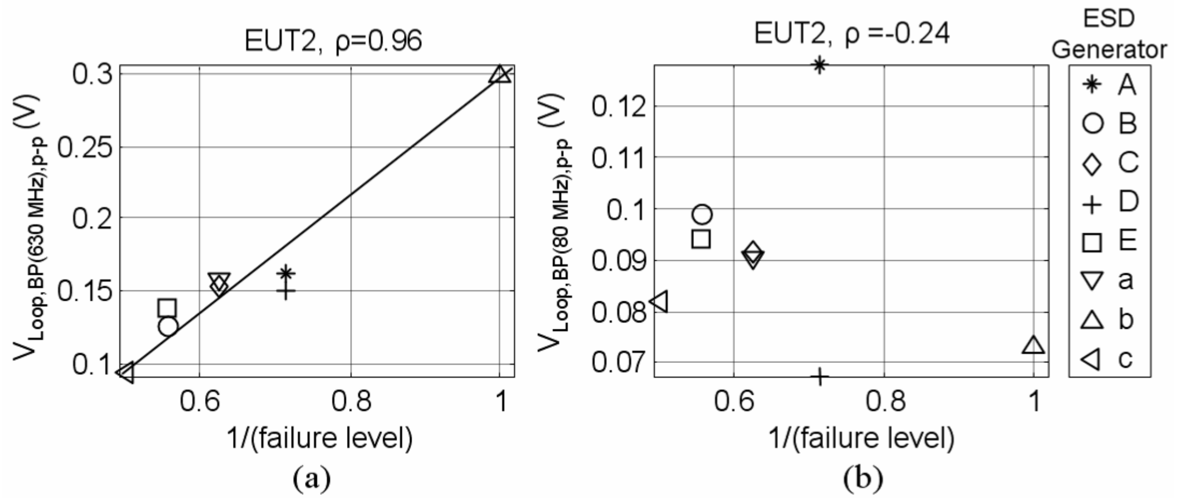


Fig. 10. An example of (a) correlation and (b) non-correlation between ESD parameter and failure level.

Most EUTs show the similar correlations at different frequencies. Cases of correlation (correlation coefficient > 0.7) are summarized in Table V where the center frequencies that had the largest correlation coefficient are shown. The example just discussed is shown in Fig. 10 (a) and is marked by an ‘*’ in the Table V.

TABLE V

EUTs whose failure levels show corrlations (Correlation coefficient > 0.7) to band-passed ESD parameters at specific center frequencies

EUT	$V_{LOOP, BP(*), p-p}$	$(di/dt)_{BP(*), p-p}$	$E_{BP(*), p-p}$
EUT12 (+)	70 MHz	X	X
EUT 14 (+)	90 MHz	120 MHz	X
EUT 16 (+)	170 MHz	170 MHz	180 MHz
EUT 16 (-)	170 MHz	170 MHz	180 MHz
EUT 15 (+)	210 MHz	200 MHz	230 MHz
EUT 9 (-)	380 MHz	360 MHz	X
EUT 9 (+)	480 MHz	420 MHz	X
EUT 2 (-)	510 MHz	470 MHz	X
EUT 2 (+)	630 MHz*	540 MHz	X
EUT 3 (+)	750 MHz	1.27 GHz	1.07 GHz
EUT 8 (-)	770 MHz	1.08 GHz	X
EUT 7 (-)	770 MHz	1.14 GHz	X
EUT 7 (+)	790 MHz	990 MHz	X
EUT 4 (-)	880 MHz	1.11 GHz	1.02 GHz
EUT 3 (-)	920 MHz	730 MHz	1.04 GHz
EUT 6 (-)	960 MHz	X	1.09 GHz
EUT 4 (+)	970 MHz	X	1.08 GHz
EUT 6 (+)	990 MHz	X	1.11 GHz
EUT 5 (+)	990 MHz	X	X
EUT 5 (-)	990 MHz	X	X
EUT 11 (-)	1.24 GHz	X	1.28 GHz
EUT 11 (+)	1.48 GHz	X	X
EUT 14 (-)	2.36 GHz	2.29 GHz	850 MHz
EUT 12 (-)	X	50 MHz	X
EUT 8 (+)	X	1.04 GHz	X
EUT 1 (+)	X	X	X
EUT 1 (-)	X	X	X
EUT 15 (-)	X	X	X
# of EUTs	23	17	11

* corresponds to Fig. 10 (a)

- X : No correlation stronger than correlation coefficient of 0.7

- (+): positive voltage discharge, (-): negative voltage discharge

The rows in the table are sorted such that the center frequencies for $V_{LOOP, BP(*), p\text{-}p}$ are in ascending order. In general, $V_{LOOP, BP(*), p\text{-}p}$ shows the correlations in a wide frequency range while either $(di/dt)_{BP(*), p\text{-}p}$ or $E_{BP(*), p\text{-}p}$ show correlations around the frequencies where $V_{LOOP, BP(*), p\text{-}p}$ correlates.

The data in TABLE V point at a frequency selective behavior of the EUT response. This is further supported by experiences in radiated immunity testing and by the plausible argument where resonances enhance the coupling between the field and the circuit. If we accept that resonances increase the variation of the sensitivity of the EUTs, then we can use this to explain one of the most surprising results of the Round Robin test: No ESD generator was the most severe on most of the EUTs, nor the least severe. This question is relevant for many reasons, not in the least that members of the standard committee often ask about the performance of commercial ESD generators. We had observed that the spectral density of e.g., the induced loop voltage varies strongly over frequency. A generator that is strong at some frequencies may show weak fields at other frequencies. The order of severity is a function of frequency and of the parameter observed. Thus, one EUT may be very sensitive to one generator, because the resonance and the range of strong fields match. However, it may not react strongly to another generator that has strong fields, but not in the range of the resonance.

Do we have proof? No, a test that uses pulses of ringing narrowband signals while observing the failure level as a function of frequency might provide proof. However, such an investigation was not part of the Round Robin test. For now we have to settle for the plausible explanation that it is strongly supported by data.

D. Which Parameter Predicts the Failure Level the Best for All EUTs?

For practical reasons and due to the problems of convincing a committee having diverse technical qualifications, it is unrealistic to require a large set of difficult to determine parameters to be included in a standard. Thus, we need to simplify by selecting the best parameter for reducing test result variations. Thus, we are looking for a correlation between all the EUT test results and the generator parameters. This requires a method of data aggregation for the EUT test results. We used an average. Please see Section V for details.

Any major deviation trend from mean failure level will be accumulated in this averaging process allowing testing for a general correlation over all the EUTs to a selected ESD parameter. Fig. 11 shows these general correlations. $V_{Loop,\ p\text{-}p}$ and $I_{BP,\ p\text{-}p}$ exhibit correlation to the failure level over all EUTs, while other parameters do not. Of course, at this point one might think that the peak current did not show a correlation, that it is not relevant, and that it could be removed from the standard. However, the variations of the peak current are small between all the ESD generators and many of the parameters are linearly dependent on the peak current in an ESD generator. Comparing the correlation coefficients, 'ρ', in Fig. 11 with the 'ρ' value in Fig. 10 (a) reveals that these overall correlations are not strong. Thus, $V_{Loop,\ p\text{-}p}$, and $I_{BP,\ p\text{-}p}$ can help to improve the ESD standard but will not solve the problem of reproducibility completely. Based on our test data, we believe that this is due to the resonant nature of the EUTs. Envelope specifications on the transient fields (e.g, expressed as the spectrum of V_{Loop}) and a limit on the frequency content of the discharge waveform could help to reduce the problem of test result reproducibility.

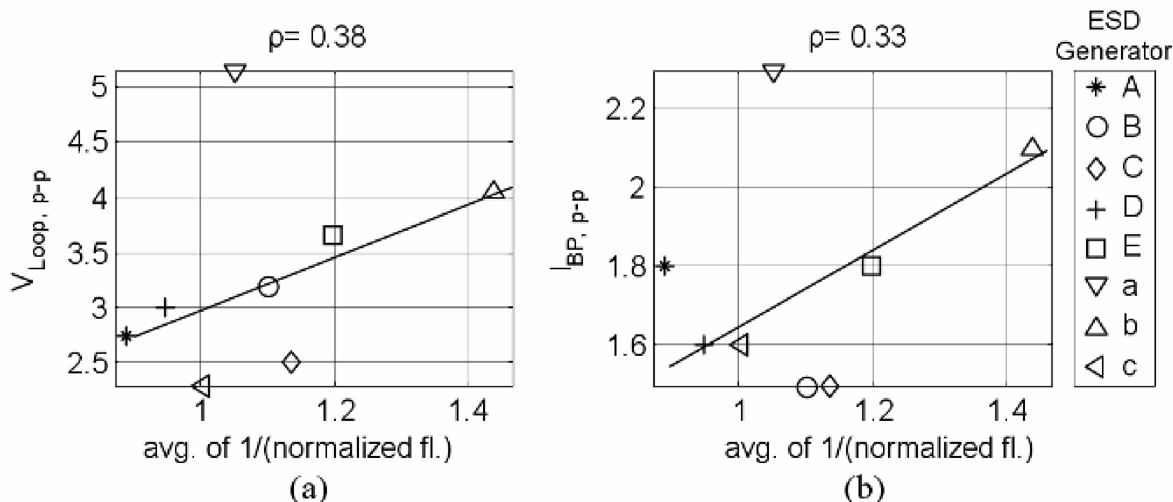


Fig. 11. The general correlation of (a) $V_{Loop,\ p\text{-}p}$ and (b) $I_{BP,\ p\text{-}p}$ to failure level over all the EUTs. Avg. of 1/(normalized fl.) represents the failure level variation trends that would cover all EUTs.

As can be see in Fig. 11 and Table II, 'Generator a' outlies from the main trends because of the high peak current beyond the standard or for unknown reasons. If it is excluded from the analysis, the correlation improves as shown in Fig. 12.

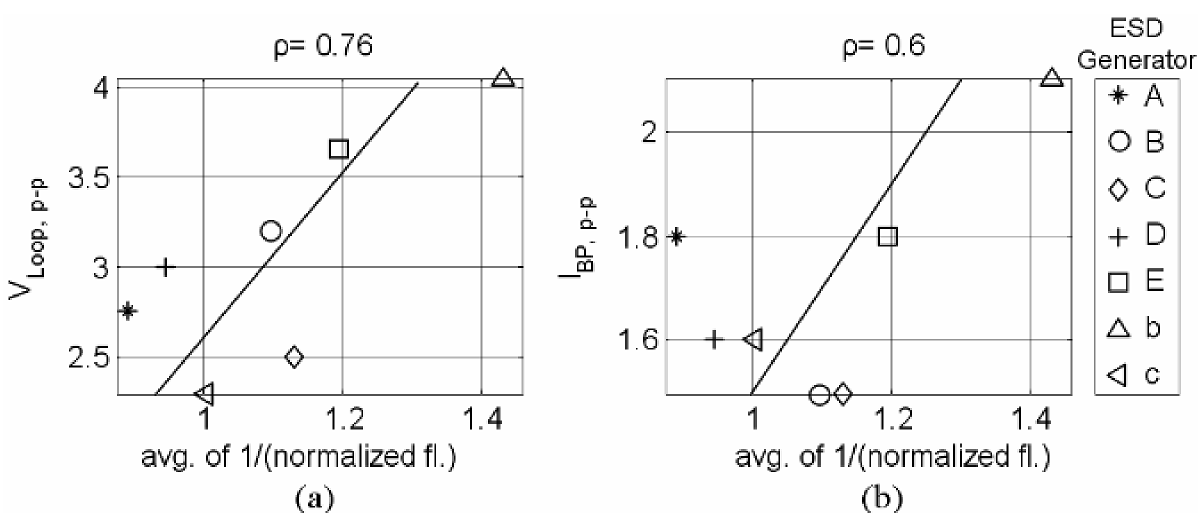


Fig. 12. General correlation of (a) $V_{Loop,\ p\text{-}p}$ and (b) $I_{BP,\ p\text{-}p}$ to failure level over all EUTs excluding 'Generator a'.

E. Limit of the Correlation Analysis

Correlation does not prove a cause-and-effect relationship. However, the correlations are supported by a plausible physical model (e.g., resonances) allowing for

cautious conclusions regarding the cause-and-effect relationships. Being able to perform experiments that monitor internal voltages and currents, and varying only one parameter may be able to prove the relationships.

V. Comparison between the Modified and the Unmodified ESD Generators

The Round Robin was initiated to test if a specification on the width of the initial pulse would improve test result repeatability. TABLE VI summarizes the modifications from the perspective of the parameters defined in the test standard. For the generators that came in pairs of a modified and an unmodified model, the width of the first pulse changed by a factor of 2.2 ~ 2.5. Other parameters specified in the standard changed by a factor of 0.8 ~ 1.3. Also all the other parameters given in TABLE II also have been changed. For example $V_{Loop,\ p\text{-}p}$, was changed by 2.8 ('Generator A') to 5.2 ('Generator a').

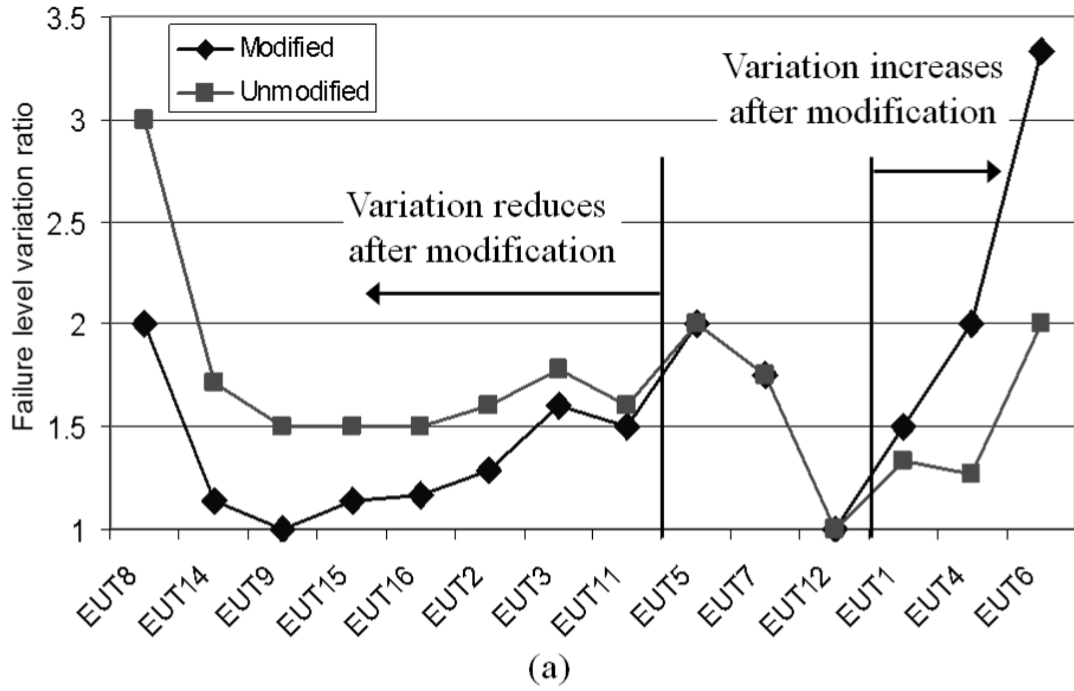
The previous section had shown that the field parameters correlate to failure levels. Increasing the width of the first pulse will also reduce ringing, thus reduce $I_{BP,\ p\text{-}p}$ which is another parameter which correlates to the failure levels. Due to the complexity of the situation, we analyzed for how many EUTs the failure level variation increased by using a modified generator and for how many it was reduced.

TABLE VI

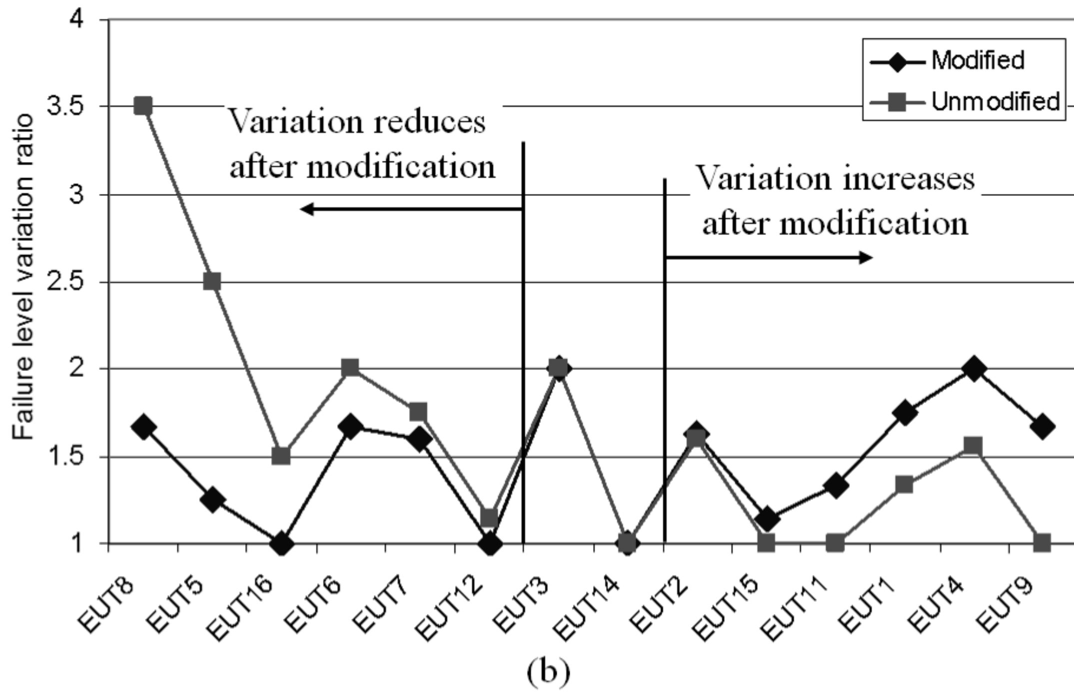
Discharge current parameters change before and after modification

ESD generator	Discharge current peak	Rise time	Current at 30 ns	Current at 60 ns	**Width of first pulse**
A (modified)	4	0.7	1.6	1.2	**2.8**
a (unmodified)	4.9	0.9	1.7	1.1	**1.1**
Change ratio (A/a)	0.8	0.8	0.9	1.1	**2.5**
B (modified)	3.6	1	2.4	0.8	**2**
b (unmodified)	3.7	0.8	2	1	**0.9**
Change ratio (B/b)	1	1.3	1.2	0.8	**2.2**

The changes in the failure level variation ratio (see TABLE II for definition) after the modifications are illustrated in Fig. 13. For the EUTs on the left side of the plot, the failure level variations reduce after modification, while they increase on the right side. Overall, the data indicates that slightly more EUTs showed improved reproducibility than worsened reproducibility. The IEC 77b MT12 ESD standard setting working group did not see this as sufficient evidence to include this specification into the standard IEC 61000-4-2.



(a)



(b)

Fig. 13. The changes in the failure level variation ratio before and after modifying the ESD generators for the (a) positive and (b) negative voltage discharges. The left side of the plot shows the reduction of the variation ratio after the modifications while right side shows the increase.

VI. Conclusion

The system level ESD Round Robin test, conducted at three laboratories, comparing eight generators, showed test result variations of up to 1:3 with 1:2 being common. No ESD generator was the most severe over all of the EUTs and no one generator was the least severe.

ESD generator parameters have been correlated to upset levels. Out of the many parameters tested, two correlated: The voltage induced in a small loop and the spectral content of the discharge generator between 200 and 800 MHz, a range that is often influenced by the falling part of the initial peak. A set of generators that had a slower falling edge and less ringing in the falling part of the waveform showed slightly reduced test result variations. Correlation between the spectral content of the ESD generator parameters and upset levels indicated resonant behavior: The narrowband spectral content correlated well with upset levels at selected frequencies for many EUTs.

The data indicate that the transient fields of ESD generators strongly contribute to the repeatability problem of system level ESD testing. Better test repeatability will only be achieved by properly controlling the transient field during discharge.

APPENDIX

SIMPLE ESD TESTING MODEL AND MATHEMATICAL MANIPULATION FOR CORRELATION ANALYSIS

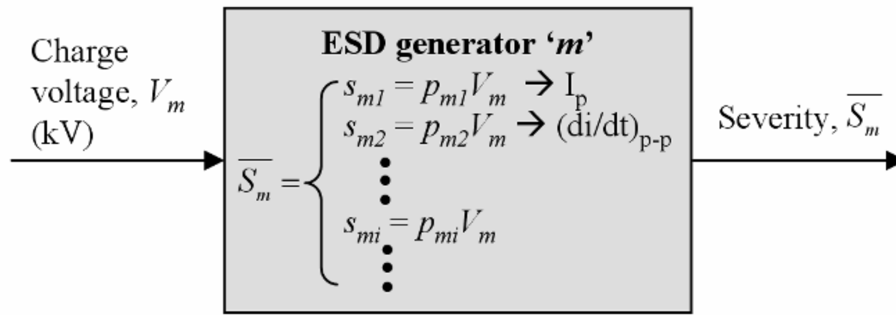
Table A-I summarizes the symbols and subscripts used in the chapter.

TABLE A- I

Glossary for symbols and subscripts used in the chapter

Symbols for vectors and matrix elements	
V	Charge voltage; ESD generator dependent
p	ESD parameter measured at 1 kV; ESD generator dependent
s	ESD parameter measured at V kV; ESD generator dependent
k	Sensitivity coefficient to an ESD parameter; EUT and ESD parameter dependent
fl	Failure level; ESD generator and EUT dependent
r	Reciprocal failure level (1/fl); ESD generator and EUT dependent
Subscripts	
i	Stands for designating a ESD parameter, i=1, 2, …
m	Stands for designating a ESD generator, m=A, B, …
j	Stands for designating a EUT, j=1, 2, …
Matrix and Vector notations	
$\overline{\overline{A}}$	Matrix A
$\overline{A}$	Row vector A or Column vector A

An ESD generator is a linear device in contact mode. Its severity can be modeled as shown in Fig. A- 1. An ESD generator receives a charge voltage set by a user as an input and it outputs various ESD parameters, such as the discharge currents and the transient fields.



where

V_m: Charge voltage set on the ESD generator '*m*' by user

p_{mi}: i^{th} ESD parameter of the ESD generator '*m*' measured at 1 kV

s_{mi}: i^{th} ESD parameter of the ESD generator '*m*' at V_m kV

Fig. A- 1. Simple model for ESD generator '*m*'.

As we assume the contact mode, the peak to peak values of the ESD parameters will be proportional to the charge voltage. This linear behavior allows for the definition of a severity vector for an ESD generator '*m*', $\overline{S_m}$, as given in (1). Here we use kV as the unit of the charge voltage.

$$\overline{S_m} = \overline{P_m} V_m \tag{1}$$

where $\overline{P_m} = \begin{bmatrix} p_{m1} & p_{m2} & \cdots & p_{mi} & \cdots \end{bmatrix}$, ESD parameter vector for generator '*m*'

Other parameters that are not proportional to the charge voltage, e.g., energy stored in the discharge capacitor or the power density of the transient field etc., are not considered in this analysis.

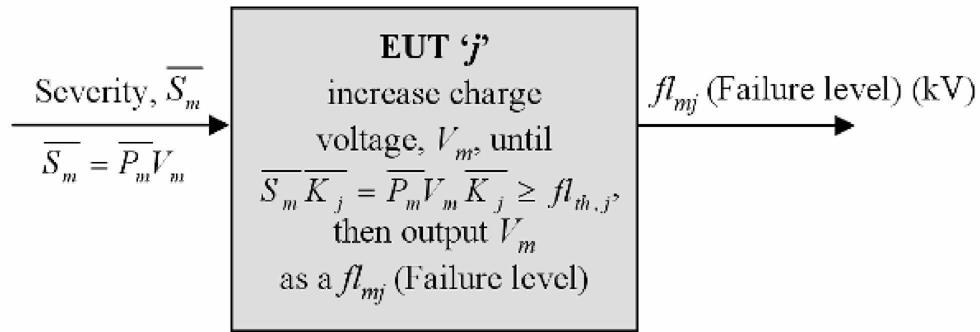
Expanding the row vector, $\overline{P_m}$, for the case of multiple ESD generators yields (2).

$$\overline{\overline{P}} = \begin{bmatrix} \overline{p_A} \\ \overline{p_B} \\ \vdots \\ \overline{p_m} \\ \vdots \end{bmatrix} = \begin{bmatrix} p_{A1} & p_{A2} & \cdots & p_{Ai} & \cdots \\ p_{B1} & p_{B2} & & \vdots & \\ \vdots & & \ddots & \vdots & \\ p_{m1} & \cdots & \cdots & p_{mi} & \cdots \\ \vdots & & & \vdots & \ddots \end{bmatrix} = \begin{bmatrix} \overline{P_1} & \overline{P_2} & \cdots & \overline{P_i} & \cdots \end{bmatrix} \quad (2)$$

where $\overline{P_i} = \begin{bmatrix} p_{Ai} & p_{Bi} & \cdots & p_{mi} & \cdots \end{bmatrix}^T$

The column vector, $\overline{P_i}$, indicates different values of a parameter among many ESD generators. The row vector, $\overline{P_m}$, indicates the different parameters for an ESD generators.

ESD testing is modeled as a threshold detection process. The charge voltage is increased during a test until a failure occurs. Once the severity inputted into the EUT exceeds a certain value, the EUT fails. The charge voltage is recorded. The ESD testing for an EUT '*j*' using ESD generator '*m*' can be modeled as shown in Fig. A- 2.



where

$\overline{K_j} = \begin{bmatrix} k_{1j} & k_{2j} & \cdots & k_{ij} & \cdots \end{bmatrix}^T$: Sensitivity vector for EUT '*j*'

k_{ij}: sensitivity coefficient of EUT '*j*' for i^{th} ESD parameter

$fl_{th,j}$: fixed threshold failure level for EUT '*j*' (kV)

Fig. A- 2. Simple ESD testing model used in the correlation analysis

When a failure occurs, the term, $\overline{S_m}\,\overline{K_j}$ in Fig. A- 2 is equal to the fixed threshold failure level for EUT '*j*', $fl_{th,j}$, as expressed by (3).

$$\overline{S_m}\,\overline{K_j} = \overline{P_m} V_m \overline{K_j} = \left(p_{m1}k_{1j} + p_{m2}k_{2j} + \cdots + p_{mi}k_{ij} + \cdots\right)V_m = fl_{th,j} \tag{3}$$

Solving (3) with respect to V_m gives the expression for a measurable failure level of EUT '*j*' using ESD generator '*m*', fl_{mj}, as in (4).

$$fl_{mj} = V_m\big|_{at\ which\ EUT\ 'j'\ fails} = fl_{th,j}\frac{1}{\overline{P_m}\,\overline{K_j}} = \frac{fl_{th,j}}{p_{m1}k_{1j} + p_{m2}k_{2j} + \cdots + p_{mi}k_{ij} + \cdots} \tag{4}$$

Now the reciprocal failure level of EUT '*j*' using generator '*m*', 'r_{mj}', is expressed as in (5).

$$r_{mj} = \frac{1}{fl_{mj}} \tag{5}$$

Expanding (5) by considering multiple ESD generators, the reciprocal failure level vector for EUT '*j*', $\overline{R_j}$, can be expressed as in (6).

$$\overline{R_j} = \begin{bmatrix} \frac{1}{fl_{Aj}} \\ \frac{1}{fl_{Bj}} \\ \vdots \\ \frac{1}{fl_{mj}} \\ \vdots \end{bmatrix} = \frac{1}{fl_{th,j}} \overline{\overline{P}}\,\overline{K_j} = \frac{1}{fl_{th,j}} \left(\overline{P_1} k_{1j} + \overline{P_2} k_{2j} + \cdots + \overline{P_i} k_{ij} + \cdots \right) \tag{6}$$

In (6), an element in the right term, $\overline{P_i} k_{ij}$, is the sensitivity of EUT '*j*' to the ith ESD parameter multiplied by the strength of this parameter. As p_{mi}, a element of $\overline{P_i}$, changes its value from generator to generator, $\overline{P_i} k_{ij}$ expresses one contribution to the failure level variation of the test results observed if different ESD generators are used. This contribution can be quantified by the correlation coefficient shown in (7).

$$\rho_{R_j P_i} = \frac{\mathrm{cov}(R_j, P_i)}{\sigma_{R_j} \sigma_{P_i}}, \quad \text{while '}m\text{' changes, } m = A, B, \ldots \tag{7}$$

where

$R_j = 1/fl_{Aj}\,,\ 1/fl_{Bj}\,,\ \cdots\,,\ 1/fl_{mj}\,,\ \cdots$

$P_i = p_{Ai},\ p_{Bi},\ \cdots\,,\ p_{mi},\ \cdots$

cov(X,Y) is the covariance of X and Y, σ_X is the standard deviation of X.

In the correlation analysis for EUT '*j*', numerous correlation coefficients, $\rho_{R_j P_i}$, were investigated changing P_i (i = 1, 2, …) while the reciprocal failure levels, R_j, was kept the same. If $\rho_{R_j P_i}$ is close to 1, the data points in 1/(failure level)-vs.-parameter are close to the straight line, as can be seen in Fig. 10 (a). Let us say the ith ESD parameter

correlates to the failure levels. This can be expressed as in (8) and the elements of $\overline{\varepsilon_j}$ should be small numbers.

$$\overline{R_j} = \begin{bmatrix} \frac{1}{fl_{Aj}} \\ \frac{1}{fl_{Bj}} \\ \vdots \\ \frac{1}{fl_{mj}} \\ \vdots \end{bmatrix} = \frac{1}{fl_{th,j}} \left(\overline{P_i} k_{ij} + C_j + \overline{\varepsilon_j} \right) \tag{8}$$

where

$$C_j + \overline{\varepsilon_j} = \overline{P_1} k_{1j} + \ \cdots \ + \overline{P_{i-1}} k_{i-1j} + \overline{P_{i+1}} k_{i+1j} + \cdots$$

C_j is a constant, $\overline{\varepsilon_j}$ indicates imperfection of the correlation.

$$\overline{\varepsilon_j} = \begin{bmatrix} \varepsilon_{Aj} \\ \varepsilon_{Bj} \\ \vdots \\ \varepsilon_{mj} \end{bmatrix}, \text{ small numbers.}$$

Eq.(8) can be read as such: In order for the ith ESD parameter to dominate the failure level variation for EUT 'j', both of the following conditions need to be satisfied.

- $k_{ij} >> k_{1j}, k_{2j}, \cdots$: EUT '$j$' has a higher sensitivity to the ith ESD parameter than to other parameters.
- $\varepsilon_{mj} << p_{mi} k_{ij} + C_j \ \ for\, all\, m = A, B, \cdots$: The accumulated effects of parameters except the ith parameter among the ESD generators on the failure level are seen as a small number, because their corresponding sensitivities are not significant.

Fig. 10 (a) is revisited as in Fig. A- 3 for the visualizations of (9).

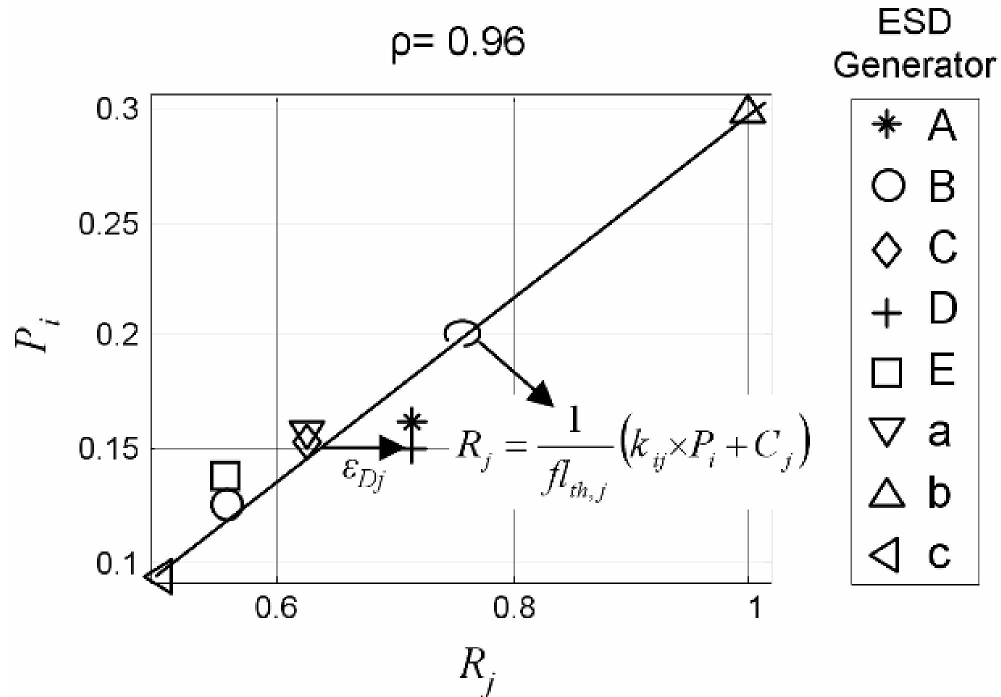


Fig. A- 3. Interpretations of the correlation plot in terms of (8).

Finding the most suitable parameter for predicting the failure level over all EUTs needs a data processing that aggregates all individual failure levels for each EUT into an overall failure level vector. This vector represents the aggregated sensitivity of all EUTs and can be correlated to parameters.

A two step process is used. In the first step we remove the difference caused in failure levels by some EUT being very robust and others being quite sensitive. This is similar to the data shown in Fig. 2. Normalized failure levels for fourteen EUTs while (a) positive voltage discharges and (b) negative voltage discharges were performed using eight ESD generators. The lowest failure level for each EUT was used for normalization. EUT 10 (rarely failed up to 10kV) and EUT 13 (indirect discharge) were excluded.

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generators. The lowest failure level for each EUT was used for normalization. EUT 10 (rarely failed up to 10kV) and EUT 13 (indirect discharge) were excluded.

, the normalization has been done to the minimal value to show the failure level variations. For the correlation analysis, a mean failure level was used for normalization. A normalized failure level, fl_{mj}^{N}, and a normalized reciprocal failure level, r_{mj}^{N}, are defined as in (9).

$$r_{mj}^{N} = \frac{1}{fl_{mj}^{N}} = \frac{fl_{th,j}}{fl_{mj}} \tag{9}$$

where

$$fl_{th,j} = \frac{1}{\#of\ generators} \sum_{m=A,B,\cdots}^{for\ all\ generators} fl_{mj}$$, a mean failure level

Then a normalized reciprocal failure level vector of an EUT, $\overline{R_j^N}$, for multiple ESD generators is defined as in (10)

$$\overline{R_j^N} = \begin{bmatrix} r_{Aj}^N \\ r_{Bj}^N \\ \vdots \\ r_{mj}^N \\ \vdots \end{bmatrix} = fl_{th,j} \begin{bmatrix} \frac{1}{fl_{Aj}} \\ \frac{1}{fl_{Bj}} \\ \vdots \\ \frac{1}{fl_{mj}} \\ \vdots \end{bmatrix} = \overline{\overline{P}}\,\overline{K_j} = \overline{P_1}k_{1j} + \overline{P_2}k_{2j} + \cdots + \overline{P_i}k_{ij} + \cdots \tag{10}$$

In the second, step we average over all EUTs to obtain a vector that represents the average sensitivity of all EUTs to each generators used. The averaged reciprocal failure level, $\overline{R^{N}{}_{avg.}}$ is shown as in (11).

$$\overline{R^{N}_{avg.}} = \begin{bmatrix} r^{N}_{A\,avg.} \\ r^{N}_{B\,avg.} \\ \vdots \\ r^{N}_{m\,avg.} \\ \vdots \end{bmatrix} = \frac{fl_{th,j}}{\#of\ EUTs} \sum_{j=1}^{all\ EUTs} \begin{bmatrix} \frac{1}{fl_{Aj}} \\ \frac{1}{fl_{Bj}} \\ \vdots \\ \frac{1}{fl_{mj}} \\ \vdots \end{bmatrix} = \overline{\overline{P}} \frac{\sum_{j=1}^{all\ EUTs} \overline{K_j}}{\#of\ EUTs} = \overline{P_1} k_{1\,avg.} + \overline{P_2} k_{2\,avg.} + \cdots + \overline{P_i} k_{i\,avg.} + \cdots \tag{11}$$

where

$$k_{i\,avg.} = \frac{\sum_{j=1}^{all\ EUTs} k_{ij}}{\#of\ EUT},$$

If the ith ESD parameter correlates to the failure levels over most of the EUTs, the corresponding $k_{i\,avg.}$ terms, an element in the right term in (11), are added up and survive in the averaging process while the rest of them are averaged out. Then $\overline{R^{N}_{avg.}}$ becomes (12).

$$\overline{R^{N}_{avg.}} = \begin{bmatrix} r^{N}_{A\,avg.} \\ r^{N}_{B\,avg.} \\ \vdots \\ r^{N}_{m\,avg.} \\ \vdots \end{bmatrix} = k_{i\,avg.}\overline{p_i} + C_{avg.} + \overline{\varepsilon_{avg.}} \qquad (12)$$

where

$$C_{avg.} + \overline{\varepsilon_{avg.}} = \overline{P_1}k_{1avg.} + \cdots + \overline{P_{i-1}}k_{i-1avg.} + \overline{P_{i+1}}k_{i+1avg.} + \cdots$$

Thus, (12) is an analogy to (8) for the correlation over all the EUTs and can be analyzed in the same way using the correlation coefficient and $\overline{R^{N}_{avg.}}$ -vs.-P_i plot as can be seen in Fig. 11 and Fig. 12.

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Paper 2

FREQUENCY DOMAIN MEASUREMENT METHOD FOR THE ANALYSIS OF ESD GENERATORS AND COUPLING

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ABSTRACT

A method for analyzing electrostatic discharge (ESD) generators and coupling to equipment under test in the frequency domain is proposed. In ESD generators the pulses are excited by the voltage collapse across relay contacts. The voltage collapse is replaced by one port of a vector network analyzer. All the discrete and structural elements that form the ESD current pulse and the transient fields are excited by the vector network analyzer as if they were excited by the voltage collapse. In such a way the method allows analyzing current and field driven linear coupling without having to discharge an ESD generator, eliminating the risk to the circuit and allowing the use of the wider dynamic range of a network analyzer relative to a real-time oscilloscope. The method is applicable to other voltage collapse driven tests, such as Electrical Fast Transient (EFT), Ultra wideband (UWB) susceptibility testing but requires a linear coupling path.

Keywords: Electrostatic Discharge; ESD, simulation, network analyzer

I. INTRODUCTION

Electrostatic discharge (ESD) is reproduced by an ESD generator to test the robustness of various electronics devices toward ESD. Most ESD generators are built in accordance to the specifications given in IEC 6100-4-2 [1]. The discharges are initiated by high voltage relays. While the mechanical movement is slow the electrical breakdown leads to sub-nanosecond voltage changes. Before the contacts touch, a surface driven or gas discharge driven (depending on the voltage) breakdown will lead to a rapid voltage collapse. These fall times have been estimated to be less than 100 ps [2]. However, the discharge current specifications call for 700-1000 ps rise time. This is achieved by pulse forming elements placed around the relay and between the relay and the tip of the ESD generator. Not only the injected ESD current, but also the rapidly changing currents within the relay and in the pulse forming elements cause transient fields. As shown in [2] and [3] this may lead to excessive > 1 GHz transient fields of ESD generators compared to human-metal ESD of equivalent current rise time.

Compliance of electronic equipment is determined by the reaction against disturbance as indicated in the regulation [1].

However, such tests reveal little information on the underlying reason for a disturbance, such as the coupling paths. Knowing the coupling paths can not only help resolve ESD issues, but can also be used to estimate system performance beforehand.

Several numerical and circuit models of ESD generators have been published and verified by measurement [4]-[6]. For analyzing > 1 GHz frequency components it is not sufficient to take a discharge current of 0.7-1 ns rise time as the excitation source. The details of the pulse forming network also need to be modeled to correctly reproduce the >

1 GHz field components. Thus, not only a detailed model of the electronic system the discharge will be applied to is needed, but it must be combined with a rather elaborate ESD generator model.

Numerous authors have applied numerical methods for calculating coupling of transient fields from ESD [7-11]. However, compared to practical systems the authors used relatively simple structures as most real systems are too complex to be modeled by numerical means.

This drawback can be avoided by experimental methods [10] - [12]. The methods have in common that ESD generators are discharged while induced voltages or currents are measured. However, in a set of difficulties arise:

- The strong common-mode coupling to the probing system may override the intended signal,
- Dynamic ranges of fast time-domain oscilloscopes are limited by 8 bit A/D converters,
- The high voltages endanger the device under test, the active test probes and possibly the oscilloscope.

In most cases the dominated coupling path involves metal shielding and coupling to wires and traces. If we limit our analysis to such linear coupling paths, then frequency domain methods can be used.

Using the frequency domain for such coupling analysis offers several significant advantages. The wider dynamic range and high accuracy of the vector network analyzer can be utilized together with the, usually built-in, time-domain transformation functions. Further, it avoids endangering the device under test or the test equipment.

This paper describes a frequency domain method for conducting coupling studies associated with ESD generator or other voltage collapse driven susceptibility problems. The novelty lies in correctly representing the currents and transient fields of all structural and discrete elements of the pulse forming circuit within the ESD generator.

Section II introduces the methodology, Section III presents currents and field measurement results in comparison to non-modified ESD generators, and Section IV discusses applications and limits of the method.

II. Methodology

A. Basic concept

The method is based on the similarity of the time and the frequency domains for linear systems. To illustrate the principle, let us start by using three circuits that represent a highly simplified ESD generator discharging into a load.

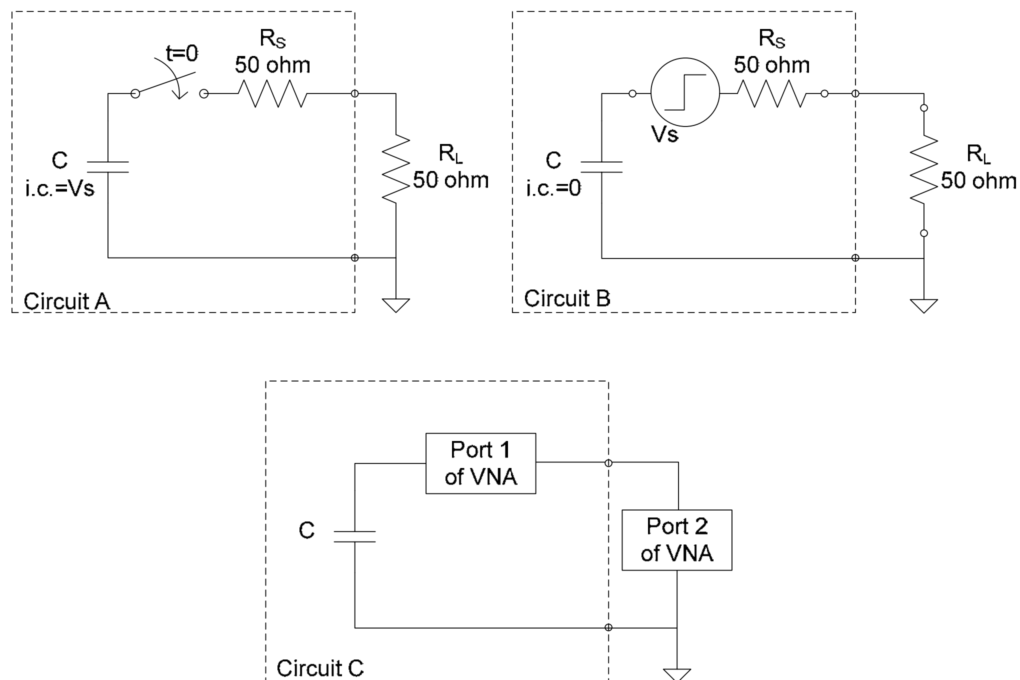

Fig. 1. Three different circuits that express the simple capacitor discharge current flowing through the resistor RL.

In Fig. 1, circuit A, a capacitor C, having an initial voltage Vs is discharged by an ideal relay at t=0. Current flows through R_S and R_L. Our interest is the voltage across R_L. The circuit elements C, Rs and the switch act as a highly simplified ESD generator and the resistor R_L as the EUT.

Analyzing the voltage and currents at the terminals connecting to R_L for t>0, there is no difference between a capacitor having an initial voltage Vs in series with a switch (Circuit A) relative to a capacitor without initial voltage in series with a step function voltage source (Circuit B).

In practice one could substitute the relay by the step function port of a Time Domain Transmission (TDT) instrument and measure the voltage across R_L (the coupled voltage) at the oscilloscope port. However, the dynamic range of TDT instruments is much less than the dynamic range of network analyzers and TDT sampling heads can easily be damaged by accidental ESD. Consequently, we substitute a network analyzer for the TDT instrument. The principle implementation is shown in Fig. 1, circuit C.

Port 1 is connected in place of the relay, while port 2 measures the voltage across the 50Ω resistor. The internal time domain transformation of the network analyzer is used to obtain time domain results. The dynamic range of a NWA is typically better than 100dB compared to 50-60 dB for a TDT measurement and about 40 dB for a real time oscilloscope measurement if no averaging or other signal enhancing techniques are applied.

B. Implementation

The main building blocks of an ESD generator are a high voltage source, a relay, a pulse forming network, a discharge resistor (R_d), an energy storage capacitor (C_s), a

ground strap and the body of ESD generator(see Fig. 2). The high voltage source charges up C_s, while the relay is open. The moment the gap between the relay blades is small enough a breakdown will cause the capacitor to discharge.

As the excitation of this circuit occurs at the relay blade contact, port 1 of the network analyzer needs to be connected at the blades as shown in Fig. 3. Obviously, the high voltage source needs to be turned off, if not removed. The network analyzer excites the ESD generator circuit by its internal source.

The voltage V in Fig. 2, collapses very rapidly [5]. It approximates a step response excitation to the ESD generator. Using the chirp-Z inverse Fourier Transform and windowing function built in the vector network analyzer, this step response can be readily displayed based on the S21 data.

The equation (1) is the expression for the discrete Fourier transform (DFT).

$$X_k = X(z_k) = \sum_{n=0}^{N-1} x_n z_k^{-n}, \quad k = 0,1,\cdots,N-1. \tag{1}$$

where $z_k = \exp(j2\pi k / N)$.

If we have z_k in the following form, it is called the chip-Z transformation (CZT).

$$z_k = AW^{-k}, \quad k = 0,1,\cdots,M-1. \tag{2}$$

Where, M is an arbitrary integer and both A and W are arbitrary complex numbers of the form $A = A_0 e^{j2\pi\theta_0}$ and $W = W_0 e^{j2\pi\phi_0}$.

The case $A = 1$, $M = N$, and $W = \exp(-j2\pi / N)$ corresponds to the DFT.

The chirp-Z transformation is one of the computational algorithms of sampled z-transform, which is more general and flexible than the FFT in their applications [16].

Windowing is needed because the band limiting response of a frequency domain measurement causes ringing in the time domain response. Windowing improves the dynamic range of the time domain results by filtering the frequency domain data prior to converting it to the time domain, at the expense of the fine frequency resolution of the transformed data [17]-[18].

Port 2 of the vector network analyzer can be connected to various types of transducers, e.g., the output of an ESD current target to capture the ESD discharge waveform, the output of a current clamp to measure currents induced in wires internal to an electronic system, to field sensors or to traces on a printed circuit board.

Such results are presented in Section III.

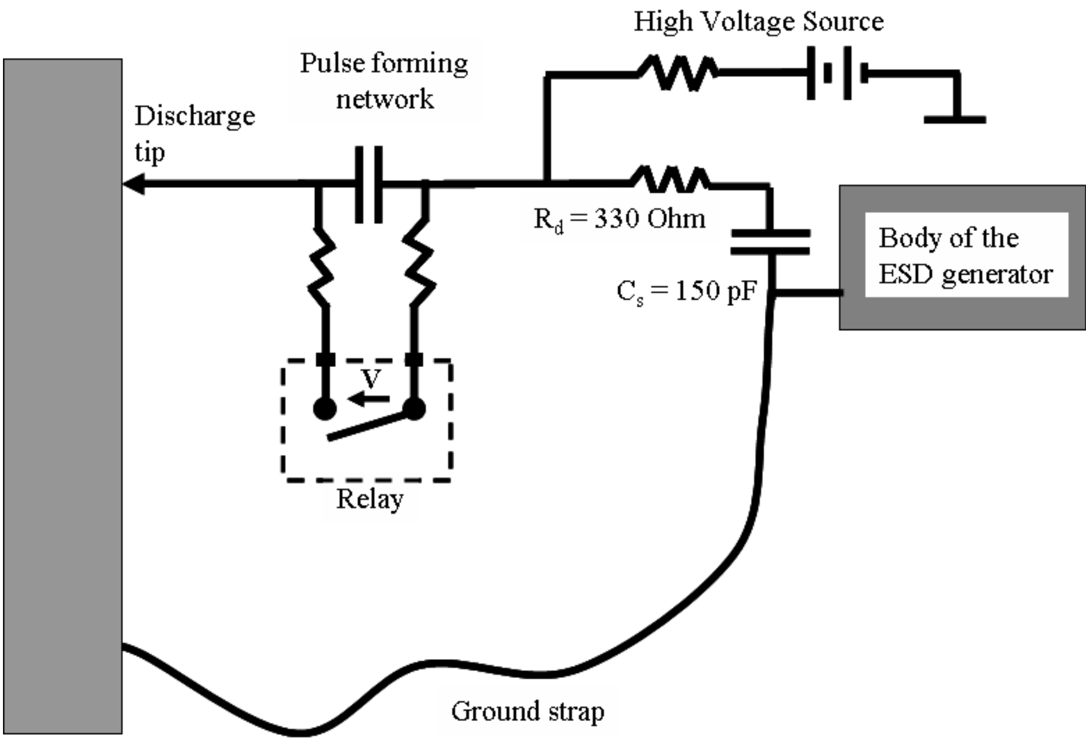

Fig. 2. Simple equivalent circuit of an ESD generator. The high voltage source charges up the energy storage capacitor (C_s). the capacitor starts to discharge the moment the relay is closed.

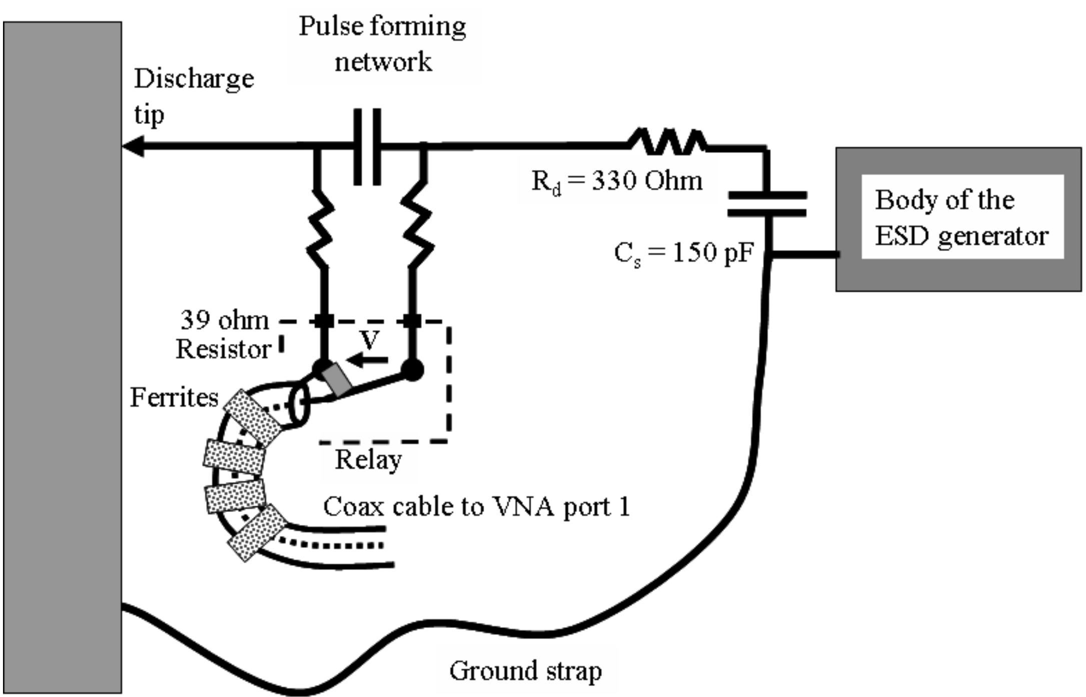

Fig. 3. Simple equivalent circuit of a modified ESD generator. In order to emulate the time domain behavior of the circuit, the voltage collapse is substituted by the vector network analyzer port 1 to allow direct contact to the relay blades. The relay enclosure was opened.

The underlying methodology, as outlined above is quite simple. However, to achieve good results a careful implementation is needed. Three points need special attention.

- Port 1 of the vector network analyzer needs to be connected exactly across the relay blades at the point of contact. Any deviation from this will change the RF behavior because the point of excitation would be moved away from its correct location. The ceramic enclosure of the relay was opened to allow direct contact to the relay blades by a thin coax cable (see Fig. 4).
- The source impedance should match the impedance created by the spark within the relay of the ESD generator circuit. The impedance across the contacts evolves through three phases. At first it is an open circuit ($t<0$), next the relay is best described by a time varying resistance ($t=0$ to about 100 ps), then the relay is best described by a series voltage source of 25-40V. Replacing the relay with a 50Ω VNA port leads to additional losses and damping of ringing by the pulse forming circuit (see discussion section). A 39Ω SMD resistor was soldered parallel to the relay contacts to reduce the source impedance. This resister is shown in Fig. 4.
- The attached cable needs to be electromagnetically invisible, i.e., no common-mode current is allowed to be flowing on it. A combination of low frequency and high frequency (brand name “Gigabuster”) material has been used to reducing common mode currents. The exact arrangement is the result of experimental optimization.

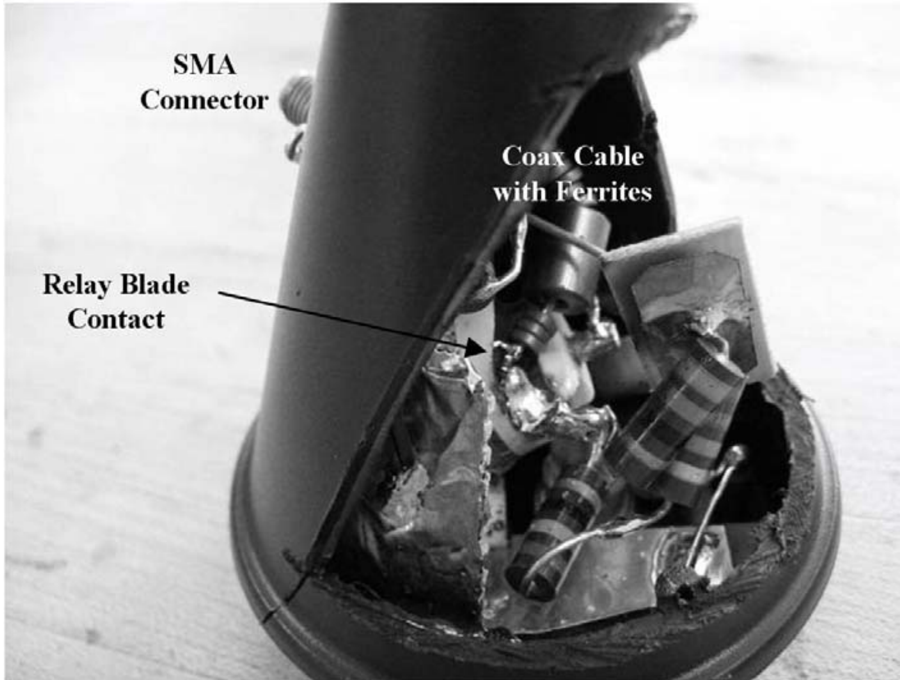

Fig. 4. Modified ESD generator module. The relay was opened and the coax cable was soldered to the relay blade contacts. The SMA connector connects to the network analyzer.

C. Verification of the methodology by SPICE simulation

A SPICE simulation was used to verify the proposed method. Based on the equivalent circuit of an ESD generator given in [5] the modifications needed for the frequency domain method have been implemented.

Several types of the equivalent circuits for ESD generators have been proposed [4-6]. For the circuit shown in fig. 5 the resistors Rt and Ri represent the current target resistance and input resistance of the oscilloscope respectively. The function of each component is explained in table 1 of [5]. The capacitor C1 is charged to an initial value. This represents the charging by the high voltage source of an actual ESD generator. After closing the relay the discharge current flowing through Rt is probed.

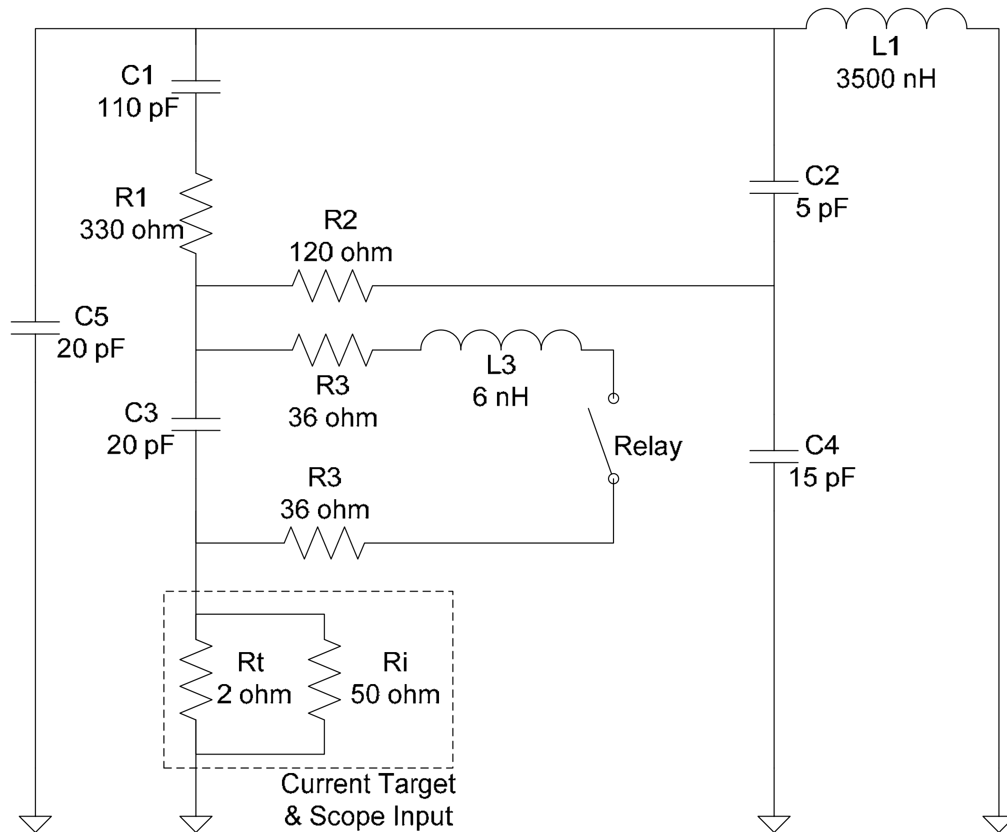

Fig. 5. Equivalent circuit of a ESD generator. Rt and Ri represent the current target resistance and input impedance of the oscilloscope.

The modified generator is shown in Fig. 6.

- The step voltage source, Vs, represents the swept frequency source of the network analyzer
- The inductance of the ground strap is represented by L1. Electric near field coupling within the ESD generator is modeled as capacitors. No radiation effects are taken into account.
- Ferrites are modeled as a pure common-mode inductor. Port 2 of the vector network analyzer is connected across the current target resistor Rt. Port 1 is connected to the relay contacts. The ferrites are modeled as a transformer which

has two perfectly coupled inductors whose values are 100 uH each. Ra is to reduce the source impedance of port 1.

- The circuit shown in Fig. 6 allows two paths to ground: One via the ground strap and one via the network analyzer. This may change the late time part of the current waveform. To avoid this effect low frequency, high permeability ferrites (in conjunction with high frequency ferrites) were place around the coax cables. The combined effect is modeled by the two perfectly coupled inductors.

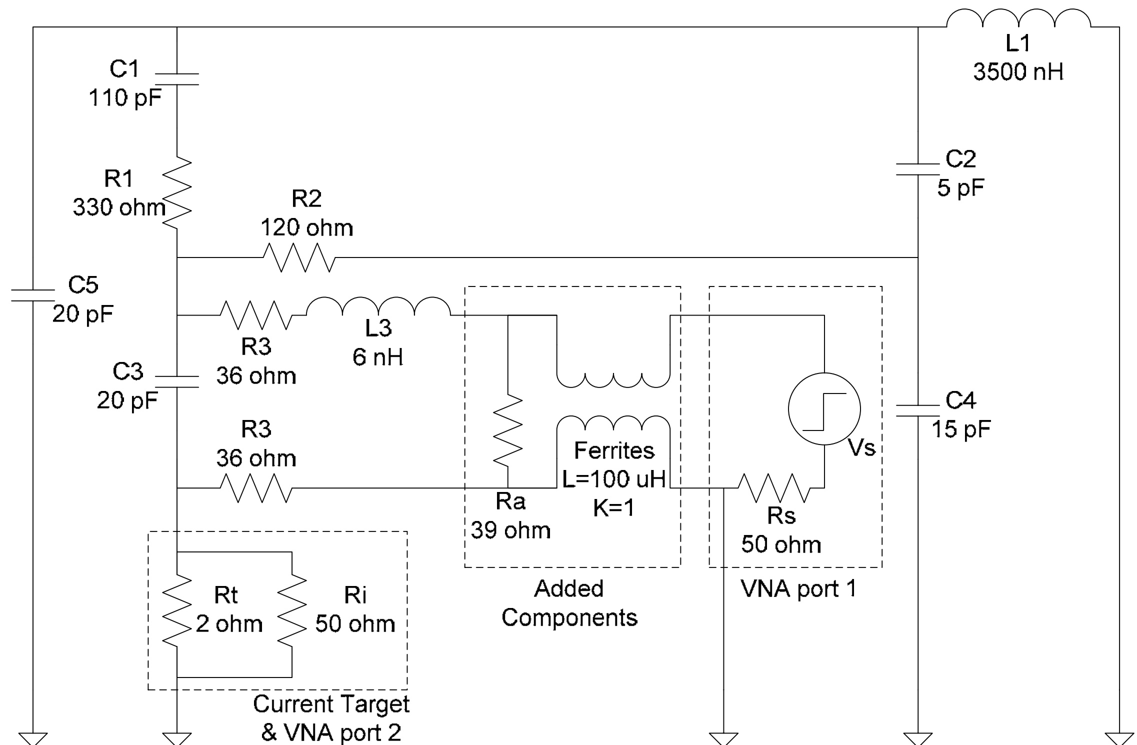

Fig. 6. Equivalent circuits of the modified ESD generator. Resistors Rt and Ri represent the current target resistance and input impedance of the vector network analyzer port 2. Port 1 is represented by a voltage source, Vs, and the internal impedance, Rs. The transformer and Ra indicate the ferrites and the added resistor for reducing source impedance respectively.

The current waveforms calculated using the circuits shown in Fig.5 and Fig. 6 are compared in Fig. 7. The data is scaled such that the second peaks have the same magnitude. Both waveforms are similar, however the circuit shown in Fig. 6 yields a

reduced first peak value, less swing and a larger rise time. This is a result of the source impedance given by the parallel connection of Rs and Ra. The source impedance increases the time constant of the pulse forming RCR low-pass filter, leading to a slightly slower rise time and a decreased discharge current.

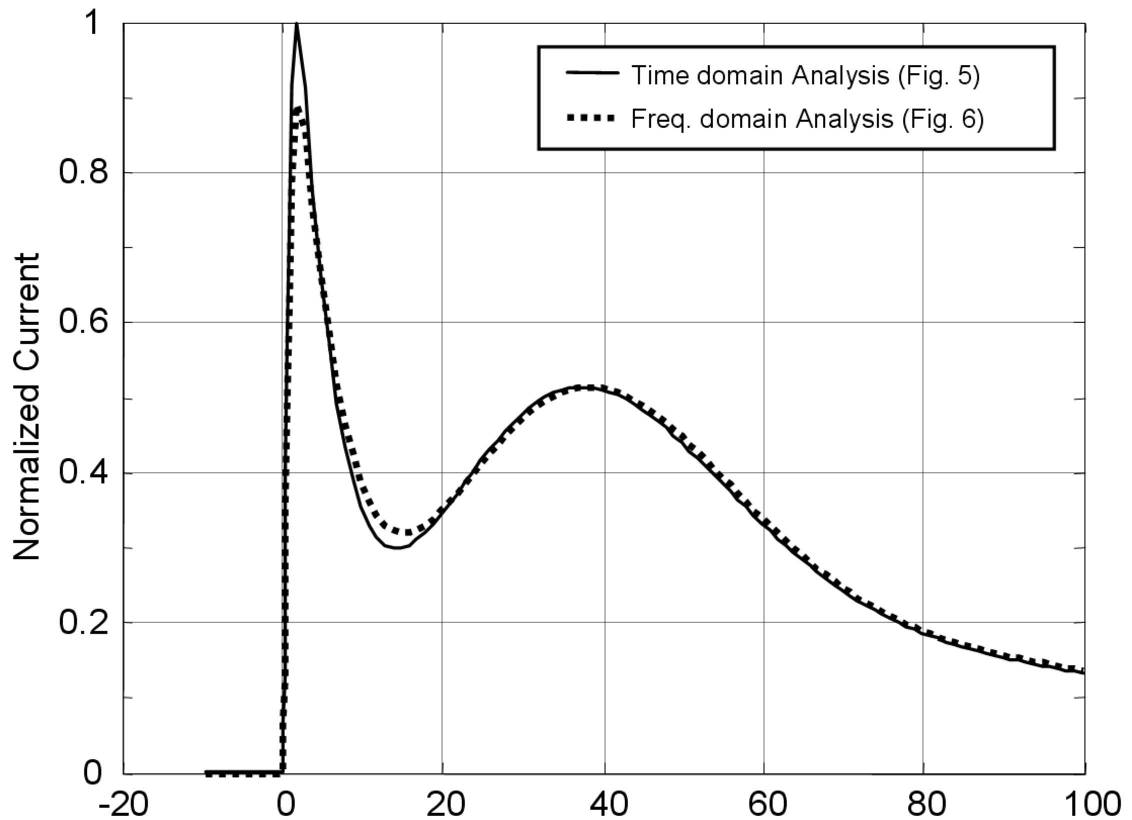

Fig. 7. Comparison of computed currents using time domain (Fig. 5) and the frequency domain analysis (Fig. 6).

III. Measurement Results

In each data set a time domain measurement (standard ESD generator) is compared to a frequency domain measurement using the modified ESD generator. Three such pairs are presented. Each emphasizes different aspects of ESD testing.

A. Time domain and frequency domain instrumentation

The testing used a 1kV setting of the normal ESD generator and a Tektronix 7404 (4 GHz BW, 20 GS/sec) oscilloscope. The oscilloscope was connected to the output of an ESD current target, an F-2000 current clamp or a small loop, respectively. For the frequency domain measurements an HP8753D vector network analyzer was used.

To compare the discharge current waveform a current target was selected as verification method. This is the best controlled measurement on ESD generators possible, see fig.8. The current target was mounted in the side wall of a shielded room. The second set of verification measurements used a small loop. Due to the derivative relationship between the field and the induced voltage this setup emphasized on the high frequency components of the fields.

In the third set of tests, a structure was selected that reflected the intended application of the method, i.e., the measurement of the coupling to the wires connecting to a PC mother board. More details of the measurement setup are shown in Fig. 13.

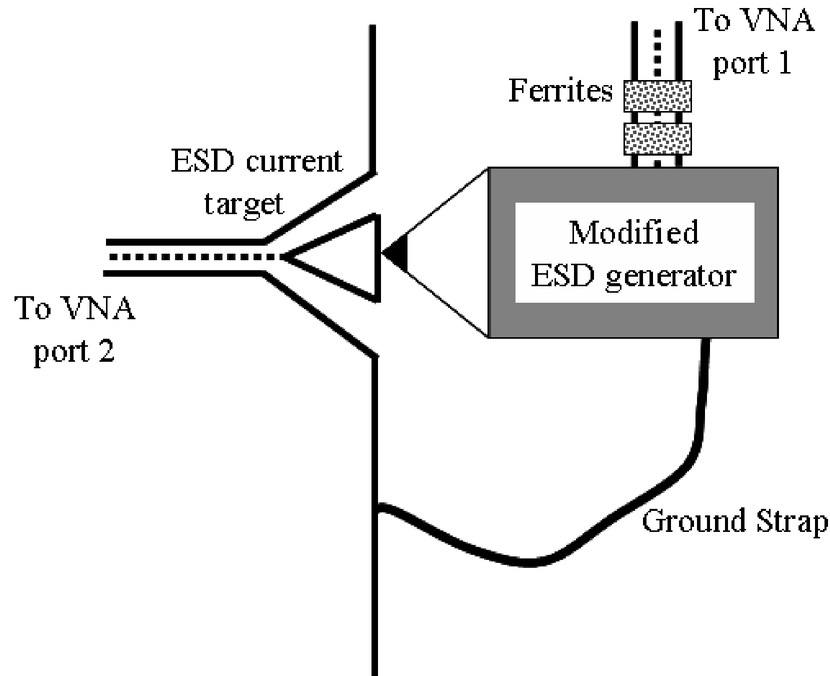

Fig. 8. Frequency domain measurement setup using vector network analyzer for the discharge current waveform.

Fig. 9 compares time and frequency domain measurements. The vector network analyzer measurement matches the general shape quite well however some deviations in the fine structure show up. The oscillations are more attenuated if captured using the VNA. Most likely this is a result of the source impedance of the VNA (39Ω || 50Ω) and the loading of the relay by the common mode impedance of the strongly ferrite loaded coax cable. The SPICE simulation of the previous section shows effects such as shifts in the frequency of the oscillations and larger attenuation.

We do not consider these differences to limit the range of applications of this method, given the variations seen between different samples of the same ESD generator models and especially between different brand simulators.

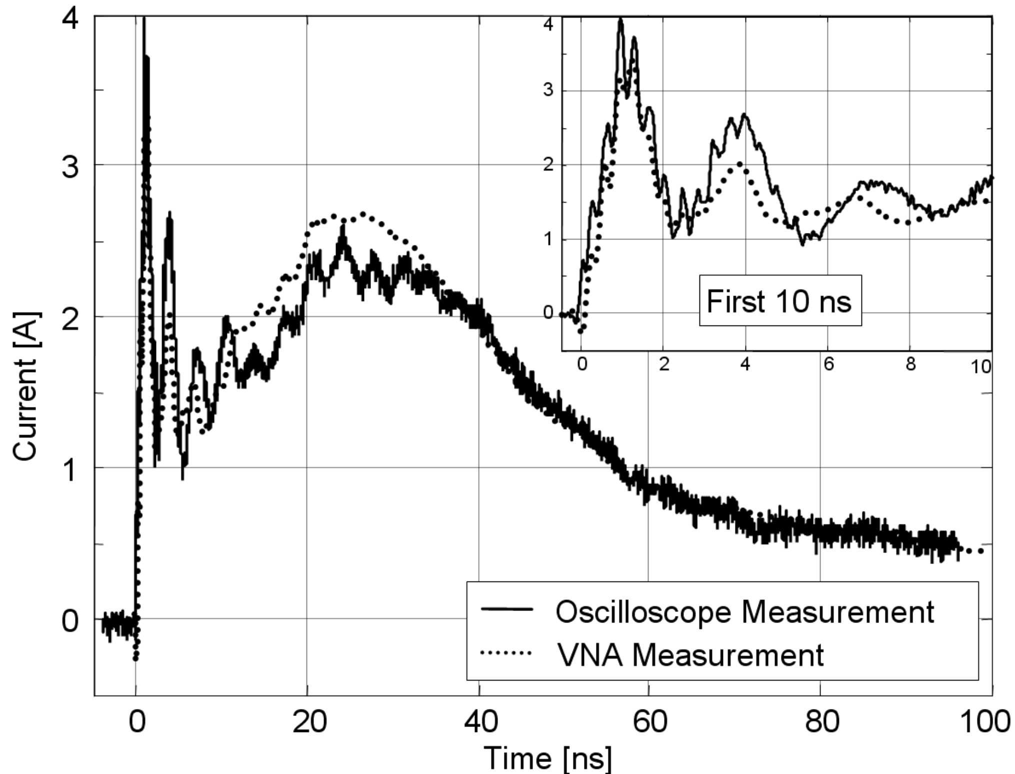

Fig. 9. ESD discharge current measured using the oscilloscope (Tektronix 7404, 4 GHz BW, 20GS/sec) compared to VNA measurements (HP8753D).

B. Induced loop voltage measurement in frequency domain

In [2] it has been shown that the transient fields are not only caused by the current at the injection point, but also by the currents within the inner structure of the ESD generator. Due to the difference in current rise times, the > 1GHz fields will be dominated by currents of the inner structure. To see the validity of the frequency domain analysis for fields especially at higher frequencies the voltage induced in a small loop has been measured.

A semi-circular loop (28 mm diameter, 0.7 mm wire diameter) was placed on a ground plane and connected to the oscilloscope or VNA respectively. See fig. 10 for the test setup and Figs. 11 and 12 for the results. These results indicate that the VNA method of measurement correctly excites the high frequency currents within the ESD generator.

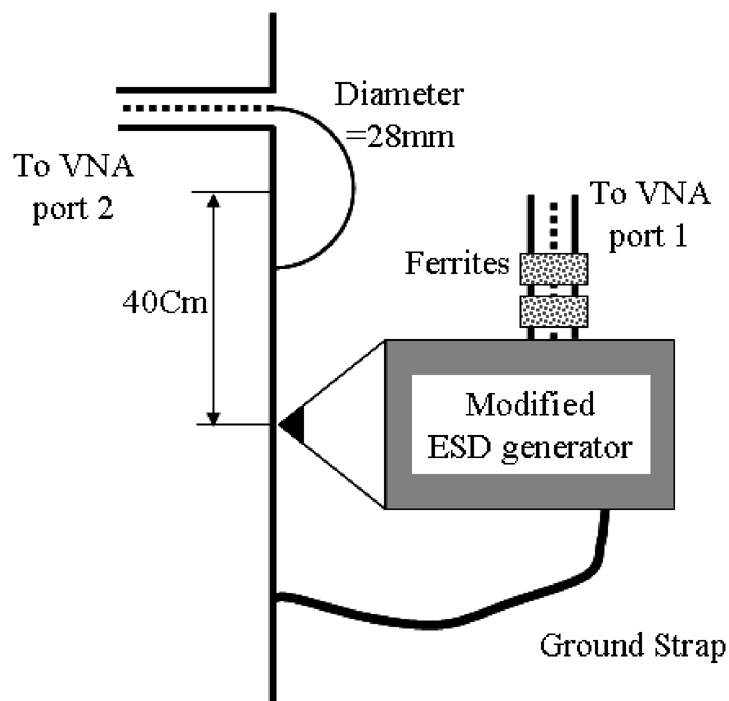

Fig. 10. Frequency domain measurement setup using a vector network analyzer for induced loop voltage measurement.

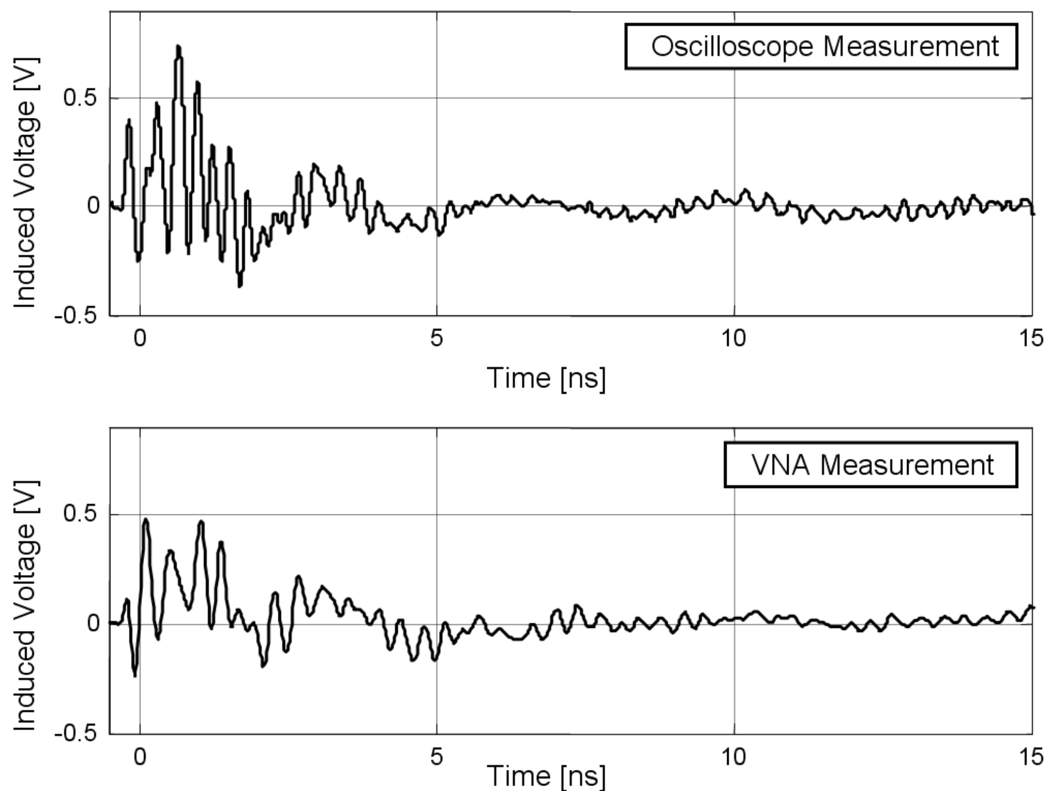

Fig. 11. Induced loop voltage for the measurement shown in Fig. 10.

Fig. 12 shows the spectrum of the measurement data presented in Fig. 11 obtained by FFT. Overall the vector network analyzer measurements reproduce the main features of the oscilloscopic measurements up to 2 GHz. The deviations at the lower frequencies are caused by the kHz low frequency cutoff of the network analyzer.

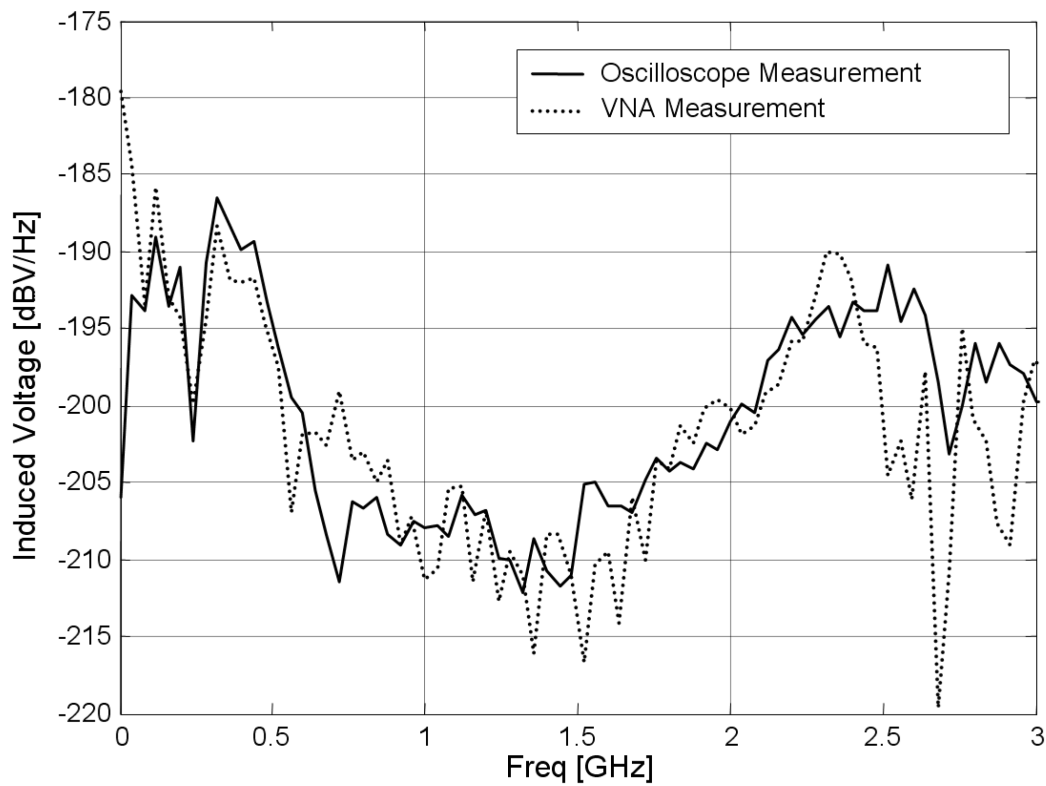

Fig. 12. Spectrum of the induced loop voltage for the measurement shown in Fig. 10.

C. Measurements of the voltage induced on a trace on a mother board in the frequency domain

A third test setup was selected that reflects the ESD coupling into the wiring and trace connected to an IC on a PC mother board. The other two test setups only emphasize one coupling path. Current target is useful for verifying if the discharge current is reproduced well and a small loop is used mainly to capture the transient fields and emphasizes the high frequency fields due to the derivative nature of the coupling.

Prior to measuring the voltage on the trace, the mother board was analyzed using the methods outlined in [14] and [15]. This showed that the "Power Good" trace was most sensitive to ESD. For this reason it was selected for monitoring the voltage induced by ESD.

The measurement setup is shown in Fig. 13. The operating mother board was placed on a metal plane using an insulating spacer. The ESDs from the generator were applied on the ground of the mother board while the voltage on the trace was measured. A ferrite loaded coax cable and a 470Ω SMT resistor were used to probe the voltage on the trace. A shunt capacitor C_{shunt} that filters the "Power Good" line coming from the power supply was removed to ensure that the upset of the mother board will be caused by coupling into the PGL wiring. This dropped the level at which the board resets from 8 kV to about 4 kV.

In Fig. 14, the comparison between the time domain and the frequency domain measurements are shown. The ESD generator was charged to -0.5 kV. At that level the mother board acts linearly, thus the trace voltage can be reproduced by the suggested method.

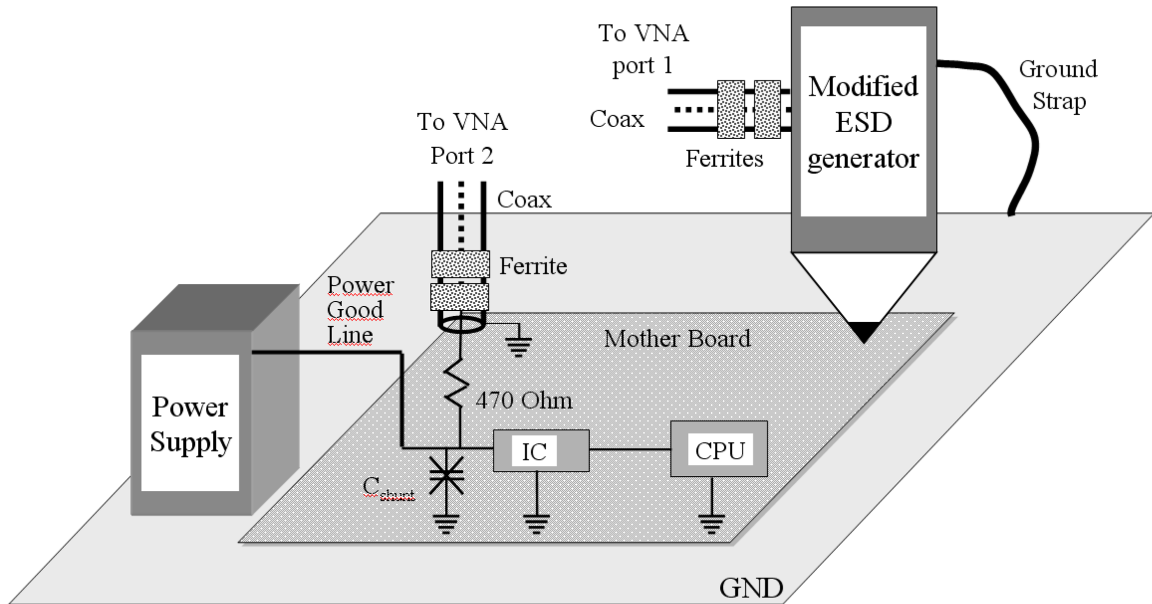

Fig. 13. Measurement setup for the ESD coupling to the mother board connecting wire and trace.

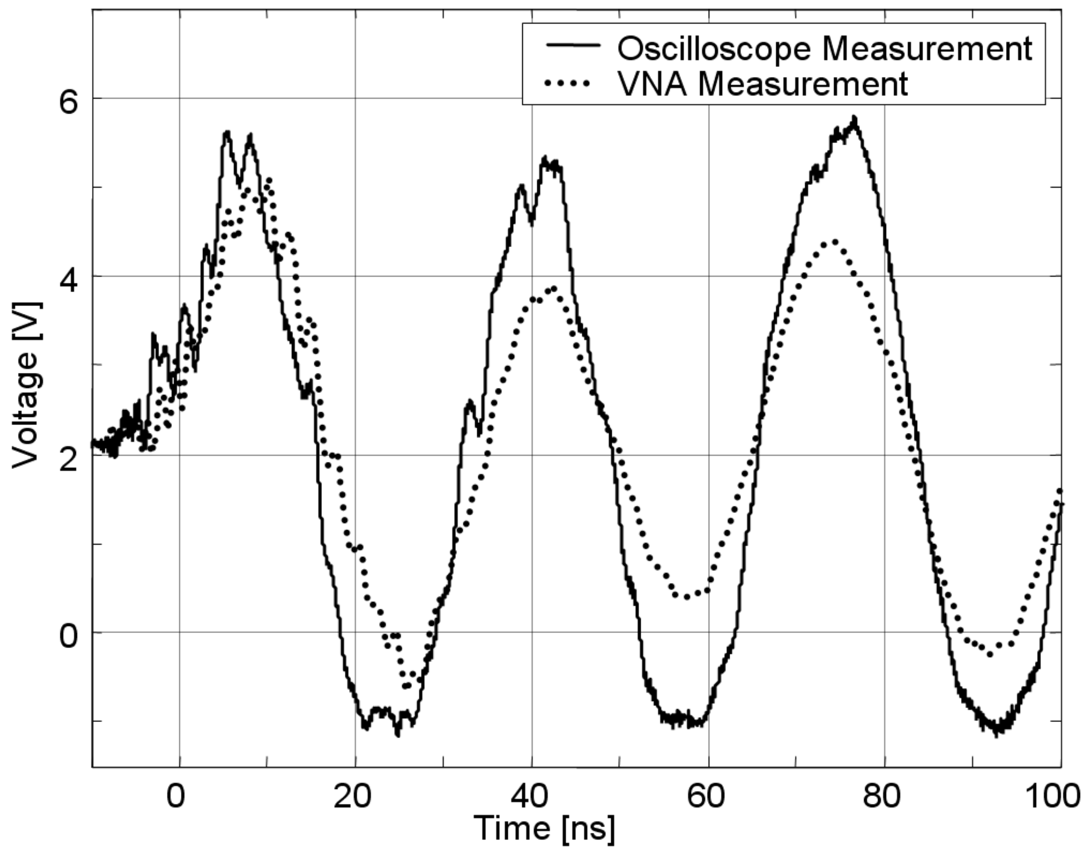

Fig. 14. Disturbed voltage measured on the "Power Good" trace on the computer mother board. The ESD generator was charged to -0.5kV. The frequency domain data was shifted by 2V DC.

IV. Discussion – Limits of the Method

The test data indicates that the VNA method is able to reproduce the ESD generator up to about 2 GHz. But the following limitations need to be considered for the proper application of the method.

A. Linearity

It requires that the coupling path is linear with respect to the applied discharge voltage. ESD generators used in contact mode are linear with respect to the charge voltage, i.e., the current waveform scales with voltage. Most coupling paths are formed by passive elements, e.g., shields, traces and inductive or capacitive coupling. In these cases the proposed methodology would correctly determine the currents and voltages on the traces. However if clamping effects of the ICs or non linear ESD protection is determining the voltages, the method could only be applied if the linear effects of "coupling into a trace" can be separated from the non linear effect of voltage clamping.

Fig. 15 shows an example of clamping. The measurement set up was the same as the one for Fig. 14, but the ESD generator was charged to -4.5 kV. The frequency domain data was scaled with the discharge voltage. If there is no dominate non-linear effect, the coupled voltage should scale linearly with the charge voltage of the ESD generator, however at -4.5 kV we see the clamping of the input voltage of the IC caused by the ESD protection diodes. Such clamping cannot be simulated by the VNA method suggested.

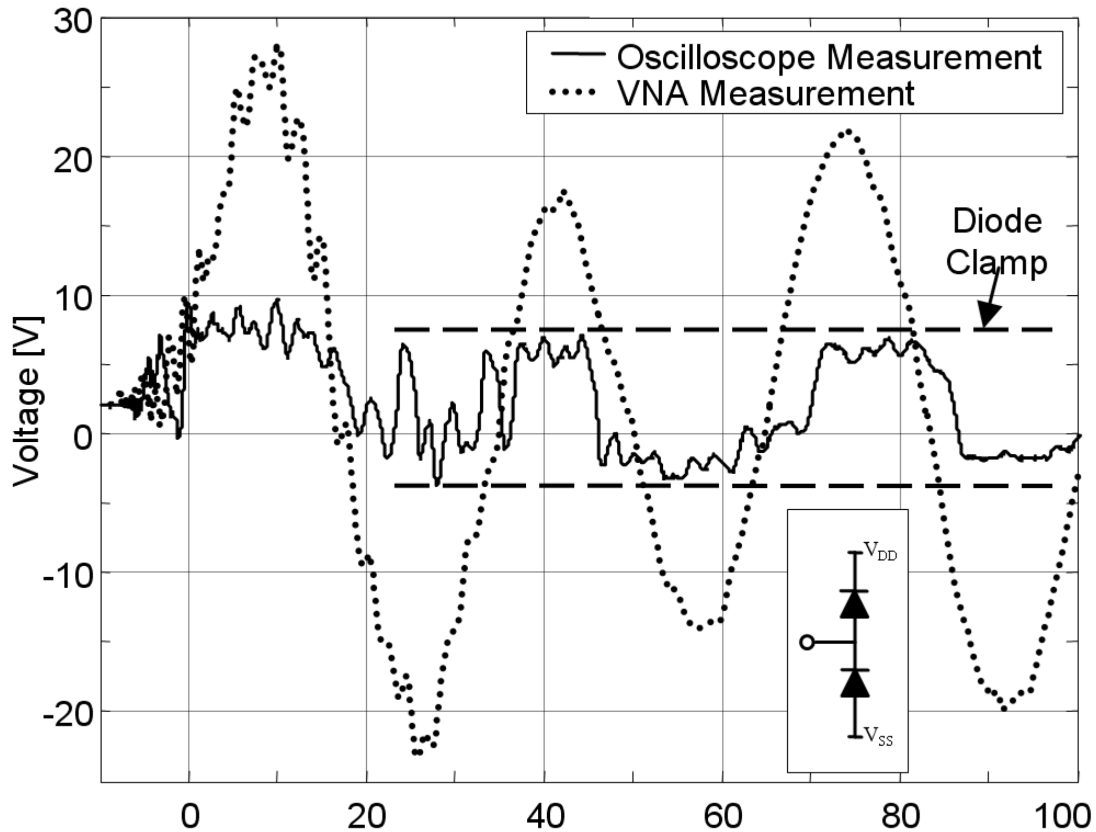

Fig. 15. Disturbed voltage measured on the "Power Good" trace on the computer mother board. The ESD generator was charged to -4.5kV and the clamping effect is shown.

When soft-errors are caused by ESD, the induced voltages are often below the clamping thresholds, as bit-flipping can occur at voltage levels between GND and VCC. Of course, in cases in which a primary ESD causes a secondary breakdown, the methodology will not be able to reproduce the coupled voltages. Overall, we suggest using the method for coupling measurements, but not for circuit response measurements. It offers the opportunity of ESD analysis without the risk of damage as one may want to perform in complex one-of-the kind systems.

Those would need to be modeled, e.g., using SPICE by combining the coupling data with the non-linear circuits.

B. Equality of the excitation

The relay blade contact is substituted by a 50 Ω VNA port having an additional 39 Ω resistor in parallel. However, the impedance of the spark within the relay cannot simply be represented by a 22 Ω (50 Ω paralleled by 39 Ω). If sufficient current is flowing it is better modeled by a constant 25-40 V drop than by a resistor. The effect of the source impedance has been analyzed by comparing two cases: A 50 Ω source impedance and a 22 Ω source impedance. It can be seen in fig. 16 that the higher impedance leads to less ringing, indicating that even 22 Ω might not be sufficiently low to fully represent the details of the initial peak of the waveform. However, since the objective is to determine the coupling, one needs to weigh the differences in the waveforms against the variability of the coupling. Its variability is determined by the reproducibility of the chassis contacts and the wire positions.

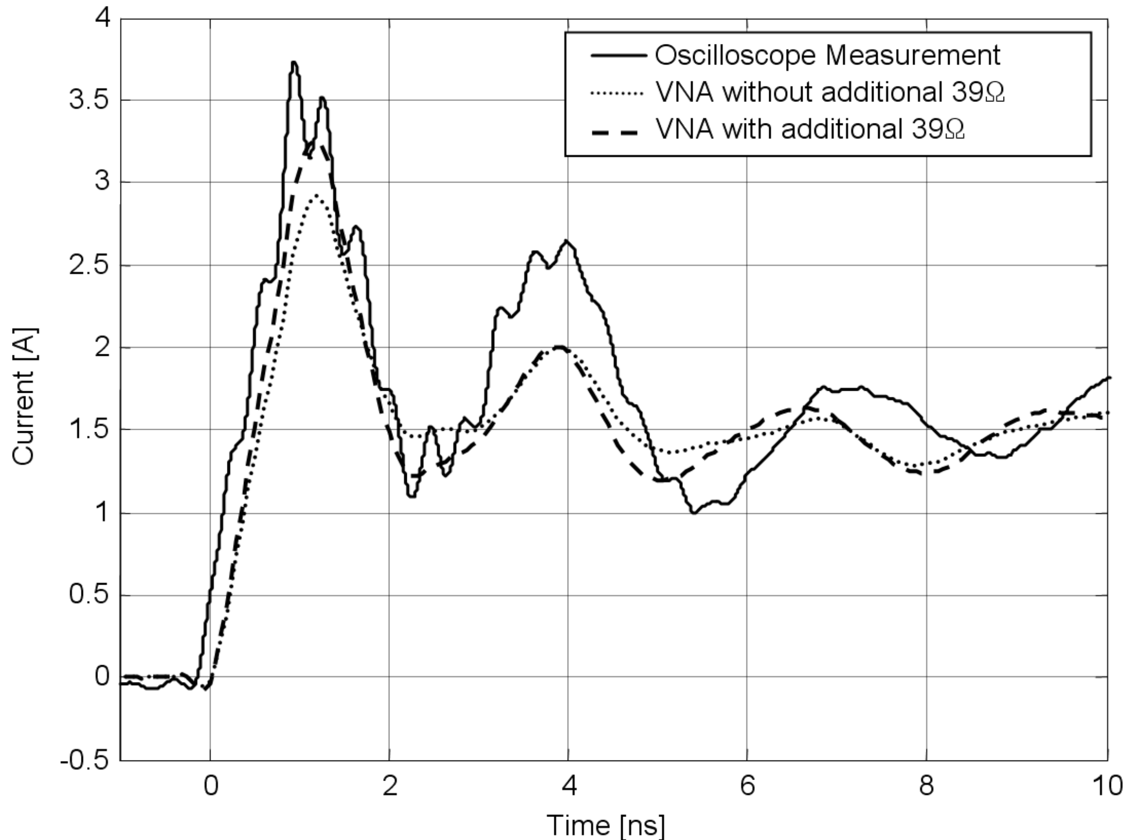

Fig. 16. Frequency domain measurement data with and without an additional parallel 50Ω resister are shown together. The effect of source impedance modeling for the voltage collapse between the relay contacts can be seen in this figure.

C. Common mode currents flowing on the coaxial cable

Ideally, the excitation would not alter any currents within the ESD generator and its ground strap. However, an additional cable is attached. Common mode currents on this cable alter the current and radiation characteristics. In our experiments a 20 mil semi-rigid cable, having many ferrite sleeves along its length and additional high permeability material to suppress any low frequency currents, was used. However, the common mode current cannot be fully suppressed. This attenuates oscillations somewhat.

V. Conclusion

A method for characterizing ESD generators and coupling in the frequency domain has been proposed. This method allows analysis of both discharge current and field effects due to the high voltage break down in the ESD generators without the need to operate at high voltages. The method has been substantiated by SPICE simulations and verified by comparison of modified to non-modified ESD generators.

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Paper 3

A NON-LINEAR μ-CONTROLLER POWER DISTRIBUTION NETWORK MODEL FOR CHARACTERIZATION OF IMMUNITY TO EFTS

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***** National Semiconductor Corp.**

ABSTRACT

A non-linear power distribution network (PDN) model for characterizing immunity of integrated circuits (ICs) to electrical fast transients (EFTs) is proposed and validated. The model includes ESD protection diodes and passive impedances between power domains. Model parameters are based on external measurements using a vector network analyzer and curve tracer. Methods developed for de-embedding the impedances that lie between power domains while the IC is operating are explained. Inclusion of active power-clamp circuitry is also explored. The model is able to successfully predict pin currents and voltages during EFTs on the power pin when the IC is operating or turned off and when the ESD power clamp is activated or not activated. This model might be used to evaluate the immunity of the IC in a variety of systems and to better understand why failures occur within the IC and how to fix them.

Keywords: Power distribution network, electrical fast transient, immunity, modeling, power rail clamp

I. INTRODUCTION

Models of integrated circuits (ICs) are becoming common for estimating emissions **Error! Reference source not found.**. Several modeling paradigms exist, including the integrated circuit electromagnetic model (ICEM) [2], [3] and the linear equivalent circuit and current-source (LECCS) [4], [5] model. The ICEM model was created to estimate the conducted emissions from an IC without significant model complexity. In this model, the noise generated from internal activity is distributed through a passive power distribution network (PDN) and inter-block coupling network. The LECCS model was proposed to evaluate the RF noise current generated by core logic on power pins **Error! Reference source not found.**. Both models are similar in design and function. Beyond estimating conducted currents, these models can be combined with a model of the printed circuit board (PCB) to estimate noise on the power bus [2], [3], **Error! Reference source not found.** and the influence of decoupling capacitors [2], [3], [7], among other applications.

While estimation of emissions is more common, IC models may also be used to predict immunity of ICs. For example, the ICEM model has been used to predict jitter in a phase-locked loop due to power-bus noise [7]. Nakayama [8] has shown that the LECCS model can estimate the noise on the IC power rail caused by direct RF power injection [9]. The use of models to anticipate the IC's response to electrical fast transients (EFTs), however, has not been explored.

Immunity to EFTs is particularly important in applications that are switching inductive loads, like motors or solenoids. The voltage and current spikes on power or I/O pins caused by the switching event may result in bit errors, chip reset, clock jitter or

interruption, or even permanent damage to the IC. The IEC defines specific standards for evaluating system-level immunity to EFTs [10]-[12]. While no standard exists yet for evaluating EFT immunity of ICs, these system-level standards are often referred to for that purpose [13], [14]. Typical disturbance source waveforms have rise times in the range of a nanosecond to several milliseconds and pulse widths in the range of tens of nanoseconds to tens of milliseconds and are applied as a single pulse or as a burst of pulses. The tests are performed while the IC is operating.

Protection against ESD events is often a primary concern of the IC designer. Protection diodes [15] are typically placed where external pins are connected to the die in order to divert ESD current to the power rails before it causes large voltage differences that would damage gates. Many ICs also use power clamps between the power and return rails. A common power clamp uses an RC-like trigger circuit to turn on the power clamp when the power rail voltage changes faster than a rate set by the RC time constant and the power rail is not powered [16]. The response of the ESD protection circuitry to EFTs, however, is rarely considered.

Deutschmann reports that conducted transient disturbances can cause the destruction of ESD protection structures, MOSFET gate oxides, and metal traces [13]. In his work, the thermal destruction of large areas of silicon after a transient event was used to link IC damage with particular test pulses. Using this information to improve transient immunity, however, is difficult because the location of failures cannot easily be used to determine the current path and *why* the IC failed at that location nor to test possible solutions to the failure.

Determining the performance of an IC in specific systems before they are built and determining the cause of EFT failures and their solution requires models of the IC for that purpose. Current models may not meet this criterion since they are largely designed to estimate emissions. In this paper, a simple non-linear PDN model of an 8-bit microcontroller is proposed and tested for estimating currents during transient events on the power network. The model is expected to yield useful information about the performance of the IC in specific systems, about how and where the current flows on the IC power rail during transient immunity tests, and about the operation of IC protection circuitry. The following paragraphs will describe the IC model, the methods used to extract model parameters from IC measurements, and the validation of the model through simultaneous measurement of pin currents and voltages while EFTs are applied to the IC. Application of the model to predict currents inside the IC and the performance of ESD protection circuitry during an EFT is also discussed.

II. PDN Model

The 8-bit microcontroller modeled here has two power domains, one for the core and one for the analog-to-digital (A/D) converter. The PDN model for this IC is illustrated in Fig. 17. The pins labeled VDD and VSS are power and return pins for the core and the pins labeled VDDAD and VSSAD are the power and return pins for the A/D converter. The average switching current consumed by each power domain is modeled as a voltage-dependent current source. Coupling between power rails is modeled using passive elements, Z_i. Capacitive coupling to the PCB is modeled with the DIE-to-PCB capacitance, C_d. ESD protection diodes are included to simulate current paths during EFT events. The bond wire and lead frame model includes the capacitance to the PCB, C_w, as

well as the inductance and resistance, L_w and R_w, associated with the structure. Initial tests only included the components discussed here in the PDN model. Later, in the applications section, a model of the active power clamp circuitry was also included as part of the PDN.

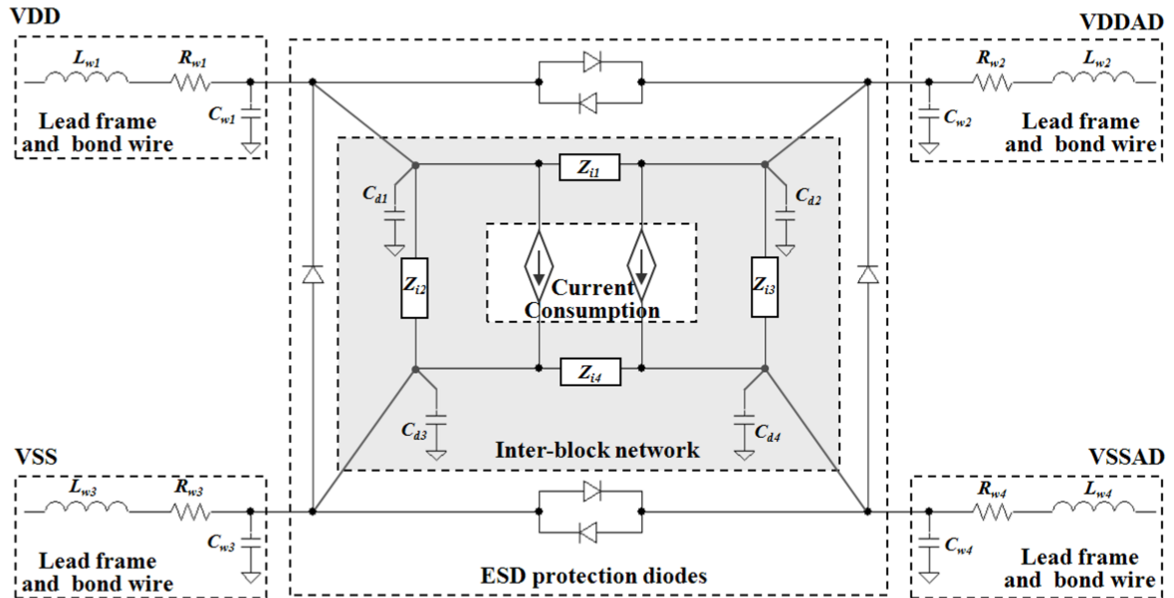

Fig. 17. Non-linear PDN model of the 8-bit microcontroller.

III. Measurement of Model Parameters

Model parameters describing the passive PDN were found through external measurements. Measurements were performed while the IC was configured in STOP mode to prevent internal switching noise from interfering with measurements. The IC included two return pins for the core, VSS1 and VSS2. The characteristics of each of these pins was found separately. Impedances were determined from 2-port S-parameter measurements and characteristics of diodes were determined from I-V curves, as described below.

A. Current Consumption

The current consumed by the IC in STOP mode is constant but is a function of the supply voltage. DC current consumption was measured with a current meter connected to each power domain supply voltage. Current consumption by the core was modeled using a diode in SPICE, where model parameters were modified to mimic the current consumption observed when the IC was powered around its normal power supply voltage. No current model was used for the A/D converter, as only negligible current was observed through VDDAD in STOP mode.

B. Inter-Power Domain Network

As the characteristics of the IC change with bias – particularly the values of capacitances associated with non-linear devices – measurements were made when the IC was powered with 5 V and when it was unpowered. The IC was placed over the solid copper plane of a PCB and full 2-port S-parameter measurements were performed for each pair of pins.

The measurement of impedance parameters for the VDDAD/VSSAD pin-pair is shown in Fig. 18. Each pin requires either a supply voltage of 5 V or of 0 V to maintain proper operation during the measurement. RF current paths through other pins (e.g. from the VNA and back through the power supply connections) are blocked by the bias T inside the VNA while maintaining a supply voltage of 5 V on VDDAD and 0 V on VSSAD. For measurement of VDDAD/VSSAD, the VSS1 and VSS2 pins were directly shorted to the PCB return plane. The VDD pin was connected directly to the power supply but effectively shorted to the PCB return plane at high frequencies using a 2.2 uF SMT capacitor mounted at the IC. The characteristics of other pins were found similarly by changing the connection of pins to the network analyzer and to the power supply. Y-

parameters for each pin-pair were then found from the full S-parameter measurements. Values of Z_i between pins were then found as $1/(-Y_{12})$ from low-frequency measurements, where the impact of the bond-wire inductance on measurements was negligible.

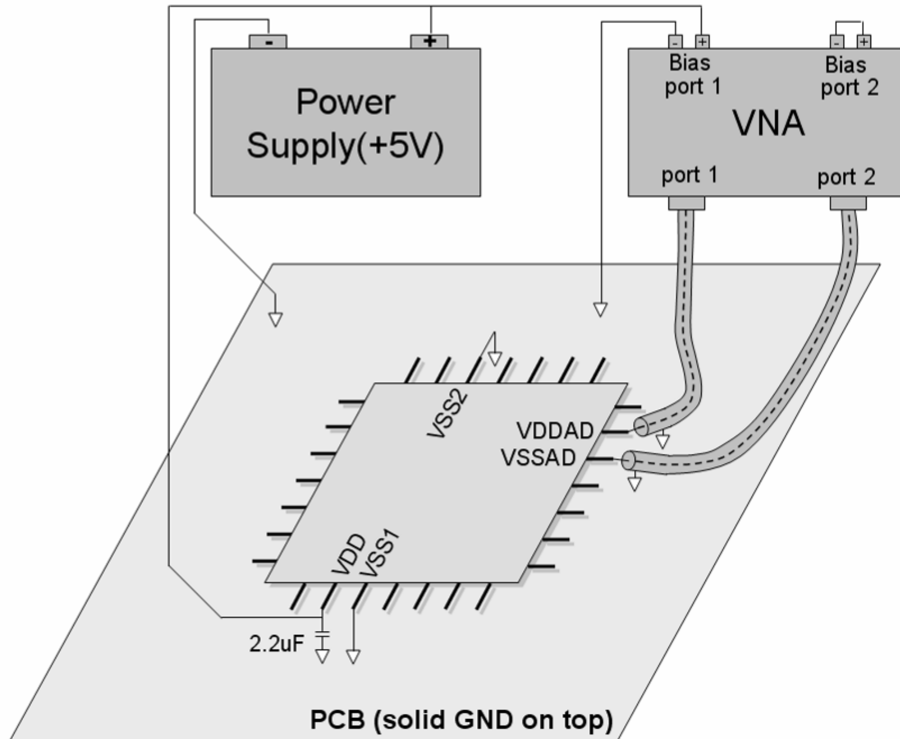

Fig. 18. Measurement of impedance parameters for the VDDAD/VSSAD pins.

An example measurement of the impedance between VDDAD and VSSAD is shown in Fig. 19 when the supply voltage was 5 V and was 0 V. In the low frequency range, the impedance is predominantly capacitive and depends on the supply voltage.

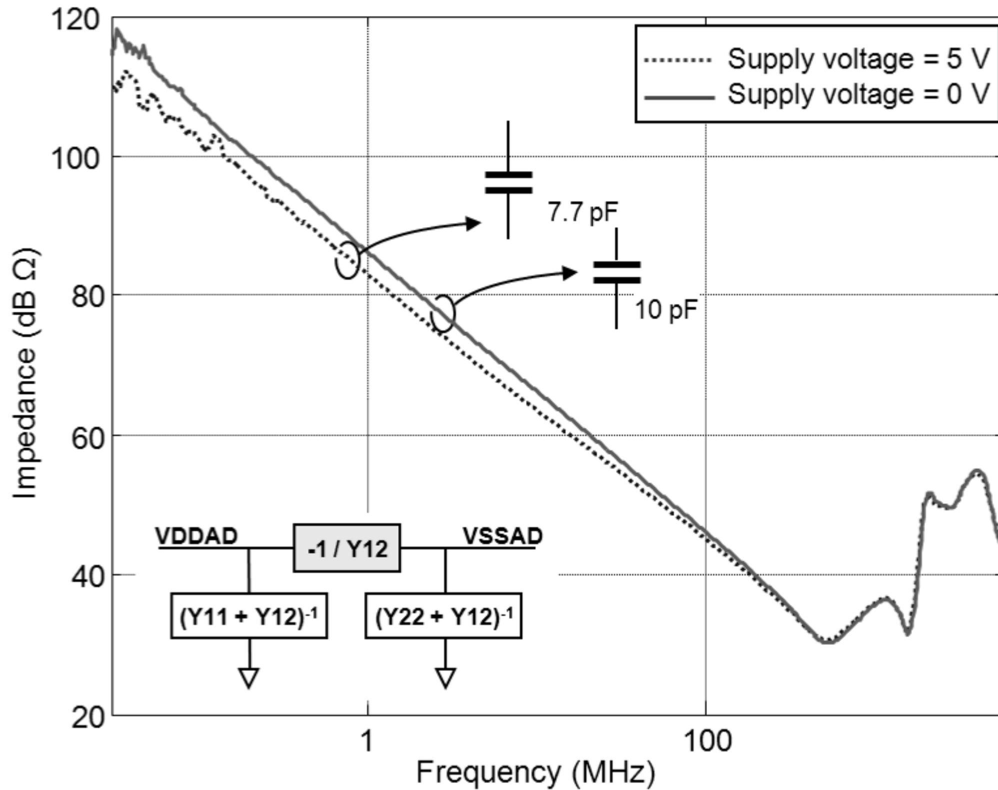

Fig. 19. Measured impedance between VDDAD and VSSAD when the supply voltage was 5 V and 0 V.

C. ESD Protection Diodes

The I-V characteristic of each ESD protection diode was measured using a curve tracer. These diodes were then modeled in SPICE by modifying the parameters of a generic diode model to match the measured curve. The voltage-dependent depletion capacitances are included in the inter-power domain capacitance and depend on the bias voltage, either 0 V or 5 V. The diffusion capacitances and reverse recovery were ignored.

D. Lead Frame and Bond Wire

Values of resistance and inductance, R_w and L_w, were found for each pin through a numerical fit of values of S_{11} or S_{22} measured as shown in Fig. 18. Fig. 20 shows an example comparison of measured and simulated impedance profiles for the VDDAD pin, while the VSSAD or VDD pin was connected to the network analyzer port as shown in

Fig. 18. The resonance at around 600 MHz is primarily determined by the lead frame and bond wire inductance of the VDDAD pin and the associated capacitance of the PDN structure.

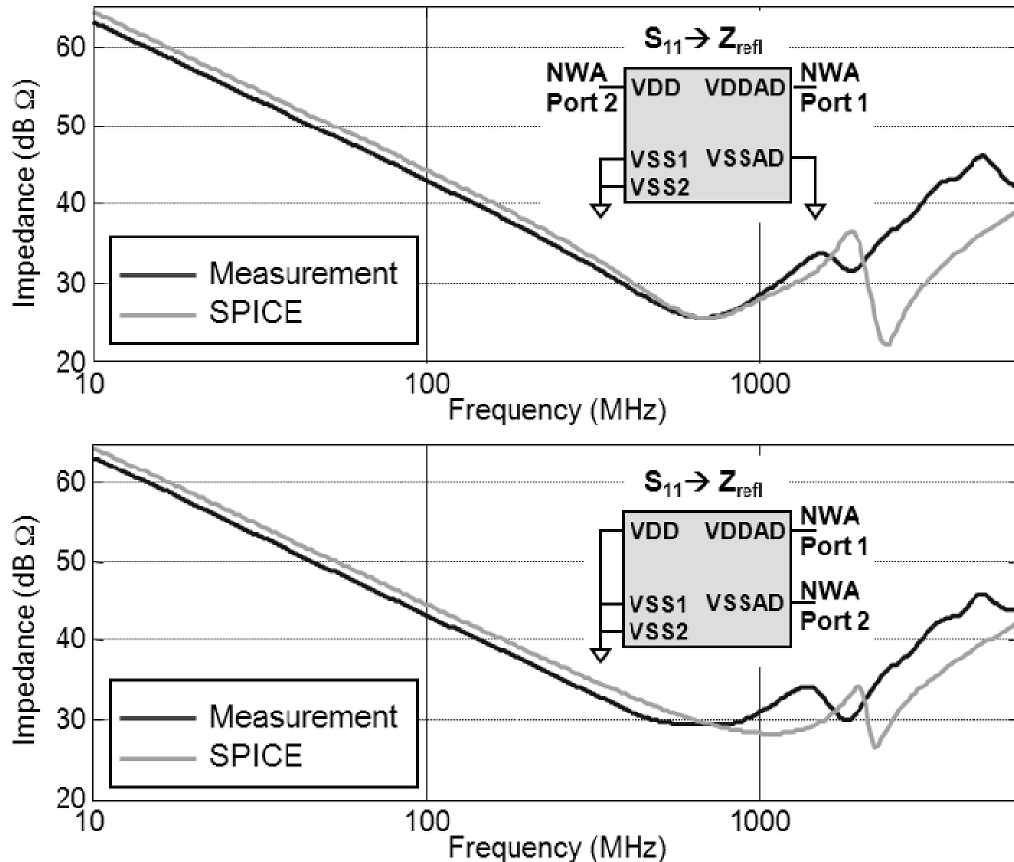

Fig. 20. Comparison between measured and simulated impedance seen from the VDDAD pin while VDD or VSSAD pin was connected to the network analyzer.

The DIE-to-PCB capacitance, C_d, and the lead-frame/bond wire-to-PCB capacitance, C_w, were estimated together by measuring S_{11} seen from the lead frame using a network analyzer as shown in Fig. 21. The network analyzer was connected to one pin (e.g. VDD), while all other pins were floated. The measured S_{11} was then converted to impedance, which was used to estimate the value of the combined capacitance, C_d+C_w.

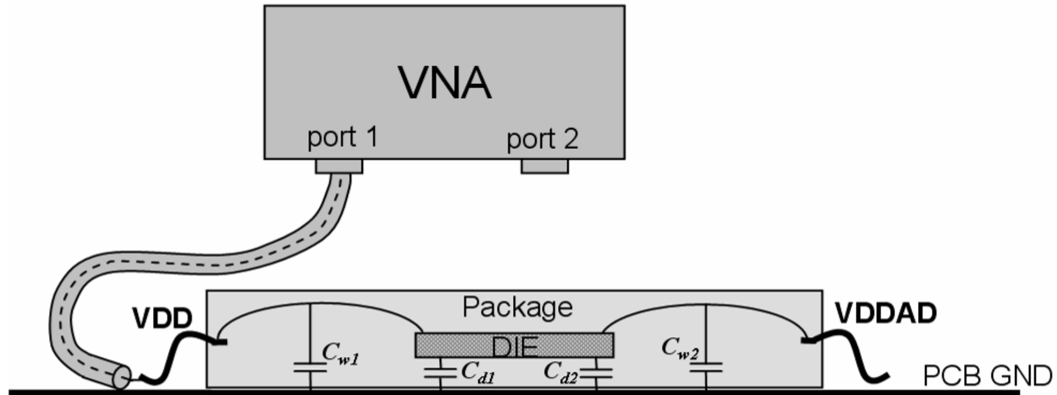

Fig. 21. Measurement of the DIE-to-PCB capacitance, C_d, and lead frame/bond wire-to-PCB capacitance, C_w.

E. Complete Models

The complete model of the PDN extracted for supply voltages of 5 V and 0 V is shown in Fig. 22. Values for a 0 V supply are shown in parentheses. Note that the capacitances in the inter-block network change when the supply voltage is changed due to the redistribution of carriers at non-linear junctions. These capacitances were calculated from measurements at tens of megahertz. The capacitance C_w includes the lumped impact of the bond wire-to-PCB, the lead frame-to-PCB, and the DIE-to-PCB capacitances, though their values are relatively small and have little impact on the model performance.

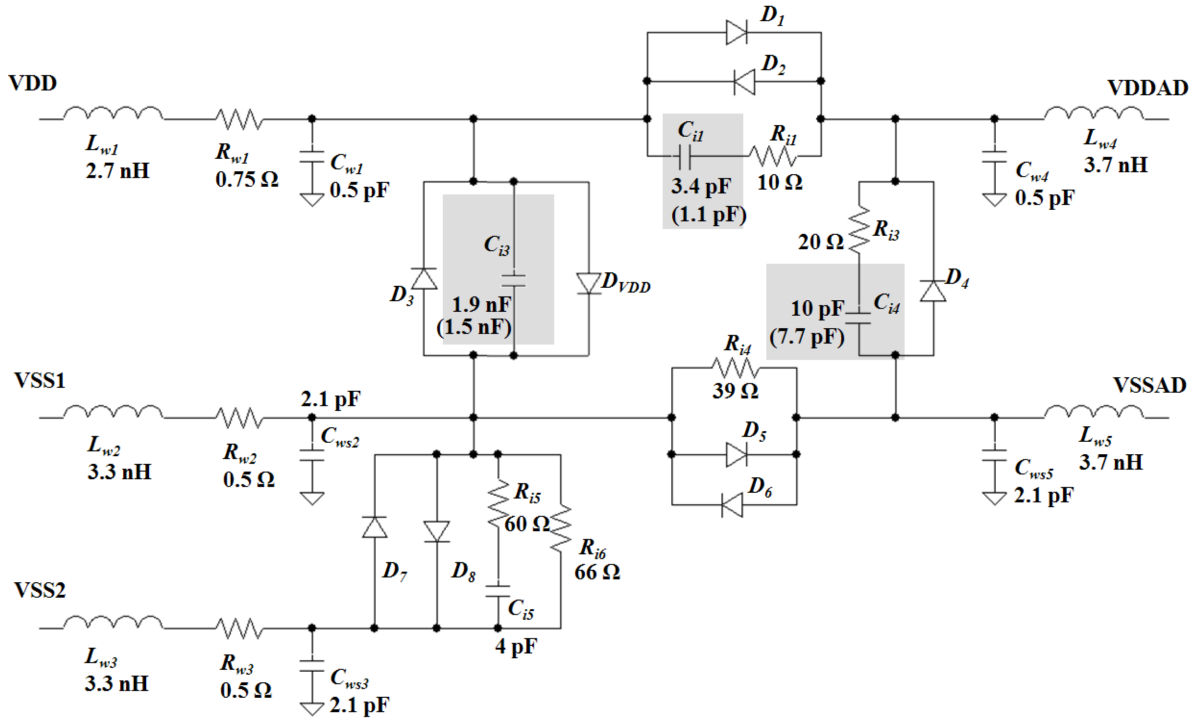

Fig. 22. Complete non-linear PDN model for the 8-bit microcontroller. The components in the shaded areas have different values for a 5 V and 0V supply. Their values when the supply voltage is 0 V are shown in parentheses.

IV. Validation

The model was validated by capacitively applying EFT pulses to the power rail using an EFT generator (EFT 500 – M from EM TEST), in compliance with IEC 61000-4-4 [10]. Pin currents were measured using a loop embedded underneath traces connected to pins of interest as shown in Fig. 23. Voltage across the loop is measured by connecting the inner conductor of a semi-rigid coax cable to one via of the loop and the outer shield to the bottom loop-trace. Mutual inductance between the trace and the loop is found through measurements of S_{21} at calibration locations on the PCB. Pin current is calculated from the mutual inductance and the voltage measured across the loop during the EFT event. Self inductance of the loop was ignored as it was not important below 1 GHz.

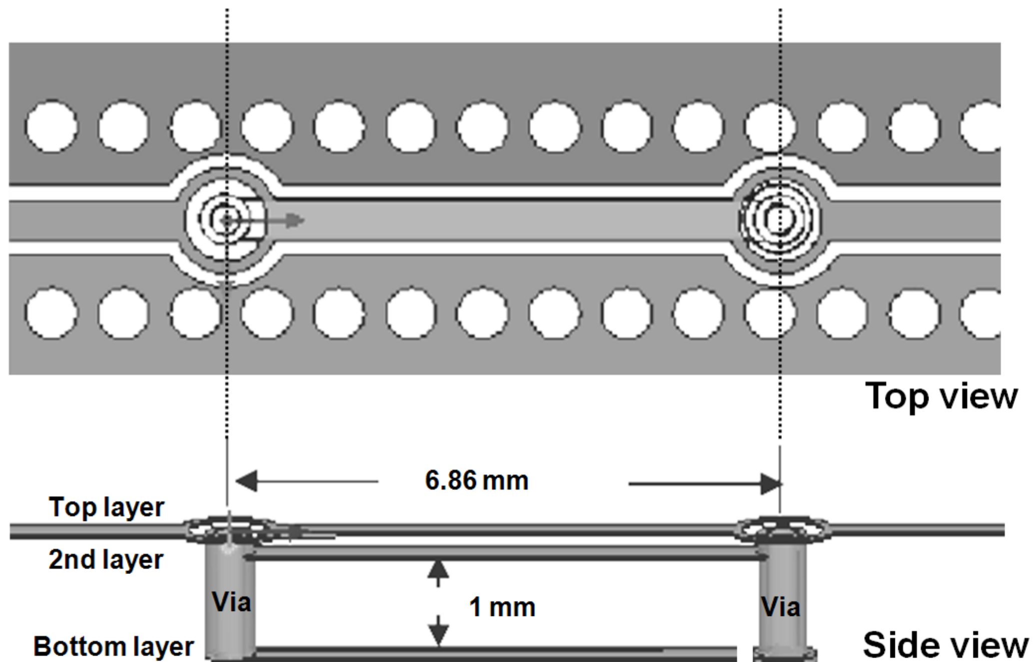

Fig. 23. The current measurement loop embedded in the 4-layer Test PCB.

The setup used to measure the IC response to EFTs is shown in Fig. 24. The IC was mounted on a test PCB which has a trace and current measurement loop for each power and ground pin. The EFT generator was connected to the VDD trace on the test PCB through a high voltage attenuator and a 10 nF capacitor. The power supply was RF-decoupled from the IC using ferrite beads. The test PCB was not configured with power planes or local decoupling capacitors, to ensure the EFT current flowed through the IC.

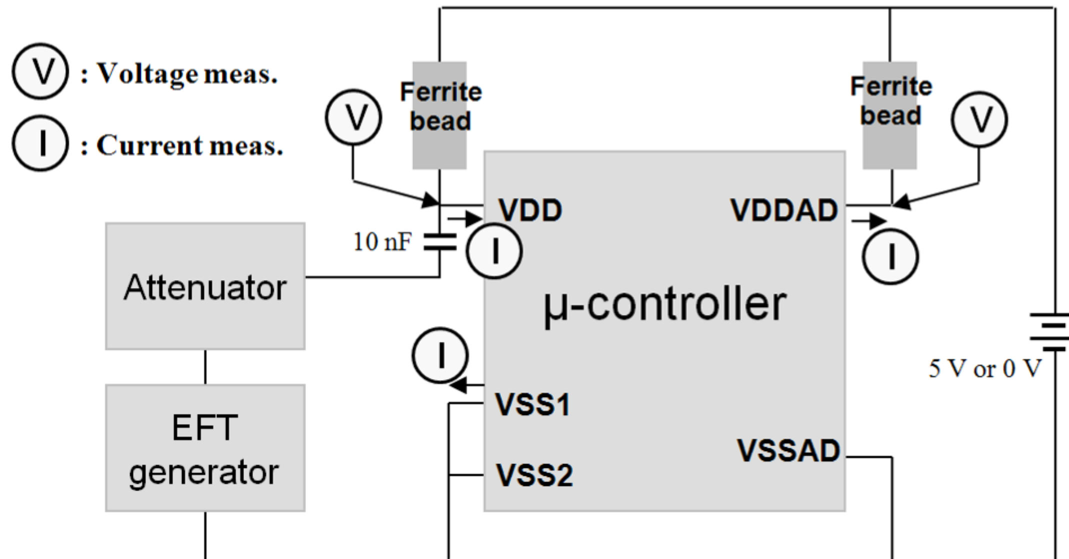

Fig. 24. Diagram of a test-setup to measure pin voltages and currents during capacitive injection of EFT current to the VDD pin.

Pin voltages and currents were measured using a 6 GHz, 20 GSa/s oscilloscope. Voltages were measured on the VDD and VDDAD pins. Currents were measured on the VDD, VDDAD, and VSS1 pins. Measurements were performed with supply voltages of 5 V and 0 V. The severity of the EFT injection was adjusted by changing the voltage set on the EFT generator and the size of the attenuator. The severity was set such that the ESD protection diodes would be fully turned on but the IC would not be permanently damaged. Different severity levels were used to trigger the power clamps or to leave them inactive.

Fig. 25 compares measured pin voltages and currents with SPICE simulation results performed using an effective injection source and a power supply voltage of 5 V. The simulations included the entire measurement circuit (e.g. ferrite beads, probe loading, etc). The EFT generator was modeled as a voltage source connected to a 50 Ω source impedance. The EFT model was found from another setup where an oscilloscope was directly connected to the EFT generator through a high voltage attenuator. The measured

EFT waveform was properly scaled and imported to SPICE to be used as the EFT voltage source. Here, the EFT generator was set to a charge voltage of 500 V and connected through a 40 dB attenuator. For the test in Fig. 25, the EFT voltage level was set so that the ESD diodes would turn on but the power clamps would not.

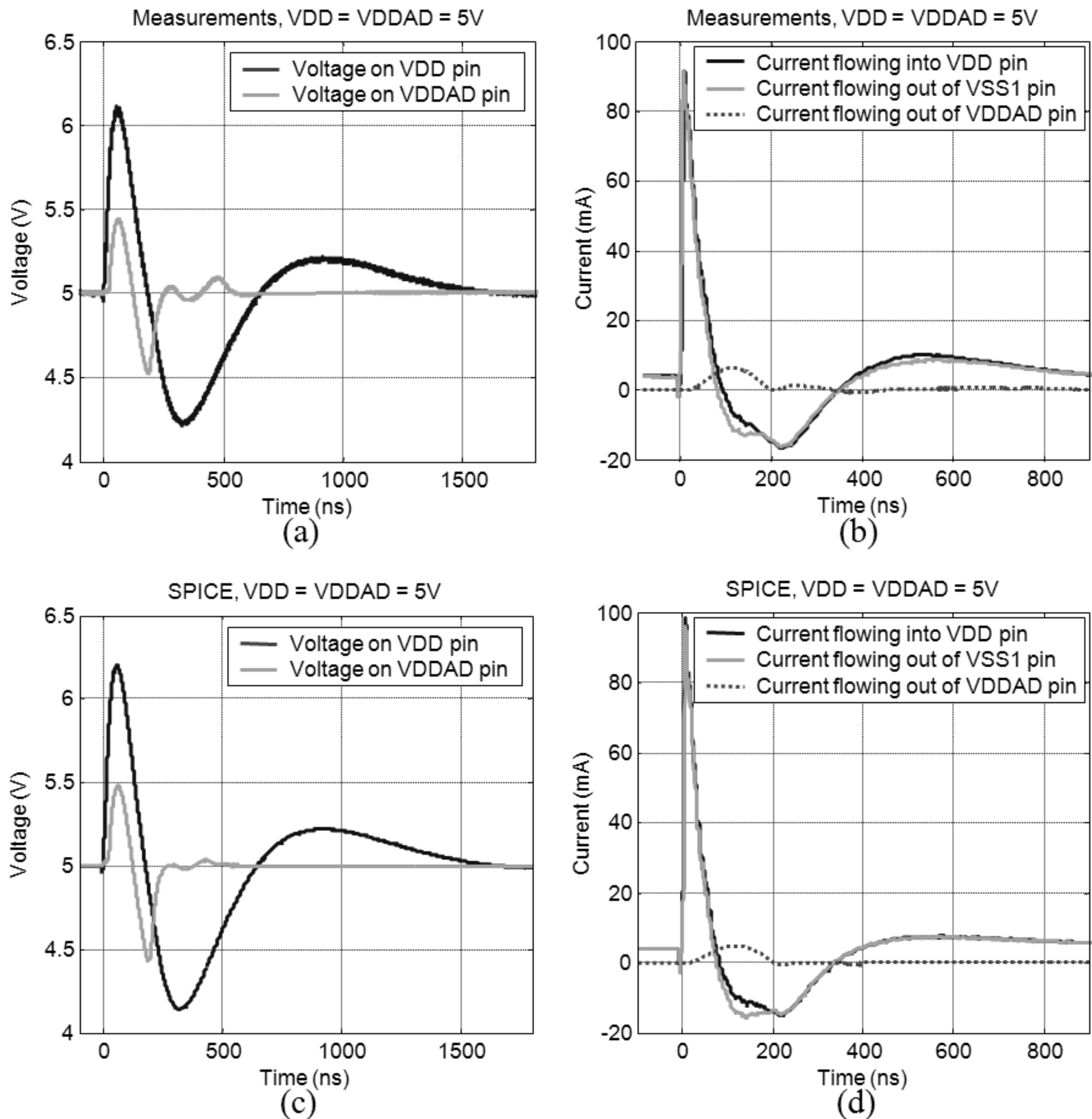

Fig. 25. Comparison of measured and SPICE simulation results for a capacitively-coupled EFT pulse (500 V with 40 dB attenuator) injected on the VDD pin with a supply voltage of 5 V.

As shown in Fig. 25, the VDD pin current for t<0 ns was approximately 3.5 mA. The embedded loop probe cannot measure DC current, so the measurement results were offset by 3.5 mA before plotting. As the EFT current flows into the VDD pin, the voltage on VDD rises and the diode between VDD and VDDAD turns on. From t=20 ns to t=200ns, current flows out of VDDAD and the voltage between VDD and VDDAD is approximately 0.7 V. Most of the current flowing into VDD comes out of pin VSS1, which is the least impedance path for both DC and RF. The SPICE simulation results closely matched the measured results in all tested cases.

Fig. 26 compares the measured and SPICE simulation results when the supply voltage was set to 0 V. Besides the offset voltage, the measurement setup was the same as in Fig. 25. The transient response here lasts for more than 1 μsec, which is much longer than the EFT pulse duration of approximately 200 nsec. The long transient response is caused by the decoupling ferrite beads mounted between the VDD and VDDAD pins and the power supply, showing that the method used to decouple the power supply may affect the EFT test results. The voltage drop on the VDD and VDDAD pins were clamped to -0.5 V at approximately 220 nsec indicating the ESD protection diode between these pins was turned on. As in Fig. 25, the measured and simulated results match well.

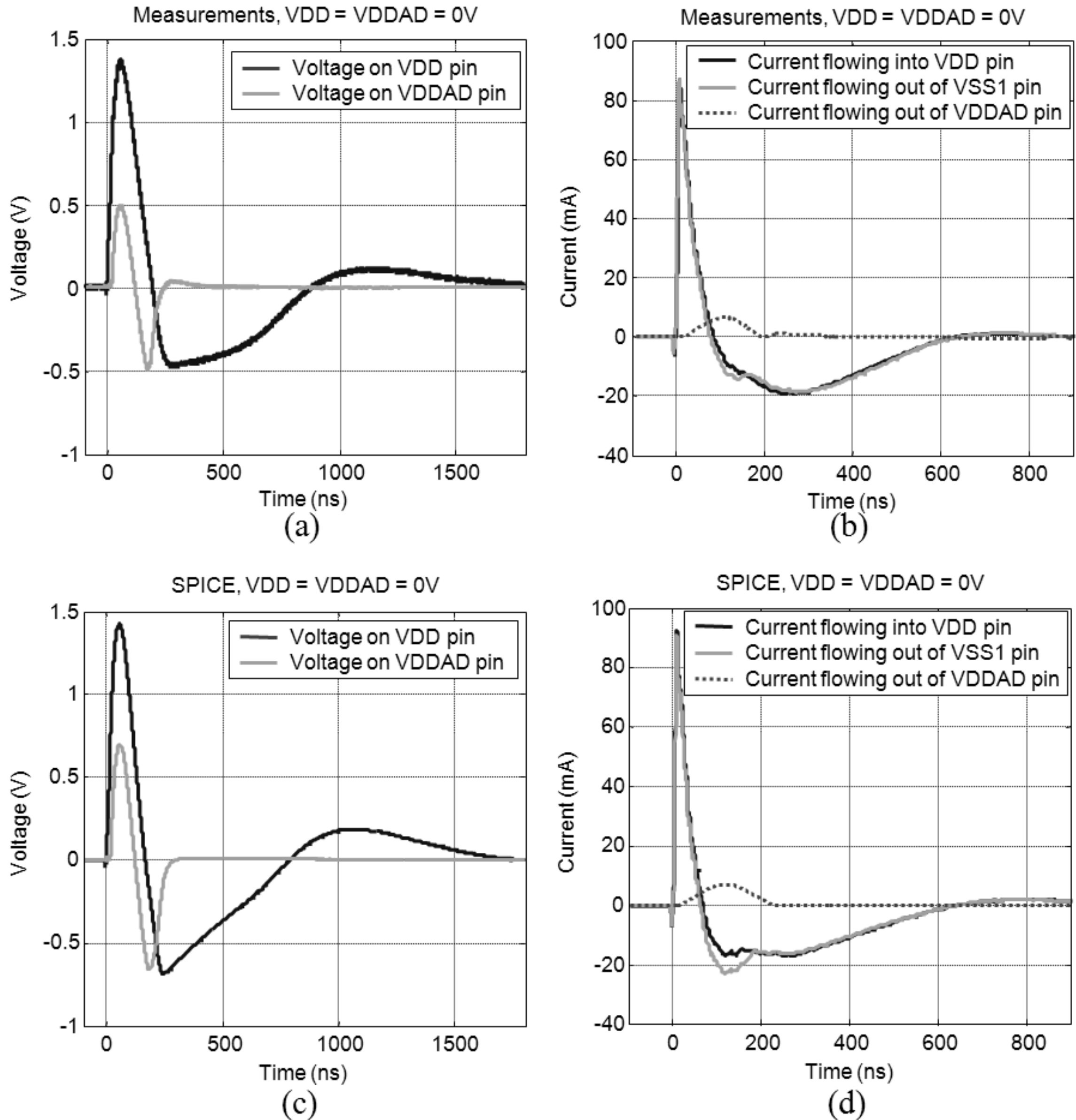

Fig. 26. Comparison of measured and SPICE simulation results for a capacitively-coupled EFT pulse (500 V with 40 dB attenuator) injected on the VDD pin with a supply voltage of 0 V.

V. Applications of the Model

A. Internal Current Estimation for low level disturbance

One advantage of modeling the power delivery network is that current inside the IC can be estimated during an EFT event, whereas such currents can not be easily measured. The ability of the model to accurately predict external voltages and currents

implies it might also be used to accurately predict internal voltages and currents as well. Fig. 27 shows the simulated values of currents inside the IC for the EFT events measured in Fig. 25 and Fig. 26. When the supply voltage was 5 V, the diodes between the power pins and ground pins were not turned on with this disturbance and the EFT current entering the VDD pin, I_{EFT}, was almost entirely routed through the internal capacitance between VDD and VSS pins, C_{i3}, as shown by the current I_{Ci3}. When the supply voltage was 0 V, however, the ESD protection diode between the VDD and VSS pins turned on and the EFT current flowed almost entirely through the protection diode from approximately t=230 nS to t=600 nS, as can be seen from the plot of I_{EFT} and $-I_{D3}$.

B. ESD power rail clamp evaluation for high level disturbance

The PDN model can also be used to evaluate the performance of an ESD power clamp during an EFT event. An ESD power clamp is designed to turn on and clamp the power rail to the return rail in the presence of a fast rising pulse [15]. The action of the clamp varies with the strength and duration of the pulse and with the power supply voltage. Many power clamps are designed to only be active when the power is off.

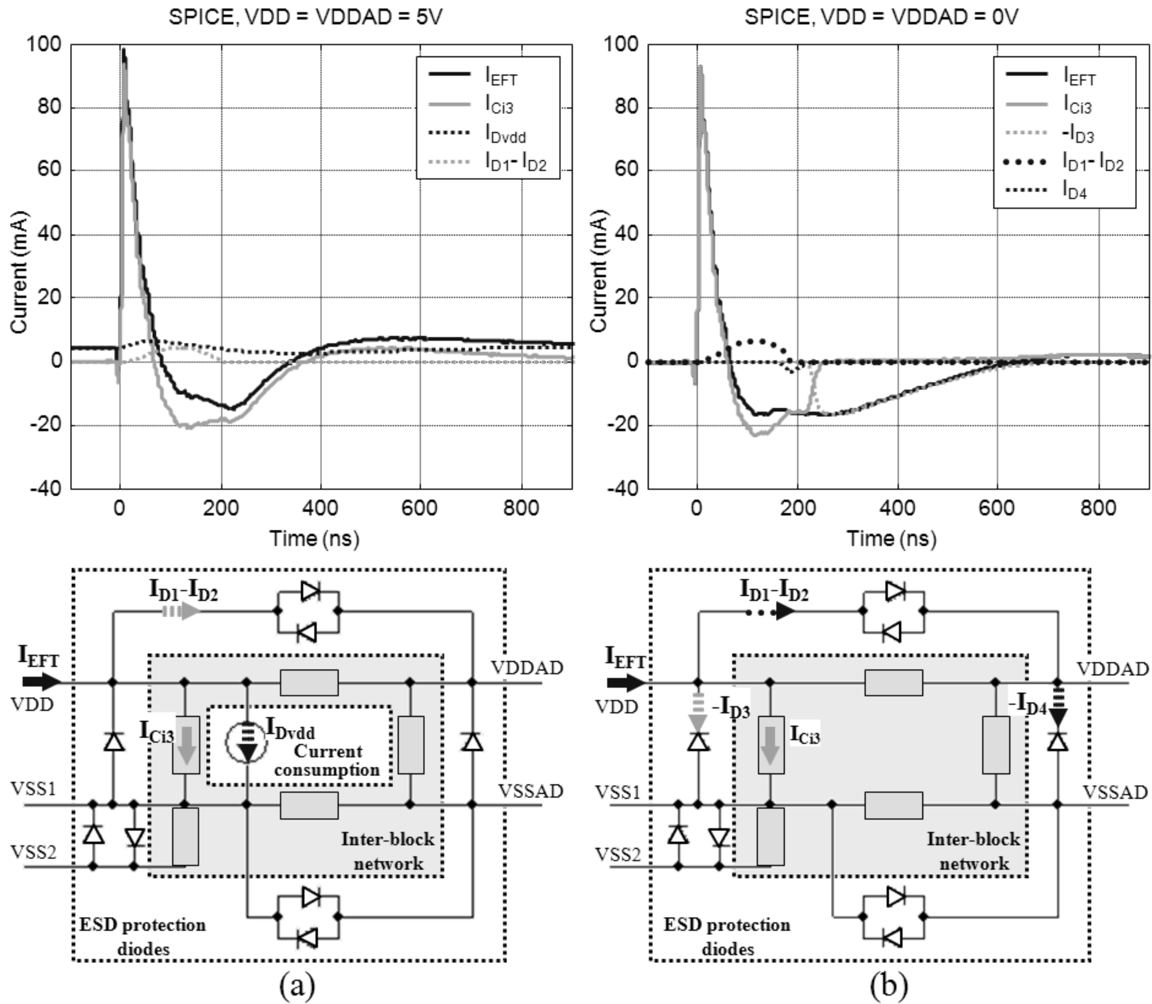

Fig. 27. Simulated currents inside the microcontroller during an EFT event (500 V with 40 dB attenuator) with a supply voltage of 5 V and0 V.

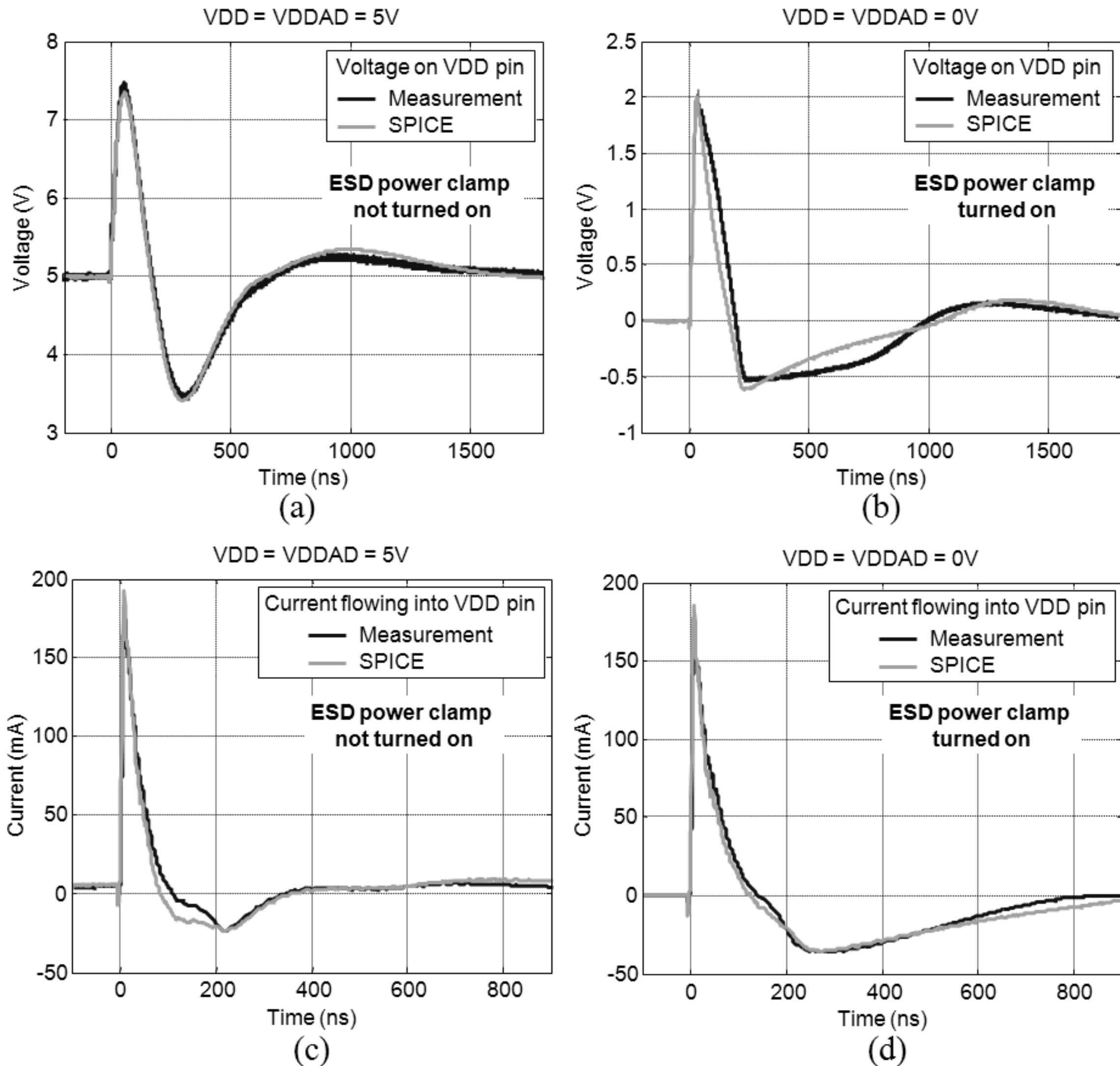

Fig. 28. Comparison of measured and SPICE simulation results for a capacitively-coupled EFT pulse (1 kV with 40 dB attenuator) injected on the VDD pin with a supply voltage of 5 V and 0 V.

To show the ability of the model to predict power clamp performance, measurements of pin currents and voltages were made during an EFT event that triggered the power clamp protection circuitry. Measurements were made with the setup shown in Fig. 24 when the EFT generator voltage was raised to 1 kV (i.e. the applied voltage through a 40 dB attenuator was raised to 10 V) in order to trigger the power clamp. SPICE simulation was performed using the non-linear PDN model combined together

with a SPICE model of the ESD power rail clamp obtained from the IC I/O designers. The SPICE simulation model predicted the measured pin currents and voltages well, as shown in Fig. 28.

Based on its ability to predict pin currents and voltages, the internal currents and voltages predicted by the model were also evaluated. The EFT current estimated to flow through the power clamp and through the other on-die circuitry is shown in Fig. 29. When the IC is powered on, most of the EFT current flows through the inter-block element between VDD and VSS1 and the power clamp is not turned on. When the IC is powered off, however, the EFT pulse turns the power clamp on and the EFT current is shunted to VSS through the clamp. Consequently the voltage on the VDD pin is clamped at 2 V at the rising edge of the EFT pulse. Fig. 29 further shows that if the ESD power rail clamp was removed the peak voltage on VDD would rise to as high as 2.8 V.

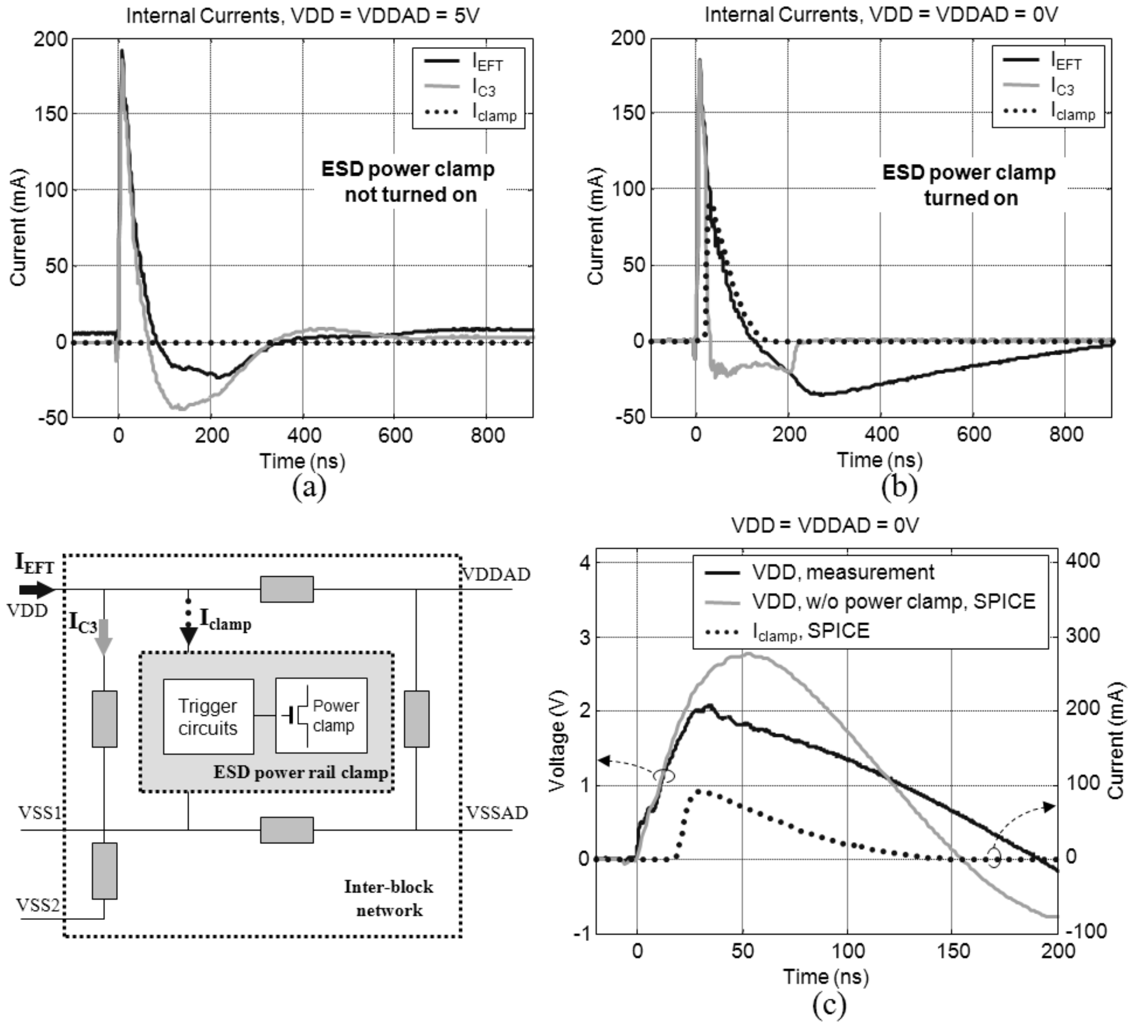

Fig. 29. Simulated currents inside the microcontroller during an EFT event (1 kV with 40 dB attenuator) injected on the VDD pin with a supply voltage of 5 V and 0 V. Simulated current with a supply voltage of 5 V is shown in plot (a). Simulated current and voltage with a supply voltage of 0 V is shown in plots (b) and (c).

VI. Conclusion

Evaluation of the immunity of ICs to electrical fast transients is important to many control applications involving inductive loads, but little research into modeling of ICs for this purpose has been done. Here, a non-linear model of the IC PDN was developed based on measurements of the IC. PDN impedances were characterized using 2-port S-parameter measurements. Internal diodes were characterized using a curve tracer.

Electrical connections between power rails (e.g. between VDD and VSS or VDD and VDDAD) were modeled using a pair of diodes and a simple RC circuit. ESD power clamps were modeled using schematics obtained from the IC manufacturer. This simple model was able to successfully predict the pin currents and voltages in response to fast transients applied to power pins. The accurate prediction of external voltages and currents suggests the model may also be used to predict voltages and currents inside the IC, though that contention could not be verified through measurement in this study. Prediction of the internal voltage and currents potentially allows the IC designer to go beyond predicting the immunity performance of their ICs in specific application by giving them the ability to understand the reason for failures and to evaluate potential solutions before they are implemented in silicon. Here we showed one potential application where the performance of the ESD power clamp was evaluated in the presence of EFTs. While power clamps are not typically evaluated for their reaction to EFTs, this evaluation may be critical in many applications where large EFTs may cause the clamp to trigger and reset the IC or worse. Such models might also be used to better understand inter-domain coupling during EFT events (e.g. from VDD to VDDAD), to better understand where physical failures might occur and why, and possibly to estimate substrate noise due to EFTs.

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