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Stability challenges and solutions in current-mode controlled power electronic converters

Seyed Mostafa Khazraei

Department: Electrical and Computer Engineering

STABILITY CHALLENGES AND SOLUTIONS IN CURRENT-MODE CONTROLLED POWER ELECTRONIC CONVERTERS

By

SEYED MOSTAFA KHAZRAEI

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Approved by:

Mehdi Ferdowsi, Advisor
Mariesa L. Crow
Keith A. Corzine
Jonathan W. Kimball
Mark W. Fitch

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ABSTRACT

This dissertation focuses on stability issues in single-staged and multi-staged current controlled power electronic converters. Most current-mode control (CMC) approaches suffer from sub-harmonic oscillations. An external ramp is usually added to solve this problem. However, to guarantee stability this ramp has to be designed for the worst possible case which consequently over damps the response. Adaptive slope compensation (ASC) methods are the solution for this problem. In paper 1 of this dissertation, first three ASC methods will be investigated and analyzed through their small signal models. Then, through simulation analyses and experimental test of a variable-input voltage converter the results will be validated. Two of the methods studies in the first paper are peak CMC methods and the last one is called the projected cross point control (PCPC) approach. This method is relatively new.. Therefore, a detailed discussion of the principles of operation of PCPC will be presented in paper 2. In addition, the small signal model of PCPC is developed and discussed through simulation and experimental analyses in the second paper of this dissertation. Peak, average, and hysteresis CMC schemes are used for comparison.

In paper 3, the stability issues which arise in multistage converters will be addressed. A solid state transformer (SST) as an example of a multistage converter will be studied. A comprehensive small signal modeling will be conducted which helps for stability analysis of SST. Time domain simulations in Computer Aided Design software (PSCAD) are presented which validates the frequency domain analysis.

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1. INTRODUCTION

1.1. OVERVIEW

Current-mode control (CMC) schemes have been widely used in switching power converter applications. Usually, CMC methods are divided into two main categories which are fixed-frequency methods and variable-frequency methods. CMC methods have several advantages over conventional voltage-mode control methods including improved transient response since they reduce the order of the converter to a first order system, improved line regulation, suitability for converters operating in parallel, and over-current protection [1]. Fixed frequency methods are more popular and include peak current-mode control (PCMC) [2-5], average current mode control (ACMC) [6-8], and charge control approaches.

Variable frequency methods such as hysteresis current-mode control (HCMC) or delta modulation are more popular in variable input or output voltage power converter applications. Both fixed frequency and variable frequency CMC methods have some disadvantages which make the system encounter some limitations in various applications. Sub-harmonic oscillation is the main disadvantage of fixed frequency methods especially in applications where the input or output voltage are variable such as (Power Factor Corrector) PFCs and inverters. In addition to sub-harmonic oscillation in CMC, there is usually a compromise between steady state current error and dynamic response which will be addressed here.

The stability challenges do not limit to individual converters. That is individual converter which have been designed carefully to be stable may show instability when they put together. This instability is due to the interaction of connected converters and is

common in multistage converters. In the next sections an introductory explanation of these challenges and possible solutions will be discussed.

1.2. STABILITY CHALLENGES

In this section an introductory explanation of stability challenges and possible solutions mentioned in section 1.1 will be discussed.

1.2.1. Stability Issue for An Individual Current Controlled Converter: Among fixed frequency methods, PCMC is one of the most common one. In order to generate the PWM gate signal in PCMC, the peak value of the inductor current is measured and compared with its reference. The PCMC method has several advantages including constant switching frequency, simplicity of implementation, and good dynamic response. However, the sub-harmonic oscillation issue affects their popularity adversely especially in applications where the input or output voltages are variable such as PFCs and inverters. On the other hand, HCMC as a variable-frequency approach enjoys stability for the entire range of operating points and hence is a good choice for variable input or output voltage application [9-13]. However, HCMC has to deal with the variable switching frequency problem.

The instability problem happens when D (duty cycle) is more than 0.5. Fig. 1.1 shows such circumstances. In this figure, the solid line is the steady state inductor current of a power converter with M_1 as the uprising slope and M_2 as the falling slope and dashed line is disturbed inductor current. As seen in this figure, when D>0.5 the initial disturbance is increased in the next switching cycle. This instability problem can be solved using slope compensation (M_a) as seen in Fig. 1.2. However, in applications with wide operating range the slope must be designed for the worst case scenario to

guarantee stability for the entire range of the operating point. For example, in PFC applications, the input voltage follows the |sin(ωt)| pattern. Hence, the worst possible instability scenario is when the input voltage nears zero which leads to *D* close to 1. A compensation designed for the worst case scenario has a large slope which adversely impacts the dynamic response and over damps the system [14, 15]. By over damping the system, there will be a considerable time interval where the inductor current is discontinuous which is undesirable and adversely affects the current total harmonic distortion.

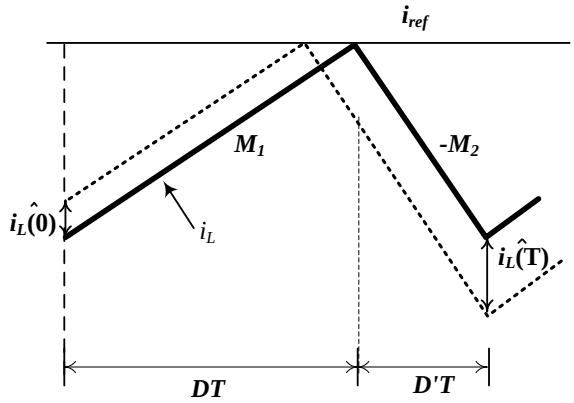

Fig. 1.1. Propagation of a perturbation in the programmed current.

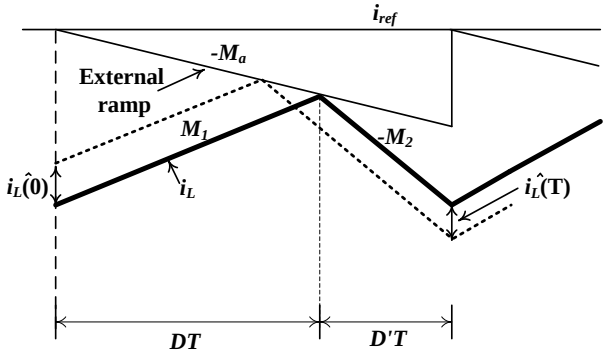

Fig. 1.2. Propagation of a perturbation under PCMC with slope compensation.

However, by using adaptive slope compensation (ASC) methods which use the instantaneous information of the system this problem can be solved. Using the basic

equation of PCMC, an ASC method is introduced in [16] which improves the dynamic response and stability of an inverter controlled under PCMC. In [17, 18] a similar slope compensation introduced for the buck converter with a wide operating range is introduced. However, none of these references present a comprehensive analysis and modeling of these methods which is necessary in power electronic converter modeling and design.

1.2.2. Steady State Current Error Vs. Dynamic Response For CMC: Along with PCMC, ACMC is one of the common fixed-frequency CMC methods. In the ACMC approach, the inductor current is first measured and fed into a compensation network to obtain its dc value. Then, the output of the compensator is compared with a saw-tooth ramp to generate the PWM gate signal [19]. In contrast to PCMC, ACMC has the ability to control the average of inductor current which means no peak-to-average current error and improvements in noise immunity. However, due to the presence of a low-pass filter in ACMC, this control method exhibits a slower dynamic response which limits this method usage in some applications. In fact this low pass filter is responsible for both the slow dynamic response and nearly zero steady-state error which means there is a compromise between fast dynamic (as in PCMC) and average current tracking capability (as in ACMC).

On the other hand, HCMC is the method which enjoys the advantage of both PCMC and ACMC methods. However, due to its variable frequency operation, HCMC is not suitable for any application that needs to synchronize the converter's switching frequency with some external clock. A possible CMC method which has the advantages

of PCMC, ACMC, and HCMC simultaneously while does not suffer from their limitations can be a very beneficial in CMC of power converters.

1.2.3. Stability Issue In Multistage Converters: Individual converters can works well if the control loop is designed carefully to be stable in all operating point. However, when stable individual converters are put together in cascaded form they might show instability. Actually, multistage converters are highly prone to instability due to the interaction of their stages. Hence, the control system must be designed in a way that it solves this detrimental interaction effect.

1.3. CONTRIBUTION TO DATE

Three papers have been written by the author of this dissertation to address the challenges discussed in section 1.2. Next the explanation of contributions in each paper will be presented.

1.3.1. Paper 1: Paper 1 is entitled As “Adaptive Slope Compensation Methods for Peak Current Mode Control of Power Converters”. As discussed in section 1.2.1 the ASC methods presented in [16-18] can solve the stability problem in PCMC. However, none of the existing works in the literature present a comprehensive analysis and modeling of these methods which will be done in paper 1 here.

Three ASC methods are discussed and analyzed in paper 1. The ASC method I is the one presented in [16] and ASC method II has been proposed in [17, 18]. ASC method III previously has been introduced by the author of this dissertation as a new CMC method called Projected Cross Point Control in [26-28] and again will be explained in more detail in paper 2 of this thesis. However, in paper 1, it will be shown that this CMC method can be seen as ASC method which is very useful in variable input or output

voltage applications. All the three proposed ASC methods in this paper have the advantage of being stable over the entire range of the operating point while benefit from fixed frequency performance. Consequently, they do not face the difficulties that HCMC usually faces due to its variable switching frequency. Simulation and experimental results are presented in paper 1 to confirm the validity of the proposed methods and models.

1.3.2. Paper 2: Paper 2 is entitled "Projected Cross Point Control – Modeling and Analysis". As argued in 1.2.2, an ideal CMC is a method which benefits the advantages of PCMC, ACMC and HCMC simultaneously while does not suffer from their limitations. The projected cross point control (PCPC) method is a recent fixed-frequency current-mode controller proposed by the author of this dissertation which combines the benefits of fixed- and variable-frequency schemes [26-28]. It can be considered as an optimal PCMC approach with adaptive slope compensation.

Similar to HCMC and unlike PCMC, PCPC is stable for the entire range of the duty cycle. In other words, perturbations introduced in the inductor's natural response will quickly damp down. The important advantage here is that the PCPC method has the same ability to be stable as HCMC, while it is a constant switching frequency controller similar to PCMC. In addition, it does not face the difficulties that HCMC usually faces due to its variable switching frequency.

Another important feature of this method is that in PCPC, similar to ACMC and HCMC, the average value of the inductor current is controlled; hence, there is no peak-to-average current error which is a common problem in PCMC. PCPC shows interesting characteristic in frequency domain such as high current loop gain and improved audio

susceptibility compared to PCMC and ACMC. Modeling, control and analysis of a converter under this control method will be presented in paper 2.

1.3.3. Paper 3: Paper 3 is entitled “Solid-state Transformer Stability and Control Considerations”. This paper discusses the stability issue that may arise in a solid state transformer (SST) because of its cascade structure. The SST is one of the key elements in implementing the Future Renewable Electric Energy Delivery and Management (FREEDM) System. The FREEDM system, namely Green Hub, is a large-scale micro-grid (MG) with greater reliance on distributed renewable energy resources (DRERs), distributed energy storage devices (DESDs) and power electronic (PE) based components as seen in Fig. 1.3. The SST actively manages DRERs, DESDs and loads [20-23].

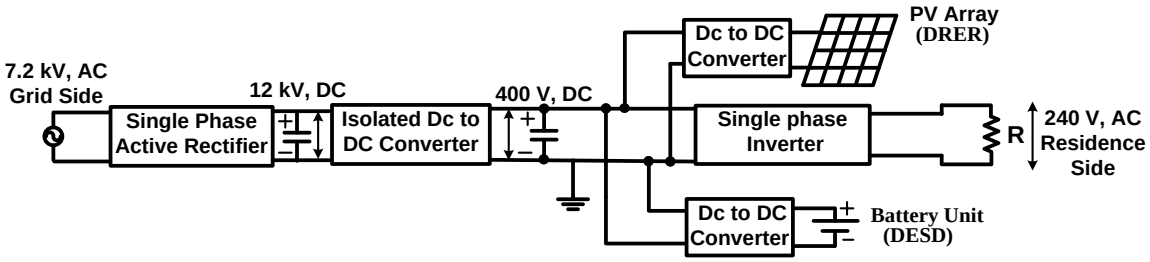

Fig. 1.3. SST diagram

The SST has been proposed as part of the FREEDM Green Hub system to substitute for the conventional distribution-level transformer. The SST includes three cascaded PE converters, including an AC/DC rectifier, a dual active bridge (DAB) converter, and a DC/AC inverter. Due to the bidirectional power flow capability of SSTs, DESDs and DRERs, such as storage units and Photovoltaics (PVs), can connect to the SST using DC/DC converter interfaces. This SST’s capability adds to the number of interacting converters. In general, multistage converters are highly prone to instability due to the interaction of their cascaded converters. In order to avoid instability, the interacting systems must meet the Middlebrook stability criteria [24]. In other words, the

impedance of the second-stage converter always must be higher than the output impedance of the first stage. This is a necessary condition to ensure stability.

The stability of the cascaded converters have been studied previously and reported in the literature. Stability analyses have been reported for cascaded DC/DC systems and distributed power systems based on DC/DC converters, AC/DC rectifiers and DC/AC inverters [25-29]. It has been shown how the independent stable systems may become unstable when combined.

On the other hand, the stability issue in multistage systems with bidirectional power flow capabilities has been rarely addressed in the literature. In [29], this issue has been studied for a system with an AC/DC rectifier connected to a DAB. However, the control used to regulate the cascaded system in [29] depends on the direction of power flow. Hence, for different power flow directions, a separate control system must be used. This means that different transfer functions and consequently different impedance models must be derived for each power flow direction. This issue makes the stability analysis more tedious, especially in the case of an SST with a DRER and a DESD in which different power flow scenarios can be defined. Moreover, switching to a different control algorithm when the direction of power changes is not a popular option in industry. In an SST, however, the same control system is used regardless of the power direction.

In paper 3, the control design and stability analysis do not depend on power flow. Hence, the derivation of small-signal modeling and transfer functions is independent of power flow, which makes the stability analysis much easier and more practical, especially in the case of SST with a DRER and a DESD in which different power flow scenarios can be defined.

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PAPER

1. ADAPTIVE SLOPE COMPENSATION METHODS FOR PEAK CURRENT MODE CONTROL OF POWER CONVERTERS

Mostafa Khazraei and Mehdi Ferdowsi

Missouri University of Science and Technology

Rolla, Missouri USA

Abstract— The peak current-mode control (PCMC) method, a fixed-frequency approach, is used widely for DC/DC conversion applications. However, in the current-mode control of power converters with a variable input or output voltage, variable-frequency methods, such as the hysteresis current-mode control (HCMC) method, are preferred. HCMC methods are considered superior to PCMC methods in part because the latter method faces instability issues for duty cycles more than 0.5. An external ramp can be added to solve this problem for the PCMC method. However, to guarantee stability, this ramp must be designed to handle the worst-case scenario, which consequently over-damps the response. Adaptive slope compensation (ASC) methods solve this problem. In these approaches, the slope of the external ramp changes based on the operating point of the system. In this paper, three ASC methods will be investigated and analyzed through their small signal models. Then, through simulation analyses and an experimental prototype of a variable-input voltage converter, here a power factor corrector circuit (PFC), the results will be validated.

Index Terms— adaptive slope compensation methods, current-mode control; power factor correction; projected cross point control

1.1. INTRODUCTION

Current-mode control (CMC) schemes have been used widely in switching power converter applications. Current mode control methods possess several advantages over conventional voltage-mode control methods, including improved transient response because they reduce the order of the converter to a first-order system, improved line regulation, suitability for converters operating in parallel, and over-current protection [1]. Usually, current-mode control methods are divided into two main categories, fixed-frequency methods and variable-frequency methods. Fixed-frequency methods are more popular and include peak current-mode control (PCMC) [2-5], average current mode control (ACMC) [6-8], and charge control approaches. PCMC [9-10] is one of the most common fixed-frequency methods.

However, the sub-harmonic oscillation issue adversely affects this method's popularity in applications in which the input or output voltage varies, such as PFCs and inverters. On the other hand, hysteresis current-mode control (HCMC) as a variable-frequency approach enjoys stability for the entire range of operating points and hence is a good choice for variable input or output voltage applications [11-15]. However, HCMC faces the variable switching frequency problem.

When slope compensation is used for PCMC, the slope must be designed for the worst-case scenario to guarantee stability across the entire range of the operating point. In PFC applications, the input voltage follows the $|\sin(\omega t)|$ pattern. Hence, the worst possible instability scenario is when the input voltage nears zero, which causes duty cycle (D) to approach 1. A compensation designed for the worst-case scenario has a large slope, which adversely impacts the dynamic response and over-damps the system [16,

17]. Over-damping the system leads to a considerable time interval during which the inductor current is discontinuous, which is undesirable and adversely affects the current total harmonic distortion.

However, this problem can be solved by using adaptive slope compensation (ASC) methods, which use instantaneous information from the system. Using the basic PCMC equation, an ASC method is introduced in [18] that improves the dynamic response and stability of an inverter controlled under PCMC. In [19, 20], a similar slope compensation introduced for the buck converter with a wide operating range is introduced. However, none of these references presents a comprehensive analysis and modelling of these methods, which will be done in this paper.

Here, three ASC methods are discussed and analyzed. ASC Method I is the one presented in [18], and ASC Method II has been proposed in [19, 20]. ASC Method III previously has been introduced by the author of this dissertation as Projected Cross Point Control in [14-16]. However, in this paper it will be shown that this current control method can be treated as an ASC method, which can be very useful in variable input or output voltage applications. All three proposed ASC methods in this paper have the advantage of being stable over the entire range of the operating point while benefitting from fixed-frequency performance. Consequently, they do not face the difficulties that HCMC usually faces due to its variable switching frequency.

ASC Method III contains an additional important feature in that the average value of the inductor current is controlled in a way similar to average current mode control and HCMC. Hence, there is no peak-to-average current error, which is a common problem in

PCMC. However, this method is more complicated compared to the first and second methods.

In Section 1.2, the current instability phenomenon and some basic equations are discussed. The first and second adaptive methods will be described in Sections 1.3 and 1.4, respectively. In Section 1.5, the third method will be explained, and finally, simulation and experimental results will be presented in Sections 1.6 and 1.7, respectively.

1.2. ADAPTIVE SLOPE COMPENSATION

In this section, some basic concepts will be reviewed to form a better understanding of ASC methods. Fig. 1.1 depicts the inductor waveform of a typical DC/DC power converter (buck, boost, etc.). Suppose the inductor current has a rising slope of M_1 and a falling slope of $-M_2$ in the steady state. Clearly, because the steady state waveform is periodic, one can write:

$$\frac{M_2}{M_1} = \frac{D}{D'} \tag{1}$$

where D is the duty ratio and D'=1-D. If a perturbation exists relative to the steady state (here defined as $\hat{i}_L(0)$) in the inductor current at the beginning of a period, the waveforms show that after one cycle, the error will have become

$$\hat{i}_L(T) = -\left(\frac{M_2}{M_1}\right)\hat{i}_L(0) = -\left(\frac{D}{D'}\right)\hat{i}_L(0). \tag{2}$$

Thus, after n cycles, the perturbation will be

$$\hat{i}_L(nT) = \left(-\frac{D}{D'}\right)^n \hat{i}_L(0). \tag{3}$$

Apparently, (3) is not a stable solution if the duty ratio is greater than 0.5.

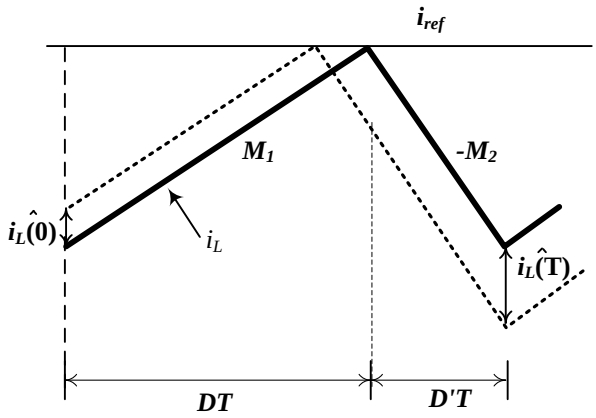

Fig. 1.1. Propagation of a perturbation in the programmed current.

This potential instability can be eliminated by adding a suitable cyclic artificial ramp to either the switch current waveform or the control signal. Waveforms for this modification are shown in Fig. 1.2, in which the control signal (i_{ref}) is added with a cyclic falling slope -M_a. Now, one can write:

$$\hat{i}_L(T) = -\frac{M_2 - M_a}{M_1 + M_a}\hat{i}_L(0) \tag{4}$$

And by defining

$$\alpha = \frac{\hat{i}_L(T)}{\hat{i}_L(0)}, \alpha = -\frac{M_2 - M_a}{M_1 + M_a} \tag{5}$$

After *n* cycles

$$\frac{\hat{i}_L(nT)}{\hat{i}_L(0)} = \alpha^n. \tag{6}$$

Considering (6), a perturbation is carried into the system with the rate of α. This rate can be set easily by selecting M_a, which is the ramp's slope.

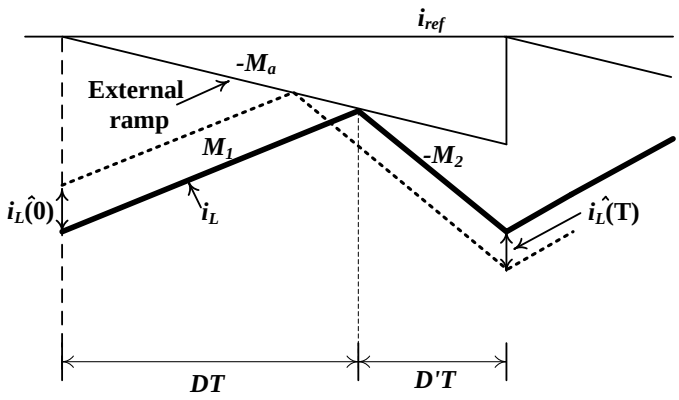

Fig. 1.2. Propagation of a perturbation under PCMC with slope compensation.

1.3. ASC METHOD I

A typical boost converter with parameters, as shown in Table 1.1, is assumed to explain ASC methods in this and future sections. This converter is very popular in PFC applications. To insure the current stability of such a converter, M_a in (5) must be chosen in order to make α less than one. A suitable choice for the ramp's slope, M_a in (5), can be:

$$M_a = M_2 / 2 \tag{7}$$

By substituting this choice into (5):

$$\left|\alpha\right| = \frac{D}{2-D} < 1 \quad for \quad 0 \le D < 1 \tag{8}$$

This is the least value of M_a that stabilizes the entire range of the duty cycle. Hence, for the PCMC control of the boost converter, one can choose M_a to be:

$$M_a = \frac{M_2}{2} = \frac{v_o - v_{in}}{L} \tag{9}$$

where v_o and v_{in} are instantaneous values of the output and input voltages of the converter. Because these two values change instantaneously, the resulting slope will be adaptive.

Table 1.1. Typical Boost Converter Parameters

Parameter	Value
Inductor	50 µH
C_{out}	400 µF
Pout	40 W
V_{in}	5-15 Volts
V_{out}	20 V
Frequency	100 kHz
R_{esr}	40 mΩ
R_L	30 mΩ
R_{sensor}	0.1 Ω
M_{a1}	400,000 (volts/H)
M_{a2}	40,000 (volts/H)

To understand how this choice improves the dynamic and stability of the system, one must obtain the small signal model of the system. Hence, this model under such a slope compensation will be presented. Fig. 1.3 shows the small signal block diagram of PCMC for a boost converter. In this block diagram, for the sake of simplicity, the gain of the current sensor is considered to be one. To model the effect of the input and output voltage perturbations on the duty cycle, feed-forward and feedback gains F_i and F_{vo} are introduced [6, 24] (see Fig. 1.3).

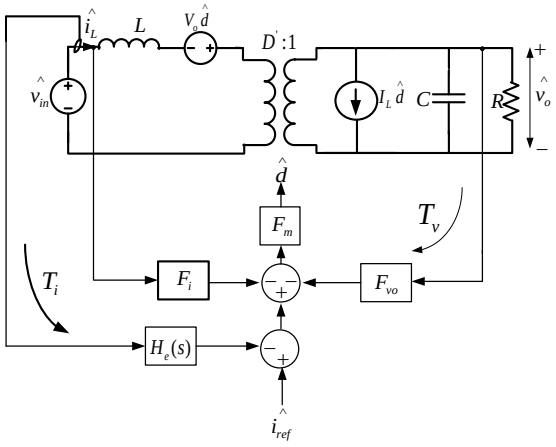

Fig. 1.3. Small signal block diagram of a boost converter under PCMC.

To obtain these feed-forward and feedback gains, the average value of the inductor current must be considered. For boost converter current loop gain, one can write:

$$< i_L >= i_{ref} - DT_s M_a - \frac{D' M_2 T_s}{2} \tag{10}$$

Where < > denotes the average value. By substitution from (9) and assuming v_{in} and i_{ref} are constant, this equation can be perturbed to obtain the dependence of the inductor current on the output voltage, which is defined as F_{vo}. To find F_{vo}, (10) is differentiated with respect to the output voltage, yielding:

$$\frac{< \hat{i}_L >}{\hat{v}_o} = \frac{-T_s}{2L} \tag{11}$$

And from the power stage depicted in Fig. 1.3, one can write:

$$(-F_{vo}\hat{v}_o - \hat{i}_L)F_m = \hat{d} \tag{12}$$

$$\hat{d}V_o - D'\hat{v}_o = 0 \tag{13}$$

The modulator gain is defined as [6, 24]:

$$F_m = \frac{1}{(M_1 + M_a)T} \tag{14}$$

which, by substituting from (9) in this application, leads to:

$$F_m = \frac{2L}{(v_{in} + v_o)T} \tag{15}$$

From (11), (12), (13), and (15), one can write:

$$F_{vo} = \frac{(D - D'^2)T}{2L} \tag{16}$$

F_i, the feed-forward gain, can be obtained using a similar approach. Table 1.2 presents the small signal parameters for basic power converters with ASC methods, which are discussed here.

Table 1.2. Small Signal Parameters of ASC Methods for Basic Converters

	F_m	F_i	F_{vo}
	ASC Method I		
Buck	$\frac{L}{T(v_{in}-v_o/2)}$	$\frac{TD}{L}(1-\frac{D}{2})$	$-\frac{T(1-D)}{2L}$
Boost	$\frac{2L}{(v_{in}+v_o)T}$	$\frac{TD'}{2L}$	$\frac{(D-D'^2)T}{2L}$
Buck-Boost	$\frac{L}{T(v_{in}-v_o/2)}$	$\frac{TD}{L}(1-\frac{D}{2})$	$\frac{T(D^2-3D+1)}{2L}$
ASC Method II			
Buck	$\frac{L}{v_{in}T}$	$\frac{TD}{L}(1-\frac{D}{2})$	$F_{vo}=\frac{T}{L}(D-\frac{1}{2})$
Boost	$\frac{L}{v_oT}$	$F_i=\frac{T}{L}(\frac{1}{2}-D)$	$F_{vo}=\frac{T}{L}(D-\frac{D^2}{2})$
Buck-Boost	$\frac{L}{T(v_{in}-v_o)}$	$F_i=\frac{T}{L}(D-\frac{D^2}{2})$	$\frac{T(\frac{D^2}{2}-2D+\frac{1}{2})}{L}$
ASC Method III			
Buck	$\frac{2L}{T(3v_{in}-v_o)}$	$\frac{TD(3-D)}{2L}$	$-\frac{T(3-D)}{2L}$
Boost	$\frac{2L}{T(v_{in}+2v_o)}$	$\frac{T(3-D)}{2L}$	$\frac{-TD'(3-D)}{2L}$
Buck-Boost	$\frac{2L}{T(3v_{in}-2v_o)}$	$\frac{TD(3-D)}{2L}$	$\frac{TD'(3-D)}{2L}$

The sampling effect of the inductor current must be considered in the small signal model as well. In [6, 24], the sample and hold effect is obtained as follows:

$$H_e(s)=1+\frac{s}{\omega_nQ}+\frac{s^2}{\omega_n^2} \text{ where } Q=\frac{-2}{\pi}, \omega_n=\frac{\pi}{T} \tag{17}$$

It is also shown that this sampling gain is invariant for all converters using constant frequency, constant on-time, or constant off-time. It always exhibits 180° of phase lag at half of the switching frequency. By considering this effect in the small signal model of PCMC, the instability of the current loop can be explained. This gain is considered in the small signal model here.

The current loop gain presents useful design information, including steady-state error and loop stability. Using the block diagram in Fig. 1.3, the analytical expression for the current loop gain is obtained as:

$$T_i(s) = \frac{H_e(s) F_m G_{i_L d}(s)}{1 + F_m F_{vo} G_{vd}(s)} \tag{18}$$

where

$$G_{vd} = \frac{V_o}{D'} \frac{(R_{esr} C s + 1).(1 - (L/(RD'^2)\, s)}{1 + (L/(R\,D'^2) + R_{esr} C) s + (LC(R_{esr}/R + 1)/D'^2) s^2} \tag{19}$$

and

$$G_{i_L d} = \frac{2V_o}{RD'^2} \frac{1 + (R/2 + R_{esr}) Cs}{1 + (R_{esr} C + L/(R\,D'^2)) s + (LC(R_{esr}/R + 1)/D'^2) s^2} \tag{20}$$

For ASC Method I, one can write:

$$T_i = \frac{4LH_e(s)}{RT_s D'} \bullet \frac{(1 + g_1 s)}{1 + g_2 s + g_3 s^2} \tag{21}$$

where

$$g_1 = (R/2 + R_{esr}) C$$

$$g_2 = \frac{(2D'^2 + 2D' - 1)L}{RD'^2} + R_{esr} C \tag{22}$$

$$g_3 = \frac{(D'^2 + D')LC}{D'^2} + \frac{(2D'^2 + 2D' - 1)LR_{esr} C}{RD'^2}$$

For a conventional PCMC, the loop gain can be obtained as [24]:

$$T_i = \frac{2LH_e(s)}{RT_s D'^3 (m_c - .5)} \bullet \frac{(1 + g_4 s)}{1 + g_5 s + g_6 s^2} \tag{23}$$

where

$$m_c = 1 + \frac{M_a}{M_1}$$

$$g_4 = (R/2 + R_{esr})C$$

$$g_5 = \frac{(m_c + .5)L}{(m_c - .5)D'^2 R} + R_{esr} C \tag{24}$$

$$g_6 = \frac{m_c LC}{(m_c - .5)D'^2} + \frac{(m_c + .5)LR_{esr}C}{(m_c - .5)D'^2 R}$$

where m_c is a parameter representing the compensation value with a constant slope.

To see the effect of ASC Method I on the dynamic of the current loop, the current loop gain equations in (21) and (23) are depicted for the mentioned boost converter with the parameter listed in Table 1.1. Note that the effect *of r*, which is the sum of the sensor resistor and the inductor series resistor *($r=R_{esr}+R_L$)*, has been considered in the computer plot but not considered in the math equations above for the sake of simplicity. For this Bode plot, the m_c is chosen to be a value that guarantees stability in the worst-case scenario, which is when the input voltage is near zero. In other words:

$$M_{a1} = \frac{v_{out\_operating} - v_{in\_\min}}{L} = 4 \times 10^5 (volts/H) \tag{25}$$

Fig. 1.4 shows the Bode plot of the current loop gain for equation (23) for three operating points with M_{a1}. Even with *D=0.75*, which relates to a low input voltage and is a critical case, the current loop gain is stable and has sufficient phase and gain margins. However, the crossover frequency for these cases is very low, which deteriorates the dynamic performance. To achieve a higher crossover frequency, the compensation slope can be decreased.

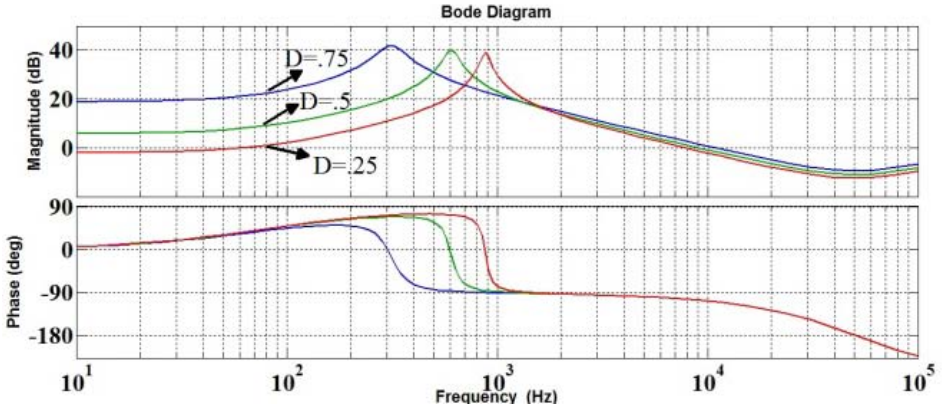

Fig. 1.4. Phase and Bode plot for various operating points with large constant slope (M_{a1}).

Fig. 1.5 shows the Bode plot of the current loop gain for equation (23) for three operating points with M_{a2} equal to 0.4×10^5(volts/H). As seen in this figure, the case in which *D=0.25* is stable with a good crossover frequency. The case in which *D=0.5* has a gain margin near zero and remains stable. However, for *D=0.75*, the gain margin is negative, which means the system is unstable.

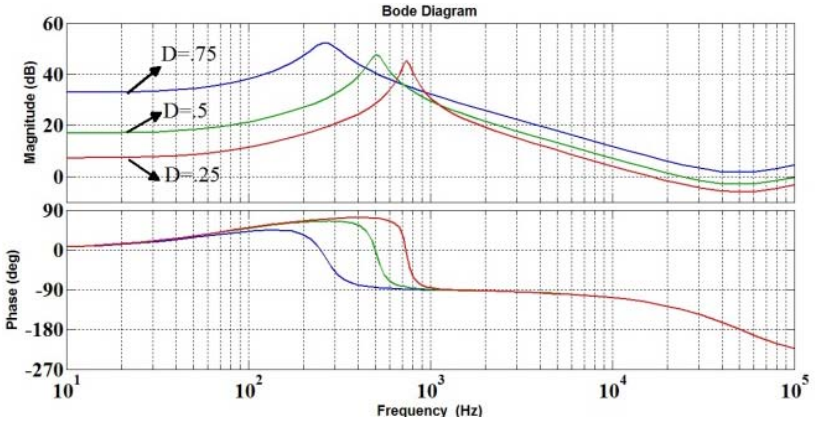

Fig. 1.5. Phase and Bode plot for various operating points with small constant slope (M_{a2}).

Comparing Figs. 1.4 and 1.5 shows that there is always a compromise between stability and speed. To achieve a faster dynamic, M_a must be decreased, which opens the

system to instability in low input voltages. This problem can be solved using ASC Method I. Fig. 1.6 shows the Bode plot for this case.

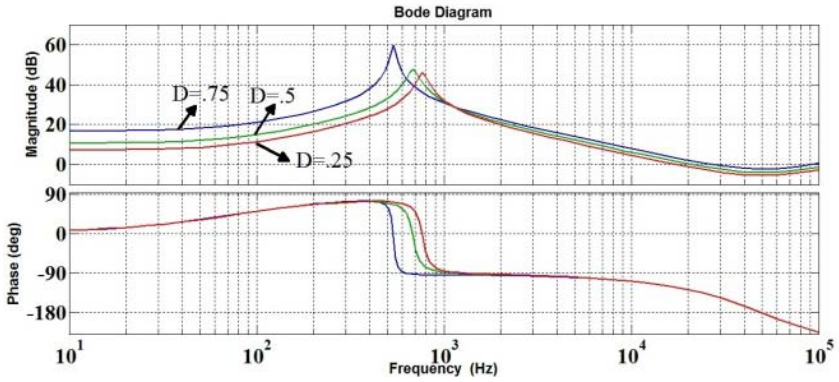

Fig. 1.6. Phase and Bode plot for various operating points with ASC Method I.

As seen in this figure, the plots for different values of *D* are closer to each other from the magnitude and phase aspects compared to Figs. 1.4 or 1.5. As mentioned previously, by using ASC Method I, the perturbation for the entire range of *D* will be cancelled, and the system will remain stable no matter what the operating point is. That is why the dependence of the plots in Fig. 1.6 on *D* is less than in Fig. 1.4 and 1.5, and, hence, the plots for different operating points are more similar to each other.

As seen in Fig. 1.6, even in the operating point with high values of *D*, the system remains stable while the crossover frequency is sufficiently high. Hence, a satisfactory compromise between speed and stability has been met for the operating point's full range. In fact, this compromise mostly advocates the fast dynamic rather than stability. This is clear by noting the small available positive gain margin. As the next section will present, ASC Method II can provide a compromise that advocates more for stability than fast dynamic.

1.4. ASC METHOD II

In ASC Method II, the slope compensation is defined as

$$M_a = M_2 \tag{26}$$

\whereas in the case of the boost converter, it is:

$$M_a = \frac{v_o - v_{in}}{L} \tag{27}$$

This choice makes the α in (5) equal to zero, meaning that all the perturbation will be damped in the first cycle for any value of the duty cycle. This property is called the dead-beat property. To obtain the small signal model of this method, the same procedure as for Method I is conducted. Consequently, the F_{vo} and F_m gains for this method will be:

$$F_m = \frac{L}{v_o T} \tag{28}$$

$$F_{vo} = \frac{T}{L}(D - \frac{D'^2}{2}) \tag{29}$$

All the small signal parameters for basic power converters are represented in Table 1.2. From (18), the loop gain will be:

$$T_i = \frac{4LH_e(s)}{RT_s D'(2 - D'^2)} \cdot \frac{(1 + g_7 s)}{1 + g_8 s + g_9 s^2} \tag{30}$$

where

$$\begin{aligned} g_7 &= (R/2 + R_{esr})C \\ g_8 &= \frac{(D'^2 + 4D' - 2)L}{(2 - D'^2)D'^2 R} + R_{esr} C \\ g_9 &= \frac{2LC}{D'(2 - D'^2)} + \frac{(D'^2 + 4D' - 2)LR_{esr}C}{(2 - D'^2)D'^2 R} \end{aligned} \tag{31}$$

Fig. 1.7 shows the Bode plot for three operating points for the loop gain of ASC Method II. At lower frequencies, the three plots from the magnitude and phase aspects

are closer to each other compared to the former plots. At higher frequencies, as demonstrated, the three plots are completely identical, which reveals the interesting feature of this method. Having an identical current loop eases the design of the voltage compensator. As seen in this figure, all three operating points have a good stability margin while their crossover frequencies lie somewhere between the frequencies given in Figs 1.4 and 1.6. In other words, this method offers a good compromise between stability and fast dynamic, with more emphasis on stability.

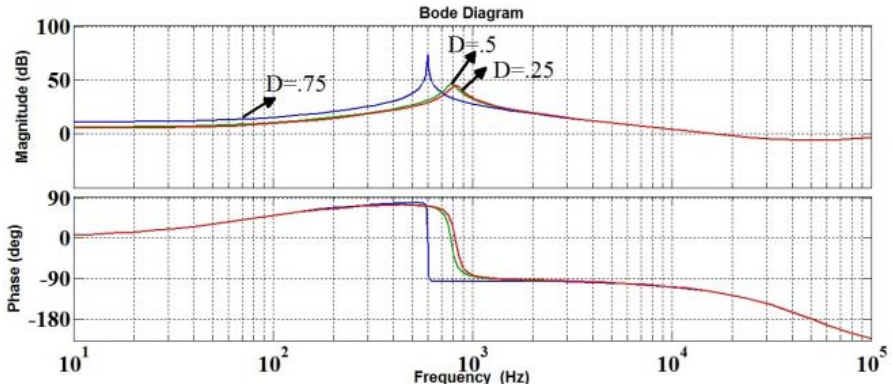

Fig. 1.7. Phase and Bode plot for various operating points with ASC Method II.

1.5. ASC METHOD III

A third adaptive slope method (ASC Method III) will be discussed here; it has been introduced by the authors in [21-23] as a new current mode control for DC/DC applications. This control method appears to be a very suitable ASC method for variable input or output voltage applications. This method is explained differently than ASC Methods I and II. To explain this method, a typical waveform of the inductor current for a power converter controlled under ASC Method III is shown in Fig. 1.8. In this figure, i_{ref} indicates the current reference. Similar to the ACMC technique, the control objective in this approach is to ensure that the average value of the inductor current follows the

current reference. To satisfy this objective, the final value of the inductor current must return to its steady-state value. In other words:

$$i_L(t = nT_s) = I_{fin,ss} = i_{ref} - \frac{\Delta I_L}{2} \tag{32}$$

where $I_{fin,ss}$ is the final value of the inductor current in the steady-state operation, ΔI_L is the steady state ripple of the inductor current, and n is the number of cycles.

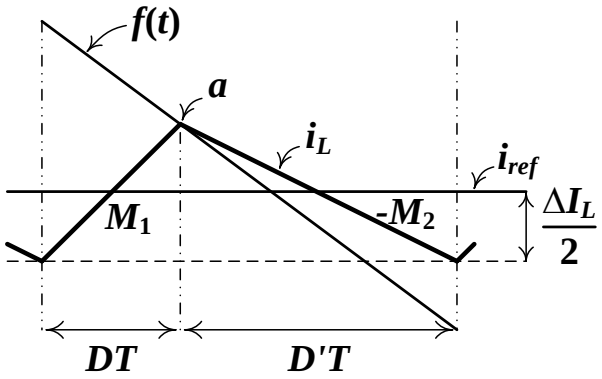

Fig. 1.8. Typical buck converter inductor current waveform with ASC Method III.

In order to satisfy the control objective, the cross point of lines i_L and i^- (the inductor current in the negative slope area) is needed. This point is marked as point '*a*' corresponding with t_{on} in Fig. 1.8. That is:

$$i_L(t = t_{on}) = i^-(t = t_{on}) \tag{33}$$

$$i^-(t) = i_{ref} - \frac{\Delta I_L}{2} - \frac{v_o - v_{in}}{L}t + \frac{v_o - v_{in}}{L}T \tag{34}$$

To solve (33), the ΔI_L value is needed, which is defined only in the steady state. However, the controller is supposed to work in transient and when there is a perturbation in the system. To solve this problem, the definition of (34) must be changed in order to include the effect of perturbations in circuit variables such as the input and output voltages.

This can be solved by substituting ΔI_L with Δi_L, which is the dynamic peak-to-peak ripple of the inductor current. For Δi_L, one can write:

$$\Delta i_L(t) = \frac{v_{in}}{L} t;\ nT_s < t < nT_s + DT_s \tag{35}$$

By applying this change to (34), a new equation can be introduced:

$$f(t) = i_{ref} + \frac{v_{in}}{2L} t_{on} - \frac{v_o}{L} t_{on} + \frac{v_o - v_{in}}{L} T \tag{36}$$

where $f(t)$ is the geometrical place of all the cross points of lines i_L and i^- for any initial inductor current value. Now, in order to find t_{on}, the cross point of lines i_L and $f(t)$ must be identified. Therefore,

$$i_L(t = t_{on}) = f(t = t_{on}) \tag{37}$$

$$i_L(t = t_{on}) = i_{ref} + \frac{v_{in}}{2L} t_{on} - \frac{v_o}{L} t_{on} + \frac{v_o - v_{in}}{L} T \tag{38}$$

In (37), t_{on} is the required ON time of the switch that guarantees the control objective. The control system solves (37) for t_{on} in real time. Why t_{on} is obtained by defining (36) and solving (37) should be investigated. It is clear that in the steady state, solving (33) and (34) produces the desired t_{on}. In fact, under steady-state conditions, substituting t with DT in (36) gives the same result as (34). Therefore, under steady-state conditions, the intersection of $f(t)$ and i_L is the same point as the intersection of i_L and i^-. Consequently, the control works under steady-state conditions.

Under transient conditions, suppose the inductor current is perturbed and increased by $\hat{\imath}_L(0)$, as seen in Fig. 1.9. All the other parameters on the right-hand side of (38) (v_{in}, v_o, and i_{ref}) are held constant. In Fig. 1.9, the perturbed inductor current is sketched in dashed lines. To guarantee stability, the final value of the inductor current must return to its steady-state value after a few periods no matter what the initial value of

the inductor current is. In Fig. 1.9, point *a*, the initial cross point of i_L and $f(t)$, is now moved to point *b* due to the disturbance. As predicted, ASC Method III decreases the duty ratio to deter instability in the inductor current. In other words, in (38), t_{on} must be decreased to stabilize the equation.

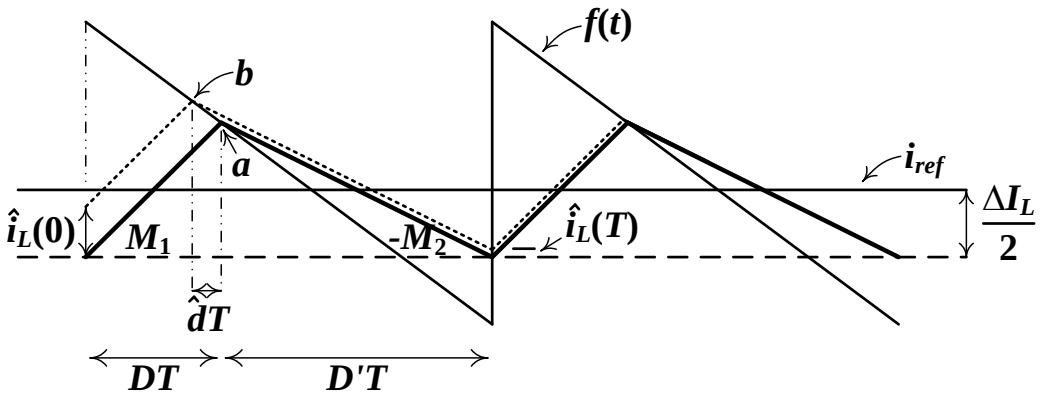

Fig. 1.9. Inductor current waveform of a buck converter controlled under the PCPC method when there is some initial disturbance.

According to Fig 1.9:

$$\hat{i}_L(0) = \left(\left| \frac{df(t)}{dt} \right| + M_1 \right) \hat{d} \tag{39}$$

$$\hat{i}_L(T) = \left(\left| \frac{df(t)}{dt} \right| - M_2 \right) \hat{d} \tag{40}$$

From (38), it is clear that

$$\left| \frac{df(t)}{dt} \right| = \frac{(\frac{v_{in}}{2} - v_o)}{L} \tag{41}$$

By combining (39), (40), and (41) and applying the steady-state relationships of a boost converter, one can write:

$$\frac{\hat{i}_L(T)}{\hat{i}_L(0)} = \frac{1-D}{3-D} \tag{42}$$

which can be expanded to the n^{th} periods as

$$\frac{\hat{i}_L(nT)}{\hat{i}_L(0)} = \left(\frac{1-D}{3-D}\right)^n \tag{43}$$

The right-hand side of (43) is always less than one; therefore, the stability for the entire range of the duty ratio is guaranteed. Clearly, the initial disturbance will be damped after just a few cycles, showing how well this approach works in transients.

Similar to (38), the control equations for buck and buck-boost converters, respectively, can be derived as:

$$i_L(t = t_{on}) = i_{ref} - \frac{v_{in} + v_o}{2L} t_{on} + \frac{v_o}{L} T \tag{44}$$

$$i_L(t = t_{on}) = i_{ref} - \frac{v_{in}}{2L} t_{on} + v_o t_{on} - \frac{v_o}{L} T \tag{45}$$

Fig. 1.10 shows the block diagram for the hardware implementation of the boost converter under this method. This block has been implemented based on (38). Equations (44) and (45) can be used to implement the control block for the buck and buck-boost topologies, respectively.

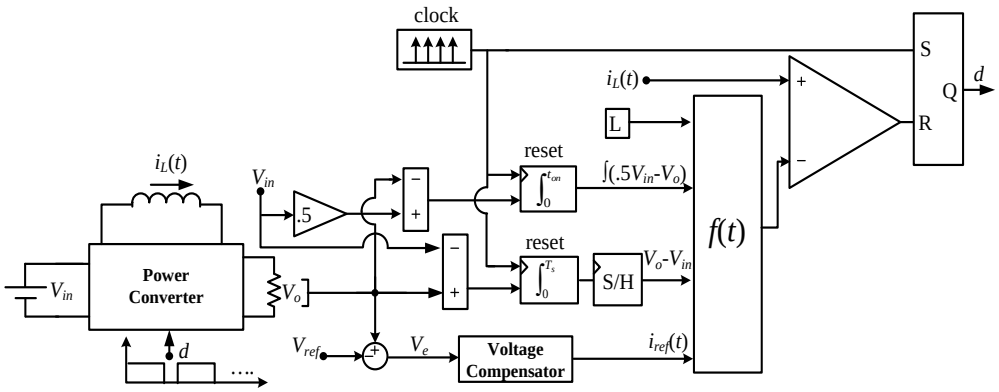

Fig. 1.10. Block diagram boost converter implementation for PCPC method.

This method can be assumed as an adaptive slope PCMC. In PCMC, the control equation is as follows:

$$i_L(t = t_{on}) = i_{ref} - S_e(t) \tag{46}$$

where $S_e(t)$ is the external ramp function with a slope equal to

$$\frac{\partial S_e(t)}{\partial t} = M_a \tag{47}$$

Comparing (38) with (46), one can conclude that the second and third expressions on the right-hand side of (38) resemble the external ramp in PCMC. This means that (38) presents the PCMC control rule as in (46) for a boost converter with:

$$S_e(t) = -\frac{v_{in}}{2L}t_{on} + \frac{v_o}{L}t_{on} - \frac{v_o - v_{in}}{L}T \tag{48}$$

where

$$\frac{\partial S_e(t)}{\partial t} = M_a = \frac{v_{in} - 2v_o}{2L} \tag{49}$$

Substituting M_a in (5) gives

$$\left|\alpha\right| = \frac{1-D}{3-D} < 1 \quad for \quad 0 \le D < 1 \tag{50}$$

which is the same result as in (42) and shows the stability of the current loop for the entire range of the duty cycle under this method.

The process of identifying the small signal parameters begins with the modulator gain F_m. Considering Fig. 1.8 for ASC Method III, one can write:

$$F_m = \frac{1}{(\frac{df(t)}{dt} - M_1)T} = \frac{L}{T(v_{in}/2 + v_o)} \tag{51}$$

For ASC Method III, under steady-state conditions, one can write:

$$< i_L > = i_{ref} \tag{52}$$

where $< i_L >$ denotes the average value of the inductor current. Assuming v_o and i_{ref} are constant, this equation can be altered to obtain the dependence of the inductor current on the input voltage. The steady-state, small-signal dependence of the average inductor current on the input voltage can be found by differentiating (52) with respect to the input

voltage, which yields:

$$\frac{<\hat{i}_L>}{\hat{v}_{in}} = 0 \tag{53}$$

Using equations (12), (13), and (53), F_{vo} can be obtained using an approach similar to that used in Method I:

$$F_{vo} = \frac{-TD'(3-D)}{2L} \tag{54}$$

Other small signal parameters for basic converters in ASCM Method III are reported in Table 1.2. For the loop gain from (18), one can write:

$$T_i(s) = \frac{2H_e(s)}{T(3-D)s} \tag{55}$$

Fig. 1.11 shows the simulation magnitude and phase plots of the loop gain for three different operating points in ASC Method III. Similar to ASC Methods I and II, it is clear that ASC Method III is consistently stable. Using (52) and considering Fig. 1.11, the crossover frequency for the entire range of D in ASC Method III can be expressed as:

$$f_s/3\pi \le f_c \le f_s/2\pi \tag{56}$$

From (55), it can be seen that the maximum crossover frequency in ASC Method III is less than half the switching frequency. Therefore, according to the Nyquist sampling theorem, the system is always stable. On the other hand, the crossover frequency is always more than a specific high value, which guarantees a high speed for the closed-loop system.

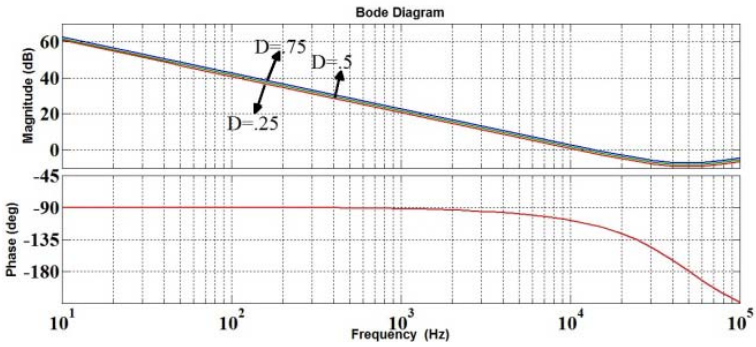

Fig. 1.11. Phase and Bode plot for various operating points with ASC Method III.

However, in a practical circuit, (55) is not an acceptable predicted model for low frequencies due to the effect of *r*. In contrast to R_{esr}, which sometimes can affect the higher-frequency characteristics significantly and can consequently influence stability, *r* does not produce a considerable effect. However, it changes the place of the existing pole and zeros in the system, as seen in this situation. Ideally, the loop gain of ASC Method III will have a pole at zero frequency; practically, the effect of *r* is that this pole moves to *r/L*. Instead of (55), then, one can write:

$$T_i(s) = \frac{2LH_e(s)}{Tr(3-D)((L/r)s+1)} \tag{57}$$

Equation (57) can be obtained easily by substituting the modified G_{vd} and G_{id} with consideration of the effect of *r* in (18, 19, 20). For the sake of simplicity, the effect of this *r* was ignored in ASC Methods I and II because changes in the pole's position caused by *r* for these two cases do not change the format of Bode plots. The modified predicted model has been plotted in Fig. 1.12. As seen, the crossover frequency and phase characteristics remain the same as in Fig. 1.11. However, the low-frequency characteristic is completely different, which does not significantly affect the dynamics compared to the ideal case in which there is no *r*.

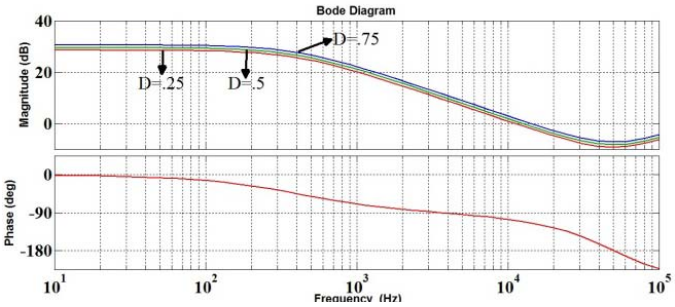

Fig. 1.12. Phase and Bode plot for various operating points with ASC Method III considering *r* effect.

Table 1.3 show the frequency characteristic comparisons for all five reviewed cases including PCMC with M_{a1}, M_{a2}, ASC Method I, ASC Method II and ASC Method III. As seen, the most stable loop belongs to PCPC and M_{a1} cases with highest possible phase margin. However, PCPC have higher cross over frequency compared to M_{a1} case. ASC Method I and M_{a2} cases have highest crossover frequencies. However, M_{a2} encounters instability. As seen, by increase of duty cycle the phase margin decreases (less stability margin) which is compatible with PCMC theory.

Table 1.3. Frequency Characteristic Comparisons for Discussed Methods

	D	f_c (kHz)	PM°
M_{a1}	.25	7.88	75.8
	.5	9.13	73.5
	.75	11	70
M_{a2}	.25	16.4	60
	.5	24.4	44.9
	.75	unstable	
ASC Method I	.25	17.5	57.9
	.5	21.2	50.9
	.75	27.3	39.1
ASC Method II	.25	16.5	60
	.5	16.5	60
	.75	16.5	60
ASC Method III	.25	11.2	72
	.5	12.5	69
	.75	14.2	66

Clearly, comparing the value of α for the three methods under consideration must confirm the information resulting from the current's loop plot comparison. The loop gain's dependency on D for ASC Method III in (50) is less than that in (8) for ASC Method I, which means that the loop gains must be more similar to each other for different operating points in ASC Method III, as is demonstrated here. Moreover, α damps faster in (50) than in (8), which means that ASC Method III has a greater stability margin than ASC Method I. Remember that in ASC Method II, α is zero for all operating points, which means that ASC Method II is superior to the other two ASC methods from the stability margin perspective. In the next section, the ASC methods discussed in this paper will be applied for an input variable voltage application to demonstrate their effectiveness.

1.6. POWER FACTOR CORRECTION APPLICATION

A variety of circuit topologies is available for PFC applications [25], most of which can be categorized into two groups, continuous-mode boost converters and discontinuous-mode boost and Flyback topologies. The control strategy in the first group often is based on current mode control techniques, while in the second group, the control strategy usually is based on voltage-mode control methods. Usually, both continuous-mode and discontinuous-mode methods can be used to control PFC circuits with boost converters. To implement a PFC using these two modes, the multiplier approach and the voltage follower approach are used, respectively.

The multiplier approach operates the boost converter while its input inductor current is continuous and the current ripple is small compared with the line current [25]. The input inductor current is constantly measured and controlled to track a sinusoidal

reference signal. This sinusoidal reference is proportional to the multiplication of the rectified ac line voltage and the output voltage error signal. In this section, a typical PFC circuit using the multiplier approach based on ASC Methods I, II, and III will be implemented, and the simulation results will be compared. Experimental implementation will be presented in the next section.

The implementation of such a PFC under ASC Methods I and II is straightforward. In addition to a conventional PCMC control system, the only necessary components are an integrator, sensed input voltage, the output voltage and the inductor value. ASC Method III requires one additional integrator and one sample and hold module, which makes the implementation more costly compared to the other two methods. For more clarity, the diagram of such a PFC under ASC Method III is shown in Fig. 1.13. The PFC parameters have been tabulated in Table 1.4. To study the current loop performance of the PFC controlled under the three ASC methods, the voltage loop is removed, and i_{ref} is commanded directly.

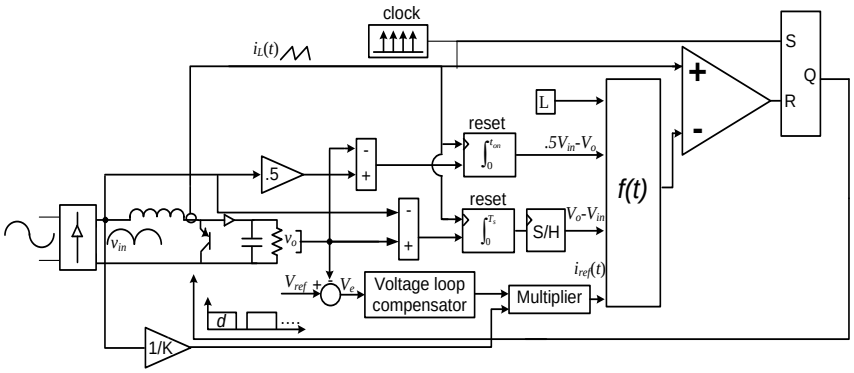

Fig. 1.13. Block diagram of PFC under ASC Method III.

Table 1.4. Typical PFC Boost Converter Parameters

Parameter	Value
Inductor	*500 μH*
C_{out}	*2,000 μF*
P_{out}	*100 W to 200 W*
V_{in}	*30-50 Rms*
V_{out}	*100 V*
Frequency	*50 kHz*
R_{esr}	*40 mΩ*
R_L	*30 mΩ*
R_{sensor}	*0.1 Ω*
M_{a1}	*50,000(volts/H)*
M_{a2}	*200,000(volts/H)*

For the sake of comparison, the PCMC with two different constant slope compensation values are considered here. First

$$M_{a1} = \frac{v_o - v_{in}(\min)}{4L} = 50000(Volts / H) \tag{58}$$

which is the undercompensated case and

$$M_{a2} = \frac{v_o - v_{in}(\min)}{L} = 200000(Volts / H) \tag{59}$$

that is the minimum value of the slope that guarantees stability for the entire range of the duty cycle. For clarity, a new notation has been defined for some of the figures related to ASC Methods I and II. The commanded i_{ref} is added to the compensation ramp, and the result of this summation is the actual current command written as I_{REF}. In all of the tests in this section, the rms of the input voltage and i_{ref} are set to 35 volts and 10.8 amperes, respectively.

Fig. 1.14 shows the inductor current and scaled input voltage (×.05) waveforms of PFC for PCMC with M_{a1} (top picture) and ASC Method I (bottom picture). As depicted, the discontinuous region of the inductor current is greater in ASC Method I than in

PCMC with M_{a1}, which is undesirable. However, the inductor current encounters sub-harmonic oscillation in the top figure. Fig. 1.15 shows the enlarged format of the former picture, which clearly depicts the sub-harmonic instability for PCMC with M_{a1}; this demonstrates the effectiveness of ASC Method I.

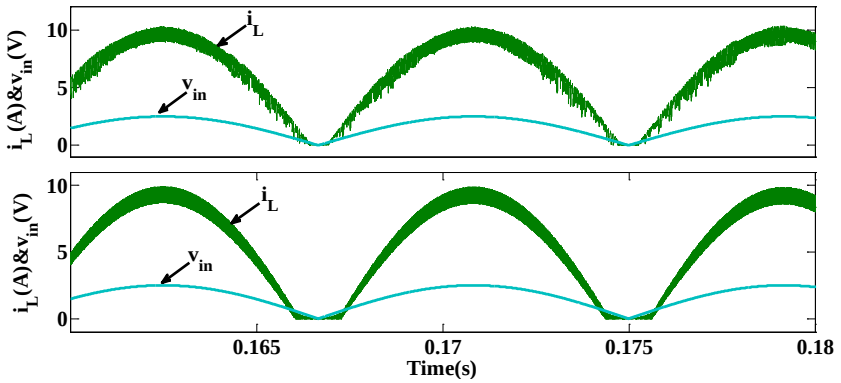

Fig. 1.14. PFC current and voltage waveforms with M_{a1} for PCMC (top) and ASC Method I (bottom).

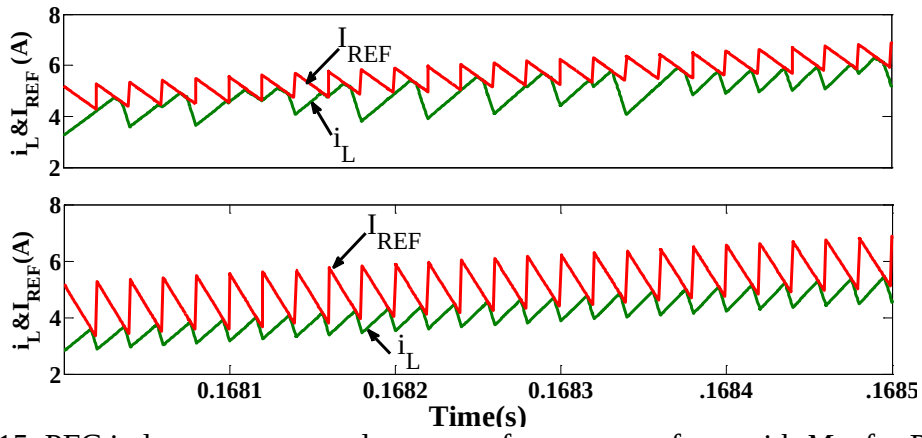

Fig. 1.15. PFC inductor current and current reference waveform with M_{a1} for PCMC (top) and ASC Method I (bottom).

Using PCMC with M_{a2} for PFC as seen in Fig. 1.16 (top trace), the discontinuous region is considerable. The application of ASC Method II in Fig. 1.16 (bottom trace) presents a high stability margin over the entire duty cycle range while also presenting nearly the same discontinuous region but with a faster dynamic, as will be seen in next figure. Fig 1.17 compares the dynamic response of these two cases when i_{ref} is doubled at

t=.095. The inductor current in ASC Method II settles faster than in PCMC with M_{a2} in Fig. 1.17 (top trace).

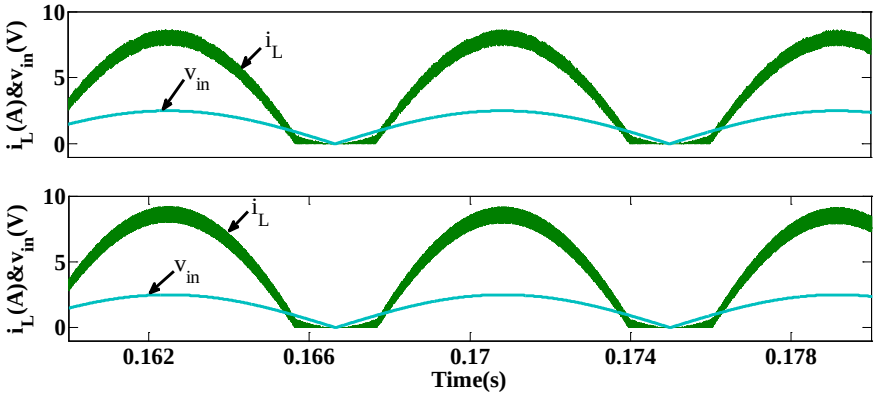

Fig. 1.16. PFC current and voltage waveforms with M_{a2} for PCMC (top) and ASC Method II (bottom).

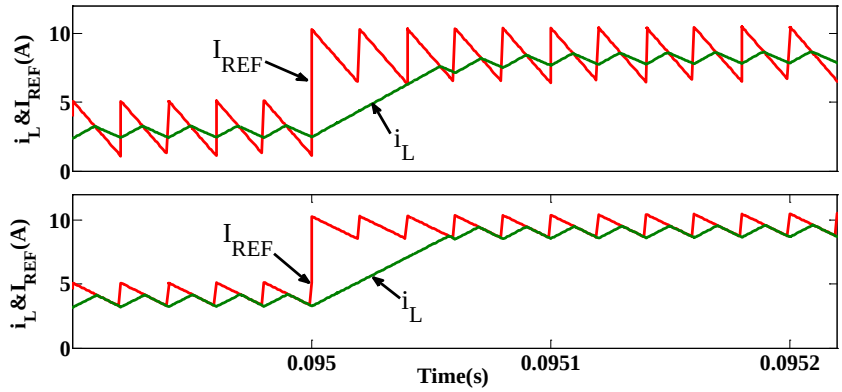

Fig. 1.17. PFC inductor current and current command waveforms for a step change in current command with Ma2 for PCMC (top) and ASC Method II (bottom).

Fig. 1.18 shows the inductor current, scaled input voltage (×.05) waveforms, current reference, and *f(t)* function for ASC Method III. As mentioned previously regarding this method, the average current tracks the current reference i_{ref}, which is why there is not a considerable discontinuous region. However, as the experimental results will reveal, the current waveform cannot be regulated so near to a zero input voltage in the lab because of limitations regarding experimental implementation.

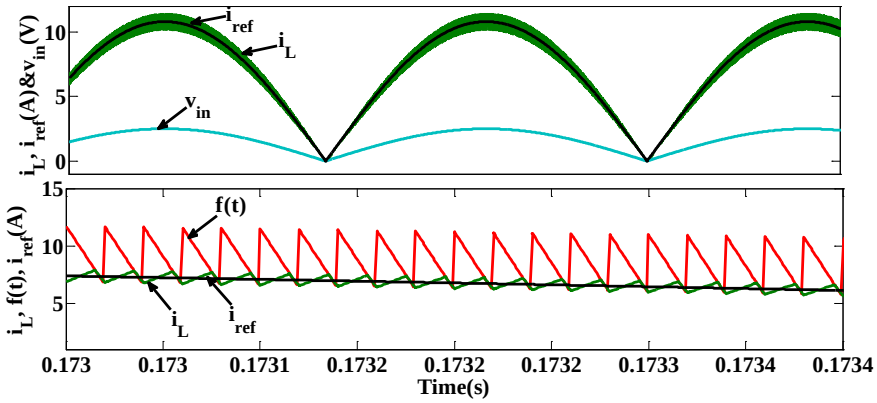

Fig. 1.18. PFC current and voltage waveforms with ASC Method III (top) and enlarged inductor current, current reference and *f(t)* waveform (bottom).

1.7. EXPERIMENTAL RESULTS

In this section, two experimental tests will be conducted. First, the small signal analysis that was performed in the previous sections through equations and simulation will be validated experimentally. Secondly, a circuit for PFC application matching the one in the previous section will be implemented. The small signal analysis that was conducted in the previous sections was for a DC/DC boost converter. However, here, as a variable input voltage application, an ac-dc PFC will be discussed. How the small signal analysis resulting from a DC/DC boost converter can be expanded to an ac-dc PFC application must be investigated. How the small signal evaluation of a boost converter for different operating points can be developed for a PFC analysis will be explained.

Two points must be considered. First, for a PFC, the line voltage, which is the input voltage of the boost converter, varies. Hence, the power stage transfer functions can be determined using quasi-static analysis [17]. In this analysis, the line and output voltages are considered constant within each switching cycle. The second point is related to the effect of the varying slope of the current reference on the modulator gain. When

the switching frequency is high, this effect is negligible. For the sake of simplicity and due to the fact that the switching frequency is usually much higher than the input line frequency, this effect can be ignored for the small signal analysis. Considering these two assumptions, the results of the small signal analysis of the boost converter for a wide range of the duty cycle can be expanded easily to a PFC application.

A boost converter with the same parameters shown in Table 1.1 was implemented in the lab for the small signal analysis test. The conventional analog injection technique is used here to measure the loop gain, as opposed to the digital modulator used in [24]. Because the analog modulation technique injects and measures the analog signal, its use is limited to the case for which the waveform at the disturbance injection point is smooth and well behaved. When in a switching regulator system, the waveform at the injection point is of a discontinuous nature and is pulse-width modulated, so an analog disturbance signal cannot be injected into the digital signal for loop gain measurement [26, 27]. Hence, because the inductor current, which is the sensed current here, does not pulsate, the conventional analog injection technique can be used to measure the loop gain. Analog signal injection works for a wide range of frequencies, up to nearly half the switching frequency. Because this range sufficiently describes the PCPC characteristics, the analog injection method is used here. Moreover, the analog injection method is much easier to implement compared to the digital injection method.

Figs 1.19, 1.20, and 1.21 represent the experimental validations of Figs. 1.6, 1.7 and 1.12, respectively. The simulation and experimental results have been plotted separately for the sake of easier plot recognition. Experimental measurements have been carried out up to 20 kHz. Measurements have not been conducted for higher frequencies

for several reasons. First, the predicted model is based on assumptions that are valid in ranges several times lower than the switching period. Second, the measured data in higher frequencies are erroneous due to noise. Moreover, measurements of frequencies up to 20 kHz, as conducted here, are sufficient to support the concept of this paper.

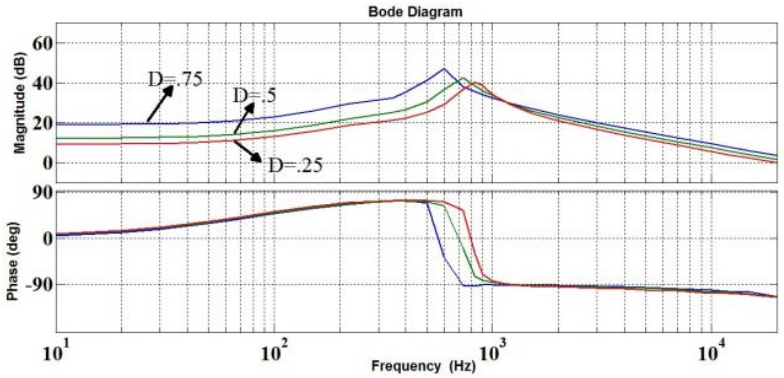

Fig. 1.19. Phase and Bode plot for various operating points with ASC Method I.

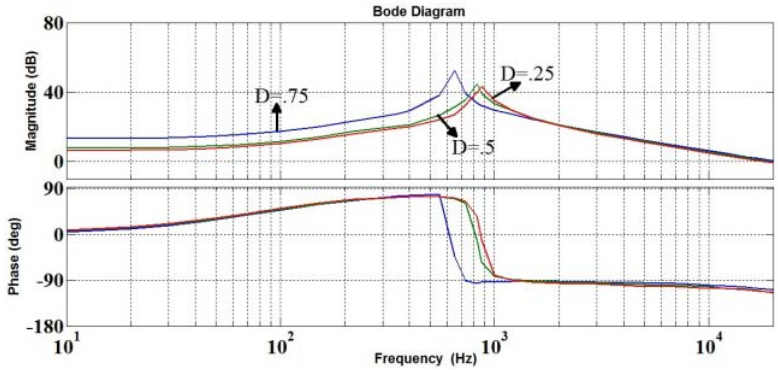

Fig. 1.20. Phase and Bode plot for various operating points with ASC Method II.

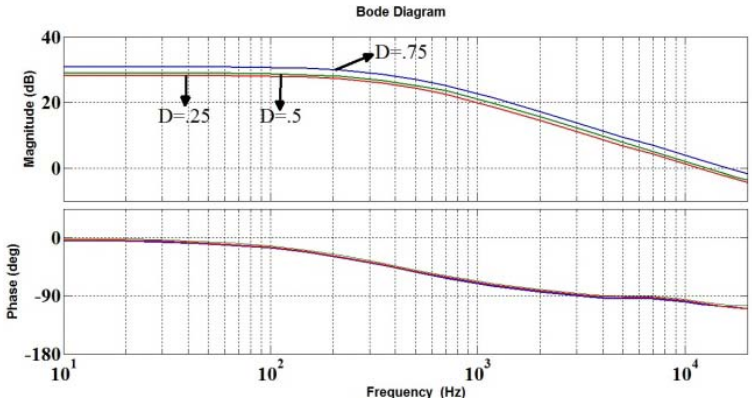

Fig. 1.21. Phase and Bode plot for various operating point with ASC Method III.

By comparing Figs. 1.6 and 1.19, 1.7 and 1.20, and 1.12 and 1.21, it can be seen that with only a few exceptions, the experimental results and the simulation results have nearly the same magnitude and phase, with a maximum discrepancy of 2 db for magnitude and 5 degrees for phase. The exceptions are related to the resonant frequency (only for ASC Methods I and II) and the phase plots for frequencies above 10 kHz. As seen in Figs. 1.6 and 1.7, the magnitude plot has a very high peak, which represents a system with a high quality factor. However, because of non-idealities, damping or resistive effect, and even measurement accuracies for very high magnitudes (over 40 db) in the experimental implementation, the simulation and experimental results do not match exactly.

The second exception is related to the value of the resonance frequency. In the boost converter, in contrast to the buck converter, this value depends on the duty cycle. Variations of a few percent in D between the simulation and the experimental test due to losses in the circuit create up to 50 Hz error in the resonant frequency. The third exception is related to phase measurement for over 10 kHz frequencies. This discrepancy is affected by the sampling effect of current mode controllers. The $H_e(s)$ function used in the predicted model and simulated here represents the sampling effect of current mode controllers and could be depicted better if the sampled digital injection technique were used to measure the sampled version of the loop gain. Other models for this frequency range presented in [27] differ from the sampled model.

In the second experimental lab test, which also is used to validate the simulation results obtained in Section 1.6, a PFC circuit is implemented with the same parameters as in Table 1.4. In all of the tests, the rms value of the input voltage and i_{ref} are set to 35

volts and 5.2 amperes, respectively. Fig. 1.22 shows the inductor current waveform along with the input voltage for the PFC with M_{a1} (see Table 1.4) for PCMC. As predicted, the region with low input voltage values experiences some instability in current because of under compensation, as seen in the enlarged portion of Fig. 1.22. Note that I_{REF} has the same definition as in Section 1.6.

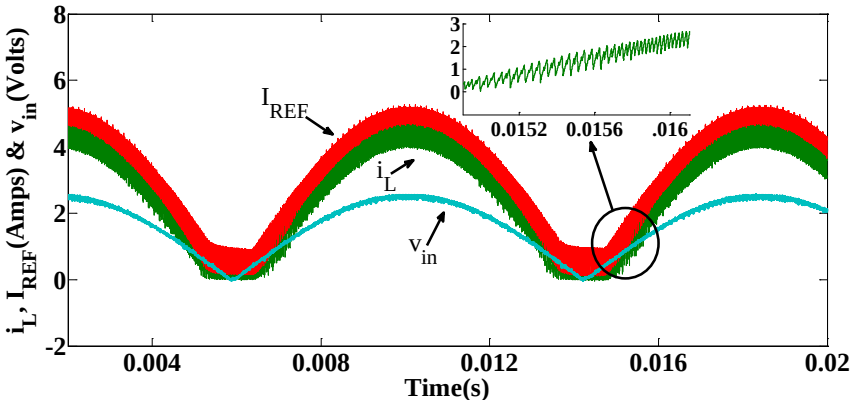

Fig. 1.22. Current and voltage waveforms of PFC with M_{a1} for PCMC.

Figs. 1.23 shows the test result obtained using M_{a2} for PCMC. As predicted, the current remains in the distorted area longer than in Figs. 1.22. However, is the current experiences no instability. Note that the peak value of i_{ref} is again 5.2 amperes; however, the peak value of the inductor current is less because of a larger external ramp.

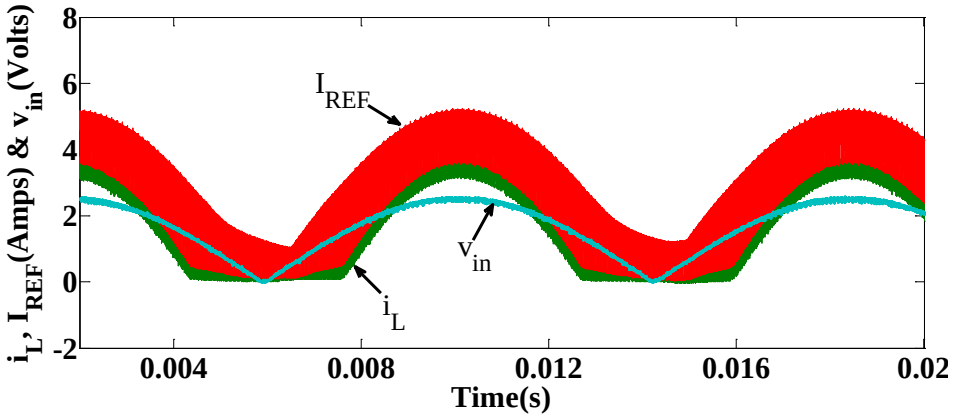

Fig. 1.23. Current and voltage waveforms of PFC with Ma2 for PCMC.

Figs. 1.24 and 1.25 depict the results for the same test with ASC Methods I and II, respectively. As predicted, both methods present stability in the current for the entire duty cycle range, while their discontinuous current regions are less than in the M_{a2} case.

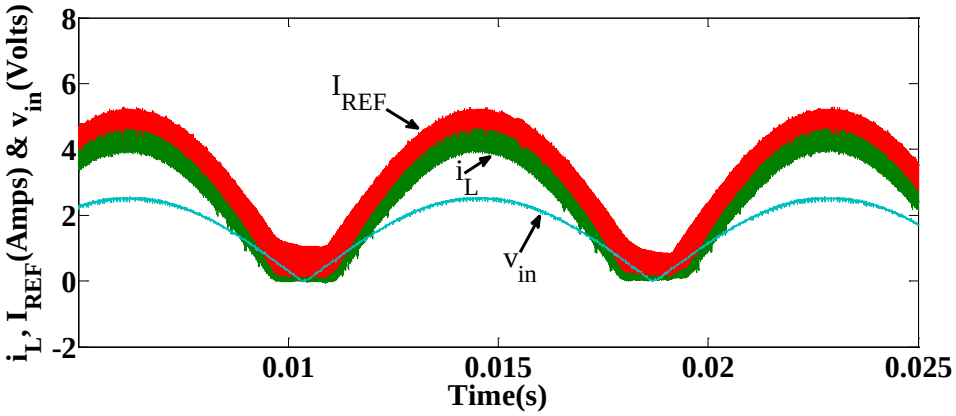

Fig. 1.24. Current and voltage waveforms of PFC with ASC Method I.

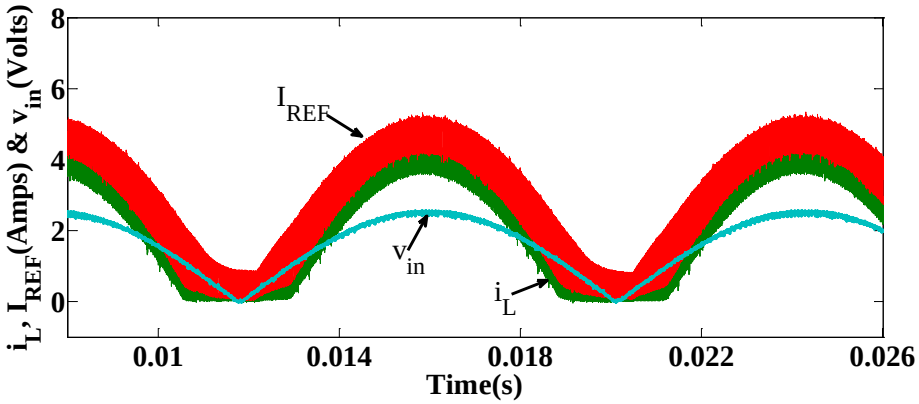

Fig. 1.25. Current and voltage waveforms of PFC with ASC Method II.

Fig. 1.26 shows the result for ASC Method III. The i_{ref} and *f(t)* (see (38)) is shown in this figure to illustrate the average current control capability of this ASC method. As seen, i_L is compared with the *f(t)* function, as discussed in (37) and (38). To see the details of current control for this method, an enlarged version of a short interval is shown in Fig. 1.26. Note that *f(t)* here has a trapezoidal shape different from the one explained in Fig. 1.8 and seen in Fig. 1.18. The reason for this inconsistency is the experimental

specification for integrator IC, which relates to its reset mode. However, because the integrator is active in the *DT* region, this limitation does not affect the control system.

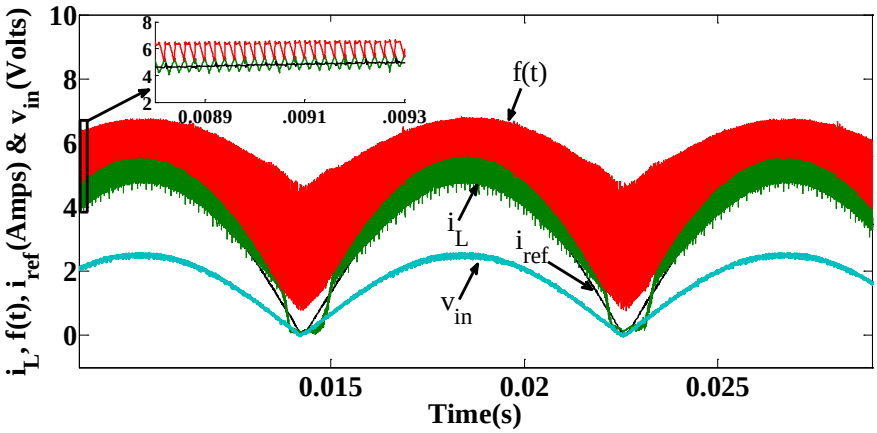

Fig. 1.26. Current and voltage waveforms of PFC with ASC Method III.

Clearly, compared to other ASC methods and PCMC with constant slopes, ASC Method III suffers from a shorter duration of discontinues current. However, because a duty cycle limit always exists in the experimental implementation, the current cannot track the average as in the ideal simulation case. As seen, this method includes no instability region for the inductor current.

1.8. CONCLUSIONS

Three different ASC methods for PCMC were presented and discussed to solve the current instability problem in a power converter with a wide range of applications. Small signal analysis and modelling of these methods were presented. The current loop gain of PCMC using these ASC methods for a wide range of operating points were investigated, which helped in understanding the effectiveness of these methods. A PFC circuit was implanted as an example of a power converter with a wide range of operating points in the lab and was tested under these ASC methods. The simulation and experimental tests demonstrated that the proposed methods could successfully guarantee

the inductor current's stability over the entire range of operating points and in general present a good compromise between satiability and fast dynamic. Moreover, the undesirable time interval during which the inductor current is discontinuous can be reduced using ASC methods.

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2. PROJECTED CROSS POINT CONTROL–MODELING AND ANALYSIS

M. Khazraei, M.Ferdowsi

Missouri University of Science and Technology

e-mail: skn96@mail.mst.edu

Abstract—This paper features the projected cross point control (PCPC) approach which is a recent current-mode control technique. PCPC benefits from advantages such as fixed switching frequency, wide stability range, high current loop gain, improved audio susceptibility, and easier design procedure. An introduction of its principles of operation is followed by detailed discussions about its stability, and dynamic response. The paper then describes the development of the small-signal model of PCPC and derives transfer functions, such as current loop gain, audio susceptibility, and output impedance. Finally, simulations and experimental results are presented. Peak, average, and hysteresis current-mode control schemes are used for comparison.

Index Terms—Current-mode control; Dynamic response; Stability; Switched mode power converter

Table 2.1. List of Abbreviations

ACMC	Average Current-Mode Control
HCMC	Hysteresis Current-Mode Control
PCMC	Peak Current-Mode Control

2.1. INTRODUCTION

Current-mode control schemes benefit from several advantages over voltage-mode control methods. For example, they are more suitable for the parallel operation of converters. They also provide over-current protection. In the buck converter, current-

mode controllers improve the transient response as they reduce the order of the converter by one. In addition, they improve line regulation. These advantages have made them the method of choice in many power supply applications since their first introduction in the late 1970s [1]. Usually, current-mode control methods are divided into two main categories, fixed-frequency methods and variable-frequency methods. Different types of fixed-frequency methods have been introduced in the literature, including peak current-mode control (PCMC) [2-6], average current-mode control (ACMC) [7-9], valley control [2], and charge control [10-13]. Among these methods, PCMC and ACMC are the most commonly used. Table 2.1 lists the control methods that will be discussed in this paper.

In order to generate the PWM gate signal in PCMC, the peak value of the inductor current is measured and compared with its reference. The PCMC method offers several advantages, including constant switching frequency, simplicity of implementation, and good dynamic response. It also has several disadvantages, such as its slope compensation requirement for duty cycles above 50% to eliminate sub-harmonic oscillations, peak-to-average error in the inductor current signal, and poor noise immunity.

In the ACMC approach, the inductor current first is measured and fed into a compensation network to obtain its dc value. Then, the output of the compensator is compared with a saw-tooth ramp to generate the PWM gate signal [7]. The advantages offered by ACMC, such as the ability to control the average inductor current and improvements in noise immunity, have been discussed in [7]. However, due to the presence of a low-pass filter, this control method exhibits a slower dynamic response.

Most constant-frequency control schemes, including PCMC and ACMC, exhibit sub-harmonic oscillations if they are not heavily compensated [7]. Variable-frequency

current-mode controllers resolve this issue due to their free-running operation. The hysteresis current-mode control (HCMC) scheme is one of the most popular variable-frequency approaches. Its principle of operation is discussed in [14-20]. HCMC has several advantages, including no slope compensation requirement for duty ratios above 50%, no sub-harmonic oscillations, and zero peak-to-average error. Despite several advantages, due to its variable frequency operation, HCMC is not suitable for any application that needs to synchronize the converter's switching frequency with some external clock.

The projected cross point control (PCPC) method was first introduced in [21, 22] as a fixed-frequency current-mode controller which is stable for the entire range of the duty cycle. It was then modified in [23, 24] to simplify its hardware realization. Earlier work on this controller primarily focuses on introducing its principles of operation whereas this paper presents an in-depth analysis and experimental validation of its small-signal model through a comparative analysis. Interesting behaviors of PCPC such as high current loop gain and improved audio susceptibility are analyzed in this work. Another important feature of this method which is discussed here is that it directly controls the average value of the inductor current; therefore, no peak-to-average current error exists.

The remaining of this paper is divided into the following sections. PCPC's principles of operation are described in Section 2.2. Its stability and dynamic response characteristics are discussed through comparison with PCMC and ACMC in Section 2.3. In Section 2.4, a small-signal model is developed which is then used to extract its important transfer functions such as current loop gain, audio susceptibility, and output

impedance. Section 2.5, presents the simulation and experimental results. Finally, concluding remarks are provided in Section 2.6.

2.2. PRINCIPLES OF OPERATION OF PCPC

A typical inductor current waveform, i_L, of a DC/DC converter is depicted in Fig. 2.1. M_1 labels the rising slope of the inductor current and $-M_2$ marks its falling slope. Here, the control objective is to make sure that the average value of the inductor current follows the current reference which is labeled as i_{ref}. In order to achieve this, one has to make sure that the final value of the inductor current returns to its steady-state value regardless of its initial state. In other words,

$$\forall i_L(t=0): \quad i_L(t=T) = i_{ref} - \frac{\Delta I_L}{2} \tag{1}$$

where ΔI_L is the steady-state peak-to-peak ripple of the inductor current. It is assumed that $t = 0$ marks the beginning of the transient period. So under ideal conditions, if the inductor current is initially perturbed by $\hat{i}_L(0)$, this perturbation is to be totally damped down at the end of the same period, or $\hat{i}_L(T) = 0$. If the switch is on from time 0 to t_{on}, there is only one value for t_{on} which satisfies the control objective and that is

$$i_L(t = t_{on}) = i^-(t = t_{on}) \tag{2}$$

where $i^-(t)$ is a straight line with a slope of $-M_2$ and satisfies

$$i^-(t = T) = i_{ref} - \frac{\Delta I_L}{2}. \tag{3}$$

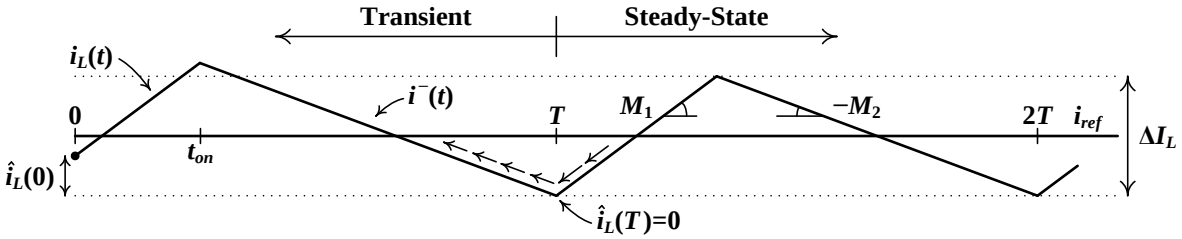

Fig. 2.1. A typical inductor current waveform of a DC/DC converter with the initial disturbance get rejected in just one cycle.

This would be as if someone were travelling back in time from the steady-state to transient conditions and sketched the correct trace for the inductor current (follow the straight arrows in Fig. 2.1. One can describe $i^{-}(t)$

$$i^{-}(t) = i_{ref} - \frac{\Delta I_L}{2} - M_2(t-T) \tag{4}$$

As will be shown later, all of the parameters in (4) which are needed to compose $i^{-}(t)$ are available except for ΔI_L. In [21, 22], a moving average mechanism is proposed to find ΔI_L. This moving average mechanism is not easy to implement.

To solve this problem, the described control method can be modified as in [23, 24]. Now instead of rejecting the disturbance in just one cycle the PCPC will reject it in more than one cycle as seen in Fig. 2.2. For this purpose the desired cross point of i_L and *i-* must happen at the point where make the *i-* settle down at point $i_{ref} - \Delta i_L/2$ at the end of period as shown in Fig. 2. 2. Δi_L in Fig. 2.2 in contrast to ΔI_L in Fig. 2.1 is defined as the peak to peak of inductor current in transient when there is an initial disturbance. Considering this modification and Fig. 2.2 the new equation for $i^{-}(t)$ can be written as:

$$i^{-}(t) = i_{ref} - \frac{\Delta i_L}{2} - M_2(t-T),\ \Delta i_L = M_1 * t\Big|_{t=t_{on}} \tag{5}$$

Now let's replace Δi_L in (5) by M_1*t. As expressed in (5) Δi_L as a constant value during each specific period is equal to M_1*t which is a varying quantity only at $t=t_{on}$. Hence, by doing the mentioned substitution the resulted equation will be different from (5) and is expressed as $i^{\sim}(t)$ in (6).

$$i^{\sim}(t) = i_{ref} - \frac{M_1 * t}{2} - M_2(t-T) \tag{6}$$

$i^{\sim}(t)$ is equal to $i^{-}(t)$ at $t=t_{on}$ which is good enough because t_{on} is the only point which is important for control purpose.

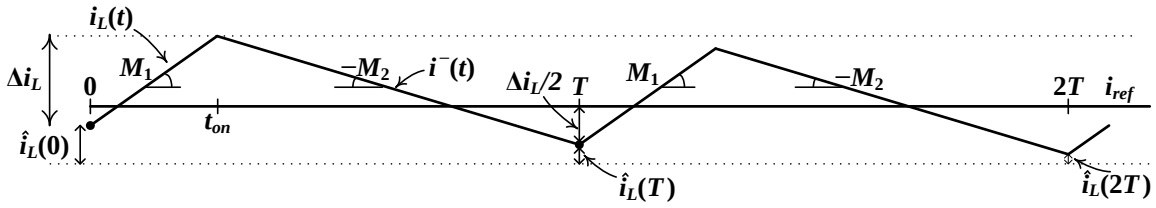

Fig. 2.2. A typical inductor current waveform of a DC/DC converter with the initial disturbance get rejected in more than one cycle.

One can interpret (6) as a straight line with $-M_2$ as slope and a variable intercept as depicted in Fig. 2.3. At the beginning of the transient switching period, the inductor current is perturbed with $\hat{i}_L(0)$ while $i^{\sim}(t)$ in (6) is not pointing to a correct final value. As time goes on and the inductor current grows, $i^{\sim}(t)$ moves down and $\hat{i}_L(T)$ gets smaller. At time $t = t_{on}$, the two lines intersect and the switch is turned off. This is when $i^{\sim}(t)$ in (6) is pointing to the correct final value and therefore the control objective is satisfied. As mentioned before this correct final point is at $i_{ref} - \Delta i_L/2$. So, in order to find the correct time to turn the switch off, one needs to find the point of intersection between lines $i_L(t)$ and $i^{\sim}(t)$ in (6).

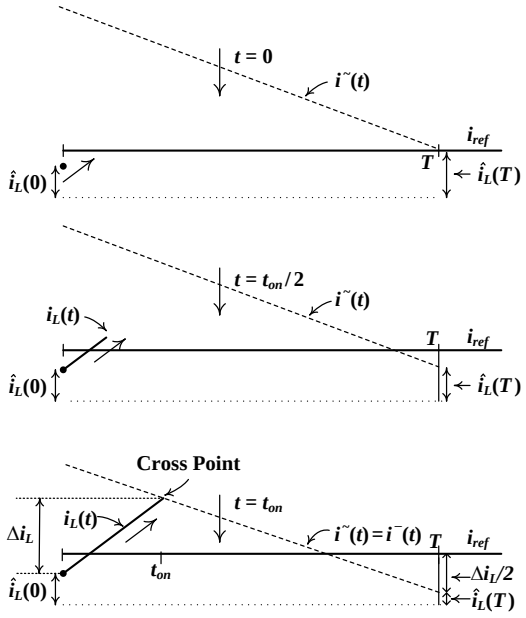

Fig. 2.3. A graphic description of how $i_L(t)$ and $i^{\sim}(t)$ intersect.

It is worth noting that Fig. 2.3 is just a graphic demonstration and that is not how things really happen. For example, in the buck converter by replacing M_1 with $(v_{in}-v_o)/L$ and M_2 with v_o/L, one can re-label and rewrite (6) as

$$f(t) = i_{ref} - \frac{v_{in}+v_o}{2L}t + \frac{v_o}{L}T \tag{7}$$

Fig. 2.4, shows how $i_L(t)$ and $f(t)$ grow over the course of one switching period and how their cross point is determined.

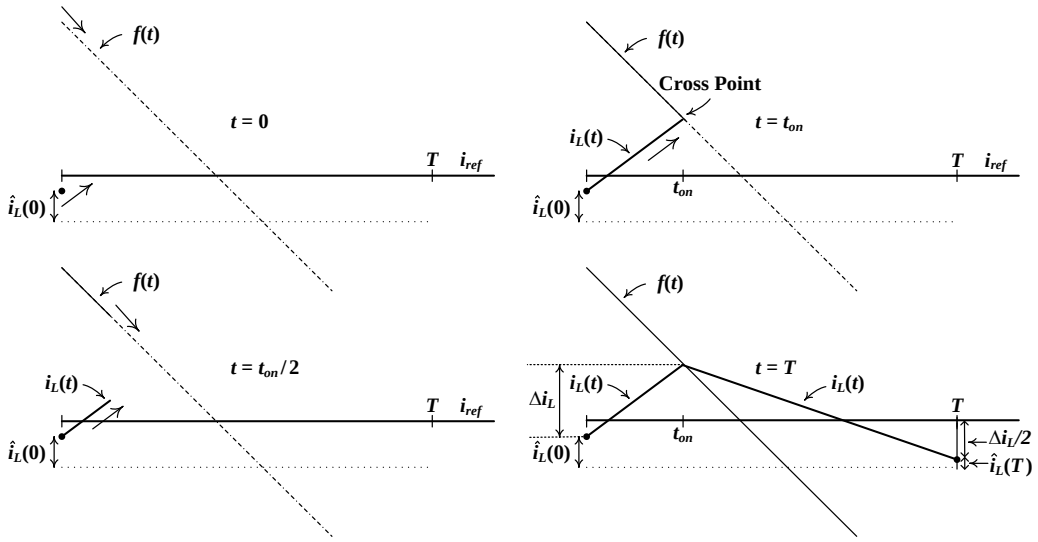

Fig. 2.4. PCPC finds the cross point of $i_L(t)$ and $f(t)$.

During a transient switching period, the value of t_{on} is slightly different than that of a steady-state switching period. Consequently, it takes more than one switching cycle to completely damp down the initial perturbation as shown in Fig. 2.5. In this figure, point *a* which was the steady-state cross point of $i_L(t)$ and $f(t)$ is now moved to point *b* due to the initial disturbance. One can write:

$$\hat{i}_L(0) = \left(\left| \frac{df(t)}{dt} \right| + M_1 \right) \hat{d} \tag{8}$$

$$\hat{i}_L(T) = \left(\left| \frac{df(t)}{dt} \right| - M_2 \right) \hat{d} \tag{9}$$

From (7), it is clear that for the buck converter

$$\left| \frac{df(t)}{dt} \right| = \frac{v_{in} + v_o}{2L} \tag{10}$$

By combining (8), (9), and (10) and applying the steady-state relationships of the buck converter one can write:

$$\frac{\hat{i}_L(T)}{\hat{i}_L(0)} = \frac{1-D}{3-D} \tag{11}$$

Equation (11) is always less than 1 no matter what the value of the duty ratio is. This suggests that PCPC always moves towards stability and away from chaos.

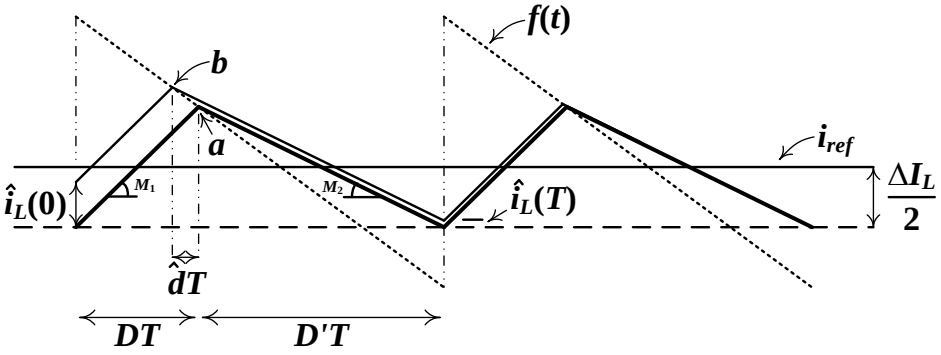

Fig. 2.5. Inductor current waveform of a buck converter controlled under the PCPC method when there is some initial disturbance.

Similar to (7), the PCPC control equations for boost and buck-boost converters can be respectively derived as:

$$f(t) = i_{ref} + \left(\frac{v_{in}}{2L} - \frac{v_o}{L}\right)t + \frac{v_o - v_{in}}{L}T \tag{12}$$

$$f(t) = i_{ref} + \left(\frac{v_o}{L} - \frac{v_{in}}{2L}\right)t - \frac{v_o}{L}T \tag{13}$$

Fig. 2.6 shows the block diagram for the hardware implementation of the boost converter controlled under the PCPC method. The clock marks the beginning of each switching cycle by setting an S-R latch. The latch is reset when the cross point happens. This is when $i_L(t)$ tends to get larger than $f(t)$, see the comparator in Fig. 2.6. For the boost converter, equation (12) is used to synthesize $f(t)$. The current reference is provided by the voltage compensator, $(v_{in}/2-v_o)\cdot t$ is the output of an integrator, and $(v_o-v_{in})\cdot T$ is measured using an integrator and a sample and hold block. Both integrators are reset by the clock and the beginning of each switching cycle. Equations (7) and (13) can be used to implement the control blocks for the buck and buck-boost converters.

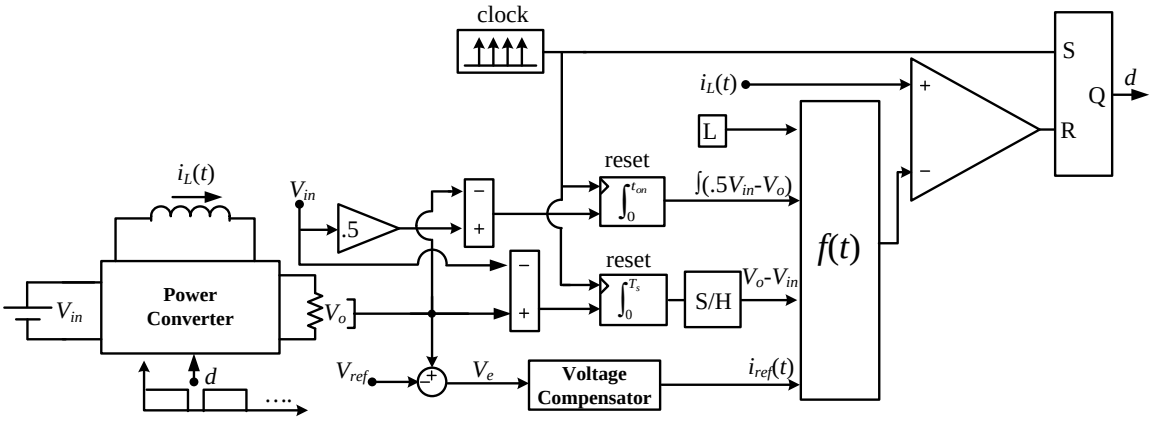

Fig. 2.6. Block diagram of the implementation of a boost converter under the PCPC method.

2.3. PCPC VS. PCMC AND ACMC APPROACHES

2.3.1. Stability And Dynamic Response: In the PCMC approach, t_{on} is determined when the inductor current tends to get larger than $i_{ref}-S_e(t)$ where $S_e(t)$ is an external ramp function. One can compare this with $f(t)$ in (7), (12), or (13) and conclude that in PCPC, the second and third expressions on the right-hand side of the expression

for *f(t)* resemble the external ramp in PCMC. This reveals that, the PCPC technique has an intrinsic self-tuned stabilization function. Similar to (11), the disturbance rejection ratio in the inductor current for the PCMC method can be described as [27]

$$\frac{\hat{i}_L(T)}{\hat{i}_L(0)} = \left(\frac{D}{1-D}\right) \tag{14}$$

Both (11) and (14) are sketched in Fig. 2.7. As shown, the disturbance rejection ratio of PCMC is less than 1 only when the duty rate is less than 0.5. Otherwise, PCMC tends to get chaotic and therefore needs external ramp compensation. Fig. 2.7 also depicts the disturbance rejection ratio for the PCMC approach when M_a, the slope of the external ramp, is chosen to be $M_2/2$ and $2M_2$ [27].

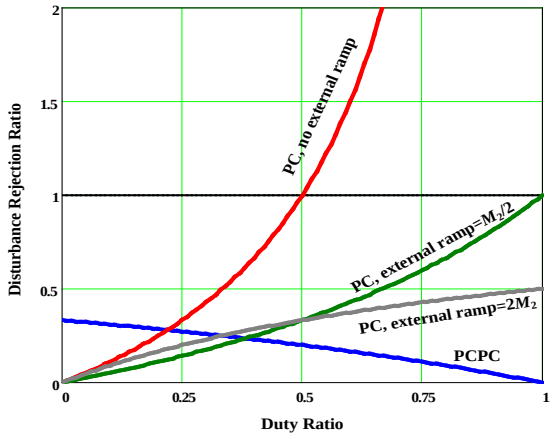

Fig. 2.7. Disturbance rejection ratio for both PCPC and PCMC

In the ACMC approach, the inductor current is sensed and fed into a compensation network to obtain its average value. The output of the compensator is then compared with a sawtooth ramp to generate the PWM control signal. ACMC is prone to sub-harmonic oscillations if it is not heavily compensated. However, this oscillation can be prevented by appropriate design of the current loop. Therefore, the design of ACMC is more complex. Another disadvantage of ACMC is its slow dynamic response since a

low-pass filter is used in its current control loop. This leads to a narrower tradeoff window between speed and stability in the ACMC [28] approach.

2.3.2. Peak-To-Average Current Error: In PCMC, only the peak value of the inductor current is controlled. Hence, the difference between the signal that must be controlled (average current) and the one that is actually controlled creates a so-called peak-to-average error. This error leads to a higher audio susceptibility in PCMC [26]. Also, in PCMC, the circuit detects the peak current; therefore, the peak-to-average current error will vary with the operating point. In PCPC the average value of the inductor current is directly controlled. Therefore, no such error exists.

2.3.3. Dependence On Inductor Value: The PCPC approach needs to have the inductor value for its operation. This can be observed in (7), (12), and (13) where L appears. The value of the inductor is not dependent on the operating conditions. However, there might be some gradual aging and thermal effects on the inductor value. This issue has been addressed in [22] where a PI controller is added to compensate for such variations. The PI controller which has a low bandwidth self tunes the value of the inductor that the controller uses based on the error between i_{ref} and the average value of the inductor current.

2.4. SMALL-SIGNAL MODEL DEVELOPMENT

The procedure applied in this section to obtain the small-signal model for PCPC is similar to the one used for the PCMC method in [25]. This procedure is conducted for the boost converter here but can be applied to any other basic converter. In PCMC, an external ramp is added to the inductor current. The result is then compared with the

current reference. Therefore, in this control method, the modulator gain (see Fig. 2.8) is [25]:

$$F_m = \frac{1}{(M_1 + M_a)T} \tag{15}$$

where M_a is the slope of the external ramp, M_1 is the rising slope of the inductor current, and T is the switching frequency. Similarly, considering (12) for the boost converter controlled under PCPC, the modulator gain can be written as:

$$F_m = \frac{1}{(\frac{df(t)}{dt} - M_1)T} = \frac{L}{T(V_{in}/2 + V_o)} \tag{16}$$

Fig. 2.8 shows the small-signal block diagram of PCPC for a boost converter. Note that in this block diagram, for the sake of simplicity, the dc gain of the current sensor is considered to be one. To model the effect of the input and output voltage perturbations on the duty cycle, feed-forward and feedback gains F_i and F_{vo} are introduced as well [25]. To obtain these gains, the average value of the inductor current must be considered. In PCPC, under steady-state conditions, one can write:

$$< i_L > = i_{ref} \tag{17}$$

where $< i_L >$ denotes the average value of the inductor current. Assuming that v_o and i_{ref} are constant, this equation can be perturbed to obtain the dependence of the inductor current on the input voltage. The steady-state small-signal dependence of the average inductor current on the input voltage can be found by differentiating (17) with respect to the input voltage, which yields:

$$\frac{< \hat{i}_L >}{\hat{v}_{in}} = 0 \tag{18}$$

From the power stage as seen in Fig. 2.8, one can write:

$$(-F_i\hat{v}_{in} - \hat{i}_L)F_m = \hat{d} \tag{19}$$

$$\hat{v}_{in} + \hat{d}V_o = 0 \tag{20}$$

$$F_i = \frac{1}{V_o F_m} \tag{21}$$

Then by substituting F_m from (16), one can write:

$$F_i = \frac{T(3-D)}{2L} \tag{22}$$

F_{vo} can be obtained using a similar approach, written as:

$$F_{vo} = \frac{-TD'(3-D)}{2L} \tag{23}$$

These small-signal gains have been derived for other basic DC/DC converters, as seen in Table 2.2.

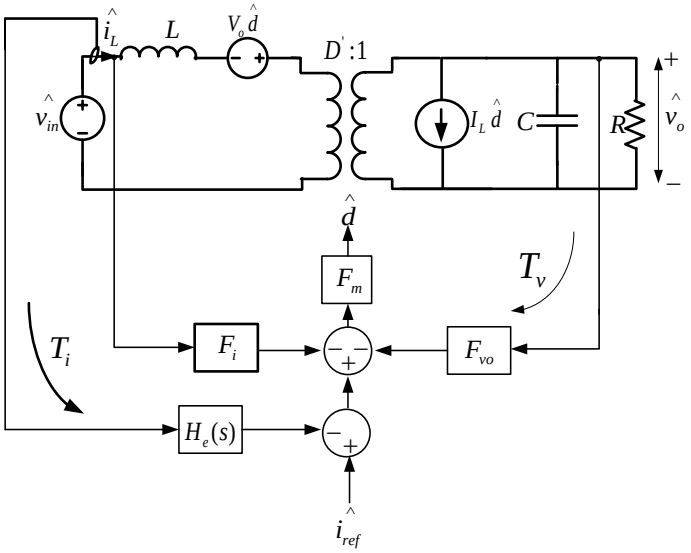

Fig. 2.8. Small-signal block diagram of PCPC for a boost converter.

Table 2.2. Small Signal Parameters of PCPC for Basic Converters

	F_m	F_i	F_{vo}
Buck	$\frac{L}{T(3V_{in}/2-V_o/2)}$	$\frac{TD(3-D)}{2L}$	$-\frac{T(3-D)}{2L}$
Boost	$\frac{L}{T(V_{in}/2+V_o)}$	$\frac{T(3-D)}{2L}$	$\frac{-TD'(3-D)}{2L}$
Buck-Boost	$\frac{L}{T(3V_{in}/2-V_o)}$	$\frac{TD(3-D)}{2L}$	$\frac{TD'(3-D)}{2L}$

The sampling effect of the inductor current should be considered in the small-signal model as well. In [25], the sample and hold effect is obtained as follows:

$$H_e(s)=1+\frac{s}{\omega_n Q}+\frac{s^2}{\omega_n{}^2} \text{ where } Q=\frac{-2}{\pi}, \omega_n=\frac{\pi}{T} \tag{24}$$

It is also shown that this sampling gain is invariant for all converters using constant frequency, constant on-time, or constant off-time control, such as PCPC. It always exhibits 180° of phase lag at half of the switching frequency. By considering this effect in the small-signal model of PCMC and ACMC, the instability of the current loop in these control schemes can be explained. Conversely, as predicted and as will be shown, no instability is observed by adding this effect into the small-signal model of PCPC. This gain is considered in the small-signal model in this paper.

Next, various transfer functions can be obtained using the derived small-signal model. All the essential transfer functions have been tabulated in Table 2.3. In this table, T_i is the current loop gain, and G_{iL_iref} is the control-to-inductor current transfer function, where:

$$G_{i_{L}-i_{ref}}=\frac{T_i}{1+T_i} \tag{25}$$

in which $\hat{v}_o / \hat{\imath}_{ref}$ is the control-to-output voltage transfer function, $\hat{v}_o / \hat{v}_{in}$ is the audio susceptibility, and Z_o is the output impedance. The loop gains for the three converters are the same. Note that r is the sum of the parasitic resistances in series with the inductor (R_L) and current sensing resistor (R_i). The resistor in series with the output capacitor (R_{esr}) is considered here, too.

Table 2.3. Small-Signal Transfer Functions of PCPC for DC/DC Converters

	T_i	$\hat{v}_o / \hat{i}_{ref}$	$\hat{v}_o / \hat{v}_{in}$	Z_{out}
Buck	$\frac{2LH_e(s)}{Tr(3-D)((L/r)s+1)}$	$\frac{G_{i_L - i_{ref}}(R_{esr}Cs+1)R}{(R+R_{esr})Cs+1}$	0	$\frac{(R_{esr}Cs+1)R}{(R+R_{esr})Cs+1}$
Boost	$\frac{2LH_e(s)}{Tr(3-D)((L/r)s+1)}$	$\frac{G_{i_L - i_{ref}}RD'}{2}\frac{(R_{esr}Cs+1)(1-Ls/(RD'^2))}{(R/2+R_{esr})Cs+1}$	$\frac{1}{2D'}\frac{R_{esr}Cs+1}{(R/2+R_{esr})Cs+1}$	$\frac{1}{2}\frac{R(R_{esr}Cs+1)}{(R/2+R_{esr})Cs+1}$
Buck-Boost	$\frac{2LH_e(s)}{Tr(3-D)((L/r)s+1)}$	$-\frac{G_{i_L - i_{ref}}RD'}{(1+D)}\frac{(R_{esr}Cs+1)(1-LDs/(RD'^2))}{(R/(1+D)+R_{esr})Cs+1}$	$\frac{-D^2}{1-D^2}\frac{R_{esr}Cs+1}{(R/(1+D)+R_{esr})Cs+1}$	$\frac{1}{1+D}\frac{R(R_{esr}Cs+1)}{(R/(1+D)+R_{esr})Cs+1}$

2.4.1. Current Loop Gain: For clarification, the properties of the PCPC loop gain will be compared with those of the PCMC and ACMC methods. In order to create a clear comparison with the common PCMC and ACMC models in the literature, r and R_{esr} are neglected for the purposes of this section only. In fact, R_L and R_i usually have negligible effects on the small-signal model and, in contrast to R_{esr}, do not produce any new zeros or poles. However, in the PCPC model, these series resistors play a role in the low frequency range. This issue will be addressed in Section 2.5.

The current loop gain presents useful design information, including steady-state error and loop stability. Using the block diagram in Fig. 2.8, the analytical expression for the current loop gain is obtained as:

$$T_i(s) = \frac{H_e(s)F_m G_{i_L d}(s)}{1 + F_m F_{vo} G_{vd}(s)} = \frac{2H_e(s)}{T(3-D)s} \tag{26}$$

Where

$$G_{vd} = \frac{V_o}{D'} \frac{1 - (L/(RD'^2))s}{1 + (L/(RD'^2))s + (LC/D'^2)s^2} \tag{27}$$

and

$$G_{i_L d} = \frac{2V_o}{RD'^2} \frac{1 + (R/2)Cs}{1 + (L/(RD'^2))s + (LC/D'^2)s^2} \tag{28}$$

Using this transfer function, the loop gain of PCPC is compared with that of the PCMC and ACMC methods. In [25], the analytical expression for PCPC loop gain is reported as:

$$T_i \approx \frac{L}{V_{in} m_c T} G_{i_L d} H_e(s) R_i \tag{29}$$

where

$$m_c = 1 + \frac{M_a}{M_1} \tag{30}$$

In (29), in contrast to (26), the effect of feedback gain F_{vo} is not considered because of its negligible effect on the format of the transfer function. A comparison between (26) and (29) reveals that in PCPC, unlike in PCPC, the loop gain is completely independent of the load. Also, its dependence on D is negligible. This is because, in PCPC, the average value of the inductor current is controlled, whereas in PCPC, the peak value of the inductor current tracks the reference, causing some peak-to-average error that is dependent on the input voltage. There is another way to interpret this issue, which is related to the dc gain. In PCPC, there is infinite dc gain in T_i, which means that the inductor current precisely tracks the current reference with no steady-state error. However, in PCPC, the dc gain is

$$T_i(s=0)=\frac{2L}{RD'^3T_s m_c} \tag{31}$$

which shows its dependency on the inductor, switching period, duty cycle, load, and external ramp.

Fig. 2.9 shows the magnitude and phase plots of the current loop gain of the PCPC and PCMC methods for different values of the external ramp. PCPC remains constantly stable, while the behavior of PCPC exhibits a compromise between stability and speed. In other words, increasing the external ramp increases the phase margin of the current loop as well as the stability. However, at the same time, the system will become slower.

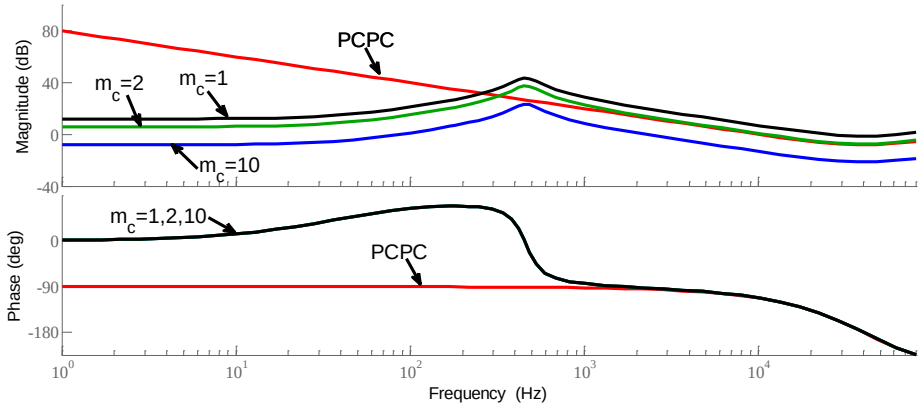

Fig. 2.9. Bode plot of current loop gain of PCPC and PCMC for different values of external ramp.

Using (26) and considering Fig. 2.9, the crossover frequency for the entire range of D in PCPC can be expressed as:

$$f_s/3\pi \le f_c \le f_s/2\pi \tag{32}$$

which indicates that the maximum crossover frequency in PCPC is less than half the switching frequency. Therefore, according to the Nyquist sampling theorem, the system is always stable. On the other hand, the crossover frequency is always more than a

specific high value, which guarantees high speed for the closed loop system.

In Fig. 2.10, the current loop gain of PCPC is compared with ACMC. In [28], the loop gain of ACMC is given as follows:

$$T_i(s) \approx \frac{V_{in}}{(M_a + M_1^{'})T} \frac{1}{Z_f} \frac{\omega_i(1+s/\omega_z)}{s} H_e(s) \tag{33}$$

where M_a and $M_1^{'}$ are the slope of the sawtooth waveform in the modulator and the compensated on-time slope of the inductor current, respectively, and Z_f is defined based on the output filter parameters, as seen in [28]. Moreover, ω_i and ω_z are the integrator gain and zero of the current compensator.

Fig. 2.10 shows the Bode plot of the current loop gain of the PCPC and ACMC approaches for different values of ω_i. Similar to PCMC, the design of ACMC, as shown in Fig. 2.10, involves a compromise between stability and speed. That is, more integrator gain leads to higher speed and higher low-frequency gain but less phase margin for the closed loop system. In contrast to ACMC, PCPC presents high low-frequency gain accompanied with good conditions for stability and speed.

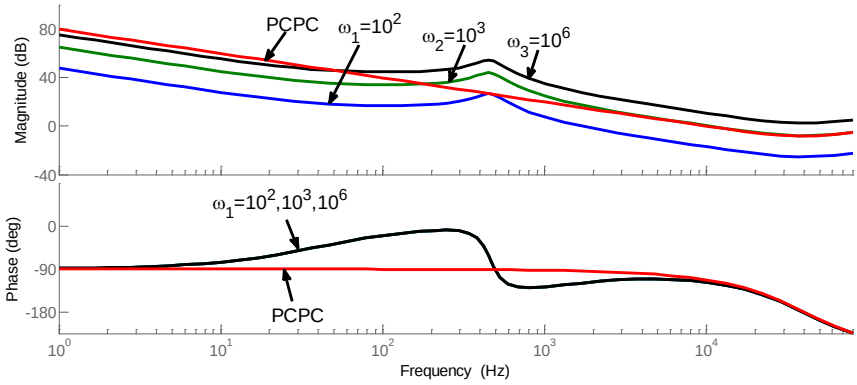

Fig. 2.10. Bode plot of the current loop gain of PCPC and ACMC for different values of the integrator gain.

2.4.2. Control-To-Inductor Current And Output Voltage Transfer Functions:

The control-signal-to-inductor-current transfer function of PCPC, G_{iL_iref}, can be obtained

using (25) and (26). This function is the same for the three basic converters. For the sake of simplicity, to study the function here, r is assumed to be zero, and $H_e(s)$ is assumed to be 1. Hence,

$$G_{i_{L\_}i_{ref}} = \frac{\hat{i}_L}{\hat{i}_{ref}} = \frac{T_i}{1+T_i} = \frac{1}{1+sT_s(3-D)/2} \tag{34}$$

This relation shows that, at low frequencies, the average of the inductor current tracks the reference without dependency on any other parameters. This lies in contrast to the PCMC, for which the low frequency value of G_{iL_iref} depends on R, L, T, and m_c [25].

Further, using Table 2.3 and neglecting the R_{esr} effect, the control-to-output voltage transfer function can be expressed as:

$$\frac{\hat{v}_o}{\hat{i}_{ref}} = \frac{RD'}{2}\frac{(1-Ls/(RD'^2))}{(R/2)Cs+1}\cdot\frac{1}{1+sT_s(3-D)/2} \tag{35}$$

The poles in (35) have been separated deliberately to clearly show the current mode's role in the plant transfer function. The control-to-output-voltage transfer function includes one dominant pole at $\omega = 2/RC$ and a high frequency pole. The goal of a current mode control scheme is to achieve a simpler approximation of the plant compared to a voltage mode method. Clearly, this goal has been satisfied here. This function is the one used to design the voltage loop in current mode control. The current mode controller reduces the order of this transfer function by one. Consequently, as seen, the voltage loop design is easier. In PCMC, for a specific operating point, this function is dependent on the external ramp. This complicates the design of the voltage loop. However, for PCPC, the function is dependent only on the operating point parameters.

2.4.3. Audio Susceptibility: A simple and also a detailed small signal model for the PCMC method are developed in [27]. The simple model neglects the peak-to-average

error and consequently governs under the assumption that the average value of the inductor current directly tracks the current reference. This model predicts zero for the audio susceptibility of the buck converter. Also in [25], an audio susepcibility transfer function is developed for the buck converter, which is not zero but can be nulled if the slope of the external ramp compensation equals half of the falling slope of the inductor current. This slope is called the optimal slope. The audio susceptability of the ACMC appraoch is developed in [28]. Because the current loop amplifier does not ideally yeild infinite gain at zero frequency, the audio suceptibilty of the ACMC approach is dependent on current compensator parameters. This consequently complicates the design procedure.

As presented in Table 2.3, the small signal model of the PCPC approach predicts that the audio susceptibility for the buck converter is zero. This is due to the fact that PCPC eliminates the peak-to-average error. Or, one might say, PCPC behaves like PCMC with an adaptive optimal slope. Another way to express this advantage is to say that PCPC is like ACMC with an infinite current loop gain at zero frequency.

2.4.4. Output Impedance Transfer Function: Similar to the audio susceptibility case, the output impedance of the PCPC model is the same as the simple model in [27]. This value nearly equals the output impedance obtained in [25] if there is no external ramp ($m_c = 1$) and the current ripple is negligible compared to the average current ($R/L << 1$). This means that all three cases, the PCPC, the simple model in [27], and the model in [25] with ($R/L << 1$ and $m_c = 1$ for the model in [25]), are representative of an ideal current source. This property, which situates PCPC as an ideal current source without any other assumptions, in contrast to the models in [25] and [28], may not be as

useful in DC/DC converters applications where a constant output voltage is desired. However, this property can be very useful in motor drive applications. Hence, the output impedance characteristic of PCPC is not discussed any further in this paper.

2.5. SIMULATION AND EXPERIMENTAL RESULTS

Time and frequency domain analyses are conducted using a typical boost converter with the parameters listed in Table 2.4. First, in order to check the current loop performance, the output voltage compensator is disabled, and i_{ref} is externally commanded. Fig. 2.11 shows the experimental waveforms of the inductor current, the *f(t)* function, and the gate signal. This is measured when the current command nearly equals 4 A, which sets the duty ratio at 0.7 approximately. As seen, the inductor current intersects the *f(t)* function, thereby turning the switch off. There is a short delay which is due to the rise and fall times the logic ICs and the gate driver.

Table 2.4. Typical Boost Converter Parameters

Parameter	Value
Inductor	50 µH
C_{out}	820 µF
P_{out}	10 ~ 50 W
V_{in}	6 to 14 V
V_{out}	20 V
Switching Frequency	80 kHz
R_{esr}	40 mΩ
R_L	30 mΩ
R_{sensor}	100 mΩ

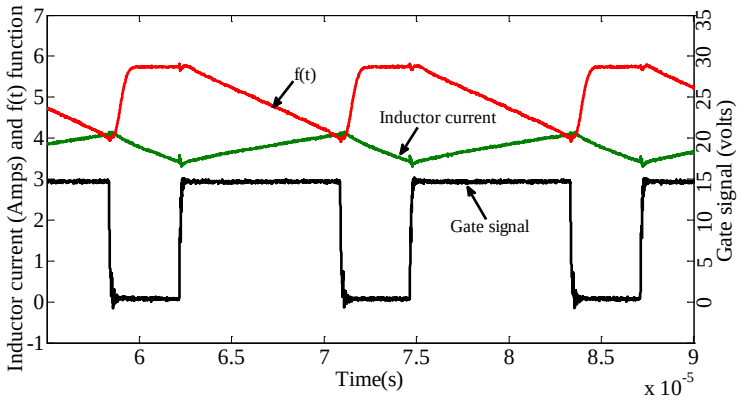

Fig. 2.11. Inductor current, the *f*(*t*) function, and gate signal experimental waveform

It is worth noting that *f*(*t*) here has a trapezoidal shape different from the one depicted in Figs. 2.4 and 2.5. This is because, in preparation for the next coming switching cycle, *f*(*t*) gets reset once the cross point is identified and the switch is turned off. This also makes the system more immune to noise by avoiding undesired interactions between i_L and *f*(*t*).

In Fig. 2.12, first the i_{ref} command experiences a step up from 3 to 5.5 A and then a step down from 5.5 to 3 A. As seen, the inductor current tracks the commanded reference well. However, if noted carefully, there is a small error between the average value of the inductor current and the reference. This error can be attributed to the device delays mentioned above and the current sensor error.

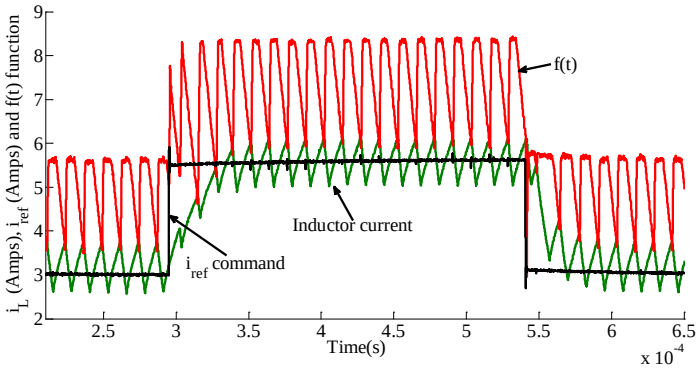

Fig. 2.12. Experimental waveforms when step up and step down changes occur in the current command.

As mentioned earlier, the PCPC method benefits from a better audio susceptibility. In order to show this, an input voltage step down from 10 V to 6.1 V and a step up from 6.1 V to 10 V are introduced to the simulation model as well as the experimental hardware. To make a fair comparison, two completely identical voltage compensators are used for both PCPC and PCMC methods. Moreover, both voltage loops are designed to be as slow as possible to make the current loop's effect dominant. Figs. 2.13 and 2.14 show the results. Two different values of the compensator slope for PCMC have been shown in Figs. 2.13 and 2.14. The value represented by m_c = 1.7 is the least value of the external slope before the PCMC becomes unstable. In other words, this is the value that gives the fastest but least stable PCMC current loop. As it has been discussed in [27], the minimum theoretical value for M_a which guarantees stability is M_a=M_2/2 which leads to an m_c slightly smaller than 1.7. However, selecting m_c to be exactly equal to its theoretical prediction still exhibits some minor sub-harmonic oscillations. Therefore, 1.7 which is slightly larger has been selected. As shown, PCMC with even this value of m_c is slower than PCPC. If a higher value of the external ramp that gives a more reliable and stable loop, such as m_c = 4, is chosen, PCMC will be even slower, as seen in Figs. 13 and 14. For validation purposes, Figs. 2.13 and 2.14 show that the experimental results of PCPC closely match the simulation results.

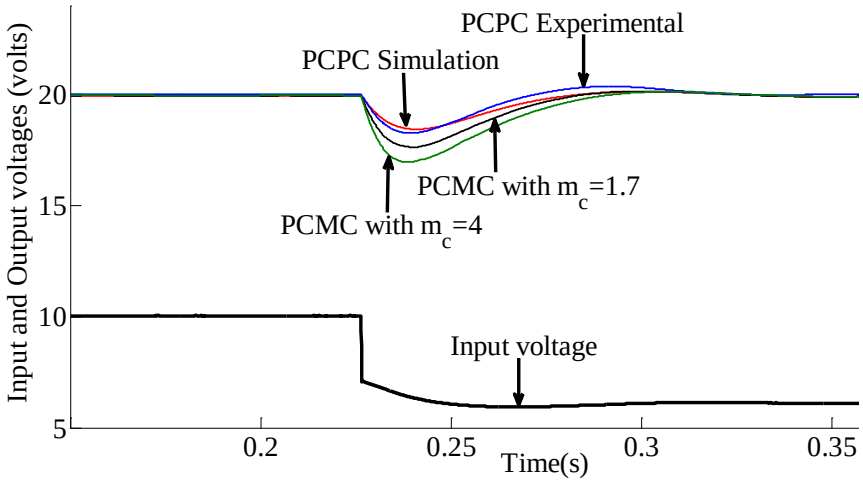

Fig. 2.13. Simulation and experimental waveforms for a input voltage step change from 10 V to 6.1 V.

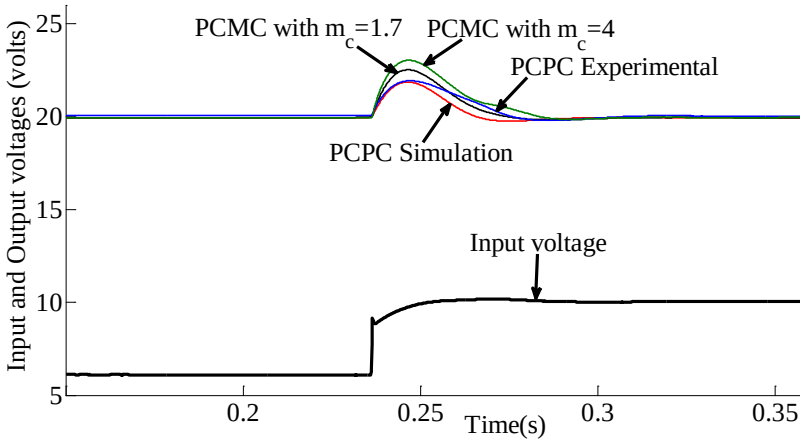

Fig. 2.14. Simulation and experimental waveforms for a input voltage step change from 6.1 V to 10 V.

In order to show that the current loop works well, the system is tested for step-up and step-down changes in the load. Again, the output voltage controller is tuned for a low bandwidth in order to make the effect of the current loop more explicit. Fig. 2.15 shows the output voltage and inductor current waveforms for a step down (and step up) from R = 18 Ω to 11 Ω. Clearly, the system works well.

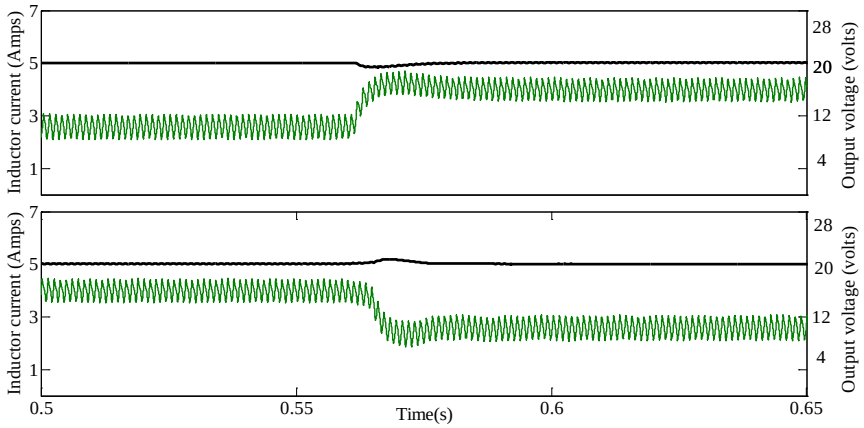

Fig. 2.15. Experimental waveforms of step down and step up in the load.

To clarify how the PCPC scheme is dependent on the value of the inductor, the following test was conducted. i_{ref} was set to be 4.5 A, the load resistance was chosen to be 10 Ω, and the inductor in the power stage as Table 2.4 suggests was 50 μH. At t=0.05 s, the assumed value of the inductor in the controller was wrongfully switched from 50 μH to 60 μH. The results are depicted in Fig. 2.16. As can be seen, the slope of $f(t)$ is reduced, and the average inductor value decreases by 0.1 A. As stated earlier in Section 2.3, this behavior can be used to self tune the controller [22].

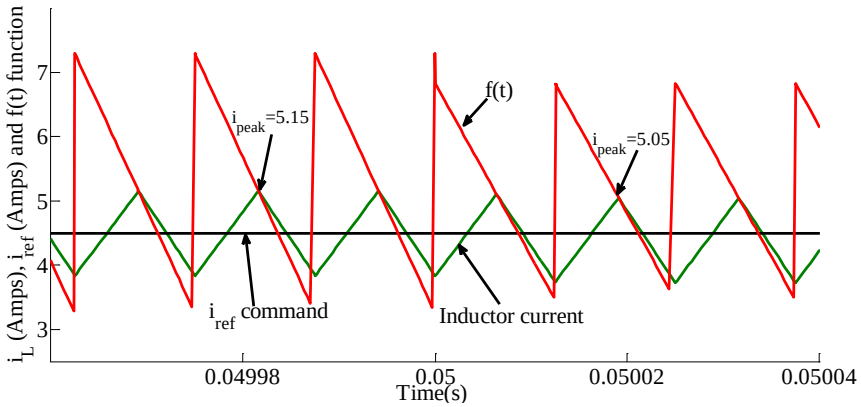

Fig. 2.16. Simulation waveform of the inductor current for a sudden change in the value of the inductor.

Another test was conducted in the simulation setup to check how PCPC performs with higher frequency current references. The converter specifications in Table 2.4 with i_{ref} at 4.5 A and a load of 10 Ω are considered. The performance of PCPC under this condition can be explained using (26) and (34). From (26), the crossover frequency will be nearly 10 kHz. This means that the inductor current can track the current reference satisfactorily if the frequency of ac command is less than 10 kHz. To test this, an ac signal with a magnitude equal to 0.5 A peak to peak with frequencies at 2.5, 5, 10, and 20 (kHz) were added to i_{ref}. Fig. 2.17 shows the results. As predicted form (34) more the frequency more the phase shift and tracking error between command and response. This result shows the superior PCPC response for a large frequency ranges lower than 10 kHz.

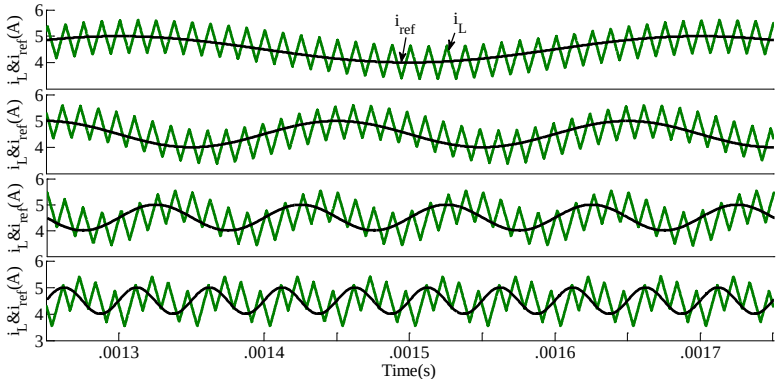

Fig. 2.17. Simulation waveforms of inductor current response to different high frequency current reference.

For the frequency domain analysis, the input voltage and load resistance were respectively set at 10 V and 30 Ω. To measure the loop gain, the conventional analog injection technique was used in this paper [25, 29, 30]. This method works for a wide range of frequencies up to nearly f_{sw} / 2 which is good enough to reveal PCPC's small signal charactristics. The FFT analysis was conducted using a window of 20 cycles in

MATLAB. The sampling frequency was at least 50 times of the injected signal frequency.

As discussed in section 2.4, the loop gain of PCPC would be ideally infinite at dc frequency. However, experimental prototypes always contain a small parasitic resistor in series with the inductor and sometimes a current sensing resistor, as in the case here. To understand the difference between the ideal and non-ideal cases, the current loop gain for ideal (simulation where $r = 0$) and non-ideal (experimental where $r = 0.130\ \Omega$) prototypes are measured. Fig. 2.18 shows the measurements vs. predicted values. The solid lines represent the predicted values obtained from the transfer functions developed in Section 2.4 while the dots represent the measured values acquired via the analog signal injection method. In the ideal case, the gain is infinite at dc frequency. This agrees with what was predicted in Section 2.4. In the non-ideal case, both hardware measurements and the analytical transfer function show that the dc gain is finite.

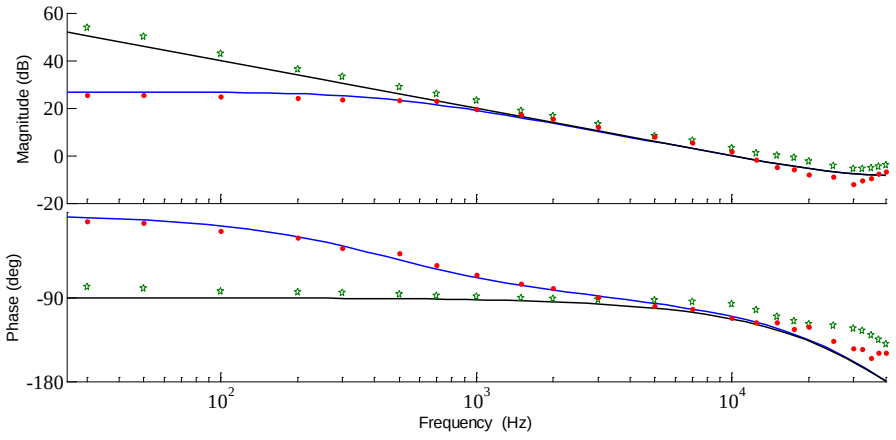

Fig. 2.18. Simulation measurements (star points), experimental measurements (round points) vs. predicted model with $r = 0\ \Omega$ (solid line with infinite dc gain) and predicted model with $r = 0.13\ \Omega$ (solid line with finite dc gain).

For all cases, the measured values are close to the predicted values up to half of the switching frequency (f_{sw} / 2). Several reasons exist for the mismatch beyond this frequency. First, the predicted model is based on assumptions that are valid at frequencies several times lower than the switching frequency. Second, in higher frequencies, the measured data are erroneous due to noise. Finally, the $H_e(s)$ transfer function used in the predicted model represents the sampling effect of current mode controllers and could be better shown if a sampled digital injection technique were. Other models for this frequency range, which differ from the sampled model, are presented in [30]. The phase measurements related to higher frequencies here are in a range between predictions in [25] and [30].

Comparing the experimental and simulation measurements clarifies the effect of r. As mentioned previously, in contrast to R_{esr}, r does not introduce any new poles or zeros. However, it changes the location of the existing poles and zeros in the system. In the ideal case, the current loop gain of PCPC has a pole at zero frequency; while in the practical case, the effect of r moves this pole to r / L.

Fig. 2.19 shows the measured and predicted (based on the transfer function in Table 2.3) values of audio susceptibility of the system. Clearly, R_{esr} has a considerable effect on this function. Fig. 2.20 shows the measured and predicted (based on the transfer function in Table 2.3) values of the commanded-current-to-output-voltage transfer function. As discussed in Section 2.4, this function is the one used to design the voltage loop in current mode controllers. There is a wide range of frequencies for which the phase is more than -90^{o}. This leads to more flexibility in designing the voltage controller.

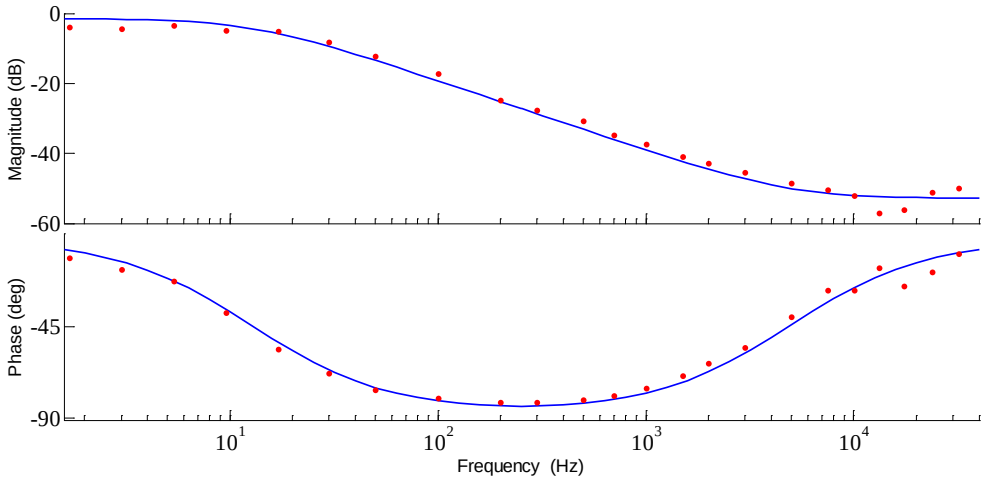

Fig. 2.19. Experimental measurements (dots) vs. predicted values (solid lines) for audio susceptibility.

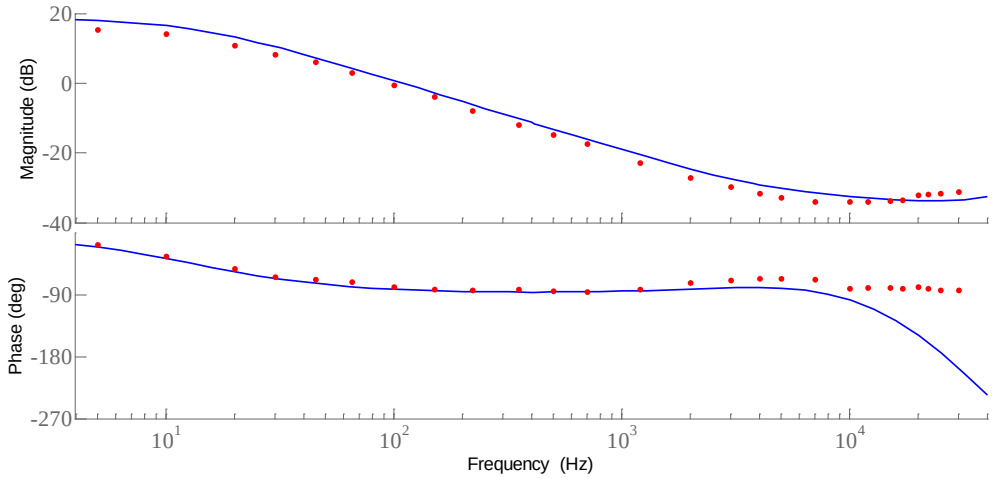

Fig. 2.20. Experimental measurements (dots) vs. predicted values (solid lines) for the control-to-output-voltage transfer function.

2.6. CONCLUSION

In this paper, a new fixed-frequency average current-mode control method first was introduced, and then its transient and small-signal behaviors were analyzed. It was proven that the projected cross point control (PCPC) method benefits from the advantages of both fixed-frequency and variable frequency current-mode controllers. This controller remains stable for the entire range of the duty cycle, and the average value of the inductor current directly tracks the reference. The steady-state error, stability, and

dynamic response issues were investigated using the small-signal model. It was shown that the PCMC and ACMC approaches force designers to make a compromise between speed and stability, whereas in PCPC, high speed and stability are guaranteed. The experimental results showed the performance of the proposed method, and the developed small signal model was validated using the measured data.

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3. SOLID-STATE TRANSFORMER STABILITY AND CONTROL CONSIDERATION

M. Khazraei, M.Ferdowsi

Missouri University of Science and Technology

e-mail: skn96@mail.mst.edu

Abstract—This paper addresses the stability issues and some control solutions in solid-state transformers (SST). An SST is built using three cascaded stages, including an AC/DC rectifier, a dual active bridge (DAB) converter, and a DC/AC inverter. Multistage converters are highly prone to instability due to the interaction of their stages. Hence, the control system must be designed in a way that solves this detrimental interaction effect. Additionally, the stability issue can become even more complicated when a distributed energy storage device (DESD) and a distributed renewable energy resource (DRER) are added to the SST. In this paper, to study the stability of the SST, the Middlebrook criteria will be applied. To do so, the converters' small signal models will be derived, and frequency domain analyses will be presented to predict the time domain behavior of the SST. Then, by means of its average model, an SST will be simulated in PSCAD in order to simulate the time domain and validate the frequency domain stability analyses predictions.

Keywords- distributed energy storage device, distributed renewable energy resource , stability, SST.

3.1. INTRODUCTION

The solid state transformer (SST) is one of the key elements in implementing the Future Renewable Electric Energy Delivery and Management (FREEDM) System. The

FREEDM system, namely Green Hub, is a large-scale micro-grid (MG) with greater reliance on distributed renewable energy resources (DRERs), distributed energy storage devices (DESDs) and power electronic (PE) based components. The SST actively manages DRERs, DESDs and loads [1-4].

The SST has been proposed as part of the FREEDM Green Hub system to substitute for the conventional distribution-level transformer. The SST includes three cascaded PE converters, including an AC/DC rectifier, a dual active bridge (DAB) converter, and a DC/AC inverter. Due to the bidirectional power flow capability of SSTs, DESDs and DRERs, such as storage units and PVs (Photovoltaics), can connect to the SST using DC/DC converter interfaces. This SST's capability adds to the number of interacting converters. In general, multistage converters are highly prone to instability due to the interaction of their cascaded converters. In order to avoid instability, the interacting systems must meet the Middlebrook stability criteria [5]. In other words, the impedance of the second-stage converter always must be higher than the output impedance of the first stage. This is a necessary condition to ensure stability.

The stability of the cascaded converters have been studied previously and reported in the literature. Stability analyses have been reported for cascaded DC/DC systems and distributed power systems based on DC/DC converters, AC/DC rectifiers and DC/AC inverters [6-10]. It has been shown how the independent stable systems may become unstable when combined.

On the other hand, the stability issue in multistage systems with bidirectional power flow capabilities has been rarely addressed in the literature. In [10], this issue has been studied for a system with an AC/DC rectifier connected to a DAB. However, the

control used to regulate the cascaded system in [10] depends on the direction of power flow. Hence, for different power flow directions, a separate control system must be used. This means that different transfer functions and consequently different impedance models must be derived for each power flow direction. This issue makes the stability analysis more tedious, especially in the case of an SST with a DRER and a DESD in which different power flow scenarios can be defined. Moreover, switching to a different control algorithm when the direction of power changes is not a popular option in industry. In an SST, however, the same control system is used regardless of the power direction.

In this paper, the control design and stability analysis do not depend on power flow. Hence, the derivation of small-signal modeling and transfer functions is independent of power flow, which makes the stability analysis much easier and more practical, especially in the case of SST with a DRER and a DESD in which different power flow scenarios can be defined.

In Section 3.2, the SST system will be introduced, and its performance will be discussed. In Section 3.3, the small-signal modeling and input and output impedance transfer functions will be derived. Sections 3.4 and 3.5, respectively, present the stability analysis for the high-voltage (HV) DC link and low-voltage (LV) DC link.

3.2. INTRODUCTION TO THE SST SYSTEM

Fig. 3.1 shows an SST fed by a conventional 7.2 kV substation. As seen in Fig. 3.1, the SST includes a single-phase active rectifier with a 7.2-kV AC input and a 12-kV DC output, followed by a DC/DC converter with a 12-kV DC input and a 400-V DC output, and finally followed by a single-phase inverter with a 400-V DC input and a 240-V rms AC output. Any of these three stages can be implemented by various topologies.

For example, for the first stage, because of the high ac input voltage, a multilevel topology [11] or a three-cascaded H-bridge configuration can be used [12].

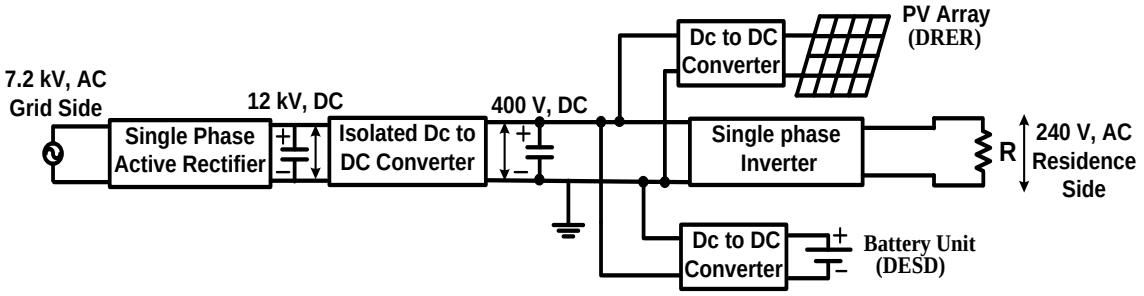

Fig. 3.1. SST overall schematic.

Fig. 3.2 shows the simplest possible detailed model for an SST, along with its basic control structure, including an H-bridge active rectifier followed by a single DAB as an isolated DC/DC converter, and an H-bridge inverter. As seen in Fig. 3.2, all three stages have closed loop control. These include conventional current-mode control in the d-q reference frame for the rectifier stage, a single voltage loop PI controller (VLC) for the isolated DC/DC stage, and average current mode control with a sinusoidal

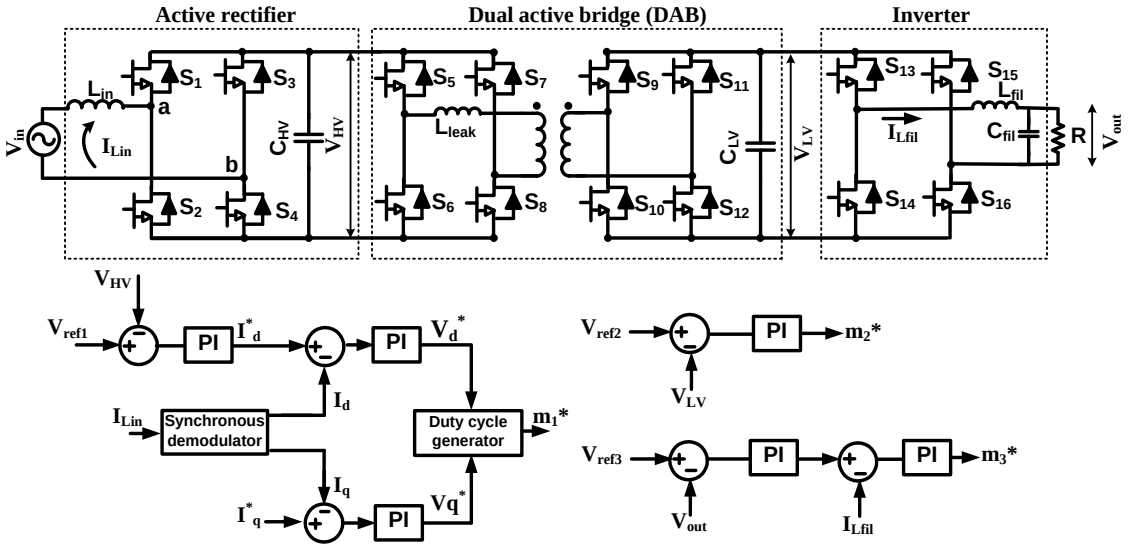

Fig. 3.2. Detailed model of SST along with basic control structure.

voltage reference for the inverter stage. In this figure, V_{ref1}, V_{ref2}, V_{ref3} and m_1^*, m_2^*, m_3^*, are, respectively, the commanded voltage references and commanded modulating waveforms for the rectifier, DAB, and inverter stages.

To better understand how the SST performs, let us review its general operation under a power scenario as an example. First, for the sake of simplicity, some power scenario nomenclature is defined as follows: $\pm P_{gs}$ -- The amount of power that is sent to the SST from the grid (+) or sent to the grid from the SST (-); $\pm P_{st}$ -- The amount of power received by the DESD (+) or sent to the SST from the DESD (-); P_{load} -- The total power received by the load. In general, the SST user commands the DESD power, and then the power drawn from grid must meet the following load power requirement:

$$P_{gs} = P_{st} + P_{load}. \tag{1}$$

Now as an example, a power scenario (SC1) is introduced as:

$$SC1: P_{gs} = 20KW, P_{st} = 0KW, P_{load} = 20KW \tag{2}$$

In SC1, the commanded power for the DESD is 0 kW, so from (1) the power required from the grid to meet the load requirement would be 20 kW. Along with the power balance requirement, the SST control must regulate the HV and LV links and guarantee unity power factor on the grid side. Note that the regulation of both DC links is crucial; that is why regulation in these links will be analyzed in this paper as a measure of SST stability. Table 3.1 shows the SST parameters. All the simulations in this paper are based on the SST with these parameters.

Table 3.1. SST Parameters.

Rectifier	
Input Voltage, Vin (RMS)	7.2 kV
Input Filter Inductance, Lin	300 mH
HV link capacitor CHV	250 uF
Switching Frequency	5 kHz
I_d Current Controller Integral Gain	10
I_d Current Controller Proportional Gain	.3
I_q Current Controller Integral Gain	10
I_q Current Controller Proportional Gain	.3
Voltage Controller Integral Gain	.1
Voltage Controller Proportional Gain	.001
DAB	
Transformer Turns Ratio	30
LV Link Capacitor	6 mF
Leakage inductance, L_{leak}	1.11 uH
DAB Switching Frequency, f	10 kHz
Voltage Controller Integral Gain	.0125
Voltage Controller Proportional Gain	.0005
Inverter	
Output Filter Inductance	4 mH
Output Filter Capacitance	500 uF
Switching Frequency	15 kHz
Current Controller Integral Gain	10000
Current Controller Proportional Gain	20
Voltage Controller Integral Gain	1000
Voltage Controller Proportional Gain	2
DC/DC Boost Interface	
Inductance	20 mH
Switching Frequency	15 kHz
Current Controller Integral Gain	10
Current Controller Proportional Gain	.3

The detailed SST model in Fig. 3.2 was simulated using Piecewise Linear Electrical Circuit Simulation (PLECS). Fig. 3.3 shows the key waveforms of SST for SC1. In this figure, plots *a*, *b*, and *c*, respectively, depict the SST input voltage, output dc voltage of the rectifier (HV link) and SST input current. Plot *d* shows the output voltage

of the DAB (LV link), and plots *e* and *f*, respectively, show the inverter output voltage and current.

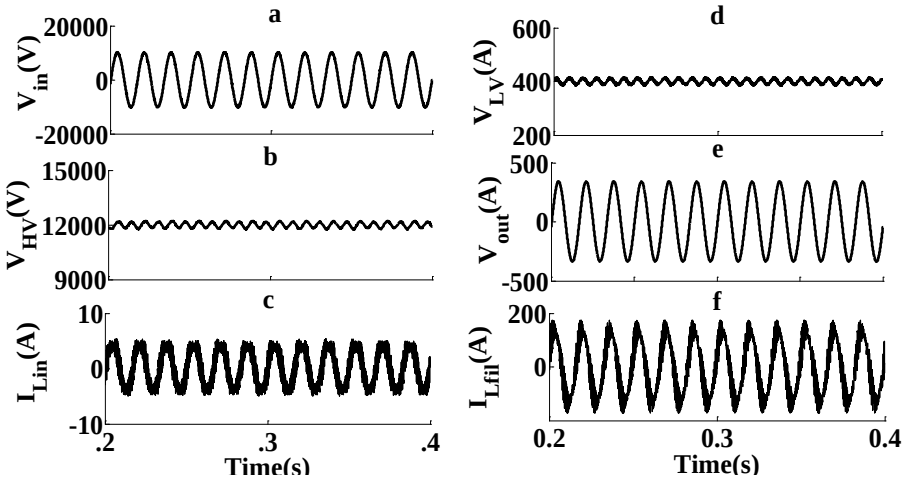

Fig. 3.3. Simulation results for SST under normal operation.

In order to conduct a stability analysis and time domain simulation, in this paper, the average SST model is used rather than the detailed model. Also, Matlab and Computer Aided Design software (PSCAD) are used for the frequency domain and time domain analyses, respectively. Obviously, using the average model and PSCAD (instead of PLECS) eases the long time-domain simulation.

3.3. SST SMALL SIGNAL MODELLING

As mentioned, to analysis the stability, the input and output impedance transfer functions of the system are needed. Fig. 3.4 shows these transfer functions and the physical point that each of these transfer functions must be derived. $Z_{o.rec}$, $Z_{in.DAB}$, $Z_{o.DAB}$, $Z_{in.inv}$ and $Z_{in.st}$ are the rectifier output impedance, DAB input impedance, DAB output impedance, inverter input impedance and storage unit input impedance respectively. As seen, Fig. 3.4 does not include the PV and its interface. Actually, as will be explained

later both storage and PV have the same effect on stability and that is why just one of them is considered here for the sake of simplicity.

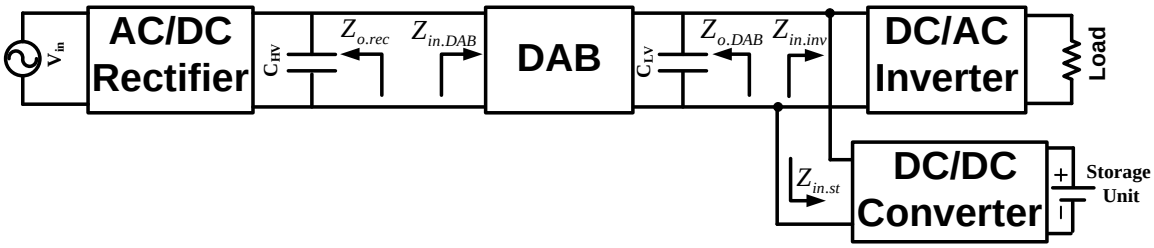

Fig. 3.4. Input and output transfer functions identification diagram.

In this section, small signal models for each stage in the SST are presented based on the converters' average models. Then, input and output impedance transfer functions will be derived based on the small signal models. In the next sections, these transfer functions will be used to study the SST's stability based on the Middlebrook stability criteria.

3.3.1. AC/DC Rectifier: The first stage is the AC/DC rectifier under d-q reference frame current mode control. Fig. 3.5 shows the average model of the rectifier in the d-q reference frame [13]. In this figure, V_m is the peak input voltage of the SST, ω_0 is the line frequency, v_d, v_q, i_d, i_q are, respectively, d, q reference frame values of the v_{ab} voltage and inductor current L_{in} (see Fig. 3.2). Also, P is defined as:

$$P = \frac{v_d i_d + v_q i_q}{2} \tag{3}$$

In [14], it has been shown that in unity power factor systems such as SSTs, the q-axis parameters and their effects on the d axis can be neglected. That is, the system in Fig. 3.5 can be approximated by a simple modified boost converter under average current

mode control. For the sake of simplicity, this approximation will be used here to model this system.

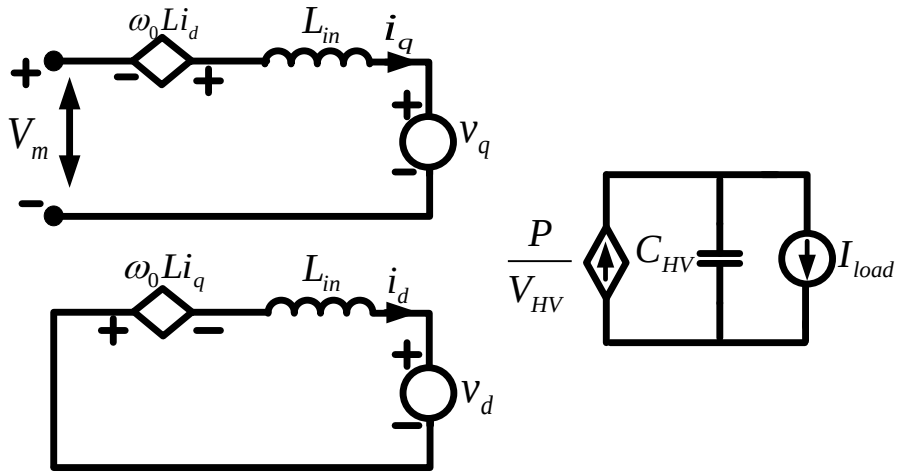

Fig. 3.5. Average model of rectifier in q-d reference frame.

Fig. 3.6 shows the small signal model of the simplified rectifier model. In this figure, D_d and I_d are the boost converter duty cycle and the operating point d-axis current, respectively [13]. $\hat{d}_d$, $\hat{v}_m$ and $\hat{i}_o$ are introduced as the perturbation in the duty cycle, the peak value of the ac input voltage and the output current source, respectively. $G_{v.rec}$ and $G_{id.rec}$ are VLC and the d-axis current loop controller (CLC), respectively. Fig. 3.7 shows the control block diagram of this system. The transfer functions used in this block diagram are defined in Table 3.2. Actually, these are the open loop transfer functions. That is, they have been evaluated when there is no feedback and only one input at the time is considered.

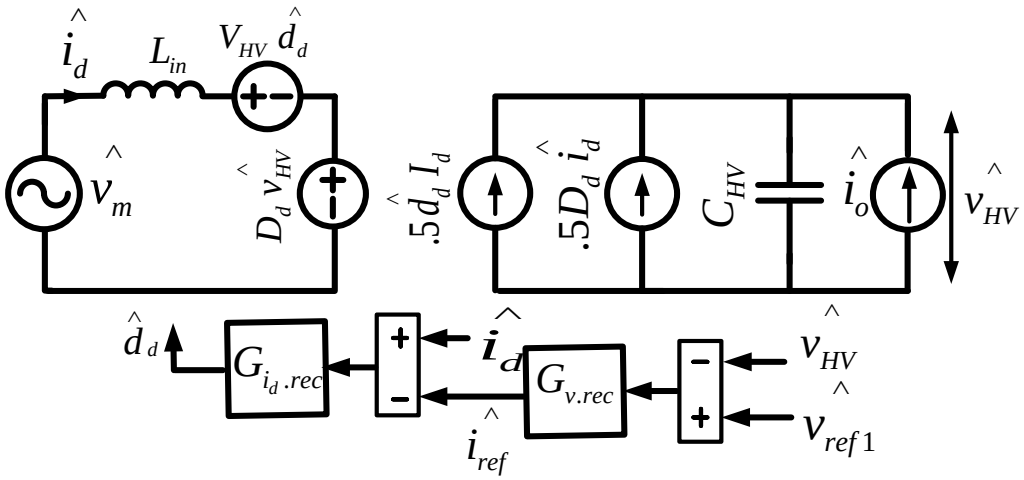

Fig. 3.6. Simplified rectifier small signal model.

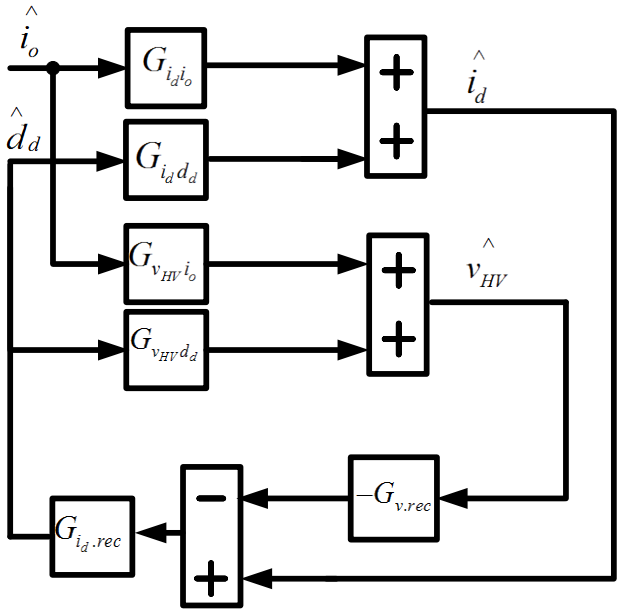

Fig. 3.7. Control block diagram model of the rectifier.

Table 3.2. Open Loop Transfer Functions for Rectifier, Inverter and DC/DC Boost.

AC/DC	$G_{i_d i_o} = \frac{-2}{D_d}\frac{1}{L_{in}C_{HV}/D_d^2 s^2+1}, G_{i_d d_d} = -\frac{I_d}{D_d}\frac{2V_{HV}/(I_d D_d)s+1}{L_{in}C_{HV}/D_d^2 s^2+1},$ $G_{v_{HV} i_o} = \frac{1}{D_d^2}\frac{L_{in}s}{L_{in}C_{HV}/D_d^2 s^2+1}, G_{v_{HV} d_d} = \frac{V_{HV}}{D_d}\frac{.5L_{in}I_d/(D_d V_{HV})s-1}{L_{in}C_{HV}/D_d^2 s^2+1}$
DC/AC	$G_{i_{L_{fil}} v_{LV}} = \frac{D}{R}\frac{RC_{fil}s+1}{L_{fil}C_{fil}s^2+L_{fil}s/R+1}, G_{i_{in} d} = I_{fil}+\frac{V_{LV}D}{R}\frac{RC_{fil}s+1}{L_{fil}C_{fil}s^2+L_{fil}s/R+1}, G_{v_{out} v_{LV}} = \frac{D}{L_{fil}C_{fil}s^2+L_{fil}s/R+1}$ $G_{i_{in} v_{LV}} = \frac{D^2}{R}\frac{RC_{fil}s+1}{L_{fil}C_{fil}s^2+L_{fil}s/R+1}, G_{i_{L_{fil}} d} = \frac{V_{LV}}{R}\frac{RC_{fil}s+1}{L_{fil}C_{fil}s^2+L_{fil}s/R+1}, G_{v_{out} d} = \frac{V_{LV}}{L_{fil}C_{fil}s^2+L_{fil}s/R+1}$
DC/DC	$G_{i_{in} v_{LV}} = \frac{D^{'2}}{L_{st}s}, G_{i_{Lst} v_{LV}} = \frac{-1}{L_{st}s}, G_{i_{Lst} d} = \frac{V_{LV}}{L_{st}s}, G_{i_{in} d} = I_{Lst}-\frac{D^{'}V_{LV}}{L_{st}s}$

Considering Fig. 3.7 and from basic control theory, the closed loop output impedance of this system can be defined as in (4).

$$Z_{o.rec} = \frac{\hat{v}_{HV}}{\hat{i}_o} = \frac{G_{v_{HV} i_o}(1-G_{i_d .rec}G_{i_d d_d})+G_{i_d i_o}G_{i_d .rec}G_{v_{HV} d_d}}{1-G_{i_d .rec}G_{i_d d_d}-G_{v.rec}G_{i_d .rec}G_{v_{HV} d_d}}. \quad (4)$$

3.3.2. DAB: The second stage is the DAB, whose characteristics and models have been discussed in [15, 17]. The simplest DAB model is depicted in Fig. 3.8. As seen, the primary and secondary sides of the DAB both behave as a controllable current source in which:

$$I_{HV} = \alpha V_{LV}\varphi(1-|\varphi|) \quad (5)$$

$$I_{LV} = \alpha V_{HV}\varphi(1-|\varphi|) \quad (6)$$

$$\alpha = \frac{1}{2fL_{leak}} \quad (7)$$

Where f and L_{leak} are the DAB switching frequency and the transformer leakage inductance, respectively. In (5) and (6), φ is the DAB normalized phase shift, which is:

$$\varphi = \frac{\pm DAB\ Control\ Pase\ Shift}{\pi}, \quad \varphi \in [-.5, .5] \quad (8)$$

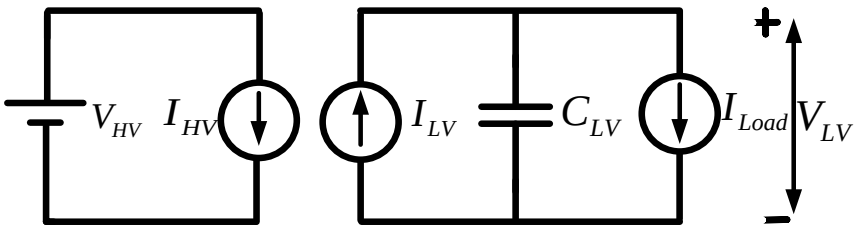

Fig. 3.8. DAB average model.

Based on the average DAB model and small signal linearization, one can propose the DAB small signal model depicted in Fig. 3.9. In this model:

$$\hat{i}_{HV} = \beta \hat{v}_{LV} + \lambda V_{LV} \hat{\varphi} \tag{9}$$

$$\hat{i}_{LV} = \beta \hat{v}_{HV} + \lambda V_{HV} \hat{\varphi} \tag{10}$$

where

$$\beta = \alpha\varphi(1 - |\varphi|) \tag{11}$$

$$\lambda = \alpha(1 - 2|\varphi|) \tag{12}$$

and $G_{v.DAB}$ is the DAB VLC.

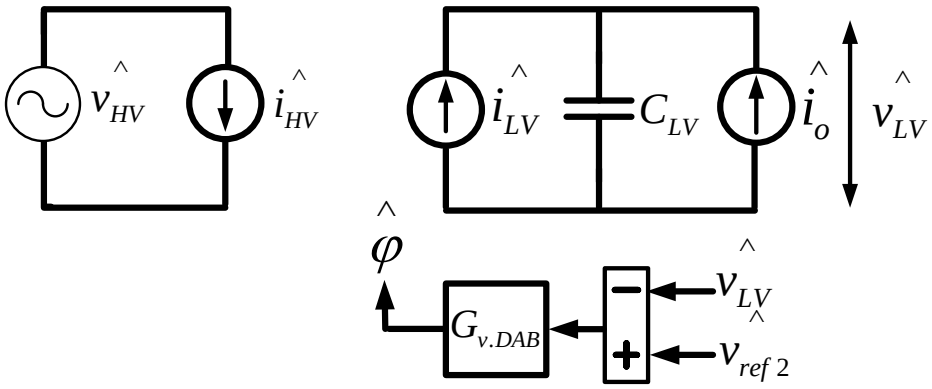

Fig. 3.9. Simplified DAB small signal model.

Based on the model in Fig. 3.9, the DAB control block diagram can be depicted as in Fig. 3.10. Note that when the input impedance of the DAB is calculated, the input impedance of any PE connected to the DAB output must be considered as the DAB load and be reflected in the equation. However, when the output impedance of the DAB is

calculated, the effect of the first stage (rectifier stage) can be neglected because the first stage only affects the DAB small signal model by introducing the HV link perturbation. However, a large HV capacitor value would make this variation negligible.

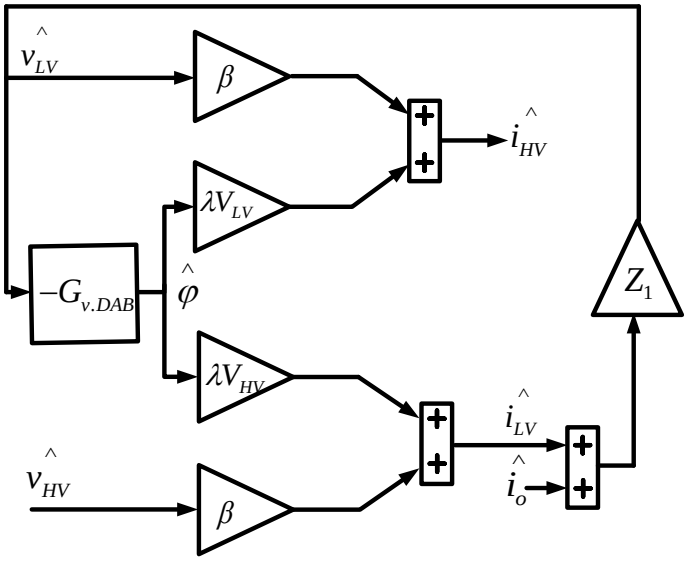

Fig. 3.10. Control block diagram for DAB.

Now, using the block diagram in Fig. 3.10, the input and output impedance of the DAB are obtained as in (13) and (15), respectively, as follows:

$$Z_{in.DAB} = \frac{\hat{v}_{HV}}{\hat{i}_{HV}} = \frac{1 + Z_1 G_{v.DAB} \lambda V_{HV}}{\beta^2 Z_1 - \beta Z_1 G_{v.DAB} \lambda V_{LV}} \tag{13}$$

$$Z_1(s) = \begin{cases} Z_{L.EQ}(s \simeq 0) \| Z_{c_{LV}} & s \le Bw.DAB \\ Z_{c_{LV}} & s > Bw.DAB \end{cases} \tag{14}$$

$$Z_{o.DAB} = \frac{\hat{v}_{LV}}{\hat{i}_o} = \frac{Z_{c_{LV}}}{1 + Z_{c_{LV}} G_{v.DAB} \lambda V_{HV}} \tag{15}$$

where $Z_{c.Lv}$ is the impedance of the DAB output capacitor, *Bw.DAB* is the bandwidth of the DAB, which can be obtained from (13), and $Z_{L.EQ}$ is the equivalent DAB load impedance seen from the LV link. Actually, it is the input impedance of the inverter ($Z_{in.inv}$), and storage unit ($Z_{in.st}$) in parallel as shown in Fig. 3.4. To calculate Z_1, $Z_{L.EQ}$ has

been evaluated at a very low frequency in (14). This eliminates the high-order transfer function, which can be obtained as an equivalent load impedance if the main transfer functions of $Z_{in.inv}$ and $Z_{in.st}$ were used. This approximation does not cause any problems. In fact, as will be shown in the next sections, only the low frequency range is important for the input impedance when it is compared to the output impedance.

3.3.3. DC/AC Inverter: The third stage is the DC/AC inverter. The average model of such an inverter can be presented by considering it as a simple DC/DC buck converter [10]. Fig. 3.11 shows the small signal model of the inverter by assuming it as a buck converter under average current mode control. As mentioned previously, the voltage reference of the inverter VLC is a sinusoidal voltage waveform. Hence, the presented small signal model has been derived by considering the perturbation frequency higher than the reference voltage waveform frequency, which is 60 Hz. Fig. 3.12 shows the control block diagram of the model in Fig. 3.11. The introduced transfer functions in Fig. 3.12 have been reported in Table 3.2. Now, to obtain the inverter input impedance using Fig. 3.12, one can write:

$$Z_{in.inv} = \frac{\hat{v}_{LV}}{\hat{i}_{in}} = \frac{1 + G_{i.inv}G_{i_{L_{fil}}d} + G_{v.inv}G_{i.inv}G_{v_{out}d}}{G_{i_{in}v_{LV}}(1 + G_{i.inv}G_{i_{L_{fil}}d} + G_{v.inv}G_{i.inv}G_{v_{out}d}) - G_{v_{out}v_{LV}}G_{v.inv}G_{i.inv}G_{i_{in}d}}. \quad (16)$$

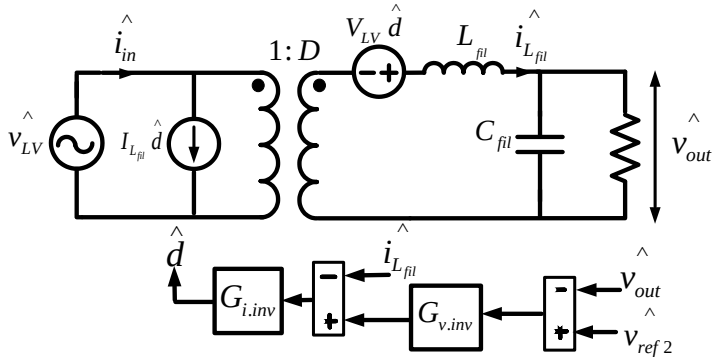

Fig. 3.11. Inverter small signal model.

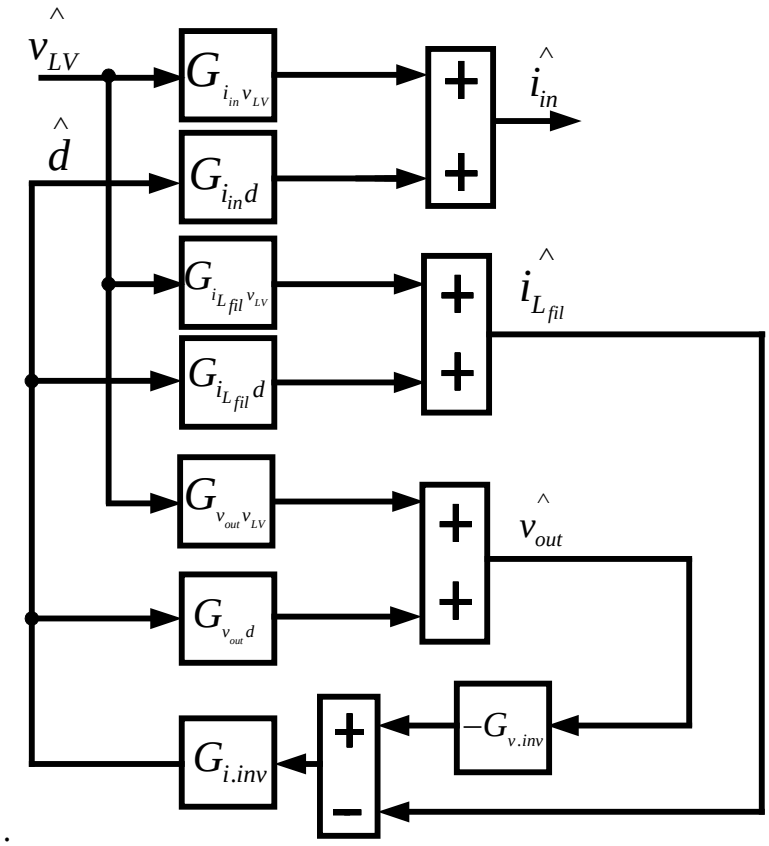

Fig. 3.12. Control block diagram for inverter.

3.3.4. DESD And DRER: As mentioned previously, one main advantage of an SST is that it can communicate with and be connected to DESDs and DRERs, such as PV, fuel cell, or storage units. These DC devices can be connected to the HV or LV links of the SST. Due to the lower voltage of the LV link, it is preferred and is studied here as the connection point of the SST and the DESD or DRER.

Adding these sources of energy makes the bidirectional power flow possible. However, these devices, along with their associated DC/DC converters, as seen in Fig. 3.1, will complicate the stability issue of the SST. In the next section, the stability effects of adding such sources will be addressed, and then whether or not the direction of power affects stability will be investigated. In this paper, a storage unit will be considered to

represent the effect of the DESD or DRER. This is because PV or fuel cells can only generate power while the battery can generate and absorb power; thus, it has the capability for bidirectional power flow. All the conclusions from the battery case study can be expanded easily for PVs and fuel cells, as well.

As previously mentioned, the stability issue arises because of the interaction of the converters; it does not depend on the internal battery model, such as the state of charge or internal resistance. Hence, here for the sake of simplicity, the battery is modeled by just a dc source, which is connected to the LV link using a DC/DC boost converter. The terminal voltage of the battery is assumed to be 200 V. The interface boost converter sends or receives power by directly commanding the inductor current of the boost converter using a simple PI CLC. The small signal model of such a boost converter is depicted in Fig. 3.13. L_{st} and D' are the boost converter inductor and duty cycle complement, respectively. $v\hat{}_{st}$ is the perturbation in battery terminal voltage and $G_{i.st}$ is the CLC. Note that though the C_{LV} voltage is assumed as this interface converter's output voltage, the C_{LV} is not a part of this model because C_{LV} is controlled by the DAB.

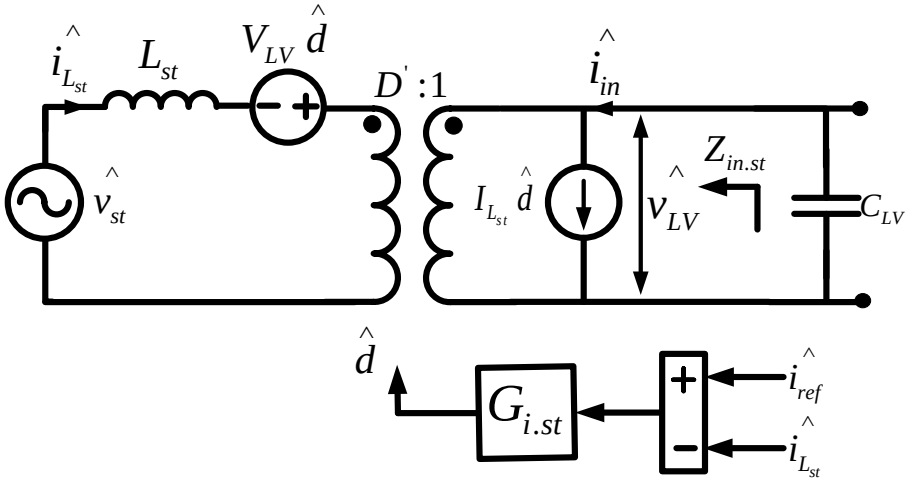

Fig. 3.13. Interface DC/DC boost converter model.

Now considering Fig. 3.13, the control block diagram of the interface DC/DC boost converter can be depicted as in Fig. 3. 14. Using this block diagram, the input impedance of the storage unit can be obtained as:

$$Z_{in.st} = \frac{1 + G_{i.inv} G_{i_L d}}{G_{i_{in} v_{LV}} (1 + G_{i.inv} G_{i_L d}) - G_{i_L v_{LV}} G_{i.inv} G_{i_{in} d}} \tag{17}$$

The transfer functions used in (17) are defined in Table 3.2.

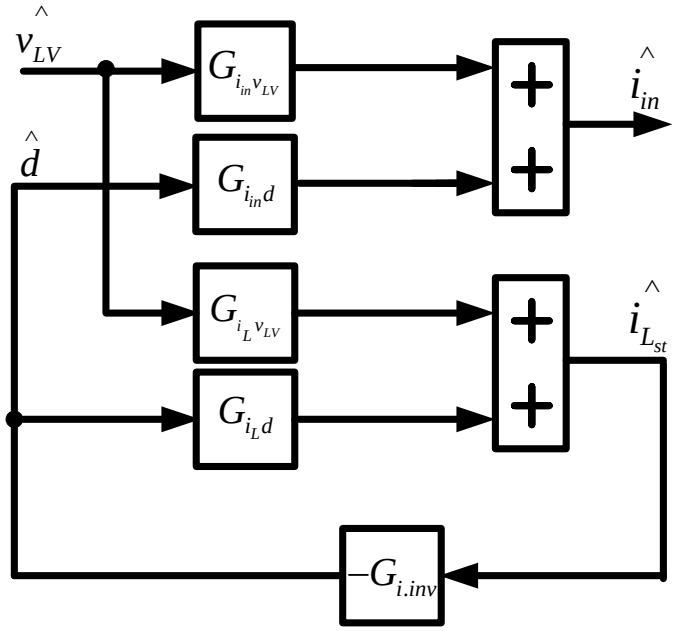

Fig. 3.14. Interface DC/DC boost converter.

Now that the necessary transfer functions have been derived, the stability analysis based on the Middlebrook criteria can be conducted. Two DC voltage links will be studied for bidirectional power flow, the HV link and then the LV link.

3.4. STABILITY DISCUSSION FOR HV LINK

In this section, the stability of the HV link is studied. As discussed in Section 3.1, the SST control sets this DC link voltage to 12,000 V. The goal is to see whether or not

the interaction of cascaded stages can destabilize this link and affect the regulation. For the first study, the following power scenario is considered:

$$\text{SC2}: P_{gs} = 15\ kW,\ P_{ss} = 0\ kW,\ P_{load} = 15\ kW \tag{18}$$

Based on the Middelbrook criteria, the input impedance of the DAB seen at the HV link must be larger than the output impedance of the rectifier:

$$Z_{o.rec} \ll Z_{in.DAB} \tag{19}$$

In fact, a smaller output impedance or larger input impedance offers a greater stability margin. The equations for $Z_{o.rec}$ and $Z_{in.DAB}$ are expressed in (4) and (13), respectively. As discussed in previous sections, to calculate $Z_{in.DAB}$, the equivalent DAB load impedance, $Z_{L.EQ}$, at low frequencies must be evaluated first. To do so one can write:

$$Z_{L.EQ}(s \simeq 0) = Z_{in.inv}(s \simeq 0) \| Z_{in.st}(s \simeq 0) \tag{20}$$

Equation (20) can be evaluated using (16) and (17) or obtained using the following power information:

$$Z_{L.EQ}(s \simeq 0) = \frac{-V^2_{LV}}{P_{ss} + P_{load}}. \tag{21}$$

The magnitudes of the $Z_{o.rec}$, $Z_{in.DAB}$ transfer functions have been depicted in Fig. 3.15 for SC2. As Fig. 3.15 reveals, (19) has been satisfied. Fig. 3.16 shows SST time domain simulation for SC2. As seen, the input current and input voltage are in phase, and the SST input current peak is nearly 3 amperes, which corresponds to SC2. The HV link voltage is stable and regulated, which validates the frequency domain results.

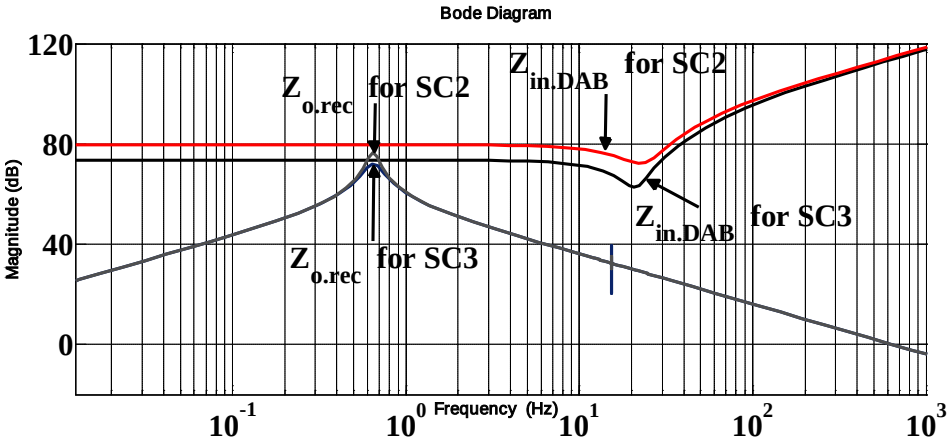

Fig. 3.15. Bode plot for HV link stability analysis for both SC2 and SC3.

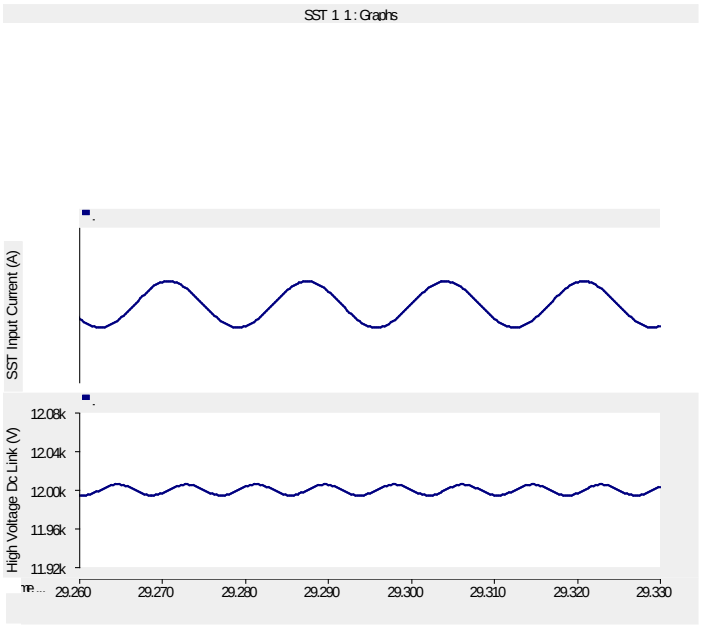

Fig. 3.16. Time domain simulation result for SC2.

3.4.1. Effect of Load Value On HV Link Stability: One important factor that affects the $Z_{in.DAB}$ is the load value. The $Z_{o.rec}$ is affected by both the VLC design and load. It is possible that a load increase could destabilize the system by reducing the magnitude of $Z_{in.DAB}$. To study this condition, let us investigate the following scenario:

$$\text{SC3}: P_{gs} = 30\ kW,\ P_{ss} = 10\ kW,\ P_{load} = 20\ kW \tag{22}$$

As seen, the load in SC3 has been doubled compared with that of SC2. Fig. 3.15 shows the frequency domain result for SC3. Clearly, there is still a sufficient stability margin. In fact, increasing the SST load will decrease the magnitude of the input and output impedance with nearly the same ratio; that is why increasing the load will not destabilize the HV link. Fig. 3.17 shows the time domain simulation for SC3. The time domain results validate the frequency domain analysis, and similar to SC2, the HV link voltage is stable and regulated.

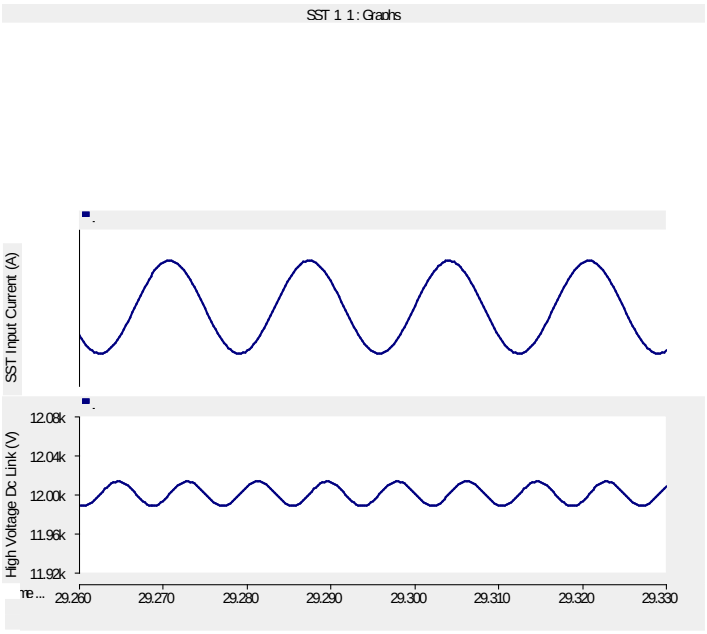

Fig. 3.17. Time domain simulation result for SC3.

Considering the rectifier small signal model in Fig. 3.6, one can explain why the $Z_{o.rec}$ decreases when the load increases. The characteristics of the output impedance in low frequency is dominated by the infinite gain of the PI VLC, and in high frequency by the low impedance of the capacitor. Increasing the load will boost the current operating point I_d in the small signal model so that the positions of the poles and zeros in the mid-band frequency change; consequently, the output impedance will decrease. A more physical reason for this issue can be expressed by considering the simple circuit equation

at the output of the model in Fig. 3.6. Considering this figure, the output impedance can be defined as in the following equation:

$$Z_{o.rec} = \frac{.5(\overbrace{\hat{d}_d\, I_d}^{a} + \overbrace{D_d\, \hat{i}_d}^{b}) - \hat{i}_{load}}{-\hat{i}_{load}} \tag{23}$$

Note that for better understanding of the issue $\hat{i}_o$ has been replaced by $\hat{i}_{load}$:

$$\hat{i}_{load} = -\hat{i}_o \tag{24}$$

In (23), to maintain positive power flow (PPF) mode, *a* and *b* must have opposite signs, and *b* must be dominant to be able to charge the capacitor. Clearly, higher power flow means larger I_d. Now, consider a situation with a +10% change of i_{load}. This means a positive $\hat{i}_d$ and negative $\hat{d}$. Clearly, a larger value of I_d yields a smaller result from the subtraction of *a* from *b*, and consequently a smaller numerator and output impedance, which is desirable.

3.4.2. Effect Of Power Flow Direction On HV Link Stability: Now, the stability in the reverse power flow (RPF) mode will be studied. The following power scenario is explored for this case study:

$$\text{SC4}: P_{gs} = -30\ kW,\ P_{ss} = -50\ kW,\ P_{load} = 20\ kW \tag{25}$$

The amount of power that the rectifier and DAB are processing in SC4 is equal to SC3 in magnitude, but in RPF mode. The RPF mode does not affect the $Z_{in.DAB}$ because the input impedance is only affected by the magnitude of the load and not its direction.

However, the RPF model will affect $Z_{o.rec}$. Actually, the change of the current sign will alter the poles and zero positions in the mid-band frequency range, as seen in

Fig. 3.18. More physical insight to explain such an increase in the output impedance for the RPF can be obtained using (23) and (24). In contrast to the PPF mode case, *a* and *b* have the same sign and reinforce each other's effect. Clearly, this leads to a larger nominator and larger output impedance. This increase in the output impedance is not desirable and, as seen in Fig. 3.18, will violate the stability condition in (19). Fig. 3.19 shows the time domain simulation for SC4. As seen, the HV link and input current waveforms are unstable, as predicted by the frequency domain results.

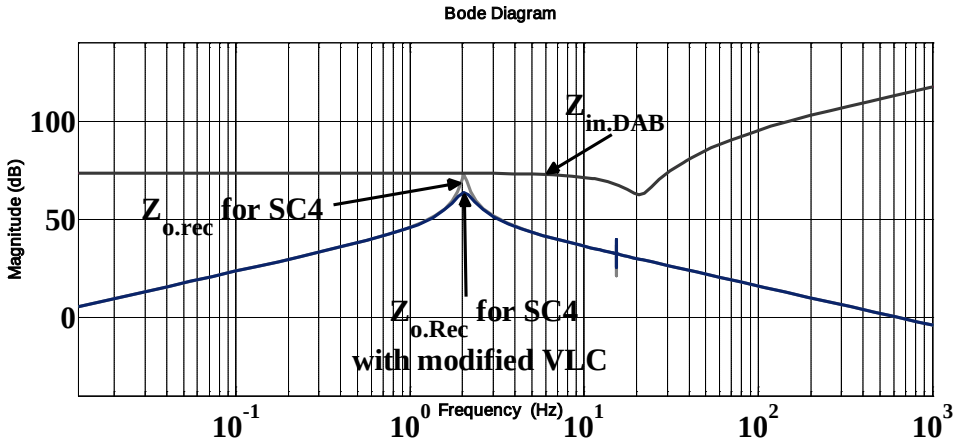

Fig. 3.18. Bode plot for HV link stability analysis for SC4.

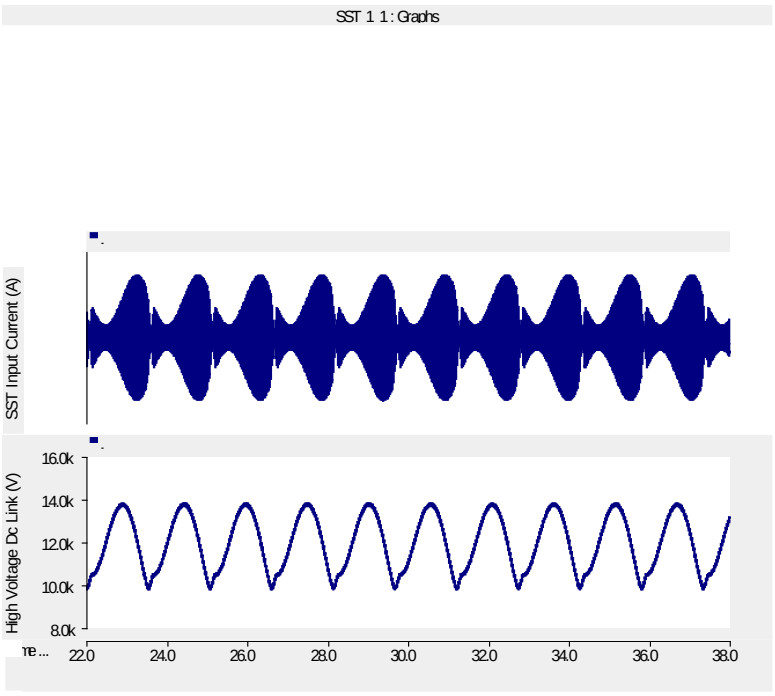

Fig. 3.19. Time domain simulation result for SC4.

In contrast to the input impedance, the output impedance is highly affected by the control parameters of both CLC and VLC. However, the effect of VLC is much more dominant than that of CLC. The SST for the SC4 case can be stabilized by modifying the parameters of the VLC of rectifier. These values have been reported in Table 3.1. Both integral and proportional gains can be modified. Here, proportional gain is doubled, and integral gain remains constant. The modified frequency domain results can be seen in Fig. 3.18. Obviously, $Z_{o.rec}$ has been reduced to allow for a greater stability margin. Note that $Z_{in.DAB}$ has not changed because no modification has been introduced for the DAB side. Fig. 3.20 shows the time domain result for SC4 with a modified VLC. A comparison of Fig. 3.20 with the results in Fig. 3.19 reveals how successfully the VLC modification can stabilize the HV link in the SST.

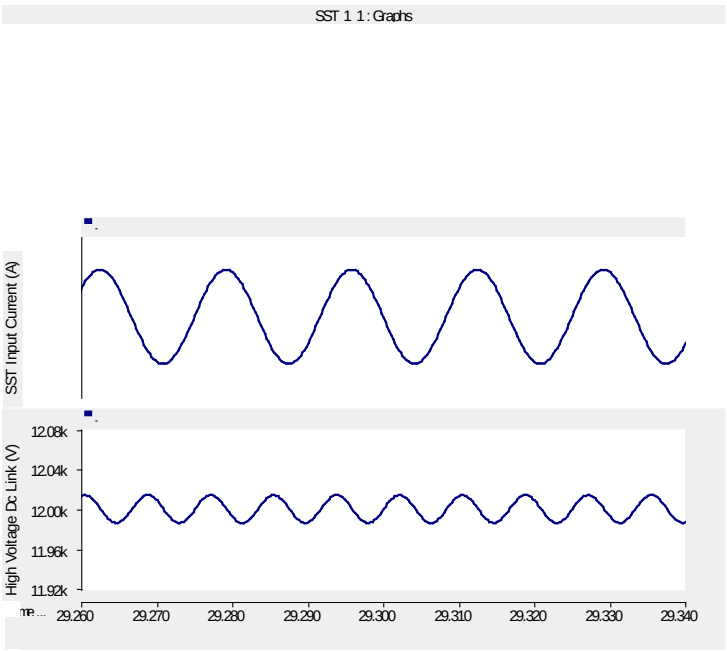

Fig. 3.20. Time domain simulation result for SC4 with modified VLC.

3.5. STABILITY DISCUSSION FOR LV LINK

Studying the LV link will be more complicated due to the connection of the DESDs or DRER. As noted in Section 3.3, only one storage unit will be considered in this paper. In this case, three PE converters are connected to the LV link. For this study, the desired transfer functions are the output impedance of the DAB ($Z_{O.DAB}$) and the equivalent input impedance seen at LV link and is equal to the parallel combination of the inverter and storage unit input impedances. This equivalent input impedance is named $Z_{in.EQ}$ and can be obtained as:

$$Z_{in.EQ}(s) = \begin{cases} Z_{in.inv} \| Z_{in.st}(s \simeq 0) & s \leq Bw.inv \\ Z_{in.inv} & s > Bw.inv \end{cases} \quad (26)$$

Where *Bw.inv* is the inverter input impedance bandwidth, which can be derived using (16). From (17):

$$Z_{in.st}(s \simeq 0) = -\frac{V_{LV}}{D' I_{ref}} = -\frac{V_{LV}^2}{P_{st}} \quad (27)$$

I_{ref} and D' are the commanded inductor current and the complement of the duty cycle for the interface DC/DC boost converter of the storage unit, respectively. In fact, to calculate $Z_{in.EQ}$, $Z_{in.inv}$ from (16) is first evaluated, but then for the storage unit here, only the low frequency approximation is used to evaluate $Z_{in.EQ}$. The reason for this approximation has been explained in Section 3.3.

3.5.1. Effect Of Load Value On LV Stability: In Section 3.4, the dependency of HV link stability on the load value was studied. As seen, the load value increment will not destabilize the HV link. Now, the same study will be conducted to analyze the effect of the load for the LV link. A power scenario is defined as follows:

$$\text{SC5}: P_{gs} = +15\,kW,\ P_{st} = -5\,kW,\ P_{load} = 20\,kW \quad (28)$$

Fig. 3.21 shows the frequency domain analysis for SC5. Obviously, the system is predicted to be stable. The time domain simulation for SC5, as shown in Fig. 3.22, validates this result.

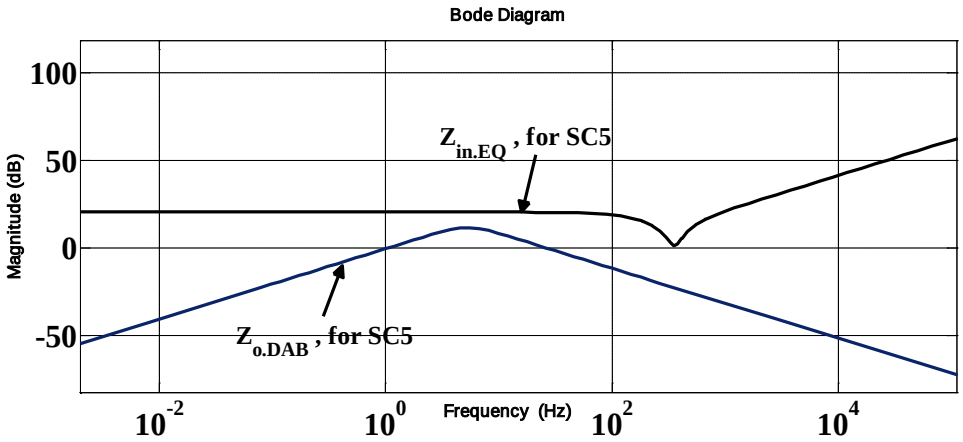

Fig. 3.21. Bode plot for LV link stability analysis for SC5.

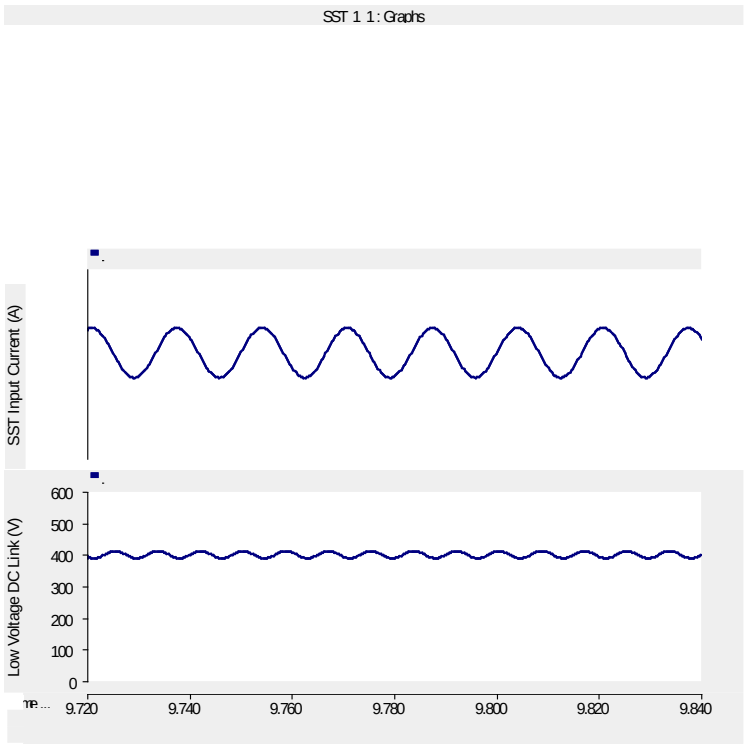

Fig. 3.22. Time domain simulation result for SC5.

Now the effect of the load value on stability is studied by introducing SC6 as:

$$\text{SC6}: P_{gs} = +30\ kW,\ P_{st} = +10\ kW,\ P_{load} = 20\ kW \tag{29}$$

As seen, the load in SC6 has been doubled compared with that of SC5. Fig. 3.23 shows the frequency domain analysis for SC6. As seen, there is no stability margin for SC6, and $Z_{O.DAB}$ nearly touches $Z_{in.EQ}$. This can explain the instability in the time domain simulation seen in Fig. 3.24. It contrasts the HV link case in which the load increment did not destabilize the system.

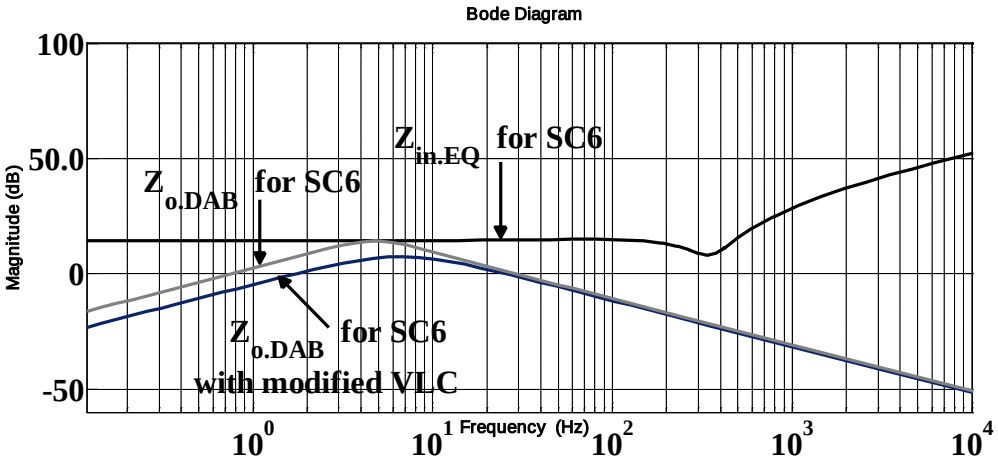

Fig. 3.23. Bode plot for LV link stability analysis for SC6.

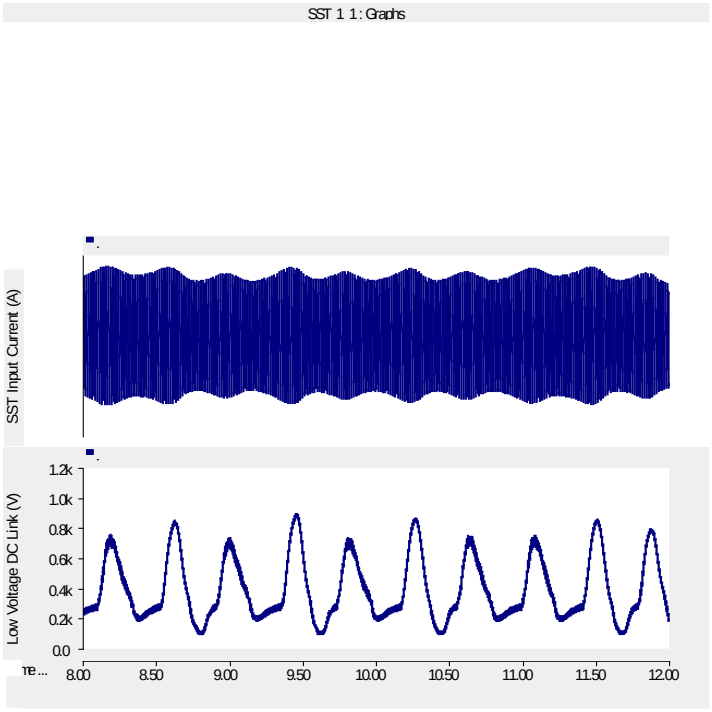

Fig. 3.24. Time domain simulation result for SC6.

This undesirable DAB characteristic occurs because, in contrast to the rectifier, the output impedance of the DAB will increase with the load increment. This is because the DAB has different characteristics than the rectifier, inverter or DC/DC boost interface. To clarify this issue, consider the power vs. control signal φ curve for the DAB in Fig. 3.25. As this figure indicates, as the output power increases, the slope decreases.

This means that for a specific amount of variation in the DAB output voltage that yields a proportional variation in control signal φ, the rate of current alteration will be less for a higher power rating. Obviously, this translates into a higher output impedance for a higher power rating.

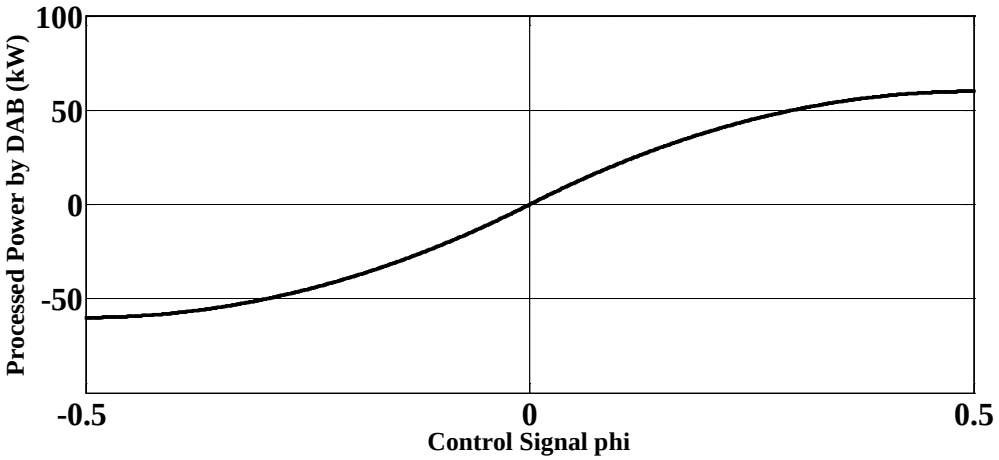

Fig. 3.25. Power vs. control signal curve for DAB.

To resolve this stability problem, $Z_{O.DAB}$ must be reduced in magnitude. The $Z_{O.DAB}$ is affected by the VLC and the DAB parameters. Clearly, the easiest way to modify $Z_{O.DAB}$ is to alter the VLC. Here, both integral and proportional gains of the VLC (which have been reported in Table 3.1) are doubled. Simply, this leads to a more dominant VLC and consequently less output impedance, as has been shown in Fig. 3.23. The resulted stability margin is sufficient to stabilize the LV link, as seen in Fig. 3.26.

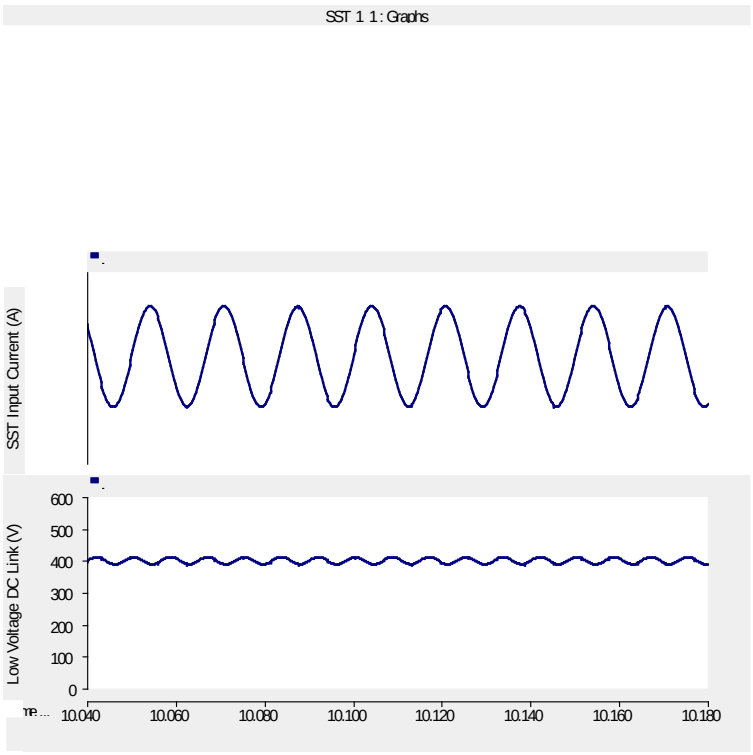

Fig. 3.26. Time domain simulation result for SC6 with modified VLC.

3.5.2. Effect Of Power Flow Direction On LV Link Stability: Another feature of the DAB that distinguishes between LV link stability and the HV link is the RPF mode characteristic. To better understand this issue, assume the following scenario:

$$\text{SC7}: P_{gs} = -30\ kW,\ P_{st} = -50\ kW,\ P_{load} = 20\ kW \tag{30}$$

The amount of power processed by the DAB for SC7 is equal to that of SC6 but with RPF. The resultant $Z_{O.DAB}$ for the DAB in RPF is equal to that shown in Fig. 3.23 for SC6 in PPF mode. The reason for this is clear considering the power vs. control signal curve for the DAB in Fig. 3.25. As seen in this figure, the curve is symmetrical. That is, for a specific value of power, whether positive or negative, the curve slope, which represents the current variation and, consequently, the output impedance, is the same. Hence, any conclusion that is true for a specific load value for LV link stability is valid for that amount of load in RPF mode, too. Fig. 3.27 shows the time domain simulation for SC7

with the same modified VLC as applied to SC6. As predicted, SC7 shows stable behavior similar to SC6 in Fig. 3.26.

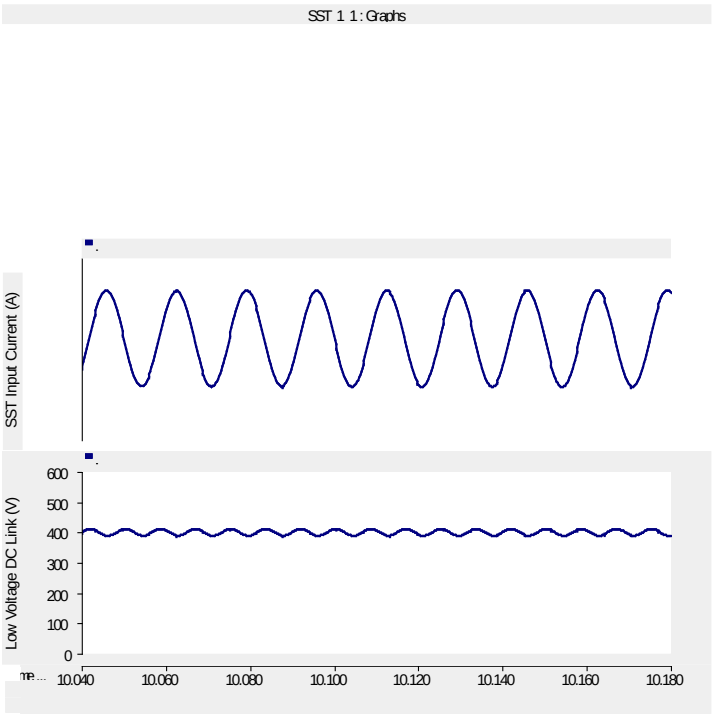

Fig. 3.27. Time domain simulation result for SC7 with modified VLC.

3.6. CONCLUSION

In this paper, SST stability issues originated by the interaction of cascaded converters have been studied, which can help control engineers to address the stability of such systems. First, small signal models for all stages of SST were derived, and then the desired impedance functions for each stage were developed. The impedance functions were applied to the Middlebrook stability analysis. Moreover, the effect of stability on the load value and power flow direction were studied. These sensitivity analyses help to achieve stable control design and increase the stability margin of the system for various load characteristics. The stability analysis method described in this paper is independent

of the direction of power. Hence, utilizing this method is easier and more practical for applications such as SST in which different power scenarios can be introduced.

3.7. REFERENCES

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SECTION

2. CONCLUSION

Some of the limitations and possible solutions related to CMC were discussed and investigated in this thesis. One of the main problem of CMC is sub-harmonic oscillation for $D>.5$. This problem can be solved by using ASC methods. Three ASC methods were explained through small signal analysis and experimental implementation. A PFC circuit was implemented in lab and it was shown how these methods can guarantee stability and improve dynamic response for the PFC. The predicted model of loop gain for three methods were obtained and validated by experimental small signal test. The small signal interpretation of the ASC methods confirm the mentioned characteristic of ASC methods.

As explained among the three discussed ASC methods, the third method can be assumed as, a new ACMC method. This method was called PCPC as mentioned in paper 2. Large signal and small signal behaviors of PCPC were analyzed. It was seen that PCPC method benefits from the advantages of both fix-frequency and variable frequency current-mode controllers. This controller is stable for the entire range of the duty cycle and the average value of the inductor current tracks the reference similar to the variable frequency current mode controller while this controller has the advantage of having constant frequency. The steady-state error, stability, and dynamic response issues were investigated using the small-signal model. It was shown that in the PCMC and ACMC approaches designers have to deal with a compromise between speed and stability, whereas in PCPC high speed and stability are guaranteed. Experimental results showed the proposed control performance and as seen the small signal model was validated using the measured data.

In paper 3, SST stability issues originated by the interaction of cascaded converters have been studied. This study can help control engineers to address the stability of such systems. First, small signal models for all stages of SST were derived, and then the desired impedance functions for each stage were developed. The impedance functions were applied to the Middlebrook stability analysis. Moreover, the effect of stability on the load value and power flow direction were studied. These sensitivity analyses help to achieve stable control design and increase the stability margin of the system for various load characteristics. The stability analysis method described in this paper is independent of the direction of power. Hence, utilizing this method is easier and more practical for applications such as SST in which different power scenarios can be introduced.

VITA

Mostafa Khazraei was born on September 3, 1983, in Darab, Fars, Iran. He received his B.S. degree in Electronics from the Khaje Nasir Toosi University, Tehran, Iran in 2005, In 2008 he received the M.S. degree in Electronics from the Iran University of Science and Technology, Tehran, Iran.

He began his research on power electronic in the electrical engineering department of the Missouri University of science and Technology in September 2008. He received his Ph.D. degree in Electrical engineering from the Missouri University of Science and Technology in August 2012.

He has published papers in reputable power Electronic IEEE conferences and journals. Some of which are listed with the references of this research. He has been a member of the Institute of Electrical and Electronics Engineers (IEEE) since 2009.