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Addressing control and capacitor voltage regulation challenges in multilevel power electronic converters

Hossein Sepahvand

Department: Electrical and Computer Engineering

ADDRESSING CONTROL AND CAPACITOR VOLTAGE REGULATION CHALLENGES IN MULTILEVEL POWER ELECTRONIC CONVERTERS

by

HOSSEIN SEPAHVAND

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Approved by

Mehdi Ferdowsi, Advisor

Keith A. Corzine, Advisor

Jonathan W. Kimball

Mariesa L. Crow

Robert G. Landers

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This dissertation consists of the following three articles:

Paper I, Pages 16-49, "Investigation on Capacitor Voltage Regulation in Cascaded H-bridge Multilevel Converters with Fundamental Frequency Switching," published in *IEEE Transactions on Industrial Electronics,* 2011.

Paper II, Pages 50-87, "Start-up Procedure and Switching Losses Reduction for a Single-Phase Flying Capacitor Active Rectifier," accepted for publication in *IEEE Transactions on Industrial Electronics.*

Paper III, Pages 88-108, "A Flexible Capacitor Voltage Regulation Method for Hybrid Multilevel Power Electronic Inverters," submitted to *IEEE Transactions on Industrial Electronics.*

ABSTRACT

Multilevel power electronic converters are the current industry solutions for applications that demand medium voltage, reasonable efficiency, and high power quality. The proper operation of these types of power converters requires special control, modulation methods, and capacitor voltage regulation techniques. Both developing capacitor voltage regulation methods and addressing their associated issues with such fall within the primary focus of this dissertation.

In this dissertation an investigation was conducted on the capacitor voltage regulation constraints in cascaded H-bridge multilevel converters with a staircase output voltage waveform. In the proposed method, the harmonic elimination technique is used to determine the switching angles. A constraint was then derived to identify modulation those indices that lead to voltage regulation of the capacitor. This constraint can be used in optimization problems for harmonic minimization to guarantee capacitor voltage regulation in these types of converters.

Furthermore, a capacitor voltage regulation method was developed using redundant state selection for a flying capacitor active rectifier. This method reduces the number of switching instances by using both online and offline state selection procedure. Additionally, a start-up procedure is proposed that pre-charges the all of capacitors in the rectifier to both avoid overstressing the switches and obtain a smoother start-up.

Finally, a flexible capacitor voltage regulation method is proposed that provides the ability to control the voltage of the capacitors in both cascaded H-bridge and hybrid multilevel converters. In this method, the capacitor voltage in each individual H-bridge cell is independently regulated by controlling the active power of each cell.

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1. INTRODUCTION

The implementation of a power electronic converter with conventional topologies is a challenging task for medium voltage applications due to the voltage limitation of the semiconductor power switches in industry [1-3]. Additionally, power quality improvement in conventional two-level converters is made possible by increasing the switching frequency. Doing so causes extensive switching losses and therefore impractical [4]. Multilevel power electronic converters were thus introduced to address these shortcomings [5, 6].

Multilevel power converters consist of several blocks of power switches and capacitors that help generate a stepped voltage in ac terminals. Using several steps in the output voltage allows inverters to reach to both higher voltages and improve the total harmonic distortion (THD). The primary advantages of multilevel converters over conventional converters include high voltage capabilities, high power quality, better electromagnetic compatibility (EMC), and lower switching losses [4, 5, 7].

Due to the nature of multilevel converters, however several structural challenges must be tackled. These challenges include the regulation of voltage of capacitors that are used for generating various voltage levels, more complex control due to the complexity of the topology when compared to conventional converters, and packaging issues (due to more elements in the converters). In addition, it is desirable to come up with ideas to be able to operate the converter while a fault has occurred in power stage. In this dissertation several methods are proposed to address issues with capacitor voltage regulation,

modulation techniques, operation after fault occurrence, and control complexity in multilevel power converters.

1.1. DIFFERENT TYPES OF MULTILEVEL CONVERTERS

Several converter topologies have been previously suggested by researchers. These topologies are categorized as multilevel converters. The primary multilevel power converter topologies include cascaded H-bridge, diode clamped, and flying capacitor converters [7]. Various types of multilevel converters are discussed in the following sections.

1.1.1. Cascaded H-bridge Multilevel Converters. A cascaded H-bridge converter consists of several H-bridge cells connected in a series to form one phase of the converter. Each H-bridge cell generates a three-level output voltage and requires a separate dc voltage source. For multiphase converters several cascaded H-bridges are used and each cascaded H-bridge makes one leg of the converter. Figure 1 illustrates a three-phase cascaded H-bridge multilevel converter. Each phase consists of two H-bridge and each H-bridge cell is supplied with an isolated voltage source.

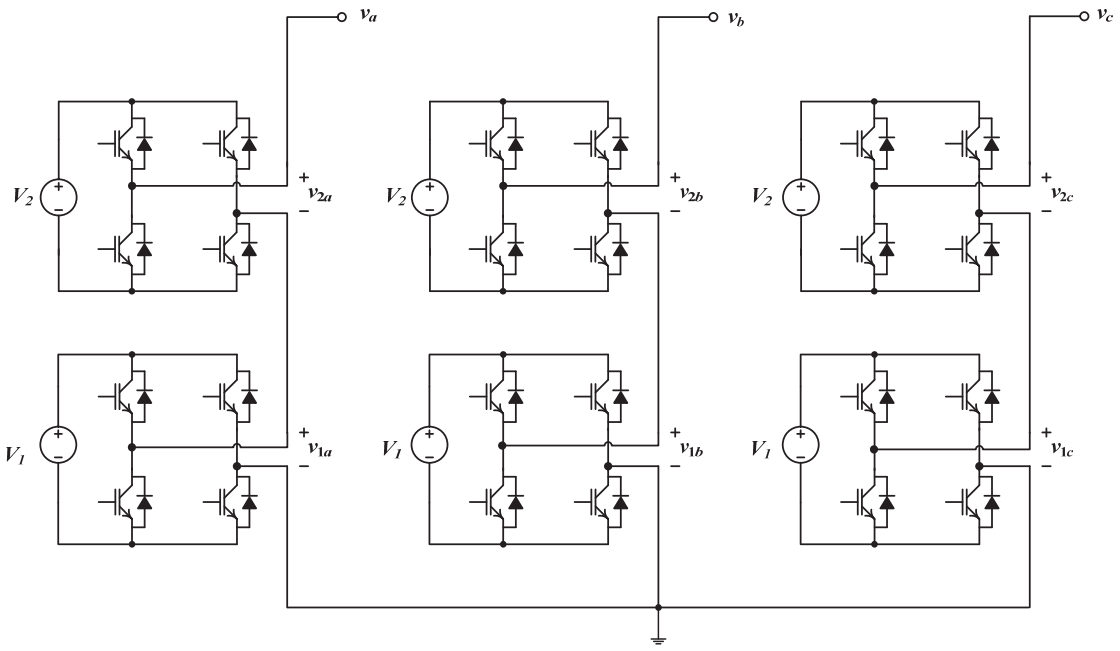

Figure 1. Three-Phase cascaded H-bridge converter.

It is possible, however to replace all of the dc voltage sources (in case more than two cells exist) with capacitors but one of them. In this case, only one dc voltage source is needed for each phase of the converter. A three-phase cascaded H-bridge with capacitor fed H-bridge cells is depicted in Figure 2. With this change the cost of converter decreases because a fewer number of isolated dc voltage sources are used especially when dc sources are supplied through ac/dc rectifiers. However the voltage of the replacing capacitors must be regulated to a certain voltage in order to have the required voltage level in the output voltage of the converter.

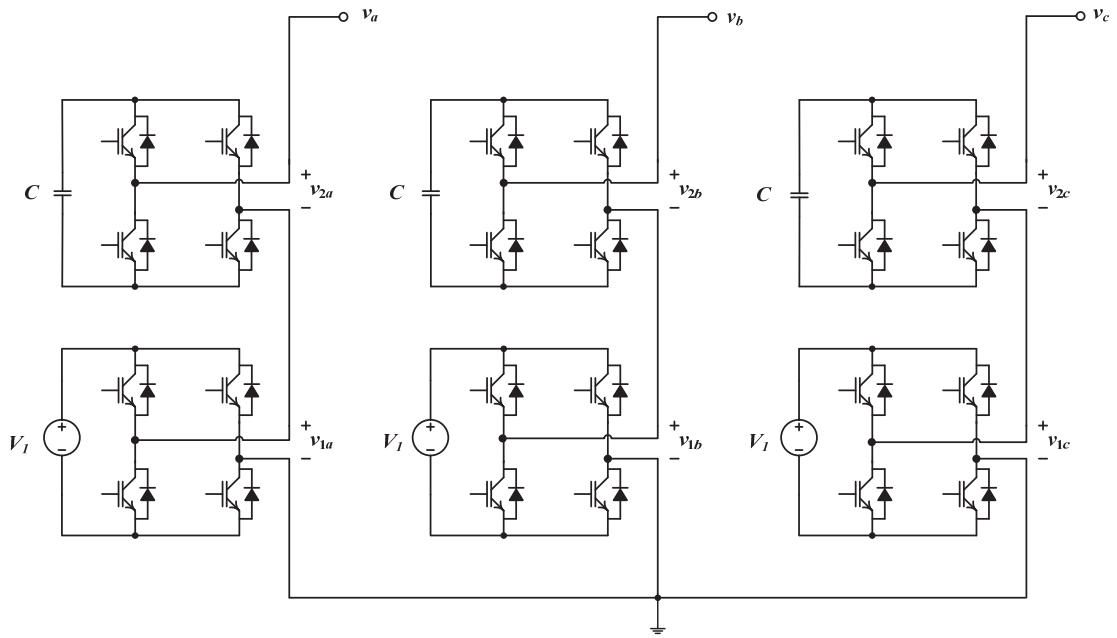

Figure 2. Three-phase cascaded H-bridge converter with capacitor fed H-bridge cells.

In this topology it is possible to use different modulation techniques [8, 9] so that each cell of the converter can have different switching frequencies. For example, in a two cell converter, one of the H-bridge cells can be switched at the fundamental switching frequency (one turned on and off per switch per cycle) while another one can be switched with pulse width modulation (PWM) switching scheme, at a higher frequency. Doing so helps reduce switching losses, especially when, the voltage sources and the power ratings of the cells are unequal [8-11].

1.1.2. Diode-clamped Multilevel Converters. In a diode-clamped multilevel converter topology, both cascaded capacitors and clamping diodes are used to generate several levels in the output voltage. Figure 3 illustrates a three-phase three-level diode

clamped converter (A three-level diode-clamped converter is also known as a neutral-point clamped (NPC) converter).

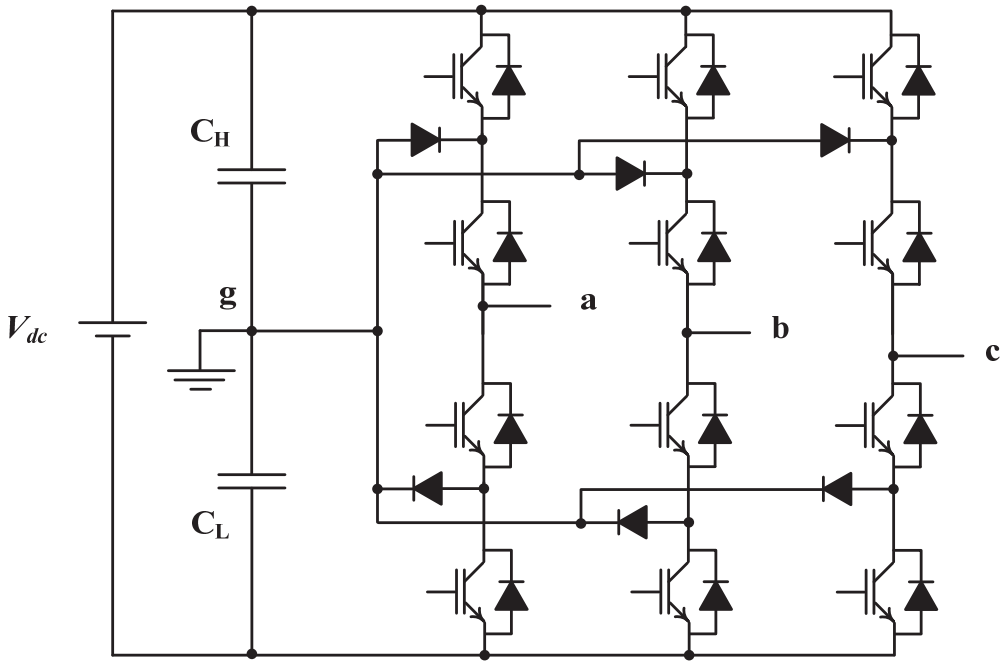

Figure 3. Three level diode-clamped converter or NPC.

In this topology, only one voltage source is needed. Additionally only one set of cascaded capacitors is used for all of the phases. This is one of the advantages of this topology. Either external converters are required or modified modulation strategies should be used to regulate the capacitors of a diode-clamped converter with more than three levels. Otherwise the capacitor voltage regulation is not always guaranteed under all of operation conditions [12-15]. Capacitor voltage regulation is possible without using any an external circuit for voltage balancing for NPC converters (three-level diode-

clamped converter). This is one of the reasons NPC is more popular than diode-clamped levels with more than three levels in industry applications [13].

1.1.3. Flying Capacitor Converters. A three-phase flying capacitor converter is illustrated in Figure 4. Unlike the diode-clamped converter, capacitors in this topology are not shared among different legs of the converter; each phase has its own set of capacitors.

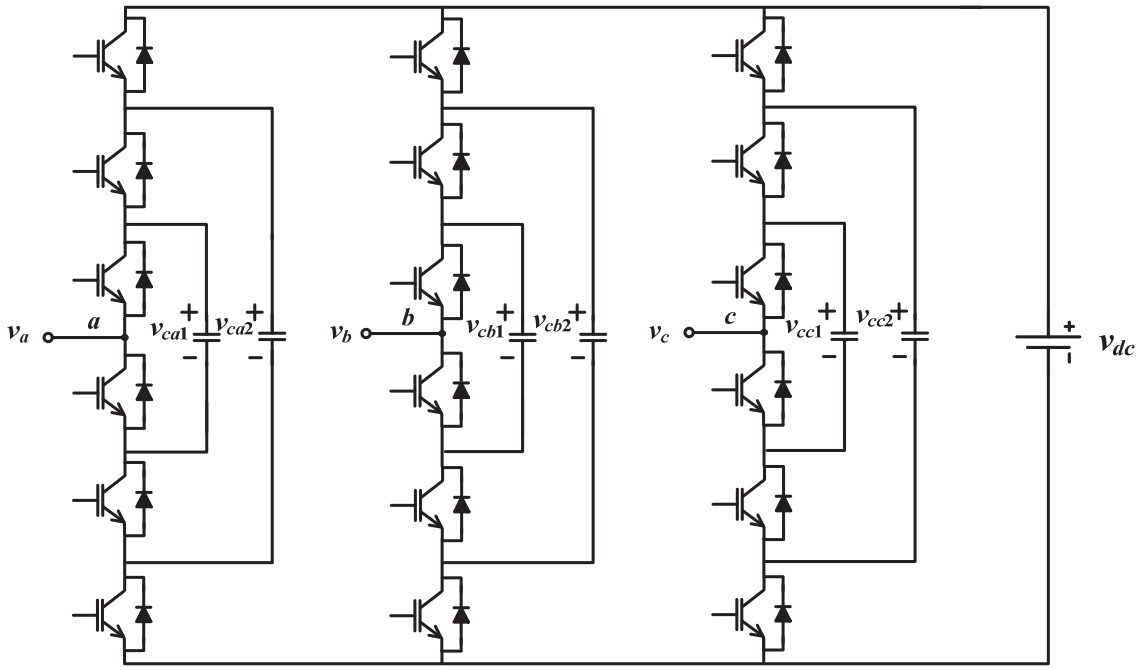

Figure 4. A three-phase flying capacitor inverter.

Regulation of capacitor voltages in this topology is possible without using an external circuit regardless of the number of levels of the converter. This is one of the advantages of this topology [16-19]. Because the voltage of the outer capacitors is higher than the inner ones, several capacitors need to be connected in a series to reach to the required voltage (the tolerable voltage for each capacitor bank). Therefore, the number of capacitors drastically increases when the number of voltage levels increases [4, 7]. Furthermore, the number of capacitors is proportional to the number of phases of the converter. This is one of the primary drawbacks of this topology.

1.1.4. Hybrid Multilevel Converters. In some applications, various types of multilevel converters are mixed to form a new type of multilevel converter in order to utilize the advantages of different topologies [20, 21]. For example, Figure 5 illustrates a hybrid converter that consists of a three-phase NPC with two H-bridge cells connected in a series with each leg of the NPC.

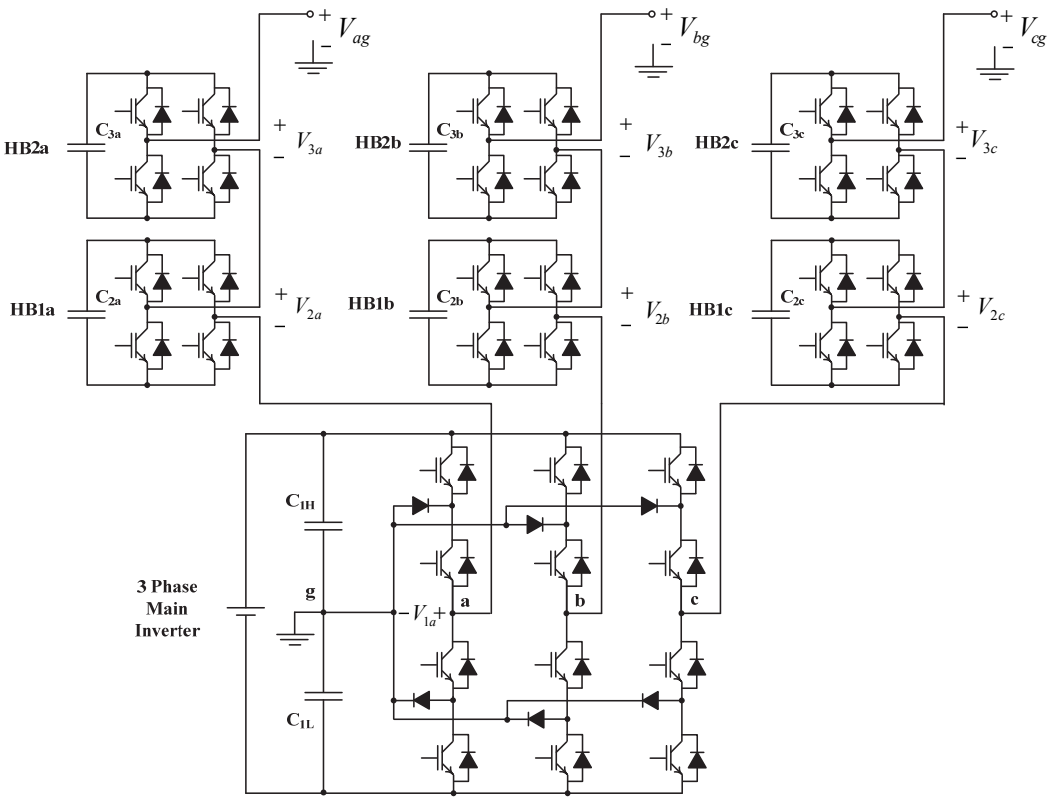

Figure 5. A three-phase, hybrid, multilevel converter.

As shown in Figure 5, the NPC is the main converter, and only one independent dc voltage source is used to supply all phases. In this topology it is possible to use different modulation techniques for different cells of the converter [8].

1.2. CONTROL AND CAPACITOR VOLTAGE REGULATION OF MULTILEVEL CONVERTERS

As mentioned in 1.1, both control and modulation methods of multilevel converter are more complicated than conventional converters due to a complex topology. Most of the standard control and modulation techniques however can be extended and successfully applied to multilevel converters [4, 5, 22]. Modulation methods used in

multilevel converters include selective harmonic elimination [9, 11, 23-31], nearest level control, level-shifted pulse width modulation (PWM) [17, 19, 32], phase-shifted PWM (PS-PWM) [32], and hybrid modulation techniques [4, 8-10].

Several capacitor voltage regulation methods have been proposed for various topologies and modulation techniques [5, 8, 18, 20, 24, 33-41]. Contributions of this dissertation in capacitor voltage regulation methods are described in the following sections.

1.2.1. Capacitor Voltage Regulation in Cascaded H-bridge Converters. As discussed in section 1.1.1, in cascaded H-bridge converters it is possible to replace all of the voltage sources that feed the H-bridge cells with capacitors except for one. Here, the H-bridge cell, which is connected to the dc source, is known as the main cell. The remaining cells are referred to as auxiliary cells.

In the staircase switching method (also known as the fundamental frequency modulation method), the switching instances occur at certain angles. The lower harmonics in the output voltage waveform of the inverter can be eliminated by choosing specific switching angles [42]. This can be accomplished by solving a set of nonlinear Fourier series equations for the output voltage waveform of the converter.

For a cascaded H-bridge converter with two H-bridge cells in each phase and in the case that voltage of the capacitor is regulated at half of the voltage of V_1 (see Figure 2) a seven-level output voltage waveform can be generated. The voltage of the capacitor in the auxiliary cell can be controlled by using redundant state selection method. In early works, the existence of redundant states was assumed enough for the regulation of the

capacitor in the auxiliary cell [29]. However based on the study presented in Paper I of this dissertation, it is shown that the voltage regulation of the capacitor is not possible in all load conditions and modulation indices [24]. In conducted research presented in Paper I, a range of modulation indices are found in which capacitor voltage regulation is possible for different types of loads. Furthermore, based on an analytical study, a simple capacitor voltage regulation constraint was found that can be used in harmonic minimization problems applied to fundamental frequency switched cascaded H-bridge converters. Using this constraint in the optimization process ensures the regulation of capacitor voltages for various loads.

1.2.2. Capacitor Voltage Regulation in Flying Capacitor Rectifier and Start-Up Procedure. Several methods to address the regulation of flying capacitors, including natural balancing, redundant state selection, and modified duty cycles, have been presented [38, 43, 44]. A new active method for the voltage regulation of a single-phase flying capacitor active rectifier was introduced in Paper II of this dissertation. This method utilizes both online and offline procedures to regulate the voltage of all of the flying capacitors. Additionally, it reduces the switching instances which lead to lower switching losses in the converter. Among all of the redundant states that lead to regulating the same number of capacitors, only one is chosen and used in the standard redundant state selection methods. In the proposed method, however, extra redundant states are kept in a table. By using an online procedure among those additional states, states which lead to less switching transitions are chosen. This method thus leads to a lower number of total switching instances in the converter.

In the flying capacitor rectifier topology, the flying capacitors must also be pre-charged to prevent over-voltage stress on the semiconductor devices. In this paper, a start-up procedure is proposed that charges all of the capacitors in the converter. Using the start-up procedure, flying capacitors are charged to the desired voltages to both avoid overstressing the switches and obtain a smoother start-up procedure.

1.2.3. Capacitor Voltage Regulation Method in Hybrid Multilevel Converters. A hybrid converter, which contains a three-phase NPC with two H-bridge cells connected to each phase of NPC, is discussed in Paper III of this dissertation. The NPC converter is a high voltage inverter switched at the fundamental line frequency. The switching strategy of the H-bridge cells, however, is based on the PWM method. The control method for the capacitor voltage regulation is discussed in Paper III section of this dissertation. Independent voltage control of each capacitor, regardless of the voltage level of the rest of capacitors, is the primary advantage of the proposed method. Additionally, this method provides a modular control for each H-bridge cell. This feature is not only helpful for the voltage regulation of the capacitors but also provides the unique ability to operate the inverter, even with a fault in the H-bridge cells.

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PAPER

I. Investigation on Capacitor Voltage Regulation in Cascaded H-bridge Multilevel Converters with Fundamental Frequency Switching

***Abstract*—** Multilevel power electronic converters have gained popularity in high-power applications due to their lower switch voltage stress and modularity. Cascaded H-bridge converters are a promising breed of multilevel converters which generally require several separate dc voltage sources. By utilizing the redundant switching states, it is possible to replace the separate DC voltage sources with capacitors and keep only the one with the highest voltage level. Redundancy in the charge and discharge modes of the capacitors is assumed to be adequate for their voltage regulation. However, the effects of the output current of the converter as well as the time duration of the redundant switching states have been neglected. In this paper, the impacts of the connected load to the cascaded H-bridge converter as well as the switching angles on the voltage regulation of the capacitors are studied. This study proves that voltage regulation is only attainable in a much limited operating conditions that it was originally reported. In addition, based on the analysis of the converter, a simplified formula is found which can be used to find those modulation indices that regulate the voltage of the capacitor. This formula can be used in harmonic minimization problems while capacitor voltage regulation is ensured. Simulation and laboratory results are provided to confirm the analysis.

I. INTRODUCTION

Multilevel power electronic converters are mainly utilized to synthesize a desired single- or three-phase voltage waveform. The desired output voltage is obtained by combining several separate dc voltage sources [1]. Solar cells, fuel cells, batteries, and ultra-capacitors are the most common sources used [2, 3]. The main advantages of such converters are the low harmonic distortion of the generated output voltage, low electromagnetic emissions, high efficiency, the capability to operate at higher voltages, and modularity [4]. In general, multilevel converters are categorized into diode-clamped, flying capacitor, and cascaded H-bridge topologies [1, 4-9]. Diode-clamped multilevel converters are used in conventional high-power ac motor drive applications like conveyors, pumps, fans, and mills [10]. They are also utilized in oil, gas, metals, power, mining, water, marine, and chemical industries. They have also been reported to be used in a back-to-back configuration for regenerative applications [10]. Flying capacitor multilevel converters have been used in high-bandwidth high-switching frequency applications such as medium-voltage traction drives [11]. Finally, cascaded H-bridge multilevel converters have been applied where high-power and power-quality are essential, for example static synchronous compensators (STATCOM) [12, 13], active filter and reactive power compensation applications [14], photovoltaic power conversion [15], uninterruptible power supplies, and magnetic resonance imaging. Furthermore, one of the growing applications for multilevel motor drives is electric and hybrid power trains. Normally, electric and hybrid vehicles use batteries to drive an electric motor. In high-power rating large vehicular motor drives (>250 kW), multilevel converters are suitable due to their high volt-ampere ratings [16, 17]. Multilevel converters can also

solve the existing problems associated with some of the present two-level PWM adjustable-speed motor drives since they can reduce the common-mode voltage causing the bearing leakage current [10].

Figure 1 shows the circuit topology of the cascaded H-bridge multilevel converter. The converter consists of two series-connected H-bridge cells which are fed by independent voltage sources. The outputs of the H-bridge cells are connected in series such that the synthesized voltage waveform is the sum of all of the individual cell outputs. The output voltage is given by

$$V_a = V_{a1} + V_{a2} \tag{1}$$

where the output voltage of the first cell is labeled V_{a1} and the output voltage of the second cell is denoted by V_{a2}. Letter '*a*' is used for phase *a* in case a three-phase converter is considered.

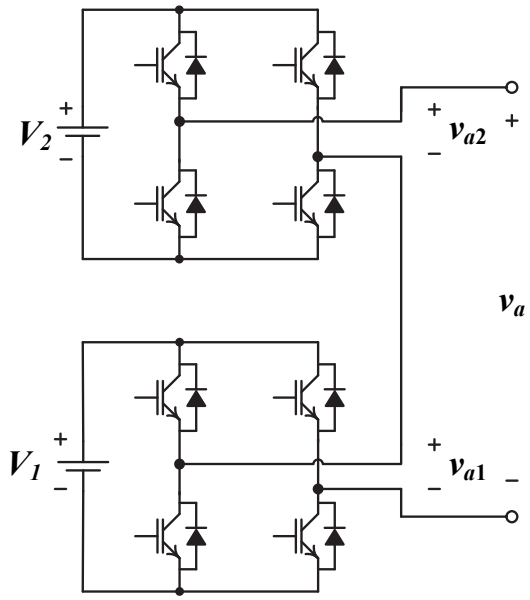

Figure 1. The structure of a cascaded H-bridge converter with two cells.

In early implementations [18-21], each H-bridge cell was supplied by an independent dc source. However, it has been shown that only one cell per phase needs to be supplied by a real dc power source and the remaining cells can be supplied with capacitors [6, 19, 22-26]. This reduces the cost of the converter; however, voltage regulation of the capacitors becomes a challenging issue. The proposed method in [24] uses the switching state redundancy for capacitor voltage regulation. The existence of redundant switching states has been assumed to be adequate for capacitor voltage regulation [24]. However, the output current of the converter as well as the time duration of the redundant switching states greatly impact the charging and discharging patterns of the replacing capacitors.

In this paper, the impact of the electric load connected to the H-bridge multilevel converter as well as the switching angles on the voltage regulation of the replacing capacitors will be studied. This study proves that voltage regulation is only achievable in a more limited range than it was originally reported in [24]. In addition, based on analytical study, a simple capacitor voltage regulation constraint is found which can be used in harmonic minimization problems applied to fundamental frequency switching cascaded H-bridges. Using this constraint in optimization ensures regulation of the capacitors for different loads. In Section II, the principles of operation of multilevel H-bridge converters and switching angles are briefly introduced and the effect of voltage source ratio is discussed. In Section III, a nonlinear set of equations is solved to find the switching angles which eliminate the fifth and seventh harmonics. Constraints for regulation of the capacitor are discussed in Section IV. In Sections V and VI simulation

are provided for resistive and inductive loads respectively. In Section VII, the hardware experimental results are provided.

II. Cascaded H-bridge Multilevel Converter

In the cascaded H-bridge with two cells shown in Figure 1, V_1 and V_2 are stiff voltages such as batteries, fuel cells, photovoltaic cells, capacitors, or ultra-capacitors. Here, they will all be referred to as voltage sources even though they may not be real voltage sources.

The effective number of output voltage levels depends on the ratio between the value of the dc sources (i.e. V_1 and V_2) as shown in Table I. For example, for a two-cell converter (n=2), output voltage V_{a1} is either -V_1, 0, or +V_1 while the output voltage of H_2 can be either -V_2, 0, or +V_2. Accordingly, the output voltage of the converter with two H-bridge cells in different cases is provided in Table II.

As can be observed from Table II, if V_1=V_2, the output voltage has only five levels comparing nine voltage levels when two dc voltage sources of H-bridges are independent. Therefore, the total harmonic distortion of the output voltage is higher than when V_1 and V_2 are independent. Regarding redundancy, in case V_1=V_{dc}=2V_2, the output voltage level at V_{dc}/2 can be generated in two different ways. One is to choose V_{a1}=V_{dc} and V_{a2}=-V_{dc}/2. In this case, V_2 absorbs energy for positive output currents. The second way is to choose V_{a1}=0 and V_{a2}=V_{dc}/2. In this case, V_2 will be discharged for positive output currents. A similar conclusion can be made when the desired output voltage is -V_{dc}/2. Therefore, the output voltage will have seven levels as illustrated in Figure 2. In Figure 2, θ_1, θ_2, and θ_3 are the staircase switching angles ($0 < \theta_1 < \theta_2 < \theta_3 < \pi/2$).

TABLE I
RELATIONSHIP BETWEEN THE NUMBER OF VOLTAGE LEVELS AND THE NUMBER OF SOURCES

Voltage levels (i=2,…, n)	Number of levels	Redundancy
Independent	3^n	0
$V_{a(i\text{-}1)} = V_{ai}$	$2n$+1	3^n-(2n+1)
$V_{a(i\text{-}1)} = 2V_{ai}$	2^{n+1}-1	3^n-(2^{n+1}-1)

TABLE II
OUTPUT VOLTAGE OF A MULTILEVEL CONVERTER WITH TWO CELLS

V_{a1}	V_{a2}	V_{an} (if V_1 and V_2 are not	V_{an} (if V_1=V_2=V_{dc})	V_{an} (if V_1=V_{dc}=2V_2)
V_1	V_2	V_1+V_2	2 V_{dc}	3V_{dc}/2
V_1	0	V_1	V_{dc}	V_{dc}
V_1	-V_2	V_1-V_2	0	V_{dc}/2
0	V_2	V_2	V_{dc}	V_{dc}/2
0	0	0	0	0
0	-V_2	-V_2	-V_{dc}	-V_{dc}/2
-V_1	V_2	-V_1+V_2	0	-V_{dc}/2
-V_1	0	-V_1	-V_{dc}	-V_{dc}
-V_1	-V_2	-V_1-V_2	-2V_{dc}	-3V_{dc}/2

The existence of the redundant states can be used to replace V_2 with a capacitor and provide voltage regulation across its voltage [24]. In addition, in [19] a technique to regulate the voltage of the replacing capacitor is described. Figure 3 shows one phase of

the converter (phase *a*) with a capacitor used as the voltage source for the auxiliary H-bridge. Here the H-bridge cell which is fed by a dc source is called the main H-bridge and the other H-bridge is called auxiliary H-bridge.

For the highest and lowest output voltage levels, e.g., $V_{an}=3V_{dc}/2$ and $-3V_{dc}/2$, there is no redundancy available for capacitor voltage balancing. In these two states, in resistive or highly resistive loads, the capacitor will always be discharged. As a result, these states have been ignored in [19] to avoid this problem. The compromise is that it would result in an only five-level voltage in the output and therefore increases total harmonic distortion. Another approach to balance the voltage of the capacitor is to use the redundant states and select the appropriate switching angels which will be described here.

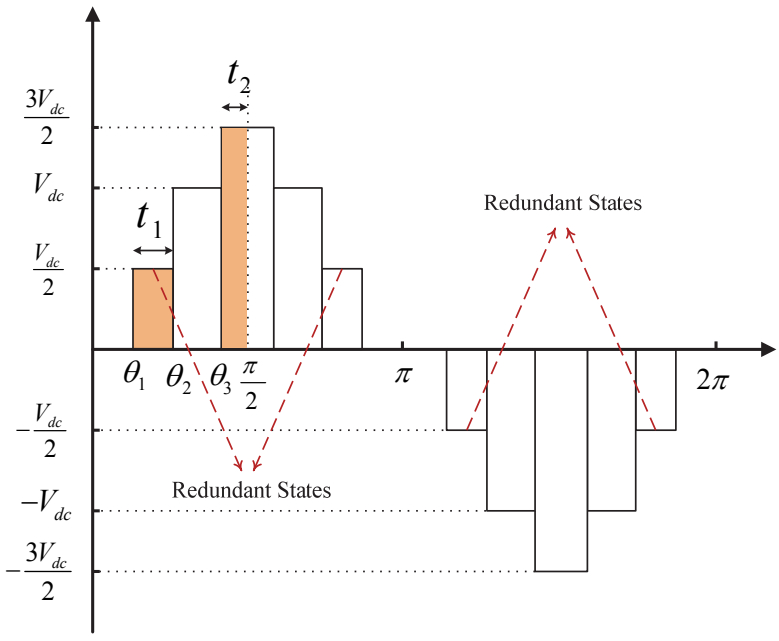

Figure 2. Output voltage waveform of a seven-level cascaded H-bridge converter.

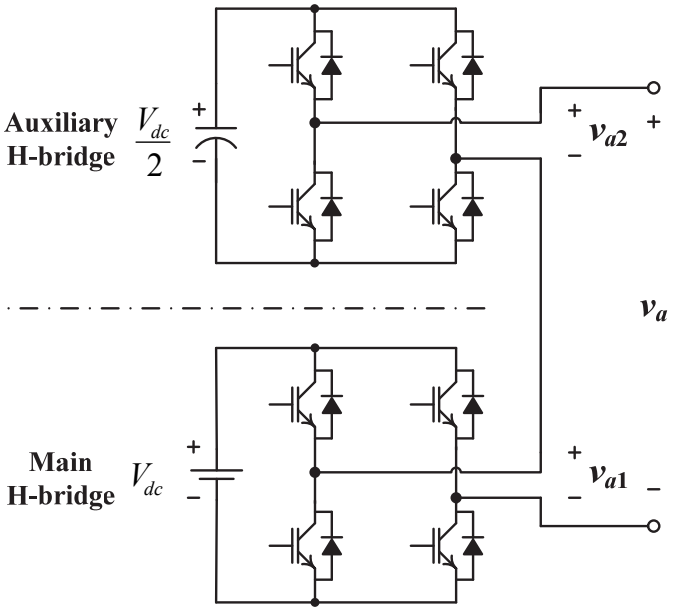

Figure 3. Circuit diagram of the cascaded H-bridge multilevel converter.

III. Selecting Switching Angles for Fifth and Seventh Harmonic Elimination

Commonly, in multilevel converters, the PWM or space vector modulation control methods are used to control the converter [13, 27-32]. Although these methods generate less low frequency harmonics in the output waveform, their high frequency switching methods generate further switching losses. These losses become a serious issue in high power converters. Therefore, fundamental frequency switching and selective harmonic elimination methods are used to address this problem [4-6, 29, 33-35]. In this study, low switching harmonic elimination method is used. In this method, in each fundamental period there are only four switching transients for the main H-bridge cell and the control algorithm of the inverter is designed in a way that the number of switching transients in the auxiliary H-bridge cell is limited to twelve in one fundamental period. In other words the control system uses only one redundant state during each

subinterval to avoid extra switching. The Fourier series expansion of the output voltage waveform which is shown in Figure 2 is

$$V_a(\omega t) = \frac{4}{\pi}\frac{V_{dc}}{2}\sum_{n=1,3,5,\ldots}^{\infty}\frac{1}{n}(\cos(n\theta_1)+\cos(n\theta_2)+\cos(n\theta_3))\sin(n\omega t). \tag{2}$$

If the amplitude of the fundamental harmonic of phase *a* is desired to be V_m, by choosing appropriate values for the angles, one can eliminate the fifth- and seventh-order harmonics [19]. The third harmonic will be automatically cancelled in a balanced three-phase system. The system of nonlinear equations that satisfies the desired modulation index and eliminates of the fifth and seventh harmonics is given by

$$\begin{aligned}
&\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3) = m\\
&\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3) = 0\\
&\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3) = 0
\end{aligned} \tag{3}$$

where *m* is the modulation index and defined as

$$m = \frac{\pi}{2}\frac{V_m}{V_{dc}} \tag{4}$$

where V_m is the peak of the desired output voltage. In order to solve the system of equations in (3), several approaches, including resultant theory, have been proposed [24]. In addition to the discussed methods, one can use MATLAB nonlinear solvers to solve this nonlinear system of equations. This method can be used without dealing with the complexity of previously proposed methods [24]. The Levenberg-Marquardt algorithm in

nonlinear solver of MATLAB is used for solving the set of equations. The solution of (3) which is the set of switching angles [6] is depicted in Figure 4. As shown in this figure, when m is between 1.488 and 1.852, the solution of the equations leads to two sets of answers. In other words, in this range, creating the required m and eliminating the fifth and seventh harmonics is possible by two sets of values for θ_1, θ_2, and θ_3.

Based on the nature of the load, the switching scheme may or may not be able to regulate the voltage across the replacing capacitor. The existence of the redundant switching states has been assumed to be adequate for capacitor voltage regulation [15, 34]. However, output current of the converter as well as the time duration of the redundant switching states greatly impact the charging or discharging patterns of the replacing capacitor. In the following section, existing constraints on the regulation of the voltage of the capacitor is discussed.

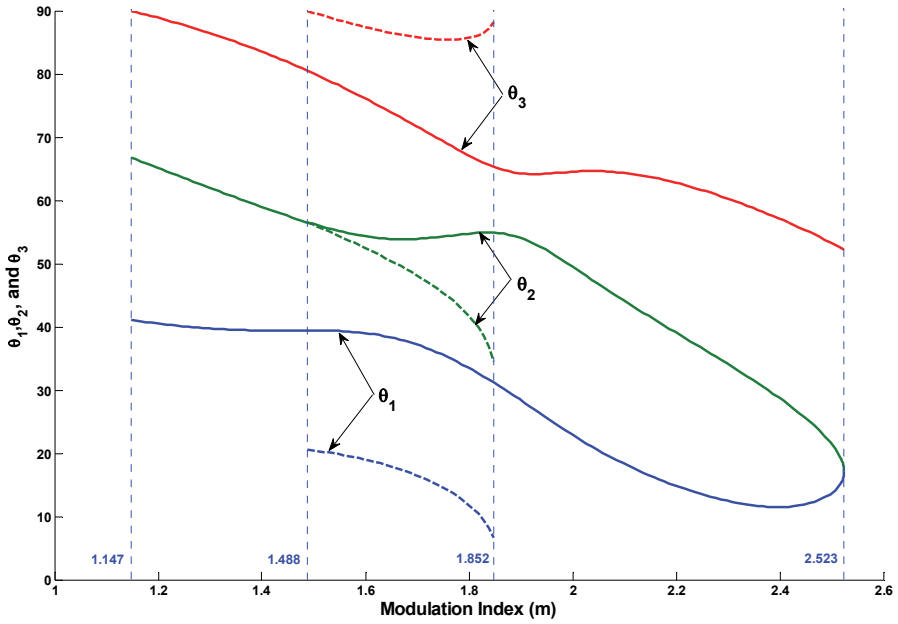

Figure 4. Solution for the switching angles.

IV. Constraints on Capacitor Voltage Regulation

In the following discussion, without loss of generality, the load is assumed to be resistive. In this converter, the maximum capacitor discharge occurs when the output voltage is at its maximum level. This is because in resistive loads, the current too is at its maximum level in this subinterval. Therefore, the capacitor is discharged faster than other types of loads (inductive or capacitive). In other words, if the constraint satisfies resistive loads it also satisfies inductive and capacitive loads.

Since the charging and discharging patterns are repeated every quarter of the period, examining only one quarter is adequate. The first quarter of the period is divided into four subintervals and the voltage level of the capacitor is investigated in each subinterval (see Figure 2).

The following two methods are presented for the investigation of the regulation condition of the capacitor.

A. Detailed Method

The four subintervals in one quarter are as follow:

$0 \rightarrow \theta_1$ *No charge or discharge subinterval*: No capacitor charge or discharge occurs in this subinterval.

$\theta_1 \rightarrow \theta_2$ *Charge or discharge subinterval*: Although it is possible to charge or discharge the capacitor in this subinterval, here only the charging option is considered since the focus is on the capacitor voltage regulation. The left-hand side of Figure 5 shows the simplified combination of the two H-bridge converter cells during this subinterval. The capacitor voltage is given by

$$V_c = V_{dc} + \frac{V_{dc}}{2}\left(1 - e^{-\frac{t}{\tau}}\right). \quad (5)$$

where τ is the time constant. The capacitor voltage increment in this subinterval can be described as

$$\Delta V_{c1} = \frac{V_{dc}}{2}\left(1 - e^{-\frac{t_1}{\tau}}\right). \quad (6)$$

By expanding the exponential term and considering that the capacitor used for the auxiliary H-bridge cell is a large capacitor; the changes in the capacitor voltage can be approximated by

$$\Delta V_{c1} = \frac{V_{dc}}{2} * \frac{t_1}{\tau} = \frac{V_{dc}}{2} * \frac{\theta_2 - \theta_1}{\omega\tau}. \quad (7)$$

$\theta_2 \rightarrow \theta_3$ *No charge or discharge subinterval*: In this subinterval the capacitor is not engaged; therefore, no charge or discharge occurs.

$\theta_3 \rightarrow \frac{\pi}{2}$ *Discharge subinterval*: The capacitor is discharged by the load current in this subinterval. The right-hand side of Figure 5 shows the simplified combination of the two H-bridge cells during this subinterval.

$$\Delta V_{c2} = -(V_{dc} + V_{c0})\left(1 - e^{-\frac{t_2}{\tau}}\right) \rightarrow \Delta V_{c2} = -\frac{V_{dc}}{2}\left(3 + \frac{t_1}{\tau}\right) * \frac{t_2}{\tau} \quad (8)$$

Since the capacitor used for the auxiliary H-bridge cell is a large capacitor, (8) can be simplified to

$$\Delta V_{c2} = -3\frac{V_{dc}}{2} * \frac{t_2}{\tau} = -\frac{3V_{dc}}{2} * \frac{\frac{\pi}{2} - \theta_3}{\omega\tau}. \tag{9}$$

The capacitor voltage increment during the charge subinterval should be more than the voltage decrement during the discharge subinterval to insure capacitor voltage regulation. Therefore, the capacitor voltage can be regulated if $|\Delta V_{c1}| > |\Delta V_{c2}|$. Consequently, the regulation condition can be described as

$$-\theta_1 + \theta_2 + 3\theta_3 > \frac{3\pi}{2}. \tag{10}$$

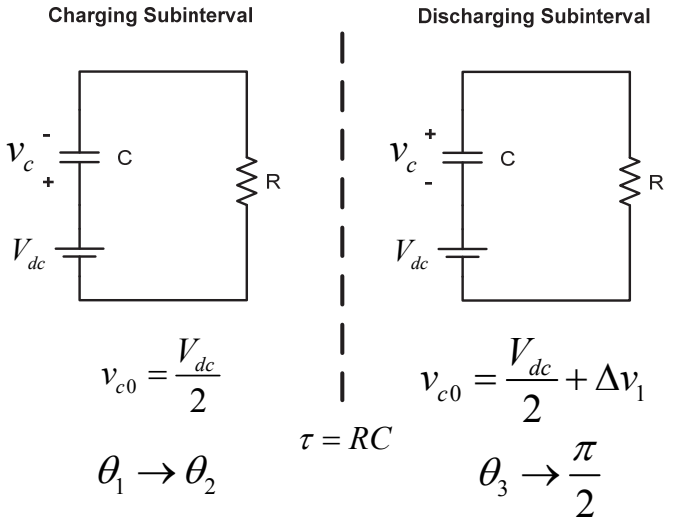

Figure 5. Simplified H-bridge converter and load in charging and discharging subintervals.

B. Simplified Method

In this method, it is assumed that the output voltage (and consequently output current) is constant during each subinterval. This assumption is valid for a large capacitor. Similar to the detailed method, capacitor regulation is investigated in one quarter of the period. In one quarter, there are four subintervals but only ($\theta_1 \rightarrow \theta_2$) and ($\theta_3 \rightarrow \frac{\pi}{2}$) intervals should be investigated for capacitor regulation conditions (only in these two subintervals the capacitor is engaged).

$\theta_1 \rightarrow \theta_2$ Charge or discharge subinterval:

Since it is assumed that the output voltage is constant in this subinterval, the output current (and capacitor current) is

$$I_{c1} = I_{o1} = \frac{V_{dc}}{2R}. \tag{11}$$

where *R* is output resistance. Changes in the capacitor charge in this subinterval can be described as

$$\Delta Q_1 = I_{c1} * t_1 = \frac{V_{dc}}{2R} * \frac{\theta_2 - \theta_1}{\omega}. \tag{12}$$

$\theta_3 \rightarrow \frac{\pi}{2}$ Discharge subinterval:

Since the capacitor is discharging in this subinterval, capacitor current is the negative of the output current. Similarly output current (and the negative of the capacitor current) in this subinterval is

$$I_{c2} = -I_{o2} = -\frac{3V_{dc}}{2R}. \tag{13}$$

Changes in the capacitor charge in this subinterval can be described as

$$\Delta Q_2 = I_{c2} * t_2 = -\frac{3V_{dc}}{2R} * \frac{\frac{\pi}{2} - \theta_3}{\omega}. \tag{14}$$

The capacitor voltage can be regulated if the capacitor net charge is positive in one quarter of the waveform. In other words, the regulation of capacitor voltage is possible if

$$\Delta Q = \Delta Q_1 + \Delta Q_2 > 0 \tag{15}$$

or

$$\frac{V_{dc}}{2R} * \frac{\theta_2 - \theta_1}{\omega} - \frac{3V_{dc}}{2R} * \frac{\frac{\pi}{2} - \theta_3}{\omega} > 0. \tag{16}$$

Equation (16) can be simplified to

$$-\theta_1 + \theta_2 + 3\theta_3 > \frac{3\pi}{2}. \tag{17}$$

This shows that both detailed and simplified methods lead to the same capacitor voltage regulation constraint.

By applying the constraint represented in (10) on Figure 4, it is possible to find the modulation indices that ensure capacitor voltage regulation. In Figure 6, the range in which capacitor voltage regulation is feasible is shown in solid lines. The dashed lines represent the range in which the capacitor voltage cannot be regulated.

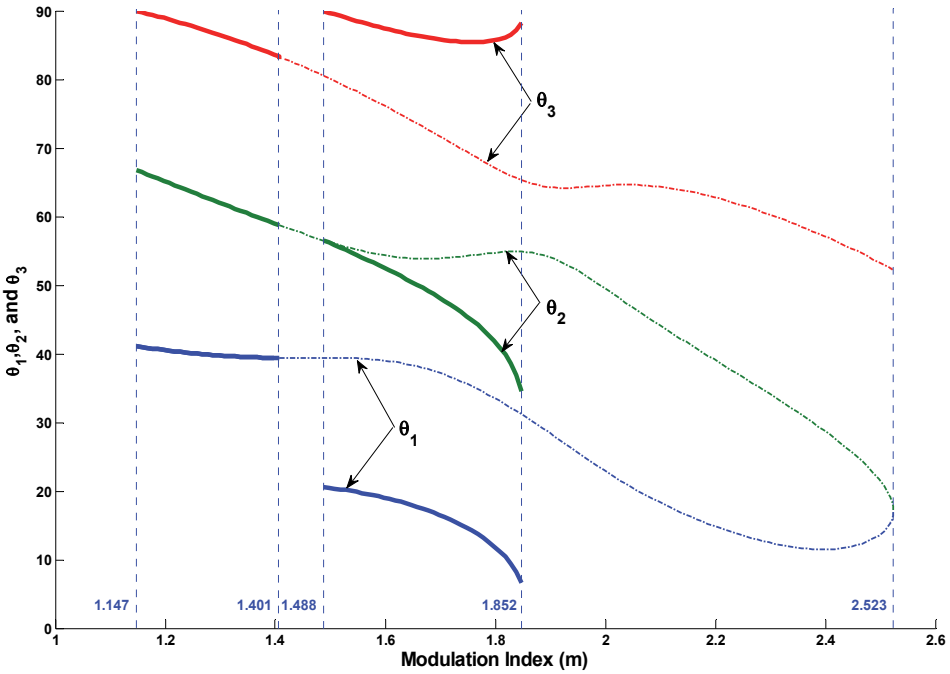

Figure 6. Capacitor voltage regulation region with resistive load.

Note that the capacitor voltage regulation constraint in (10) can be used in harmonic minimization problems as an extra condition to guarantee the regulation of the capacitor voltage in all different load conditions.

V. Converter Operation with Resistive Load

In this study, a control system is used to regulate the voltage of the capacitor. In this system, based on the difference between the desired capacitor voltage and actual capacitor voltage, redundant states are selected in a way to keep the voltage of the capacitor close to the desired voltage. If the voltage of the capacitor is less than $V_{dc}/2$ those states that charge the capacitor are selected and H-bridge cells are switched based on this selection. Decision for using different redundant states is made at the beginning of

each $V_{dc}/2$ or $-V_{dc}/2$ levels. This ensures having a constant number of switching transitions for each H-bridge cell during a cycle. In other words, the numbers of switching instants per cycles for both H-bridge cells are constant disregarding load condition, modulation index, and voltage of the capacitor.

Here, two cases are examined for two different modulation indices. In the first case, capacitor voltage regulation is not possible however in the second case the regulation of the capacitor is possible in that modulation index. For the following demonstrations, V_{dc} is considered to be 100 V and the replacing capacitor (acting as voltage source for the auxiliary H-bridge) is chosen to be 3.5 mF. The load is a 16 Ω resistor. The control objective is to regulate the capacitor voltage at 50 V (i.e. $V_{dc}/2$). In the following, regulation of the capacitor is investigated for two selected modulation indices.

Operation at m=1.2 (capacitor voltage regulation is possible): for m=1.2, based on Figure 4 switching angles are chosen as θ_1=40.54º, θ_2=65.12º, and θ_3=88.88º. Note that m=1.2 is located in the solid section of Figure 6. Therefore, based on the presented analysis, capacitor voltage regulation should be possible with this modulation index.

In Figure 7, the output voltage of the main cell (V_{a1}), the output voltage of the auxiliary cell (V_{a2}), the total output voltage of the cascade H-bridge converter (V_a), the voltage of the capacitor (V_c), and 'Reverse' command are shown from top to bottom. Note that at the beginning of the subinterval during which the output voltage is supposed to be $\pm V_{dc}/2$, the actual voltage of the capacitor is compared against $V_{dc}/2$ (the desired level for the capacitor voltage). Based on this comparison and the direction of the load current at this moment, the decision is made to select the H-bridge switching in the way

to charge or discharge the capacitor. When the 'Reverse' command is 1, the redundant state in which the output voltage of the auxiliary H-bridge opposes the polarity of the output voltage of the main H-bridge cell is selected. The 'Reverse' command is updated at the beginning of each subinterval with $\pm V_{dc}/2$ output voltage levels. 'Reverse' command is determined based on the positive or negative alternative of the converter's output voltage, voltage of the capacitor, and output current direction of the converter. In resistive loads, if 'Reverse' is 1 the redundant state which charges the capacitor is selected. As it is shown in Figure 7, by choosing different redundant states, the control system has been successful in regulating the voltage of the capacitor.

Operation at m=2.4 (capacitor voltage regulation is not possible): For m=2.4, based on Figure 4 switching angles are chosen as θ_1=11.50º, θ_2=28.72º, θ_3=57.11º. With this set of switching angles, the capacitor charging time is less than its discharging time. Therefore, the voltage of the capacitor will not remain at a constant level and will decrease continuously until it discharges completely. Note that m=2.4 is located in the dashed section of Figure 6. Therefore, based on the presented analysis, regulation of the voltage of the capacitor is not possible in this modulation index.

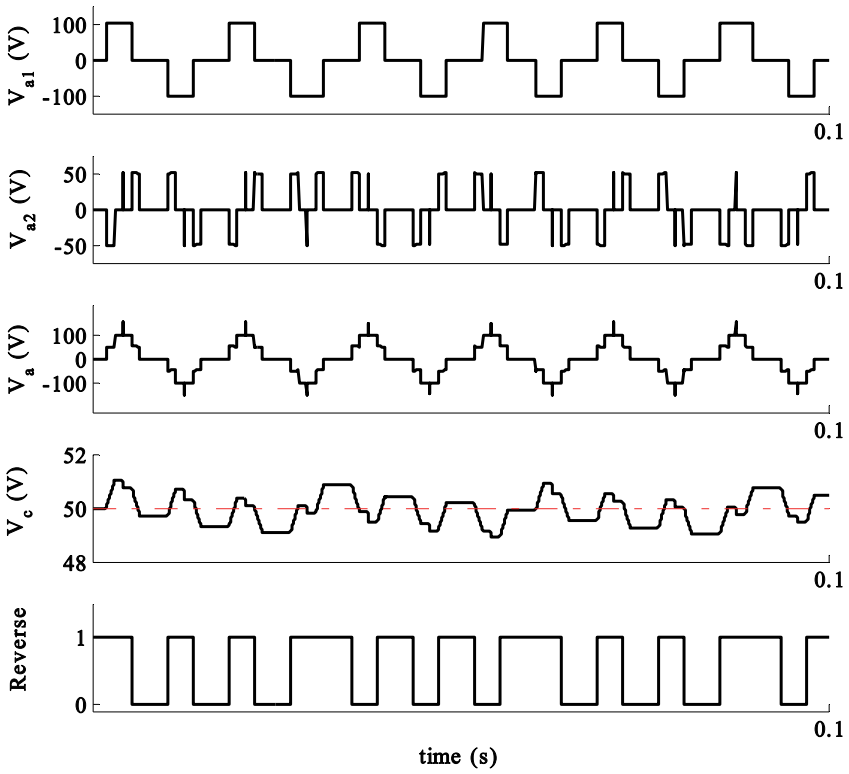

Figure 7. Output voltage of each H-bridge cells with total output voltage of converter at m=1.2 for resistive load.

Figure 8 depicts the operation of the converter using this set of switching angles. Even though the controller selects the states for charging capacitor (‘Reverse’ command is always one), capacitor voltage eventually falls to 0 V. As shown, the output voltage waveform gradually deteriorates as the capacitor gets discharged. Finally, due to complete discharge of the capacitor, four levels out of seven levels of the converter output voltage are lost. As shown in this case, it is not possible to keep the charge of the capacitor.

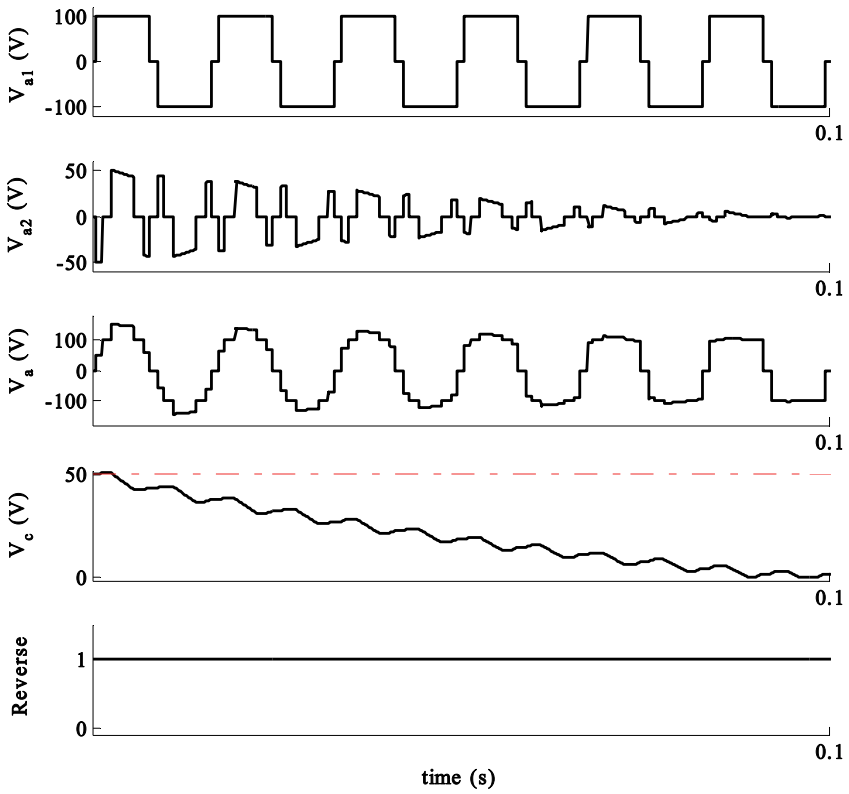

Figure 8. Output voltage of each H-bridge cells with total output voltage of converter at m=2.4 for resistive load.

VI. Converter Operation with Inductive Load

In most power applications, the load is inductive [36]. For this reason, the operation of the converter is investigated with an inductive load. Here, the simulation is repeated for *m*=2.4 with an inductive load to observe if load inductivity effects the regulation of the capacitor voltage. The inductive load consists of a 16 Ω resistance connected in series with a 0.1 H inductor. Simulation results for this type of load are depicted in Figure 9. As can be observed, the capacitor voltage is regulated in this case. Note that capacitor voltage regulation was not possible with the same modulation index (m=2.4) in the resistive load case. Because in an inductive load the peak value of the

output current does not coincide with the peak value of the output voltage. The phase shift between the load current and the output voltage of the inverter reduces the rate of discharging of the capacitor. Therefore, in highly inductive loads it is always possible to keep the charge of the capacitor at the desired level.

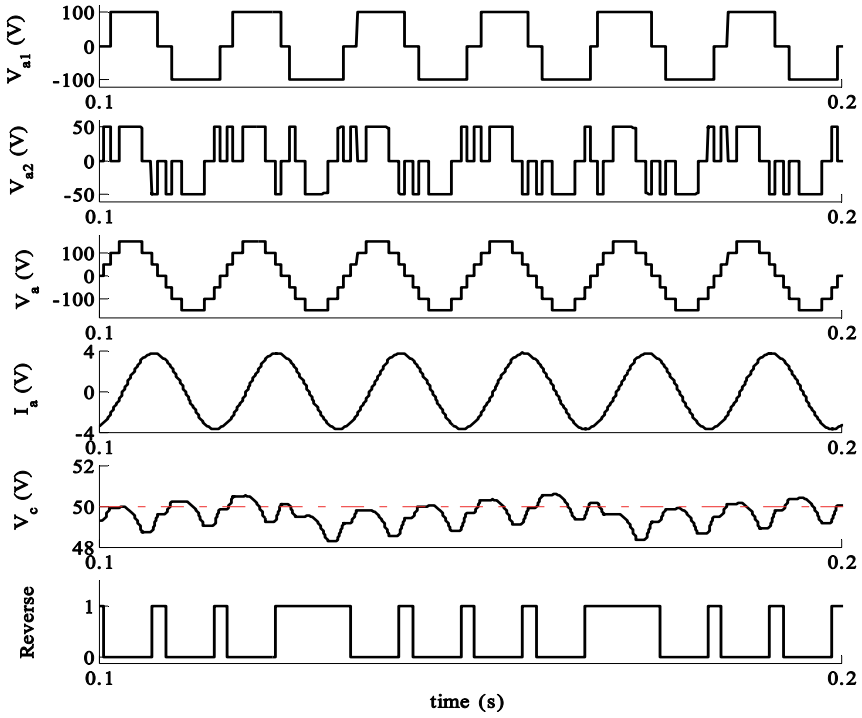

Figure 9. Output voltage of each H-bridge cells with total output voltage of converter with inductive load at m=2.4.

A. Load's Power Factor Effect on the Regulation of the Voltage of the Capacitor

In order to study capacitor voltage regulation for different inductive loads a variable inductive load that changes in a wide range of power factor is used. For this reason a constant inductor with value of 0.1 H is connected with a variable resistance to

obtain different power factors. Using simulation method, for each individual value of power factor the regulation of the capacitor is checked for the entire range of the modulation indices (m) and the maximum modulation index for each power factor is recorded. The results are depicted in Figure 10. According to this figure, capacitor voltage regulation is possible for every modulation index and power factor under the curve. In this case, continuous curves of switching angles in Figure 4 are utilized. When the load is more inductive (low power factor); the regulation region will extend to almost the entire region. However the power factor of most loads is above 0.7 where the capacitor voltage regulation region faces limitations.

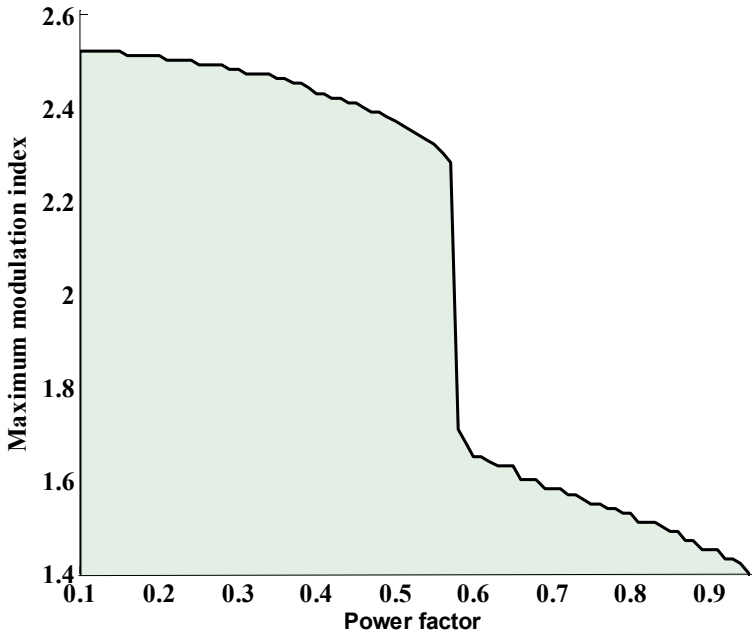

Figure 10. Effect of power factor on the capacitor voltage regulation.

VII. Experimental Results

In order to verify the simulation and analytical results, a hardware prototype of the system was developed. In the experiments, the main H-bridge cell is fed by a 100 V DC source and a 3.5 mF capacitor is connected to the auxiliary H-bridge cell and the voltage of the capacitor is regulated to 50 V. A Texas Instrument TMS320F2812 digital signal processer (DSP) and CY37128P84 complex programmable logic device (CPLD) are used for programming the control method. Figure 11 shows the hardware diagram of the cascaded H-bridge converter with its control loop.

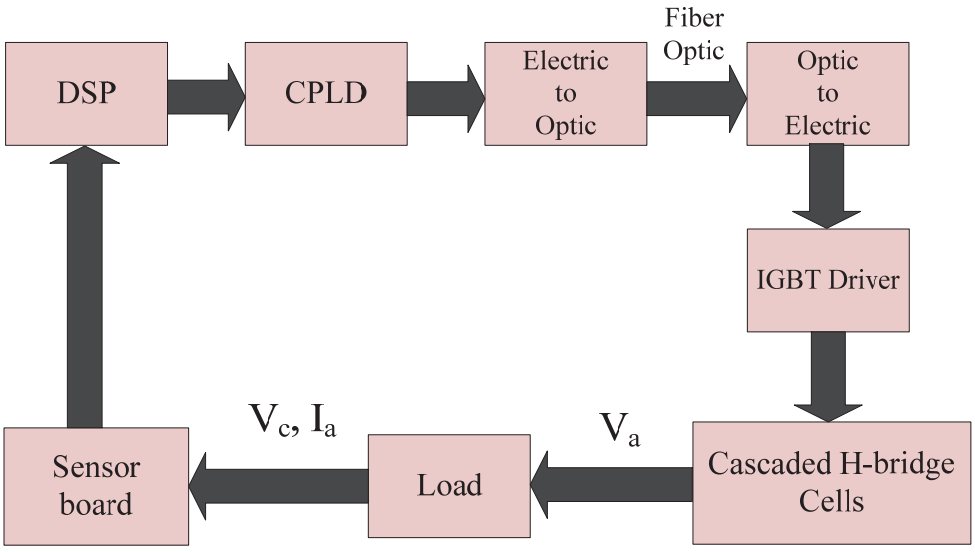

Figure 11. Hardware diagram of cascaded H-bridge converters and its control system.

In the following, the simulation and analytical results of the pervious section are verified for both resistive and inductive loads.

A. Operation with Resistive Loads

For the resistive load experiments, a 16 Ω resistor is used as load. First, the operation of the converter is repeated in experiment for *m*=1.2 and 2.4.

Operation at m=1.2:

Figure 12 shows the output voltage of converter and the output voltage of both H-bridge cells along with the voltage of the capacitor. According to the figure, the capacitor voltage is regulated around 50 V using the control system.

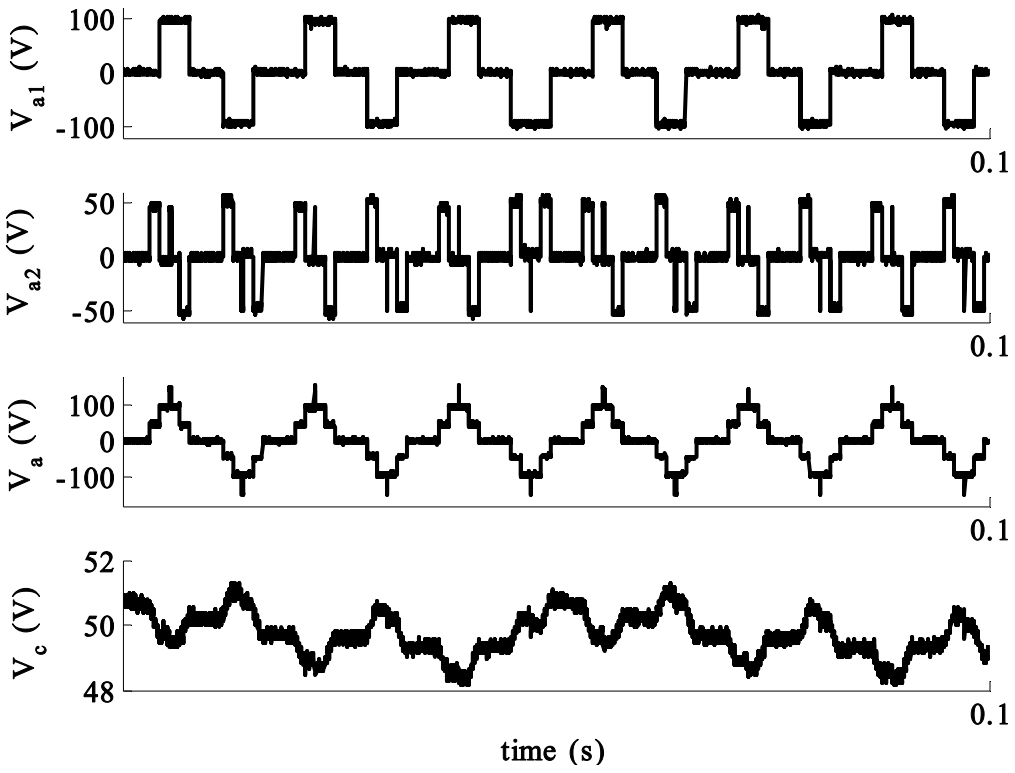

Figure 12. Output voltage of each H-bridge cells with total output voltage of converter with resistive load at m=1.2.

Operation with switching from m=1.2 to m=2.4:

Figure 13 shows the operation of the converter when modulation index is changed from 1.2 to 2.4. When the modulation index is 1.2, the capacitor voltage is regulated but when the modulation index is changed to m=2.4 at t_1 the capacitor voltage regulation is not possible anymore and the voltage of the capacitor is decreased until it is discharged completely. As can be observed, the output voltage waveform gradually deteriorates as the capacitor gets discharged.

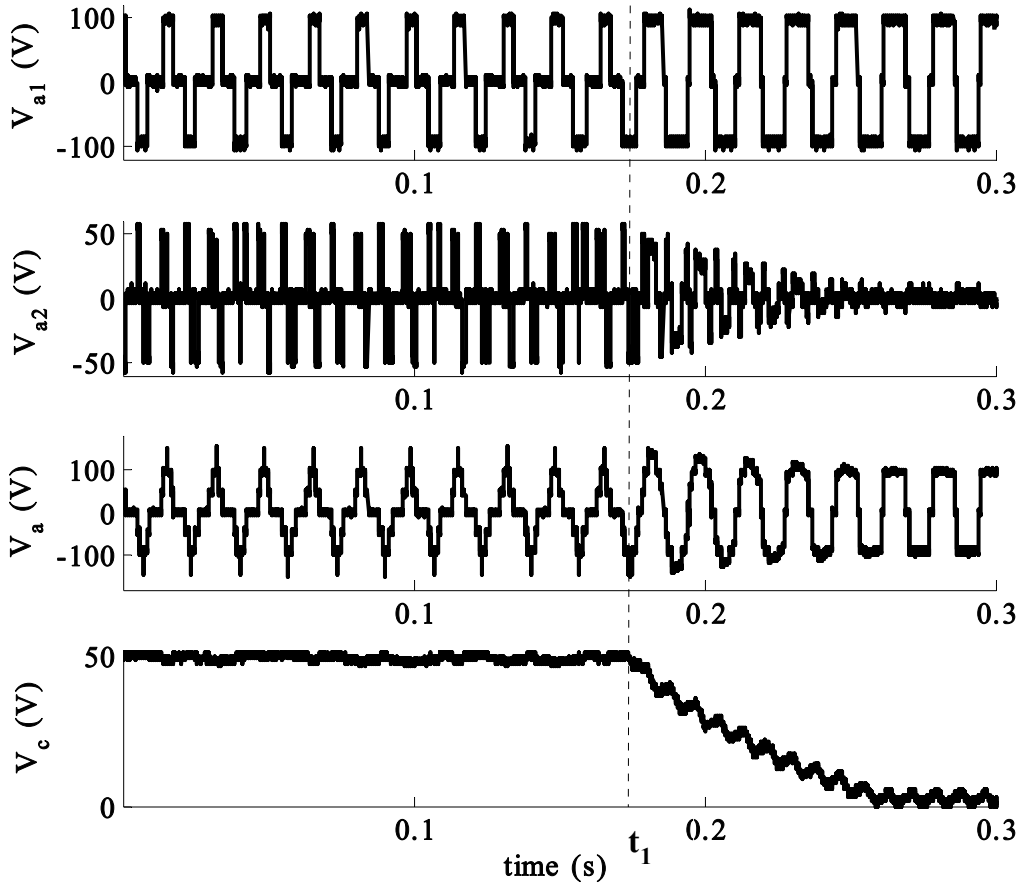

Figure 13. Output voltage of each H-bridge cells with total output voltage of converter with resistive load when m is changed from 1.2 to 2.4.

Operation at m=1.85:

According to Figure 6, there are two sets of possible angles for this modulation index. Here the switching angles are chosen as θ_1=6.29º, θ_2=33.88º, θ_3=88.52º which is located in the discontinuous part of the curve where regulation is possible. In Figure 14 the start-up operation with discharged capacitor is shown. The voltage of capacitor builds up and it is regulated around 50 V. In order to experimentally verify the analysis that led to Figure 6, capacitor voltage regulation is investigated in all range of possible modulation indices. Solid squares in Figure 15 show the modulation indices at which regulation is possible and hollow squares show the modulation indices at which regulation is not possible. This figure shows that the experimental result strongly supports the analysis.

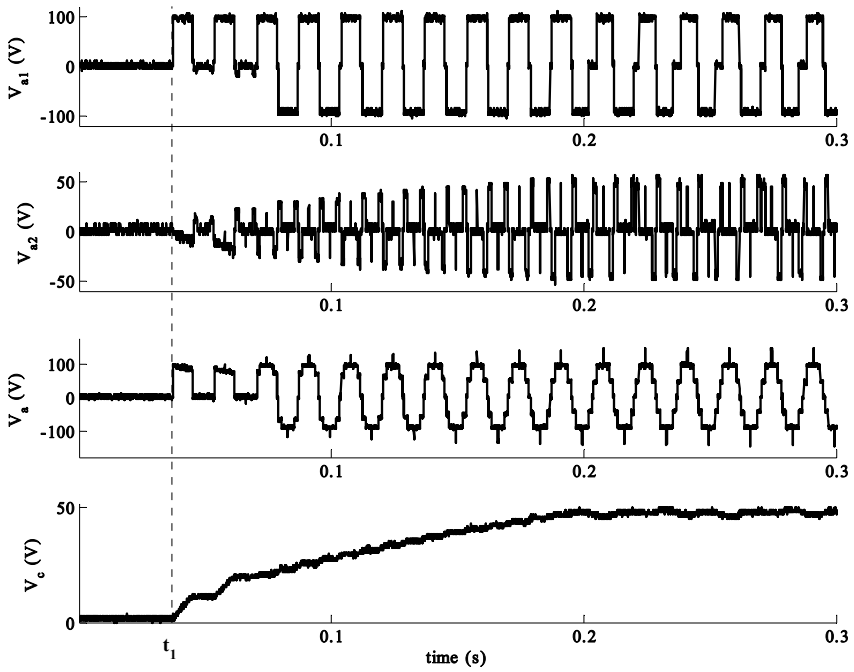

Figure 14. Start-up operation and charging the capacitor with resistive load at m=1.85.

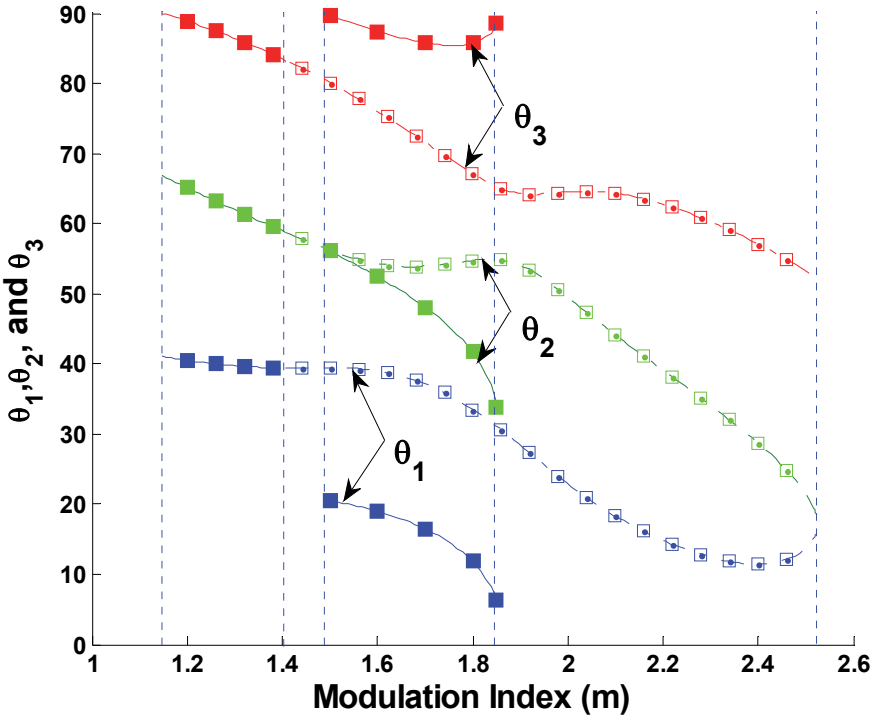

Figure 15. Experimental verification of capacitor voltage regulation for resistive loads (Solid square: regulation is possible; hollow square: regulation is not possible).

B. *Operation with Inductive Loads*

For the inductive load experiments, a 0.1 H inductor is connected in series with a variable resistor. Figure 16 shows the operation of the converter for m=2.4 and an inductive load with a 16 Ω resistor and a 0.1 H inductor. As can be observed, the capacitor voltage is regulated with this load. However, according to Figure 13, regulation of voltage of capacitor was not possible for this modulation index when the load was resistive. The experiment for this load is repeated for several modulation indices and the regulation of capacitor voltage is tested. Solid squares in Figure 17 show the modulation

indices at which the regulation is possible and hollow squares show the modulation indices at which the regulation is not possible.

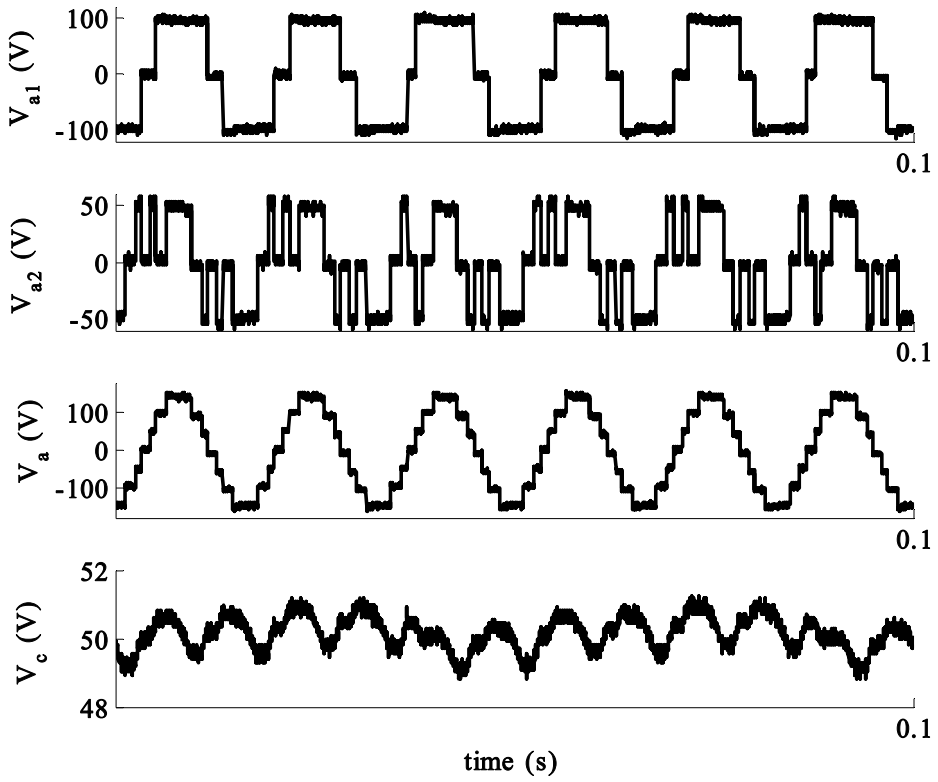

Figure 16. Output voltage of each H-bridge cells with total output voltage of converter with inductive load at m=2.4.

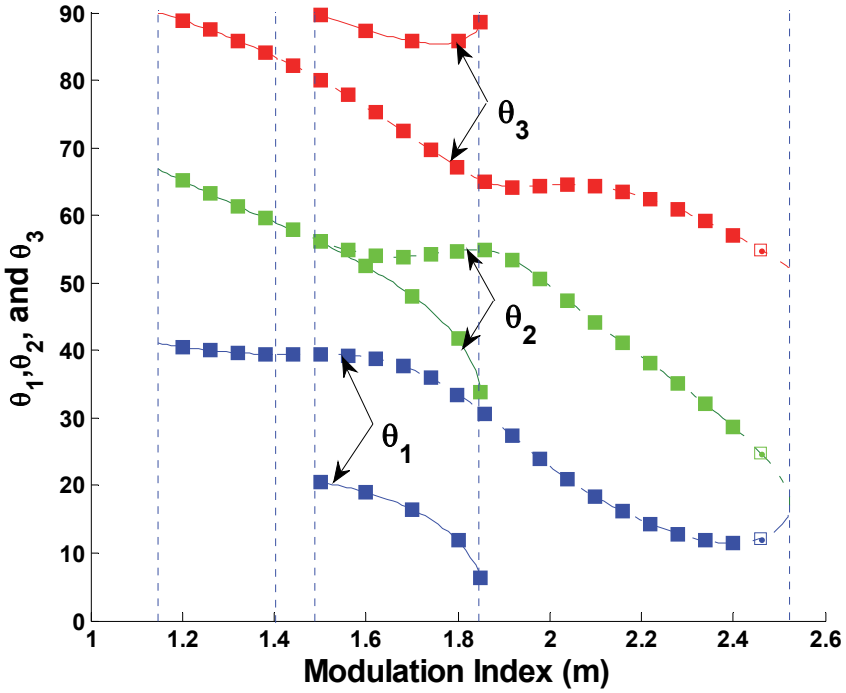

Figure 17. Capacitor voltage regulation for an inductive load with R=16 Ω and L=0.1 H (Solid square: regulation is possible; hollow square: regulation is not possible).

In order to study the effect of the power factor on the voltage regulation of the capacitor, for different modulation indices, the resistor which is connected in series with the 0.1 H inductor is changed and the regulation of the capacitor is monitored. The maximum resistance which corresponds with the maximum power factor is recorded for each modulation index and these points are shown with squares in Figure 18.

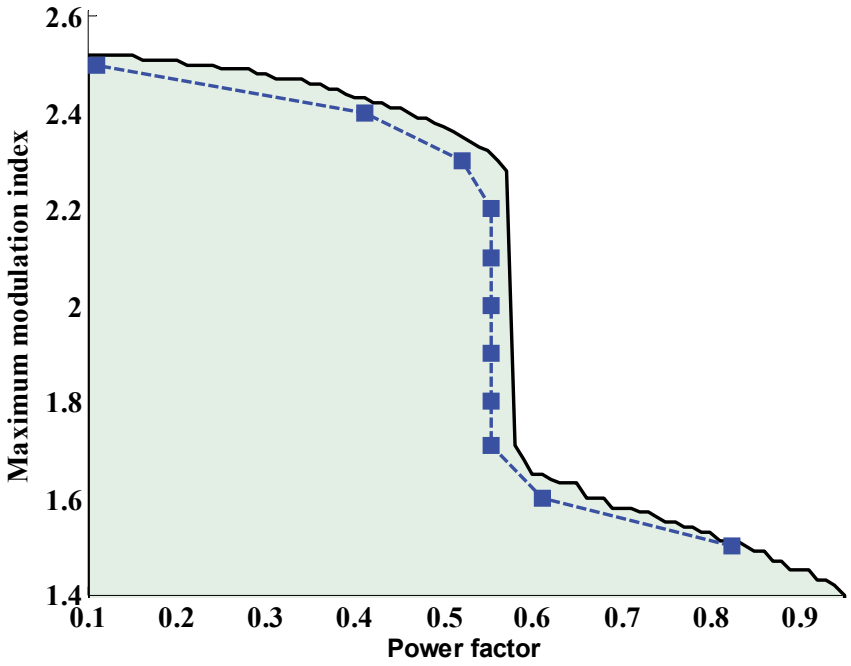

Figure 18. Experimental verification of effect of power factor on the capacitor voltage regulation.

VIII. Conclusion

In this paper, a cascaded H-bridge multilevel converter consisting two H-bridge cells are investigated. In the topology of the converter, one of the H-bridges is fed by a dc source while the other is supplied by a capacitor. The operation of the converter is studied with different types of loads. Using analysis, it is proven that capacitor voltage regulation is not attainable in all load conditions. Also, a simple formula is derived which can be used to identify modulation indices which lead to voltage regulation of the capacitor. This constraint can be used in optimization problems for harmonic minimization or harmonic mitigation to guarantee capacitor voltage regulation in all load condition (i.e. resistive, inductive, or capacitive). In addition, the effect of the variations of the power factor on

the voltage regulation of the capacitor is studied. Simulation and hardware implementation of the converter is carried out to evaluate the theory. This study shows that the simulation and hardware implementation results support the theoretical analysis.

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II. Start-up Procedure and Switching Losses Reduction for a Single-Phase Flying Capacitor Active Rectifier

***Abstract*—** This paper describes a research conducted on a single-phase flying capacitor active rectifier. An online process is introduced that reduces the total number of switching events, which leads to a reduction of switching losses in the converter. This method is based on redundant state selection, which is used to regulate the voltage of flying capacitors. The proposed approach is general and can be applied to flying capacitor converters with any number of levels. Furthermore, in order to control the inrush current at the start of operation and avoid extra voltage and current stress for active switches and capacitors, a start-up procedure is proposed that pre-charges the flying capacitors. With this pre-charge procedure, no additional hardware is needed. Simulation and laboratory results demonstrate these new concepts.

I. Introduction

Multilevel converters are today the industrial solution for applications that demand medium output voltage, high dynamic performance, and high power quality [1-6]. There are three main topologies for multilevel converters; cascaded H-bridge, neutral point diode-clamped, and flying capacitors (FC) converters [7]. The flying capacitor topology has some distinct advantages over the neutral point diode-clamped topology including modularity [1], the absence of clamping diodes, and the ability to regulate the

voltage across the flying capacitors through per-phase redundant state selection even when the number of voltage levels is greater than three.

Today, multilevel converters are the industrial solution for applications that demand medium output voltage, high dynamic performance, and high power quality [1-6, 8]. There are three main topologies for multilevel converters: cascaded H-bridge, neutral point diode-clamped, and flying capacitor (FC) converters [7]. The flying capacitor topology has some distinct advantages over the neutral point diode-clamped topology, including modularity [1], the absence of clamping diodes, and the ability to regulate the voltage across the flying capacitors through per-phase redundant state selection even when there are more than three voltage levels.

In this paper, a single-phase flying capacitor active rectifier (FCAR), which is used as the first stage (ac to dc) of a solid-state transformer (SST), is described [9, 10]. The first stage of an SST consists of an ac-dc converter that is connected to the medium voltage grid; therefore, using a multilevel power converter is one of the viable solutions for this kind of application [10]. Active rectifiers have two main control objectives; adjusting voltage in the output side of the rectifier and providing a unity power factor in the input side. However, in the flying capacitor rectifier, the voltage of the flying capacitors should be regulated as well. Several nonlinear and linear control methods exist, including the hysteresis, predictive [11], feed forward [12], deadbeat [13], and reference frame (*d*-*q*) control [14, 15] methods, that can be utilized to obtain an output voltage adjustment and unity power factor. Although some of these methods were originally introduced for controlling conventional converters, with some modifications, they also can be applied to multilevel converters. In this paper, a reference frame (*d*-*q*)

control method, which is a well-established and well-known current mode control, is used for controlling the FCAR [16].

The natural capacitor voltage balancing approach is among the simplest approaches for regulating the voltage of flying capacitors. However, to ensure tighter voltage regulation under critical operating conditions, it is necessary to employ more elaborate methods [17-20]. Among several modulation methods, phase-shifted pulse width modulation (PS-PWM) and phase disposition PWM are widely used in multilevel and flying capacitor converters because of their straightforward implementation [21-23]. PS-PWM has the ability to naturally balance a capacitor's voltage if it used for a symmetrical FC converter [22-24]. However, in a practical FC with varying capacitors, a load that has disturbances, and unequal switching delays, and that sometimes operates at low modulation indices, natural balancing is challenged [15, 23, 25]. In order to ensure better capacitor voltage balancing with better dynamics, active voltage balancing methods, such as switching state selection, external circuits, and a modified modulation index, are used by researchers [11, 15, 23, 26-31].

The voltage balancing method introduced in this paper is based on the multilevel modulation method, a table that is generated offline for gate switching commands [11, 26]. It employs a redundant state selection (RSS) table for capacitor voltage balancing. Here, the proposed method consists of both offline and online procedures (unlike standard offline-only methods), which helps to generate switching commands. In the offline procedure, all the best switching states for all possible capacitor charge conditions are selected; then, in the online procedure, the switching states that generate the least switching changes will be chosen. Note that in this approach, the redundant states in legs

a and *b* are combined in the same table. In the standard table method, among all the redundant states that lead to regulating the same number of capacitors, only one is chosen and used. However, in the proposed method, extra redundant states are kept in the table. Then, using an online procedure, among those additional states the one is chosen that leads to less change in switching. This method yields less total switching in the converter.

In an active rectifier application, it is important to pre-charge the output capacitor in order to reduce the inrush current at the start of operation [32]. This ensures that the current of active switches and capacitors remains within the tolerable range of the electric components. In a conventional active rectifier, there is only one set of capacitors at the output that can be pre-charged by a series resistor and a switch or contactor. However, in the FCAR topology, the flying capacitors must also be pre-charged in order to prevent over-voltages on the semiconductor devices. In [22, 33, 34] self pre-charge methods for FC inverters with natural balancing are presented, but these methods cannot be applied readily to flying capacitor rectifiers. During the start-up procedure in inverters, it is possible to command the inverter with a specific constant duty ratio [34] or a specific pattern for the duty ratio [33] and charge the capacitors. However, due to the existence of the ac voltage source in the input side of the rectifier, using the same method is not possible and may cause an excessive inrush current during start-up. In this paper, a start-up procedure is proposed that charges all of the capacitors in the converter with a commonly-used input resistor and switch without using extra circuitry. In this method, flying capacitors are charged to the desired voltage, which is proportionate to the output voltage, to avoid overstress to switches and obtain smoother start-up.

In Section II of this paper, the principle behind the reference frame (*d-q*) control method is described for clarity. Section III explains the capacitor voltage balancing method, along with the switching reduction algorithm. In Section IV, the switching losses of the converter are modeled. Section V is dedicated to the start-up procedure and the proposed method to pre-charge the capacitors. Finally, Section VI demonstrates the experimental verification of the proposed methods.

II. Reference Frame (d-q) Control Method

For the sake of clarity, the *d-q* model and control of the FCAR are explained here. Figure 1 shows the topology of the rectifier.

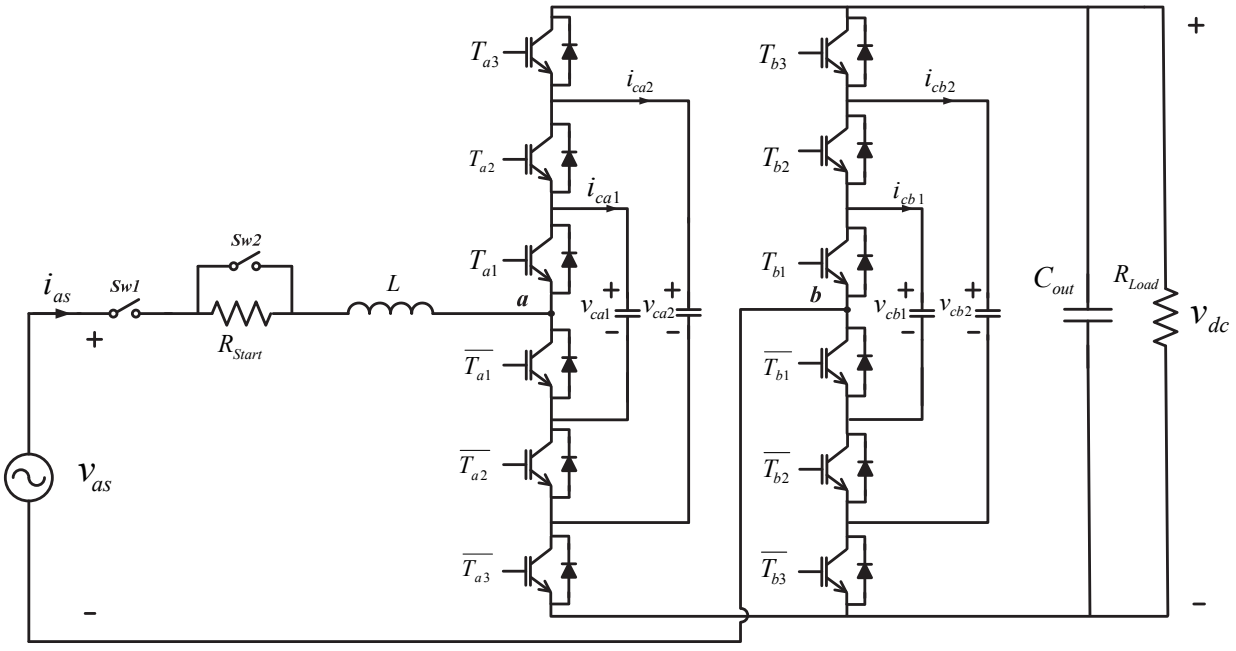

Figure 1. FCAR circuit along with the start-up circuit.

By neglecting the losses in the converter, the input and output equations of a single-phase rectifier are given by

$$v_{as} = L\frac{di_{as}}{dt} + v_{ab} \tag{1}$$

$$C_{out}\frac{dv_{dc}}{dt} = \frac{P_{rect}}{v_{dc}} - \frac{v_{dc}}{R_{out}} \tag{2}$$

where P_{rect} is the instantaneous input power of the rectifier and is defined by $P_{rect}=v_{ab}\cdot i_{as}$.

In order to use the *d-q* transformation [16], the single-phase system should be transformed into a two-phase system by generating an imaginary phase that is 90 degrees delayed with respect to the original one. If the input voltage source is defined as

$$v_{as} = v_m \cos(\omega t) \tag{3}$$

then the two-phase system with α and β phases is determined by

$$v_\alpha = v_{as} = v_m \cos(\omega t) \tag{4}$$

$$v_\beta = v_m \sin(\omega t). \tag{5}$$

By transforming this system into a d-q frame that rotates with synchronous speed, i.e., ω, the *d* and *q* components of the variable can be found. In this paper, the *d* and *q* axes are defined based on [16]. The synchronous frame transformation of the two-phase system is repeated here

$$\begin{bmatrix} f_q \\ f_d \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ \sin(\omega t) & -\cos(\omega t) \end{bmatrix} \begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} \tag{6}$$

where *f* can be a voltage or current. By applying this transformation on the ac variable and equations, the rectifier equations in the *d-q* system are obtained [14] as

$$v_m = L\frac{di_q}{dt} + L\omega i_d + v_q \tag{7}$$

$$0 = L\frac{di_d}{dt} - L\omega i_q + v_d \tag{8}$$

$$C_{out}\frac{dv_{dc}}{dt} = \frac{v_q i_q + v_d i_d}{2v_{dc}} - \frac{v_{dc}}{R_{out}} \tag{9}$$

where v_q and v_d are q and d components of v_{ab} (note that v_{ab} is a sinusoidal waveform). The equivalent circuit of a single-phase rectifier in the *d-q* system is shown in Figure 2.

The control diagram of the active rectifier is shown in Figure 3. In this figure, the control variables, such as i_{as}, v_{as}, v_{dc}, and the switch commands are defined in Figure 1. The transformation matrix in (6) is used in the "synchronous demodulator" block. In this control, the *q* axis is used to regulate the dc output voltage, while the control in the *d* axis ensures the unity power factor (for a unity power factor, i_d^* should be set to zero).

Using the following equations, the commanded *q* and *d* axis voltages are translated into a modulation index and a phase angle:

$$m = \frac{\sqrt{v_q^2 + v_d^2}}{v_{dc}} \tag{10}$$

$$\varphi = tan^{-1}(-\frac{v_d}{v_q}). \tag{11}$$

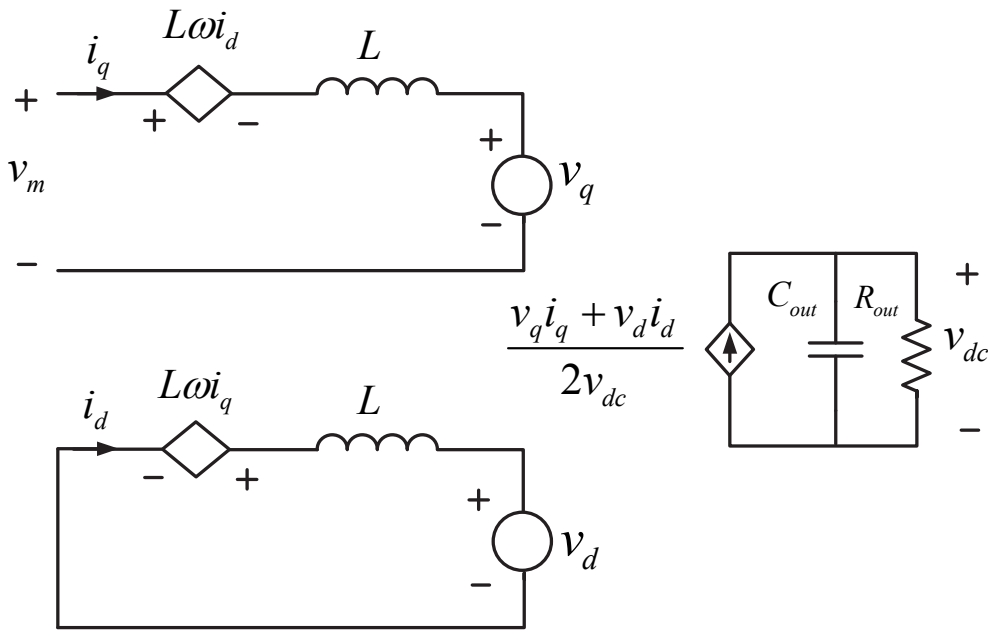

Figure 2. Equivalent circuit model of a single-phase rectifier.

Herein, the standard phase disposition PWM method [21, 35, 36], also called level-shifted PWM modulation [37] with 2(n−1) vertically-stacked triangular waveforms, is used, in which n is the number of levels of the FC converter. Using the calculated control variable, the new modulation index for the phase disposition method is given by

$$D_{ab} = (n-1)(1 + m\,cos(\omega t + \varphi)). \tag{12}$$

Note that D_{ab} is scaled in 0 to n−1 range. In the next step, $Level_{base}$ is defined as the largest integer not greater than D_{ab} (i.e., $floor(D_{ab})$ or $\lfloor D_{ab} \rfloor$). The final modulation index used for PWM is given by

$$m_{PWM} = D_{ab} - Level_{base}. \tag{13}$$

Finally, this value, which is the output of PWM and can be either zero or one, is added to $Level_{base}$ and generates $Level_{ab}$, which determines the level of the ac side of the rectifier (i.e., v_{ab}). $Level_{ab}$ is one of the variables used as an input variable of the table (described in the next section) to find the switching set at each switching interval.

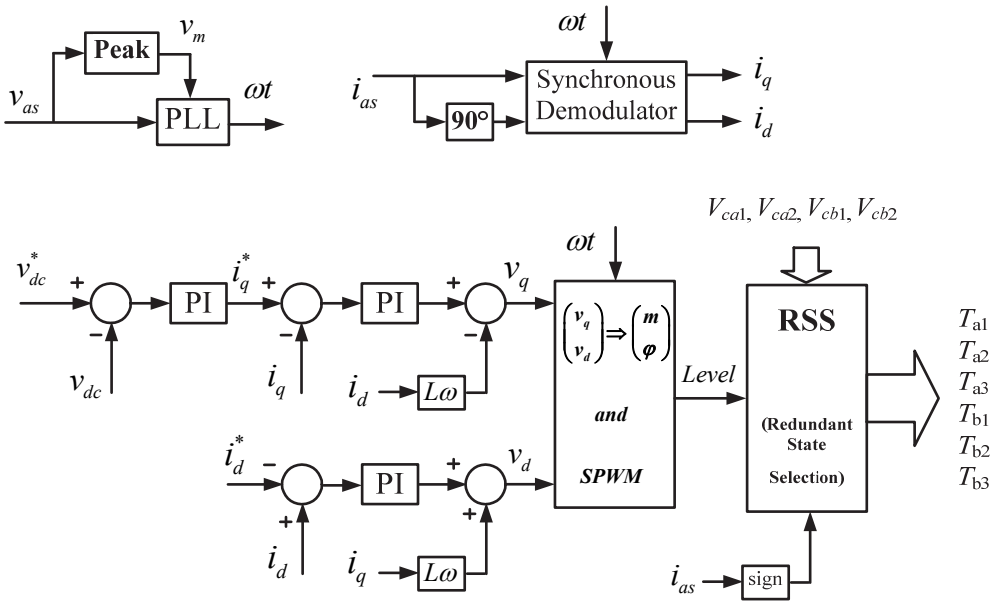

Figure 3. Control diagram of the active rectifier.

III. RSS FOR CAPACITOR VOLTAGE BALANCING

In this section, the proposed voltage balancing method and the online switching reduction method are elaborated upon. The general goal of this section is to find the best state from the pool of redundant states that generates the desired voltage level while simultaneously helping to regulate the flying capacitors voltages. In addition, the online

algorithm attempts to pick the specific state that leads to a reduction of switching losses. There are two levels of redundancy, which will be described later. This section is generalized for an FCAR with n levels or (n−1) flying capacitors in each leg. Although this method is presented for a rectifier, it can be used for a flying capacitor inverter also.

Figure 4 shows the RSS block that generates the gate signals for the switches in the FCAR. The first part of the RSS contains a look-up table that is generated offline. In the first part, based on the desired voltage level and voltage condition of the flying capacitors, as well as the direction of the current, a list of best states are selected that help to regulate the flying capacitors. In the second part, from among the list of best states, a state is selected that has minimum changes compared with the previous state sent to the FCAR switches to ensure a reduction in the switching losses. In the following subsection, each part of the RSS block is described.

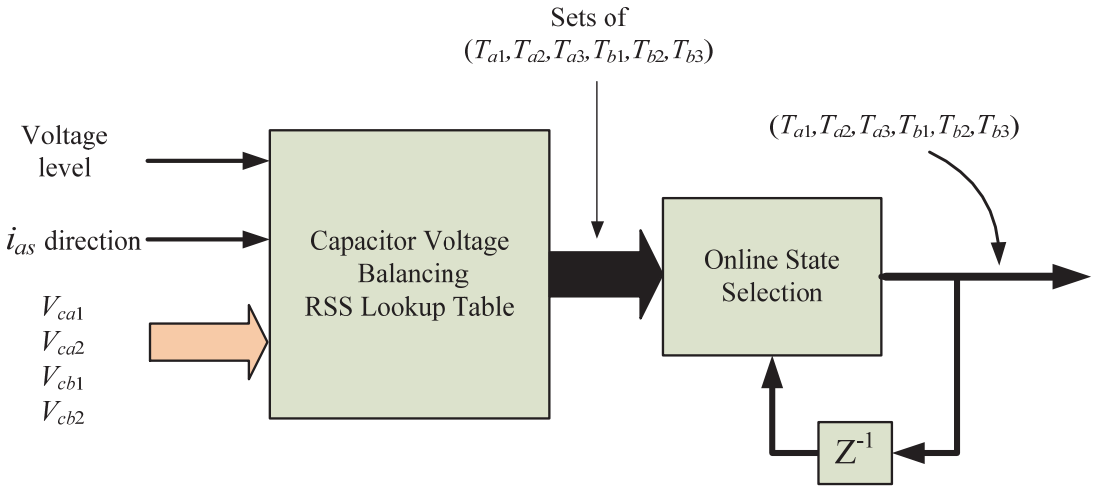

Figure 4. RSS block that generates the gate signals for the switches.

A. Offline RSS

This subsection explains the derivation method of the RSS table for finding the best states for balancing the flying capacitor. The following variables are defined to explain the method:

$$T_{ai}\,, T_{bi} = \begin{cases} 1 & ON \\ 0 & OFF \end{cases} \tag{14}$$

$$V_{ai} = \begin{cases} 1 & v_{cai} < v_{cai}^{*} \\ -1 & v_{cai} > v_{cai}^{*} \end{cases} \quad , \quad V_{bi} = \begin{cases} 1 & v_{cbi} < v_{cbi}^{*} \\ -1 & v_{cbi} > v_{cbi}^{*} \end{cases} \tag{15}$$

$$I_{as} = \begin{cases} 1 & i_{as} > 0 \\ -1 & i_{as} < 0 \end{cases} \tag{16}$$

where T_{ai} and T_{bi} are the status of each switch, V_{ai} and V_{bi} are flags that determine the voltage balance status of each capacitor compared to their desired voltage levels, and I_{as} denotes the input current direction (see Figure 1). Using the defined flags, the direction of the current for each flying capacitor can be expressed as

$$I_{cai} = \left(T_{ai} - T_{a(i+1)}\right) I_{as} \quad , \quad I_{cbi} = \left(T_{b(i+1)} - T_{bi}\right) I_{as}. \tag{17}$$

The output voltage level (v_{ab}) generated by the switching state is given by

$$Level_{ab} = \sum_{i=1}^{n-1} (T_{ai} - T_{bi}). \tag{18}$$

In order to compare the effect of each state on the voltage balancing of the capacitors, a goodness index is defined as

$$\begin{aligned} GD_{index} &= \sum_{i=1}^{n-2} (I_{cai}\, V_{ai} + I_{cbi} V_{bi}) = \\ &= I_{as} \sum_{i=1}^{n-2} [\left(T_{ai} - T_{a(i+1)}\right) V_{ai} + \left(T_{bi} - T_{b(i+1)}\right) V_{bi}]. \end{aligned} \tag{19}$$

In (19), the current direction flag of each capacitor is multiplied by the voltage balance status of the corresponding capacitor. Therefore, each flying capacitor that is approaching its desired voltage level will add 1 to the goodness index, and each capacitor that is deviating from its desired voltage subtracts 1 from the goodness index. In fact, the value of the goodness index is a criterion that determines the extent to which a switching state can be useful for balancing the voltages of the flying capacitors at each condition. Consequently, a state with a higher goodness index is superior to other redundant states that can generate the same output voltage level in each specific input current direction. The maximum value of the goodness index is equal to the number of flying capacitors, i.e., 2(n−2). In order to connect all of the capacitor voltage balancing statuses in a single variable, a variable referred to as the capacitor voltage index is defined as

$$V_{Cindex} = \sum_{i=1}^{n-2} 2^{i-1} V_{cai} + 2^{n-2} \sum_{j=1}^{n-2} 2^{j-1} V_{cbi}. \tag{20}$$

The capacitor voltage index is used to organize the final RSS look-up table; it also provides a unique value for each capacitor voltage balancing status.

In order to find the RSS table, first all of the possible statuses of switches (i.e., T_{ai} and T_{bi} with $2^{2(n-1)}$ combinations), the input current direction (i.e., I_{as} with 2 combinations), and the voltage status of all of the flying capacitors (i.e., $V_{Cstatus}$ with $2^{2(n-1)}$ combinations) are listed in a large table. There will be 2^{4n-5} possible combinations. Then, using (18) and (19), the output voltage level and the goodness index for each condition, respectively, are found. Next, the table is sorted so that for each voltage level, capacitor balance index, and current direction, all of the goodness indices and switch

states are listed. Then, for each condition, only those states are selected that have maximum goodness indices. In other words, the selected states are those that can help balance the voltage of a larger number of capacitors. In some conditions, there are several states that have the maximum goodness index; all of these states are retained in the final table. Unlike previous publications [2, 11, 14, 26], this paper proposes keeping all the states with superior goodness indices in the table and using them for switching event reduction.

In this study, there are 4 voltage levels for each leg (i.e., n=4). Among all $2^{11} = 2048$, only 368 appear in the final RSS table, and in 80 operating conditions, more than one switching state is stored in the table. For clarification purposes, the selected redundant states in which $Level_{ab}$ is +1 and the input current direction is positive are tabulated in Table I. According to this table, in one condition there are six redundant states with the maximum possible goodness index for that condition.

To clarify the concept of the goodness index and the voltage balancing method, two cases from Table I are illustrated in Figures 5 and 6. In Table I, two redundant states are presented for the [V_{b2} V_{b1} V_{a2} V_{a1}]=[−1 1 1 −1] case (highlighted in gray). In this case, the cb2 and ca1 capacitors are undercharged, while the cb1 and ca2 capacitors are overcharged. In Figure 5, the conduction path in the circuit is shown when [T_{a1} T_{a2} T_{a3} T_{b1} T_{b2} T_{b3}]= [1 0 1 0 0 1]. In this case, ca1 and cb2 are charging and ca2 is discharging, while cb1 is not engaged; therefore, its voltage does not change. Because the voltages of three of the capacitors are becoming balanced, the goodness index for this case is 3. Likewise, Figure 6 shows the case when [T_{a1} T_{a2} T_{a3} T_{b1} T_{b2} T_{b3}]= [1 0 1 1 0 0]. In this case, ca1 is charging while ca2 and cb1 are discharging, meaning that three capacitors are

getting balanced at the same time, which yields a goodness index of 3. As expected, both cases depicted in Figures 5 and 6 balance the voltage of the same number of capacitors (i.e., three capacitors) which is the maximum number of capacitors that can be regulated in this case.

TABLE I
A SECTION OF RSS TABLE FOR $LEVEL_{AB}$=1 AND I_{AS}=1

V_{b2}	V_{b1}	V_{a2}	V_{a1}	$[T_{a1}\ T_{a2}\ T_{a3}\ T_{b1}\ T_{b2}\ T_{b3}]$
−1	−1	−1	−1	110001
			1	010000, 011001, 110001
		1	−1	101001
			1	011001
	1	−1	−1	110001, 110100, 111101
			1	010000, 011001, 011100, 110001, 110100, 111101
		1	−1	101001, 101100
			1	011001, 011100, 111101
1	−1	−1	−1	110010
			1	011010, 110010
		1	−1	101010
			1	011010
	1	−1	−1	110100
			1	010000, 011100, 110100
		1	−1	101100
			1	011100

B. Online RSS for Switching State Reduction

The offline part of the RSS look-up table provides a list of the best redundant states in each operating condition. Then, in the switching loss reduction section, a state is

selected that has minimum changes compared with the previous state sent to the gates in the last switching cycle. This means that fewer IGBT switching events will change their conduction status (i.e., ON or OFF) in the new switching cycle. This algorithm leads to fewer switching events in a given fundamental period cycle, thereby reducing switching losses. The online part can be implemented using an exclusive OR (i.e., XOR) logic command of all possible switching states against the last switching state. Therefore, the online part is a very fast processing procedure that can be executed with very few cycles of the digital processor.

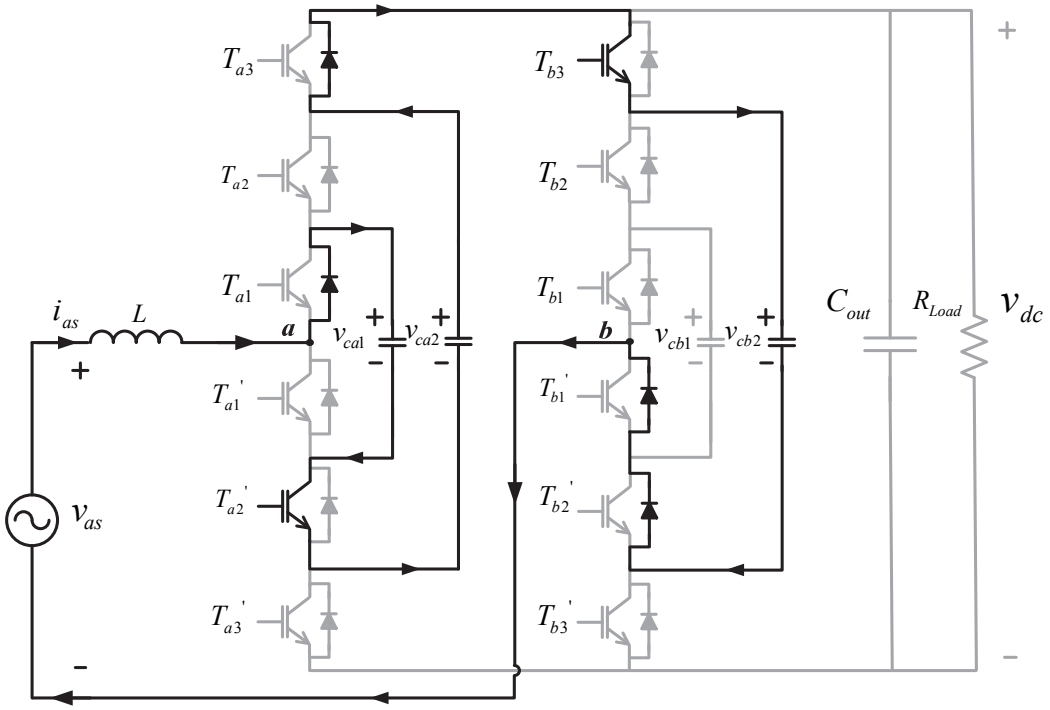

Figure 5. Conduction path when [T_{a1} T_{a2} T_{a3} T_{b1} T_{b2} T_{b3}] = [1 0 1 1 0 0] and I_{as}=1.

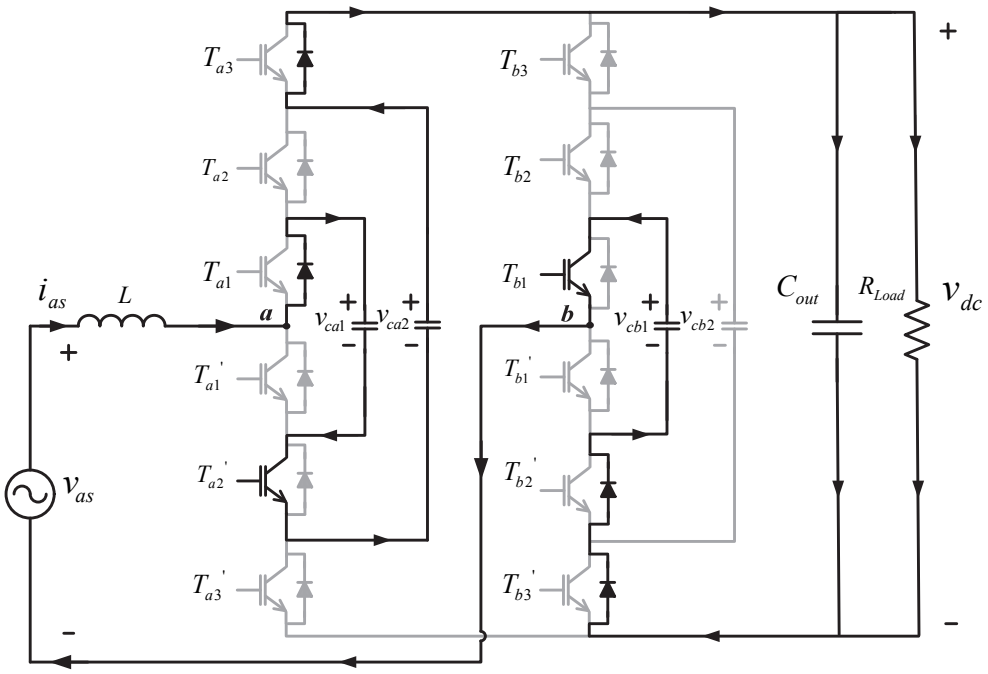

Figure 6. Conduction path when [T_{a1} T_{a2} T_{a3} T_{b1} T_{b2} T_{b3}] = [1 0 1 0 0 1] and I_{as}=1.

IV. Switching Losses Modeling

In order to display the effect of the switching loss reduction algorithm, the switching losses of FCAR are modeled in this section. To model the switching losses in each switching event, the turn-on or turn-off losses of the switches and diodes of the circuit are calculated based on the magnitude and direction of their current. During normal operation when all the capacitors are balanced, the blocking voltage of the switches is $v_{dc}/3$. Therefore, the energy loss of the switches when they are turned on (i.e., E_{onT}) or turned off (i.e., E_{offT}), and diode losses due to reverse recovery (i.e., E_{offD}), can be defined as

$$E_{onT} = E_{ONT}(i_{as}) * \frac{v_{dc}}{3V_{cc}} \tag{21}$$

$$E_{offT} = E_{OFFT}(i_{as}) * \frac{v_{dc}}{3V_{cc}} \tag{22}$$

$$E_{offD} = \frac{1}{6} Q_{rr} v_{dc} \tag{23}$$

where V_{cc} is the test voltage for switching data, which is usually provided by the switch manufacturer; $E_{ONT}(i_{as})$ is the turn-on energy loss and $E_{OFFT}(i_{as})$ is the turn-off energy loss, both of which depend on the current of the switch; and Q_{rr} is the reverse recovery charge of the diodes. Here, the switching losses of leg *a* are derived. A similar method can be extended to calculate the losses in leg *b*. To explain the switching loss calculation method, several variables are defined as

$$\Delta T_{ai} = T_{ai}(k) - T_{ai}(k-1) \tag{24}$$

$$\Delta T_{ai}^{+} = \begin{cases} 1 & \Delta T_{ai} = 1 \\ 0 & otherwise \end{cases}, \quad \Delta T_{ai}^{-} = \begin{cases} 1 & \Delta T_{ai} = -1 \\ 0 & otherwise \end{cases} \tag{25}$$

$$I_{as} = \begin{cases} 1 & i_{as} > 0 \\ -1 & i_{as} < 0 \end{cases} \tag{26}$$

where $T_{ai}(k)$ and $T_{ai}(k-1)$ are the current and last switching states of switch T_{ai}, and ΔT_{ai} denotes the switch state change variable, which can be −1, 0, or 1. ΔT^{+}_{ai} is the switch on-to-off detector (positive edge of gate command), which was 1 only when the switch was previously off; it is turned on in the current switching event. Similarly, ΔT^{-}_{ai} is the switch on-to-off detector (negative edge of gate command), which was 1 only when the switch was previously on; it is turned off in the current switching event.

In the flying capacitor topology, when a gate signal of a switch is 1 (T_{ai}=1), the current direction determines that either the switch or its corresponding diode is on. For example, if ΔT^{+}_{a2} is 1 and I_{as} is −1 (I_{as} is defined in (16)), this means that the switch was

turned off but has now been turned on, and the current is beginning to pass through the IGBT. Therefore, one instance of energy loss for the IGBT (i.e., E_{onTa2}) should be added to the current value of the switching losses of the circuit. At the same time, the diode of the complementary switch (T'_{a2}) is turned off; therefore, one instance of energy loss for the diode reverse recovery should also be added.

Based on the defined variables, a closed form equation for the switching losses of leg *a* of the converter can be written as

$$E_{swloss,a}(k) = E_{swloss,a}(k-1) + \sum_{i=1}^{3}\left(\frac{1-I_{as}}{2}\Delta T_{ai}^{+}\left(E_{onT}+E_{offD}\right) + \frac{1+I_{as}}{2}\Delta T_{ai}^{-}E_{offT}\right) \quad (27)$$

Similarly, the switching losses for leg *b* can be developed. Using the described method, the switching losses of the FCAR are simulated with a 1.6 kVrms input, a 3 kV commanded output voltage, and a 450 Ω dc load.

In the experimental setup of the rectifier, CM75DU-24F IGBTs from Powerex are used, which are rated to 1200 V and 75 A. Thus, the switching data of this type of IGBT are also used in the simulation. The switching losses of the rectifier during the steady state for the described working operation are shown in Figure 7. In this figure, the switching losses both with and without using the switching loss reduction algorithm are illustrated. As shown, when the switching loss reduction algorithm is used, the switching power loss is reduced to 16.7 W; without using the algorithm, this value is approximately

18.4 W. Therefore, the switching losses decrease by about 9.2%. In both cases, the conduction loss of the converter is 91 W.

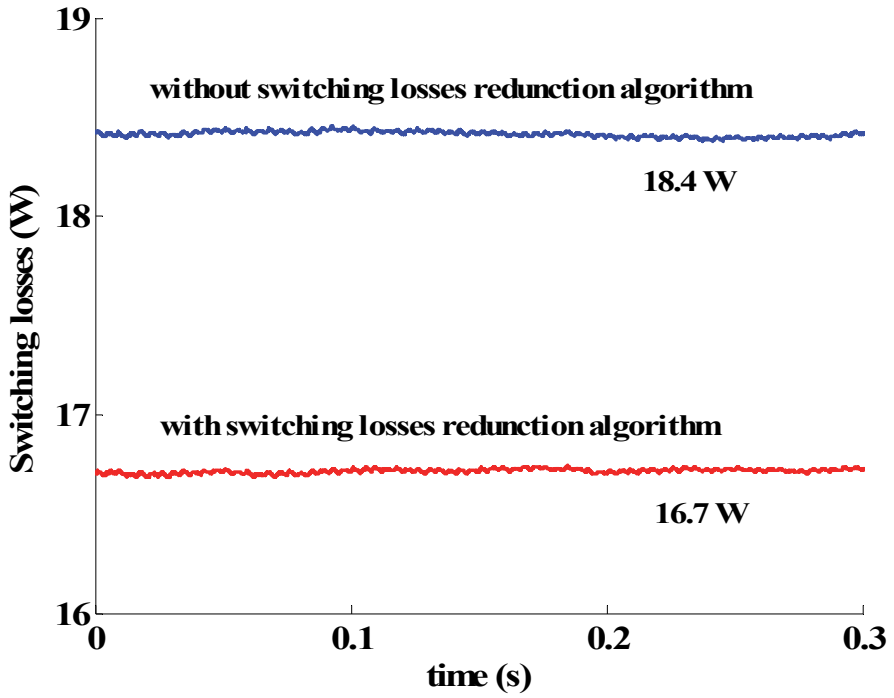

Figure 7. Switching losses with and without switching loss reduction algorithm.

V. START-UP PROCEDURE

In conventional active rectifiers, the output capacitor is charged during the start-up procedure to reduce the inrush current [32]. However, in the FCAR, flying capacitors also should be charged to limit the input inrush current and avoid causing excessive voltage stress on the switches. Limiting the inrush current is not only important for protecting the switches but also for avoiding exceeding the maximum current that

capacitors can tolerate. For this purpose, a start-up procedure has been proposed to charge the output capacitor and all the flying capacitors before the normal operation of the active rectifier. The capacitors are charged during the start-up procedure in several consecutive steps. As shown in Figure 1, two contactors are used to connect or disconnect the input voltage and enter or remove the start-up resistor from the circuit. The value of the input resistor is chosen so that the inrush current during the first cycle is less than the maximum tolerable current of the capacitors [16, 32].

For better operation immediately after starting the rectifier, it is important not only to charge the capacitors but also to have the correct voltage ratio. In other words, the pre-charged voltage of the inner flying capacitors should be one-third of the pre-charged voltage of the output capacitor. Similarly, the pre-charged voltage of the outer flying capacitor should be two-thirds of the pre-charged voltage of the output capacitor. In this case, all the voltage levels of v_{ab} are generated properly immediate after beginning to operate the rectifier. For this reason, the peak input voltage is measured using the input voltage sensor. Using online steady-state calculation in DSP, the final value of the output voltage is calculated, and the correct reference value for the voltage of flying capacitors is used for the start-up procedure. This ensures the correct voltage ratio for capacitors after the start-up procedure.

Several start-up procedure and shutdown modes are listed in Table II. The start-up procedure consists of three modes. In the first two modes, the input resistor is in the circuit to limit the input current. In this table, '*D*' stands for 'Disable', which means that both complementary switches are OFF. Due to the topology, if the voltage of each capacitor exceeds the voltage of the outer capacitor(s), then the inner capacitor discharges

to the outer capacitor(s) through the diodes until all of them reach the same voltage level. In the start-up procedure, at first all of the capacitors are charged until their voltage reaches $V_{dc\_start}/3$ (where V_{dc_start} is the final voltage of the output capacitor after the start-up procedure). At this time, the mode changes, and the inner capacitors are not charged any further (mode 1). The charging process continues until the voltage of the outer capacitors and the output capacitor reaches $2/3\times V_{dc\_start}$ (mode 2). At this time, the outer capacitors are removed from the circuit and are not charged anymore.

TABLE II
START-UP AND SHUTDOWN OPERATION MODES

Mode	Process	$Sw1$	$Sw2$	T_{a1}, T_{b1}	T_{a2},T_{b2}	T_{a3}, T_{b3}	Charged capacitor
1	Start-up	1	0	*'D'*	0	0	$C_{out,}$ C_{a2}, $C_{b2,}$ C_{a1}, C_{b1}
2	Start-up	1	0	*'D'*	*'D'*	0	$C_{out,}$ C_{a2}, C_{b2}
3	Start-up	1	1	*'D'*	*'D'*	*'D'*	C_{out}
4	Normal	1	1	PWM	PWM	PWM	-
5	Shutdown	1	1	*'D'*	*'D'*	*'D'*	-
6	Shutdown	1	0	*'D'*	*'D'*	*'D'*	-
7	Shutdown	0	0	*'D'*	*'D'*	*'D'*	-

In modes 1 and 2, with a positive current (i.e., $i_{as}>0$), the flying capacitors in leg *a* are charged, while with a negative current, those in leg *b* are charged. Here, only the current flow in mode 2 when i_{as} is positive (or, equivalently, $i_{as}>0$) is shown in Figure 8, though other modes with different polarity of input current can be driven in the same fashion. As shown, in this mode, only T'_{a3} and T'_{b3} are switched ON, and the other

switches are left OFF. When i_{as}>0 C_{a2} and C_{out} are charged while in the negative alternative, as are C_{b2} and C_{out}. In the negative alternative, the voltage of C_{a2} remains constant, and C_{b2} starts charging until its voltage reaches that of the output capacitor. In this case, both C_{b2} and C_{out} charge with each other.

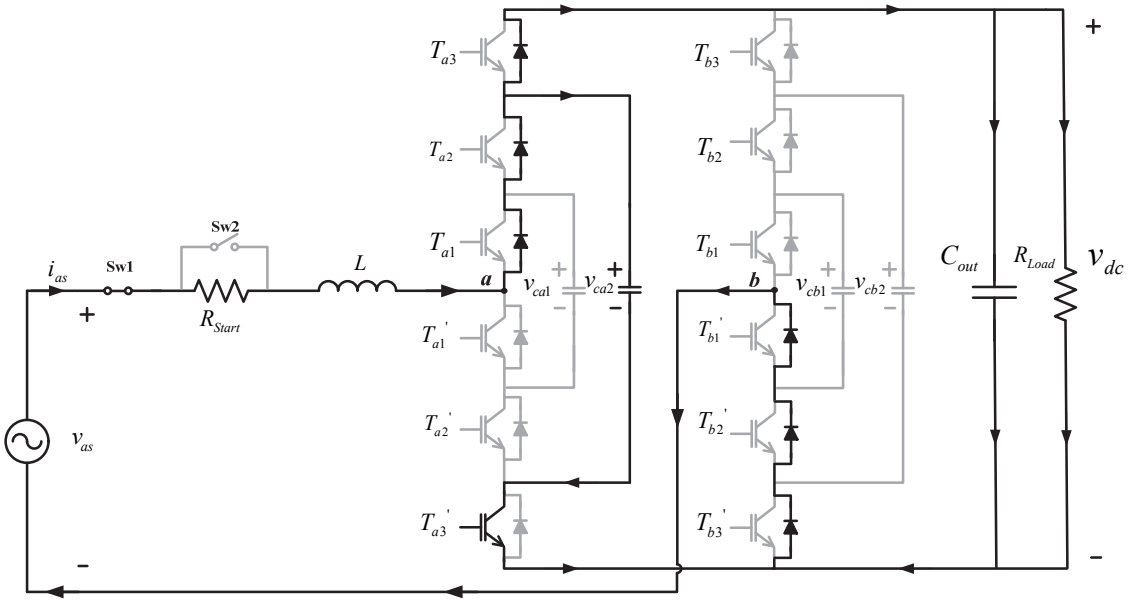

Figure 8. Start-up mode 2: Charging the outer flying capacitors and output capacitor.

In mode 3, *Sw*2 is turned on shorting the input resistor and all the switches are disabled allowing the output capacitor to charge to its maximum voltage level while the other capacitors remain at the desired value. In mode 4, normal PWM switching commands are sent to switches. During the shutdown process, IGBTs first are

commanded off, and then the series (start-up) resistor comes into the circuit; finally, the input contactor (i.e., *Sw*1) disconnects the input source to ensure a safe turn-off process. In order to avoid an unwanted voltage surge on the inductor, the source is detached when the inductor current is zero.

VI. Experimental Results

In order to verify the proposed methods, a 2-kW hardware prototype FCAR was constructed. The hardware setup is a low voltage prototype of a medium voltage rectifier for an SST. Figure 9 shows the hardware setup. The prototype is built in three different sliding shelves. The top shelf is dedicated to the control circuits and signal conditioning boards.

The middle shelf consists of capacitors, as well as IGBTs and their drivers and sensor boards. The bottom shelf input inductor contains the hardware current protection, dc power supplies, and contactors. A TMS320C2812 DSP from Texas Instruments is used for processing, and IGBT gate commands are passed from the top shelf to the middle shelf using fiber optic cables. The bank of capacitors is designed to decrease the length of wire and stray inductances. CM75DU-24F IGBTs from Powerex are used, which are rated at 75 A and 1200 V. The equivalent output and outer capacitors are 3.9 mF, and the equivalent capacitances of the inner capacitors are 7.8 mF. A switching frequency of 6 kHz is used in all experiments.

Figure 10 illustrates the experimental result for the operation of FCAR in all modes, including start-up, normal operation, and shutdown procedures. In this figure,

each mode is shown on the top plot, and descriptions for each mode are provided in Table II. In this test, the input voltage is 230 Vrms, the commanded output voltage is 360 V, and the load is 100 Ω.

Figure 9. Prototype of the FCAR.

In Figure 10, the output voltage of the rectifier (v_{dc}), the voltage of capacitors in leg *a* (v_{ca1} and v_{ca2}), and the input current (i_{as}) are shown. The voltage of the capacitors in leg *b* are almost the same as those in leg *a*; therefore, they are not shown. As shown in mode 1, all of the capacitors charge with each other, and when the voltage reaches 81 V, the v_{ca1} stops charging and mode 2 begins. In mode 2, v_{ca2} and v_{dc} continue to charge until the voltage of v_{ca2} reaches 162 V, thereby ending mode 2. In mode 3, only the output capacitor is charged while the bypassing contactor (i.e., sw2) is closed.

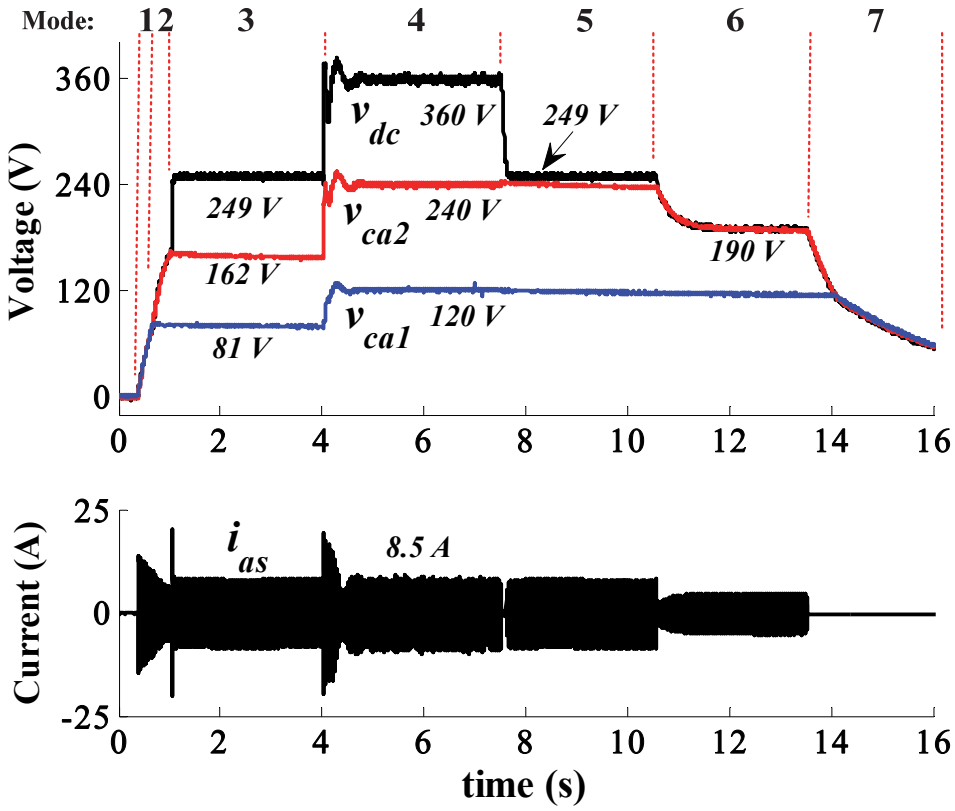

Figure 10. Lab results of FCAR operation modes: start-up, normal, and shutdown procedures.

In order to show the effect of pre-charging the capacitors in the inrush current, two different start-up cases are considered, and simulations and experimental results for these cases are provided. In both test cases, the input voltage is 190 Vrms, and the commanded output voltage is 300 V with a 1500-W DC load.

In the first case, only the output capacitor is charged, and all of the flying capacitors are left discharged before the rectifier begins to operate. The simulation waveforms for this case are shown in Figure 11.

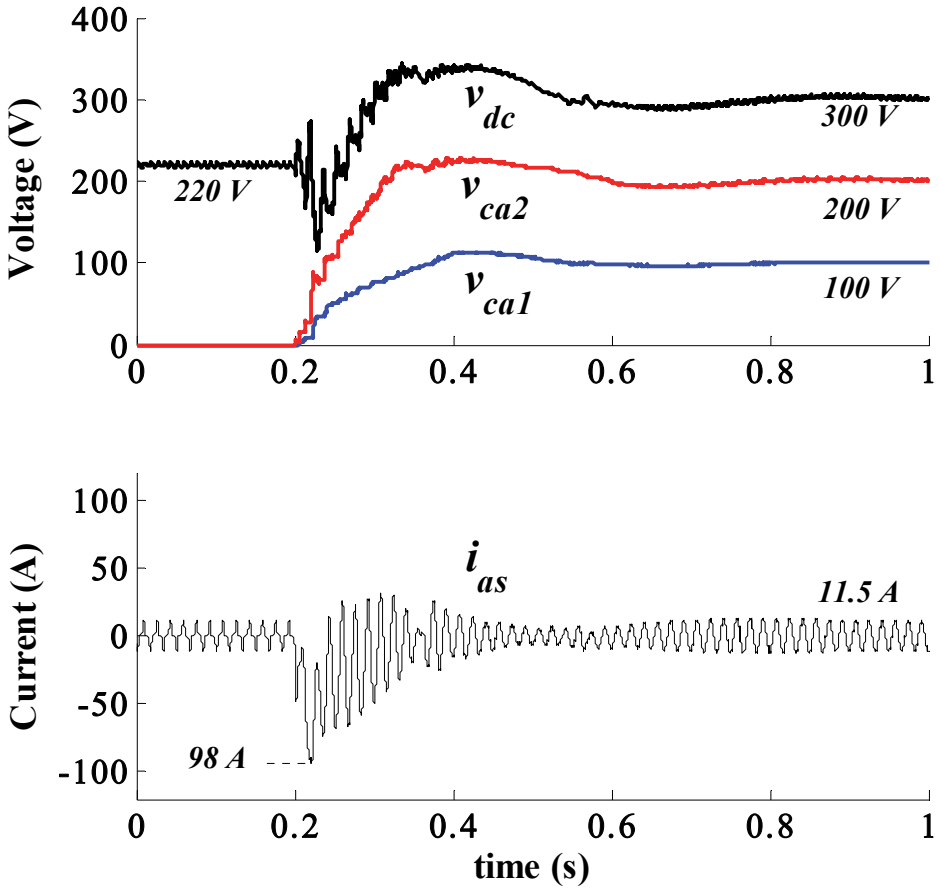

Figure 11. Simulation waveforms when only the output capacitor is pre-charged.

In Figure 12, the experimental results for the same case are illustrated. In these figures, the voltages of v_{ca1} and v_{ca2} are zero before 0.2 s; however, the output capacitor is charged. At 0.2 s, the rectifier begins to operate, the output voltage reaches 300 V using the control algorithm, and the voltages of the capacitors are regulated accordingly. In the simulation case, the peak of the inrush current immediately after operation begins is 98 A, while in the experimental case, this value is approximately 101 A. All of the components in the rectifier should be able to withstand this inrush current for a short period of time to avoid permanent damage.

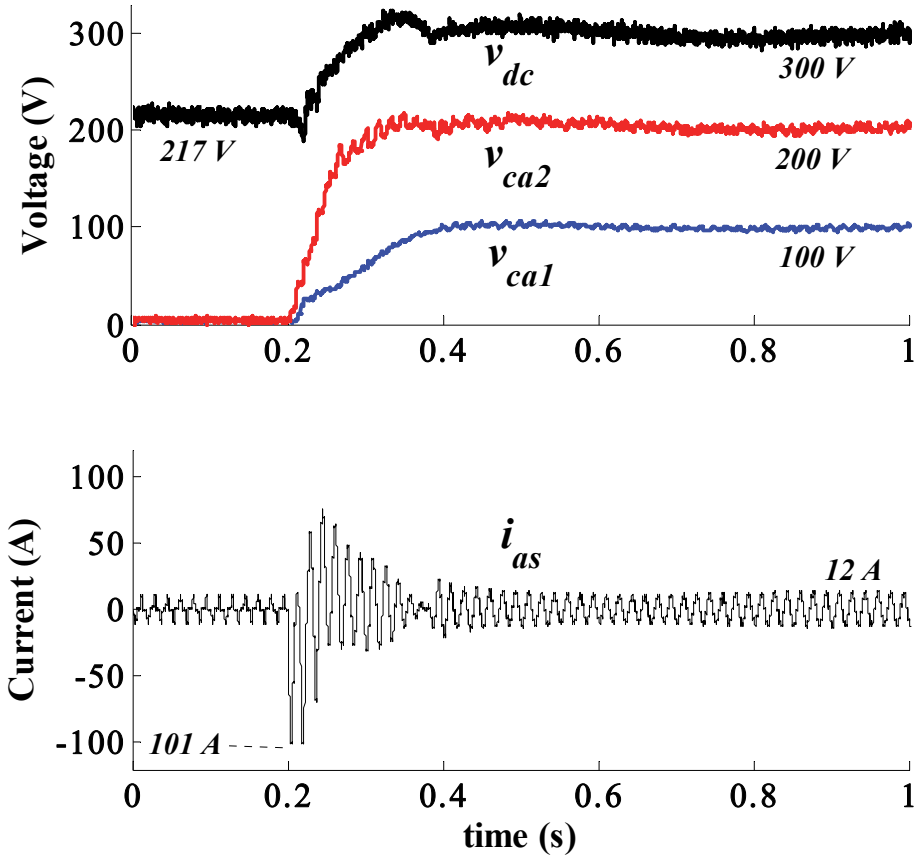

Figure 12. Experimental waveforms when only the output capacitor is pre-charged.

In the second case, before the rectifier begins to operate, the flying capacitors are also pre-charged to 1/3 and 2/3 of the voltage of the output capacitor using the start-up procedure described in Section V. The simulation and experimental results for this case are depicted in Figures 13 and 14, respectively.

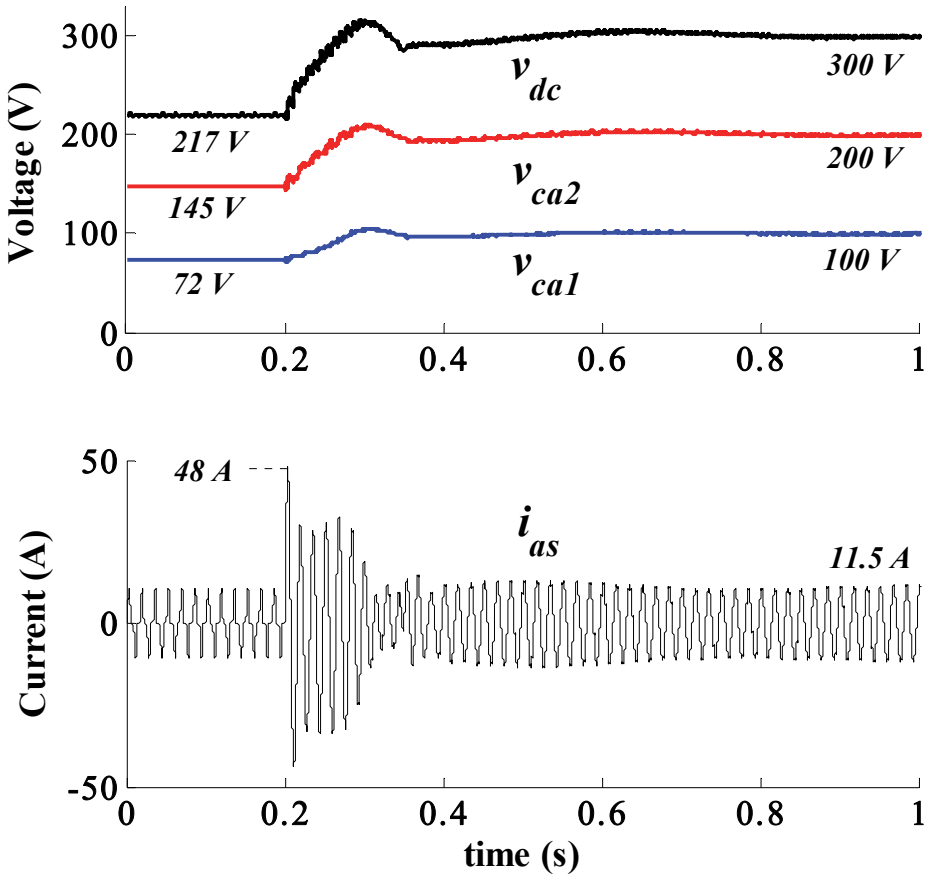

Figure 13. Simulation waveforms when all of the capacitors are pre-charged.

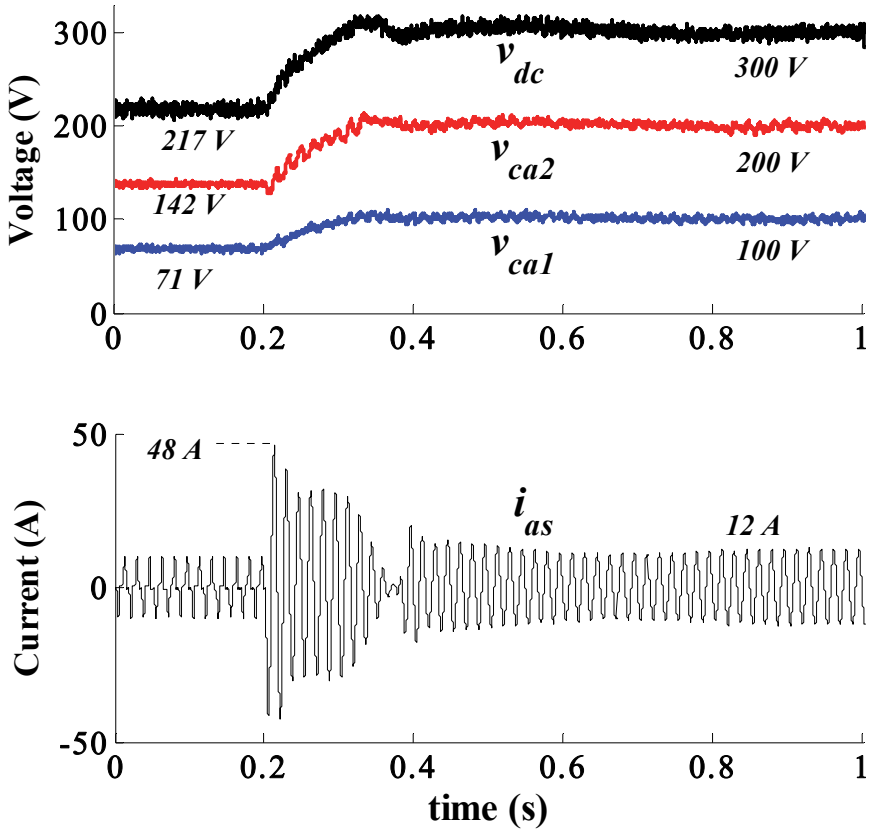

Figure 14. Experimental waveforms when all of the capacitors are pre-charged.

As shown in both figures, the peak of the inrush current is approximately 48 A, which is almost half of the peak of the current in the first case (i.e., with only pre-charging the output capacitor). In other words, the inrush current realized when the rectifier begins to operate and when all of the capacitors are pre-charged is reduced to half of the current realized when only the output capacitor is pre-charged. Note that the scale in the current plot of Figures 12 and 14 is different than that in Figures 11 and 13. In both cases, the experimental and simulation results match closely.

In this paper, voltage references for the capacitors are determined based on the real value of the output voltage rather than the commanded voltage. This yields an even

distribution of excessive voltages during transients to all the switches and capacitors and avoids overvoltage for a single switch or capacitor. In addition, because the capacitor voltage ratios are maintained constant during the transients, the synthesized voltage of the rectifier suffers less distortion.

The normal operation of the rectifier with 130 Vrms input, 210 V commanded output, and a 1700-W load is shown in Figure 15. The input voltage and input current with different scales are depicted on the same plot to show the operation of the rectifier at a unity power factor. In this figure, the proper formation of voltage levels shows the successful voltage balancing of the capacitors.

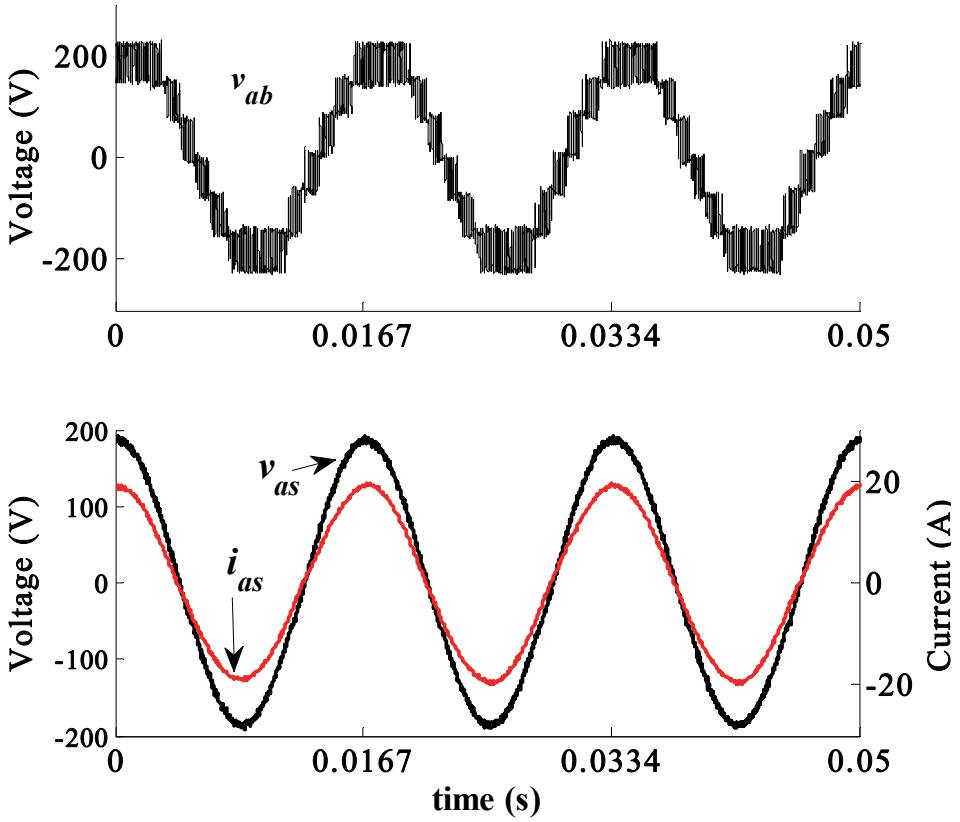

Figure 15. Normal operation of the FCAR with 1700-W load.

In the next three experimental cases, test results are provided that show the proper operation of the output voltage control of the FCAR and capacitor voltage balancing method. The rectifier under load changes from 850 W to 1700 W and back to 850 W with a 130 Vrms input and commanded 210 V output voltage is depicted in Figure 16. According to the figure, all the flying capacitors are regulated at their desired voltages in all three load conditions.

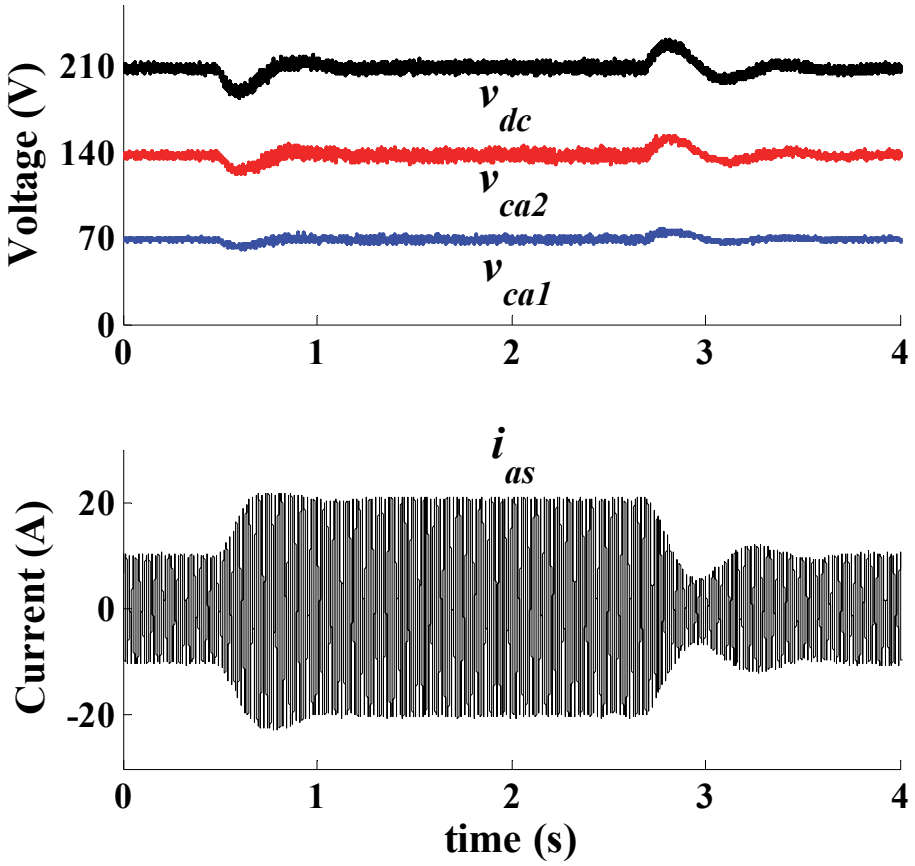

Figure 16. Rectifier under load change.

The designed FCAR is intended to be used as the first stage of an SST (medium voltage grid connected converter), so it should be able to overcome input voltage changes in the grid, especially voltage sags due to overloading in the grid. As a result, the following voltage sag test is conducted, the results of which are presented in Figure 17. In this figure, while the load is kept constant at 1700 W, the input voltage is changed from 135 Vrms to 80 Vrms and then back to 135 Vrms.

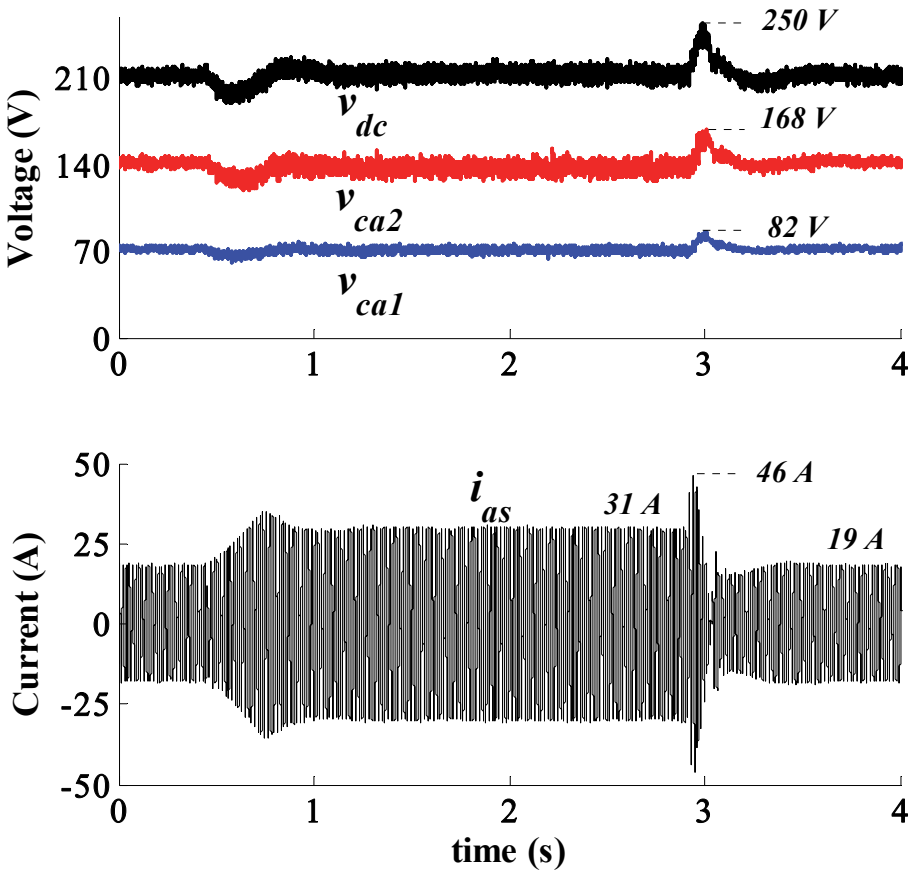

Figure 17. Response to input voltage change.

According to the figure, it takes around 0.3 s to return to the steady-state after the input voltage changes. In Figure 18, the commanded output voltage is increased from 230 V to 250 V at 0.4 s and then decreased to 210 V, while the load and input voltage are kept constant at 26 Ω and 135 Vrms. This test indicates that while the *d-q* control method is handling the change in the output voltage command, the capacitor voltage balancing system is able to regulate the voltage capacitors at different voltage levels, even during transients.

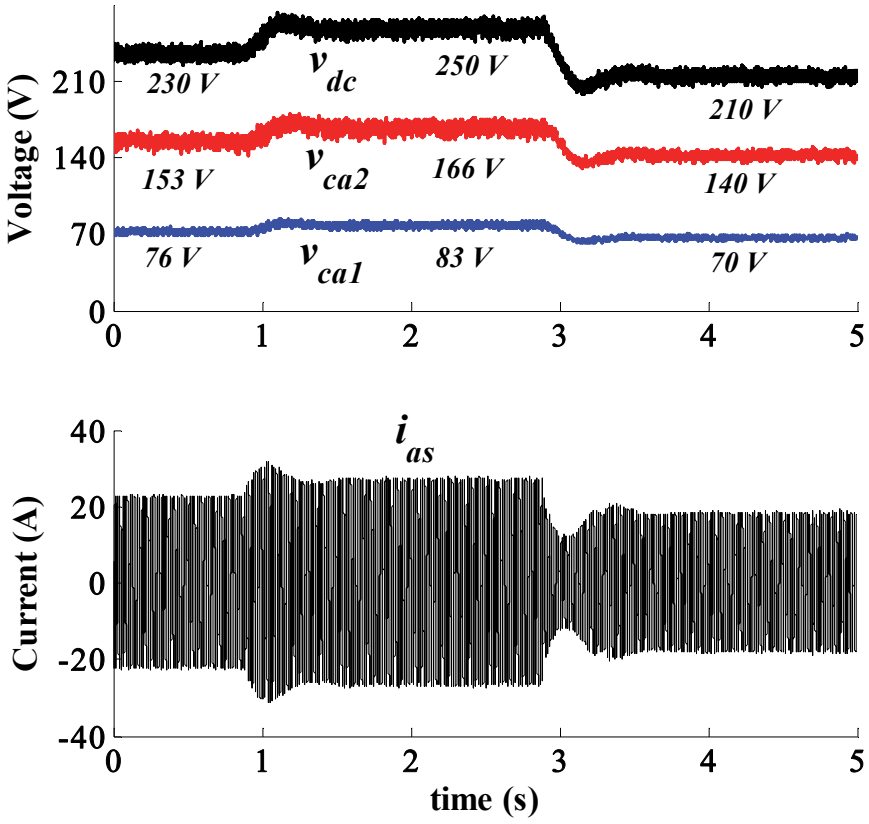

Figure 18. Response to a change in the output voltage command.

In order to test the switching loss reduction algorithm using the capacitor voltage regulation method under the same operating conditions, two different sets of experiments are conducted, with and without using the switching reduction algorithm. For this reason, during the steady-state operation of the FCAR, the number of times that each IGBT gate signal for the top switches in both legs are turned ON is counted for a 10-second period. The number of times that each switch is turned on during 10 second operation is tabulated in Table III. This table provides the results for two different cases with different loads (i.e., 26 Ω and 52 Ω loads), and for each case, switching counts are given for both with and without the switching loss reduction algorithm. As shown, the number of total switching counts is reduced in both cases. This indicates that the method has successfully decreased the number of switching events and consequently reduced switching losses in the converter.

TABLE III
NUMBER OF TURN ON TIMES FOR TOP SWITCHES IN EACH LEG AND FOR TWO DIFFERENT LOADS BOTH USING AND NOT USING THE SWITCHING REDUCTION ALGORITHM AT TWO DIFFERENT LOADS

R_{out} (Ω)		26		52	
Switching reduction method		with	without	with	without
Number of switch ON per second	T_{a1}	1704	1796	1666	1845
	T_{a2}	1330	1782	1236	1468
	T_{a3}	1241	1310	1197	1400
	T_{b1}	1521	1334	1499	1361
	T_{b2}	1274	1595	1201	1813
	T_{b3}	1568	1937	1681	1476
	Total	8638	9754	8480	9363
Overall change (%)		11.44		9.43	

VII. Conclusion

In this paper, a single-phase flying capacitor active rectifier with a reference frame (*d*-*q*) control method is studied. A redundant state selection algorithm is used to balance the flying capacitors under all operating conditions. Because the redundant state selection method leads to more switching losses, a method is proposed to handle this problem. Utilizing additional redundant states, an algorithm is designed that reduces the switching losses in the rectifier. In addition, a start-up procedure for safely starting the rectifier is added; it charges the flying capacitors to reduce the voltage stress over switches and the inrush current before start-up. Results show a reduction in the inrush current using this method. The provided simulation and experimental verification of the methods supports the concepts introduced herein.

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III. A Flexible Capacitor Voltage Regulation Method for Hybrid Multilevel Power Electronic Inverters

Abstract— In the multilevel inverter configuration used in this study, cascaded H-bridge cells are connected in series in each phase of a three-phase, three-level, neutral-point clamped (NPC) inverter. The NPC inverter is fed by a single dc voltage source, whereas all of the cascaded H-bridge cells are supplied by capacitors. In this study, in order to regulate the voltage across the H-bridge capacitors, a small fundamental harmonic is added to or subtracted from the original PWM reference of each H-bridge cell. In addition, the operation of the inverter is studied when a fault occurs in the cascaded H-bridge cells. A strategy for fault recovery and compensation using the remaining H-bridge cells in the corresponding phase is proposed. This method allows the inverter to operate fairly when one of the H-bridge cells is not functioning. Simulation results and laboratory experimentation verify the success of the capacitor voltage regulation and the fault recovery strategy.

I. INTRODUCTION

Multilevel power electronic converters have been gaining popularity in recent years due to their high voltage capabilities, high power quality, good electromagnetic compatibility (EMC), and acceptable switching loss [1-8]. The most common multilevel converters include the diode-clamped, flying capacitor, and cascaded H-bridge structures [3, 9, 10]. Among these topologies, the aspects that set cascaded H-bridge cells apart are

the advantages of modularity and independence in the switching frequency of each H-bridge cell [3, 9, 11]. This feature helps the cascaded H-bridge topology avoid excessive switching losses by allowing low switching frequency operation of high-voltage cells and high switching frequency operation of low-voltage cells [3, 5, 12]. However, each H-bridge cell requires an isolated voltage source, which increases the complexity and cost of the inverter [2, 6]. Recent research in this area has focused on replacing some of the isolated sources with capacitors [13-16]. This method reduces the cost of the converter by eliminating the need for individual, isolated dc voltage sources for all of the H-bridge cells. However, the voltage across the capacitors must be regulated while the converter is operating. In multi-phase applications, cascaded H-bridge cells connected to a dc voltage source can be replaced with a single multi-phase, multilevel inverter. The advantage of this approach is that only one dc voltage source is required. Also, the current ripple in the dc bus is reduced [12, 17]. Multi-phase, multilevel converters with diode-clamped as opposed to flying capacitor topologies have the advantage of using fewer capacitors because diode-clamped structures use only one chain of capacitors for all phases, while flying capacitor converters use separate sets of capacitors for each phase. The three-level diode-clamped converter which is also called NPC is the most common type of the diode-clamped converter in industry due to its automatic capacitor voltage balancing [18].

The topology of the investigated hybrid multilevel inverter is illustrated in Figure 1. The main inverter is a three-phase, three-level NPC inverter supplied with a single dc voltage source. Each phase of the NPC is connected in series with two cascaded H-bridge cells. The NPC is a high-voltage inverter switched at a square waveform pattern or fundamental line frequency (four switching instances per cycle); however, the switching

strategy of the H-bridge cells is based on the pulse width modulation (PWM) method. The proposed method is applicable when there are more than two cascaded H-bridge cells in each phase. However, for the sake of simplicity in this study, only two H-bridge cells are considered.

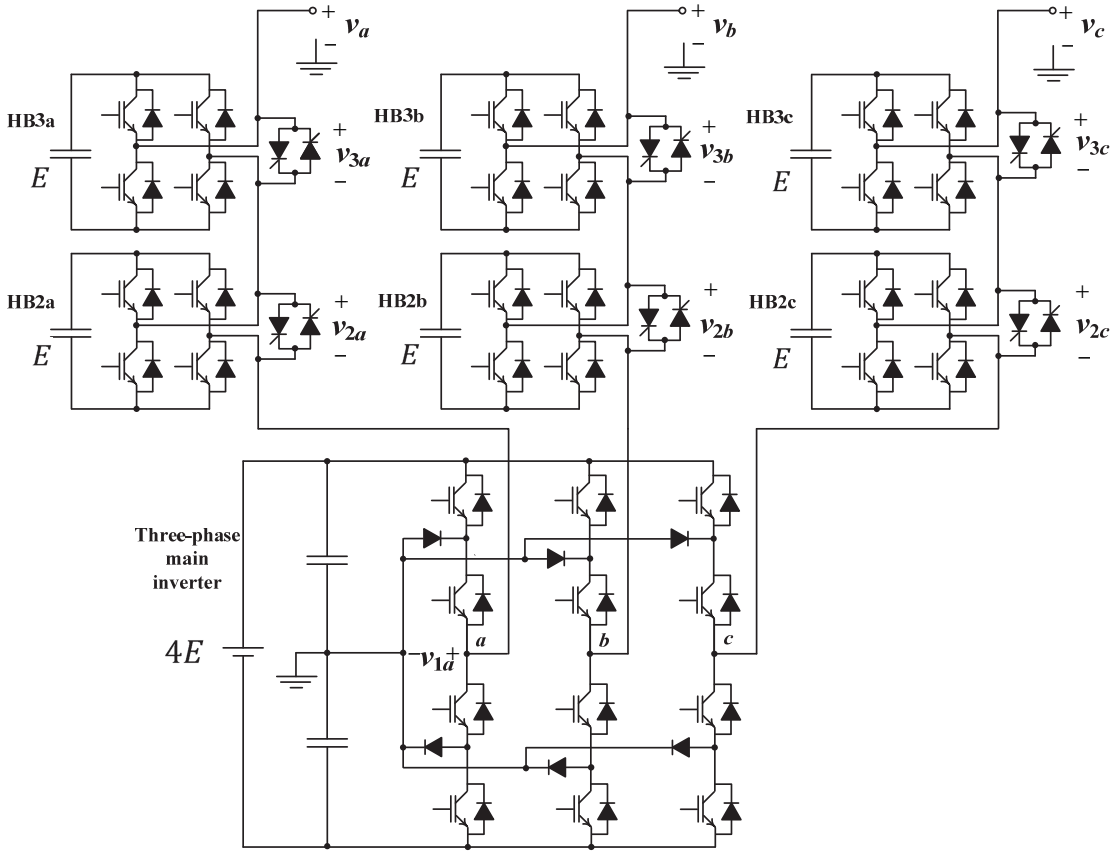

Figure 1. Three-phase hybrid multilevel inverter.

In the inverter topology shown in Figure 1, the voltages of the capacitors in the H-bridge cells must be regulated around one-fourth of the dc bus of the main inverter (i.e., *E*). A voltage control technique is required for this task. Several capacitor voltage

regulation methods have been introduced in the literature for cascaded H-bridge converters and multilevel power converters with floating capacitors [1, 15, 19-22]. In [21], the capacitor voltage is balanced by shifting the output voltage of the main inverter to the left or right while the total output voltage of the inverter remains unchanged. By shifting the voltage of the main inverter, the active power sent to or received from the H-bridge cell is controlled, which therefore controls the voltage of the capacitor. Drawbacks of this method include its inability to regulate the voltage of the capacitor when the load is purely resistive and its limitation to only one H-bridge cell per phase. In [22, 23], existing redundant states are utilized for capacitor voltage regulation in the floating cells. While this method offers simplicity and low computational burden, it cannot be generalized easily when the number of H-bridge cells increases. Also if a fault occurs in one of the H-bridge cells a new switching table must be used. In addition, current sensors are required for detecting the direction of the current.

In this paper, a new method is proposed for capacitor voltage regulation in the cascaded H-bridge cells. The main advantage of the proposed method is independent voltage control of each capacitor regardless of the voltage level of the other capacitors in other H-bridge cells. This feature allows more than one H-bridge cell to be connected in series in each phase of the converter. By adding more H-bridge cells to each phase, it is possible to reduce the total harmonic distortion (THD) of the output voltage. In addition, incorporating more than one H-bridge cell in each phase reduces the shared voltage for H-bridge cells, which makes it possible to use lower voltage rated switches and even to increase the switching frequency for the H-bridge cells. Unlike the method investigated in [21] that cannot regulate the voltage of capacitors of H-bridge cells for resistive loads,

the method proposed here can regulate the voltage of the capacitors regardless of the type of load. Furthermore, this method provides a modular control for each H-bridge cell, which not only helps regulate the capacitors but also provides the unique ability to operate the inverter even with a fault in the H-bridge cells. In other words, if a fault occurs in one H-bridge cell, the control system removes the fault using the bypass circuit and increases the voltage reference of the capacitor, feeding the healthy H-bridge cell into the corresponding phase.

In Section II, the topology of the inverter is described. In Section III, the capacitor voltage regulation method is explained in detail. Finally, Section IV is dedicated to the experimental verification of the method.

II. Inverter Topology

In the considered topology, the main inverter is a three-phase, three-level NPC fed by a single dc voltage source that can be supplied by a standard rectifier. As shown in Figure 1, the input voltage source of the main inverter is assumed to be $4E$. By using the proposed capacitor voltage regulation method, which will be discussed later, the voltages across all capacitors of H-bridge cells are regulated at the E level. Also shown in Figure 1, the output voltage of each phase is defined in reference to the voltage of the node between the two capacitors in the main inverter.

Since the main inverter is a higher voltage inverter, a square waveform switching pattern is used, which leads to lower switching loss. In this case, each phase of the inverter is switched four times during each period cycle. To eliminate the low-frequency harmonics generated by the main inverter, the two low-voltage H-bridge cells function

like conditioning inverters or series active power filters. Therefore, a higher switching frequency is used for the H-bridge cells. These cells operate at a lower voltage level; therefore, the switching loss for these inverters is acceptable. In this inverter, a bypass circuit is connected in parallel with each H-bridge cell to remove faulty cells from the circuit in case of a fault.

III. Capacitor Voltage Regulation

In the inverter considered here, the NPC inverter generates the amplitude of the fundamental harmonic of the entire output voltage (i.e. v_a), while the H-bridge cells, using PWM switching, eliminate the low-frequency harmonics in v_a. In other words, H-bridge cells do not contribute to the generation of the fundamental harmonic, so the average active power that they supply is zero in a fundamental line frequency period. This is the key element of the capacitor voltage regulation method.

Hereafter, the discussion refers to phase a of the inverter, though the concept generalizes easily to other phases. Figure 2 shows how the switching angles of the main NPC converter are chosen and how the reference voltage for the H-bridge cells is generated based on the desired amplitude of the inverter's output voltage for phase a. If the desired output voltage of phase a is $v_a^* = V_m \cos(\omega t)$, then V_m would be the amplitude of the desired fundamental component of the output voltage of the inverter. Using the Fourier series expansion method, the firing angle of the main NPC converter is given by:

$$\alpha = \operatorname{acos}\left(\frac{\pi}{8E} V_m\right). \quad (1)$$

Using this angle, the output voltage waveform of the NPC inverter is determined. In Figure 2, the extra compensation term added to Vm, which will be discussed in detail later, is used to avoid output voltage amplitude fluctuations caused by the operation of the capacitor voltage regulation system. This term will be discussed in detail later. Next, the reference of the output waveform of the main inverter is subtracted from the desired sinusoidal output waveform (i.e., v_a^*) to find the reference waveforms for the two cascaded H-bridge cells. As the H-bridge cells are identical, the remaining part of the waveform ($v_{2a}^{*\prime} + v_{3a}^{*\prime}$) is divided by two and used as the first part of the voltage reference for the PWM switching of each H-bridge cell in the corresponding phase. The first part of the voltage reference for each H-bridge cell is given by:

$$v_{2a}^{*\prime} = v_{3a}^{*\prime} = 0.5 * (V_m \cos(\omega t) - v_{1a}^*). \quad (2)$$

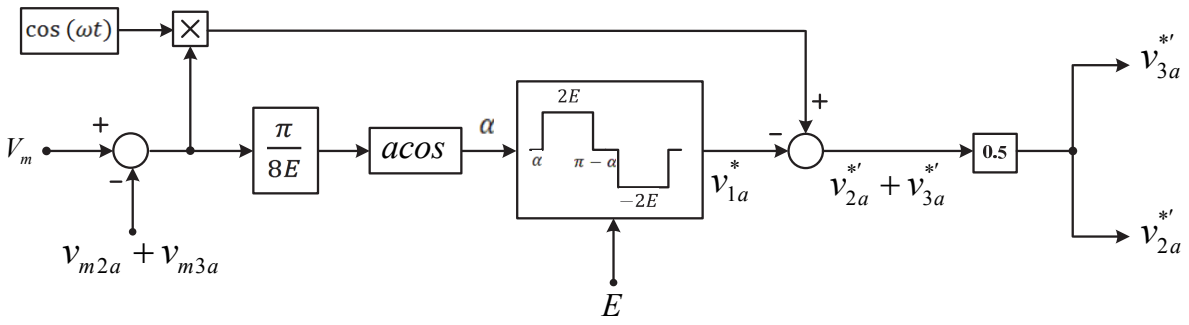

Figure 2. Switching logic for the main inverter and H-bridge cells.

To clarify the operation principle of the inverter, the inverter is simulated using MATLAB/Simulink. In the simulation, E is assumed to be 50 V; therefore, the voltage of each capacitor is meant to be regulated around 50 V. The phase shift sinusoidal pulse width modulation (PS-SPWM) method is used for switching all H-bridge cells [14]. In this method, symmetrical triangles of PWM carriers for the H-bridge cells of each phase are shifted for one quarter of a cycle. Figure 3 shows the operation of the inverter when the amplitude (i.e., V_m) of the desired output voltage is 120 V.

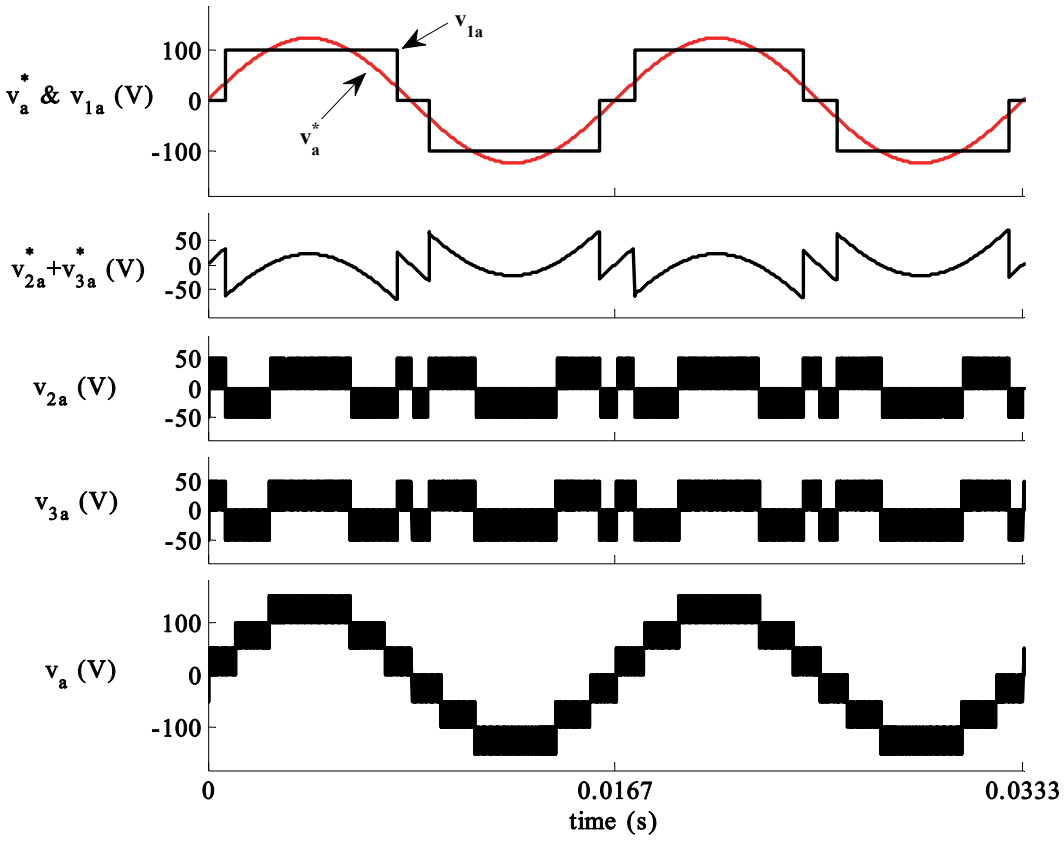

Figure 3. Operation principle of the hybrid multilevel inverter.

The top section of this figure depicts the desired output waveforms (in red) and the output voltage of the main inverter (i.e., v_{1a}). The second section from the top shows the result of v_a^* - v_{1a}, which is the reference voltage for HB2a and HB3a cells. The third and fourth traces in Figure 3 illustrate the actual output voltage of HB2a and HB3a, respectively Note that these two output waveforms are almost identical, but their PWM carriers have one quarter of a cycle phase shift that yields different levels when they are added to each other [14]. The bottom waveform in the figure shows the output voltage of phase *a* of the inverter, which consists of seven voltage levels.

In order to regulate a capacitor's voltage, a small portion of the fundamental harmonic is added to or subtracted from the first part of the voltage reference of each H-bridge cell. Figure 4 illustrates the diagram of the capacitor voltage regulation controller for cell HB2a (see Figure 1). As shown in Figure 4, a sinusoidal waveform that is in phase with the desired output voltage waveform of the corresponding phase is subtracted from the first part of the voltage reference to form the final PWM reference for the corresponding H-bridge cell. The amplitude of the second part of the reference is generated by an anti-windup proportional integral (PI) controller. The capacitor voltage regulation control operation principle is based on the supplied power of each H-bridge cell, meaning that if the capacitor's voltage is more than the desired value (here, E), then a small sinusoidal waveform with the fundamental frequency is added to the reference of the corresponding H-bridge cell. This means that the H-bridge cell will contribute to the generation of the fundamental harmonic of the output waveform and supply active power to the load. Because the H-bridge cell is supplying active power, its capacitor charge decreases, which helps regulate the voltage of the capacitor at the desired value. Note that

under normal operating conditions, the average active power supplied by the H-bridge cells is zero in a period of fundamental line frequency, but using this technique, a small amount of active power is supplied or absorbed for the purpose of capacitor voltage regulation. The final reference voltage for the HB2a cell is defined as:

$$v_{2a}^{*} = v_{2a}^{*\prime} - \left(K_p + \frac{K_i}{s}\right) * (v_{c2a}^{*} - v_{c2a}) * \cos(\omega t) \tag{3}$$

where K_p and K_i are proportional and integral coefficients of the PI controller, respectively. Also v_{c2a}^{*} is reference voltage and v_{c2a} is measured voltage of the capacitor in the HB2a cell, respectively.

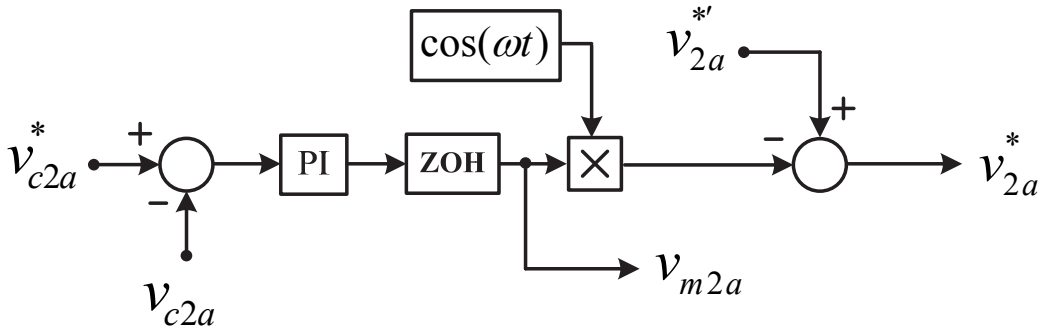

Figure 4. Capacitor voltage regulation controller for HB2a cell.

To avoid any increase or decrease in the amplitude of the fundamental harmonic of the entire inverter, the fundamental harmonics added to the reference for both of the cascaded H-bridge cells in each phase are fed back (i.e., v_{m2a}^{*} in Figure 4) and added to

the original desired amplitude of the output voltage of the corresponding phase. As shown in Figure 4, a zero-order hold (ZOH) block is used, which samples the output of the PI controller every period cycle. In this way, the fundamental harmonic added to the reference of each H-bridge is kept constant during each line period to avoid distortion in the output voltage caused by the capacitor voltage regulation system.

IV. Experimental Results

To verify the proposed method, a hardware prototype of one phase of the hybrid multilevel inverter has been constructed in the laboratory. The CM75DU-24F insulated-gate bipolar transistors (IGBTs) from Powerex have been used as active switches in the inverter. The TMS320C2812 digital signal processor (DSP) from Texas Instruments Inc. has been used for implementing the digital control. IGBT gate commands were passed from the control board via fiber optic cables to IGBT driver boards. Furthermore, a sensor board was used to measure the voltage of the capacitor and then feed it back to the DSP through a signal conditioning board.

3.9 mF capacitors were used in the cascaded H-bridge cells. The fundamental frequency of the output voltage was chosen as 60 Hz, and the PWM switching frequency was 10 kHz. The following experimental results are based on a 200 V dc voltage source for the main inverter; therefore, the voltage of the capacitors in the H-bridge cells was regulated at around 50 V.

Figure 5 shows the output waveforms of the different sections of the hybrid inverter when the commanded V_m was 120 V. The load was comprised of a 13 Ω resistor placed in series with a 22.5 mH inductor. Thus, the power factor (p.f.) in this case was

0.85. Figure 5 depicts the output voltage of the inverter (v_a), the main inverter (v_{1a}), the first H-bridge cell (v_{2a}), and the second H-bridge cell (v_{3a}), respectively, from top to bottom. As shown, the peak voltage of v_{2a} and v_{3a} was 50 V, which indicates that the voltage of the capacitor was regulated.

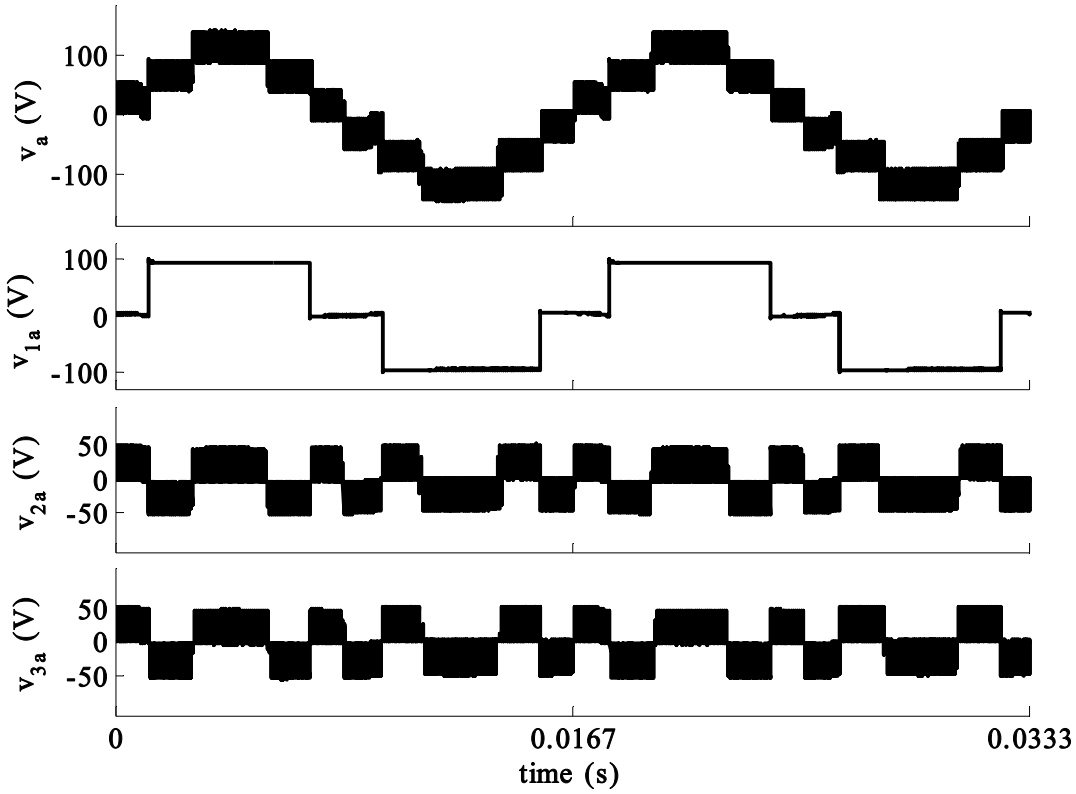

Figure 5. Output voltages of different inverter sections at V_m=120 V.

In Figure 6, the charging process at the start of the inverter's operation is shown when the commanded output voltage was 110 V and the load was comprised of a 13-Ω resistor and a 22.5-mH inductor. In this figure, the output voltage of the inverter, the voltage of the HB2a and HB3a capacitors, and the output current are shown, respectively,

from top to bottom. Before beginning to operate, the capacitors were fully discharged, and the capacitor voltage regulation charged them up to 50 V. Because the output of the PI controllers was saturated, small fixed power was sent to the capacitors; therefore, the voltages of the capacitors increased almost linearly. Using an anti-windup algorithm in the PI controllers, after reaching the desired value (50 V) without any excessive overshoot, the voltage of the capacitors was regulated. As shown, the peak output current remained constant during operation because the fundamental component of the output voltage was only supplied by the main inverter. However, lower-frequency harmonics exist in the output current when the capacitors are not charged to the desired value.

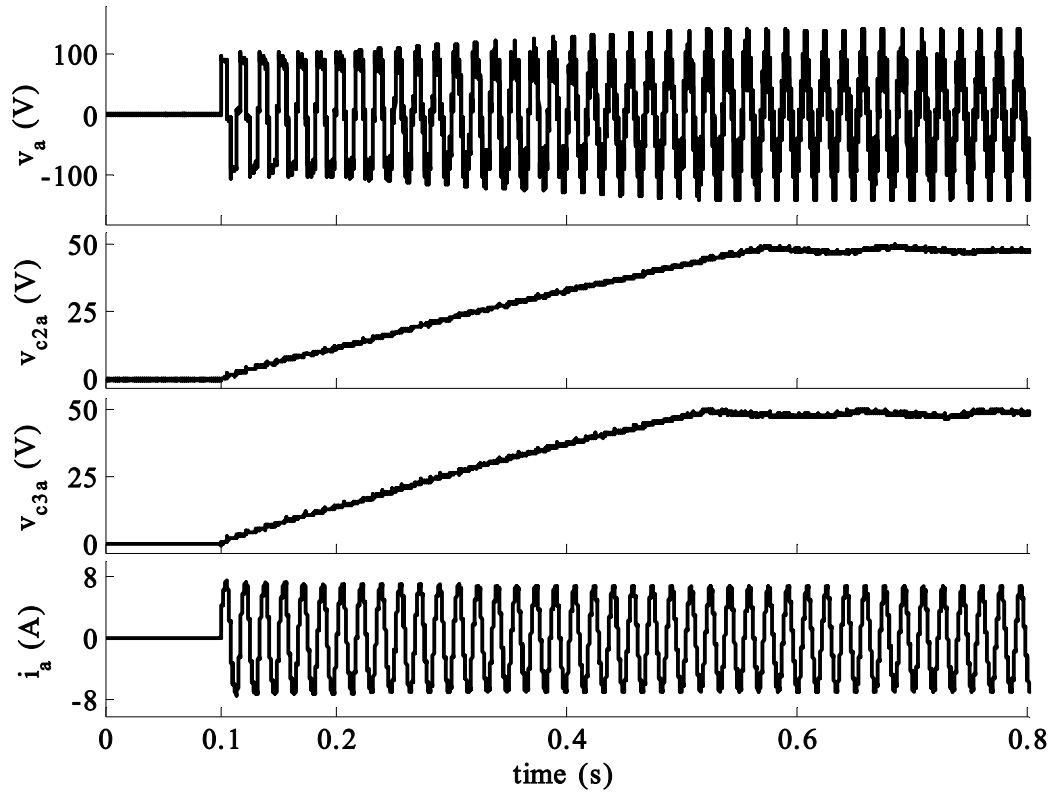

Figure 6. Charging the capacitors of H-bridge cells at the start of operation.

Figure 7 depicts the effect of a sudden load change in capacitor voltage load change in capacitor voltages. In this test, the load consisted of the connection, in series, of a constant 22.5-mH inductor and a variable resistor that changed during the operation of the inverter. At 0.1 s, the resistor changed abruptly from 40 Ω to 13 Ω, returning again to 40 Ω at 0.42 s. As illustrated in Figure 7, the capacitor voltages were controlled, only fluctuating within 1 V.

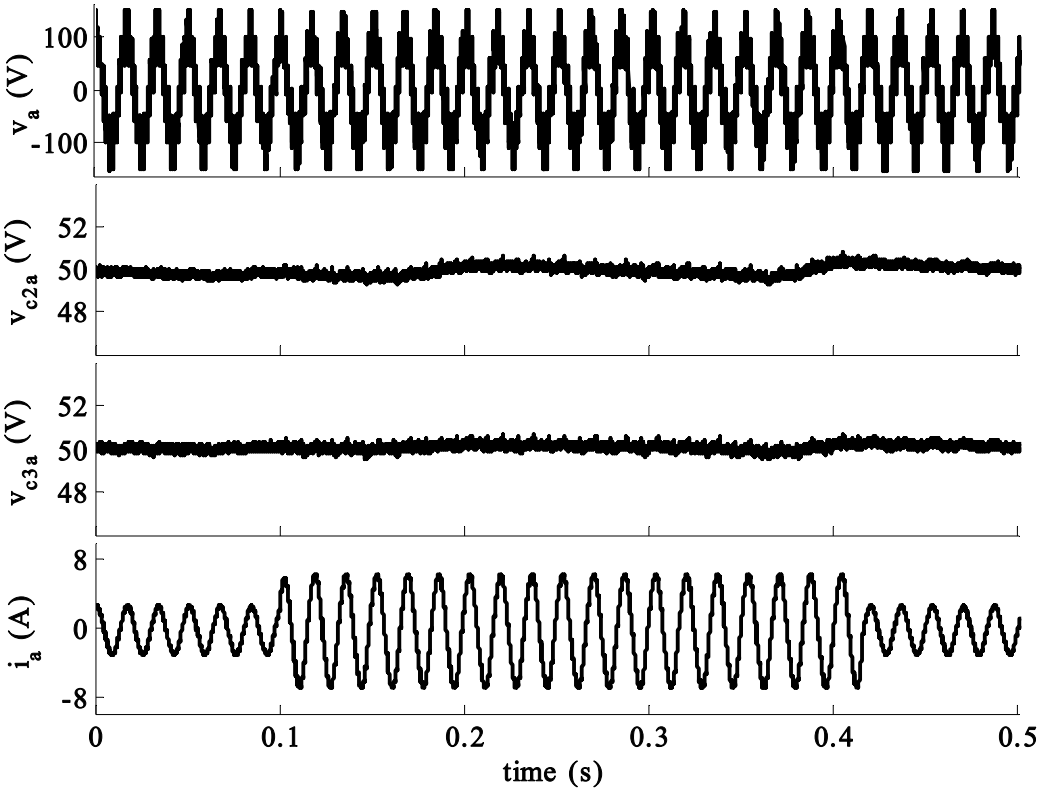

Figure 7. Capacitor voltage regulation during load change.

Figure 8 shows the waveforms of the inverter when the commanded output voltage changed abruptly from 55 V to 110 V. The load used in this test was the same

inductive load used in the test depicted in Figure 5. As shown, when the commanded voltage was 55 V, there were only five output voltage levels, as opposed to seven levels with a 110-V commanded output voltage. When the output voltage current increased, so did the ripple in the capacitor voltages; however, the voltage of the capacitors remained regulated around the desired value with a ripple of less than 2 V. The same test demonstrated in Figure 8 was repeated, as shown in Figure 9, but in this case, the load was purely resistive with a 13-Ω resistor. As shown, the voltage regulation control succeeded at maintaining the voltage of the capacitor at different commanded output voltages. The results of this test indicate that unlike the method described in [21], this method can regulate the voltage of a capacitor even with a resistive load.

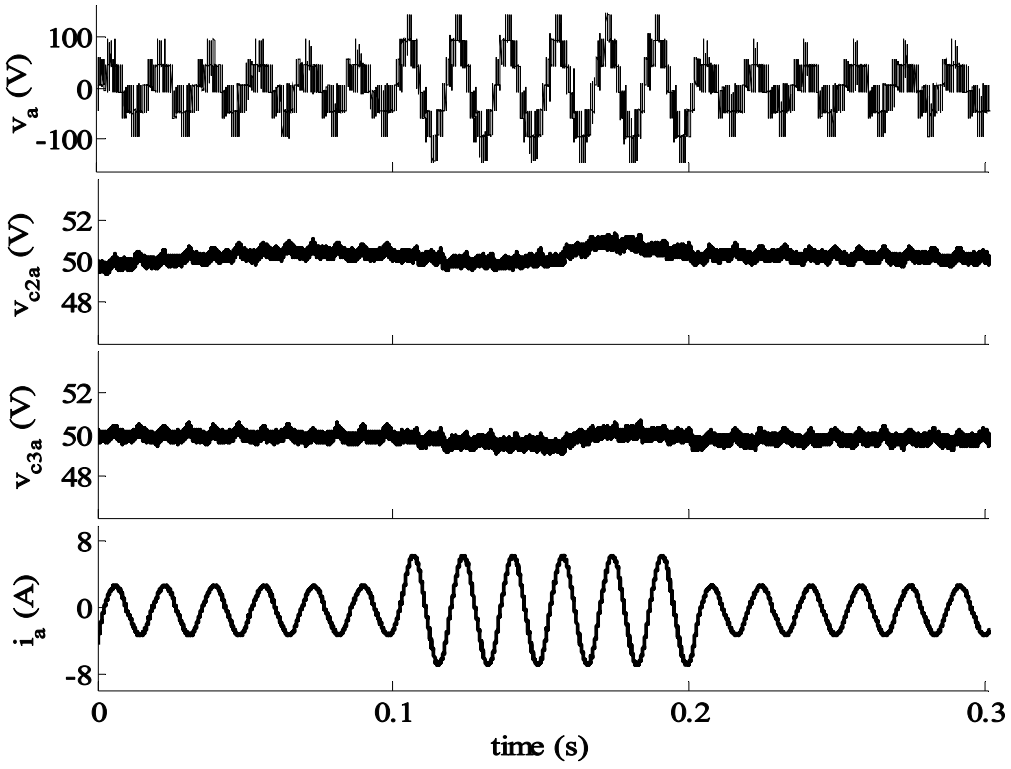

Figure 8. Sudden change in commanded output voltage with inductive load.

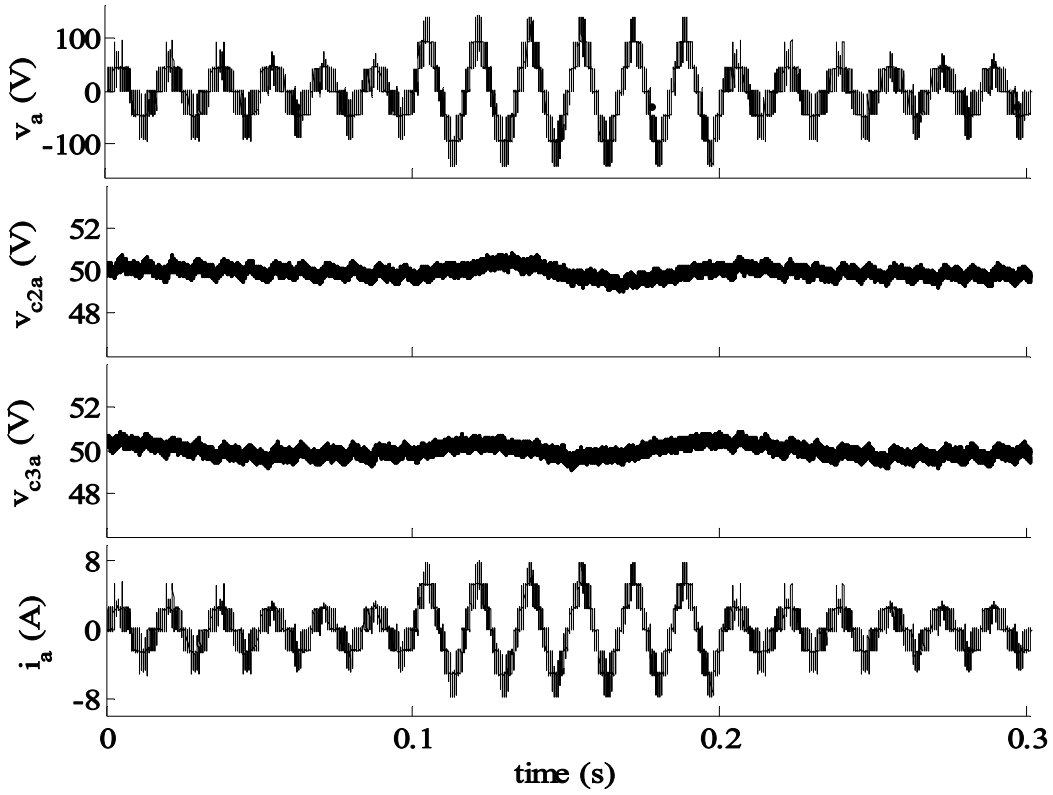

Figure 9. Sudden change in commanded output voltage with resistive load.

In order to study the inverter during a fault in one of the H-bridge cells, three modes of operation were defined. “Normal mode” refers to the inverter working normally without any fault in the H-bridge cells. In “Fault mode,” a fault has occurred in HB3a, and the bypass circuit of HB3a is activated so that the output of HB3a is zero. “Recovered mode” is when the inverter is recovering or has recovered from the fault. In this mode, in order to overcome the malfunction of the inverter due to a fault in one of the H-bridge cells, the voltage reference of HB2a was doubled (i.e., $v_{c2a}^{*} = 2E$) to compensate for the missing H-bridge cell. In addition, the reference voltage for HB3a was set to zero, and the commanded voltage for HB2a was multiplied by two. In other

words, the healthy H-bridge cell in the phase became responsible for generating the remaining part of the desired waveform. Therefore, the commanded voltage for the healthy H-bridge cell (i.e., HB2) is given by (see Figure 2):

$$v_{2a}^{*\prime} = (V_m - v_{2ma})\cos(\omega t) - v_{1a}^{*}. \quad (4)$$

In addition, this method allows the inverter to operate without shutting down all the phases and also allows the operator to schedule maintenance to replace the faulty H-bridge cell at a suitable time. In order to overcome the fault condition, the H-bridge cells in this case should be rated for double their normal operating voltage. However, this value decreases when more H-bridge cells are used in one phase.

Figure 10 shows the voltage waveforms of the different inverter sections before, during, and after a fault in phase *a*. This figure indicates that the inverter operated normally before 0.1 s. At 0.1 s, a fault occurred in HB3a, and the HB3a bypass circuit was activated. As shown in this mode, v_{3a} was almost zero, and the small voltage ripple appearing in the figure was caused by the voltage drop of the bypass circuit. The polarity of the ripple changed based on the direction of the output current. After four cycles, the "Fault recovery" mode has begun. As shown, the voltage of the capacitor began to increase until it reached its commanded value of 100 V. The output current is shown in Figure 11 at the time the fault occurred (around 0.1 s). Due to the inductive load, the current during normal operation was approximately sinusoidal, but after the fault, which began at 0.1 s and lasted for 4 cycles, the output current was distorted. However, after 4 cycles, the commanded waveform for HB2a was corrected, resulting in a current waveform with fewer low-frequency harmonics.

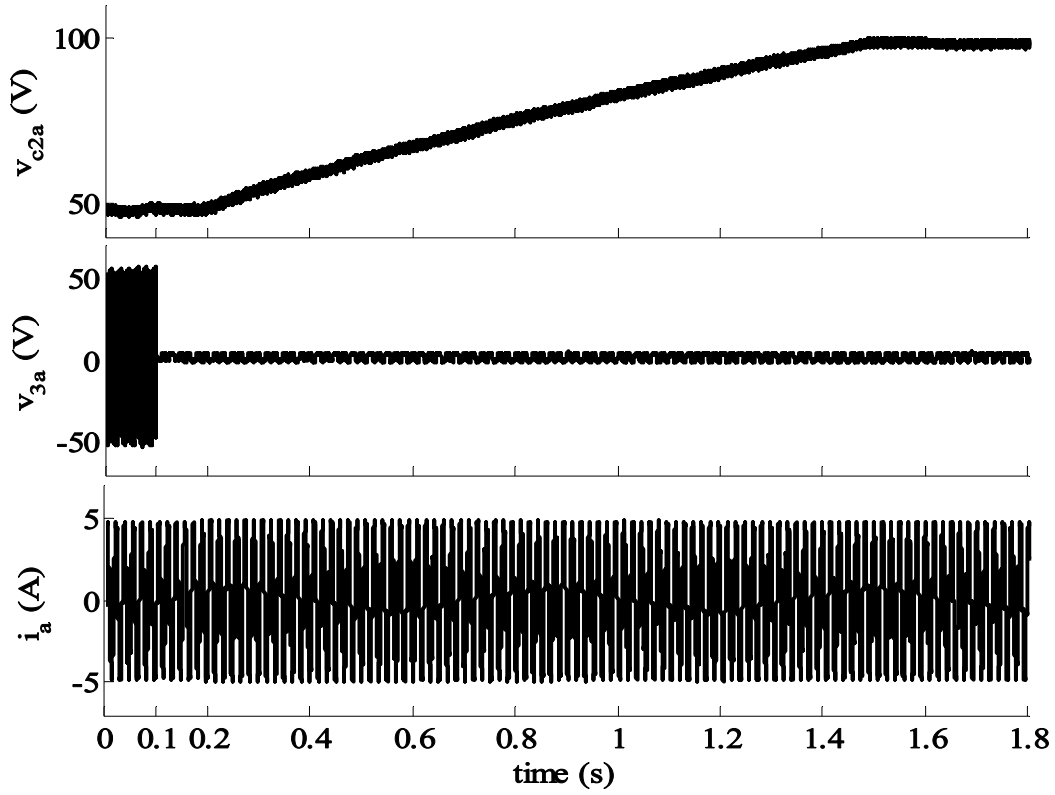

Figure 10. Operation of inverter during normal, fault, and fault recovery modes.

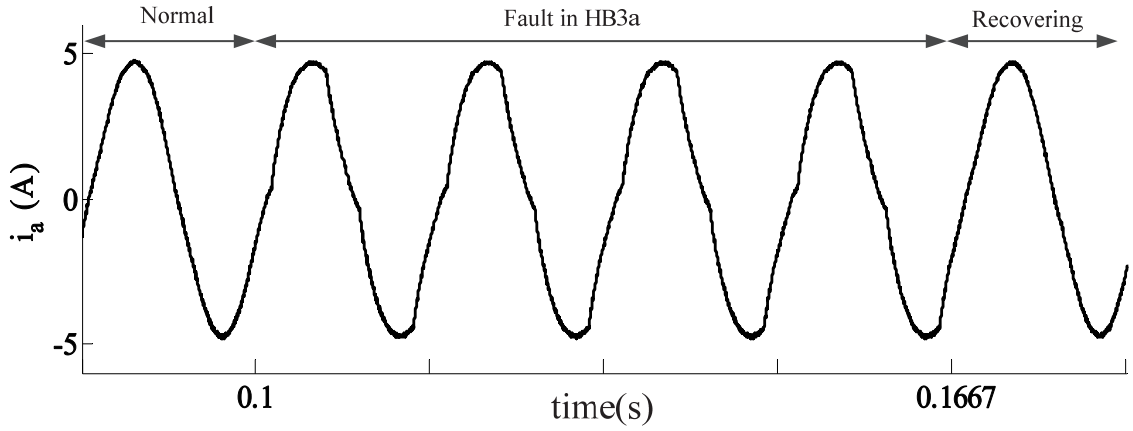

Figure 11. Output current during normal, fault, and fault recovery modes.

V. Conclusion

In the inverter topology considered in this paper, each phase of a three-phase, three-level NPC (main inverter) was connected in series with two cascaded H-bridge cells. The main inverter generates the fundamental harmonic of the entire inverter using a square waveform switching pattern, and the two cascaded H-bridges in each phase generate the remaining waveform to eliminate low harmonics and increase the power quality. A control method has been used to regulate the capacitor voltage in the H-bridge cells. This method allows more than one H-bridge cell to be used in each phase. Combined with the capacitor voltage regulation method, a fault recovery strategy successfully removes the faulty H-bridge cell using a bypass circuit and compensated for the missing H-bridge by increasing the voltage level of the remaining H-bridge cells. This technique allows the inverter to operate even when one of the H-bridge cells is missing, thus increasing its reliability and fault tolerance. The proposed method was validated in the laboratory.

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2. CONCLUSION

In this dissertation, various methods are presented regarding the capacitor voltage regulation in multilevel power electronic converters. These methods have been applied to cascaded H-bridge multilevel converters, flying capacitor active rectifiers, and hybrid multilevel converters.

A cascaded H-bridge multilevel converter consisting two H-bridge cells is investigated in the first section of this dissertation. In the topology of the converter, one of the H-bridge cells is fed by a dc voltage source while the other is supplied by a capacitor. Using analysis, it is proven that capacitor voltage regulation is not attainable in all load conditions. The conducted study shows that at higher power factors maximum output voltage is more limited compare to the loads with lower power factors. Also, a simple formula is derived which can be used to identify modulation indices which lead to voltage regulation of the capacitor. Simulation and experimental verification of the inverter verifies the analysis.

A single-phase flying capacitor active rectifier with a reference frame (*d*-*q*) control method is studied in the second section of this dissertation. A redundant state selection algorithm was used to balance the flying capacitors in all operating conditions. Utilizing additional redundant states, without adding significant computational burden, an algorithm was proposed that reduced the switching loss in the rectifier. The method reduces the switching loss by 10%. Additionally, a start-up procedure for safely starting the rectifier is proposed that pre-charges the flying capacitors. This method keeps the voltage stress over the switches during start-up lower than that of during normal operation of the rectifier. At the same time due to using start-up procedure, the inrush

current during the start-up is reduced. Results indicate a 50 percent reduction of the inrush current using the method.

A hybrid multilevel inverter topology is studied in the third section of this dissertation. In this study a method is proposed for voltage regulation of H-bridge capacitors. The primary feature of this method is that the voltage of the capacitor in each H-bridge cell is independently controlled. This feature allows capacitor voltage regulation for more than one H-bridge cell in each leg. In addition, this method is able to regulate the capacitor voltages regardless of the type of load. Combined with the capacitor voltage regulation method, a fault recovery strategy successfully removes the faulty H-bridge cell using a bypass circuit and compensated for the missing H-bridge by increasing the voltage level of the remaining H-bridge cells. This technique allows the inverter to operate even when one of the H-bridge cells is missing, thus increasing its reliability and fault tolerance.

VITA

Hossein Sepahvand was born in Khorram Abad, Iran. He received the B.S. degree in electronics from Zanjan University, Zanjan, Iran in 2000. He earned the M.S. degree in electrical engineering from the University of Tehran, Tehran, Iran in 2003. He received the Ph.D. degree from Missouri University of Science and Technology in December 2012.