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De-embedding method for electrical response extraction of through-silicon via (TSV) in silicon interposer technology and signal integrity performance comparison with embedded multi-die interconnect bridge (EMIB) technology

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DE-EMBEDDING METHOD FOR ELECTRICAL RESPONSE EXTRACTION OF THROUGH-SILICON VIA (TSV) IN SILICON INTERPOSER TECHNOLOGY AND SIGNAL INTEGRITY PERFORMANCE COMPARISON WITH EMBEDDED MULTI-DIE INTERCONNECT BRIDGE (EMIB) TECHNOLOGY

by

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ABSTRACT

Traditional two-dimensional system-in-package (2D SiP) can no longer support the scaling of size, power, bandwidth, and cost at the same rate required by Moore's Law. Three-dimensional integrated circuits (3D-ICs), 2.5D silicon interposer technology in which through silicon vias are widely used, are implemented to meet these challenges. Embedded multi-die interconnect bridge (EMIB) technology are proposed as well.

In Section 1, a novel de-embedding method is proposed for TSV characterization by using a set of simple yet efficient test patterns. Full wave models and corresponding equivalent circuits are provided to explain the electrical performance of the test patterns clearly. Furthermore, broadband measurement is performed for all test patterns up to 40 GHz, to verify the accuracy of the developed full wave models. Scanning Electron Microscopy (SEM) measurements are taken for all the test patterns to optimize the full wave models. Finally, the proposed de-embedding method is applied to extract the response of the TSV pair. Good agreement between the de-embedded results with analytical characterization and the full-wave simulation for a single TSV pair indicates that the proposed de-embedding method works effectively up to 40 GHz.

In Section 2, the signal integrity performance of EMIB technology is evaluated and compared with silicon interposer technology. Two examples are available for each technology, one is simple with only one single trace pair considered; the other is complex with three differential pairs considered in the full wave simulation. Results of insertion loss, return loss, crosstalk and eye diagram are provided as criteria to evaluate the signal integrity performance for both technologies. This work provides guidelines to both top-level decision and specific IC or channel design.

ACKNOWLEDGMENTS

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1.1. INTRODUCTION

In traditional two-dimensional system in packaging (2D SiP) technology, chips with different functionalities are usually mounted in the same package substrate in a single plane and connected with each other via long wire-bonding or flip-chip solder bumps [1]. It becomes increasingly difficult for conventional 2D SiP to keep up with Moore's Law due to the large parasitic resistance, inductance and capacitance associated with long interconnects [2]. Even though the performance of the chips can be scaled with Moore's Law, the overall performance of the SiP cannot due to the large parasitics [3].

Driven by the demand of high operating frequency, high performance, high density, low power consumption, and low cost, three-dimensional integrated circuits (3D ICs) have become a very promising technology [4], [5] to meet those demands. In 3D ICs, two or more chips are stacked on top of each other in the vertical direction. By doing so, higher operating frequency, higher interconnects density and lower power consumption can be achieved because the shorter interconnects are realized by the 3D IC technology. TSV is the enabling technology for 3D ICs, connecting the stacked chips in the vertical direction. The performance of the system can be highly improved by using TSVs as they provide very short connection and thus small parasitic inductance and conduction loss [6-8]. Considering the thermal and manufacturing reliability issues related to 3D IC technology [9], 2.5D IC technology is brought up as an incremental step from the traditional 2D SiP technology to the true 3D IC technology. In the 2.5D IC technology, a silicon interposer is placed between the chips and the package substrate.

TSVs in the silicon interposer are used to connect the metallization layers on its upper and lower surfaces. Considering the important role that TSV plays in both 3D ICs and 2.5D IC technologies, it becomes essential to characterize the electrical performance of TSV accurately and efficiently to better analyze the performance of 3D IC or 2.5D IC technologies.

The most straightforward method to get the electrical response of TSVs is by measuring the scattering parameters (S-parameter) of the TSVs using a Vector Network Analyzer (VNA). In [10] and [11], two-port microprobe measurement is performed to get the insertion loss and return loss of single-ended TSV up to 20 GHz. However, the dimensions of the studied TSV are large with a diameter of 50 μm and a pitch of 250 μm; and the double-sided probing system applied in [10] and [11] increases the complexity and difficulties of the measurement significantly. For TSVs with smaller dimensions and pitch sizes, probing pads are usually provided and connected with the TSVs via connecting traces. In [12], high speed TSV channel is characterized based on frequency domain measurement up to 20 GHz. However, the measurement results include the contribution not only from the TSV pair, but also the interconnections in the silicon interposer used to connect TSVs. In [13], RF test structures are proposed and measured to extract the electrical performance of TSVs. However, it requires many adaptor structures which results in increase of measurement times; and the adoption of the GSG probe makes it difficult to get good planarity in the measurement.

In this paper, a novel de-embedding metrology for characterization of TSV pair in silicon interposer is introduced. Electrical performance of the test patterns was analyzed based on full wave simulation results. Further, broadband frequency domain

measurement is performed to verify the effectiveness of the proposed method up to 40 GHz. In Section 1.2, the methodology of the proposed de-embedding method was introduced. In Section 1.3, full wave models and equivalent circuit models were built for each test pattern to understand their corresponding electrical performance. In Section 1.4, to further optimize the simulation models, SEM measurements were performed for all the test patterns. Full wave models were optimized based on the measured dimension and structural information. In Section 1.5, wide-band frequency domain measurement is performed for all test patterns. Throughout discussion about the quality of the calibration, accuracy of the measured results, and correlation between the results from simulation and measurement is provided in this Section as well. As shown in Section 1.6, the response of the TSV was obtained by de-embedding pads and traces from the TSV pair simulation with the test fixtures. The results were then verified by both analytical solution [14] and full wave simulation of the TSV pair only. Conclusion is given in Section 1.7.

1.2. METHODOLOGY OF NOVEL DE-EMBEDDING METHOD

The proposed de-embedding method to remove the effect of pads and traces is illustrated in this Section. A detailed description of the de-embedding method is given in [15, 16]. Figure 1.1 shows the geometries of the first three test patterns and their corresponding models. These test patterns only consist of the probing pads and connecting traces with no TSV connected. The first two test patterns as shown in Figure 1. 1 (a) and (b), represent the test patterns of ‘Open’ and ‘Short’ with open and short termination, respectively. For the test pattern ‘Short’, it uses a trace with the same length as the TSV pitch to short the two connecting traces. In the third test pattern ‘Short2’, a trace with twice the length as ‘Short’ is used to connect the two connecting traces.

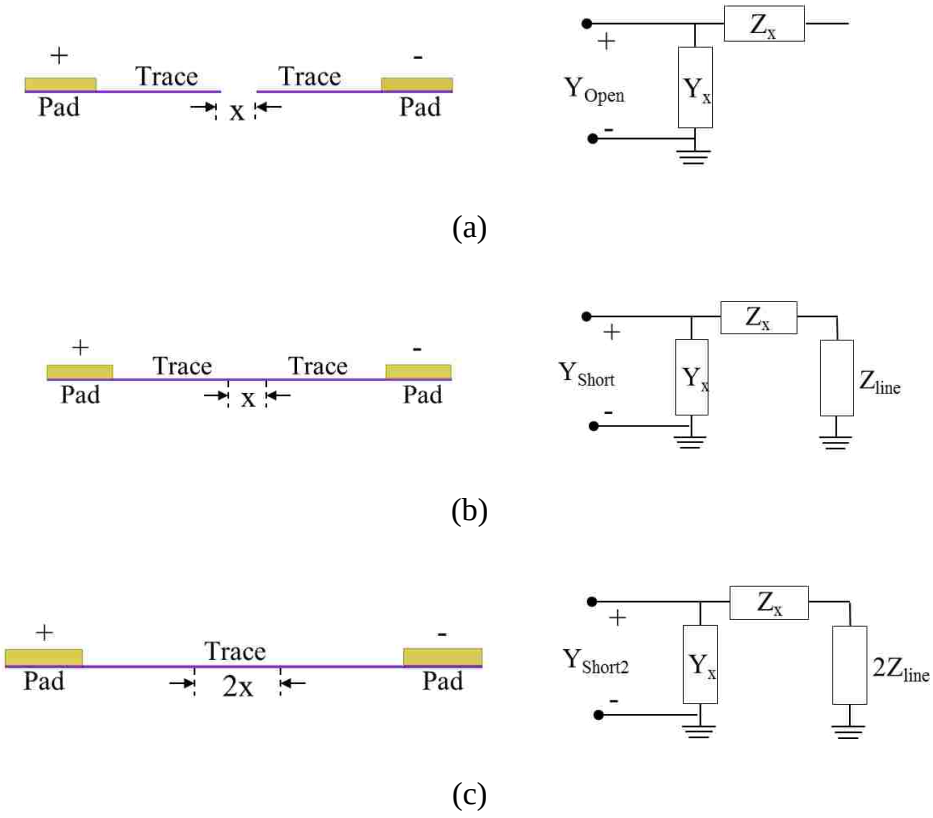


Figure 1.1. Geometries and equivalent models of the first three test patterns.

Above three test patterns are used to characterize the pads and traces as lumped elements Y_x and Z_x, representing the shunt admittances and series impedances of the contact pads and traces. Z_{line} represents the impedance of the extra trace used in the 'Short' pattern. In 'Open' pattern, Y_x is equal to Y_{Open}, which is the admittance looking into the 'Open' pattern as shown by Equation 1.1:

$$Y_x = Y_{Open} \tag{1.1}$$

Similarly, Y_{Short} and Y_{Short2} are the admittances looking into the port for 'Short' and 'Short2' patterns, as shown in Equation 1.2 and Equation 1.3, respectively. Test patterns 'Short' and 'Short2' use traces with different lengths to implement the short

path. Assuming Z_{line} is proportional to the length of the trace, from Equation 1.2 and Equation 1.3, Z_{line} can be found as shown in Equation 1.4.

$$Y_{Short} = Y_x + \frac{1}{Z_x + Z_{line}} \tag{1.2}$$

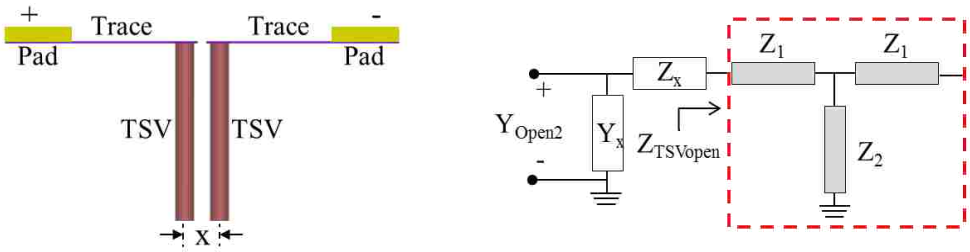
$$Y_{Short2} = Y_x + \frac{1}{Z_x + 2Z_{line}} \tag{1.3}$$

$$Z_{line} = \frac{1}{Y_{Short2} - Y_x} - \frac{1}{Y_{Short} - Y_x} \tag{1.4}$$

From Equation 1.2, Z_x can be calculated out using Equation 1.5:

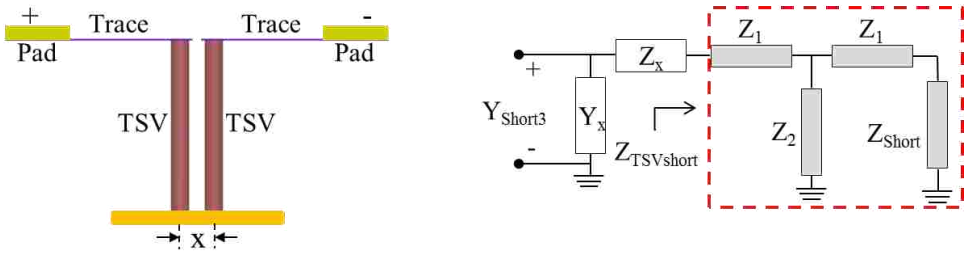
$$Z_x = \frac{1}{Y_{Short} - Y_x} - Z_{line} \tag{1.5}$$

Figure 1.2 shows the remaining two test patterns, which consist of the pads, traces, and the TSV pair. The two test patterns have different load conditions, namely open or short. The model for the TSV pair is a symmetrical T-network to represent the series and shunt impedances, Z_1 and Z_2, respectively.



(a)

Figure 1.2. Geometries and equivalent models of the remaining test patterns used for $Z_{TSVopen}$ and $Z_{TSVshort}$ extraction.



(b)

Figure 1.2. Geometries and equivalent models of the remaining test patterns used for $Z_{TSVopen}$ and $Z_{TSVshort}$ extraction. (Cont)

Independent of the load condition, the effect of pad and trace can be removed using Equation 1.6, where the $Y_{Original}$ and $Z_{De\text{-}embedded}$ are the Y and Z parameters before and after removing the contribution of pads and traces (Y_x and Z_x), respectively.

$$Z_{De-embedding} = \frac{1}{Y_{Original} - Y_x} - Z_x \tag{1.6}$$

Using Equation 1.6 for each case, the impedance looking into the TSV pair after de-embedding can be written as:

$$Z_{TSVopen} = \frac{1}{Y_{Open2} - Y_x} - Z_x \tag{1.7}$$

$$Z_{TSVshort} = \frac{1}{Y_{Short3} - Y_x} - Z_x \tag{1.8}$$

Figure 1.3 shows the resulting models of the two test structures with TSV after de-embedding. The input impedance of the two models can be used to solve for Z_1 and Z_2, provided the Z_{Short} (impedance of structure used to implement a short on the bottom side of the interposer) is known.

$$Z_{TSVopen} = Z_1 + Z_2 \tag{1.9}$$

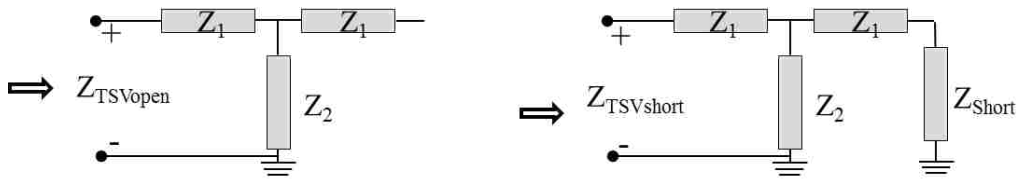
$$Z_{TSVshort} = Z_1 + (Z_1 + Z_{Short}) // Z_2 \tag{1.10}$$

Solving for Z_1 and Z_2 from Equation 1.11 and Equation 1.12,

$$Z_1 = Z_{TSVopen} + Z_{Short} - \sqrt{\left(Z_{TSVopen} + Z_{Short}\right)^2 - \left[Z_{TSVopen}Z_{TSVshort} + Z_{Short}\left(Z_{TSVshort} - Z_{TSVopen}\right)\right]} \tag{1.11}$$

$$Z_2 = Z_{TSVopen} - Z_1 \tag{1.12}$$

The choice of Z_{Short} influences the value of Z_1 and hence the value of Z_2. For an implementation with very low value of Z_{Short} compared to Z_1 and Z_2, Z_{Short} chosen as zero have little influence on the results. However, if Z_{Short} is comparable to the value of Z_1, then the value has to be carefully estimated as it will significantly influence the value Z_1.



(a) (b)

Figure 1.3. Equivalent models for (a) open, (b) short TSV pair after de-embedding probing pads and connecting traces.

For identifying the corner cases, a minimum value zero and a maximum value Z_{line} is used later, where Z_{line} is the trace impedance found in Equation 1.4. Z_{line} represents the trace connecting two connecting traces on the top side of the interposer, and will not be the same as a trace on the bottom of the interposer. So the maximum value is just representative of a trace connecting the TSVs and not real. In real implementations,

depending on the availability of process cycles the short on the bottom of interposer could be larger solder bump or a trace.

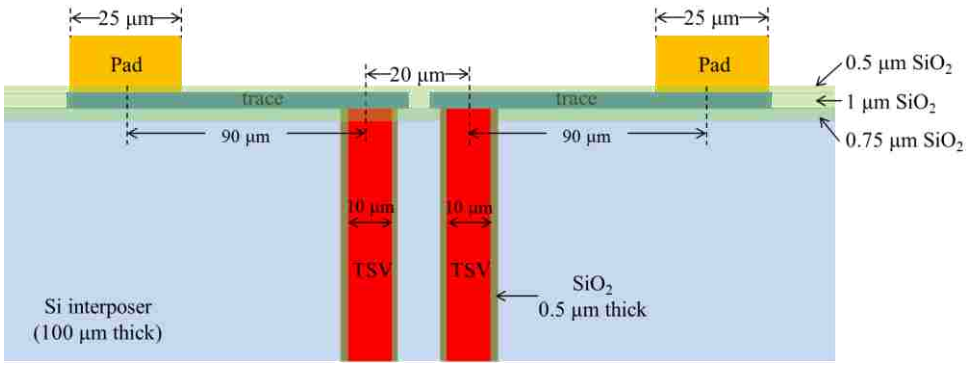
Using the proposed de-embedding method, impedance of the TSV pair can be extracted conveniently. The choice of Z_{Short} controls the accuracy of the Z_1. Better results can be obtained based on information about the implementation of the short standard. An application of this methodology is shown in the Section 1.6.

However, as the test pattern as shown in Figure 1.2 (b) failed to be manufactured successfully, only the first four test patterns will be discussed in the remaining part of this paper. The electrical performance of the TSV pair with open termination $Z_{TSVopen}$ can still be calculated.

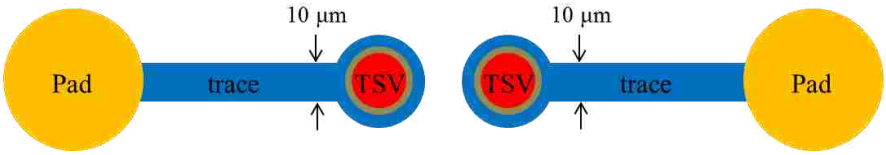
1.3. MODELING AND CIRCUIT ANALYSIS OF TEST PATTERNS

In this Section, broadband electrical modeling for the test patterns is performed using a full wave solver up to 40 GHz. To better understand the electrical performance of each test pattern, corresponding circuit models are built and analyzed.

1.3.1 Full Wave Modeling. All the developed full wave models consist of three generic parts: pads used for landing micro-probes, traces used to connect the TSVs to the pads, and the TSV pair to be studied. The pads are 40 μm ×40 μm squares, and 200 μm apart, and start from metal layer of the trace and go to the top layer where they are accessible to the probes. The traces are 1 μm thick and 10 μm wide, on the first metal layer form the silicon, connecting the TSVs to the pads. The TSVs are 10 μm in diameter and placed with a 20 μm pitch. A dielectric layer SiO2 (with thickness of 0.5 μm) surrounds each TSV to isolate them from the Si interposer. Figure 1.4 shows the pads, traces, and TSV structure's top view and cross-Section with their dimensions.



(a)

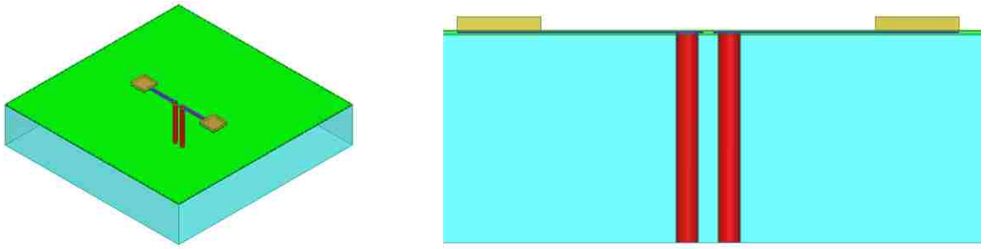


(b)

Figure 1.4. The (a) top view and (b) cross-Section of pads, traces, and TSVs with dimensions.

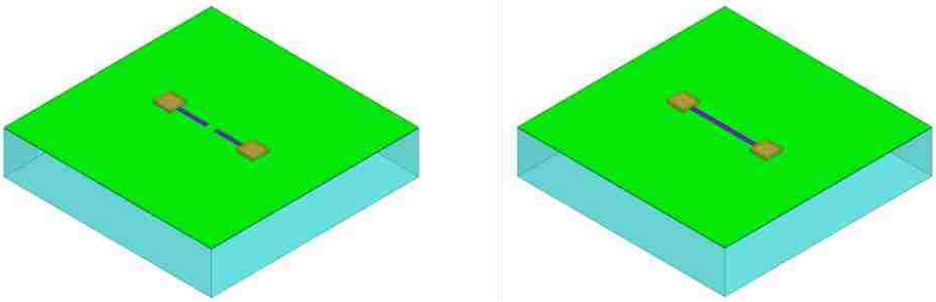
Five full wave models are generated in a full wave solver based on the proposed patterns as shown in Figure 1.5 and Figure 1.6. Figure 1.5 (a) and (b) show the 3D and side views of the full wave model for test pattern 4 (shown in Figure 1.2 (a)). The model consists of the probing pads, the connecting traces and the open-ended TSV pair. The TSV pair is located in the silicon interposer and is surrounded by a 0.5 µm thick SiO_2 layer for DC isolation. The traces are embedded in the SiO_2 layer with a thickness of 1 µm. Part of the pads and TSVs are also embedded in the SiO_2 layer with a thickness of 0.5 µm and 0.75 µm, respectively. The detailed dimensional information is listed as follows: pad size is 40 µm * 40 µm * 7 µm, trace size 10 µm wide with a thickness of 1 µm, the diameter of TSV is 5 µm, the height of the silicon interposer is 100 µm, the center-to-center distance between the pads is 200 µm, and the distance between the TSVs

is 20 μm. Figure 1.6 (a) and (b) show the 3D view of the full wave models for test patterns 1 and 2, which are similar to that of test pattern 4, except there is no TSV pair.



(a) (b)

Figure 1.5. The full wave model for test pattern 4: (a) 3D view, and (b) side view.



(a) (b)

Figure 1.6. The 3D view of full wave models for (a) test pattern 1, (b) test pattern 2.

Test pattern 1 is open structure, while test pattern 2 is a short structure. Both structures consist only of pads and traces. The only difference between test patterns 1 and 2 is that in test pattern 2, the two traces in test pattern 1 are further connected as shown in Figure 1.6 (b). Test pattern 3, as shown in Figure 1.1 (c), is pretty similar to test pattern 2

except that the length of the trace is 20 μm longer. The other dimensions for the pads, traces, SiO_2 layers and silicon interposer in all the test patterns are the same.

1.3.2 Analysis of Full Wave Simulation Results. The input impedance results of the test patterns are calculated using the full wave solver and are shown in Figure 1.7.

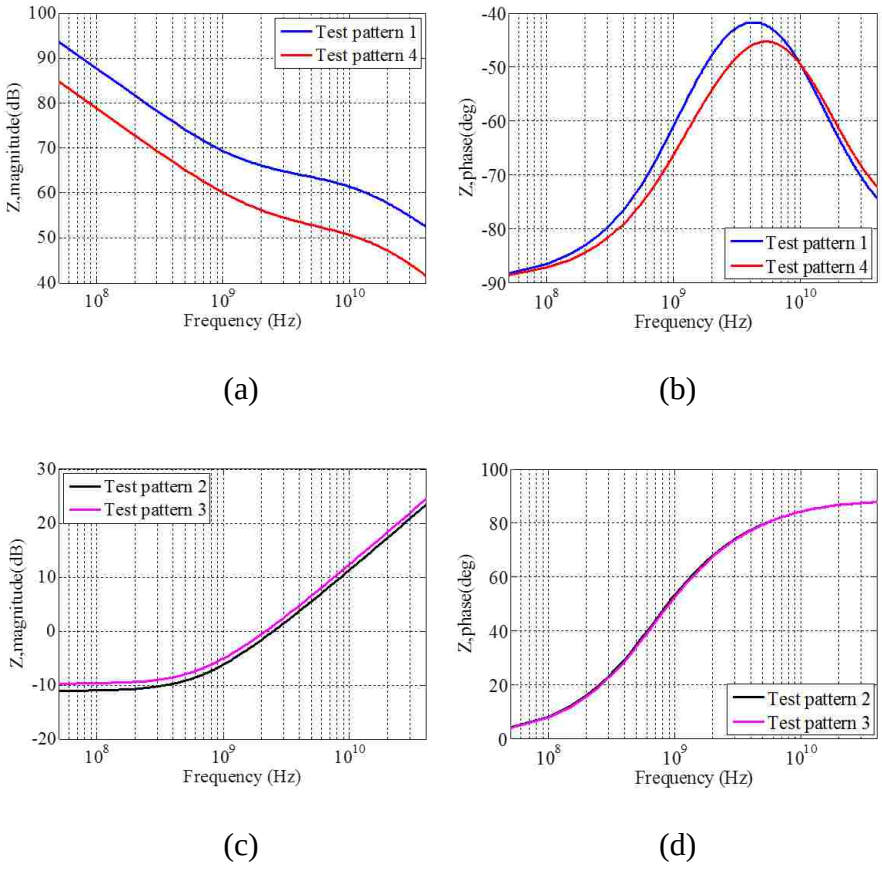


Figure 1.7. Simulated input impedance results of the test patterns.

It can be seen that parasitic capacitance dominates when geometry is open terminated and parasitic inductance dominates when geometry is short terminated. Detailed analysis and discussions will be provided in the next Section.

1.3.3 Circuit Model Analysis. To better understand the electrical performance of each test pattern, a circuit model was built and analyzed. Parametric study was also performed to evaluate the dependency of the electrical characteristics of the test patterns on both structural and material parameters. The parametric study can help validate the accuracy of the proposed circuit model. Figure 1.8 shows the side view of test pattern 4 and its equivalent circuit model. A one port measurement was adopted in the full wave simulation, with the probing pad on the right side set as the reference.

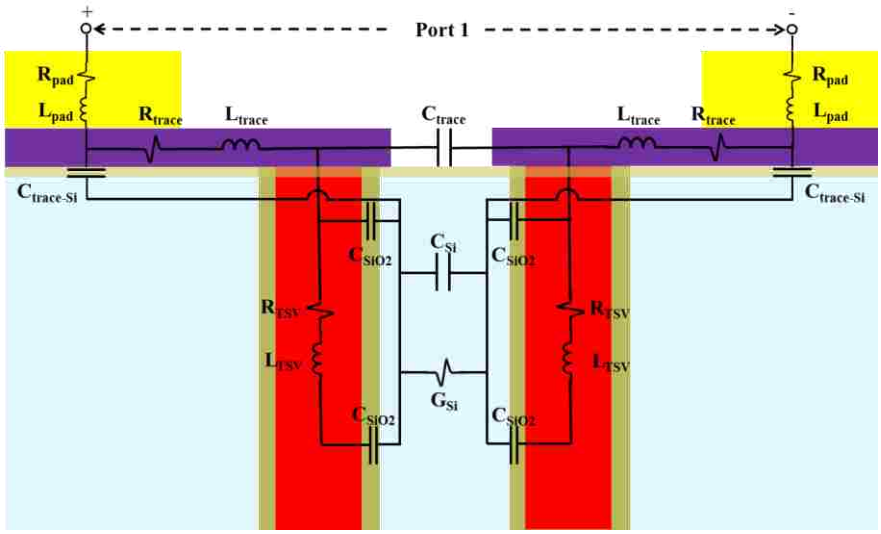


Figure 1.8. The side view and equivalent circuit model of test pattern 4.

In the proposed circuit model, R_{pad} and L_{pad} represent the parasitic resistance and inductance of the probing pads, R_{trace} and L_{trace} represent the parasitic resistance and inductance of the connecting traces, R_{TSV} and L_{TSV} represent the parasitic resistance and inductance of the TSVs, C_{SiO2} represents the parasitic capacitance between each TSV

and the silicon interposer, C_{Si} represents the parasitic capacitance between the TSVs, C_{trace} represents the parasitic capacitance between the two connecting traces, and G_{Si} represents the parasitic conductance of the silicon interposer between the two TSVs. Further, since there is a thin SiO_2 layer under the connecting traces, there exists a parasitic capacitance between the trace and the silicon interposer, which shows effect at low frequencies.

The magnitude and phase of the simulated input impedance of test pattern 4 are shown in Figure 1.7 (a) and (b), respectively. The results suggest that capacitance dominates across the observed frequency range. However, there is a transition from capacitance to resistance from around 1 GHz to 4 GHz. At higher frequencies, it transitions back to capacitance. By analyzing the above circuit model, the impedance behavior of test pattern 4 can be understood in a very clear way. At low frequencies, the capacitance between each TSV and the silicon interposer C_{SiO2} dominates. When frequency goes up to approximately 1 GHz, the conducted loss in silicon dominates and G_{Si} shows its effect. When frequency goes higher than 4 GHz, silicon acts as a dielectric and the capacitance between the two TSVs dominates [17].

Circuit models are developed for the other test patterns, and corresponding parametric study was performed as well. Detailed results are not included in this paper considering the page limitation. However, a brief analysis is given below.

Test pattern 1 only consists of the probing pads and traces, with both located on the top of the silicon interposer. Since test pattern 1 is an open structure, the electrical performance is dominated by the capacitance between the metal structure and silicon

interposer. In this case, the capacitance changes dramatically by changing the pad size and the trace size.

Test pattern 2 is composed of the probing pads, which are connected together by the trace. In this case, inductance that is determined by the size of the loop formed by the probing pads and the trace dominates the electrical response of the test pattern. So, the trace length and width are the most important parameters as they determine the overall loop size. Test pattern 3 is almost the same as test pattern 2 except its trace is 20 μm longer.

1.4. PARAMETRIC STUDY

It can be known from the circuit model analysis that the overall performance of test pattern 4 is determined by the circuit element values, which are determined by the dimensions or the material properties of the test pattern. Taking C_{SiO2} for instance, both the permittivity and the thickness of the SiO_2 layer surrounding the TSVs affect the capacitance value dramatically. To better evaluate the parameters and their impact on the TSV performance, a parametric study was performed to evaluate the dependency of the electrical characteristics of the test patterns on both structural and material parameters.

1.4.1 Material Properties. First of all, the effect of material property including the conductivity of Si and the permittivity of SiO_2 to the electrical performance of test pattern 4 was investigated. Figure 1.9 (a) and (b) show the effect of the conductivity of Si, and Figure 1.9 (c) and (d) show the effect of the permittivity of SiO_2.

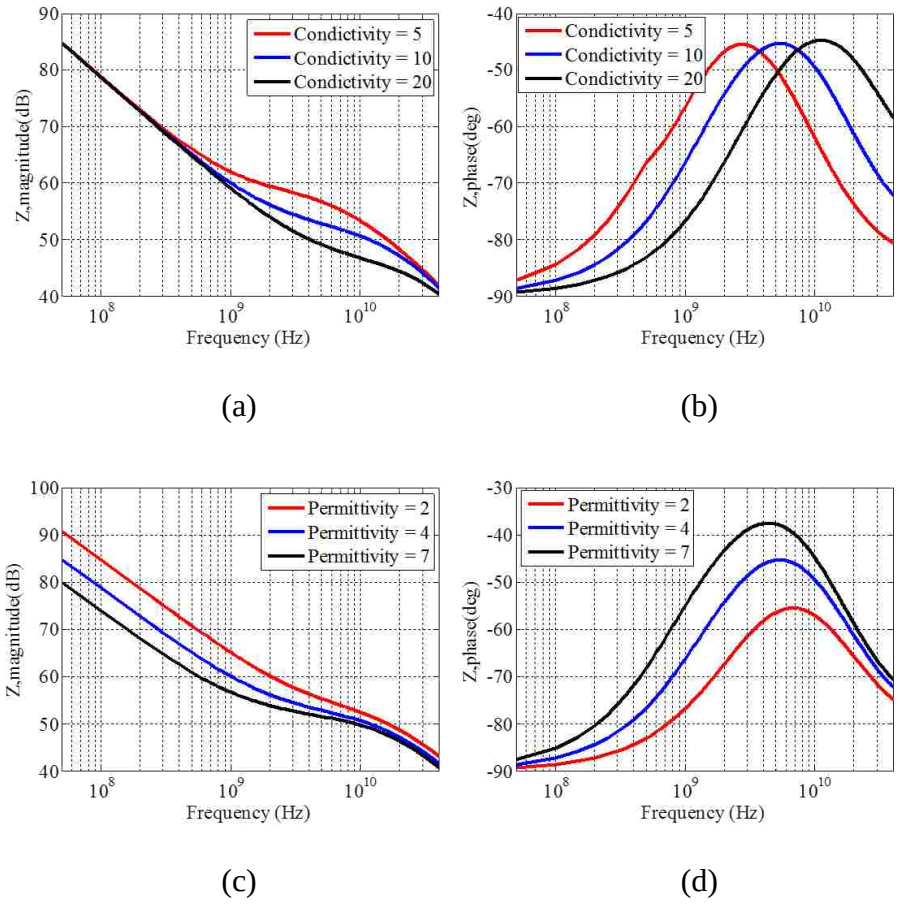


Figure 1.9. Impact on the electrical performance of test pattern 4 of: (a), (b) the conductivity of Si; and (c), (d) the permittivity of SiO_2.

The conducted loss of the silicon substrate is related to the conductivity of Si (a function of the doping concentration). The larger the conductivity, the smaller the resistance between the two TSVs through the silicon. The transition frequency also shifts higher. The capacitance C_{SiO2} between each TSV and the silicon interposer vary with the permittivity of SiO_2. When the permittivity of SiO_2 increases, C_{SiO2} increases, resulting in a lower impedance magnitude at the low frequencies. Figure 1.9 clearly demonstrated these physical understandings.

1.4.2 Dimension Properties. Further, the structural parameters can be important contributors to the test pattern performance as well. So the effects of structural parameters including the radius of the TSVs, height of the TSVs, gap between the TSVs and thickness of the SiO_2 isolation layer were studied as well. Figure 1.10 shows the simulated impedance comparisons of test pattern 4 among different TSV radii and heights.

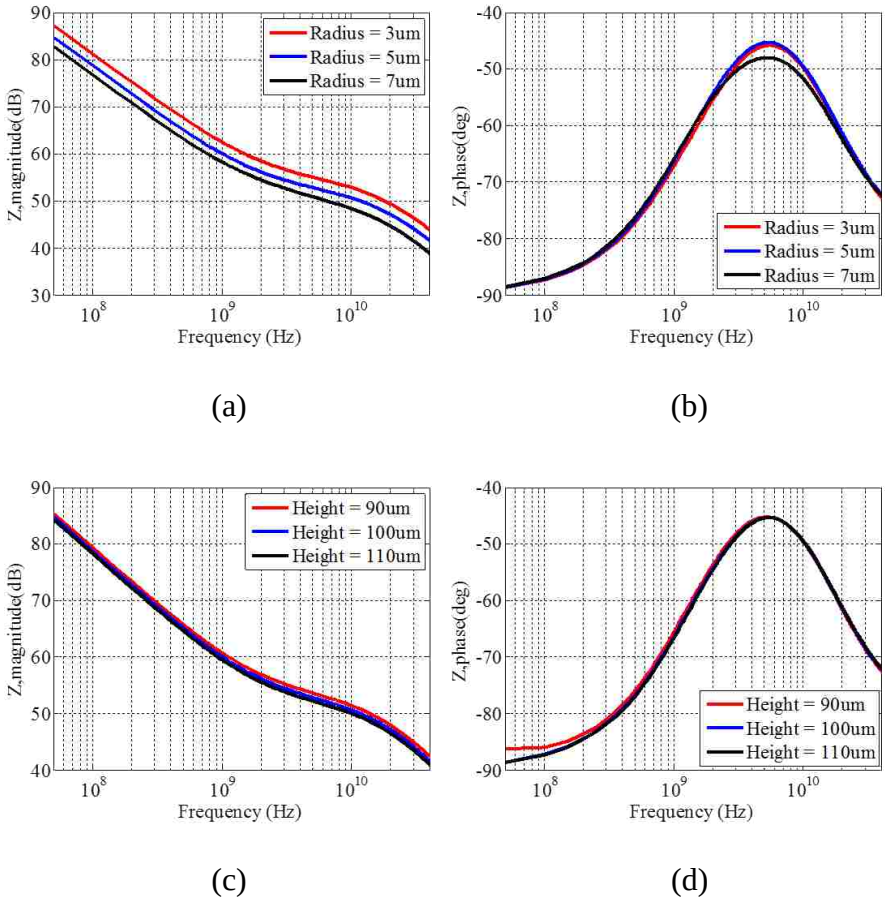
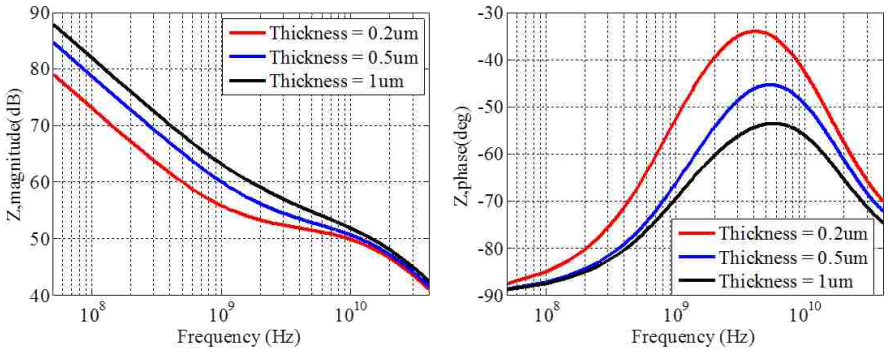


Figure 1.10. Impact of (a), (b) TSV radius, and (c), (d) TSV height on the electrical performance of test pattern 4.

As shown in Figure 1.10 (a), a larger TSV radius gives a lower impedance in the entire frequency band because it increases the capacitances (both between the TSV and silicon interposer as well as between the TSVs) and reduces the resistance between the TSVs. Figure 1.10 (c) demonstrates that a longer TSV mainly increases the inductance, resulting in small impedance changes in the open case.

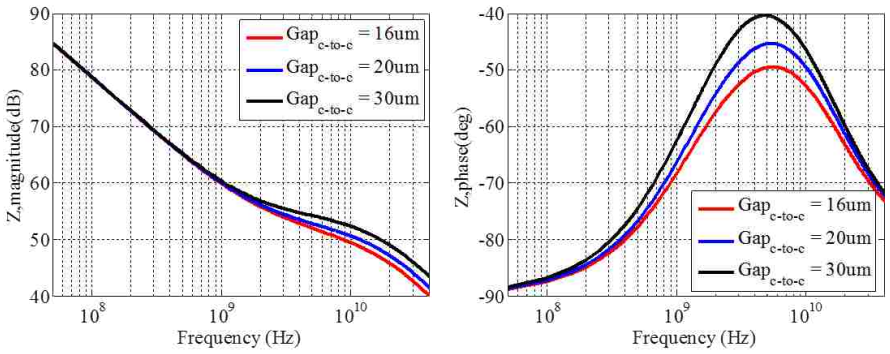
Figure 1.11 shows the simulated impedance comparison of test pattern 4 among different thickness values of the SiO_2 isolation layer. The thickness of the SiO_2 isolation layer is another critical parameter besides the permittivity of SiO_2 and the dimensions of TSVs. By increasing the thickness of the isolation layer, the TSV-to-silicon capacitance decreases and the low-frequency impedance increases.



(a) (b)

Figure 1.11. Impact of thickness of SiO_2 isolation layer surrounding TSVs to the impedance performance of test pattern 4.

Figure 1.12 shows the simulated impedance comparison of test pattern 4 among different center-to-center distances between the two TSVs.



(a) (b)

Figure 1.12. The effect of different center-to-center distances to the impedance performance of test pattern 4.

The center-to-center distance between the two TSVs determines the resistance and the capacitance between the two TSVs. The further away the TSVs are from each other, the smaller the capacitance and the larger the resistance between them. Thus the high-frequency impedance of the test pattern increases, as verified by the simulation results.

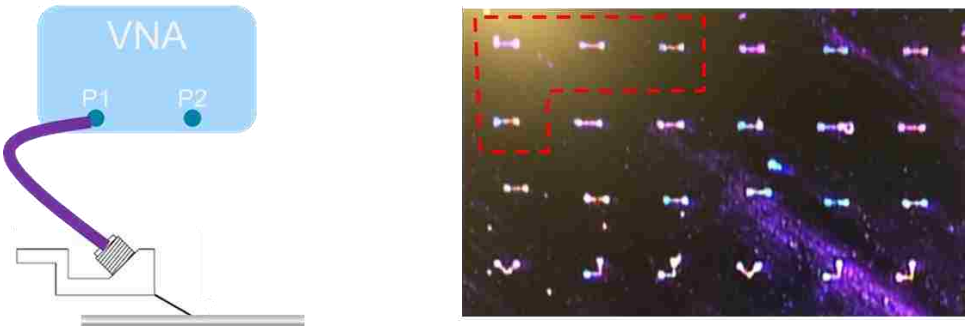
The influence of other structural parameters such as the pad and trace dimensions to the electrical performance was also studied. Those parameters have little effect to the overall performance of test pattern 4.

1.5. MICRO-PROBE STATION MEASUREMENT

To verify the accuracy and effectiveness of the developed full wave models, one-port microprobe measurement is performed for all test patterns up to 40 GHz [18]. In this Section, the quality of the calibration used in the measurement is discussed in detail, which can be used as guideline for Vector Network Analyzer (VNA) measurement. The measurement results of the test patterns are then provided and discussed based on

effective calibration. Furthermore, the full wave models of the test patterns are optimized based on SEM measurement and then compared with the measurement results.

1.5.1. Measurement Setup. One-port microprobe station measurement is performed to measure the S-parameter of the test patterns. The schematic of the measurement setup is shown in Figure 1.13 (a). To enable the measurement, the microprobe is connected with one end of the precision cable; the other end of the cable is connected to the port of VNA.



(a) (b)

Figure 1.13. The (a) schematic of the measurement setup and (b) the chip under test.

Agilent E8364B is used in this measurement with effective working frequency of 10 MHz to 50 GHz. For microprobe, GGB-40A-SG-200DP is used with pitch size of 200 μm and effective working frequency up to 40 GHz. CS-8 is used as the calibration substrate to perform short-open-load (SOL) calibration. Many sets of high precise elements, such as shorts, opens, loads and throughs, are available in CS-8 for ground-signal (GS), signal-ground (SG), ground-signal-ground (GSG) footprints with

recommended pitch range of 50 μm to 250 μm. It is suitable for all microprobes from DC to 220 GHz. Figure 1.13 (b) shows the chip for testing, with all test patterns to be measured marked by the red dashed line.

Before performing the measurement, SOL calibration is applied to move the reference plane of the measurement from the port of VNA to the tip of microprobe. Effect of VNA, precision cable and microprobe is removed after calibration. The quality of calibration determines the accuracy of the microprobe measurement for the test patterns, so, it's important to ensure the high quality of the calibration.

1.5.2. Discussion of Calibration Quality. To evaluate the effectiveness of the SOL calibration, comparison for the parasitic of the calibration standards is performed between the standard values provided by GGB and the ones calculated from the measurement results. Table 1.1 shows the calibration coefficients for CS-8 calibration substrate provided by the vendor.

Table 1.1. The standard calibration coefficients for CS-8 calibration substrate.

CALIBRATION COEFFICIENT FOR CS-8

Calibration Pattern	Calibration Coefficient
Open	4.3fF
Short	25.8pH
Load	16.7pH

For 'Open' calibration standard, the parasitic capacitance is 4.3 fF; for 'Short' and 'Load' calibration standards, the parasitic inductances are 25.8 pH and 16.7 pH.

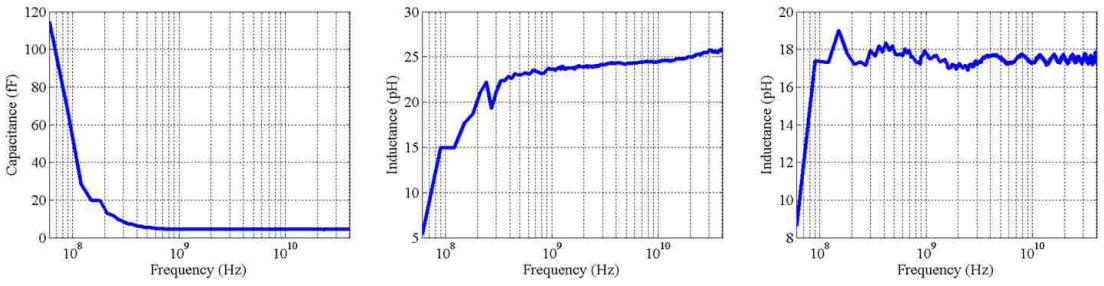
To calculate the parasitic values from the measurement, SOL calibration is performed first and the microprobe is re-landed to the 'Open', 'Short' and 'Load' calibration standards. S-parameters for each standard are measured and then converted to Z-parameters. The corresponding parasitic capacitance and inductance for the calibration standards can be calculated according to the following two equations:

$$C = \frac{1}{2\pi f \left| Z_{imag} \right|} \tag{1.13}$$

$$L = \frac{\left| Z_{imag} \right|}{2\pi f} \tag{1.14}$$

where, C and L represent the calculated parasitic capacitance and inductance, respectively; and f represents frequency; Z_{imag} represents the imaginary part of Z-parameter.

By substituting the converted Z-parameter into Equation 1.13 and Equation 1.14, the corresponding parasitic for each pattern can be obtained as shown in Figure 1.14 (a), (b) and (c).

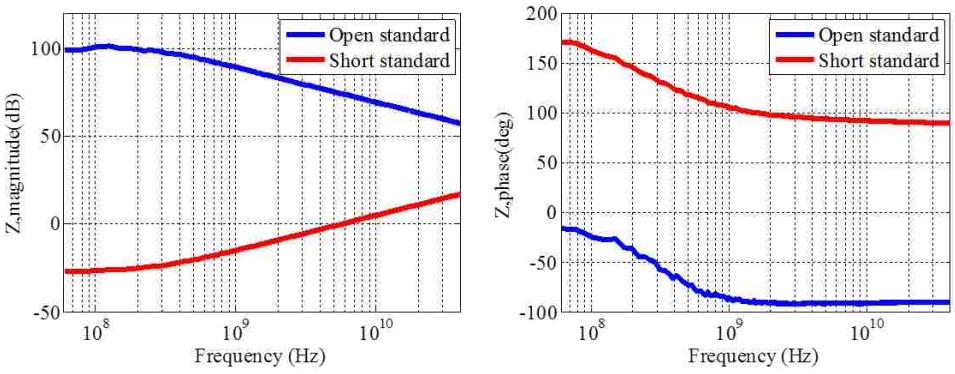


(a) (b) (c)

Figure 1.14. The (a) calculated parasitic capacitance from measurement for 'Open' calibration standard, (b) the parasitic inductance for 'Short' calibration standard and (c) parasitic inductance for 'Load' calibration standard.

Figure 1.14 (a), (b) and (c) represent the calculated parasitic capacitance for ‘Open’ calibration standard, parasitic inductances for ‘Short’ and ‘Load’ calibration standards, respectively. The results shown in Figure 1.14 indicate that the parasitic capacitance for ‘Open’, ‘Short’ and ‘Load’ calibration standards are 4.33 fF, 24.5 pH and 17.3 pH when the frequency is beyond 1 GHz, respectively. The good agreement between the provided and calculated parasitic values demonstrates the high quality of the SOL calibration in this measurement.

1.5.3. Dynamic Range of the Measurement. To estimate the effective frequency of the one-port microprobe measurement, dynamic range of the measurement is discussed in this part. The measured dynamic range is as shown in Figure 1.15.



(a) (b)

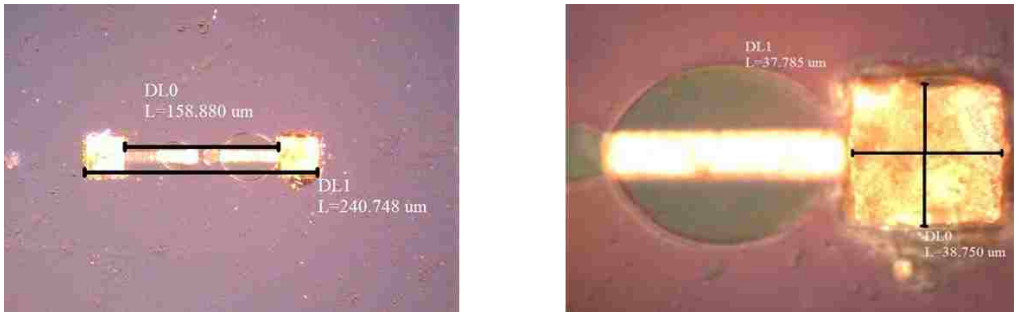
Figure 1.15. The dynamic range of the 1-port microprobe measurement.

The upper and lower bounds are defined as the measured Z-parameter when the probe is landed on the ‘Open’ and ‘Short’ calibration standards. In general cases, considering geometries with open and short terminations, the corresponding phases of the

input impedance should be around -90^{o} and 90^{o}, respectively. However, it can be seen from Figure 1.15 (b) that, the measured phases of the 'Open' and 'Short' calibration standards are not accurate when the frequency is below 1 GHz. So the effective frequency range for this measurement is from 1 GHz up to 40 GHz.

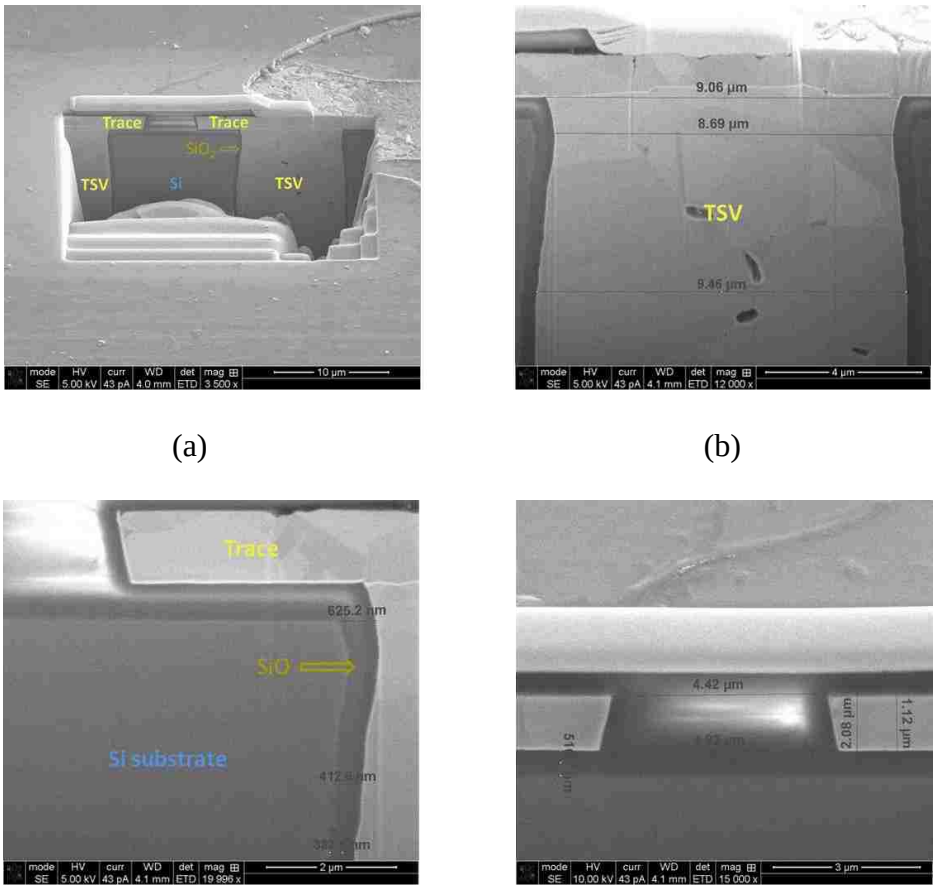
1.5.4. Full Wave Model Optimization. Considering manufacturing tolerances, there is great possibility that the dimensions of the test patterns in the manufactured chip are different from those of the original design. Due to those unpredictable manufacturing tolerance, the electrical performance of the test pattern may vary much from the designed ones. To optimize the full wave models, both optical scope and SEM measurements were taken to extract the structural information for all the test patterns. By using the measured structural information in the simulation, more accurate simulation results were obtained.

Figure 1.16 and Figure 1.17 show dimensions of test pattern 4 from the optical scope and SEM measurements, respectively. Detailed and accurate dimensions were obtained from the above measurements. These results also show the real structure of test patterns 4. In agreement with the manufacturer's description, the SEM images show that the SiO_2 thickness of the isolation layer around the TSVs gradually decreases along the TSV length (thickest at the TSV top and thinnest at the TSV bottom). Besides, according to the SEM measurement, it can be seen that there is a Ti layer with a thickness of around 0.1 μm between the pad and trace. Based on the thickness information, considering the conductivity of Ti, the resistance value of the thin Ti layer was calculated to be 0.14 mΩ, which can be neglected in the full-wave model. So the thin Ti layer is not considered herein. Similar measurements are repeated for the other test patterns, which are not shown in this paper due to space limitation.



(a) (b)

Figure 1.16. The measured dimensions of test pattern 4 taken by optical scope.



(a) (b)

(c) (d)

Figure 1.17. The dimension measurement results of test pattern 4 using SEM.

Figure 1.18 shows the simulation result comparisons before and after optimization for all the test patterns. Solid and dashed lines represent the simulation results obtained from the models before and after optimization, respectively. A larger difference is observed in both the magnitude and phase for test patterns 1 and 4, than those for test patterns 2 and 3.

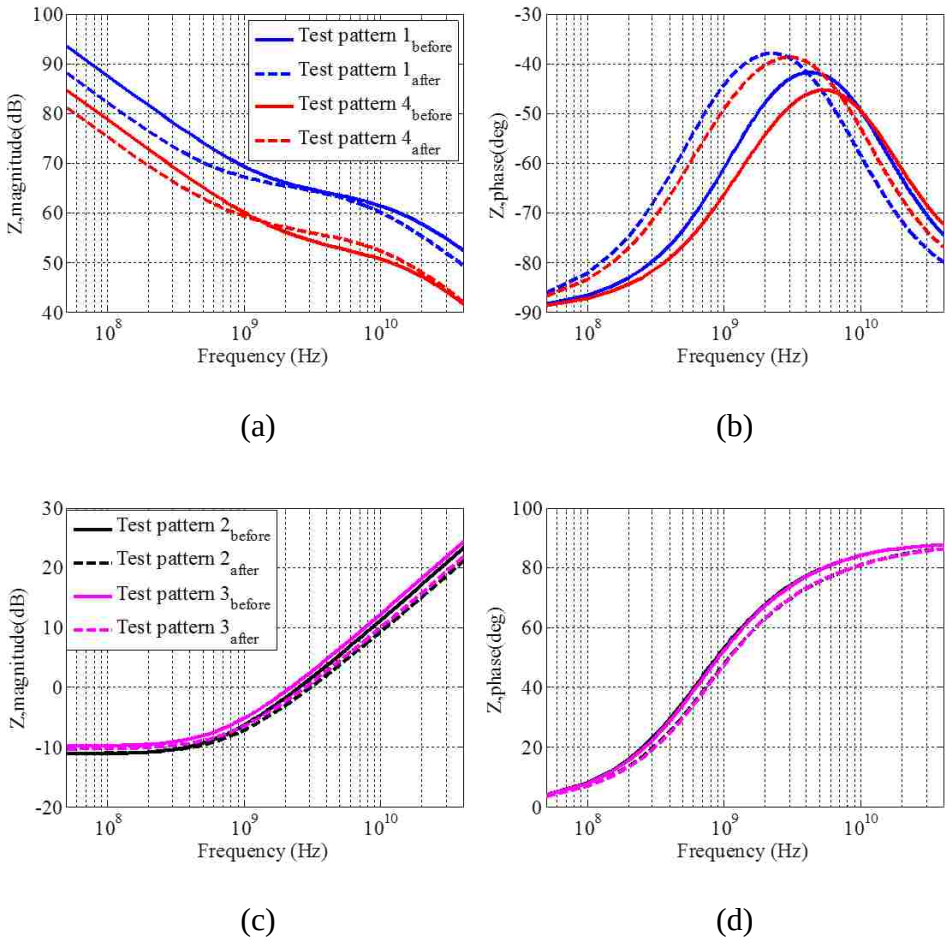
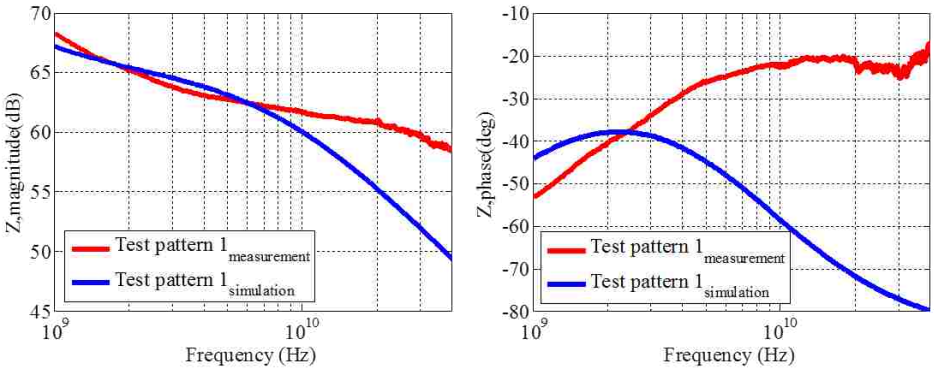


Figure 1.18. The simulation comparison results before and after optimization.

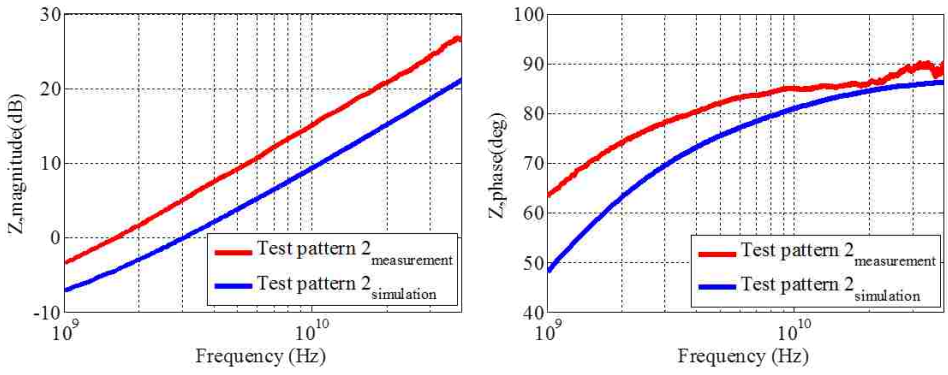
The capacitance at low frequencies for both test patterns 1 and 4 increases, while at high frequencies the parasitic capacitance increases for test pattern 1 and decreases for test pattern 4. Relatively small difference is observed for test patterns 2 and 3. By using the measured dimensions, the simulated inductance for both test patterns decrease a little since the loop size shrinks after model optimization.

1.5.5. Measurement and Simulation Results Correlation. By applying the measured structural information into the full wave models, accurate simulation results are obtained. Figure 1.19 shows the comparison results of Z-parameter between the measurement and simulation. Figure 1.19 (a) and (b), (c) and (d), (e) and (f), (g) and (h) represent the comparison results for test patterns 1, 2, 3 and 4, successively. Blue and red lines represent measurement and simulation results. Test patterns 1 and 4 are with open termination, the impedance performance is dominated by capacitance; test patterns 2 and 3 are with short termination, the impedance performance is dominated by inductance.



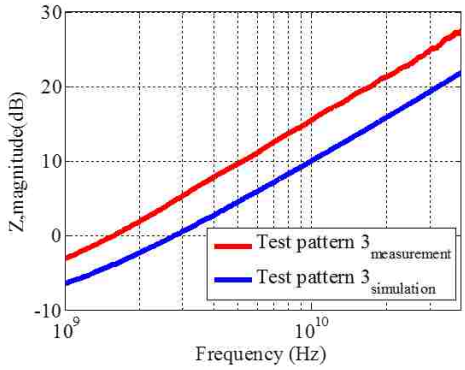
(a) (b)

Figure 1.19. The comparison results of Z-parameter between measurement and simulation of all test patterns.

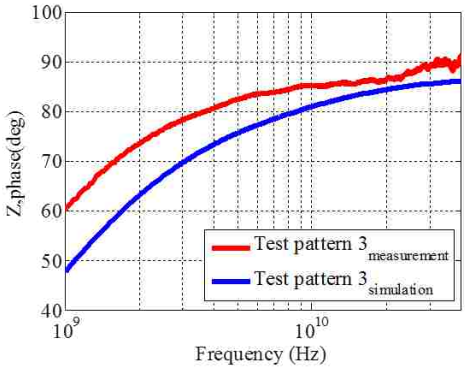


(c)

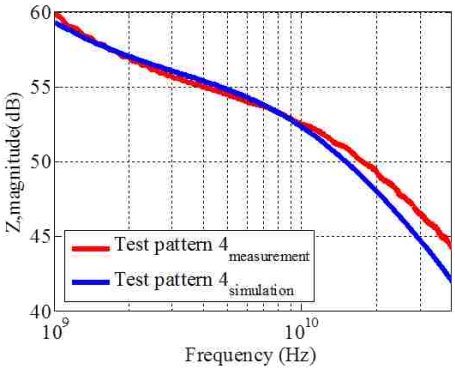
(d)



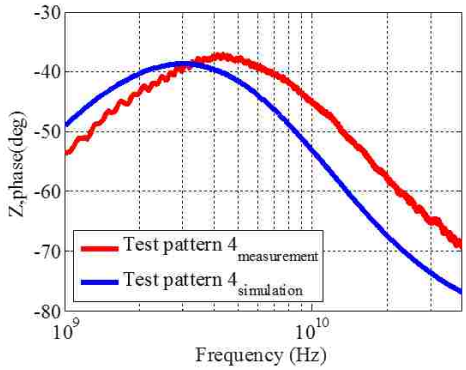
(e)



(f)



(g)

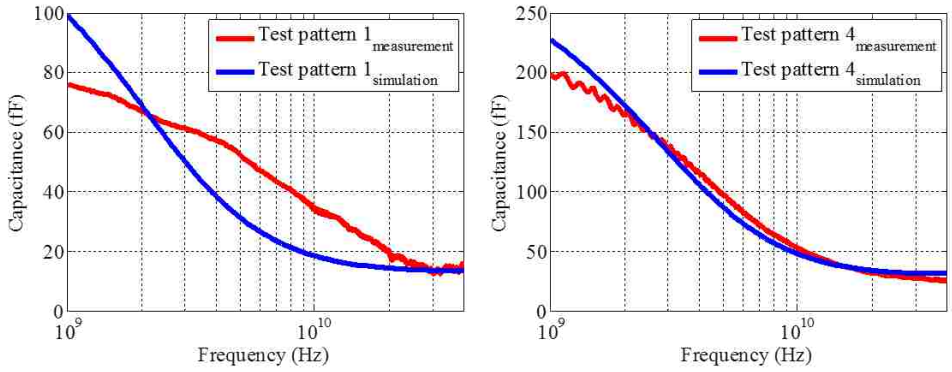


(h)

Figure 1.19. The comparison results of Z-parameter between measurement and simulation of all test patterns. (Cont)

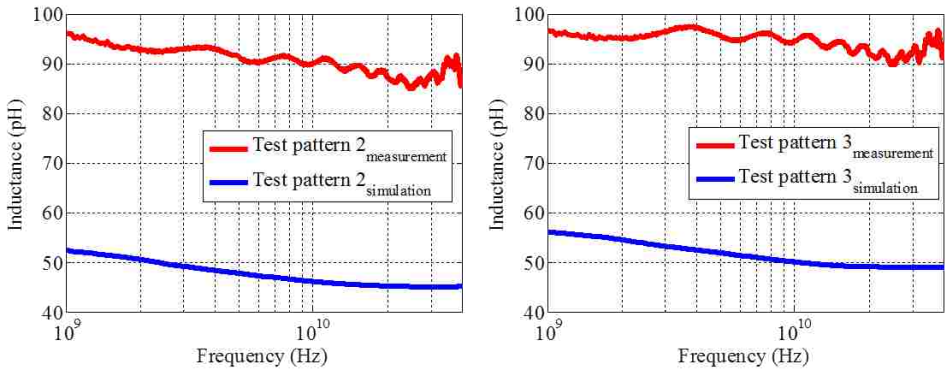
The comparison results indicate that, for test patterns 2 and 3, the differences of the Z-parameter between simulation and measurement are stable in the measured frequency, which are about 3.4 dB for magnitude and 12º for phase. For test pattern 1, relatively large difference is observed between the measurement and simulation results when the frequency is beyond 5 GHz, especially for the phase part. Best correlation between simulation and measurement is achieved in test pattern 1, with 2 dB for magnitude and 9º for phase. The possible reasons result in the non-ignorable difference will be discussed in next part.

1.5.6. Measurement Error Analysis. Further analysis regarding to the difference between the measurement and simulation results is provided. As shown in Figure 1.20 (a), (b) and (c), (d), corresponding capacitance and inductance are calculated for test patterns 1, 4 and test patterns 2, 3, respectively, based on the converted Z-parameters.



(a) (b)

Figure 1.20. The (a), (b) calculated capacitance for test patterns 1 and 4; and (c), (d) inductance for test patterns 2 and 3.



(c) (d)

Figure 1.20. The (a), (b) calculated capacitance for test patterns 1 and 4; and (c), (d) inductance for test patterns 2 and 3. (Cont)

From Figure 1.20, it can be seen that the calculated capacitance for test patterns 1 and 4 have relatively good correlation between simulation and measurement, which are in the range of 10 fF to 100 fF for test pattern 1 and 20 fF and 220 fF for test pattern 4, respectively. For test patterns 2 and 3, the calculated inductance values varies more between simulation and measurement: the calculated inductance are around 50 pH for test pattern 2 and 55 pH for test pattern 3 obtained from simulation; while they are around 90 pH for test pattern 2 and 95 pH for test pattern 3 obtained from measurement.

The possible reason that results in the difference of the calculated inductance is launching parasitic. Launching parasitic can be caused during the measurement by many factors, such as material difference between the substrate of the sample under test and the one used in the calibration substrate. The parasitic of the probe itself will introduce some extra parasitic inductance or capacitance in to the measurement results as well. Furthermore, since it's very difficult to ensure same landing condition during the measurement for each test pattern, the field excitation of the probe tips to the calibration

standards and the test patterns can be different, which future results in parasitic with different types and values. The study from [19] and [20] suggests that, the parasitic inductance for Model 40A GS probe with pitch size of 225 μm and CS-14 used as the calibration substrate is in the range of tens to hundred pH. In this paper, as the used calibration substrate is CS-8 instead of CS-14 and the pitch size of the adopted microprobe is 200 μm instead of 225 μm, different parasitic inductance will be introduced into the measurement. Actually, depends on the material difference between the calibration substrate and the one used in sample under test, and the landing difference of the measurement for different test patterns, it's possibly that both parasitic inductance and capacitance can be introduced into the measurement. The effect of launching parasitic can be further removed according to the study provided in [21].

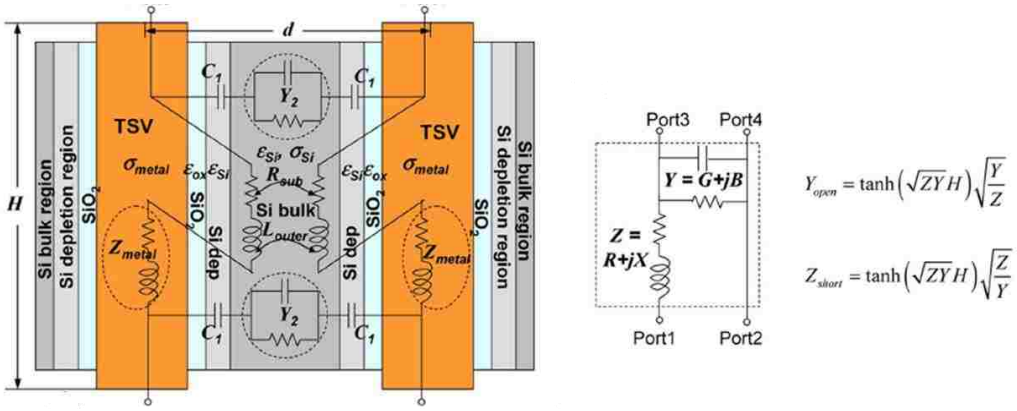
However, the studied TSV pair is in test patterns 4 in this paper, whose capacitance response along with the frequency is given in Figure 1.20 (b). Considering that the electrical performance of test pattern 4 is dominated by the TSV pair, and the effect of the parasitic inductance introduced by the probing pads and connecting traces is significantly small to the final impedance value, the proposed de-embedded can still extract the electrical performance of the studied TSV pair effectively and good correlation of the de-embedded results can be achieved between simulation and measurement, as will be shown in Section 1.6.

1.6. ELECTRICAL PERFORMANCE EXTRACTION OF TSV PAIR

The proposed de-embedding method is applied to both the simulation and measurement results to extract the electrical performance of the TSV pair. The effect of

the fixtures including the probing pads and connecting traces are removed after de-embedding. Furthermore, analytical solution [15] and full wave simulation for a single TSV pair are also available to verify the accuracy of the de-embedding results.

1.6.1. Analytical Solution. In [15], an equivalent distributed circuit (RLCG) model is proposed for a pair of TSVs. The MOS effect and AC conduction in silicon, the skin effect in the TSV metal, and the eddy currents in silicon are considered for the high-frequency analysis in this model, as shown in Figure 1.21.



(a) (b)

Figure 1.21. The structures and RLGC equivalent circuit model of one TSV pair.

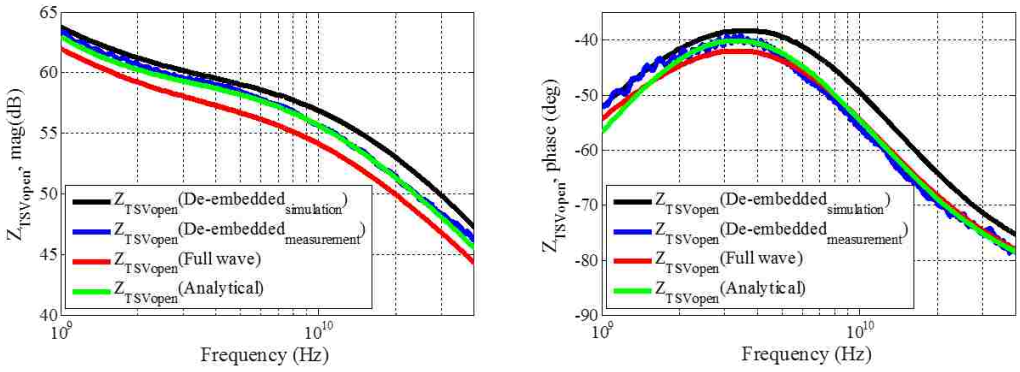
This modeling method is used to calculate the analytical impedance parameters of a single TSV pair to verify the feasibility and accuracy of the proposed de-embedding method. For a one-to-one comparison between the analytical model and the proposed TSV model, the Z_1 and Z_2 are calculated using the relationship given by:

$$Z_1 = \frac{Z}{2} \tag{1.15}$$

$$Z_2 = \frac{1}{Y} \tag{1.16}$$

where, Z and Y are the per unit length series impedance and the per unit length admittance for a single TSV pair in [15].

1.6.2. De-embedded Results and Results Validation. Figure 1.22 shows the comparison results of $Z_{TSVopen}$ obtained from different methods. The electrical response of the TSV pair with open termination is dominated by capacitance as shown in the above results. There is a transition to resistance around 1 GHz due to the property of the silicon substrate.



(a) (b)

Figure 1.22. The $Z_{TSVopen}$ comparison results.

Good agreement is achieved between the de-embedded results, the analytical solution and full wave simulation results up to 40 GHz. It demonstrates the accuracy of the models of the test patterns and the effectiveness of the proposed de-embedding method. Furthermore, corresponding capacitance of the TSV pair are calculated, as

shown in Figure 1.23. It can be known that the capacitance value of the studied TSV pair is around 140 fF at 1 GHz and gradually decreased to 20 fF when frequency goes up to 40 GHz.

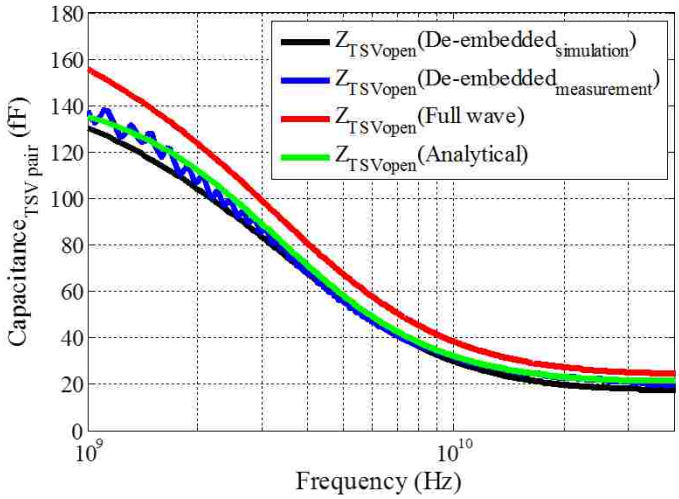


Figure 1.23. The comparison results of the calculated capacitance of the TSV pair.

At low frequency, the TSV-silicon substrate capacitance C_{SiO2} is dominated. When frequency goes higher than few gigahertzes, the TSV-to-TSV capacitance C_{Si} dominates.

1.7. CONCLUSION

In this paper, a very practical de-embedding method based on simple test patterns was introduced. The proposed test patterns were modeled accurately using a full wave solver up to 40 GHz and corresponding equivalent circuit models were analyzed. Further, frequency domain measurement is performed for the test patterns up to 40 GHz to verify

the accuracy and effectiveness of the full wave models, which were optimized further based on the dimension measurements using SEM. Finally, the de-embedding method was applied to both the full wave simulation and microprobe measurement results to extract the electrical behavior of the TSV pair with open termination. The de-embedded results were verified by both the analytical solution and the full wave simulation of one single TSV pair.

2. SIGNAL INTEGRITY EVALUATION OF EMBEDDED MULTI-DIE INTERCONNECT BRIGE (EMIB) AND SILICON INTERPOSER TECHNOLOGIES FOR NEXT GENERATION HIGH SPEED DESIGN

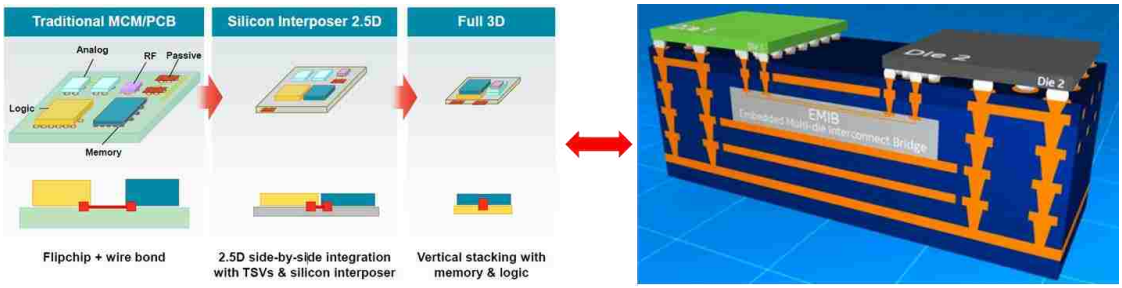
2.1. ABSTRACT

In this session, preliminary study is performed for signal integrity performance evaluation for EMIB technology. Full wave simulation models are developed for both EMIB and silicon interposer technologies. The comparison starts from a simple case in which only one trace pair is considered, and then a more complex case in which multiple trace pairs are included in the full wave simulation are also investigated. The comparison results indicate that, both EMIB and silicon interposer technologies have similar performance in terms of the insertion loss/return loss/crosstalk when no TSV is included in silicon interposer technology. However, with TSVs considered in silicon interposer technology, EMIB technology has better signal integrity performance compared with silicon interposer technology. Furthermore, for the complex case, parametric study of the capacitance value at the load end is performed to better evaluate the effect of the load condition to the eye diagram performance for both technologies. The comparison results provide importance and practical guidelines for next generation high speed design.

2.2. INTRODUCTION

Three-dimensional integrated circuit (3D-IC) and 2.5D interposer technology are very promising technologies to support Moore's Law. In 3D-IC technology, chips are stacked on top of each other in the vertical direction using TSVs. Higher operating frequency and interconnect density, lower power consumption can be achieved since shorter interconnects are realized by the 3D-IC technology. In 2.5D interposer

technology, a silicon interposer is placed between the chips and the package substrate. In EMIB technology, a small silicon chip is embedded in the underlying package substrate to enable the connection between two chips and offers ultra-high-density interconnect between dies [22-24]. Compared with the traditional 2.5D silicon interposer technology, the number of chips that can be integrated together is not limited by the physical dimension of the EMIB, thus very high density interconnection can be realized by adopting EMIB technology; however, in traditional 2.5D silicon interposer technology, a large piece of silicon interposer that is placed on top of the package substrate is used and the number of chips that can be integrated is determined by the area of the used silicon substrate. It makes the solution cost prohibitive and surfer from many issues, such as warpage, etc. Figure 2.1 shows the concept figures of traditional 2.5D interposer, 3D-IC and EMIB technologies.



(a) (b)

Figure 2.1. The concept figures of traditional 2.5D interposer, 3D-IC and EMIB technologies.

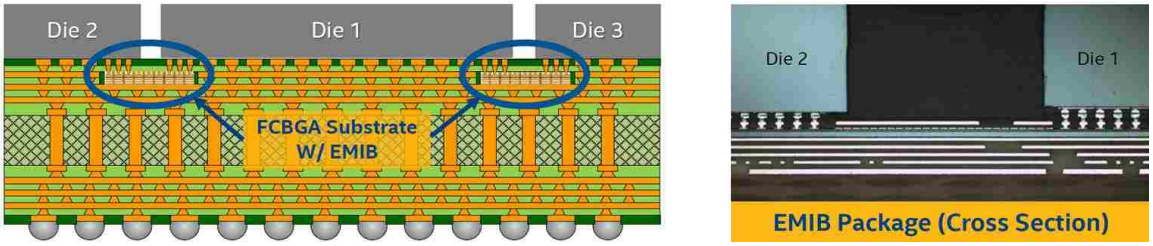
Since EMIB is a novel interconnection technology that is newly proposed by Intel, there isn't much research related to its signal integrity performance evaluation readily available yet. In this session, the signal integrity performance of EMIB technology is investigated and then compared with silicon interposer technology to provide practical guidelines for the next generation high speed designs. In Section 2.3, full wave models are developed for both EMIB and silicon interposer technologies to study the corresponding electrical performance. For silicon interposer technology, three different cases are proposed considering the chips may be placed on the same or/and the opposite sides of the silicon interposer. In Section 2.4, the signal integrity performance is compared between EMIB and silicon interposer technologies. The investigation starts from simple case in which only one trace pair is considered, and then a more complex case is studied as well in which three differential pairs are considered in the full wave simulation. Comparison results of insertion loss, return loss, near-end crosstalk, far-end crosstalk and eye diagrams between the two technologies are provided as criteria of the signal integrity performance evaluation. Conclusion is given in Section 2.5.

2.3. FULL WAVE MODELING

In this Section, broadband full wave simulation models for both technologies are developed using a full wave solver up to 50 GHz.

2.3.1 EMIB Technology. Full wave modeling for EMIB technology is challenging since there is no accurate dimensional information readily available. Only concept configuration is provided in some official documents provided by Intel and Altera, as show in Figure 2.2 and Figure 2.3. Figure 2.2 (a) represents the concept figure of EMIB technology provided by Intel and Figure 2.2 (b) shows the cross-Sectional view

of EMIB package measured under SEM. From the following two figures, it can be seen that a small silicon chip is embedded in the package to realize very high density connection between two chips in EMIB technology. Very few TSVs are required in EMIB technology, and the elimination of TSVs enables many advantages such as low cost, high yield and high manufacturing repeatability compared with silicon interposer technology.



(a) (b)

Figure 2.2. The (a) concept configuration of EMIB technology from Intel and (b) the cross-sectional view of EMIB taken by SEM.

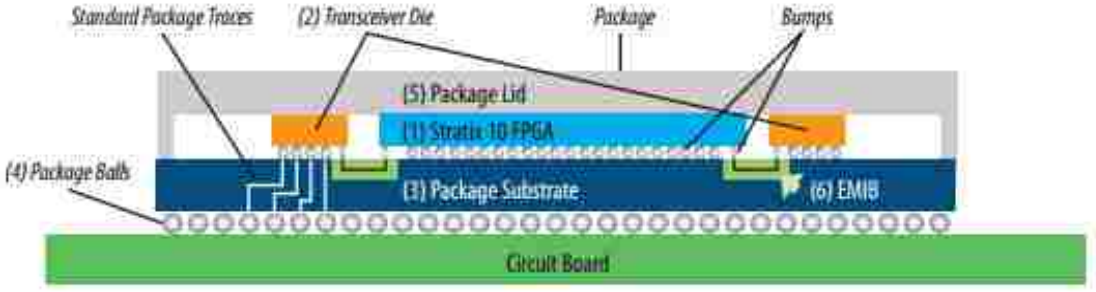


Figure 2.3. The concept figure of EMIB technology provided by Altera.

To develop more accurate full wave simulation model for EMIB technology, detailed interconnections used to enable the connection between the chip and EMIB such as the micro-vias and small pads in chips; the micro-bumps, vias and pads in the package, are considered. Since there is no dimension information that is readily available, more investigation is required to determine the reasonable dimension range of the detailed interconnections in EMIB technology.

In [25] and [26], recommended dimensions for the detailed structures are provided, as shown in Table 2.1 and Table 2.2.

Table 2.1. Recommended dimensions of TSV and micro-bump from Amkor.

				2015	2016
TSV Via Size	μm				
3D wafer thickness	50	50	40	30	<
3D TSV dia/depth	5/50	5/50	4/40	3/30	<
2.5D TSV wafer thickness	100	100	70	60	50
2.5D TSV dia/depth	10/100	10/100	10/70	10/60	10/50
Micro-bump	μm				
Cu pillar pitch	40	40	30	20	<
Cu pillar diameter	20	20	15	10	<
Cu pillar height	40	40	30	25	<
Bump pad size	20	20	15	10	<

Table 2.2. Recommended dimensions of TSV and substrate from Xilinx.

Overall package	Body size	42.5*42.5 mm
Top chip	Chip size	4 slices Each 7 mm*12 mm
	Pitch/solder	45 μm /SnAg
TSV interposer	Via diameter	10 μm
Organic substrate	Core thickness	800 μm
	BGA pitch	1 mm
	Interposer pitch	180 μm

A schematic of package configuration is available in [26], as shown in Figure 2.4.

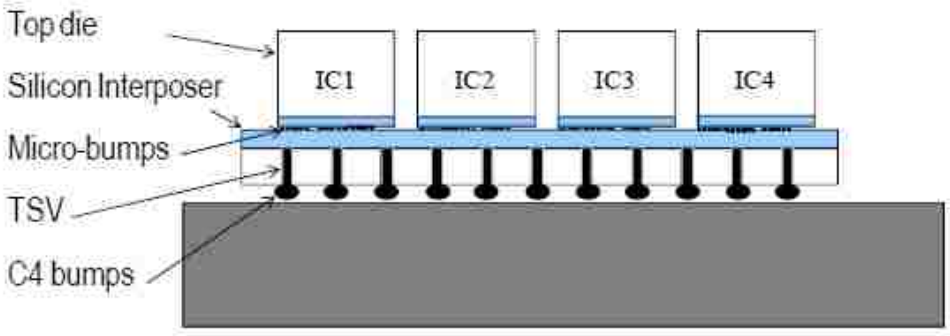
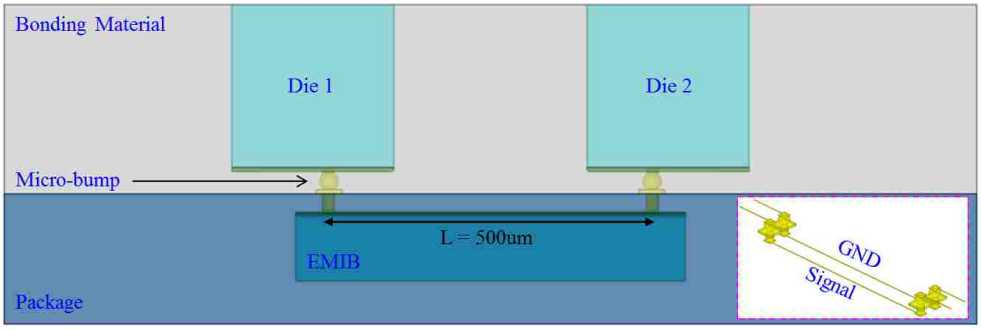


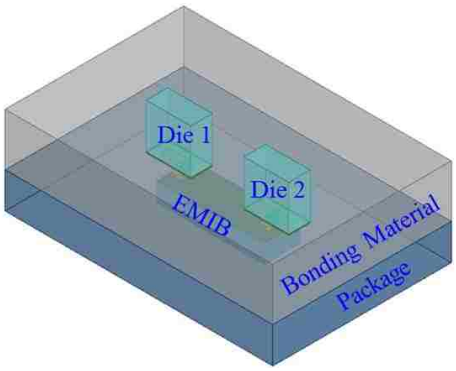
Figure 2.4. The schematic of package configuration.

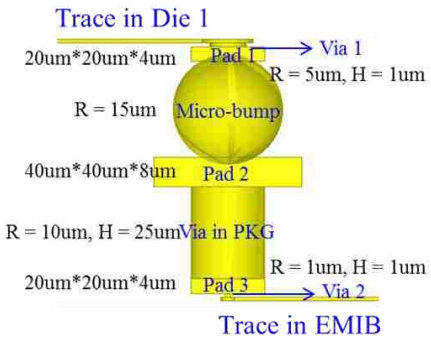
Based on above study, the full wave simulation model for EMIB technology is developed with reasonable dimension considered. The developed full wave model is shown in Figure 2.5. Figure 2.5 (a) and (b) show the cross-Sectional view and the 3D view of the full wave model for EMIB technology, respectively. Figure 2.5 (c) shows the

configuration of the interconnection between chip and EMIB with dimension information presented. According to the full wave simulation model, two dies are connected with each other via EMIB, which is embedded in the package. Bonding material is considered to better represent the real application. The material for package and bonding structure are chosen to be Teflon and Polymaid according to [27 - 29]. In this case, only one single trace pair, in which one trace serves as signal and the other one serves as GND, is considered in the full wave model.



(a)





(b) (c)

Figure 2.5. The (a) cross-sectional, (b) 3D views of full wave model of EMIB, (c) detailed configuration of the interconnections from die to EMIB with dimension information presented.

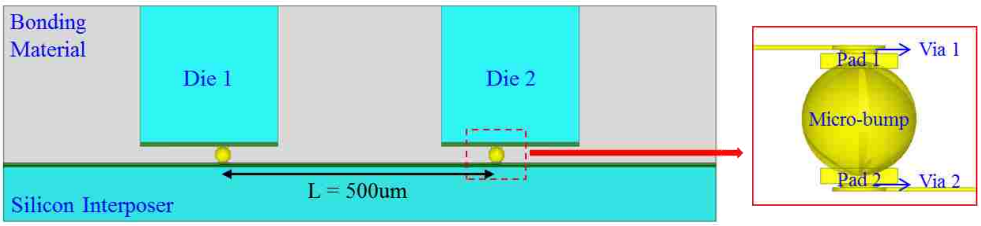
The detailed interconnection from the traces in die 1 to the traces in EMIB technology is shown in Figure 2.5 (c): chip level via and pad, package level micro-bump and pad, finally connected with the traces in EMIB with via in package and chip level pad and via. Detailed dimensions of the structures applied in the full wave simulation model for EMIB technology is provided in Table 2.3.

Table 2.3. Detailed dimensions of the structures applied in the full wave simulation model for EMIB technology.

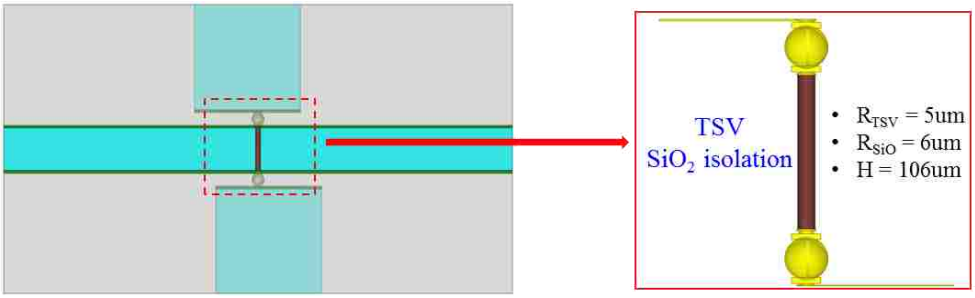
Geometry	Dimension
Die 1&Die 2	250 μm *120 μm *250 μm
EMIB chip	600 μm *200 μm *107 μm
Package	1500 μm *1000 μm *200 μm
Bonding material	1500 μm *1000 μm *293 μm
Height of SiO2 in Die 1&2	4 μm + 3 μm
Height of SiO2 in EMIB	4 μm + 3 μm
Trace width/thickness	2 μm /1 μm

2.3.2 Silicon Interposer Technology. Full wave models for silicon interposer technology are developed as well. Considering the chips can be both on the same or/and the opposite sides of the silicon interposer, three different cases are taken into consideration when developing the full wave simulation models for silicon interposer technology. Figure 2.6 (a), (b) and (c) show the full wave simulation modeling for case 1,

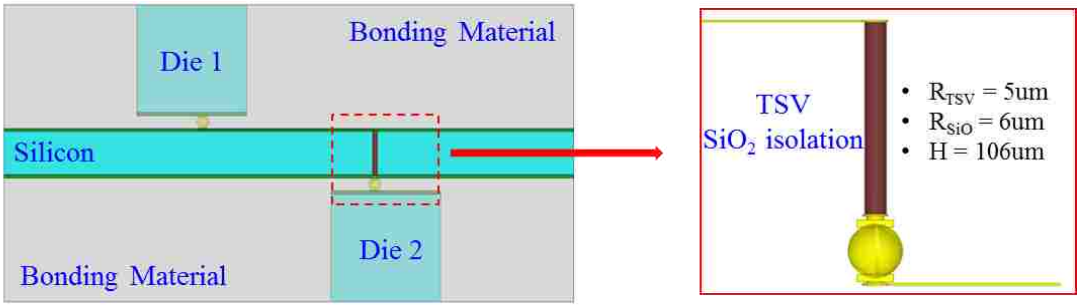
case 2 and case 3. Compared with EMIB technology, there is no package level via required as the chips are directly connected with the silicon interposer in 2.5D silicon interposer technology.



(a)



(b)



(c)

Figure 2.6. The full wave models for silicon interposer technology of (a), (b), (c) corresponds to case 1, case 2 and case 3.

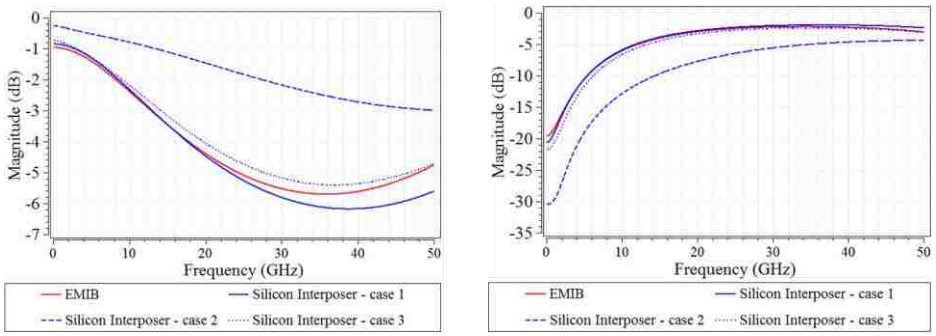
In case 1, the chips are placed on the same side of the silicon interposer, no TSVs are required in this case; in case 2, two chips are placed on different sides of the interposer and connected directly with each other by TSVs, no extra trace existing in this case to realize the connections; case 3 is similar with case 2, two chips are placed on different sides of the silicon interposer, but extra traces with length of 500 μm are implemented in the horizontal direction between chip 1 and chip 2.

2.4. PERFORMANCE COMPARISON BETWEEN EMIB AND SILICON INTERPOSER TECHNOLOGIES

In this Section, the signal integrity performance of EMIB technology is evaluated from the perspectives of insertion loss, return loss and eye diagram performance. The comparison results between EMIB and silicon interposer technologies are provided as well in this Section. In part 2.4.1, a simple case will be studied in which only one trace pair is considered. In part 2.4.2, a more complex case is discussed in which three differential pairs are developed in the full wave simulation model.

2.4.1. Single Trace Pair. The full wave simulation models with single trace pair considered are shown in Figure 2.5 and Figure 2.6 for EMIB and silicon interposer technologies, respectively. In the models developed for both technologies, the traces are all with widths of 2 um, thicknesses of 1 um, lengths of 500 μm and the edge-to-edge gap of 45 μm. Lumped ports with given impedance of 50 ohm are applied in all the simulation models. The comparison results of the calculated insertion loss and return loss are shown in Figure 2.7 (a) and (b), respectively. It can be known from the comparison results that, the insertion loss and return loss for case 2 in silicon interposer technology are -3 dB and -5 dB at 50 GHz; while the values are around -5 dB and -3 dB at 50 GHz

for the other three cases. Case 2 in silicon interposer technology has the smallest insertion loss and the largest return loss, since it has the shortest signal path compared with the ones in the other cases. The other three cases have similar performance with each other since they have signal paths with similar lengths. Furthermore, the insertion loss for all cases doesn't start from 0 dB due to the high resistance caused by the narrow and thin traces applied in the full wave models.



(a) (b)

Figure 2.7.The comparison results of (a) insertion loss and (b) return loss.

Besides the comparison of insertion loss and return loss, the eye diagram performance is evaluated as well. Channel simulation is performed in advanced design system (ADS) to calculate the eye diagrams for both technologies. The setup for the eye diagram calculation is simple as shown in Figure 2.8. A transmitter is connected with the S-parameter block and a 100 fF capacitor [30 - 32] is adopted at the load end. A single-ended eye probe is used at the load end to detect the eye diagram of the channel. PRBS 31 is adopted in the channel simulation with bit rate of 20 Gbps. The highest and lowest

voltages are set to be 1 V and 0 V, respectively. The rise and fall time are both 20 psec. Furthermore, the source impedance is set to be 50 ohm for all cases, to keep consistent with the settings in full wave simulation.

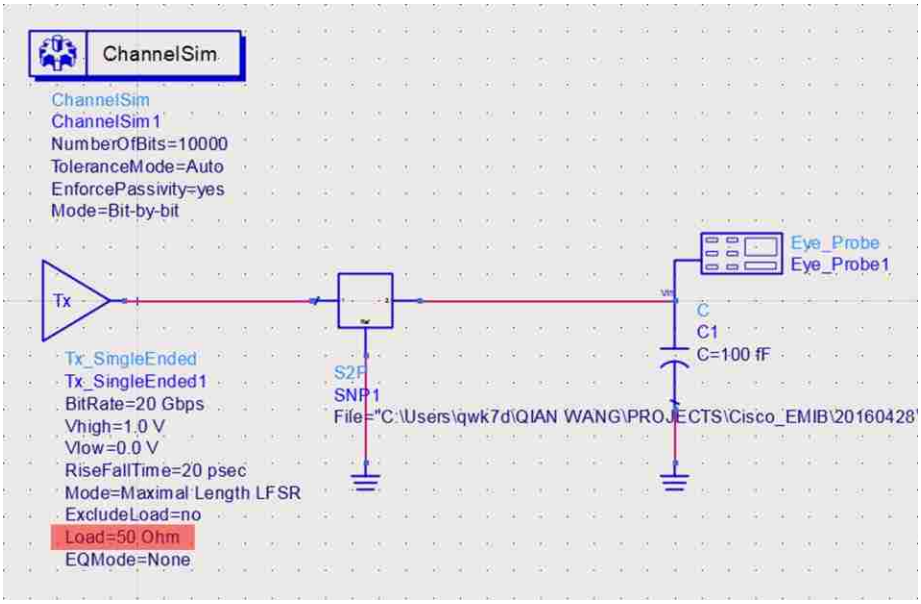


Figure 2.8. The setup for eye diagram calculation.

The calculated eye diagrams are shown in Figure 2.9. Figure 2.9 (a), (b), (c) and (d) represent the calculated eye diagrams for EMIB technology, case 1, case 2, and case 3 in silicon interposer technology, respectively. Since the source impedance used for the transmitter is 50ohm, there will be reflection caused by the impedance mismatch between the source and the simulated geometries. Compared with silicon case 2, more severe reflection is observed in EMIB technology, case1 and case 3 in silicon interposer technology.

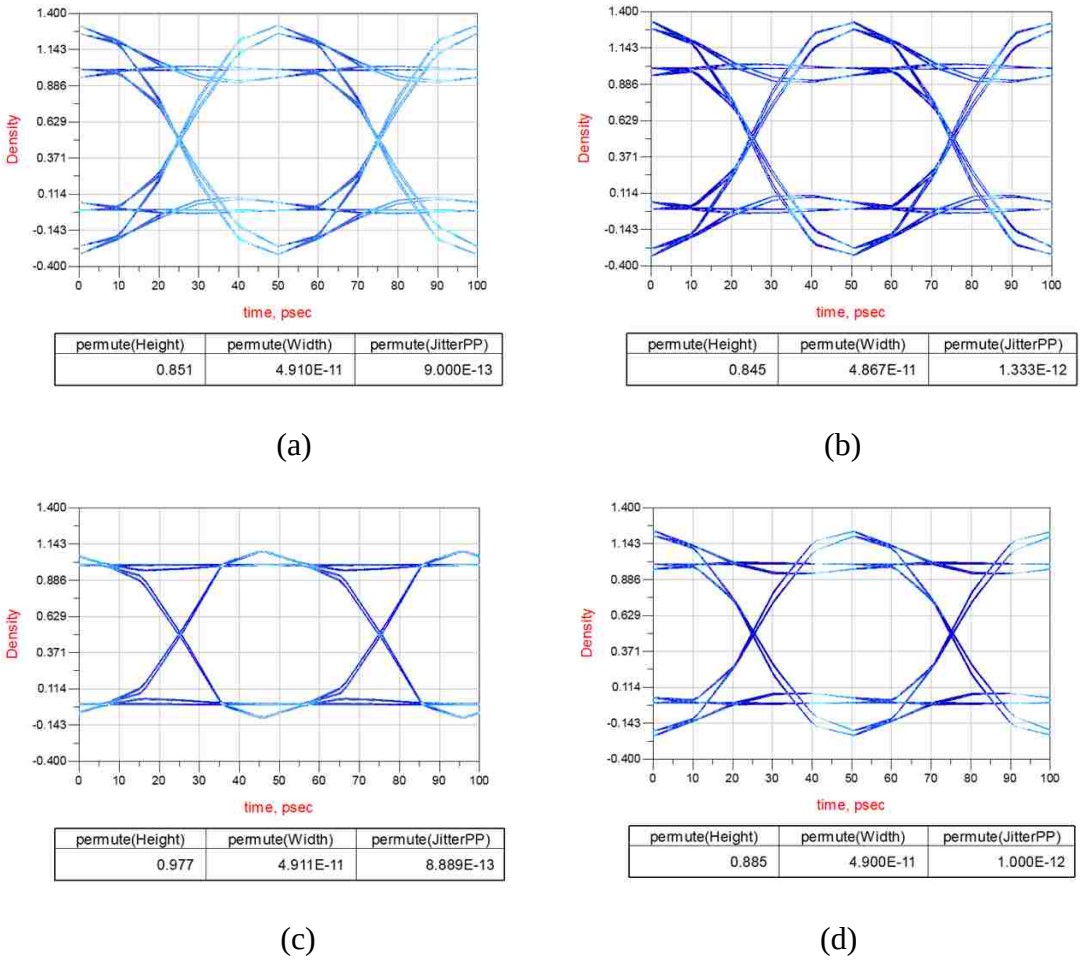


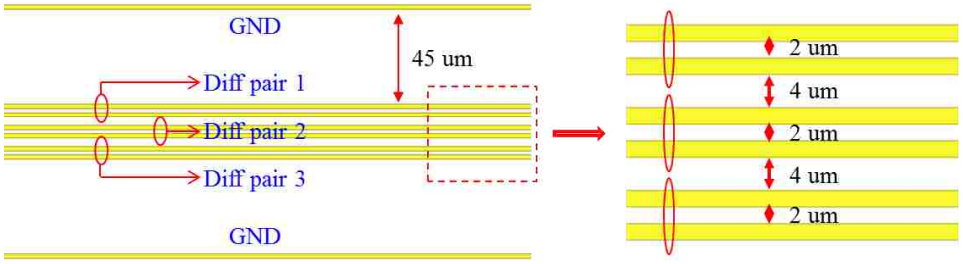
Figure 2.9. The eye diagrams for (a) EMIB, (b) case 1, (c) case 2, and (d) case 3 of silicon interposer technology.

Furthermore, the calculated total jitter for EMIB, case 1, case 2 and case 3 of the silicon interposer technologies are 0.9 psec, 1.3 psec, 0.89 psec and 1 psec, respectively. Since case 2 in silicon interposer has the smallest insertion loss, it has the largest eye height, width and smallest total jitter accordingly compared with the other cases.

2.4.2. Multiple Trace Pairs. Based on the study of the simple case, more complex case is considered for both EMIB and silicon interposer technologies. Three differential pairs are considered in this case in the full wave simulation models. The trace

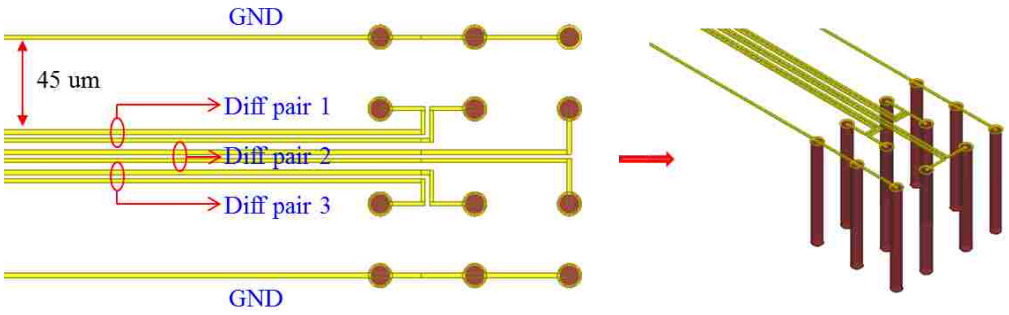
are all with widths of 2 μm and thicknesses of 1 μm, the gaps between two traces in a differential pair are 2 μm, the gaps between 2 diff pairs are 4 μm. In the full wave simulation model for EMIB technology, only traces are considered in the full wave simulation, the detailed interconnection between the chip and EMIB, such as the micro-bumps, are not considered in the full wave models for simplicity of the modeling. The total lengths of the traces are all 500 μm, no TSVs are included. In Silicon interposer technology, 16 TSVs are included besides the traces. The TSVs are with diameters of 10 μm and heights of 100 μm, with a 0.5 μm thick SiO_2 surrounded. Considering the significant number of the traces and TSVs, wave ports are applied in the full wave simulations. Different with lumped port, the impedance of wave port is automatically matched with the impedance of the simulated geometry during simulation. The simulated frequency is from 50 MHz to 50 GHz.

Figure 2.10 (a) and (b) show the full wave simulation models for EMIB and silicon interposer technologies with three differential pairs, respectively.



(a)

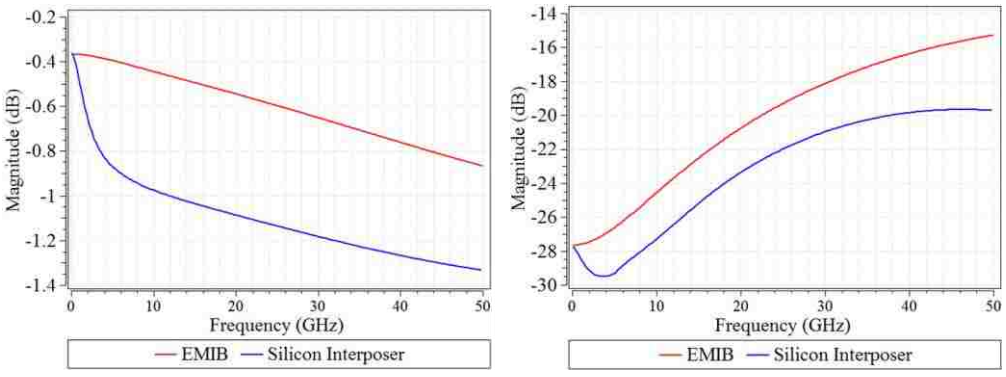
Figure 2.10. The developed full wave models for (a) EMIB, (b) silicon interposer technologies with three differential pairs.



(b)

Figure 2.10. The developed full wave models for (a) EMIB, (b) silicon interposer technologies with three differential pairs. (Cont)

The calculated insertion loss and return loss results for both technologies are shown in Figure 2.11 (a) and (b). The red and blue lines represent the results for EMIB and silicon interposer technologies, respectively. The silicon effect can be observed in silicon interposer technology around 2 GHz to 4 GHz.



(a) (b)

Figure 2.11. The calculated insertion loss and return loss for (a) EMIB, (b) silicon interposer technologies.

Furthermore, since there are no TSVs considered in the full wave simulation model for EMIB technology, it has smaller insertion loss compared with silicon interposer technology.

Near-end crosstalk (NEXT) and far-end crosstalk (FEXT) comparison results between EMIB and silicon interposer technologies are analyzed as well, as shown in Figure 2.12. The red and blue lines represent the results for EMIB and silicon interposer technologies; the solid and dashed lines represent the results for NEXT and FEXT, respectively.

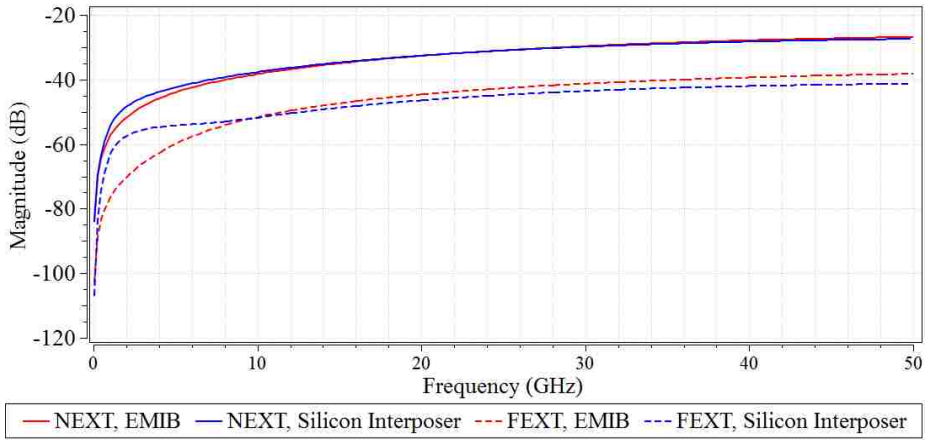


Figure 2.12. Near-end crosstalk (NEXT) and far-end crosstalk (FEXT) comparison results between EMIB and silicon interposer technologies.

EMIB technology has very similar NEXT and FEXT performance with silicon interposer technology when frequency beyond 8 GHz. The average level is around -30 dB for NEXT and around -40 dB for FEXT for both technologies. However, silicon

interposer technology has relatively severer crosstalk compared with EMIB technology, due to the noise coupling introduced by the TSVs.

Channel simulation is performed to study of the eye diagram for both technologies for the complex case. The setup for eye diagram calculation in ADS is as shown in Figure 2.13.

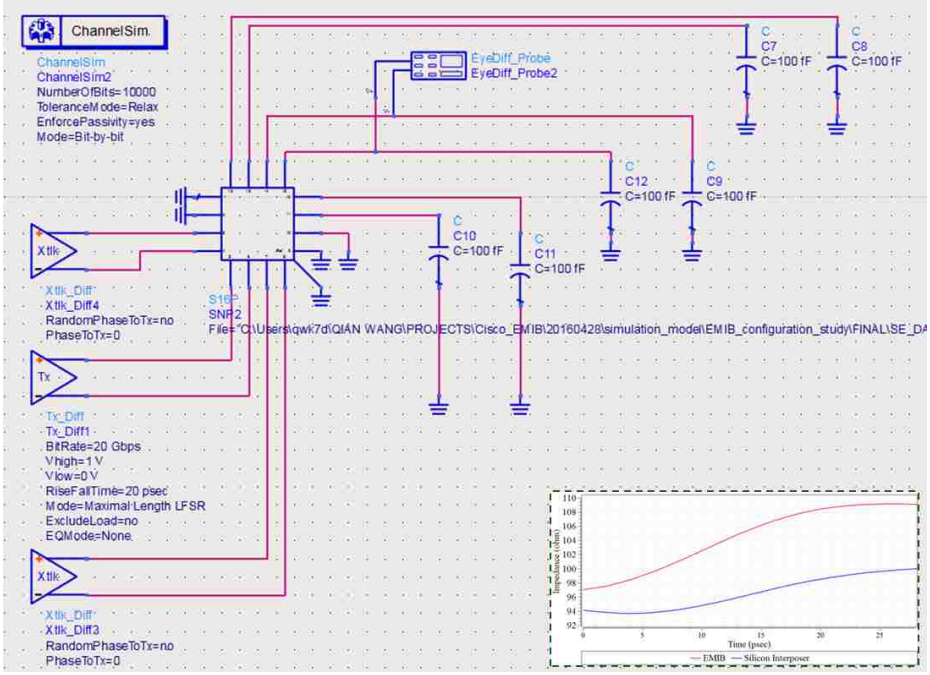
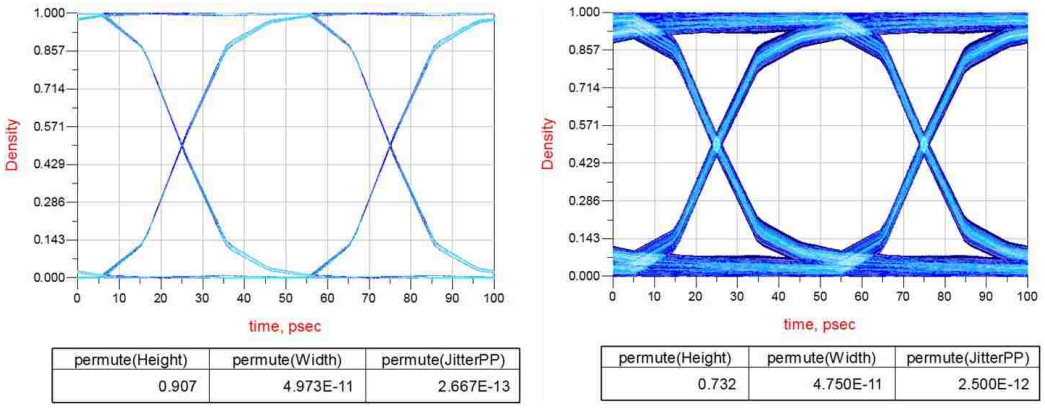


Figure 2.13. The setup for eye diagram calculation in ADS for complex case.

Since wave ports are used in the full wave simulations for the studied complex case, the source impedance of both the transmitter and crosstalk transmitters are set to be the same as the impedance of the simulated differential pairs. The impedance distribution of the simulated differential pair is shown in the green dashed rectangle in Figure 2.13.

A differential transmitter is used at the excitation end and connected to the two ports corresponding to the middle differential pair of the S-parameter block; the ports of the other two differential pairs at the excitation end are connected with two crosstalk transmitters. All other ports the S-parameters block at the load end are connected with 100 fF capacitors. PRBS 31 with bit rate of 20 Gbps is applied in the channel simulation. The highest and lowest voltages are set to be 1 V and 0 V. The rise and fall time are both 20 psec. A differential eye probe is used to detect the eye diagram at the load end.

Considering that the phase difference between the transmitter and the crosstalk transmitters can either be fixed as 0 or random in real applications, both synchronous crosstalk and asynchronous crosstalk are investigated for the complex case. The calculated eye diagrams considering synchronous crosstalk for both EMIB and silicon interposer technologies are as shown in Figure 2.14 (a) and (b), respectively.

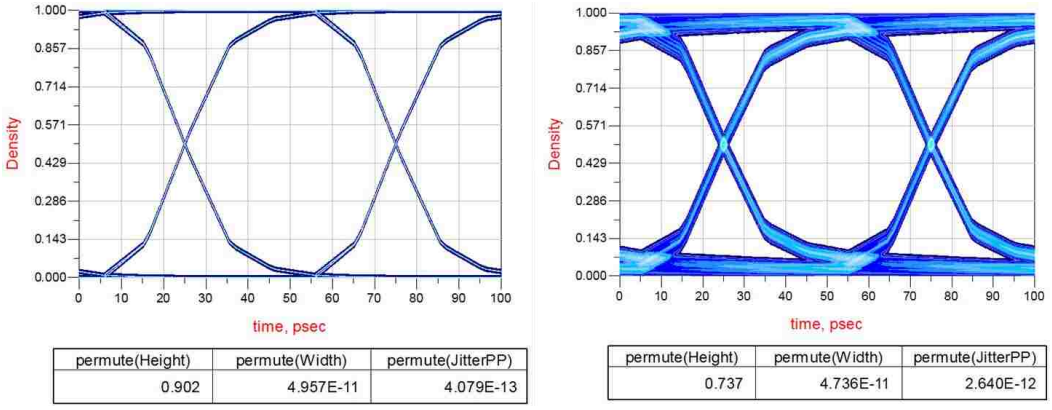


(a) (b)

Figure 2.14. The calculated eye diagrams for (a) EMIB and (b) silicon interposer technologies for synchronous case.

The comparison results suggest that, the total jitter becomes more severe in silicon interposer technology since TSVs are introduced into the full wave model for silicon interposer technology. The eye height and width become smaller accordingly in silicon interposer technology.

The comparison results of calculated eye diagrams for asynchronous case are obtained as well, as shown in Figure 2.15. Figure 2.15 (a) and (b) represent the calculated eye diagrams for EMIB and silicon interposer technologies, respectively. Similar conclusion is obtained for asynchronous crosstalk: the silicon interposer technology has worse eye diagram performance due to much effective silicon effect introduced by TSVs.



(a) (b)

Figure 2.15. The calculated eye diagrams for (a) EMIB and (b) silicon interposer technologies for asynchronous case.

To investigate the effect of the load capacitance to the performance of the eye diagram, three different capacitance values (10 fF, 100 fF and 500 fF) are applied in the channel simulation in ADS for both technologies. The comparison results of eye

diagrams for synchronous case are shown in Figure 2.16. Figure 2.16 (a), (c), (e) represent the corresponding results for EMIB technology with capacitance value of 10 fF, 100 fF and 500 fF; while Figure 2.16 (b), (d), (f) represent the corresponding results for silicon interposer technology with capacitance value of 10 fF, 100 fF and 500 fF, respectively.

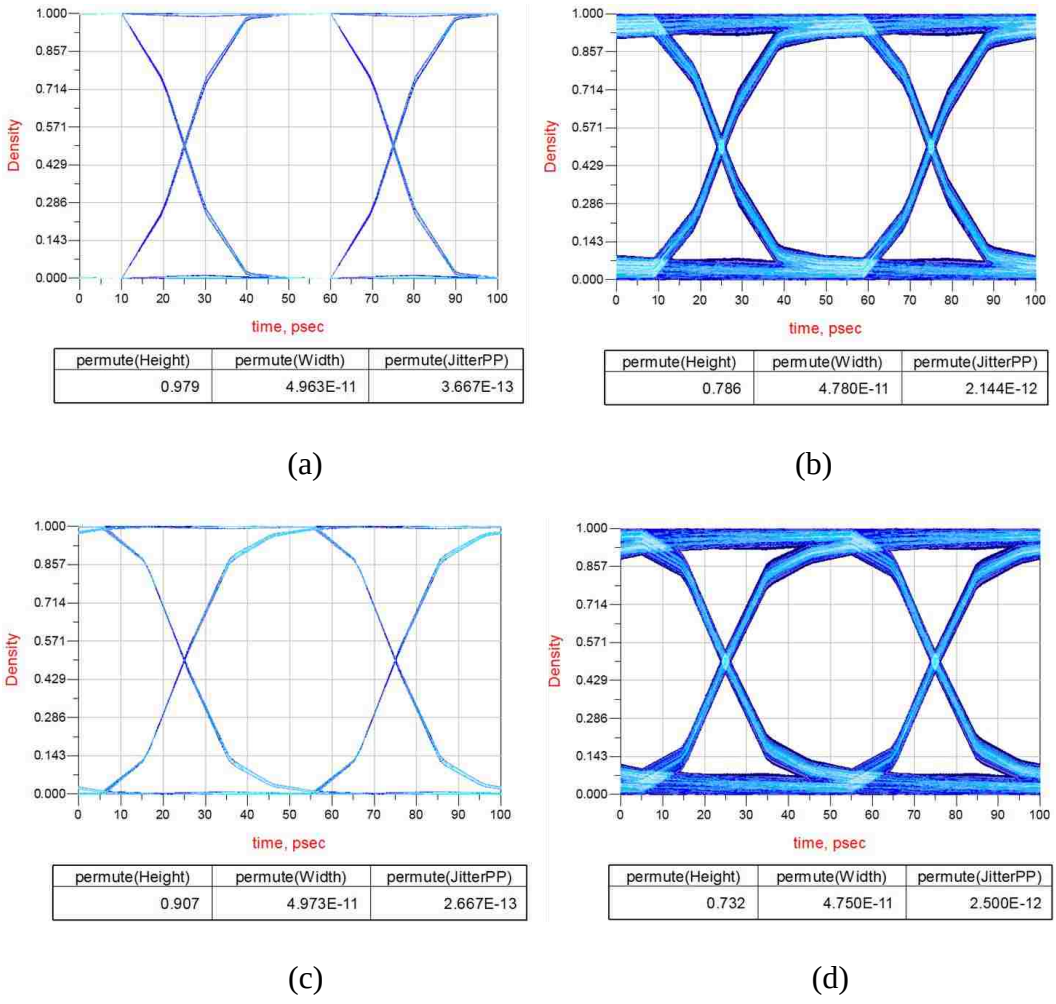
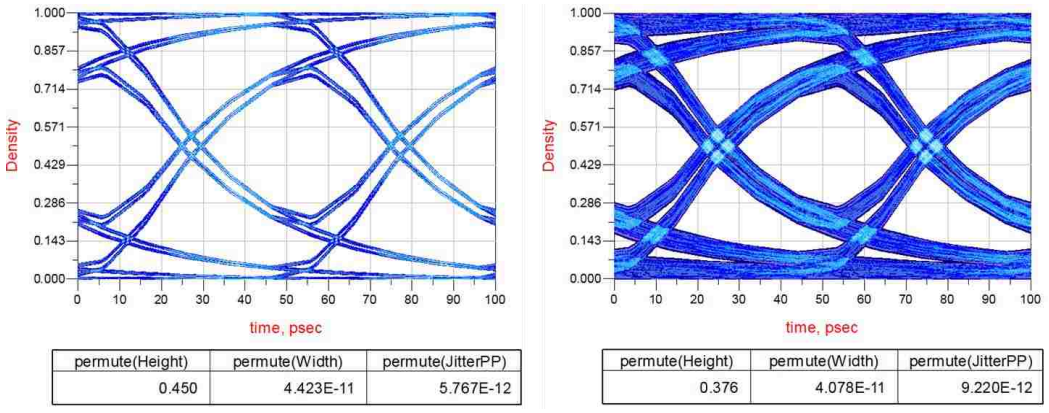


Figure 2.16. The calculated eye diagrams in synchronous case of (a), (c), (e) EMIB technology, (b), (d), (f) silicon interposer technology with different load capacitances applied.

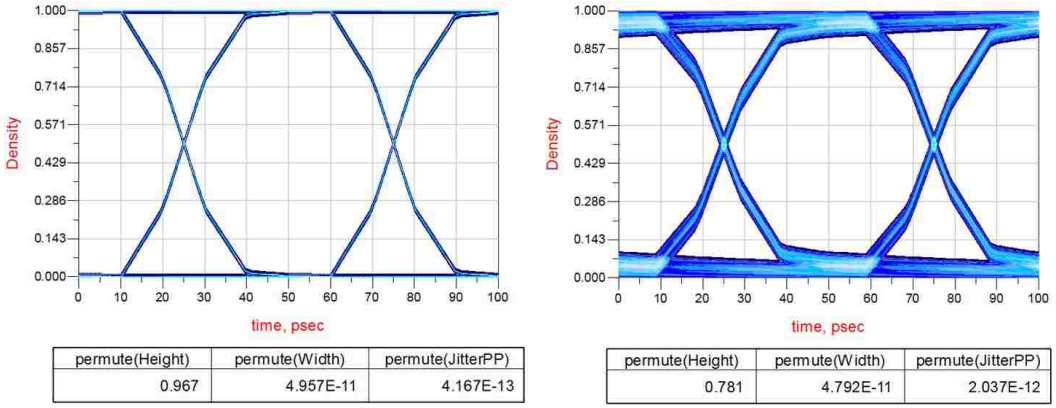


(e) (f)

Figure 2.16. The calculated eye diagrams in synchronous case of (a), (c), (e) EMIB technology, (b), (d), (f) silicon interposer technology with different load capacitances applied. (Cont)

With the increase of the values of the load capacitance, the total jitter becomes larger due to the increase of resistance-capacitance (RC) time constant. More severe inter symbol interference (ISI) is observed in the case with 500 fF load capacitance.

The comparisons of eye diagram for asynchronous case are shown in Figure 2.17. Figure 2.17, (a), (c), (e) represent the corresponding results for EMIB technology, (b), (d), (f) represent the corresponding results for silicon interposer technology. Similar conclusion can be obtained for asynchronous case compared with the synchronous one. The larger the capacitance values are, the larger the total jitters are introduced into the calculated eye diagram for both technologies. ISI issues become more severe when the load capacitance value is increased into 500 fF for both technologies. Due to the increase of the time constant when larger load capacitance is used, it will take longer time for the ‘high/low’ signal goes back to ‘low/high’.

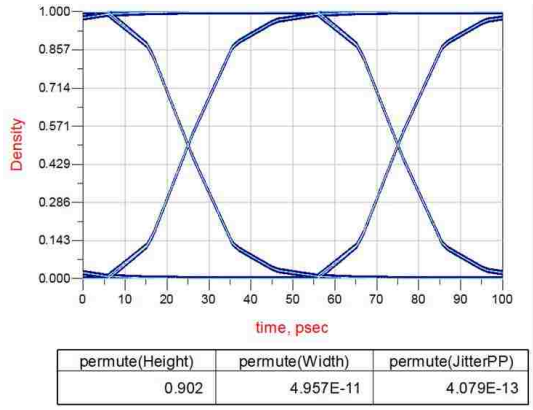


permute(Height)	permute(Width)	permute(JitterPP)
0.967	4.957E-11	4.167E-13

(a)

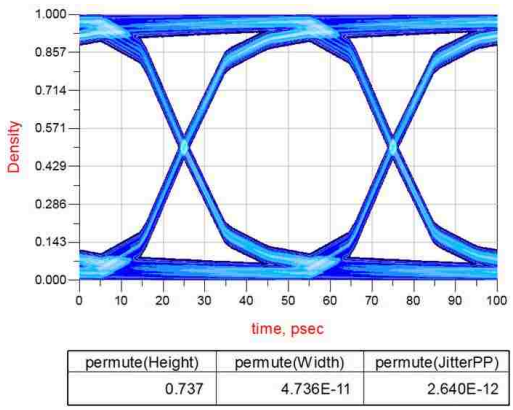
permute(Height)	permute(Width)	permute(JitterPP)
0.781	4.792E-11	2.037E-12

(b)



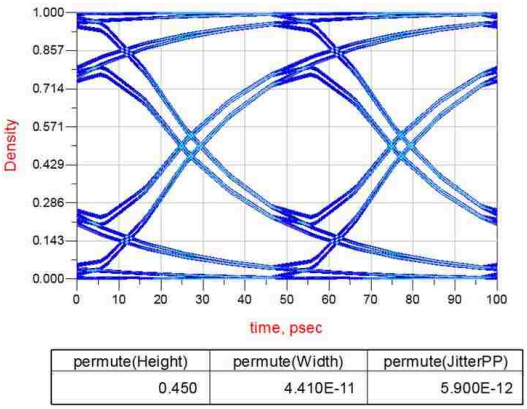
permute(Height)	permute(Width)	permute(JitterPP)
0.902	4.957E-11	4.079E-13

(c)



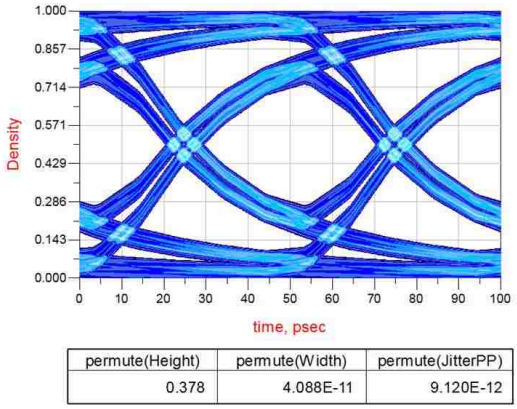
permute(Height)	permute(Width)	permute(JitterPP)
0.737	4.736E-11	2.640E-12

(d)



permute(Height)	permute(Width)	permute(JitterPP)
0.450	4.410E-11	5.900E-12

(e)



permute(Height)	permute(Width)	permute(JitterPP)
0.378	4.088E-11	9.120E-12

(f)

Figure 2.17. The calculated eye diagrams in asynchronous case of (a), (c), (e) EMIB technology, (b), (d), (f) silicon interposer technology with different load capacitances applied.

2.5. CONCLUSION

Preliminary study of signal integrity performance evaluation is provided for both EMIB and silicon interposer technologies. The obtained results suggest similar performance between EMIB technology and silicon interposer technology in terms of the insertion loss/return loss/crosstalk when no TSVs are considered. However, better signal integrity performance is observed in EMIB technology compared with silicon interposer technology with TSVs are considered, since the noise coupling between TSVs. As next step, the coupling effect between TSVs can be investigated more thoroughly for silicon interposer technology, considering the effect of the distances between the TSVs, the thickness of the SiO_2 surrounding the TSVs to the signal integrity performance of the technology. Power integrity performance for both technologies can be evaluated as well for EMIB and interposer technologies can be evaluated.

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