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A hybrid cavity and parallel-plate PEEC method for analysis of complex power net area fills, and a tool development for peak distortion analysis

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Department:

A HYBRID CAVITY AND PARALLEL-PLATE PEEC METHOD FOR ANALYSIS OF COMPLEX POWER NET AREA FILLS, AND A TOOL DEVELOPMENT FOR PEAK DISTORTION ANALYSIS

by

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ABSTRACT

Modern ASICs and FPGAs are becoming more and more dense, which is causing an increasing demand of the current draw from the power distribution network (PDN). And one of the main design objectives of a power distribution network is to reduce the voltage noise ripple below a specified allowable limit. Although the target impedance is a commonly used criterion in most PDN designs, it may not be efficient because it's usually rather pessimistic. Herein a time domain voltage ripple decomposition approach is proposed to avoid overdesign as well as provide design guidance to PI engineers. Based on a physics-based circuit model for PDN and a switching current generator including both high frequency switching and low frequency power gating, the total voltage ripple can be divided into several components. Each component will have a one-to-one correspondence to the real PDN geometry. Thus design curves can also be derived, which can guide PI engineers when making design decisions.

Peak distortion analysis (PDA) is commonly used to find the worst-case eye diagram and data pattern. Compared to traditional long transient simulations, PDA can significantly reduce the computation time by only taking into consideration the worst case. Generally PDA is based on a superposition technique with a single bit response (SBR), which requires the system to be linear time invariant (LTI) or can be well approximated as an LTI system. SBR is no longer applicable for systems which have different rising and falling edge responses due to asymmetric I/O design or mismatches between pull-up and pull-down drivers. Also sometimes the nonlinearity can extend beyond the edge transitions which can result from the voltage noise on the power distribution network (PDN). Herein PDA based on the superposition of multiple edge responses (MER) is proposed to account for a non-LTI system as well as asymmetric rising and falling edges.

ACKNOWLEDGMENTS

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1. INTRODUCTION TO AN EQUIVALENT CIRCUIT MODEL FOR PCB PDN BASED ON THE CAVITY MODEL AND PEEC

With the increasing device density and decreasing power supply voltage for modern ASICs and FPGAs, to satisfy the total current demand is becoming more and more challenging. IC current flowing from power to power return (often known as "ground") can be as high as hundreds of Amperes and thus can cause significant voltage ripple in the power supply, resulting in power integrity (PI) problems such as logic malfunction and timing jitter in signals [1]. So one of the main design objectives of a power distribution network is to reduce the voltage ripple below a specified allowable limit.

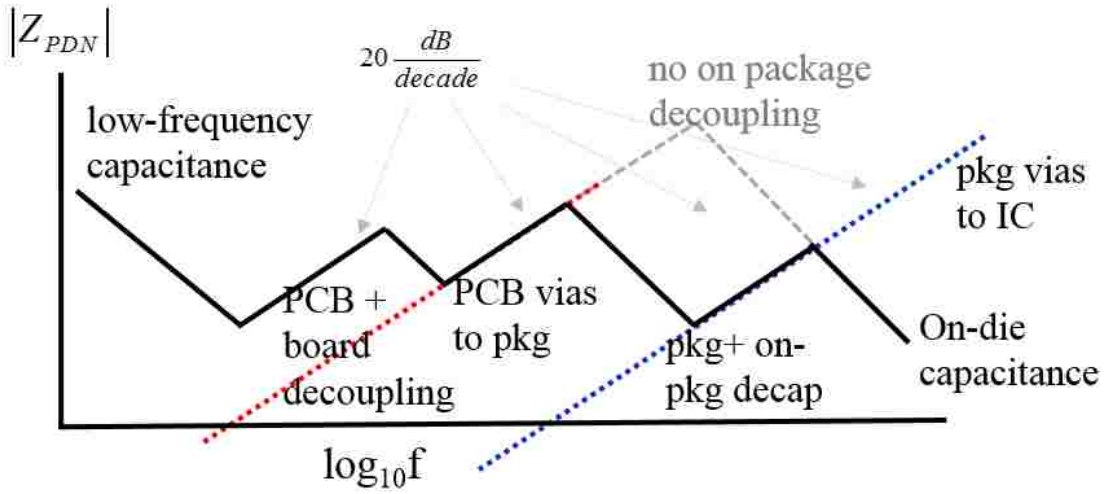


Figure 1.1. Typical input impedance of a cascaded PCB and package PDN.

The input impedance in frequency domain of a typical cascaded PCB PDN and matched package PDN is as depicted in Figure 1.1. Different kinds of decoupling capacitors are used to lower the PDN input impedance at different frequencies, resulting in many resonances and anti-resonances in the impedance curve. To determine the number or location of those decoupling capacitors, a very common and convenient guideline for PDN design is the target impedance in frequency domain [2]. It is defined as the input impedance

seen by the IC that results in the maximum tolerable voltage fluctuation for a specified current draw by the IC. There must be enough decoupling capacitors in a PDN to ensure an input impedance lower than the target impedance, which can then ensure a voltage noise ripple lower than the limit.

Although target impedance is a very straightforward and intuitive concept. However, this definition might be overly pessimistic and can result in overdesign. A relationship between the PDN geometry, the PDN input impedance and the actual voltage ripple would be more useful in the early design stages.

1.1. THE CAVITY MODEL

The cavity model was first proposed and used to solve the problem of finding the radiation patterns and impedance of a patch antenna [3]. In [3], the theoretical result is shown to compare favourably with the experimental result. Thus it can be validated to treat those narrow-banded patch antennas as cavities with appropriate boundary conditions. Later on the cavity model is applied to calculate both self and mutual inductances associated with PCB vias that are between a pair of parallel plates [4]. Since in most PCBs, its vertical size is usually much smaller than its horizontal size, the same method can be applied to treat two consecutive PCB layers as a two dimensional planar circuit [5]. A planar circuit is in the sense that the circuit elements are much smaller in size as compared with the wavelength in one direction, but comparable to the wavelength in the other two directions, that is, within that cavity, the derivative of the electromagnetic field with respect to the vertical coordinate can be assumed to be zero. So the 3-D Helmholtz equation for the PCB cavities comprised of two adjacent metal layers and a dielectric layer can be reduced to a 2-D Helmholtz equation and can thus be easily solved.

1.1.1. Wave Equation and Boundary Conditions for the Cavity Model. As shown in Figure 1.2, a typical cavity structure in a multi-layer PCB is formed by two adjacent rectangular layers. A via penetrating those two layers with electrical current

flowing through it can excite electromagnetic field inside that cavity. So it's pretty straightforward that the solution of the Maxwell's equations with an impressed electrical current source inside that cavity is what needs to be derived, as shown in Equation (1.1).

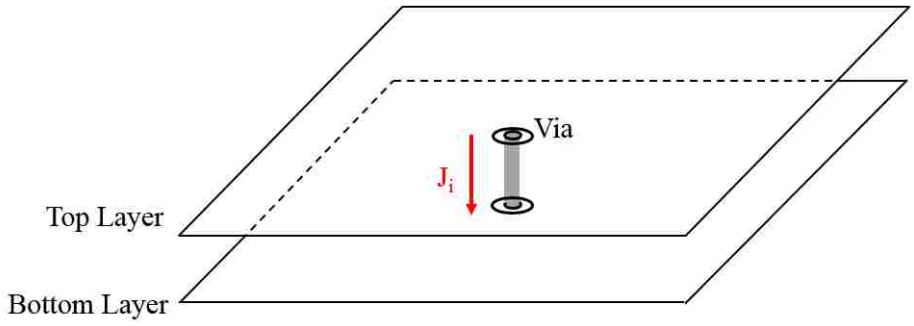


Figure 1.2. A Cavity formed by two adjacent PCB layers.

In Equation (1.1), J_i is the impressed electric current density and there is no other kind of source in this case such as impressed magnetic current or electric charge.

$$\begin{aligned} \nabla \times E &= -j\omega\mu H \\ \nabla \times H &= J_i + j\omega\varepsilon E \\ \nabla \cdot E &= 0 \\ \nabla \cdot H &= 0 \end{aligned} \tag{1.1}$$

Substitute the first equation of Equation (1.1) into the left side of the second equation in Equation (1.1) and use the vector identity as shown in Equation (1.2), we can derive the Helmholtz equation for the electric field as shown in Equation (1.3). Note that the divergence of the electric field is zero since there is no electric charge herein.

$$\nabla \times \nabla \times F = \nabla(\nabla \cdot F) - \nabla^2 F \tag{1.2}$$

$$\nabla^2 E + \omega^2 \mu\varepsilon E = j\omega\mu J_i \tag{1.3}$$

Equation (1.3) is a vector Helmholtz equation and can be reduced to a scalar Helmholtz equation by applying the top and bottom boundary condition and the planar circuit assumption. Figure 1.3 shows the impressed source current and the response electric field. Since the top and bottom layers are metal layers, PEC boundary condition can be applied. The electric field in the x and y direction can be assumed to be zero at the top and bottom surfaces. Also since the planar circuit assumption is satisfied herein, the variation of the electric field in the z direction is assumed to be zero, which means

$$\frac{\partial E_z}{\partial z} = 0$$

Thus only the electric field in the z direction can exist in the whole cavity. The 3-dimensional vector Helmholtz equation can therefore be reduced to a 2-dimensional scalar Helmholtz equation as in

$$\frac{\partial^2 E_z}{\partial x^2} + \frac{\partial^2 E_z}{\partial y^2} + \omega^2 \mu \varepsilon E_z = j\omega \mu J_i \tag{1.4}$$

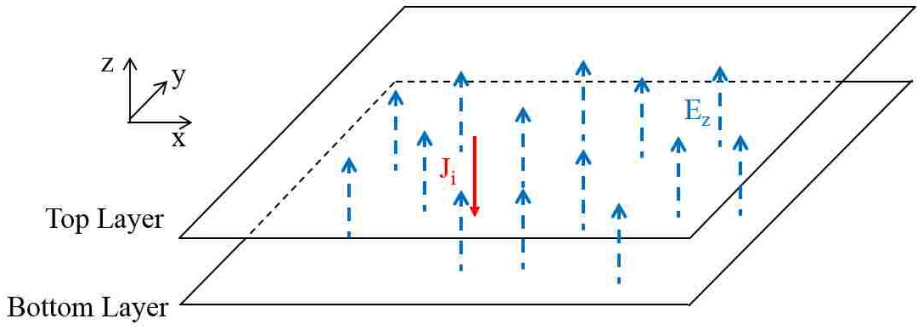


Figure 1.3. Source current and electric fields.

Since the magnetic field always wraps the conductors and the planar circuit assumption is satisfied, so the tangential part of the magnetic fields should be zero, that is, PMC boundary conditions should be applied to the cavity sidewalls. A more intuitive way to think

about this is that the surface current cannot flow outwards the cavity. Also the distortion at the corners can be neglected due to the planar circuit assumption. This is shown in Figure 1.4.

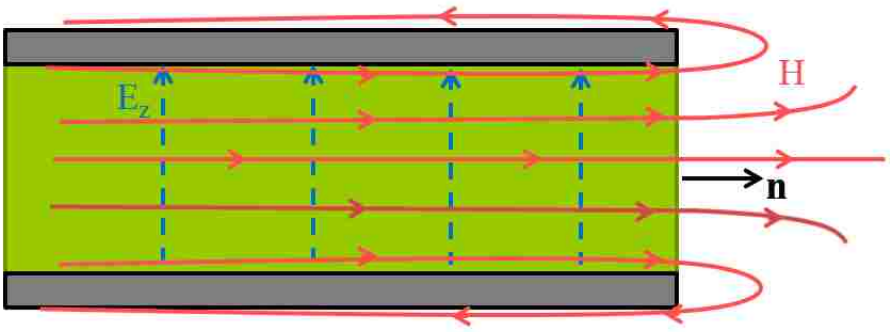


Figure 1.4. Field distribution at the cavity edges.

The electric field is related to the magnetic field by the first equation of Equation (1.1) as

$$\frac{\nabla \times E}{-j\omega\mu} = H$$

So the Neumann's (second-type) boundary condition is derived for the electric field as

$$\frac{\partial E_z}{\partial n} = 0, \quad (x = 0,\ x = a,\ y = 0,\ y = b) \tag{1.5}$$

Here $(x = 0, x = a, y = 0, y = b)$ is the boundary of the cavity.

1.1.2. Solution to the 2-D Scalar Helmholtz Equation and an Equivalent Circuit Model for the Cavity. Green's function is a common approach to solve the wave equation Equation (1.4), which has been reduced to a 2 dimensional Helmholtz equation with the boundary condition as in Equation (1.5). The problem to be solved is thus the 2 dimensional Helmholtz equation with a delta electric current source as in

$$\frac{\partial^2 G}{\partial x^2} + \frac{\partial^2 G}{\partial y^2} + \omega^2 \mu\varepsilon G = j\omega\mu\delta(x - \xi)(y - \eta) \tag{1.6}$$

Here (ξ, η) is the coordinate of the current source. The homogeneous form of Equation (1.6) is

$$\frac{\partial^2 G}{\partial x^2} + \frac{\partial^2 G}{\partial y^2} + \omega^2 \mu \varepsilon G = 0 \tag{1.7}$$

The eigenfunctions and eigenvalues of the homogeneous equation Equation (1.7) can be easily derived by separation of variables [6]. Since the second-type boundary conditions are applied for this case, so the eigenfunctions are in the form of $\cos\left(\frac{m\pi x}{a}\right)\cos\left(\frac{n\pi y}{b}\right)$ whose derivatives at the cavity edges are zero. After normalization, the eigenfunctions can be derived as

$$\begin{aligned}
&\psi_{mn}(x, y) = \frac{\sigma_m \sigma_n}{\sqrt{ab}} \cos\left(\frac{m\pi x}{a}\right)\cos\left(\frac{n\pi y}{b}\right), \quad m, n = 0, 1, 2\ldots \\
&\sigma_m = \begin{cases} 1; m = 0 \\ \sqrt{2}; m \neq 0 \end{cases} \\
&\sigma_n = \begin{cases} 1; n = 0 \\ \sqrt{2}; n \neq 0 \end{cases}
\end{aligned} \tag{1.8}$$

The corresponding eigenvalues are

$$\lambda_{mn} = \left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2 \tag{1.9}$$

By Sturm-Liouville operator theory [7], the Green's function can be expressed as a double summation of two-dimensional eigenfunctions as

$$G(x, y; \xi, \eta) = j\omega\mu \sum_m \sum_n \frac{\psi_{mn}(\xi, \eta)\psi_{mn}(x, y)}{\lambda - \lambda_{mn}} \tag{1.10}$$

Here $\lambda = \omega^2 \mu\varepsilon$ is the wave number, $\lambda_{mn} = \left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2$ is the eigenvalue of the eigenfunction ψ_{mn}. Assuming the PCB vias can be approximated as rectangulars and the current is uniformly distributed over the entire cross section, as shown in Figure 1.5 and

expressed in Equation (1.11). The electric field can thus be determined by the integration of the Green's function with the source current distribution as in Equation (1.12).

$$J(\xi, \eta) = \frac{I}{t_x t_y} \tag{1.11}$$

$$E_z(x, y) = \int_o^{t_x} \int_0^{t_y} G(x, y, \xi, \eta) J(\xi, \eta) d\xi d\eta \tag{1.12}$$

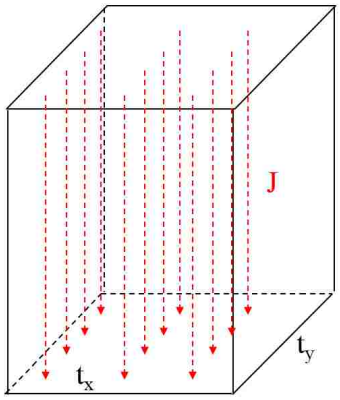


Figure 1.5. A port is set to the outer boundaries of the antipads.

To extract an equivalent circuit model for the PCB vias, a port is set to the outer boundaries of the antipads of that via, as shown in Figure 1.6. One terminal of that port is the outer boundary of the antipad on the top layer and the other terminal is the outer boundary of the antipad on the bottom layer. Since the electric field is assumed to be constant along the z direction, the voltage drop between the top layer and the bottom layer at any point can be obtained by simply multiplying the electric field with the thickness of the dielectric as in

$$V(x, y) = E_z(x, y) \times d \tag{1.13}$$

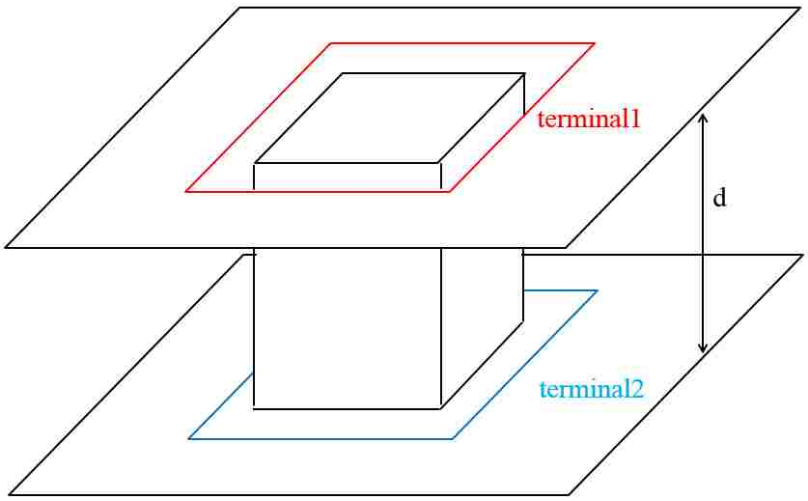


Figure 1.6. PCB via geometry and current distribution approximation.

The voltage difference between the two terminals of the via caused the impressed current source can then be derived by taking the average voltage over the cross section of the via as in

$$V = \frac{d \int_0^{t_x} \int_0^{t_y} E_z(x, y) dx dy}{t_x t_y} \tag{1.14}$$

The input impedance of that via port is thus calculated by

$$Z = \frac{V}{I} \tag{1.15}$$

Figure 1.7 shows the connection between the via and the cavity with or without the antipad, in which the via can be assumed as a short. When the via antipad is present, the via is connected to the port by the parasitic capacitance, which can be neglected in the frequency range of interest.

When multiple vias are present, the Z parameters of that cavity with all the via ports can then be calculated from Equation (1.10) to Equation (1.15) as in

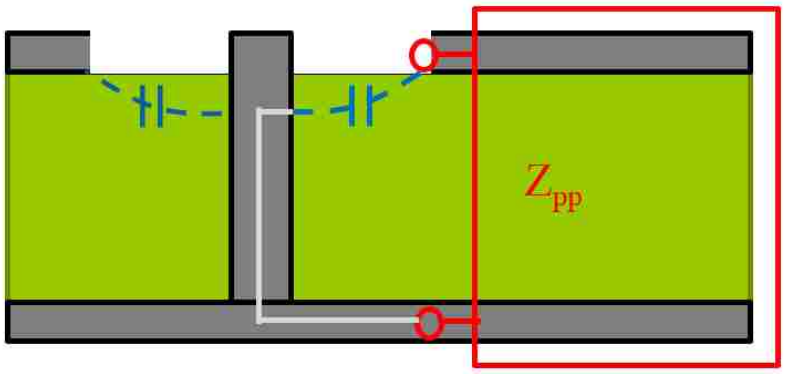


Figure 1.7. Via to cavity port connection.

$$
\begin{aligned}
&Z_{ij} = \tfrac{1}{j\omega C_P} + j\omega L_{ij}(\omega);\\
&where\\
&C_P = \tfrac{\varepsilon ab}{d},\\
&L_{ij}(\omega) = \tfrac{\mu d}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \tfrac{\sigma_m^2 \sigma_n^2}{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2 - \omega^2 \mu\varepsilon}\\
&\qquad \times \cos\left(\tfrac{m\pi x_i}{a}\right) \cos\left(\tfrac{m\pi t_{xi}}{2a}\right) \cos\left(\tfrac{n\pi y_i}{b}\right) \cos\left(\tfrac{n\pi t_{yi}}{2b}\right)\\
&\qquad \times \cos\left(\tfrac{m\pi x_j}{a}\right) \cos\left(\tfrac{m\pi t_{xj}}{2a}\right) \cos\left(\tfrac{n\pi y_j}{b}\right) \cos\left(\tfrac{n\pi t_{yj}}{2b}\right)
\end{aligned}
\tag{1.16}
$$

Note that Z_{ij} can be decomposed into a capacitor, which is the parallel plate capacitance between the top and bottom layers, and a frequency dependent inductor [8]. To get the lumped circuit model, the frequency dependent term is neglected, that is, only the DC inductance is used and the distribution behaviour can not be captured by using this lumped circuit model. However, it has been found that The frequency dependent inductance is nearly constant at the frequencies below approximately 60% of the first cavity resonance frequency, which is usually higher than the frequency range of interest for PDN analysis, and therefore it can be approximated to the DC value, when $\omega = 0$ [4]. Thus a circuit model for the cavity with multiple vias can be extracted as shown in Figure 1.8.

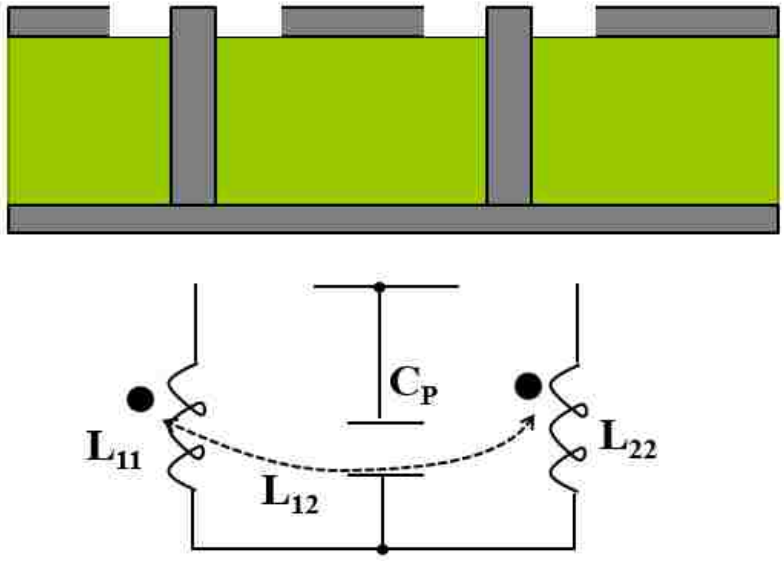


Figure 1.8. Equivalent circuit model for the a cavity with two vias connected to the bottom layer.

1.1.3. Limitations of the Circuit Model. The first limitation of the circuit model is that the computation time for the inductance is long when there are a lot of vias. Although the infinite summation can be truncated in practice as soon as target convergence is achieved, the mode number still needs to be more than $m = n = 800$ to reach the target convergence within 5% for the test structure in paper [8]. A faster way to calculate this double-sided summation is to replace it with the single-sided summation [9]. With the single-sided inductance formula, the computation time for the inductance matrix associated with several hundreds of vias can be reduced to less than 1 hour with acceptable accuracy.

Another approach is discussed herein to try to derive the closed-form expressions for the inductance calculations. For 1D Helmholtz equation, the closed-form expression can be easily derived [9] because the singularity at the source location can be written as just the derivative of a step function. However, it's not the case for a 2D Helmholtz equation and only the series form is found in literature. However, as has been mentioned earlier, only the DC inductance is needed for common PI analysis and the 2D Helmholtz equation can be reduced to a 2D Poisson equation when $\omega = 0$. A closed-form solution to the 2D

Poisson equation in a rectangular area with the first-type boundary condition has already been derived in [10]. A similar approach is taken herein to find the closed-form solution to the 2D Poisson equation in a rectangular area with the second-type boundary condition. The approach is to apply conformal Schwarz-Christoffel transformation and image theory to convert the boundary of a rectangular to infinity. Since the closed-form solution to the free space Green's function for a 2D Poisson equation has already been derived [9], the closed-form solution to the Poisson equation with a rectangular boundary can then be extracted.

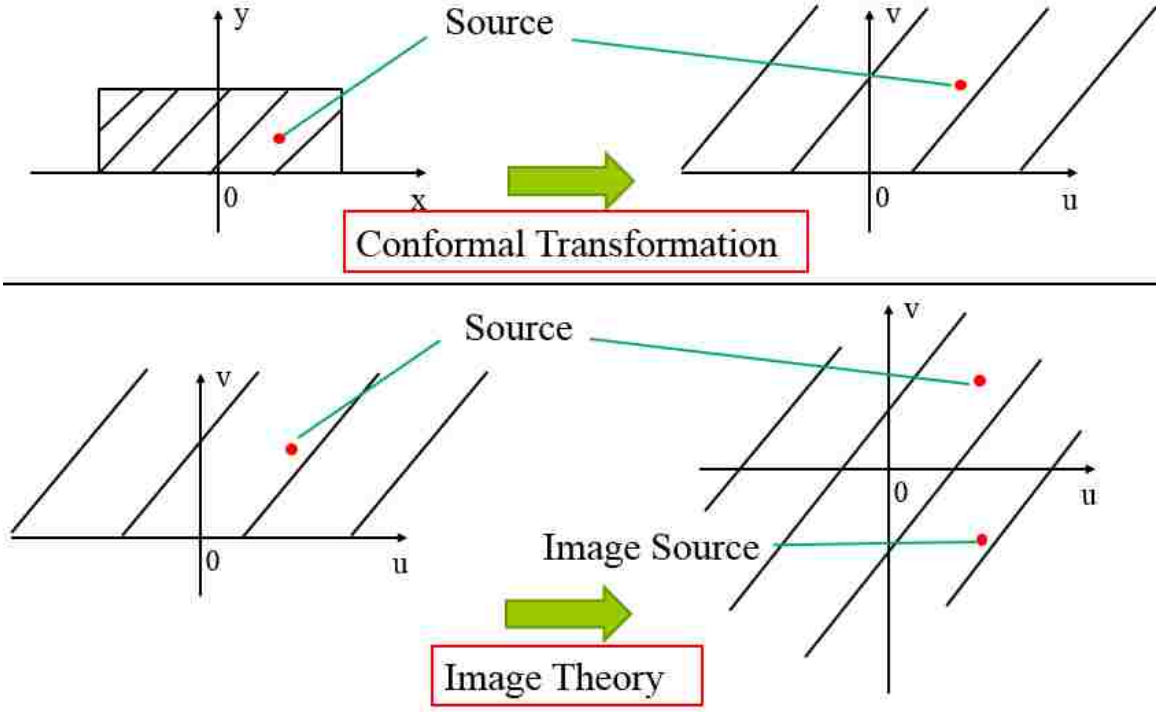


Figure 1.9. Conformal transformation and image theory are applied.

As shown in Figure 1.9,by using conformal Schwarz-Christoffel transformation, the rectangular boundary can be converted to the whole u axis in the z plane. For the first-type boundary condition, the image source has opposite polarity as the original source, which can result in a zero value at infinity. However, for the second-type boundary condition, the Green's function goes to infinity since the image source has the same polarity as the

original source. So, although the computation time can be significantly reduced (in the example shown in Figure 1.10 and Figure 1.11, the computation time can be reduced from 7s to 3ms), this approach doesn't apply to the second-type boundary condition.

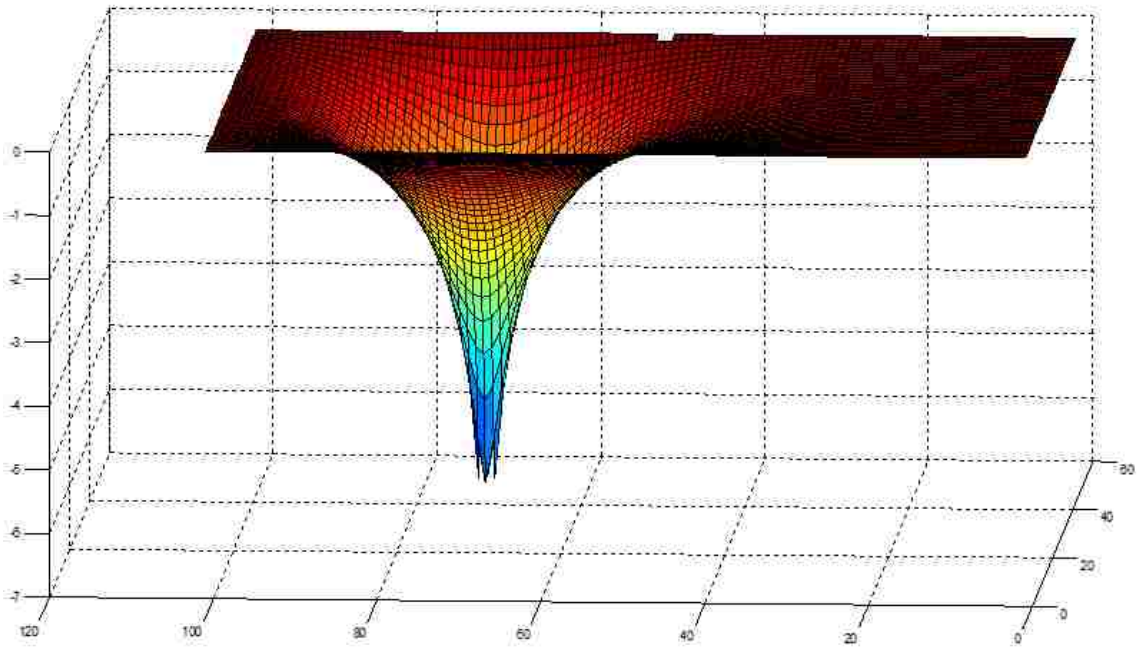


Figure 1.10. Green's function of a 2D Poisson equation in a rectangular area with first-type boundary condition.

The second limitation of the lumped circuit model is that it cannot capture the distributed behaviour since the frequency dependent term has been removed in Equation (1.16) to construct the lumped circuit model. As has been mentioned earlier, this approximation is appropriate for most PDN designs since the frequency range of interest is usually low.

The third limitation of the circuit model is that the Green's functions is derived by using impressed current source, which means the boundary conditions at the edges of the vias are not taken into consideration. Since multiple scattering can happen at the via boundary and can have a significant influence on the inductance value when the via diameter to pitch ratio is large [11], so the circuit model is no longer suitable for closely-spaced vias. However, the circuit model can be improved by applying a more practical current distribution which can account for the proximity effect. The current distribution

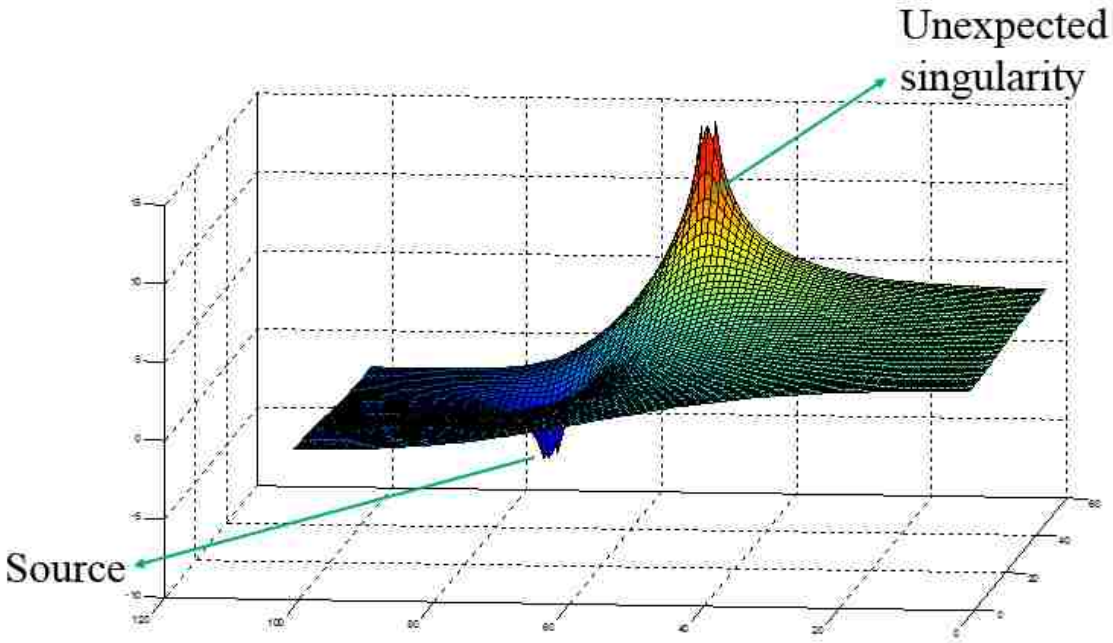


Figure 1.11. Green's function of a 2D Poisson equation in a rectangular area with second-type boundary condition.

accounting for the proximity effect for multi-turn loop antennas has been derived in [12]. For most PCB PDNs, the circuit model is acceptable since usually the via diameter to pitch ratio in PCBs are not so large. A comparison between the cavity model and full-wave simulations is shown in Figure 1.12.

1.2. PEEC METHOD

There are many other structures in PCBs that the cavity model cannot handle, such as some power net area fills which has many cutouts and voids, or the SMT decoupling capacitors and soldering pads. PEEC method is thus applied to extract the equivalent circuit model for those geometries.

Unit: pH, d = 10mils

drill	Anti-pad	pitch	Lcst	Lcavity	Error
7.8mil	20mil	1mm	231.61	244.61	5.61%
		0.8mm	209.36	221.92	6.00%
		0.6mm	181.55	192.67	6.12%
drill	Anti-pad	pitch	Lcst	Lcavity	Error
20mil	30mil	1.2mm	157.56	169.14	7.35%
		1mm	139.44	150.61	8.00%
		0.8mm	117.39	127.99	9.03%
drill	Anti-pad	pitch	Lcst	Lcavity	Error
40mil	50mil	2mm	139.44	150.9	8.21%
		1.6mm	117.20	128.21	9.40%
		1.4mm	104.48	114.69	9.76%

Figure 1.12. Comparison between the cavity model and full-wave simulations.

For the decoupling capacitors of the PDN, the equivalent circuit model can be extracted by using PMSR [13], [14], which can take into consideration all the ESL, the soldering pad and the trace. Figure 1.13 shows how the equivalent total inductance is derived for a pair of decoupling capacitors[1].

For power net area fills with irregular shapes, a specific PEEC method is proposed called parallel plate PEEC (PPP) [15]. Basically PPP and the cavity model deals with the same PCB structure. The difference is that PPP can deal with all kinds of cutouts and voids

[1]In this thesis, all the results and circuit models for the decoupling capacitors are provided by Ying, Xiang and Tamar, students at MST EMC laboratory.

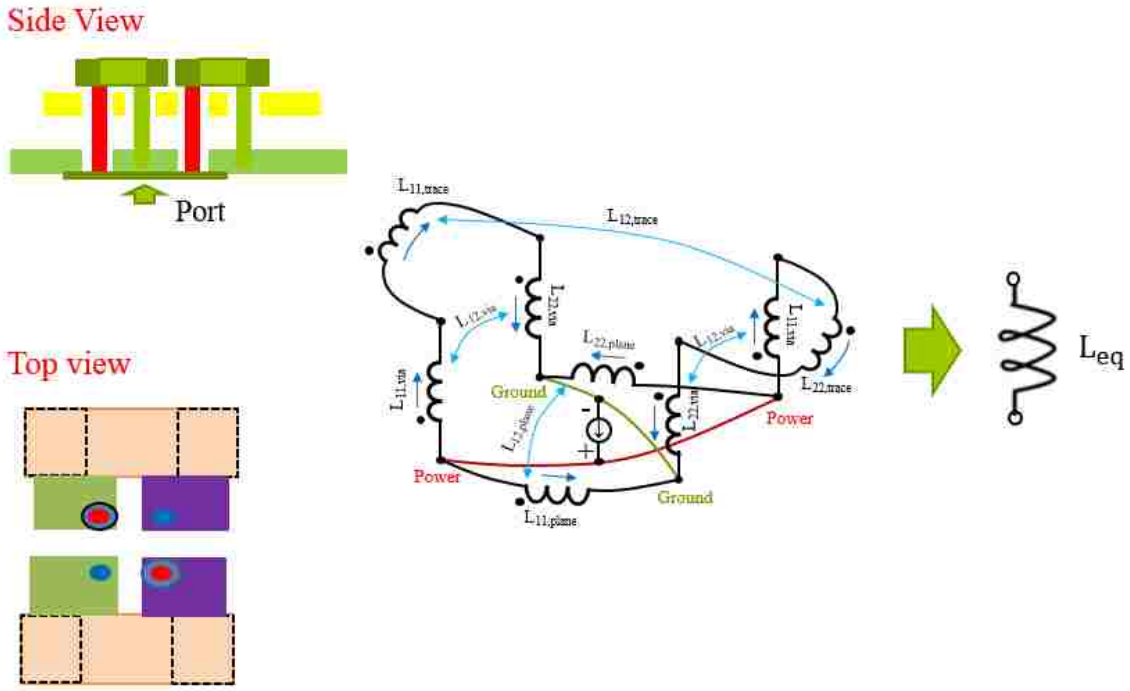


Figure 1.13. PEEC method is applied to the decoupling capacitor modeling.

on the metal layer while the cavity model cannnot handle them. An example is shown in Figure 1.14, in which the input impedance is compared for the PPP calculations and full-wave simulations[2].

1.3. MERGE POWER CAVITIES AND GROUND CAVITIES

Basically there are two types of cavities in a common PCB PDN design. One is called ground cavity and comprises two full rectangular ground layers and the other is power cavity comprising one ground layer and one power layer. Usually the power layer has many cutouts and voids, so it's not a full plate and often called a power net area fill instead. As has been discussed earlier, the ground cavity can be handled easily with the cavity model while the power cavity has to be dealt with PPP because the boundary conditions that are applied to the cavity model are not appropriate any more for power net area fills with many

[2]In this thesis, all the data and circuit models from PPP are provided by Siqi, a PhD student at MST EMC laboratory.

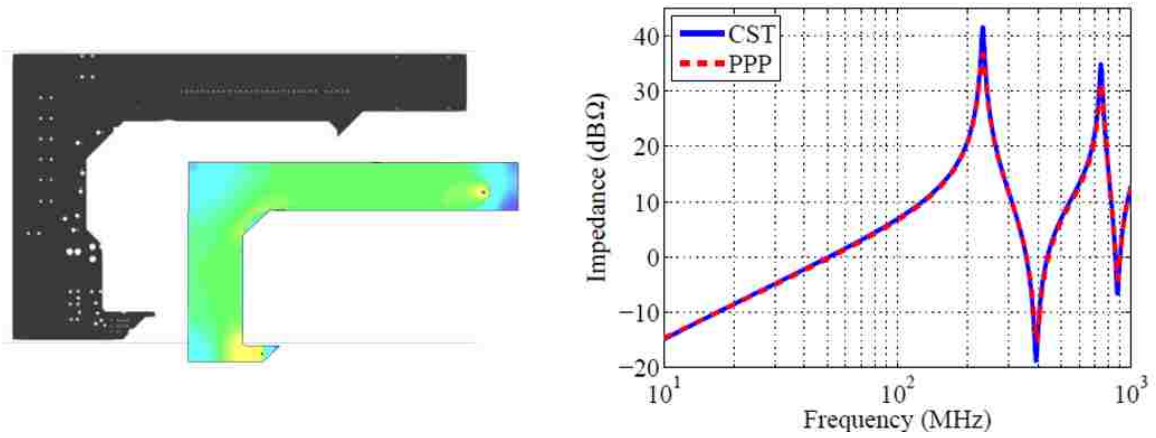


Figure 1.14. PPP is applied to irregular power net area fills modeling.

cutouts and voids. Since two methodologies are applied herein, the question then arises as to how to connect power cavities and ground cavities. Two ways are shown in this section: one is by just adding the inductance together and the other is by internal ports. The results are shown to compare favourably with experiments or full-wave simulations.

1.3.1. Connecting Power Cavities and Ground Cavities in an Inductance Fashion. Generally a PDN design is more concerned with the total inductance associated with the current path from decoupling capacitors to ICs because the PDN impedance is closely related to the total inductance at higher frequencies. So sometimes at early PDN design stages, it's more useful to provide a fast total inductance estimation than to analyze the total input impedance over the required frequency range.

The total inductance can be divided into different pieces by tracing the current path. As shown in Figure 1.15, there are 4 pieces of inductance: $L_{PCB\_IC\_Via}$ is the inductance associated with the PCB IC vias, L_{PCB_plane} is the inductance associated with the PCB power net area fills, $L_{PCB\_IC\_Decap\_Via}$ is the inductance associated with the PCB decoupling capacitor vias and $L_{PCB\_Decap\_above}$ is the inductance associated with the PCB decoupling capacitor mounting and ESL. As has been discussed earlier, they can be calculated with different modeling methods. $L_{PCB\_IC\_Via}$ and $L_{PCB\_IC\_Decap\_Via}$ are related to the ground cavity and can be calculated with the cavity model. L_{PCB_plane} is related to

the horizontal current flowing across the power net area fill and can thus be calculated by using PPP. And $L_{PCB\_Decap\_above}$ is about the decoupling capacitors and can be calculated with PEEC. Usually the capacitor vendors also provide a circuit model and ESL value for their capacitors, which are often obtained by experiments.

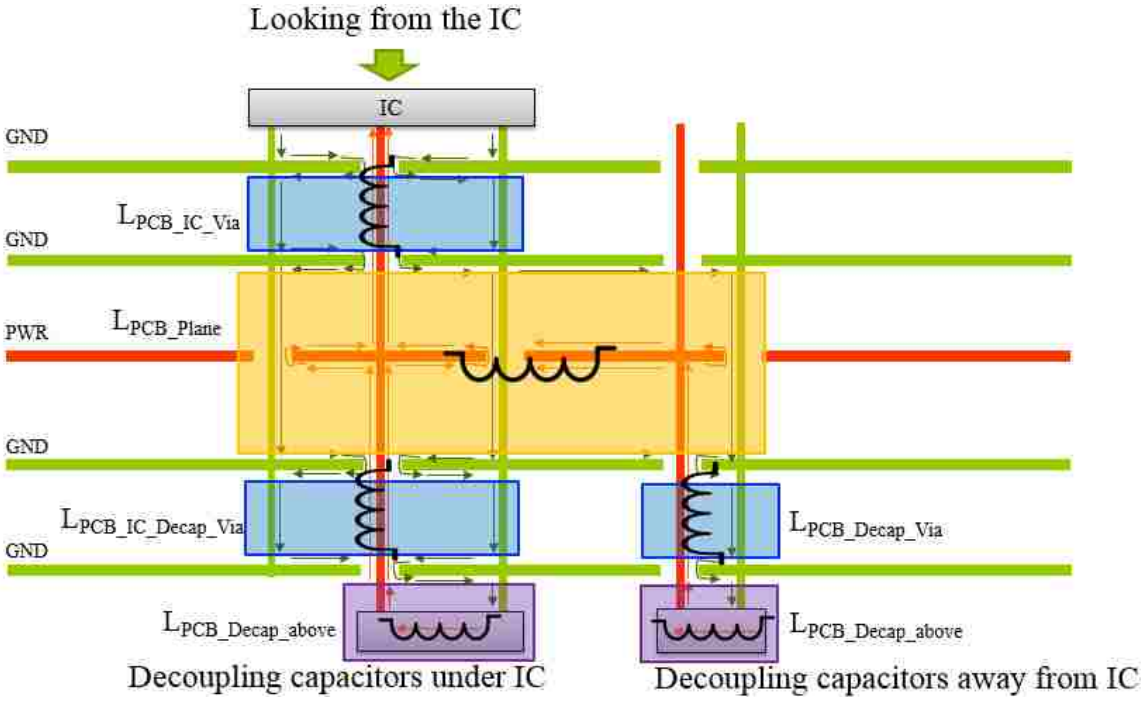
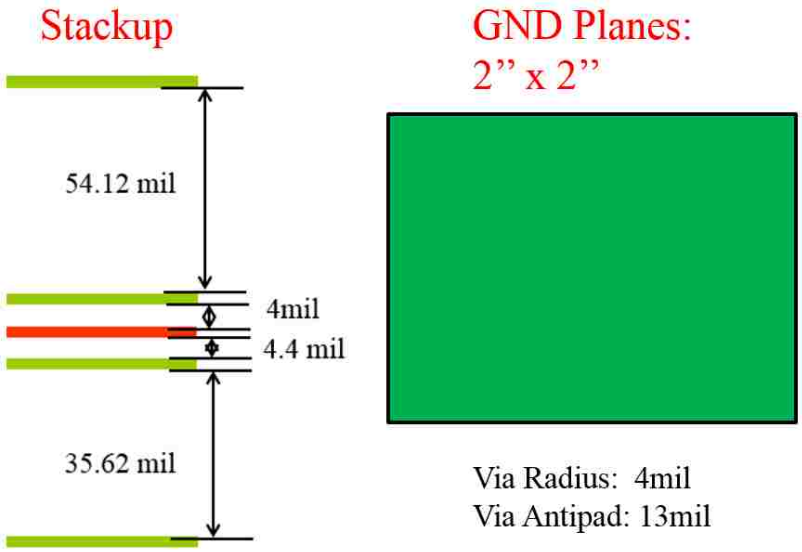
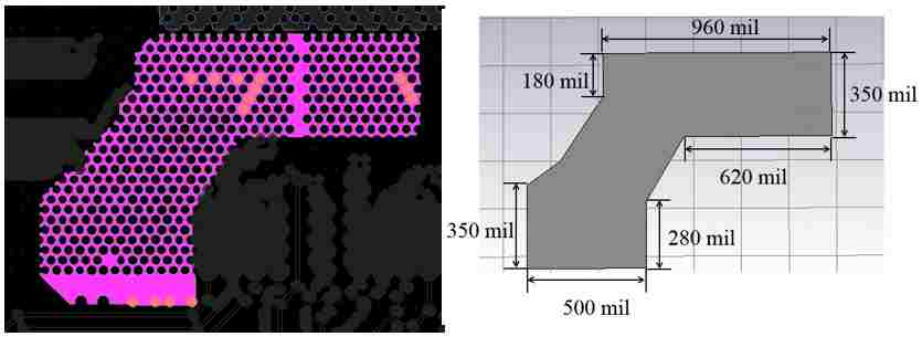


Figure 1.15. Total inductance can be divided by tracing the current path.

A test vehicle is used herein to validate this methodology. Figure 1.16 shows the geometries of the test vehicle. Decoupling capacitors are placed at the left bottom side under the PCB. The inductance associated with both the IC vias and the decoupling capacitor vias are first calculated using the cavity model. As for the power cavities, since the current flow in the upper power cavity and the current flow in the lower cavity are parallel, as shown in Figure 1.17, the total inductance related to power cavities is then the parallel inductance of the upper power cavity inductance and the lower power cavity inductance, which can be calculated using PPP. To make it simpler, the value 500pH used herein for $L_{PCB\_Decap\_above}$ is just a typical ESL value associated with common decoupling capacitors, which is obtained



(a) Stackup and ground layers.

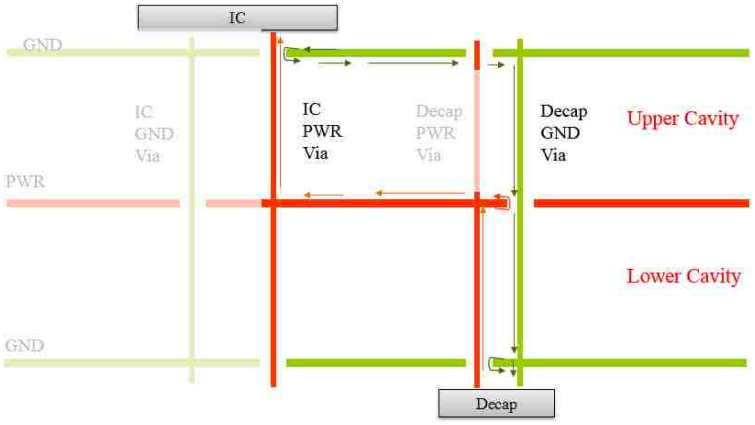


(b) Power net area fill.

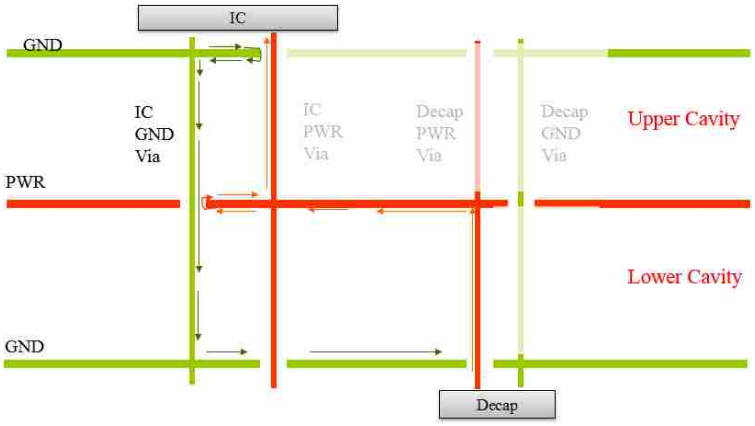
Figure 1.16. Geometries of the test vehicle.

from muRata. The total inductance associated with the current path from the decoupling capacitors under the PCB all the way to the IC is then calculated by adding up $L_{PCB\_IC\_Via}$, L_{PCB_plane}, $L_{PCB\_IC\_Decap\_Via}$ and $L_{PCB\_Decap\_above}$.

Four different cases are taken into consideration herein with different number of decoupling capacitor pairs, as show in Table 1.1. $L_{PCB\_IC\_Via}$, L_{PCB_plane} and $L_{PCB\_IC\_Decap\_Via}$ are first calculated for the one pair case. As the number of decoupling capacitor pair increases, only the current associated with the decoupling capacitor will change. Since decoupling capacitors are parallel with each other and the mutual inductance can be neglected between each decoupling capacitor pair, so for the rest three cases, $L_{PCB\_IC\_Via}$



(a) Current flow in the upper power cavity.



(b) Current flow in the lower power cavity.

Figure 1.17. Current flow in the upper and lower power cavities.

and L_{PCB_plane} are assumed to be same as the one pair case while $L_{PCB\_IC\_Decap\_Via}$ and $L_{PCB\_Decap\_above}$ are approximated as proportional to $1/n$, where n is the number of decoupling capacitor pairs.

The total inductance values for all the four cases are also simulated by using CST Microwave Studio. Table 1.1 shows the comparison between calculations using the cavity model and PPP and simulations using CST. It can be seen from Table 1.1 that the calculations agree well with simulations with less than 10% difference.

1.3.2. Connecting Power Cavities and Ground Cavities in a Network Fashion. While the total inductance of a PDN gives some idea about the quality of that PDN, a more rigorous and common way to analyze the performance of a PDN is to compare its input

impedance with the target impedance [2]. Since an alternating current has the tendency to flow only on the surface of a PEC conductor due to skin effect, so two adjacent cavities are actually separated by metal layers and connected through voids and cutouts. Based on this concept, herein two adjacent cavities are connected through internal ports which are set over via antipads as shown in Figure 1.18.

Table 1.1. Inductance values from both calculations and simulations.

Regular:	**# of Decap Pairs**			
pH	1	2	3	4
LPCB_IC_Via	460	460	460	460
LPlane	267	267	267	267
LPCB_Decap_Via	734	367	244	183
LPCB_Decap_above	595	297	198	149
Ltotal_calculated	2056	1391	1169	1059
Ltotal_CST	1965	1266	1116	975

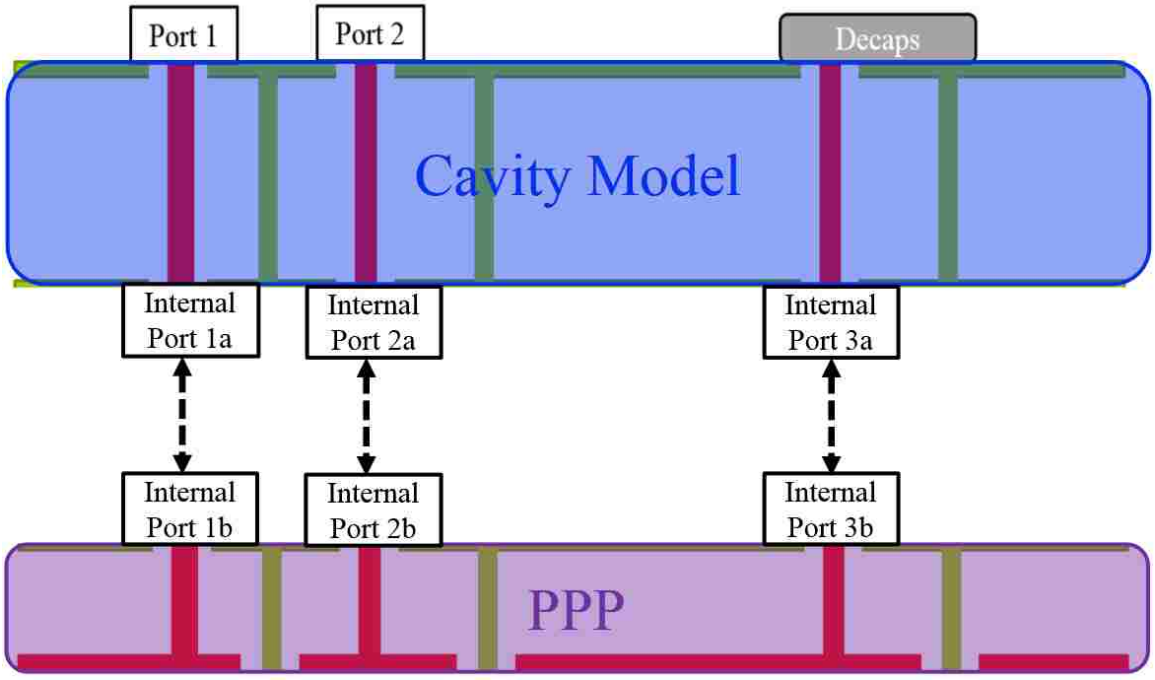


Figure 1.18. Ground cavities and power cavities are connected through internal ports.

Figure 1.18 shows the connection between a ground cavity modelled with the cavity model and a power cavity modelled with PPP that are immediately below that ground cavity. It can be seen that for a ground cavity, internal ports should be set at power vias on both the top and bottom planes. And for a power cavity, internals ports should be set at power vias on one plane and ground vias on the other. Then network parameters of the ground cavity can be extracted from the cavity model with Equation (1.16). And network parameters of the power cavity can be extracted from PPP with the circuit models mentioned in [15]. With those network parameters of different cavities, the input impedance of a PCB PDN can thus be extracted by cascading all the network parameters through their common internal ports. External components such as decoupling capacitors and chip packages can also be connected through external ports as shown in Figure 1.18.

1.3.3. Measurement Validation. A test vehicle is designed and the input impedance of that test vehicle is measured to validate the hybrid method of modeling multi-layer PCB PDNs by connecting different cavities through internal via ports. The stackup of the test vehicle is shown in Figure 1.19. As can be seen from Figure 1.19, the test vehicle comprises 6 metal layers and 5 cavities in total. 1 oz copper is used for metal layers and the power layer is colored in red and is the fourth layer from top to bottom.

The size of the ground planes is 4 inch by 7 inch, as shown in Figure 1.20. Power net area fill is colored in red, which looks like a letter P. Two types of decoupling capacitors are used in the test vehicle: 10 capacitors with 2.2uF capacitance and 4 capacitor with 10uF capacitance. There are in total 4 different port locations for the input impedance measurement and in this paper only Port 2 is used. There is a void grid at Port 3, which is used to represent the dense antipads under IC regions. The size of the void grid is shown in Figure 1.21. Also for the plated-through hole vias used in this test vehicle, the finished hole size is 15mils and their antipad diameter is 42mils.

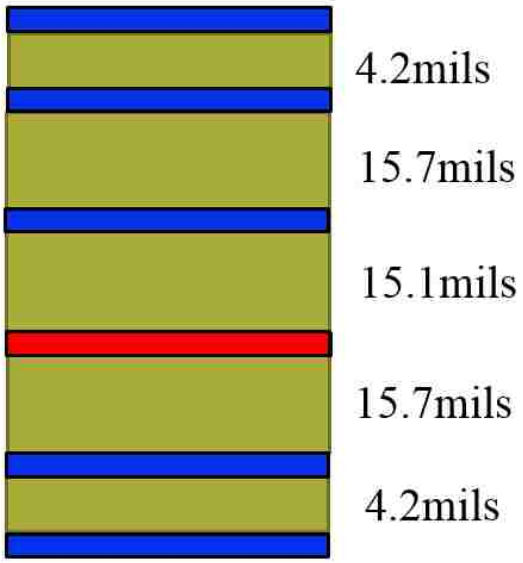


Figure 1.19. Test vehicle stackup.

The PDN port pad pattern looks like that of a surface mounted SMA connector, as shown in Figure 1.22. There are four ground vias connected to a circular ground pin and one power via connected to the power pin. The input impedance of the PCB PDN is then the impedance by looking into the test vehicle from those power and ground pins.

To measure the input impedance of the test PCB PDN, a two-port transfer impedance measurement approach is employed herein [**?**]. Since PDN usually has a very low input impedance, $S_{11} \approx 1$. Thus conventional one-port impedance measurement using S_{11} requires well-characterized and precise test fixtures for locating reference plane and accurate phase information, which is difficult or expensive to achieve, as is the case in [16], where a precise wafer probe is used to perform input impedance measurement for a production-level PCB PDN.

The port settings to perform a two port measurement herein is as shown in Figure 1.23. Two coaxial cables are connected to the VNA two ports and at the other end of the two cables, the cable jacket is removed so that the signal and ground of the cable can be soldered to the power and ground pins of the test vehicle respectively. In this way,

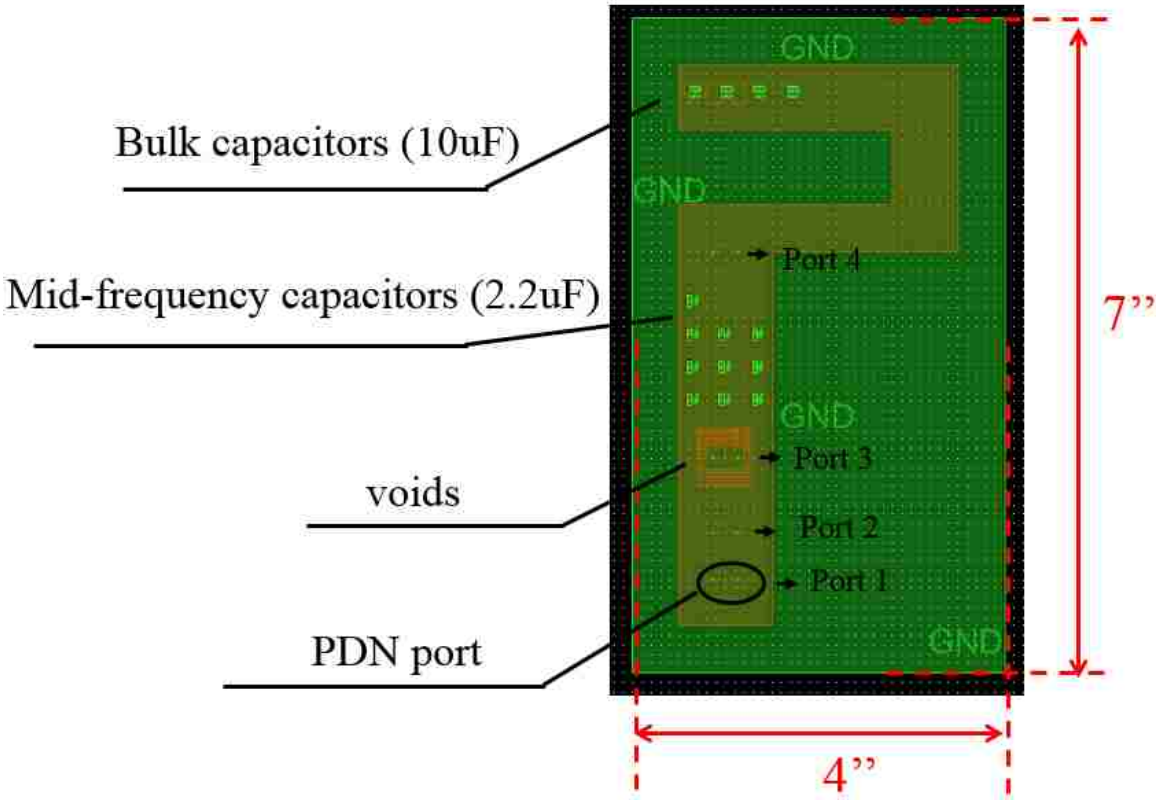
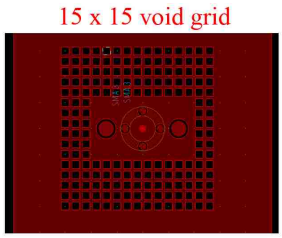


Figure 1.20. Test vehicle top view.

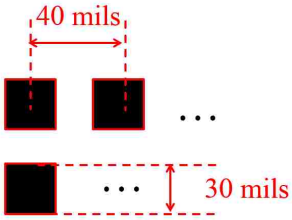
the measurement is set up with the two ports as marked in Figure 1.23. Since both the power nodes and ground nodes of the two ports are connected to the same power pin and ground pin of the test vehicle respectively, so the transfer impedance Z_{12} or Z_{21} between the two ports is thus equal to the input impedance of the test PCB PDN. When the PDN input impedance is low, Z_{12} can be related to S_{12} simply by [**?**]

$$|Z_{12}| \approx \frac{|S_{12}|}{2} Z_0. \tag{1.17}$$

With this simple relationship between Z_{12} and S_{12}. It's much easier to perform a two port measurement than a one port measurement. Even port extension is not needed if the two cables are not too long.



(a) Void grid.



(b) Void size.

Figure 1.21. Void region at Port 3.

The measurement setup with all the decoupling capacitors soldered is shown in Figure 1.23 and Figure 1.24. Four 10uF 0805 decoupling capacitors are soldered at the top and ten 2.2uF 0805 decoupling capacitors are soldered in the middle. There are one power via and one ground via associated with each decoupling capacitor and one power via and four ground vias associated with each PDN port. So in total 48 internal ports are needed to connect the power cavities and ground cavities. Herein Port 2 is used to perform the two port PDN input impedance measurement. Besides the measurement, simulations to get the input impedance looking into Port 2 are also done with Cadence Sigrity tools.

The input impedance results looking into Port 2 from measurements, simulations and calculations based on the hybrid method mentioned in Section 1.3.2 are compared in Figure 1.25. The results from calculations based on PPP and the cavity model are shown to compare favourably with the results from measurements and simulations. The total inductance results are also compared in Table 1.2. It can be seen that the hybrid approach based on PPP and the cavity model can capture the total inductance of the test PCB PDN accurately with only around 3% difference from measurements and around 7.5% difference

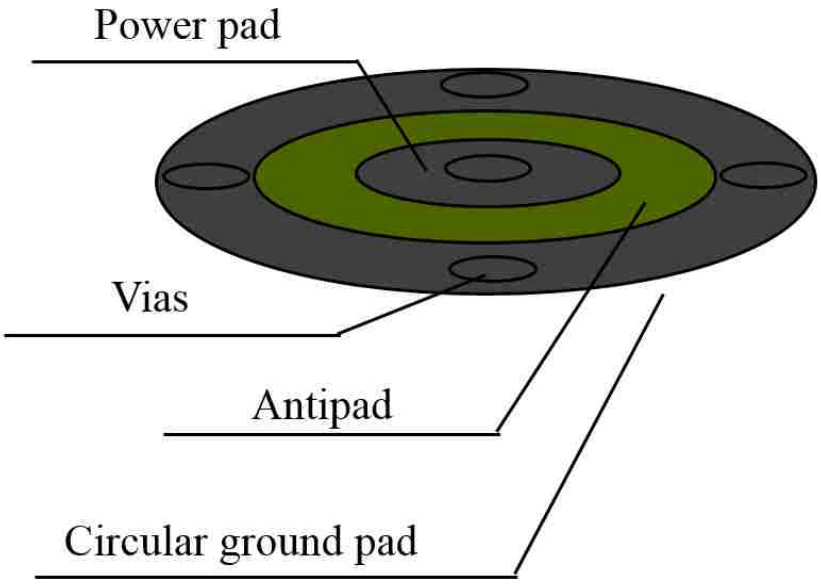


Figure 1.22. Test vehicle port pad pattern for input impedance measurement.

from simulations. Herein 48 vias are used in the test vehicle which are related to 48 internal ports for the connections between different cavities. More complicated PCB PDNs can be modelled using the same hybrid approach based on PPP and the cavity model by modifying the PPP circuit and increase internal ports.

Figure 1.25 also shows that by merging different cavities in a network fashion, other external components such as decoupling capacitors can also be taken into consideration. As can be seen from Figure 1.20, two types of decoupling capacitors with two different capacitance values are used in the test vehicle and the capacitors with larger capacitance are located further away from Port 2 than capacitors with less capacitance. This means the parasitic inductance associated with the current flowing from Port 2 to the 10uF capacitors is larger than that of the 2.2uF capacitors. Thus at lower frequency, current would flow through those 10uF capacitors and before those 2.2uF capacitors come into effect, there will be a resonance between the larger parasitic inductance related to the 10uF capacitors and the capacitance of those 2.2uF capacitors. This resonance can be observed from Figure 1.25 which happens around 1MHz. It is shown in Figure 1.25 that although there is an obvious

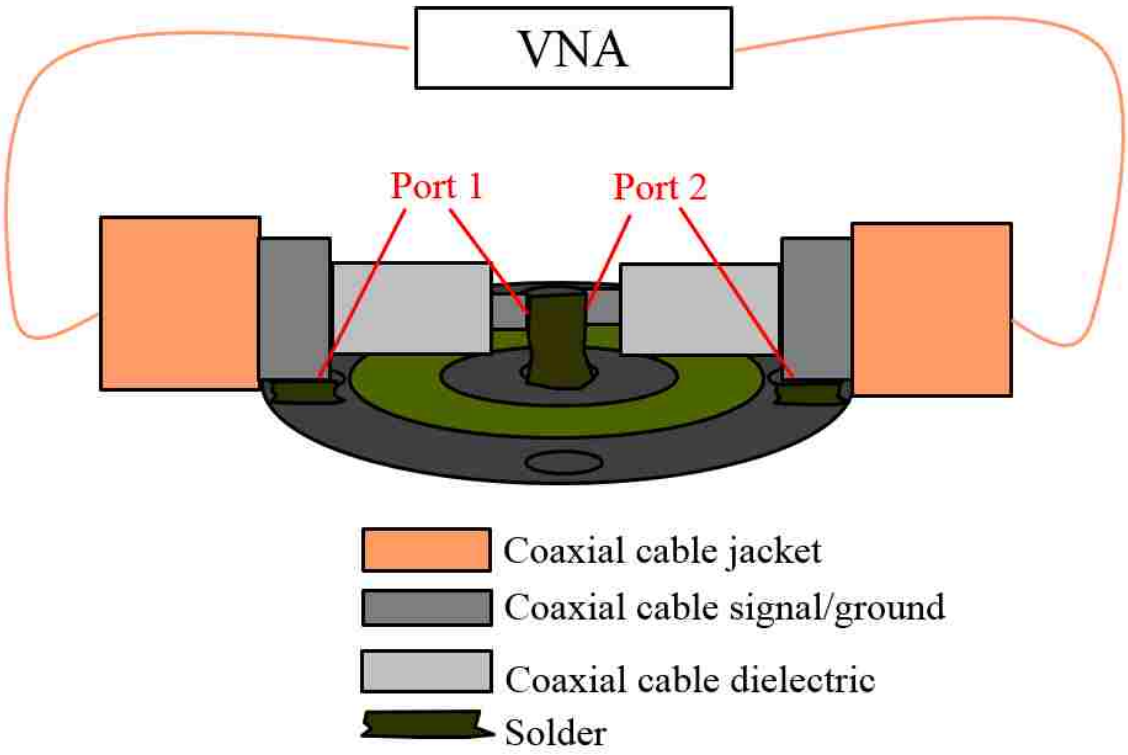


Figure 1.23. Two port measurement settings.

difference of the Q factor between the calculations and measurements, the hybrid approach with merging different cavities in a network fashion can capture the resonance frequencies between different types of decoupling capacitors very well. Moreover, the difference of the Q factor is mainly due to the absence of some loss terms in the PPP method and the cavity model and the hybrid approach can be further improved by including those loss terms.

Another mismatch between the calculations and the measurements which can be seen from Figure 1.25 is the resonance happens at around 500M. This resonance is due to the parallel-plate parasitic capacitance of the power net area fills and the ground planes. After that resonance, current would mostly go as displacement current from the power net area fills to the nearby ground planes instead of travelling all the way to decoupling capacitors which have larger parasitic inductance. Figure 1.25 shows the resonance frequency calculated from PPP and the cavity model is higher than that from measurements or simulations,

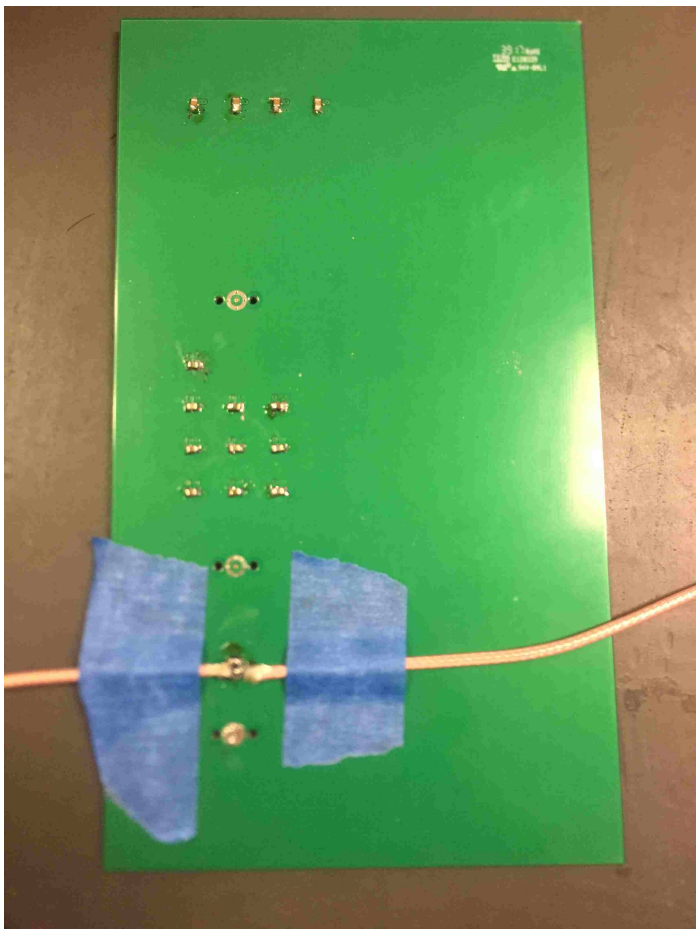


Figure 1.24. Measurement setup.

which means the parasitic parallel-plate capacitance from the hybrid approach is smaller since they have almost the same total inductance. This could be due to the absence of the fringing capacitance in PPP and the cavity model.

However for most PCB PDN designs, this resonance is of little concern because usually chip packages will provide extra decoupling capacitance which is larger than the parasitic parallel-plate capacitance. So that resonance generally cannot be observed in a system-level PDN input impedance curve with chip packages included.

1.3.4. Conclusion. The paper shows a hybrid multi-layer PCB PDN modeling approach with good accuracy based on PPP and the cavity model. This method is based on model extraction for a single cavity comprised of two adjacent metal layers and a

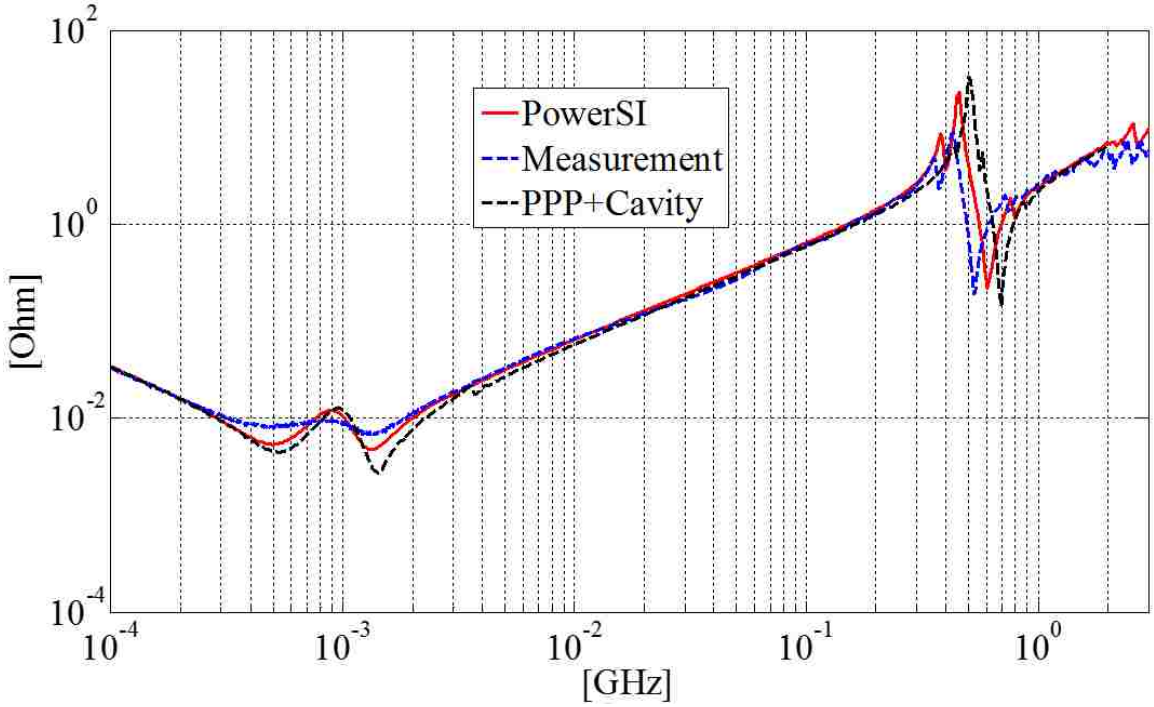


Figure 1.25. Input impedance results comparison between calculations, simulations and measurements.

Table 1.2. Total inductance comparison of test PCB PDN at Port 2 between calculations, measurements and simulations.

Total inductances (pH) @ 100 MHz		
Simulations	measurements	Cavity model + PPP calculations
1017	972	941

merging method of different cavities using internal ports set across via antipads. Both fast total inductance calculations and input impedance extractions can be performed with this approach for multi-layer PCB PDNs. The total inductance calculation was first verified by comparing with simulations for a PCB PDN model based on a practical PDN design. Later on the input impedance extraction was also verified by comparing the response from the hybrid method with that from simulations using Cadence Sigrity tool and a two-port measurement. The results from simulations and measurements are shown to agree well

with the results from the hybrid method. Despite the absence of the fringing capacitance, this hybrid approach can still give an accurate model for multi-layer PCB PDNs to run system-level PDN analyses.

2. POWER INTEGRITY WITH VOLTAGE RIPPLE SPECTRUM DECOMPOSITION FOR PCB AND PACKAGE PDNS

As has been mentioned earlier, although target impedance is a very straightforward and intuitive concept, this definition might be overly pessimistic and result in overdesign. A relationship between the PDN geometry, the PDN input impedance and the actual voltage ripple would be more useful in the early design stages.

Previous work has focused on PCB PDNs [17]. For a typical PCB PDN, its input impedance can be calculated by using an equivalent circuit model extracted from cavity model. With the information of switching current, the voltage ripple can then be obtained either by using a frequency segmentation method [17]. By decomposing the voltage ripple of a typical PCB PDN into a high frequency component and a low frequency component, relationships between the PCB PDN geometry and its voltage noise ripple can thus be derived. The high frequency component is mainly due to vias connecting the IC to the power plane, while the low frequency component is closely related to vias connecting decoupling capacitors. Thus increasing the number of decoupling capacitors can only help to reduce the low frequency voltage component while the high frequency component remains approximately the same. This low frequency component can be reduced to nearly zero if there are enough decoupling capacitors. On the other hand, adding more IC vias can only reduce the high frequency voltage ripple component and won't change the low frequency component.

In this chapter, a switching current synthesizer based on chip-level simulations is discussed first in Section 2.1. It can generate a switching current profile based on a given joint probability distribution function of the parameters. Both the high frequency component at GHz and the lower frequency component from power gating or clock gating are included in this synthesizer. Later on an equivalent circuit model is introduced in Section 2.2 and the one-on-one correspondence between the circuit elements and the PDN geometry pieces are

illustrated. Next the voltage ripple spectrum decomposition approach proposed in [17] is extended for cascaded PCB and package PDNs in Section 2.3. The one-on-one relationships between the voltage aspects, the PDN geometry and the PDN input impedance in frequency domain are also discussed in Section 2.3. Last section shows how this extended approach is applied to a real design. Relationship between different voltage aspects and the number of on-PCB decoupling capacitors are discussed in Section 2.4 .

2.1. A SWITCHING CURRENT SYNTHESIZER

IC switching current profiles are essential to perform a time domain system-level analysis of the whole PDN. The current signature can dramatically influence the voltage ripple since the voltage ripple is just the product of the switching current and the input impedance of PDN in frequency domain. IC switching current may not be unique and is dependent on the functions and operation modes of the silicon. So the current profile should be able to mimic the switching activities of the silicon [18]. Apart from the chip operations at several GHz, in modern ICs, techniques such as power gating (kHz to 0.1MHz), clock gating (0.1 to 100MHz) and dynamic voltage/frequency scaling (<kHz) are commonly used to maximize the power efficiency of a system. Those chip operations are usually at very low frequency and can make radical changes on the current signature which could cause a serious simultaneous switching noise (SSN) [19].

To capture chip operations at both high frequency and at low frequency, herein current profiles are synthesized by multiplying a high-frequency component and a low-frequency component. Both components consist of a trapezoidal pulse unit and a bit sequence.

The unit trapezoidal pulse is showed in Figure 2.1. It contains 6 parameters: I_{peak}, I_{idle}, t_r, t_{on}, t_f and t_{off}. In these 6 parameters, I_{peak} and I_{idle} are related to the IC switching current amplitude at on state and idle state respectively, and t_r, t_{on}, t_f and t_{off} describe the time scale of a unit pulse: t_r and t_f are the rise time and the fall time during the switching,

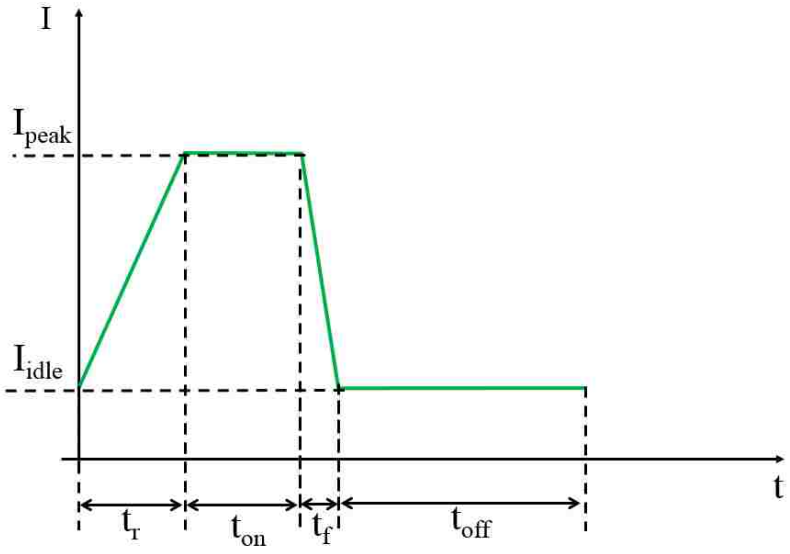


Figure 2.1. Unit trapezoidal pulse when the bit value is 1.

and t_{on} and t_{off} are the on time and the off time. In order to capture the noise during IC operations, these 6 parameters are assumed to be random variables. For every pulse, a set of these 6 parameters are generated from a realization based on the joint probability distribution function (PDF) of these 6 random variables.

Figure 2.2 shows the flow chart to generate a high-frequency or a low-frequency switching current component. For both the high-frequency and the low-frequency components, a bit sequence is defined at the beginning. A trapezoidal pulse is then generated from a realization for every bit with value 1. For zero bits, the current amplitude is I_{idle} at any time during that bit. Next the high-frequency component and the low-frequency component are obtained by combining all the pulses and finally the total switching current is derived by multiplying the high-frequency component and the low-frequency component, as shown in the example in Figure 2.3.

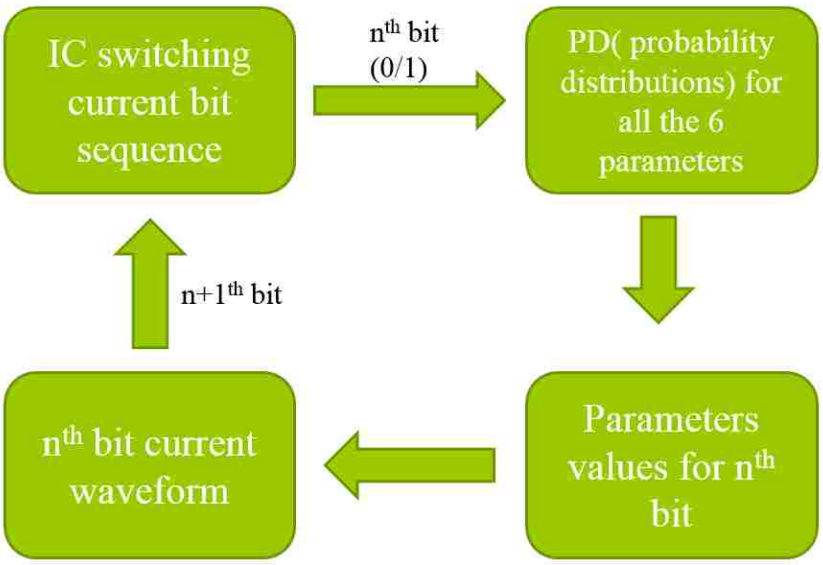


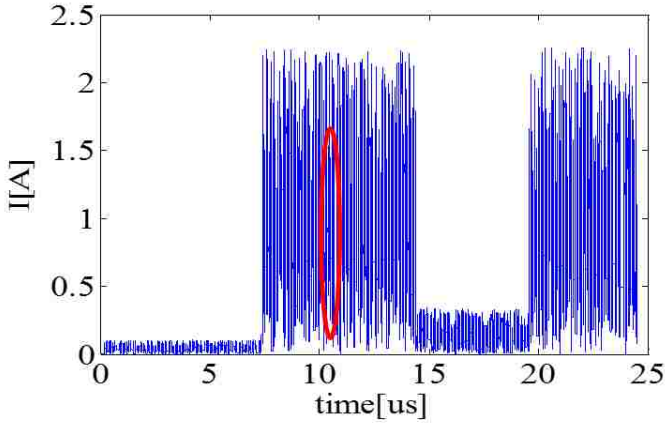
Figure 2.2. Flow chart to generate the low/high frequency current component.

2.2. AN EQUIVALENT CIRCUIT MODEL

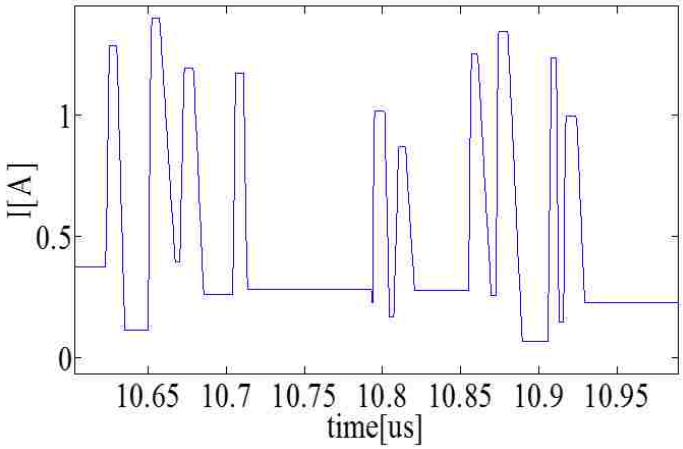
Many reports in the literature on power distribution network have focused on extracting the parasitic inductance or capacitance associated with a certain piece of the PDN geometry [13], [14], [20], [15]. And thus an equivalent circuit model can be derived based on those inductances and capacitances [21], [16].

Despite the fact that the PDN geometry can be very complicated, the equivalent circuit model is always simple.Typically several types of decoupling capacitors are employed in a power distribution network to lower the input impedance in different frequency ranges, which can provide hierarchical charge reservoirs for the IC. In general, PCB decoupling capacitors have larger capacitance and loop inductance while on-package decoupling capacitors have smaller capacitance and inductance. Thus the PDN structure can be modeled as cascaded LC circuits, as shown in Figure 2.4 and Figure 2.5.

It's also fairly common that different capacitors are used for PCB PDNs. In the circuit model shown in Figure 2.4(b), each vertical RLC branches represents a group of capacitors which have similar capacitance and loop inductance. The blue branch is associated with



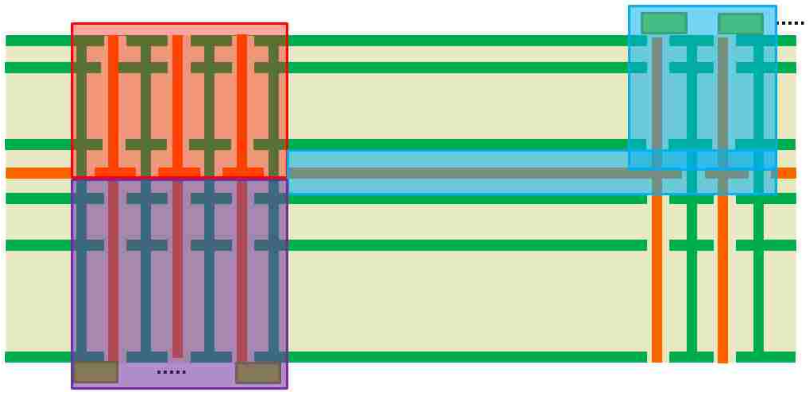
(a) Total switching current.



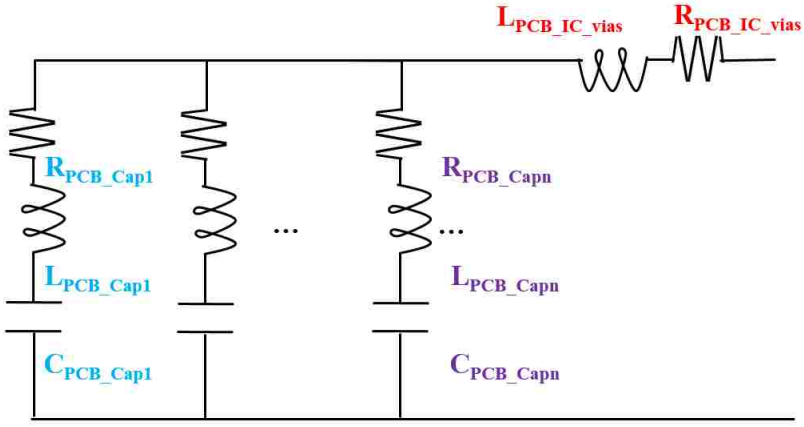
(b) Zoomed-in current waveform in the red circle.

Figure 2.3. A synthesized current profile example.

capacitors on the top layer and away from the IC, power net area fills between the IC and the capacitors, and also vias and pads connecting the power net area fills to those capacitors. And the purple branch is related to capacitors under the IC. Apart from the vertical circuit components, the horizontal red resistor $R_{PCB\_IC\_vias}$ and inductor $L_{PCB\_IC\_vias}$ represent the resistance and inductance associated with vias connecting IC pads to power net area fills respectively.



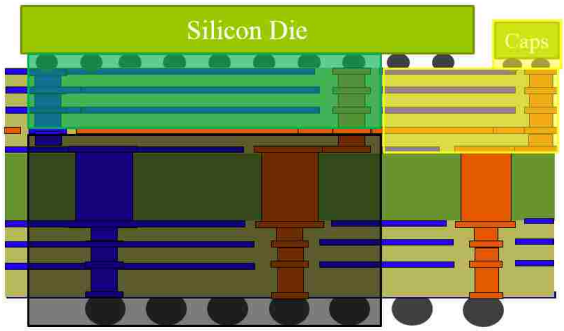
(a) Typical PCB PDN geometry.



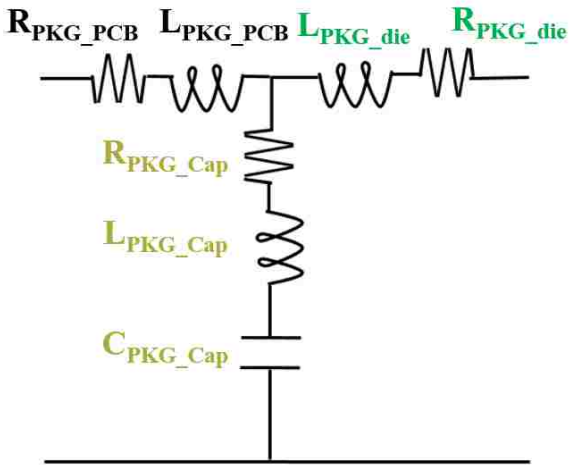
(b) Corresponding circuit model.

Figure 2.4. An equivalent circuit model for the PCB PDN.

Due to limited space, there are much less decoupling capacitors in the package. However the one-on-one correspondence between the package PDN geometry and the package PDN equivalent circuit is very similar to that of the PCB PDN. In the circuit model shown in Figure 2.5(b), the vertical resistor R_{PKG_Cap} and inductor L_{PKG_Cap} are associated with the current that starts from the power net area fill, flows to the on-package decoupling capacitor and returns through adjacent ground planes, as colored yellow in Figure 2.5(a). The vertical capacitor C_{PKG_Cap} then represents all the capacitance of the on-package decoupling capacitors. Similar to $R_{PCB\_IC\_vias}$ and $L_{PCB\_IC\_vias}$ in Figure 2.4(b),



(a) Typical package PDN geometry.



(b) Corresponding circuit model.

Figure 2.5. An equivalent circuit model for the package PDN.

the horizontal black resistor R_{PKG_PCB} and inductor L_{PKG_PCB} relate to solder balls and vias connecting those balls to the power net area fill. And R_{PKG_die} and L_{PKG_die} relate to solder bumps and vias connecting those bumps to the power net area fill.

2.3. VOLTAGE RIPPLE SPECTRUM DECOMPOSITION

By combining the current profile generated from the current synthesizer mentioned in Section 2.1 with the circuit models mentioned in Section 2.2, the time-domain voltage noise ripple can then be calculated. And finding one-on-one relationships between PDN ge-

ometries and different voltage ripple aspects based on those calculations will be much more helpful to the PDN designing because the dominant voltage ripple aspect and associated geometry can thus be identified easily.

Closed-form expressions for the maximum transient noise voltage caused by a triangle current pulse on a power distribution network comprised of traces with decoupling capacitors have been derived in [22], which is very helpful in early design stages by giving a simple and intuitive relationship between the PDN geometry and the actual noise voltage. And later on that idea was extended for a burst train of triangle current pulses [23]. However, although the shape of the input impedance curve of a PDN structure with power traces as used in [22] and [23] is fairly similar to that of a multi-layer PCB PDN, when the switching current profile is more complicated, it's no longer practical to solve the voltage noise ripple analytically in time domain. Thus a voltage noise ripple calculation and decomposition approach in time domain has been proposed for the PCB PDN in [17]. Herein this approach is extended for cascaded PCB and package PDNs.

2.3.1. Input Impedance Spectrum Decomposition and Its One-on-one Correspondence with the PDN Geometry. As mentioned in Section 2.1. In frequency domain, the voltage noise ripple is the product of the switching current and the PDN input impedance. Thus to establish a one-on-one correspondence between different voltage aspects and the PDN geometry, it's critical to first find the relationship between the PDN input impedance and the PDN geometry. The one-on-one relationship between the PCB PDN input impedance and the PCB PDN geometry has been given in [17]. To extend that idea to cascaded PCB and package PDNs, the entire range of frequencies is divided into 3 subdivisions based on the antiresonance frequency between the PCB inductance and the on-package capacitance, as shown in Figure 2.6.

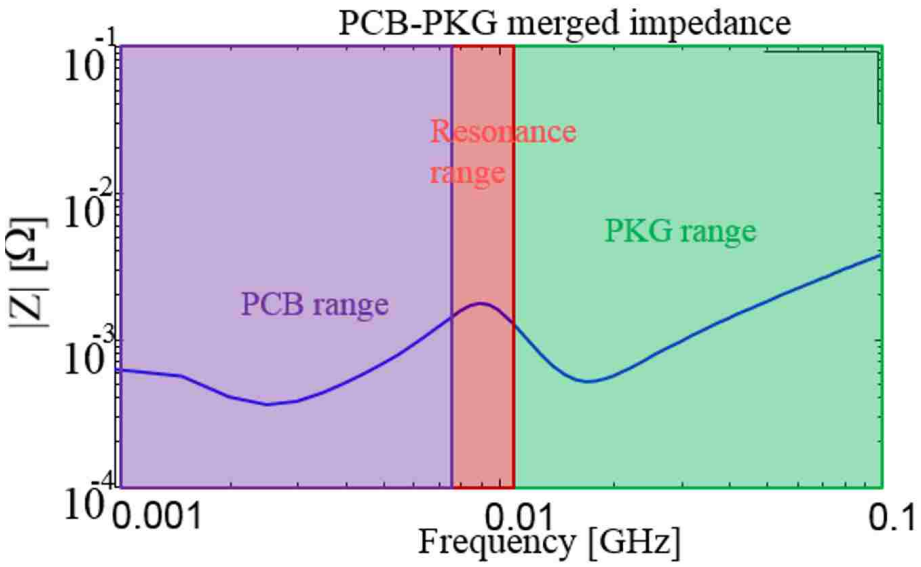


Figure 2.6. The entire range of frequencies are divided into 3 subdivisions: PCB range, resonance range and package range.

Figure 2.6 is from a real design, and the 3 subdivisions are PCB range, resonance range and package range. The antiresonance in the resonance range is caused by the parallel LC resonance between the PCB inductance and the package capacitance. A basic LRC circuit model is drawn in Figure 2.7, and the impedance of that circuit is given as

$$Z = \frac{j\omega L(1 + j\omega CR)}{1 - \omega^2 LC + j\omega CR}, \quad where\ \omega = 2\pi f. \tag{2.1}$$

And the parallel LC resonance frequency and the input impedance at that frequency is given as

$$f_{peak} = \frac{1}{2\pi\sqrt{LC}} \tag{2.2}$$

$$Z_{peak} = \frac{L + jR\sqrt{CL}}{RC}. \tag{2.3}$$

It can be seen from Equation (2.3) that if R goes to zero, the denominator RC would go to zero at $f = f_{peak}$ and the total input impedance Z_{peak} of that circuit would approach infinity. That means the PDN input impedance around that resonance frequency can be very

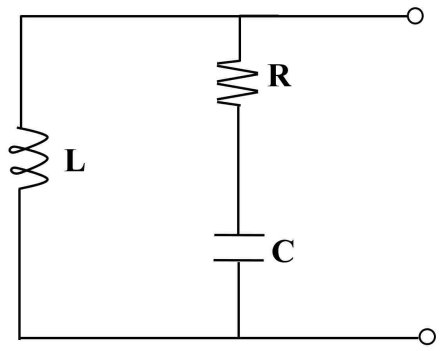
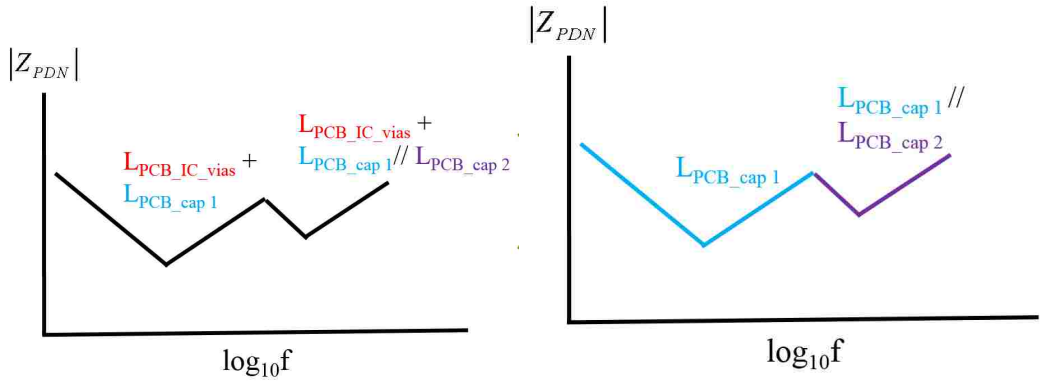


Figure 2.7. Basic LRC circuit.

high if the resistance is not designed well to damp that resonance, which is a very important design consideration because the voltage noise can be very significant if the resonance is not damped well and the switching current happens to have much energy around that frequency. Thus the resonance range in Figure 2.6 is related to the cascaded PDN impedance when the PCB inductance and the on-package capacitance resonates and can be used to check the associated voltage noise ripple aspect that can dominate if there is not enough resistance to damp that resonance. Since generally more resistance means more associated inductance and it's also essential to keep the inductance low to bring down the total input impedance at high frequencies, there is always a trade-off between more resistance and less inductance when choosing on-package capacitors.

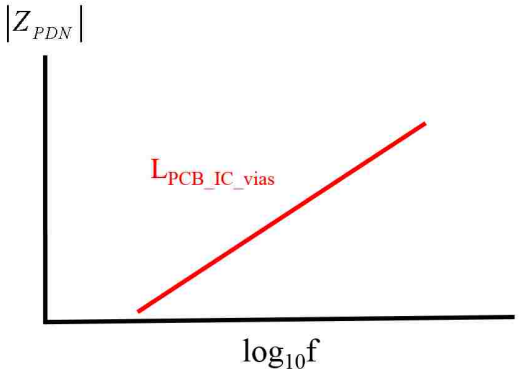
Before establishing one-on-one relationships between the cascaded PDN input impedance with the PDN geometry for the other two frequency ranges in Figure 2.6 , an open circuit approximation is proposed herein which assumes the on-PCB decoupling capacitors are open circuits in the package range while the on-package capacitors are open circuits in the PCB range. Although on-PCB capacitors always have larger capacitance and thus lower impedance at low frequencies than on-package capacitors, they also have larger loop inductance, which gives them higher impedance at high frequencies than the on-package capacitors. So the approximation is valid when the ratio of the on-package capacitance and the on-PCB capacitance and ratio of the package inductance and the PCB inductance

associated with those decoupling capacitors are sufficiently large, which is always the case for PCB PDNs and matched package PDNs. Thus the one-on-one correspondence between the PDN impedance and the PDN geometry for both the PCB frequency range and the package frequency range in Figure 2.6 can be derived from the same approach as is used in [17].



(a) Total input impedance in the PCB range.

(b) Input impedance aspect associated with PCB decoupling capacitors.



(c) Input impedance aspect associated with PCB IC vias.

Figure 2.8. PDN input impedance spectrum decomposition and its one-on-one correspondence with the geometry in the PCB range.

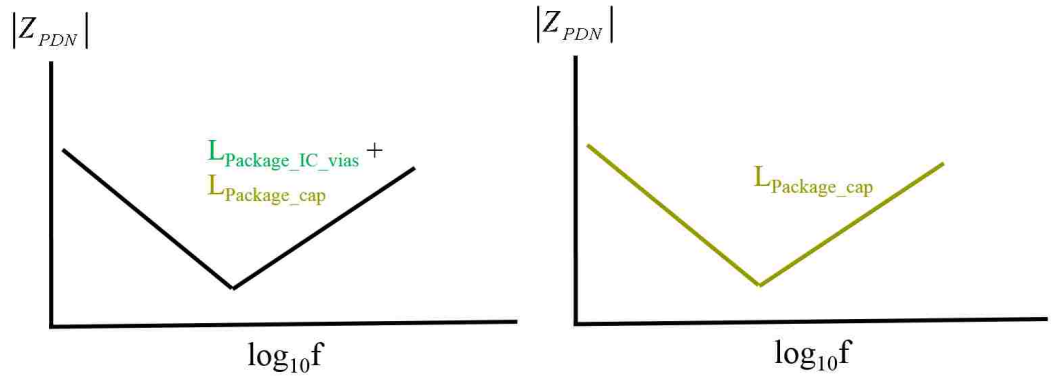
As shown in Figure 2.8, the PDN impedance in the PCB range is divided into 2 parts, one is associated with PCB decoupling capacitors and the other is related to PCB IC vias, as depicted in Figure 2.4. Same colors are used for corresponding geometry pieces, equivalent circuit elements and input impedance aspects in frequency domain. For the PCB PDN, decoupling capacitor types and their locations can be very different, which

can result in several resonances in the PCB range. Sometimes the parasitic parallel-plate capacitance of the PDN power and ground planes can resonate with the loop inductance of the decoupling capacitors as well. Since this capacitance is very similar to that of the decoupling capacitors, it's not drawn in Figure 2.4(b), The example shown in Figure 2.4(a) has two types of decoupling capacitors as illustrated in Section 2.2. Herein cap 1 represents the decoupling capacitors that are away from the IC and have larger capacitance and loop inductance than cap 2, which is related to those small 0402 SMT capacitors that are right under the IC. The input impedance aspect associated with the PCB decoupling capacitors can be further reduced to nearly zero if enough capacitors are added despite the fact that the apparent impedance seen between the power and ground planes may not decrease as 1/N as might be thought due to mutual terms [24].

Another impedance aspect is related to the PCB IC vias, as is colored red in Figure 2.4 and Figure 2.8. This part of the impedance is from the inductance and resistance associated with the part of the PCB IC vias that interconnects the PCB IC pads and the power net area fill. So instead of adding or removing decoupling capacitors, which will have no influence on this impedance aspect, adding IC vias or alternating IC power and ground vias can help to bring down the impedance.

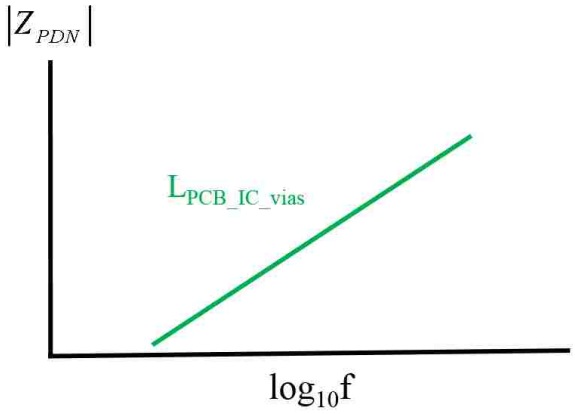
Same decomposition approach can be adopted for the package range, as shown in Figure 2.9. Unlike the PCB PDN, generally there is only one series LC resonance in the package frequency range due to the limited space for decoupling capacitors in packages. However, the relationships between the package PDN input impedance and the package PDN geometry is very similar to that of the PCB PDNs. The impedance aspect related to on-package capacitors which is colored yellow in Figure 2.5 and Figure 2.9 would also go to zero as more and more on-package capacitors are added. The impedance aspect colored green is related to the part of the vias that interconnects the solder bumps and the power net area fill in the package. There are also inductance and resistance associated with another part of the vias that interconnects the solder balls and the power net area fill of package

PDNs, namely L_{PKG_PCB} and R_{PKG_PCB} in Figure 2.5. However they are not shown in Figure 2.9 because based on the approximation proposed earlier in this subsection, the PCB is assumed to be open in the package frequency range and thus L_{PKG_PCB} and R_{PKG_PCB} won't contribute to the total impedance in the package range.



(a) Total input impedance in the package range.

(b) Input impedance aspect associated with package decoupling capacitors.



(c) Input impedance aspect associated with package IC vias.

Figure 2.9. PDN input impedance spectrum decomposition and its one-on-one correspondence with the geometry in the package range.

2.3.2. Voltage Noise Ripple Calculation and Decomposition. The IC switching current can also be divided into 3 parts according to Figure 2.6. With the input impedance spectrum decomposition mentioned in last subsection, the total voltage noise ripple can

then be calculated and decomposed as

$$
\begin{aligned}
v(t)_{total} &= F^{-1}\left\{I(f)_{total} \times Z(f)_{total}\right\} \\
&= F^{-1}\left\{I(f)_{PCB} \times Z(f)_{total} + I(f)_{resonance} \times Z(f)_{total} + I(f)_{PKG} \times Z(f)_{total}\right\} \\
&= F^{-1}\left\{I(f)_{PCB} \times Z(f)_{PCB} + I(f)_{resonance} \times Z(f)_{resonance} + I(f)_{PKG} \times Z(f)_{PKG}\right\} \\
&= F^{-1}\left\{I(f)_{PCB} \times Z(f)_{PCB\_decap}\right\} + F^{-1}\left\{I(f)_{PCB} \times Z(f)_{PCB\_IC\_vias}\right\} + \\
&\quad F^{-1}\left\{I(f)_{resonance} \times Z(f)_{resonance}\right\} + F^{-1}\left\{I(f)_{PKG} \times Z(f)_{PKG\_decap}\right\} + \\
&\quad F^{-1}\left\{I(f)_{PKG} \times Z(f)_{PKG\_die\_vias}\right\} \\
&= v(t)_{PCB\_decap} + v(t)_{PCB\_IC\_vias} + v(t)_{resonance} + v(t)_{PKG\_decap} + v(t)_{PKG\_IC\_vias}
\end{aligned}
$$

Herein the total voltage noise ripple is calculated using inverse Fourier transform and it comprises 5 aspects in frequency domain. Since both Fourier transform and inverse Fourier transform are linear operations, the total voltage noise ripple can then be divided into 5 aspects in time domain, as shown in the equation above.

2.4. EXAMPLES BASED ON A REAL DESIGN

The decomposition approach proposed in this paper is applied to a real PCB and package design in this section. Since the high frequency component are already well decoupled at chip level for this design, herein only a low frequency component is considered for this design. The switching current waveform used in this example is 1MHz periodic triangles as depicted in Figure 2.10. And the input impedance of the cascaded PCB and package PDN is shown in Figure 2.11. Normalized impedance are shown in Figure 2.11 to be compared with the switching current spectrum which is also normalized. Same as what has been discussed in Section 2.3, herein two types of on-PCB decoupling capacitors are used. Cap 1 refers to the decoupling capacitors that are away from the IC and the other capacitors are 0402 capacitors under the IC. It can be seen from the impedance curve that as more and more cap 1s are added, the first anti-resonance which is due to the loop inductance

of all cap 1s and the capacitance of all the 0402 capacitors disappears because the loop inductance associated with cap 1s is reduced. However, adding more on-PCB capacitors won't change the inductance of the PCB IC vias or the package impedance because they are related to other parts of the PDN geometry.

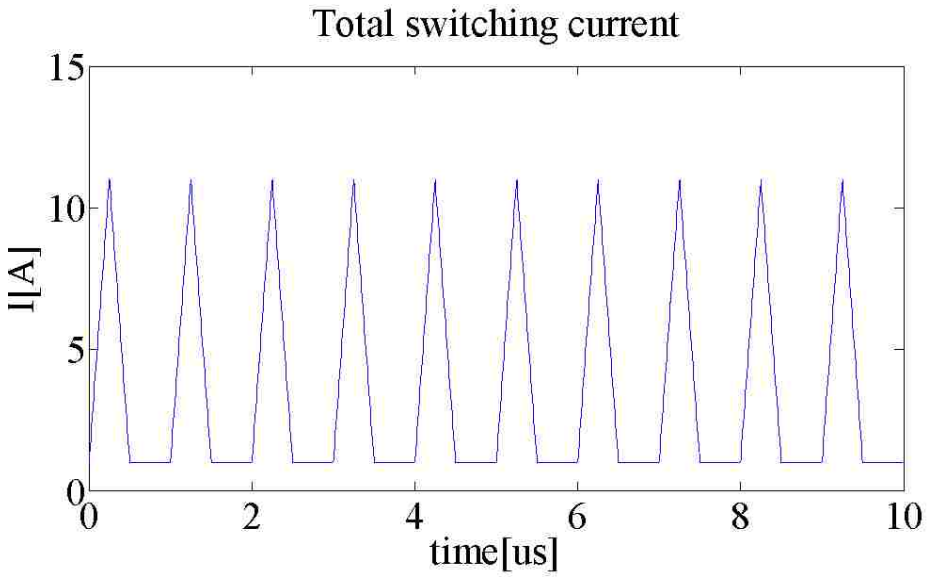


Figure 2.10. Switching current waveform.

The total voltage noise ripple seen at the package bumps caused by that switching current is then calculated using FFT and IFFT, as shown in Figure 2.12(a). After that the decomposition method is applied. Two dominant voltage aspects are shown in Figure 2.12(b) and Figure 2.12(c). Other aspects are not shown here because they are too subtle. It can be seen from Figure 2.12(b) that as more and more PCB decoupling capacitors are added, the voltage ripple aspect associated with PCB PDN capacitors is reduced significantly. The maximum voltage ripple related to the PCB capacitors is reduced by about 1.3mV if 9 more capacitors are added, as can be seen from the red and green curves in Figure 2.12(b). And instead of using 100 cap 1s, 10 cap 1s might be enough because it takes another 90 capacitors to lower the maximum voltage ripple only by 0.2mV.

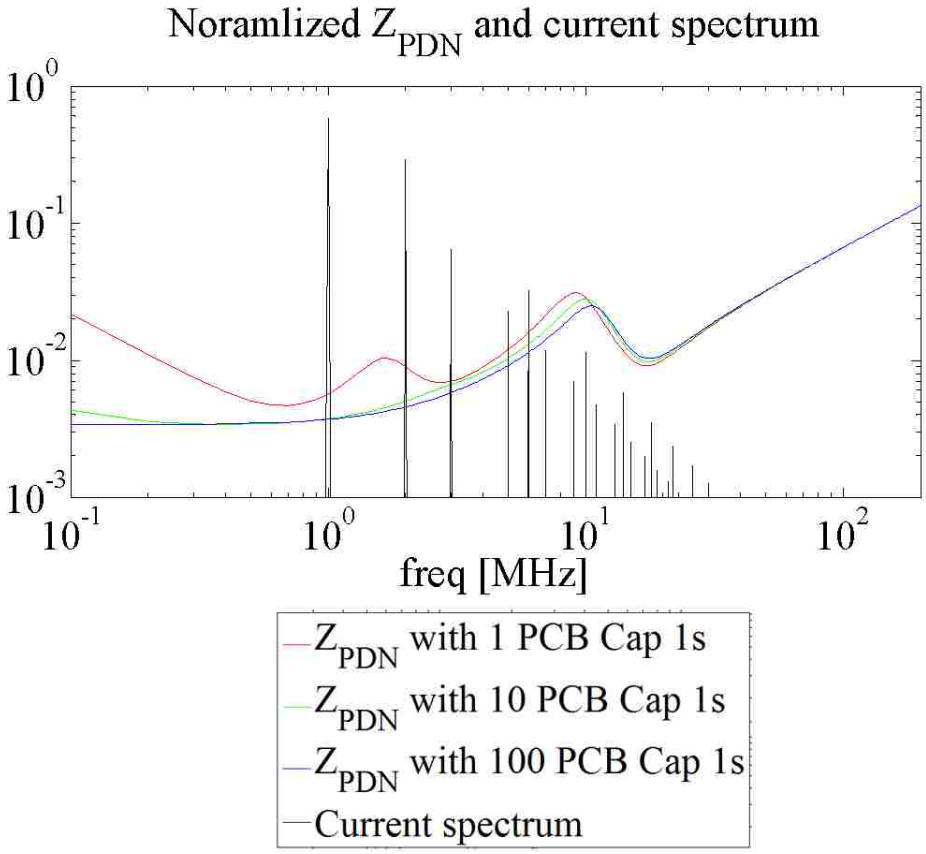
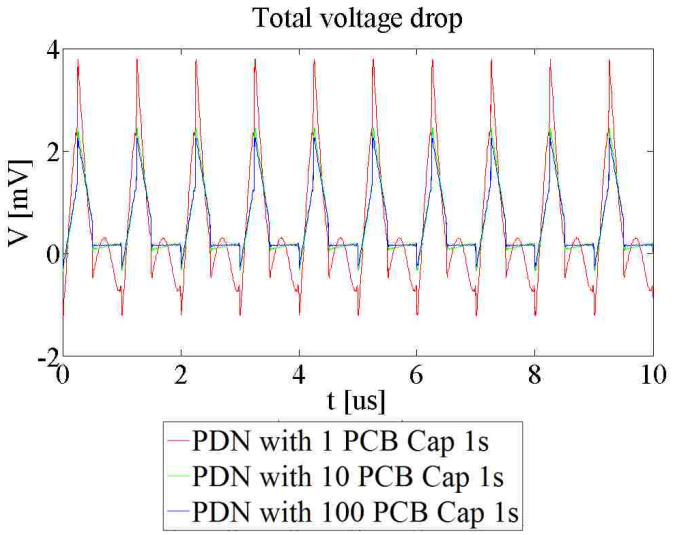


Figure 2.11. Normalized Z_{PDN} and current spectrum.

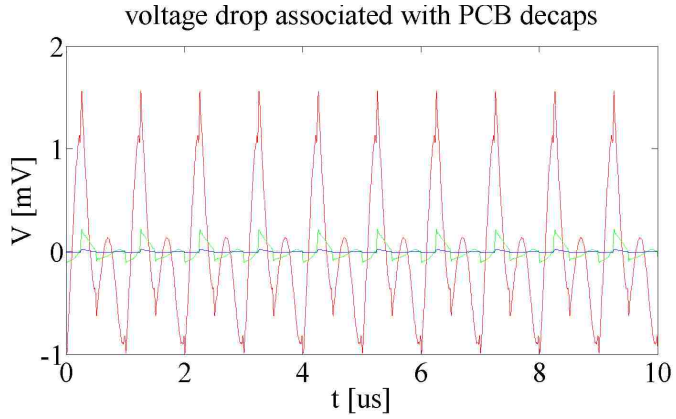
Figure 2.12(c) shows another dominant voltage ripple aspect which is related to the PCB IC vias and the PCB-package interconnects. In this voltage ripple aspect waveform, those sudden jumps are related to the inductance which happen when the derivative of the switching current changes at the triangle vertexes, and those slopes are associated with the resistance which are related to the triangle sides of the switching current. Adding more PCB capacitors won't help to reduce this voltage ripple aspect. A more effective way to bring down this voltage ripple aspect would be adding more IC vias or changing IC via patterns to make the mutual inductance between the power vias and ground vias larger [24].

2.5. CONCLUSION

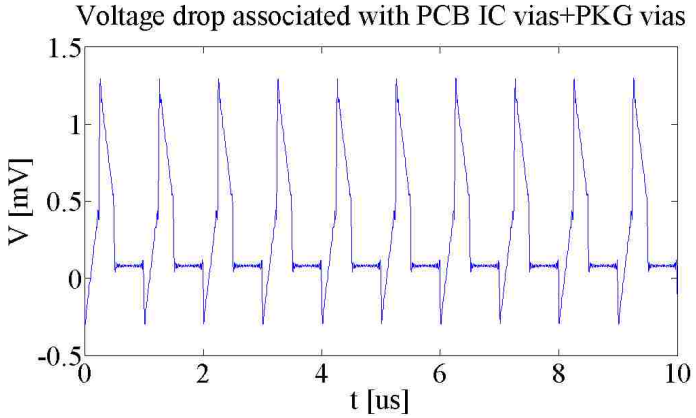
For PDN time domain voltage ripple calculation, the switching current profile can be synthesized by multiplying a high frequency component and a low frequency component based on a given joint probability distribution function of the parameters of the components. Based on an open circuit approximation, the voltage ripple spectrum decomposition approach is extended from PCB PDNs to cascaded PCB and package PDNs. The one-on-one relationships between the voltage aspects, the PDN geometry and the PDN input impedance in frequency domain are then established. An example based on a real design shows how this decomposition approach can help to find the dominant voltage ripple aspects and their associated parts of the PDN geometry, thus avoiding too much overdesign.



(a) Total voltage ripple.



(b) Voltage noise across the PCB decoupling capacitors.



(c) Voltage noise across the PCB and package IC vias.

Figure 2.12. Voltage noise ripple.

3. A TOOL DEVELOPMENT FOR PEAK DISTORTION ANALYSIS BASED ON MULTIPLE EDGE RESPONSES

Intersymbol interference (ISI) is playing a more and more important role in the signal integrity of modern high-speed systems. And eye diagrams are the main diagnostic technique for evaluating the signal quality. Although conventional transient simulations with a long PRBS source can accurately characterize the eye diagram, sometimes it can take a very long time. Thus peak distortion analysis (PDA) is often used to extract the worst-case eye diagram and associated worst-case bit pattern in a much shorter time by only looking into the worst-case [25].

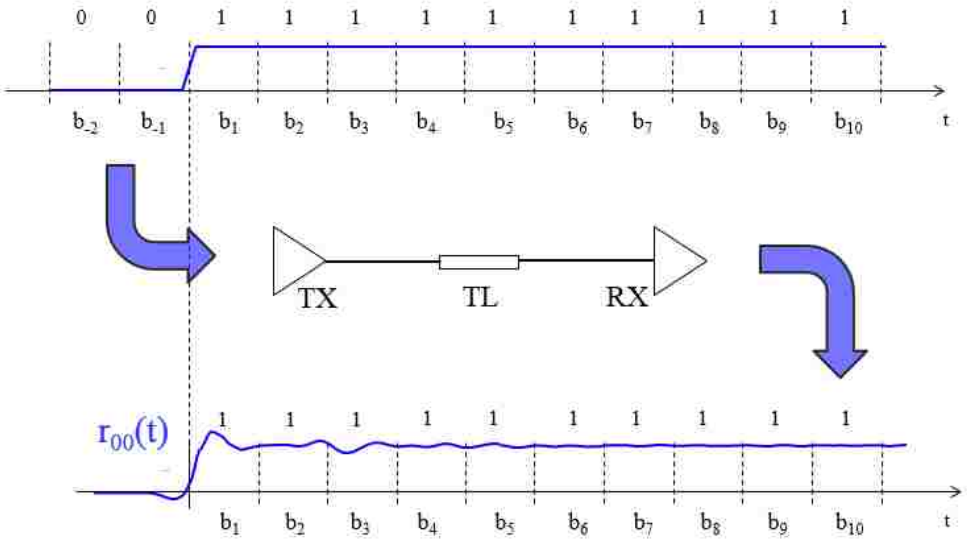
For linear time invariant (LTI) systems or systems that can be well approximated as an LTI system, single bit response (SBR) can work very well [25]. However, non-linearity is a common limitation for the use of SBR. Although the double edge response (DER) approach can handle asymmetric rising and falling edges [26], a more general edge response set is needed for non-linear systems, which is called multiple edge responses (MER).

3.1. NONLINEAR SYSTEMS AND MULTIPLE EDGE RESPONSES

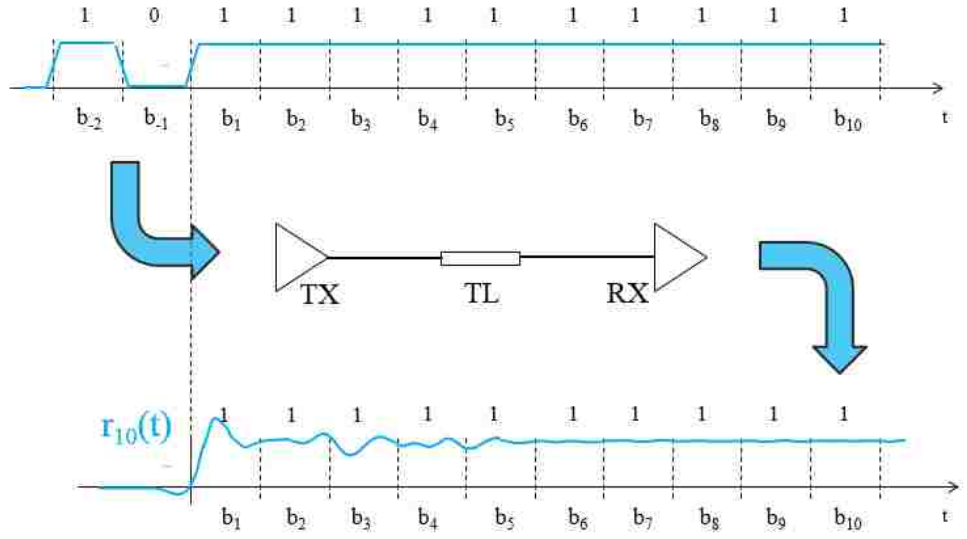
In [27], [28], and [29], a DER or MER approach is applied to nonlinear systems with voltage noise associated with the power supply network. However, as indicated in [30], even with a clean power supply, nonlinearity also needs to be taken into consideration to give an accurate worst-case estimation.

MER is very similar to DER in the way that any response can be decomposed as a summation of a set of edge responses and their shifted versions. An edge response set of DER only consists of a rising edge response and a falling edge response. However, due to nonlinearity, different bit patterns that are previous on the edge response can have different impact on that edge response, which means the edge response set needs to be extended by

also considering the previous bit pattern to be able to capture the nonlinearity in systems. Depending on the duration of the nonlinearity, the number of previous bits needed can be different. This can be related to the time constant associated with the power distribution network or the delay time of the channel. Thus MER is proposed for nonlinear systems, with the order of MER to be the number of previous bits needed.



(a) Rising edge response with previous two bits to be 00.



(b) Rising edge response with previous two bits to be 10.

Figure 3.1. Different rising edge responses associated with different previous bit patterns for 2nd order MER.

[28] gives a rigorous way to extract the edge response sets of different order of MER. Herein only basic illustration is given as in Figure 3.1 and Figure 3.2 with the use of a simple example by assuming the MER order to be 2 and the edge response duration to be 9 UIs, which means after 9 UIs, the edge response will settle down. Since 2^{nd} order of MER is assumed, there are four different previous bit patterns: "00", "01", '10' and '11'. Among them "00" and "10" are associated with two rising edge responses as shown in Figure 3.1, and "01" and "11" are associated with two falling edge responses. Herein $r_{10}(t)$ refers to the rising edge response with the previous two bit pattern to be "10" and etc.

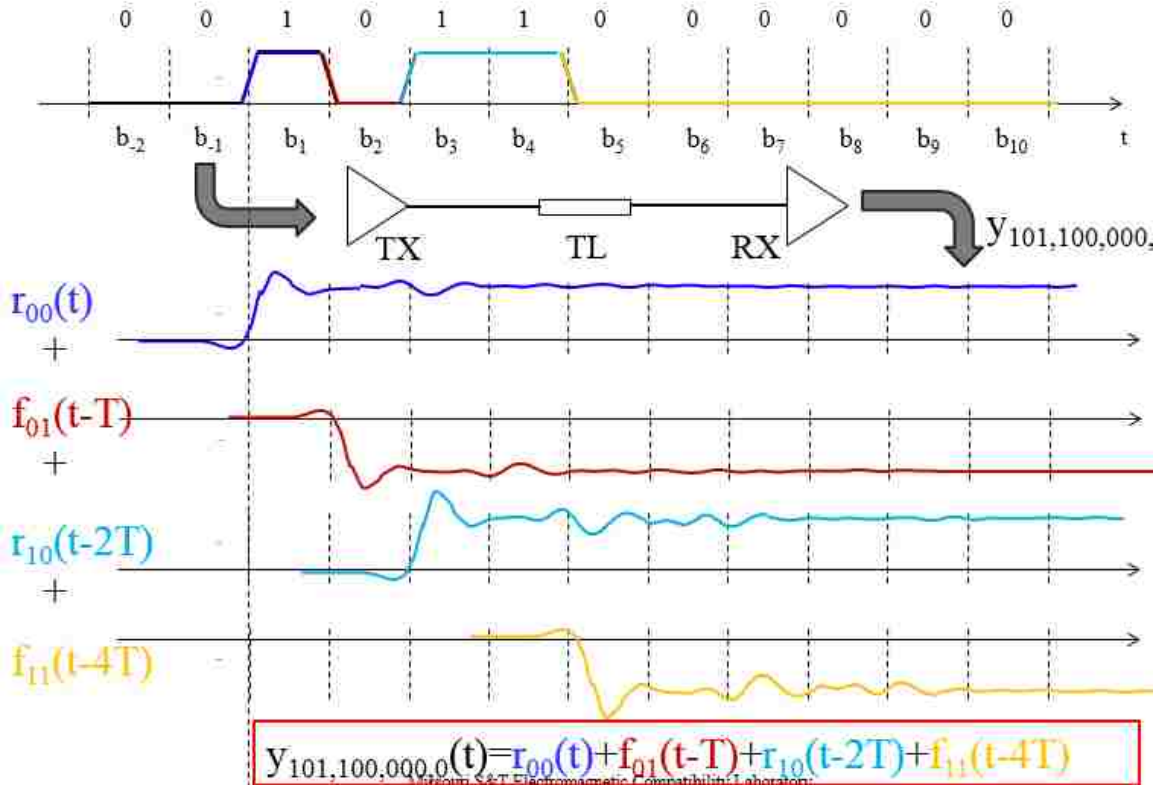


Figure 3.2. Any response can be decomposed as a summation of shifted MERs.

After extracting all the edge responses, any response with any input bit pattern can be synthesized by the superposition of corresponding shifted edge responses. An example is shown in Figure 3.2 with the input bit pattern to be "00 101 100 000 0". For the first rising edge, since the previous bit pattern is "00", $r_{00}(t)$ is thus used. For the second rising edge, since the previous bit pattern is "10", $r_{10}(t)$ is used. And the same goes for the other

falling edge responses. The total response is thus constructed by adding up all these shifted edge responses. Herein $y_{101,100,000,0}(t)$ refers to the response of the input bit pattern "101 100 000 0" from b_1 to b_10.

3.2. PEAK DISTORTION ANALYSIS BASED ON MERS

A rigorous peak distortion analysis approach based on MER is given in [31] by using the idea of dynamic programming [32]. Herein a simpler and more intuitive explanation is given in Figure 3.3 and Figure 3.4 with the same example as in last section.

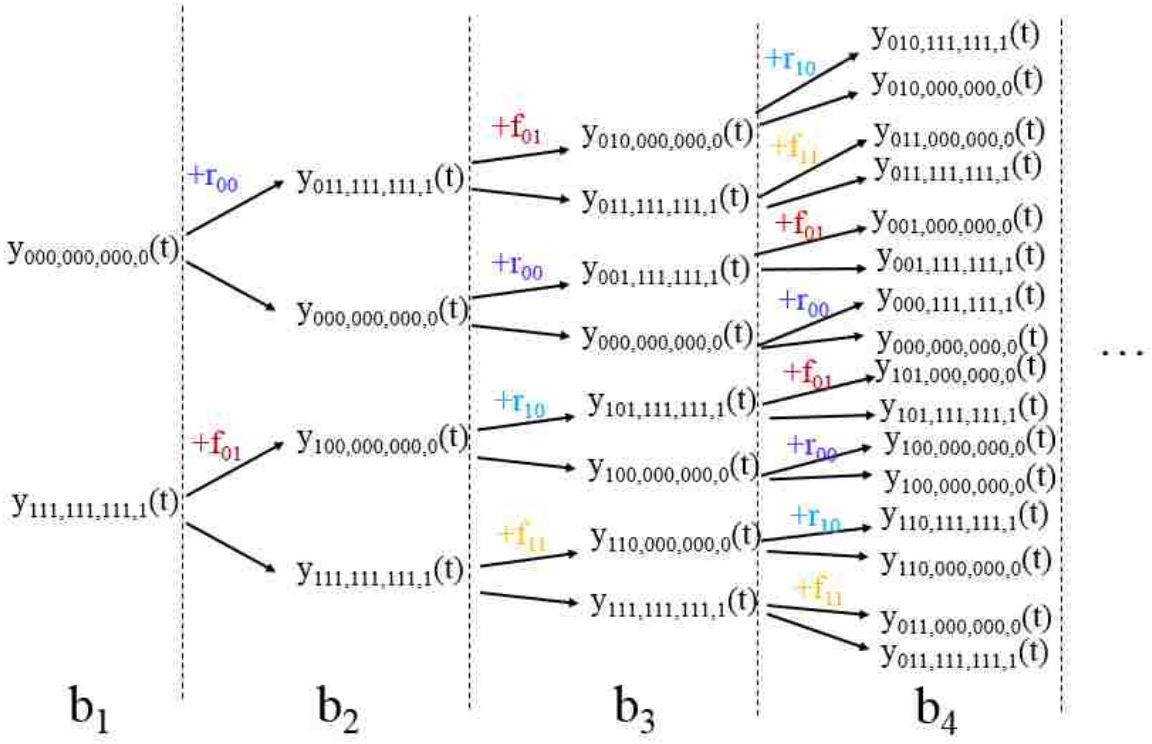


Figure 3.3. Recursive relationship.

The general way to determine the worst-case eye diagram is to compare all the possible responses at b_10 since the assumption is made that the duration of edge responses is 9 UIs. Extracting all the responses from $y_{000,000,000,0}(t)$ to $y_{111,111,111,1}(t)$ can be done by using the synthesizing approach mentioned in last section. However, it's obvious from

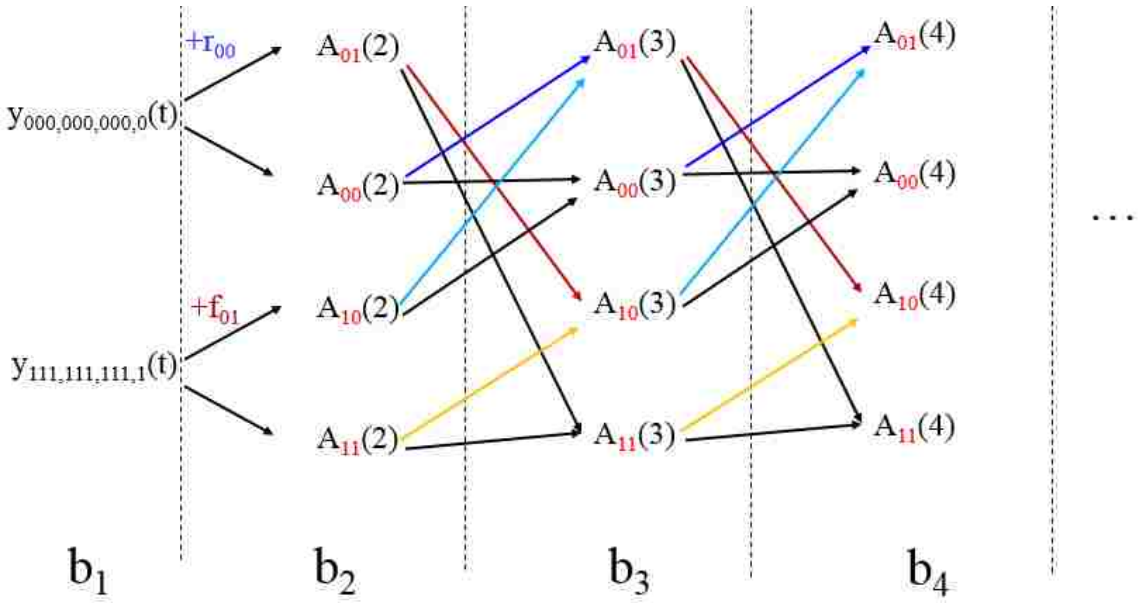


Figure 3.4. Recursive relationship using dynamic programming.

Figure 3.3 that the total number of comparisons is exponential to the number of UIs that the edge responses need to settle down. In this case, it takes around $2^{10} = 1024$ times of comparisons.

A better way to perform the comparisons, as mention in [31], can be realized by using dynamic programming. This is done by comparing temporary worst-case with different bit patterns at each bit from b_1 to b_10. Herein $A_{bxby}(j)$ refers to temporary worst case response ending with bxby at the j^{th} bit. It's obvious from Figure 3.4 that the total number of comparisons now becomes roportional to the number of UIs. Only $2^2 \times 10 = 40$ times of comparisons is needed. This can save a lot of computation time when the duration of edge responses are long.

3.3. A MATLAB TOOL DEVELOPMENT FOR PDA BASED ON MERS

A Matlb tool is developed based on the algorithm in [31]. Figure 3.5 shows the flow chart of the tool. Automatic Hspice simulations are run first to extract the edge response set needed. Then PDA calculation is performed based on the edge response set and worst-case eye diagram and associated worst-case bit pattern are given to the user.

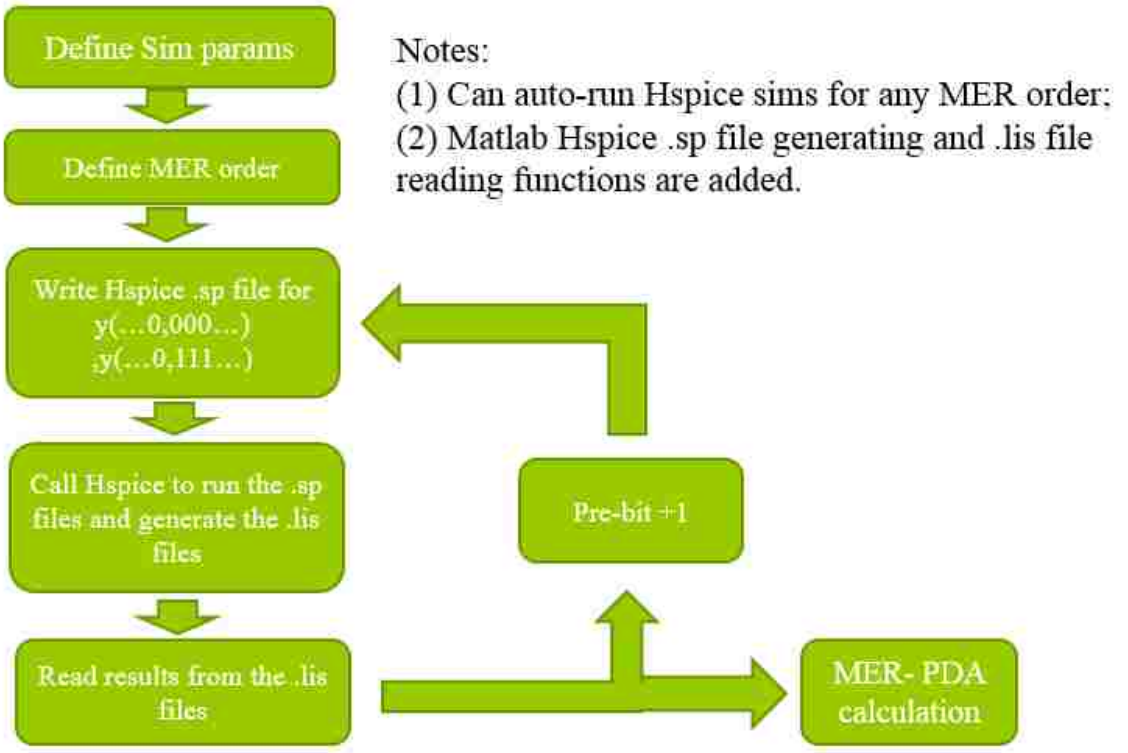


Figure 3.5. Flow chart of the PDA tool.

Figure 3.6 and Figure 3.7 show a nonlinear circuit model used for test and the PDA calculation results respectively. It can be seen that compared to PDA based on SBR, PDA based on MER can better capture asymmetric r/f edges and non-linearity in the system. Also by increasing the order of MER, the worst case eye extracted from PDA calculation is more and more close to the real worst-case eye.

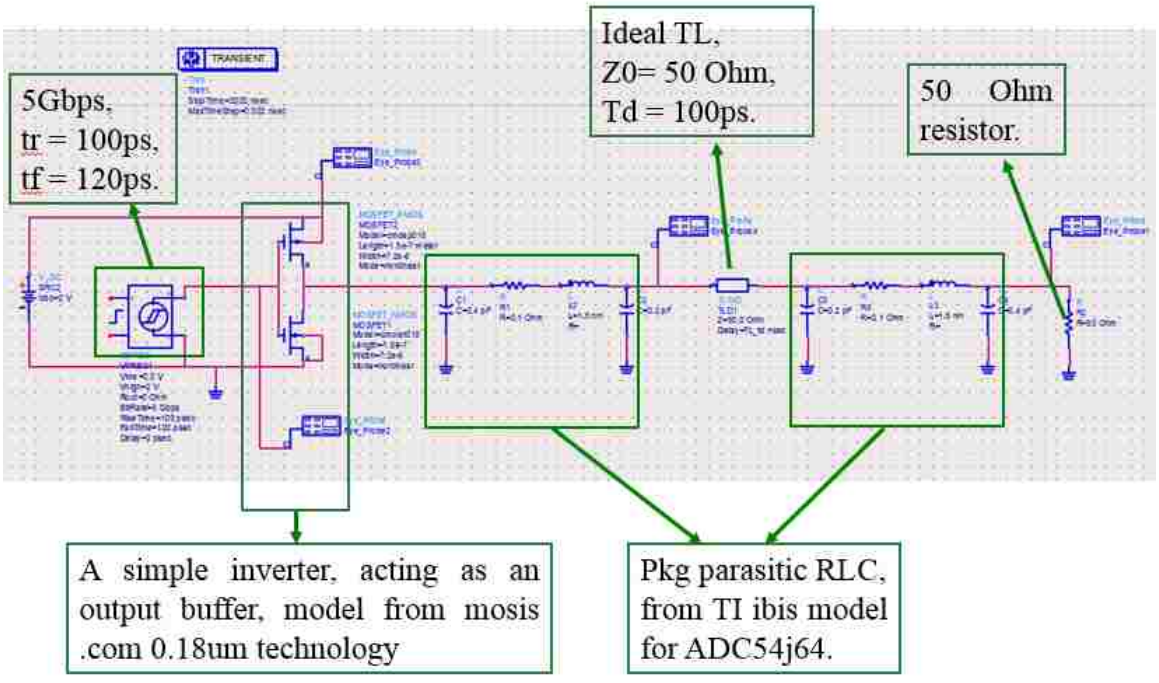
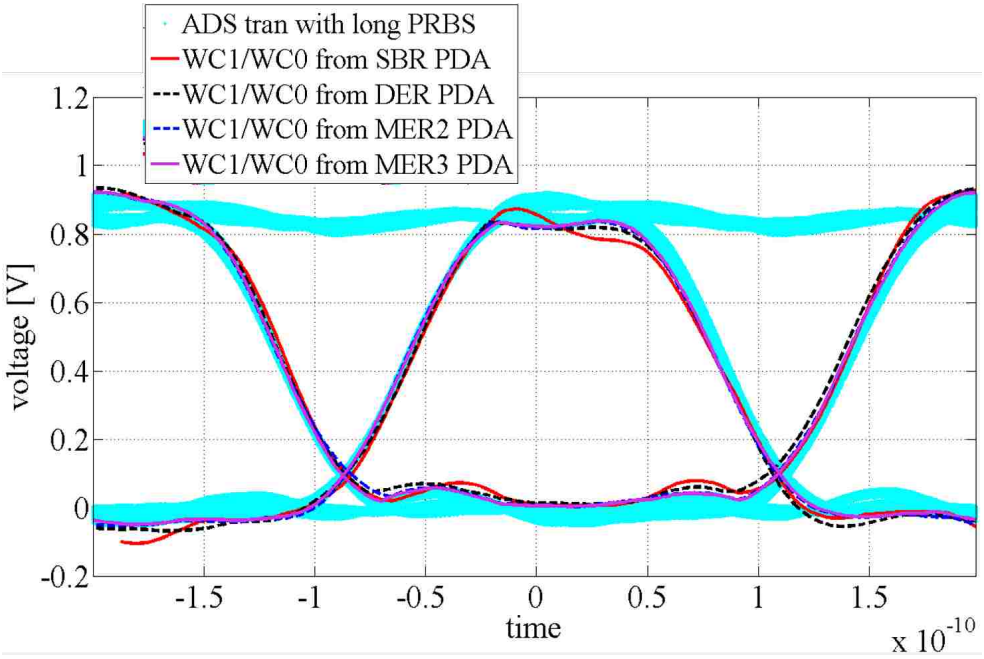
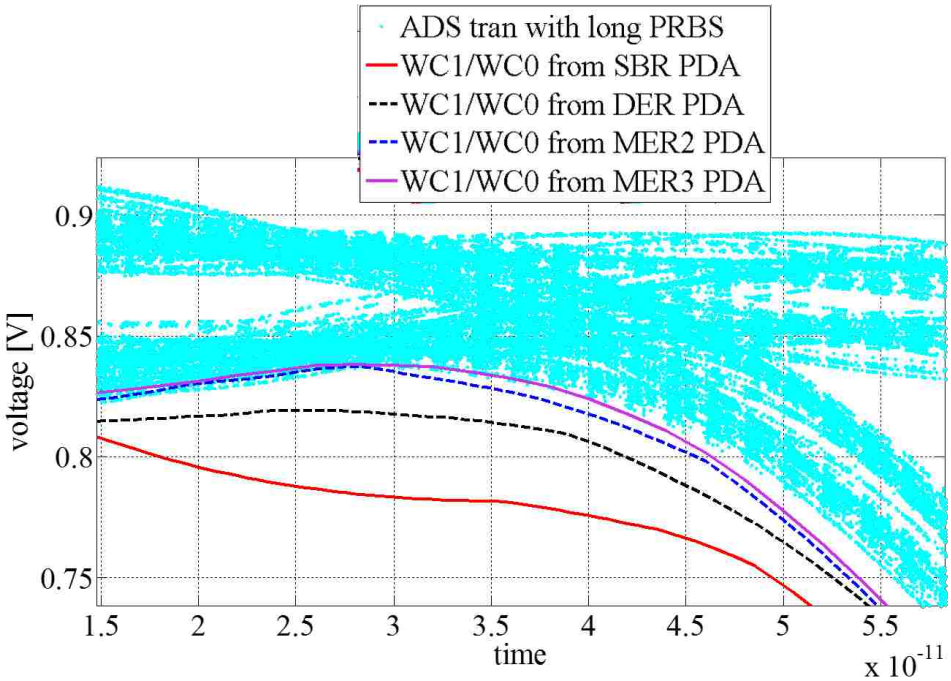


Figure 3.6. Test circuit of the Matlab tool.



(a) Results in 2 UIs.



(b) Zoomed-in at the right corner.

Figure 3.7. Comparison between PDA and transient simulation.

REFERENCES

[1] J. Kim, M. D. Rotaru, S. Baek, J. Park, M. K. Iyer, and J. Kim, "Analysis of noise coupling from a power distribution network to signal traces in high-speed multilayer printed circuit boards," *IEEE Transactions on Electromagnetic Compatibility*, vol. 48, no. 2, pp. 319–330, May 2006.

[2] J. Kim, S. Wu, H. Wang, Y. Takita, H. Takeuchi, K. Araki, G. Feng, and J. Fan, "Improved target impedance and ic transient current measurement for power distribution network design," in *2010 IEEE International Symposium on Electromagnetic Compatibility*, July 2010, pp. 445–450.

[3] Y. Lo, D. Solomon, and W. Richards, "Theory and experiment on microstrip antennas," *IEEE Transactions on Antennas and Propagation*, vol. 27, no. 2, pp. 137–145, Mar 1979.

[4] L. Ren, J. Kim, G. Feng, B. Archambeault, J. L. Knighten, J. Drewniak, and J. Fan, "Frequency-dependent via inductances for accurate power distribution network modeling," in *2009 IEEE International Symposium on Electromagnetic Compatibility*, Aug 2009, pp. 63–68.

[5] T. Okoshi, *Planar circuits for microwaves and lightwaves*. Springer Science & Business Media, 2012, vol. 18.

[6] C. A. Balanis, *Advanced engineering electromagnetics*. John Wiley & Sons, 1999.

[7] D. G. Dudley, *Mathematical foundations for electromagnetic theory*. IEEE press New York, 1994.

[8] J. Kim, K. Shringarpure, J. Fan, J. Kim, and J. L. Drewniak, "Equivalent circuit model for power bus design in multi-layer pcbs with via arrays," *IEEE Microwave and Wireless Components Letters*, vol. 21, no. 2, pp. 62–64, Feb 2011.

[9] D. G. Duffy, *GreenâĂŹs functions with applications*. CRC Press, 2015.

[10] Q. Shou, Q. Jiang, and Q. Guo, "The closed-form solution for the 2d poisson equation with a rectangular boundary," *Journal of Physics A: Mathematical and Theoretical*, vol. 42, no. 20, p. 205202, 2009.

[11] Y.-J. Zhang and J. Fan, "An intrinsic circuit model for multiple vias in an irregular plate pair through rigorous electromagnetic analysis," *IEEE transactions on microwave theory and techniques*, vol. 58, no. 8, pp. 2251–2265, 2010.

[12] G. Smith, "The proximity effect in systems of parallel conductors and electrically small multiturn loop antennas," HARVARD UNIV CAMBRIDGE MA DIV OF ENGINEERING AND APPLIED PHYSICS, Tech. Rep., 1971.

[13] Y. S. Cao, T. Makharashvili, J. Cho, S. Bai, S. Connor, B. Archambeault, L. Jiang, A. E. Ruehli, J. Fan, and J. L. Drewniak, "Inductance extraction for pcb prelayout power integrity using pmsr method," *IEEE Transactions on Electromagnetic Compatibility*, vol. 59, no. 4, pp. 1339–1346, Aug 2017.

[14] Y. S. Cao, T. Makharashvili, S. Connor, B. Archambeault, L. J. Jiang, A. E. Ruehli, J. Fan, and J. L. Drewniak, "Top-layer inductance extraction for the pre-layout power integrity using the physics-based model size reduction (pmsr) method," in *2016 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, July 2016, pp. 324–329.

[15] S. Bai, C. Huang, B. Zhao, J. Fan, A. Rueli, J. Drewniak, B. Archambeault, S. Connor, M. Cracraft, M. Cocchini, and B. Achkir, "Inductance extraction for physics-based modeling of power net area fills with complex shapes and voids using the plane-pair peec method," in *2016 IEEE/ACES International Conference on Wireless Information Technology and Systems (ICWITS) and Applied Computational Electromagnetics (ACES)*, March 2016, pp. 1–2.

[16] K. Shringarpure, S. Pan, J. Kim, J. Fan, B. Achkir, B. Archambeault, and J. L. Drewniak, "Formulation and network model reduction for analysis of the power distribution network in a production-level multilayered printed circuit board," *IEEE Transactions on Electromagnetic Compatibility*, vol. 58, no. 3, pp. 849–858, June 2016.

[17] C. Huang, B. Zhao, K. Shringarpure, S. Bai, X. Fang, T. Makharashvili, H. Ye, Y. S. Cao, M. Cracraft, M. Cocchini, S. Connor, Q. Gaumer, S. Scearce, B. Archambeault, B. Achkir, E. Li, L. Jiang, A. Ruehli, J. Fan, and J. Drewniak, "Power integrity with voltage ripple spectrum decomposition for physics-based design," in *2016 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, July 2016, pp. 318–323.

[18] W. Cheng, A. Sarkar, S. Lin, and J. Zheng, "Worst case switching pattern for core noise analysis," *Design Con*, 2009.

[19] K. Koo, Y. Lee, and W. Baek, "Power integrity analysis of chip–package–system (cps) of a mobile ap using extended cpm technique," in *DesignCon*, 2014.

[20] J. Kim, L. Ren, and J. Fan, "Physics-based inductance extraction for via arrays in parallel planes for power distribution network design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 9, pp. 2434–2447, Sept 2010.

[21] J. Kim, K. Shringarpure, J. Fan, J. Kim, and J. L. Drewniak, "Equivalent circuit model for power bus design in multi-layer pcbs with via arrays," *IEEE Microwave and Wireless Components Letters*, vol. 21, no. 2, pp. 62–64, Feb 2011.

[22] J. Kim, L. Li, S. Wu, H. Wang, Y. Takita, H. Takeuchi, K. Araki, J. Fan, and J. L. Drewniak, "Closed-form expressions for the maximum transient noise voltage caused by an ic switching current on a power distribution network," *IEEE Transactions on Electromagnetic Compatibility*, vol. 54, no. 5, pp. 1112–1124, 2012.

[23] J. Kim, J. Lee, S. Ahn, and J. Fan, "Closed-form expressions for the noise voltage caused by a burst train of ic switching currents on a power distribution network," *IEEE Transactions on Electromagnetic Compatibility*, vol. 56, no. 6, pp. 1585–1597, Dec 2014.

[24] B. Archambeault, B. Zhao, K. Shringapure, and J. Drewniak, "Design tips," *IEEE Electromagnetic Compatibility Magazine*, vol. 4, no. 2, pp. 106–107, nd 2015.

[25] J. Proakis, *Digital Communications*, ser. McGraw-Hill series in electrical and computer engineering : communications and signal processing. McGraw-Hill, 2001. [Online]. Available: https://books.google.com/books?id=aUp2QgAACAAJ

[26] F. Lambrecht, C.-C. Huang, and M. Fox, "Technique for determining performance characteristics of electronic systems," Aug. 10 2004, uS Patent 6,775,809.

[27] V. Drabkin, C. Houghton, I. Kantorovich, and M. Tsuk, "Aperiodic resonant excitation of microprocessor power distribution systems and the reverse pulse technique," in *Electrical Performance of Electronic Packaging, 2002 IEEE 11th Topical Meeting on*. IEEE, 2002, pp. 175–178.

[28] C.-C. Chou, H.-H. Chuang, T.-L. Wu, S.-H. Weng, and C.-K. Cheng, "Eye prediction of digital driver with power distribution network noise," in *Electrical Performance of Electronic Packaging and Systems (EPEPS), 2012 IEEE 21st Conference on*. IEEE, 2012, pp. 131–134.

[29] J. Cho, H. Kim, J. Fan, and B. Achkir, "Investigation of statistical eye-diagram estimation method for hbm including isi, x-talk, and power noise," in *Electromagnetic Compatibility & Signal/Power Integrity (EMCSI), 2017 IEEE International Symposium on*. IEEE, 2017, pp. 411–415.

[30] S. Pan and J. Qian, "An improved multiple edge responses method for memory simulation considering worst case and nonlinear crosstalk," in *Electromagnetic Compatibility and Signal Integrity, 2015 IEEE Symposium on*. IEEE, 2015, pp. 139–143.

[31] J. Ren and K. S. Oh, "Multiple edge responses for fast and accurate system simulations," *IEEE Transactions on Advanced Packaging*, vol. 31, no. 4, pp. 741–748, 2008.

[32] T. H. Cormen, *Introduction to algorithms*. MIT press, 2009.

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