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A novel power integrity modeling method based on plane pair PEEC

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A NOVEL POWER INTEGRITY MODELING METHOD BASED ON PLANE PAIR PEEC

by

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ABSTRACT

A low impedance power distribution network (PDN) is essential for high frequency integrated circuits. A novel modeling mothed, i.e. the plane pair PEEC method is proposed in this thesis to model the PDN of the multi-layered printed circuit board. The modeling results agrees favorably with full wave simulation and measurement. A PDN tool is develop based on this method.

ACKNOWLEDGMENTS

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1. INTRODUCTION

The power distribution network (PDN) is designed to provide a low impedance path for the time-varying current, without major disturbance of the voltage level. Recent chips integrated with millions of transistors consumes large power. The instantaneous switching current can generate simultaneous switching noise in the power distribution network, which is known to be the cause of system performance degradation, leading to problems such as jitter in high speed channels and electromagnetic interference (EMI) [1][2][3].

The PDN geometry and the physic based circuit is shown in Figure 1.1. The off-chip decoupling capacitors are widely used on printed circuit board (PCB) to sustain the switching current at megahertz to hundreds megahertz range. However, the efficiency of these capacitors are limited by the parasitic inductance associated with the current path on the power/ground planes, which can be segmented into 4 parts: Labove, Ldecap_via, Lplane, and LIC_via [4]. Modeling and quantifying the PDN impedance is important for securing the system performance.

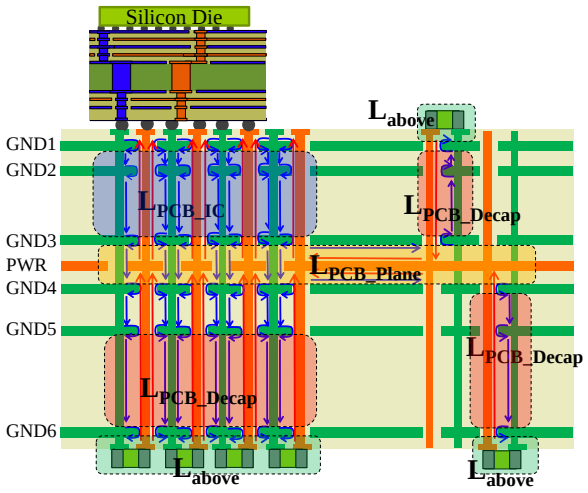


Figure 1.1.The PDN geometry and the physics based circuit.

The study of the PDN impedance has a long history. Full-wave electromagnetic simulations can accurately calculate the impedance, including the finite element method (FEM), finite-difference time domain (FDTD) method[5], the method of moments (MoM),

transmission-line grid method (TLM)[6], and the partial element equivalent circuit (PEEC) method[7][8][9]. However, the full-wave models require significant time and memories for the complex multilayer PCBs.

An efficient approach, based on the cavity model is proposed to fast estimate the PDN impedance for the rectangular power/ground structures with via arrays [4][10][11]. However, the cavity model method is only suitable for the rectangular structures, and it cannot model the PCB power nets which usually have arbitrary shapes and voids.

An improved PEEC model, i.e. the plane-pair PEEC (PPP), is proposed in [12][13][14][15], to efficiently model the complex shaped power/ground plane pair. This special PEEC method is a 2D solver, taking advantage of the symmetric current on the plane pair, to obtain a circuit where the coupling only happens to adjacent elements. These will result in a sparse linear system, which significantly reduces the run time and memory, compared to traditional full-wave solver.

Due to its efficiency and the ability to model complex shape, PPP is a promising technic for PCB PDN calculation. However, the previous study only focused on a fairly simple and unrealistic 2-layer geometry, with only one port and one short. There are many difficulties for applying PPP on a multi-layered PCB, such as unsymmetrical power/ground shape and multiple power layers, and multiple vias. PPP also have difficulty to solve the ground-ground layers due to the unsymmetrical current distribution. The solution for this difficulties is discussed in detail in this thesis.

The PPP method is briefly introduced in Section 2. In Section 3, the unsymmetrical power/ground shape is solved by image theory techniques, which convert such geometry to a symmetric one. The multiple power layers and multiple ground layers are solved by using the modified nodal analysis (MNA) method to solving the admittance matrices. In Section 4, The methodology is applied to a 6 layer PCB, with 14 decoupling capacitors and a complex shaped power net. The modeling results agrees with measurements and a commercial tool. Section 5, 6 and 7 shows the applications on PCB power nets, package power plane and Labove. The last Section shows a tool based on PPP.

2. PLANE-PAIR PEEC FORMULATION

2.1. PARTIAL INDUCTANCE FORMULATION FOR PEEC

The inductance is defined as the ration of the total magnetic flux going thru the closed loop surface and the current flowing on the loop. A closed loop C , carrying current I , has an area of S_1 , as shown in Figure 2.1. Then the magnetic flux penetrating the loop is,

$$\Psi = \iint_{S_1} \vec{B} \cdot d\vec{s} = \oint_C \vec{A} \cdot d\vec{l} \tag{1}$$

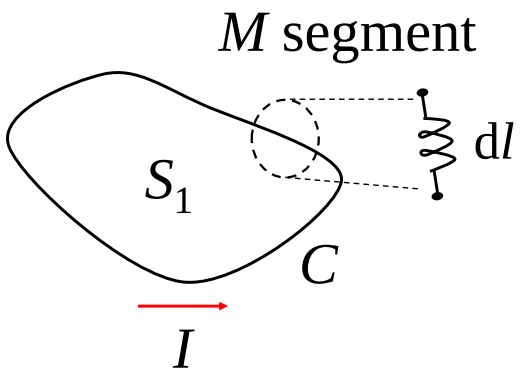


Figure 2.1. A closed loop carrying current. The loop is segmented into *M* segment. A partial inductance can be defined for each segment.

The inductance associated with the loop is defined as,

$$L = \frac{\Psi}{I} = \frac{\oint_C \vec{A} \cdot d\vec{l}}{I} \tag{2}$$

where $\vec{A}$ is the vector potential. Then consider a two loop system, segmenting the first loop into *M* pieces, and the second loop into *N* pieces, as shown in Figure 2.2.

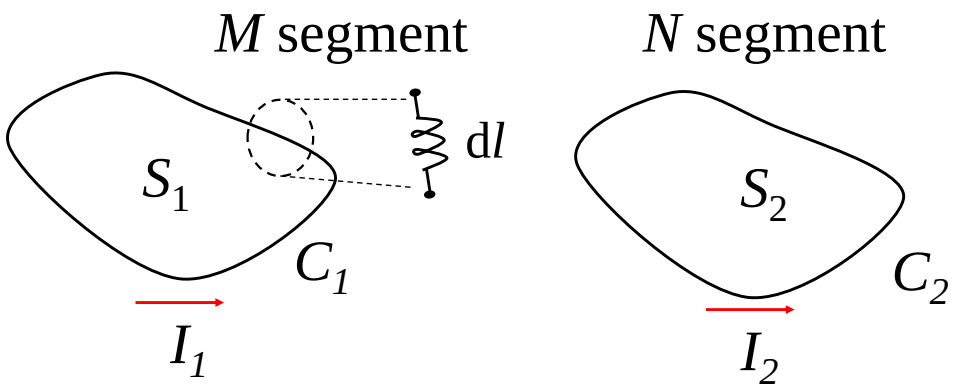


Figure 2.2. A two loop system. The first loop is segmented into *M* pieces, and the second loop is segmented into *N* pieces.

$$L = \frac{1}{I}\sum_{i=1}^{M}\int_{l_i}\vec{A}\cdot d\vec{l} = \sum_{i=1}^{M}\frac{\int_{l_i}\vec{A}\cdot d\vec{l}}{I} = \sum_{i=1}^{M}L_i \tag{3}$$

The magnetic flux is rewritten as,

$$\Psi_1 = \sum_{i=1}^{M}\int_{l_i}\vec{A}\cdot d\vec{l} \tag{4}$$

The vector potential is expressed as,

$$\begin{aligned}\vec{A} &= \oint_{C_1}\frac{\mu I_1}{4\pi|\vec{r}-\vec{r}\,'|}dl' + \oint_{C_2}\frac{\mu I_2}{4\pi|\vec{r}-\vec{r}\,'|}dl' \\ &= \sum_{j=1}^{M}\frac{\mu I_1}{4\pi}\int_{l_j}\frac{1}{|\vec{r}-\vec{r}\,'|}dl' + \sum_{j=M+1}^{M+N}\frac{\mu I_2}{4\pi}\int_{l_j}\frac{1}{|\vec{r}-\vec{r}\,'|}dl'\end{aligned} \tag{5}$$

Substitute (5) into (4), then the magnetic flux can be written as the summation of the partial inductance of each segment,

$$\begin{aligned}\Psi_1 &= I_1\sum_{i=1}^{M}\sum_{j=1}^{M}\frac{\mu}{4\pi}\int_{l_i}\int_{l_j}\frac{1}{|\vec{r}-\vec{r}\,'|}dl' + I_2\sum_{i=1}^{M}\sum_{j=M+1}^{M+N}\frac{\mu}{4\pi}\int_{l_i}\int_{l_j}\frac{1}{|\vec{r}-\vec{r}\,'|}dl' \\ &= I_1\sum_{i=1}^{M}\sum_{j=1}^{M}Lp_{ij} + I_2\sum_{i=1}^{M}\sum_{j=M+1}^{M+N}Lp_{ij}\end{aligned} \tag{6}$$

where the Lp_{ij} is the partial inductance associated with each segment,

$$Lp_{ij} = \frac{\mu}{4\pi}\int_{l_i}\int_{l_j}\frac{1}{|\vec{r}-\vec{r}\,'|}dl' \tag{7}$$

The physical meaning of the partial inductance Lp_{ij} is the current on segment j, penetrating the loop formed by segment i and the infinity.

2.2. . INDUCTANCE MODEL FOR PPP

The power/ground planes are subdivided into $2N$ cells and $2M$ branches, with conventional orthogonal meshing as shown in Figure 2.3. A partial inductance is then assigned to each mesh cell, indicated by the dashed lines, in either x or y direction. The partial self inductance Lp_{kk} associated with the k^{th} cell, and the partial mutual inductance Lp_{km}, can be calculated analytically by the formula (8) for two parallel thin conductor as shown in Figure 2.4.

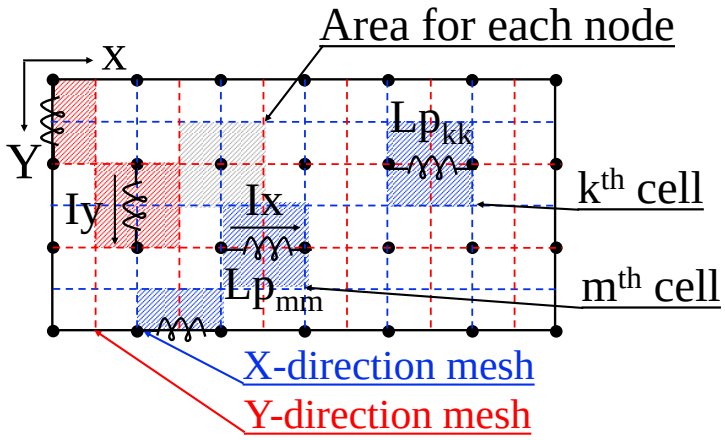


Figure 2.3. Orthogonal mesh for PPP. X-direction mesh and Y-direction mesh are performed separately.

$$Lp_{ij} = \frac{\mu}{4\pi}\frac{1}{W_i W_j}\sum_{k=1}^{4}\sum_{m=1}^{4}(-1)^{m+k}\left[\frac{b_m^2 - C^2}{2}a_k \log\left(a_k + \rho\right)\right.$$
$$\left. + \frac{a_k^2 - C^2}{2}b_m \log\left(b_m + \rho\right) - \frac{1}{6}\left(b_m^2 - 2C^2 + a_k^2\right)\rho - b_m C a_k \tan^{-1}\frac{a_k b_m}{\rho C}\right] \quad (8)$$

$$\rho = \sqrt{a_k^2 + b_m^2 + C^2}$$

$$a_1 = a_{ij} - \frac{f_a}{2} - \frac{s_a}{2},\ a_2 = a_{ij} + \frac{f_a}{2} - \frac{s_a}{2},\ a_3 = a_{ij} + \frac{f_a}{2} + \frac{s_a}{2},\ a_4 = a_{ij} - \frac{f_a}{2} + \frac{s_a}{2}$$

$$b_1 = b_{ij} - \frac{f_b}{2} - \frac{s_b}{2},\ b_2 = b_{ij} + \frac{f_b}{2} - \frac{s_b}{2},\ b_3 = b_{ij} + \frac{f_b}{2} + \frac{s_b}{2},\ b_4 = b_{ij} - \frac{f_b}{2} + \frac{s_b}{2}$$

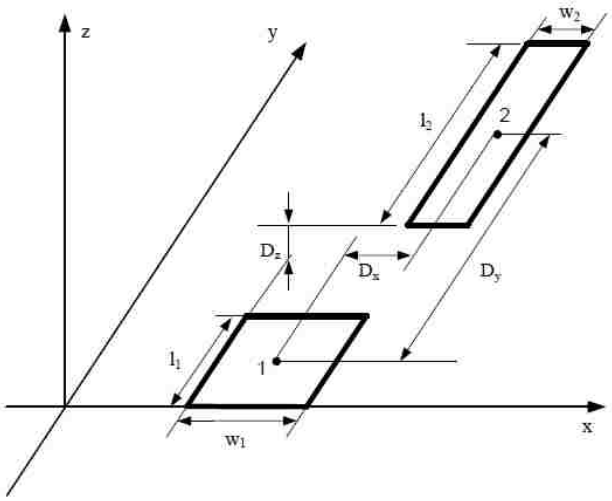


Figure 2.4. The coupling between two parallel rectangular sheets.

Note that the mesh cells on the two planes are exactly the same, which are then combined into one section, as shown in Figure 2.5. The voltage drop on the kth cell due to the current on the mth section I_m, as described by Figure 2.6, is given by (9). The mutual partial inductance of these two sections Ls_{km} is then derived in (10).

$$V_a - V_b = sI_m\left(Lp_{km} - Lp_{km'} + Lp_{k'm'} - Lp_{k'm}\right) \tag{9}$$

$$Ls_{km} = \frac{V_a - V_b}{I_m} = 2\left(Lp_{km} - Lp_{km'}\right) \tag{10}$$

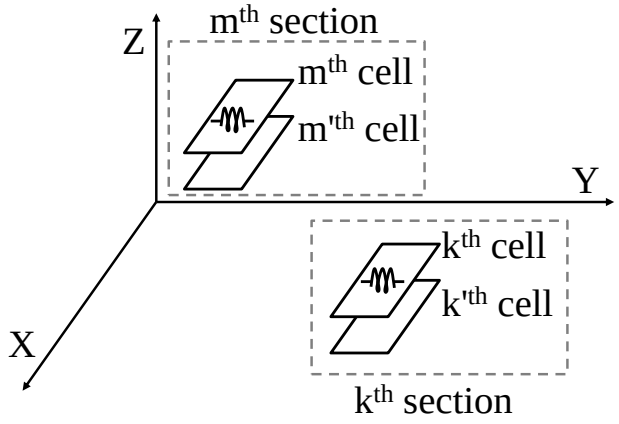


Figure 2.5.Two mesh cells at the same location are combined into one section. This will reduce the total number of cells by half.

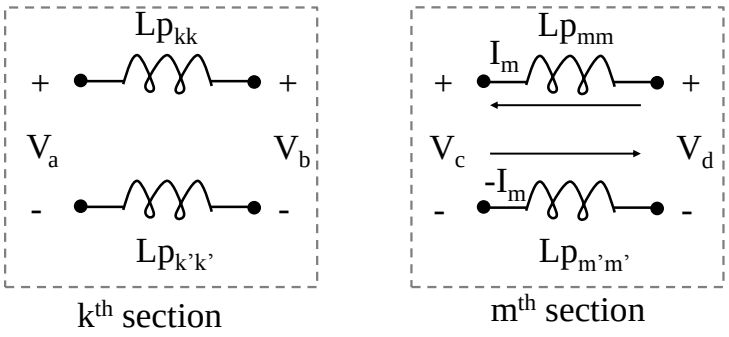


Figure 2.6. The coupling between two sections. The current I_m on the m^{th} section. will cause voltage drop on the k^{th} section.

2.3. CAPACITIVE MODEL FOR PPP

Solving the dynamic electromagnetic problem requires the inclusion of capacitances as well as the inductances. Conventional PEEC requires the calculation of the potential coefficient matrix including all the mutual terms, which is then inversed to get the capacitance matrix. In PPP, however, the capacitive coupling between two sections are even more local than inductive coupling, a simple parallel plate capacitor model is sufficient for this problem. This approach lead to a fast computation of a diagonal capacitance matrix, with a value of $C = \varepsilon A/d$, where A is the area of the nodes, the grey area as shown in Figure 2.3, and d is the plane separation. The sparsity of the capacitance matrix further reduced the run time and memory.

It is important to note that in PPP when calculating the inductances and capacitances, the retardation term is neglected. This is because the coupling between two section decays in the order of r^3, where r is the center to center distance.

The resistive model can also be included if necessary. The resistance Rc of each cell is add in serial to the inductance, using a 1D skin-effect model

$$R_c = 2\frac{\Delta x}{\sigma \Delta y \delta} \tag{11}$$

Here σ is the conductivity of the planes, Δx and Δy are the dimensions for the cell in the perpendicular direction which is parallel to the current directions. It assumes that skin-depth $\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$ is smaller than conductor thickness.

An equivalent circuit of the entire plane can be developed using the modified nodal analysis (MNA) method. By applying Kirchhoff's voltage (KVL) and current laws (KCL), the circuit equation can be written as (12).

$$\begin{pmatrix} \overline{\overline{C}} & \overline{\overline{A}} \\ \overline{\overline{A^T}} & \overline{\overline{L+R}} \end{pmatrix} \begin{pmatrix} \overline{\overline{V}} \\ \overline{I} \end{pmatrix} = \begin{pmatrix} \overline{\overline{I_s}} \\ \overline{0} \end{pmatrix}, \tag{12}$$

Where, $\overline{\overline{A}}$ is the incident matrix which stores all the connection information, $\overline{\overline{I_s}}$ is the external current source, $\overline{\overline{L}}$ is partial inductance matrix, $\overline{\overline{R}}$ is resistance matrix, and $\overline{\overline{C}}$ is capacitance matrix. The current $\overline{I}$ and voltage $\overline{\overline{V}}$ at the notes can be calculated by solving the circuit equations.

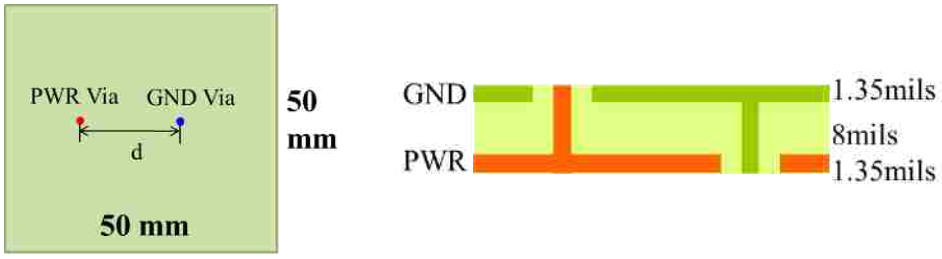
2.4. CURRENT DISTRIBUTION

The current distribution of the power distribution network gives insights into the physics, since the inductance will be collected when the current is impeded. By solving the MNA matrix, the currents on all the branches are obtained. The location and size of the branches are unknown, so the current density can be plotted easily.

A single rectangular cavity formed by a power layer and a power-return layer with a power via and a shorting power-return via is used as the test geometry to illustrate the coupling mechanism in different situations, as shown in Figure 2.7. One of the via is defined as a port and the other via is shorted to both plates of the cavity.

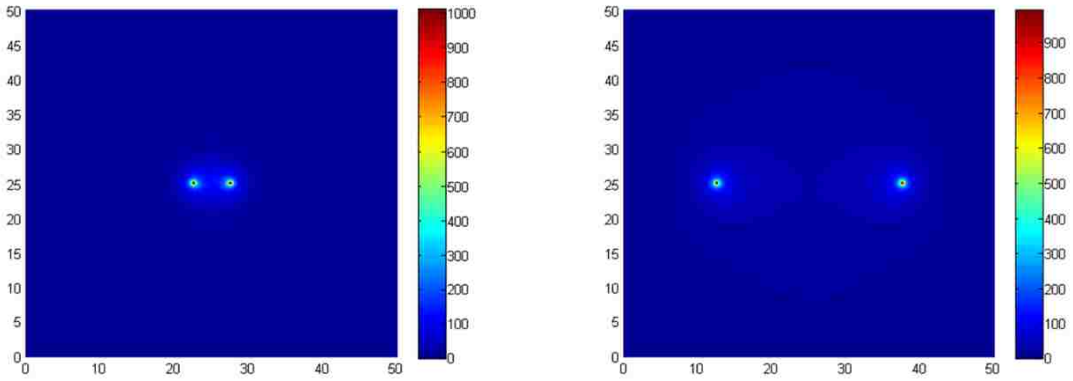
The comparison is designed to show how the distance of the vias influence the coupling between them. The two vias are placed close (d=5mm) in one case, and are placed far away (d=25mm) in another case. The surface current density for the cases are shown in Figure 2.8 **[15]**.

The surface density distribution for the case with d=25mm based on the plane-pair PEEC is calculated and compared with the result based on the cavity model as shown in Figure 2.9.



(a) (b)

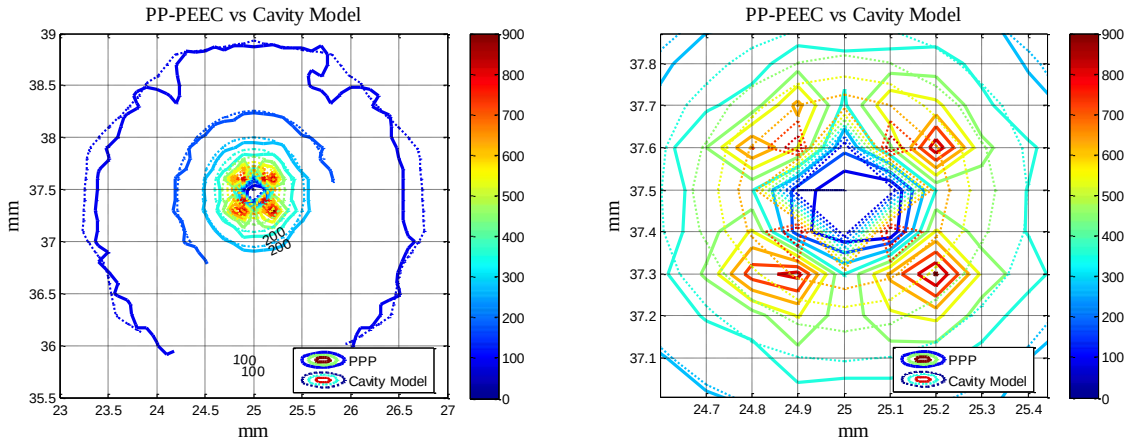
Figure 2.7. A plane-pair cavity with a power via and a shorting ground via placed with distance d, (a) top view of the test case, (b) stack-up of the test case.



(a) (b)

Figure 2.8. Current density plot based on PPP for the geometry shown in Figure 2.7 with different d values, (a) d=5mm, (b) d=25mm.

The results obtained from the two methods are identical, but the magnitude contour from the plane-pair PEEC provides more details than the one from the cavity model in the outside region. For the area near the vias, the contour shapes are different for the two methods, while the magnitudes are similar.



(a) (b)

Figure 2.9. Current density comparison around the vias between cavity model and PP-PEEC for the geometry shown in Figure 2.7 for d=25mm, (a). the via region, (b).zoom-in region for the via center shown in (a).

3. EXTENTION FOR ARNOTARY SHAPED MULTILAYER PCB

The PBC PDN is mainly constituted of the metal layers for the power and ground, which can be solved efficiently by PPP. However, there are a few difficulties when applying the PPP method to real boards. The power and ground layers are usually have different shape, so the assumption of equal current is not valid. Another difficultly is that the power net usually is irregular shape, with cutouts and voids. The solutions are discussed in detail in this Section.

3.1. UNSYMETRICAL POWER/GROUND PAIR

The traditional PEEC method meshes both power and ground planes, which will give very accurate results. But this will takes long time because the total number of unknowns and the coupling between each cell. PPP combines the two cell on the same (x, y) location to one section, reducing total cells and mutual coupling, based on the assumption that the current distribution is symmetric on power/ground pairs.

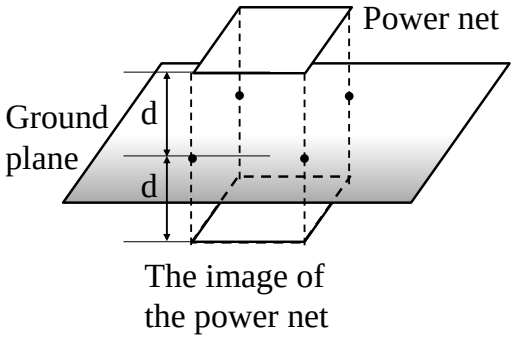


Figure 3.1. The ground plane in PCB is usually larger than the power net, and the separation is usually small. The image theory can be applied in this situation. Replacing the ground plane with an image of the power net will not change the field in the space above the ground plane.

For the unsymmetrical power ground pairs, we want to convert it to a case where the current distribution is symmetric, so that the PPP tricks can be apply. This is feasible, since in PCB, the ground plane usually occupy the entire layer and is much larger than the power net, as shown in Figure 3.1. In resent multi-layer PCBs, the dialectic thickness of these layers is

usually a few mils, much smaller than the size of the of ground planes. This allows the application of the image theory. The ground plane can be replaced by an image of the power net, while the field distribution remains the same.

By applying image theory, the original problem is converted to a symmetrical plane pair. The cell k on the power net and the cell k' on the image net is then combined into one section, as shown in Figure 3.2. Note that the distance between the cells increased to $2d$, while the voltage drop across the section reduced to $2(V_a - V_b)$. The new expression for the partial mutual inductance between two section k and section m becomes (13):

$$Ls_{km} = \frac{V_a - V_b}{2I_m} = Lp_{km} - Lp_{km'} \tag{13}$$

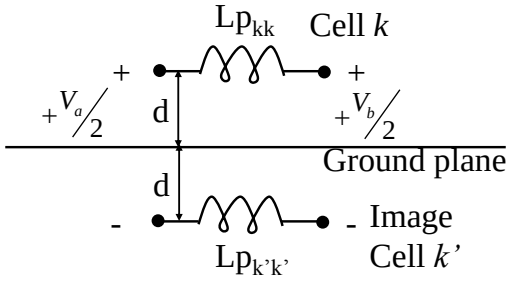


Figure 3.2. By applying the image theory, the cell on the power net and its' image can be combined into one section.

3.2. IRREGULAR SHAPED POWER NET

The PPP use orthogonal mesh, which is difficult to mesh the arbitrary shape directly. In this work, a simple approach base by MNA method is proposed. This is done by meshing the entire working plane and then delete the nodes and branches correspond to the cutouts.

Figure 3.3 represent the mesh for the metal, which is the grey area, and cutouts, which is the white area. The meshing is performed on the entire layer covers both metal and anti-etch area. The total number of nodes is noted as N , and the total number of branches is noted as M . Assuming node 1 to node i are metal, and node $i+1$ to node N are cutouts. The branches with one terminal connected to node $i+1$ to node N are correspond to cutout, marked as branch $k+1$ to branch M . The MNA matrix can be re-written as (4),

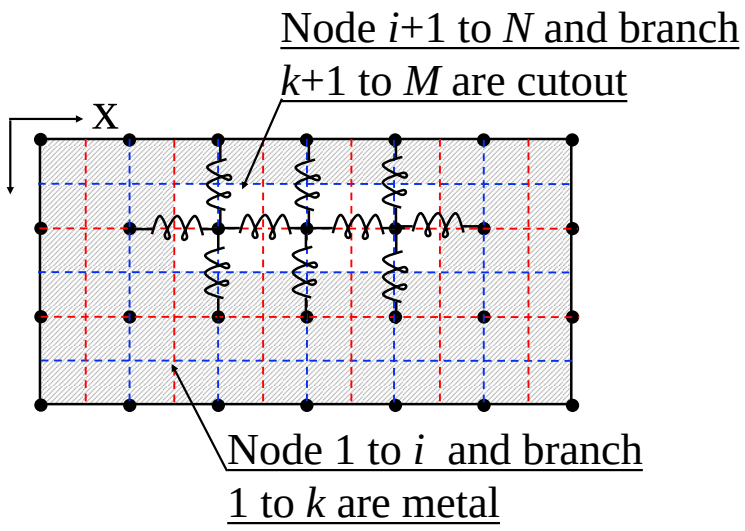


Figure 3.3. The mesh for PPP in the presents of cutout. The grey is metal and the white area is cutout.

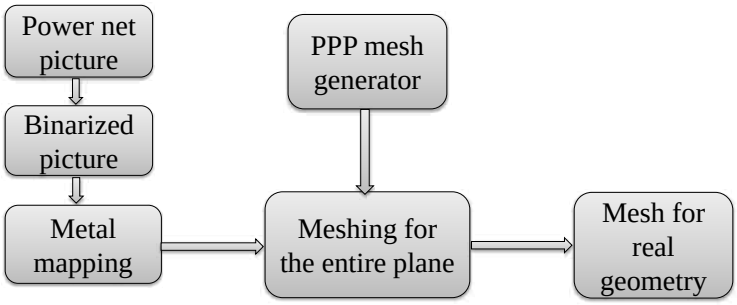
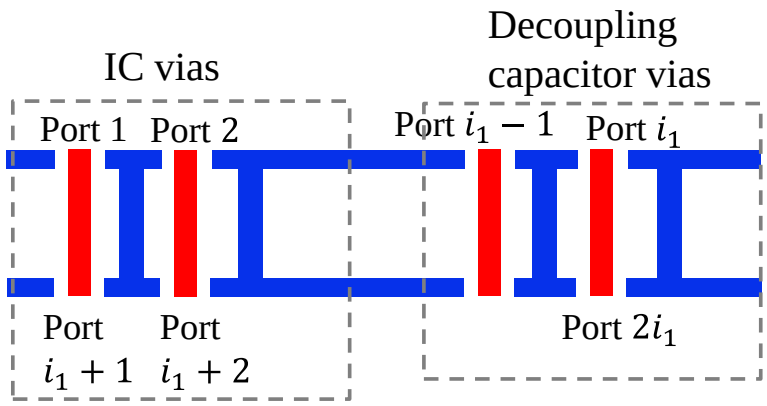


Figure 3.4. The shape of the power net can be read from an image processing procedure. By binarizing the picture, a map can be obtained to distinguish metal and no-metal. The map is used for meshing in the next step.

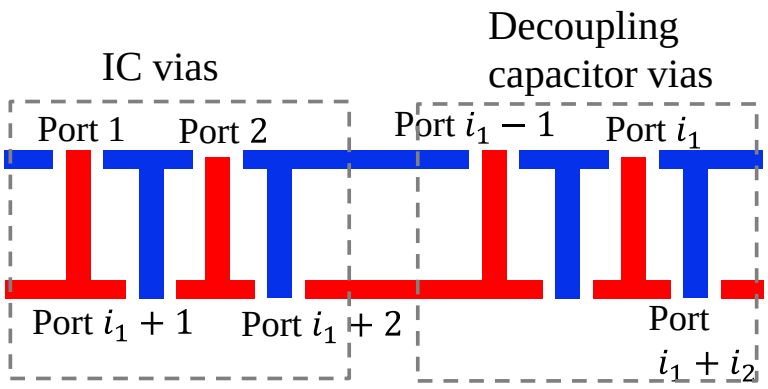
The geometry information can be get by an image process, as shown in Figure 3.4. The input image can be a screen shot from cadence, a commercial tools, with black background and green for copper etch. The image is convert to a 3D matrix with RGB format. A threshold value is chosen to binarized the image, so that the pixels representing metal are set to be 1 and the other pixels are set to be zero. The (x,y) location of each pixel is known, so that a map is obtained. This map is then using in the next step when meshing is being performed.

3.3. MULTIPLE PORTS

When modeling the multi-layer PCB, PPP can be applied to each layer, and then the total PDN response can be obtained by cascading the network parameters. The Figure 3.5 shows the ground/ground pair and power/ground pair. The main difficulty is that PPP is a 2D solver, it cannot distinguish top ports and bottom ports.



(a)



(b)

Figure 3.5. Multiple shorts and multiple ports on top and bottom surfaces. (a) ground/ground pair, the port 1 to i_1 are on top and port i_1 to port $2i_1$ are on bottom. (b) power/ground pair, the port 1 to i_1 are on top and port i_1 to port $i_1 + i_2$ are on bottom.

When modeling the ground/ground pairs, the ports are on the power vias, which are all floating. This is a trouble because the conventional PPP method solves the Z parameters, which in this case is a large number dominated by the displacement current. To avoid that, Y

parameters are used in this work. When solving Y parameters at port i , all the other ports are shorted, so that the symmetrical current assumption is true. Note that there are i_1 ports on top of the power via and i_1 ports on the bottom of the power via. While the PPP is a 2D solver, it cannot distinguish top and bottom ports. This problem is also solved by the symmetrical current assumption. Port i and port $i+i_1$ are two port on the same power via, on top surface and bottom surface respectly. Then I_i is equal to $-I_{i+i1}$. By calculation the Y-parameters for port 1 to port i, the Y-parameters for port i1+1 to port $2i_1$ are also obtained as shown in (14) and (15). The mutual terms are calculated similarly, as shown in (16).

$$Y_{ij} = \left.\frac{I_i}{V_j}\right|_{V_k=0,k\neq j} = \left.\frac{I_{i+i_1}}{V_{j+i_i}}\right|_{V_k=0,k\neq j} = Y_{i+i_1,j+i_1}(i \le i_1,\, j \le i_1) \tag{14}$$

$$Y_{ij} = \left.\frac{I_i}{V_j}\right|_{V_k=0,k\neq j} = -\left.\frac{I_{i-i_1}}{V_j}\right|_{V_k=0,k\neq j} = -Y_{i-i_1,j}(i > i_1,\, j \le i_1) \tag{15}$$

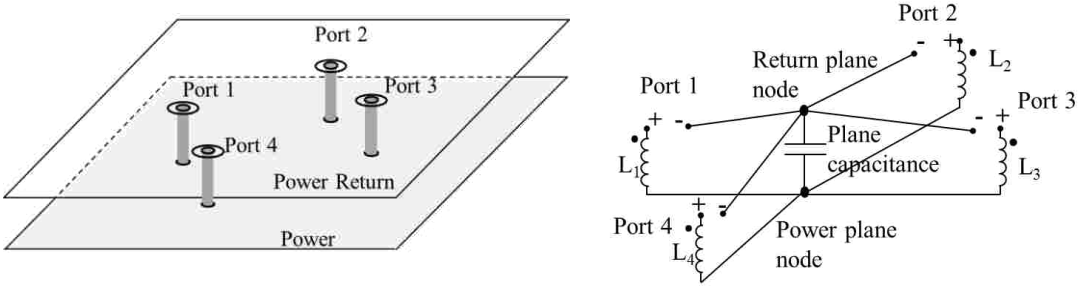
$$Y_{ij} = Y_{ji} \tag{16}$$

When modeling the power/ground pairs, port 1 to port i_1 are on the top surface of the power vias, port i_1+1 to port i_1+i_2 are on the bottom surface of the ground vias. Y-parameters is chosen in this case as well since the Z-parameter is dominated by the displacement current.

4. A HYBRID MODELING METHOD FOR MULTI-LAYER PCB

4.1. THE CAVITY MODEL FORMULATION

The cavity model is a problem of the two dimensional planar circuit since in most PCBs, its vertical size is usually much smaller than its horizontal size, and can thus be treated as electrically small and functional invariant in PI analyses. The cavity model was first proposed and used to solve the problem of finding the radiation patterns and impedance of a patch antenna. Later on the cavity model is applied to calculating both self and mutual inductances associated with PCB vias that are between a pair of parallel plates. The cavity model is derived by solving Maxwell equations by applying PEC boundary conditions at the top and bottom side of the cavity and PMC boundary conditions at the four side walls. The via and the plane around it in the cavity is represented as an inductor, as shown in Figure 4.1. The cavity capacitance is calculated as plane-pair capacitance. For multi-layered PCB PDN geometries, the circuit modelling rule can be extended to include the vias and cavities in the physics-based circuit model [4][15].



(a) (b)

Figure 4.1. (a) An open plane-pair cavity with four vias; (b). The equivalent circuit mode based on the cavity model .

The impedance looking into a via i in a rectangular cavity when the source is placed at via j can be written as,

$$Z_{ij} = \frac{1}{j\omega C_p} + j\omega L_{ij}(\omega) \tag{17}$$

where, C_p is a parallel plate capacitance for the first cavity mode with (m, n) = (0, 0) given by

$$C_p = \varepsilon \frac{ab}{d} \tag{18}$$

and the inductance is found using,

$$L_{ij} = \frac{\mu d}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{(2-\delta_m)(2-\delta_n)}{k_{mn}^2 - k^2} g_{mni} g_{mnj} \Bigg|_{(m,n)\neq(0,0)} \tag{19}$$

where,

$$k_{mn}^2 = \left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2 \quad , \quad k^2 = \omega^2 \mu\varepsilon \quad \text{,and}$$
$$g_{mni} = \cos\left(\frac{m\pi x_i}{a}\right)\cos\left(\frac{m\pi y_i}{b}\right)\operatorname{sinc}\left(\frac{m\pi W_{xi}}{2a}\right)\operatorname{sinc}\left(\frac{m\pi W_{yi}}{2b}\right). \tag{20}$$

Here, a, b, and d: Dimensions of cavity along the x, y, and z directions, respectively,

(x_i,y_i) : Location of the i^{th} port,

W_{xi}, and $W_{yi,}$: i^{th} Port dimensions along the x and y directions, respectively,

m, and n : Cavity mode indices in the x and y directions, respectively,

μ : permeability of the dielectric layer, and

ε : permittivity of the dielectric layer.

δ_m and δ_n : the Keronechker delta function.

4.2. CONNECTING POWER CAVITIES AND GND CAVITIES

While the total inductance of a PDN gives some idea about the quality of that PDN, a more rigorous and common way to analyze the performance of a PDN is to compare its input impedance with the target impedance. Since an alternating current has the tendency to flow only on the surface of a PEC conductor due to skin effect, so two adjacent cavities are actually separated by metal layers and connected through voids and cutouts. Based on this concept, herein two adjacent cavities are connected through internal ports which are set over via antipads as shown in Figure 4.2.

For a ground cavity, internal ports should be set at power vias on both the top and bottom planes. And for a power cavity, internals ports should be set at power vias on one plane and ground vias on the other. Then network parameters of the ground cavity can be extracted from the cavity model. And network parameters of the power cavity can be extracted from PPP with the circuit models mentioned in the Section 3 of this thesis. With those network

parameters of different cavities, the input impedance of a PCB PDN can thus be extracted by cascading all the network parameters through their common internal ports. External components such as decoupling capacitors and chip packages can also be connected through external ports as shown in Figure 4.2.

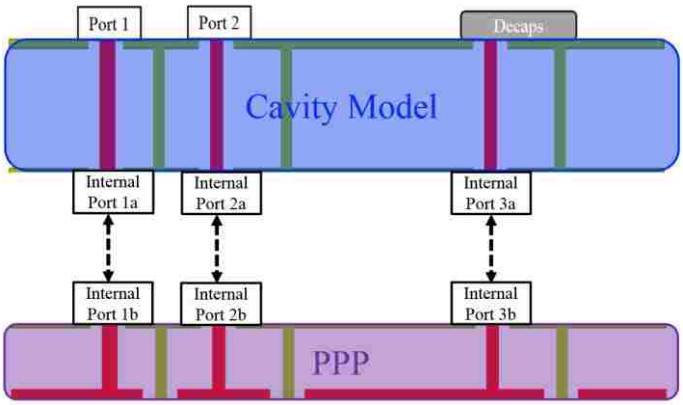
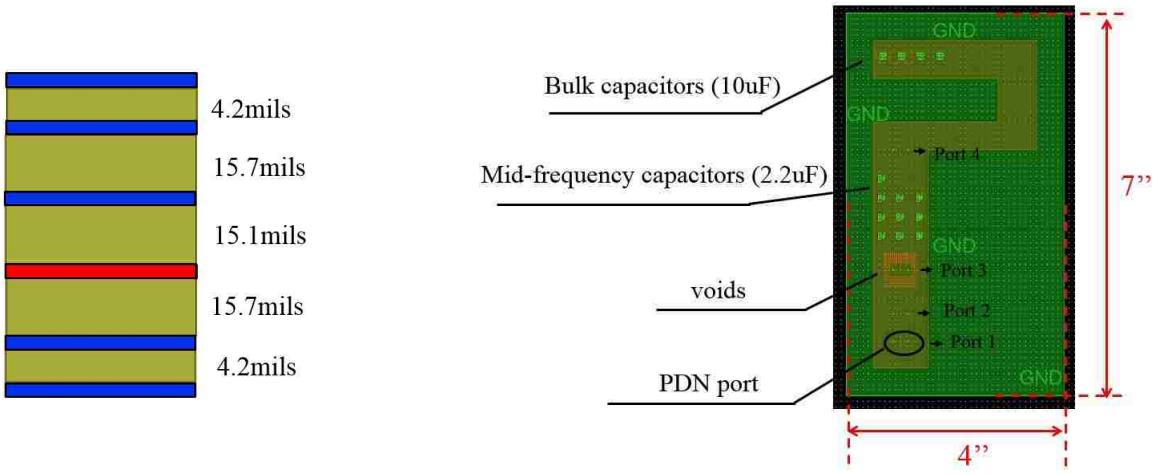


Figure 4.2. Ground cavities and power cavities are connected through internal ports.

4.3. MEASUREMENT CORRELATION

A test vehicle is designed and the input impedance of that test vehicle is measured to validate the hybrid method of modeling multi-layer PCB PDNs by connecting different cavities through internal via ports. The stack-up of the test vehicle is shown in Figure 4.3. As can be seen, the test vehicle comprises 6 metal layers and 5 cavities in total. 1 oz copper is used for metal layers and the power layer is colored in red and is the fourth layer from top to bottom.

The size of the ground planes is 4 inch by 7 inch, as shown in Figure 4.3. Power net area fill is colored in red, which looks like a letter P. Two types of decoupling capacitors are used in the test vehicle: 10 capacitors with 2.2uF capacitance and 4 capacitor with 10uF capacitance. There are in total 4 different port locations for the input impedance measurement and in this paper only Port 2 is used. There is a void grid at Port 3, which is used to represent the dense antipads under IC regions. Also for the plated-through hole vias used in this test vehicle, the finished hole size is 15mils and their antipad diameter is 42mils.



(a) (b)

Figure 4.3. (a) Test vehicle stack-up. (b). Test vehicle top view.

There are four ground vias connected to a circular ground pin and one power via connected to the power pin. The input impedance of the PCB PDN is then the impedance by looking into the test vehicle from those power and ground pins. To measure the input impedance of the test PCB PDN, a two-port transfer impedance measurement approach is employed herein [16]. Since PDN usually has a very low input impedance, $S_{11} \approx 1$. Thus conventional one-port impedance measurement using S_{11} requires well-characterized and precise test fixtures for locating reference plane and accurate phase information, which is difficult or expensive to achieve.

Four 10uF 0805 decoupling capacitors are soldered at the top and ten 2.2uF 0805 de-coupling capacitors are soldered in the middle. There are one power via and one ground via associated with each decoupling capacitor and one power via and four ground vias associated with each PDN port. So in total 48 internal ports are needed to connect the power cavities and ground cavities. Herein Port 2 is used to perform the two port PDN input impedance measurement. Besides the measurement, simulations to get the input impedance looking into Port 2 are also done with Cadence Sigrity tools.

The input impedance results looking into Port 2 from measurements, simulations and calculations based on the hybrid method mentioned are compared in Figure 4.4. The results from calculations based on PPP and the cavity model are shown to compare favorably with the results from measurements and simulations. The total inductance results are 941pH for the calculation and 972pH for measurement. It can be seen that the hybrid approach based

on PPP and the cavity model can capture the total inductance of the test PCB PDN accurately with only around 3% difference from measurements and around 7.5% difference from simulations. Herein 48 vias are used in the test vehicle which are related to 48 internal ports for the connections between different cavities. More complicated PCB PDNs can be modelled using the same hybrid approach based on PPP and the cavity model by modifying the PPP circuit and increase internal ports.

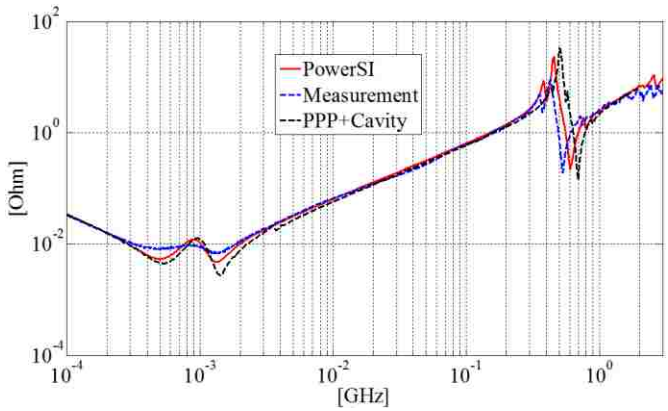


Figure 4.4. Input impedance results comparison between calculations, simulations and measurements.

A mismatch between the calculations and the measurements which can be seen from Figure 4.4 is the resonance happens at around 500M. This resonance is due to the parallel-plate parasitic capacitance of the power net area fills and the ground planes. After that resonance, current would mostly go as displacement current from the power net area fills to the nearby ground planes instead of travelling all the way to decoupling capacitors which have larger parasitic inductance. The results show the resonance frequency calculated from PPP and the cavity model is higher than that from measurements or simulations, which means the parasitic parallel-plate capacitance from the hybrid approach is smaller since they have almost the same total inductance. This could be due to the absence of the fringing capacitance in PPP and the cavity model. However for most PCB PDN designs, this resonance is of little concern because usually chip packages will provide extra decoupling capacitance which is larger than the parasitic parallel-plate capacitance. So that resonance generally cannot be observed in a system-level PDN input impedance curve with chip packages included.

5. THE INDUCTANCE PHYSICS FOR THE LPLANE WITH VOIDS

A low impedance PDN is essential for the functionality of high speed printed circuit boards. A pre-layout impedance calculation can avoid time consuming changes on the design during post layout stage. Design curves for inductance estimation are convenient to use in pre-layout stage. However, the high density voids on the power plane, which is caused by the anti-pads, are not considered in those design curves.

The cavity model is a widely used and validated tool for PDN calculations. However is cannot model the voids on the power net, which will result in an underestimation for the inductance value. It is important to understand how much the void will affect the inductance, when using cavity model to approximately calculate the power net with voids.

This Section discussed the extra inductance caused by the anti-pads, in two common situations.

5.1. THE VOID GRIDS ON THE POWER NET

An effective pre-layout methodology is proposed in early work [], where a family of inductance for rectangular shaped power net are provided. But the void region under the IC caused by the anti-pads are not taken into account. This Section discussed about the effect anti-pads on plane inductance, under two different situations as shown in Figure 5.1, which is very common in real designs.

(a) (b)

Figure 5.1. Test power net area fill geometries. (a) The power via is inside the anti-pad region (11x11 anti-pad region for example). (b) The anti-pad region is between power and ground vias (11x11 anti-pad region for example).

Case A reflects the current path from decoupling capacitors thru the anti-pad region to the power net BGAs which are in the middle of the CPU/FPGA BGA grids. Case B reflects the current path from decaps to the memory module. The anti-pad regions are between the power vias and the decap.

The first model is a 50mm x 50mm square board, with 4 decoupling capacitor located 10mm away from the IC power Via, which is in the center of the circle. The second model is a 50mm x 30mm rectangular board. The power via and the ground via are on the center line of the board with a separation 2D. The anti-pad region is between the power via and the ground via. For both models, the anti-pad region consists of round anti-pads, with a radius of 0.25mm and 1mm pitch size.

It is expected that the inductance will increase because the void will restrict the current flow. This increase is a function of the plane separation and the number of voids, which is investigated in detail in the following Section.

5.2. CORRELATION WITH CST

PPP is used to do the calculations. To start with, a correction with full wave simulation is desired. For validation, PPP is compared to the CST microwave studio, for the case where h=0.7mm, D=12.5mm, anti-pad region size=11x11 for the first model, and 7x7 for the second model. The results shown in Table 5.1 shows good correlation between PPP and CST. Note that PPP is a 2D solver, which requires less mesh than the 3D full wave simulation, and runs faster.

Table 5.1. Correlation between PPP and CST.

Situation	**Cell Number/ Unknown**		**Plane Pair Inductance**		**Difference**	**Computation Time**	
	CST	**PPP**	**CST**	**PPP**		**CST**	**PPP**
Situation A	185254	20815	622 pH	611 pH	1.8%	1003s	292s
Situation B	209385	17955	1547 pH	1484 pH	4.1%	1103s	151s

5.3. THE EFFECT OF VOIDS ON LPLANE

With PPP calculation, we want to study the relationship between plane inductance and the geometry parameters including plane separation *h*, anti-pad region size and via-anti-pad-region distance *D*.

The thickness of a usual stack up for PCB is from 2mil to 40mil thus the plane separation *h* is set to be [0.05, 0.1, 0.2, 0.3, 0.5, 0.7, 0.9]mm. Three different sizes of anti-pad region are investigated, which are 7x7, 11x11, and 15x15. The inductance as well as the increase ratio in (17) is studied.

$$\text{Increase Ratio\%} = \frac{L_{void} - L_{plane}}{L_{plane}} \times 100\% \tag{21}$$

The results are shown in Figure 5.2. As expected, the inductance increases as the plane separation increase. The anti-pad grid also causes an additional inductance increase, especially when h is small, as illustrated in Figure 5.3. For both case A and case B, the increase ratio is higher as the stack-up become more compact. In case A the effect of the voids can be as significant as 40% while in case B the effect is below 10%.

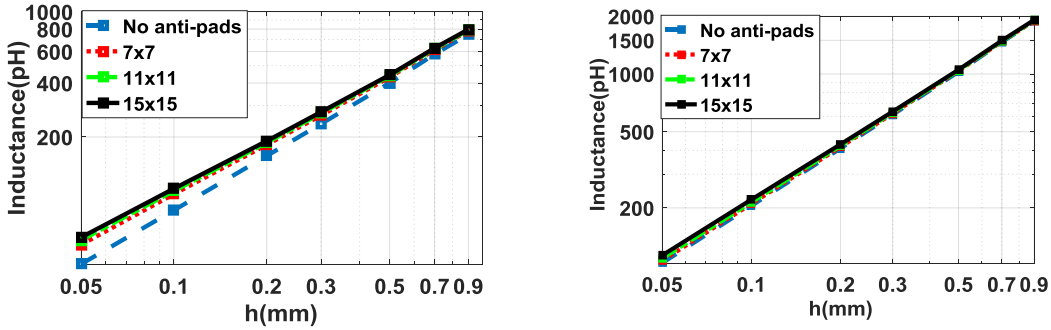


Figure 5.2. Inductance value as a function of h. (a) For the geometry shown in Figure 5.1(a). (b) For geometry shown in Figure 5.1(b).

Note that from cavity model theory, the inductance of a rectangular plane pair is linearly proportional to the plane separation. However, if there are voids on the plane then this linear relationship is not true.

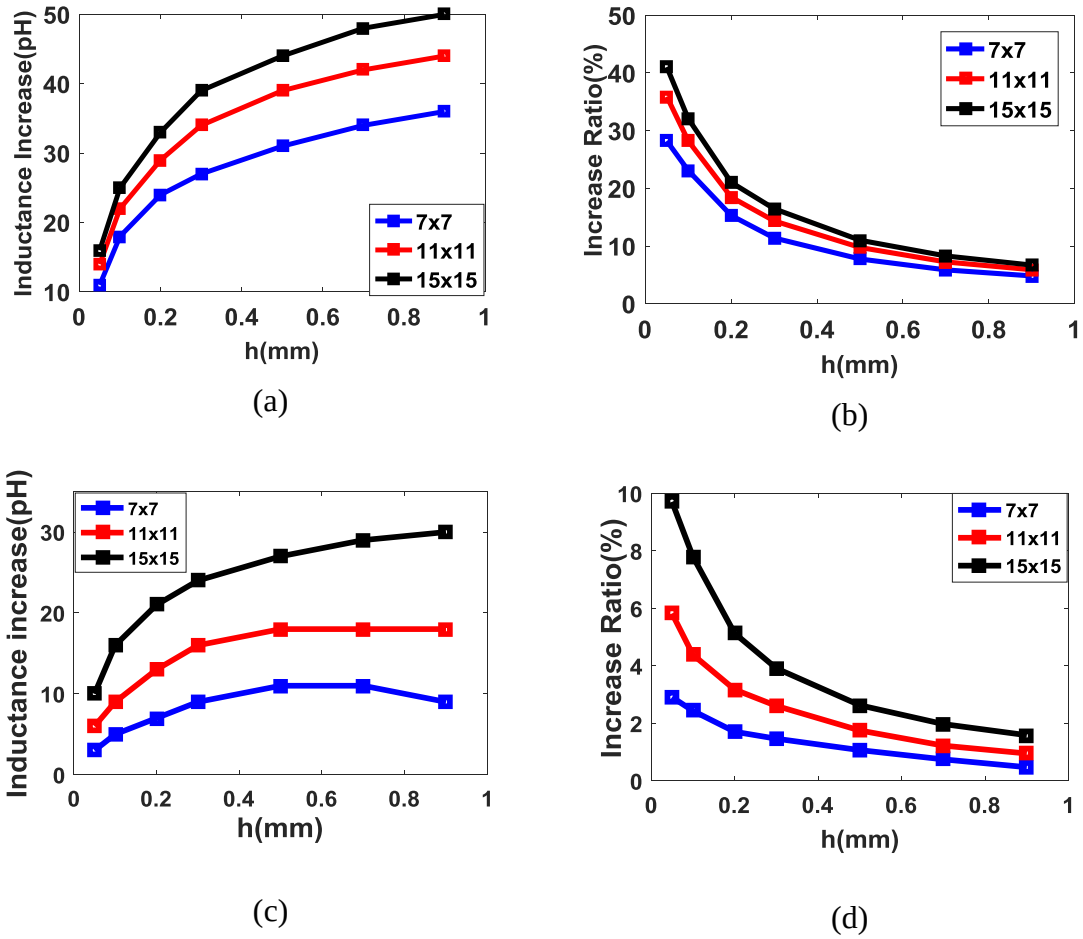


Figure 5.3. (a) Inductance increase in absolute value for case A. (b) The inductance increase ratio for case A. (c) Inductance increase in absolute value for case B. (d) The inductance increase ratio for case B.

5.4. MEASUREMNT CORRELATION

The PPP modeling method is validated on a test PCB, where there are two layers, with rectangular voids on the top layer. The PCB layout is shown in Figure 5.4, with 2 vias, one for port and the other one for short.

Two port measurement in Figure 5.5 is a validated method to measure a low inductance, which is suitable in this case [16]. Two probes are soldered on the same via, and then connected to the VNA ports, as shown in Figure 6.5. Then the input impedance is calculated from:

$$Z_{DUT} = 25\Omega \times S_{21} \tag{22}$$

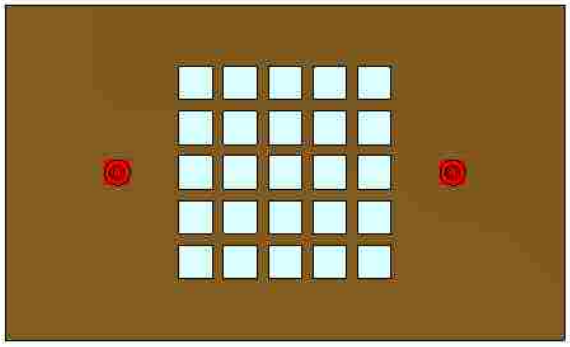
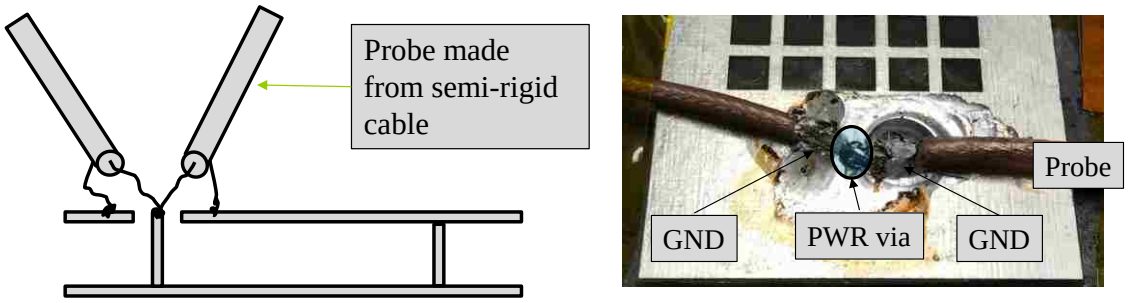


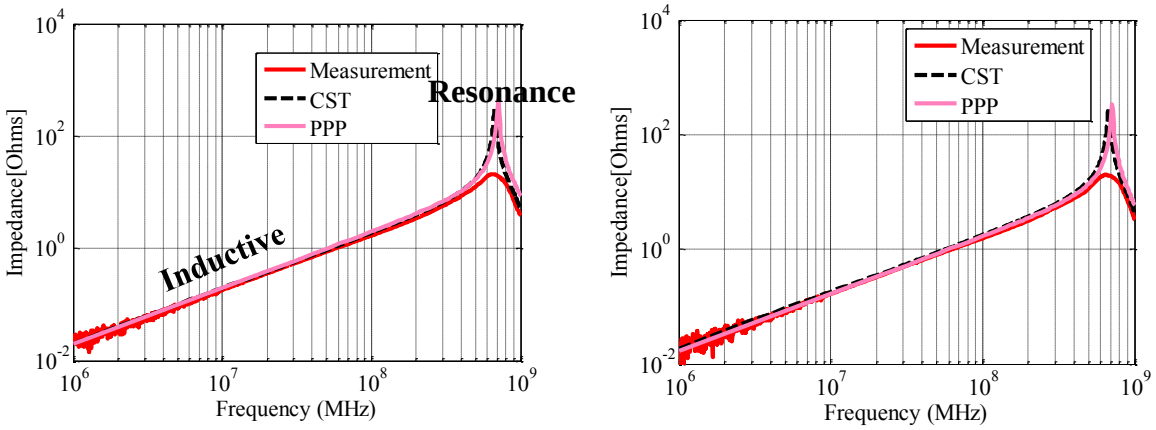
Figure 5.4. PCB layout. There are two vias, one for the port and the other one is shorted.

The result in Table 5.2 and Figure 5.6 shows good correlation between PPP and measurement. The difference is with 10%.



(a) (b)

Figure 5.5. (a) Schematic of the two port measurement. (b) Two semi-rigid probes are soldered in the PCB.



(a) (b)

Figure 5.6. (a) Without voids. (b) With voids.

Table 5.2. Inductance comparison between PPP, CST and measurement.

	Measurement	**CST**	**PPP**
No voids	2.48nH	2.81nH	2.69nH
With voids	2.81nH	3.03nH	3.13nH

6. APPLICATION IN A COMMERCIAL PACKAGE

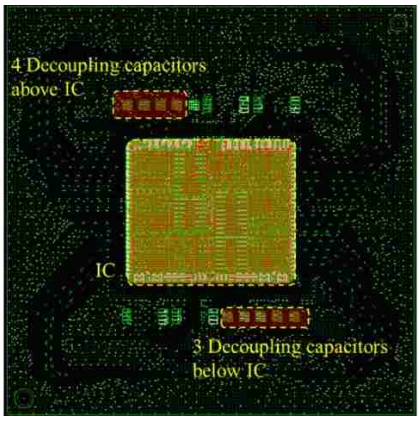
Recent FPGAs and CPUs consume significant power, and a low impedance power distribution network (PDN) is critical to get a robust performance. The decoupling capacitors in package usually provide charge for mid frequency switching currents, from tens of MHz to a few hundreds of MHz. The effectiveness of these capacitors are limited by the inductance associated with the current loop. Although commercial tools can estimate the PDN impedance, they do not generate a physics-based circuit which provides insight of where the inductance collects. In this short paper, a plane pair partial element equivalent circuit (PPP) method is applied to extract the inductance of the power layers on package. The method is validated by comparing with the cavity model and a commercial tool. The extracted inductance can be used to generate a physics based circuit model.

6.1. THE POWER NET AREA FILL OF A COMMERCIAL PACKAGE

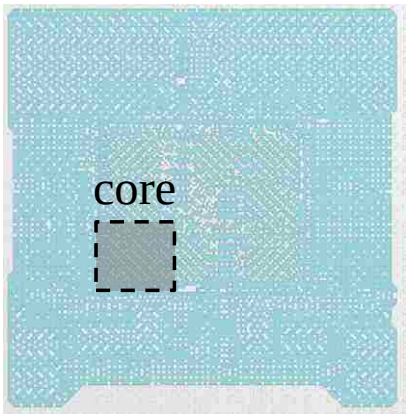
The PPP method is applied to the package of a computing system, with 7 on package decoupling capacitors, as shown in Figure 6.1.

First of all, the details of the target PKG PDN needs to be determined for accurate modeling. We are looking here at a single power domain of a chip with the GND as reference. The target PKG PDN includes 2 layers, FC1 the power layer and FC2 the GND layer. Due to the geometry complexity, if the simulators are based on 3D structures, ports cannot be assigned to all possible decoupling capacitor positions in a reasonable amount of time so the simulation needs to be run again if the number or the position of decoupling capacitors changes.

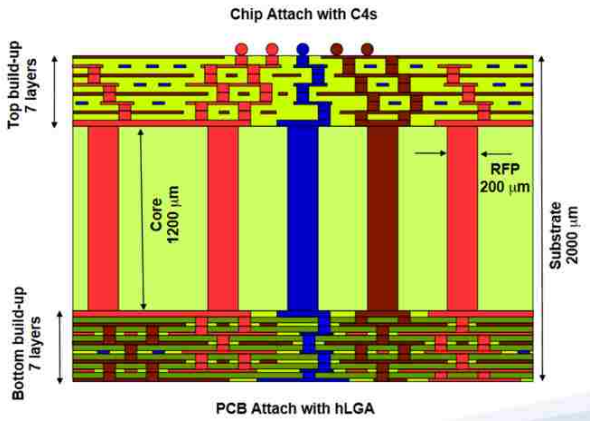
By applying PPP, the inductance of the power net can be extracted efficiently, without the need to trick the tools. Engineers usually want to know if they move the capacitors how the inductance will change. This will usually require changing the layout in the commercial software and do the simulation back and forth a few times. By applying PPP, layout change is not needed.



(a)



(b)



(c)

Figure 6.1. Target package PDN: (a) Top view of package PDN. IC is placed on the center of PKG while 7 surface mount decoupling capacitors are mounted on PKG around IC. (b) Top view of the power net to be modeled for a single core. 9 ports are put in the core area. (c) The stack-up view. The Target power net is located in the core layer FC1.

6.2. MODELING THE PLANE INDUCTANCE

L_{plane} is calculated for the cavity between layers FC1 and FC2. As shown in Figure 6.2, bottom-side of ground vias are not connected to any layer and only power vias are considered in cavity model to calculate L_{plane}. However, the vias are still more than one thousand which take long time to calculate. Instead of modeling all the vias, a 3 by 3 port matrix is being applied to the core area, as shown in Figure 6.3.

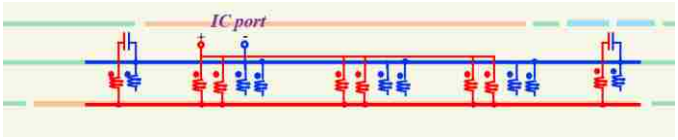
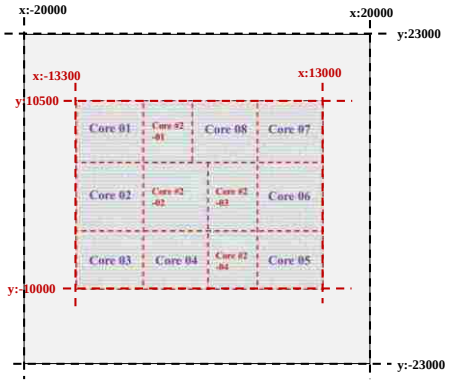
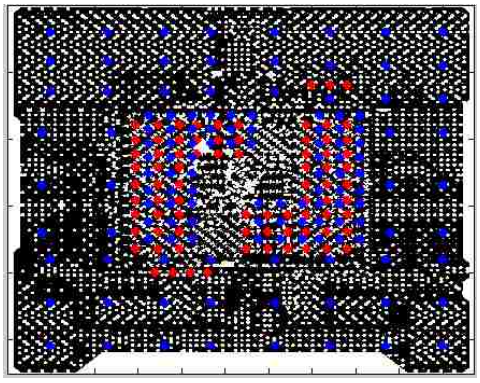


Figure 6.2. Equivalent circuit to get Lplane. Ground vias are floating and do not need to be considered.



(a)



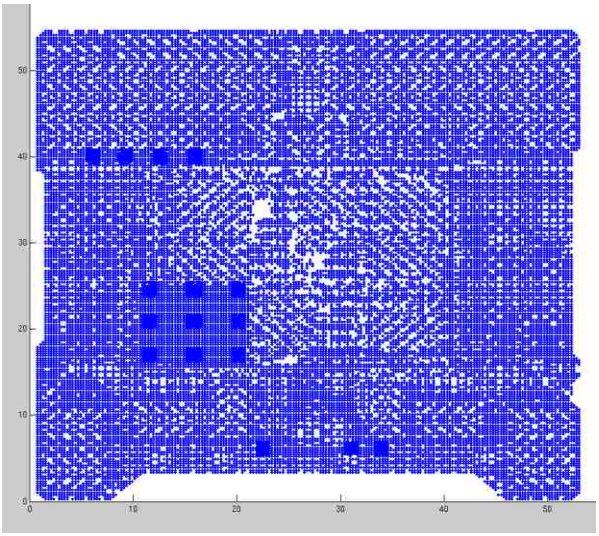
(b)

Figure 6.3. Core division. (a) The entire plane are subdivide into 12 cores. (b) A 3 by 3 port matrix is applied to each core.

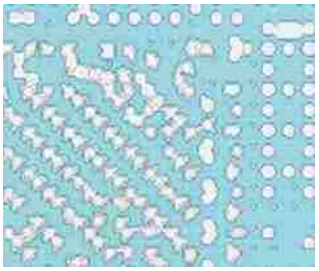
6.3. MESHES

PPP first divide the entire rectangular plate into electrical small meshes, the mesh nodes representing the voids and cutouts is then deleted. Dense meshes are added to the via location, as shown in Figure 6.4. The total number of nodes and branches are 149,040.

It's important to note that the Lplane will be increased significantly by the voids in the solid plane, which is caused by the anti-pads of some the vias. So it is important to have enough meshes to capture the voids. The effect of voids will be discussed in detail in later Sections.



(a)



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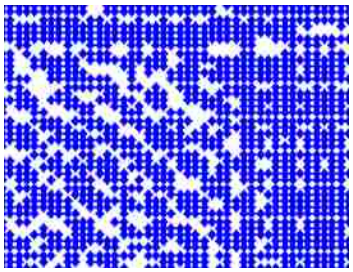


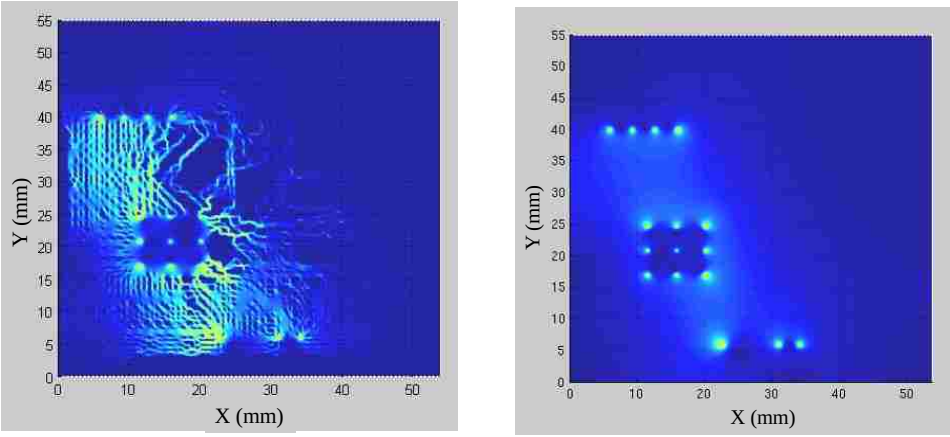
(c)

Figure 6.4. Meshes for the power net. (a) The meshes after deleting the nodes for cutouts and voids. (b) The shape of the power net in the core area, filled with voids which are caused by the anti-pads. (c) The corresponding meshes in PPP which captures all the voids.

6.4. MODELING RESULTS

First PPP is compared with cavity model. Since cavity model assumes the power net to be a solid plane, this comparison is done without all the voids and cutout. Then PPP is compared with a commercial tool. Note that the PPP extract inductance directly from an inductive circuit, while the commercial tool extract inductance indirectly from an impedance curve. The results shown in Table 6.1 indicate that PPP agrees with the cavity model method and the commercial tool within 10% difference.

Figure 6.5 shows the current distribution from one of the cores to the 7 decoupling capacitors. It is clear to see that the current is constrained by the voids, which are the anti-pads. So it is not surprising to see that the model with void have 37.1pH of inductance, twice as much as 18.9pH, the one without modeling the voids. This shows the importance of modeling the real shape of a package power. Tools which cannot model the voids and cutouts, such as the cavity model, will under estimate the inductance.



(a) (b)

Figure 6.5. The current distribution from one of the cores to the 7 decoupling capacitors, (a) for the real package power net; (b) for a hypothetical solid rectangular power plane.

Table 6.1. Inductance comparison between PPP, the cavity model and a commercial tool.

	W/O voids	With voids
PPP	18.9pH	37.1pH
Commercial tool	N/A	39pH
Cavity model	19.9pH	N/A

7. PPP MODELING FOR L_{ABOVE}

7.1. L_{ABOVE} MODELS

As discussed in Section 1, the equivalent inductance for PCB PDN can be separated into L_{IC}. L_{plane} L_{decap} and L_{above}. L_{above} is the equivalent inductance from the decap to the PCB above the top GND plane when the decaps are shorted, including the trace inductance, and pad and via inductances, as shown in Figure 7.1. In industry people often use the ESL value provided by capacitor vendors for PDN simulation. However, the ESL value are measured in a certain PCB environment, and may not suitable to be used directly because the it is highly dependent on the local coupling between the pads, traces, vias and ground plane[18][19].

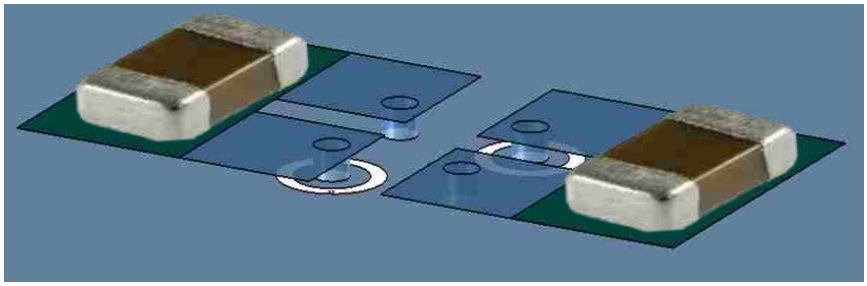


Figure 7.1. The L_{above} is highly depend on the layout. A single ESL value is not an accurate way to model L_{above}, because the value changes in different layout.

Instead of using the ESL value provided by vendors, a new modeling approach based on plane-pair PEEC is proposed in this thesis. The assumption is that in MHz frequency range, the current mainly flows on the bottom surface of the decap, so that the decap can be replaced by a PEC sheet across the pads, as shown in Figure 7.2.

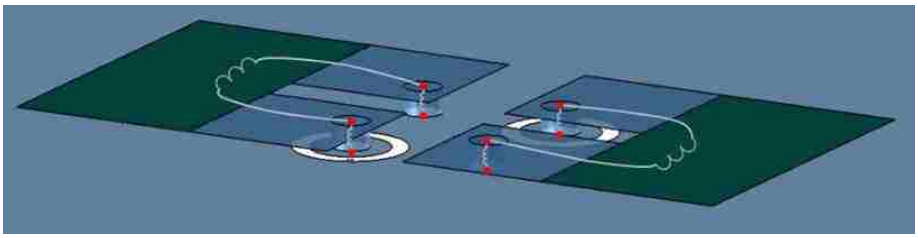
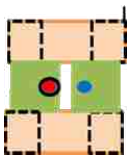
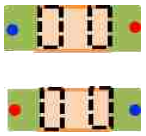
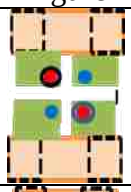
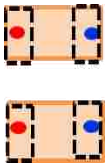
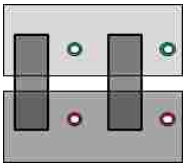
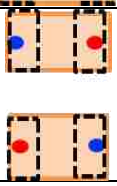
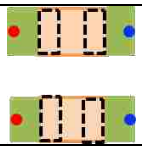
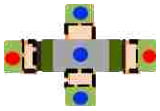
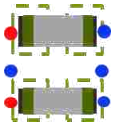


Figure 7.2. The simplified L_{above} model with traces and pads. This two layer geometry can be effectively calculated using PPP method.

7.2. L_{ABOVE} DESIGN SPACE

Nine decap placement patterns are proposed in [18][19], which are widely used in industry, as shown in Table 7.1. For every decap placement pattern, three different sizes 0805/0603/0402 of the decap need to be calculated. All these designs can be calculated by PPP, since they are all 2-layer planar structures.

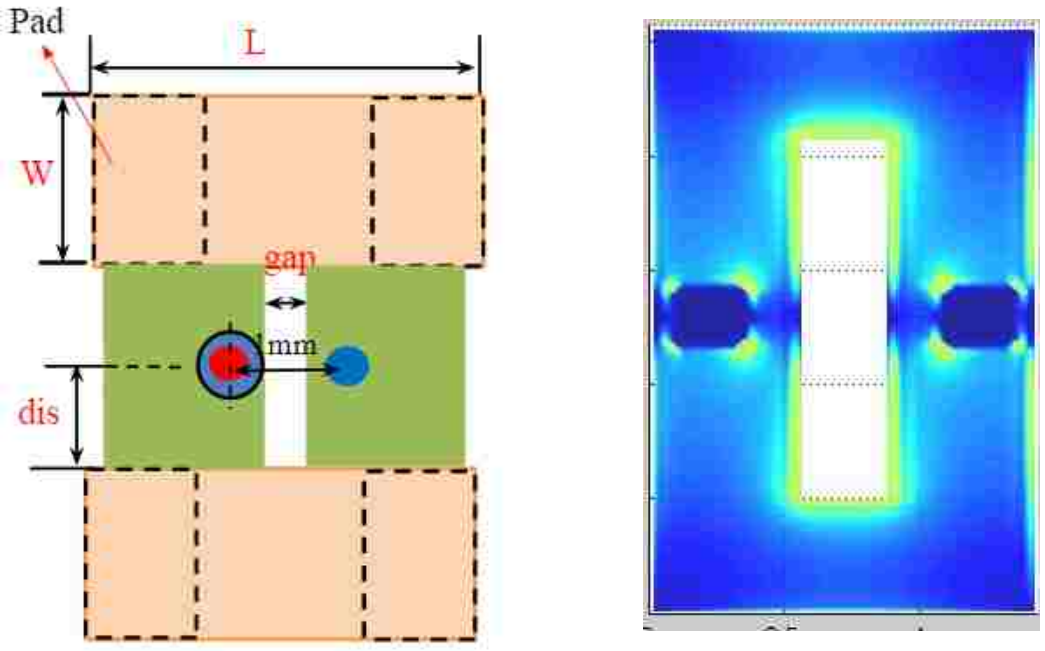
Table 7.1. Decoupling capacitor of sizes 0805/0603/0402 for L_{above} design space.

#	Name	Figure	#	Name	Figure	#	Name	Figure
1	Shared via		2	Alternating		3	Doublet	
4	Via in pad aligned		5	Shared pad		6	Via in pad alternaing	
7	Aligned		8	3-terminal decap		9	Multi-via	

7.3. NUMERIAL EXAMPLES

The shared via design is chosen as an example here for validation, as shown in Figure 7.3. (a) Shared via design. Inside the black dashed lines are the decoupling capacitors, and they are shorted with a metal plate between pads. (b) Current distribution calculated by PPP.. The PPP calculation results are compared with CST microwave studio, for 3 package size: 0402, 0603 and 0805. The dimensions for the corresponding designs are listed in Table 7.2. The distance between top layer and ground layer h is 5, 10, 15, 20, 25 and 30 mils. The calculated inductances are listed in Table 7.3. The difference is within 10%, as shown in Figure 7.4.

The calculation time is only around 1 minute for PPP while 30 minutes for CST. Therefore, using PPP is more time-saving than commercial tool. This algorism is being implemented in FEMAS PDN tool. More details can be found in Section 7 in this thesis.



(a) (b)

Figure 7.3. (a) Shared via design. Inside the black dashed lines are the decoupling capacitors, and they are shorted with a metal plate between pads. (b) Current distribution calculated by PPP.

Table 7.2. Dimensions for shared via layout with 0805/0603/0402 sizes.

	0402	**0603**	**0805**
L (mil)	56	78	100
W (mil)	20	30	50
gap (mil)	18	18	11.8
dis (mil)	14	20	31.5
pitch (mil)	39	39	39
Via Diameter (mil)	10	10	10

Table 7.3. Numerical results for shared via layout with 0805/0603/0402 sizes.

h (mil)	PPP(pH)			CST (pH)		
	0402	0603	0805	0402	0603	0805
5	153.2	161.8	173.67	165.6	174.3	182.4
10	273.3	290.1	311	265	279	292.3
15	380.1	401.6	427.9	358.2	374.3	389.1
20	485.1	509.3	538.59	452.1	468.8	483.6
25	589.7	615.5	637.74	547.7	564.5	578.8
30	694.2	721.2	744.07	645	661.8	675.2

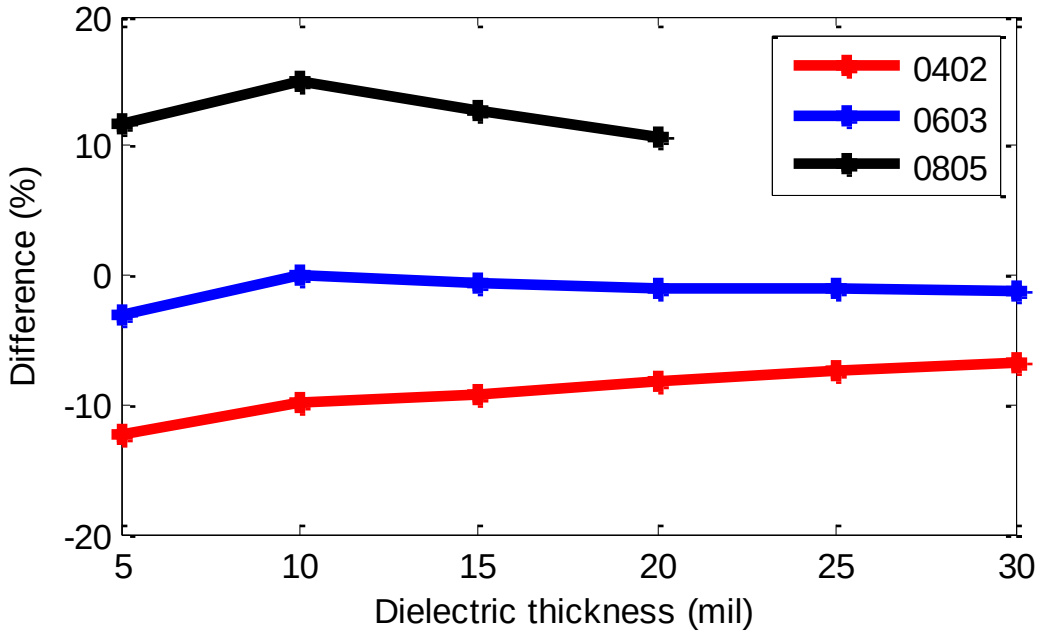


Figure 7.4. The difference between PPP and CST.

8. TOOL DEVELOPMENT

Fast EM Analysis Suite (FEMAS) is a software developed by EMCLAB, MST, in cooperation with industries partners. A toolbox, i.e. the PDN tool, is being developed in FEMAS to provide a fast and accurate solution for PCB PDN analysis. This tool is based on the hybrid method proposed in Section 4 and the Labove modeling algorism proposed in Section 7.

Figure 8.1 shows the GUI for the PDN tool. The main contribution for this thesis is the PPP calculation c++ code embedded in the tool. The tool can read an input file, which contains information of the board size, via locations, mesh settings and the geometry shap information. The tool can calculate an inductance matrix for multiple ports and multiple shorts for a arbitrary shaped power net.

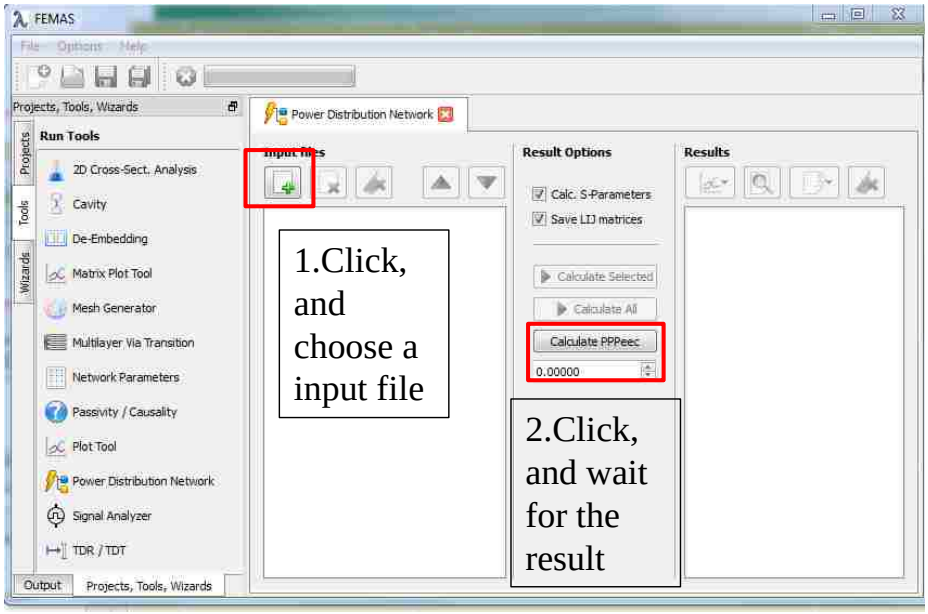


Figure 8.1. PDN tool GUI for FEMAS.

Figure 8.2 shows a test geometry for the tool. The extracted inductance and calculation time are listed in Table 8.1.

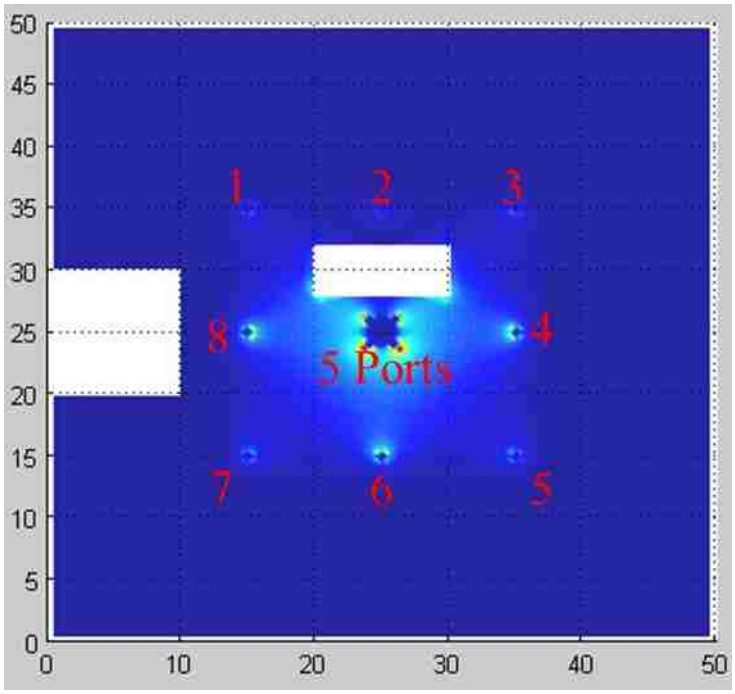


Figure 8.2. Test geometry for the numerical experiment. A 50mm by 50mm board with 2 ports and 2 shorts.

Table 8.1. Calculation example.

	Unknowns	L(pH)	time
Matlab	16,612	234	19s
Femas	16,612	245	20s

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VITA

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