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TVS transient behavior modeling method, and system-level effective ESD design for USB3.x interface

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TVS TRANSIENT BEHAVIOR MODELING METHOD, AND SYSTEM-LEVEL EFFECTIVE ESD DESIGN FOR USB3.X INTERFACE

by

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ABSTRACT

This research proposal presents a methodology whereby a protection device can be modeled in SPICE compatible platforms with respect to the transient behaviors during Electrostatic Discharge (ESD) events. This methodology uses an exclusively "black-box" approach to characterize the parameters of the protection device, thereby allowing it to be implemented without intimate knowledge of the DUT. Results of this methodology can be used to predict the transient response (conductivity modulation and snapback delay) of the ESD protection devices, and thereby predicts how much current could flow into the device (typically a digital IO pin) under protection. The transient behavior modeling methodology for the ESD protection device is developed for the purpose of system level ESD design, and it is part of the study of System-level Effective ESD Design (SEED) methodology. During the work, the transient behavior modeling method and the SEED methodology have been applied to a high-speed USB3.x repeater IC circuit design. This article introduces a PCB test board working as USB3.x repeater, which allows to place various on-board protection devices and to measure the residual voltage and current at the IO pin accurately.

In Section 2, the transient behavior modeling framework and the characterization method will be introduced. The validation results of three different types of protection devices are shown in the end of the section. In Section 3, the implementation of SEED methodology to a USB3.x system design will be introduced. The measurement setup is described in detail. Finally, the validation results for different scenarios will be shown.

ACKNOWLEDGMENTS

This thesis represents not only my work at EMC lab since 2016, it is a result of all accumulative efforts made by all previous students, industrial colleagues and research professors for more than three years.

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Thank you also to the rest of my committee, Dr. Jun Fan and Dr. Victor Khilkevich, for their insights into this work. I would like also to extend special thanks to Dr. Harald Gossner, who has supported the research project during my whole study period.

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

Page

LIST OF TABLES

1. INTRODUCTION

ESD damage is common in the electronic devices, to protect the DUT from ESD damage, multiple protection devices have been developed to suppress the voltage transiently during ESD event. There can be found thousands of millions ESD protection devices in the market. During ESD event, the devices will be triggered, thus most of the ESD current can be bypassed and will not damage the device under protection. However, the turn on mechanism and speed are very different among them. The turn on time for a spark gap device can be in range of microseconds to milliseconds. Comparably, the TVS diode could be turn on much faster, in range of several nanoseconds. The turn on time severely weakens the ESD protection effectiveness. Besides turn on time, the performance of an ESD protection device is also related to the lowest conductivity.

The goals of the transient behavior modeling method are to provide a model that:

1. combines small signal and large signal response.
2. can predict the transient response of the protection device during ESD event.
3. can be used in multiple SPICE based platform.
4. can be extracted from measurements in a 'black box' way.
5. works for variant protection devices.

System level Effective ESD Design (SEED) methodology has been successfully applicated in many situation during the last several years. However, SEED methodology on high speed interfaces design has not been widely applied yet. For high speed interfaces, On-chip ESD protection is limited in area size since the capacitance is proportional to the size of P-N junction, and the higher capacitance sacrifices the bandwidth of the transmission channel. High-speed interfaces are more sensitive to transient overshoots than slower interface types, thus the transient responses of the IO pin during the ESD event are investigated in this work.

In this work, the SEED methodology has been applied to a high-speed USB3.x repeater IC circuit design. It introduces a PCB test board working as USB3.x repeater, which allows to place the off-chip ESD protection devices at multiple positions and to measure the residual voltage and current at the IO pin accurately.

2. TRANSIENT BEHAVIOR MODELING FOR ESD PROTECTION DEVICES

Having accurate SPICE models which capture the transient behavior of TVS devices is important in system-level ESD simulations. Such simulations will predict whether the protection device or the protected device will trigger. Table 1.1 lists the advantages and disadvantages of different existing models. Column 1 in Table 1.1 represents the author of the prior work.

During the protection device turn-on process, there are two major transient behaviors: the inductive overshoot and the non-inductive overshoot.

The inductive overshoot is due to the fast time-changing current which flows through the apparent inductance inducing a peak voltage. The duration of the overshoot is related to the rise time of the transient current.

The non-inductive overshoot of a TVS diode is attributed to the conductivity modulation of the device [5] as well as the snapback delay within the device. In a spark gap, the static time lag can be observed, and it is very similar behavior as the snapback delay of a TVS diode. The duration for this overshoot is determined by the injection level. In general, for the injection level closed to the device trigger voltage, the turn-on process could last approximately in the range of several nano-seconds to tens of nano-seconds. For the injection level which is much higher than the device trigger voltage, the turn-on process could reduce to within nano-second.

The breakdown of a spark gap may occur in micro-second after the voltage across it reaches the trigger voltage.

Table 1.1. Comparison of existing models used for describing the large signal response

Author	What has been modeled	Advantages	Disadvantages
R. P. Santoro [1]	• Quasi-static VI curve	• Easy to implement • Portable to multiple platforms	• Quasi-static VI curve • Convergence issue in transient solver • No transient behavior
N. Monnereau [2] L. Wei [3]	• Quasi-static VI curve • Snapback behavior • Small signal model for RF analysis	• Combines small signal and large signal model	• Not compatible with SPICE solver • No conductivity modulation behavior
D. Dobrescu [4]	• Static VI curve	• Portable to multiple platforms • VI curve fitted	• No transient behavior included
Z. Pan [5] J. R. Manouvrier [6]	• Conductivity modulation • Snapback behavior	• Particle physics-based model • Overshoot due to the conductivity modulation has been well modeled	• Particle-based simulation not portable to SPICE • Difficult to be implemented in SEED
J. Di Sarro [7] P. Juliano [8]	• Conductivity modulation	• Non-linear transient overshoot included • SPICE based model	• Valid for SCR type TVS devices, not applicable BJT type devices

The proposed modeling method was developed for variant ESD protection devices include TVS, spark gap and varistor. All kinds of the devices can be modeled to capture all three overshoot mechanisms discussed [9]. The model is portable to different SPICE type platforms and demonstrates good correlation with measurement for both the overshoot peak voltage as well as duration (approximately <10% error). The modeling method is validated for simulating the transient behaviors of spark gaps, varistors and other overvoltage protection devices.

2.1. REVIEW OF LITERATURE

In previous study, three main different models are created by different groups. They all give their own benefits and limitations.

2.1.1. Piecewise Linear Model. Piecewise linear model describes only the voltage and current relationship of the protection device. For different types of device, the piecewise linear model can be easily used to predict the quasi-static IV curve. The modeling method is introduced in [1][4], and it is possible to be ported the model to multiple SPICE based platforms. However, two issues are mainly seen in this method:

1. A suddenly changed voltage or current would causes convergence issue.

2. The piecewise linear model doesn't contain transient behavior.

Figure 2.1 is showing an example of modeled quasi-static IV curve and the time domain waveform during a TLP injection.

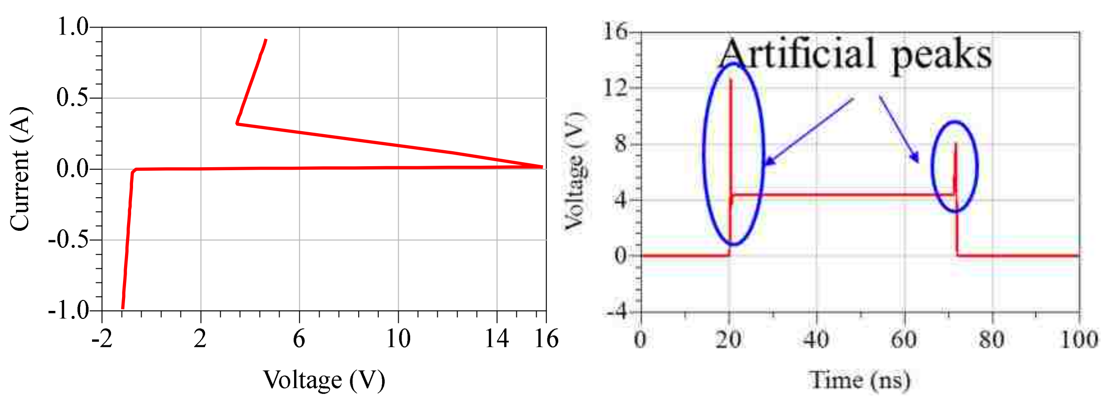

Figure 2.1. Quasi-static IV curve of the piecewise linear model (left) and its time domain waveform (right)

In the time domain waveform, the artificial peaks can be observed at both rising edge and falling edge of the TLP pulse because the model describes only the relationship between the voltage and current of the DUT.

2.1.2. Physics Based Numerical Model. The physics mechanism of the transient overshoot is introduced in [5] [12] [13]. Paper [5] explains the mechanism of the overshoot due to conductivity modulation, the simulation has been implemented in TCAD, and the time domain measurement result is compared to the simulation result. Paper [12][13] describes the conductivity modulation as well as the snapback delay. The voltage and current of the device are expressed in the differential equations. However, the comparison between the measurement and the simulation is not shown in the two paper.

The limitations of the model are:

1. These models are numerical models, cannot be easily implemented in SPICE based solvers.

2. Operators must have very strong physical background in semi-conductor technology to create a model based on the articles.

3. The models can only be used to predict one of the transient behaviors but in practical, the transient response of an ESD protection device are combination of multiple behaviors, such as conductivity modulation, snapback delay and the inductive overshoot.

4. The model cannot be used for other types of ESD protection devices, such as spark gap and varistor.

2.1.3. State Machine Model. Compare to the piecewise linear model, the state machine model improves the convergence, it defines three regions in the IV curve: off, snapback, and on. However, same as the piecewise linear model, the state machine model expresses the voltage as the function of current, hence, only the quasi-static IV curve is fitted, the non-linear overshoot behaviors are not included. As a result, the turn on time of the protection device cannot be modeled by this method.

2.2. MODELING FRAMEWORK

The block diagram of the proposed SPICE model for the TVS device is shown in Figure 2.2. It contains a linear small signal model, and a non-linear large signal model. The non-linear behavior is separated into a turn on behavior model and a large signal quasi-static model for the time after snapback (D3 and D4).

The turn on behavior model in Figure 2.2 includes a snapback delay model and the conductivity modulation model. The core blocks that influence the current flow are: 1). Small signal model; 2). D5 (D6); 3). Snapback delay model (if the device is a snapback type); 4). Conductivity modulation model; 5). D3 (D4). Diodes D1 and D2 are ideal diodes, but D3 to D5 have modified VI curves, they do not show the typical 0.7 V turn on of a PN diode.

The model frame in Figure 2.2 is symmetric for both polarities and the model parameters can be tailored to fit the specific TVS, varistor or spark gap of interest.

2.2.1. Linear Small Signal Model of The Protection Device. The linear small signal model replicates the RF performance of the TVS device when it is not turned on, which is needed to simulate the effect of the TVS on signal integrity. It contains the junction capacitance (C1) of the TVS device, the effective series resistance at resonance (R2, in order of Ohms), the apparent inductance (L1) arising due to the current path, as well as the leakage current resistor (R1) that is usually a very large value (MOhms or higher). The junction capacitance of a diode usually varies with voltage, here we use the zero-biased value of the junction capacitance as C1.

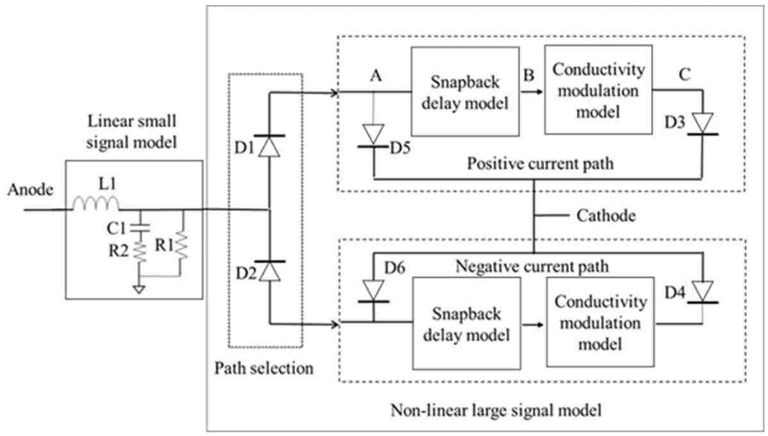

Figure 2.2. Block diagram of the transient behavior model

In large signal simulations, the parameters (R2, C1, L1) also impact the initial overshoot in both voltage and current waveforms. The voltage can be calculated from:

$$v(t) = \frac{L1 \cdot di(t)}{dt} + R_{TVS}(t) \cdot i(t) \tag{1}$$

where $\frac{L1 \cdot di(t)}{dt}$ determines the overshoot voltage. The $R_{TVS}(t)$ is the time variant resistance of the ESD protection device (non-linear resistance of the device). In the implementation, $R_{TVS}(t)$ includes the snapback delay model, conductivity modulation model and the quasi-static VI curve (D3).

For devices having a larger junction capacitance, the charge up of this capacitance leads to a current pulse that can be described by:

$$i_{junction}(t) = \frac{C1 \cdot dv_c(t)}{dt} \tag{2}$$

where, $v_c(t)$ is the voltage across the junction.

2.2.2. Non-Linear Large Signal Model. The non-linear large signal model structure contains five sub-models: the pre-clamping diode model before snapback D5/D6 (in Section 2.3.2.1), the path selection diode D1/D2 (in Section 2.3.2.2), and the quasi-static VI curve D3/D4 (in Section 2.3.2.3), snapback delay model (in Section 2.3.2.4), and conductivity modulation model (in Section 2.3.2.5). The combination of these models describes the transient behavior of the TVS.

2.2.2.1. Pre-clamping diode model. Some snapback devices demonstrate a 'bending' in the VI curve before they go into snapback. A TVS example (PESD3V3Z1BSF) is shown in Figure 2.3.

In Figure 2.3(b), the forward TLP voltage is 15 V, before the TVS snaps back, it clamps the voltage at 8.5 V. This behavior is due to the snapback triggering component inside the device (e.g. in [9] the Zener diode is used for triggering) and characterized using a very fast TLP (VF-TLP, pulse width is 6 ns) [10]. This clamping is modeled by D5 and D6 (in Figure 1.2).

2.2.2.2. Path selection diode. The path selection adds a directional feature to the model. For a positive transient event, diode D1 (Figure 2.1) turns on activating the positive current path while the negative current path is activated through diode D2 for a negative transient stress event. Diodes D1 and D2 are set only to have several mV voltage drop and they are practically ideal diodes.

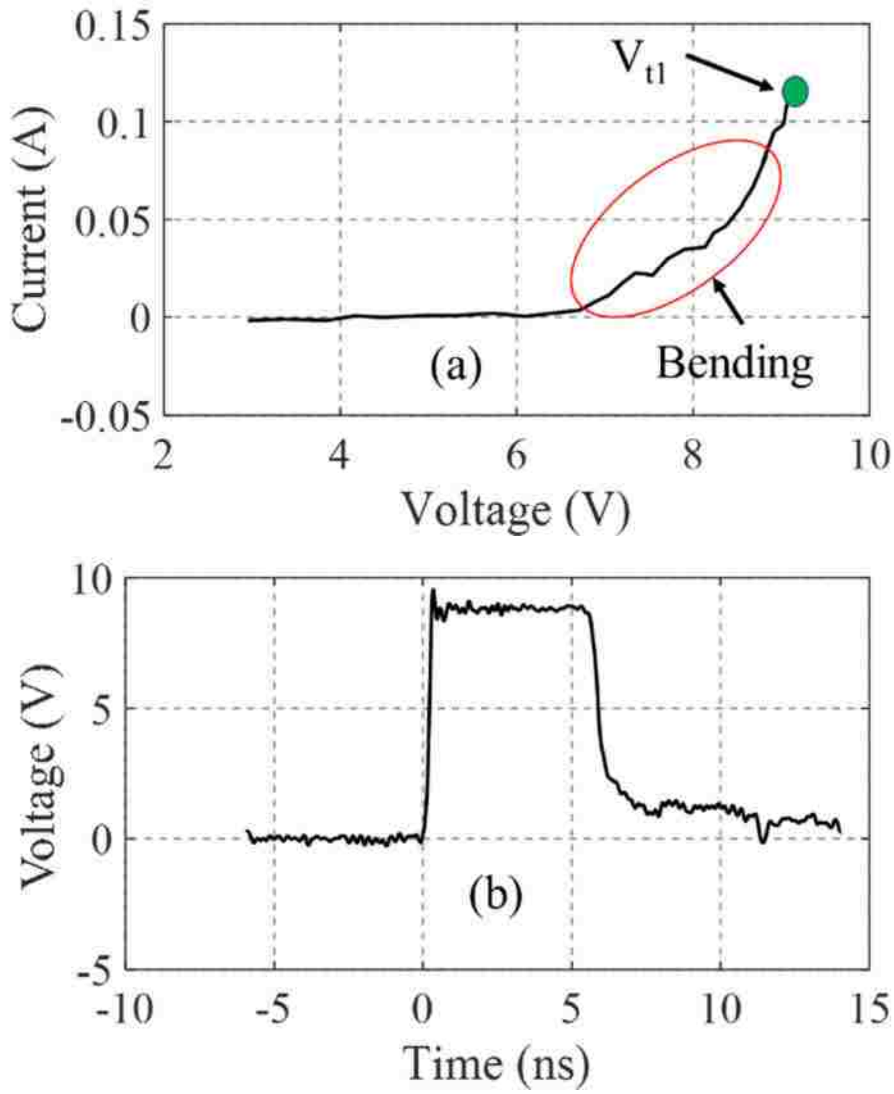

Figure 2.3. a) VF-TLP VI curve at the low current (I < 0.2 A) region, and b) the time domain pre-clamping behavior measured at 15 V forward voltage

2.2.2.3. VI curve after turn-on. Disregarding the transient behavior, the device can be modeled as a PN diode (I_s, R_s and N are the parameters needed in the diode model) in SPICE, D3 and D4 in Figure 2.2 are used to model the quasi-static VI curve. The data is extracted from 100 ns TLP measurements.

In Figure 2.4(a) the red dash line shows one of the modeled TVS (PESD5V0C1USF) VI curve after turn-on.

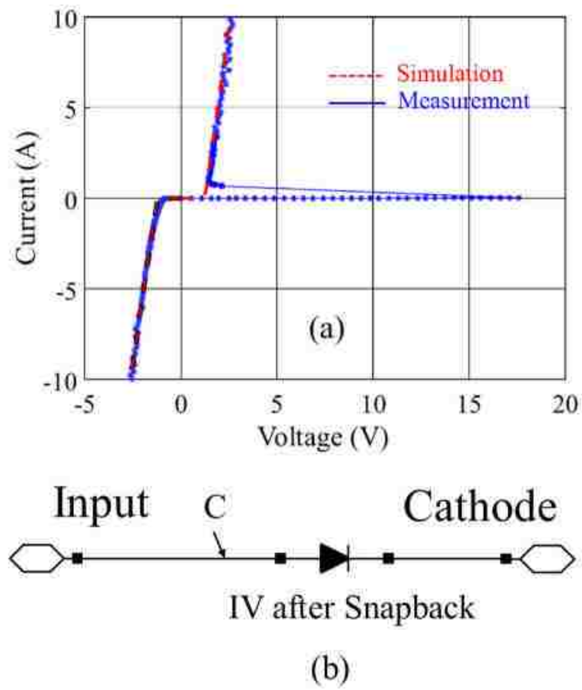

Figure 2.4. a) Simulated quasi-static VI curve after turn-on vs. measured quasi-static VI curve and b) circuit of the model

2.2.2.4. Snapback delay model. A TVS device does not go into snapback immediately when the voltage crosses the snapback threshold voltage. This delay is termed as snapback trigger delay. Snapback trigger delay is an inherent behavior of all snapback type devices. A spark gap may show nanosecond to millisecond delay which is usually called static time lag of dielectric breakdown. This effect is demonstrated in Figure 2.5. Physical reasons for this delay have been analyzed in [11][12][13].

The example shows a TVS (PESD5V0C1USF) under 5 ns TLP stress at 20, 22, and 30 V forward voltage. The quasi-static snapback threshold voltage (V_{t1}) is 17 V. The area size of S_1 and S_2 in Figure 2.5 is equal to the constant value, "snapback_trigger", when the snapback occurs within the device. With increased forward voltage, the snapback delay is reduced. However, this TVS device did not snapback at 20 V forward voltage for the 5 ns pulse, because the area, S3, is smaller than the threshold value "*snapback_trigger*". The pulse length is not long enough.

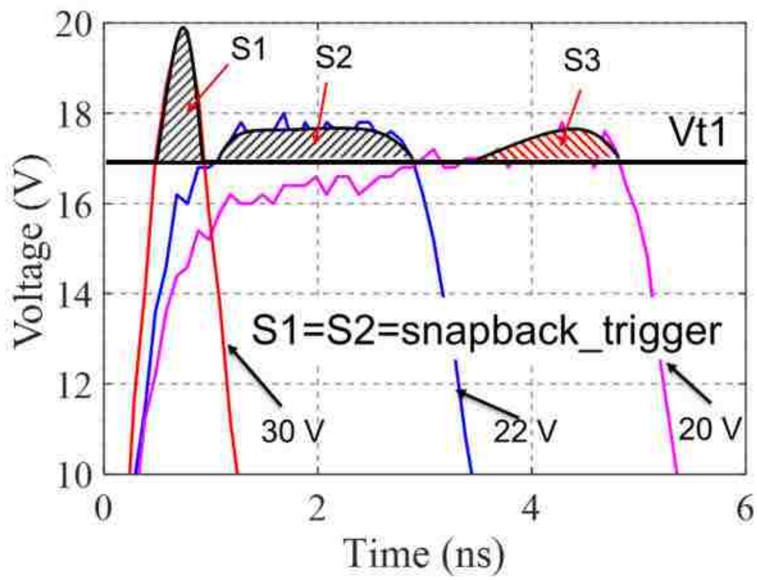

Figure 2.5. Snapback trigger delay behavior of one TVS sample

The snapback delay is modelled the following way. If the voltage across the TVS (V_{TVS}) is larger than the snapback threshold voltage (V_{t1}), then the difference between V_{TVS} and V_{t1} is integrated. The resulting value of the integration is compared to a threshold value (*snapback_trigger*) of a SPICE switch. Once the voltage reaches this threshold the switch switches its state from OFF to ON.

The SPICE implementation for the snapback trigger delay is shown in Figure 2.6 which is a sub-circuit used in Figure 2.2.

The voltage between the input node and the Cathode is the voltage drop across the TVS device (V_{TVS}). V_{t1} is determined from 100 ns TLP quasi-static VI measurements. The voltage difference between V_{TVS} and V_{t1} is descripted in term of V_{int} as:

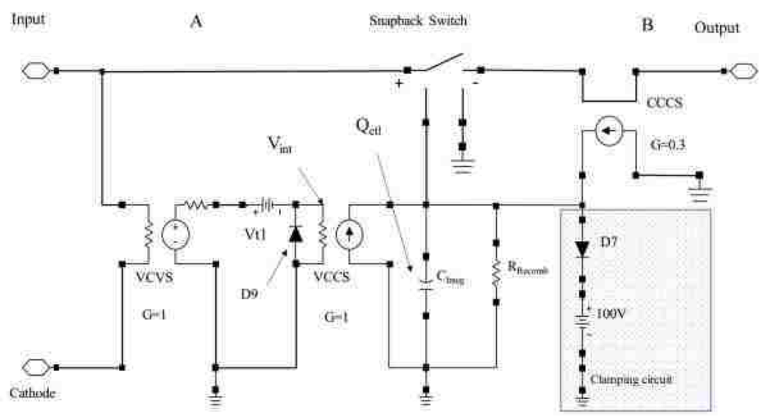

Figure 2.6. Snapback delay model circuit diagram

$$V_{int} = V_{TVS} - V_{t1} \tag{3}$$

The relationship between the delay and the V_{TVS} is described by the charge (Q_{ctl}) accumulated in C_{integ}, and expressed in:

$$\frac{1}{R_{trans}} \int_{t0}^{t} V_{int} \cdot dt = Q_{ctl} \tag{4}$$

where *t0* is the time instant when V_{TVS} is higher than the trigger voltage (V_{t1}). R_{trans} is the transfer impedance of the VCCS which is 1 Ohm. In the model, V_{TVS} is applied to a VCVS having a gain of 1. This reproduces the voltage. Next, the threshold voltage V_{t1} is subtracted. The resulting voltage (V_{int}) is used to control a VCCS. Before t0, V_{int} is clamped to Cathode voltage by D9. The controlled output current charges C_{integ}. V_{sb} is the voltage across C_{integ}, which is also the control level for the switch, it is determined by:

$$V_{sb} = \frac{Q_{ctl}}{C_{integ}} \tag{5}$$

V_{sb} is then compared to the "*snapback_trigger*" and determines the state of the switch. D7 and D8 are used to clamp the voltage of V_{sb} such that V_{sb} is never negative, and cannot exceed 100 V.

Once the switch is turned on, the voltage at the input is reduced and V_{sb} goes below "*snapback_trigger*". Avoiding the turn-off of the switch after triggering, a current-controlled current source (CCCS) is implemented in the model.

The output of this model (node B) is connected to the input of the conductivity modulation model. If the TVS does not exhibit snapback, the snapback delay model can be removed, node A and node B will be shortened in Figure 2.2.

2.2.2.5. Conductivity modulation model. Conductivity modulation in a semiconductor device is associated with the change in carrier concentration due to the avalanche and injection processes [5]. The conductivity is modulated by the amount of carriers in the neutral region near the depletion region edge. The conductivity modulation will increase the voltage across the TVS beyond the value predicted by the quasi-static VI curve during the transition.

Figure 2.7 shows the SPICE model which was developed to capture the conductivity modulation for the TVS device.

The current-controlled current source (CCCS) mirrors the transient current flowing through the device into the capacitor (C_{switch}). C_{switch} is related to the diffusion capacitance which is an equivalent capacitance due to the minority carrier distribution in the quasi-neutral region [16].

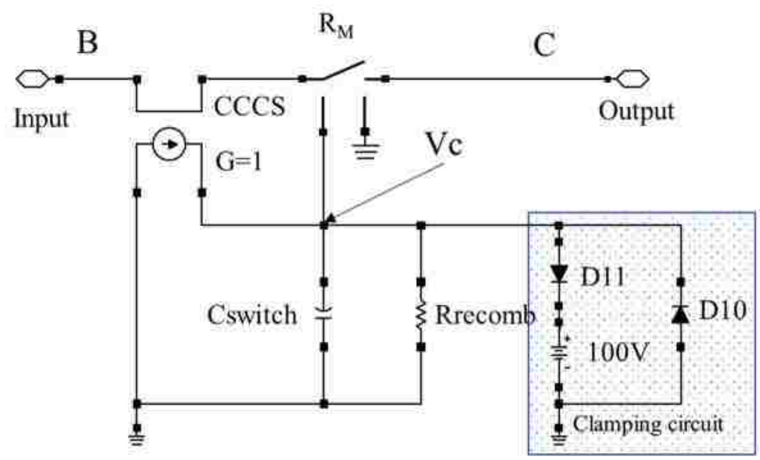

Figure 2.7. Conductivity modulation model circuit diagram

The SPICE model does not model the physical process. Some similarities exist as the model has a capacitor C_{switch} that is charged by the current to create a voltage that is used to change the resistance of the switch. V_C is the voltage across the diffusion capacitor C_{switch} in the SPICE model. It is used to control the conductivity by changing the value of the variable resistor (R_M). The variable resistance was created using a voltage-controlled switch model [14]. When C_{switch} charges up, V_C rises, thus, lowering the value of R_M. A turn-on threshold voltage (V_{turnon}) is derived from the charge threshold (Q_{th}) shown later. When V_C is greater than V_{turnon}, the resistance R_M is fixed to a low value (1mohm) and the model is completely turned on. The total charge delivered during a transient stress can be calculated as

$$Q_M = \int_{t_0}^{t} I_{tvs}(\eta)\, d\eta \tag{6}$$

where Q_M is the accumulated charge at time instant t, I_{tvs} (Disregarding the current flowing through R1, R2 and D5 in the model) is the current through the TVS device, t_0 is the start time, and t is the end time for the charge calculation. Q_{th} is referred as the charge at the turn-on moment (t_{turnon}) thus, it is the amount of charge needed to complete the phase in which the conductivity of the TVS is increasing. After this phase the quasi-static VI curve determines the current. This can be extracted by monitoring the current waveforms obtained from the VF-TLP measurements. Q_{th} describes the result from integrating the current through the device from t_0 to $t_{turn\text{-}on}$. The value of Q_{th} is determined from measurements. Next, V_{turnon} can be determined from

$$V_{turnon} = Q_{th}/C_{switch} \tag{7}$$

At last, the resistor R_{recomb} is the recombination resistor that discharges the charge in C_{diff} after the ESD event, which also helps the solver to converge. The value of R_{recomb} is 1 MOhm for general implementation. The parameters extraction procedure will be introduced in Appendix A.

2.3. TRANSIENT MODEL VALIDATION

11 ESD protection devices listed in Table 2.1 are selected in broad range, models for the devices were created in Keysight ADS using the proposed methodology, the models are also ported to LTspice without changing any parameter. All the models listed in Table 2.1 are attached in Appendix B. In Figure 2.8, the simulation result of using ADS and LTspice are compared with the measurement result (for PESD3V3Z1BSF). It

can be observed that the simulation results for both platforms are identical when the same set of parameters are used.

Table 2.1. TVS models have been created

TVS model number	Type
PESD5V0C1USF	Unipolar snapback device
PESD3V3Z1BSF	Bi-polar snapback device
PESD5V0H1BSF	Bi-polar snapback device
PESD5V0S1USF	High capacitance(42pF) unipolar Zener diode
DF2S5M4SL	Unipolar snapback device
ESD102-U1-02ELS	Unipolar snapback device
DF2S5.6	High capacitance (40pF) unipolar Zener diode
RClamp2431T	High voltage TVS(32V), bipolar Zener
uClamp2801T	High voltage(36V), high capacitance (25pF), unipolar Zener
BK33000702	Spark gap
AVLC 5S 02 050	Varistor

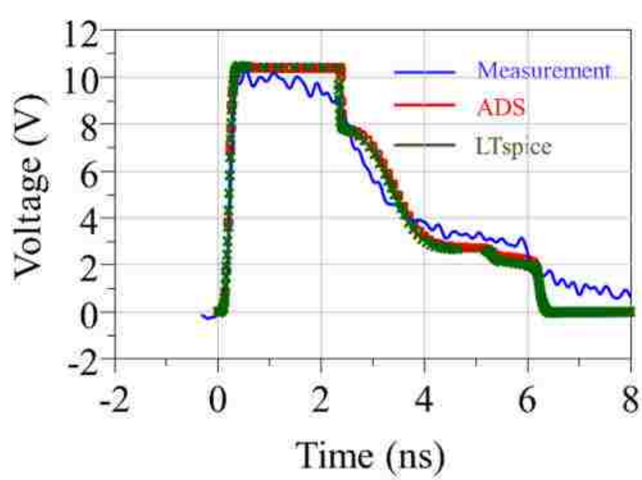

Figure 2.8. 30 V TLP injection result comparison among two different simulation platforms and the measurement

The simulation results of TLP are compared to the measurement, regarding the peak voltage, turn on time and quasi-static VI curve and show a good match. Some of the models' simulation results are also validated by the HMM test. The TLP pulse width used for the characterization in this article was selected to be 6 ns, but the models have been tested for other pulse widths as well. The TLP characterization was tested on both snapback and non-snapback type devices while the HMM stress was tested on a snapback device.

2.3.1. Validation Using TLP Source. The quasi-static IV curve (of PESD3V3Z1BSF) taken from the 100 ns TLP measurement result and the transient simulation result are compared in Figure 2.9. The average window for both measurement and simulation are set to 70% to 90 % of the time domain waveforms.

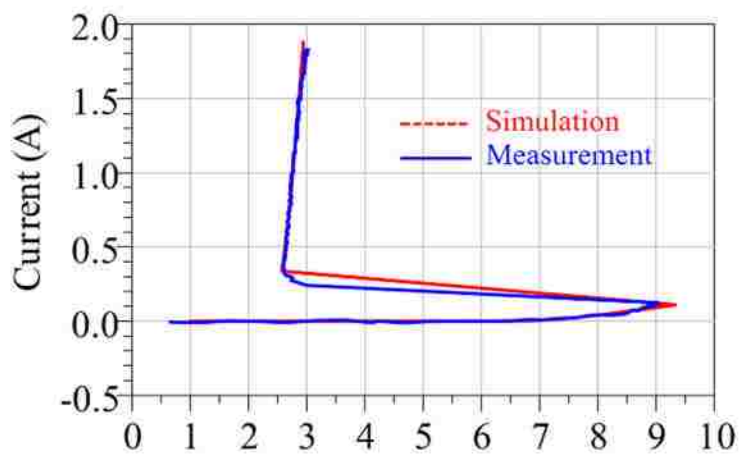

Figure 2.9. Quasi-static VI curve comparison of the 100 ns TLP measurement result and the simulation result

The time domain simulation result of the model was validated using a TLP 45 V to 1000 V forward voltage. Figure 2.10 compares measurement and simulation data for this snapback device (PESD3V3Z1BSF) at 45 V and 1000 V. The TVS triggers at 9 V. The simulation matches the measured delay. At 1000 V, the delay is very short, and the overshoot is mainly inductive. The simulations successfully captured the transient response observed in the measurements.

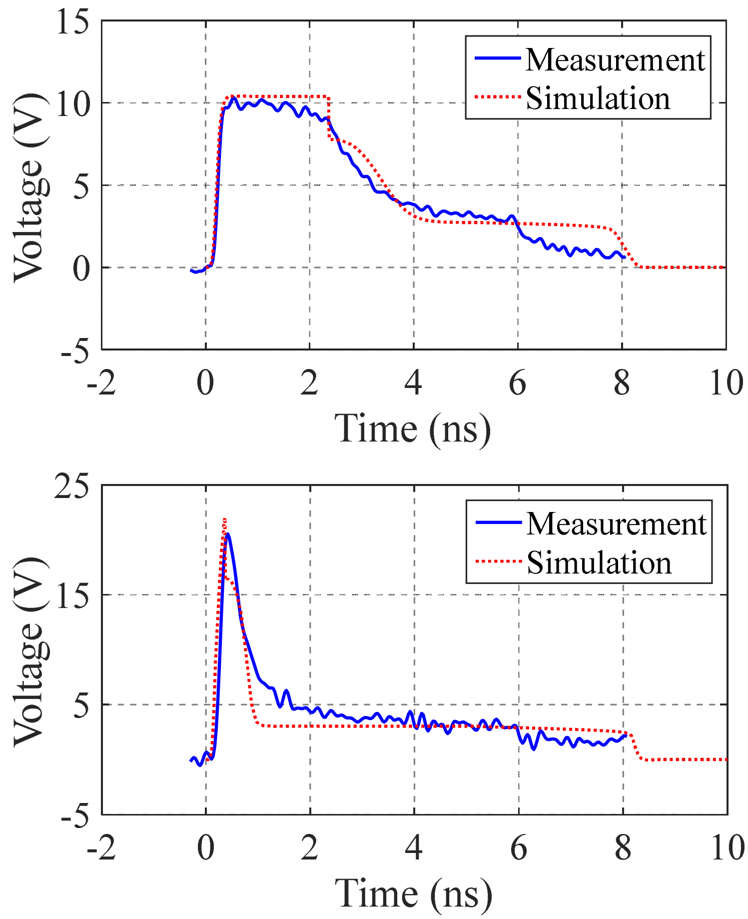

Figure 2.10. TLP validation result for snapback type of TVS device with forward voltage of 45 V (top) and 1000 V (bottom)

A similar type of characterization was performed on a non-snapback type device (PESD5V0C1USF). The comparison between measurement and simulation is shown in Figure2.11. The TLP forward voltage for Figure 2.11 (a) was -40 V while it was -500 V for Figure 2.11 (b). The simulation model successfully predicts the overshoot voltage and overshoot duration within 10 % tolerance.

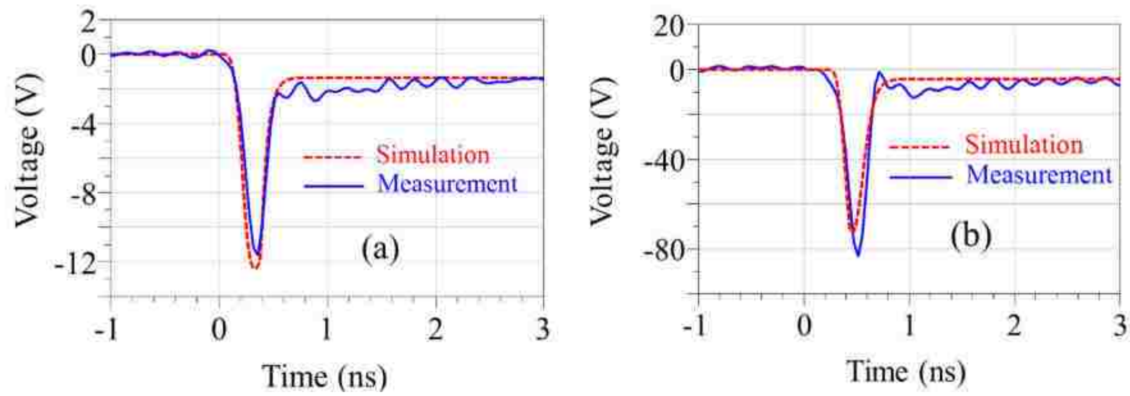

Figure 2.11. TLP validation result for non-snapback type of TVS device with forward voltage of a) -40 V and b) -500 V

2.3.2. Validation Using ESD Gun Generator. The same snapback device used in the TLP characterization was stressed with an ESD generator. The device was tested with two stress levels as shown in Figure 2.12.

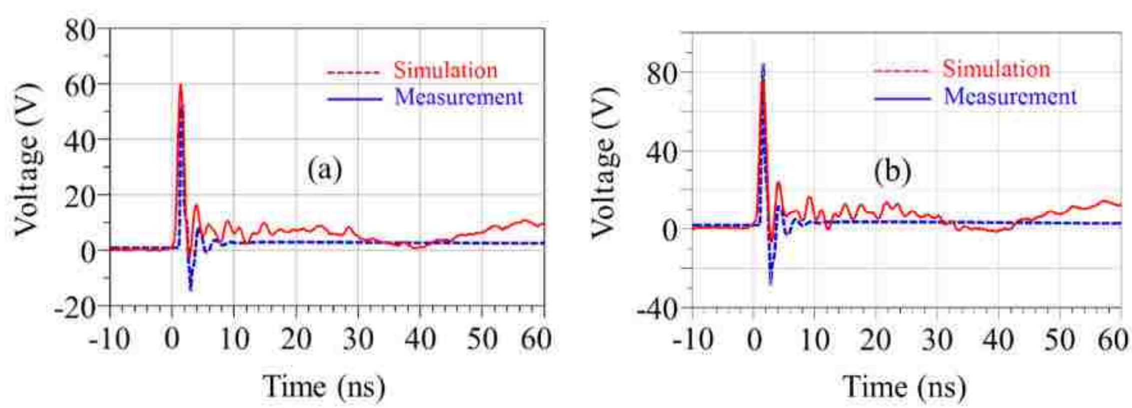

Figure 2.12. IEC validation results with source voltage set at a) 1 KV and b) 2 KV

The peak voltage was observed to be nonlinear based on the peak transient injection which indicates it was related to the non-linear part of the overshoot model. The simulation model was able to predict the transient response in terms of the peak voltage and ringing frequency for the device under test. The model is able to predict the quasi-static behavior after the ringing is settled.

2.4. SUMMARY AND FUTURE WORK

In this section, the transient behavior modeling method has been proposed for various ESD protection devices. It allows to predict the transient behaviors such as snapback delay (static time lag for spark gap), conductivity modulation and quasi-static IV curve. The model also combines the RF response of the protection devices. The model has been validated by both TLP injection and ESD gun test.

To adapt the model to different TVS, a set of parameters needed to be tuned based on measurements. This model was written to operate on most SPICE solvers. A very detail instruction of modeling procedures has been introduced so that other students and engineers can follow it and model the protection devices for their own usage purpose.

The next step for this work is to automatically generate the SPICE model by simply import the measured S-Parameters and TLP results.

3. AN APPLICATION OF SYSTEM LEVEL EFFICIENT ESD DESIGN FOR HIGH-SPEED USB3.X INTERFACE

High-speed interfaces like USB3.x or HDMI need optimized selection and placement of off-chip ESD protection devices regarding parasitic capacitance (<1 pF) and turn-on time. On-chip ESD protection is limited in area size since the capacitance is proportional to the size of P-N junction. High-speed interfaces are more sensitive to transient overshoots than slower interface types [17][18][19]. It is important to consider that both on board and on-chip ESD protection devices might show a delay in turn-on. Thus, not only the static VI curves but the transient turn-on behavior needs to be considered [20][21]. This uncertainty in the design process can be evaluated and an optimal solution found by applying System Level Efficient ESD Design (SEED) methodology [22][23].

In the system level ESD design, engineers mostly consider the susceptibility of the event based on IEC61000-4-2 and ISO10605 standards [24], yet in the field, CDE [25] (cable discharge event) is another type of stress that can cause malfunction or damage of the system [26]. In this paper, the SEED methodology has been applied to a high-speed USB3.x repeater IC circuit design. The paper discusses the application of the SEED methodology, and it introduces a PCB test board working as USB3.x repeater, which allows to place various PCB protection devices and to measure the residual voltage and current at the IO pin accurately.

3.1. DESCRIPTION OF THE VALIDATION TEST SYSTEM

The system is built around TI SN65LVPE512, which is an USB 3.0 repeater IC. The IC compensates the frequency response of the USB3.0 transmission channel, such that no distortion of the signal at the end of the channel.

3.1.1. USB3.X Test Board. An on-board current and voltage measurement structure captures the pin voltage and current close to the IC's RX and TX pin. Figure 3.1 represents the PCB designed for this investigation.

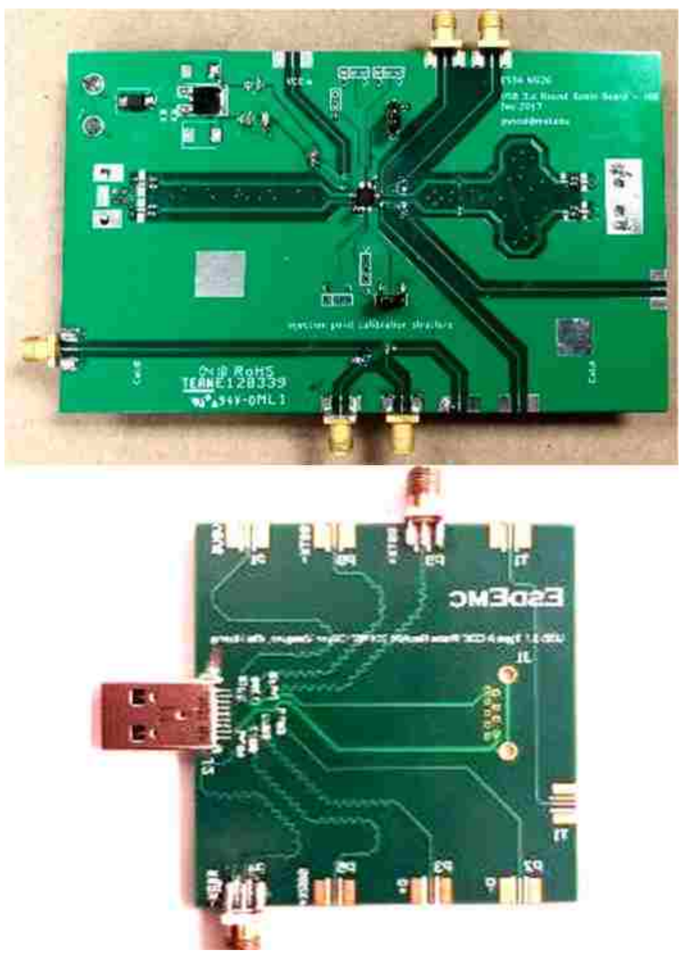

Figure 3.1. Photograph of the USB3.x repeater board (top) and the ESD injection board (bottom)

The USB3.x repeater board includes two USB ports, one of them is connected to an ESD injection board. Besides the repeater and its measurement ports, the PCB contains a calibration structure (lower side of the PCB, the top image of Figure 3.1 that replicates the voltage and current measurement circuit. It allows calibrating the voltage and current measurement port transfer functions.

To measure the current two choices have been considered: Inductive and via the voltage drop along a 1 Ohm resistor [27]. As the 1 Ohm resistor introduces a significant voltage drop (relative to the $R_{dynamic}$ of the I/O and the TVS), we decided to use an inductive method and accept its disadvantage of more complex signal processing to obtain the current from the measurement voltage.

Figure 3.2 shows the critical part of the layout of the voltage and current measurement ports. The 1 kOhm resistor R3 together with the input impedance of the oscilloscope forms a 26.4 dB voltage divider. The two adjacent lines (red lines) form a transformer for capturing the current.

The induced voltage $V_{ind}(t)$ is given by

$$V_{ind}(t) = M\frac{di}{dt} \quad (8)$$

The mutual inductance, M, is determined by the local trace geometry. Its value is measured 0.31 nH. The inductor L1, in conjunction with the parallel resistors R1 and R2 form a low pass filter. This partially compensates for the frequency response of the inductive pick-up transformer. Its cutoff frequency fc is 79 MHz. The low pass is added to allow for better usage of the dynamic range of the oscilloscope. Without the low pass, the initial current rise would cause a large initial peak, forcing a large voltage scale setting. This complicates the current measurement for later parts of the waveform and worsens the effect of oscilloscope offset. Figure 3.3 shows the frequency response between the injection port and the current measurement port with and without the RL integrator.

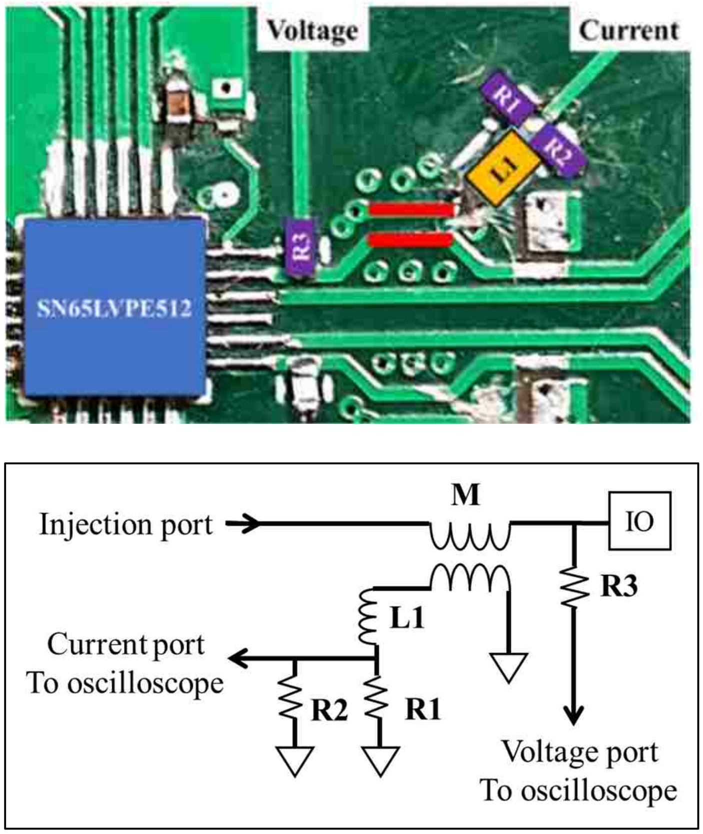

Figure 3.2. Layout pattern (top) and schematic (bottom) of the voltage and current measurement structures

To obtain the current values from the measured voltage a deconvolution of the frequency response is needed. The method used is described in [28]. Figure 3.4 is the frequency response for the current measurement structure, deconvolution structure and the expected response after deconvolution. It can be observed that the transfer function of the current measurement structure and the deconvolution structure are symmetric to the 0 dB line.

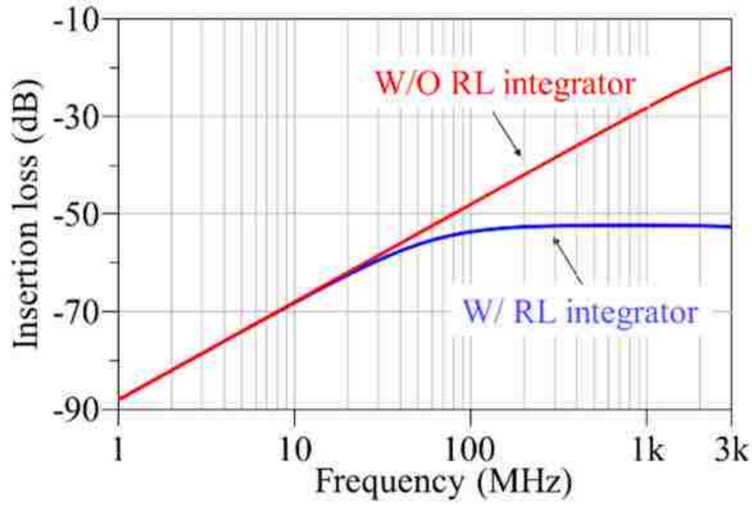

Figure 3.3. Frequency response between the injection port and the current measurement port in simulation

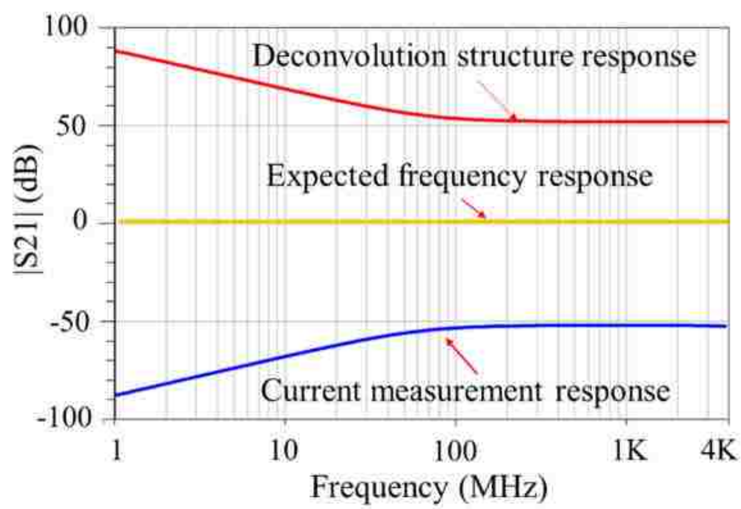

Figure 3.4. Frequency response of the inductive current measurement structure, deconvolution structure and the expected response after deconvolution

3.1.2. TLP Injection Setup. In the TLP injection test setup, the TLP output is connected to the injection board through a coax cable, the injection board is plugged into the USB3.x test board. Figure 3.5 is the illustration of the TLP injection test setup.

The onboard current and voltage measurement ports are connected to the oscilloscope, ESD protection and attenuator are placed in between to protect the channels of the oscilloscope.

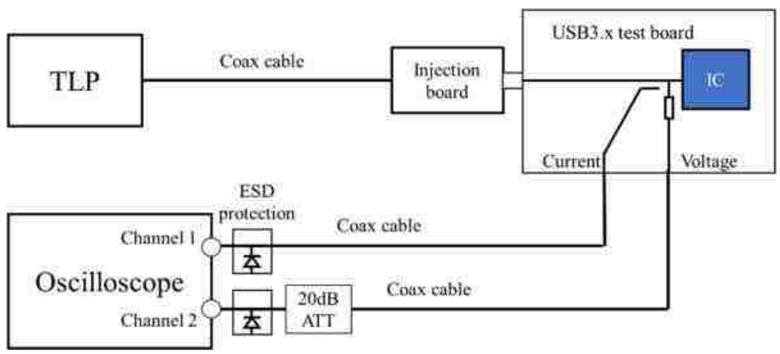

Figure 3.5. TLP injection setup

3.1.3. HMM Injection Setup. The connection of the HMM injection setup is similar to the TLP injection setup. However, due to the strong emission during the discharge event (When the relay is closed, the E-field collapses causing large dD/dt and the current through the tip suddenly increases which causes large dB/dt), the transient field could be coupled to both the onboard traces and the oscilloscope, thus, ruining the measurement results. To avoid the transient field coupling, the oscilloscope and the USB3.x test board are well shielded during the discharge event. Additionally, the FCC F65 current probe is used in this measurement to measure the current which is injected by the ESD gun. The HMM injection test setup is shown in Figure 3.6.

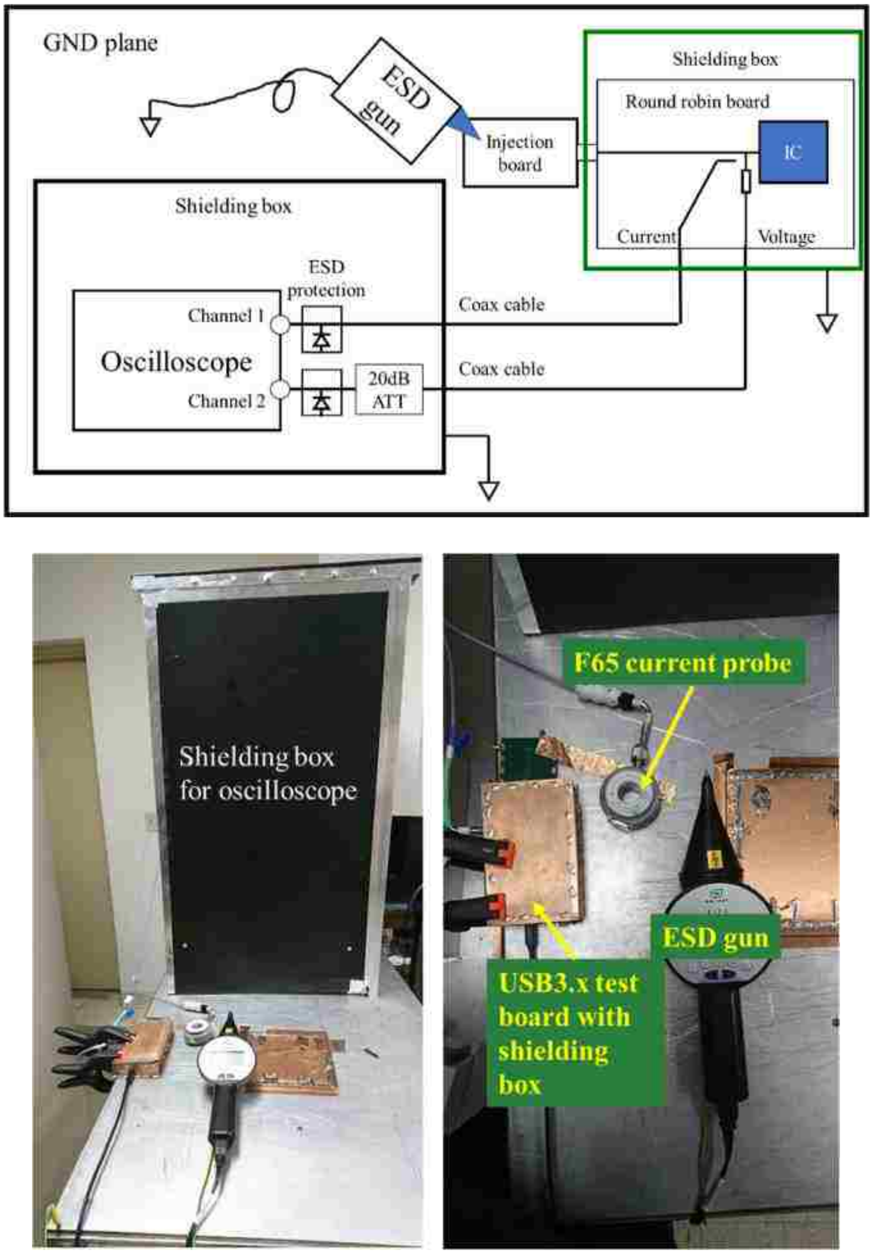

Figure 3.6. Illustration of the HMM (ESD gun) injection test setup(top) and the photo of the real test system(bottom)

3.2.MODELING METHODOLOGY

The objective of the modeling work is to predict the ESD current flow in the TVS and the IC's I/O pin. This requires including the source (e.g., HMM or TLP), the passive components (e.g., transmission line, series and shunt RLC components), and both the IO and the external ESD protection. For all components besides, measured data are used to create and verify the model.

3.2.1. TLP And HMM Source Model. The TLP waveform is less complex and it provides an efficient method to evaluate some forms of the Cable Discharge Event (CDE). The TLP model and test instrument use a waveform of 0.2 ns rise time and 100 ns pulse length. The spice model creates the rising edge by applying a 0.2 ns rise time filter to an ideal step response. Figure 3.7 shows the SPICE model for the TLP source.

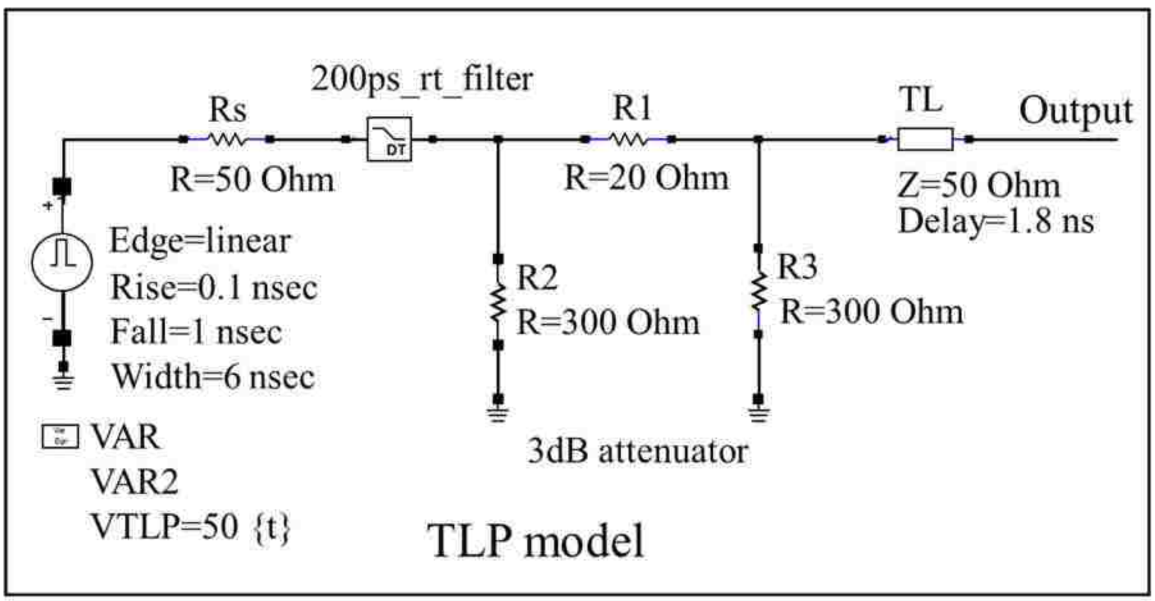

Figure 3.7. SPICE model for TLP source

Figure 3.8 shows the effect of the rise time filter which smooths the transition of the waveform.

To realize the HMM injection the contact mode ESD gun model shown in [29] is used. Figure 3.9 shows the ESD gun contact discharge model and Figure 3.10 compares the simulated current waveform with the measured waveform from a real ESD gun (EMTEST Dito).

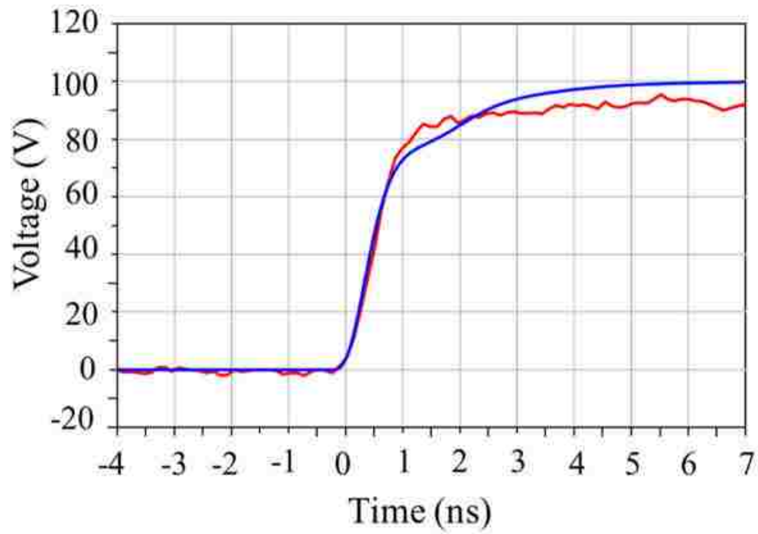

Figure 3.8. The comparison between measured and simulated waveform

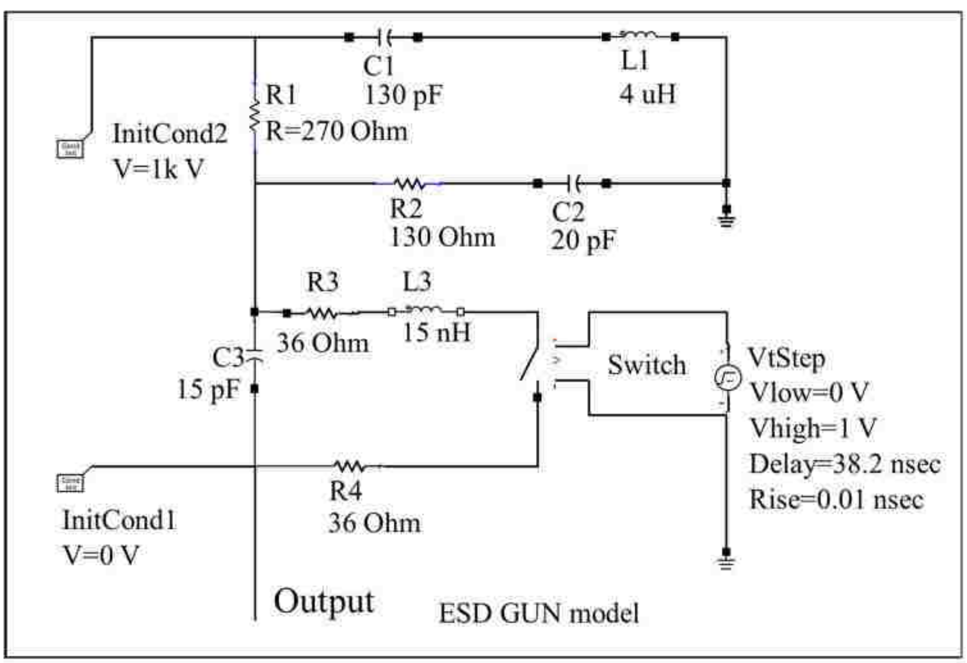

Figure 3.9. ESD gun contact discharge model

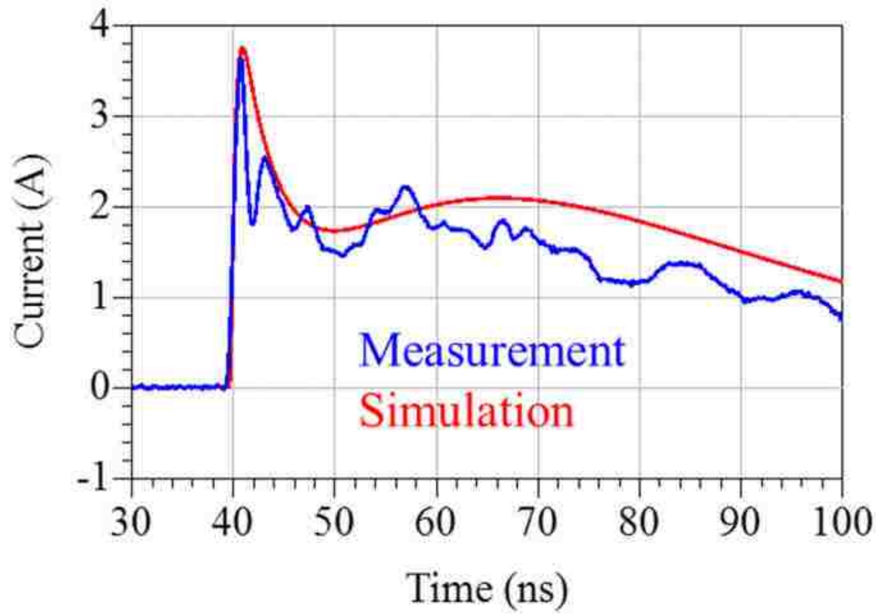

Figure 3.10. The current waveform of simulation and measurement

3.2.2. Large Signal IO Pin Model. The IO pin response is characterized and modeled using the method discussed in [30]. Figure 3.11 shows the TX pin model of the USB3.x equalizer IC for the positive current path.

3.2.3. Transmission Path Model. Three elements are included in the channel path model, the series components, shunt components and the transmission line. A 100 nF capacitor is used to block DC. The ESD protection design may include a series resistor to limit the current into the IC and to cause a more favorable ratio of currents flowing through the TVS relative to the current flowing into the IO pad. The transmission line model can be extracted either from insertion loss measurement or from the numerical simulation. In this paper, we used a physical based transmission line model provided by the simulation tool, based on the required parameters, such as geometry, permittivity, and the dielectric loss tangent.

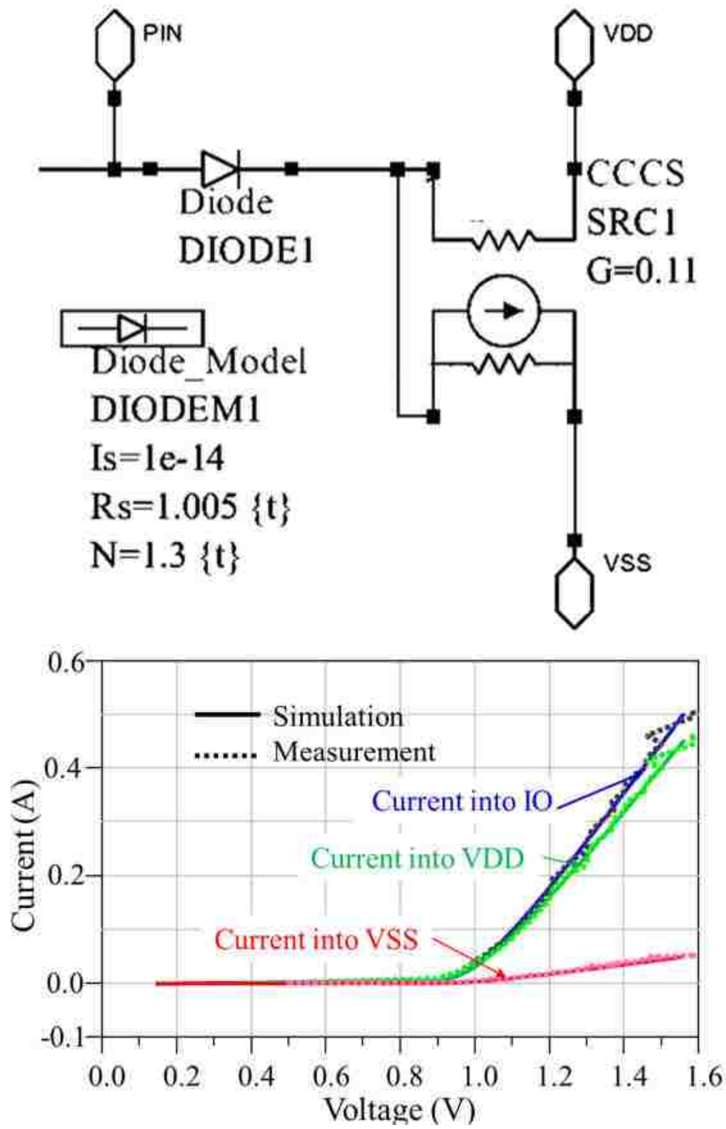

Figure 3.11. Positive polarity injection IO model of the TX pin. The positive model of IO (top); Measured and simulated IV curve of the IO pin model (bottom)

3.2.4. ESD Protection Device Model. A snapback type Transient Voltage suppressor (TVS) is modeled using the methodology proposed in Section 2 [21]. Figure 3.12 compares measurements to simulations of quasi-static IV curve and the transient responses at 45 V and 1000V TLP charge voltage.

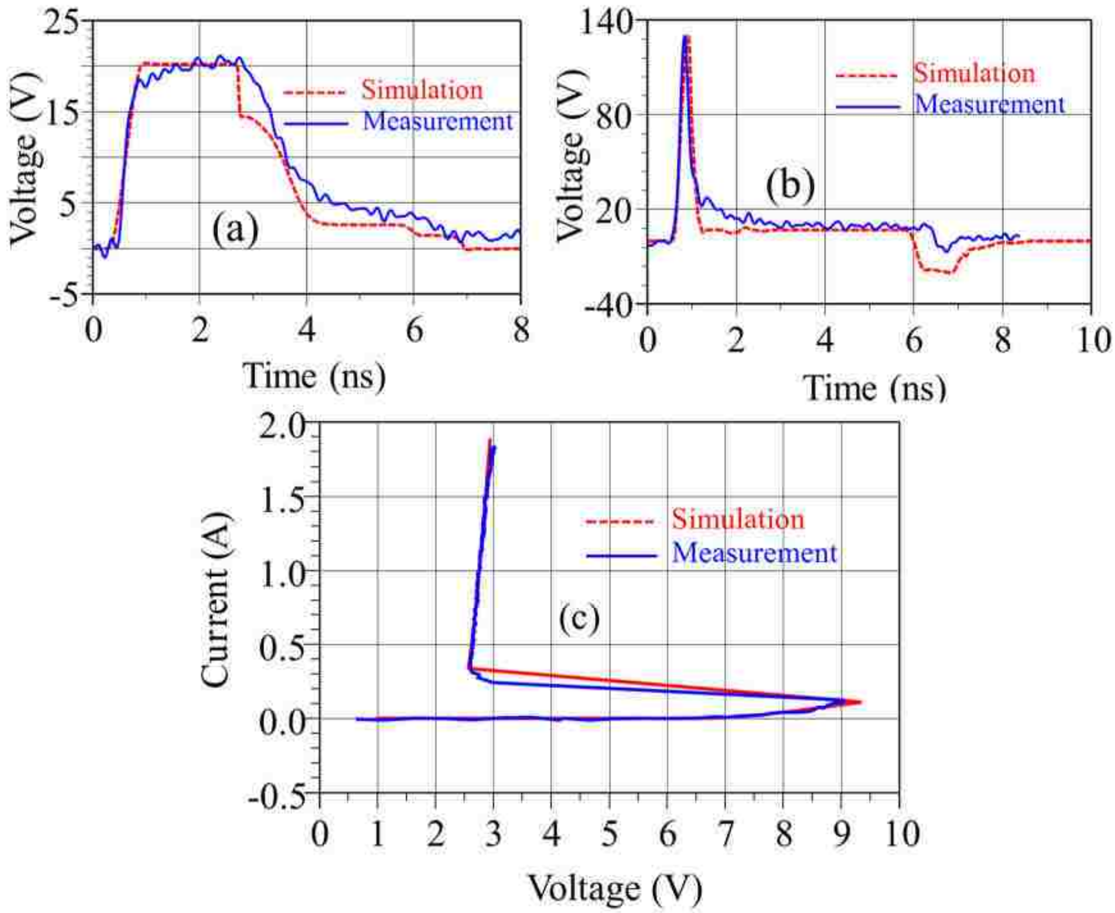

Figure 3.12. TLP validation result for a snapback type TVS at TLP charge voltages of a) 45 V and b) 1000 V, and c) the comparison of the simulated and measured quasi-static IV curve

3.2.5. The Full System Model. Figure 3.13 shows the combined model for system level ESD simulation. The 200 nF capacitor provides an RF short from VDD pin to VSS pin. The additional 1 uF capacitor and 4.7 uH inductor are used in the test setup to isolate the VDD pin from the supply. The voltage measurement port has also been included in the simulation model as it bypasses part of the current. However, the current measurement port is not simulated since the coupling is less than -50 dB at frequencies lower than 3 GHz. Both powered (VDD=3.3 V) and unpowered (VDD=0 V) configurations are tested.

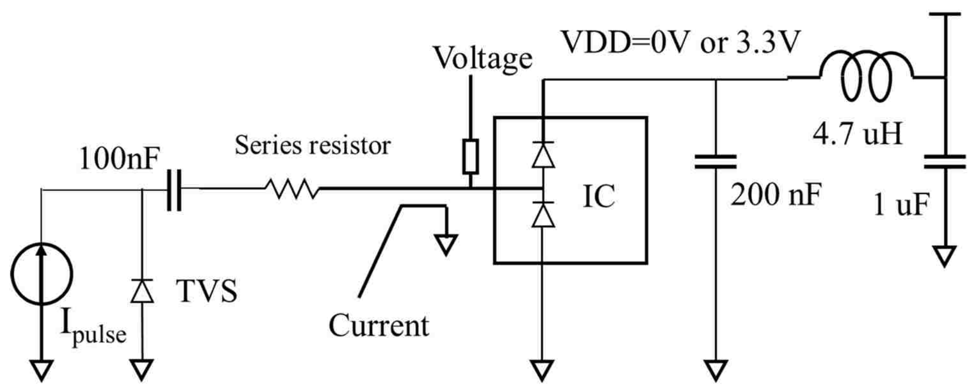

Figure 3.13. Combined system model

3.3. SYSTEM LEVEL ESD SIMULATION AND MODEL VALIDATION

Both power on and power off situation of the system level model are validated by TLP and ESD gun injection.

3.3.1. TLP Injection. The 50 Ohm TLP generator is charged to 100 V, the rise time is 0.2 ns, and the pulse length is 100 ns. Both powered and unpowered situations are considered.

3.3.1.1. Scenario I: 2 A TLP injection, VDD = 0V. The measured and simulated transient response of the IO pin is shown in Figure 3.14 for the unpowered case.

The sub-Figure 3.14(b) emphasis on the ringing. It is caused by multiple reflections at both ends of the transmission line. Both the TVS and the IO pin form low-value resistances (after turn-on), thus the wave is reflected at both ends of the transmission line. The period of the ringing is 1 ns, which is twice the delay time of the trace.

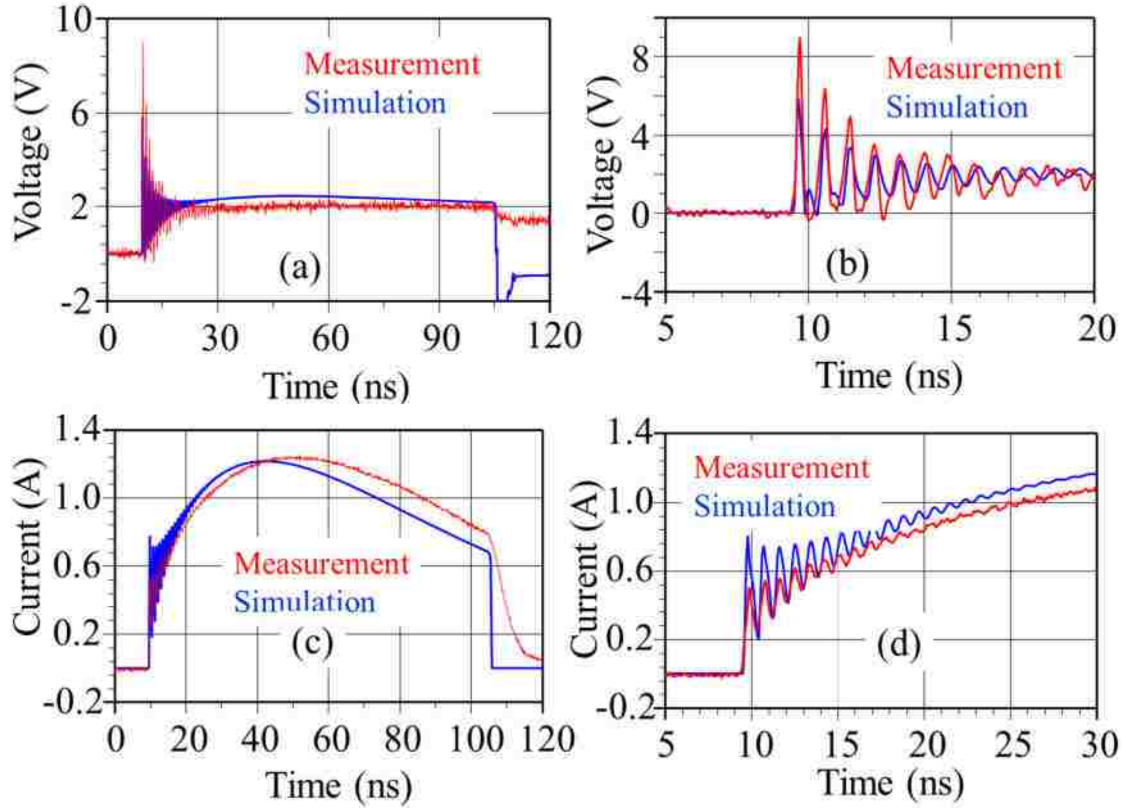

Figure 3.14. Voltage (a) (b) and current (c)(d) transient response of the IO pin. VDD=0 V, TLP charged voltage = 100 V

Figure 3.14(c) shows a bump-like current waveform. This effect will be explained in Section 3.5. Here the voltage ringing is underestimated, and the current is overestimated due to the transmission line model in the simulation is the ideal delay line with no loss parameter. The average difference between the simulation and the measurement results is less than 10%.

3.3.1.2. Scenario II: 2 A TLP injection, VDD = 3.3 V. The test and simulation configuration is identical to the previous one, but the IC is powered with VDD = 3.3V. In general, if the IC is powered, the IO will behave differently. The results are shown in Figure 3.15.

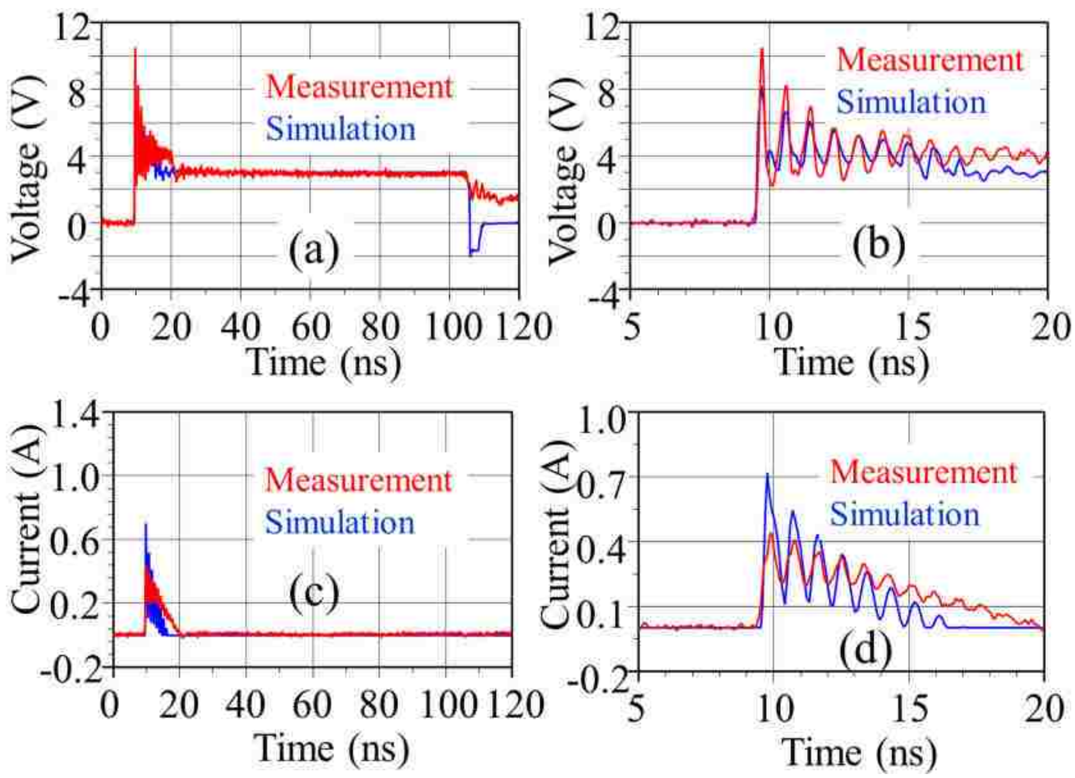

Figure 3.15. Voltage (a) (b) and current (c)(d) transient response of the IO pin. VDD=3.3 V, TLP charged voltage = 100 V

Compared to Figure 3.14, the result shows the effect of having the IC powered. The unpowered case poses a larger risk to the IC. Once the IC is powered, its positive trigger voltage is increased by 3.3 V. Thus, the external TVS will carry most of the current (1.85 A in this case).

3.3.2. HMM Injection. The measurement has well validated the simulation results using the TLP as the source. However, the HMM is the essential test method for system level ESD test. The HMM pulse is a more complicated source compared to the TLP source. Thus, a correct prediction of the interaction of the various components under HMM conditions is very important for applicability of the SEED methodology.

3.3.2.1. Scenario I: 1 kV HMM injection, VDD=0 V. Figure 3.16 Shows the measurement results compared to the simulation results. In Figure 3.16 (a), the total injection current is measured by FCC F65 current probe. The measured peak current is 3.6 A, the simulated peak current is 3.5 A, the difference is only 0.1 A. The difference of the second current peak at 30 ns after the first peak is 0.5 A, which is allowed within the tolerance according to IEC61000-4-2. However, the discrepancy of the second current peak causes the difference of the peak current flows into the IO pin between the simulation and measurement as shown in Figure 3.16 (b). The IO current is measured during the first HMM injection. If continuous multiple injections have been performed, the current flow into the IO reduces. This effect is due to a charging of the floating part of the transmission line and will be described in more detail in Section 3.5.

3.3.2.2. Scenario II: 1 kV HMM injection, VDD=3.3 V. When the system is powered, hardly any current flows into the IO pin after about 10 ns, in Figure 3.17, it can be observed that both the measurement and simulation results are showing the same current waveform at the IO pin.

In the initial phase of the ESD pulse, the TVS is off, and the incident wave triggers the on-chip protection resulting in a current flow into the IO pin. A ringing with a periodicity of 1 ns is observed (like for TLP) due to reflections in the transmission line between the IO pin and the TVS. The ringing then attenuates to zero after about 10 ns.

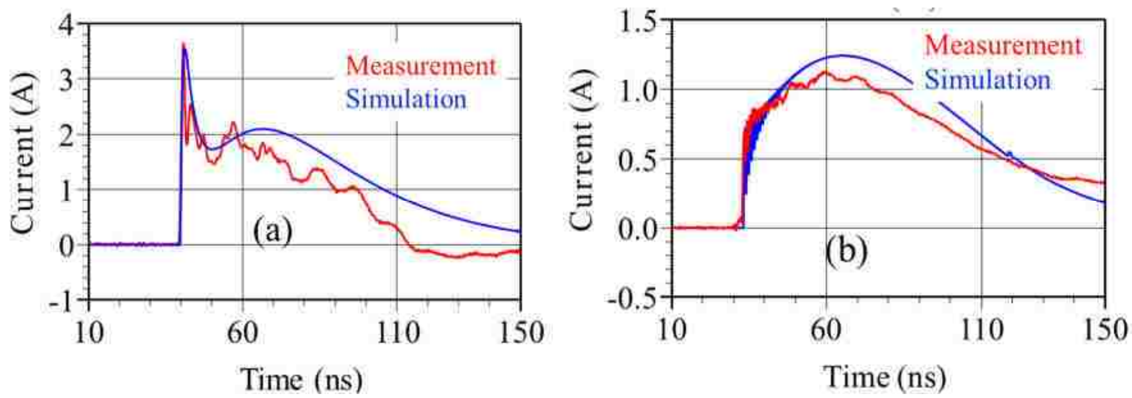

Figure 3.16. The current output from the ESD gun (a) and the current flows into the IO pin (b) during a 1 kV HMM injection to the unpowered system

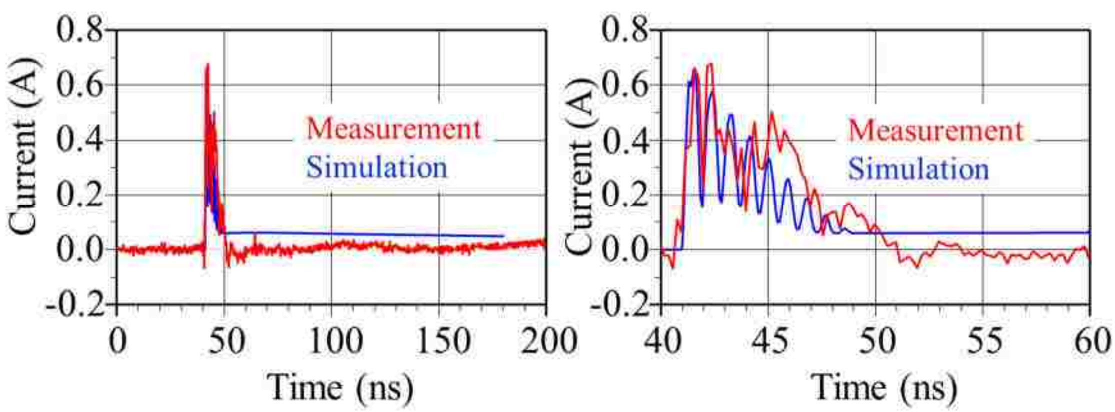

Figure 3.17. The current flows into the io pin during a 1 kv hmm injection to the powered system (left) and the close view of the current waveform in the initial 10 ns

3.4.DISCUSSION

In last section, the measurement result shows very good agreement to the simulation result. However, many interesting behaviors have been observed. These effects can be categorized into non-linear effect and passive linear effect, and the reasons are discussed below.

3.4.1. IV Characteristics. Figure 3.18 Shows the quasi-static IV (measured by 100 ns TLP, average window sets to 70%-90% of the pulse width) characteristics of the unpowered and powered IO pin (w/o TVS) during TLP pulsing and the selected TVS device. It can be observed that under certain injection level, the unpowered IO pin clamps at lower voltage than the TVS device. Hence, ESD current would flow into the IO other than the TVS.

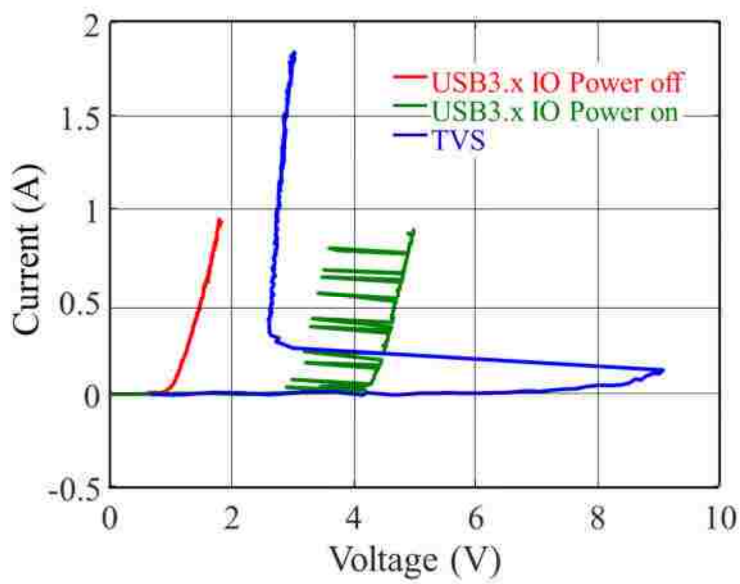

Figure 3.18. Quasi-static IV curve comparison: unpowered/powered IO pin vs. TVS

However, the clamping voltage of the powered IO pin is much larger than the TVS. Thus, TVS conducts most of the ESD current once it is triggered. It is understandable that this type of TVS cannot provide sufficient protection for the unpowered situation if no additional component added. The spikes of the IV curve of the powered IO pin are due to the level at the IO pin switching between 0 V to 1.8 V if the IC is powered. This is the normal operation of the repeater IC in the powered state.

3.4.2. Passive Component Effects. The passive components in the system level ESD design have an important role to the transient behavior.

3.4.2.1. Transmission line. One of the effects of the transmission line is the delay effect (delay time of the 70 mm TL is 0.5 ns). Figure 3.19 shows a set of IV curves measured at the IO pin, it can be observed that if the TVS is placed very close to the IO pin, the IV curve measured at the IO pin is identical to the IV curve without TVS because the clamping voltage of the on-chip protection is much lower than the trigger voltage (Vt1) of the TVS thus the TVS stays off. However, if the TVS is placed at the other end of the 70 mm transmission line, the IV curve changes. In Figure 3.19 (a), the IC is unpowered, the TVS at the other end of the transmission line increases the IV curve slope (dynamic resistance) of the IO pin, because the TVS partially bypasses the ESD current thus less current flows into the IO.

In Figure 3.19 (b), the IC is powered. The red curve shows that if the TLP output current is larger than 0.6 A, the TVS clamps the voltage at less than 3 V, and the current flowing into the IO pin reduces to zero. The TVS diode can trigger and snaps back within nanoseconds.

Another effect of the transmission line is the inductive behavior. The inductance of the 70 mm transmission line can be calculated (from the geometry) as 30 nH. Figure 3.20 shows the inductive effect of the transmission line during a 100 V TLP injection to the unpowered system with TVS placed at position 1. In order to investigate the inductive effect only, the capacitors are shorted in this simulation. If one end of the transmission line is shorted it behaves like an inductor and adds inductance. The time constant in the waveform is determined by the inductance (30 nH) and the load resistance (0.6 ohm) and results to 50 ns.

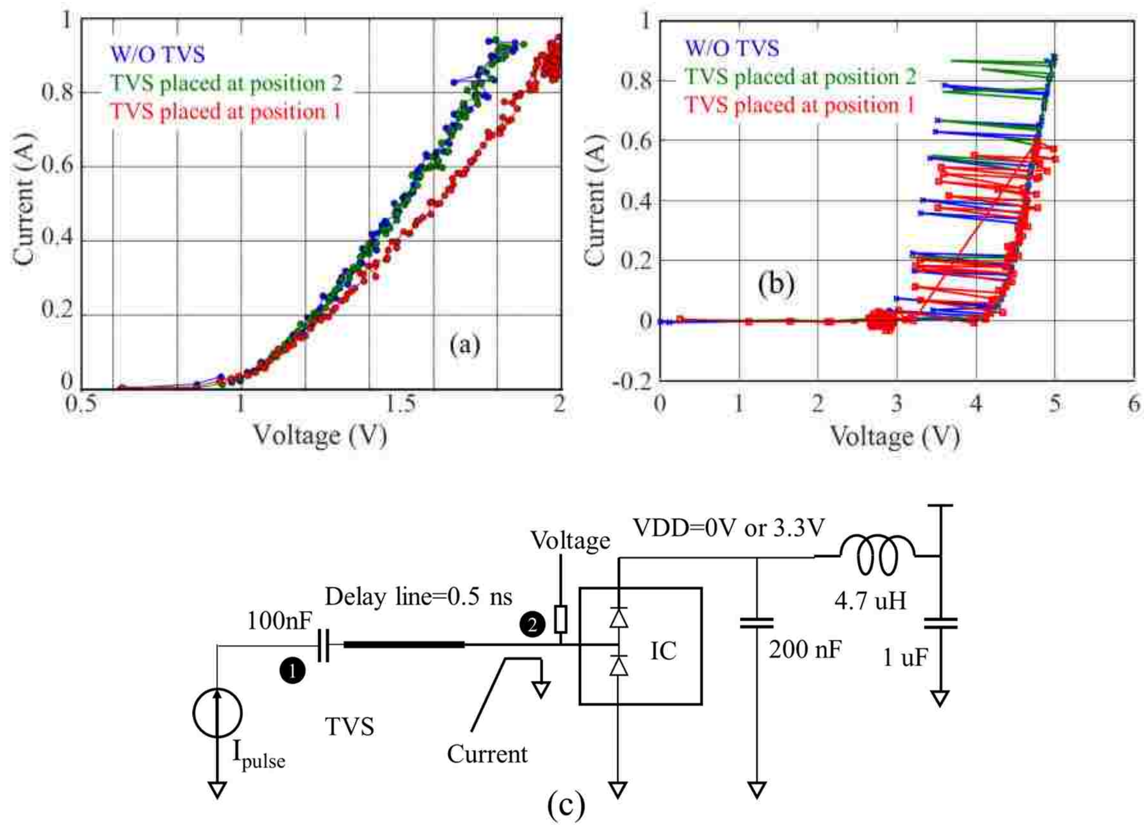

Figure 3.19. Quasi-static IV curve measured at the IO pin for different TVS positions, VDD = 0 V (a), VDD = 3.3 V (b), circuit diagram (c)

This effect explains the growing portion of the current waveform in Figure 3.14(c) and Figure 3.16(b). If there is no path for the capacitor to be discharged after injection, then it is highly possible that a USB device plug into the system could be damaged.

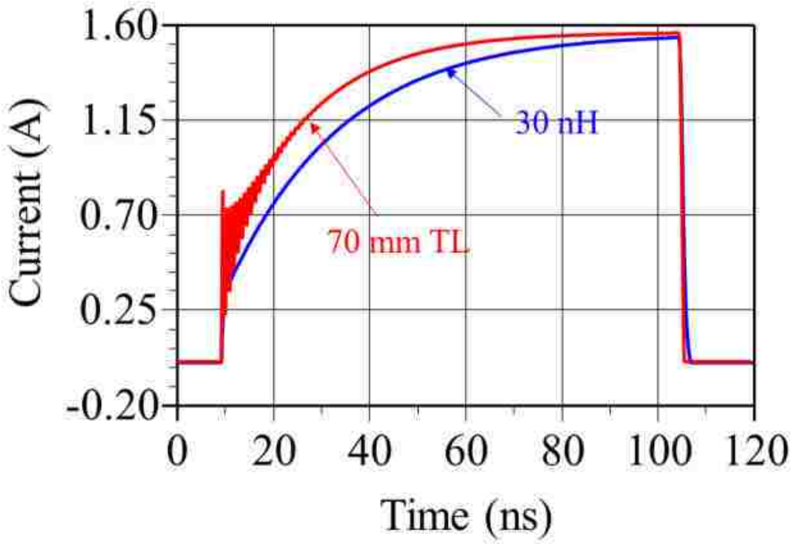

Figure 3.20. Inductive effect of the 70 mm transmission line

3.4.2.2. Capacitors. During the TLP injection, the capacitors (DC block capacitor and the decoupling capacitor) are charged. Hence, the TVS sees a more significant voltage (for a 2 A TLP injection, the 200 nF capacitor is charged to 2 V) at its input and gradually conducts more current. Figure 3.21 shows the effect of the capacitors being charged up during the injection. If both the DC block capacitor and the decoupling capacitor are both shorted, only the inductive effect could be seen.

While the TLP source is grounded after the application of the pulse, in case of the use of the ESD gun as injection source, the tip of the ESD gun is actually left floating after the injection. Thus, the charges remain in the DC block capacitor, consequently influences the system response of the next injection. (Note: According to IEC61000-4-2, the system should be discharged after every injection.)

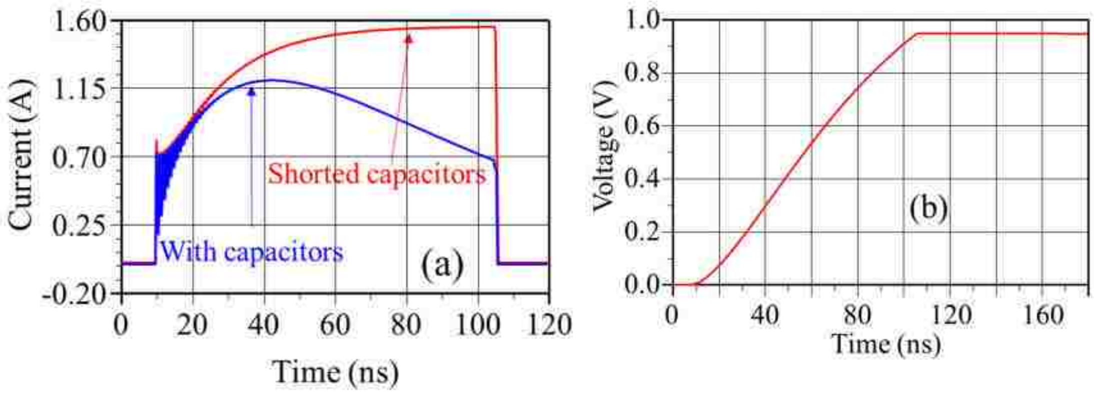

Figure 3.21. Capacitor effect during a 100 V TLP injection to the system. Comparison of shorted and unshorted capacitors effects (a), and the voltage across the DC block capacitor (b)

Figure 3.22 compares the voltage and current waveform measured at the IO pin during the first HMM injection and the 20th HMM injection. It can be observed that the voltage of the 20th injection has been pulled down to below 0 V.

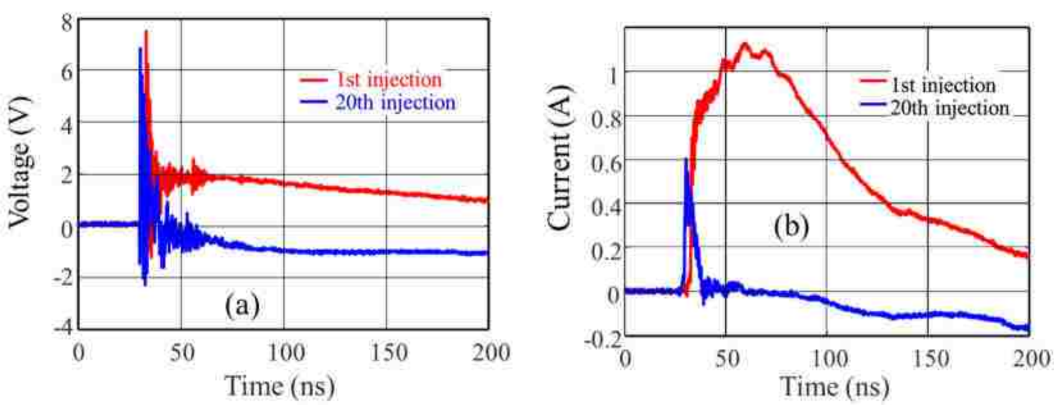

Figure 3.22. Comparison of the voltage and current response at the IO pin during the 1st HMM injection and the 20th HMM injection.

During an ESD event, when TVS is turned on, the input node of the TVS has been pull to “GND” and the DC block capacitor is trying to maintain the voltage across it, hence, the voltage of the IC side reversed to negative. Due to the discharge path of the IC side is high resistance, the voltage will remain negative during the ESD event. On the other hand, before the TVS is turned on, the voltage at the TVS input is higher for the 20th injection than the 1st injection. Hence, the TVS turns on much faster if multiple discharges are applied.

3.4.2.3. Series resistor. Since the ESD current flows into the IO pin is not significantly bypassed by the TVS device in the unpowered system, adding a series resistor is a practical method of limiting the current. Figure 3.23 (a) is the measurement result of using different values of the series resistor during the 100 V TLP injection. A reduction of peak current into the IO can be seen.

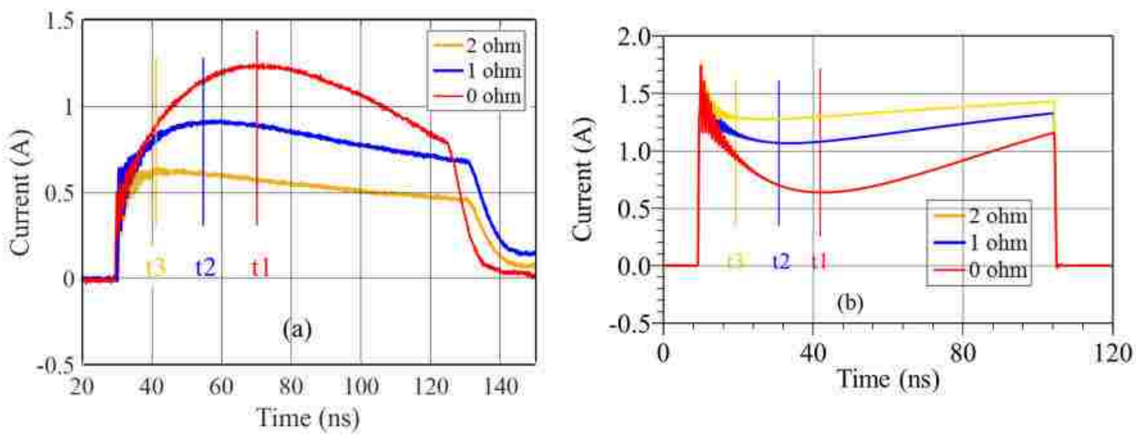

Figure 3.23. Measured current flows into the IO pin when different values of series resistor are used (a), simulated current flows through the TVS when different values of series resistor are used (b)

In Figure 3.23 (b), it can also be observed that the larger resistance of the series resistor the current into the TVS increases faster. This can be explained by the voltage drop of series resistor which boosts the voltage at the input of the TVS device and triggers the TVS faster.

3.5. SUMMARY AND FUTURE WORK

A PCB has been designed for simulating the ESD protection of a USB 3.x repeater IC in conjunction with different external protection diodes. The purpose of the board is to illustrate SEED simulations which are verified by measurements. For this reason, voltage and current measurement ports are included on the board. The board will be used in a round robin test of SEED simulation [31].

From the SEED simulation results, the reactions of the passive components during an ESD event are of considerable importance, the core findings here are:

1) The transmission line between the TVS device and the IO pin delays the clamping behavior of the on-chip ESD protection, therefore the TVS can be turned on even though the V_{t1} of the TVS diode is much larger than that of the on-chip protection.

2) The capacitors (DC block capacitor and the decoupling capacitor) series in the current path can be charged up during the ESD event, the voltage drop across the capacitors increases the voltage at the input of the TVS, thus, helps the TVS to be triggered.

3) The series resistor can be used additionally to limit the current flows into the IO pin.

4) The off-chip ESD protection gives much better protection for the powered IC, because the trigger voltage of the on-chip ESD protection increases after Vdd is applied.

Finally, the measurement results validate our proposed SEED simulation model, the modeling method can be applied to other high-speed interfaces.

The test boards were sent to multiple labs, the next steps of this work are collecting data from the labs that have joined the round robin test, comparing the measurement results and simulation results among labs.

4. CONCLUSION

In Section 2, the transient behavior modeling method has been proposed for various ESD protection devices. It allows to predict the transient behaviors such as snapback delay (static time lag for spark gap), conductivity modulation and quasi-static IV curve. The model has been validated by both TLP injection and ESD gun test.

In Section 3, a PCB has been developed to measure the transient response of the IO pin under various scenarios, such as power on/off, different positions of the protection device, with and without decoupling capacitors. A full system level model has been introduced including the source model, TVS model, passive components model and the IO pin model. Finally, the simulation results are validated by the measurement results.

APPENDIX A.

TRANSIENT MODEL EXTRACTION PROCEDURE

In this section, the parameters extraction of one TVS (PESD3V3Z1BSF) sample and the tuning process is described. Table A.1 lists all the nine parameters needed to be tuned, their effects to the small/large signal behavior, and it explains which measurement is needed to tune them.

Table A.1 Parameters that need to be tuned and their effects

Parameters	**Sub-model**	**Small signal effects**	**Large signal effects**	**Measurement**
L1	Linear small signal	Small signal bandwidth	Inductive voltage overshoot	VNA S-parameter
C1	Linear small signal	Small signal bandwidth	Current overshoot if the capacitance is large	VNA S-parameter
R2	Linear small signal	Depth of the resonance	Current overshoot	VNA S-parameter
V_{t1}	Snapback delay	No effect	Snapback voltage of the quasi-static VI curve	100ns TLP
Snapback trigger	Snapback delay	No effect	Snapback delay time	VF TLP
Diode quasi-static VI after snapback	Quasi-static VI curve	No effect	Quasi-static VI curve	100ns TLP
Pre-clamping diode before snapback	VI curve	No effect	Voltage clamped by the triggering component inside the TVS before snapback.	VF-TLP
$R_{turnoff}$	Conductivity modulation	No effect	Non-inductive overshoot	VF-TLP
V_{turnon}	Conductivity modulation	No effect	Non-inductive overshoot; Time constant of the forward recovery; fully turn on time	VF-TLP

A. SMALL SIGNAL PARAMETERS

The linear small signal model characterization is performed according to the method discussed in [15].

The steps to create the small signal model are:

1. Mount the DUT on a series through test fixture shown in Figure A.1, then measure S21 and calculate the junction capacitance(C1) use the equation in:

$$Z_{DUT} = \frac{100(1-S21)}{S21} \quad (1)$$

$$Z_{DUT} = \left|\frac{1}{j\omega C1}\right| \quad (2)$$

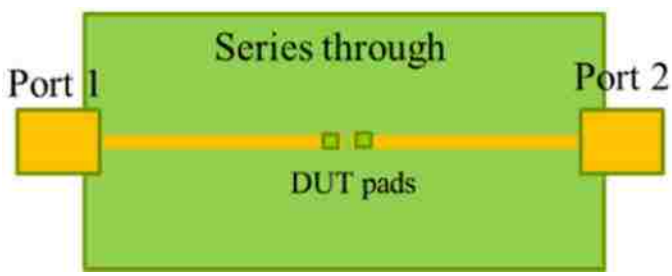

Figure A.1 Series through test fixture

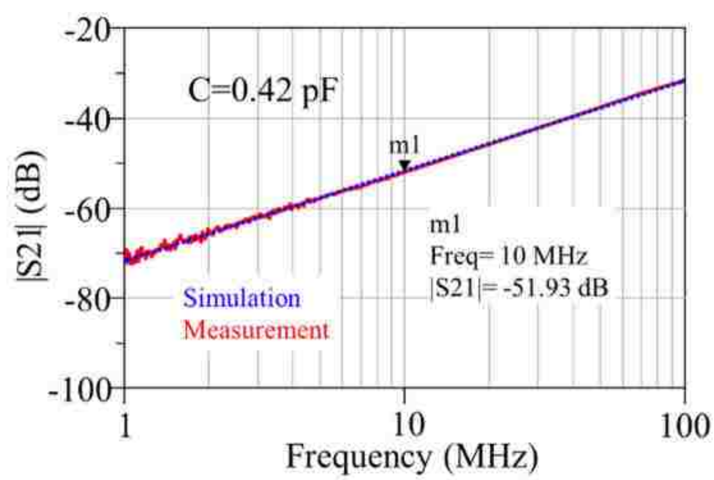

Figure A.2 Measured frequency response of a TVS DUT

An example of the measured series through S21 is shown in Figure A.2. The capacitance for this TVS sample is 0.42 pF.

2. Mount the DUT on a shunt through fixture which is shown in Figure A.3. This provides the resonance frequency, using the capacitance value (C1) measured from the previous step, the inductance (L1) and the effective series resistance at resonance (R2) are calculated using:

$$j\omega L1 = 1/j\omega C1 \tag{3}$$

$$ESR = |25 \times \frac{S21}{1-S21}| \tag{4}$$

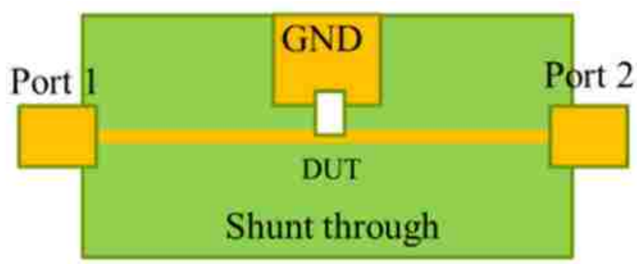

Figure A.3 Shunt through test fixture

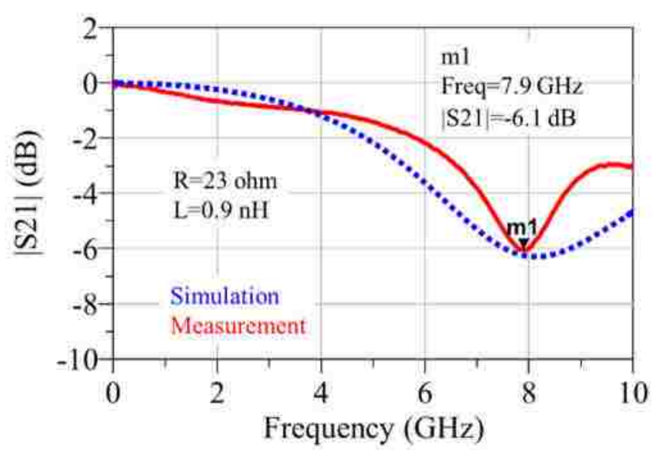

Figure A.4 The shunt through measurement result of the DUT compares to the simulated small signal frequency response

An example of a shunt through measurement result is shown in Figure A.4.

The apparent inductance and the effective series resistance of the TVS sample is 0.9 nH and 23 ohm, respectively. However, the inductance value depends on how the DUT is mounted and the actual inductance in the final application may be different.

B. PRE-CLAMPING DIODE MODEL AND AFTER-SNAPBACK VI DIODE MODEL

The pre-clamping behavior (see Section 2.2.2.1) can be characterized by using the VF-TLP measurement. Three parameters (I_S, R_S and N) of the pre-clamping diode model need to be tuned to fit the measured VI curve before snapback.

The fitted parameters value of the model are:

$$I_S = 1.4\times10^{-20}\text{ A}, R_S = 10\text{ ohm}, N = 8.6$$

Figure A.5 shows the measured quasi-static VI curve before snapback and the simulated VI curve for the pre-clamping diode model.

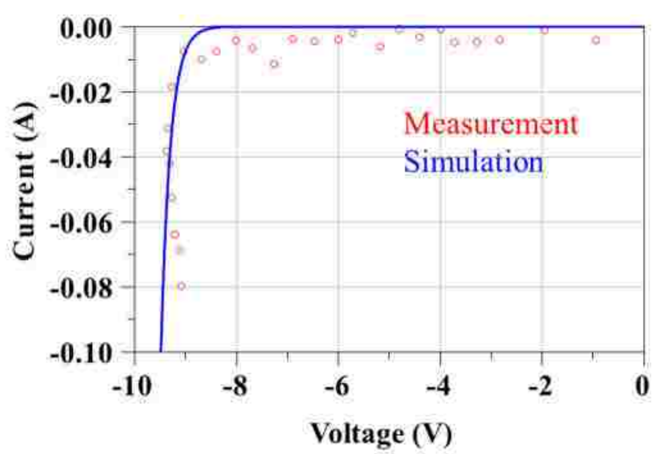

Figure A.5 Measured quasi-static VI curve before snapback and simulated VI curve for the pre-clamping diode model of the DUT

Similarly, the after snapback quasi-static VI diode model can also be created by tuning the three parameters to fit the measurement result. Figure A.6 shows the measured quasi-static VI curve of the TVS sample compared with the fitted VI curve of the after-snapback diode model.

The fitted parameters value of the after-snapback diode model are:

$$I_S = 6 \times 10^{-15}\ \text{A},\ R_S = 0.15\ \text{ohm},\ N = 3.1$$

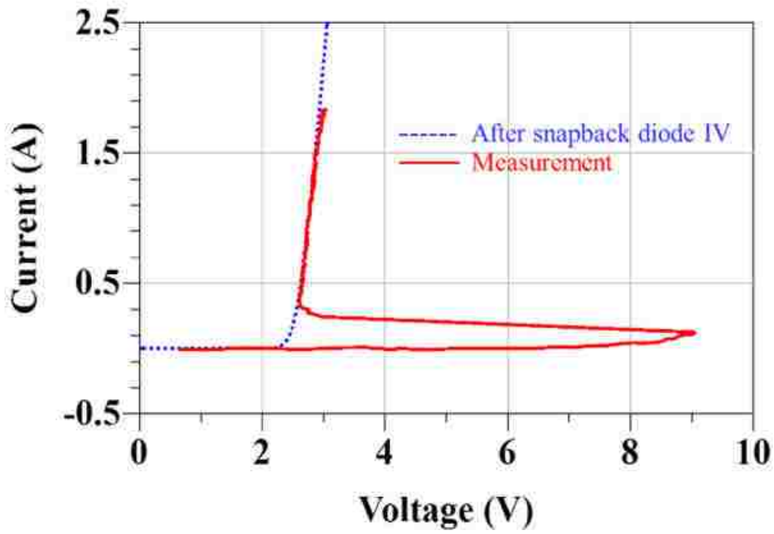

Figure A.6 Measured TVS quasi-static IV curve and the after-snapback diode model IV curve

C. CONDUCTIVITY MODULATION MODEL

The following steps are applied to create the conductivity modulation model:

1. Select one of the time domain current waveforms that clearly shows the turn on behavior. In this example, a -25 V TLP injection result was selected and is shown in Figure A.7;

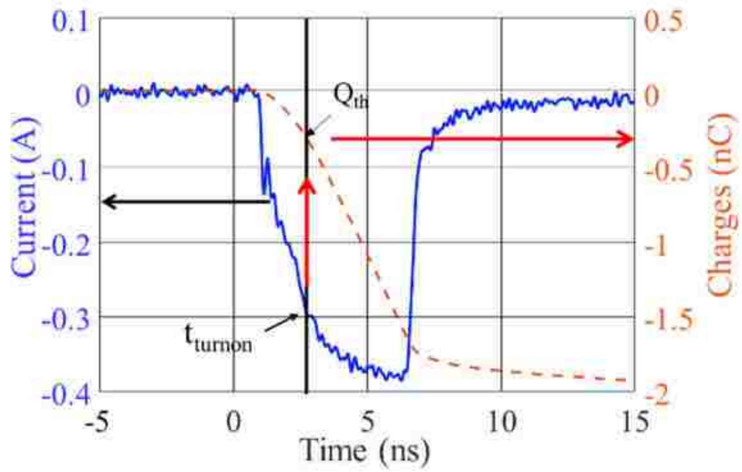

Figure A.7 Measured current waveform of -40 V TLP injection and integration of current over time

2. Identify the turn on moment (t_{turnon}) and find the related total charges (Q_{th}) at t_{turnon} as Q_{th} is the amount of the injected charge that is sufficient to approximately increase the channel conductivity to its final value, such that a quasi-static VI curve describes the behavior. In the example, Q_{th} is observed as 0.38 nC;

3. Specify the C_{switch} to 100 pF and determine the V_{turnon} using (7). Here the V_{turnon} is the voltage value at which the switch turns on.

V_{turnon} in the model is the control voltage for the "ON" state of the switch (R_M) in the model. For the "OFF" state, the control voltage is 0 V;

5. To obtain the "OFF" state resistance ($R_{turnoff}$) of R_M, we need to first distinguish the inductive overshoot from the total overshoot.

Figure A.8 shows the voltage and current waveform of a 40 V TLP injected into the TVS sample.

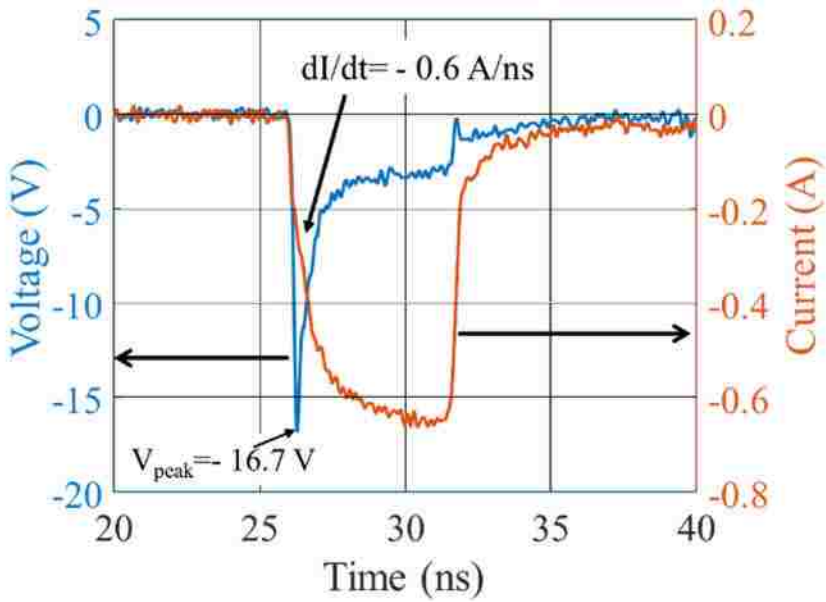

Figure A.8 Voltage and current waveform of 40 V TLP injection to the TVS sample

The peak voltage is -16.7 V and the peak value of current derivative is 0.6 A/ns. The inductive overshoot can be calculated by

$$V_{ind} = \frac{L \cdot dI}{dt} \tag{5}$$

$$R_{turnoff} = \frac{V_{peak} - V_{ind}}{I} \tag{6}$$

The resistance value can be derived as 25 ohm. R_{turnon} as the "ON" state resistance of R_M is set to 1 milliOhm.

6. Finally, the V_{turnon} and $R_{turnoff}$ value need to be fine-tuned to match the measured waveforms.

D. SNAPBACK DELAY MODEL

The steps for creating the snapback delay model are:

1. Extract V_{t1} from the quasi-static VI curve of the 100 ns TLP measurement result. The value for the given TVS sample is 9 V as shown in Figure A.9.

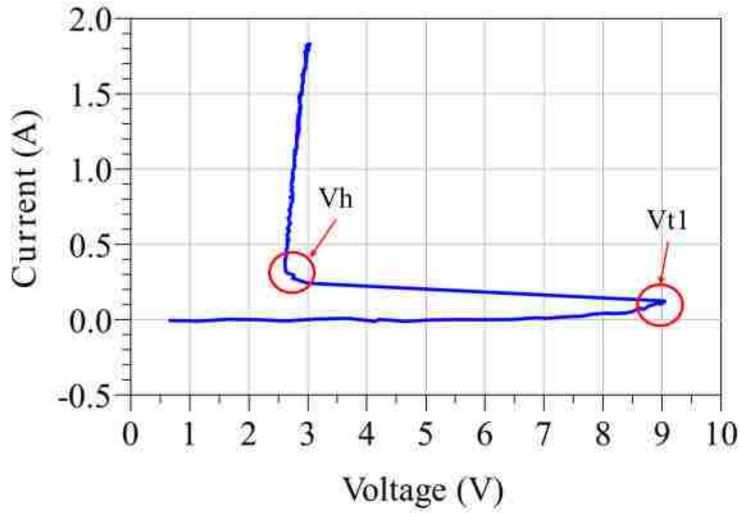

Figure A.9 Quasi-static VI curve taken from the100 ns TLP measurement result for the selected TVS sample

2. Select one of the voltage waveforms around the V_h point in the quasi-static VI curve from the VF-TLP measurements. Figure A.10 shows the voltage waveform of 24 V TLP injection result for the given TVS sample.

3. Identify the snapback moment $t_{snapback}$ from the waveform as the point in time where the voltage drops below V_{t1}.

4. Integrate $V_{TVS} - V_{t1}$ from t_0 to $t_{snapback}$. The red curve in Figure A.10 shows the result of this integration. A value of 1V·ns is then selected for "*snapback_trigger*".

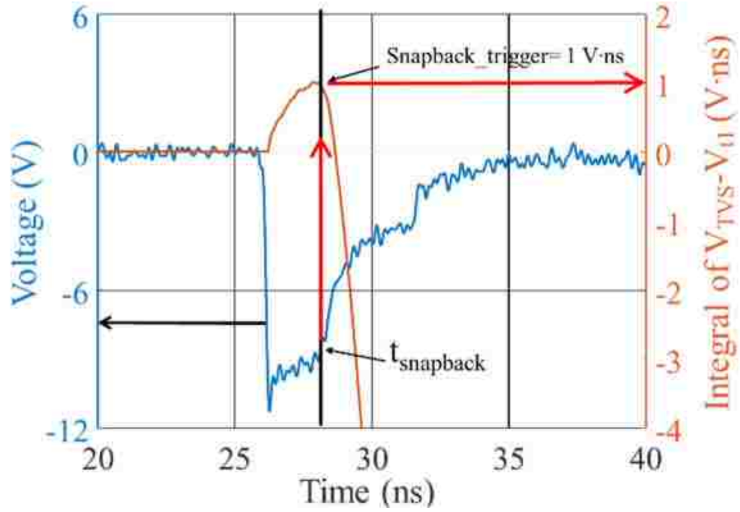

Figure A.10 Voltage waveform of 24 V VF-TLP injection to the selected TVS sample and the integration result of V_{TVS}-V_{t1}

5. In the model, the "*snapback_trigger*" is the control voltage of the "ON" state of the snapback switch. The "OFF" state control voltage is set as "*snapback_trigger*" – 0.1 V to ensure the transition is fast enough. Correspondingly, the "ON" and "OFF" state resistance are set to 1 milliOhm and 1 GOhm respectively.

6. Finally, the value of "*snapback_trigger*" needs to be fine-tuned to match the measurement results for both high level and low level injections.

APPENDIX B.

MODELS CREATED BY THE TRANSIENT BEHAVIOR MODELING METHOD

A. INTRODUCTION

Included with this thesis, 11 models of the ESD protection devices have been created using the transient behavior modeling method. The schematic of each device model is shown as follows.

B. TRANSIENT BEHAVIOR MODEL FRAMEWORK

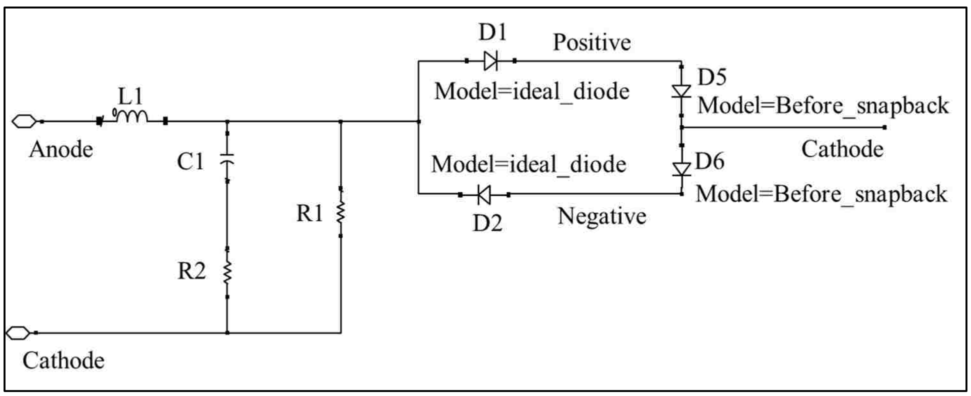

Figure B.1 Small signal, path selection and IV before snapback

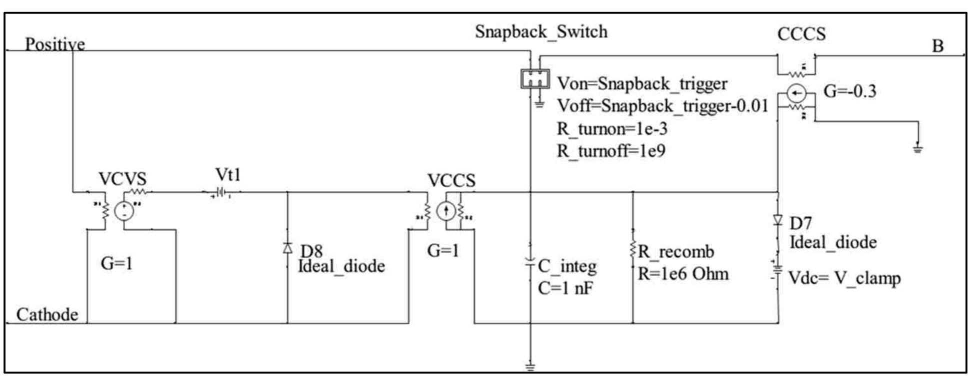

Figure B.2 Snapback delay model of positive path

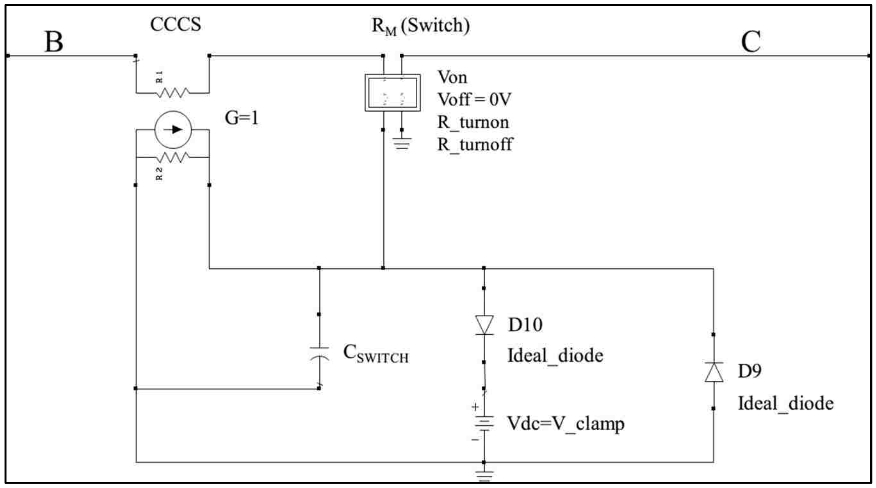

Figure B.3 Conductivity modulation model of positive path

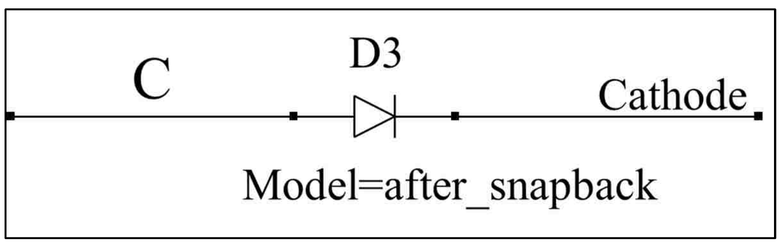

Figure B.4 After snapback IV curve model of positive path

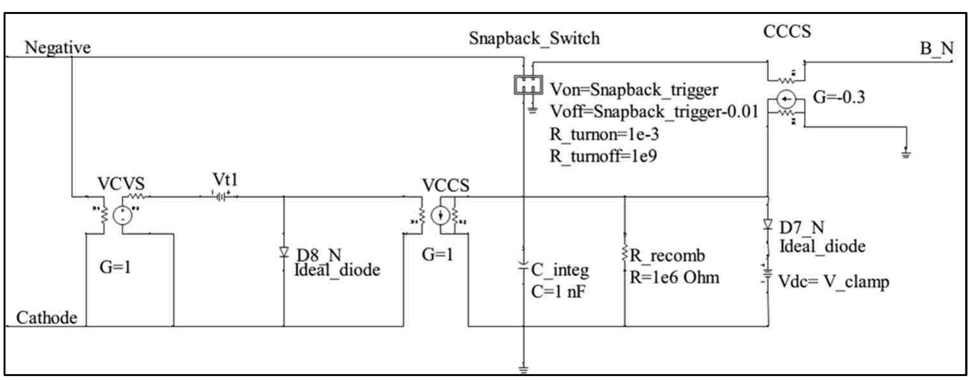

Figure B.5 Snapback delay model of negative path

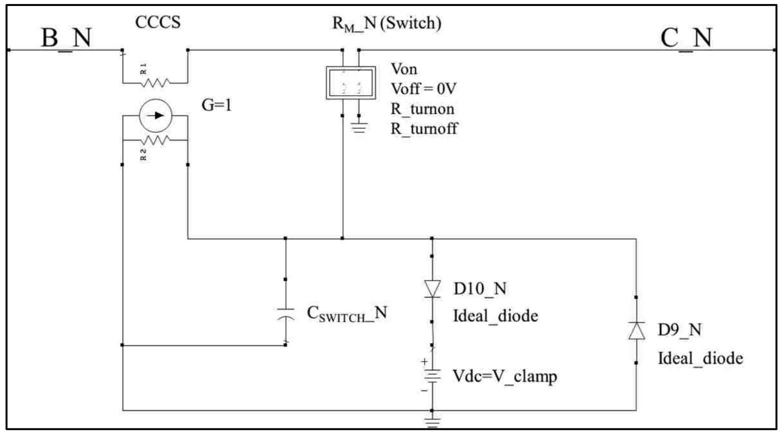

Figure B.6 Conductivity modulation model of negative path

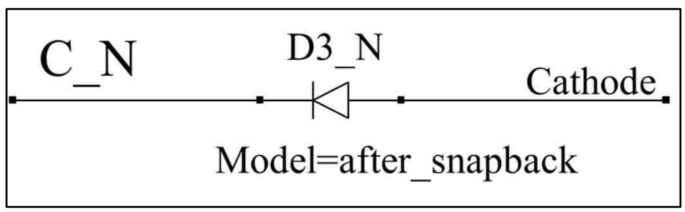

Figure B.7 After snapback IV curve model of negative path

For all the switch model, R_turnon is set to 1e-3, and it is not necessary to be tuned in most of the cases.

The parameters for the ideal diode model are listed below:

IS = 1e-14

Rs = 0

N = 1e-2

Note: in ADS the parameter Imax needs to be set as a large value, it has been set to 1e6 for the diode models in this modeling work.

C. MODEL PARAMETERS FOR THE ESD PROTECTION DEVICES

BK33000702

Spark gap.

Parameters	Value	Sub-model
R1	10M ohm	Small signal
R2	10	Small signal
C1	0.3 pF	Small signal
L1	0.7 nH	Small signal
Vt1	700 V	Snapback delay
V_clamp	3000 V	Snapback delay, conductivity modulation
Snapback_trigger	2500	Snapback delay
C_{SWITCH}, C_{SWITCH}_N	1n F	Conductivity modulation
Von (R_M, R_M_N)	100 V	Conductivity modulation
R_turnoff (R_M, R_M_N)	50	Conductivity modulation
Is (D5, D6)	Disable	Pre-clamping diode
Rs (D5, D6)	Disable	Pre-clamping diode
N (D5, D6)	Disable	Pre-clamping diode
Is (D3, D3_N)	1e-15	IV after snapback
Rs (D3, D3_N)	0.15	IV after snapback
N (D3, D3_N)	20	IV after snapback

AVLC 5S 02 050

Varistor

Parameters	Value	Sub-model
R1	10M ohm	Small signal
R2	0.5	Small signal
C1	42 pF	Small signal
L1	0.5 nH	Small signal
Vt1	Disable	Snapback delay
V_clamp	100 V	Snapback delay, conductivity modulation
Snapback_trigger	Disable	Snapback delay
C_{SWITCH}, C_{SWITCH}_N	1n F	Conductivity modulation
Von (R_M, R_M_N)	100 V	Conductivity modulation
R_turnoff (R_M, R_M_N)	4	Conductivity modulation
Is (D5, D6)	Disable	Pre-clamping diode
Rs (D5, D6)	Disable	Pre-clamping diode
N (D5, D6)	Disable	Pre-clamping diode
Is (D3, D3_N)	0.0135	IV after snapback
Rs (D3, D3_N)	0.43	IV after snapback
N (D3, D3_N)	241.28	IV after snapback

Note: the varistor is not a snapback device, the node "positive" and "B" are shorted, node "neagtive" and "B_N" are shorted.

PESD5V0C1USF

Uni-polar snapback type TVS diode, low capacitance.

Parameters	Value	Sub-model
R1	10M ohm	Small signal
R2	5	Small signal
C1	0.3 pF	Small signal
L1	0.7 nH	Small signal
Vt1	15 V	Snapback delay
V_clamp	100 V	Snapback delay, conductivity modulation
Snapback_trigger	1.3	Snapback delay
C_{SWITCH}	1n F	Conductivity modulation
Von (R_M)	1 V	Conductivity modulation
R_turnoff (R_M)	20	Conductivity modulation
C_{SWITCH}_N	100p F	Conductivity modulation
Von (R_M_N)	3	Conductivity modulation
R_turnoff (R_M_N)	76	Conductivity modulation
Is (D5, D6)	Disable	Pre-clamping diode
Rs (D5, D6)	Disable	Pre-clamping diode
N (D5, D6)	Disable	Pre-clamping diode
Is (D3)	1e-18	IV after snapback
Rs (D3)	0.127	IV after snapback
N (D3)	1.21	IV after snapback
Is (D3_N)	1e-18	IV after snapback
Rs (D3_N)	0.133	IV after snapback
N (D3_N)	1.18	IV after snapback

Note: for negative path, the node “Negative” and “B_N” are shorted.

PESD3V3Z1BSF

Bi-polar snapback type TVS diode, low capacitance

Parameters	Value	Sub-model
R1	10M ohm	Small signal
R2	10	Small signal
C1	0.3 pF	Small signal
L1	0.07 nH	Small signal
Vt1	9 V	Snapback delay
V_clamp	100 V	Snapback delay, conductivity modulation
Snapback_trigger	1.2	Snapback delay
C_{SWITCH}, C_{SWITCH}_N	100p F	Conductivity modulation
Von (R_M, R_M_N)	15 V	Conductivity modulation
R_turnoff (R_M, R_M_N)	20	Conductivity modulation
Is (D5, D6)	1e-20	Pre-clamping diode
Rs (D5, D6)	14	Pre-clamping diode
N (D5, D6)	7	Pre-clamping diode
Is (D3, D3_N)	1e-18	IV after snapback
Rs (D3, D3_N)	0.127	IV after snapback
N (D3, D3_N)	1.21	IV after snapback

PESD5V0H1BSF

Bi-polar snapback TVS diode, low capacitance.

Parameters	Value	Sub-model
R1	10M ohm	Small signal
R2	10	Small signal
C1	0.3 pF	Small signal
L1	0.07 nH	Small signal
Vt1	19 V	Snapback delay
V_clamp	100 V	Snapback delay, conductivity modulation
Snapback_trigger	1.1	Snapback delay
C_{SWITCH}, C_{SWITCH}_N	100p F	Conductivity modulation
Von (R_M, R_M_N)	15 V	Conductivity modulation
R_turnoff (R_M, R_M_N)	40	Conductivity modulation
Is (D5, D6)	1e-18	Pre-clamping diode
Rs (D5, D6)	10	Pre-clamping diode
N (D5, D6)	19.5	Pre-clamping diode
Is (D3, D3_N)	1e-18	IV after snapback
Rs (D3, D3_N)	0.227	IV after snapback
N (D3, D3_N)	2.3	IV after snapback

PESD5V0S1USF

High capacitance(42pF) unipolar Zener diode.

Parameters	Value	Sub-model
R1	10M ohm	Small signal
R2	100	Small signal
C1	42 pF	Small signal
L1	0.2 nH	Small signal
Vt1	Disable	Snapback delay
V_clamp	100 V	Snapback delay, conductivity modulation
Snapback_trigger	Disable	Snapback delay
C_{SWITCH}, C_{SWITCH_N}	1n F	Conductivity modulation
Von (R_M)	3 V	Conductivity modulation
R_turnoff (R_M)	0.5	Conductivity modulation
Von (R_{M_N})	2.3 V	Conductivity modulation
R_turnoff (R_{M_N})	0.9	Conductivity modulation
Is (D5, D6)	Disable	Pre-clamping diode
Rs (D5, D6)	Disable	Pre-clamping diode
N (D5, D6)	Disable	Pre-clamping diode
Is (D3)	6.8e-21	IV after snapback
Rs (D3)	0.5	IV after snapback
N (D3)	6	IV after snapback
Is (D3_N)	6.8e-21	IV after snapback
Rs (D3_N)	0.37	IV after snapback
N (D3_N)	0.9	IV after snapback

Note: the Zener diode is not a snapback device, the node “positive” and “B” are shorted, node “neagtive” and “B_N” are shorted.

ESD102-U1-02ELS

Uni-polar snapback type TVS diode, low capacitance.

Parameters	Value	Sub-model
R1	10M ohm	Small signal
R2	100	Small signal
C1	0.5 pF	Small signal
L1	0.7 nH	Small signal
Vt1	6.5 V	Snapback delay
V_clamp	100 V	Snapback delay, conductivity modulation
Snapback_trigger	1	Snapback delay
C_{SWITCH}	2n F	Conductivity modulation
Von (R_M)	5 V	Conductivity modulation
R_turnoff (R_M)	5	Conductivity modulation
C_{SWITCH}_N	1p F	Conductivity modulation
Von (R_M_N)	20	Conductivity modulation
R_turnoff (R_M_N)	400	Conductivity modulation
Is (D5)	1e-11	Pre-clamping diode
Rs (D5)	50	Pre-clamping diode
N (D5)	13.55	Pre-clamping diode
IS, Rs, N (D6)	Disable	Pre-clamping diode
Is (D3)	1e-18	IV after snapback
Rs (D3)	0.294	IV after snapback
N (D3)	4.1	IV after snapback
Is (D3_N)	1.7e-15	IV after snapback
Rs (D3_N)	0.25	IV after snapback
N (D3_N)	1.09	IV after snapback

Note: for negative path, the node “Negative” and “B_N” are shorted.

DF2S5M4SL

Uni-polar snapback type TVS diode, low capacitance.

Parameters	Value	Sub-model
R1	10M ohm	Small signal
R2	100	Small signal
C1	0.38 pF	Small signal
L1	2 nH	Small signal
Vt1	8 V	Snapback delay
V_clamp	100 V	Snapback delay, conductivity modulation
Snapback_trigger	3	Snapback delay
C_{SWITCH}	1n F	Conductivity modulation
Von (R_M)	8.96 V	Conductivity modulation
R_turnoff (R_M)	13.55	Conductivity modulation
C_{SWITCH}_N	1p F	Conductivity modulation
Von (R_M_N)	20	Conductivity modulation
R_turnoff (R_M_N)	400	Conductivity modulation
Is (D5)	1.4e-20	Pre-clamping diode
Rs (D5)	10	Pre-clamping diode
N (D5)	8.6	Pre-clamping diode
IS, Rs, N (D6)	Disable	Pre-clamping diode
Is (D3)	8e-15	IV after snapback
Rs (D3)	0.4	IV after snapback
N (D3)	7	IV after snapback
Is (D3_N)	6.96e-11	IV after snapback
Rs (D3_N)	0.3	IV after snapback
N (D3_N)	1.9	IV after snapback

Note: for negative path, the node “Negative” and “B_N” are shorted.

DF2S5.6

High capacitance(42pF) unipolar Zener diode.

Parameters	Value	Sub-model
R1	10M ohm	Small signal
R2	50	Small signal
C1	40 pF	Small signal
L1	0.3 nH	Small signal
Vt1	Disable	Snapback delay
V_clamp	100 V	Snapback delay, conductivity modulation
Snapback_trigger	Disable	Snapback delay
C_{SWITCH}, C_{SWITCH}_N	1n F	Conductivity modulation
Von (R_M)	3.8 V	Conductivity modulation
R_turnoff (R_M)	1.5	Conductivity modulation
Von (R_M_N)	1.6 V	Conductivity modulation
R_turnoff (R_M_N)	2	Conductivity modulation
Is (D5, D6)	Disable	Pre-clamping diode
Rs (D5, D6)	Disable	Pre-clamping diode
N (D5, D6)	Disable	Pre-clamping diode
Is (D3)	6.8e-21	IV after snapback
Rs (D3)	0.19	IV after snapback
N (D3)	6	IV after snapback
Is (D3_N)	4.2e-6	IV after snapback
Rs (D3_N)	0.27	IV after snapback
N (D3_N)	18.725	IV after snapback

Note: the Zener diode is not a snapback device, the node “positive” and “B” are shorted, node “neagtive” and “B_N” are shorted.

uClamp2801T

High capacitance(42pF) unipolar Zener diode.

Parameters	Value	Sub-model
R1	10M ohm	Small signal
R2	20	Small signal
C1	25 pF	Small signal
L1	0.7 nH	Small signal
Vt1	Disable	Snapback delay
V_clamp	100 V	Snapback delay, conductivity modulation
Snapback_trigger	Disable	Snapback delay
C_{SWITCH}, C_{SWITCH}_N	1n F	Conductivity modulation
Von (R_M)	1 V	Conductivity modulation
R_turnoff (R_M)	0.5	Conductivity modulation
Von (R_M_N)	0.1V	Conductivity modulation
R_turnoff (R_M_N)	100	Conductivity modulation
Is (D5, D6)	Disable	Pre-clamping diode
Rs (D5, D6)	Disable	Pre-clamping diode
N (D5, D6)	Disable	Pre-clamping diode
Is (D3)	4e-16	IV after snapback
Rs (D3)	0.1	IV after snapback
N (D3)	0.98	IV after snapback
Is (D3_N)	5e-21	IV after snapback
Rs (D3_N)	0.67	IV after snapback
N (D3_N)	30.125	IV after snapback

Note: the Zener diode is not a snapback device, the node “positive” and “B” are shorted, node “neagtive” and “B_N” are shorted.

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