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ESD RELATED SOFT ERROR DETECTION

AND ROOT CAUSE ANALYSIS

by

SUYU YANG

A THESIS

Presented to the Graduate Faculty of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

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Approved by

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ABSTRACT

In this article, several methods are outlined for detecting functional changes in an IC due to external interference such as ESD or EMI. The goal is to provide diagnostic tools for detection of potential soft failure susceptibilities of complex systems during the hardware design stage without the aid of any complex software. After the soft errors are found, circuit modeling techniques are used to characterize the DUT. By running the circuit model, the soft error threshold can be predicted and the circuit model can be used to evaluate the performance of other ESD protection methods. In the end several methods are used to separate local soft-failures from distant errors related to noise on the power distribution network (PDN) is demonstrated. Two approaches are used, one passive and one active, which duplicate the noise on a system PDN caused by some intentional injection onto a second system where the intentional injection is not present.

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TABLE OF CONTENTS

Page

ABSTRACT iii

ACKNOWLEDGMENTS iv

LIST OF ILLUSTRATIONS vii

LIST OF TABLES ix

NOMENCLATURE x

SECTION

1. INTRODUCTION 1

1.1. OBJECTIVE AND MOTIVATION 1

1.2. METHODOLOGIES 2

2. PREDICTING THE SOFT FAILURE SUSCEPTIBILITY OF A DUT 3

2.1. INTRODUCTION 3

2.2. SOFT FAILURE DETECTION BASED ON CURRENT CONSUMPTION ... 4

2.3. SOFT FAILURE DETECTION BASED ON THERMAL IMAGING 6

2.4. SOFT FAILURE DETECTION BASED ON EM FIELD SCANNING 8

2.5. CONCLUSION FOR SOFT FAILURE DETECTION 12

3. IC MODELING TECHNIQUES FOR DISTANT ERROR PREDICTION 14

3.1. INTRODUCTION 14

3.2. IC MODELING TECHNIQUES 14

3.3. SOFT FAILURE DETECTION USING TLP 18

3.4. IC MODELING PROCEDURE 25

3.5. SOFT FAILURE PREDICTION BASED ON IC MODEL 39

3.6. CONCLUSION 42

4. PDN NOISE INJECTION FOR SOFT FAILURE ROOT CAUSE ANALYSIS 43

4.1. INTRODUCTION 43

4.2. SOFT FAILURE DETECTION METHODOLOGY 43

4.3. MIRRORED (PASSIVE) PERTURBATION 44

4.4. PLAYBACK VIA ARBITRARY WAVEFORM INJECTION 47

4.5. CONCLUSION 48

5. CONCLUSION AND FUTURE WORK 50
BIBLIOGRAPHY 52
VITA. 53

LIST OF ILLUSTRATIONS

Page

Figure 1.1. Simplified PDN inside a portable electronics product. 1
Figure 2.1. Step change in DC current consumption triggered by latch up. 5
Figure 2.2. The current consumption during an interference-induced reboot 6
Figure 2.3. DUT placed inside an opaque screen with TLP injection probe. 7
Figure 2.4. Thermal emissions of DUT during an ESD-induced restart. 7
Figure 2.5. Time-domain near-field scanning and IC orientation. 9
Figure 2.6. Observed Hx field spectrum during a continuous GPIO polling operation. .. 10
Figure 2.7. Observed Hx field spectrum above the DUT during a GPIO read error. 11
Figure 2.8. Observed Hx field spectrum above the DUT during an ADC read. 12
Figure 2.9. Observed Hx field spectrum above the DUT during an ADC read error. 13
Figure 3.1. VNA measurement setup for IC PDN. 15
Figure 3.2. Z11 measurement and simulation of IC power pin 44. 16
Figure 3.3. Reflective measurement system. 17
Figure 3.4. Waterfall plot generation flow chart. 17
Figure 3.5. Use 50 Ohm as DUT, 3D view of the waterfall plot. 18
Figure 3.6. Arduino Leonardo board. 19
Figure 3.7. Software error detection flow chart. 21
Figure 3.8. I/O injection setup block diagram. 22
Figure 3.9. Hardware setup for soft error detection. 22
Figure 3.10. IC pin definitions. 25
Figure 3.11. VNA measurement setup for IC PDN. 27
Figure 3.12. S21 measurement of IC power pins. 27
Figure 3.13. Z11 measurement of IC power pin 2. 29
Figure 3.14. Z11 measurement and simulation of IC power pin 44. 29
Figure 3.15. Z11 measurement and simulation of IC power pin 14&44. 30
Figure 3.16. Z11 measurement and simulation of IC power pin 24&34. 31
Figure 3.17. Reflective measurement system block diagram and settings. 32
Figure 3.18. Using 8.5 Ohm as DUT, 3D view of the waterfall plot. 33

Figure 3.19. IC measurement result: Pin 24 AVCC to pin 34 VCC. 34
Figure 3.20. Pin 24 - Pin 34 IV curve measurement and simulation result. 35
Figure 3.21. Pin 24 - Pin 34 models... 35
Figure 3.22. Complete model of IC PDN. 36
Figure 3.23. IO pin model measurement block diagram. 37
Figure 3.24. IO pin PD6 model.. 37
Figure 3.25. PD6 IV curve measurement vs simulation 38
Figure 3.26. PDN model simulation vs measurement at different voltage level. 39
Figure 3.27. IC soft error test block diagram. 40
Figure 3.28. Simulation block diagram before adding 10 Ohm resistor. 40
Figure 3.29. Soft error threshold – reference case. 41
Figure 3.30. Simulation block diagram after adding 10 Ohm resistor. 41
Figure 3.31. Soft error threshold – after adding 10 Ohm resistor case. 42
Figure 4.1. Stress program structure. 44
Figure 4.2. TLP Injection probe landed on the DUT. 44
Figure 4.3. Schematic representation of the image injection method. 45
Figure 4.4. Photograph of the joined DUTs. 45
Figure 4.5. The mirrored voltage disturbance at pin 34 (VCC) on the two DUTs. 46
Figure 4.6. AWG Injection flowchart. 47
Figure 4.7. The generated voltage disturbance at pin 34 (VCC) on the two DUTs.......... 48

LIST OF TABLES

Page

Table 3.1. Test result for I/O pin read error – 1. 23
Table 3.2. Test result for I/O pin read error – 2. 24
Table 3.3. Test result for EEPROM read/write error. 24
Table 3.4. IC pin DC measurement results. 26
Table 4.1. Mirrored Perturbation Failure Results. 46
Table 4.2. Active PDN Disturbance 48

NOMENCLATURE

Symbol	Description
ESD	Electrostatic Discharge
PDN	Power Distribution Network

1. INTRODUCTION

1.1. OBJECTIVE AND MOTIVATION

ESD can cause many types of soft-errors in portable electronic products, out of which, the visual errors are very critical for the products with displays such as digital cameras and cell phones. Commonly observed soft-errors are the stripes on the display screen, system hang-up, system re-boot and latch-up in some cases. ESD sensitivity of such a product is a function of the individual sensitivities of the ICs, components and traces. Also, the impact of ESD on one section (either an IC or a trace) on other sections is not easy to predict. For example, if the CPU IC is affected by ESD, any peripheral that is controlled by it may malfunction. One such important section of the electronics product, which is connected to many other sections, is the “power distribution network (PDN)”. A typical PDN used in many electronics products is shown in the Figure 1.1. During an ESD event, noise can be induced on the PDN either because of the sensitivity of the some of the ICs (oscillator IC, CPU and other ICs) or due to field coupling to the PDN traces. PDN noise may further cause related errors thereby becoming one of the potential causes of the visual soft-errors. Hence, there is a need to establish a systematic methodology to analyze the effect of ESD induced PDN noise on the electronics product. Such a methodology has been demonstrated in this study by investigating soft-error mechanisms on Arduino Leonardo board and Open-Q 8084 mobile development board.

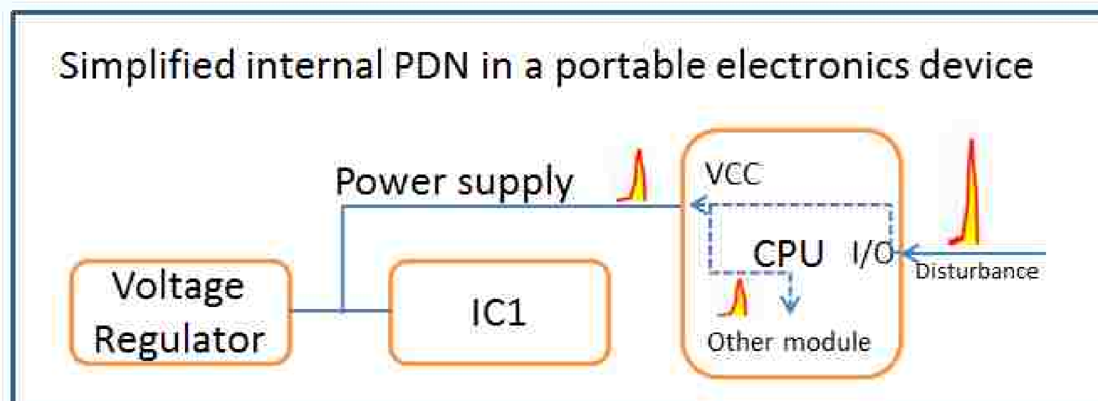

Figure 1.1. Simplified PDN inside a portable electronics product.

1.2. METHODOLOGIES

This study consists of three sections, 1) Measurement Techniques to Predict the Soft Failure Susceptibility of a DUT, 2) IC Modeling Techniques for Distant Error Prediction and 3) Mirrored Power Distribution Network Noise Injection for Soft Failure Root Cause Analysis.

At the beginning, we present three different test methods which can be performed at the hardware level which have the potential of detecting issues caused by EMI or ESD that can lead to incorrect IC functionality.

The closest way of emulating a real ESD event is to perform system level ESD testing of the DUT using ESD simulators. This helps in exposing the soft-errors that can occur inside the DUT in real ESD events, but, it doesn’t provide any further insight into the root cause. So instead performing system level ESD testing, we can perform direct injection on IC to study how the ESD will affect IC’s behavior and check the soft error types and soft error thresholds. In this step, TLP will be used as the noise source to check soft error types and soft error thresholds, because it is convenient to change the ESD pulse shapes such as pulse rise time, pulse width and pulse magnitude, etc. After knowing the soft error types, further study will be needed to characterize the IC, because if we have the IC model, then it will be easier for us to predict how the soft error threshold will change if some protection strategy are applied to the IC. And this is helpful in further system level design. DC measurements, RF measurements and TLP measurements are needed to characterize the IC, and ADS model for the IC is build based on previous measurement results.

After knowing the soft error types and soft error thresholds, further analysis will be needed to find out the root cause of the soft errors and check if the ESD induced soft errors are related to PDN disturbance. Two different methods are developed in this section, one is the image injection method, and the other is the AWG + RF-AMP injection method.

2. PREDICTING THE SOFT FAILURE SUSCEPTIBILITY OF A DUT

2.1. INTRODUCTION

As the complexity of systems increase from both a hardware and software point of view, the potential for soft failures in the final system also increases [1]. Soft failures are system failures that do not result in physical damage. Examples of soft failures are bit errors, unwanted resets, application hang, operation system lock-up, disturbance in displays, etc. For some of the electronic devices such as general purpose evaluation board , laptop or mobile phones on the market, some visible change can be observed when soft failure occur, such as LCD screen hang up, keypad not responding, etc. However, many such soft failures are often not discovered until the system hardware is already finalized and the software team is preparing the product for launch. At this point it is time consuming to make changes to the product hardware in response to soft errors discovered by software design teams. Such problems would be far easier to correct while the hardware designs are still fluid. In order to discover and subsequently correct such issues, the goal must be to detect potential soft-failure causing design errors in the product phase which is on the border between existing hardware and the software that has yet to be written.

In this session we present three different test methods which can be performed at the hardware level which have the potential of detecting issues caused by EMI or ESD that can lead to incorrect IC functionality. The three test methods are:

1. DC current consumption
2. Thermal imaging
3. Electromagnetic field scanning

These tests are performed on several different DUTs with varying results. Because of the extreme difficulty of detecting soft errors without a software platform to disturb, the application of several overlapping tests provides a fuller picture of potential system failures. At most, these tests only require very simple code to be written to activate different subsystems.

In this session, there are two separate DUTs tested with various methods. The first is an Arduino Leonardo, a development board based on the Atmel ATMega32u4

microcontroller. In order to test different functional blocks of this microcontroller, several different short (< 50 lines) programs are looped during the various injection and measurement tests. Such programs are used to read a value from a digital IO pin, an analog input, or to read/write data to the internal EEPROM. These programs are designed to be short and simple as to only stress a small portion of the IC and include a built-in sanity check to test the success of each operation and flag failures by illuminating an LED. In this way, a picture of the susceptibility of the system to soft failures can begin to be constructed even without knowing the final application.

The second DUT is a BeagleBone Black, a single-board computer based on the Texas Instruments AM335x ARM Cortex-A8 CPU. Such a system, being far more complex than the previous DUT, requires slightly more software. This system is loaded with only an operating system (Debian 7.4, kernel version: 3.8.13-bone47). No user level applications(such as music player, video player or other applications with GUI) is running on the DUT, representing a very early stage in system development where only supervisory software or the core thereof has been written.

In all cases, a transmission line pulser (TLP) is used to generate large interference signals. Such signals are injected into the DUTs via several methods such as direct resistive injection, diode injection [2], or field injection [3]. Because of the broad and searching nature of these tests, details of the injection method used to generate the various failures captured in measurement are not discussed in depth.

2.2. SOFT FAILURE DETECTION BASED ON CURRENT CONSUMPTION

With the expansion of battery powered and/or power-conscious designs, small changes in the DC current consumption can provide a picture of the operational state of a system. Systems can be falsely brought into or out of low-power states by external stimulus, and individual ICs can fail by way of nondestructive latch-up or transient latch-up which can change the power state or causes excess loading on power rails leading to reduced noise margins. To detect such changes, the total system current consumption can be monitored during interference tests or, if possible, individual IC supply currents can be monitored to detect more subtle changes in the current consumption of different portions of the system.

Changes in current consumption due to latch-up are often quite significant in low power devices. Figure 2.1 shows such a change in current amounting to a 75% increase in current consumption and cessation of periodic changes in current consumption likely due to wakeup cycles. Noting the scale, this change in consumption is likely permanent, requiring a power cycling of the DUT to recover from. This phenomenon was triggered by a resistive injection on the battery connection pins of the system power management IC (PMIC).

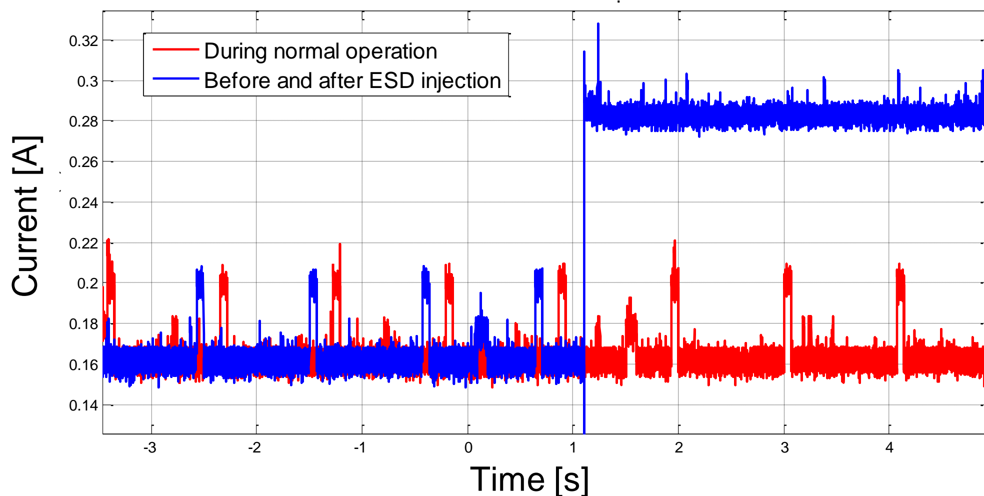

Figure 2.1. Step change in DC current consumption triggered by latch up.

Other phenomenon such as re-starts can easily be seen during injection. The current consumption during an interference-induced reboot compared to the cold-start current is shown in Figure 2.2. It shows the sudden collapse and subsequent increase in current consumption caused by an interference-triggered restart. The failure waveform is compared to a measurement of the current consumption across the first several seconds of a cold-start, strongly indicating that the IC experienced a complete shutdown. This phenomenon was also triggered by a resistive injection on the battery connection pins of the PMIC.

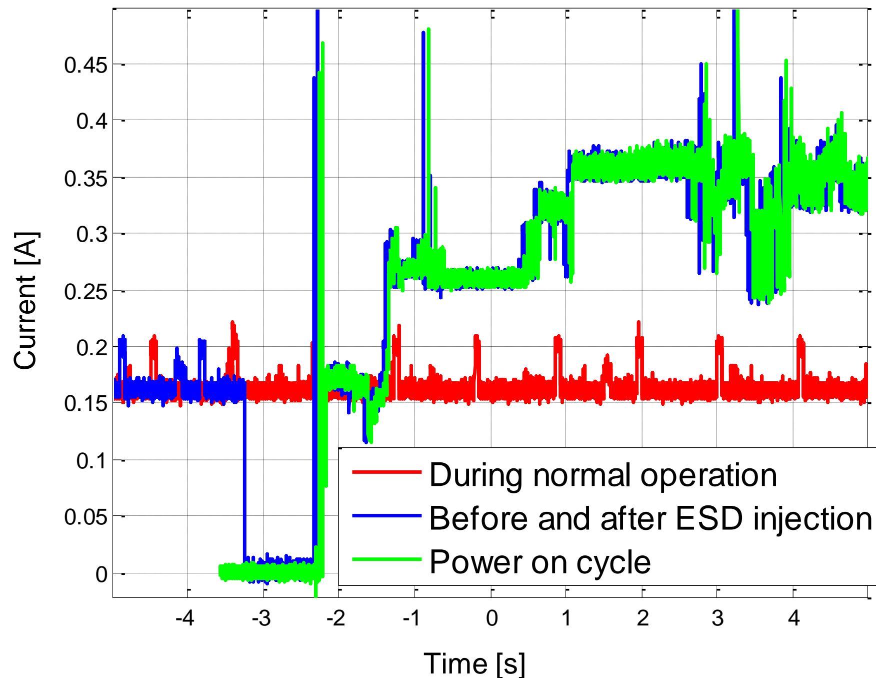

Figure 2.2. The current consumption during an interference-induced reboot

2.3. SOFT FAILURE DETECTION BASED ON THERMAL IMAGING

In many cases, measurement of specific currents may be a difficult task. In such cases, viewing the system with a high-resolution thermal imaging device can quickly show system hot spots. Several such images or real-time video can then be roughly interpreted as a spatial depiction of relative current consumption, not only at the IC level, but throughout the entire system. In such cases where the overall current consumption kdoes not change significantly or simply cannot be measured, detection of shifts in thermal emissions due to changing functionality can rapidly indicate the activation, deactivation, or reset of system components.

The thermal camera used in this study was the TAMARISK 320 from DRS Technologies. This camera allows the user to select from a wide range of gains, making the device suitable for measuring a wide range of temperatures. In this case, the camera was optimized to view temperatures in the range of TEMP1 to TEMP2. The DUT was placed in an opaque enclosure to ensure that it was the primary source of thermal emissions, and the TLP was used to disturb the PMIC via resistive injection, and the

primary processor via field injection. An image of this setup is shown in Figure 2.3. The system was then observed in real-time on the thermal imaging camera to observe changes in the thermal emissions pattern. Injection into the DUT revealed several failure signatures. One such critical signature is an unexpected shutdown and restart. This is often caused by a processor watchdog timer after the system becomes unresponsive or a power supply under voltage event. Figure 2.4 shows a heat-map of the DUT during such a shutdown. The entire event was captured at 25 frames per second (FPS) but the event is neatly captured by only the 2.5 FPS window shown below.

Figure 2.3. DUT placed inside an opaque screen with TLP injection probe.

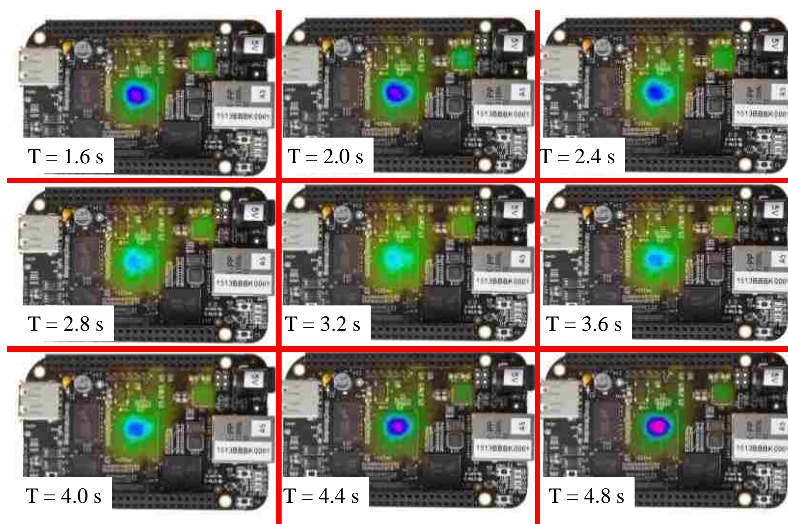

Figure 2.4. Thermal emissions of DUT during an ESD-induced restart.

2.4. SOFT FAILURE DETECTION BASED ON EM FIELD SCANNING

The third technique is to perform a rough measurement of the electric or magnetic field over the DUT. This method can be applied either locally to one IC or other location of interest or globally over the entire DUT to create a map of the fields above the system. Analysis of the fields can also take several forms. A broadband view of a single field component (Ex, Ey, Ez, Hx, Hy, or Hz) at multiple locations in a plane over the DUT is difficult to interpret due to its high dimensionality (R4). Therefore it is desirable to reduce the data by focusing on only specific components of the data. Such simplifications include:

1. Focusing on a single frequency (such as a system clock) across multiple locations to map over several frames.
2. Focusing on a single frequency at a single location on the DUT to determine if a specific subsystem is running.
3. Plotting the spectrogram of a broadband measurement made over a specific location (such as a large IC) that may indicate changes in functional blocks, PLL frequency drifts, etc.

The strength of this technique is in the flexibility that it offers. By allowing the engineer to view the problem from a variety of angles, it has the potential to offer the most insight into system changes, all while remaining minimally invasive.

To demonstrate the method, a setup such as Figure 2.5 is used to scan a “hot spot” over the IC which is in close proximity to the primary crystal oscillator. This location was chosen to pay maximum attention to the primary IC clock frequency and PLL-derived multiples thereof.

TLP Settings:

Charge Voltage: up to 1400 V

Pulse Rise time: 1 ns

Pulse Width: 27 ns

Scope Setting:

Sampling rate: 20Gs/s

BW: 4GHz(max)

Trigger source: H-probe output

Scale: 50mV/div

The following STFFT settings are used to generate the FFT figure:

Sa = 20 Gs/s; (sample_rate)

NS = 2^15pts; (window_size)

noverlap_pts = window_size*(0.9);

These values are the tuned to meet both frequency and time domain resolution.

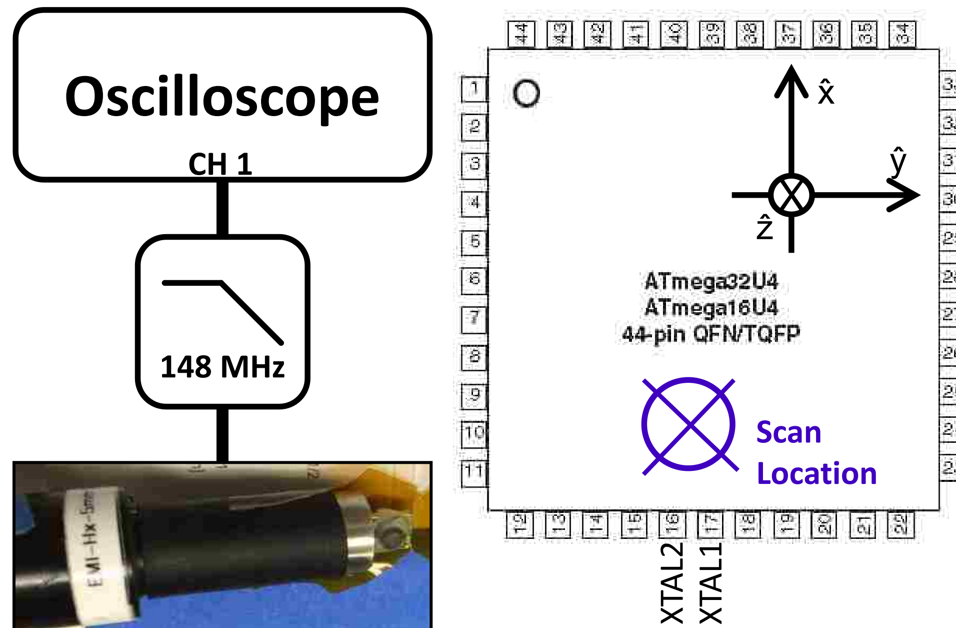

Figure 2.5. Time-domain near-field scanning and IC orientation.

Long time-domain records (~500 μs) are used to capture the IC behavior for a short time before the injection event as well as several hundred microseconds afterwards to observe the response of the IC in the aftermath of the injection. The system is calibrated by calculating the spectrogram during normal operational states without interference.

Short programs are written to place the processor in one of several basic states such as polling a GPIO pin, reading a value from an analog pin, or reading and writing to internal EEPROM. Because these programs are short and the system conditions are known a priori, each operation (e.g. analog voltage read) can be compared to the

expected value inside the program. Furthermore, because this comparison is done in software, the IC can be set to write detected errors to the EEPROM to record bad results. Such a write operation is even visible in the results of the test which will be shown later.

Figure 2.6 shows the spectrogram of the Hx field above the IC while a GPIO pin is repeatedly polled. Primary and harmonic clock frequencies are clearly visible as well as a number of other strong intermittent signals.

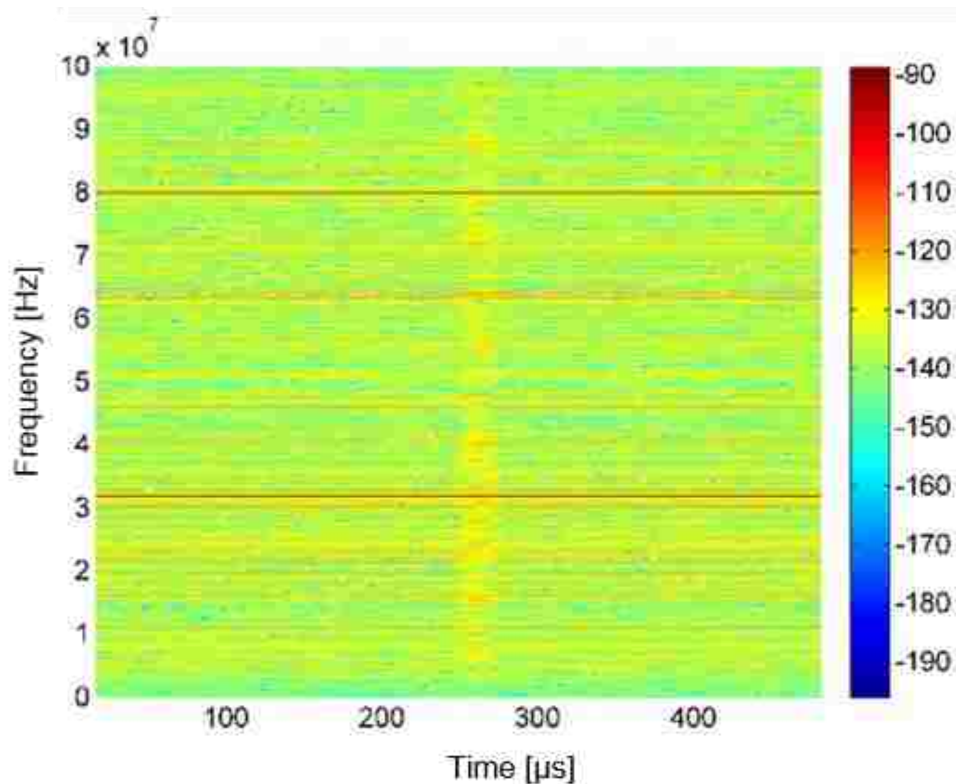

Figure 2.6. Observed Hx field spectrum during a continuous GPIO polling operation.

GPIO polling operation which is interrupted by an interference pulse delivered directly to the system via TLP. This disturbance is shown clearly in the spectrogram as a broadband signal at 250 µs shown in Figure 2.7. After the injection, several observations are made:

1. The primary clock signal at 16 MHz is undisturbed
2. The “background” fields are reduced

3. Several new strong signals appear 150 μs after the injection. These correspond to an EEPROM write operation which is triggered when the short monitoring program detects a soft failure.

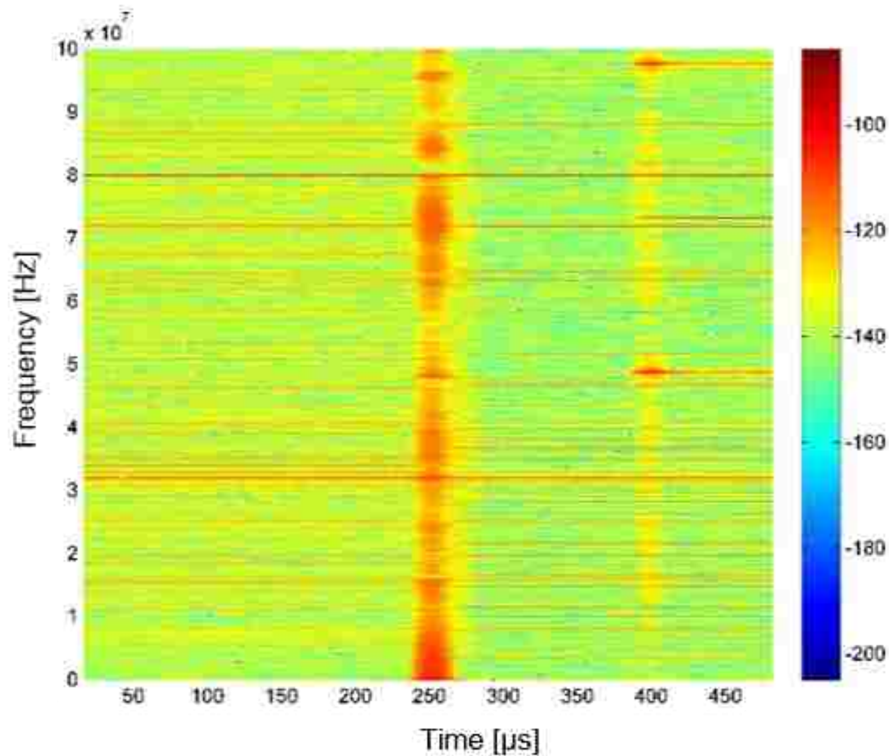

Figure 2.7. Observed Hx field spectrum above the DUT during a GPIO read error.

Figure 2.8 shows the spectrogram of the Hx field above the IC during a simple A/D converter read operation. The results clearly show periodic broadband changes in the magnetic field every 110 μs which is within the range of sample times of the onboard A/D converter (60 – 260 μs).

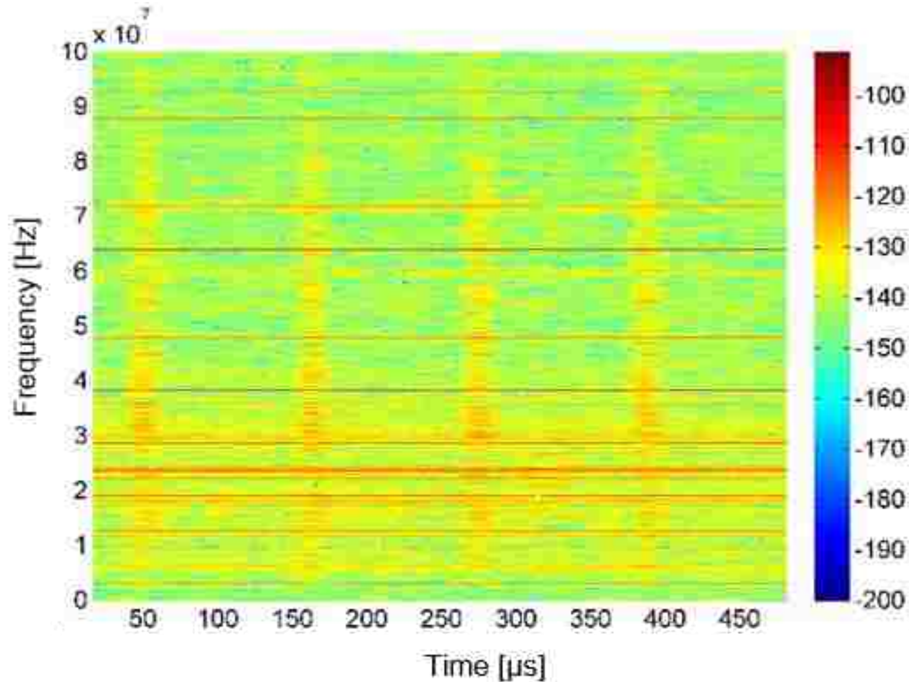

Figure 2.8. Observed Hx field spectrum above the DUT during an ADC read.

Figure 2.9 shows the results of the field-scanning test above the IC when an ADC read operation is disturbed by TLP injection. Again, this disturbance appears at 250 µs and is visible as broadband noise. Several observations are made:

The primary clock signal at 16 MHz is undisturbed

The “background” fields remain similar, but dozens of extra frequency components appear immediately following the TLP injection.

Several new strong signals appear 150 µs after the injection. These correspond to an EEPROM write which is triggered when the short monitoring program detects a soft failure.

2.5. CONCLUSION FOR SOFT FAILURE DETECTION

In this chapter we present three different hardware measurement methods for detecting soft failures without the aid of a mature software stack. The methods were demonstrated on two DUTs of different levels of complexity, showing changes in operation due to injection without invasively monitoring the system state.

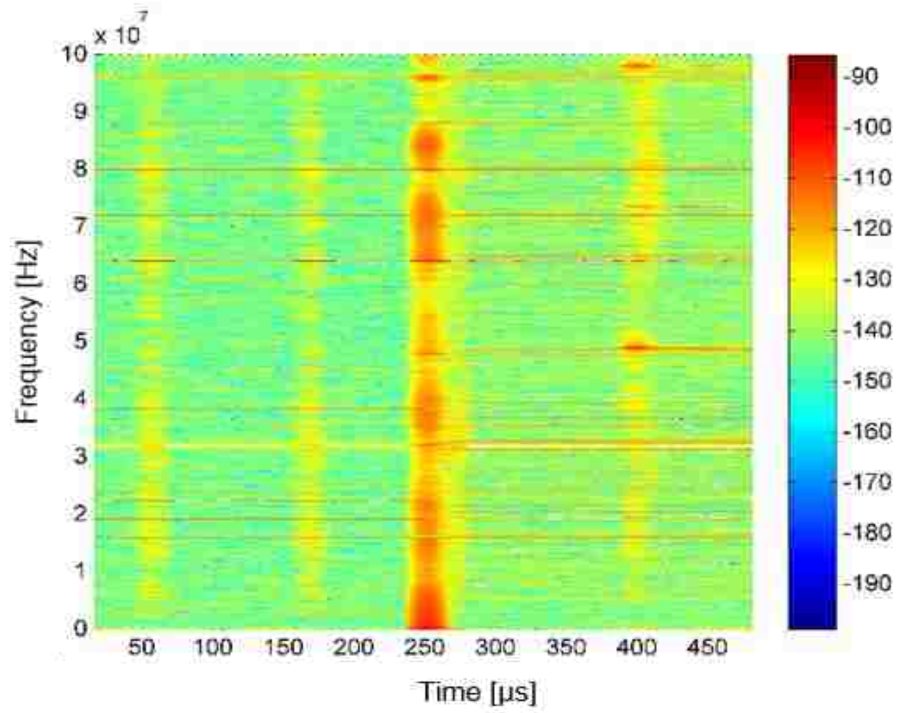

Figure 2.9. Observed Hx field spectrum above the DUT during an ADC read error.

3. IC MODELING TECHNIQUES FOR DISTANT ERROR PREDICTION

3.1. INTRODUCTION

The objective for the IC modeling is to understand the current flow through the IC during ESD injection, which can help to improve further ESD protection design in the system. In order to model the desired current flow, an equivalent behavioral model of the IC's I/O pin and IC's PDN is assembled from many individual large and small signal measurements of the IC pin behaviors. Once assembled, the PDN model is simulated under stress to better understand the current propagation inside the IC and complete system.

Performing DC measurement is to quickly get an overview of the connection inside the IC pins. This part is to measure the resistance between different VCC pins using Ohmmeter, during this measurement, other pins are left open. If an open circuit is detected between two pins, measure in diode mode between the two pins.

Performing RF measurements is to determine the parasitic capacitance and inductance value. Because the on-die capacitance and the inductance of the IC would affect the transient voltage and current waveforms, and matching the transient I/V waveforms are necessary for IC pin modeling.

Since the RF parameters can not predict the ESD injection case, as the diodes are not turned on during RF measurement, but during ESD injection, diodes may be turned on. So TLP measurement is needed in order to build the large signal model.

3.2. IC MODELING TECHNIQUES

As the characteristics of the IC change with bias—particularly the values of capacitances associated with nonlinear devices—measurements were made when the IC was powered with 5 V and when it was unpowered. The IC was placed over the solid copper plane of a PCB and full two-port S-parameter measurements were performed for each pair of pins.

The measurement of impedance parameters for the Power/Ground pin pair is shown in Figure 3.1. The center conductor of two semi-rigid coaxial cables was soldered to the power and ground pins of the IC and the cable shields were soldered to the PCB return plane. The VNA was calibrated to the end of the coaxial cables, where they

connected to the IC. Each pin requires either a supply voltage of 5 or 0 V to maintain proper operation during the measurement. RF current paths through other pins (e.g., from the VNA and back through the power supply connections) are blocked by the bias T inside the VNA while maintaining a supply voltage of 5 V on power pins and 0 V on ground.

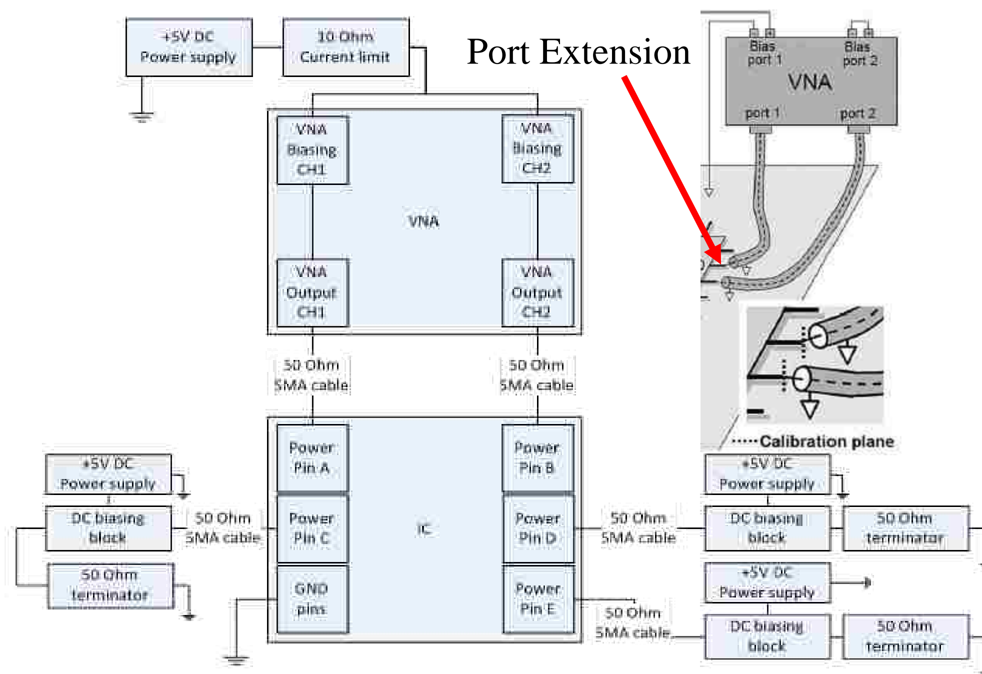

Figure 3.1. VNA measurement setup for IC PDN.

Then the S11 is measured and converted to Z11, which indicates the connection between power pin to ground. Use the following Z11 measurement result we make the RF model of IC's one power pin in Figure 3.2, for example.

1, Low frequency: L1, L2 is short, C1 is open, R1 dominates, because of the resistance from pin to ground, the slop at low frequency is not 20dB/div.

2, Frequency increase: Zc1 decrease, L1, L2 impedance increase but not enough, C1 dominates.

3, Resonance point: determined mainly by R2

4, Frequency increase: Zc1 decrease, L1, L2 impedance increase and dominates, the inductances are caused by bond wires inside the IC.

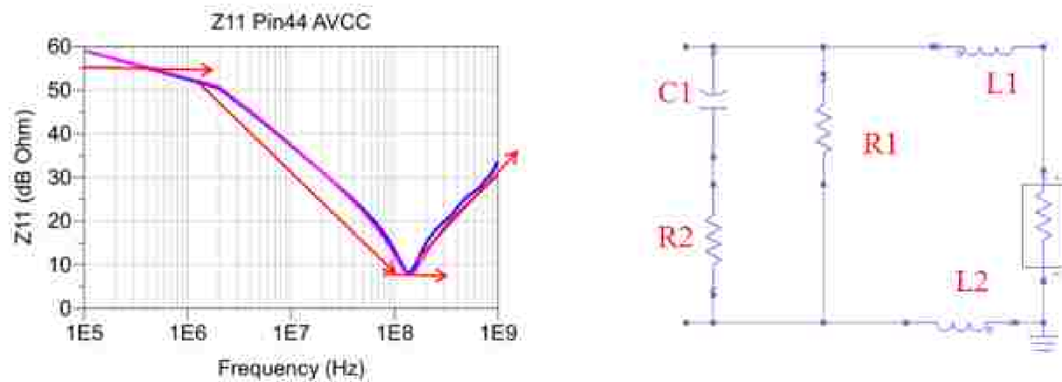

Figure 3.2. Z11 measurement and simulation of IC power pin 44.

TLP measurement setup is different from RF measurement setup, in our test setup, reflective TLP measurement method is used which is shown in Figure 3.3. For very fast TLP measurements (VF-TLP) with pulse widths < transmission line delay, incident and reflected signals are recorded separately with a wide-band pickoff tee in the pulse-force line. The transient device response is calculated by combining the incident and reflected pulse signals numerically.

Actually direct current measurement is also a choice, however, current measurement will be limited by the bandwidth of current probe, also there will be some discontinuity of the current path at the current probe caused by the inductance created due to the insertion of the current probe. Using reflective measurement system is better for current calculation.

The IV curve is measured and shown as waterfall plot R(t, VForward) and then compared with DUT's real value. Here 50 Ohm resistor is used for test since 50 Ohm DUT is a standard reference.

DUT is soldered close to the voltage measurement probe to make voltage measurement as close as possible. Waterfall plot shows how the measured RDUT change with time and TLP charging voltage level, then it can be used to check if the R(t, VTLP)

is close to RDUT's actual value. Then we know which part of TLP time domain waveform can be used to characterize the IC.

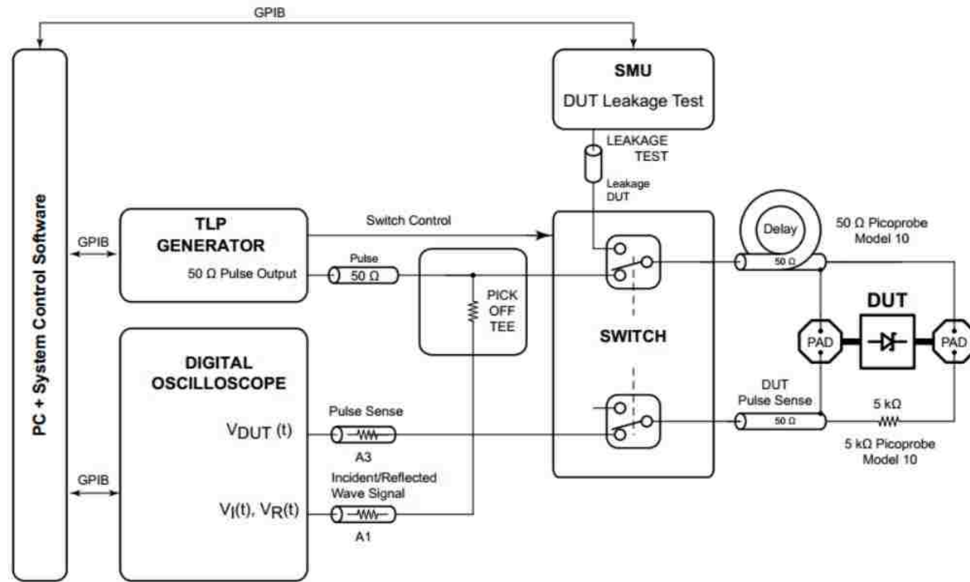

Figure 3.3. Reflective measurement system.

The flow chart of generating the waterfall plot is in Figure 3.4.

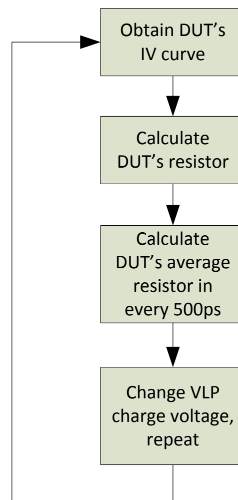

Figure 3.4. Waterfall plot generation flow chart.

Using the 50 Ohm resister as DUT, we generated the following waterfall plot in Figure 3.5.

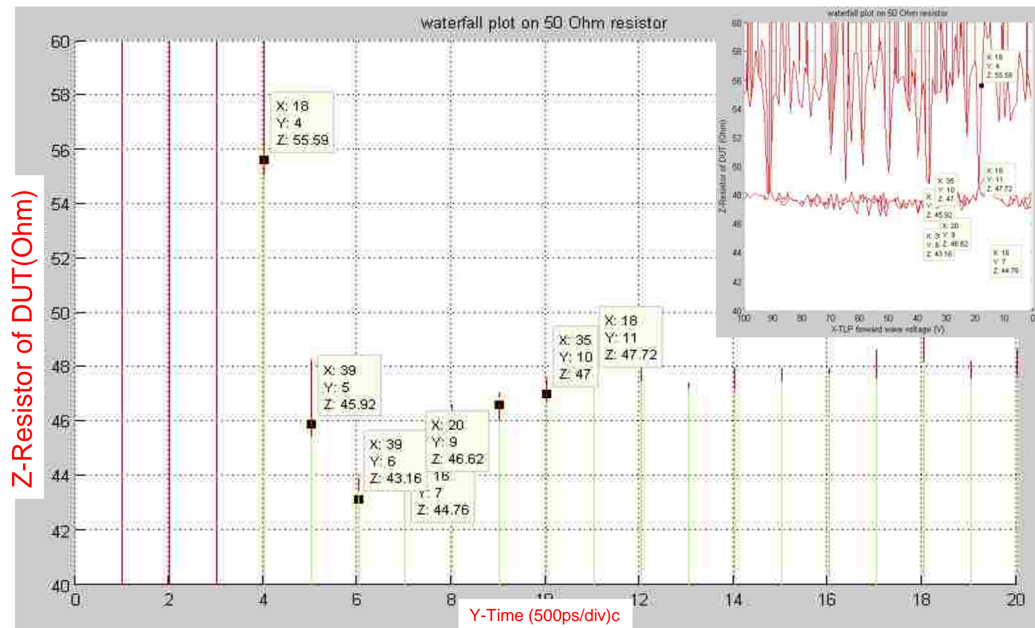

Figure 3.5. Use 50 Ohm as DUT, 3D view of the waterfall plot.

The resistance value of about 50 ohm is measured. At the beginning of the time domain waveform, overshoot is observed, this kind of overshoot are due to the inductance of the measurement system, and that's why the first 3ns waveform can not be used to characterize the DUT. And after 3ns, the data can be used for IC modeling, as the error rate between measured resistor and actual value is less than 12%.

If the DUT is a diode, then the modeling is much more complicated, since the dynamic resistance will change with applied voltage on DUT, so voltage controlled switch will be used to match the IV curve. Also, if there are some snapback behaviors on the DUT, then negative resistors will be used in the diode modeling, these techniques will be shown in the study case.

3.3. SOFT FAILURE DETECTION USING TLP

The DUT for IC modeling case study is Arduino Leonardo board which is shown in Figure 3.6, the Arduino Leonardo is a microcontroller board based on the

ATmega32U4. It has 20 digital input/output pins (of which 7 can be used as PWM outputs and 12 as analog inputs), a 16 MHz crystal oscillator, a micro USB connection, a power jack, an ICSP header, 2 LEDs, a reset button and build-in EEPROM.

This DUT has been selected based on following reasons: first of all, the MCU on this board is ATmega32U4, it has 5 power pins and 2 different power domains, so it is good for PDN investigation; secondly, There are not too much components on this board, so it is easier to focus on the investigation of MCU; also there are lot of space on the board for modification; furthermore, the availability of a development platform allows us to test generated models in a real system.

Figure 3.6. Arduino Leonardo board.

The goal of performing this kind of injection is to find out soft errors, associate these soft errors to different types and this can further help to find out root causes. While E-field and H-field injections help in identifying the ESD sensitive regions in a DUT, it is difficult to estimate the exact voltage or current injected by E & H-field probes because the coupling depends strongly on the local geometry. Therefore, TLP (transmission line pulse generator) is used to perform local injection on IC pins.

The soft error types and thresholds are not only related to injection settings, but also related to the software that running on the DUT. So a special code is written to cautiously check if soft errors occurred on the DUT.

The software automatic detects these following soft errors: AD converter reading error, math calculation error, internal EEPROM read/write error, I/O pin reading error and watch dog timer reset error. These error codes are defined as follows:

```
/* AD converter reading error */
#define ERR_ADC_READ       1
/* Math calculation error */
#define ERR_CALC           2
/* Internal EEPROM R/W error */
#define ERR_RW_EEPROM      3
/* Input pin in the same power domain reading error */
#define ERR_RD_IO_SAME_DM  4
/* Input pin not in the same power domain reading error */
#define ERR_RD_IO_DIFF_DM  5
/* Watch dog timer reset error */
#define ERR_WDT_RST        6
```

Since the Leonardo board is too simple, the best choice for soft error checking is to use LED. Normally, LED is off, when an error occurs: 1, Error code will be saved in EEPROM; 2, LED will blink, number of blinks is the same as error code number (From 1-6); 3, System will not reset if error is not watch dog timer error. The software main flow chart is as Figure 3.7:

At the same time, watch dog timer is also enabled, and if program goes to unknown location, the watch dog timer interrupt handling program will be executed, after entering watchdog interrupt sub-routine, system will resets automatically and the error code will be recorded in EEPROM. The hardware setup block diagram is as Figure 3.8. Figure 3.9 shows the actual hardware setup.

For I/O read error, since the threshold for read error might be different on different IO pins, so different configurations are tested, here the pin under injection is I/O pin PD6, and it belongs to AVCC power domain.

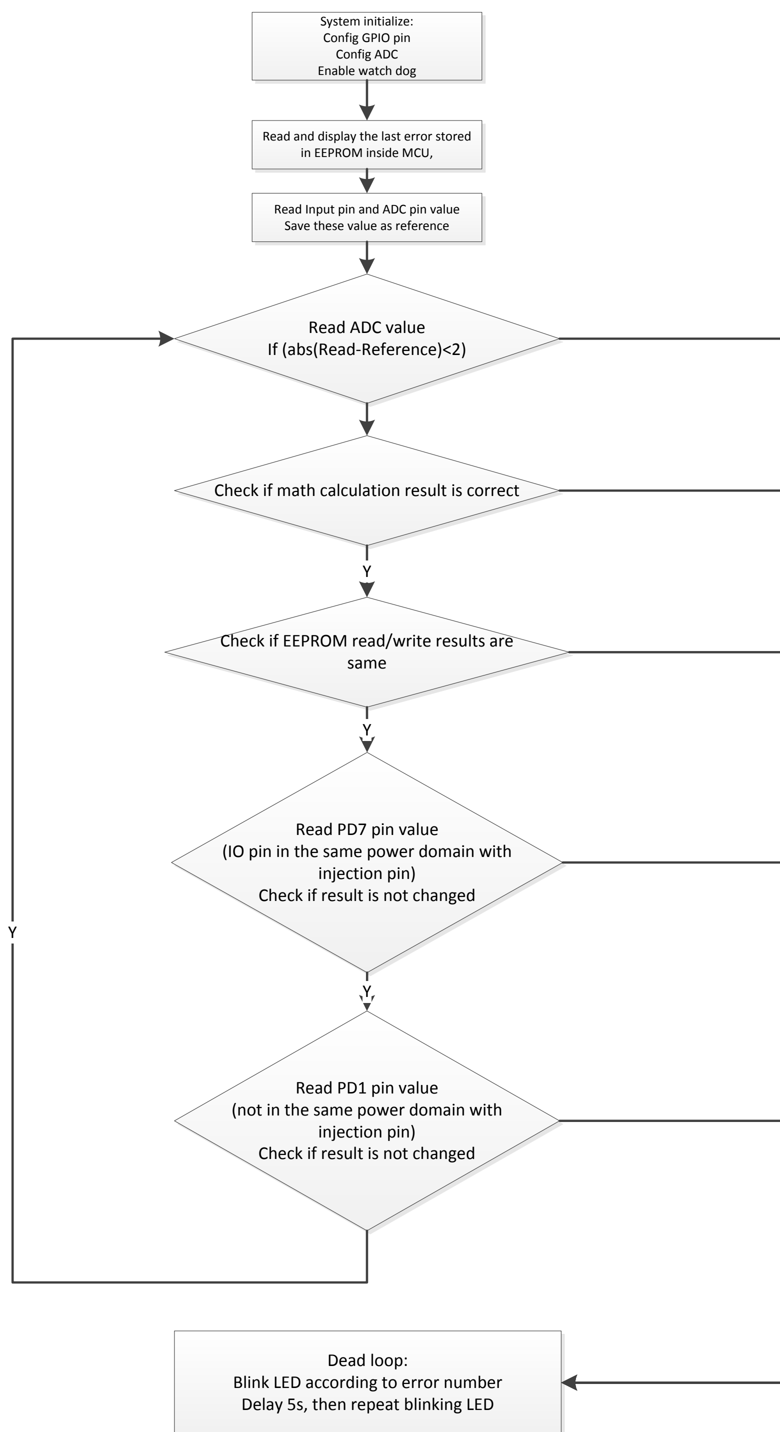

Figure 3.7. Software error detection flow chart.

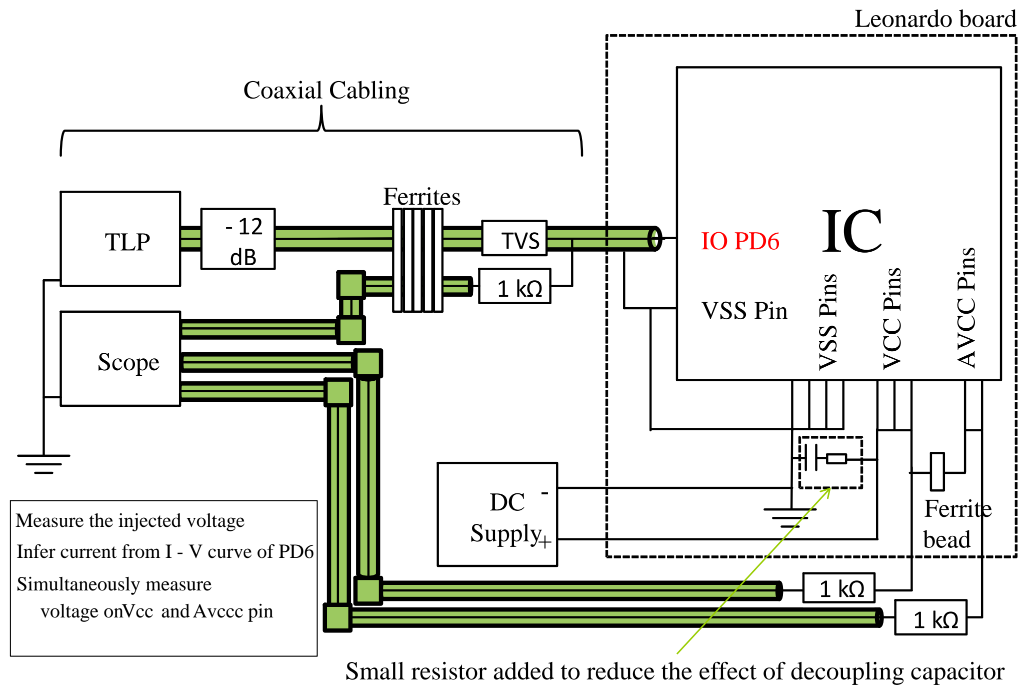

Figure 3.8. I/O injection setup block diagram.

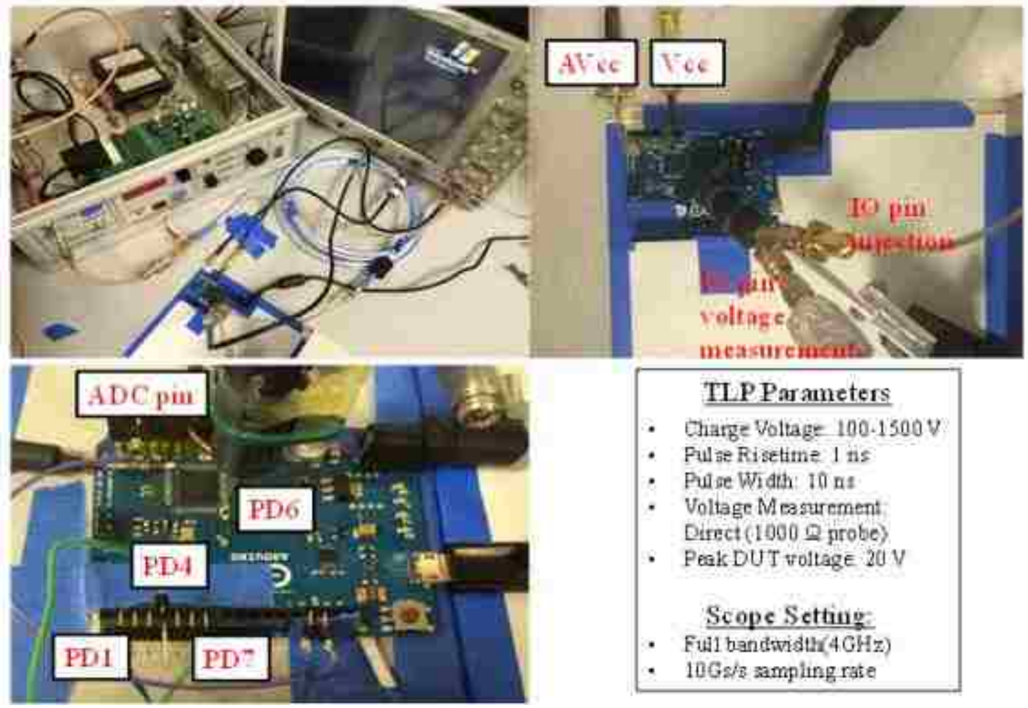

Figure 3.9. Hardware setup for soft error detection.

1, Test I/O pin read error. Choose I/O pin PD7 which is in the same power domain with the I/O pin under injection (PD6). In this case PD7 is set as Input. The test result is shown in Table 3.1.

2, Test I/O pin read error. Choose I/O pin PD1 which is in the different power domain with the I/O pin under injection (PD6). In this case PD1 is set as Input. The test result is shown in Table 3.2.

3, Test EEPROM R/W error, we have the following summary for soft error threshold. Here the EEPROM read and EEPROM write case are studied together. The test result is shown in Table 3.3.

Table 3.1. Test result for I/O pin read error – 1.

PD 7 Connection	Ground	+5V	PD4 (Output : low, to PD7)	PD4 (Output : High, to PD7)
Soft error threshold	No soft error, IC latch up @TLP charging voltage = 1500V	Soft error @TLP charging voltage = 1300V, voltage on DUT approximately 18V. No latch-up is observed	No soft error, IC latch up @TLP charging voltage = 1500V,	Soft error @TLP charging voltage = 1450V, voltage on DUT=20V. Also latch-up is observed

When the TLP pulse width is 10ns and pulse rise time is 1ns, applying 15V voltage on IC's I/O pin PD6 will cause the EEPROM soft error happen. To summarize the test result, it can seen that the EEPROM R/W error and IC reset error are the soft errors most frequently occurred. Other soft error types such as I/O pin read error, and calculation errors are not occurred easily.

Table 3.2. Test result for I/O pin read error – 2.

PD 1 Connection	Ground	+5V	PD4 (Output : low, shorted to PD1)	PD4 (Output : High, shorted to PD1)
Soft error threshold	No soft error, IC latch up @TLP charging voltage=1500V	No soft error, IC latch up @TLP charging voltage=1500V	No soft error, IC latch up @TLP charging voltage = 1500V	No soft error, IC latch up @TLP charging voltage=1500V

Table 3.3. Test result for EEPROM read/write error.

Soft error type	IO pin PD1 configuration	Injection type	Soft error threshold
EEPROM R/W error	Input	Positive	TLP charge voltage = 890 V No latch up occur
		Negative	No soft error observed after TLP charge voltage reaches -1 kV
	Output high	Positive	Very infrequently we observed a system halt (twice in 100s of tests). The IC does not respond and the watch dog timer crash
		Negative	No soft error observed after TLP charge voltage reaches -1 kV
	Output low	Positive	No soft error observed after TLP charge voltage reaches 1 kV
		Negative	No soft error observed after TLP charge voltage reaches -1 kV

3.4. IC MODELING PROCEDURE

The objective is to understand the current flow through the IC during ESD injection, which can help to improve further ESD protection design in the system. In order to model the desired current flow, an equivalent behavioral model of the IC's I/O pin and IC's PDN is assembled from many individual large and small signal measurements of the IC pin behaviors. Once assembled, the PDN model is simulated under stress to better understand the current propagation inside the IC and complete system.

The first step is DC measurement. The goal of performing DC measurement is to quickly get an overview of the connection inside the IC pins which is shown in Figure 3.10. This part is to measure the resistance between different VCC pins using Ohmmeter, during this measurement, other pins are left open. If an open circuit is detected between two pins, measure in diode mode between the two pins.

The DC measurement result is shown in Table 3.4. This result indicates that different power pins are well isolated between each other, and other measurement methods are needed for the PDN modeling.

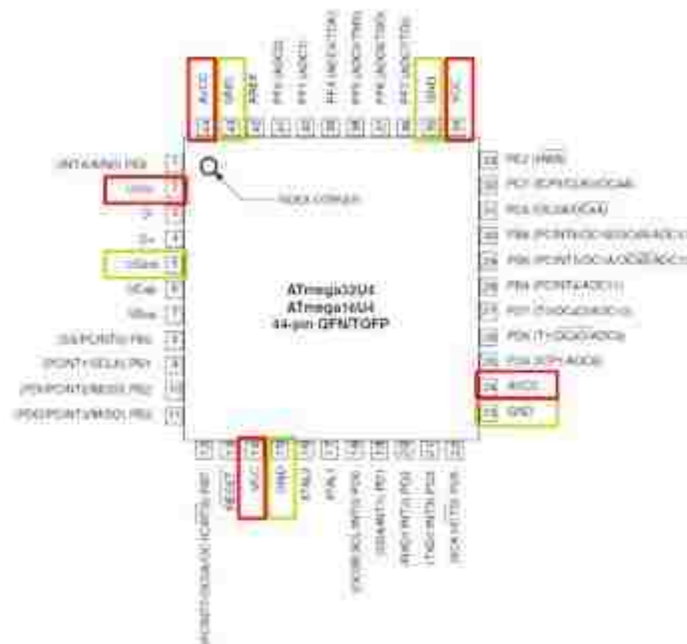

Figure 3.10. IC pin definitions.

Table 3.4. IC pin DC measurement results.

Pos \ Neg	UVcc (2)	VCC (14)	AVcc (24)	Vcc (34)	AVcc2 (44)
UVcc (2)	-----	OPEN	OPEN	OPEN	OPEN
VCC (14)	OPEN	-----	OPEN	OPEN	OPEN
AVcc (24)	OPEN	OPEN	-----	0.72 V	OPEN
Vcc (34)	OPEN	OPEN	0.72 V	-----	0.72 V
AVcc2 (44)	OPEN	OPEN	OPEN	0.72 V	-----

The purpose of performing RF measurements is to determine the parasitic capacitance and inductance value. Because the on-die capacitance and the inductance of the IC would affect the transient voltage and current waveforms, and matching the transient I/V waveforms are necessary for IC pin modeling.

The small signal parameters of the coupling between the 5 different power domains were measured. Biased S-parameters are used to measure the small signal behavior between domains.

Setup for RF measurement:

All ports terminated with 50 Ω

All power pins are 5V biased.

A current limit is set to protect the IC

5V will be verified at each IC PIN

Port extension is performed and the calibration plane is on the IC power pins

VNA settings:

100 KHz – 1 GHz

1601 measurement points

Output power [-5dBm, 0dBm, 10dBm]

DC Biased with 5V for all power pins

The real measurement setup is shown in Figure 3.11:

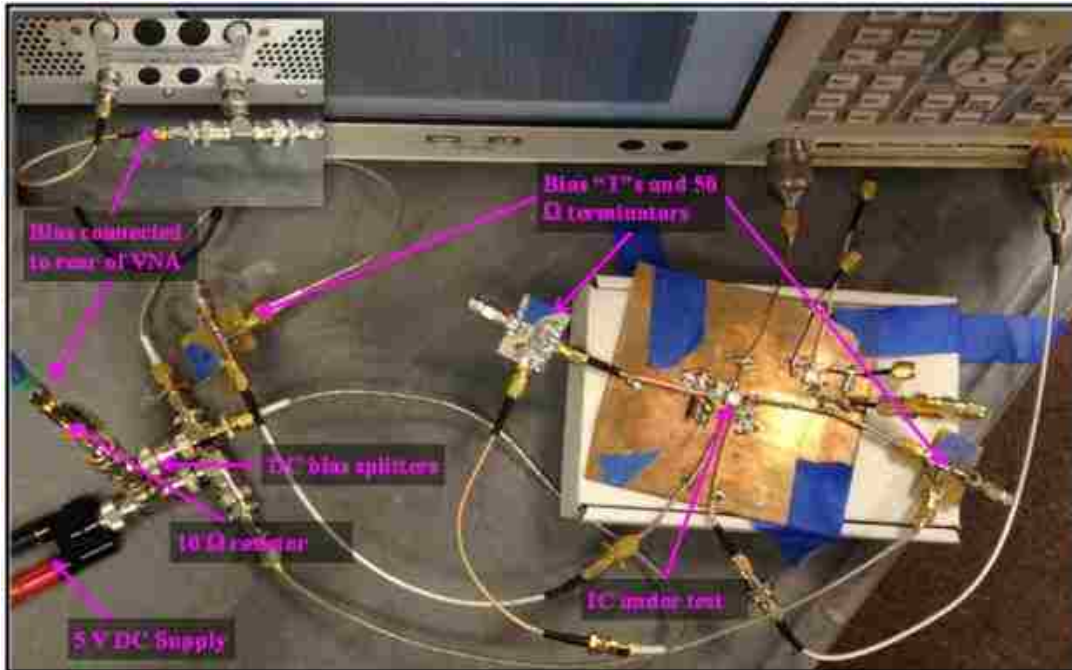

Figure 3.11. VNA measurement setup for IC PDN.

To determine the coupling between domains, the output power of the VNA was varied to ensure that unwanted turn-on of inter-domain diodes was not occurring. The S21 measurement of IC power pins is shown in Figure 3.12:

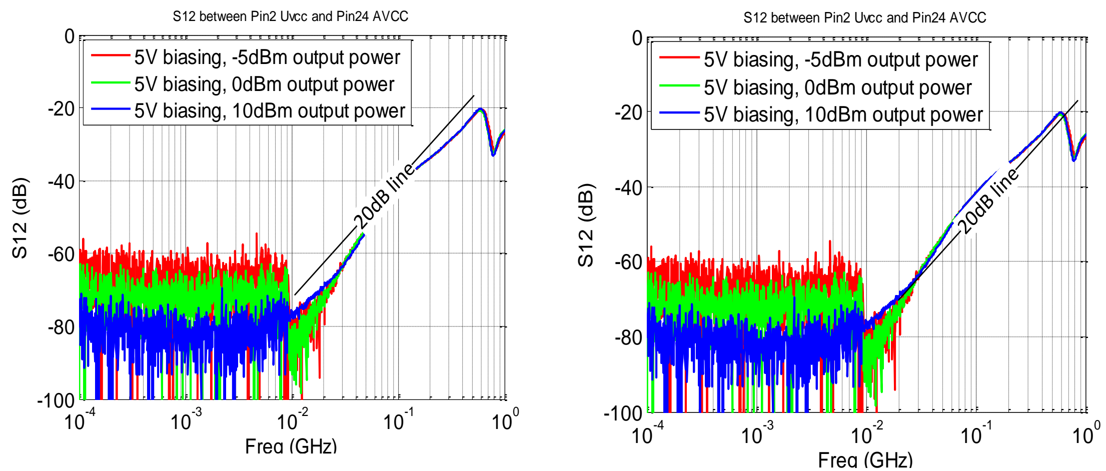

Figure 3.12. S21 measurement of IC power pins.

According to the measurement results, the behavior of the S21 does not depend on the excitation power within in this range (-5 to 10 dBm). This indicates that no nonlinear junction is excited strong enough to influence the S-parameters significantly.

In addition, The coupling between domains increases with frequency. It is capacitive. This is not a surprise, as the domains are isolated from each other, as long as the voltage difference between the domains is not too large to start causing significant conduction current in the connecting nonlinear junctions. The estimated capacitance value is several pF.

Below 10 MHz the data is dominated by the noise floor of the system. The noise floor could have been reduced, e.g., by adding an amplifier in the receive path, however, no new information would have been gained based on experience with similar measurements. The inter-domain coupling is capacitive, thus, for low frequencies the S-parameters approach very large negative values.

Some resonances are visible above 700 MHz. These are caused by the interaction of the capacitance inside the IC, the effective inductances of the connections inside the IC and by the measurement. As the dominating frequency range is below 700 MHz no special attention was given to these effects.

Then the S11 is measured and converted to Z11, which indicates the connection between power pin to ground. IC power pin 2 is used as an example which is shown in Figure 3.13, form the Z11 plot, we have the following conclusions:

1, Z11 doesn’t change with the biasing level for Pin2, Uvcc pin;

2, at low frequency, it is high impedance;

3, as frequency increase, impedance reduces, behave like a capacitor;

4, at 500-600MHz a resonance point occurred, it do not depend on the output power level;

5, though there is some resonance, still capacitive behavior dominates in frequency range up to 1GHz.

Use the following method the RF model of IC power pins 44 can be made, the method is shown in Figure 3.14, for an example.

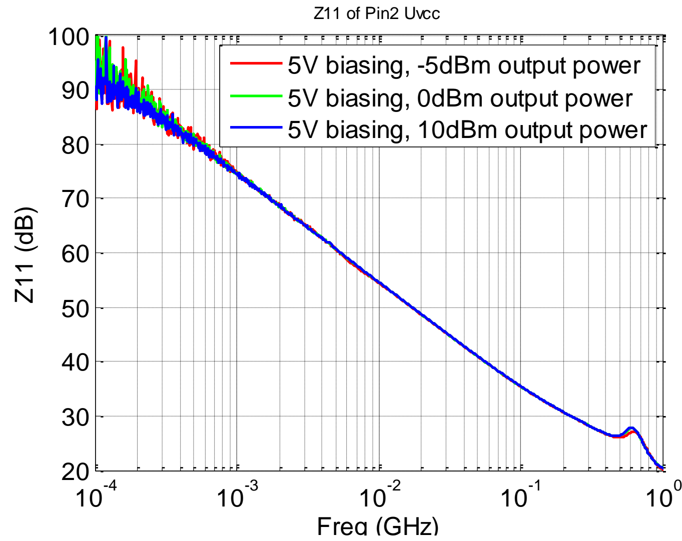

Figure 3.13. Z11 measurement of IC power pin 2.

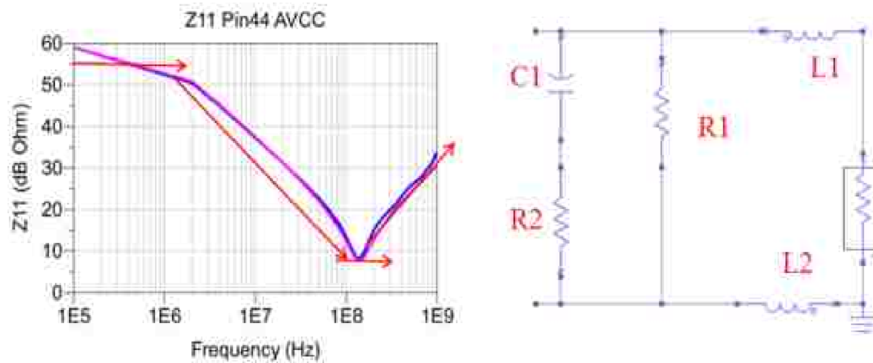

Figure 3.14. Z11 measurement and simulation of IC power pin 44.

1, Low frequency: L1, L2 is short, C1 is open, R1 dominates, because of the resistance from pin to ground, the slop at low frequency is not 20dB/div

2, Frequency increase: Zc1 decrease, L1, L2 impedance increase but not enough, C1 dominates

3, Resonance point: determined mainly by R2

4, Frequency increase: Zc1 decrease, L1, L2 impedance increase and dominates, the inductances are caused by bond wires inside the IC.

Using this method, the RF model of different power pins can be created which is shown in Figure 3.15 and Figure 3.16:

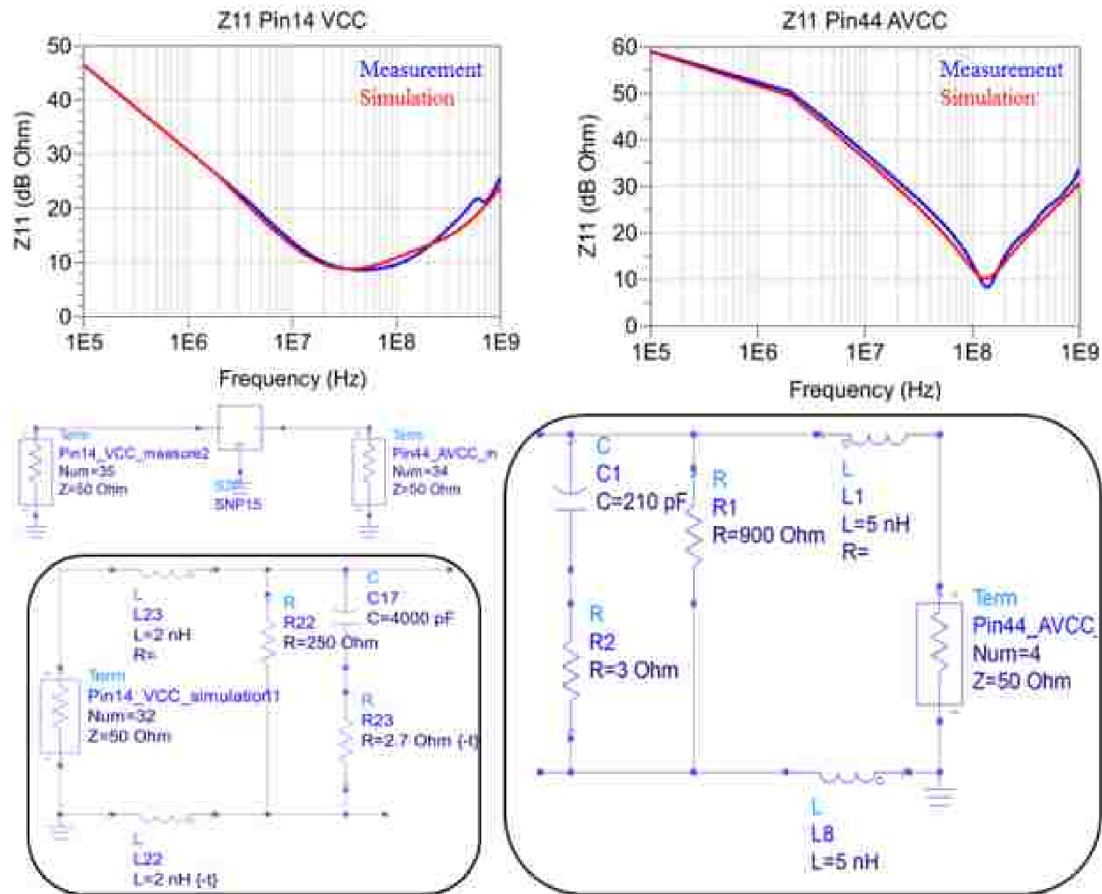

Figure 3.15. Z11 measurement and simulation of IC power pin 14&44.

According to the RF measurement, the following conclusions can be made:

1, The Z11 measurement showed all the 5 power pins have similar characteristics; this is also an indication that the measurement result is correct.

2, The Z11 model can match the measurement result well, this is a strong indication that the modeling is correct.

3, The S21 parameters for all 5 power pins shows good isolation between power domains at low frequency for small signal excitation.

4, S21 parameters can not predict the ESD injection case, as the diodes are not turned on during S21 measurement. This is the main reason why the TLP measurement is needed.

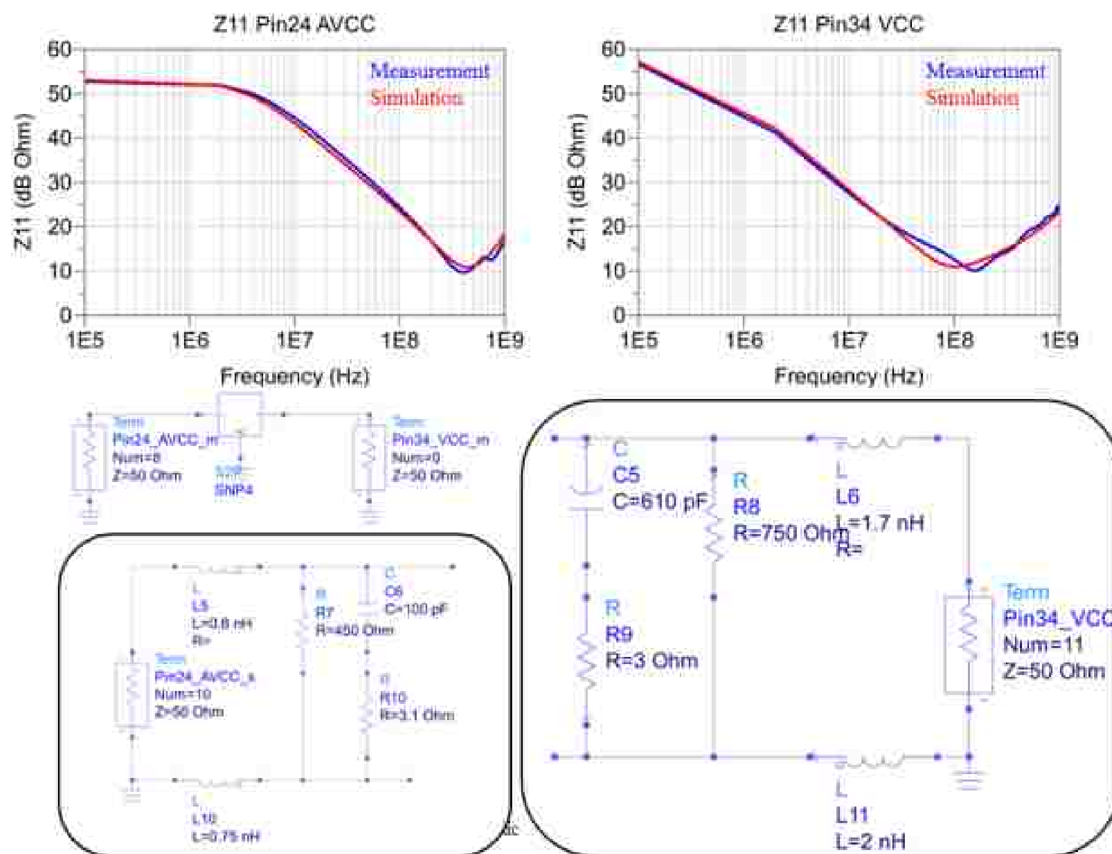

Figure 3.16. Z11 measurement and simulation of IC power pin 24&34.

Then the TLP measurements are performed. The block diagram of our actual setup is in Figure 3.17.

Since this is a quite complex setup, so before performing the actual measurement starts, it would be necessary to verify the system first, this can be done by measuring a known DUT. Here a reference test is done using a small resistor: The IV curve is measured and shown as waterfall plot R(t, VForward) and then compared with DUT's real value. Also 50 Ohm and 8.5 Ohm resistor are used for test, 50 Ohm DUT is a standard reference, 8.5Ohm value is small and we are interested in the low resistance case.

DUT is soldered close to the voltage measurement probe to make voltage measurement as close as possible. Waterfall plot shows how the measured RDUT change with time and TLP charging voltage level, then it can be used to check if the R(t, VTLP)

is close to RDUT's actual value. Then we know which part of TLP time domain waveform can be used to characterize the IC.

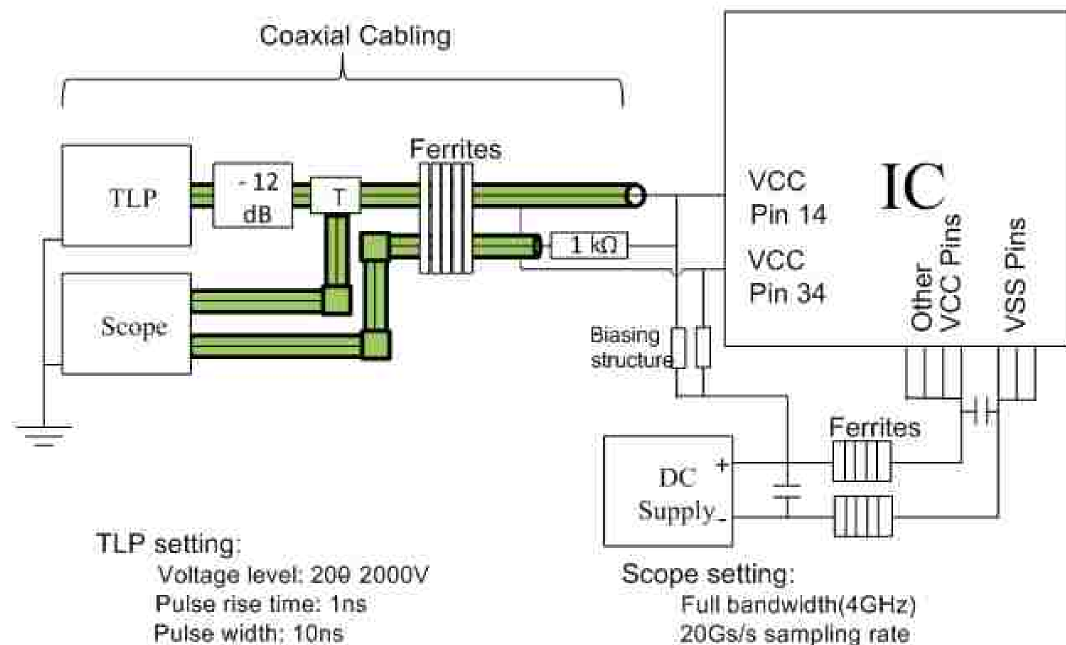

Figure 3.17. Reflective measurement system block diagram and settings.

Using the 50 Ohm resister as DUT, we generated the following waterfall. The resistance value of about 50 ohm is measured. At the beginning of the time domain waveform, overshoot is observed, this kind of overshoot are due to the inductance of the measurement system, and that's why the first 3ns waveform can not be used to characterize the DUT. And after 3ns, the data can be used for IC modeling, as the error rate between measured resistor and actual value is less than 12%. Then 8.5 Ohm resistor is used as our DUT and the measurement result is shown in Figure 3.18, form the plot we can see that the first 3ns waveform can not be used to characterize the DUT, and after 3ns, the data can be used for IC modeling as the error rate between measured resistor and actual value is less than 7%. Then the IV curve of different power pins and power pin to GND are measured.

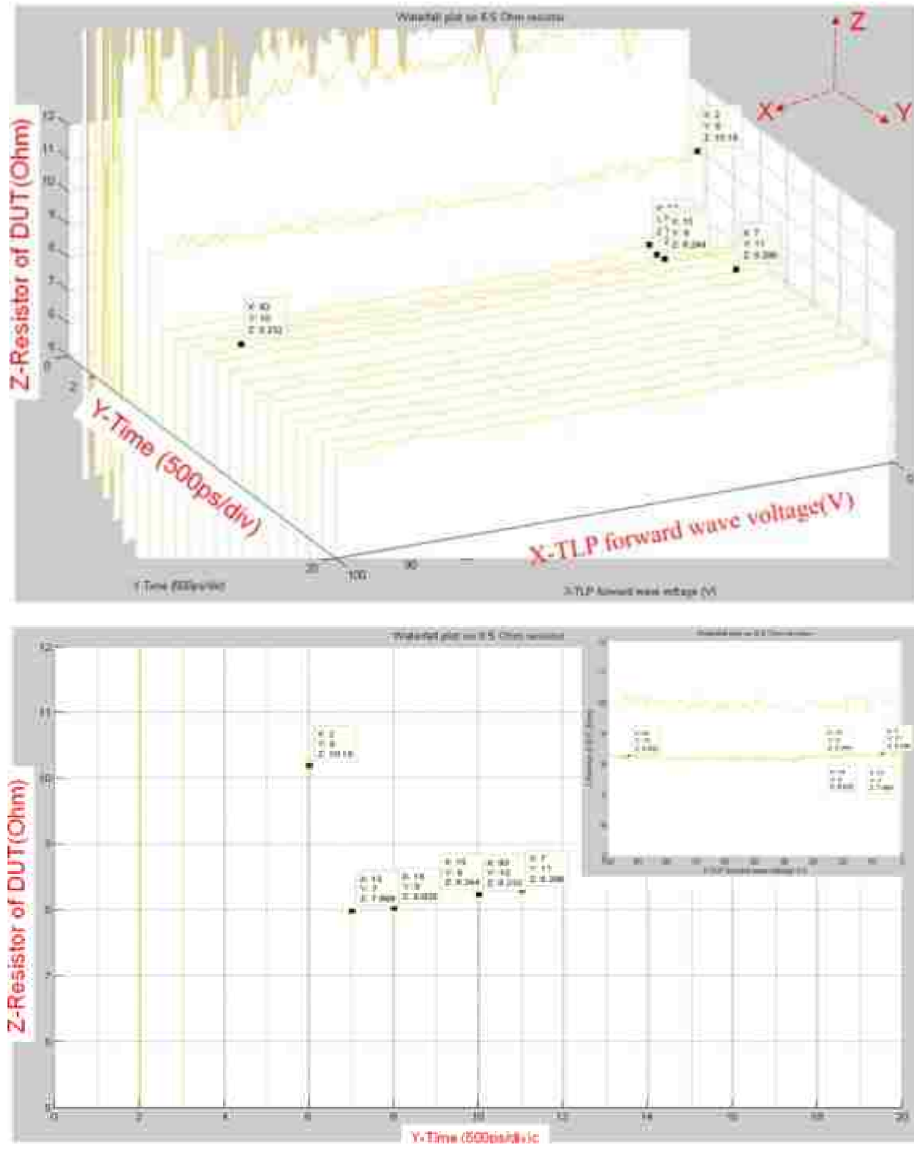

Figure 3.18. Using 8.5 Ohm as DUT, 3D view of the waterfall plot.

The IC pin measurement result is shown in Figure 3.19. After 4ns, the data can be used for IC modeling. When the TLP forward voltage is low, the resistance between pin 24 and 34 is large and can reach up to 16 Ohm, and if TLP forward voltage can go lower, resistor will still increase. When TLP forward voltage increases the resistance decreases to 4 Ohm.

By placing a series of voltage controlled switches in parallel, a circuit with a voltage dependent resistance can be used to match the measured characteristic. Here the connection between pin 24 and pin 34 is used as an example:

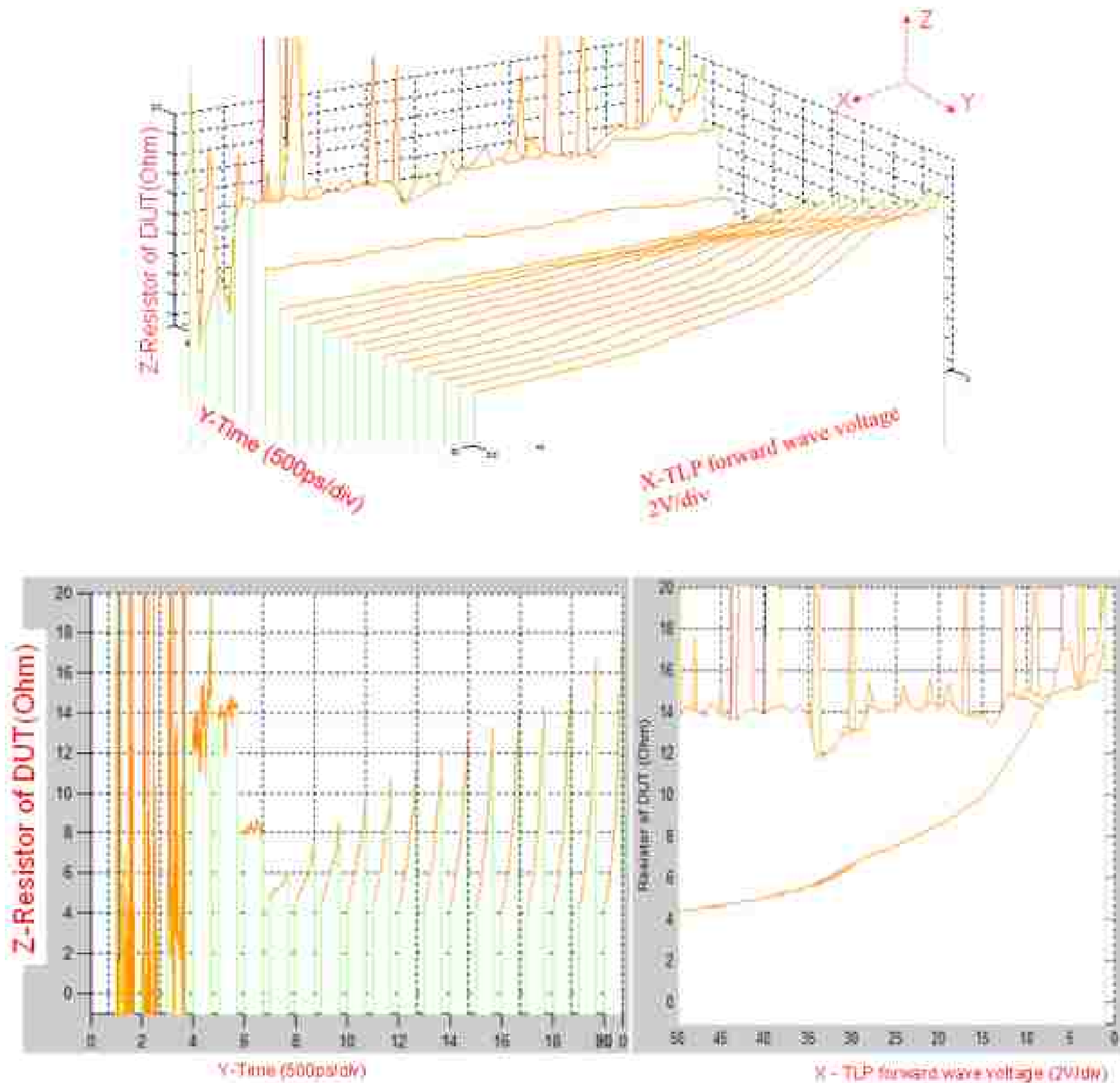

Figure 3.19. IC measurement result: Pin 24 AVCC to pin 34 VCC.

The idea is to use the voltage controlled switch to represent the dynamic resistor change. According to the IV curve, the dynamic resistor changes occur at 0.7V, 8.7V and 13V. Before voltage reaches 0.7V, current is almost 0, and when voltage is between 0.7V-8.8V, the dynamic resistor is about 10 Ohm, etc. The IV curve and IC pin model is shown in Figure 3.20 and Figure 3.21. Using this method the complete IC PDN model can be build and the IC PDN model is shown in Figure 3.22.

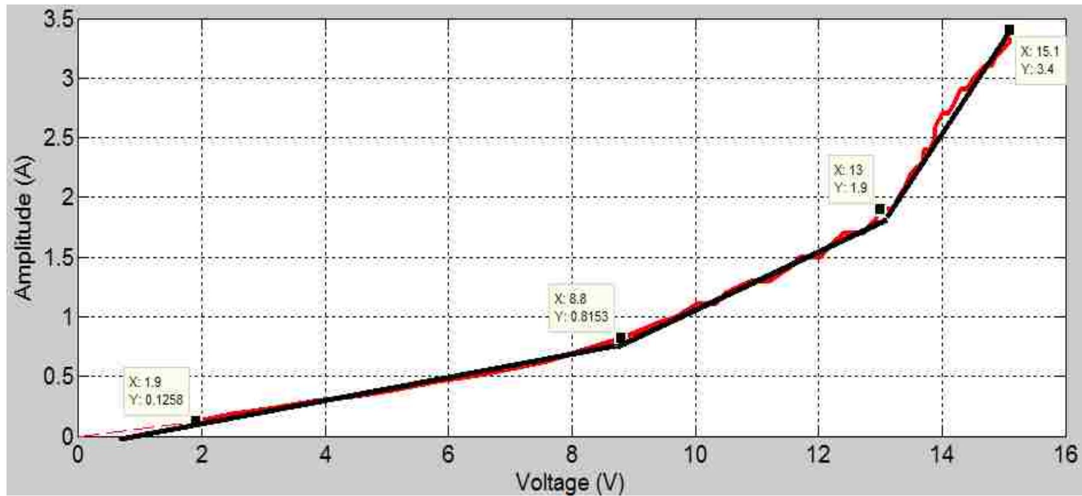

Figure 3.20. Pin 24 - Pin 34 IV curve measurement and simulation result.

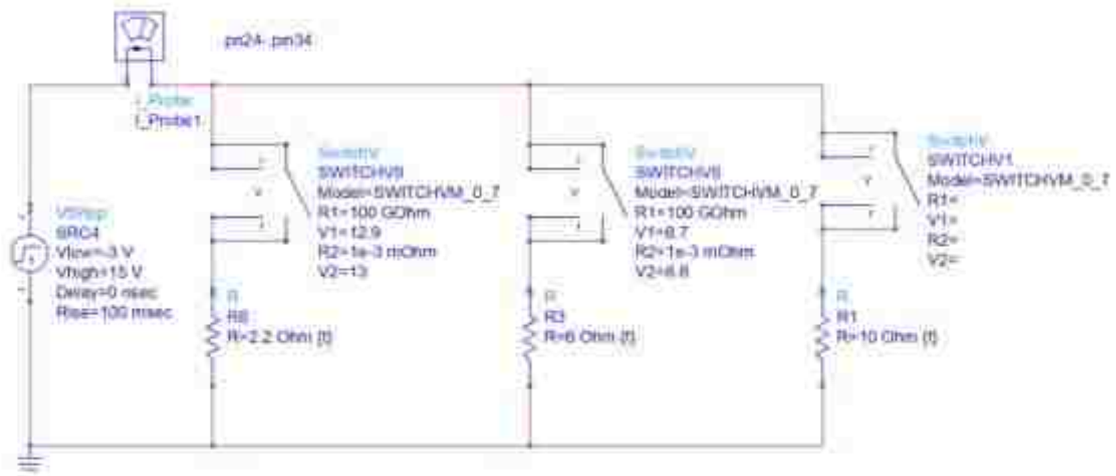

Figure 3.21. Pin 24 - Pin 34 models.

Both the PDN and I/O pin need to be measured using TLP. The I/O pin characterization uses similar principles as the Vcc pin characterization. The setup is shown in Figure 3.23.

In the model, SWITCHV1 turns on at about 0.7V, SWITCHV8 turns on at about 8.8V and SWITCH9 turns on at about 13V. The dynamic resistors are R1, R1//R2, R1//R2//R3 respectively.

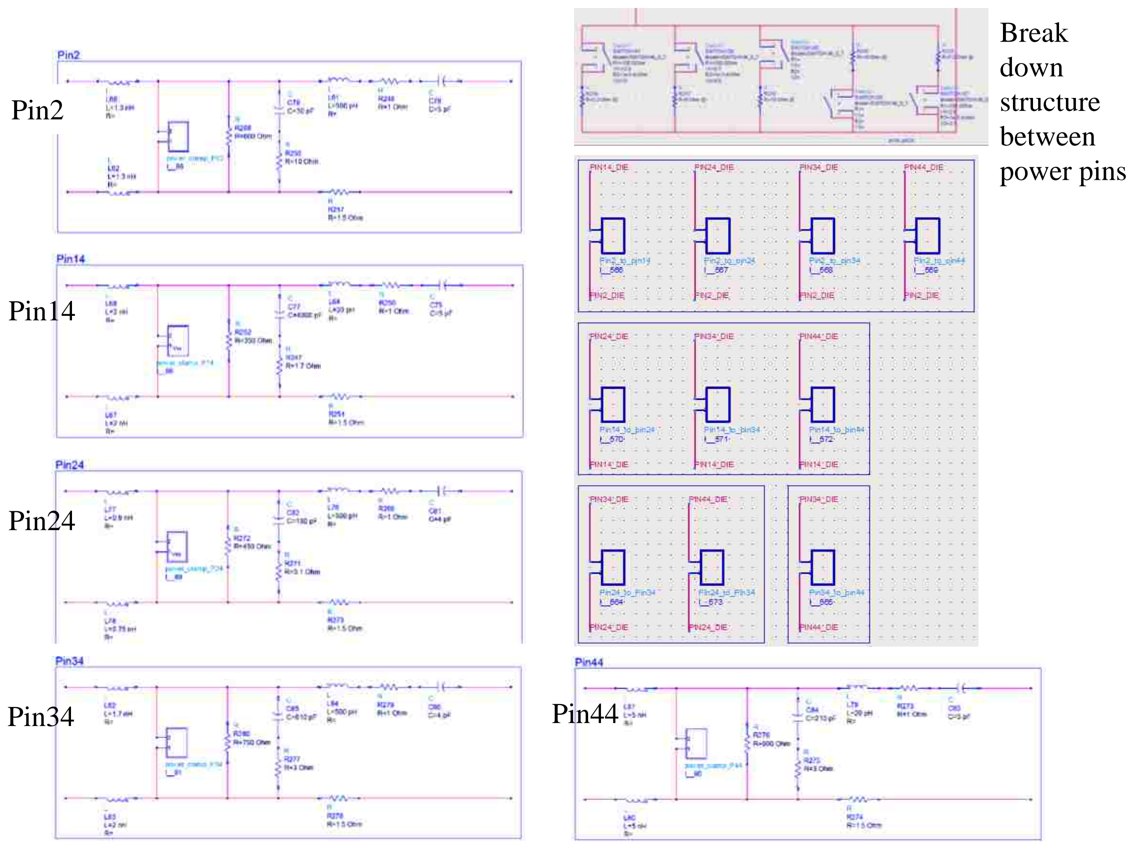

Figure 3.22. Complete model of IC PDN.

The measurements provide the data needed for creating an approximate model for the behavior with respect to ground. The observed snap back behavior is expressed by blocks connected in series. Each block describes on section of the snap back behavior. The blocks follow the principle described in Figure 3.24 and contain parallel circuits of equation blocks, resistors, and current sources. The IV curve for PD6 pin is shown in Figure 3.25.

The snap back curve is approximated by linear sections. The current sources set the break points between the linear segments. To begin from zero volts, the first current source should be removed or left at 0A.

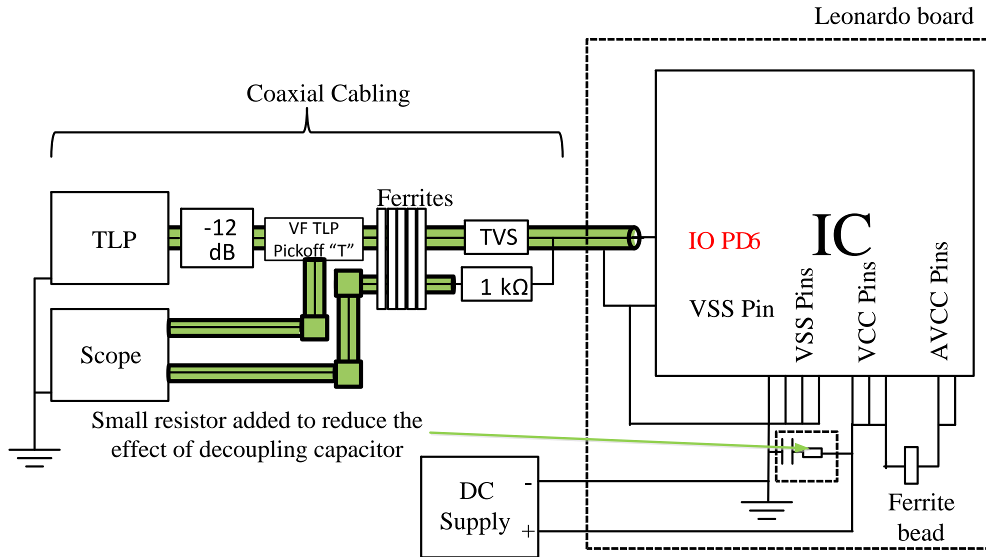

Figure 3.23. IO pin model measurement block diagram.

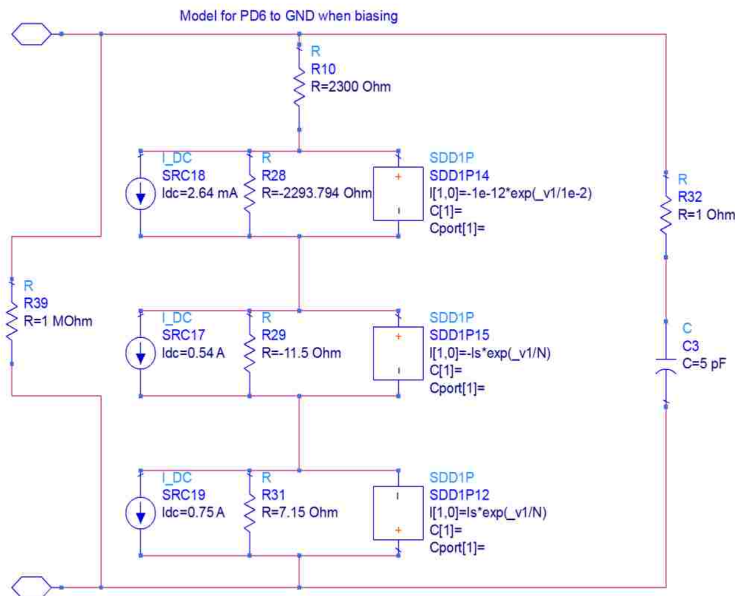

Figure 3.24. IO pin PD6 model.

The resistances represent the dynamic resistance of the linear branch. That is to say that the Nth segment of the piecewise curve has a resistance of sum (R1, R2, R3,....,RN).

The equation blocks form a diode like VI curve. When reducing the resistance of the N+1th segment from the resistance of the Nth segment is needed, the N+1th diode should have a negative Is and be reverse biased. When you need to increase the resistance of the N+1th segment from the Nth segment, the N+1th diode should have a positive Is and be forward biased.

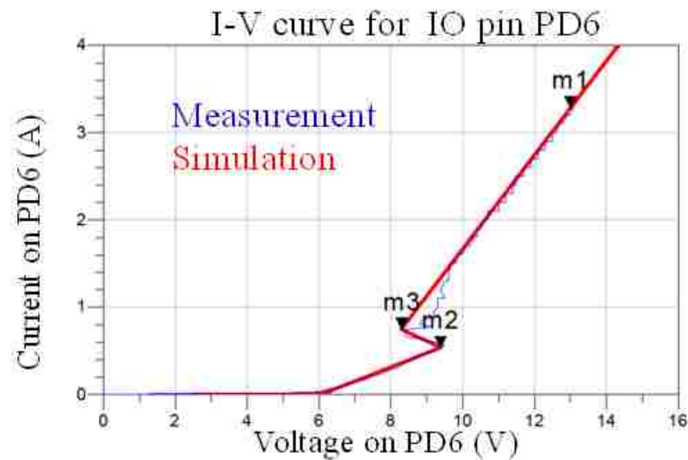

Figure 3.25. PD6 IV curve measurement vs simulation

Using this method, the snap back behavior can be modeled well, and this model can present the quasi-static behavior of the IO pin during TLP injection.

After assembled the complete model, the comparison of measurement and simulation is performed which is shown in Figure 3.26. For low voltages, the clamp remains at a high impedance and the capacitor charging waveform dominates. Once the device has clamped, it has been observed that a flatter top to the voltage and spike in the current, suggesting that the parasitic inductance plays a greater role than the decoupling capacitance.

In Figure 3.26 it has been shown that there are some jags on the measured time domain waveforms. Actually these jags are not real. When exporting the time domain waveforms from the TLP measurement software to the ADS, there are some accuracy loss. These accuracy losses caused the jags but the overall waveform shapes are OK for the comparison between the measurement and simulation results.

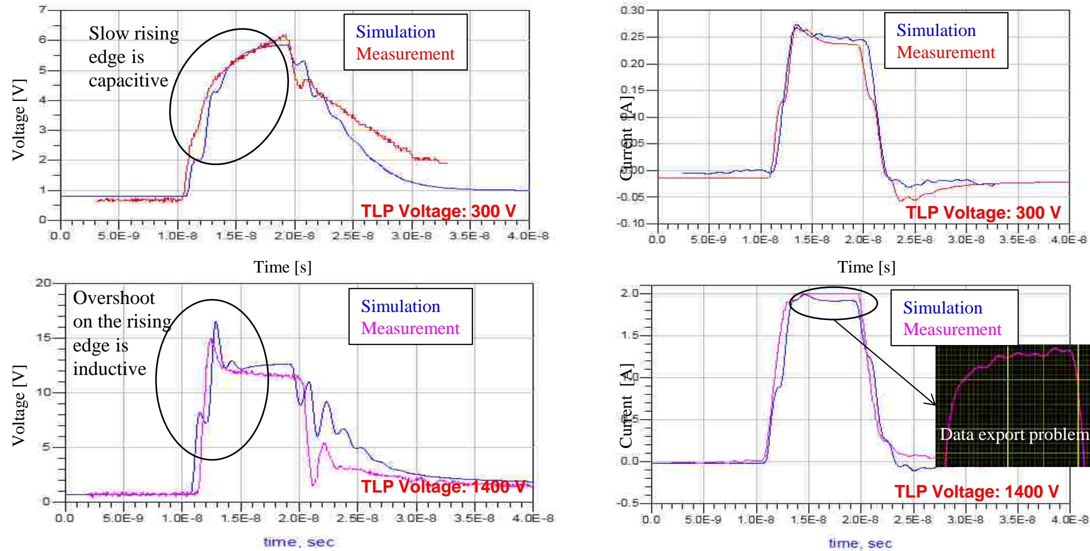

Figure 3.26. PDN model simulation vs measurement at different voltage level.

According to the TLP measurement, we have the following conclusions:

1, When TLP pulse is applied at one power pin, all the other power pins will be disturbed, since the diode between IC power pins are turned on during TLP injection.

2, by looking at the waterfall plot of different pins, it can be determined that which part of the time domain waveform can be used for the IC pin modeling.

3, by combining the RF model and large signal model together, the simulated transient time domain waveform can somehow match the measurement result.

3.5. SOFT FAILURE PREDICTION BASED ON IC MODEL

The goal of performing this test is to see if we can model the effect to predict the effect of ESD mitigation methods. The steps are as follows:

1, Measure the reference. This is done by measuring the IC’s soft error threshold on the Leonardo board without modification with the newly mounted IC.

2, Add a resistor along the IO trace under injection, then observe how the soft error threshold changes.

3, Compare the measured IV curve with the simulation result.

The measurement setup is in Figure 3.27:

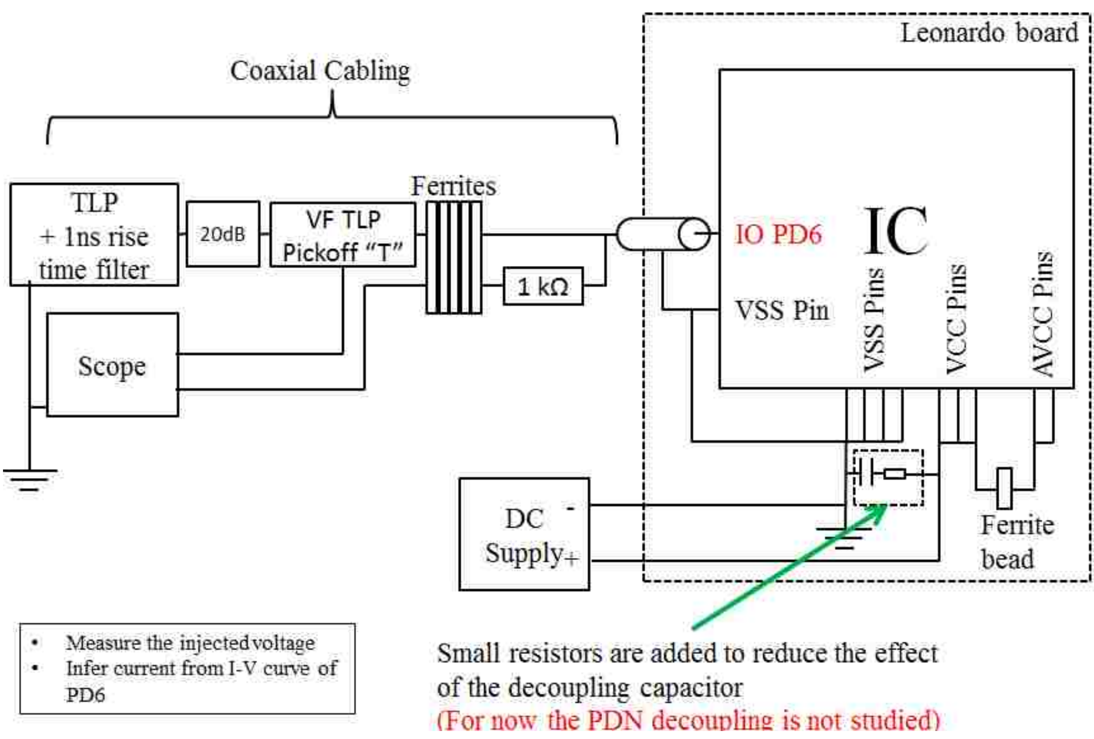

Figure 3.27. IC soft error test block diagram.

The simulation block diagram is in Figure 3.28 and the simulation result is shown in Figure 3.29.

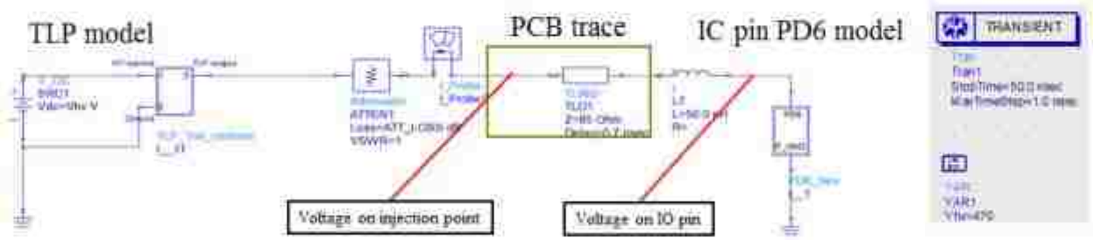

Figure 3.28. Simulation block diagram before adding 10 Ohm resistor.

The EEPROM R/W soft error threshold is as follows:

TLP charge voltage = 470V

Injection current = 0.75A

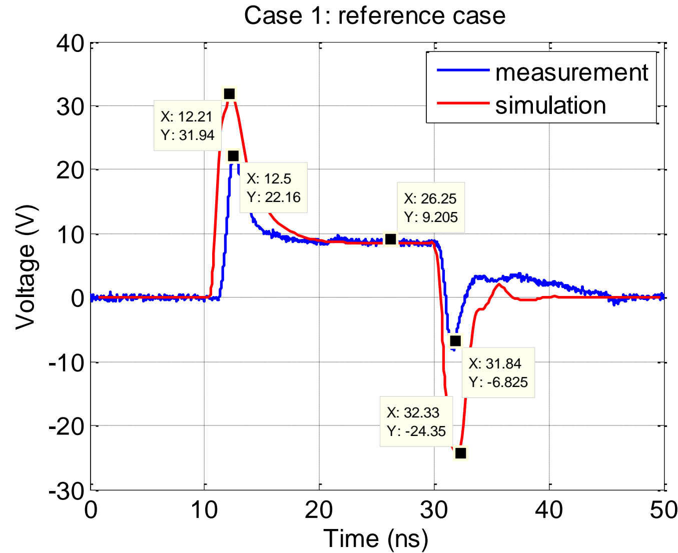

Figure 3.29. Soft error threshold – reference case.

Injection voltage at the edge of board has a peak at the beginning due to inductance in the system as well as the reflection from the IC pin model. The voltage is about 8.5V at the edge and the IO pin when stable. Figure 3.29 shows the voltage waveform at the injection point when the EEPROM R/W error occurs. From this plot we can see there is a peak at the beginning of injection which is similar to the simulated peak. After the voltage becomes stable at about 9V, the current is about 0.75A according to the IV measurement of the pin.

After adding the 10 Ohm resistor, the soft error threshold should be higher, according to the IC model; we can infer the new soft error threshold. The simulation setup is shown in Figure 3.30.

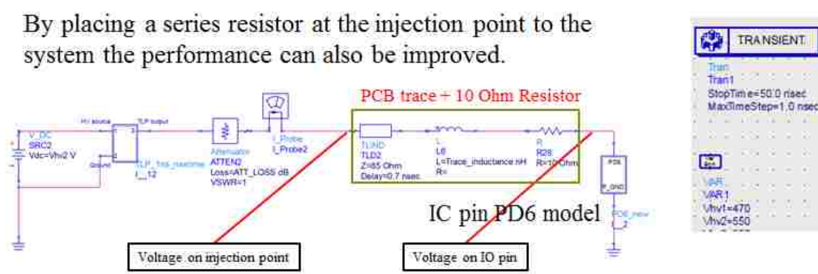

Figure 3.30. Simulation block diagram after adding 10 Ohm resistor.

The comparison between simulation and measurement result is shown in Figure 3.31 .

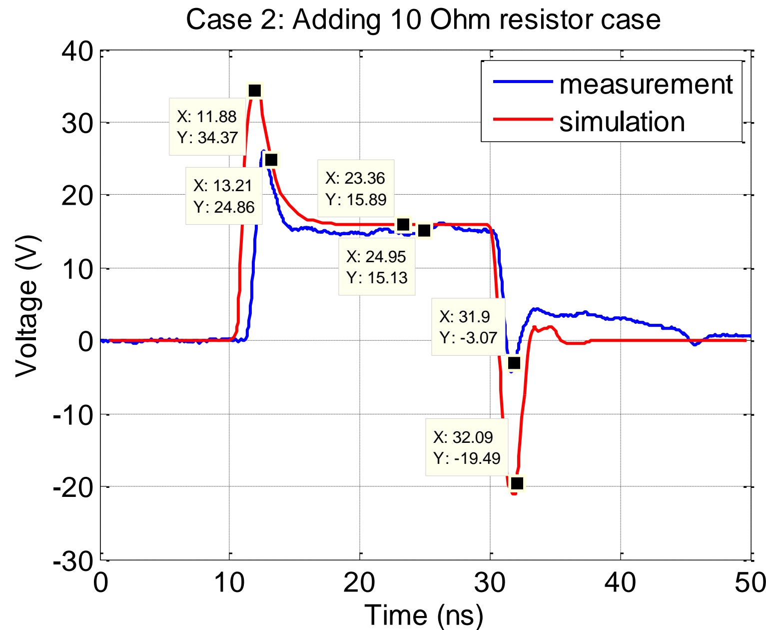

Figure 3.31. Soft error threshold – after adding 10 Ohm resistor case.

EEPROM R/W error threshold: TLP charge voltage = 550V, VDUT=16V, VPD6=8.5-9V, Istatic=0.75A. This plot shows the voltage waveform at the injection point when EEPROM R/W error occurs. From this plot we can see there is a peak at the beginning of injection which is similar to the simulated peak. After the voltage becomes stable, it is about 15-16V, according to the IV curve the calculated current is about 0.75A.

From the comparison we can see in this case, the IO behavior model can simulate the injection quite well. After adding the 10 Ohm resistor the error threshold increases by 7V.

3.6. CONCLUSION

By combining the RF measurement result and TLP measurement result the IC's I/O pin and PDN model are build. And this IC pin model can be used for soft error threshold prediction and also can be used to evaluate the effect of ESD protection design.

4. PDN NOISE INJECTION FOR SOFT FAILURE ROOT CAUSE ANALYSIS

4.1. INTRODUCTION

During root-cause analysis of observed soft failures in systems, it is necessary to understand the chain of events. This chain usually consists of some ESD event which somehow travels through the system and upsets an unknown victim, resulting in a soft failure. In the context of a system-level ESD issue, the chain of interest is: entry point -> coupling path -> victim IC. Such a chain is usually sufficient to solve the problem by making low-cost changes to the system such as redesigning the PCB or altering cable or connector geometry.

In this session, we focus on the victim IC and perform a more in-depth root-cause analysis to determine where inside the IC the upset occurs. The goal is therefore to determine if the victim IC is subject to a local error or to a distant error [4], possibly caused by a disturbance on the system power distribution network (PDN). Because it is often impossible to look inside an IC to measure voltages and currents at different points along the resistive IC-level PDN, the following measurement technique cannot account for errors caused by disturbances inside the IC package and therefore focuses on board-level PDN events.

In order to detect whether or not the error condition is caused by PCB-level PDN fluctuations, two methods are presented for mirroring the voltage disturbance on VDD that occurs during an observed soft failure. In this paper a small microcontroller featuring an ATMega32u4 is used as the DUT. Several simple programs are written for this IC which can be used to activate different functional blocks of the processor such as the EEPROM, A/D converter, or GPIO pins.

4.2. SOFT FAILURE DETECTION METHODOLOGY

In order to search for various soft failure susceptibilities, the DUT IC was placed into one of several infinite loops. The program structure is shown in Figure 4.1 where the $OPP block performs one of the following operations: ADC read, EEPROM read, and an IO pin read. This method was chosen as a way to activate specific functional blocks of the IC while the interference method remains constant.

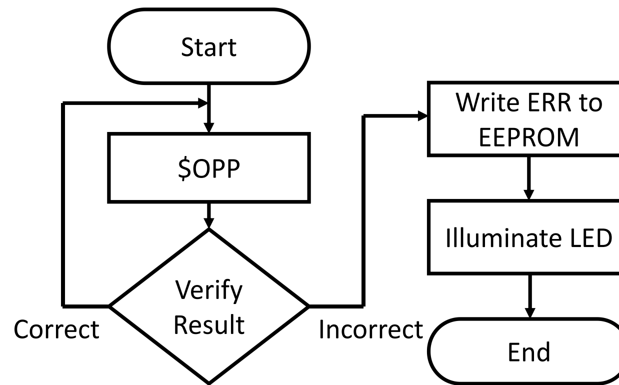

Figure 4.1. Stress program structure.

The stress pulse is provided by a transmission line pulsing system [5] attached to various pins of the DUT. A photograph of the injection is shown in Figure 4.2.

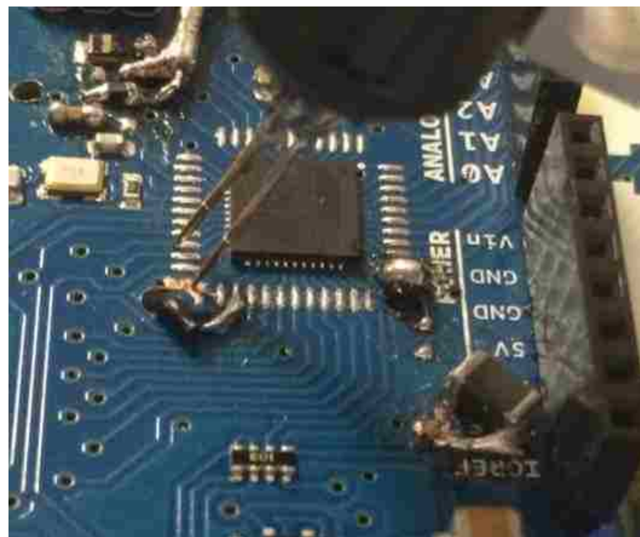

Figure 4.2. TLP Injection probe landed on the DUT.

4.3. MIRRORED (PASSIVE) PERTURBATION

The first method couples the PDNs of two separate DUTs together, forcing them to share similar high frequency disturbances. In this way, an injection on DUT A which results in a soft-failure will mirror any high frequency PDN disturbances onto DUT B, placing it in a similar set of conditions. Because each DUT is supplied by an independent power supply, affects such as brown outs resulting from events such as latch-up are not mirrored into DUT B. Conceptually this configuration can be viewed as the DUTs

attached to two separate power supplies through low pass filter networks and shorted together near the ICs. This ensures that the low frequency load on each supply is not significantly different from normal operation, but that the DUTs both share similar noise profiles. A block diagram is shown in Figure 4.3 and a photograph of the implementation is shown in Figure 4.4.

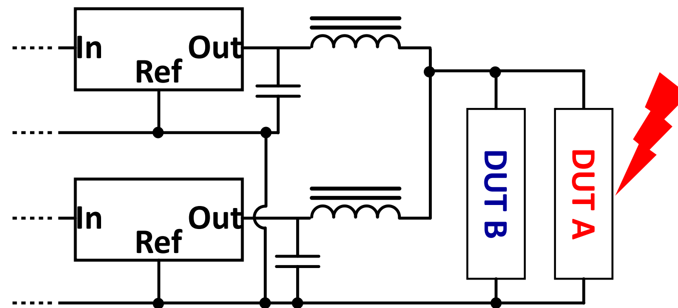

Figure 4.3. Schematic representation of the image injection method.

Figure 4.4. Photograph of the joined DUTs.

Using this configuration, the voltages at both DUTs was measured independently during injection to observe the effectiveness of the high frequency coupling. An example waveform during GPIO injection on DUT A.is shown in Figure 4.5.

From this we see that the PCB-level PDN disturbance is nearly exactly duplicated onto DUT B by injection on DUT A, verifying good connectivity between the DUTs. The DUT pair was then stressed during each program. The results are recorded in Table 4.1.

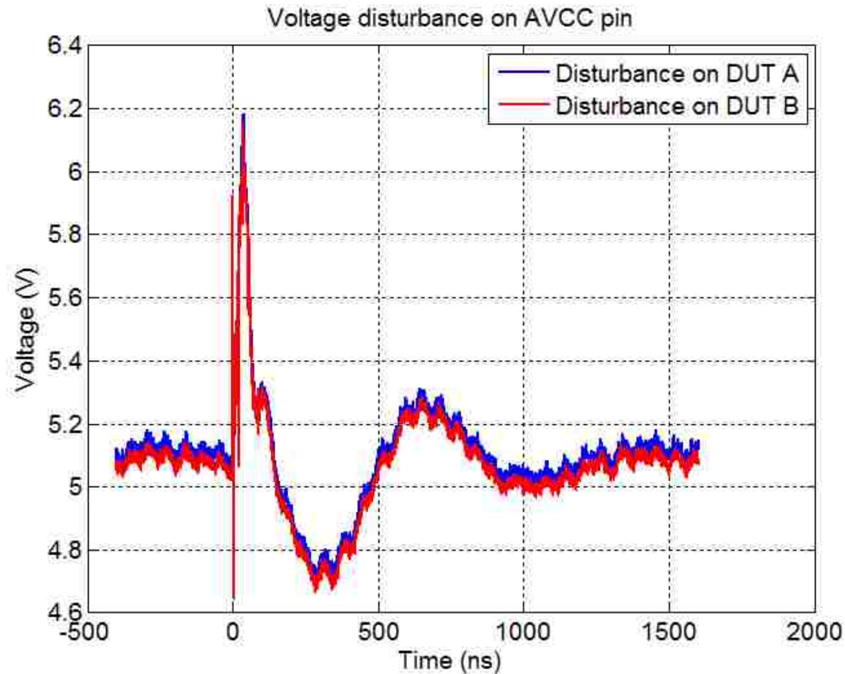

Figure 4.5. The mirrored voltage disturbance at pin 34 (VCC) on the two DUTs.

Table 4.1. Mirrored Perturbation Failure Results.

Test	DUT A (I/O)	DUT B (PDN)
ADC Read	A soft error is observed @ Vdut ≈ 15 V, Idut ≈ 3.5A	No error
EEPROM Read/Write	A soft error is observed @ Vdut ≈ 13 V, Idut ≈ 3A	Duplicate Error
GPIO Read	A soft error is observed @ Vdut ≈ 15 V, Idut ≈ 3.5A	No error
Watchdog Reset	A soft error is observed @ Vdut ≈ 13 V, Idut ≈ 3A	Duplicate Error

Using this method, the EEPROM read/write and watchdog reset errors were able to be triggered by the independent PDN disturbance, indicating that the root cause of

such errors is actually the supply stability and not the current injected into the IO pin itself. The ADC and GPIO read errors were not duplicated by this technique.

4.4. PLAYBACK VIA ARBITRARY WAVEFORM INJECTION

The second method can be implemented on only a single DUT by recording the voltage disturbance on the DUT PDN during an error condition and then “replaying” the disturbance through a high power amplifier to recreate the VDD waveform. This replay method results in a greater disparity between the two DUTs, but the interference is still very similar. Figure 4.6 shows a block diagram of the injection system used to disturb the VDD network. The voltage waveform is first recorded from the DUT during the IO injection and then replayed through an amplifier into the same DUT to duplicate the VDD disturbance at a later time.

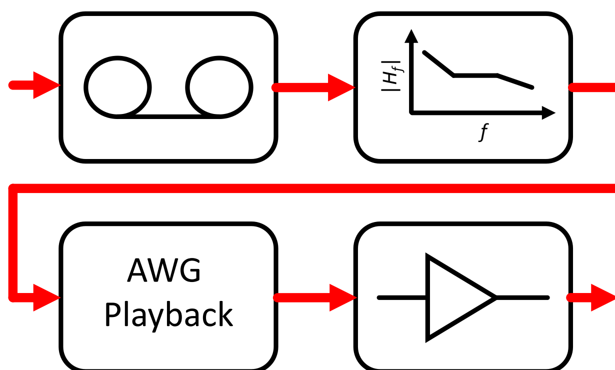

Figure 4.6. AWG Injection flowchart.

Figure 4.7 shows the resultant disturbance of the injection system. Using this method, the disturbance on VDD is nearly exactly recreated without the need for a duplicate DUT or carefully crafted VDD network. The primary down-side of this method is the increased time required to perform two sets of tests as well as the additional equipment required by the method. The results of the tests DUTs during GPIO injection on DUT A are shown in Table 4.2.

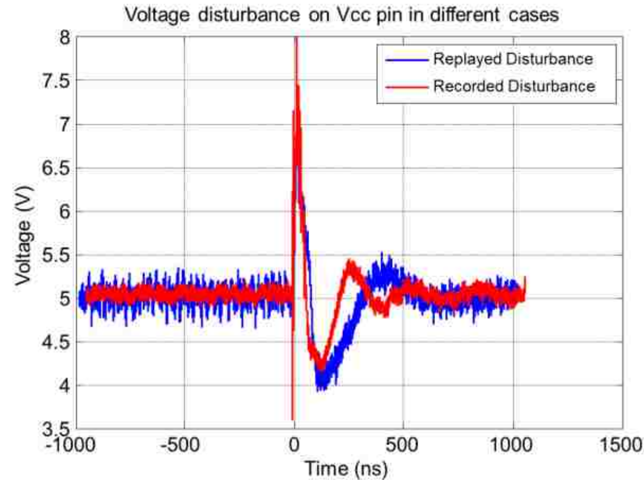

Figure 4.7. The generated voltage disturbance at pin 34 (VCC) on the two DUTs.

Table 4.2. Active PDN Disturbance

Test	Injection A (I/O)	Injection B (PDN)
ADC Read	A soft error is observed @ Vdut ≈ 15 V, Idut ≈ 3.5A	No error
EEPROM Read/Write	A soft error is observed @ Vdut ≈ 13 V, Idut ≈ 3A	Duplicate Error
GPIO Read	A soft error is observed @ Vdut ≈ 15 V, Idut ≈ 3.5A	No error
Watchdog Reset	A soft error is observed @ Vdut ≈ 13 V, Idut ≈ 3A	Duplicate Error

Running the same test cases using the second PDN disturbance method results in the same failure signature as revealed by the first method. Both the EEPROM and the device watchdog were disturbed by the intentional PDN disturbances however the ADC and GPIO read operations were not.

4.5. CONCLUSION

In this session, two methods are presented to duplicate the disturbances on the VDD of a system. Both methods can recreate the voltage disturbance on the PCB-level

PDN with reasonable accuracy and are used to trigger soft failures which are also observed when an IO pin is the source of the disturbance. These tests indicate that the observed errors may be caused by the secondary effect of a voltage disturbance on the PCB PDN as a result of current injected onto the bus by the ESD protection rather than by the injection into the IO pin itself.

5. CONCLUSION AND FUTURE WORK

Using three different hardware measurement methods, potential soft failures can be detected without the aid of a mature software stack. The methods were demonstrated on two DUTs of different levels of complexity, showing changes in operation due to injection without invasively monitoring the system state. The thermal imaging is good, it is easy to do and no need to adding wires, cables, etc. to the system. But some errors or error situation will not be visible. DC voltage measurements are not so difficult to do, but they only show useful information under some situations, like power supply disturbance, or latch ups. STFFT and spectrum take some luck to find a change caused by an ESD, but we see that it is possible. Sometimes the changes are kind of small, or some very small frequency component. In addition, STFFT takes time, since the data needs to be captured and then transport the data to Matlab. It would be good to have a much faster STFFT process, like Scope via LAN to Matlab, etc.

Using TLP injection method, different types of soft error are observed on different DUTs. For the Arduino Leonardo board, the most frequent occurred soft errors are: EEPROM Read/Write error and IC reset error. I/O read error; calculation error and ADC error are not easy to be observed. For Open-Q 8084 mobile development board, LCD display error and USB communication error have been found during TLP injection.

In the Arduino Leonardo board case study, several ways has been tested to observe soft error, first approach and the most naïve approach is to observe the DUT behavior change, such as system log, message box on the DUT screen, LED status. However in some case there is no such obvious status change on the DUT, that’s why another method has been used for soft error detection: using STFFT method to observe how the spectrum change before and after ESD injection.

In order to identify the root cause of soft error, several different test methods have been used. Using image injection method and AWG+RF-AMP method, EEPROM R/W error is observed. So there is a strong indication that the EEPROM R/W error is PDN related distant soft errors. Comparing with the image injection method, AWG injection system can be applied to more complicated systems. But it requires more complicated measurement setup and compensation.

The image injection system can only work for some simple system, like Leonardo board, But the AWG injection system can be used for more complicated system. And still some more improvement can be done to make better performance.

After understanding the soft error root causes, an ADS model has been built to characterize the IC. The ADS model is a combination of parasitic capacitors / inductors / resistors and ESD protection diode/power clamps. In order to measure the parasitic capacitors / inductors / resistors, VNA has been used to measure the S-parameter between different ports. The S11 can be converted to Z11. With the Z11, the parasitic capacitors / inductors / resistors can be determined. For characterize the ESD protection diode and power clamps, TLP will be used to measure the IV curve of IC pins. Based on the IV curve, non-linear model of the IC can be build.

With the complete IC model, the soft error threshold can be predicted if some other protection devices are added to the system. This can be used to guide ESD protection circuit design in the future products.

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VITA

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