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# Methodology for 3D full-wave simulation of electrostatic breakdown across an air gap

Darwin Zhang Li



Department:

# METHODOLOGY FOR 3D FULL-WAVE SIMULATION OF ELECTROSTATIC BREAKDOWN ACROSS AN AIR GAP

by

DARWIN ZHANG LI

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James Drewniak
Victor Khilkevich

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Paper I: Pages 4-21 have been accepted by the Electrostatic Discharge Symposium.

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Paper III: Pages 38-63 have been submitted to IEEE Transactions on Electromagnetic Compatibility.

# ABSTRACT

The Rompe-Weizel SPICE model is used to obtain the time dependent arc resistance during simulation of air gap discharge. The SPICE model is solved using a circuit simulator, and the accompanying 3D model is solved using the transmission-line matrix time domain numerical method. Transient co-simulation is a new technique that is used to solve both circuit and 3D models at the same time. Transient co-simulation with the Rompe-Weizel SPICE model is first validated for different arc lengths using a simple geometry of a rod discharging to a ground plane. Validation is achieved by comparing the discharge currents from simulation with measurement. Next, a new simulation setup that uses a circuit switch along with the Rompe-Weizel model to capture the full physics of the Secondary ESD is tested. This simulation setup is tested by using an adjustable spark gap structure to generate Secondary ESD and validating it with measurements of the voltage across the gap and the discharge curents. Finally, the methodology is tested for practical usage by simulating the Secondary ESD in an actual smartphone product that is susceptible to secondary breakdown. The system level simulation predicts the coupling from ESD to a victim trace in the smartphone. Measurements performed at several stages of modeling the smartphone validate the simulation results. Using this novel methodology, the user can simulate secondary discharge in products to predict ESD damage and disruption on a system level.

# ACKNOWLEDGMENTS

Most of the work here was funded in part by the National Science Foundation (NSF) under Grants IIP-1440110. However, I would like to acknowledge Dassault Systèmes and Computer Simulation Technology, both of which sponsored my master's thesis. Specifically, I would like to thank Dr. David Johns, who provided me with this opportunity to expand my knowledge and career and for being as understandable as possible to the time commitment required for this thesis. Furthermore, most of the work here was done using the Transmission Line Matrix algorithm, which was invented by the Johns'; without this algorithm, most of these simulations would not be possible.

I would also like to thank my advisor, Dr. David Pommerenke, who was understanding during my surgery, recovery, and overall situation. Balancing work, school, and research was extremely hectic, but under Dr. David Pommerenke, it was manageable. I want to also give special thanks to Dr. Ahmad Hosseinbeig because his work ethic and eagerness to help me was inspiring.

Of course, I would like to thank my friends and family in San Francisco who provided me emotional support.

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# 1. INTRODUCTION

## 1.1. BACKGROUND

Damage and soft failures from ESD (Electrostatic Discharge) are well known and characterized by the coupling from the discharge point to the sensitive circuit. Non-contact air ESD can cause damage directly to electronic components such as the case of a human finger discharging to a fingerprint module (Wei *et al.*, 2017). Furthermore, one ESD may cause a secondary ESD within a product. This occurs if the primary ESD (which can also be sourced by a human body) causes a voltage between a non-grounded part, e.g., a decorative piece of metal and the grounding of a system. If this gap breaks down, the currents in the electronic system can reach much higher values than the primary ESD (Wolf and Gieser, 2015). For this second case of secondary ESD, the damage or disruption is not direct; but rather, there is a coupling path that leads to voltage on a victim trace (Wolf and Gieser, 2015). Work by Park *et al.* (2017) alludes to this as they have developed a measurement technique to look at voltages developed at the suppressor devices due to Secondary ESD on a system level. As such, there is a need to develop a simulation methodology suitable for system level analysis of Secondary ESD.

Past works by Liu *et al.* (2011) and Xiao *et al.* (2012) explain the simulation of air discharge, but skip the investigation of the system level coupling inside a product. Furthermore, they use an unsuitable approach with a frequency domain representation of the model. The work presented here uses the novel technique of transient co-simulation to

bypass the need for a frequency domain representation, so neither the high bandwidth due to the fast rise time of ESD nor the prohibitively long simulation required for accurately capturing the low frequency points in a system with large capacitances is a problem.

## 1.2. CO-SIMULATION

The term "co-simulation" as used in this paper and by CST (2017) refers to a hybrid electromagnetic full-wave algorithm with circuitry. In all implementations of electric breakdown simulation thus far, circuit components are used to capture the non-linear physics behind the arc formation. So, there is a need to include the circuitry with the full-wave simulation. There exists multiple types of co-simulation, and currently the widely available version is a "circuit co-simulation" where the full-wave model is treated as another circuit element in the frequency domain. A relatively new co-simulation method is called "transient co-simulation" where the circuit inputs and outputs of Voltage/Current are passed through the full-wave algorithm's inputs and outputs of E-Field/H-Field. This passing of inputs and outputs at the interface between circuit and full-wave occurs at every time-step of a time-domain based full-wave algorithm. Generally, circuit co-simulation is a two step process:

1. The structure is simulated using a 3D solver (time or frequency domain). This 3D analysis provides the full S Matrix.

2. The S Matrix is used in the circuit simulator for further tasks such as finding the response due to the Rompe-Weizel model.

This two-step process is not complete with regards to field results. The method and results from Liu *et al.* (2011) show that it is possible to take the currents from the two-step process and then re-import them into CST as a custom waveform to get the transient fields. However,

this method of re-import is not generalized to other Rompe-Weizel model applications such as secondary air discharge, which depends heavily on voltages at the gap (Xiao *et al.*, 2012). Furthermore, the re-import method still requires two simulations.

Transient co-simulation requires only one simulation and does not require a re-import. Transient co-simulation is complete and essential for ESD simulation and visualization of transient surface currents due to the ESD event. Prior to this work, no paper has successfully used transient co-simulation to full efficiency and potential in simulating air discharge. Transient co-simulation is used with 3D transient solvers (FIT or TLM) and time stepping is performed on the circuit and 3D level simultaneously. This then allows field visualization with included non-linear elements in the 3D simulation.

## 1.3. ORGANIZATION

The work presented in this thesis is chronological. Each simulation component is gradually validated – from the Rompe-Weizel SPICE model (Pommerenke and Aidam, 1996), to the ESD Generator (Liu *et al.*, 2009), and even the DUT (Device Under Test) smartphone. Each paper builds on the previous by adding more complexity with the end goal of presenting a practical methodology to simulate non-contact ESD and secondary ESD and predict the disruption on a system level. For the three papers presented in the thesis, I performed every single simulation. Though I was not the first author in Paper II, the simulation methodology of adding a circuit switch to achieve the full physics of Secondary ESD was pioneered by me. Also, the explanation of the physics and 3D/circuit modeler were all written by me.

# PAPER

## I. TRANSIENT ELECTROMAGNETIC CO-SIMULATION OF ELECTROSTATIC AIR DISCHARGE

D. Z. Li

Department of Electrical Engineering

Missouri University of Science and Technology

Rolla, Missouri 65409–0050

Tel: 415-375-0867

Email: dzldh8@mst.edu

## ABSTRACT

Transient electromagnetic co-simulation is used to simulate the currents in a discharging rod. The simulation model simultaneously solves Maxwell's equation and the arc resistance equations in time domain to estimate the currents and fields for a given geometry, charge voltage and arc length. The Rompe-Weizel model is used to obtain the time dependent arc resistance, and results from different simulation methods are compared to measured data.

## 1. INTRODUCTION

ESD discharge between metal parts can produce discharge currents up to hundreds of ampere at sub nanosecond rise times. The current levels and rise times depend on the voltage and the local source impedance which drives the current, but also on the time dependent arc resistance which is a strong function of the arc length. The fields associated with

such currents will couple into flex cables, PCBs and other metallic structures. To simulate such currents one needs to combine an electromagnetic description of the geometry with a non-linear description of the arc resistance (Pommerenke, 1995). A variety of approaches has been published such as those by Jobava *et al.* (1998), Fujita and Namiki (2013), and Fujita *et al.* (2017) which prove the concept of non-contact ESD numerical modeling and simultaneous time-stepping with SPICE, but these are only suitable for simple geometries with numerical methods that are rarely used for consumer electronics design. In this paper, we explain and compare multiple methodologies to solve for air discharge current and fields within the widely used CST Studio Suite (CST, 2017). For methodology, the full-wave simulation is either combined with the arc resistance law of Rompe-Weizel (RW) directly by exchanging voltage and current information in every time step or the combination is achieved by a two-step process which first simulates impedances which are then combined with the arc model in a circuit simulation. Using a simple model of a discharging rod, it is shown that the methodology can match measured current and current derivative results. As for the significance to system level ESD, simulation of contact mode ESD is already widely used in industry to predict results such as soft failures (Kim *et al.*, 2010), and we will analyze how this new methodology can improve the existing simulation workflows with a simple real world example with an ESD gun.

## 2. MEASUREMENT TECHNIQUES

The experimental setup is similar to the one used in Pommerenke (1995).

**2.1. Measurement Equipment.** Figure 1 shows the test setup. A 102 cm long rod with 1.80 cm diameter placed above ground forms a transmission line impedance of about 200 ohm characteristic impedance.

The tip of the rod is round. The diameter reduces from 1.8cm to 1.35 cm close to the discharge point as shown on the transition on the rod in Figure 2.


Figure 1. Test setup showing the rod, arc length measurement, oscilloscope in a shielded enclosure and the high voltage supply inside a climate chamber.

**2.2. Measurement Procedure.** The rod is charged to 6, 8, or 10 kV and moved towards the ESD current target. Once a discharge event occurs, the arc length is measured and the current is recorded. For slow approach speeds, the arc length will equal the value predicted by Paschen's Law. For faster approach speeds, the arc length is reduced due to the interplay of the statistical time lag (Wan *et al.*, 2014) and the speed of approach. For the purposes of the measurement procedure, âĂIJslowerâĂİ and âĂIJfasterâĂİ approach speeds are only qualitative and there was no measurement made on the actual speed the experimenterâĂŹs hand moved. Qualitative approach speed is confirmed to be sufficient since the experimenter was able to collect a good range of raw data to view in Figure 3. The setup of this equipment and data collection is explained in detail in (Pommerenke, 1995).

Figure 2. Rod Tip and parts of the arc length measurement system.

**2.3. Measurement Results.** Figure 3 presents measured results for the peak current derivative and compares them to published data (Pommerenke, 1995) of a related, but not identical geometry. The comparison indicates a general agreement which gives confidence in the measured data. Furthermore, this also gives confidence in the basic underlying arc resistance law.

## 3. SIMULATION TECHNIQUE

**3.1. Simulation Modeling.** Four different simulation models and methods are used. Z-Parameters used here is synonymous with Impedance Parameters, which are defined as a matrix of N by N size solved by $V_m = [Z_{m,n}]I_n$ for an N port network where $V_m$ and $I_n$ are the Voltages and Currents at port $m$ and $n$ respectively. Z-Parameters may be transformed into S-parameters and vice-versa.

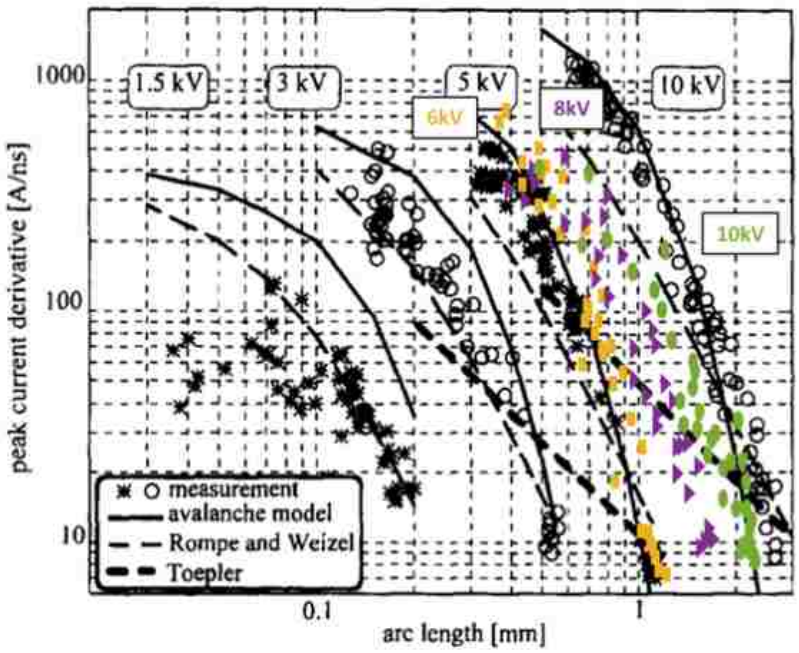


Figure 3. Peak Derivative Current measurement results at 22% Humidity and 15°C overlaid on the results published in (Pommerenke, 1995)

a) The rod model's impedance between the end of the rod and the ESD target is simulated in frequency domain using Finite Element Method (FEM). The impedance information (Z-parameters) is compared to the other simulation algorithms (Figure 6)

b) The same is done with the Finite Integration Technique (FIT) for Figure 6.

c) The same above is done with Transmission Line Matrix (TLM) for Figure 6, but in addition to it, the Z-Parameters, expressed as S-parameters is used in a SPICE-like simulation after combining it with the arc resistance model. This produces the results in Figure 9.

d) A transient co-simulation is performed. During the transient co-simulation, the arc resistance model is directly attached to the 3D structure. During each time step voltage and current information is exchanged between the arc resistance model and the electromagnetic simulation. For the transient co-simulation the voltage and arc length must be given prior to starting the simulation.

Figure 4 depicts the CST Microwave Studio simulation model. The ports in the 3D modeler connect to the circuit simulator which allows for modeling non-linear elements such as SPICE models.

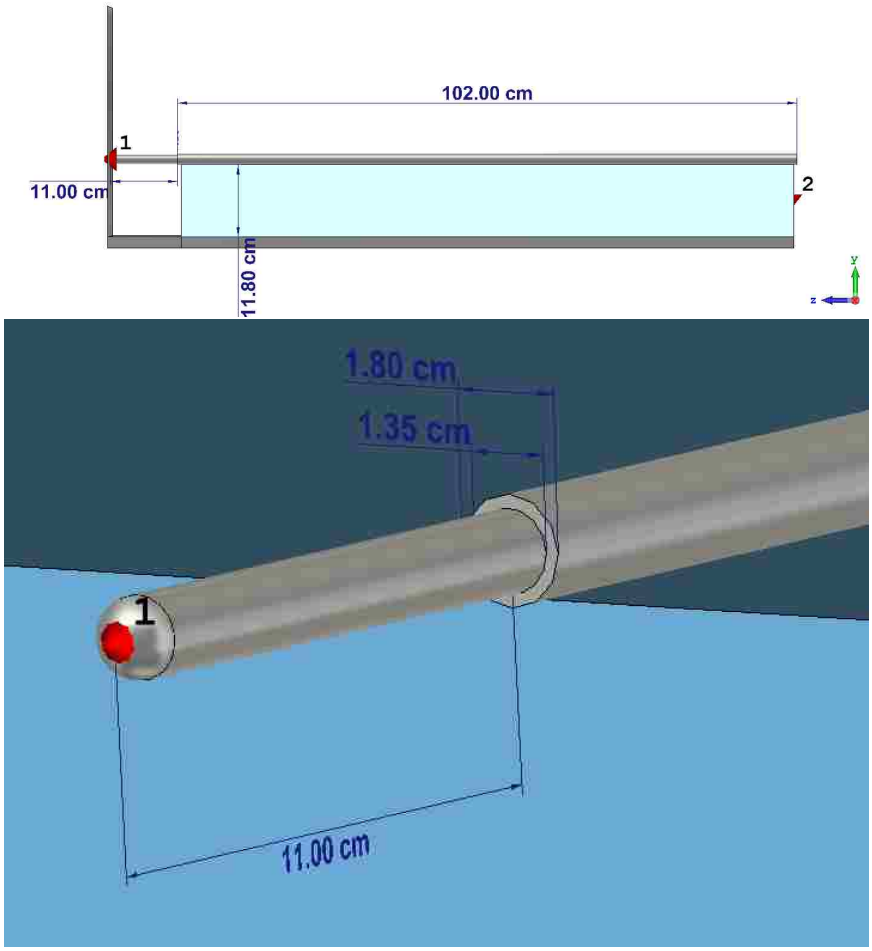


Figure 4. Rod with round tip discharging to a ground plane. Labels 1 and 2 are the ports

Figure 5 shows the different meshing schemes. It is apparent that the sub-gridding utilized by the TLM mesh is the most efficient grid solution. It avoids gridding regions that do not need fine grid (grid bleeding) seen in the FIT grid. The TLM solution is obtained in 25 minutes vs. 45 minutes in FIT. Experience in comparing TLM to FIT solution has shown that the optimal solution is problem dependent, however discussing the underlying reason is beyond the scope of this paper. Neither method shows consistent advantage over the other gridding method. As the TLM solution offered faster solution speed it was used in most of the simulations presented here.

Since transient-co-simulation requires a time-domain algorithm to simultaneously pass the voltages and currents between the 3D full-wave model and the non-linear circuit elements, FEM cannot be used to obtain non-linear time domain results directly. Nevertheless, it is good to run with FEM at least to show the agreement of the Z-Parameters at low frequency as shown in Figure 6.

Figure 7 shows the circuit modeler in CST that integrates the 3D Model and the circuit elements.

At Port 1, the same input voltage waveform is used as in Liu *et al.* (2011) and Pommerenke and Aidam (1996), which is a high voltage pulse. The Rompe-Weizel model (abbreviated as RW) describes the time-dependent arc resistance (Pommerenke, 1995):

$$R(t) = \frac{d}{\sqrt{2 \cdot a \cdot \int_0^t i(x)^2}} \tag{1}$$

where $R$ is the arc resistance in Ohms, $d$ is the gap distance of the electrode or arc length in meters and will be swept for different values in simulation. $a$ is an empirical constant with value of $1.5e-4\frac{m^2}{(V^2 \cdot s)}$ and $i$ is the discharge current in amperes.

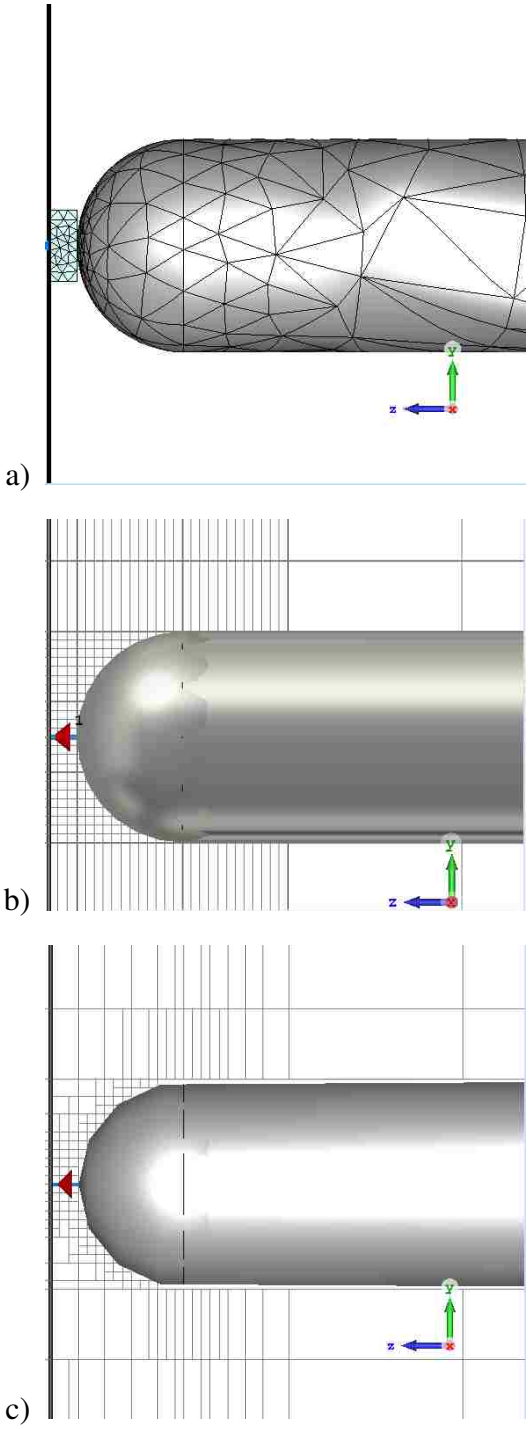


Figure 5. Different meshing algorithms: a) FEM, b) FIT, and c) TLM

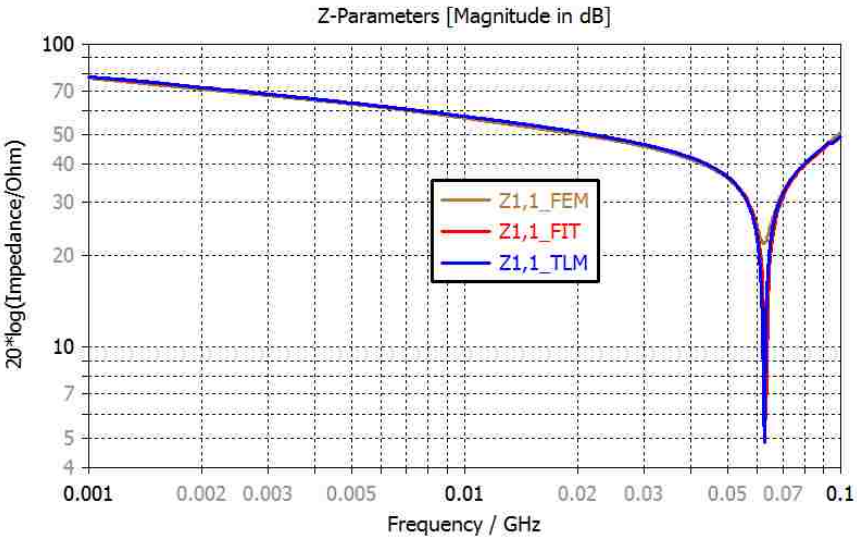


Figure 6. Z-Parameters comparison for the impedance between the tip of the rod and ground for three full-wave algorithms

The SPICE code for the RW model is given in Pommerenke and Aidam (1996) and was adapted to be compatible with CST. There are two methods presented in this paper to run the simulation with this SPICE Model. The first method presented in this paper is a two-step process for obtaining currents:

1. The structure is simulated using a 3D solver (time or frequency domain). This 3D analysis provides the full S Matrix.

2. The S Matrix is used in the circuit simulator for further tasks such as finding the response to the RW model.

This two-step process is not complete with regards to field results. The method and results from Liu *et al.* (2011) show that it is possible to take the currents from the two-step process and then re-import them into CST as a custom waveform to get the transient fields. However, this method of re-import is not generalizable to other Rompe-Weizel model applications such as secondary air discharge, which depends heavily on voltages at the gap (Wolf and Gieser, 2015). Furthermore, the re-import method still requires two simulations. The

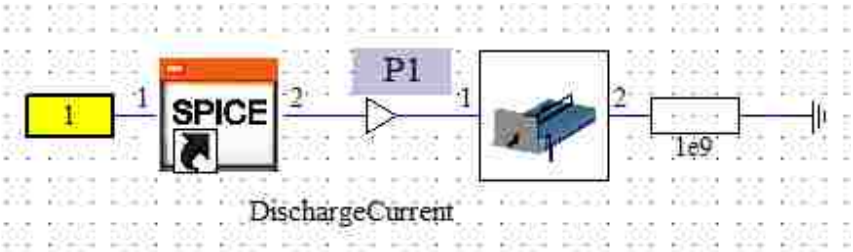


Figure 7. Circuit setup in CST Design Studio with Port 1 connecting to the Rompe-Weizel spice mode, a probe to monitor the current at P1, the connection to the 3D Rod model's port placed at the rod's tip, and a large value termination resistor connected to the other port at the rod in its 3D representation.

second method presented in this paper, which is transient co-simulation, requires only one simulation and does not require a re-import. As explained below, Transient co-simulation is complete and essential for ESD simulation and visualization of surface currents in time due to the ESD event. Transient-co-simulation is used with 3D transient solvers (FIT or TLM) and time stepping is performed on the circuit and 3D level simultaneously. This then allows field visualization with included non-linear elements in the 3D simulation.

## 4. RESULTS AND DISCUSSION

**4.1. Comparing Current Waveforms.** It is not possible to match the current waveforms exactly to measurement, but for ESD induced soft-failure, mainly the peak current and current rise time are the results of interest. As shown in Figure 8, the simulated current waveforms have the correct features which include the peak discharge current. After the first peak one needs to consider that the RW model leads to a very low resistance and a low voltage drop along the arc. However, the real arc may act more like a constant voltage drop of 25-40V. At present, we did not include this transition from a resistive phase to a constant voltage drop phase into the modeling.

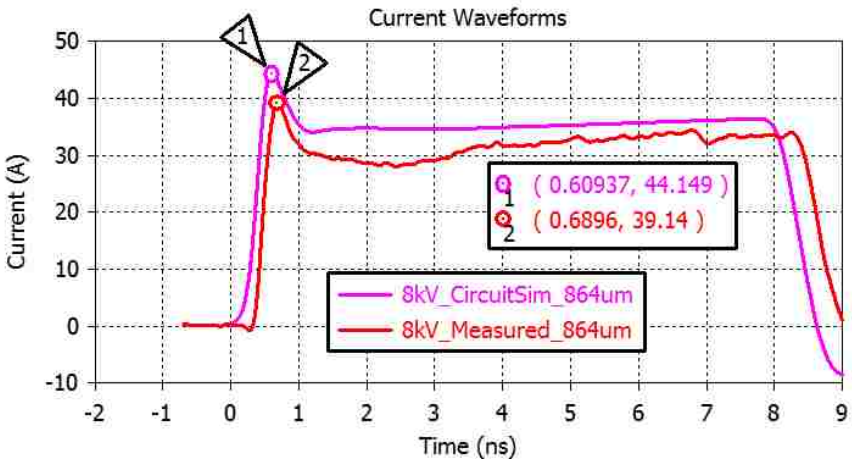


Figure 8. Comparison of the Current Waveform with the peaks.

**4.2. Comparing Simulation to Measurement for Different Gap Lengths.** Arc length $d$ in the SPICE file is swept at 0.1 mm to simulate the $\max(\frac{di}{dt})$ vs. arc length at step 2) of the two-step process. We treat arc length as being the same as the gap distance between the tip of the rod and the ground plane. We are interested in $\max(\frac{di}{dt})$ vs. arc length because rate of current change and the associated rise time are important with respect to induced noise voltages. This comparison is shown in Figure 9. Since the measurement data is bandwidth limited by the oscilloscope, a 3 GHz filter with rectangular response is applied:

$$H(f) = \begin{cases} 1 & \text{if } f < 3 \text{ GHz} \\ 0 & \text{if } f \geq 3 \text{ GHz} \end{cases}$$

The following steps are taken to apply the filter:

1. Obtain the current waveform (Simulation)
2. Fourier Transform (Post-Processing)
3. Apply the above low pass filter (Post-Processing)

4. Inverse Fourier Transform (Post-Processing)

5. Compute max($\frac{di}{dt}$) (Post-Processing)

The results shown in Figure 9 represent the measured data and the simulation. The simulation data is shown as functions relating the max($\frac{di}{dt}$) to the arc length. The measurement data is presented as one value per measurement performed. Both measured and simulated data show an increase of the max($\frac{di}{dt}$) if the arc length is reduced. However, this increase levels off. The leveling off is a result of the measurement bandwidth and can be matched by simulation if a 3 GHz low pass filter is applied. Each of the voltage levels has distinct results, which is the correct behavior that implies repeatability (Pommerenke, 1995). For the transient co-simulation, it is swept at 0.2 mm intervals but the results are exactly the same as the two-step process.

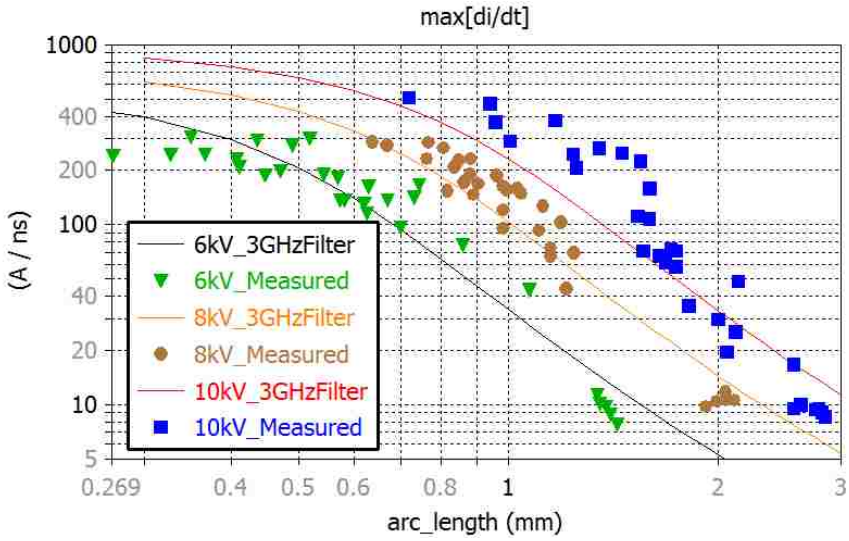


Figure 9. Comparison of maximum time derivative of current between Simulation and Measurement.

For this study, the two-step process requires a single 25 minute run for S-Parameters and then a few seconds for each circuit simulator run. Transient co-simulation takes 1 hour for each run, but since transient co-simulation is the only way to get transient Field data, then

this would be the method for completeness. Furthermore, numerical convergence of the discharge current is guaranteed with transient co-simulation whereas the two-step process requires convergence at step 1. for the S matrix.

**4.3. Simple Example with Realistic ESD Generator.** As mentioned in international ESD testing standard IEC 61000-4-2, ESD current has a wide frequency bandwidth and a high peak current level which can cause failures in the device. An ESD air-gap discharge testing scenario can be modeled with a realistic ESD generator and a DUT. Many references have already shown that this can be done with simulation even for today's ESD generators used in the industry in contact mode (Caniggia and Maradei, 2007), (Liu *et al.*, 2009), (Kim *et al.*, 2010). In particular the work in Liu *et al.* (2009) is relevant to the modeling and simulation of such generators. The only change that would need to be made from using the methodology in Liu *et al.* (2009) is that a port can then go in between the ESD gun tip and ground plane rather than a lumped element to facilitate the interfacing between full-wave and circuit that includes the Rompe-Weizel SPICE model. As shown in Figure 10, a complex ESD generator is modeled in full-wave and discharging to a ground plane. The current distribution in 3D is given in Figure 12 at three different times and highlights the novelty in this new methodology of a single transient co-simulation for system-level considerations. In Figure 11, the current waveform can be seen at the air-gap and can be correlated to Figure 12. Just as we expect from looking at Figure 11, there is negligible current that forms on the ground plane until 1.5 ns, and this is what we see from looking at the plots of Figure 12 in that order.

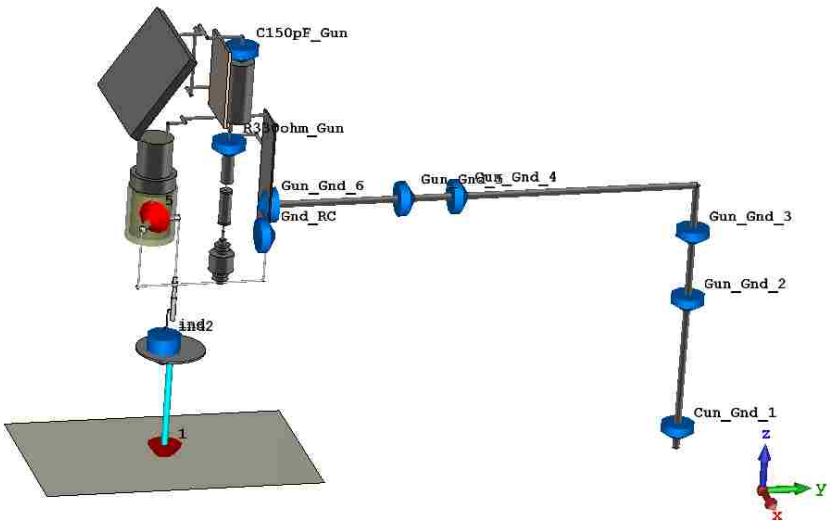


Figure 10. Example model of a ESD Generator discharging to a metal plane in non-contact/air gap mode (0.8 mm gap distance and 8 kV).

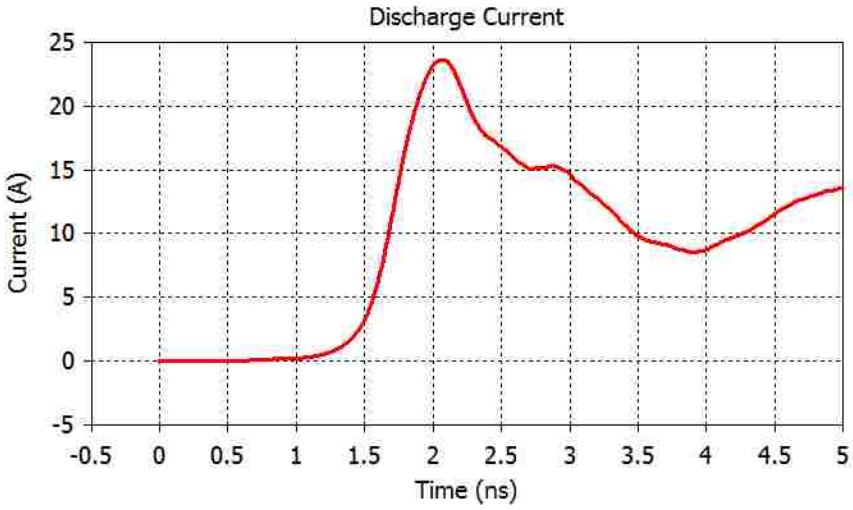


Figure 11. Current waveform from the arc across the air gap for the example in Figure 10.

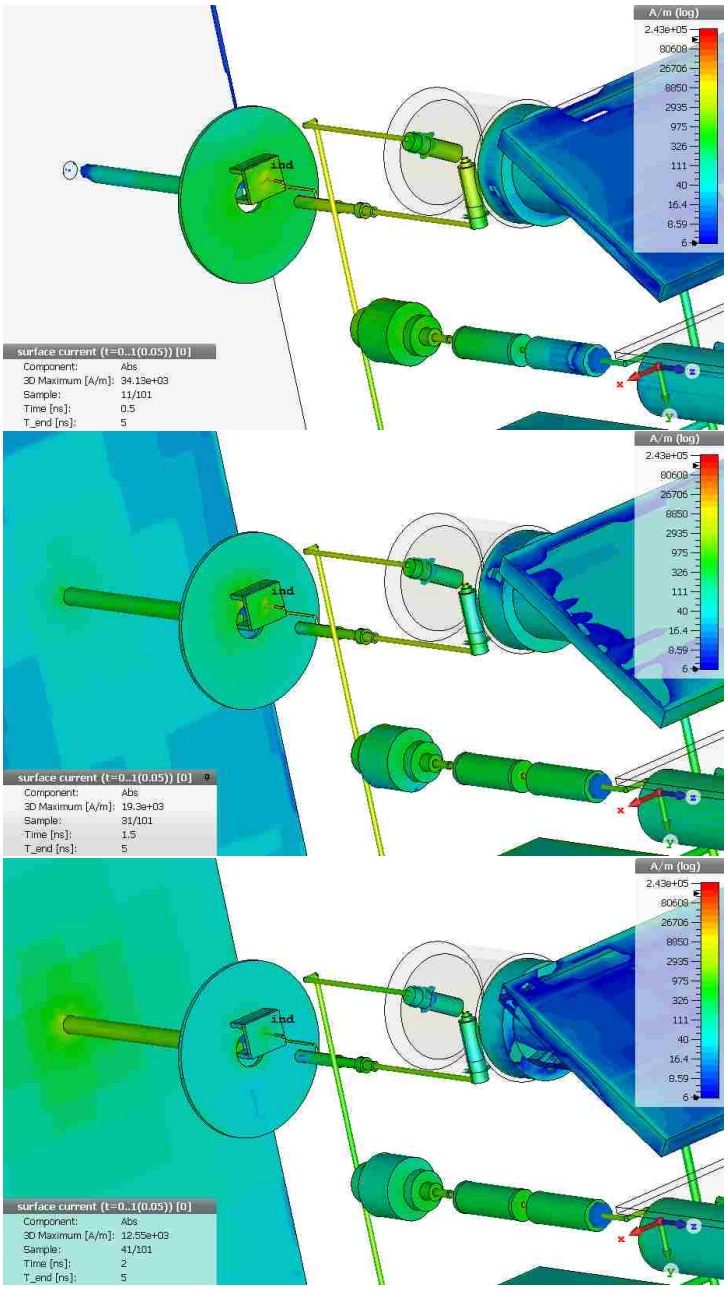


Figure 12. Surface current plots at 0.5 ns, 1.5 ns, and 2.0 ns for the example in Figure 10.

## 5. CONCLUSION

A measurement setup that is well known in literature (Pommerenke, 1995) is used and a full-wave simulation of this setup is accomplished. Analysis of different numerical methods leads to the conclusion that for this particular measurement setup, the TLM algorithm has the best performance, and the two-step process is used to gather the current waveforms and rise times. Transient co-simulation, which is a new method for air gap discharge with the Rompe-Weizel model, is presented and its ability of complete transient field data all in one simulation run is compared to the two-step process and the re-import method by Liu *et al.* (2011). Simulation results correlate very well to the measurement which shows the validity of the numerical methods used. Finally, results from a simple example with a realistic ESD generator discharging to a ground plane are shown.

## ACKNOWLEDGEMENTS

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# II. ON SECONDARY ESD EVENT MONITORING AND FULL-WAVE MODELING METHODOLOGY

D. Z. Li

Department of Electrical Engineering

Missouri University of Science and Technology

Rolla, Missouri 65409–0050

Tel: 415-375-0867

Email: dzldh8@mst.edu

## ABSTRACT

An adjustable spark gap structure is designed to generate Secondary ESD. The primary and the secondary discharge current are directly measured. The setup is modelled using CST full-wave simulation software. The goal is to predict secondary ESD induced current levels using simulation methods, to assist designers in product development in the early design stage.

## 1. INTRODUCTION

Secondary electrostatic discharge (ESD) events may cause damage inside electronic products (Wolf and Gieser, 2015). Typically, a product is evaluated for its system level ESD robustness using IEC 61000-4-2 testing. The secondary ESD event occurs when a floating metal discharges to a surrounding grounded metal inside a product. The discharge occurs across a spark gap between the floating and the grounded metal. The over-voltage across the spark gap leads to the breakdown of the spark gap and the initiation of the secondary ESD current. A statistical time lag is associated with the initiation of the secondary ESD current, which is investigated in the study by Wan *et al.* (2014). Methods to model the

secondary ESD have been investigated in Xiao *et al.* (2012). The modeling method requires a two-step process for determining the fields caused due to the occurrence of the secondary ESD current. It requires the re-import of the secondary ESD current into the full-wave simulation model. A decorative floating metal setup is designed to generate secondary discharges for known spark gap distances. This measurement setup is similar to the in-situ measurement setup in the work by Wolf and Gieser (2015) for monitoring the secondary ESD current measurements. The study performed by Wolf and Gieser (2015) makes use of the measured secondary ESD currents to improve the ESD robustness of the desired IC under test. However, the in-situ measurement setup does not monitor other waveforms such as the ESD gun discharge currents and the floating metal voltage. The decorative metal geometry is modelled using CST full-wave software. The secondary ESD event peak current, statistical time lag and the voltage on the decorative metal are compared with the simulation model. This study introduces the full-wave modelling method to predict the currents induced during a secondary ESD event. The simulated results are compared to the measured waveforms and the accuracy of the full-wave simulation method is discussed.

## 2. MEASUREMENT SETUP

Figure 1 shows the block diagram of the measurement setup for the decorative metal. This simplified setup is designed to generate repeatable secondary ESD events. A metal screw is mounted on the decorative metal plate. The distance between the screw tip and the current target (1.9 Ω) is called as the spark gap distance. Accurate spark gap distance of 0.8 mm is obtained using feeler gauges.

The current target measures the secondary ESD current, when the overvoltage-spark gap breaks down. The decorative metal plate is kept approximately at a distance of 5 mm from the shielded enclosure. The simplified measurement setup is improved from one of the measurement setups done by Marathe *et al.* (2017), and offers the capability to monitor the floating metal voltage. A 1000:1 high voltage Tektronix probe is used measure the high

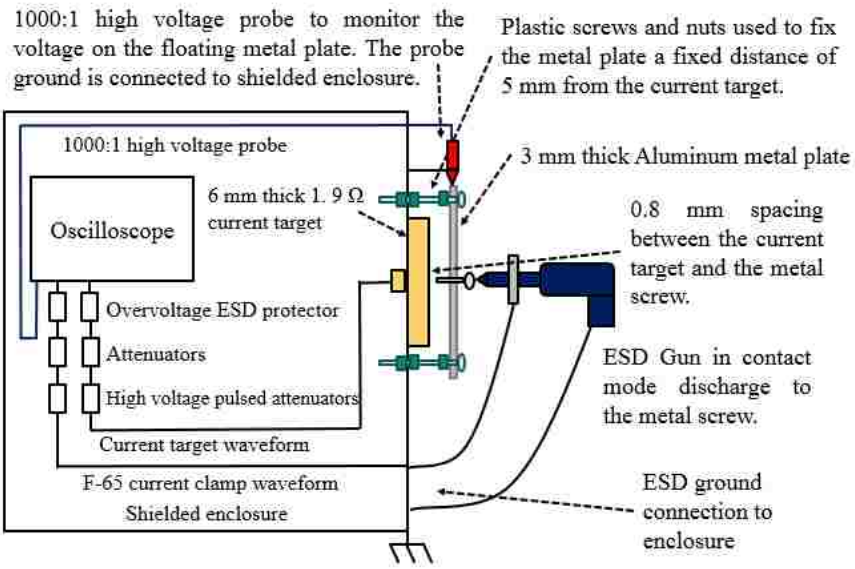



Figure 1. Decorative floating metal measurement setup.

voltage generated on the decorative floating metal. The ESD gun is discharged in contact mode at 6 kV voltage setting on the metal screw connected to the decorative metal. Clip-on ferrites are added to the measurement cables to reduce field coupling due to the ESD gun discharges. Sand paper is used to expose the metal surface of the shielded enclosure. The high voltage probe ground is well connected to the enclosure by gasket. Tie wraps are used to increase the mechanical contact of the probe ground to the shielded enclosure.

An F-65 current clamp is used to measure the primary discharge current at the tip of the ESD gun. The frequency bandwidth of the measurement setup enabled to resolve the secondary ESD current rise time down to 50 ps. To protect the oscilloscope from undesired ESD testing related damages, the high voltage pulsed attenuators (ESDEMC) and overvoltage ESD clamps are used in the measurement setup.

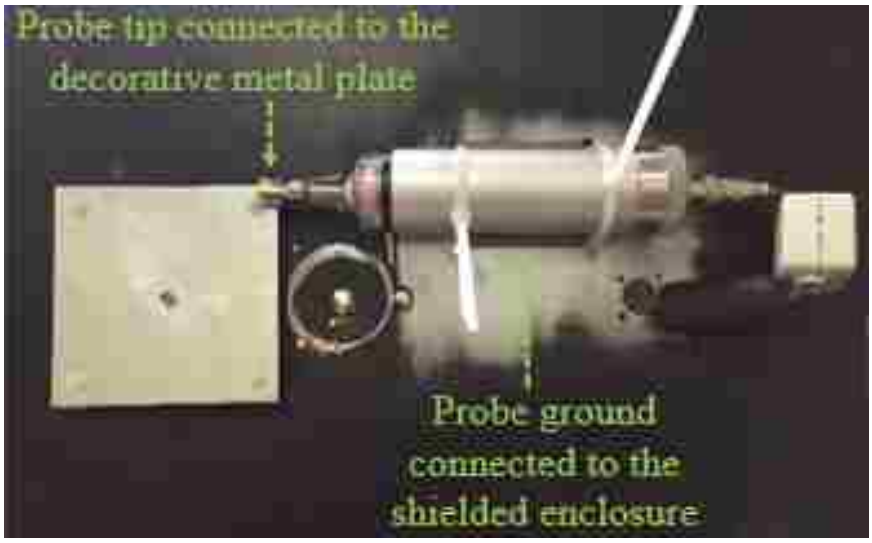



Figure 2. 1000:1 high voltage Tektronix probe is used for measuring the decorative floating metal voltage. Gasket is used at the tip of the high voltage probe and the decorative metal to ensure electrical contact between the two surfaces.

## 3. MEASURED WAVEFORMS

The measurement results are post-processed to correct for the attenuation introduced by the cables and the pulsed attenuators. Figure 3 shows the measured current clamp (primary discharge), the current target (secondary discharge), and the high voltage probe (floating metal voltage). The measured waveform parameters are summarized in the Table 1. The Paschen value for the static breakdown of the spark gap distance $d$ equal to 0.8 mm is calculated to be 3.91 kV using the formula (Pommerenke, 1995), where $d$ is in cm and $U$ is in kV units.

$$U = 25.4 \cdot d + 6.64\sqrt{d} \tag{1}$$

The voltage on the decorative floating metal rises when the primary discharge occurs on the floating metal. If the voltage is higher than the Paschen value, then the secondary ESD discharge will occur after a time delay. This time delay is called as the statistical time

lag. The statistical time lag is the parameter is calculated by the difference in time instant ($t_1$) at which the floating metal is equal to the Paschen value and the time instant ($t_2$) at which the floating metal voltage collapses, indicating the initiation of the secondary ESD event. The ringing measured near the falling edge of the floating metal voltage waveform is an artifact from the probing. The high voltage probe frequency bandwidth is up to 75 MHz and the frequency content present in the fast falling time of the voltage waveform is higher than that of the probe. Trade off was made by using a bandwidth limited probe in order to monitor the high voltage (1000:1 attenuation). It should be noted that the bandwidth limitation does not limit the capability of the probe to measure the statistical time lag parameter associated with the floating metal voltage measurement.

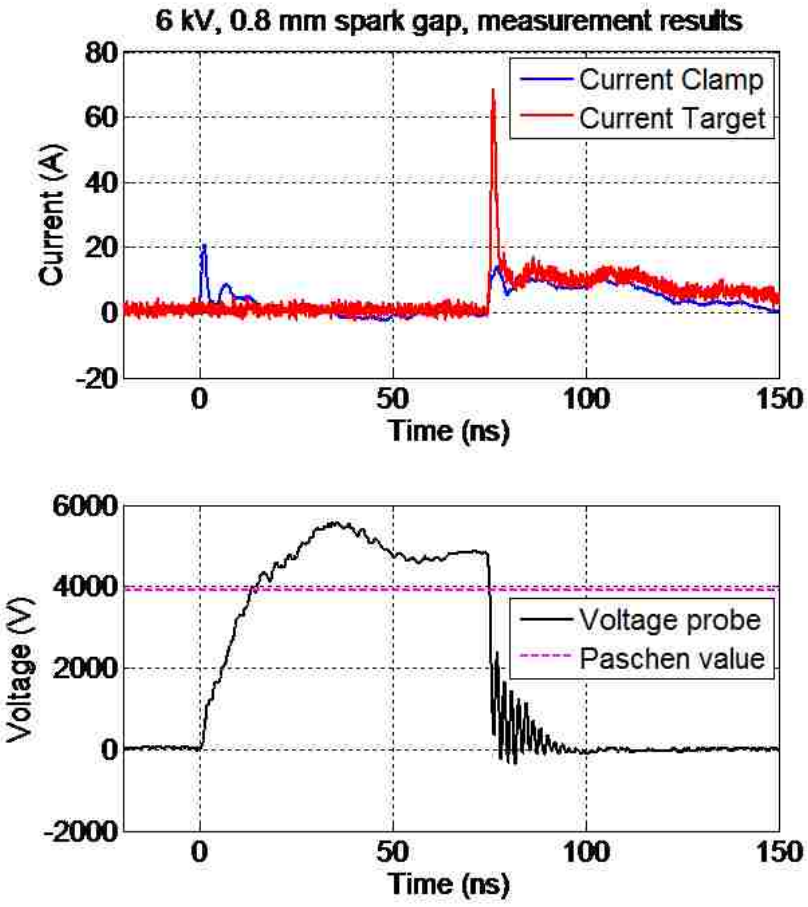



Figure 3. Primary discharge, secondary discharge and the measured floating metal voltage.

## 4. FULL-WAVE SIMULATION MODELING

The primary discharge current levels of the current target and the ESD gun are verified in simulation to make sure that the passive component parameters of the ESD gun match the one used in the measurement. The verification step involves the ESD Gun discharging directly to a target in contact mode and making sure that the peak discharge current and rise time match measurement. After the model is verified, the decorative floating metal plate is introduced in the model, as shown in Figure 4. The secondary ESD event will occur at the location shown by a red arrow numbered 3 in the Figure 4.

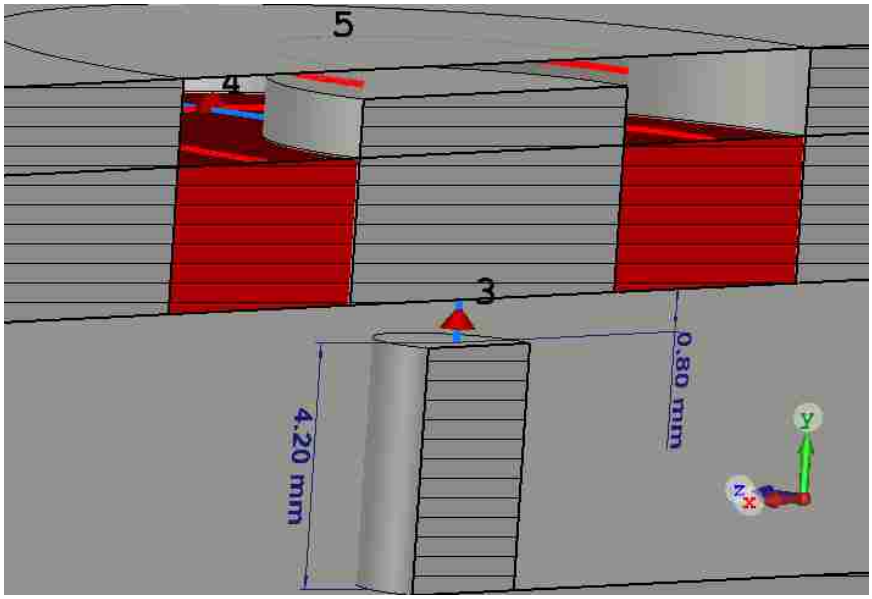
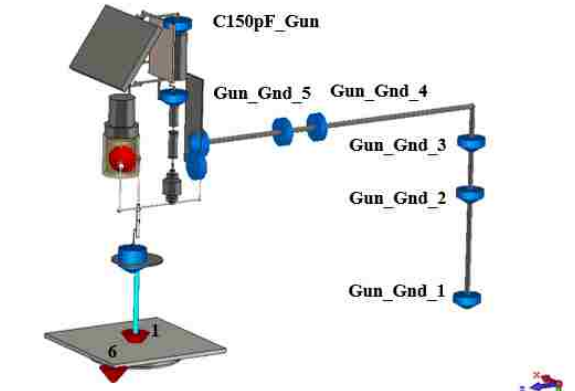



Figure 4. The metal screw to current target interface in the full-wave simulation model is shown. Secondary ESD event occurs across this spark gap interface. 3D Model's ports 3 through 5 are shown in this image.

Figure 5 shows the full-wave model snapshot. The red arrow numbered 1 represents the primary discharge monitor. The red arrow numbered 6 represents the floating metal voltage monitor. It measures the voltage between the decorative floating metal and the ground.

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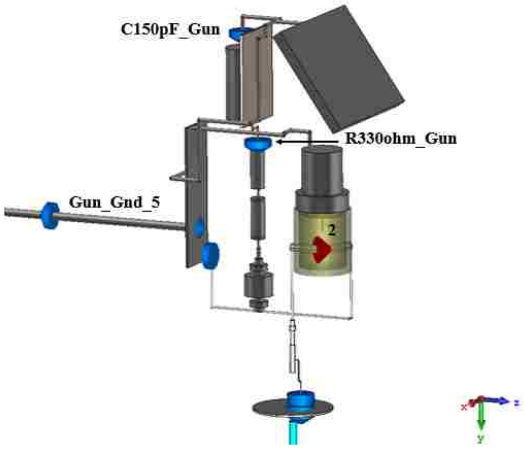


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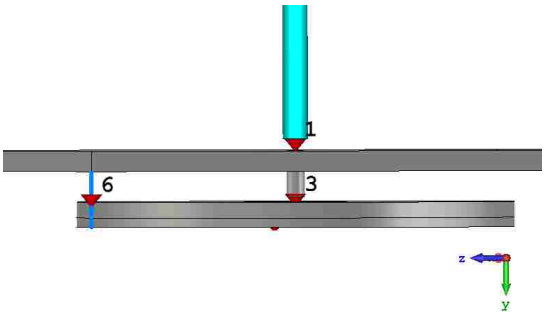


c)

Figure 5. (a) Overview of full-wave simulation model (b) Port 2 location in the full-wave model (c) ESD gun discharging to a plate with a current target underneath to measure the secondary ESD event in the simulation model. Ports 1, 3 and 6 location are shown in the full-wave model.

In the circuit model shown in Figure 6, the primary discharge is monitored at the yellow port number 3. The yellow port number 3 connects to the 3D block's pin 1 labeled as "Primary Discharge" in the same figure. This pin 1 represents the port 1 of the 3D model in Figure 5. The secondary discharge is monitored at P3 or P4 in the schematic shown below. The yellow color port 1 connects to the relay in the ESD gun, yellow color port 2 connects to the 50 ohm coaxial port impedance, yellow port 3 connects to the 0.1 ohm impedance, and yellow port 4 is connected to the current target parallel resistors. In the circuit modeler of CST (2017), a switch is used to control the on or off state of the Rompe-Weizel (RW) model (Pommerenke, 1995). This is shown in Figure 6. The switch is needed to model the statistical time lag. The RW model has an initial charge value which allows it to start current flow. The switch determines when the RW model will initiate the discharge current (Pommerenke and Aidam, 1995). Thus, the switch allows to model the statistical time lag. Here multiple approaches are possible. If time lag data is known for the geometry the switch delay can be set appropriately, if no time lag data is known one can use the gap voltage as guidance. In most cases the discharge will be initiated once the field strength has reached 50 kV/cm. In cases in which the surface is clean and smooth it may take 200 kV/cm to initiate the breakdown. Thus, by using the gap distance one can estimate the voltage at which the field strength is high enough to create enough initial electrons that will lead to a breakdown with less than a few nanosecond delay (Xiao *et al.*, 2012).

In this case the initiation of the secondary ESD event in the simulation model is adjusted to be close to the collapse voltage value of the decorative floating metal obtained by monitoring the floating metal voltage. The decision of closing the switch and initiating the secondary ESD event in the simulation model and, at the same time, start the collapsing of the voltage on the floating metal is made by selecting the peak floating voltage value from the measurement. It should be noted that the voltage value must be higher than the Paschen value of 3.91 kV obtained using the formula for a spark gap distance of 0.8 mm. The Paschen value represents the over-voltage required over the spark gap (0.8 mm) to cause

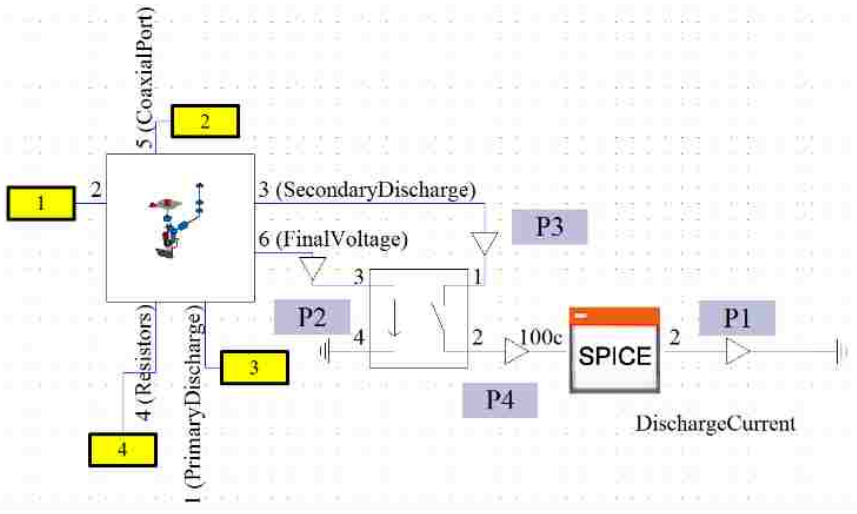


Figure 6. Switch-controlled RW model implementation in circuit modeler of the full-wave simulation software.

the initiation of the secondary ESD event. The criterion for closing the switch is based on measurement data. The accuracy of the resulting waveforms is discussed in the following section.

## 5. MEASUREMENT AND SIMULATION COMPARISON

The measurement waveforms are shown in Figure 3 and the simulated waveforms are shown in Figure 7. The measured statistical time lag can vary and it is affected by many parameters such as the humidity, shape of the spark gap geometry, high voltage across the spark, gap etc. The definition of statistical time lag is explained by Xiao *et al.* (2012), and is exemplified in Figure 8. There is a statistical time lag between the primary charging current and secondary discharge current. The statistical time lag is defined as the time difference when the Paschen voltage is reached and the point in time of formation of the arc. In Figure 8, this is marked by starting at the Paschen Voltage in the Voltage plot and ending when the secondary discharge current begins to rise (the Current plot and Voltage plot in Figure 8 are synchronous in time). The measured and simulated waveforms are plotted in different

figures because it is difficult to match the measured statistical time lag with the simulated value. Therefore overlaying the measured and the simulated waveforms will make it difficult to observe individual waveforms for the given figure axis scale settings.

Table 1 shows the comparison results for the various parameters between the measurement and the simulation.

Table 1. Comparison of measured and simulated parameters

| Parameters for 6 kV at 0.8 mm spark gap | Measurement | Simulation |
|---|---|---|
| Primary charging current peak | 21 A | 19A |
| Primary charging current rise time (20% - 80%) | 650 ps | 550 ps |
| Secondary ESD peak current | 69 A | 82 A |
| Secondary ESD current rise time (20% - 80%) | 61 ns | 5 ns |
| Statistical time lag between the primary charging current and Secondary ESD | 61 ns | 5 ns |
| Paschen breakdown voltage | 3.91 kV | 3.91 kV |
| Peak metal plate voltage | 5.6 kV | 4.7 kV |

The primary charging current is expected to be around 3.75 A/kV to be around 22.5 A for contact mode discharge into a large ground plane. The simulated primary discharge current is within 10% variation of the measured current in to the decorative metal plate.

In simulation, when the peak floating decorative metal voltage is at 4.7 kV, the peak secondary ESD current was found to be 82 A. This corresponds to around a 20% error when compared to the measurement. The peak decorative metal plate voltage is explicitly handled for simulation because by design of the switch, it will point exactly to when the secondary discharge occurs. However, this peak decorative metal plate voltage for measurement is affected by the stochastic process of air discharge and the measurement tools that cause the secondary breakdown to occur at a value lower than the peak floating decorative metal voltage. This is a very important concept because it gives credence to the RW model since it can correctly form the arc resistance with the appropriate voltage at the point of breakdown.

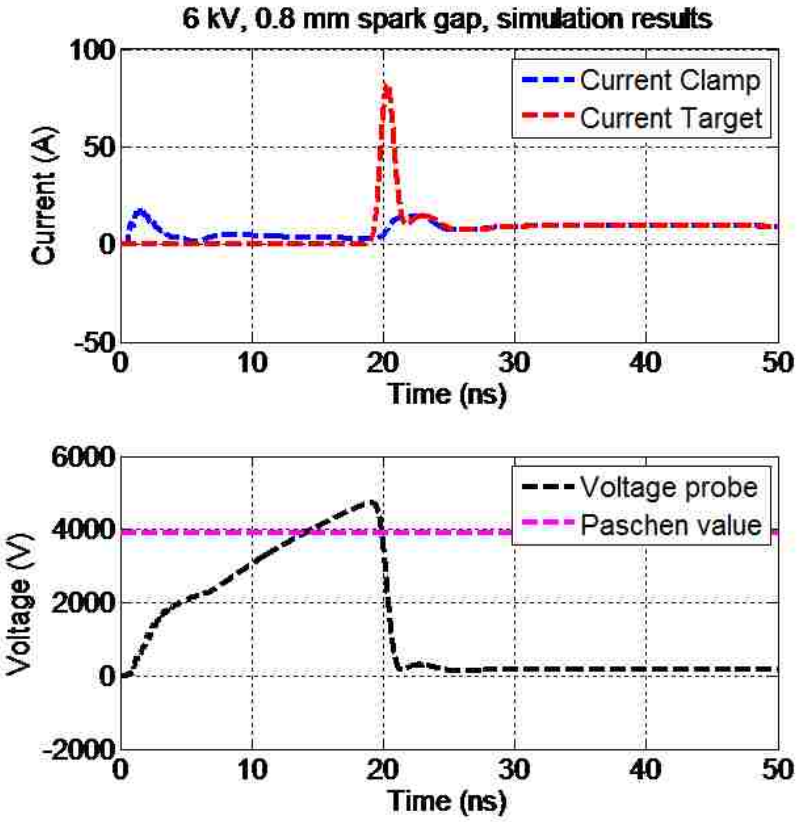


Figure 7. The simulated waveforms obtained from the full wave model.

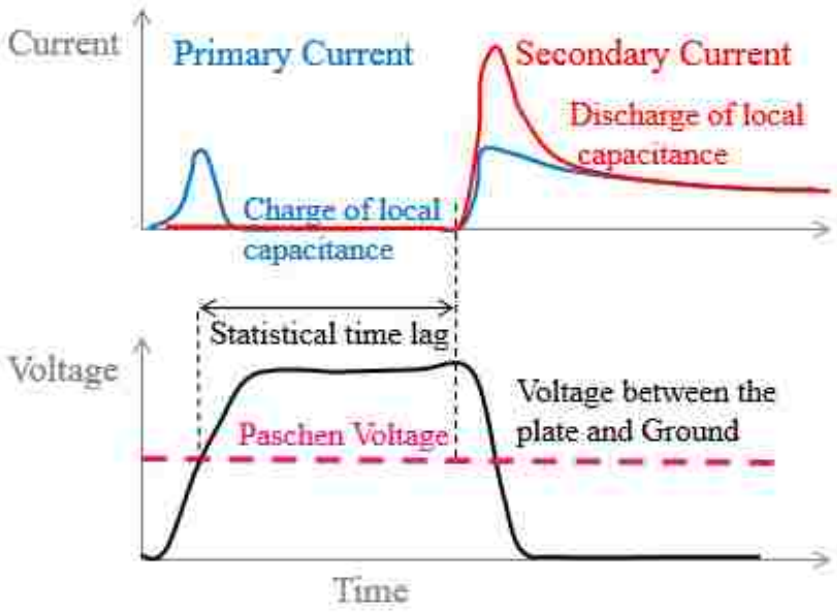


Figure 8. Abstraction of the Secondary Discharge process.

## 6. DISCUSSION AND CONCLUSION

In general, the rise time of the secondary ESD currents is faster than that of the primary charging ESD current from the ESD gun. In real products, measuring the secondary discharge at the source location would be difficult to access and would require the use of external measurement equipment such as the wire loop antenna, F-65 current clamp or monitoring the floating metal voltage in the real product using a high voltage probe to detect the occurrence of the secondary ESD event (Marathe *et al.*, 2017). In some cases, it may not be possible to access the source location of the secondary ESD event inside a real product, which will lead to bandwidth limitation of the rise time measurements performed using the external equipment. The rise time measurement is bandwidth limited due to the added inductance/capacitance in the measurement due to the equipment being away from the source location of the secondary ESD event.

The secondary discharge setup represents a product example having decorative metal placed for aesthetic purposes. The floating metal is modelled using the CST software. In this study, a controlled setup is used to measure the induced secondary ESD peak current, rise time and the statistical time lag. The current target is placed right at the source of the secondary ESD event. This measurement setup allows the user to measure the secondary discharge currents at the spark gap, which may not be always be possible in complex electronic products. The full-wave simulation methodology predicts the measured secondary ESD current within 20% accuracy.

This simulation methodology can be extended to real systems, but one needs to modify the decision control in the closing of the switch in the circuit modeler in order to initiate the secondary ESD event. To identify the worst case rise time, and the peak secondary ESD current, closing the switch at twice or three times the Paschen value. In measurements, this will be affected by the statistical process of the statistical time lag, and may be difficult to reproduce the statistical time lag, which may cause the breakdown of the spark gap geometry at twice or three times the Paschen value for a specific value of

the spark gap distance (0.8 mm in this case). If the statistical time lag is long, it may give the floating metal voltage the time required to reach twice or thrice the Paschen value. If in measurement the statistical time lag parameter is small, then the collapse of the floating metal voltage will occur before it reaches the twice or thrice the Paschen value. The rise in the floating metal voltage depends on the local capacitance between the floating metal and the ground. It should be noted that the collapse of the floating metal voltage is associated with the initiation of the secondary ESD event.

In real systems, it would be difficult to measure the rise time and the peak secondary ESD current, if the source location of the event is not accessible. This makes it difficult to assess the accuracy of the parameter values obtained from the simulation model. In such cases, the values obtained can be considered as a suggestive guideline for worst case rise time and peak secondary ESD discharge current.

In modeling the geometry of the ESD gun with the DUT, the combined mesh count is often based on the complex model between the DUT and the ESD gun. As long as both are meshed properly individually, then combining the two models with the mesh of the more complex model will also be accurate. Material properties should also be as accurate as possible, though more studies need to go into what type of simplifications we can make. Understanding the most likely spark gap geometries on a product and performing early design stage simulations will help to predict the worst case secondary ESD current stress on the electronic product.

## ACKNOWLEDGEMENTS

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# III. FULL-WAVE SIMULATION OF SYSTEM-LEVEL DISRUPTION DURING SECONDARY ESD EVENTS IN A SMARTPHONE

D. Z. Li

Department of Electrical Engineering

Missouri University of Science and Technology

Rolla, Missouri 65409–0050

Tel: 415-375-0867

Email: dzldh8@mst.edu

## ABSTRACT

To demonstrate the electromagnetic full-wave simulation of secondary ESD, an ESD generator is modeled in 3D and in contact mode discharging to a non-grounded, metallic earmesh of a smartphone. The nonlinear Rompe-Weizel SPICE model computes the arc resistance of the secondary discharge between ungrounded metal and a grounded enclosure. The SPICE model is solved using a circuit simulator, and the 3D model is solved using the transmission-line matrix time domain numerical method. Transient co-simulation is a new technique that is used to solve both circuit and 3D models at the same time. The simulation predicts the coupling from ESD to a victim trace in the smartphone. Measurements performed at several stages validate the simulation results. Using this novel methodology, the user can simulate secondary discharge in products to predict ESD damage and disruption on a system level.

**Keywords:** Acoustic transducers, Air gaps, Arc discharges, Breakdown voltage, Cellular phones, Circuit simulation, Consumer electronics, Current measurement, Electric breakdown, Electromagnetic analysis, Electromagnetic coupling, Electromagnetic modeling,

Electromagnetics, Electrostatic discharges, Immunity testing, Integrated circuits, Low-pass filters, Nonlinear circuits, Numerical simulation, RF signals, Spark gaps, Time-domain analysis, Voltage measurement

## 1. INTRODUCTION

Disruption and damage from electrostatic discharge (ESD) can be observed even if the discharge does not directly go into a sensitive trace. An ESD may also cause a secondary ESD event within a product. An example of a secondary ESD is sparking between decorative metal and the grounded housing of a system. Being a function of the capacitance between the decorative metal and the grounded enclosure, the secondary spark currents can reach as high as 600 Amperes – five times higher than that of the primary ESD (Xiao *et al.*, 2012), (Wolf and Gieser, 2015), (Kim *et al.*, 2010); the rise time of this current can be as low as only a few hundred picoseconds. Two factors contribute to the higher currents and faster rise times. The charged capacitance between the ungrounded metal and the grounded structures forms a low impedance source for the secondary spark. Secondly, the spark gap is usually a highly overvoltage effect; i.e., the fast charging of the gap by the primary ESD allows the voltage across the secondary gap to reach voltages higher than the static breakdown voltage. So, once the breakdown is initiated, the voltage collapse time will be much shorter than the voltage collapse time of the static breakdown case. Both effects lead to high peak currents associated with sub-nanosecond rise times. The voltage collapse's associated currents can couple capacitively and inductively into the circuitry, causing a noise disturbance or even damage (Wolf and Gieser, 2015). An illustration of the capacitive coupling scenario is given in Fig. 1.

Techniques for measuring secondary ESD noise on voltage suppressor devices under different operating conditions are described by Kim *et al.* (2010). There is a need for a simulation methodology to predict the disruption levels for design consideration. Previous works by Xiao *et al.* (2012) explain the simulation of secondary discharge, but do not

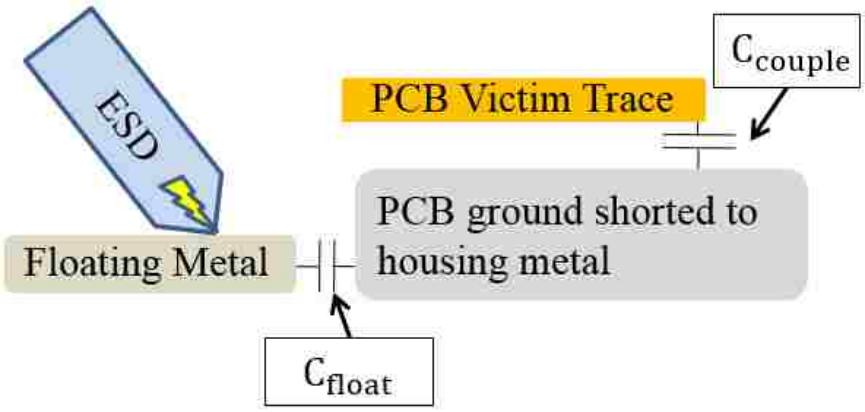



Figure 1. Illustration of system-level secondary discharge disruption on a victim trace due to capacitive coupling. $C_{float}$: Capacitance that gets charged between floating metal and metal housing before the breakdown occurs. $C_{couple}$ : Capacitance between PCB trace and PCB ground that causes capacitive coupling.

emphasize the investigation of system-level coupling inside a product. The work presented here uses transient co-simulation to bypass the need for a frequency domain representation and to make the visualization of transient fields and transient surface currents possible.

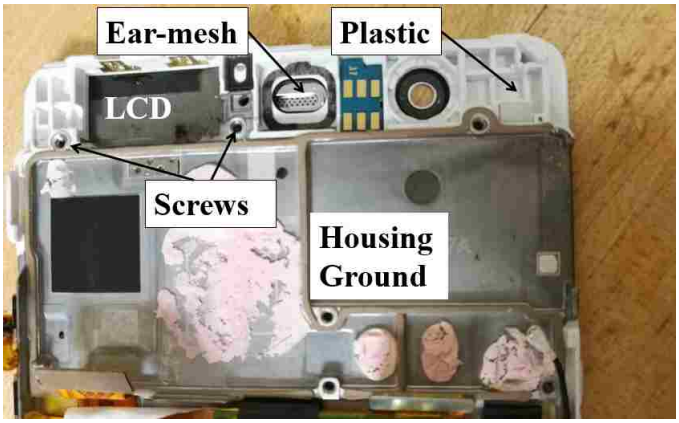
## 2. MODELING OF THE DEVICE UNDER TEST

The device under test (DUT) is a smartphone with some details that can be simplified during modeling. The passive model must first be verified before introducing the nonlinear spark. Such validation can be performed by comparing solutions from different solvers or comparing against measurements; we elected to compare against measured S-parameters.

**2.1. Desciption of the Passive Model.** For the verification of the DUT's model, the ESD generator was not modeled, but it was understood that the generator would be in contact mode to the earmesh (Fig. 2 (a) and Fig. 3) during the secondary discharge simulation. S-parameters represent the coupling of a system, so the S-parameters between

measurement and simulation are compared to validate the passive model. Port 1 is at the termination of the victim trace (Fig. 4), while Port 2 is between the floating earmesh and the housing ground (Fig. 3).

(a)

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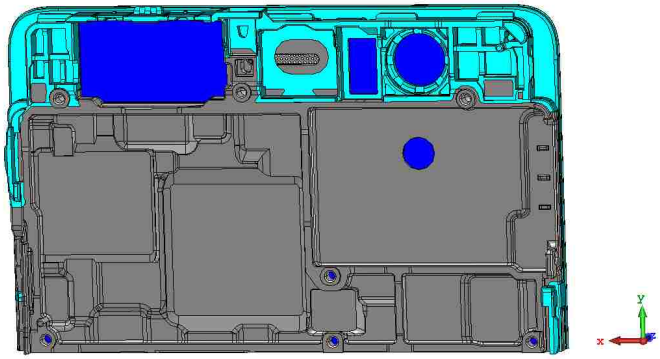


Figure 2. (a) Overview of full-wave simulation model (b) Port 2 location in the full-wave model (c) ESD gun discharging to a plate with a current target underneath to measure the secondary ESD event in the simulation model. Ports 1, 3 and 6 location are shown in the full-wave model.

The charging or discharging of the floating earmesh is effectively the input at Port 2, and the output of interest is the signal at Port 1, so the S-parameter of interest is S21. The phone was kept in the off state during the measurements, and the battery is disconnected from the PCB. The PCB can be removed from the housing, but under testing conditions, the PCB is grounded to the housing via seven screws (Fig. 4).

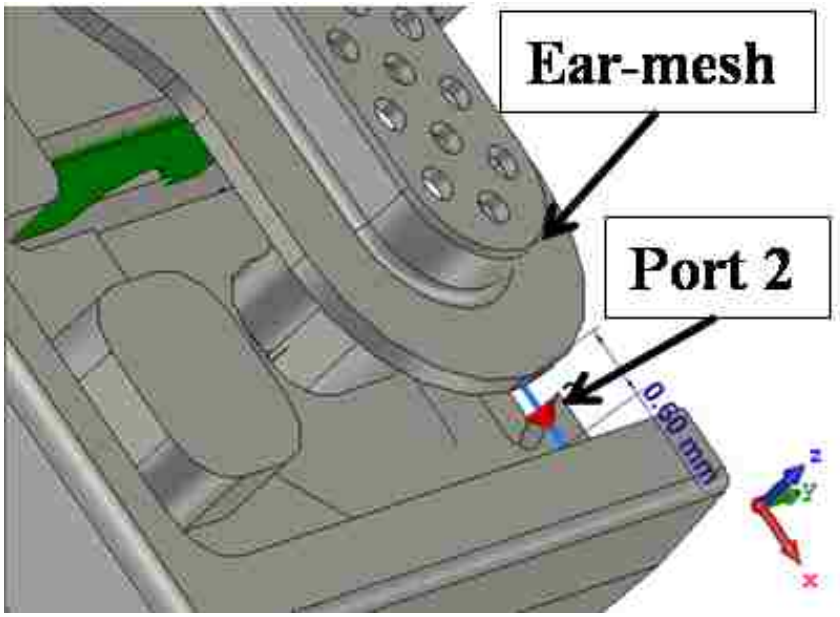
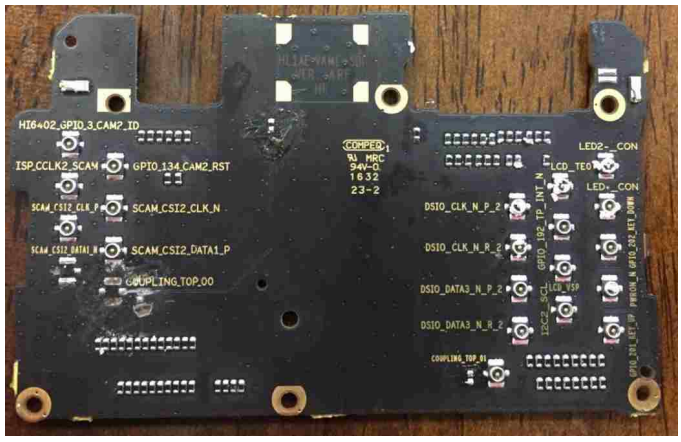


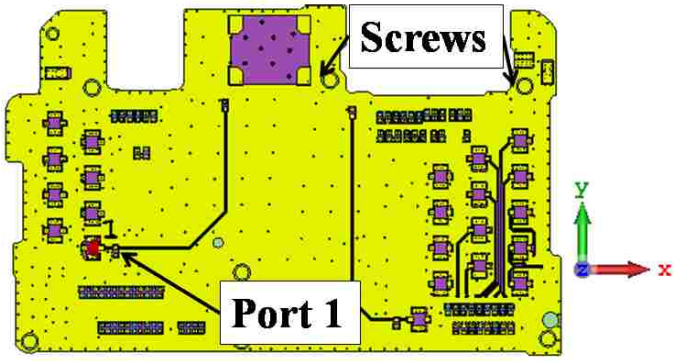

Figure 3. View of simulation model showing the 0.6 mm gap between the floating earmesh and housing ground with and S-parameter Port 2 labeled. The LCD is hidden in this view.

**2.2. 3D Model of the DUT.** CST Microwave Studio (CST, 2017) was used as the modeling tool. The full CAD geometry of the phone and PCB contained details that are not relevant to the simulation so we restricted the model to only the top half of the phone containing the PCB. The white plastic (turquoise in simulation) was modeled as a lossy dielectric. Both the simulation model and the real model are shown in Fig. 2.

The LCD screen (deep blue) was also modeled as a lossy dielectric. With the LCD hidden in Fig. 3, the floating earmesh can be seen, and Port 2 is placed at the location of the smallest gap between the earmesh and the metal housing ground. This gap distance is 0.6 mm as shown in Fig. 3. Port 2 is necessary for S-parameter model verification as well as interfacing between the full wave simulator and the SPICE circuit simulator.




(a)




(b)

Figure 4. Main PCB with the victim trace is shown in (a) the real model and (b) the simulation model.

The PCB was simplified to include only the top layer containing the victim trace, the next ground plane, the substrate in between, the vias, and the solder mask. Shown in Fig. 4 are the PCB imported into CST and the real PCB. There are seven screws that connect the housing ground to the PCB ground layers. In CST, they are modeled as cylinders. The trace terminations and the port impedances are all set to 50 Ω.

**2.3. Verification of 3D Model with Measurement.** To verify the 3D structure, an S-parameter measurement is done with the physical smartphone as described in section 2.1.

Important passives to account for are the metallic structures that can form a capacitive path between the two ports of interest. One such structure is the audio transducer that sits right below the earmesh. The transducer is shown in Fig. 5. The effect of the transducer is

first tested by performing the same S-parameter comparison with and without the transducer. In Fig. 6, the comparison is shown and it can be concluded that the transducer effect is small enough to not require modeling.

Figure 5. Audio transducer that sits below the earpiecemesh.

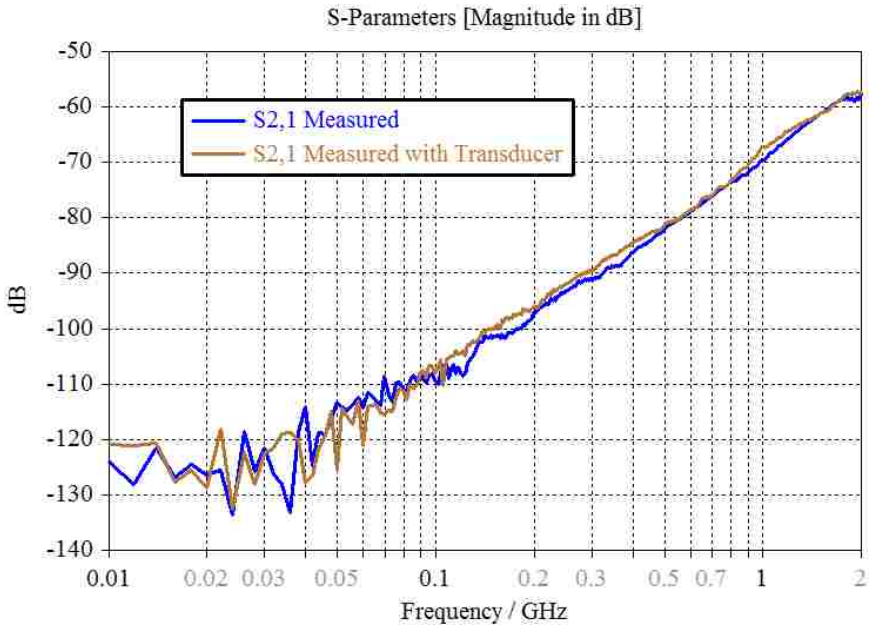



Figure 6. S-parameter comparison with and without the transducer. Port 2 (Fig. 3) is between earpiece-mesh and metal housing and Port 1 (Fig. 4 (b)) is between the far end of the victim trace and top layer ground.

The 3D model was solved using the transmission-line matrix (TLM) algorithm, which also supports the transient co-simulation that will be used for the secondary discharge simulation. As shown in Fig. 7, there is good agreement in slope and magnitude when comparing the S-parameters between measurement and simulation. The S21 plot shows a 40 dB/dec slope, but a coupling path that is either purely capacitive or purely inductive

would result in a 20 dB/dec slope. Since the slope of the S-parameter results in Fig. 7 is 40 dB/dec, the coupling is second order and must include capacitive and inductive coupling. Due to the complexity of the structure, it is not possible to identify the exact structural elements for the inductive coupling path.

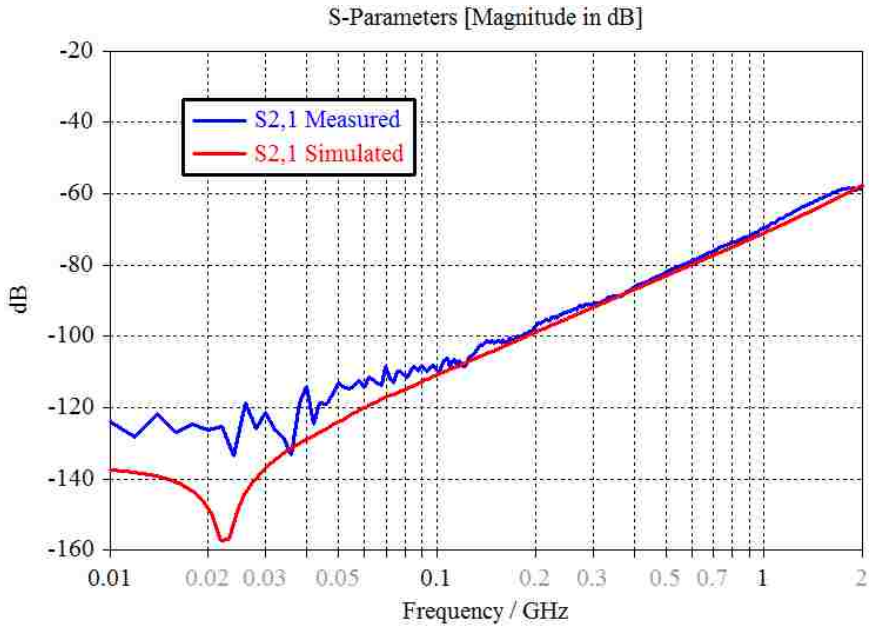



Figure 7. S-parameter comparison between measurement and simulation of the 3D smartphone model. Port 2 (Fig. 3) is between earpiece-mesh and housing metal and Port 1 (Fig. 4 (b)) is between the far end of the victim trace and top layer ground.

The simulation was ran with two Tesla K80 GPU cards. The CPU is a 3.4 GHz Intel Xeon E5 v3 processor with 512 GB of DDR4 RAM. The model failed to mesh with the finite element method (FEM) solver. Since the model had 2,831,782,591 mesh cells, the finite integration technique (FIT) method could not be used with this hardware. However, the TLM solver was able to lump the mesh cells and reduce the complexity to 6,886,873 mesh cells. The simulation took 38 hours in total for the converged S-parameters.

# 3. SECONDARY DISCHARGE SET-UP

**3.1. Physics of the Secondary Discharge Event.** For the secondary discharge to occur, floating metal must first be charged relative to grounded metal (Chiper *et al.*, 2008), (Mesyats *et al.*, 1969), (Meek and Craggs, 1978), (Lin and Welsher, 1993). The test standard requires contact mode discharge to the floating metal for the model investigated here because the earmesh is an exposed conductive surface (IEC 61000-4-2).

Paschen's law governs the breakdown voltage across an air gap (Meek and Craggs, 1978), (Pommerenke, 1995), (Pommerenke and Aidam, 1996), (Pedersen *et al.*, 1984). For homogenous fields, Paschen's voltage is equal to the static breakdown voltage (Pommerenke, 1995), and breakdown voltage is given by (1) (Meek and Craggs, 1978):

$$U = 25.4 \cdot d + 6.64\sqrt{d} \tag{1}$$

where $d$ is the gap distance in cm and $U$ is the voltage across the gap in kV.

The voltage in (1) is a necessary but insufficient condition for the breakdown to occur. The movement of the first electron across the gap to begin the breakdown is a stochastic process (Fowler and Nordheim, 1928). The time between when the static breakdown voltage is reached and when the first electron moves through the air gap is called the statistical time lag (Wan *et al.*, 2014), (Levinson and Kunhardt, 1982), shown as $t_s$ in Fig. 8. After the first electron moves through the gap, the arc begins to form. From there on we modeled the arc as a time-varying resistance (Pommerenke, 1995). Eventually the resistance will collapse, and the time from the formation of the arc to the collapse of its resistance is called the formative time lag (Wan *et al.*, 2014), (Levinson and Kunhardt, 1982), shown as $t_f$ in Fig. 8. The model used here for this time-varying resistor representation of the arc is called the Rompe-Weizel model (Pommerenke, 1995). Its resistance is described in (2).

$$R(t) = \frac{d}{\sqrt{2 \cdot a \cdot \int_0^t i(x)^2}} \tag{2}$$

where $R$ is the arc resistance in Ohms, $d$ is the gap distance of the electrode or arc length in meters and will be swept for different values in simulation. $a$ is an empirical constant with value of $1.5e-4\frac{m^2}{(V^2 \cdot s)}$ and $i$ is the discharge current in amperes.

Fig. 8 illustrates the timing of the secondary discharge process. The overvoltage effect (Wan *et al.*, 2014), (Levinson and Kunhardt, 1982) can be seen after $t_0$ and occurs when the primary ESD excitation uses a voltage much higher than the static breakdown voltage of the secondary gap. During the time period $(t_0 + t_s)$, the local capacitance of the gap between the metal and the ground is charged. After $(t_0 + t_s)$, the charge stored by the local capacitance begins to discharge due to the formation of the arc.

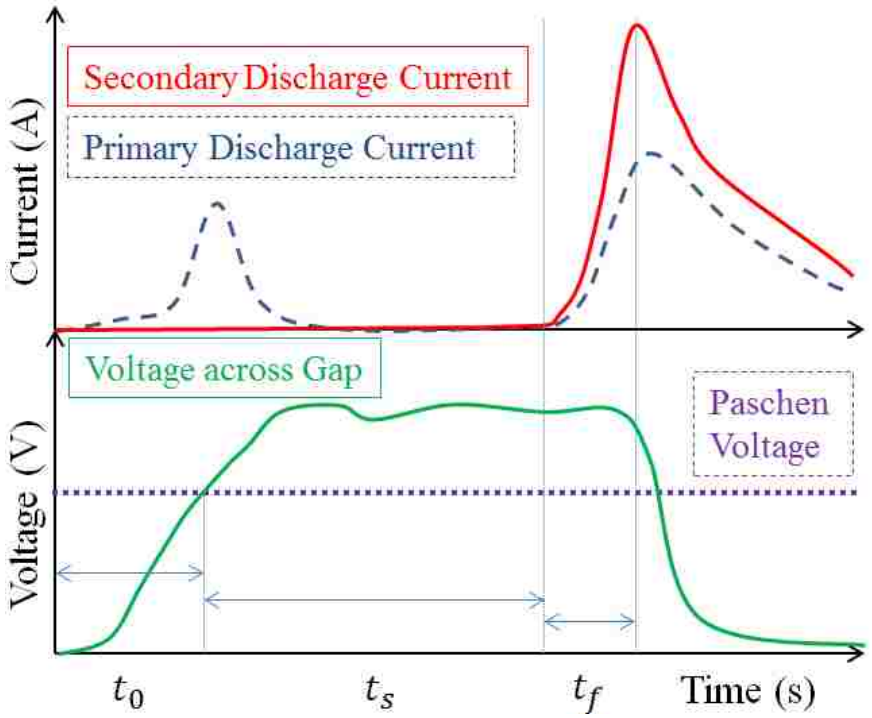



Figure 8. Illustration of the secondary discharge breakdown process including the voltage across the secondary air gap, an illustration of the secondary discharge current across the air gap, and the primary discharge current charging up the floating metal. Labeled times are $t_0$: time to reach Paschen's voltage; $t_s$: statistical time lag; $t_f$: formative time lag.

**3.2. Measurement Technique.** The measurement technique presented in Marathe *et al.* (2017b) was used to perform the detection and monitoring of the secondary ESD. The ESD gun was discharged in contact mode at the earmesh. An F-65 current clamp was used to monitor the primary charging event as well as the secondary ESD. In this geometry, the secondary ESD coupling to victim traces on the main PCB was of interest. A semi-rigid coax was used for probing the voltage on the critical trace; the semi-rigid coax ground was well connected to the main PCB ground and ferrites were added to prevent any noise coupling. The secondary ESD event may occur after a primary charging event by a variable time delay, ranging from nanoseconds to milliseconds. To acquire the desired waveforms, an oscilloscope enabled with a fast-retrigger acquisition mode was used which enabled the capture of multiple ESD events separated by time gaps (Marathe *et al.*, 2017b).

Discharge monitoring locations using an F-65 current clamp included the tip of the ESD gun, the ground connection of the DUT, and the ground cable of the ESD gun. The advantage of positioning the F-65 current clamp at the tip of the ESD gun was that position allowed for the capture of high frequency components of the primary discharge current. By contrast, positioning the F-65 current clamp at the ESD gun ground strap offered the advantage of being convenient in handling, but had the disadvantage of not being able to detect the initial peak current correctly, as shown in Fig. 9.

One limitation of the measurement set-up was that the voltage of the floating earmesh could not be measured because the voltage probe tip was too large relative to the small earmesh; the voltage probe itself would introduce another capacitance and would affect the measurement results.

**3.3. Simulation Set-up.** Transient co-simulation in CST Microwave Studio requires a connection between the ports in the 3D model and the circuit elements in CST Design Studio (CST, 2017). During each time step, voltage and current information is exchanged between the circuit simulator and the full-wave electromagnetic simulator. The TLM algorithm was chosen for the full-wave portion of transient co-simulation since it is

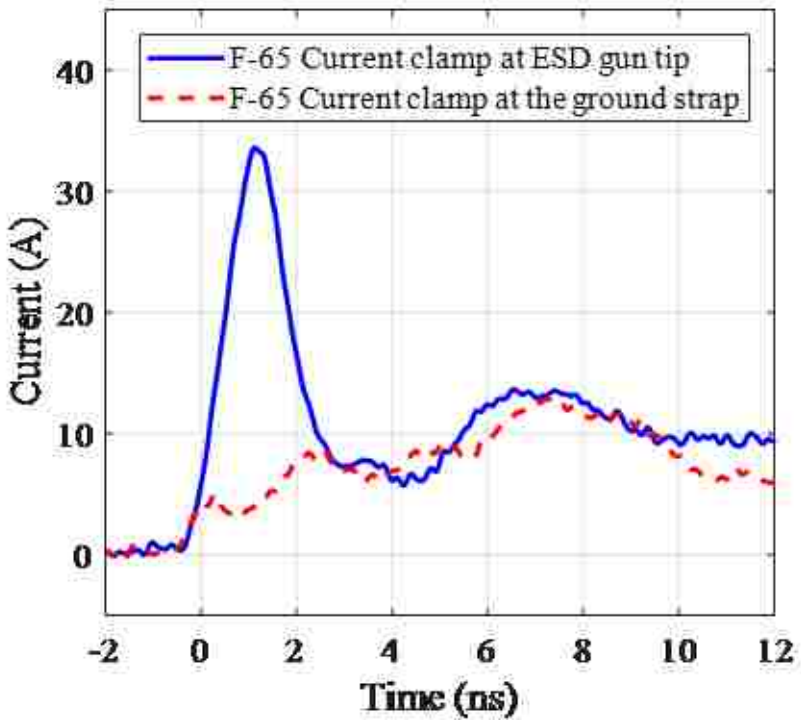



Figure 9. Comparison of the F-65 current clamp monitor location at the ESD gun tip (blue) and the ESD gun ground strap (red).

the most efficient method for air-gap discharge in a large computational domain (Li *et al.*, 2017). To prepare the 3D model of the DUT for secondary discharge simulation, we first imported the ESD generator geometry. The same ESD generator model was used as in Marathe *et al.* (2017a) and Li *et al.* (2017). The full system is shown in Fig. 10 (a), and Port 5 represents the ESD generator relay. As shown in the zoomed view of Fig. 10 (b), two more ports, Port 3 and Port 4, were added to the system. Port 3 represents the voltage between the floating earmesh and housing ground while Port 4 represents the contact between the ESD generator tip and the floating earmesh. Ports 1 and 2 remained the same as in Fig. 4 (b) and 3, respectively.

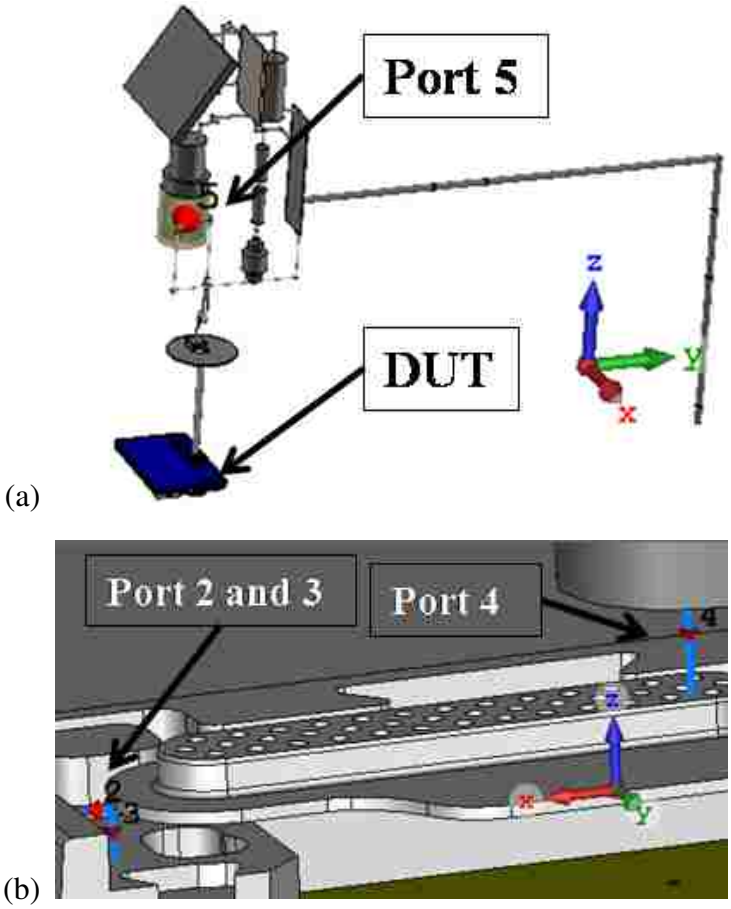



Figure 10. Secondary discharge 3D set-up showing (a) the full 3D model with Port 5 and DUT labeled and (b) a zoomed in view of the DUT with the dielectrics hidden and Ports 2, 3, and 4 labeled.

Fig. 11 shows the connections to the circuit from the 3D ports. The yellow port 1 in Fig. 11 is used for the 15 kV voltage excitation by the ESD generator. The yellow ports 2, 3, 4, and 5 are termination resistors that have the same values as their respective 3D Ports. For example, yellow port 3 is connected to a pin labeled "1 (J2305)" and the "1" represents the 3D port number. The secondary discharge current will occur across the 3D port 2 in Fig. 10 (b). The SPICE block for the Rompe-Weizel arc resistance model is described by (2) and the code is given by Pommerenke and Aidam (1996). The distance *d* in (2) is set to 0.6 mm as given in the real structure and shown in Figure 3. The static breakdown voltage is

estimated using Paschen's law at 3150 V. The Rompe-Weizel model alone is not sufficient to create the secondary breakdown process because the secondary breakdown across the gap should only occur after the static breakdown voltage is reached. The Rompe-Weizel model alone would incorrectly begin the breakdown at the very start of the simulation. As such, the voltage-controlled switch in Fig. 11 solves this problem by controlling the start of the Rompe-Weizel arc model. The response of the DUT to the secondary discharge depends on the secondary discharge current and rise time. The secondary discharge current depends on the over-voltage across the gap (Levinson and Kunhardt, 1982); hence, the voltage-controlled switch is best controlled by the voltage across the gap, which is equivalent to the voltage on Port 3 in Fig. 10 (b). For this experiment we ran a simulation sweep, controlling for the voltage condition of the voltage-controlled switch in Fig. 11 and setting it to be 3150 V, 6300 V, and 9450 V, which is Paschen's voltage, twice Paschen's voltage, and three times Paschen's voltage, respectively. This provided a range of simulated results which can be compared to measurements, and will be the proposed workflow for simulations of system-level damage due to secondary ESD.

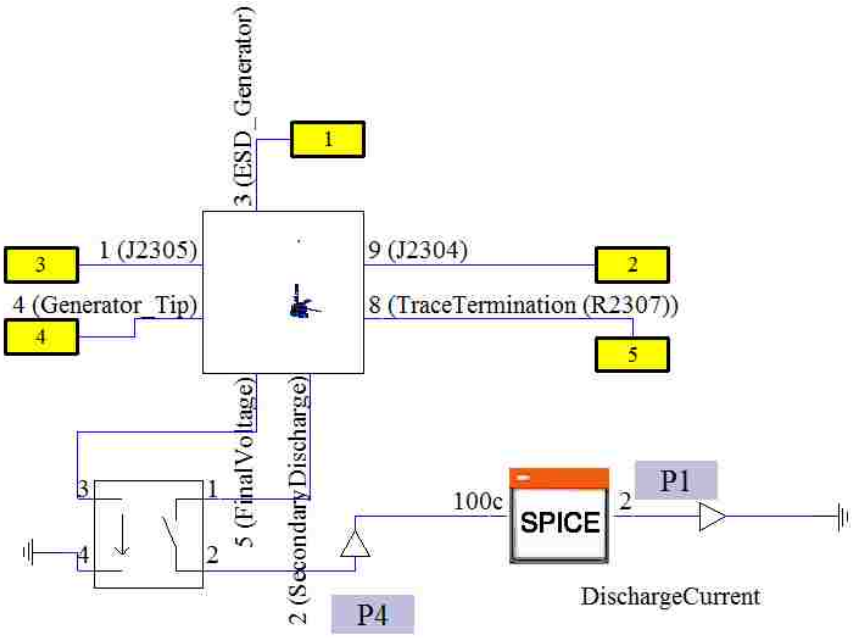



Figure 11. Secondary discharge schematic showing the connections from the 3D simulation to the circuit elements.

# 4. RESULTS AND ANALYSIS

**4.1. Simulation Prediction and Measurement Comparison.** Simulation and measurement results are compared for the cases where the ESD generator is set to 15 kV. Multiple simulations were done with the voltage condition on the voltage switch in Fig. 11 set to be 3150 V, 6300 V, and 9450 V. When comparing the current waveforms in Fig. 12, the peak current value at the ESD generator tip is closest to the simulation result for the voltage switch condition set at 3150 V. From Fig. 12, the formative time lag from the measured current waveform was around 0.7 ns, which is the same as the formative time lag from the simulated current waveform for the 3150 V condition. If a voltage measurement could be performed on the floating earmesh relative to the housing ground, then the voltage at which the secondary breakdown occurs could be found. Without this measurement, the best hypothesis is that the secondary breakdown voltage of the measurement is closer to 3150 V than it is to 6300 V.

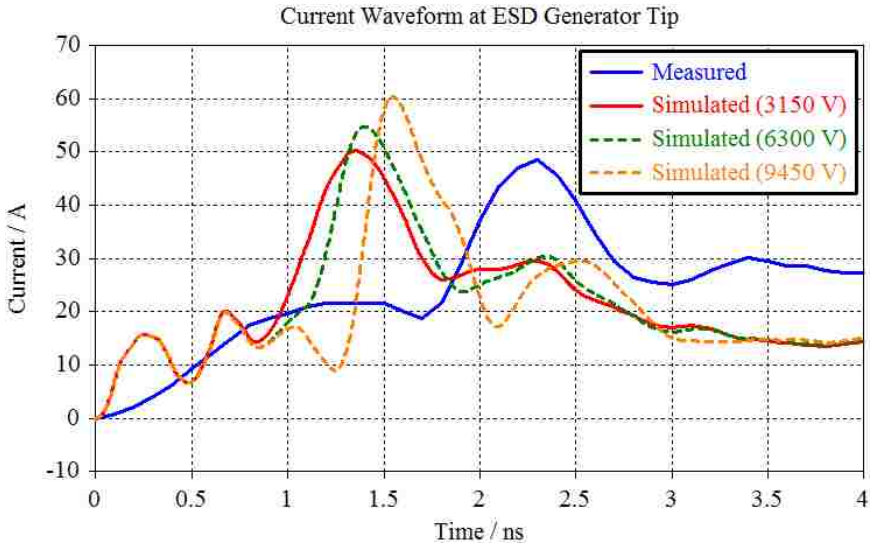



Figure 12. Compared is the discharge current waveform at the ESD generator tip in simulation and in measurement.

In Fig. 13, the voltage waveform on the floating metal during simulation is shown. The arc did not form until the voltage condition was reached. With regards to the formative time lag of the arc, explanation and measurements are given by Fletcher (1949). Fletcher found that the formative time lag does not vary with gap width or the applied voltage – it only varies with the electric field across the gap. Looking at Fig. 13, the simulated result for a voltage condition of 3150 V has around 6000 V across the gap, which corresponds to $\frac{6000\text{ V}}{0.6\text{ mm}} = 100\frac{\text{kV}}{\text{cm}}$ in the gap. Looking up this value for the value of electric field in the gap from the chart by Fletcher (1949) yields 0.8 ns for the formative time lag, which is close to the measured and simulated results for the 3150 V condition.

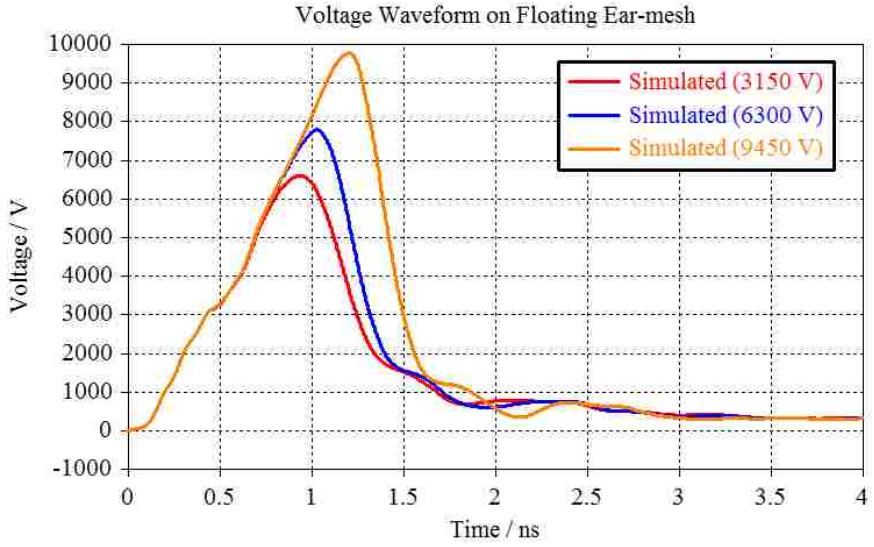



Figure 13. Simulated voltage waveform on the floating earmesh relative to grounded housing.

It is important to understand that in the SPICE representation of (2), there is a setting on the initial condition of the integration value that controls the formation of the arc. The Rompe-Weizel SPICE code in Pommerenke and Aidam (1996) computes the magnitude of the arc resistance with (3).

$$R(t) = \frac{d}{\sqrt{2 \cdot a \cdot V_C(t)}} \tag{3}$$

Comparing (2) and (3), $\int_0^t i(x)^2$ is numerically equivalent to $V_c(t)$, which is the voltage across a capacitor. The SPICE standard has a variable that the user can set for the initial voltage condition of the capacitor, or $V_C(t = 0)$. If the initial condition is set to be $V_C(t = 0) = 0$ V, then $R(t = 0)$ approaches infinity, no current would flow in any subsequent time steps, and an arc would never occur. Therefore, the initial voltage condition must not be zero, and it will determine the simulation's formative time lag, $t_f$, adding another degree of uncertainty to the simulation. The simulation results are shown in Table 1 and the measurement results are shown in Table 2. For the transient co-simulation, the time sampling rate is 60 GHz. It is known that the oscilloscope for measuring the induced voltage waveform on the victim trace has a bandwidth limitation of 2 GHz. For this reason, we applied a filter to the simulation as a post-processing step to analyze the effect of the frequency limitation of the oscilloscope. Fig. 14 shows the comparison of the simulated voltage waveform filtered to 2 GHz with measurement.

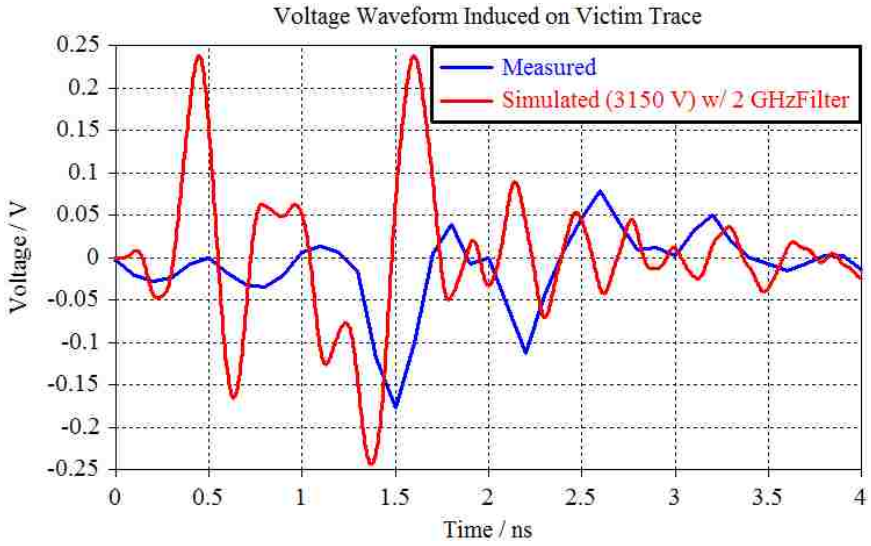



Figure 14. Voltage waveform induced on the victim trace of interest compared between measurement and simulation. The results are obtained using a secondary gap breakdown voltage of 3150 V and low pass filtering the simulation results by 2 GHz to match the measurement bandwidth.

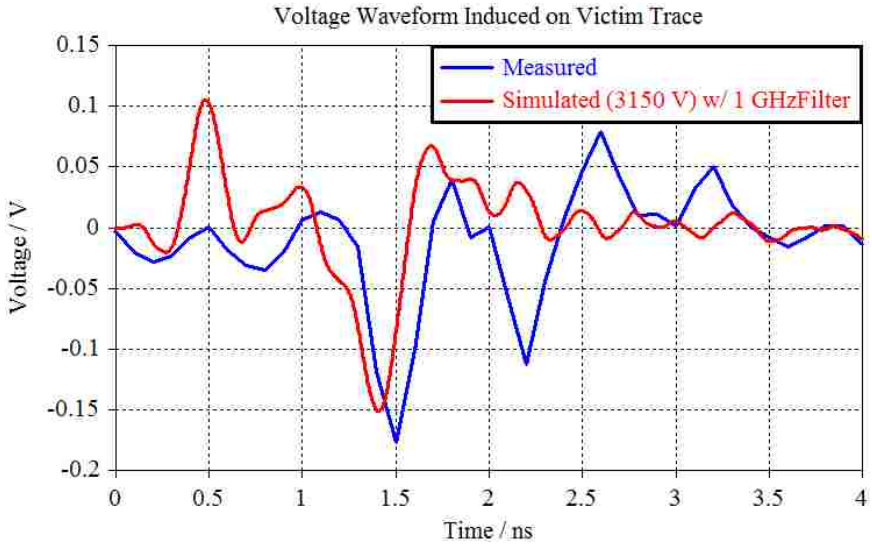



Figure 15. Voltage waveform induced on the victim trace of interest compared between measurement and simulation. The results are obtained using a secondary gap breakdown voltage of 3150 V and low pass filtering the simulation results by 1 GHz.

Qualitatively, the 2 GHz filtered simulation time signal still showed a much higher frequency ringing than the measurement. Fig. 15 shows the comparison of the simulated voltage waveform filtered to 1 GHz. The simulated voltage waveform filtered to 1 GHz qualitatively matched better in terms of ringing. It is possible that the true measurement bandwidth is between 2 GHz and 1 GHz due to the cables and components in the set-up. Simulation results filtered to 20 GHz showed almost no deviation from the results without filtering, and so the simulation set-up has a converged sampling rate for the waveforms. Also shown in Table 1 are results that were filtered to 3 GHz to demonstrate the trend that a narrower frequency band led to lower peak values in the voltage waveform.

Overall, the measured results in Table 2 fall in the range of predicted values from the simulation in Table 1. If the goal is to predict the absolute peak voltage induced on a trace (for example, to make sure that it falls below certain value to protect an integrated circuit), then the unfiltered peak values should be used to predict the outcome.

Using the same machine with two Tesla K80 GPU cards, the TLM solver was able to lump the mesh cells and reduce the complexity to 8,199,223 mesh cells from 5,326,634,035 mesh cells. The simulation took 272 minutes for a simulation time duration of 4 ns.

Table 1. Simulation Results for 15 kV ESD Generator Setting

| Voltage Condition of Switch | Frequency Filter | Peak Voltage on Victim trace | Peak current at ESD Generator Tip due to Primary Discharge | Peak current at ESD Generator Tip due to Secondary Discharge |
|---|---|---|---|---|
| 3150 V | 60 GHz | 498 mV | 19.9 A | 50.2 A |
| | 20 GHz | 498 mV | | |
| | 3 GHz | 310 mV | | |
| | 2 GHz | 238 mV | | |
| | 1 GHz | 151 mV | | |
| 6300 V | 60 GHz | 858 mV | 19.9 A | 54.7 A |
| | 20 GHz | 848 mV | | |
| | 3 GHz | 613 mV | | |
| | 2 GHz | 412 mV | | |
| | 1 GHz | 218 mV | | |
| 9450 V | 60 GHz | 954 mV | 19.9 A | 60.3 A |
| | 20 GHz | 953 mV | | |
| | 3 GHz | 784 mV | | |
| | 2 GHz | 519 mV | | |
| | 1 GHz | 278 mV | | |

Table 2. Measurement Results for 15 kV ESD Generator Setting

| Peak Voltage on Victim trace | Peak current at ESD Generator Tip due to Primary Discharge | Peak current at ESD Generator Tip due to Secondary Discharge |
|---|---|---|
| 177 mV | 21.5 A | 48.8 A |

**4.2. Time Lag.** Time lag is a quantity that is not important from a design perspective (Marathe *et al.*, 2017a), but plays an important role in the physics of secondary breakdown. As mentioned in section 3.2, the time lag of the secondary breakdown can

be quantified if the voltage across the floating earmesh can be measured and the time at which Paschen's voltage is reached can be found. Since this voltage waveform could not be measured for this experiment as explained in section 3.2, the time lag cannot be computed in this measurement. However, we have the voltage waveforms in simulation, so another set of simulations was done (also at 15 kV ESD generator setting) to show the method of setting the time lag rather than setting the voltage condition.

Fig. 16 shows the voltage between the floating earmesh and the grounded housing for statistical time lag settings of 0.8 ns and 1.2 ns. For these simulations, the voltage controlled switch in Fig. 11 is replaced with a time controlled switch that will close after time $t_c$ has been reached in the simulation. Looking at Fig. 16, a gap voltage value that reaches the static breakdown voltage or 3150 V is reached at 1.0 ns, so $t_0$= 1.0 ns (as defined in Fig. 8). $t_c$ can be set by using equation (4).

$$t_c = t_0 + t_s \tag{4}$$

If the goal is to achieve a statistical time lag of $t_s$= 0.8 ns, then $t_c$ should be set to 1.8 ns. Similarly, for achieving $t_s$= 1.2 ns, $t_c$ should be set to 2.2 ns. For these trials, the simulated current waveforms at the ESD generator tip are shown in Fig. 17. Using the time lag solution path, the peak value of current is higher than the peak value of current using the voltage condition solution path. It is apparent that these $t_s$ values lead to a voltage on the floating earmesh that is above 9450 V, and so higher secondary discharge currents and induced voltages on the victim trace are expected.

The level of current from secondary breakdown depends on the conserved quantity, charge (Coulombs), stored across the gap. Though voltage is not a conserved quantity, through the capacitor equation, it is directly proportional to the charge. Hence, the exact statistical time lag does not matter; only the voltage at which the secondary breakdown occurs matters. Controlling the breakdown condition in simulation using a predefined time

lag is not recommended because the time lag parameter does not provide a unique result even in the real world; i.e., the voltage at breakdown can be 5000 V using a time lag of 3 ns or 10 ns.

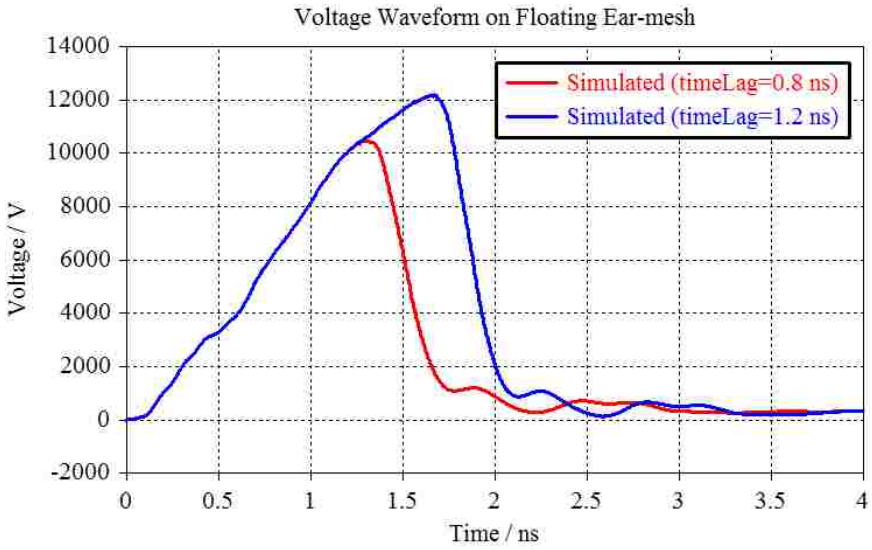



Figure 16. Voltage waveform on the floating earmesh relative to grounded housing. Simulated results with time lag set to be 0.8 ns and 1.2 ns. Paschen's voltage (3150 V) is reached at 1 ns. ESD generator is set at 15 kV.

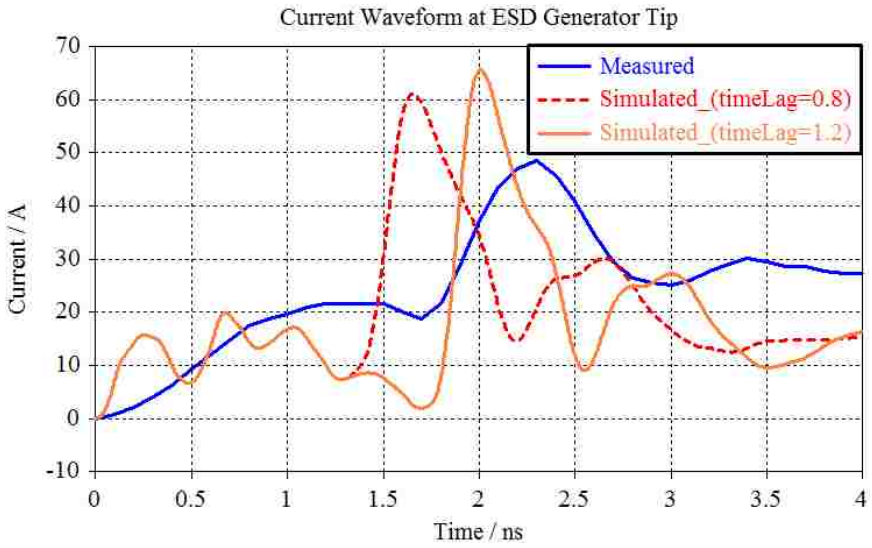



Figure 17. Discharge current waveform at the ESD generator tip, comparison between measurement and simulations that use the time lag condition.

## 5. CONCLUSION

Modeled in 3D was a smartphone susceptible to system level disruption due to secondary breakdown between an ungrounded metal and grounded housing. For the first time, a system-level simulation was performed that could capture noise voltages induced by the secondary ESD. Transient co-simulation was used and did not require computing the entire S-parameter matrix. Two solution paths for controlling the timing of the secondary breakdown in the simulation were given: using a voltage condition and using a time-lag condition. The results were verified by measurements of the noise voltage induced in a victim trace. For future work, the situation of dual air-gap discharge can be simulated, and the disruption on a system-level can be observed. Instead of the primary discharge being in contact mode, it would be in non-contact mode. Two Rompe-Weizel SPICE models would exist in the circuitry, but only the one designated for secondary discharge would be connected to the voltage-controlled switch.

## ACKNOWLEDGEMENTS

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# SECTION

# 2. SUMMARY AND CONCLUSIONS

Transient co-simulation is a novel technique for system level simulation of ESD that does not require the characterization of the 3D model as a set of S-Parameters. Traditional circuit co-simulation can only handle the non-linearity of ESD across an air gap if the S-Parameters of the 3D model are causal, passive, and converged; these are not trivial to achieve for complex models. Furthermore, transient co-simulation is suitable as a complete methodology that would allow visualization of transient fields and surface currents.

In Paper I, the experimental setup of a rod discharging to a ground plane is modeled in 3D. The match between simulation and measurement shows that the Rompe-Weizel model returns the correct discharge current behavior for the tested arc lengths. Also proven in this paper is that the transient co-simulation solution is identical to the circuit co-simulation solution as long as the S-Parameters used in the circuit co-simulation are converged. The visualization of the surface currents with respect to time is also shown.

Next, Paper II modeled a realistic ESD generator and an adjustable spark gap. The physics of Secondary ESD are different than that of single Primary ESD across an air gap, so it was necessary to add more circuit components to the transient co-simulation. The secondary breakdown physics achieved by the new circuit setup were validated by comparing the simulated and measured breakdown voltages on the floating metal. The secondary ESD simulation was validated by comparing to the measured rise times and peaks of the discharge currents.

Finally, Paper III showed how to use the simulation setup in Paper II to accommodate a system level simulation of Secondary ESD in a smartphone and predict the induced voltages on the traces within the smartphone. A methodology was devised to verify (with

measurement) the passive model of the smartphone itself for the coupling path from the Secondary ESD to the victim trace. The simulation method is shown to be practical, efficient, and accurate.

System level simulations involving other exposed modules such as the fingerprint sensor (Wei *et al.*, 2017) or the LCD screen (Shinde *et al.*, 2016) of a smartphone can be performed. The DUT can be modeled, validated, and simulated for air-gap discharge with or without Secondary ESD. As mentioned in Paper III, the situation of the dual gap discharge can now be simulated, and this would be a natural extension to the work done here.

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# VITA

Darwin Zhang Li was born in Manhattan, New York, NY, USA in 1991. He received a B.A. in physics and a B.A. in public health – both from UC Berkeley, Berkeley, CA, USA in 2013. He began pursuing a Master of Science in Electrical Engineering from Missouri S&T in May 2016 and received the degree in May 2018. He has been working full time for Computer Simulation Technology (now 3DS) since January, 2014.