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Comparison of voltage regulation between SST and conventional transformers in high penetration PV power systems

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Department:

COMPARISON OF VOLTAGE REGULATION BETWEEN SST AND CONVENTIONAL TRANSFORMERS IN HIGH PENETRATION PV POWER SYSTEMS

by

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ABSTRACT

Solid state transformers (SST) are power electronic transformers combined with high-frequency conventional transformers and control circuitry capable of delivering high performance and flexible power control capabilities. This thesis focuses on analyzing the performance of SSTs in a distribution system with photovoltaic (PV) injection. In order to validate the performance of SSTs, average value models are used on the IEEE 34 bus distribution feeder network scaled to 12.47 kV. SST voltage profiles on the load side are analyzed and the unity power factor capabilities are demonstrated. This is followed by the study of voltage profiles on the primary side of the SST. Additionally, distributed energy resources such as PV systems tend to cause power quality issues which are handled using the SST's volt-var control capabilities. In this case, both AC and DC side integration of PV systems in SST is demonstrated. DC side integration is one of the advantages of this type of solid state device.

To compare this system to a conventional distribution system, the IEEE 34 bus system with similar load and PV injection profiles is built using conventional single-phase distribution transformers. By comparing the results of the SST (with AC and DC side PV integration) with a conventional transformer, the performance of the SST can be reviewed. To provide a complete analysis, voltage regulators are redesigned for the scaled IEEE 34 distribution feeder network using PSCAD while mounting conventional transformers, and its comparison is provided. Further, the impacts and performance of SST with PV penetration greater than 100% is studied and its results are presented and contrasted with conventional transformers.

ACKNOWLEDGMENTS

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1. INTRODUCTION

Conventional distribution transformers are robust in design and capable of delivering power at a desired voltage to the end consumers. Conventional systems require voltage regulators or tap changing transformers to handle voltage regulation to maintain the feeder voltages within a specified range. In this thesis, the capabilities of solid state transformers (SSTs) to provide voltage regulation and reactive power support is compared against conventional transformers. The Future Renewable Electric Energy Delivery and Management (FREEDM) Center is at the spearhead of the SST development. The capability of the SST to maintain unity power factor at the load is also demonstrated. The SST performance is thoroughly studied in PSCAD in a scaled IEEE 34 bus distribution test bed. Each SST has a single-phase voltage rating of 7.2 kV AC primary and hence the IEEE 34 is scaled to a 12.47 kV three-phase system from the original 24.9 kV system. Distributed energy resources such as photovoltaic (PV) systems are integrated on the AC and DC bus of SSTs. The SST consists of three stages – the active rectifier stage, the dual-active bridge stage and the inverter stage. This allows the integration of the PV system directly to the DC bus of SST's inverter stage without the usage of a separate PV inverter. The PV system with its PV inverter is also connected on the AC side of the SST to compare the performance.

The idea of SST has been discussed since 1970. The limitation of high voltage power electronic devices of that time led to very little progress in improving SST performance. In this paper, the 20 kVA SST used is made of commercially available 6.5 kV silicon IGBTs and silicon diodes to reach required voltage levels [1]. Figure 1.1 shows the three stages of the SST. The AC/DC rectifier converts the single phase 7.2 kV AC voltage to three 3.8-kV DC output voltages using three cascaded H-bridge rectifiers. The rectifier has the ability to hold the reference 3.8 kV DC bus voltage while maintaining unity power factor at the input side. Three high voltage high frequency DC-DC converters in the Dual Active Bridge (DAB) stage convert the 3.8 kV to 400 V. A voltage source inverter (VSI) that inverts 400 V DC to 60 Hz, 240/120 V is part of the inverter stage. A switching model of the solid state transformer must be simulated with very short time steps that leads to very long simulation times. An average model

developed in [2] is therefore used in simulation in PSCAD. An average model reduces the simulation time and memory requirement when compared to detailed switching models. This average model is integrated to the IEEE 34 distribution system and the loads are connected to the 240 V terminals directly for simulation. This is at the discretion of the user to choose between 120 or 240 V output, and does not affect the study of performance of SST.

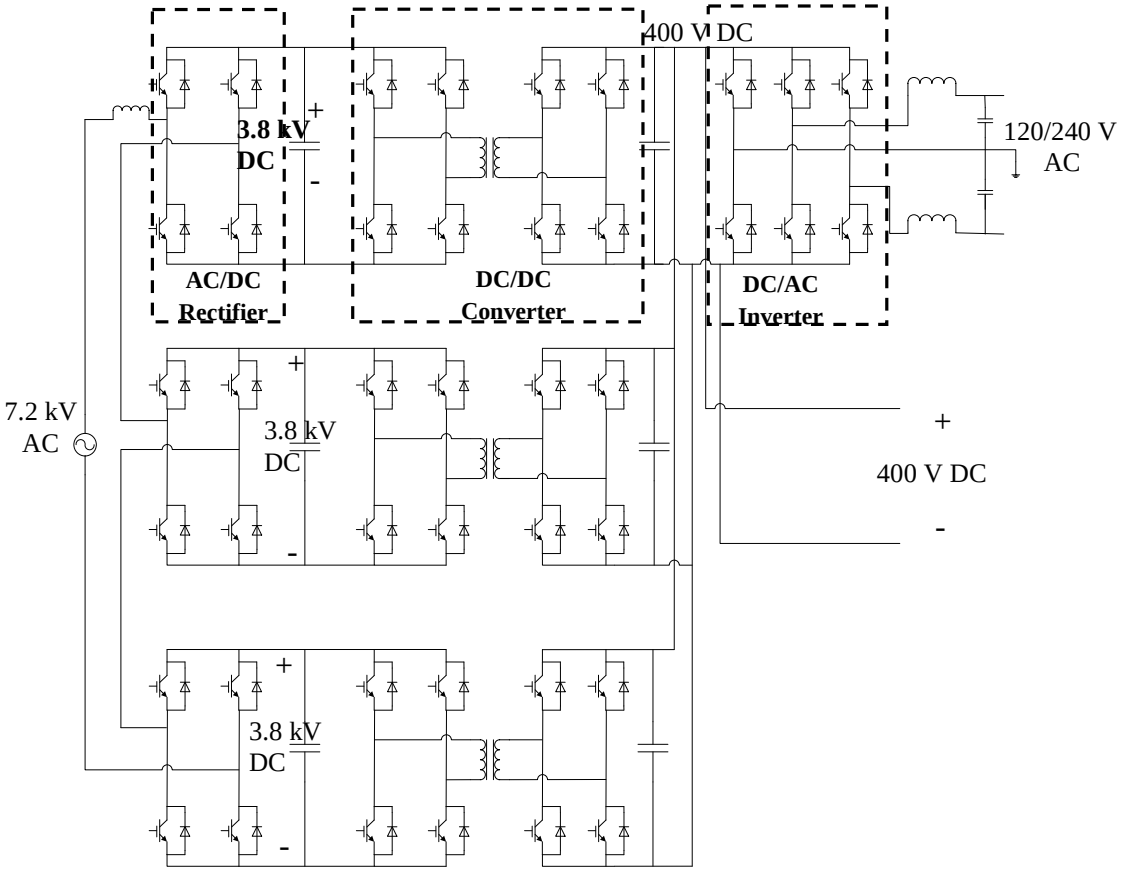

Figure 1.1. Structure of SST

2. SCALED IEEE 34 BUS DISTRIBUTION TEST FEEDER

The IEEE 34 Node Test Feeder has a nominal voltage of 24.9 kV. It is an actual feeder characterized by long and lightly loaded overhead transmission lines, two in-line regulators, and an in-line transformer for a short 4.16 kV section. Figure 2.1 shows the configuration of the IEEE 34 bus system. It serves a total of 24 unbalanced loads with two shunt capacitors. The two in-line voltage regulators are required to maintain feeder voltage profile, but are removed when SSTs are introduced in the feeder. This arrangement will demonstrate the SST's voltage regulation capabilities.

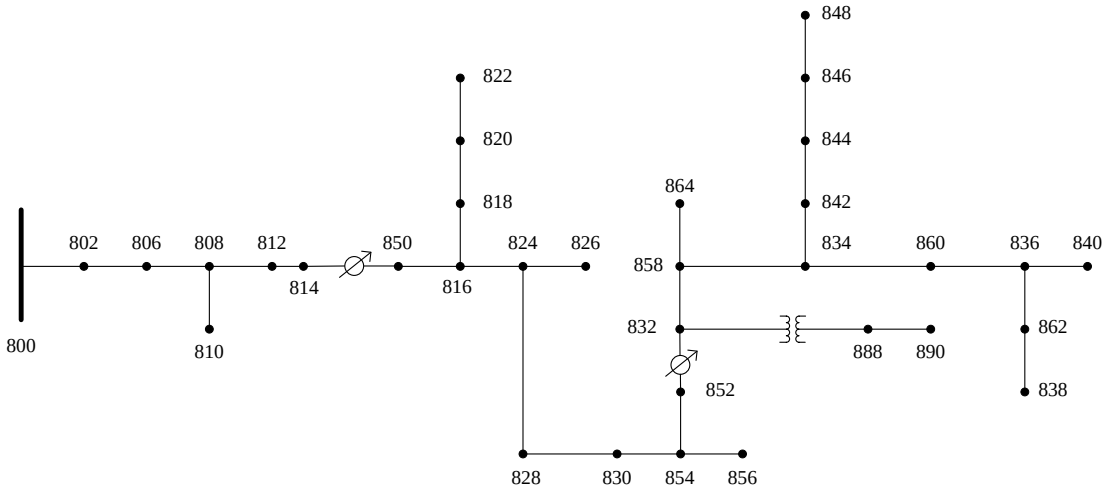

Figure 2.1. Original IEEE 34 Bus System Configuration

The substation is modeled as a 12.47 kV (7.2 kV phase) constant line voltage source to remain consistent with the SST ratings. All parameters, including line impedances, have been converted to a consistent base while scaling [3]. The paper [3] does not provide a method to model or scale voltage regulators to the 12.47 kV source voltage (7.2 kV phase to ground) and is detailed separately in this paper. The SSTs are aggregated to provide a 200 kVA power rating at each bus to remain consistent with the IEEE 34 bus distribution system in PSCAD. The SSTs used are single-phase, to better

accommodate the single-phase feeder laterals and all loads are converted to wye-connected RL loads. Table 2.1 shows the peak load data based on the IEEE 34 from which R and L values at each SST are calculated [4]. Capacitor banks in the original IEEE 34 bus system are also removed since it will be demonstrated that the SSTs provide voltage regulation.

Table 2.1. Peak Load Data Based on IEEE 34 System

Node	kW_A	$kVAr_A$	kW_B	$kVAr_B$	kW_C	$kVAr_C$
822	135	70	0	0	0	0
820	34	17	0	0	0	0
806	0	0	30	15	25	14
810	0	0	16	8	0	0
824	0	0	5	2	0	0
826	0	0	40	20	0	0
828	0	0	0	0	4	2
830	17	8	10	5	25	10
856	0	0	4	2	0	0
858	7	3	2	1	6	3
864	2	1	0	0	0	0
834	4	2	15	8	13	7
860	36	24	40	36	130	71
836	30	15	10	6	42	22
840	27	16	31	18	9	7
838	0	0	28	14	0	0
844	144	110	135	105	135	105
846	0	0	25	12	20	11
848	20	16	43	17	20	16
890	130	75	130	75	130	75

The transformer on bus 832 is scaled down to 12.47kV/4.16 kV. The load varies throughout the day in accordance with the normalized daily load curve shown in Figure 2.2, which represents a typical residential load [4].

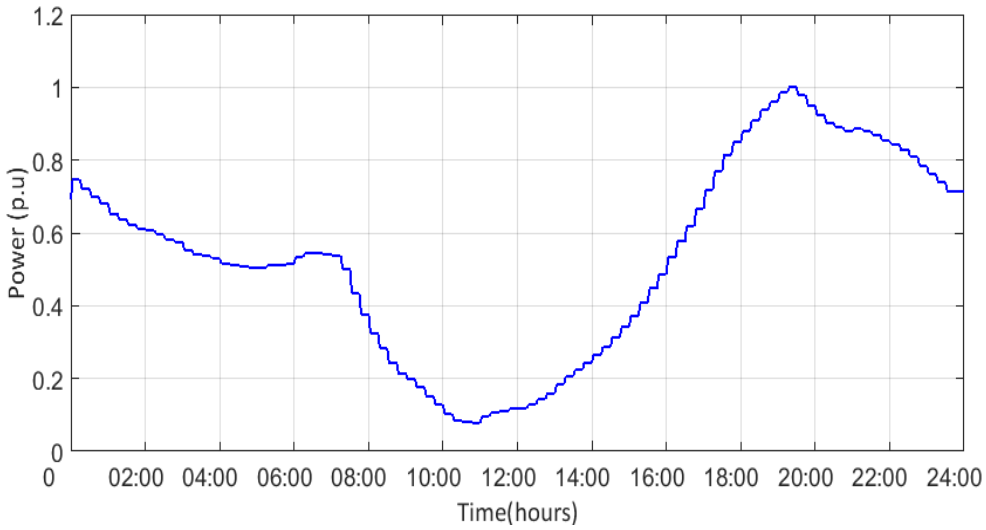

Figure 2.2. Daily Load Profile in Per Unit

3. PV SYSTEM INTEGRATION

3.1. PV SYSTEM FOR INJECTION THROUGH AC AND DC BUS IN SST

PV injection is achieved by direct integration of the PV array with its inverter on the AC load side of the SST as shown in Figure 3.1. The PV system is modelled to inject current based on the insolation profile shown in Figure 3.3. The PV system is modeled as a current source. The maximum voltage the PV module can provide is 212.8 V. Therefore, to provide the voltage up to the reference voltage setpoint, a DC-DC boost converter is connected to the PV module. The MPPT control and inverter control is achieved using simple PI controllers. The MPPT controller controls the switching duty cycle of the DC-DC Boost converter to achieve the reference voltage set by the MPPT algorithm. The inverter controller controls the input current to the inverter based on the output voltage of the DC-DC boost converter.

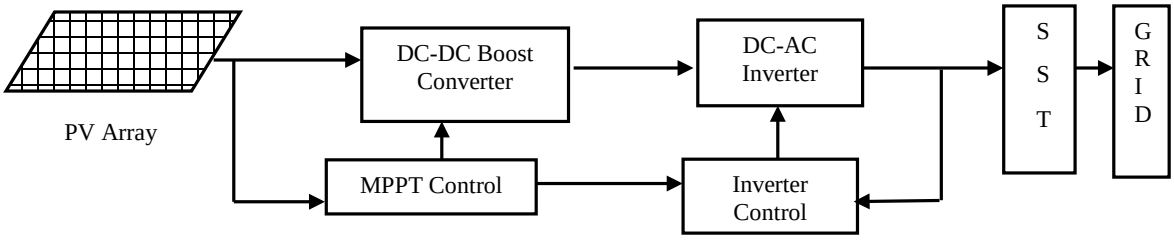

Figure 3.1. Block Diagram of the PV Model Integrated to Load of SST

In the case of connecting the PV module to the secondary side of the DAB link, the need for the inverter is eliminated as secondary of the DAB link is a low voltage DC link at 400 V. Figure 3.2 shows this arrangement without the need for a separate PV inverter.

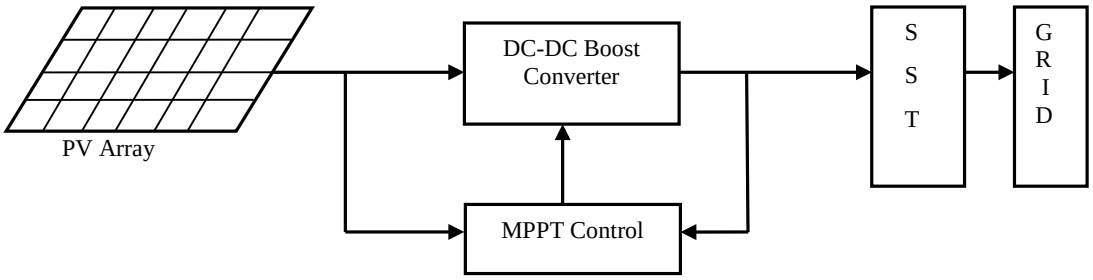

Figure 3.2. Block Diagram of the PV system connected to the DAB link of SST

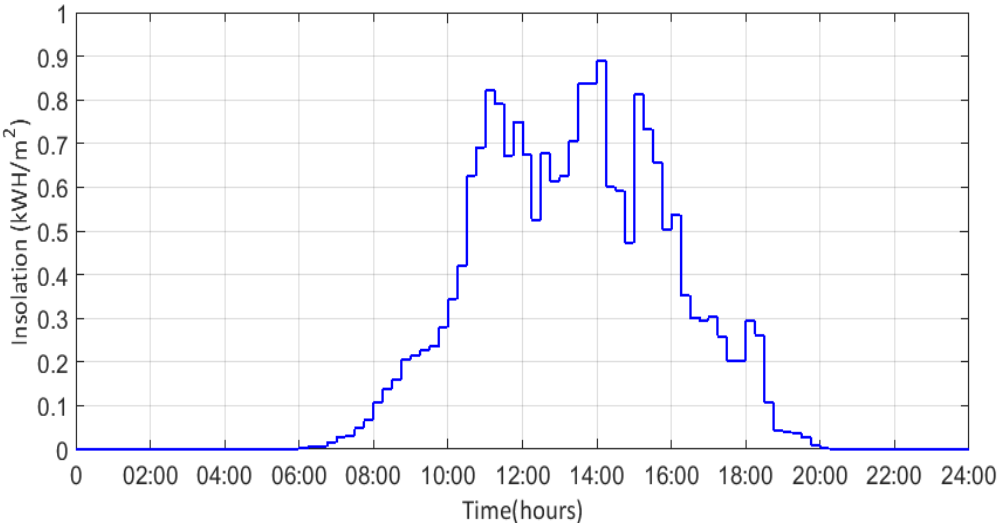

Figure 3.3. Daily Insolation Profile

3.2. CURRENT BASED PV MODEL

The current from the PV module, I_{pv} is based on the standard equivalent circuit of a photovoltaic cell.

$$I_{pv} = I_{ph} - I_0 \left[e^{\frac{q*(V_{pv}+R_s*I_{pv})}{NsKT_j}} - 1 \right] - \frac{V_{pv} + R_s * I_{pv}}{R_{sh}} \quad (1)$$

In equation 1, I_{pv} is the current of the PV cell; I_{ph} is the photocurrent, which is directly proportional to solar irradiance (G); I_0 is the reverse saturation current of the diode; q is the electron charge (1.602×10^{-19} C); K is the Boltzmann's constant (1.381×10^{-23} J/K); A is the diode ideality factor, T_j is junction temperature of the panels, and V_{pv} is the voltage across the PV cell. A large wealth of literature is devoted to developing mathematical methods to solve equation 1 [5]. The study of these mathematical methods is omitted here, as this is not the goal of this thesis. Based on one of the analytical methods, the PV module is modelled and simulated in PSCAD software. The PSCAD model of the PV module is shown in Figure 3.4. In Figure 3.4, the inputs to the developed model are the input voltage of the boost converter (Vpv), the solar insolation (ins), and the ambient temperature (tc) where Ipv is the PV module current.

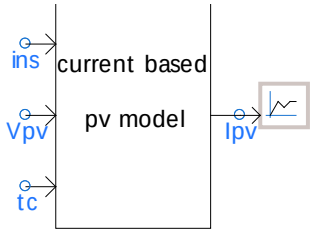

Figure 3.4. PSCAD Model of the PV Module

3.3. MPPT CONTROLLER

There are numerous MPPT controller algorithms with varying complexities [6]. Since the focus of this thesis is the SST and not the MPPT, the simple Perturb & Observe (P&O) algorithm is implemented as the controller in PSCAD. The control variable chosen for the maximum power control in the model is solar array terminal voltage (Vp). Figure 3.5 shows the PSCAD model of the MPPT controller and its algorithm.

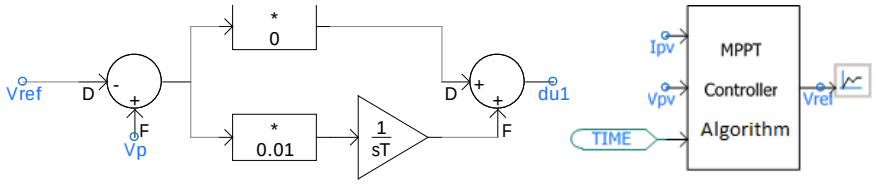

Figure 3.5. PSCAD Model of MPPT Controller and Control Algorithm

3.4. AVERAGE BOOST MODEL

To maximize the output power of the PV array, a power conditioner is added between the PV array and the load. A DC-DC converter is often used. The boost converter is designed, modelled, and simulated to fulfill this purpose. The circuit diagram of the boost converter is shown in Figure 3.6.

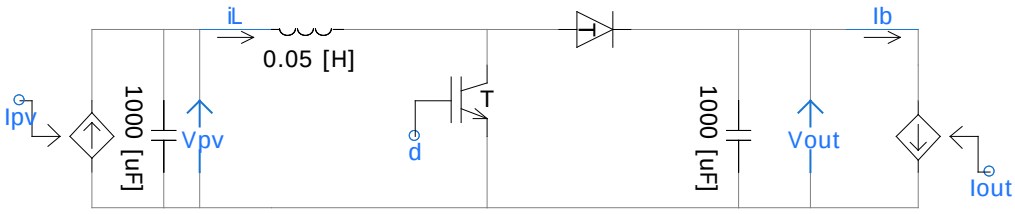

Figure 3.6. Circuit Diagram of the Boost Converter

There are three states in the boost converter: the input capacitor voltage (Vpv), the inductor current (iL), and the output capacitor voltage (Vout). The average steady state equations for the three states of the converter are given in equations 2 to 4.

$$V_{pv} = \frac{1}{C_{in}} \int \left(I_{pv} - i_L \right) dt \tag{2}$$

$$i_L = \frac{1}{L} \int \left(V_{pv} - (1-d) * V_{out} \right) dt \tag{3}$$

$$V_{out} = \frac{1}{C_{out}} \int \left((1-d) * i_L - i_{out} \right) dt \tag{4}$$

The three equations above are modeled in PSCAD. Figure 3.7 shows the equations modeled in PSCAD and the average boost model

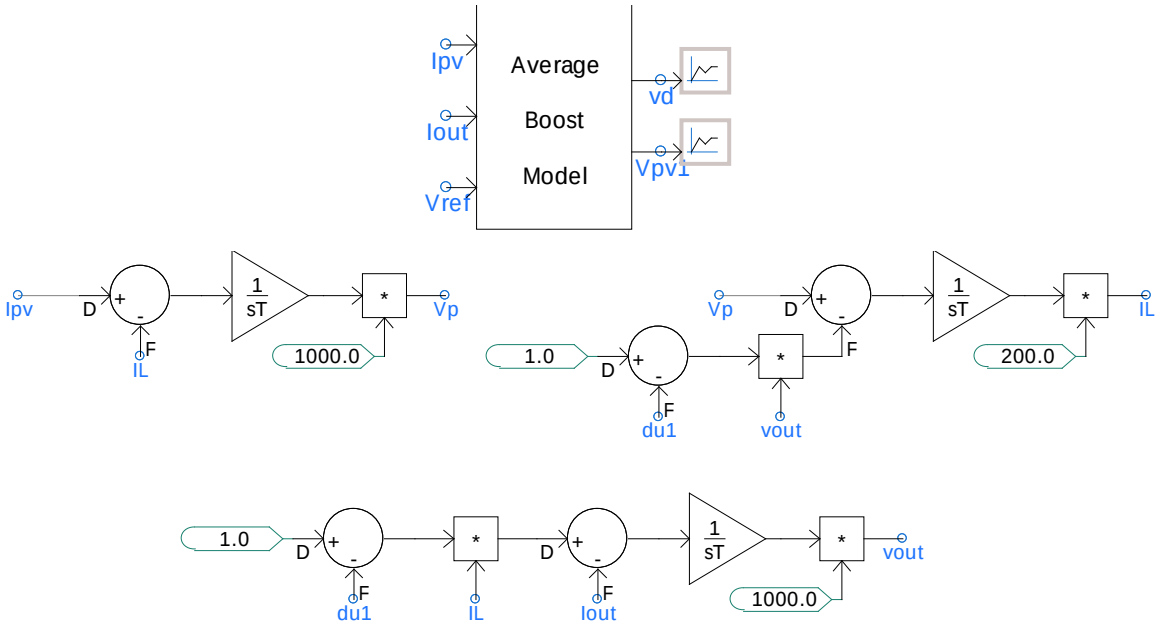

Figure 3.7. Average Boost Model and States of the Boost Converter in PSCAD

3.5. AVERAGE INVERTER MODEL

In order to inject PV in the AC side of the SST, a PV inverter must be used. The inverter is based on [7] and Figure 3.8 shows the basic switching circuit on which an average model is based. The inverter control parameter is the input current provided to the inverter which is calculated using the relationship in equation (5).

$$V_{out} \cdot I_{out} = V_{load} \cdot I_{load} \tag{5}$$

The input current is computed by the controller based on the reference voltage provided. Figure 3.8 shows the controller that computes this input current and the average model realization in PSCAD is shown in Figure 3.9.

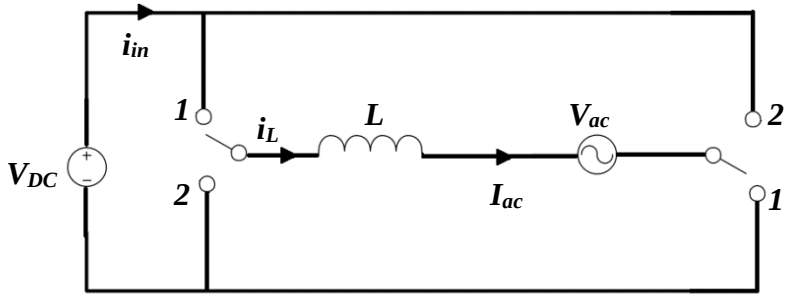

Figure 3.8. Circuit Representation of Single-phase Inverter

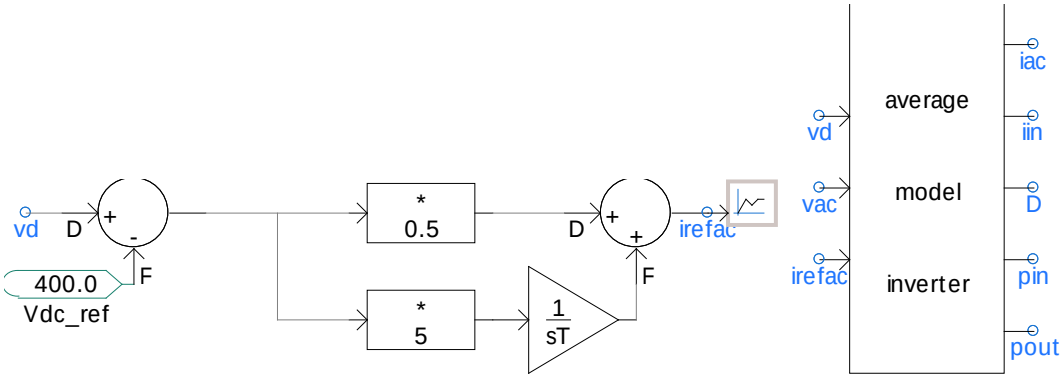

Figure 3.9. Inverter Controller and Average Model of Inverter Modelled in PSCAD

The inputs to this inverter model are the output voltage of the DC-DC boost converter (Vd), the line-to-line voltage of the load side of the SST (vac), and the reference current (irefac), which is peak load current of the inverter. The peak load current is multiplied with a sinusoidal component which is in phase with the load. The phase of Iload is calculated accordingly using a PLL (Phase Locked Loop). Iload is then converted to iac. The output of the inverter model iin is filtered to get the current iout.

4. SST PERFORMANCE WITH 100% PV INJECTION

4.1. SST OPERATION IN UNITY POWER FACTOR MODE

The SST's ability to regulate voltage on the load side is based on the active rectifier's single-phase d-q decoupled control on the high voltage side [2]. In the absence of a reactive current command to the q-component of active rectifier, the power factor is maintained at unity. This has been demonstrated in [4] as a feature of the SST where input voltage to the SST is in phase with input current despite the load power factor. This feature of the SST is also verified through simulation to establish the result and make further comparisons to the various modes of SST operation in this report with 100% PV penetration at select buses. The selection of pilot buses on such an unbalanced feeder is based on availability of the phase at the node and its impact on voltage profile. Among various methods to select the buses, the method used in [4] is used in this thesis. For 100% PV penetration, the total power rating of the installed PV on a particular bus should be equal to the maximum load that occurs at a given point in the day at that bus. This presents an undesirable bus voltage profile on the high voltage side since the load peak and PV power peak occur at different periods in the day, as evident from Figure 2.2 and Figure 3.3. When high penetration of PV is available, the load demand is lower, causing voltage levels to rise above 1.05 p.u. The voltage falls below 0.95 p.u when the load demand is higher at night, with corresponding PV power injection at its lowest. The absence of battery storage in demonstrating voltage control presents a challenge in maintaining voltage profile.

Figure 4.1 shows the 7.2 kV AC input voltage is in phase with the current irrespective of load magnitude and nature of load by means of the active rectifier in the SST bus 890 phase A. The SST renders the load voltage unaffected by feeder voltage variations as seen in Figure 4.2. The PV injection from the distribution feeder impacts the magnitude and direction of the current drawn at the primary side of the SST. When the PV injection exceeds the load capacity due to a variable load profile, the excess power is sent back to the grid in the absence of any battery storage, which is the case analyzed. Thus, the reactive power command of the SST will still be set to zero while the direction of current would reverse, thereby providing bi-directional capabilities.

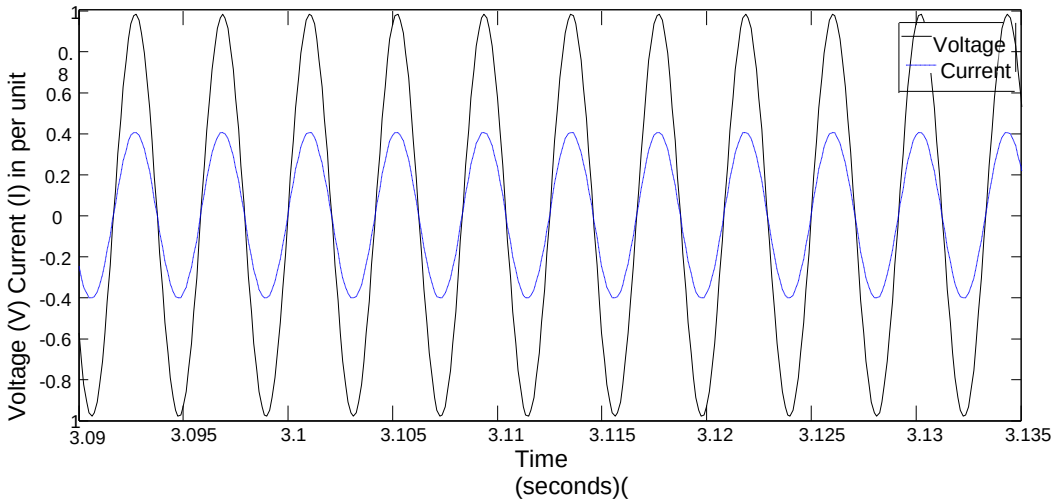

Figure 4.1. SST Input Current and Voltage Waveforms during Active Power Transfer

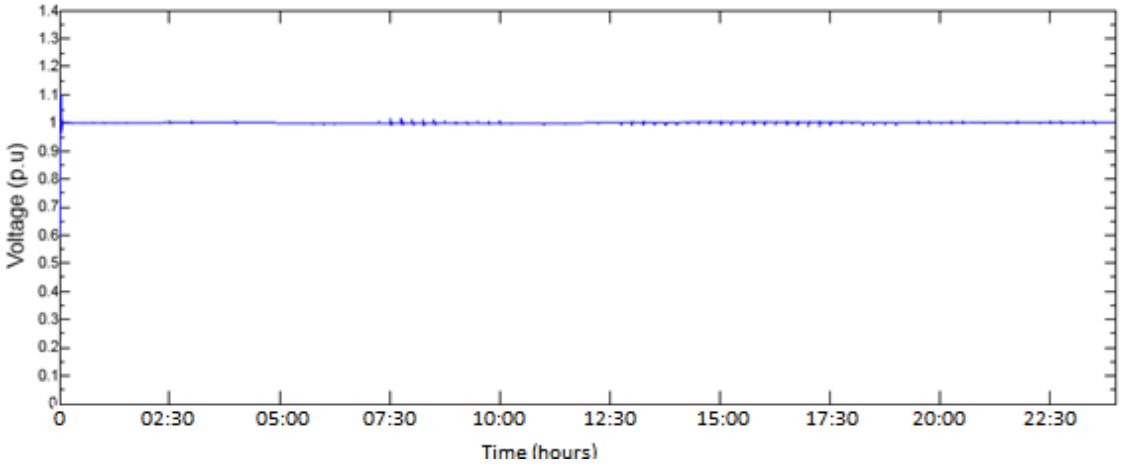

Figure 4.2. Voltage on the Load Side of the SST at Bus 890 A

The voltage of the 3.8 kV DC capacitor in Figure 1.1 is regulated by the active current [8]. However, the IEEE 34-bus test system is inherently unbalanced and with the voltage regulators removed, the voltages in the primary side are not maintained within the acceptable limits of 0.95 to 1.05 p.u. When the reactive power regulation is zero from the SST, the primary side voltage of phase A at 890 is shown in Figure 4.3 where the voltage exceeds the acceptable limits. Figure 4.4 and Figure 4.5 show the 890 phase B and phase voltages respectively.

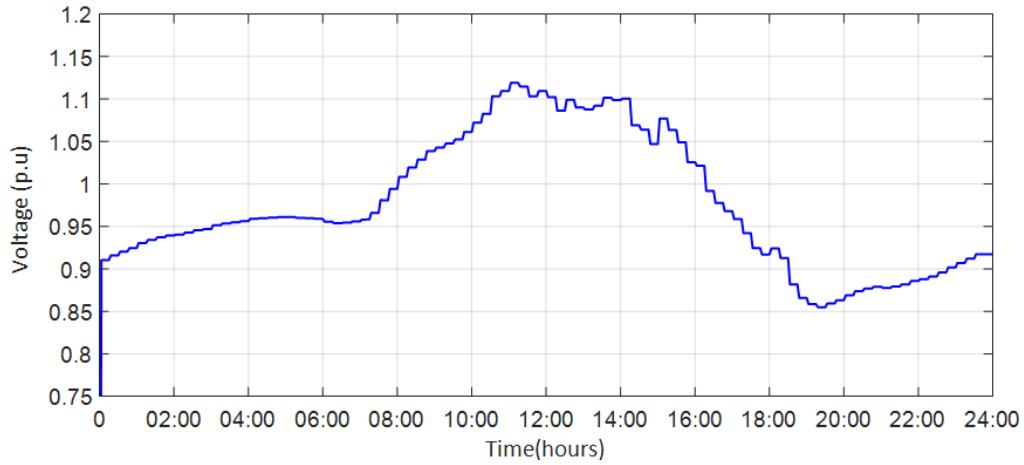

Figure 4.3. Voltage on the SST Primary at Bus 890 A without VVC

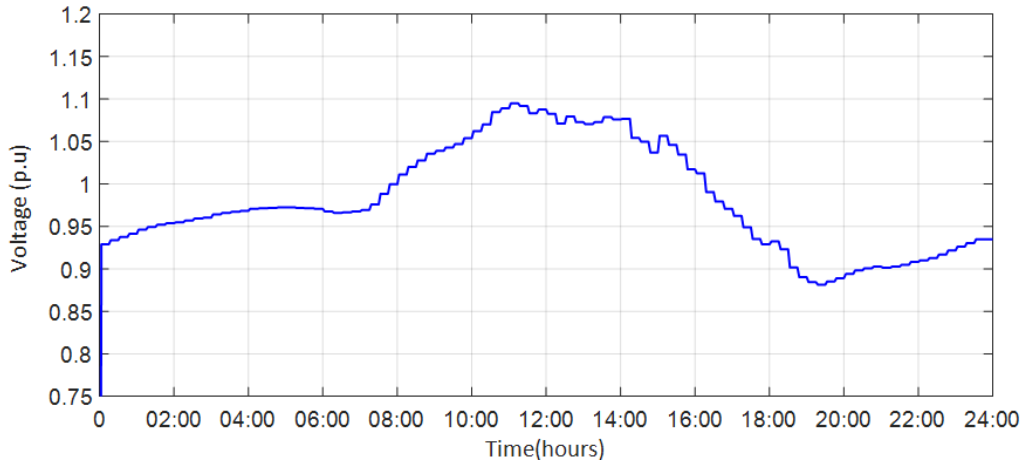

Figure 4.4. Voltage on the SST Primary at Bus 890 B without VVC

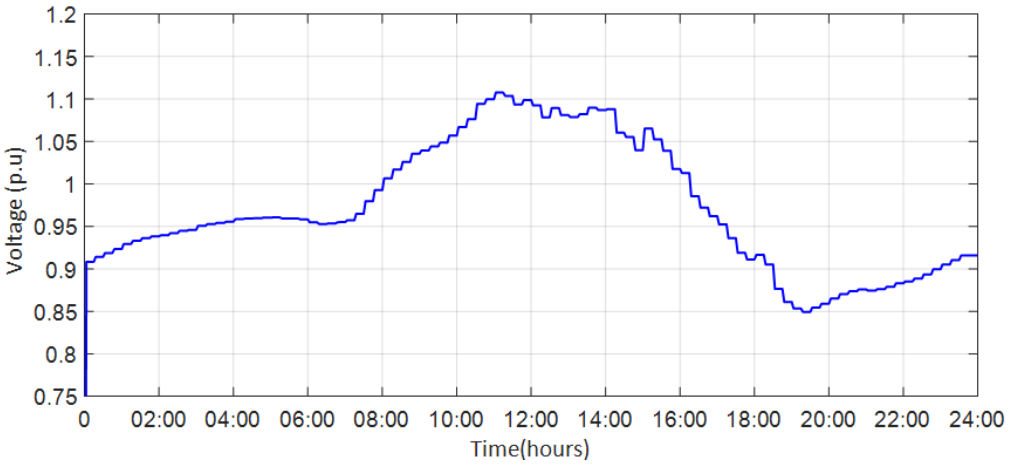

Figure 4.5. Voltage on the SST Primary at Bus 890 C without VVC

Reactive power injection is necessary to maintain acceptable voltage profile and the SST is capable of either absorbing or generating this reactive power. In [4], an algorithm to maintain the primary SST voltage within the acceptable limits was proposed. This provides a reference for the reactive current instead of maintaining a unity power factor. In unity power factor case, reactive power exchange is negligible as seen from Figure 4.6, achieving near unity power factor.

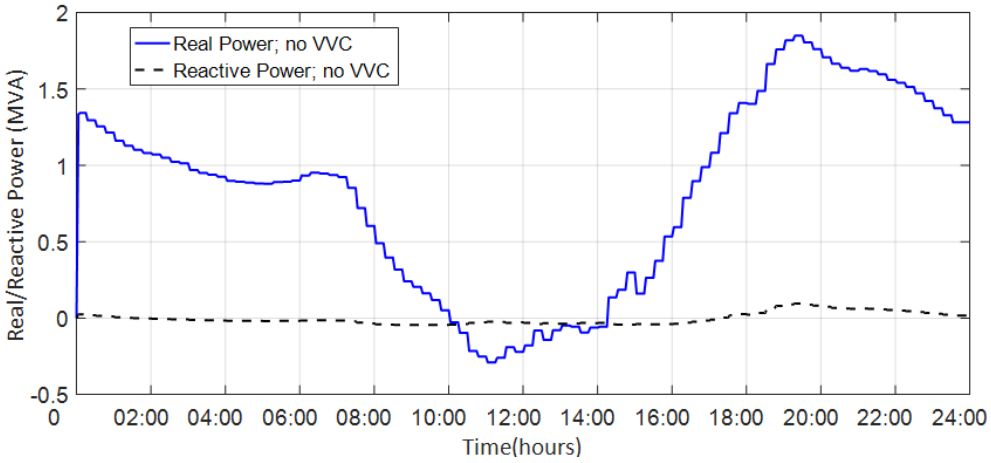

Figure 4.6. Total Active and Reactive Power Input in Substation without VVC

Even with reactive current exchange, the power factor is closer to unity, and reactive power capabilities are well within the rating of the SST. The SST is able to provide bidirectional capabilities with PV integration in the DC bus or on the AC low-voltage load bus. An effort is made to replicate the result of DQDV algorithm method in [4] with PSCAD showing DC injection of PV power, with volt-var control (VVC). Following DC injection, the AC side PV injection with volt-var control is achieved in IEEE 34 bus system and seamless PV integration is demonstrated.

4.2. SST VOLTAGE PROFILE WITH PV INJECTION ON DC BUS AND VVC

The SST's ability to regulate load side voltage to nearly 1 p.u was demonstrated using PSCAD and this result as shown in Figure 4.2. When bus voltage are beyond acceptable limits, the DQDV algorithm allows the voltage variation in response to reactive power injection or absorption, tending to keep the voltage within acceptable range of 0.95 and 1.05 pu. A FORTRAN script is written to provide a definition of the algorithm in PSCAD. The inputs to the algorithm are the RMS voltage for grid voltage reference and active power P. The algorithm will command the active rectifier to inject reactive power to the ac grid when the voltage is below 0.95 and absorb reactive power if the voltage exceeds 1.05. The reactive power is translated to reactive current component reference Iq*, which is part of the single phase d-q vector controller in the active rectifier. The rate at which Q varies is kept to 20 kVARs per second, and this speed can be directly implemented in real-time [4]. The algorithm ensures that the apparent power rating of the SST is not allowed to reach more than 200 kVA. Even with reactive power injection or absorption, the total power is within the SST limits. In [4], a piece-wise look-up table is used to pair values of the required reactive power reference Q* with Iq*. Since the values are nearly linear, instead of the look-up table, the values of Iq* can be derived directly by the slope of Q vs. I plot from the look-up table. This results in a continuous change instead of step-wise change of reactive current for any change in Q reference and either approach will yield volt-var control.

Figures 4.7, 4.8 and 4.9 show the effect of volt-var control algorithm on the primary side voltages of the SST in buses 890 A, 890 B and 890 C. The variable load and insolation profile render variations in the voltage profile. The voltage is maintained

within the lower and upper bounds of 0.95 and 1.95 pu on a 7.2 kV base. The reactive power exchange is significantly higher with VARs incoming and outgoing through the substation as seen in Figure 4.10.

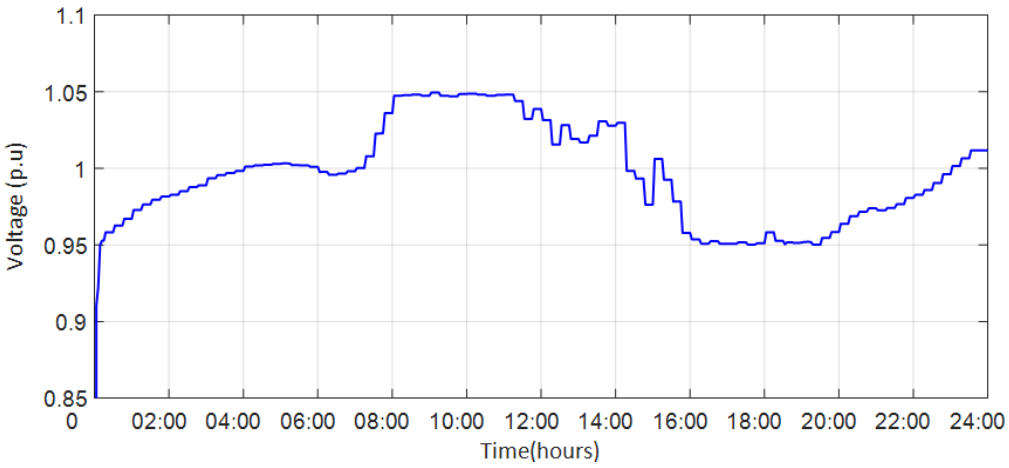

Figure 4.7. Voltage on SST Primary in Bus 890 A after VVC

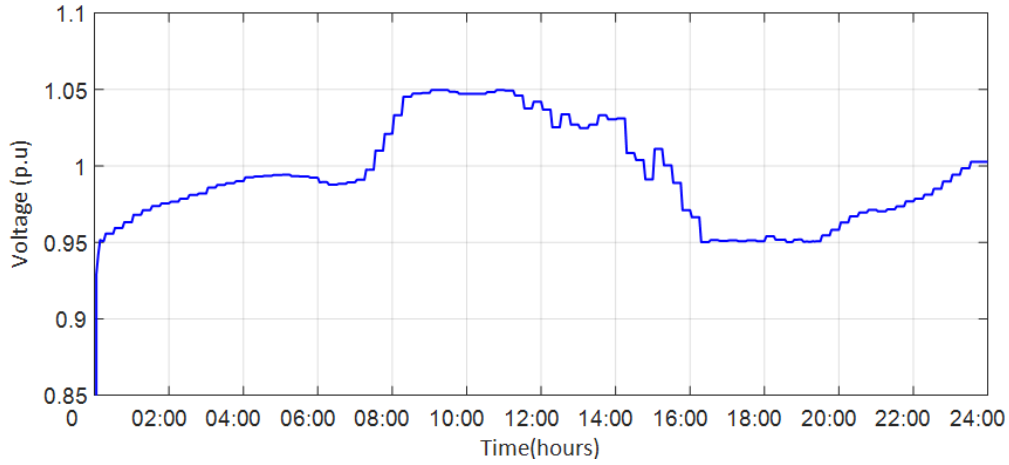

Figure 4.8. Voltage on SST Primary in Bus 890 B after VVC

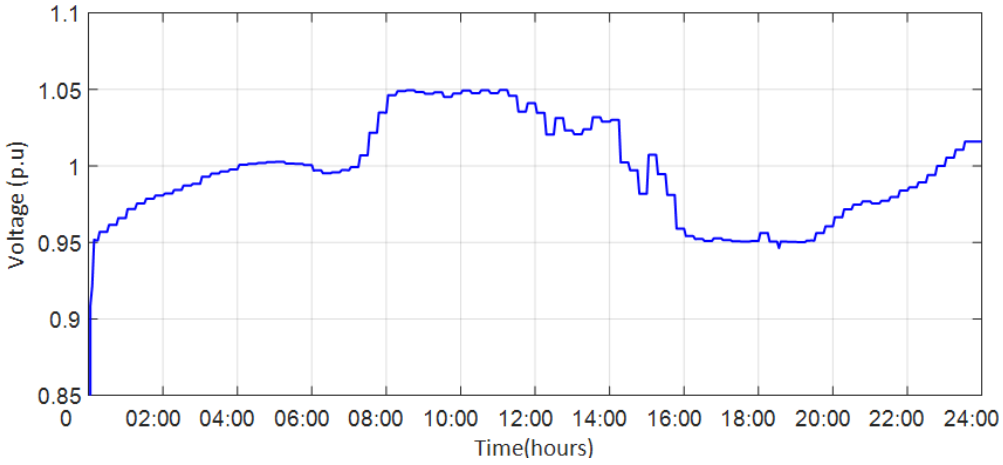

Figure 4.9. Voltage on SST Primary in Bus 890 C after VVC

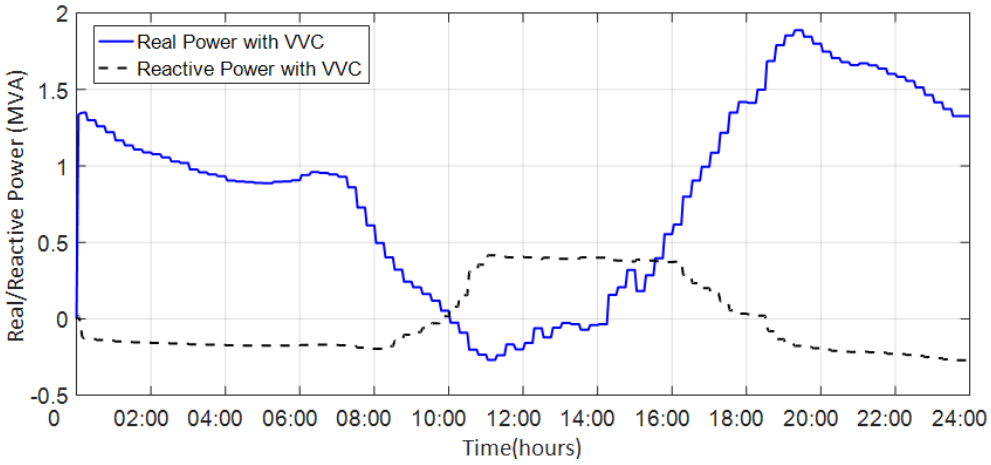

Figure 4.10. Substation Active and Reactive Power Input after VVC

4.3. SST VOLTAGE PROFILE WITH PV INJECTION ON AC BUS AND VVC

Only the DC bus injection of PV was demonstrated in [4] with its subsequent voltage control. The SST is capable of allowing PV integration on the AC side. The addition of an inverter is necessary for the AC side integration of the PV source. In Section 3.1.4, an average model of a single phase inverter is introduced. This inverter average model is based on the simple H-bridge configuration to demonstrate the PV AC side integration [7]. The PV inverter current is in phase with the grid AC voltage, with

grid reference angle, theta provided by means of a phase-locked loop (PLL). The losses are also modeled in the inverter averaged model and the AC current is directly fed to the grid.

With the integration of PV on the AC side, the SST is able to maintain its unity power factor operation on the AC load side when Iq* reference is zero. In the buses with PV integration on AC, the bidirectional power transfer is also seamless, demonstrating the SST's flexibility. Figure 4.11 demonstrates the SST's ability to hold AC load side voltages to nearly 1 pu while PV is integrated to the AC load bus.

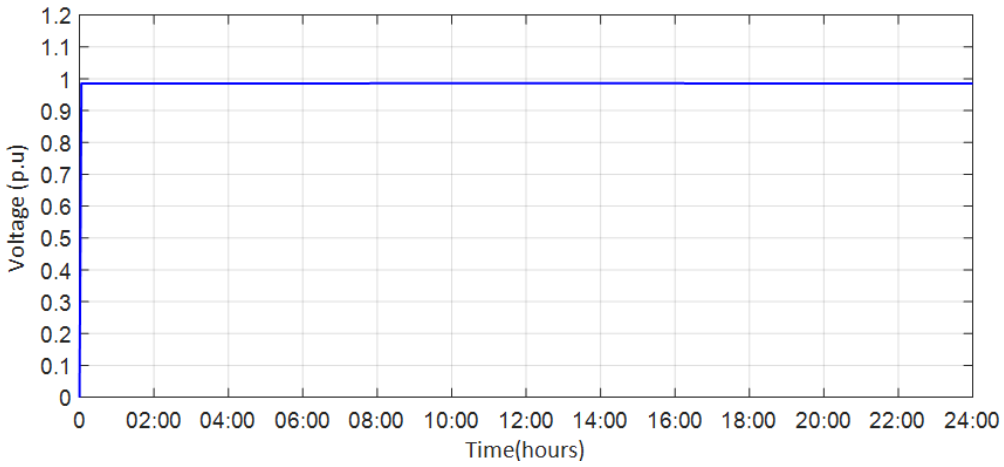

Figure 4.11. Voltage on the Load Side of the SST at Bus 890 A with PV AC injection

The maintenance of the low side voltage to near 1 pu indicates the successful integration and power delivery to the load with a distributed energy resource (DER) on the AC side via the inverter. The SST's capacity to maintain the grid side AC voltage depends on the reactive power management of the SST. Since power sharing is seamless, the reactive power management through the tested volt-var control method used for DC PV injection is successfully demonstrated for the AC side PV integration. The results are validated for four pilot buses with PV AC side injection. The buses 810 B, 806 C and 822 A are well within the 0.95 and 1.05 limits. Typically bus 890 is critical, for which the results of all three phases are represented. The expected power profile of the SST is

similar to the DC injection of PV. Figure 4.12 shows the PV injection in bus 890A on the AC load side with volt-var control indicating the intended PV power is successfully injected through the PV inverter interface, delivering AC power. Figure 4.13 to 4.15 show the voltage profiles of bus 890.

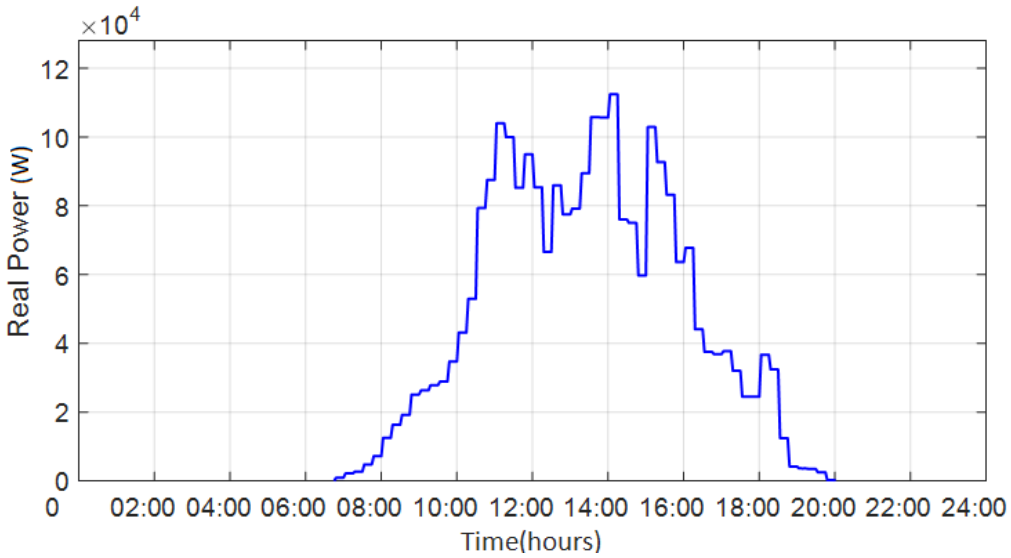

Figure 4.12. PV Injection on the AC Load Side of the SST at 890 A

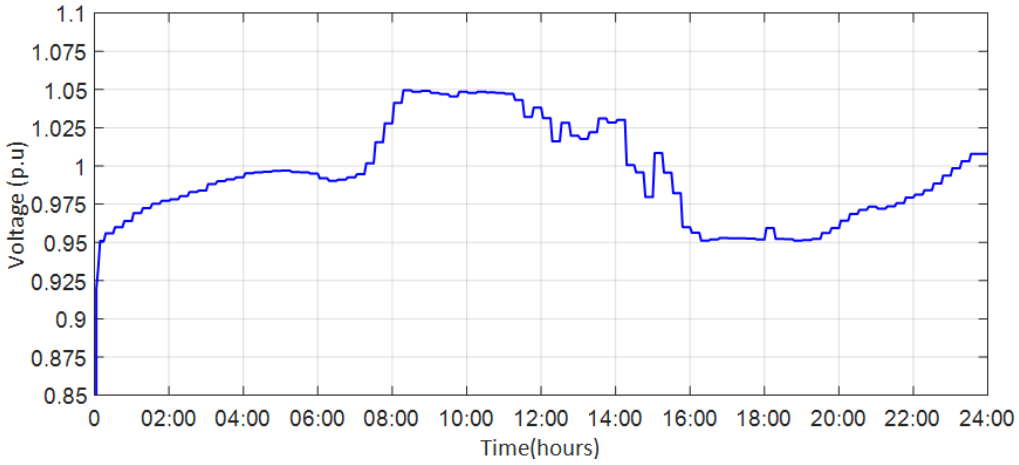

Figure 4.13. Voltage on the SST Primary at Bus 890 A after VVC and PV AC injection

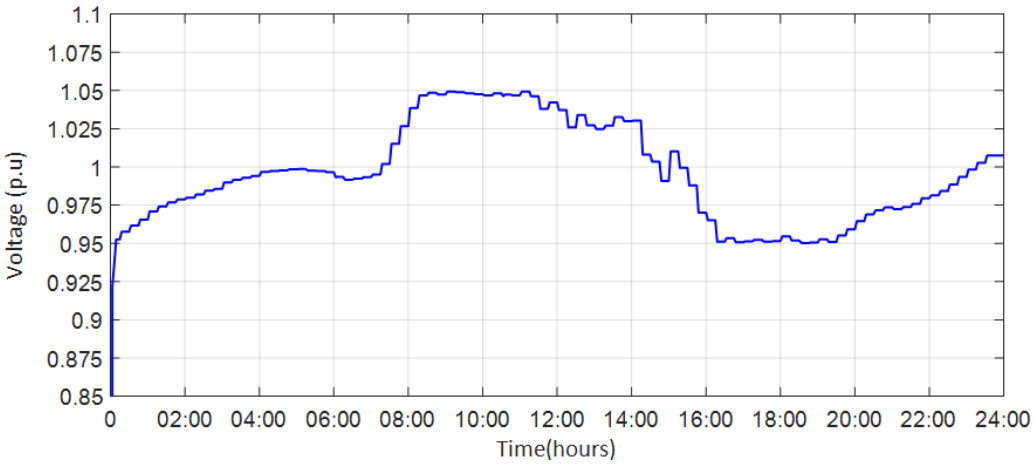

Figure 4.14. Voltage on the SST Primary at Bus 890 B after VVC and PV AC injection

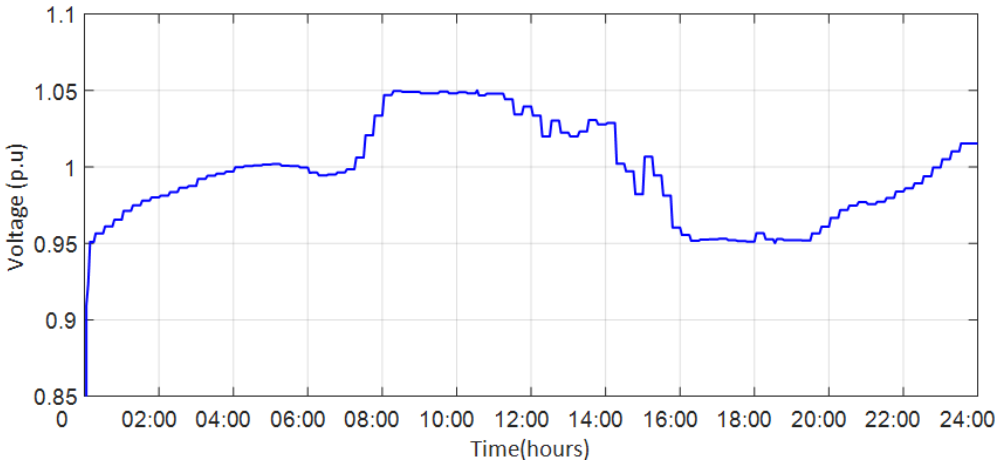

Figure 4.15. Voltage on the SST Primary at Bus 890 C after VVC and PV AC injection

It is evident from the results that 100% AC integration of PV can be seamless and offer reliable performance as DC PV injection. The generation and absorption of reactive power is facilitated by the SST and is reflected in the substation. The total active power and reactive power of the system is shown in Figure 4.16 after VVC is implemented in the SST. Voltage regulation performance is comparable to the DC PV injection case. The effect of adding the inverter for AC side coupling is visible in the power injected by

PV and consequent absorption from the grid. As expected, the inverter losses contribute to marginally lower PV injection compared to the DC PV injection case, which renders the power deficit to drawn from the grid as evident from Figures 4.17 and 4.18.

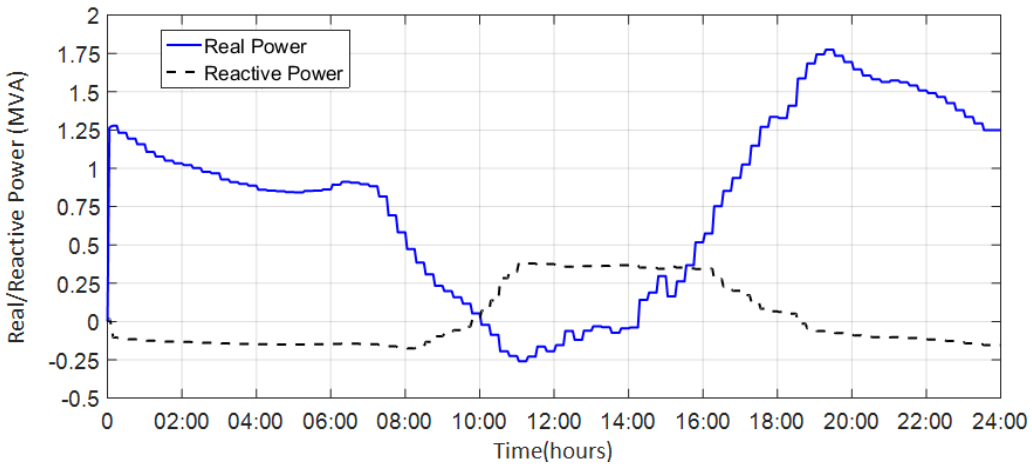

Figure 4.16. Substation Active and Reactive Power Input after VVC with AC PV injection

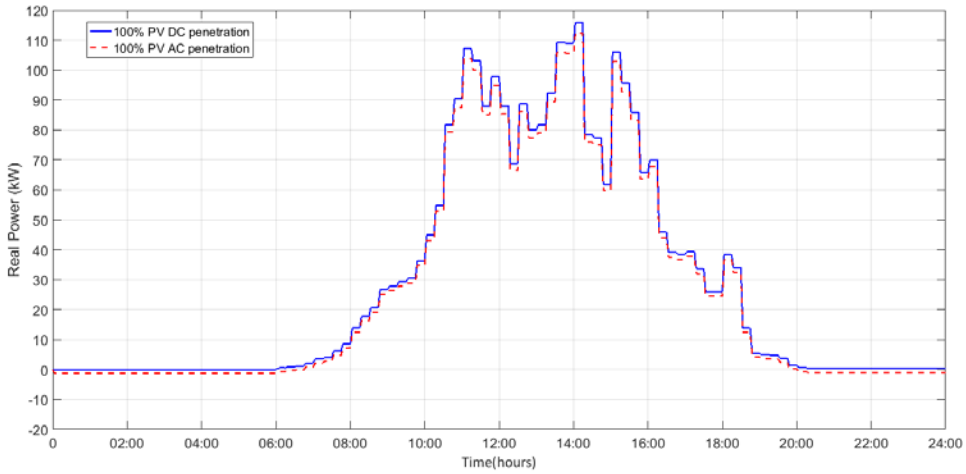

Figure 4.17. PV injection in Bus 890 A with AC and DC PV injection

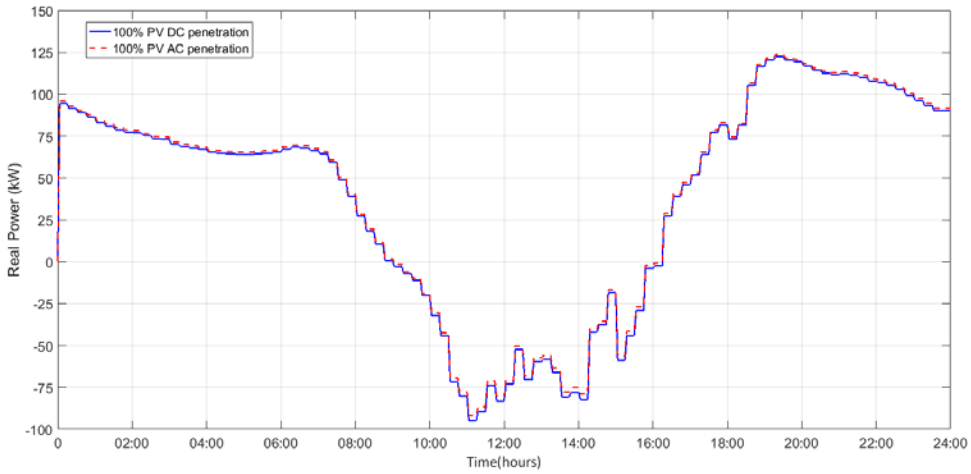

Figure 4.18. Active Power in Bus 890 A with AC and DC PV injection

5. COMPARISON OF SSTS WITH CONVENTIONAL TRANSFORMERS IN THE IEEE 34 BUS SYSTEM

5.1. DEPLOYMENT OF CONVENTIONAL TRANSFORMERS

To contrast the performance of the SST in a typical distribution system, conventional transformers are integrated into the scaled IEEE 34-bus system. The transformer is a single-phase 7.2 kV to 240 V transformer output. A typical distribution system has split-phase 120/240 V output, but for comparison with SSTs which have loads connected across 240 V outlet, the single-phase transformer is simplified to a normal two-winding 7.2 kV to 240 V configuration in the PSCAD simulations. A typical two-winding transformer at the 200 kVA level can have a 4% to 6% leakage impedance. A leakage impedance of 4% is chosen based on [9]. A typical two-winding transformer in PSCAD is shown in Figure 5.1.

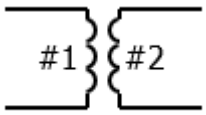

Figure 5.1. A Two-winding Transformer in PSCAD

The transformers are deployed at every bus that was previously served by a SST. The load model and load profile remain unchanged from the load models used with solid state transformers. The transformers and load are placed in a single module in PSCAD and the workspace of the IEEE 34 testbed with transformers shown in Figure 5.2 depicts the scale of simulation. In the chosen configuration to be deployed, there are no on-line tap changers. Initial comparisons are made with removal of the two in-line voltage regulators presented in the IEEE 34-bus distribution feeder data to remain consistent with the system used for SST deployment.

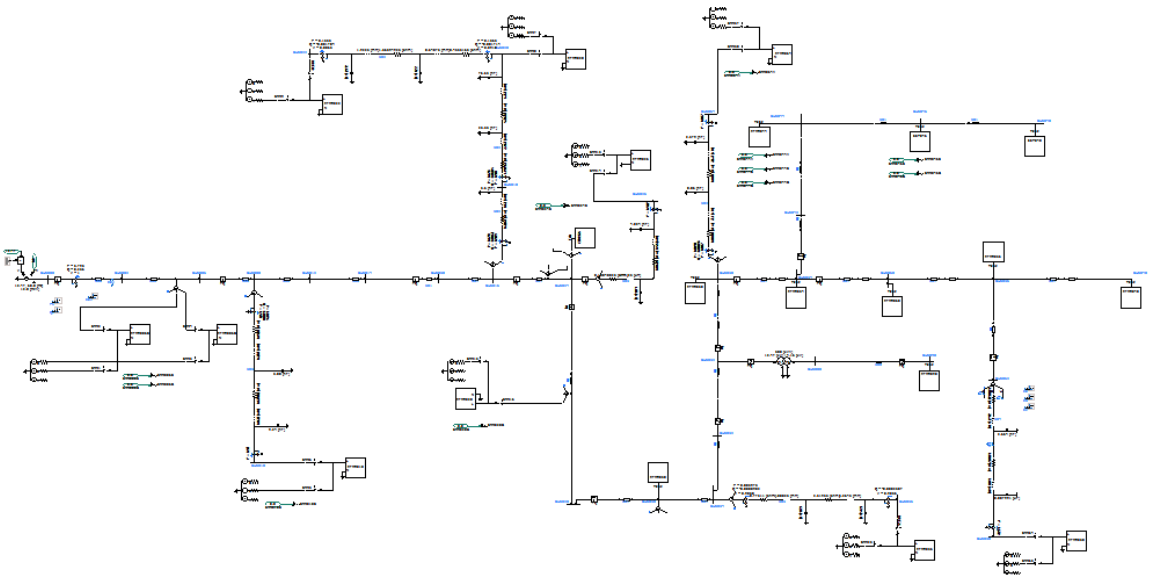

Figure 5.2. Modified IEEE 34-Bus System with Conventional Transformers in PSCAD

5.2. VOLTAGE REGULATION CONTROL IN SCALED IEEE 34 BUS SYSTEM

Conventional transformers provide no voltage regulation independently. Unlike the SST, the load and bus voltage are equally affected, except for the load voltage drop due to leakage impedance of transformer. The voltage profiles of the electrically distant bus with PV injection, Bus 890, at the transformer primary is shown in Figure 5.3 to 5.5.

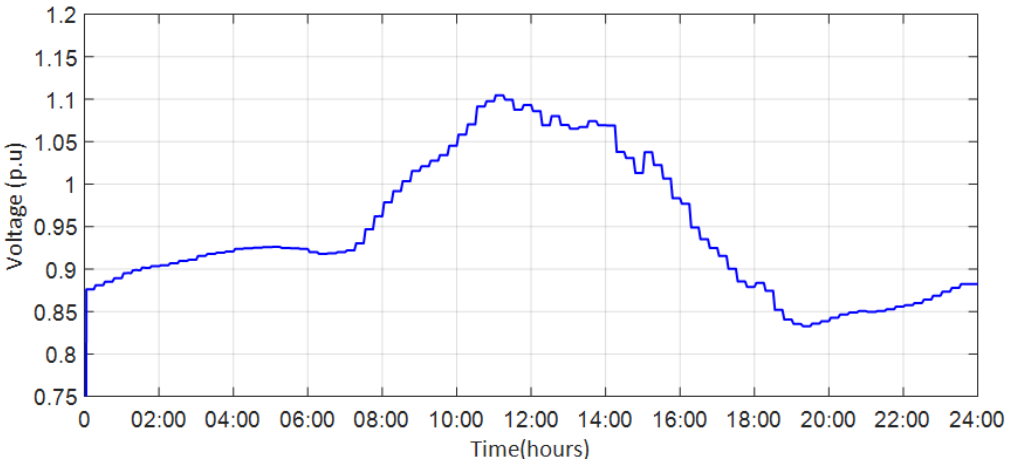

Figure 5.3. Voltage on the Transformer Primary at Bus 890 A without Regulators

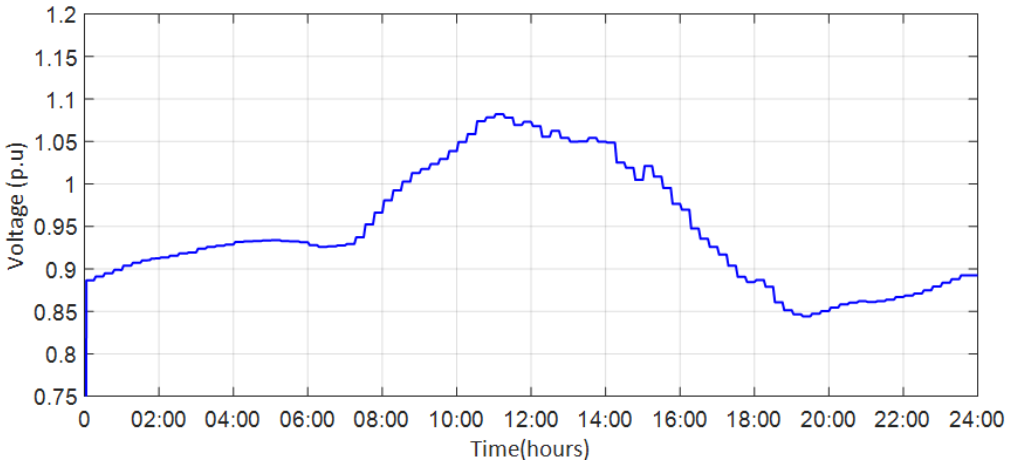

Figure 5.4. Voltage on the Transformer Primary at Bus 890 B without Regulators

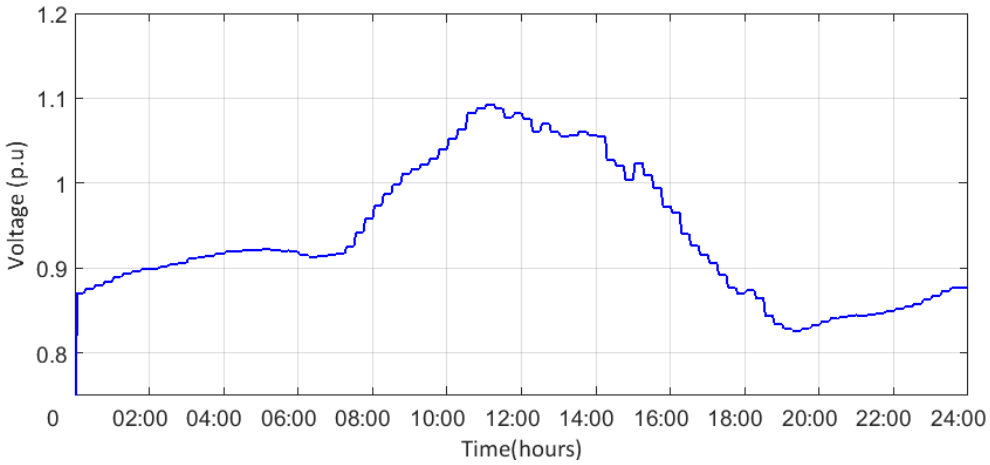

Figure 5.5. Voltage on the Transformer Primary at Bus 890 C without Regulators

The voltage profiles are not within the desired 1.05 pu upper and 0.95 pu lower limits in any phase of node 890. This further makes a case for the use of a SST which ensures nearly 1 pu voltage on the secondary and voltage profile within acceptable limits in its primary. The original IEEE 34 bus distribution system includes two voltage regulators between buses 814 and 850 and between buses 852 and 832. The IEEE PES Distribution System Analysis Subcommittee's Distribution Test Feeder Working Group

provides the regulator data for IEEE 34 Node Test Feeder [10] for the 24.9 kV test feeder, shown in Table 5.1.

Table 5.1. Regulator Data for the Original IEEE 34 Node Test Feeder

Regulator ID:	1		
Line Segment:	814 - 850		
Location:	814		
Phases:	A - B -C		
Connection:	3-Ph,LG		
Monitoring Phase:	A-B-C		
Bandwidth:	2.0 volts		
PT Ratio:	120		
Primary CT Rating:	100		
Compensator Settings:	Ph-A	Ph-B	Ph-C
R - Setting:	2.7	2.7	2.7
X - Setting:	1.6	1.6	1.6
Volltage Level:	122	122	122
Regulator ID:	2		
Line Segment:	852 - 832		
Location:	852		
Phases:	A - B -C		
Connection:	3-Ph,LG		
Monitoring Phase:	A-B-C		
Bandwidth:	2.0 volts		
PT Ratio:	120		
Primary CT Rating:	100		
Compensator Settings:	Ph-A	Ph-B	Ph-C
R - Setting:	2.5	2.5	2.5
X - Setting:	1.5	1.5	1.5
Volltage Level:	124	124	124

In scaling the IEEE 34 Node Test Feeder to a 12.47 kV system, the voltage regulator settings must be changed accordingly while keeping the location of the regulators in the feeder unchanged. A method to model step voltage regulators including calculating the compensator R and X settings provided in [11] is used to evaluate the

original settings and calculate the parameters for the scaled regulator. A regulator is represented as a single-phase two winding transformer with an automatic tap changer to maintain a set voltage at a defined regulation point. The regulation point is the location at which the regulator tries to maintain the set voltage despite a varying load profile. The circuit that automates the tap changes to reach the set voltage level at the regulation point is the compensator. A one-line of typical compensator is shown in Figure 5.6.

A compensator is built such that the voltage across the voltage relay will be a scaled model of the actual voltage at the regulation point. To avoid frequent changes to the transformer tap, a bandwidth is specified. Bandwidth is the voltage band outside of which the tap changes. This is defined as twice the allowed deviation on the set voltage level. In the IEEE 34 Test Feeder, this band is 2 volts on a 120 volt base.

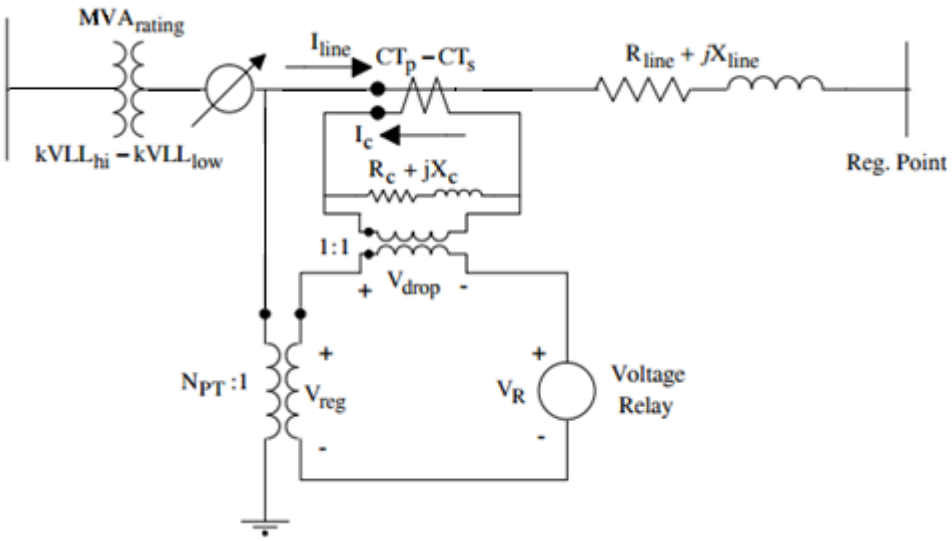

Figure 5.6. Compensator Circuit Representation [11]

The IEEE 34 Node Test Feeder data [10] does not provide additional information of the number of taps available in the regulator used to run the test case. From the test results in the feeder data, the highest tap value recorded is 13 for bus 890 A. It is common for tap changers to possess 33 taps (one center tap) which are ± 16 taps for

raising or lowering the voltage. Each tap changes the voltage by 0.00625 p.u. with ±10% regulator range. With this information, the compensator circuit can be modeled to ensure each tap changes the voltage by 0.75 volts per step for which R and X settings must be determined. The R and X voltage drops (Z_{volts}) to set in the compensator are given by:

$$Z_{volts} = Z_{line} \cdot \frac{CT_p}{N_{PT}} \tag{6}$$

In equation (6), CT_p is the primary rating of the CT, which is 100 A, and N_{PT} is the potential transformer ratio, which is 120 in the original case. Z_{line} is the impedance in ohms at the distance from the regulator intended to be the regulation point. In Table 5.1, since the R and X voltage drop of the compensator is known already, the Z_{line} can be found. The value of Z_{line} is found to be 3.241 + j1.92 ohms for regulator 1. This indicates that the intended regulation point is at an equivalent ohmic value calculated. This is only the impedance seen by the regulation point. It does not represent the value of the line impedance in terms on ohmic positive sequence impedance of the transmission line. This is because the line has laterals tapped and branches. Thereby, between the node where regulator voltage is measured and the intended node (V_{node}), Z_{line} is the equivalent impedance. To get the impedance, current measured from the regulator output is used in equation 7.

$$Z_{line} = \frac{V_{814} - V_{node}}{I_{814}} \tag{7}$$

V_{node} is any node downstream the regulator at the end of Z_{line} the voltage at a node that is intended as a regulation point for regulator 1. Voltage setting 122 (on a 120 volt base) from Table 5.1 indicates the voltage set point requested at Vnode is 1.017 p.u. With Z_{line} in ohms known, the R and X settings in volts can be found from the equation (7). The compensator in the Figure 5.6 has R and X whose value in ohms from $Z_{comp(volts)}$ is given by equation 8, where CT_s is the value of the secondary rating of the current transformer.

$$Z_{comp(ohms)} = \frac{Z_{comp(volts)}}{CT_s} \tag{8}$$

For the regulator at node 832, the R and X settings are found in the similar manner but in the scaled system, the dynamics of the system change with the introduction of PV injection. While the above illustration of a step-by-step approach can be used to calculate the intended location and settings, an empirical approach combined with the procedure illustrated can be used to finalize the regulator settings in the scaled system.

5.3. VOLTAGE REGULATOR SETTINGS AND BUS VOLTAGE PROFILES

For both regulators, the primary CT rating and PT ratio are the same and scaled according to the scaling of the system. In this case, with the halving of the voltage and maintaining a constant load, the PT ratio is also halved in order to get 120 volts at the secondary of the PT when 1 pu voltage is present on the regulator bus. Similarly, the CT primary current is doubled to serve the same load at half the voltage. With these settings configured, the location of the first regulator from the IEEE 34 feeder data is line segment 814-850. While the location of regulators can be changed and calculated based on [11], the intention is to study the impact of transformer with PV injection when they are used in the IEEE 34 bus system with its voltage regulators intact. Thus, the steps to calculate the node to install the regulator is skipped for this case. For the first regulator at location 814-850, the voltage set point needs to be determined. Since a second a regulator is also present at node 852, the node of concern downstream of the first regulator is node 822 A since it has PV injection. Nodes 806 C and 810 B are upstream of the regulator and node 890 is downstream of the second regulator. Therefore, a voltage set point that regulates voltages at load buses up to node 822 A is needed. Initially R and X settings are set to zero, with a voltage set point of 126 volts. This yielded overvoltages in node 822 A. Reducing the set point to 121 volts yields a favorable voltage profile at all nodes up to and including node 822 A. Since the downstream voltages up to 822 A do not drop below 0.95 volts, a remote regulation point is not required, i.e. R and X can remain at zero for the Regulator 1. If remote regulation point is to be used, new R and X settings for the compensator must be found. This

requires the selection of voltages for equation (7) which is a greater challenge than seen in [11] since voltage profile in this case varies greatly over time.

5.3.1. Voltage Regulator Settings for Regulator 2. The second regulator in the segment 852-832 must be configured to support the 4.16 kV line segment with the transformer, which makes voltage support for the node 890 critical. Before the second regulator is added, the node 890 voltages are well beyond acceptable limits, while other load buses without PV injection hover close to the accepted limits. To gauge the requirement of a regulation point, the set point voltage of the second regulator is set to 126 volts with R and X set to zero ohms initially. The results of the load flow indicate the voltages in phase 890 are beyond 1.05 and 0.95 limits. The long line, coupled with 12.47:4.16 kV transformer section and large variation in load with PV contribute to the wide variation in voltage. In order to regulate at node 890, the equivalent impedance from the regulator location and bus 890 must be found.

$$Z_{line} = \frac{V_{852} - V_{890}}{I_{852}} \tag{9}$$

However, the RMS voltage and currents are not constant over the time period in any node. The approach used in this thesis is to select a time, t_{reg} in the voltage profile that warrants regulation based on its magnitude. The voltage and current required for equation 9 are then noted for the same time t_{reg}. For regulating node 890, it is seen that the voltage goes well beyond 1.05 and is highest around 11:00 hours. This is a point of high PV injection with very low loading and the time corresponding to it is taken as t_{reg} for this case. Z_{line} is found using the voltages and current at t_{reg} for all three phases. It must be noted that in addition to the voltage and current at t_{reg}, phase angle is also necessary since solution is required for the complex value of Z_{line}. The average from all three phases is used so all phases can have the same R and X settings. However, any variation in the voltage profiles due to the unbalance between phases is compensated with the taps, which automatically change to different positions. The value of Z_{line} is 4.23 + j2.54716 Ω. Z_{volts} can be found using equation 6 and the R and X settings in ohms needed for the compensator is found using equation 8. The value of R and X in ohms is

70.3 and 42.45 ohms (0.1126 H). However, even with regulation point set to see node 890, the voltage profile is not within acceptable limits of 0.95 and 1.05 p.u. This is because the regulator hits the tap limit of 16 during very high load periods. Installing static shunt capacitors on 890 does not provide acceptable voltage profile. Since the voltage profile at points of low load and high PV injection are exacerbated with the addition of a static capacitor, large capacitor cannot be chosen. Therefore, if the transformers are present in the system with only two regulators, the node 890 will not be regulated within acceptable limits.

To regulate bus voltages at 890, the solution is to add a third voltage regulator in the section between 888 and 890 at the output of the transformer in the section 832-888 [11]. Since the third regulator has to be added to regulate node 890, the R and X settings for the existing regulator 2 are reset to zero so as to not see the remote regulation point. A value of set point voltage at 1 p.u or greater that keeps the bus voltages below 1.05 is chosen. A set point of 122 volts (1.0166 p.u) is requested. This setting is verified to provide an acceptable voltage profile at all nodes downstream the regulator, with the exception of 890, and this value is chosen after studying the effect of excess PV from 890 causing overvoltage in other nodes.

5.3.2. Adding the Third Voltage Regulator. Since the third regulator is present to regulate node 890, the impedance to the remote point is only the positive sequence impedance up to the node 890 [11]. The third regulator is added at the 4.16 kV side of the transformer and the potential transformer (PT) ratio is changed to:

$$PTratio = \frac{(4.16kv/\sqrt{3})}{120} \approx 20 \tag{10}$$

A PT ratio of 20 will yield a secondary voltage of 120 on the potential transformer to provide set point on a 120-volt base. The current transformer ratio can remain the same for the purposes of simulation as it will not affect the R and X setting in volts. However, it must be ensured that the value of CT_s in equation 8 corresponds to the correct CT ratio used in the PSCAD model of compensator. The positive sequence impedance of the section is 2.24 + j1.876 Ω. With the PT ratio and CT primary rating

known, the R and X settings in volts are 22.4 + j18.76 volts. The R and X settings in ohms for the compensator are 112 + j93.8 Ω (0.2488 H). For this case, the voltages at the primary of bus 890 are well within the acceptable limits. With this regulator, all the buses are within the acceptable limit. The result of adding the third regulator is shown for the primary of node 890 from Figure 5.7 to Figure 5.9.

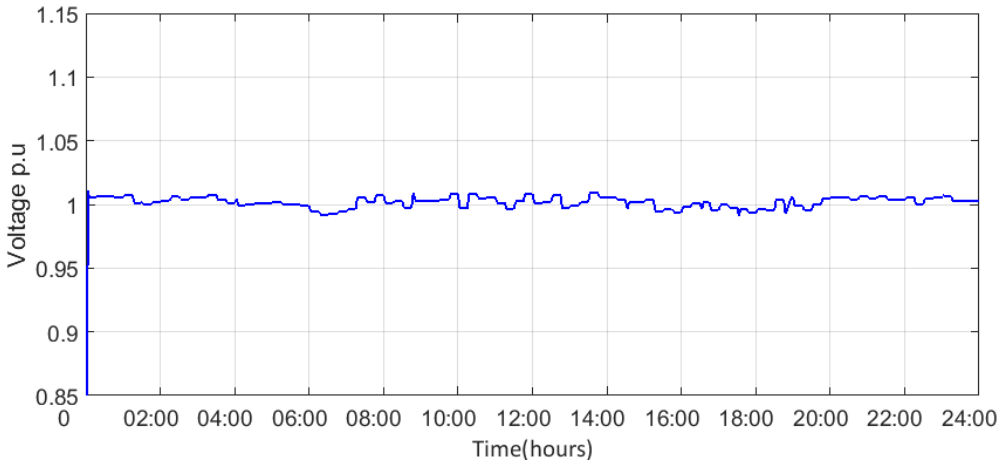

Figure 5.7. Voltage in Transformer Primary of Node 890 A after Regulation

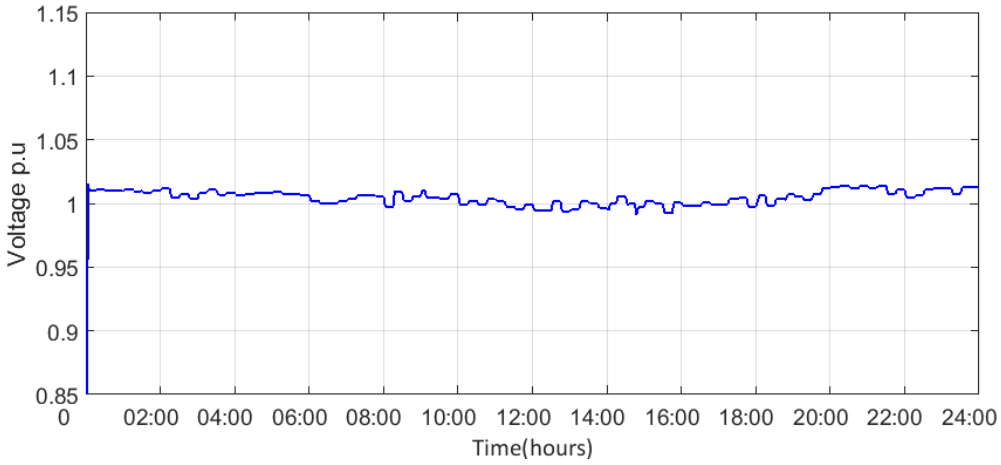

Figure 5.8. Voltage in Transformer Primary of Node 890 B after Regulation

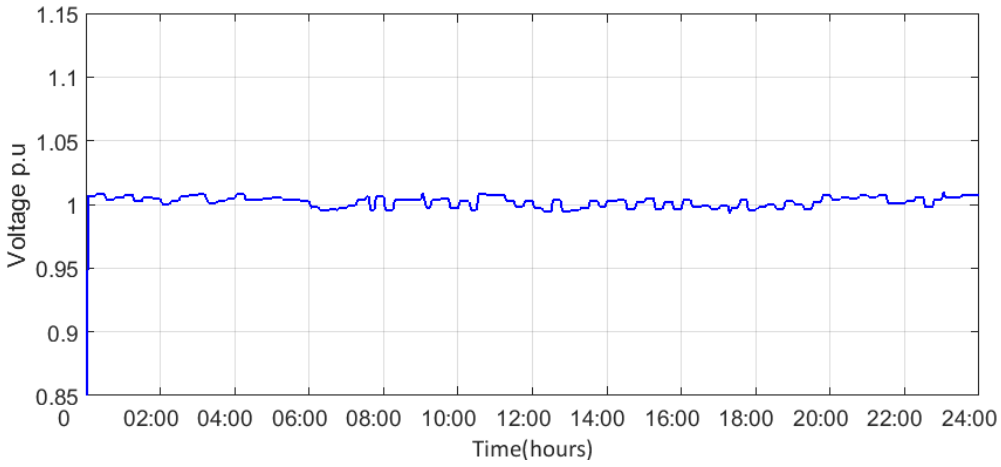

Figure 5.9. Voltage in Transformer Primary of Node 890 C after Regulation

The action of tap changing in the regulator ensured that the voltage was as close to the set point voltage at 1 p.u at the remote regulation point, which in the case above was the bus 890. The discrete tap changing varies the voltage varies widely to ensure the voltage at the bus 890 (the remote set point location) is at its set point voltage. Figure 5.10 shows the action of tap changing that takes place in discrete steps in order to achieve voltage profile in Figure 5.7. Each tap changes the voltage the regulation point by 0.00625 p.u, with the 15^{th} tap depicting a change of 0.09375 p.u to achieve the desired set point voltage. The voltage regulator however cannot maintain the load power factor close to unity, and the substation supplies the VARs needed by all loads. This leads to line and equipment losses as the total current drawn from the substation is higher. This is evident from the total active and reactive power seen at the substation in Figure 5.11. For comparison, the power reactive power drawn is seen in Figure 4.6 for the unity power factor mode of SST while achieving a load voltage of nearly 1 p.u. In var control mode, the SST is commanded to handle reactive power, as observed through Figure 4.10, to keep voltage within limits on the bus.

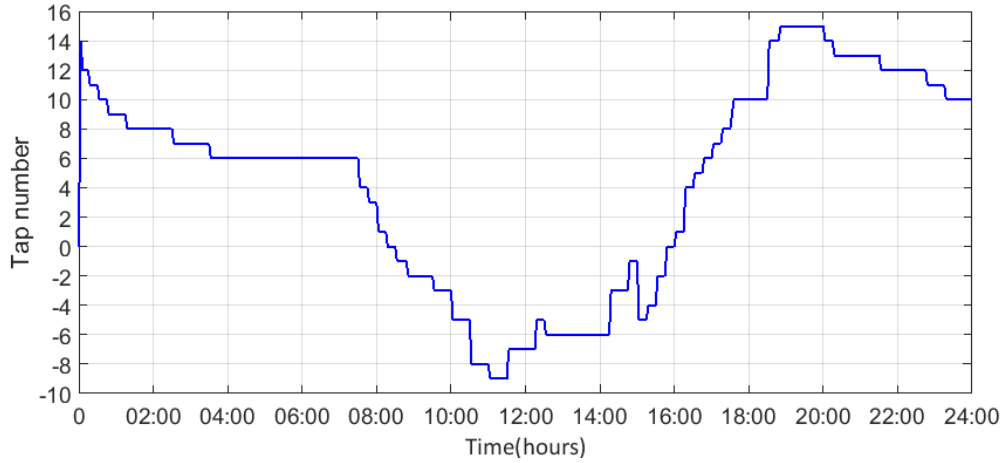

Figure 5.10. Tap Positions in Phase A of Third Regulator in Section 888-890

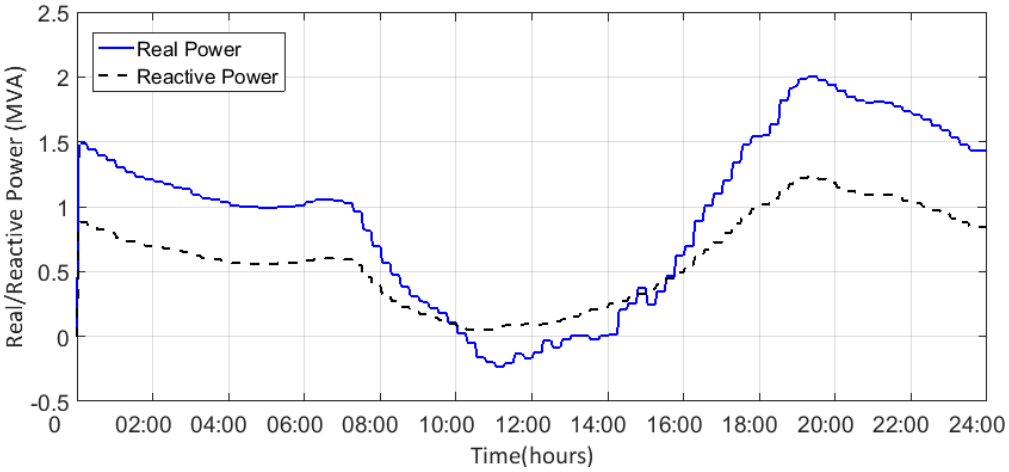

Figure 5.11. Total Power Seen at the Substation

6. BEYOND 100% PV PENETRATION

In the previous sections, 100% PV penetration was demonstrated on four pilot buses in solid state transformer and conventional transformers. With solid state transformers rated at 200 kVA, there is a potential to increase the PV power injected in these four buses. The increased penetration will yield lesser active power drawn from the system, thereby rendering lesser voltage drops. The impact of lower load periods with high PV injection periods is overvoltage. However, the SST has the capability to inject or absorb the reactive power with a constraint to ensure the total power in the SST is within its rating. The volt-var control on the SST is tested for PV penetration at 125% and 150% higher than the total load at the particular node with PV injection. The same penetration levels are then compared with conventional transformers with regulators.

6.1. SOLID STATE TRANSFORMERS WITH 125% AND 150% PV INJECTION

With respect to PV penetration levels, a value beyond 100% refers to the installed capacity of photovoltaic system. Even with 100% PV penetration, the insolation profile yields maximum active power close to 90% of the PV array's capacity. This is further reduced when the averaged models of the PV subsystem are modeled with losses which are in the range of 3 to 5 percent. In any case, more than 100% net PV power is seen by the SST and its ability to regulate voltage and rating adequacy is studied.

6.1.1. SST with Increased PV Injection from DC Bus. The buses with PV injection are commanded for increased by 25% and then by 50%. The larger impact on increasing the PV injection is seen at the period when load levels are lower. To manage the overvoltage during this period, the DQDV algorithm will command the SST to absorb reactive power necessary to keep the voltage from exceeding 1.05 p.u. Bus 822 and 890 are observed carefully when PV injection is close to the SST kVA ratings. Initial run of the test case with 125% injection triggered voltage distortion in the higher loading period. The effect of voltage distortion is seen in all buses, but more significantly in bus 890. The system was for checked for any limits, controller instability and PV scaling issues and the case is rerun. The issue persisted and more parameters were observed. It was seen that the reactive power injection at each phase of nodes 890 were incessant at the

same time period of voltage distortion. It was noted that to serve the SSTs, which have a 7.2 kV primary voltage rating, a transformer is introduced that steps up 2.14 kV (4.16 kv-three phase) of the IEEE 34 bus feeder system transformer to 7.2 kV. Since the transformer introduced is not present in the original case, the transformer leakage reactance was taken below 0.01 p.u and losses were set zero. This resulted in numerical instability when solving the power flow. The PSCAD program is able to override this numerical instability in the 100% PV penetration cases, but at 125% and 150%, the combination of high PV and dynamically changing voltage leads to voltage distortion. This is corrected when the leakage reactance of the transformer introduced is given a significant value of 4% on its own base with total losses of 1.2% [12]. The result after correcting the reactance with 150% PV penetration is shown from Figure 6.1 to 6.3 for voltage profile at bus 890 for all three phases. Prior results in the 100% case were also shown for the same transformer parameters.

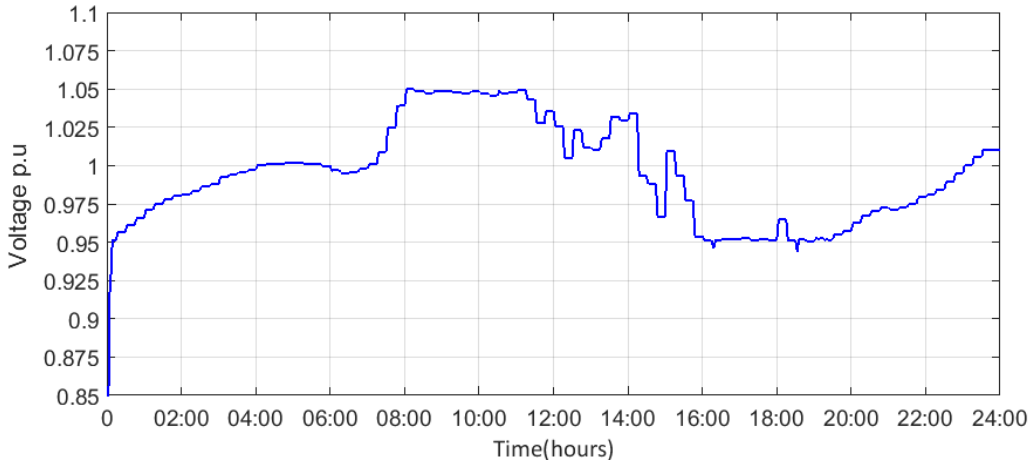

Figure 6.1. Voltage in Primary of Node 890 A with 150% PV and VVC

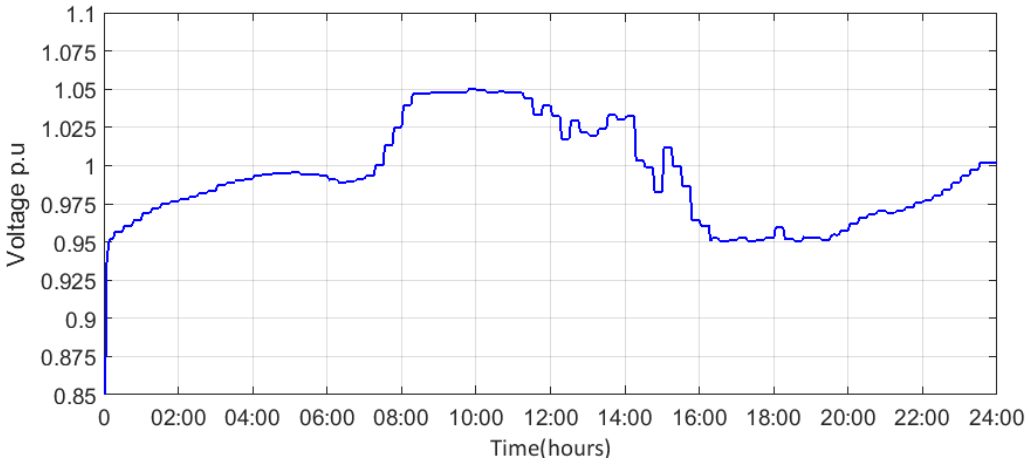

Figure 6.2. Voltage in Primary of Node 890 B with 150% PV and VVC

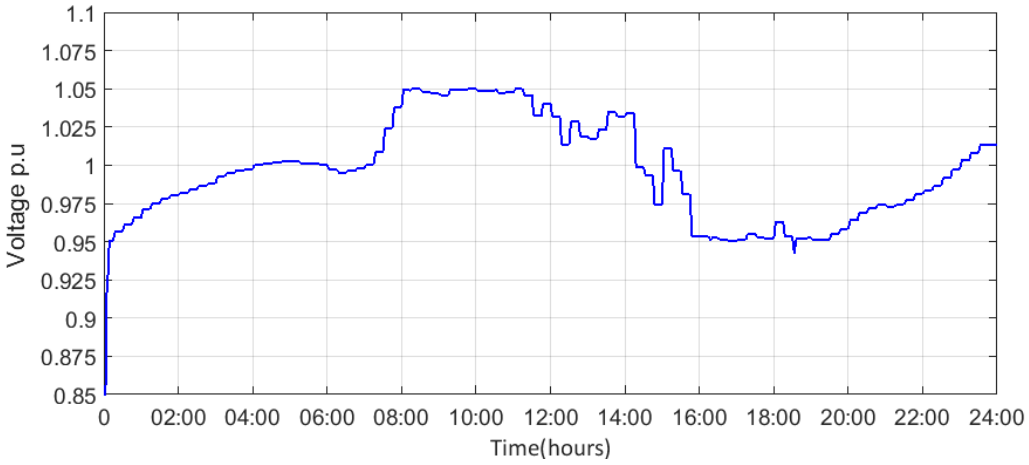

Figure 6.3. Voltage in Primary of Node 890 C with 150% PV and VVC

The voltage profile at 125% PV penetration is also within acceptable limits. It is seen that the voltage profiles are similar to the 100% injection case where voltages are within the acceptable limits. An appreciable difference in case of high PV injection is observed through Figure 6.4 where the total active the substation are shown. While the voltage profiles are similar to the 100% injection case, the total active power sent back to the substation is higher with higher PV injection. Higher PV injection at periods of lower loads is also handled effectively by the SST. In this case, the SST has to absorb greater

amount of reactive power as high PV power injected yields lower line voltage drop and will cause voltage to swell. The SST will thus absorb more reactive power during this period to keep voltage within the 1.05 upper limit. This is seen in Figure 6.5, where with higher PV injection the reactive power absorbed is increased.

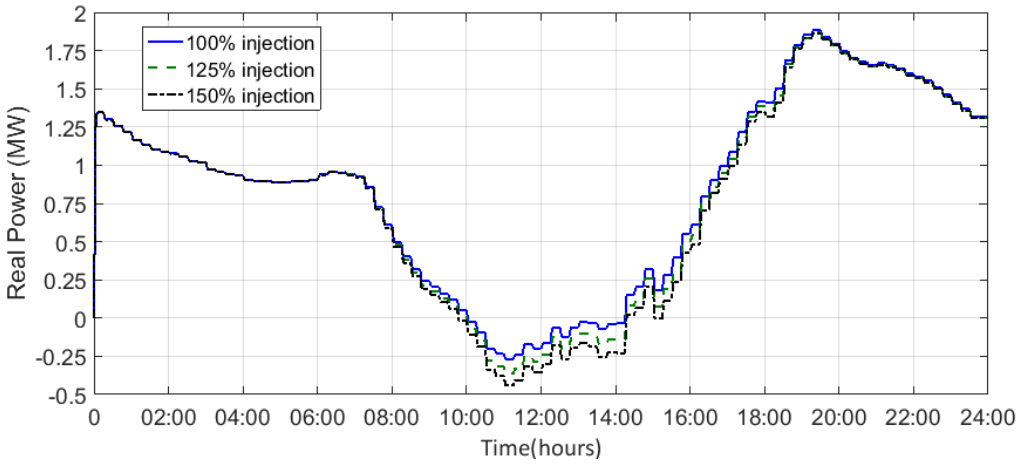

Figure 6.4. Active Power at the Substation

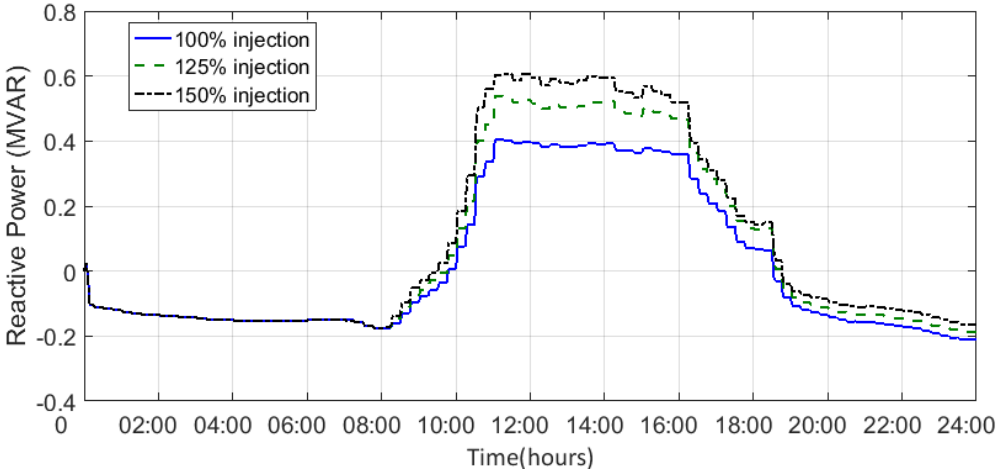

Figure 6.5. Reactive Power at the Substation

Since total power seen at the substation is increased, it is important to realize that each SST with volt-var control will deliver/absorb greater reactive power individually. Therefore, it must be ensured that even with excess PV injection, the SST does not exceed its kVA rating. It is during period of high PV that active power consumption is low. This works in favor of the SST which needs to absorb greater reactive power at this stage, still allowing the SST power handled to remain within its rating. Figure 6.6 shows the SST at 890 A with varying PV injection.

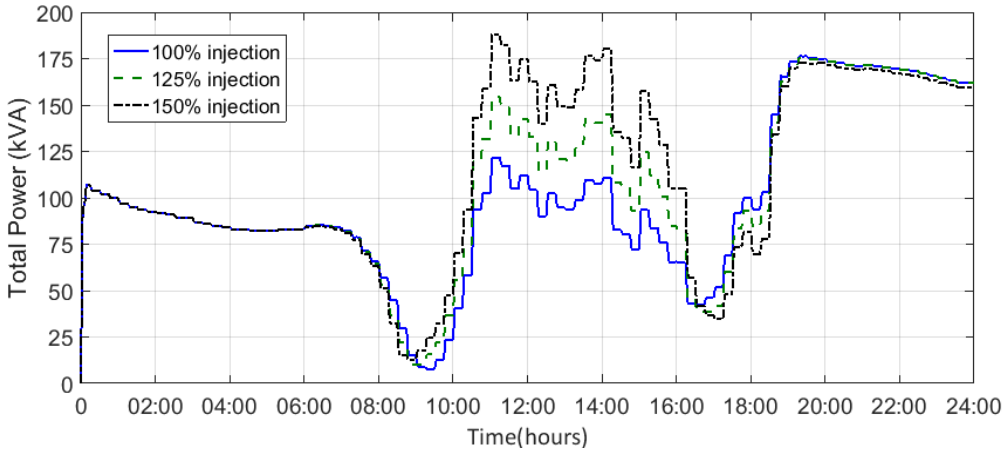

Figure 6.6. Total Power at 890 A SST

6.1.2. SST with Increased PV Injection from AC Bus. With the successful demonstration of 100% PV injection in the AC side of the SST, 125% and 150% are also achieved. In this case, the inverter and SST settings remain unchanged from the 100% case. As observed with DC injection, a distortion appeared in the voltage waveform of bus 890 and is similarly attributed to numerical instability caused by very low leakage reactance setting of the transformer. The results of power flow indicate the successful integration of PV with increased capacity on the AC side of the SST. The voltage profiles shown for bus 890 from Figure 6.7 to 6.9 are within the acceptable voltage limits. Other phenomena such as the increased reactive power handling during the period of low load and higher PV are similar to the DC side injection. Therefore, the SST delivers

performance while remaining within its rated capacity and also validates the case for the PV inverter's seamless integration.

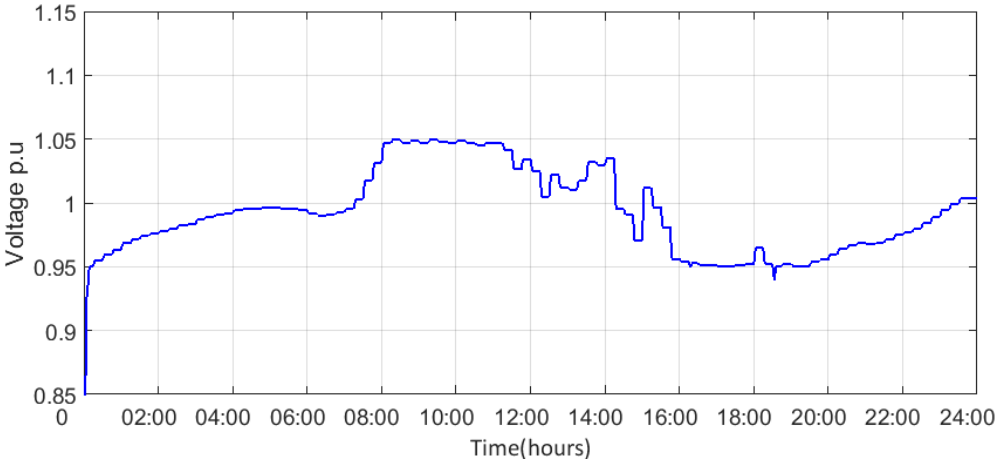

Figure 6.7. Voltage in Primary of Node 890 A with 150% PV on AC Side

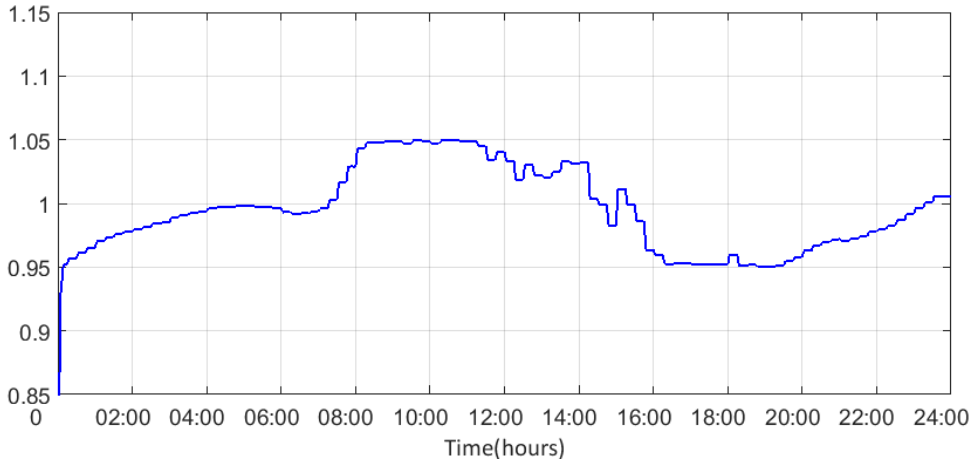

Figure 6.8. Voltage in Primary of Node 890 B with 150% PV on AC Side

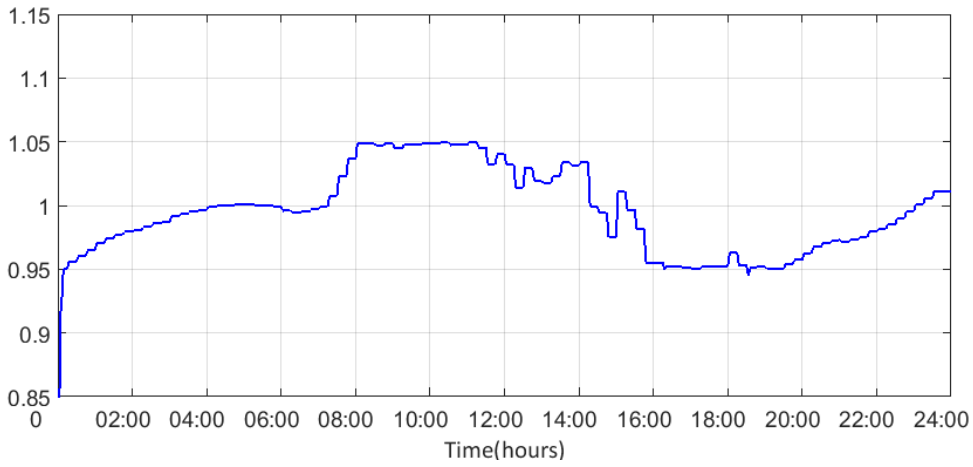

Figure 6.9. Voltage in Primary of Node 890 C with 150% PV on AC Side

6.2. CONVENTIONAL TRANSFORMERS WITH 125% AND 150% PV INJECTION

With conventional transformers, it was observed that three regulators were needed to regulate voltage at all nodes within acceptable limits with 100% PV penetration. It is good practice to ensure that the same compensator settings and device location are able to regulate the voltage even with higher PV penetration. This was taken into consideration while working out the settings in the earlier section. Hence, shunt capacitors were avoided, as PV penetration rendered overvoltage that needed to be corrected with regulators. With the third regulator, the system does not reach tap limit, which occurs in the case with only two regulators. It is seen that the voltage profiles are within acceptable limits with 125% and 150% penetration with three regulators. The results are shown for the more limiting case, i.e. 150% PV penetration for node 890 from Figure 6.10 to Figure 6.12. The voltages brought within the acceptable range by means of the third regulator closely follow the 100% PV penetration case. The difference in the cases are prominent in the position of taps seen in Figure 6.13. In this case, during higher penetration, the range of tap changes are higher because of the increased overvoltage magnitudes, compared to the tap positions in Figure 5.10 for the 100% PV penetration case. In the case of higher PV penetration, there is negligible change in total reactive power between 100% and 150% PV penetration case, with active power sent to the

substation increasing, as seen in Figure 6.14. Overall, the reactive power drawn with conventional transformers in the system is higher compared to SST in its unity power factor mode. In var control mode, the reactive power is absorbed and injected as voltage exceeds the upper limit and lower limits respectively.

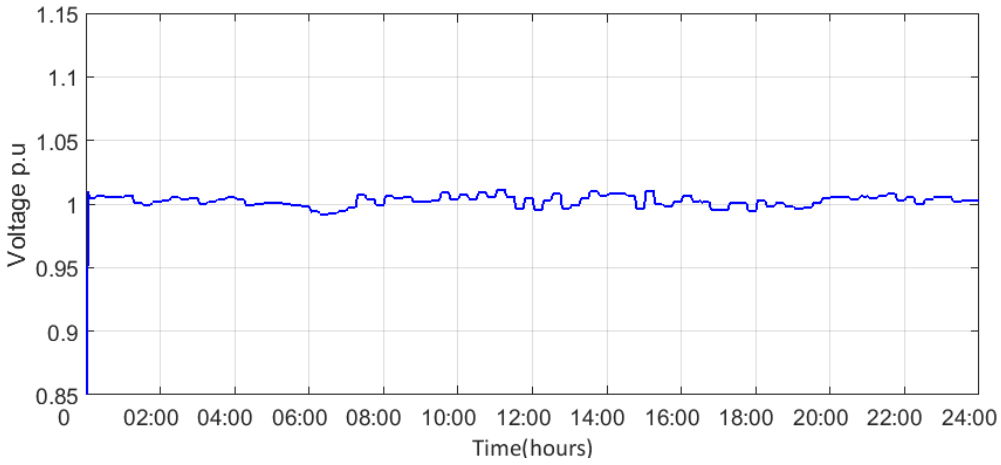

Figure 6.10. Voltage in Primary of Node 890 A with 150% PV and Regulators

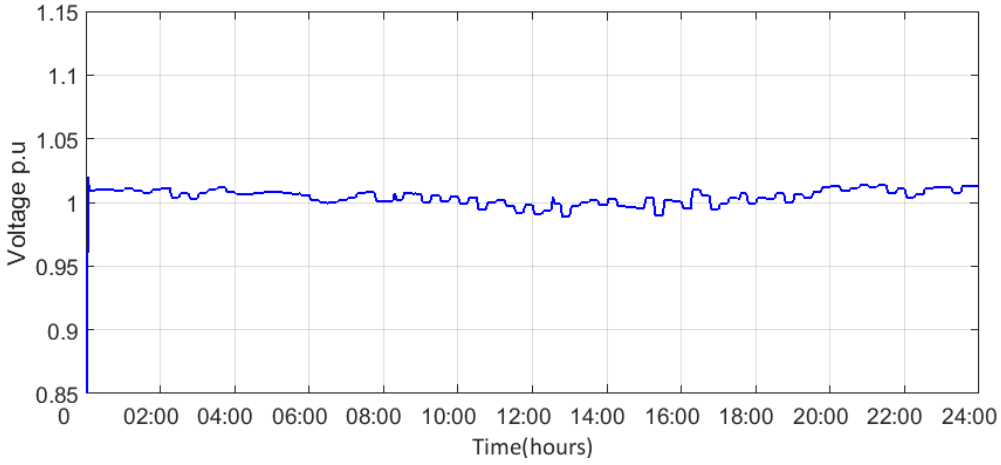

Figure 6.11. Voltage in Primary of Node 890 B with 150% PV and Regulators

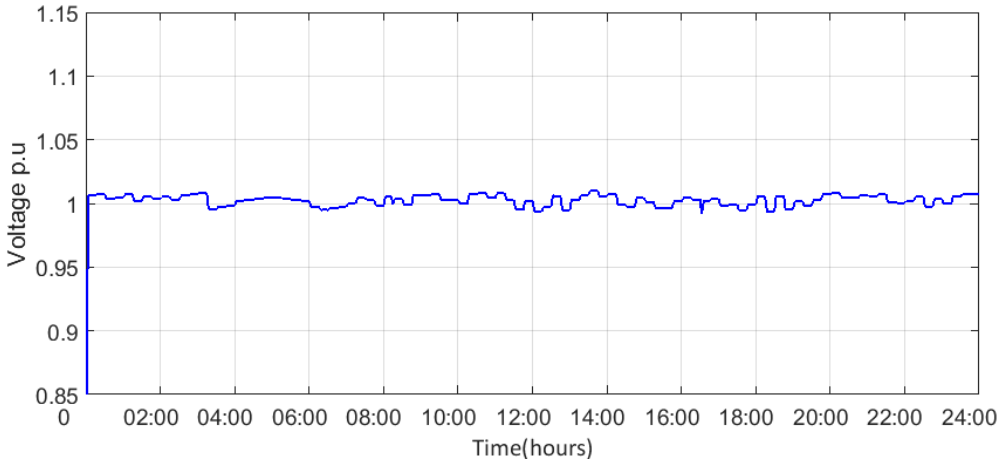

Figure 6.12. Voltage in Primary of Node 890 C with 150% PV and Regulators

The conventional transformer's reactive power profile is largely unaffected by PV penetration as it does not compensate overvoltage or undervoltage. The reactive power profile is a function of the load power factor and equipment, such as lines and transformers. Thus, the conventional transformer does not offer the flexibility in terms of voltage regulation as demonstrated by the various modes of operation in solid state transformers.

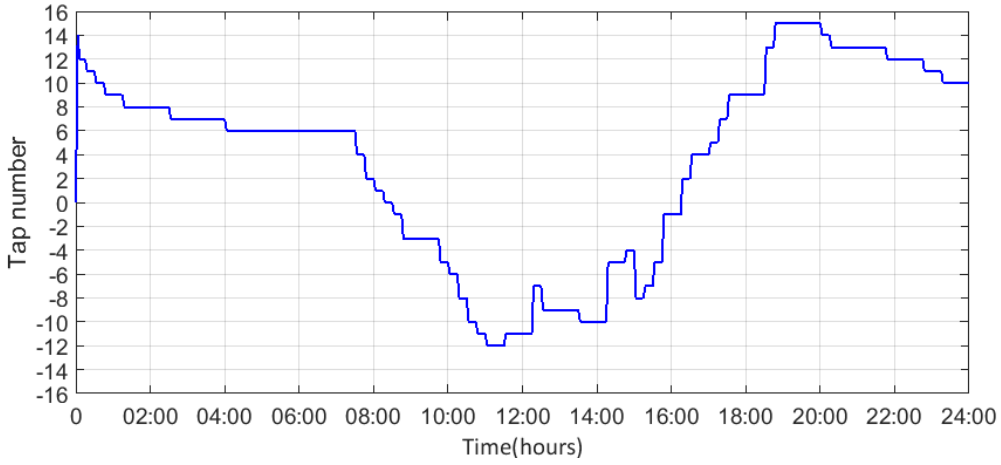

Figure 6.13. Tap Positions for 150% PV Penetration Case with Transformers

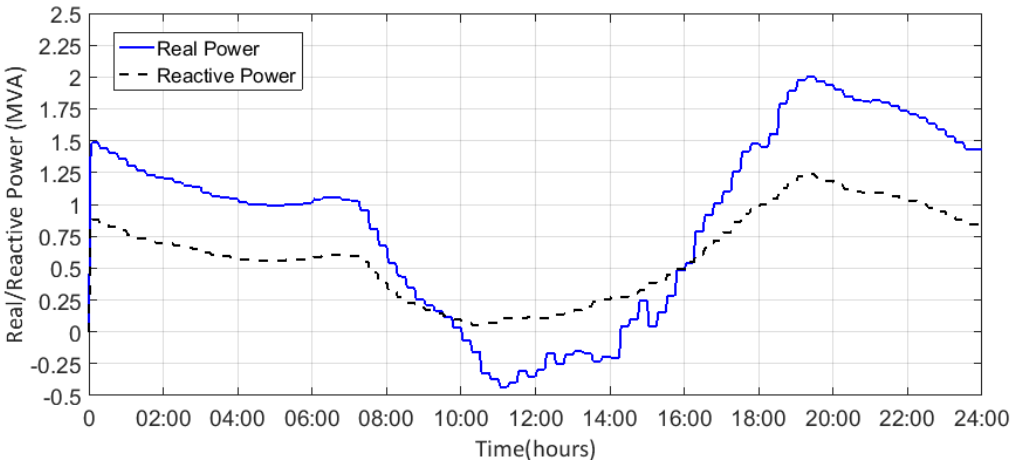

Figure 6.14. Total Power at the Substation with 150% PV Penetration with Transformers

7. CONCLUSION

This research dealt with the comparison of solid state transformer performance in var control and unity power factor mode with both AC and DC side photovoltaic power injection. Seamless AC side PV integration demonstrates the flexibility of the solid state transformer as performance is comparable to DC side integration. The two cases were compared against the performance of conventional transformers in the same system. To achieve the desired voltage limits between 0.95 and 1.05 per unit bus voltage, the conventional system required the operation of three voltage regulators in the IEEE 34 bus test system. Even with voltage regulation, it was observed that the total power, and hence losses, in the system were higher with conventional transformers when compared to the SST in unity power factor or var control modes. The SST is tested to its limits with photovoltaic penetration beyond 100% and it was compared against the transformer case. In future, the capability of the PV inverter integrated to the transformer can be explored to provide var capability, to provide a comparison against the SST's own reactive power capabilities.

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VITA

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