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Forward converter for solar power applications

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FORWARD CONVERTER FOR SOLAR POWER APPLICATIONS

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ABSTRACT

Most solar arrays used today are connected in series and have tremendous power losses in partially shaded conditions. This document explores photovoltaic arrays in a parallel connection to reduce the power losses in other solar cell connected applications. The two main issues with any photovoltaic arrays are solar modules being shaded and the efficiency of the power converters used within the solar array. This thesis concentrates on alleviating these problems with the development of a two phase dc to dc forward converter with a snubber circuit as well as connecting a solar array in parallel to increase the performance in partially shaded conditions. This work illustrates a fully functional forward converter that boost the input voltage within a solar array. The experiments include efficiency tests at certain voltage within the specifications as well as outdoor solar testing in sunny and partially shaded conditions. These tests illustrate that in a parallel connected array, the shaded solar module does not have a dominating effect on the overall output power of the combination, but rather the converter's efficiency is the main factor of the performance of the array.

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NOMENCLATURE

Symbol	Description
K_e	Electrical coefficient
K_g	Core geometry
J	Current Density
ε	Skin Depth
A_w	Bare wire area
N_P	Primary Number of turns
I_P	Primary RMS Current
A_{wp}	Primary bare wire Area
NS_P	Primary Strands used
R_p	Resistance in primary wire
P_P	Copper loss in primary
N_S	Number of secondary turns
I_s	Secondary RMS current
A_{ws}	Secondary bare wire area
NS_s	Secondary Strands used
R_s	Secondary wire resistance
P_S	Copper loss in secondary
P_{cu}	Copper loss in primary and secondary
α	Transformer Regulation
N_T	Number of tertiary turns
L_T	Inductance in tertiary winding
I_T	Tertiary winding current
I_{Trms}	Tertiary winding RMS current

A_w	Wire area of tertiary winding
K_u	Window utilization
P_{fe}	Transformer core loss
P_Σ	Total transformer DC loss
ψ	Watts per unit area
T_r	Calculate Temperature Rise
PV	Photovoltaic
D	Duty Ratio
V_{In}	Input Voltage
V_{Out}	Output Voltage
V_{SMax}	Maximum Switching Voltage
n	Number of phases
I_{Out}	Output Current
I_{In}	Input Current
V_L	Output Inductor Voltage
I_C	Output Capacitor Current
ΔI	Change in Output Current
ΔV	Change in Output Voltage
IPOS	Input Parallel Output Series
A_e	Cross-sectional Area of the Transformer

1. INTRODUCTION

1.1 MOTIVATION

As fossil fuels constantly decrease due to extraction and overuse alternative energy sources such as solar power are becoming more important [1, 2]. At the end of the year 2000 the total installed capacity of photovoltaic (PV) systems worldwide was approximately 1200 MWp and increased to 6500 MWp six years later, which is an average annual growth rate of more than 35% [3]. Solar energy is also predicted to have a massive impact on supplying electrical power and providing the most electrical power of all other renewable energy sources by 2040 due to its limitless energy source [4]. Although this prediction may be true one of the main hindrances of PV arrays is operation during partial shaded conditions [5]. In a series connected array configuration, a single cell that is partially shaded will cause a decrease in power among the entire array [6] leading to fully functional solar panels operating at a fraction of their optimal capability, and reducing the solar-electric conversion efficiency throughout the solar array. To counteract this issue, this thesis presents a parallel-connected array topology, where the power loss affects only the shaded module rather than the entire array [6]. This is one alternative to increase the efficiency of the overall photovoltaic system.

Another important element in obtaining an efficient solar array is developing an effective power converter to boost each solar panel's voltage. In most grid solar applications, a simple boost converter is unable to perform at high efficiency due to large current ripples in the power devices causing an increase in the device's conduction losses [7]. Also, the voltage stress of the switches and diodes in the boost converter are equal to

the output voltage, thus multiplying component cost in the circuit [7]. Therefore, this document investigates a new type of forward converter topology that was designed and developed by harmonizing different types of strategies for increasing forward converter efficiency. The work presented in this thesis provides a better process of creating a higher efficiency photovoltaic array and power converter.

1.2 SOLAR ARRAY OVERVIEW

Many applications for solar arrays have been and are being developed to tackle the energy issues in today's society. A large portion of solar array research deals with the use of solar energy for grid type of applications. In some instances, grid application algorithms for maximum power point tracking (MPPT) like the work done in [8] are used to facilitate optimal solar array operation. In others, the goal is to develop a smart grid system which enables a customer to manage energy consumption, use plug-and-generate and plug-and-store energy devices are areas that systems like the Future Renewable Electric Energy Delivery and Management (FREEDM) cover [9]. The FREEDM system uses a 400 V DC bus that allows for an alternative interface for PV converters providing advantageous results such as the PV converter controller does not need a current regulator nor a phase lock loop and the converter can be encompassed of a single power stage [9].

Other types of PV systems are developed as stand-alone system which usually consist of a PV module, a system controller, a high step up converter, an active sun tracker, an inverter, and an output load [10]. In most cases a stand-alone PV system will have a battery pack for energy storage [3, 11] to allow a system to be operational during

times of little or no sunlight. In applications with battery storage the power converter's main focus is to charge the battery(s) but can also be used for MPPT [11]. The plethora of solar panel functions demonstrates the importance in on or off the grid applications. This allows the ideas researched in both applications to be interchanged to create an efficient PV system.

The two elements of a PV energy system that can cause the most efficiency problems are the step up converter and inverter. A step up converter is needed in a PV system because the voltage of a photovoltaic module is relatively low and performance of a module can deteriorate easily when the module is inactive [10]. Similar to the step-up converter the inverter must be at a high efficiency to allow maximum power gain for the PV system. In most instances, inverters can be purchase with a 95% efficiency rating and some companies even promote transformer-less inverters at 98% efficiency [3]. Since transformers cause approximately 3%-5% power loss alone in addition to a weight and cost increase in an inverter [3], special attention must be given to the power converter to ensure an efficient PV array.

The most common connection for photovoltaic arrays is in a series connection also know as a string which can be seen in Figure 1.1 [2].

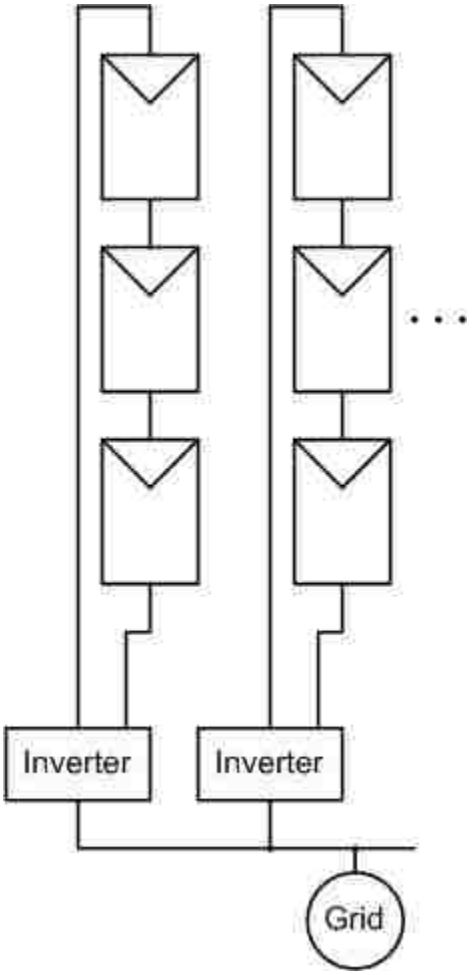

Figure 1.1 Photovoltaic modules in series strings [6]

The strings are used because of the ability to obtain high voltages but the greatest drawback of the string is partial shading issues [2, 6]. This shading is especially seen in urban areas [7], which would otherwise be excellent places to install solar arrays. Another type of connection for the solar modules is to connect the panels in parallel and series, seen in Figure 1.2, obtaining a high-power and high-voltage capacity [2].

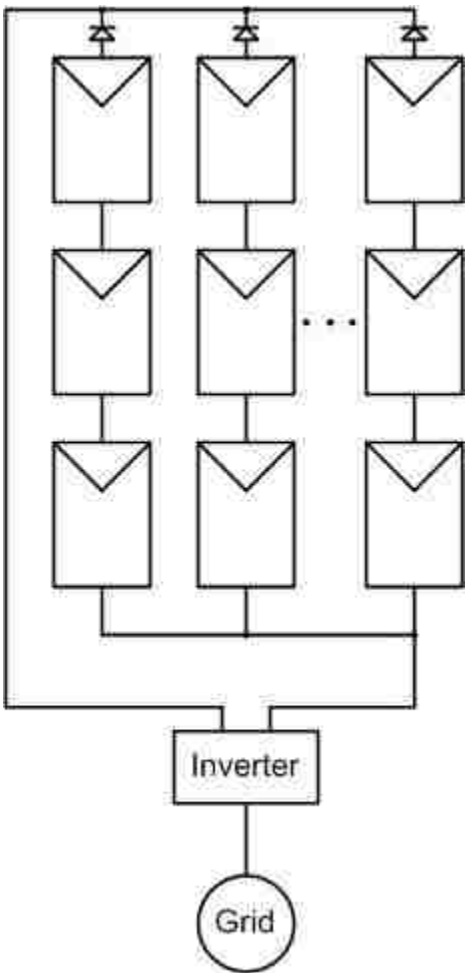

Figure 1.2 Photovoltaic arrays in parallel and series [6]

The downside to this type of connection is low efficiency of PV mutual influences and extra diodes in each string, partial shading issues, and high DC voltage cables [2]. The final type of connection is connecting the modules in parallel which can be found in Figure 1.3.

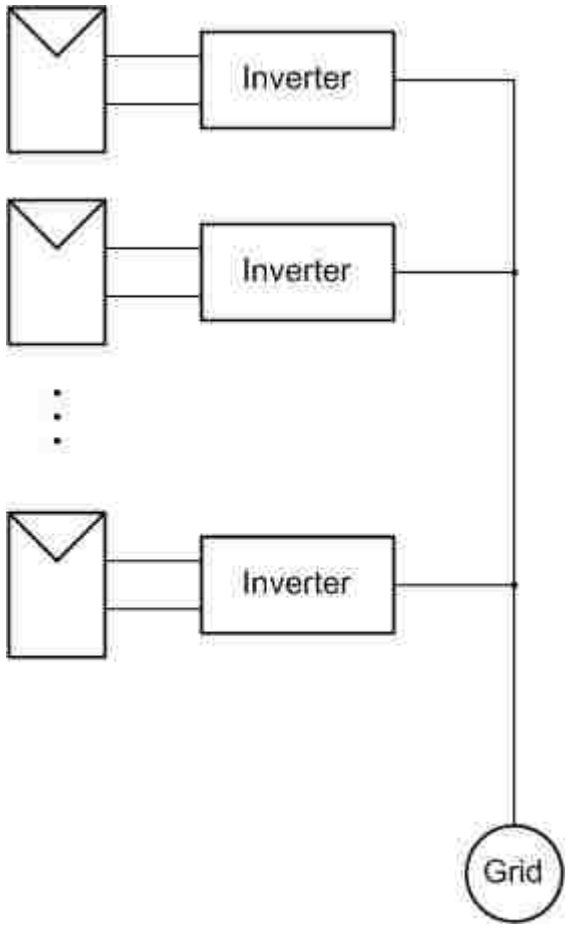

Figure 1.3 Photovoltaic arrays in parallel [6]

This configuration is the best for shaded conditions among the three described because each module is treated as its own unit and shading one particular unit will not propagate throughout the entire PV system [6]. However, the use of a highly-complex inverter on each panel can lead to high cost and low efficiency.

1.3 FORWARD CONVERTER

New power converter topologies for solar cell applications are created to enhance the efficiency of the solar arrays such as the work done in [1]. Even converters as simple

as a boost converter can be applied to solar cell arrays similar to the experiment in [12]. In particular, the forward converter is a well-known and useful topology that can successfully be employed in medium to low power converters. The forward converter is most similar to a buck converter and traditionally has a transformer to step-down the voltage in a circuit. It is an ideal converter for use for multiple outputs for applications such as a personal computer [13]. Depending on the transformer ratios, the forward converter can also boost the voltage of a circuit while maintaining the simple and relatively uncomplicated design. These qualities of the converter allow vast usage in different power boosting or bucking scenarios [14]. Figure 1.4 below illustrates a practical forward converter topology with turn ratios.

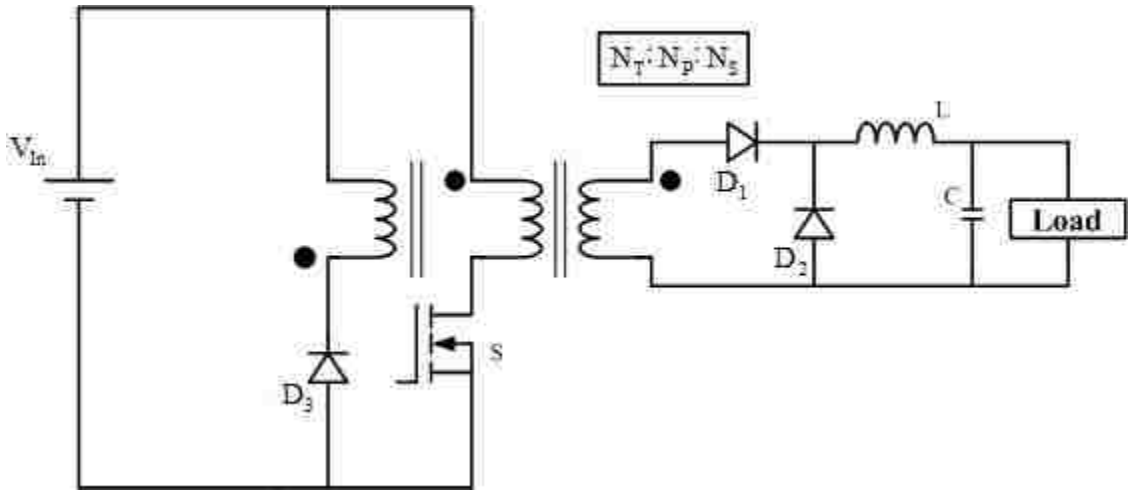

Figure 1.4 Practical forward converter [15]

Assuming ideal conditions, in the first mode of the converter the switch S is turned on and the primary winding is connected to the input voltage; allowing the

simultaneous conducting of the primary and secondary winding. The current path of the first mode provides the diode D_1 on the secondary side with forward bias charging the inductor L. The load voltage is the input voltage multiplied by the transformer ratio. In the second mode of the converter the switch S is turned off causing D_1 to turn off as well. When the switch is turned off, a sudden demagnetization of the transformer core would occur and cause an infinitely large voltage leading to a devastating outcome. Therefore, the converter is created with a three winding transformer, with the primary and secondary windings acting as a normal transformer. The tertiary winding along with the diode D_3 are used to recover the magnetization energy creating a current path and clamping any destructive voltages from the transformer. This requires D_3 to turn on at the same instant the switch S turns off. Also, the magnetic coupling between the primary and tertiary winding must be excellent to guarantee the transfer of flux linking from the primary to the tertiary winding. The inductor L and output capacitor C in the second mode are discharging the energy stored from the first mode and the diode D_2 is conducting permitting a continuous and consistent voltage flow to the load during the second mode [15].

Forward converters are used in various types of applications with their main challenge dealing with techniques to reset the transformer(s) within the circuit [16]. There are an abundance of methods to reset the transformers which include: an inductor and capacitor (LC) snubber, a tertiary winding on the transformer, an active clamp reset, using two switches and many more [17, 18]. Each type of reset topology can have a different and dominating effect on the forward converter. A correctly computed LC snubber in the converter leads to a higher efficiency for the circuit [18] while using a two

switch converter allows for the least amount of voltage stress on the switches in any forward converter topology [18, 19].

Another disadvantage of the forward converter is it can only be used for certain applications because of its power rating. To overcome this limitation two or more forward converters can be connected in parallel to reduce the current stress and power loss in each phase of the converter [20]. Using this method with an active clamp on the switches that can absorb stored energy in the leakage inductance of the transformer and limit the voltage stress on the switch generates an efficiency of 87.2% in [20]. Similar to the ideas discussed in [20], using three switches instead of two produce a simple forward converter where the active clamp can be substituted for a clamp diode [21]. This method achieves great efficiency, approximately 93%, and is not limited by the 50% duty ratio of a two switch forward converter [21]. The main issues with this topology are the difficulty in controlling three switches and the complexity in each mode of the power stage.

By using an LC non-dissipative current snubber, two phases (with two transformers), and an input parallel output series topology; this paper presents a combination of methods to increase the efficiency of a forward converter that are combined to obtain a low power loss converter. Along with an increased efficiency the converter still obtains a relatively simple and practical design.

1.4 VOLTAGE MODE CONTROL

To obtain a closed loop converter that can compensate for minor disruptions on the photovoltaic array a control circuit must be implemented. The two most common

forms of control are current and voltage mode control which can best be illustrated in block diagrams. Voltage mode is the simpler of the two types of control and is most commonly used in buck converters. Figure 1.5 illustrates the controller of a buck converter.

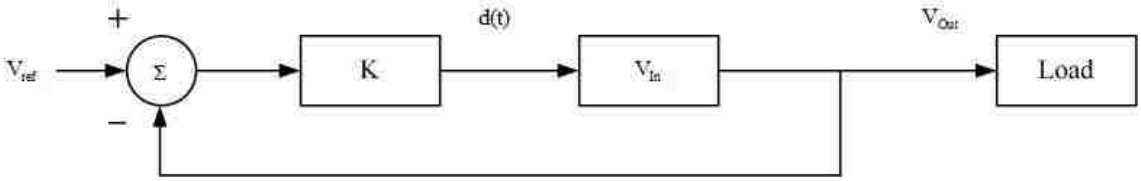

Figure 1.5 Control block diagram for buck converter [22]

In Figure 1.5, V_{ref} is the reference value to which the output voltage is compared and the resulting error signal is processed to provide a duty ratio command. K is the gain in the system with the transfer function given as [22]

$$V_{out} = \left(\frac{KV_{In}}{1 + KV_{In}} \right) \cdot V_{ref} \quad (1)$$

From these basic principles of voltage mode control in buck converters there is a vast amount of research to improve this control method. One of the issues is intermittency, which is a phenomenon that causes the system to bifurcate from initial regular operation to a destructive higher sub-harmonic operation, and then proceeding back to the original operation in the same bifurcation route in reverse [23]. Voltage mode control may also be used in z-source converters and the work done in [24] demonstrates voltage mode control achieving better performance than current mode programmed control [24]. From

the information given, the close knit relationship of the buck and forward converter would promote the use of a simple voltage mode circuit to control a forward converter to obtain a closed-loop system. However, the work described in this thesis did not require tight voltage regulation, so the converters all operated in open-loop mode.

1.5 STRUCTURE OF THESIS

This thesis begins with Section 2, the design, development, and computation of the forward converter used in the experiment. Next Section 3 reviews the simulated results of the forward converter and is followed by Section 4, which is the conclusion that summarizes the results in the experiment and provides extensions for the project. After Section 4, Appendix A is the screenshots of the schematic and board layouts of the forward converter. Appendix B are the tables of the solar data collected in the experiment for review or reference.

2. FORWARD CONVERTER DESIGN

To enable the solar array to have high efficiency, a reliable yet simple converter needed to be developed. The solar panels used for this experiment had a power rating of 205 W. Therefore, a forward converter was selected due to its high performance around 200 W. This project encompassed boosting a 24 V solar panel to 240 V that can be used on the grid. The specifications for the forward converter can be found below in Table 2.1

Table 2.1 Forward converter specifications (nominal)

Input Voltage	24 V
Output Voltage	240 V
Output Current	0.423 A
Diode Voltage drop	1 V
Efficiency Target	99%
Max Duty Cycle	50%
Frequency	100 kHz
Peak Flux Density	0.1 T
Number of Phases	2
Output Power	101.475 W
Input Power	102.5 W
Current Ripple	10%
Voltage Ripple	1%

To begin the design for the forward converter equations for the buck converter were computed to obtain unknown variables. First, to determine the output inductance and capacitance of the converter the general inductor and capacitor equations

$$V_L = L \cdot \frac{di}{dt} \tag{2}$$

and

$$I_C = C \cdot \frac{dv}{dt} \tag{3}$$

were manipulated to obtain

$$L = \frac{\left(V_{In} \cdot \frac{N_S}{N_P} - V_{out} \right) \cdot D}{f} \cdot \frac{n}{\Delta I} \tag{4}$$

$$C = \frac{\Delta I}{8 \cdot f \cdot \Delta V} \tag{5}$$

To determine ΔI for (5), equation (4) was solved for ΔI and substituted in (5) to obtain

$$\Delta I = \frac{\left(V_{In} \cdot \frac{N_S}{N_P} - V_{out} \right) \cdot D}{f} \cdot \frac{n}{L} \tag{6}$$

Equations (4) through (6) are similar to the inductor and capacitor equations of a buck converter with the addition of the transformer ratio $\frac{N_S}{N_P}$. The current ripple for equation (4) and the voltage ripple for equation (5) were selected to be 10% as listed in Table 2.1.

To obtain the output and input currents of the circuit, the basic power equation was solved for the current to obtain

$$I_{Out} = \frac{P_{Out}}{V_{Out}} \tag{7}$$

The input current was computed by plugging the result of (7) into

$$I_{In} = \left(\frac{I_{Out}}{1 - D} \right) \cdot \frac{N_S}{N_P} \tag{8}$$

which is derived from the property of a buck converter with the addition of the transformer ratio. A more in depth discussion on component choices can be found in Section 2.2.

Next simple equations were used to obtain values from the specifications given. Analogous to the inductance and capacitance equations, the forward converter equations were similar to a buck converter and can be observed in [25]. Understanding these concepts, the equations for the forward converter were computed. First the relationship of the output voltage and duty cycle was derived as

$$\frac{V_{Out}}{V_{In}} = \left(\frac{N_S}{N_P} \right) \cdot D \tag{9}$$

to determined the number of turns on the secondary winding. The buck converter has the same voltage and duty cycle relationship as (9) without the turns ratio. Next, the maximum duty cycle was selected at 50% which is shown above in Table 2.0. The actual duty cycle was calculated from equation (9) by solving for D and by dividing the result by two which was the number of phases used in the converter. This result yielded a 40% duty cycle, which was less than the maximum duty cycle and allowed some leeway when the MOSFET is "off" to not exceed a 100% duty ratio. To validate that the converter is in continuous conduction mode (CCM),

$$D \cdot \left(1 + \frac{N_T}{N_P} \right) < 1 \tag{10}$$

was used to establish boundaries for the values of the duty ratio, primary, and secondary number of turns. Also,

$$\frac{N_p}{N_p + N_T} < 1 \tag{11}$$

was verified to ensure continuous conduction mode within the forward converter. Next, the voltage stress on the switch must be calculated from

$$V_{SMax} = \left(1 + \frac{N_P}{N_T}\right) \cdot V_{In} \tag{12}$$

to compute the maximum voltage the MOSFET must handle during switching. To make certain the V_{SMax} value was low for this project, the primary and tertiary windings were set equal obtaining a $2 \cdot V_{In}$ relationship for the maximum voltage stress. As alluded to in Section 1.3, the use of two switches allows for the maximum stress voltage to equal V_{In}. This is helpful because the switches used will probably be cheaper than a switch that can handle a higher amount of voltage [26]. The drawback of a two switch converter is that the duty cycle cannot exceed 50%. The inability to exceed a 50% duty ratio can lead to the transformer's failure to properly re-set as well as during wide input variations the duty ratio becomes small causing an increase in current on the primary side resulting in amplified conduction and switching losses [26]. Satisfying equations (9) through (12) yielded the parameters given in Table 2.2.

Table 2.2 Forward converter calculated parameters

N_P	2 turns
N_S	25 turns
N_T	2 turns
V_{SMax}	48 V
Equation (11) Satisfied	.8 < 1 ✓
Equation (12) Satisfied	.5 < 1 ✓

2.1 NEW FORWARD CONVERTER TOPOLOGY

Similar to the work done in [27], the new forward converter topology that was created is an input parallel and output series (IPOS). The converter is equipped with two

phases to decrease the input current by splitting the current across two transformers. The developed forward converter topology can be observed in Figure 2.1.

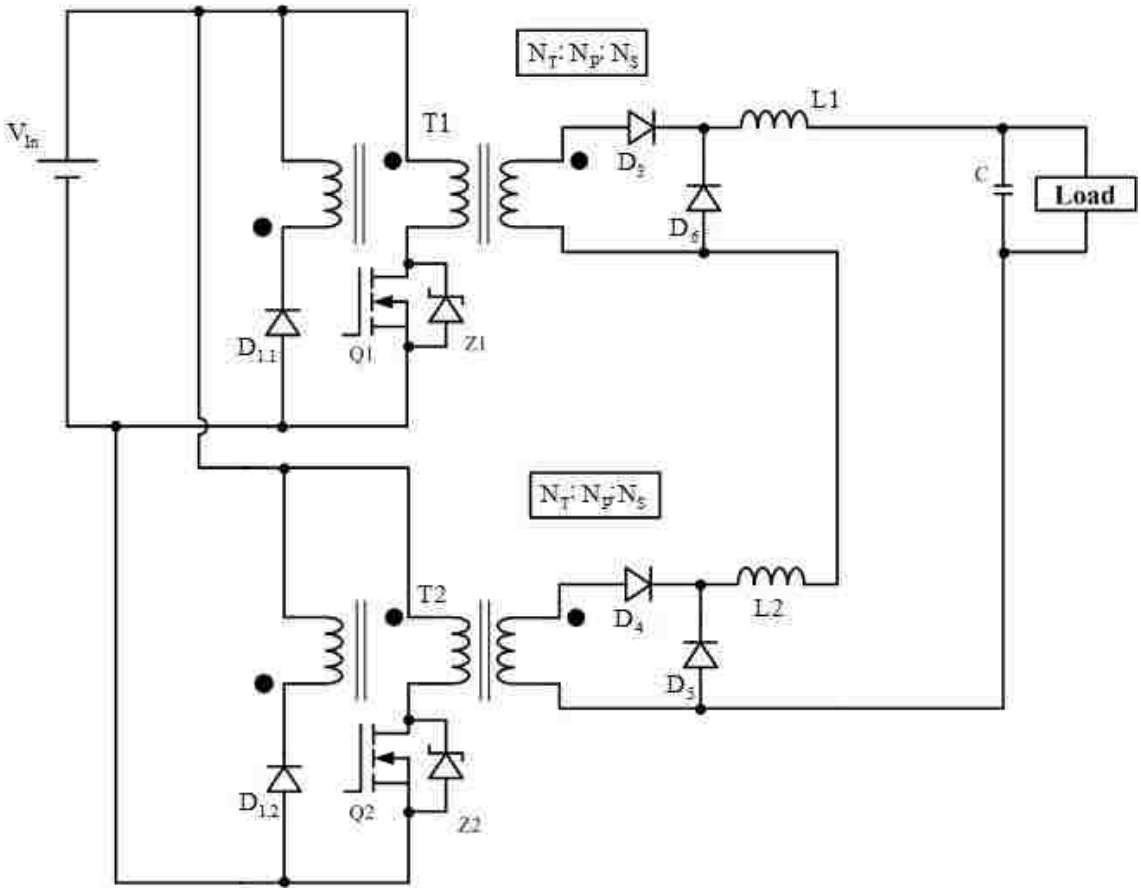

Figure 2.1 Developed forward converter topology

The circuit in Figure 2.1 performs similarly to the single phase forward converter explained in Section 1.3 with a couple of additions. On the primary side of the converter's transformers the MOSFETs, Q1 and Q2, switching is complementary with Q2 having a phase shift of 50%. This enables one phase to be "on" at a time delivering

half of the desired output voltage, in this case 120 V to the load. Both phases are combined on the output to yield 240 V. The series properties of the output of the circuit cause the inductors L1 and L2 to naturally share and interleaving decreases the current ripple.

To increase the efficiency of the converter by counteracting the leakage inductance of the transformers a snubber was added to Figure 2.1 across the MOSFETs and can be observed in Figure 2.2.

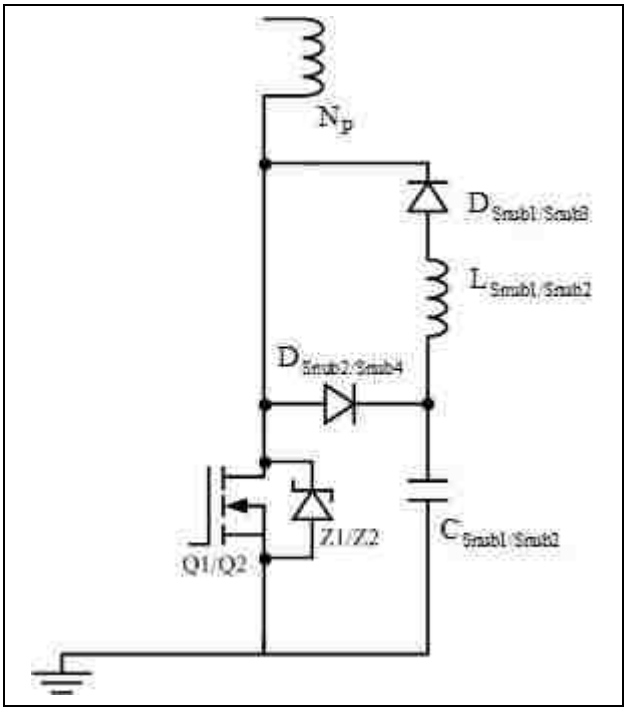

Figure 2.2 Snubber circuit

The snubber is activated when Q1/Q2 turns “off” the energy from the switch should be stored into the inductor of the snubber for half of the switching cycle. When the MOSFET turns “on”, the energy stored should be released into the MOSFET; thus,

allowing the energy from the leakage inductance from the primary to be recycled into the converter.

2.2 SELECTED COMPONENTS FOR FORWARD CONVERTER

To select the components for the forward converter calculations from the equations in Section 2 in combination with the simulated results found in Section 3 of this document were analyzed. First the output inductors for the converter were selected by computation of equation (4) to gain the value of $11.23\,\mu H$. This denotes that the output inductor's calculated value must be greater than or equal to $11.23\,\mu H$ to remain in continuous conduction mode. Next, values greater than the calculated inductor value were placed into the simulation for inductors L1 and L2 maintaining equivalence between both inductors. As the inductor's value increased, the output voltage became more stable and the output current ripple decreased; on the other hand, if the value was too high, the simulated response would become very sluggish and the output voltage of 240 V would not be achieved. From this test, it was concluded that roughly $500\,\mu H$ would permit a stable performance, thus the $470\,\mu H$ Axial Lead Power Chokes-PCH-27 by Coil Craft was selected for both inductors on the secondary side of the forward converter. This inductor has a relatively low direct current resistance (DCR) at 1.04 ohms and a saturation current of 0.573 A which is greater than the calculated output current of 0.423 A (found in Table 2.1).

The next component computed was the value of the output capacitor from equations (5) and (6). From these equations the output capacitor value equaled $1.11\,\rho F$; parallel to the output inductor the actual capacitor value selected must be greater than or

equal to the calculated output capacitor value to keep the converter in CCM. The capacitor selected was the Nichion VZ Series, an aluminum electrolytic $10\,\mu F$ capacitor that could withstand 315 V with a 0.0212 ohm equivalent series resistance (ESR). This capacitor was used because the voltage rating was greater than 240 V and a low ESR decreasing the conduction losses in the circuit. The input capacitor in the forward converter mimicked the output capacitor and performs as a filter to clear any unwanted noise on the input voltage.

The diodes on the primary side of the forward converter were selected to be the COMCHIP SB560E-G, 5 A, 60 V diode. Although the calculated input current is approximately 8.89 A the original solar panels for the experiment were set of KYOCERA 205 W panel, can only achieve a maximum current of 7.71 A for $1000\,W/m^2$ in ideal test conditions. At $600\,W/m^2$, the most probable operation range of the solar panel, the maximum current is about 4.8 A at $25°C$. Also since the forward converter has two phases each phase should only endure half of the input current which the simulation does not measure the input current after it is divided by two. The actual set of panels used in the outdoor experiment were the SunWize SW-S85P Solar Module panels rated at 85 W, 16.7 V, and 5.1 A with a maximum system voltage of 600 Vdc. The diodes will be able to operate at this range with no issues, and the diode can withstand a peak forward surge of 125 A in case the solar panel has a large current spike. The diodes D6, D4, and D5 on the secondary side of the converter were the MUR840 provided by ON Semiconductor with specifications of 8 A and 400 V. These diodes were selected because their voltage and current ratings are greater than 240 V and 0.423 A respectively. The diode D3 on the secondary side of the transformers was selected a C3D10060A–Silicon Carbide Schottky

Diode with ratings of 600 V and 10 A. The MUR840 ultrafast diode is incapable of switching fast enough to stop the negative voltage flow from the output causing a large negative voltage spike across D3 and a swift decrease in switching voltage in the MOSFET, which inevitably causes the destruction of the D3 diode. The C3D10060A Schottky Diode can switch much faster yielding a negative voltage spike and allows the converter to perform properly with an added bonus of zero switching losses.

The MOSFETs in the forward converter were selected as the International Rectifier IRLB4030PbF, with 100 V, and 180 A maximum voltage and current respectively. This MOSFET is able to endure the maximum input current and voltage of the converter. It also has an $R_{DS(on)}$ of $3.4\text{m}\Omega$, which keeps the conduction losses to a minimum. To protect the MOSFETs by providing a current path while the IRLB4030PbF is switching and clamping the voltage at approximately 56 V, the 1N4758A, 56 V zener diode was selected with the anode and cathode of the zener connected to the source and drain of the MOSFETs respectively. The diode can also withstand a maximum surge current of 80 A for 8.3 ms.

The gate-to-source voltage rating of the IRLB4030PbF is ±16 V, which is why the MIC4424 gate driver by MICREL was chosen. The MIC4424 has a wide operating range of +4.5 to +18 volts, allowing it to drive the IRLB4030PbF easily. Also the gate driver has a peak current of 3 A which will allow the MOSFET to switch at its optimal capability.

The snubber components were selected using a trial and error method within the simulation. The snubber was constructed many different ways in the simulation and finally similar to Figure 2.2 with the snubber inductor and capacitor initially set to

$500\,\mu H$ and $10\,\mu F$, respectively. From the trial and error process the inductor selected for the snubber was the $1.0\,\mu H$ Power Choke, vertical mount Coilcraft PCV-0-102-25L inductor which is rated for an rms current of 21.8 A. The snubber capacitor was the ECWF61136L $0.011\mu F$ Panasonic metalized polypropylene film capacitor. This capacitor can handle a maximum of 630 V with a dissipation factor of less than 0.20% at 10 kHz.

2.3 TRANSFORMER DESIGN

To construct the transformers, the core geometry or K_g approach obtained was used to determine the proper specifications. The design of the forward converter transformer commenced with the assumption that the primary and tertiary number of windings were equal and [28]

$$\frac{R_{ac}}{R_{dc}} = 1$$

This is important when building the tertiary winding of the transformer because the equations in this design are validated from this understanding.

First, the wire size was calculated for the transformer design, this included the skin depth and diameter of the wire which can be determined in

$$\varepsilon = \frac{6.62}{\sqrt{f}}[\text{cm}] \tag{13}$$

and

$$D_{wire} = 2(\varepsilon)[\text{cm}], \tag{14}$$

respectively. With equations (13) and (14), the bare wire area is

$$A_w = \frac{\pi \cdot D_{Wire}^2}{4} [cm^2] \quad (15)$$

where D_{wire} is the result of (14). From (15) the American Wire Gauge (AWG) can now be selected and the wire gauge selected is greater than the result of (15), which is a common rule of thumb.

Next the electrical coefficient was calculated

$$K_e = .145 \cdot f^2 \cdot \Delta B^2 \cdot 10^{-4} \quad (16)$$

where, f is the switching frequency and ΔB is the operating flux density (both can be found above in Table 2.0). The result of (16) allows the transformer core geometry (K_g) to be selected with the equation

$$K_g = \frac{(P_{in} \cdot D_{max})}{\alpha \cdot K_e} [cm^5] \quad (17)$$

Once the K_g is found from (17) a transformer core was selected from the K_g calculation. As with the wire size selection, the core with a value closest to and greater than the calculated K_g was chosen.

The next set of equations deals with the primary windings of the transformers. The first step was to find the number of turns on the primary winding using

$$N_P = \frac{(V_{in[min]} \cdot D_{max} \cdot 10^4)}{f \cdot A_c \cdot \Delta B} [turns] \quad (18)$$

followed by the current density,

$$J = \frac{\left(2 \cdot P_{in} \cdot \sqrt{D_{max}} \cdot 10^4\right)}{f \cdot \Delta B \cdot A_c \cdot W_a \cdot K_u} [\text{amps per } cm^2] \quad (19)$$

Then the calculation of the primary RMS current was found using the expected input power, minimum input voltage, and the maximum duty ratio in

$$I_P = \frac{P_{in}}{V_{in[min]} \cdot \sqrt{D_{max}}} \text{ [amps]} \quad (20)$$

Equation (20) should be divided by the number of phases in the converter to achieve a more accurate value of the current entering the primary transformer winding; in this case it was divided by two. The values determined in (19) and (20) enabled the primary bare wire area to be computed by

$$A_{wp} = \frac{I_P}{J}[cm^2] \quad (21)$$

Using (21), the calculation of the number of strands for the primary winding can be obtained by

$$NS_P = \frac{A_{wp}}{A_w \text{ of \#AWG used}} \quad (22)$$

Equation (22) allows for the proper amount of strands of AWG to be selected for the primary winding. When the number of wire strands for the primary winding exceeds four, the transformer becomes physically impossible to construct. To alleviate this issue, flat wire was used in place of the traditional AWG wire and the conversion factor for the flat wire to AWG is

$$\frac{.067741}{A_w \text{ of \# AWG used}} \quad (23)$$

After obtaining the correct value for the wire strands, the new micro-ohm per centimeter must be calculated using

$$(\text{new})\frac{\mu\Omega}{\text{cm}} = \frac{\frac{\mu\Omega}{\text{cm}}}{NS_P} \tag{24}$$

Equation (24) enables the resistance and thus the primary copper loss for the winding to be calculated with

$$R_p = MLT \cdot N_P \cdot \left(\frac{\mu\Omega}{\text{cm}}\right) \cdot 10^{-6}[\Omega] \tag{25}$$

and

$$P_P = I_P^2 \cdot R_P \ [\text{W}], \tag{26}$$

respectively.

The calculations for the secondary winding must be determined and were similar to the procedure in the primary winding calculations. To begin these calculations, the secondary number of turns and current were determined with

$$N_S = \left(\frac{N_P \cdot V_{out} \cdot V_d}{D_{max} \cdot V_{in[min]}}\right) \cdot \left(1 + \frac{\alpha}{100}\right)[\text{turns}] \tag{27}$$

and

$$I_s = \frac{I_{out}}{\sqrt{2}}[\text{A}] \tag{28}$$

Next the bare wire area and the amount of wire strands for the secondary wire were calculated by,

$$A_{ws} = \frac{I_s}{J}[\text{cm}^2] \tag{29}$$

and

$$NS_s = \frac{A_{ws}}{A_{\text{w of \# AWG used}}} \tag{30}$$

The new micro-ohm per centimeter is computed next by

$$(\text{new})\frac{\mu\Omega}{\text{cm}} = \frac{\frac{\mu\Omega}{\text{cm}}}{NS_S} \tag{31}$$

This allows the resistance and the copper loss to be calculated by

$$R_s = MLT \cdot N_S \cdot \left(\frac{\mu\Omega}{\text{cm}}\right) \cdot 10^{-6}\ [\Omega] \tag{32}$$

and

$$P_S = I_S^2 \cdot R_S [W] \tag{33}$$

Equations (26) and (33) are added together to produce

$$P_{cu} = P_p + P_s\ [W] \tag{34}$$

which was the total primary and secondary copper loss of the transformer and from (34) the regulation of the transformer can be calculated as

$$\alpha = \frac{P_{cu}}{P_{out}} \cdot 100[\%] \tag{35}$$

The final set of equations deal with the tertiary winding of the transformer and deriving the estimated losses in the transformer. First the inductance in the tertiary winding is calculated in the transformer (keeping in mind that the first and third windings are equivalent) using

$$L_T = L_{1000} \cdot N_T^2 \cdot 10^{-6}\ [mH] \tag{36}$$

Next, the time during which the magnetizing current increases was calculated by

$$\Delta t = \frac{1}{f} \cdot D_{max}\ [s] \tag{37}$$

along with the tertiary winding current using

$$I_T = \frac{V_{in} \cdot \Delta t}{L_T} \text{ [A]} \tag{38}$$

The tertiary RMS wire current is calculated along with the wire area and are viewed, respectively, as

$$I_{Trms} = \Delta I_T \cdot \sqrt{\frac{D_{max}}{3}} \text{ [A]} \tag{39}$$

and

$$A_w = \frac{I_{Trms}}{J} \text{ [cm}^2\text{]} \tag{40}$$

Next, each winding's number of turns was multiplied by the number of strands and the sum of the result of each was taken. This can be observed via

$$N = N_p \cdot NS_P + N_S \cdot NS_s + N_T \cdot NS_T \tag{41}$$

which produced the window utilization factor

$$K_u = \frac{N \cdot A_w \text{ of \#AWG used}}{W_a} \tag{42}$$

To obtain the core loss in the transformer first the $\frac{mW}{g}$ was found using

$$\frac{mW}{g} = .000318 \cdot (f^{1.51}) \cdot (B_{ac})^{2.747} \tag{43}$$

and then the power of the core was computed by

$$P_{fe} = \left(\frac{mW}{g}\right) \cdot \left(W_{tfe}\right) \cdot \left(10^{-3}\right) [W] \tag{44}$$

The results of equations (34) and (44) allow the total losses of the transformer with

$$P_\Sigma = P_{cu} + P_{fe} \text{ [W]} \tag{45}$$

Finally, the watts per unit area and the temperature rise in the transformer were calculated by

$$\psi = \frac{P_{\Sigma}}{A_t} \left[\frac{\text{Watts}}{\text{cm}^2}\right] \tag{46}$$

and

$$T_r = 450 \cdot (\psi)^{.826} [℃], \tag{47}$$

respectively. The calculation results of equations (13) through (47) are compiled below in Table 2.3 to Table 2.7. To obtain a simple calculation method each equation was inputted into Microsoft Excel. As the numbers of Table 2.1 and Table 2.3 were entered in the excel workbook each equation would update to obtain the correct result. This allowed any minor mistakes to be quickly identified and corrected.

Table 2.3 Transformer specifications

OutPut Power	101.475 W
Input Power	102.500 W
Electrical Coefficient (calculated)	1450
Core Geometry (calculated)	0.071 cm^5
Current Density	164.71797 amps per cm^2

Table 2.4 Wire calculations

Skin depth	0.021 cm
Wire Diameter	0.042 cm
Aw	0.001 cm^2
Aw (actual)	0.001 cm^2 (AWG #26)
Cu Resistance	1339 $\mu\Omega / cm$

Table 2.5 Primary winding calculations

Primary Turns	9.585
Primary Turns (actual)	2
Primary RMS Current	3.020 A
Bare Wire Primary	0.018 cm^2
Primary Stands	14.212
Primary Stands (actual)	52
Primary new uohm	25.75 $\mu\Omega / cm$
Primary in Resistance	0.0004 Ω
Primary Copper Loss	0.004 W
Strand Conversion (Flat Wire)	52.512

Table 2.6 Secondary winding calculations

Secondary Turns	60.25
Secondary Turns (actual)	25
Secondary RMS Current	0.149 A
Bare Wire Secondary	0.0009 cm^2
Secondary Stands	0.703
Secondary Stands (actual)	1
Secondary new uohm	1339 $\mu\Omega / cm$
Secondary Resistance	0.278 Ω
Secondary Copper Loss	0.006 W
Primary & Secondary Cu Loss	0.010 W
Transformer Regulation	0.010%

Table 2.7 Tertiary calculations & losses

Tertiary Inductance	0.0112 mH
Time	0.000005 s
Tertiary Current	0.011 A
Tertiary RMS Current	0.004 A
Tertiary Wire Area	2.655E-05 cm^2
Ku (calculated)	0.085
Milliwatts per gram	3.010 mW / g
Core Loss	0.181 W
Total Loss (w/# phases)	0.381 W
Total Loss (single Transformer)	0.191 W
Watts Per Unit Area	0.003 $Watts / cm^2$
Temp (Tr)	3.429 ℃

2.4 TRANSFORMER CALCULATED CORE LOSS

To obtain estimated core losses in the transformers different core materials at different frequencies were used with material specification charts to obtain estimated core losses in the transformers. The two types of cores that were used in the experiment were the 3C90 and the 3F3 materials for the ETD39 transformer. To calculate the specific power loss the flux density must be calculated by

$$\Delta B = \frac{\int V dt}{N_P \cdot A_e} \tag{48}$$

To obtain the numerator of (48) an estimation was made based on the square waveform of the input voltage and can be observed in

$$\int V dt = V_{in} \cdot D \cdot T \tag{49}$$

To obtain the peak flux density (48) is divided by 2 and a chart for each core to obtain the core power loss at different frequencies in Figure 2.3 and 2.4, respectively.

Once the value of the core loss by volume from Figure 2.3 and 2.4 was determined, it was multiplied by the volume of the transformer core to obtain an approximate core loss of the transformer for a particular frequency. A rough estimate was used to calculate the power loss at 150 kHz and 250 kHz due to the lack of data for those specific frequencies. Table 2.8 illustrates the estimated calculations below and Figure 2.5 conveys a graphical analysis of the core material and frequency by power loss.

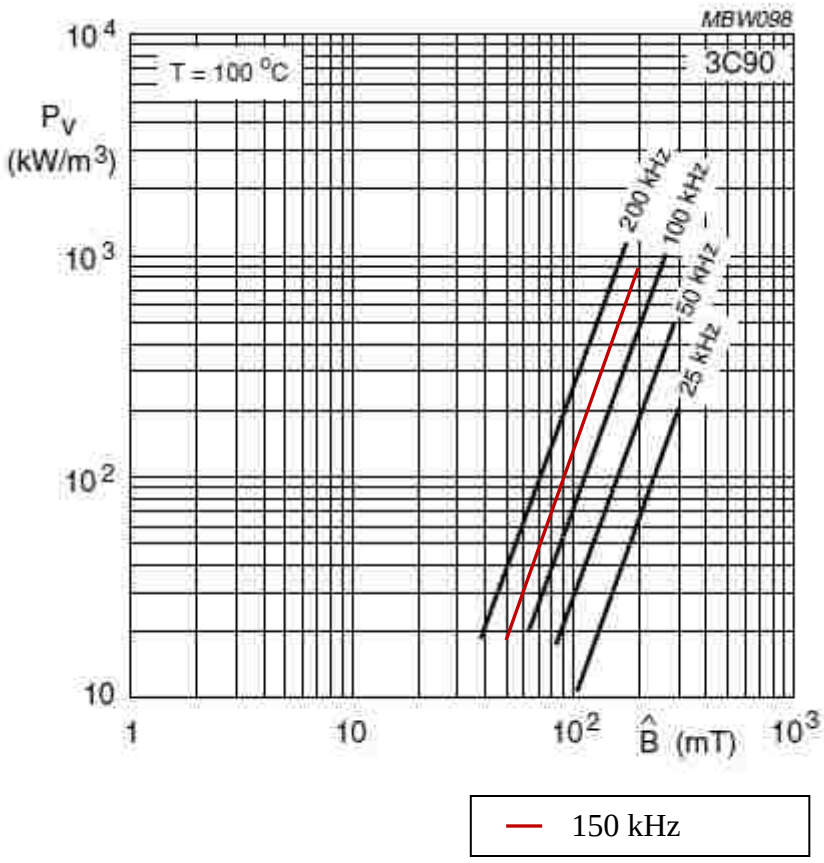

Figure 2.3 3C90 material specification chart [29]

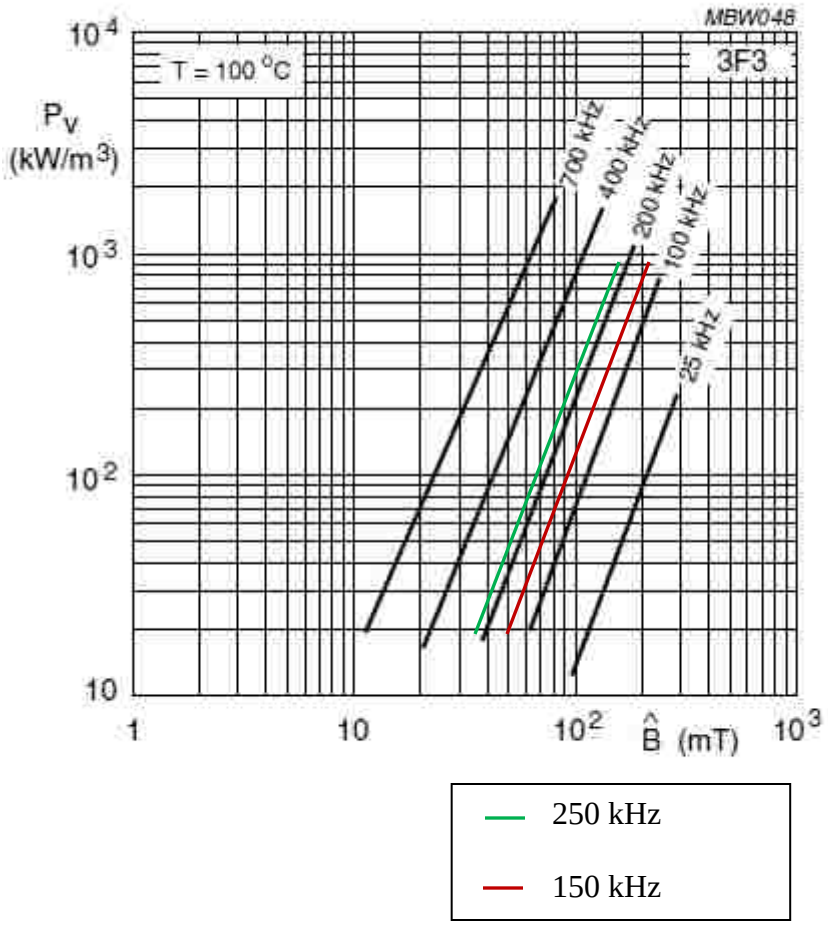

Figure 2.4 3F3 material specification chart [30]

Table 2.8 Transformer core loss of 3C90 & 3F3 at different frequencies

Input Voltage (V)	Frequency (kHz)	Core Type	Vdt (Vμs)	Bpk (mT)	P_core (kW / m^3)	P_core (W)
10	100	3C90	40	80	40	0.46
15	100	3C90	60	120	150	1.73
24	100	3C90	96	192	450	5.18
10	150	3C90	26.667	53.333	22	0.25
15	150	3C90	40	80	73	0.84
24	150	3C90	64	128	150	1.73
10	200	3C90	20	40	20	0.23
15	200	3C90	30	60	60	0.69
24	200	3C90	48	96	215	2.47
10	100	3F3	40	80	38	0.44
15	100	3F3	60	120	130	1.50
24	100	3F3	96	192	405	4.66
10	150	3F3	26.667	53.333	21	0.24
15	150	3F3	40	80	70	0.81
24	150	3F3	64	128	145	1.67
10	200	3F3	20	40	18	0.21
15	200	3F3	30	60	55	0.63
24	200	3F3	48	96	200	2.30
10	250	3F3	16	32	15	0.17
15	250	3F3	24	48	42	0.48
24	250	3F3	38.4	76.8	143	1.64

The results in Table 2.8 and Figure 2.5 allow one to conclude that increasing the input voltage has a very large effect on the increase in core losses in each material of the transformer. In general, the 3F3 material has less power losses then the 3C90 material; this may be due to the 3F3 material's ability to perform at frequencies up to 700 kHz and the data in Table 2.8 illustrates as the frequency increases in the material, with the voltage being constant, the core power loss decreases illustrating the increase in frequency yields a decrease in core loss.

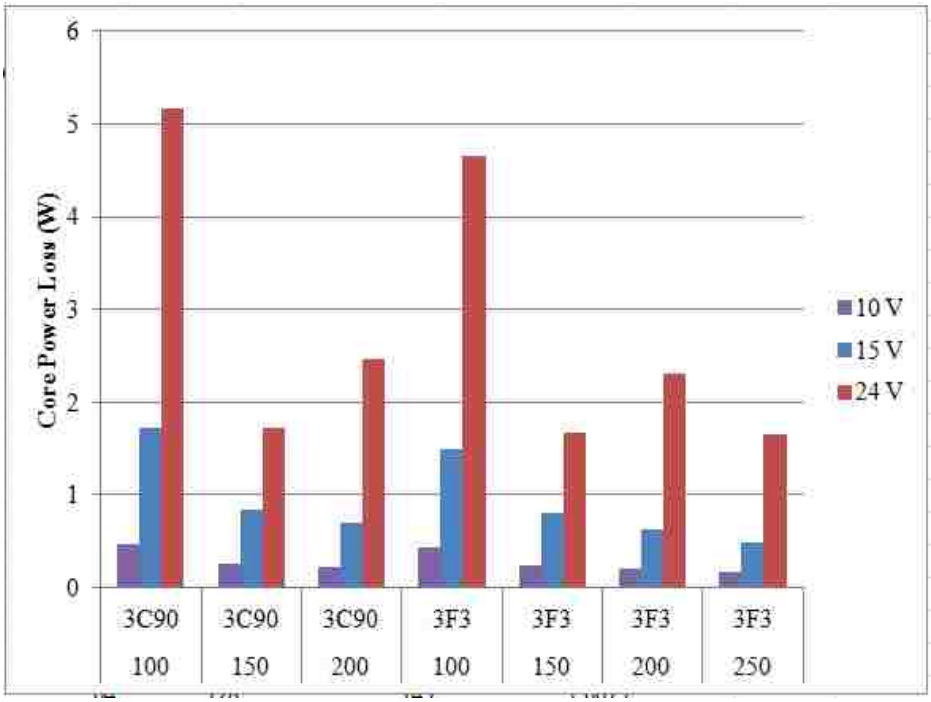

Figure 2.5 Core material and frequency versus core power loss

The increase in frequency does however, have a negative effect on the skin and proximity effect of the wire. This will cause skin losses in the wires of the transformer when the frequency is increased, illustrating that the increase in frequency will decrease the core losses and simultaneously increase the skin losses of the wire. Therefore, increasing the frequency of the converter can only increase the efficiency of the transformer to a certain degree.

2.5 TRANSFORMER CONSTRUCTION

Based on the MLT of the transformer the flat wire was measured to the proper specification. To construct leads for the primary and tertiary windings an 18 AWG was soldered onto the edges of the flat wire. First a butane torch was used to burn the lacquer

from the ends of the 18 gauge wire and a screw driver was used to scrape the lacquer ashes from the wire to reveal the copper. The 18 gauge wire was soldered to the flat wire, ensuring that the 18 gauge wire does not overlap the flat wire but is juxtaposed to the edge (as close as possible). To do this a vice grip was used to hold the flat wire into place and a large amount of flux was placed around the edge of the flat wire and the 18 gauge wire. The large amount of flux is needed to make certain the copper to copper solder joint is strong and reliable. The length of the lead created was approximately 6 inches to guarantee that there was enough wire to solder onto the bobbin of the transformer. A standard soldering iron was used to solder the elements.

After soldering, yellow polyester film electrical tape by 3M™ was used to cover the entire flat wire, the soldered portion of the wire, and a small amount of the leads to create an insulator around the flat wire. The same tape was used to tape the flat wire onto the bobbin of the transformer. This process began with the tape being folded and connected to itself to allow the adhesive of the tape to be on all sides. Then the tape was placed on the bobbin first and the flat wire was placed firmly on top of the tape onto the bobbin. In conjunction with this another piece of tape (not folded) covered the bobbin and one edge (where the soldered lead is) of the flat wire; this should allow minimal movement of the flat wire onto the bobbin. Also the lead was lined up with the lead on the bobbin. From this point the flat wire was turned as tight as possible onto the bobbin, using pliers to obtain a very snug winding (the tape should be strong enough to allow the pliers to be used). The leads of each transformer winding were labeled as primary, secondary, and tertiary to avoid confusion. The primary and tertiary windings must be wound on top of the other; the order placement of the windings does not matter. Then a

zip-tie was applied after both flat wires were applied to the bobbin thus keeping a firm fit on the windings. Since the current of the primary winding was greater than the tertiary, a thinner flat wire was used for the tertiary, but the same process was followed.

The secondary wire was a much smaller gauge of wire (26 AWG), which can be viewed in Table 2.4. To wrap the secondary wire very tightly, no measurements were taken; instead the wire was kept on the original spindle. Two turns of the wire were wrapped around the bobbin and there was enough excess wire to allow a solder onto the lead of the bobbin. Next the bobbin was turned horizontally and rolled by hand naturally creating a taut winding (this is similar to rolling a sleeping bag) around the bobbin. The weight of the spindle allows the wire to hold a tight fit as the spinning occurs and most of the rolling pressure should be applied to the bobbin rather than the spindle. Once the amount of turns needed was obtained excess wire was placed onto the bobbin's leads.

Finally the leads of all three windings were soldered to the bobbin leads. First, the leads were cut to fit onto the transformer leads and then the lacquer was burned and scraped away as previously stated. Each negative and positive lead was kept relatively close together; the primary and tertiary were on one side of the bobbin and the secondary was on the other side of the bobbin. For this project the tertiary was placed on the bobbin first, then the primary was placed on top of the tertiary, and finally the secondary was placed on the upper open part of the bobbin. The core of the transformer was placed into the bobbin and the transformer is completed. Figures 2.6 through 2.8 illustrate completed transformers:

Figure 2.6 Transformer picture A

Figure 2.7 Transformer picture B

Figure 2.8 Transformer picture C

3. RESULTS

3.1 SIMULATION PROCEDURE AND RESULTS

To verify the new forward converter topology presented in Section 2.1, a simulation was developed in PLECS[1], which is a Blockset for MATLAB/Simulink[2]. Figure 3.1 below illustrates the simulation model of the forward converter. The components in the simulation were specified to match with the physical components that are described in Section 2.2 of this document. Multiple simulations were conducted with the circuit shown in Figure 3.1 to observe the current and voltages of each diode, capacitor, MOSFET, and inductor produced by the forward converter topology. To obtain the best simulation results, components such as the duty ratio, output capacitor (C_{Out}), the transformers (T1 and T2), and the output inductors (L1 and L2) were modified to observe how the output voltage waveform was affected. A simple MATLAB m-file was used in combination with the simulation to simplify component adjustments.

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[1] PLECS is a registered trademark of Plexim Gmbh

[2] MATLAB and Simulink are registered trademarks of The Mathworks, Inc.

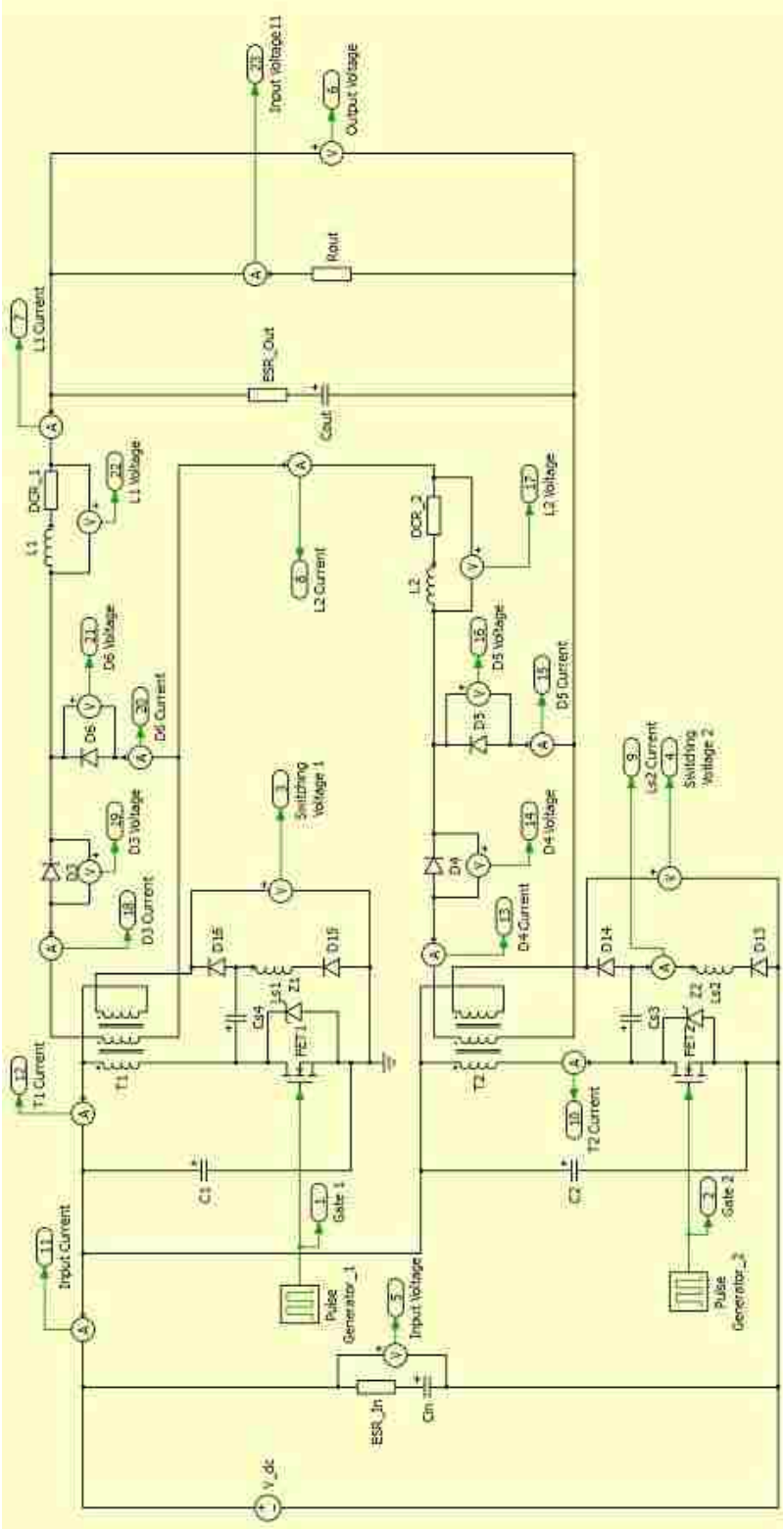

Figure 3.1 Simulation model for new forward converter

The first waveform that was observed in the simulation was the output voltage, which can be found in Figure 3.2.

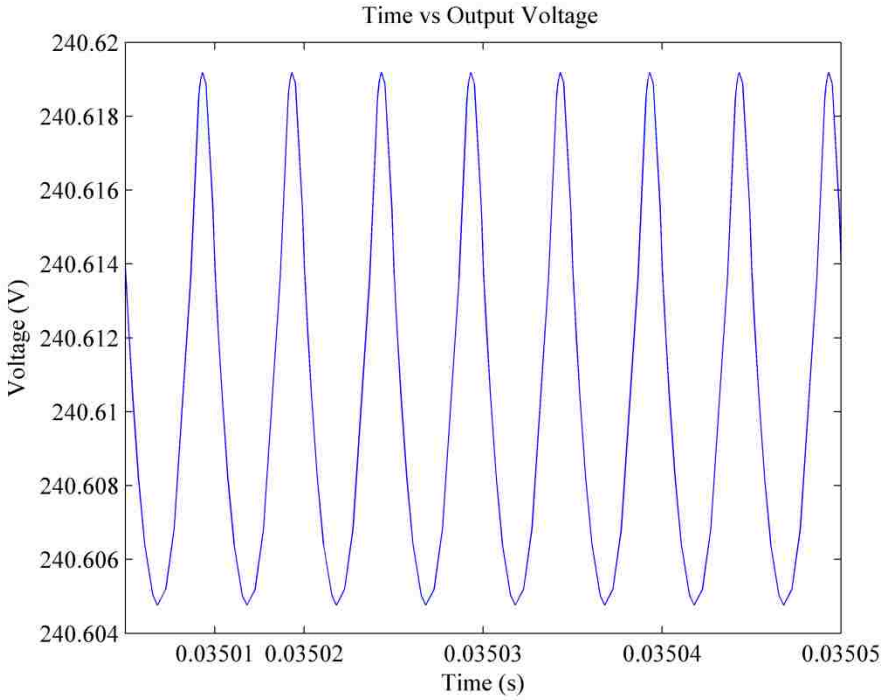

Figure 3.2 Simulated output voltage

Figure 3.2 verifies that the calculations for equations (2) through (11) produce a 240 V output from the values found in Table 2.1. The average output voltage was 240.61 V and the maximum voltage was about 240.62 V. The voltage ripple exceeds expectations by having a ripple that was less than 0.1 V, which was less than the target of 0.24 V (1% of the output voltage). This simulated result would suggest that the forward converter topology developed was able to be physically achieved.

Next Figures 3.3 and 3.4 confirm the inductor currents L1 and L2, respectively. The time scale of each graph was the same to enable a comparison of the waveforms accordingly. The average inductor currents were approximately 0.86 A and the maximum current was 0.97 A.

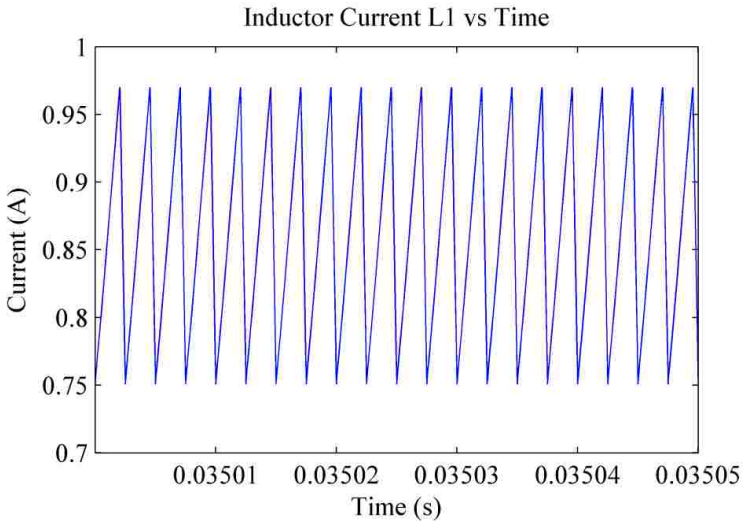

Figure 3.3 Simulated inductor current (L1)

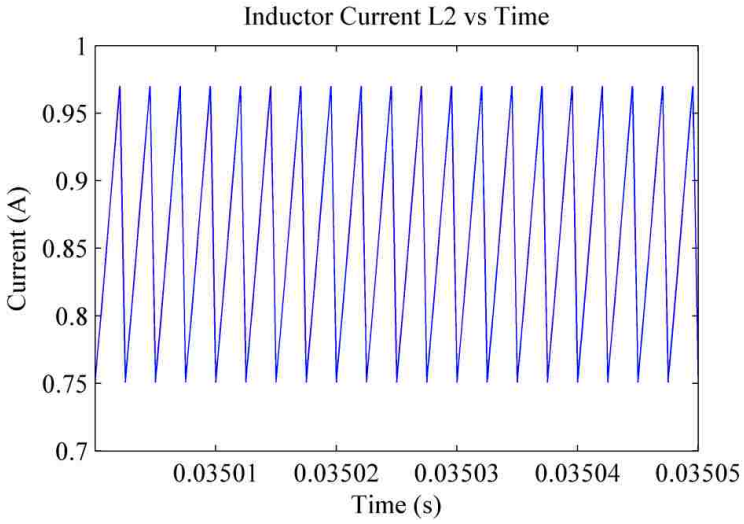

Figure 3.4 Simulated inductor current (L2)

The Figures 3.3 and 3.4 above are exactly the same, demonstrating the current sharing expected with an output parallel connected circuit. This current sharing is reflected onto the output current which yields the same waveform as L1 and L2 inductor currents. Since the two inductors naturally share current in this configuration the closed loop circuit selection of voltage mode control is a reasonable choice.

Figure 3.5 shows the input current of the simulated forward converter with an average current of approximately 20.25 A, which was very high. The calculated value for the input average current was roughly 9 A causing a huge gap between the two current values. The solar panel is unable to pull 9 A or 20 A of current. Therefore, one can conclude that the input current value was estimated to be closer to the calculated result of 9 A. The error in the simulation may be due to the lack of recognition of the both phases in the simulated converter and limitations in the PLECS program.

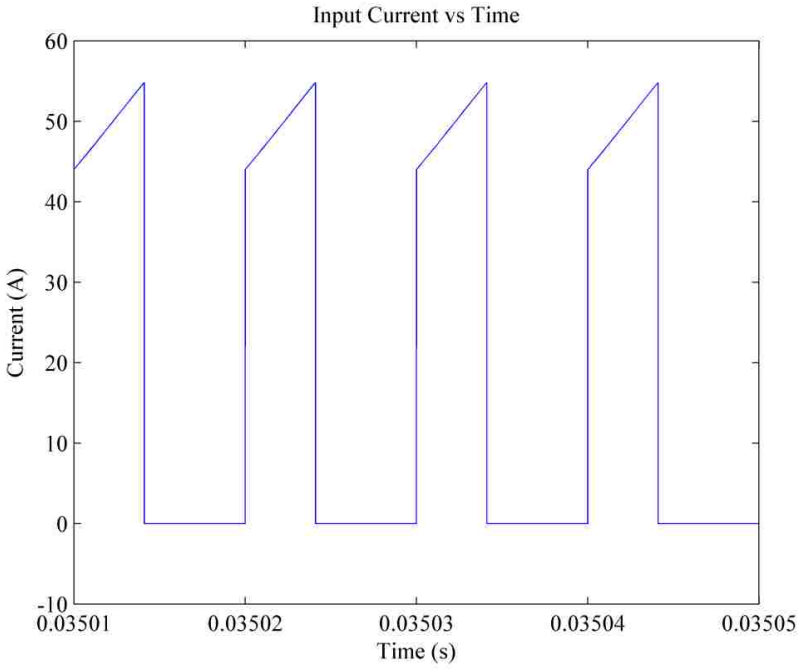

Figure 3.5 Forward converter input current

3.2 EXPERIMENTAL RESULTS

To conduct the experiment for the forward converter, which can be viewed in Figure 3.6, a test station was developed using four Fluke 8845A Digit Precision Multimeters (5), an Agilent N3300A System Electronic Load (6), a BK Precision Programmable PFC D.C. Supply (4), and a Tektronix TDS 2024 Four Channel Digital Storage Oscilloscope (1). A Tenma Switching Mode Power Supply (3) and an AFG 3022B Dual Channel Arbitrary/Function Generator (2) were also used before the microcontroller configuration was applied. Figure 3.7 illustrates the test station area with the numbers in red to verify the equipment. To observe the test station arrangement Figure 3.8 shows the schematic of the test station. Finally the computer program LabVIEW was used to compile the data from the testing station; a screenshot of the program can be viewed in Figure 3.9.

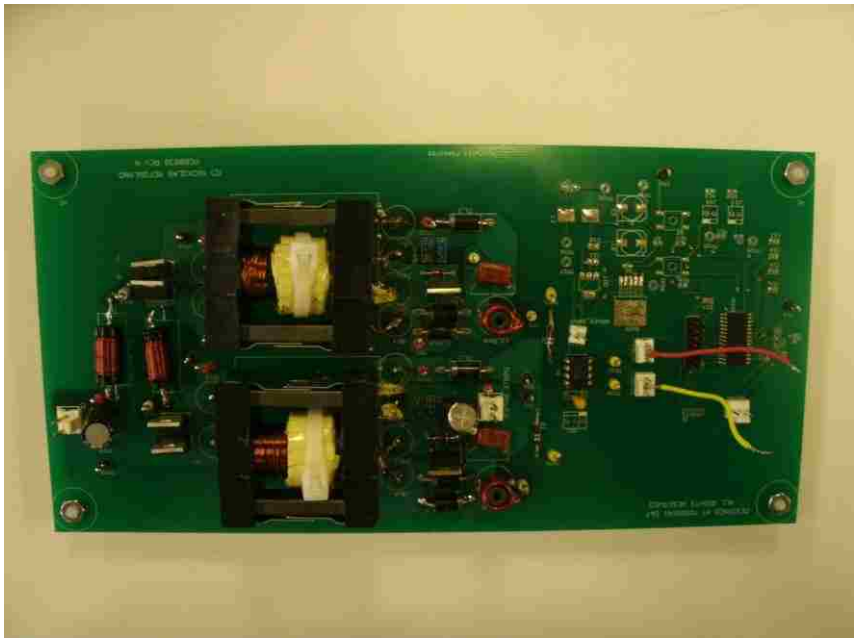

Figure 3.6 Forward converter

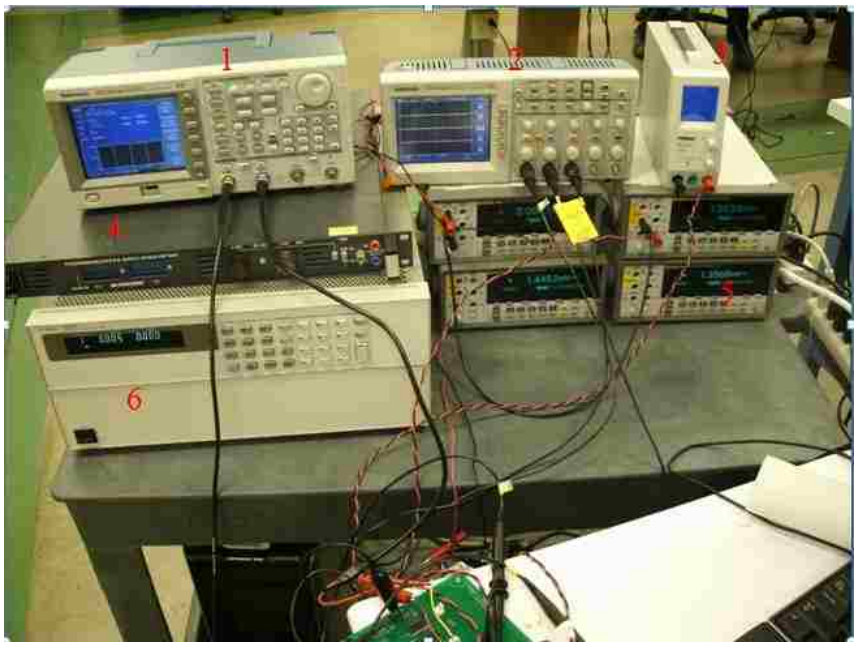

Figure 3.7 Testing station for forward converter

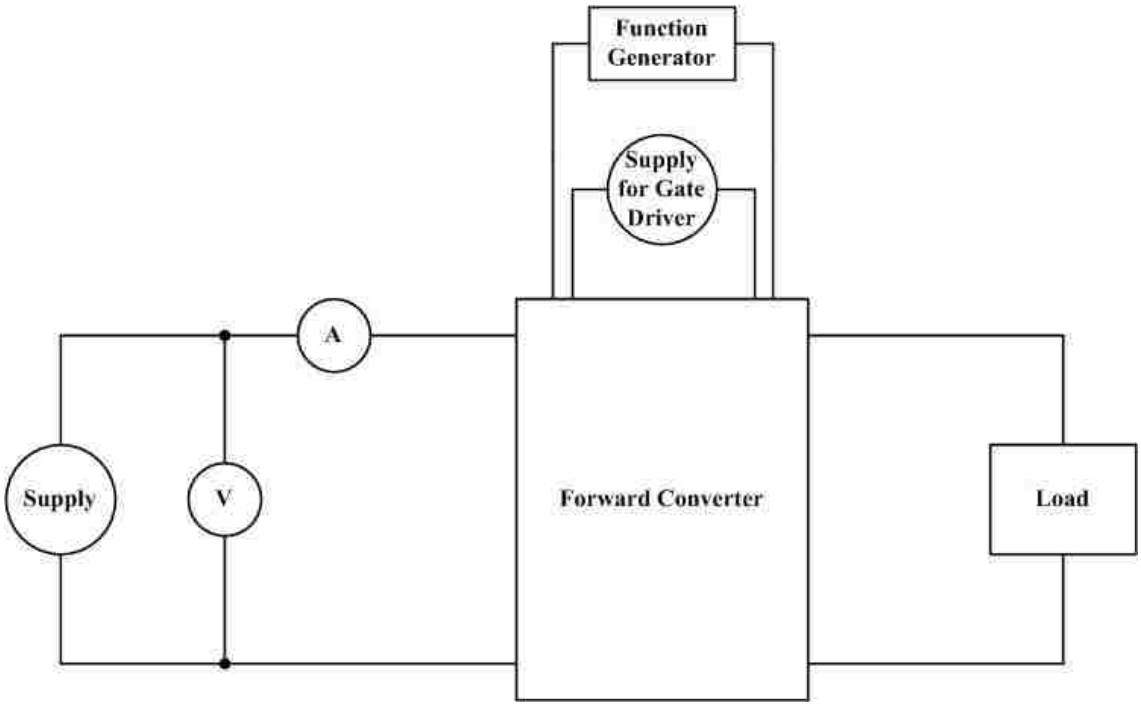

Figure 3.8 Test station schematic

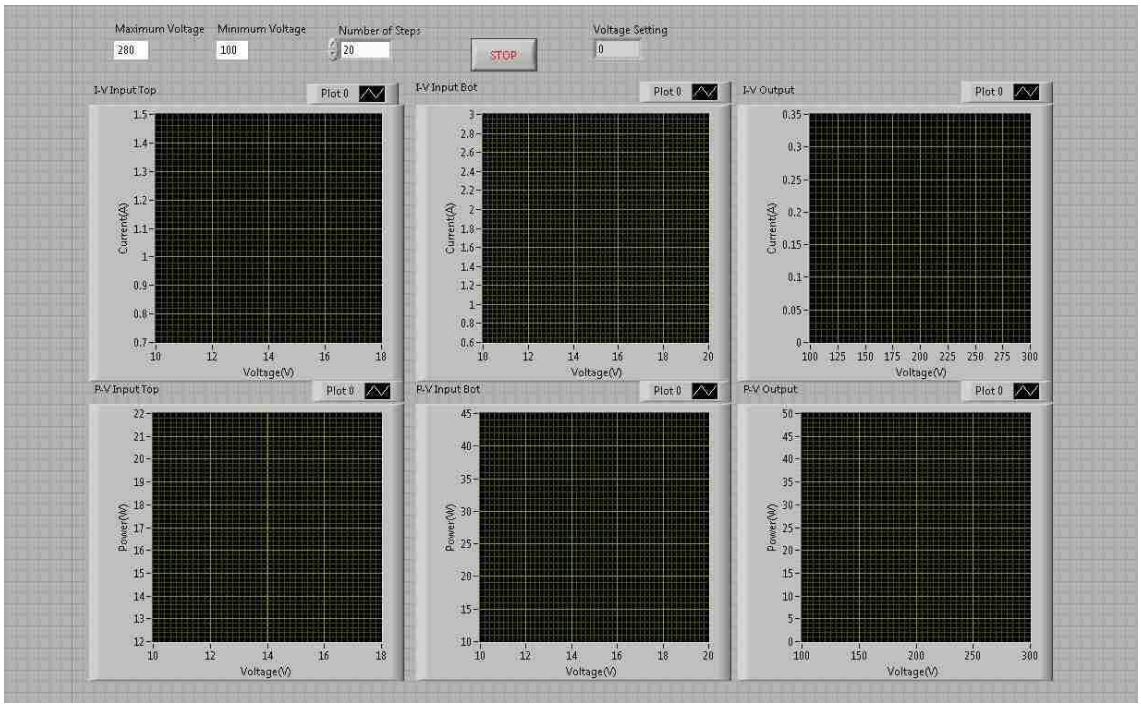

Figure 3.9 LabVIEW screenshot

The two outputs of the function generator were each set to a 40% duty cycle and a frequency of 100 kHz. The second output was given a 50% delay to ensure the switching signals were complimentary. The BK Precision D.C. Supply was set to the desired voltage for a particular test. The LabVIEW program controlled the Agilent N3300A Electronic Load, which was set to constant current mode, the Fluke Multimeters, and generated the input/output current and voltage for the forward converter in a Microsoft Excel document. During the testing waveforms for the output voltage, switching voltage, and snubber voltage were captured and can be observed in Figures 3.10, 3.11, and 3.12, respectively.

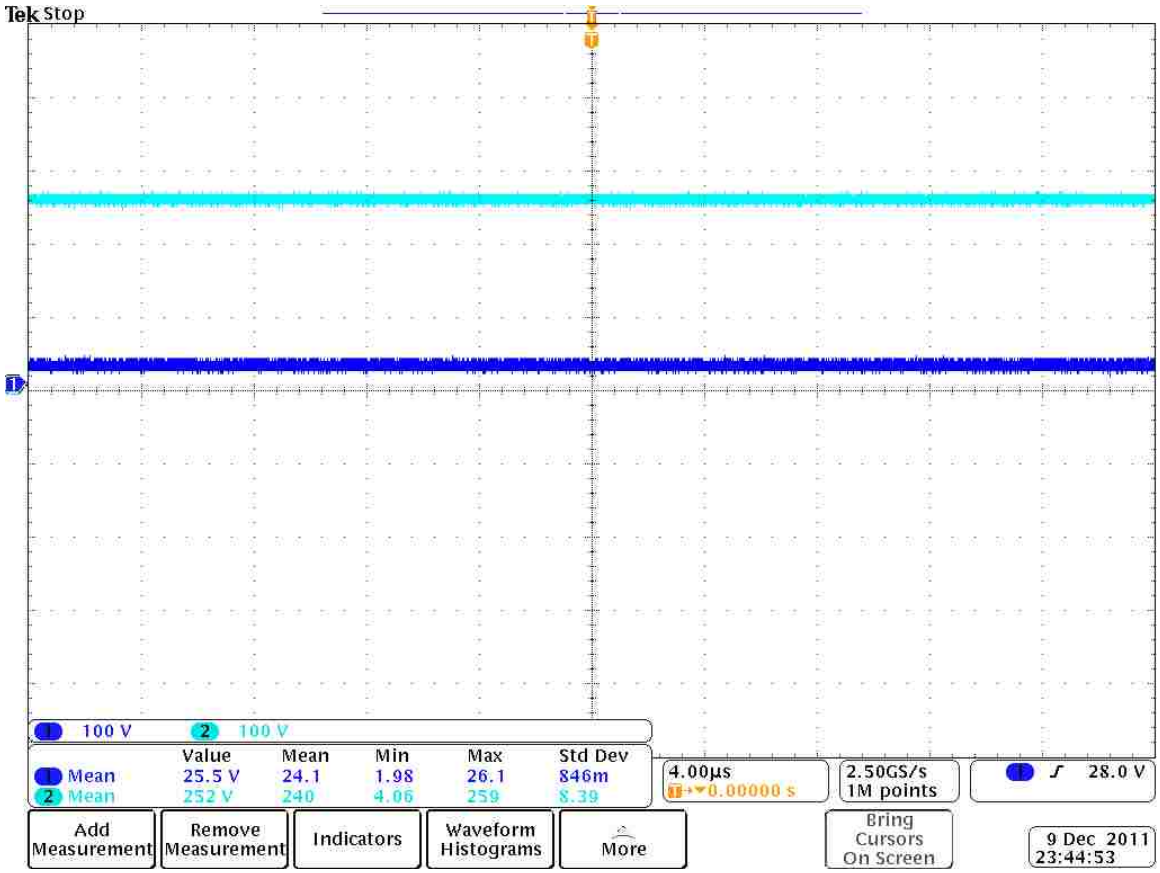

Figure 3.10 Measured output voltage from test point 15

Figure 3.10 illustrates the input and output voltage of the forward converter from the testing station. The Tektronix MSO 4034 Mixed Signal Oscilloscope was set at 100 V per division alone with the listing of the peak-to-peak, minimum, and maximum voltage for both waveforms. The constant current load was set to 0.1 A to obtain a reasonable comparison between the input and output voltage. The peak-to-peak voltage of the waveform is 12 V which is large but the voltage ripple does not play a significant role in the parameters of this project. The voltage ratio of input voltage to output voltage is approximately 0.01 higher than the selected ratio of the transformer in Table 2.2. This is due to the transformers in the actual circuit being slightly different causing a minute variation in the voltage.

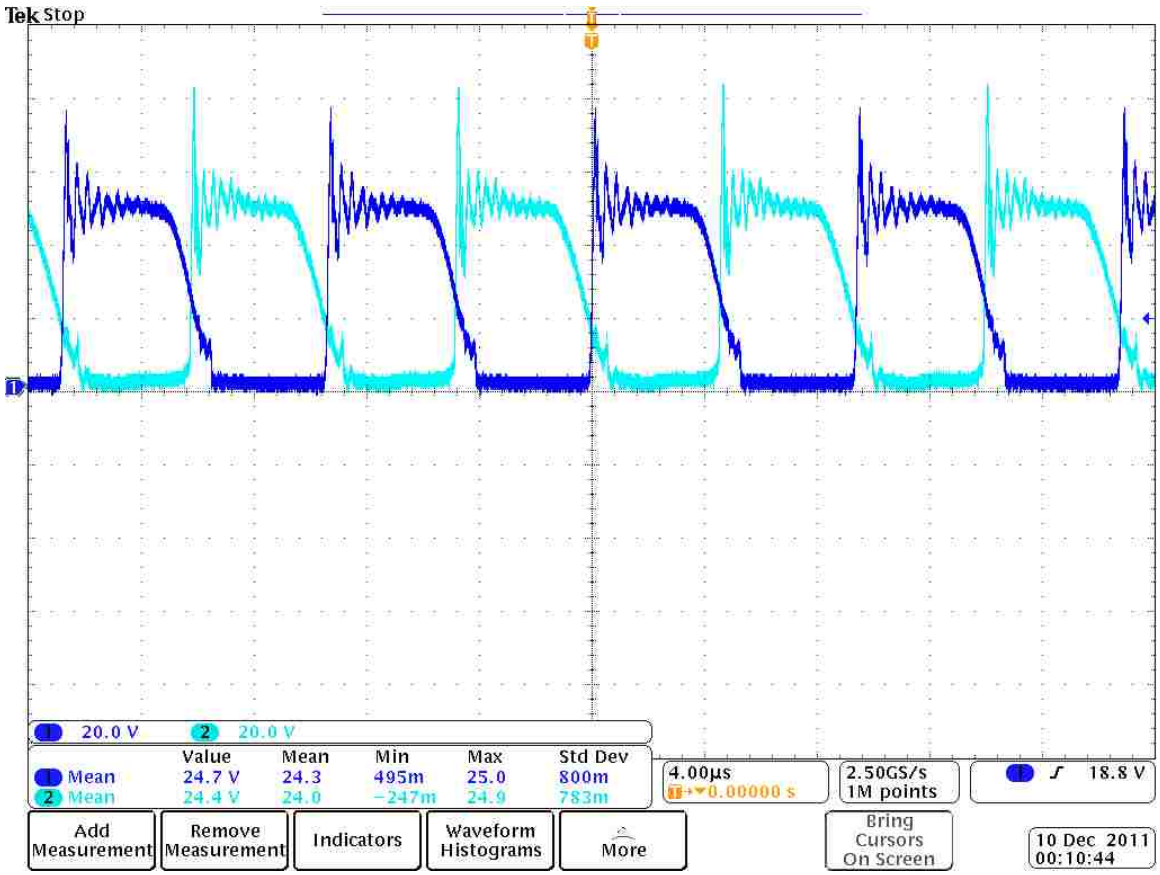

Figure 3.11 Measured switching voltage from test point 22 & 23

In Figure 3.11, the switching voltages of the MOSFETs are shown with phase 1 and phase 2 as channel 1 and channel 2, respectively. From the waveform, the complementary performance of the two phases in the forward converter can be observed along with the mean measurements on the waveform, exemplifying both MOSFETs at approximately 48 V which is double the input voltage. The voltage spike on each switch is the clamping of the voltage by the zener diode when the MOSFET is turned "off". The subtle difference in channels 1 and 2 in Figure 3.11 is due to the minor difference between the leakage inductance in the transformers, which were handmade, slightly

decreasing their equivalency. Furthermore, the waveform of the snubber voltage in Figures 3.12 and 3.13 coincides with the switching of the MOSFET.

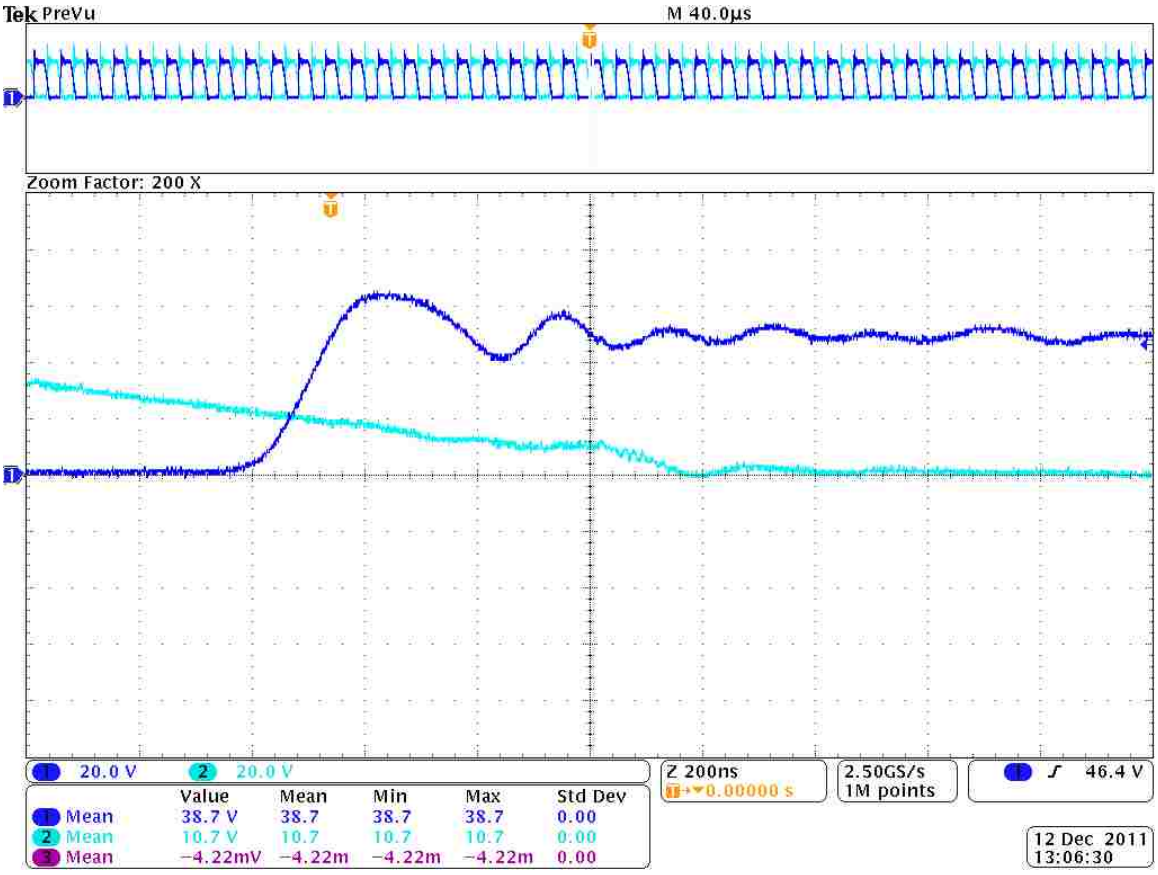

Figure 3.12 Phase 1 measured snubber voltage from test point 6

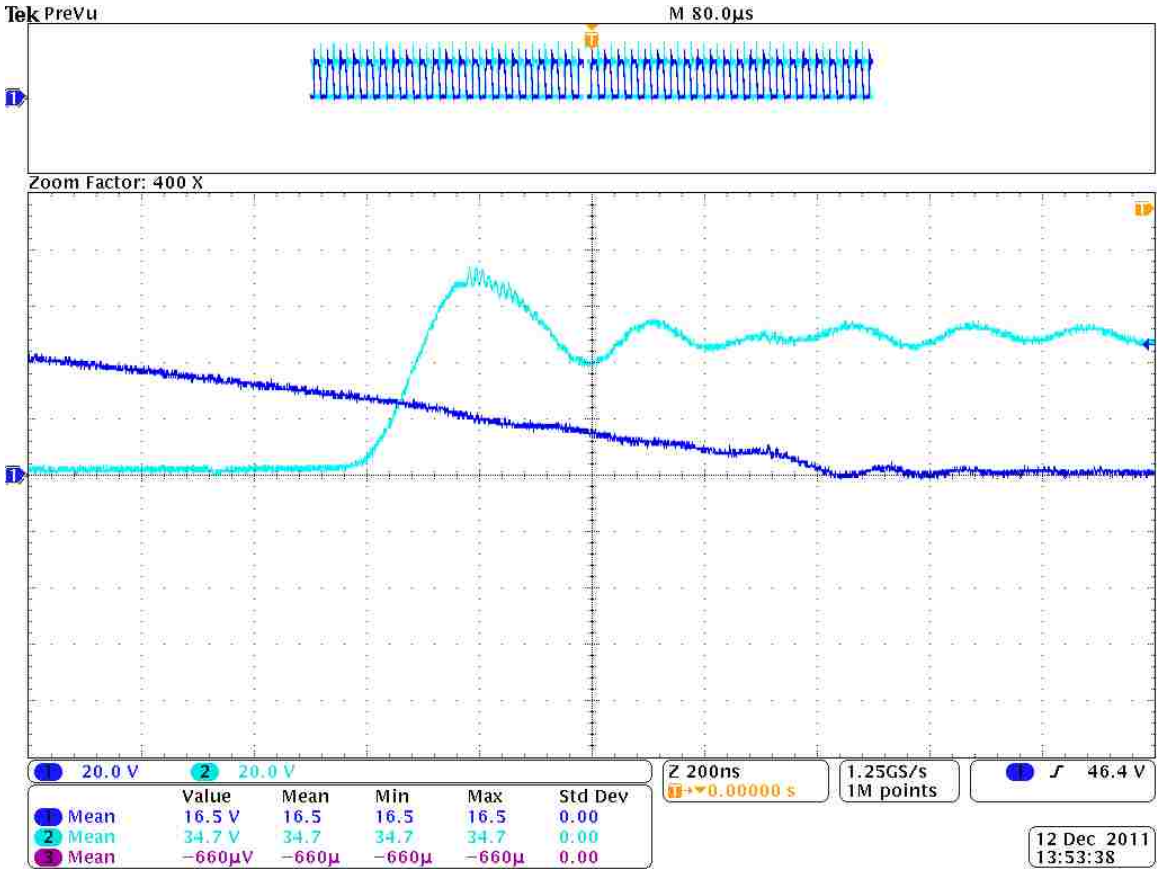

Figure 3.13 Phase 2 measured snubber voltage from test point 34

The pictures in Figure 3.12 and 3.13 are zoomed in pictures of the spikes of the switching voltage of the MOSFET (phase 1 and phase 2 respectively). The rounded nature of the voltage spike is due to the snubber, which should increase the efficiency of the converter by absorbing the energy in the leakage inductance of the transformer. To verify that the snubber is functioning properly it was removed from the circuit and the resulting MOSFET waveform can be viewed in Figure 3.14.

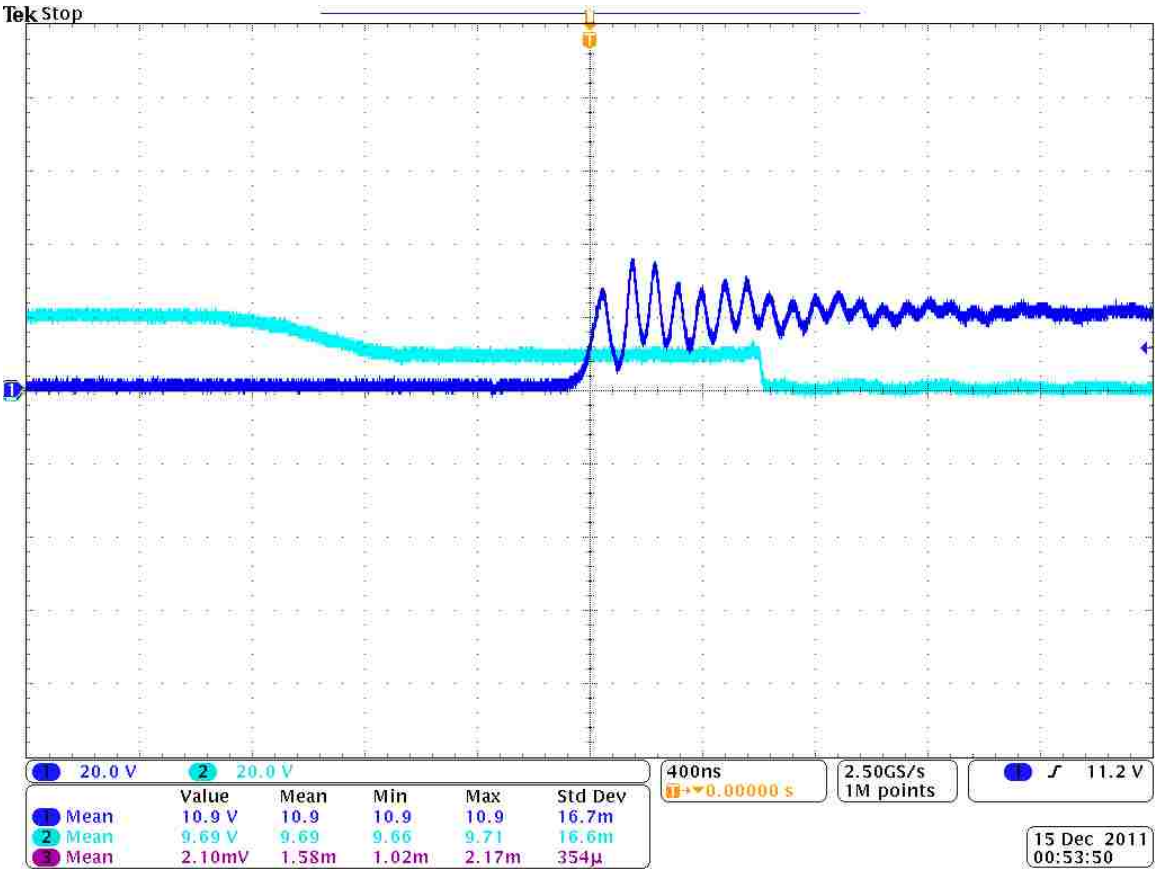

Figure 3.14 Phase 1 MOSFET voltage with snubber removed from test point 6

Compared to Figure 3.12, Figure 3.14 has a greater settling time with a large dip in the MOSFET voltage that reaches approximately 4 V. The removal of the snubber also results in a decrease in stability, as seen in the increase in ripple that Figure 3.14 possesses. These differences in the waveforms in the non-snubber and snubber circuit also have an effect on the efficiency which can be viewed below in Figure 3.15 below. From the data presented in the test, Figures 3.15, 3.16, 3.17, and 3.18 where Figure 3.18 is the efficiency with the snubber, the efficiency at each of the three voltage settings is greater with the snubber than without the snubber.

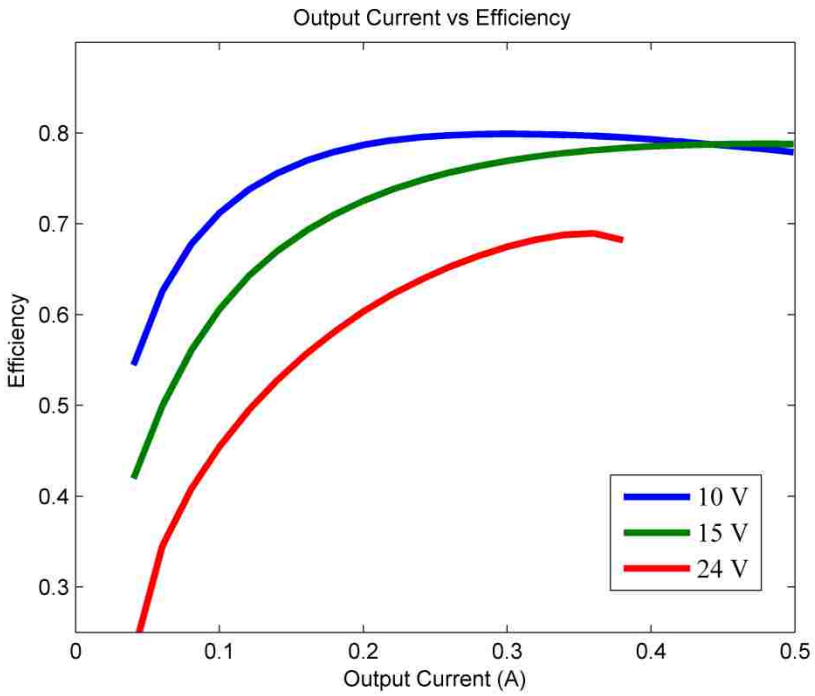

Figure 3.15 Efficiency of forward converter without snubber (100 kHz 3C90)

To obtain a greater understanding of the snubber's influence on the MOSFET, the snubber capacitor was changed from $0.011\mu F$ to $0.1\mu F$. The resulting switching waveforms can be viewed below in Figure 3.16. This figures illustrates a much softer spike in the than the waveforms in Figures 3.12 and 3.14. The increase in the snubber capacitor to $0.1\mu F$ capacitor generates little noise in the MOSFET waveform but the efficiency is less than the snubber capacitor of $0.011\mu F$. The efficiency curve with no snubber, meaning $0\mu F$ was also compared to the efficiencies of the $0.011\mu F$ and $0.1\mu F$ capacitors and the three curves can be found in Figure 3.17. From this waveform it can be viewed that decreasing the capacitance to zero does not offer a better efficiency. In fact, the zero capacitance waveform has a similar efficiency as the $0.1\mu F$ capacitor. This

demonstrates that there is an optimal capacitance for the snubber to operate most effectively.

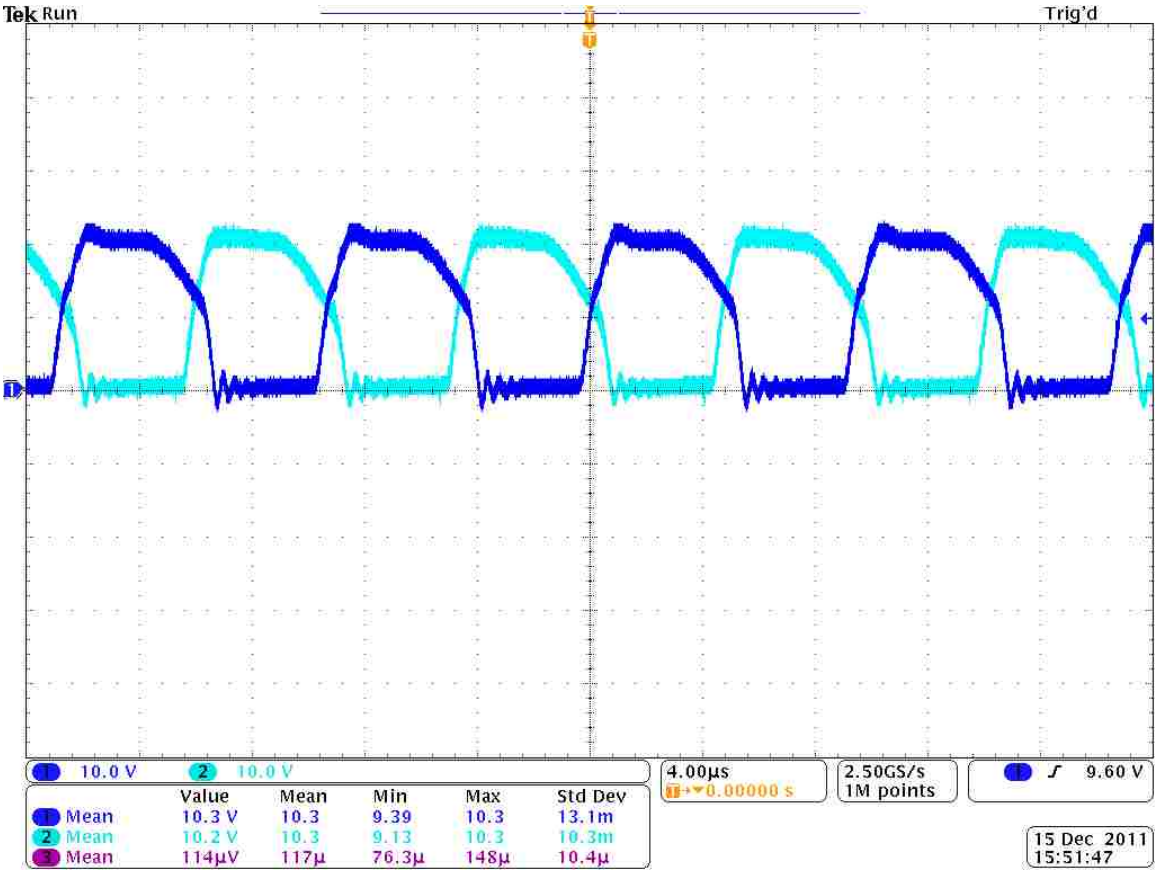

Figure 3.16 Snubber with $0.1\mu F$ snubber capacitor at 10 V

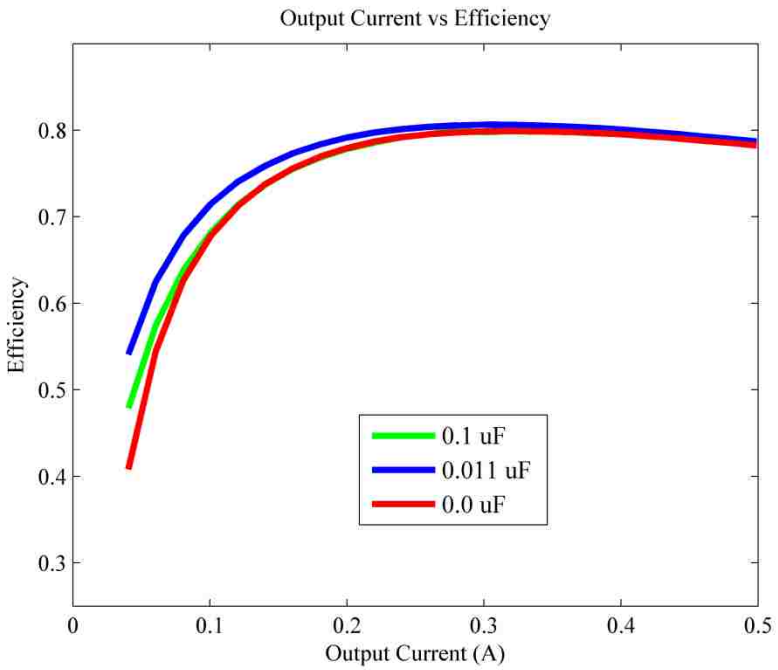

Figure 3.17 Efficiency of forward converter at 10 V $0.011\mu F$ & $0.1\mu F$ (100 kHz 3C90)

Next the efficiencies of the forward converter were calculated at different points with different elements changed such as frequency and transformer core to obtain the most efficient result. This allowed the forward converter efficiency to be calculated quickly for different voltages, in this experiment 10 V, 15 V, and 24 V which can be viewed in Figure 3.18 through 3.24.

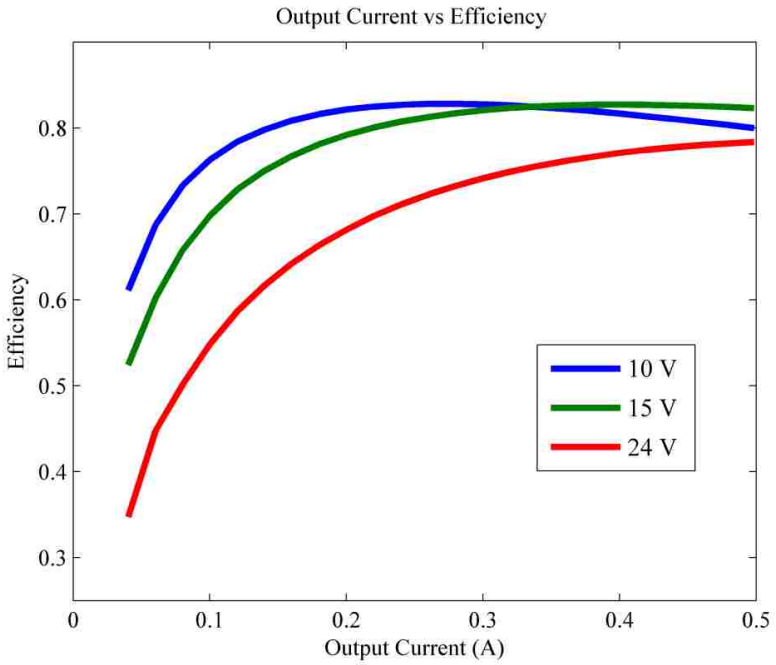

Figure 3.18 Test station efficiency at 100 kHz & 3C90 core

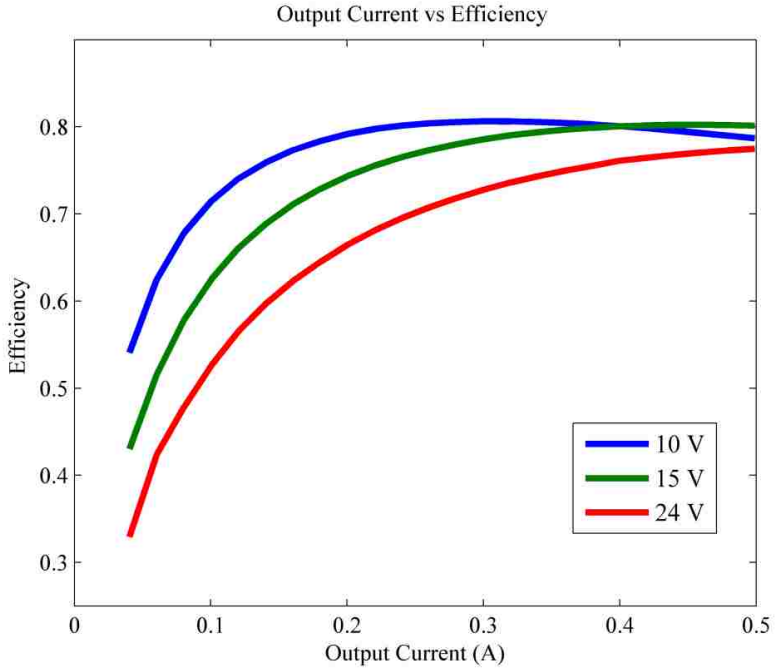

Figure 3.19 Test station efficiency at 100 kHz & 3F3 core

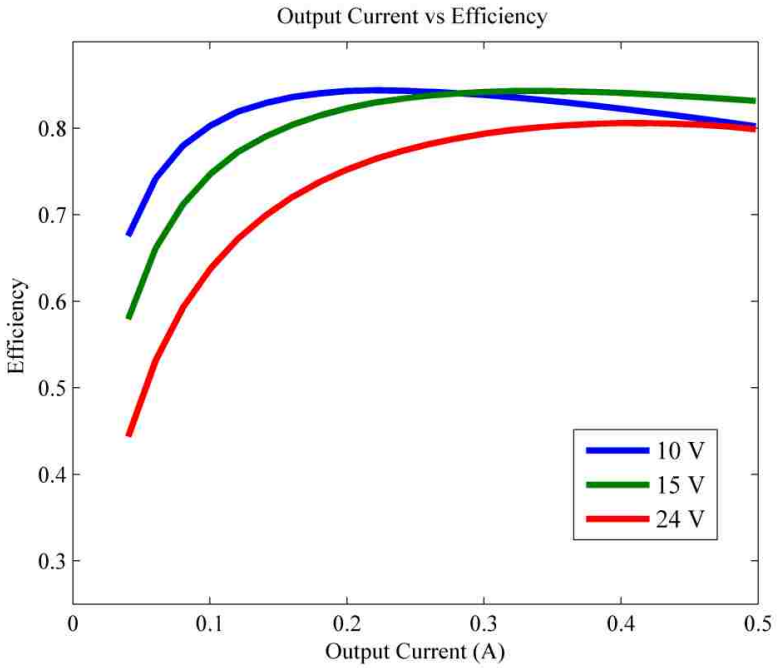

Figure 3.20 Test station efficiency at 150 kHz & 3C90 core

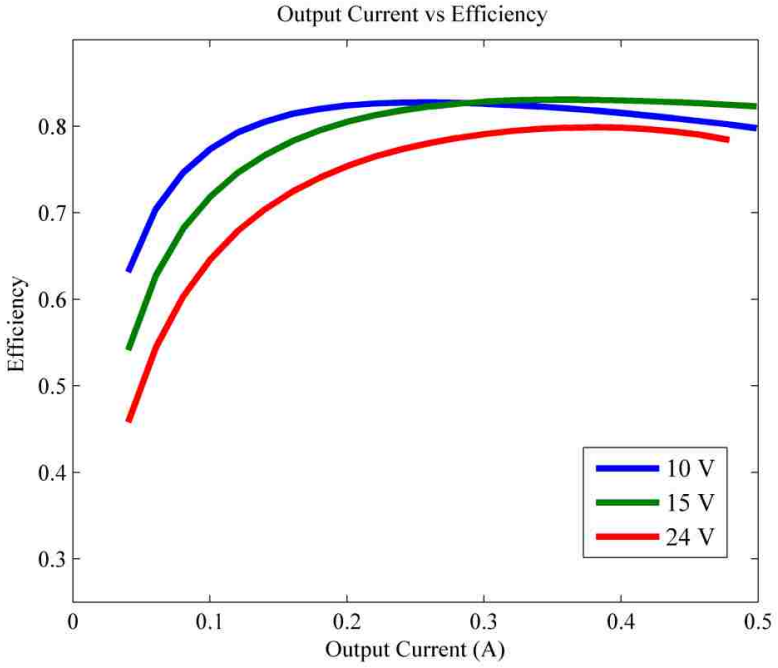

Figure 3.21 Test station efficiency at 150 kHz & 3F3 core

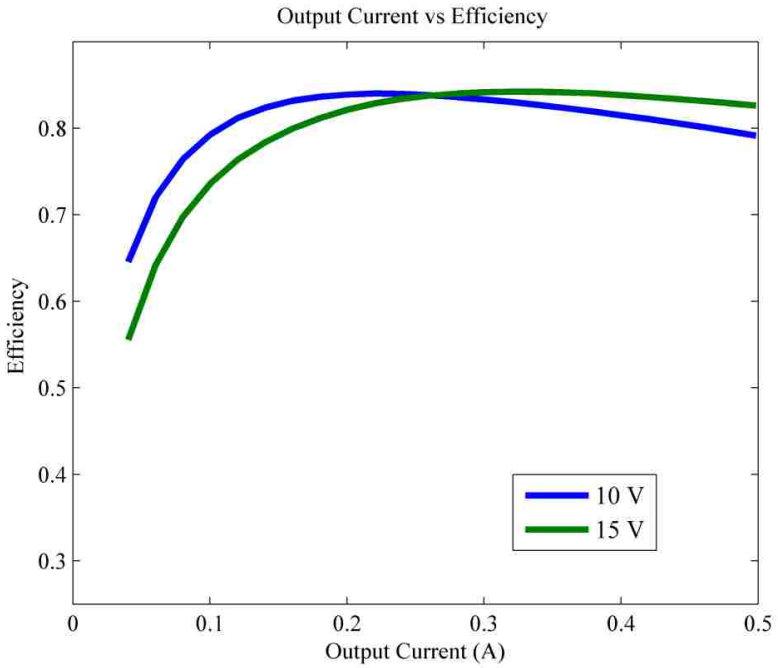

Figure 3.22 Test station efficiency at 200 kHz & 3C90 core

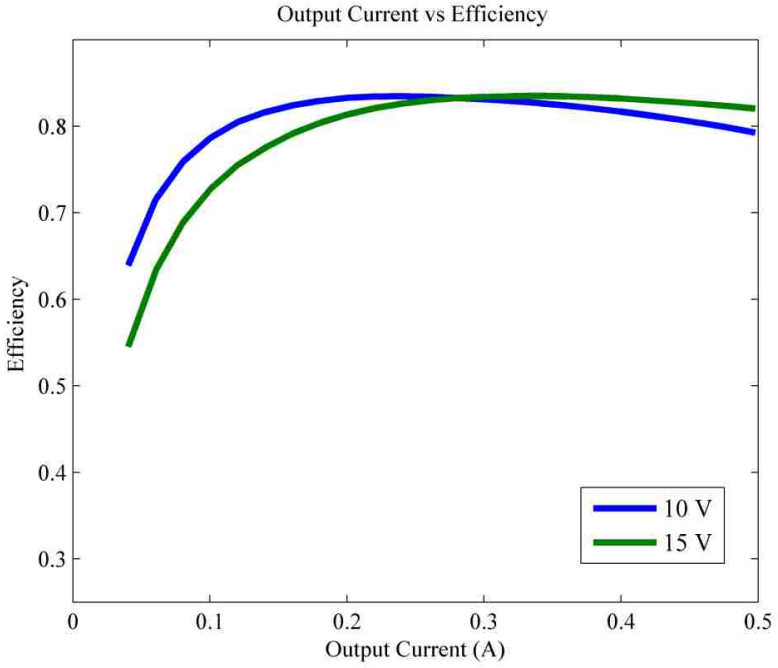

Figure 3.23 Test station efficiency at 200 kHz & 3F3 core

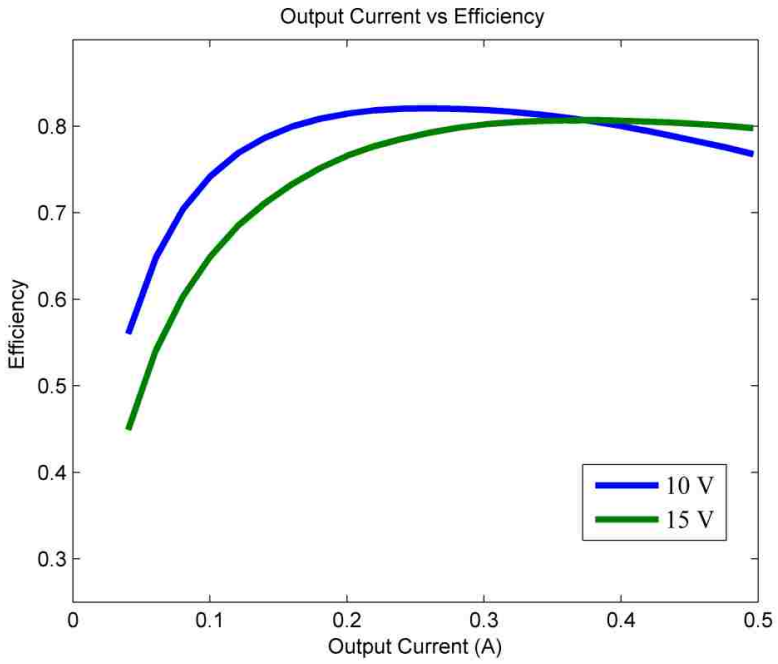

Figure 3.24 Test station efficiency at 250 kHz & 3F3 core

The 24 V measurements for Figures 3.22 through 3.24 were unable to be obtained during the testing period. As the frequency was set to 200 kHz or greater with the input voltage at 24 V the input current would increase to currents above 7.5 A which exceeds the rating of the solar panels and may destroyed the forward converter thus, the test were abandoned.

The highest efficiency voltage, frequency, and core material combination are located in Figure 3.20 at 15 V, 150 kHz, and 3C90 core material at an efficiency of 84.31%. From the estimated calculation in Table 2.8 in Section 2.4, the core power loss for a single transformer was approximately 0.84 W; comparing this with the calculated total transformer loss in Table 2.7, which was 0.191 W, the graphical method of the actual core material gave a better estimated power loss of the transformer. The graphical

analysis may be the better method because the analytical approach to obtain the total power loss begins with the assumption that

$$\frac{R_{ac}}{R_{dc}} = 1$$

In the case of a pair of handmade transformers, this assumption may not be true because the error in constructing as well as the difference in make of both transformers changes this ratio.

The losses in the transformers are probably much greater due to a much higher leakage inductance than expected. By comparing Figures 3.15 (no snubber) and 3.18 (with snubber) the observation can be made that the snubber is able to counteract a small amount of the leakage inductance because the converter had a greater efficiency while the snubber was intact.

The next phase of the experiment was using two forward converters in parallel with two solar panels. A picture of the solar array connection with shaded and non-shaded solar cells is in Figure 3.25 and Figure 3.26, respectively. Figure 3.27 contains the schematic of one solar panel forward converter circuit. The solar testing was performed between 2 p.m. and 3 p.m. on a sunny day (no cloud cover) at a temperature of approximately 56 degrees F. The solar tests were conducted using the LabVIEW program, using voltage instead of current like the efficiency test. The maximum amount of voltage was set to 280 V and the minimum was set to 100 V. The test took 20 steps, thus obtain 20 readings for each experiment conducted. Appendix B has the data collect from the LabView program.

Figure 3.25 Physical non-shaded solar array with forward converters

Figure 3.26 Physical shaded solar array with forward converters

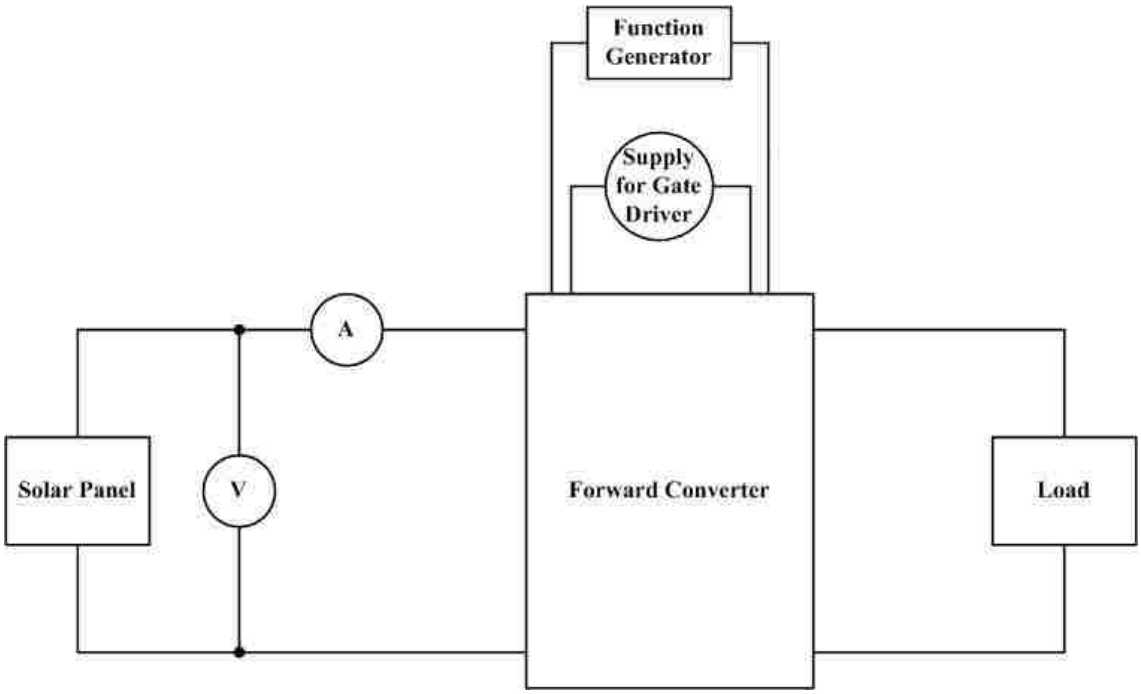

Figure 3.27 Solar array with forward converter schematic

Figure 3.26 was similar to Figure 3.8 with the substitution of a solar panel for the power supply. To confirm that the second converter has a similar efficiency as the first efficiency tests were performed and results can be found in Figure 3.28, which is similar to Figure 3.18.

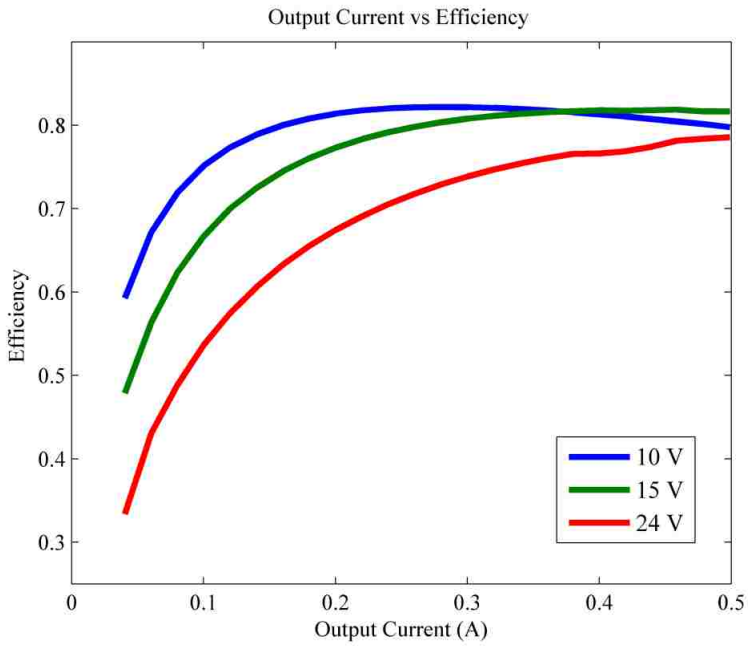

Figure 3.28 Second forward converter efficiency testing at 100 kHz & 3C90 core

To simulate shading a sheet of translucent plastic was used to cover a solar panel, the phrase "shaded 1 time" refers to 1 sheet of plastic. The output voltage versus power curves for the solar panels in parallel were taken, first with no shading for both panels found in Figure 3.29. Next, solar panel 1 was shaded once, twice, and finally three times with panel 2 being non-shaded which can be viewed in Figures 3.30 to 3.32, respectively. Figures 3.33 through 3.35 illustrate the same experiment with panel 2 being shaded and panel 1 being non-shaded.

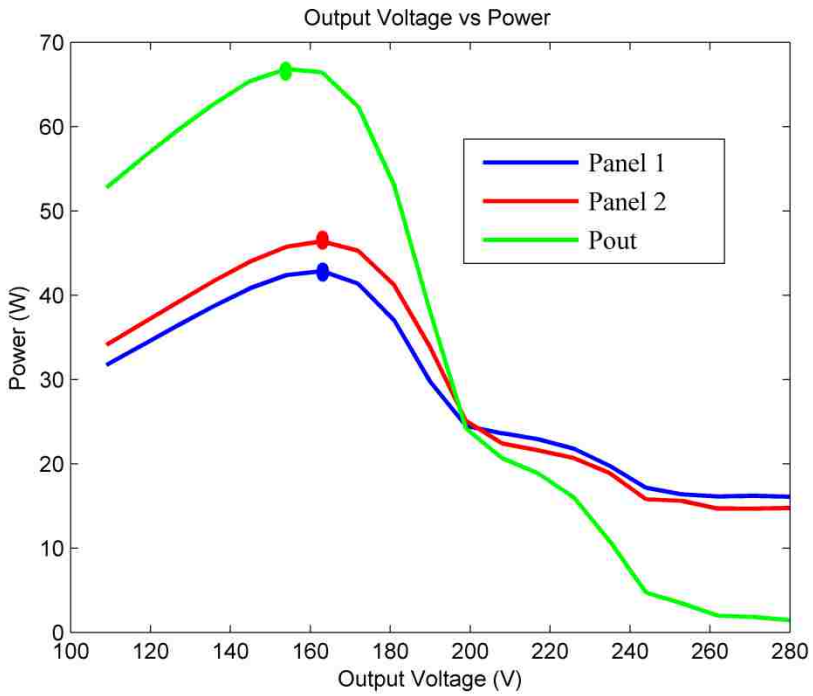

Figure 3.29 Panels 1 and 2 with no shading in the solar array MPP

Figure 3.29 illustrates that panels 1 and 2 were operating at similar conditions with panel 2 being approximately 5 W greater than panel 1. This may be due to the slight difference between the forward converters used in the experiment and/or the difference in the leakage inductance in the transformers in the converters. Panels 1 and 2 both have their MPP at 162.96 V while the output power peaked at 153.96 V the voltage step before panels 1 and 2 illustrates the MPP are almost at the same point. To calculate the percent error of the solar panels the use of

$$\frac{P_{max} - P_{at\ max V_{out}}}{P_{max}} \tag{50}$$

(50) enables the calculation of the percent error at the output voltage where the output power reaches its maximum. For Figure 3.29 panels 1 and 2 approximately 1.39 % and 1.08 % , respectively within the maximum output power.

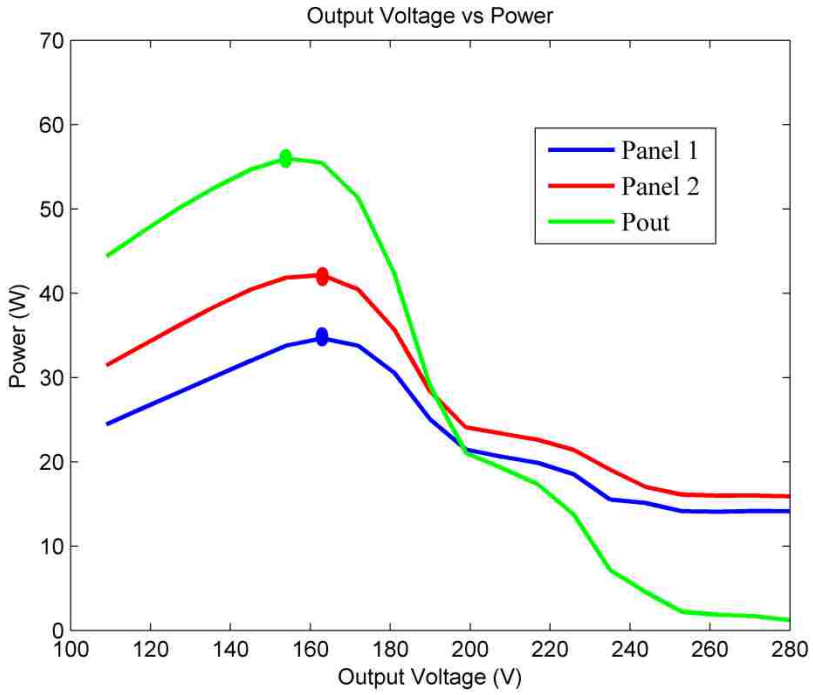

Figure 3.30 Panel 1 shaded once in the solar array MPP

In Figure 3.30 the results are very similar to the non-shaded condition in Figure 3.29 which is expected. Panel 1 illustrates a decrease in power because of the shading but its maximum power point is still congruent with panel 2. Again the output power peaks one step behind the panels and panels 1 and 2 had a 2.47 % and 0.71 % difference in power from the maximum.

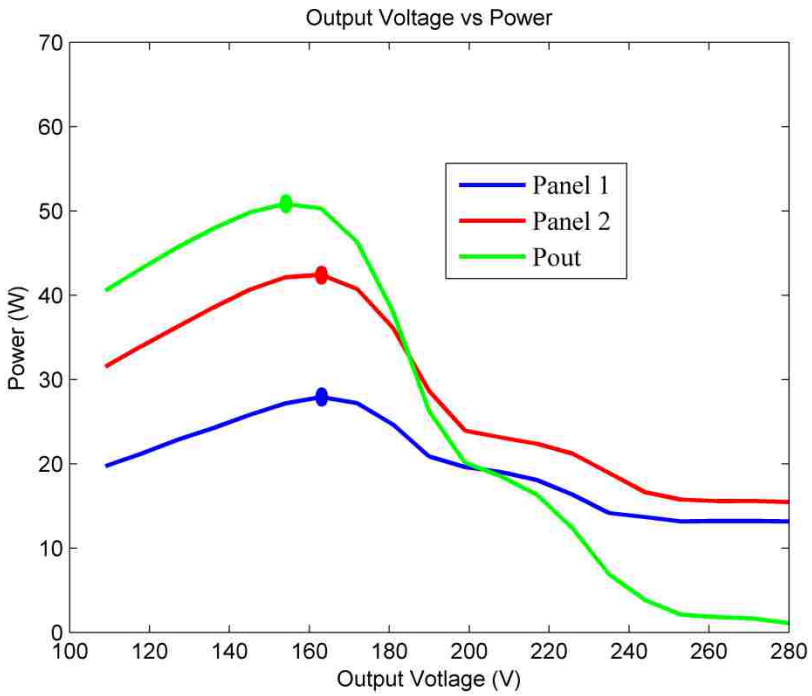

Figure 3.31 Panel 1 shaded twice in the solar array MPP

Figure 3.31 illustrates a similar waveform as Figure 3.30 and 3.29. The decrease in power of panel 1 was more evident greater than the waveform in Figure 3.30 which was expected. From the percent error calculation of (50) panel 1 and 2 are 2.69 % and 0.72 % within the maximum power.

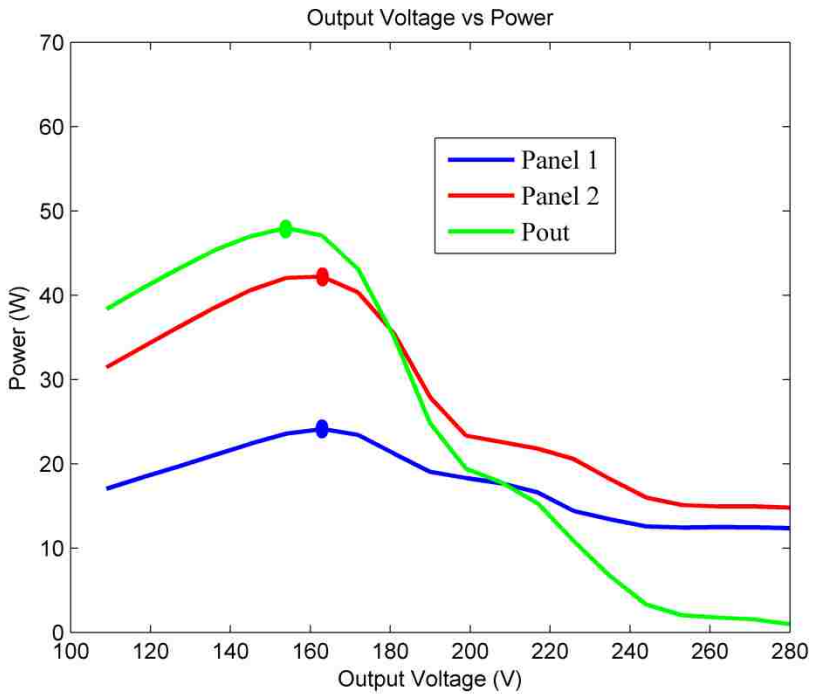

Figure 3.32 Panel 1 shaded three times in the solar array MPP

Finally, Figure 3.32 illustrates panel 1 with 3 shades and the results are similar to the pervious experiments. Panels 1 and 2 are within the maximum output power by 2.25 % and 0.38 %.

Figure 3.33 begins the experiment with panel 2 being shaded and panel 1 with no shade. By shading panel 2 once, the waveform illustrates panels 1, 2 and the output voltage having the same MPP at the same voltage, which was the optimal result of the experiment. This illustrates panel 1 and 2 having a 0 % error for panel 2 shaded one time.

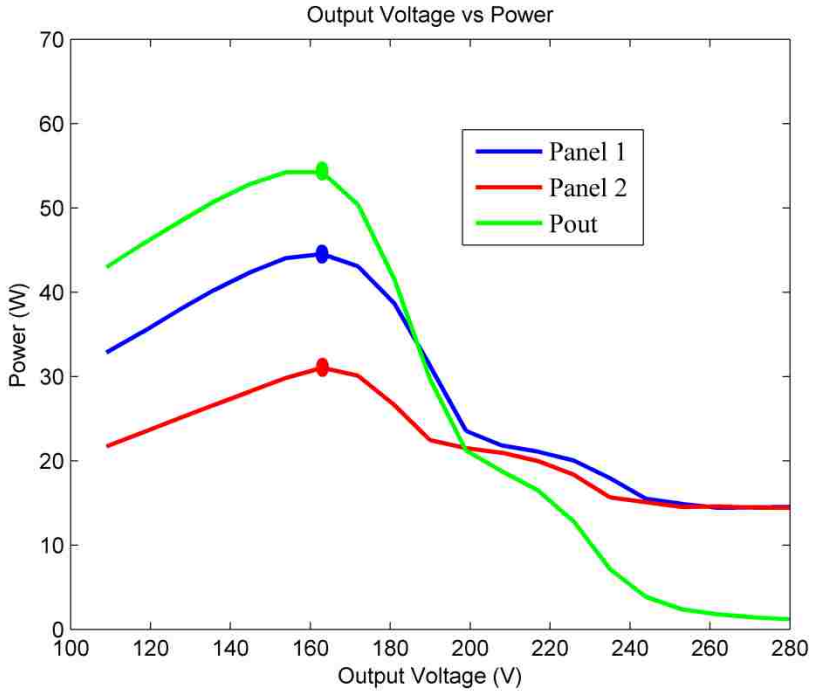

Figure 3.33 Panel 2 shaded once in the solar array MPP

Figure 3.34 is more like the figures where panel 1 was shaded and does not have the excellent results of Figure 3.33. Panels 1 and 2 are within 1.32 % and 3.47 %, respectively, of the maximum output power at the voltage where the output power peaks

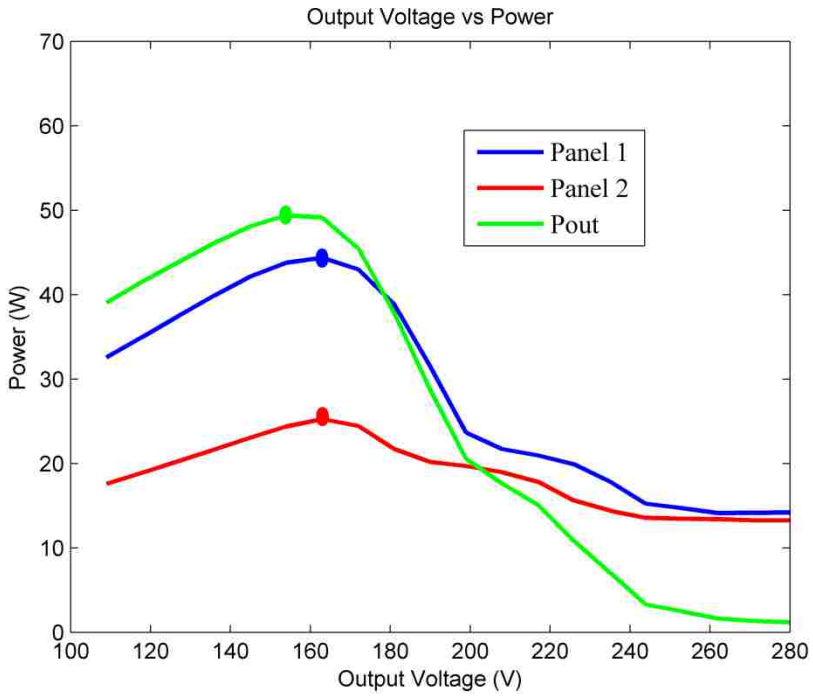

Figure 3.34 Panel 2 shaded twice in the solar array MPP

The final waveform is Figure 3.35 which illustrates panel 2 shaded three times. In this waveform the power of panels 1 and 2 do not follow the trends of the other figures in the experiment. The power of panel 1 seems too high and the power for panel two seems too low, this may be due to the sun changing angles since this was the last test of the day. This also may occur because this test may have fallen on a different point on the efficiency curve then some of the pervious figures. Panels 1 and 2 were 1.43 % and 2.31 % within the maximum output power.

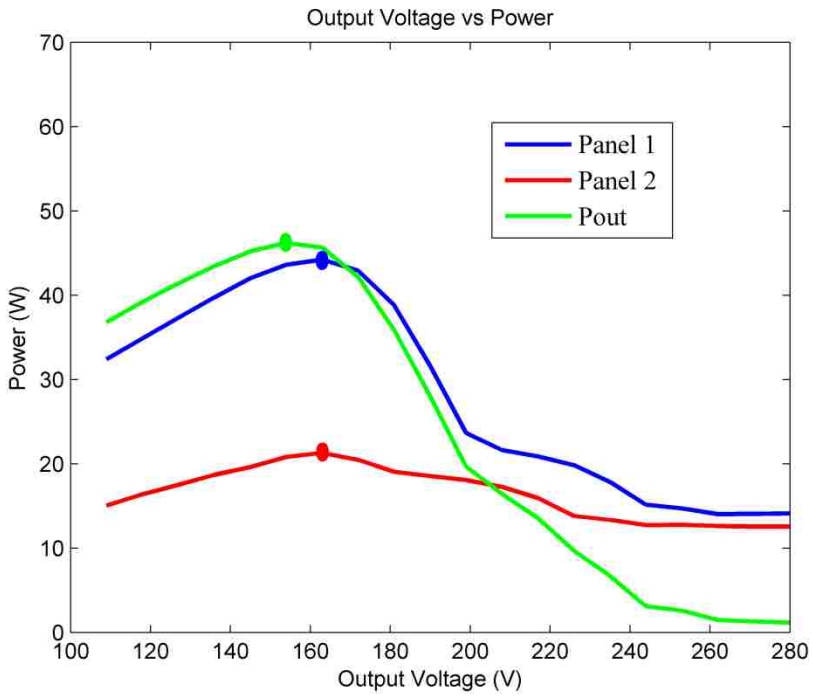

Figure 3.35 Panel 2 shaded three times in the solar array MPP

The data presented in the Figures 3.30 through 3.35 illustrate that the shaded solar panel does not dominate the performance of the PV array. It also can be concluded that the forward converter connected to panel 2 performed better then the converter connected to panel 1 as seen from Figure 3.29, where panel 2 is operating at a higher power than panel 1. Table 3.1 below summarizes the percent error of the maximum output power with the shading of panels 1 and 2.

Table 3.1 Summary of % error of power at maximum output voltage

		% Error of Power at Max V_{Out}	
Shading Panel 1	Shading Panel 2	Panel 1	Panel 2
none	None	1.39%	1.08%
1	None	2.47%	0.71%
2	None	2.69%	0.72%
3	None	2.25%	0.38%
none	1	0%	0%
none	2	1.32%	3.47%
none	3	1.43%	2.31%

4. CONCLUSION

4.1 SUMMARY OF RESULTS

The work completed in this thesis further examined a new method of connection of photovoltaic arrays. This work illustrated that a parallel connect PV array can be a practical approach due to its ability to perform in partially shaded conditions.

A simulation was developed for a two phased forward converter topology that performs fairly accurately to the physical forward converter. The simulation also has conduction losses in the circuit based on the values of the components.

A new type of forward converter was developed within this work by harmonizing different efficiency boosting strategies in hopes of increasing the efficiency of the forward converter. Although that did not occur many positive features were realized such as the snubber circuit, which is able to absorb some of the energy from the leakage inductance of the transformer to increase efficiency.

The abstraction of solar data as well as efficiency testing was completed in the work presented in this document. From the solar data obtained, it is reinforced that the shaded panel does not have a huge negative effect on the solar array.

4.2 EXTENSIONS OF PROJECT

The main issue with the work presented is the efficiency of the forward converters in the solar array. Some extensions to boost the efficiency would be to create or purchase better transformers, since they are a large chunk of the efficiency loss. Also exploring new types of snubbers and different inductor and capacitor combinations could aid in

decreasing the leakage inductance of the transformers. When collecting solar data, it may be more advantageous to increase the step size in LabVIEW to greater than 20 to obtain a better resolution of data points in the maximum power point waveforms. This may lead to obtaining more accurate data and yield the output power MPP from being one step behind the panel 1 and 2 MPP so consistently. Finally, the addition of a control circuit should be looked into for future work of the project.

APPENDIX A.

PRINTED CIRCUIT BOARD DESIGN

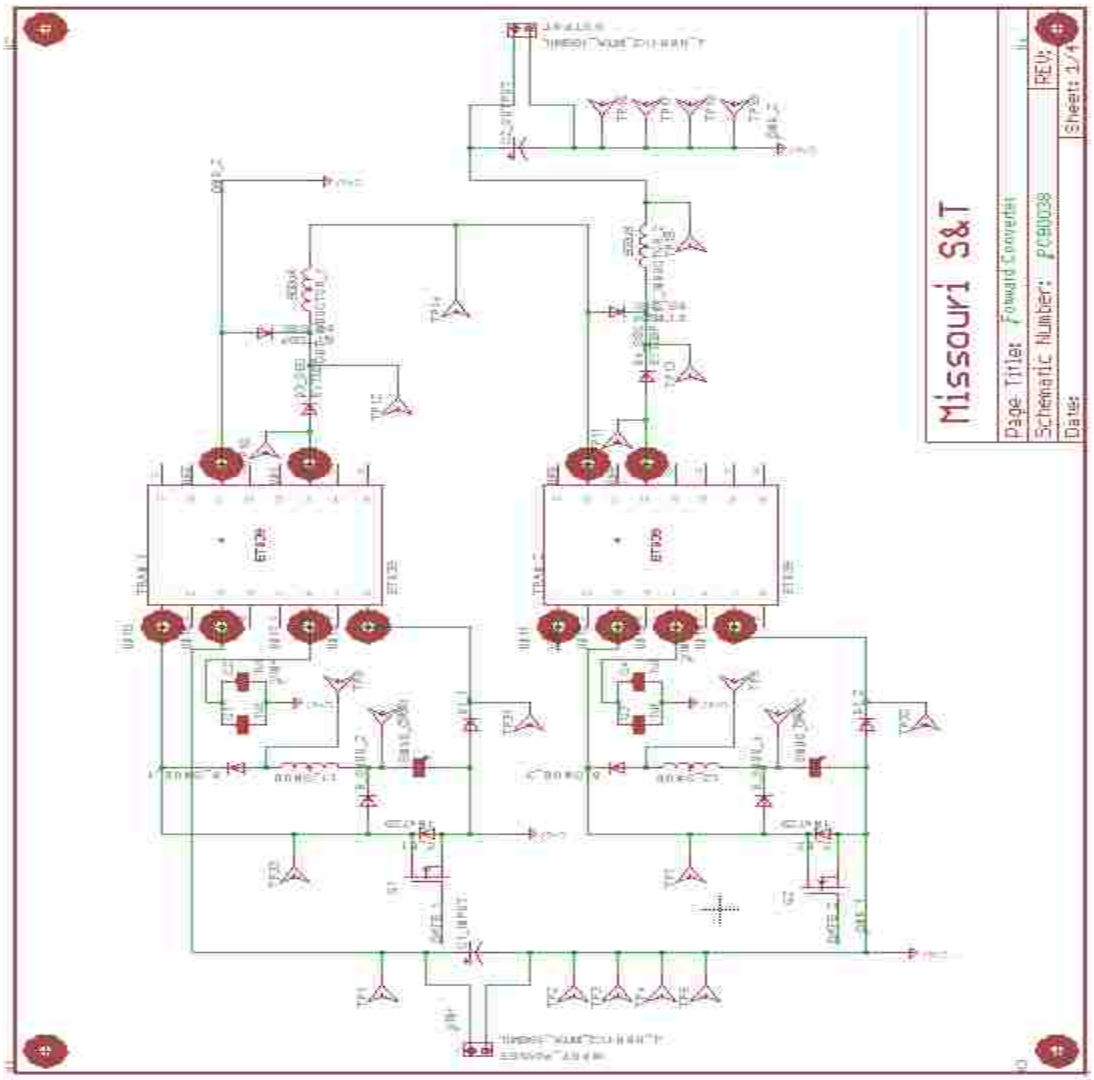

Figure A.1 Sheet 1 forward converter

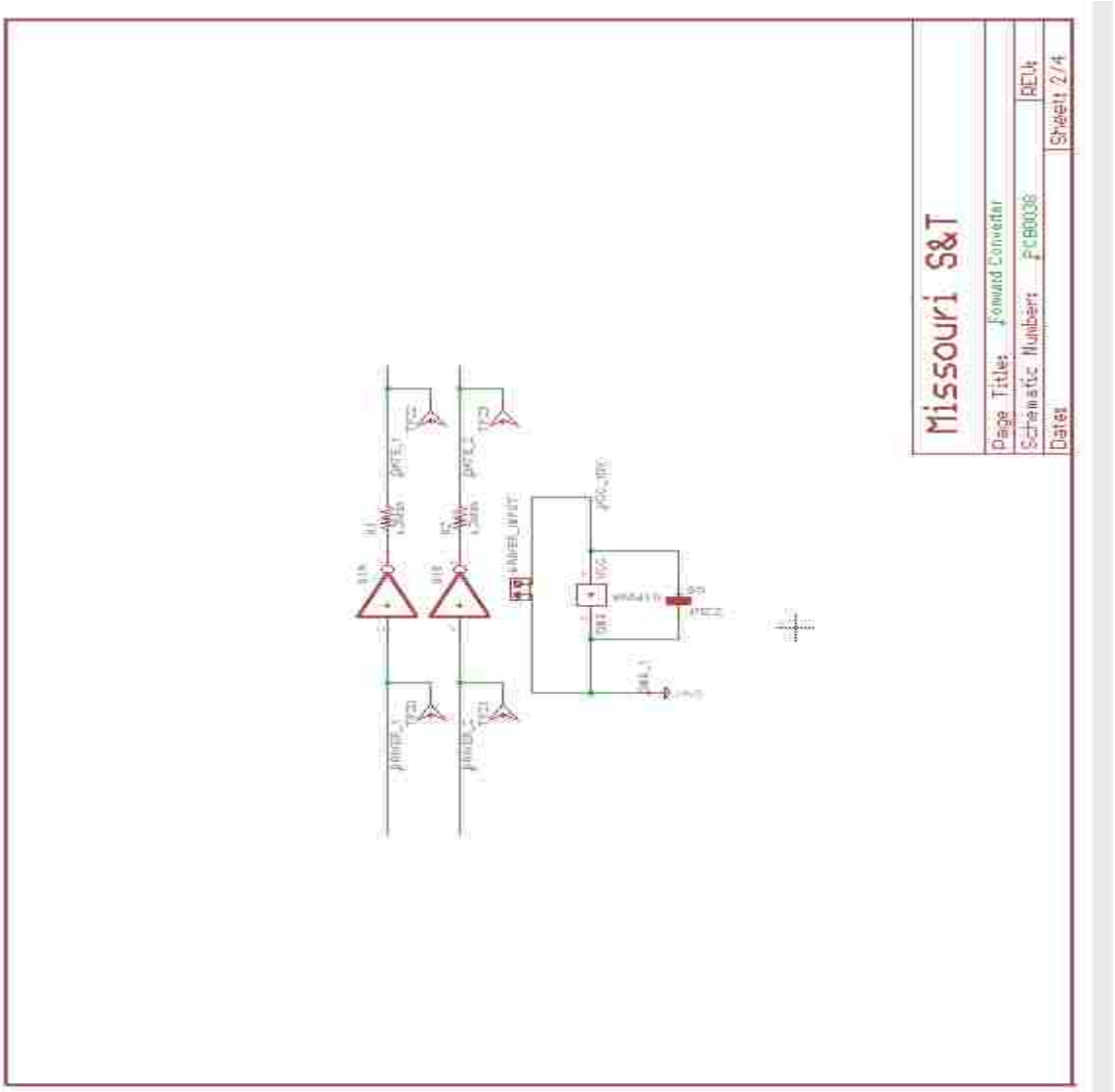

Figure A.2 Sheet 2 gate driver configuration

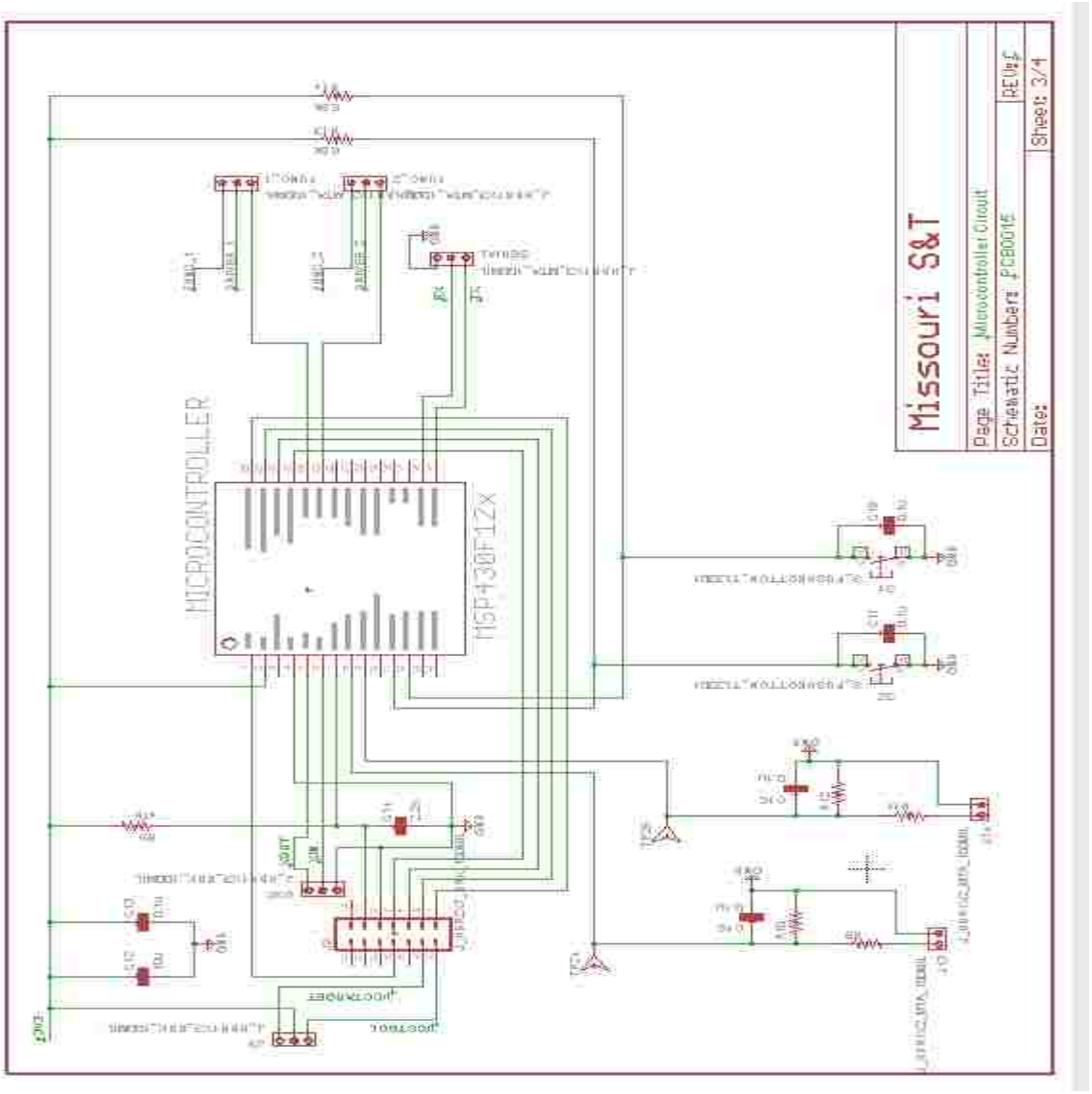

Figure A.3 Sheet 3 microcontroller configuration [31]

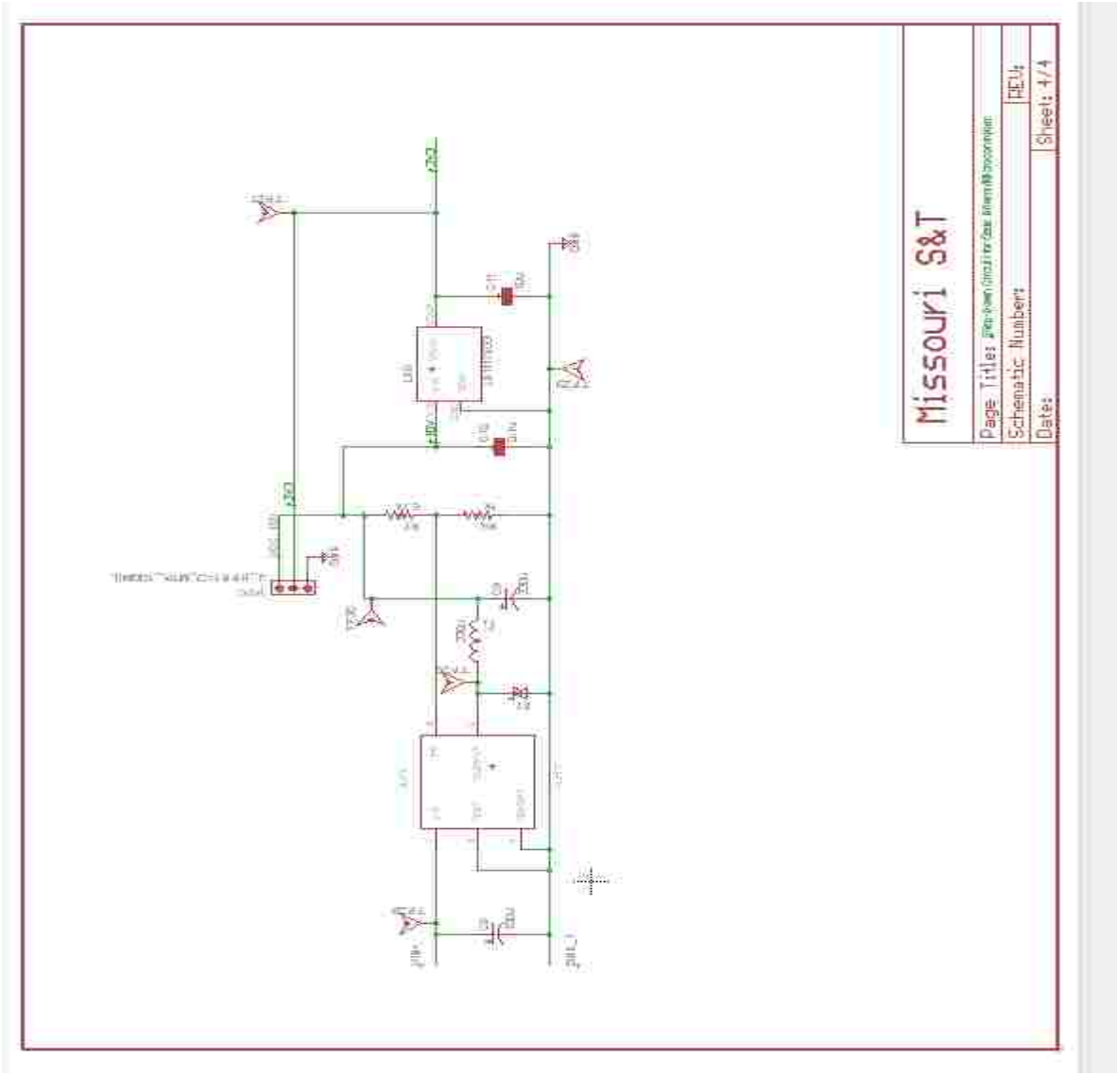

Figure A.4 Sheet 4 step down circuit to Gate Driver/Microcontroller [31]

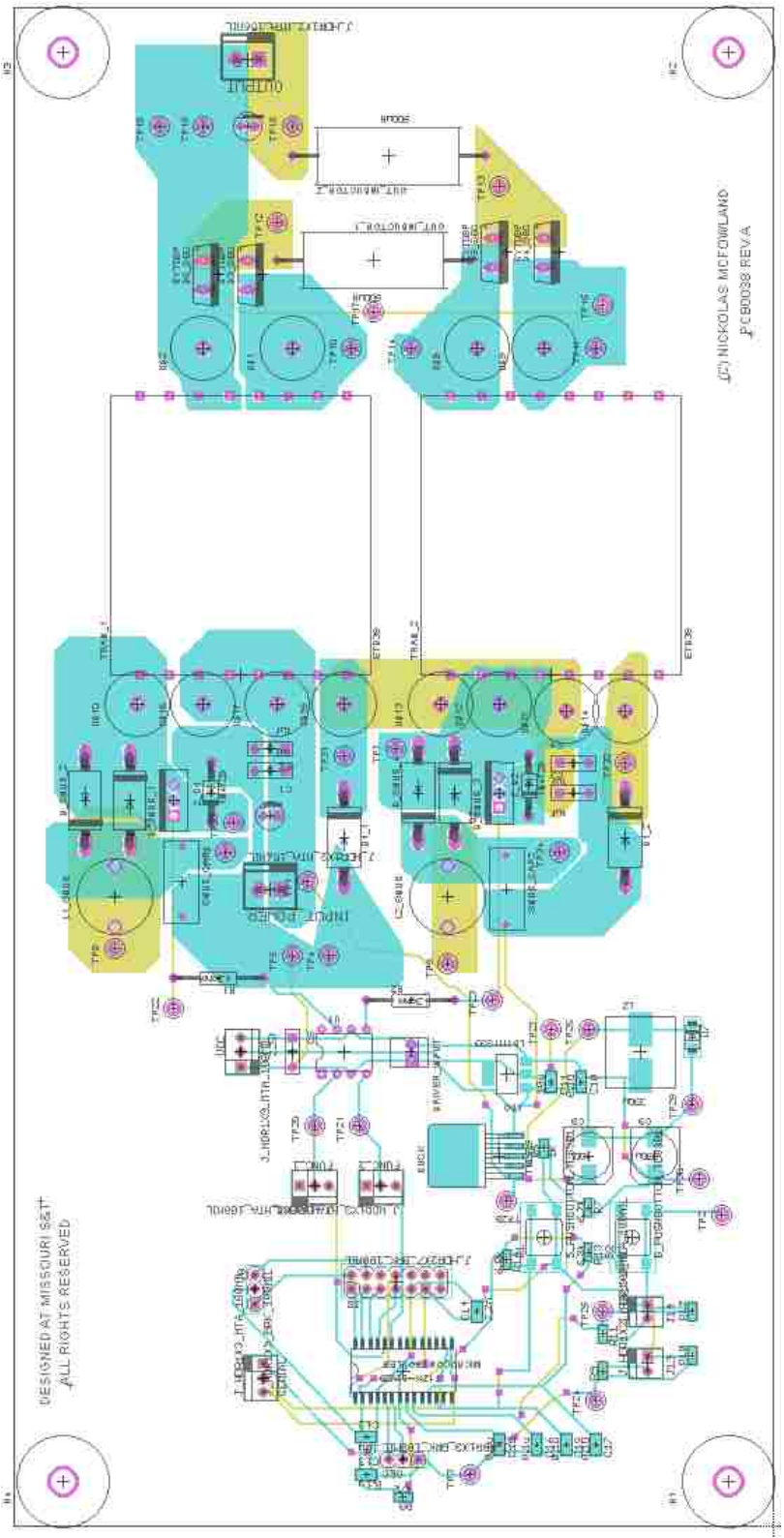

Figure A.5 Physical board layout

APPENDIX B.

SOLAR RESULTS TABLES

Table B.1 Panel 1 non-shaded

I_{In} (A)	V_{In} (V)	I_{Out} (A)	I_{In} (V)
0.887389	18.96364	0.002521	279.954
0.891826	18.9564	0.003929	270.949
0.886203	18.95555	0.004276	261.946
0.928057	18.91945	0.0084	252.945
0.954338	18.89577	0.011143	243.948
1.12781	18.75531	0.02732	234.954
1.222024	18.6747	0.03935	225.959
1.280859	18.62105	0.048193	216.956
1.317033	18.5881	0.054289	207.956
1.38482	18.52532	0.063189	198.9534
1.773945	18.12699	0.101406	189.9495
2.221937	17.49064	0.145828	180.9541
2.539051	16.75945	0.178985	171.9577
2.717333	15.97609	0.199486	162.9598
2.811025	15.16672	0.212092	153.9619
2.853373	14.34215	0.21992	144.9644
2.870926	13.51131	0.224963	135.9585
2.87457	12.67615	0.22927	126.9574
2.878393	11.84217	0.233174	117.9545
2.878322	11.00701	0.23709	108.9628

Table B.2 Panel 2 non-shaded

I_{In} (A) (P1)	V_{In} (V) (P1)	I_{Out} (A)	I_{In} (V)
0.798096	19.66682	0.003175	279.955
0.793233	19.69832	0.003414	270.949
0.791499	19.6956	0.003779	261.946
0.838482	19.65848	0.008328	252.944
0.84781	19.65099	0.009517	243.948
1.008641	19.52459	0.023877	234.954
1.102155	19.44712	0.03473	225.958
1.151174	19.40542	0.041385	216.956
1.192628	19.37188	0.047239	207.955
1.335979	19.24741	0.062213	198.9558
1.830183	18.73703	0.108944	189.9512
2.296406	18.06536	0.154182	180.9544
2.624271	17.30977	0.187492	171.9573
2.822339	16.50481	0.208642	162.9609
2.922256	15.67068	0.221647	153.9604
2.96931	14.79263	0.228883	144.9642
2.98547	13.96154	0.233842	135.9588
2.990037	13.09967	0.237483	126.9587
2.995187	12.2083	0.241369	117.9541
2.996567	11.37084	0.24486	108.9626

Table B.3 Panel 1 and 2 non-shaded solar array

I_{In} (A) (P2)	V_{In} (V) (P2)	I_{In} (A) (P1)	V_{In} (V) (P1)	I_{Out} (A)	I_{In} (V)
0.858384	18.76208	0.749905	19.6952	0.005195	279.955
0.864316	18.75994	0.747012	19.6709	0.006805	270.949
0.860657	18.75977	0.746482	19.69757	0.007668	261.945
0.874096	18.74789	0.794494	19.66048	0.013676	252.946
0.9181	18.71258	0.805296	19.62246	0.01943	243.95
1.061888	18.5993	0.96724	19.5238	0.046102	234.956
1.178045	18.50317	1.064422	19.44695	0.070888	225.958
1.243569	18.447	1.115095	19.37571	0.087045	216.956
1.283925	18.41229	1.158669	19.36873	0.099499	207.954
1.33379	18.3697	1.305173	19.24354	0.121691	198.9547
1.648474	18.06671	1.80841	18.7365	0.20056	189.9521
2.122477	17.45865	2.282192	18.06396	0.293195	180.9562
2.47136	16.74298	2.61634	17.30869	0.3627	171.9574
2.683972	15.96984	2.816477	16.47642	0.40783	162.9599
2.795998	15.16515	2.919557	15.67387	0.434198	153.9605
2.847789	14.34369	2.968966	14.82463	0.451317	144.9637
2.867991	13.51242	2.988025	13.96569	0.461331	135.9595
2.876027	12.67819	2.992881	13.1035	0.469706	126.9582
2.879011	11.84288	2.997125	12.23951	0.477217	117.9556
2.88219	11.00598	2.999969	11.37334	0.484444	108.9629

Table B.4 Panel 1 with one shaded solar array

I_{In} (A) (P2)	V_{In} (V) (P2)	I_{In} (A) (P1)	V_{In} (V) (P1)	I_{Out} (A)	I_{In} (V)
0.853957	18.64998	0.737403	19.20076	0.004408	279.954
0.859265	18.64552	0.73845	19.19722	0.006322	270.947
0.858302	18.64806	0.734398	19.20105	0.007153	261.947
0.865023	18.64192	0.737909	19.19464	0.008793	252.945
0.915198	18.60319	0.789744	19.14345	0.018628	243.95
1.031589	18.51437	0.813346	19.11818	0.030581	234.954
1.163796	18.40801	0.977968	18.94592	0.060825	225.958
1.232173	18.35077	1.05409	18.86201	0.079917	216.957
1.275395	18.31331	1.096281	18.81081	0.092638	207.955
1.318024	18.27219	1.145546	18.74903	0.10581	198.9554
1.575358	18.02202	1.356871	18.46912	0.152863	189.9497
2.050338	17.43108	1.714555	17.84058	0.23445	180.9548
2.418678	16.7271	1.976237	17.0958	0.298414	171.9582
2.641496	15.95957	2.127877	16.28766	0.340451	162.96
2.761511	15.15709	2.18832	15.4468	0.363749	153.9605
2.820545	14.33616	2.193017	14.58761	0.377041	144.9651
2.843515	13.50514	2.194653	13.7256	0.386261	135.9611
2.854069	12.6698	2.194421	12.86429	0.39427	126.9603
2.857068	11.83283	2.196405	12.00117	0.400879	117.9542
2.859124	10.99592	2.196542	11.135	0.407305	108.9612

Table B.5 Panel 1 with two shaded solar array

I_{In} (A) (P2)	V_{In} (V) (P2)	I_{In} (A) (P1)	V_{In} (V) (P1)	I_{Out} (A)	I_{In} (V)
0.827449	18.6925	0.699077	18.86755	0.003951	279.955
0.834945	18.68979	0.702844	18.83559	0.006154	270.95
0.834291	18.69207	0.701352	18.86387	0.006996	261.947
0.84444	18.68283	0.699162	18.86394	0.008401	252.945
0.892856	18.6467	0.727447	18.83054	0.015797	243.951
1.020775	18.5463	0.754153	18.79385	0.029492	234.955
1.149263	18.44372	0.877324	18.63354	0.054549	225.958
1.217501	18.38529	0.978109	18.48824	0.075301	216.957
1.260564	18.3488	1.033798	18.40182	0.089108	207.955
1.307175	18.30779	1.070186	18.34412	0.101251	198.9544
1.588655	18.03853	1.147393	18.20887	0.138393	189.9515
2.070615	17.44442	1.395397	17.67229	0.210207	180.9567
2.434223	16.73577	1.605784	16.94613	0.269347	171.958
2.658136	15.96667	1.729532	16.14719	0.30875	162.9607
2.778758	15.16393	1.774956	15.31012	0.330232	153.9599
2.834609	14.34172	1.785699	14.45713	0.343629	144.9648
2.854279	13.50896	1.783951	13.59851	0.352378	135.9587
2.861114	12.67348	1.793823	12.74101	0.359855	126.9578
2.86818	11.83757	1.785752	11.88085	0.366036	117.9551
2.866517	10.99845	1.792064	11.01987	0.372348	108.9646

Table B.6 Panel 1 with three shaded solar array

I_{In} (A) (P2)	V_{In} (V) (P2)	I_{In} (A) (P1)	V_{In} (V) (P1)	I_{Out} (A)	I_{In} (V)
0.79357	18.67616	0.664673	18.63197	0.003563	279.954
0.801076	18.66642	0.669721	18.62463	0.005796	270.948
0.801595	18.66575	0.671315	18.62166	0.00682	261.946
0.810465	18.65711	0.668198	18.6247	0.008107	252.945
0.860668	18.61817	0.676286	18.61246	0.013689	243.95
0.983337	18.52486	0.724245	18.54415	0.028573	234.955
1.11641	18.41657	0.781164	18.45724	0.047952	225.958
1.187356	18.35961	0.910423	18.23833	0.070493	216.957
1.232411	18.32223	0.977045	18.1105	0.085464	207.955
1.277974	18.28011	1.016217	18.03088	0.097564	198.9528
1.548328	18.02394	1.063172	17.9275	0.130745	189.9512
2.034014	17.43343	1.209827	17.54754	0.193754	180.9567
2.410358	16.73024	1.392371	16.83687	0.250591	171.958
2.644935	15.96417	1.503943	16.05111	0.288863	162.9615
2.774072	15.16272	1.550003	15.22396	0.311761	153.9608
2.831835	14.34097	1.557386	14.37379	0.324109	144.9647
2.852162	13.50657	1.556695	13.51865	0.333381	135.9599
2.858396	12.67091	1.555743	12.66146	0.339712	126.9576
2.858734	11.83354	1.558619	11.80299	0.346236	117.9543
2.860499	10.99592	1.558131	10.94369	0.352107	108.9635

Table B.7 Panel 2 with one shaded solar array

I_{In} (A) (P2)	V_{In} (V) (P2)	I_{In} (A) (P1)	V_{In} (V) (P1)	I_{Out} (A)	I_{In} (V)
0.791961	18.22942	0.744569	19.52899	0.004373	279.954
0.793033	18.22686	0.742311	19.52899	0.005316	270.948
0.801147	18.21644	0.739106	19.52907	0.006892	261.947
0.797772	18.21872	0.76341	19.50852	0.009492	252.946
0.830703	18.18659	0.795954	19.48403	0.015864	243.95
0.863798	18.15227	0.927025	19.37914	0.03051	234.955
1.020086	17.98064	1.039078	19.28621	0.056569	225.958
1.117888	17.86668	1.09639	19.23756	0.076093	216.957
1.178787	17.78896	1.135847	19.20499	0.090226	207.955
1.21288	17.74056	1.232881	19.11596	0.106686	198.9556
1.272038	17.66381	1.675306	18.66619	0.156244	189.9503
1.54896	17.20976	2.149527	18.01502	0.230049	180.9543
1.821118	16.52333	2.494306	17.26781	0.292929	171.9591
1.970661	15.75627	2.704167	16.46901	0.332899	162.9596
1.998806	14.93805	2.81766	15.64018	0.352364	153.961
2.001467	14.10921	2.870239	14.7636	0.364603	144.9644
2.006558	13.27918	2.890057	13.93412	0.373473	135.96
2.008689	12.44656	2.896292	13.07178	0.380396	126.9587
2.011265	11.61404	2.896021	12.18027	0.387496	117.9562
2.015343	10.77846	2.896544	11.34259	0.394385	108.9655

Table B.8 Panel 2 with two shaded solar array

I_{In} (A) (P2)	V_{In} (V) (P2)	I_{In} (A) (P1)	V_{In} (V) (P1)	I_{Out} (A)	I_{In} (V)
0.741108	17.92104	0.726587	19.55033	0.004272	279.954
0.741371	17.92047	0.725137	19.55341	0.005039	270.949
0.748955	17.90899	0.723378	19.55577	0.006291	261.946
0.752149	17.90688	0.753626	19.53766	0.009889	252.946
0.7586	17.89811	0.781838	19.48854	0.013507	243.95
0.809055	17.83326	0.920474	19.409	0.030218	234.953
0.881059	17.73336	1.030888	19.31725	0.047966	225.956
1.018211	17.52948	1.087933	19.27032	0.06958	216.955
1.090406	17.40611	1.128857	19.23678	0.084863	207.956
1.138165	17.32232	1.235785	19.14578	0.103452	198.9534
1.170013	17.26201	1.688885	18.67994	0.151435	189.951
1.275942	17.03099	2.157767	18.02129	0.209241	180.9559
1.493549	16.37645	2.490774	17.27014	0.264666	171.9573
1.617504	15.62162	2.694871	16.46955	0.301549	162.9625
1.646659	14.81293	2.800482	15.63932	0.321068	153.962
1.648445	13.99532	2.850369	14.7903	0.331798	144.9647
1.644708	13.16672	2.863906	13.93151	0.339207	135.9593
1.644723	12.34006	2.867388	13.06745	0.345396	126.9582
1.644261	11.51075	2.867883	12.20275	0.352365	117.9551
1.647596	10.68033	2.872444	11.33794	0.358518	108.9634

Table B.9 Panel 2 with three shaded solar array

I_{In} (A) (P2)	V_{In} (V) (P2)	I_{In} (A) (P1)	V_{In} (V) (P1)	I_{Out} (A)	I_{In} (V)
0.713694	17.60888	0.720745	19.59629	0.004195	279.954
0.713704	17.60849	0.718684	19.59758	0.004843	270.948
0.717445	17.60285	0.716824	19.59565	0.005657	261.946
0.726386	17.58833	0.752552	19.56712	0.010294	252.945
0.724401	17.59005	0.774953	19.54639	0.012768	243.949
0.762223	17.53102	0.918817	19.43109	0.028587	234.954
0.791016	17.48087	1.026651	19.33926	0.042967	225.958
0.925748	17.23312	1.082397	19.29198	0.062532	216.958
1.01398	17.03962	1.123717	19.25815	0.079037	207.956
1.069788	16.90412	1.235258	19.15823	0.099089	198.9535
1.104009	16.81349	1.694797	18.68191	0.147698	189.9508
1.141639	16.69953	2.155021	18.01928	0.198263	180.9561
1.261555	16.24495	2.486228	17.26645	0.245236	171.957
1.374316	15.50723	2.686814	16.46422	0.280249	162.9598
1.414845	14.71463	2.790329	15.63245	0.300235	153.9599
1.411623	13.90233	2.842982	14.78561	0.312019	144.9643
1.429044	13.08694	2.853384	13.92549	0.319714	135.9579
1.428572	12.26612	2.857053	13.0633	0.326164	126.9586
1.433357	11.44305	2.859426	12.19956	0.332507	117.9549
1.419083	10.61025	2.860806	11.33361	0.337795	108.9643

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