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Solid state fault interruption devices in medium voltage distribution systems with distributed generators

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Department:

SOLID STATE FAULT INTERRUPTION DEVICES IN MEDIUM VOLTAGE DISTRIBUTION SYSTEMS WITH DISTRIBUTED GENERATORS

by

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ABSTRACT

Faults in electric power grids often result in long term interruption of electricity supply. The frequent and the sudden occurrences of faults undermine the reliability and continuity of electric networks However, the new age digital economy demands a continuous supply of electricity of high power quality. This demand of continuous supply and the effort to increase the penetration of renewable power sources into the electric grid has led to a need of highly efficient and flexible systems with the ability to provide power of very high quality. The solid state fault interruption device (SSFID) is one amongst those devices. It is used to quickly isolate sections of the networks where permanent faults have occurred.

The development and simulated testing of a SSFID to validate its use in future medium voltage transmission systems is discussed. Also, the effects of using these SSFIDs in such systems during faults are investigated.

ACKNOWLEDGMENTS

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1. INTRODUCTION

1.1. BACKGROUND

Power systems must operate with optimum economy, reliability and power quality. Historically, the reliability of a network has been measured by its ability to supply electricity with the lowest possible frequency and duration of interruptions throughout the year. The cost of supplying electricity is measured by the combined cost of generating and distributing electricity. With the advent of the digital economy, it has now become imperative to have strict control over the quality of electricity supplied to the customer. With the advent of deregulation and, in some cases, re-regulation, the meaning of reliability and cost of delivering electricity has taken a whole new meaning. It is now required that the electricity supply has excellent quality of voltage and current at all times, which usually increases the cost. Momentary interruptions are now considered part of system reliability indices and thereby actions must be taken to reduce the impact of momentary events.

Precisely for this purpose, the National Science Foundation has launched the experimental Future Renewable Electric Energy Delivery and Management (FREEDM) system. The FREEDM system makes use of the assimilation of the innovations in semiconductor technology to improve the adoption of renewable technologies as well as to improve the performance of the network. This is achieved by not only making use of the newest semiconductor, but also innovations in control and communications and distributed generation technologies. The semiconductor technology being used for the FREEDM project allows very fast switching and high blocking capacity even at medium voltage levels. This has proven to be a boon with the ability to limit fault currents and

almost instantaneous isolation of faulted sections from the network which was hitherto impossible with conventional transformers and circuit breakers. The immediate isolation of faulted sections has made it possible to have high power quality even in the cases of faults. Precisely for this purpose, the Solid State Circuit Breaker (SSCB)/ Solid State Fault Interruption Device (SSFID) has been developed. The SSFID eliminates the problems of deep voltage sags that occur during faults in a distribution network when conventional circuit breakers are used

The objective of this thesis is to demonstrate that the SSFID is a superior alternative to the contemporary mechanical circuit breaker used in power systems. This thesis proves that the SSFID is much faster at isolating faulted sections of an electric network resulting in better power quality. The SSFID has been subjected to simulated tests where it has been tested for its interrupting capabilities to validate its use in medium voltage distribution systems. A comparison of effects in a medium voltage distribution system with distributed generators having SSFIDs or circuit breakers during faults has been done.

1.2. SOFTWARE USED

Although there are various simulation tools available in the market like MATLAB based Simulink and SimPower Systems, ASPEN's DistriView etc, PSCAD (Power Systems Computer Aided Design) was chosen for performing the simulated tests and studying the distribution system for transients during faults. Another reason was to maintain the uniformity of software used by the team members of the Fault Isolation Device Sub-thrust team of the FREEDM project.

1.3. OUTLINE OF THESIS

This thesis is divided into five sections. The first section introduces the need for SSFID.

The second section introduces important terms pertinent to the development of a circuit breaker. This section also presents the various testing methods presently used for the development and validation of circuit breakers.

The third section deals with the development of the SSFID, its efficiency and speed performance. It also deals with the tests proposed for the development of the SSFID.

Section four deals with the effects of using SSFIDs on faults in a microgrid test system. Section five presents the conclusions drawn from this work.

2. CIRCUIT BREAKERS IN POWER SYSTEMS

2.1. BACKGROUND

A circuit breaker (CB) is a mechanical device capable of making, carrying and breaking currents under normal circuit conditions and also making, carrying for a specific time and breaking currents under specific abnormal circuit conditions such as those like short circuits [1]. They are used in all sections of an entire power system, i.e., generation, transmission, and distribution for protection purposes. They are switched open during undesirable conditions in a power system which may cause excessive currents to flow and hence cause damage to components of the power system.

The selection of a circuit breaker depends on its application and is decided by its ratings. The rating of a circuit breaker is a designated limit of operating characteristics that is based upon the usual service conditions [2]. The commonly used ratings for the selection of circuit breakers are [2]:

2.1.1 Rated Maximum Voltage. It is the highest rms phase-to-phase voltage for which the circuit breaker is designed, and is the upper limit for operation

2.1.2 Rated Power Frequency. It is the frequency at which it is designed to operate. The standard frequencies are 50 Hz or 60 Hz

2.1.3 Rated Continuous Current. It is the established limit of current in rms amperes at rated power frequency that it shall be required to carry continuously without exceeding any of the limitations designated in [2].

2.1.4 Rated Dielectric Withstand Capability. It is the voltage withstand capability when voltages of specified magnitudes and wave-shapes are applied under specified conditions [3].

2.1.5 Rated Power Frequency Withstand Voltage. It is the rms voltage that the circuit breaker can withstand when tested under conditions given in [3].

2.1.6 Lightning Impulse Test Voltage. It is the peak voltage that a circuit breaker must withstand when a standard 1.2/50 μs lighting impulse voltage wave is applied to it under conditions specified in [3].

2.1.7 Required Symmetrical Interrupting Capability. It is the value of the symmetrical component of the short-circuit current in rms amperes at the instant of arcing contact separation that the CB shall be required to interrupt at a specified operating voltage, on the standard operating duty cycle, and with a direct current component of less than 20 % of the current value of the symmetrical component [2].

2.1.8 Required Asymmetrical Interrupting Capability. It is the value of the total rms short-circuit current I_t at the instant of the arcing contact separation that the CB will be required to interrupt at a specified operating voltage and on the standard operating duty cycle [2]. This value is determined from the rated value of the symmetrical component and the direct component of the current expressed as a percentage of the peak value of the symmetrical current $I_{sym.}$

$$I_t = I_{sym}\sqrt{1+2\left(\frac{\%dc}{100}\right)^2} \tag{2.1}$$

2.1.9 Rated Transient Recovery Voltage (TRV). It is the maximum voltage that a CB can withstand when it interrupts three-phase grounded and ungrounded terminal faults at the rated short circuit current at the rated maximum voltage.

2.2. TESTING OF CBs

Design testing is an important stage in the development of any kind of switchgear equipment. The CB has to be subjected to design tests to confirm whether it will be able to withstand the interrupting duty during faults. Only after a CB has been design tested, the type of CB is certified to be used in power systems.

2.2.1 Direct Tests. In this method, the CB is tested on a three phase system, and at a short circuit MVA equal to its full rating i.e. on a three phase circuit at full current and at full voltage [1].

2.2.2 Indirect Tests. These tests permit the use of alternate test methods to demonstrate the capabilities of the CB in three-phase grounded and ungrounded systems [1].

The methods commonly employed are:

1. Single phase tests
2. Unit tests
3. Synthetic tests

2.2.2.1 Single phase tests. The testing of an individual interrupter of a three phase breaker is considered perfectly acceptable irrespective of whether it has been tested by a three–phase or a single-phase source as long as it is subjected to the same voltage and currents that are present during faults. In a three phase application, at the instant of current zero, or in the phase where the current interruption is about to take place, the interrupter itself does not know that there are two phases lagging behind this phase. If the first phase fails to interrupt the current at the current zero, the next sequential phase will attempt to clear the circuit. Thus, there is a higher probability of successfully interrupting

a three phase current than a single phase fault. The interruption in the three phases is shown in Figure 2.1. As shown in the diagram, attempts are made to interrupt the current in phase B, followed by A and, finally, current is interrupted in phase C. The other two phases interrupt current simultaneously at A-B.

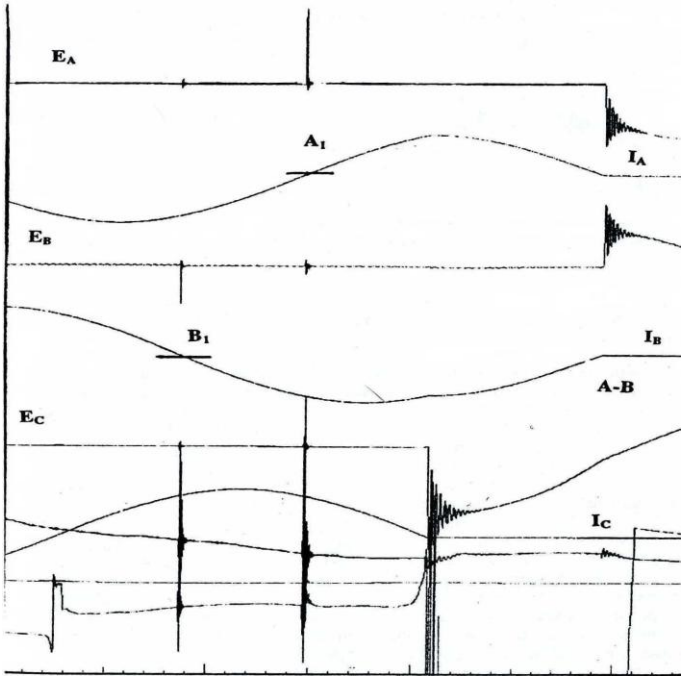


Figure 2.1. Single Phase Tests -Current Waveforms for Phases a, b, and c.

Since in a three phase circuit, the high frequency oscillations of the load side TRV die down and before the other two phases interrupt the current, the source side power frequency recovery voltage is reduced to 87%of the line-to-line voltage, due to neutral shift, it is necessary to ensure that a proper transient recovery voltage is applied across the interrupter while testing.

After the currents in all three phases are interrupted, the voltage in each phase becomes equal to the line-to-neutral voltage which corresponds to 58% of line-to- line voltage. This reduction takes approximately 4 milliseconds which is long enough to justify that the CB has gained its full dielectric capability. Possible effects of electromechanical forces produced by the currents and of gas exhaust from adjacent poles should also be considered while designing and testing.

2.2.2.2 Unit tests. This method is a variation of the single phase test method and is used for validate the interrupting capability of a single interrupter in multiple interrupter pole [1]. This test is performed at full rated short circuit current and at a voltage level that is equivalent to the ratio of the number of interrupters used in pole assembly to the full rated voltage of the complete pole. The distributed voltage must be properly adjusted to compensate for the uneven voltage distribution that exists across each series interrupter unit due to stray capacitances (between adjacent poles and between pole and ground). The test voltage must be at least equal to the highest stressed unit in the complete CB arrangement.

2.2.2.3 Synthetic tests. This test is needed and performed on a single-phase basis since it is very difficult to perform the test on a three-phase basis in a small laboratory due to power limitation [1]. These tests are generally performed combining a moderate voltage source which supplies the full primary short circuit current with a second, high voltage, low current, power source which injects a high frequency, high voltage pulse at a precise time near the natural current zero of the primary current. The behavior of the CB in thermal and dielectric regions is evaluated by the high voltage that is superimposed by the injected current/voltage which when properly timed embraces the transition point

where the peak of the extinction voltage just appears and the point where the peak of the recovery voltage is reached, thus covering the thermal and dielectric recovery regions.

2.2.2.3.1 <u>Parallel current injection method</u>. This test simulates the conditions that occur across the contacts of the interrupter during the interruption of fault current. The CB is tested for the simulated high fault current and for the successively appearing transient recovery voltage conditions Figure 2.2 shows circuit for parallel current injection test.

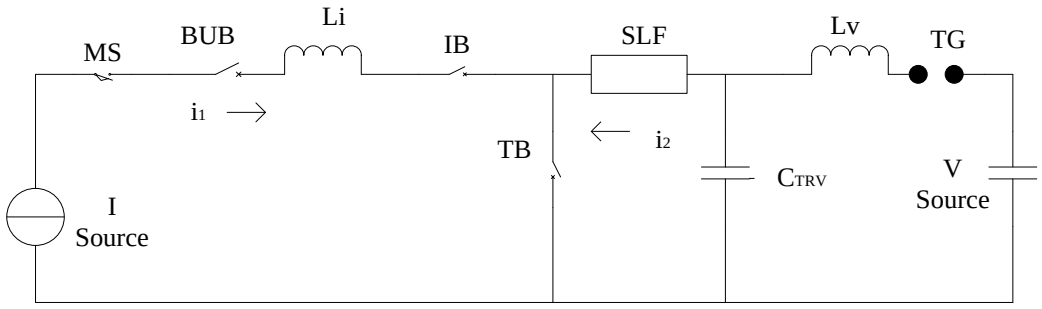


Figure 2.2. Parallel Current Injection Test Circuit.

MS- making switch

BUB- back up circuit breaker

Li- limiting reactor

IB- isolation CB

TB-test CB

SLF-short line fault

TG-triggered spark gap

V source-capacitor bank

The test is initiated by closing the MS which lets the current i_1 flow from IS through IB and TB. As current approaches zero crossing, the spark gap is triggered, and at time t_1, the injected current i_2 begins to flow. The current $i_1 + i_2$ flows through TB until t_2 is reached. At this time, main current i_1 goes to zero and IB separates the two power sources. At t_3, injected current is interrupted and high voltage, supplied by the high voltage source, provides the desired TRV which now appears across the TB terminals. The current waveforms are shown in Figures 2.3 and 2.4.

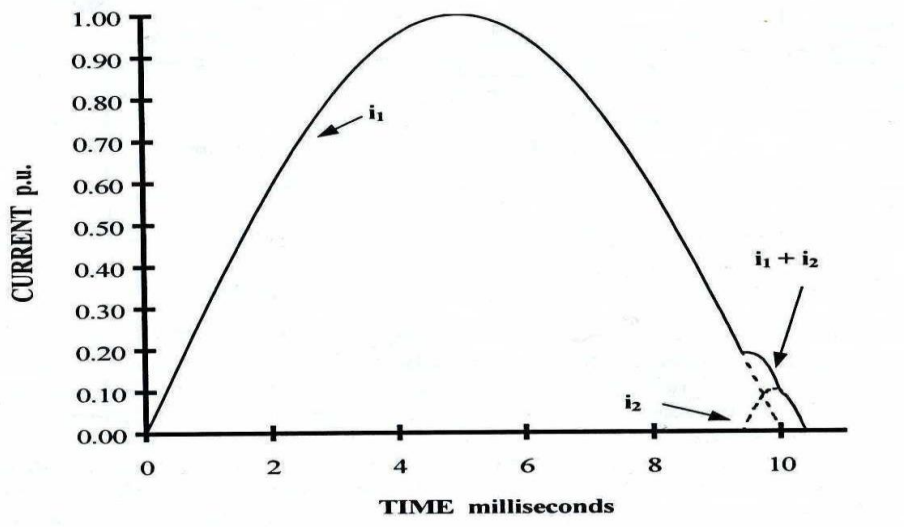


Figure 2.3. Current in TB for Parallel Injection Method.

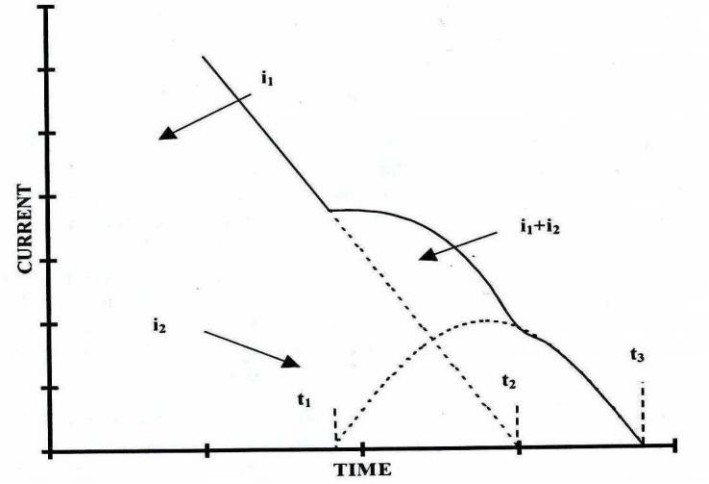


Figure 2.4. Zoomed Version of Current in TB for Parallel Injection Method.

2.2.2.3.2 <u>Series injection method</u>. For this test, the high voltage source is connected in series with the high current source voltage. This test is performed for the same reason for which the parallel current injection test in performed Figure 2.5 shows the circuit for the series injection test.

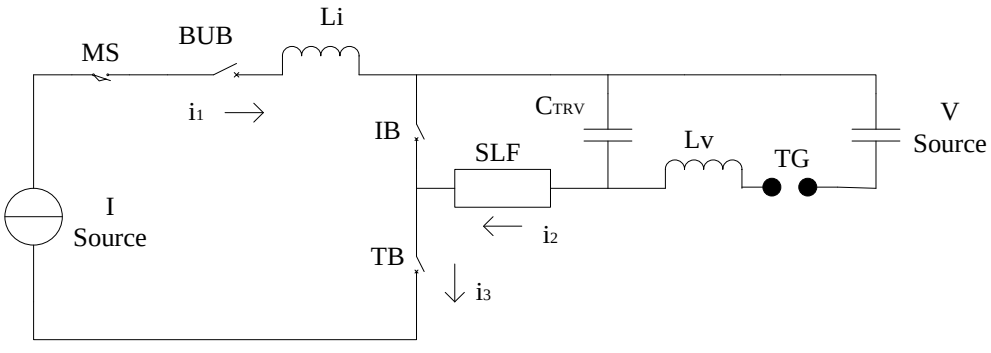


Figure 2.5. Series Injection Method.

MS- making switch

BUB- back up circuit breaker

Li- limiting reactor

IB- isolation CB

TB-test CB

SLF-short line fault

TG-trigger gap

V source-capacitor bank

At initiation of test, MS is closed and at t_1 spark gap is triggered, thus allowing i_2 to flow through IB but in opposite direction to that of i_1 from high current source. At t_2, when i_1 and i_2 are equal, current in IB is interrupted and between instants t_2 and t_3, i_3 flows in the TB. This current i_3 is equal to $i_1 + i_2$, which is produced by series combination of high current and high voltage sources. Following interruption of i_3 at t_3, resulting TRV supplied by high voltage source appears across TB terminals. Figures 2.6 and 2.7 show currents in the test breaker.

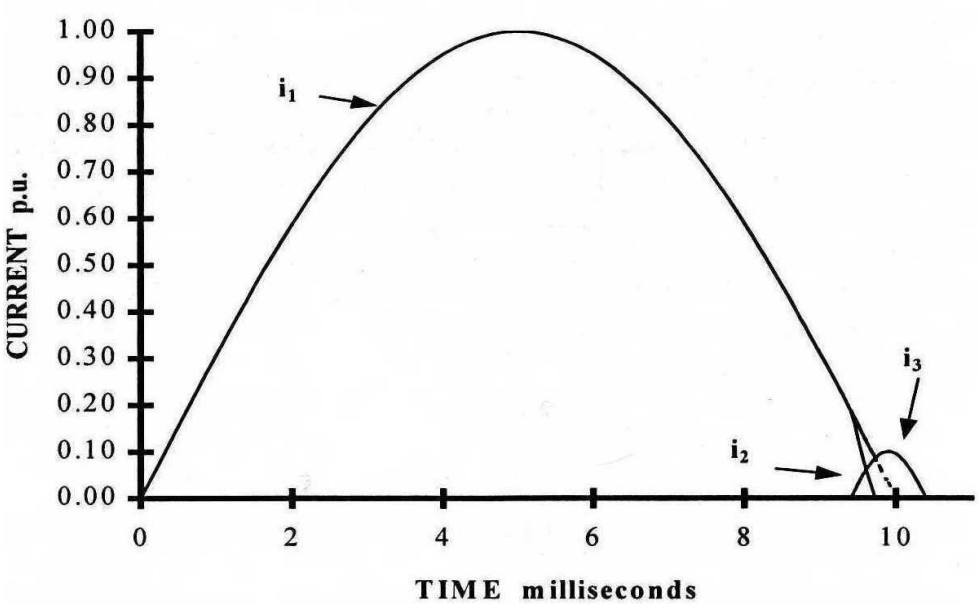


Figure 2.6. Current in TB for Series Injection Method.

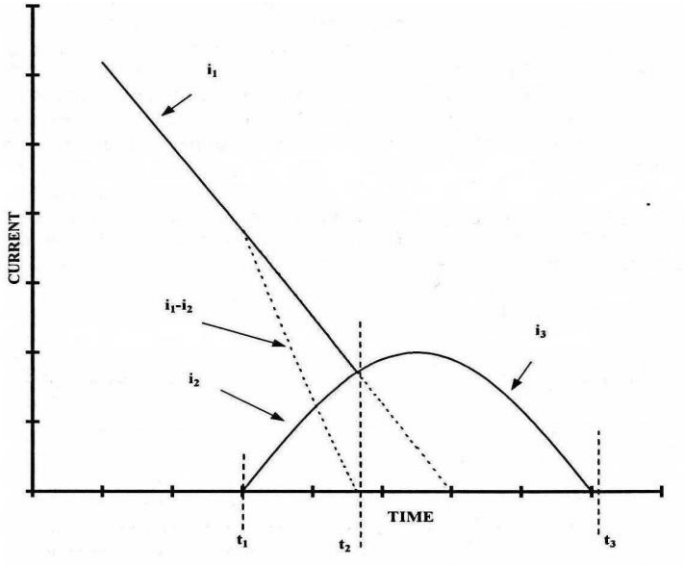


Figure 2.7. Zoomed Version of Current in TB for Series Injection Method.

2.2.2.3.3 **<u>Voltage injection method</u>.** This test is another type of synthetic test used to simulate fault conditions across the CB. This method is similar to Parallel current

injection method with the difference being that the output of the high voltage source is injected across the open contacts of the TB following the interruption of the short circuit current. The short circuit current is supplied by the high current source. The high voltage is injected immediately after the current zero and near the peak of the recovery voltage that is produced by the power frequency current source. A capacitor is connected in parallel across the IB contacts to apply the recovery voltage of the current source to the TB.

2.2.2.3.4 Advantages of synthetic tests. The following are the advantages of synthetic tests.

- These are non-destructive in nature and therefore ideal for development test purposes.
- It is an adequate method of testing and in some cases the only way for performing short line fault tests.

2.2.2.3.5 Disadvantages of synthetic tests. The following are the advantages of synthetic tests.

- It is difficult to do fast re-closing with extended arcing times.
- This method is not suitable for testing CBs which have impedance connected in parallel with the CB contacts in which case it is likely that the full recovery voltage cannot be attained due to power limitations of the high voltage source.

3. SOLID STATE FAULT INTERRUPTION DEVICE

3.1. BACKGROUND

The integration of loads which are sensitive to power quality has led to an increased demand for better power quality. Hence, the need to have devices which eliminate or reduce the impact of disturbances occurring in the system has become imperative. It is known that faults are responsible for causing large disturbances in the system and hence they need to be cleared as soon as possible. Currently, mechanical circuit breakers (CBs), which take several 10 ms [4] to clear the fault, are being used for this purpose. However, this span of several 10 ms may be enough to distort power quality to unacceptable levels. The other disadvantages with mechanical CBs are [1]:

1. The slow switching time has no influence on the peak current. The peak current may rise to 20 times the maximum operating current. This high current stresses the components both electrically and mechanically. Hence, all grid components have to be oversized to withstand this peak value.
2. Limited number of short-circuit clearances.
3. Limited turn-off capability.

Because of the above mentioned drawbacks, solid state CBs would be preferred as a replacement for mechanical CBs as they should be able to clear faults within 100μs to 5 ms. The clearing time is enough to maintain a healthy voltage in the power system. Also the fault current can be prevented from reaching its peak value due to the ultra-fast operation of solid state devices. Today, high-power semiconductors with blocking voltages upto 9kV are available. These semiconductors can even be connected in series to give higher blocking voltages. However, the only drawbacks of these devices are their

high initial costs and their conduction losses when used for constructing a solid state circuit breaker.

3.2. AVAILABLE TOPOLOGIES

The different semiconductors currently available in the market that can be considered for this application are thyristors, IGBTs, GTOs, GCTs etc. However, only IGBT-based topologies have been considered in this thesis. As mentioned earlier in section 3.1, the SSFID may consist of several semiconductor devices connected in series to achieve a blocking voltage that is greater than the maximum grid voltage. If multiple modules of semiconductor devices are used, then the blocking voltage rating of the device should be greater than, the phase voltage divided by the number of the modules used, to achieve successful operation. The current rating should be calculated from the maximum power flowing through the SSFID. Asymmetric IGBTs have used been used for these applications. Hence, additional diodes have been connected in parallel with each IGBT.

3.2.1 Topology # 1. A snubber circuit consisting of a resistor and a capacitor may be needed to limit the voltage during turn-off. Topology # 1 is shown in Figure 3.1 [5].

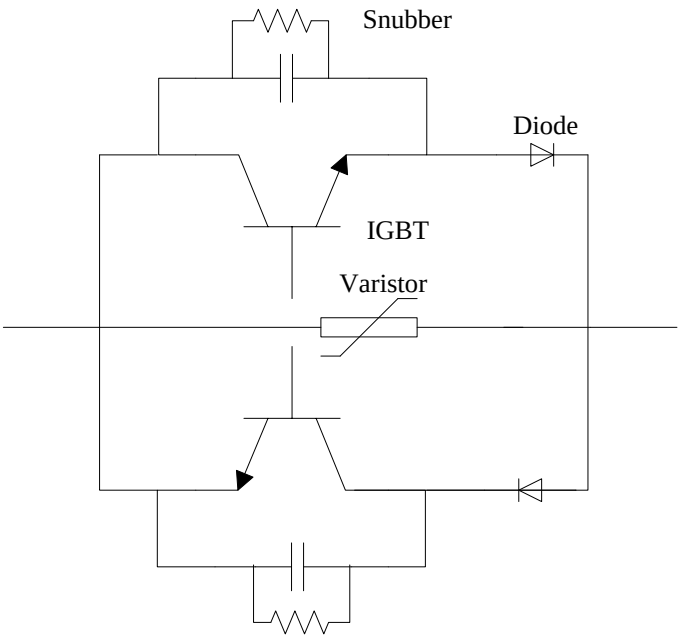


Figure 3.1. SSFID Topology with IGBT and a Snubber Circuit.

The disadvantage of topology # 1 is that it has a high initial cost due to the large number of components.

3.2.2 Topology # 2. The snubber circuit may be replaced by a varistor to limit the over-voltage during turn-off [5]. Topology # 2 is shown in Figure 3.2. The disadvantage of topology # 2.is that it has a high initial cost due to the large number of components and non-modular construction.

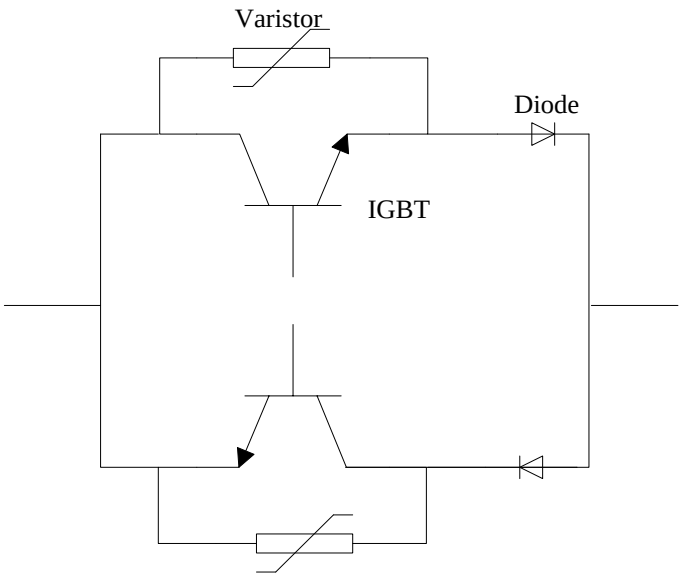


Figure 3.2. SSFID Topology with IGBT and a Varistor.

For both topologies, each half cycle of the grid current flows through either the upper or the lower branch of the circuit.

3.2.3 Topology # 3. To reduce the number of IGBTs used, another topology that uses a full diode bridge rectifier as shown in Figure 3.3 was considered [5]. This topology uses a single IGBT and a snubber / varistor across it.

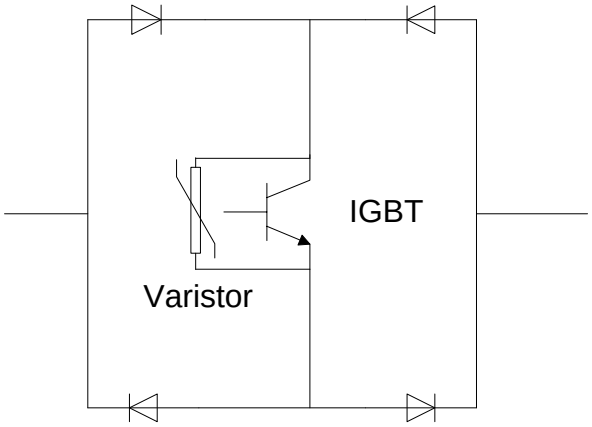


Figure 3.3. SSFID Topology with Full Diode Rectifier with IGBT.

3.2.3.1 Advantage of topology # 3. One IGBT has been replaced by two diodes. Thus, the initial cost of the module is highly reduced.

3.2.3.2 Disadvantage of topology # 3. The IGBT conducts over two half-cycles and there is one more diode in the circuit which also produces additional losses. Hence, the operational cost of this topology is higher.

3.2.4 Topology # 4. It consists of IGBTs and thyristors [6]. It also consists of a small transformer with a small inductance and pre-charged capacitance integrated into the circuit. Topology # 4 is shown in Figure 3.4.

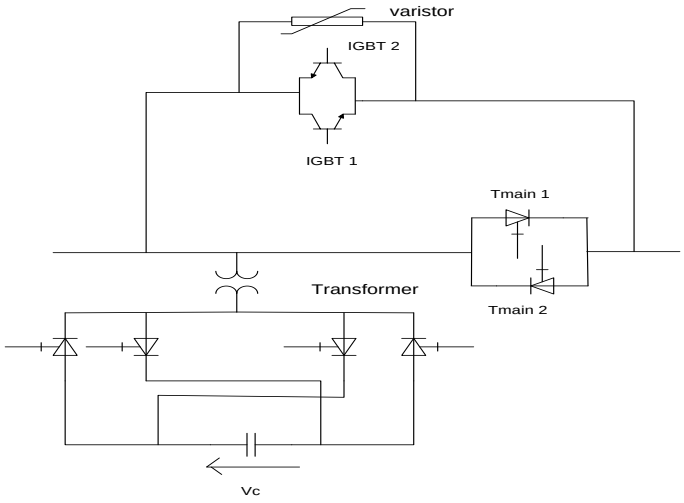


Figure 3.4. IGBT and Thyristor-based Topology.

During normal operation, the current flows through the main thyristors. When a fault is detected, the auxiliary circuit (IGBTs and thyristors) are turned on. The energy stored in the pre-charged capacitor is used to demagnetize the inductance and the current will commutate to the IGBT circuit [6]. After the hold-off interval of the main thyristors is over, the IGBTs interrupt the short circuit current. With such a topology, the interruption lasts less than 0.5 ms [6]. Hence, even with this circuit, the peak current is limited.

The disadvantage of topology # 4 is that this topology with thyristors and IGBTs has a higher initial cost when compared to the first three topologies since it has a transformer as well as 6 thyristors and a capacitor.

Tests carried out by Meyer and DeDoncker [6] on the topologies show that the performance of all four topologies is nearly the same. During the short-circuit test, the

fault current never exceeded twice the maximum operating current. Also, the voltage in the grid is disturbed for only about 100 μs.

3.3. COMPARISON OF DIFFERENT TOPOLOGIES

3.3.1 Technical Comparison. For each of the topologies, the time required for interrupting the fault current by the IGBTs is 100-500 μs. Thus, the power quality attained, by using any of the above topologies is almost the same. Due to the above reason, it is necessary to analyze the topologies on an economical scale.

3.3.2 Economical Comparison. The primary component responsible for a high initial cost of the SSFID is the semiconductor itself and hence losses are used for comparing operating costs. Although the rectifier topology (Topology # 3) with only one IGBT is comparatively cheaper to implement, the presence of one more diode in the circuit adds to the conduction loss. The losses associated with a semiconductor device can be estimated by the following equation [5]

$$P_V = I_{rms}^2 \times r_t + I \times V_T \tag{3.1}$$

r_t –slope / on-state conduction resistance

V_T -threshold voltage/on-state voltage drop

I -average value of 60 Hz sinusoidal current

I_{rms} -rms value of 60 Hz sinusoidal current

Thus, each of the above topologies has its own pros and cons when compared on the basis of cost. It is, therefore, necessary to evaluate the topologies on the basis of break-even point. The time to reach the break-even point depends on the amount of

power transmitted through the SSFID. At the break-even point, the difference of investment costs must be equal to the costs associated with additional losses [2].

Thus, if m = cost per kWh

ΔC = difference in investment costs

T = hours per year = 8760

a = the number of years

ΔP = difference in losses

$$\Delta C = a x T x m x \Delta P \quad (3.2)$$

Hence, the most cost-effective solution for selecting a topology for a SSFID depends on the average transmitted power through it and the time for which it will be in operation in the grid.

3.4. SOLID STATE FAULT INTERRUPTION DEVICE

The proposed SSFID will have 3 modules of IGBT-diode pairs [8]. Each module will consist of two pairs, IGBT-diode in anti-parallel, connected in the common emitter configuration. Each module is protected by a metal oxide varistor and a resistor in parallel with the module. Just like the conventional CBs, the SSFID should be placed in series with disconnect switch connected in series that can be opened after the SSFID is switched off. The disconnect switch helps to completely open a circuit that was previously still ‘live’ through the resistor in the SSFID. The SSFID design is shown in Figure 3.5.

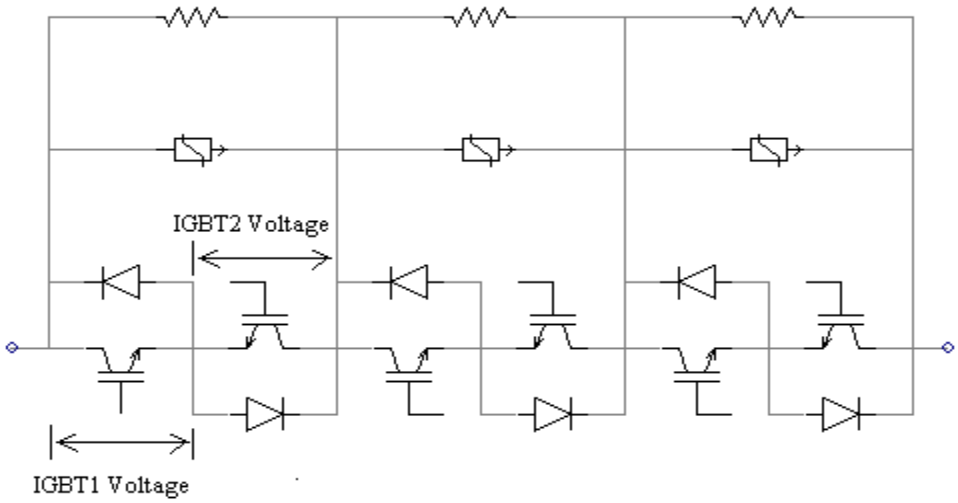


Figure 3.5. SSFID Model.

For the SSFID, an IGBT module 5SNA 0400J650100 from [9] with forward breakdown voltage of 6.5 kV and continuous rated current of 400 A has been selected. Its parameters for the rated operating point in the three-phase 1MVA, 12.5 kV, 46.2A FREEDM distribution system [10] are given in Table 3.1. No snubber circuits will be provided for the IGBTs since they have high leakage currents and higher losses.

Table 3.1. IGBT Parameters

IGBT ON resistance	0.02 Ω
IGBT OFF resistance	1e6 Ω
Forward Voltage Drop	0.0024kV
Forward Break-over Voltage	6.5 kV
Reverse Withstand Voltage	6.5kV

The diode to be used for the SSFID is built into the IGBT module and connected in anti-parallel with each of the IGBTs in the module. Diode parameters for the rated operating conditions are given in Table 3.2. No snubber circuit is provided for the diode for reasons mentioned earlier.

Table 3.2. Diode Parameters

Diode ON resistance	0.011 Ω
Diode OFF resistance	1e6 Ω
Forward Voltage Drop	0.0017 kV
Forward Break-over Voltage	6.5 kV
Reverse Withstand Voltage	6.5 kV

A specific type of MOV V242BB60 having disc size of 60mm [11] is selected for protecting the IGBT-diode pair in case of over-voltages. One MOV of voltage rating equal to 2.4 kV is connected across each module in the SSFID. The I-V characteristic for the MOV has been derived from the [11] and entered as a user-defined characteristic for the MOV in PSCAD. The characteristic for the MOV is shown in Figure 3.6. To calculate the voltage across the MOV in per unit for different leakage currents, the arrester voltage rating has been considered as the base voltage.

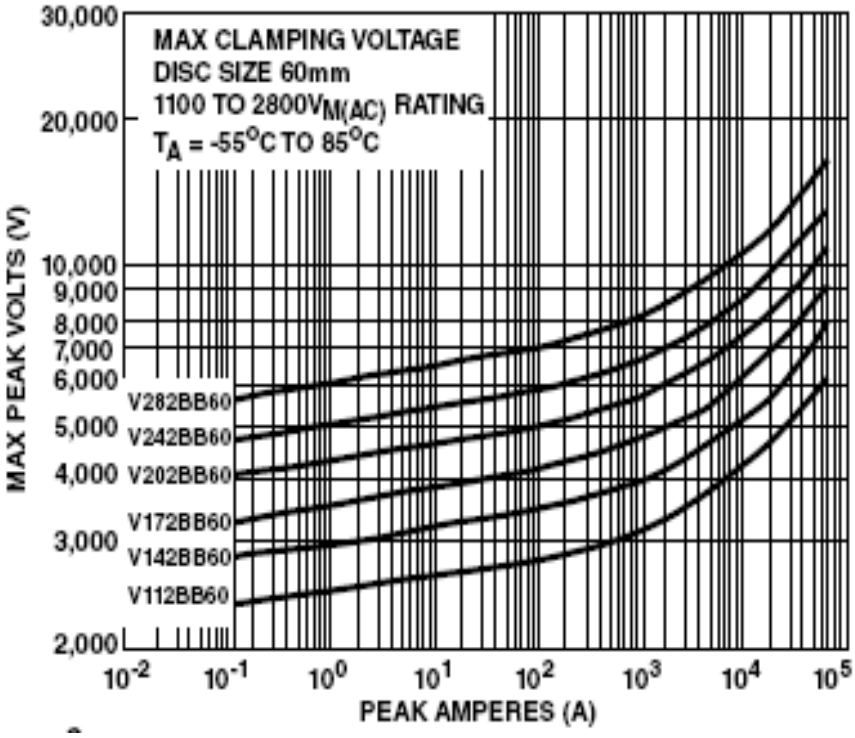


Figure 3.6. MOV Voltage Clamping Curve.

Along-with the MOV, a resistor of 250 kΩ is inserted in parallel with each module for limiting over-voltages.

3.5. PRINCIPLE OF OPERATION

The SSFID is supposed to conduct current when normal conditions exist in the network and interrupt the current during abnormal conditions in the network that cause an unacceptable increase in current, e.g., during faults. For smooth bidirectional flow of current, gate voltages of 20 V are continuously provided for IGBTs. This prevents undesired voltages spikes from developing across the SSFID due to commutation or changes in power factor. If there are spikes, the MOV provides a low resistance path when spikes exceed the threshold rating of the MOV and hence limits the voltage across each module.

3.5.1. Advantages of the SSFID Model.

- With only one MOV per module and the modular structure of the IGBT used, fewer number of components are required to make up the SSFID module. Hence, the cost of the SSFID reduces. The addition of a resistor does not increase the cost significantly as resistors are rather inexpensive.
- The IGBT module is readily available in the market, thus making replacement easier.

3.5.2. Disadvantage of SSFID Model.

- The addition of the resistor adds to the losses.

3.6. TESTING OF THE PROPOSED SSFID MODEL

To test the validity of the SSFID for use on the FREEDM distribution system, the SSFID model should be first subjected to a variety of tests. The model should be tested for (i) continuous current-carrying capability, (ii) operation at frequencies different from the nominal frequency, (iii) short-circuit current interrupting capability and (iv) lightning impulse voltage withstand capability.

3.6.1. Continuous Current-Carrying Test. This test should be done to verify whether the SSFID can carry the continuous rated current at rated frequency without exceeding its temperature limitations as given in [3]. The conditions in which this test should be carried out are also given in [3]. The test can be carried out on a single pole of the SSFID.

The continuous current test should be performed and three readings of different points in the assembly should be taken at 30 min intervals. The temperature of the points in the assembly should not change by more than 1°C for the three readings. The SSFID is said to have passed the test if the temperature readings do not exceed the limits specified in [2]. For the measurement of temperature, thermocouples or resistances may be used. The measuring device is located at a point from where the hottest accessible spot can be made. Measurements should be made at junction points of insulation and conducting parts to prevent exceeding limits of the insulation [12]. The resistance of the main circuit should be measured for comparison between the circuit breaker originally design tested and all other circuit breakers of the same type subjected to routine tests. A DC source is used to measure the voltage drop or resistance across the terminals of each pole. The ambient temperature can be determined as given in [12].

For simulating the test, a 0.333 MVA, 7.2kV generator, the SSFID model and a load resistor are connected in series. An auxiliary circuit breaker is used for back-up protection. An inductor is used for current limiting purposes. The value of the load resistor is given by Equation (3.3). The test circuit is shown in Figure 3.7.

$$R = \frac{7.2kV}{0.046kA} = 156\Omega \tag{3.3}$$

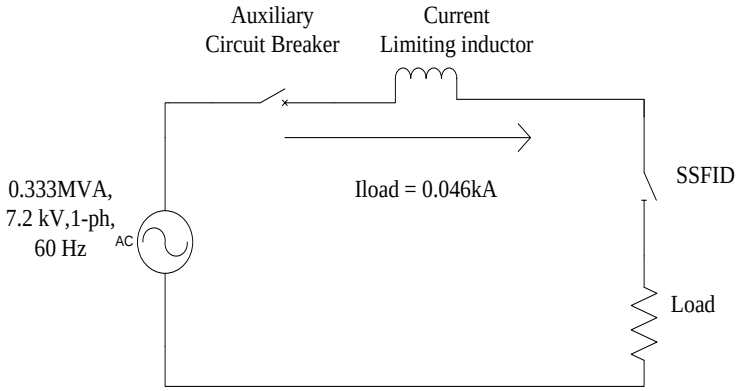


Figure 3.7. Continuous Current Carrying Test on a Single-phase Test Circuit.

The currents in the IGBTs were found to be as expected, i.e., 0.065 kA (0-peak). Currents for the two IGBTs are shown with continuous and dashed lines in Figure 3.8. Identical currents were observed for diodes.

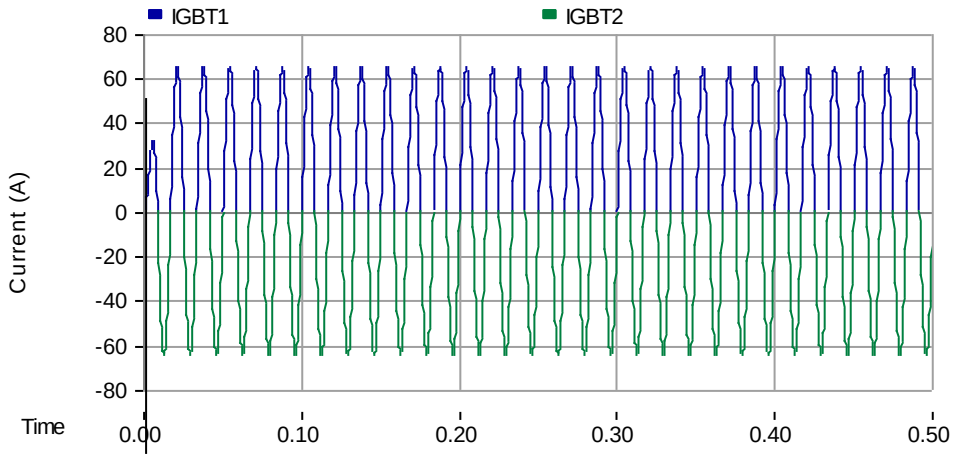


Figure 3.8. IGBT Currents in the SSFID for Continuous Current Carrying Test.

3.6.2 Power Frequency Test. This test should be performed to determine the ability of the SSFID to withstand its rated power frequency withstand voltage. The test should be simulated with a sinusoidal voltage having a peak value of 41.57 kV which is equivalent to 1.414 times the rated rms power frequency withstand voltage of 29.4 kV for the rated maximum design voltage. This voltage is adopted from the recommended test in [3]. The voltage test frequency shall be equal to the rated power frequency ±20%. According to [12], there should be no flashovers during the 1 minute test and no damage to the insulation should be observed after the tests. Figure 3.9 shows the circuit for this test.

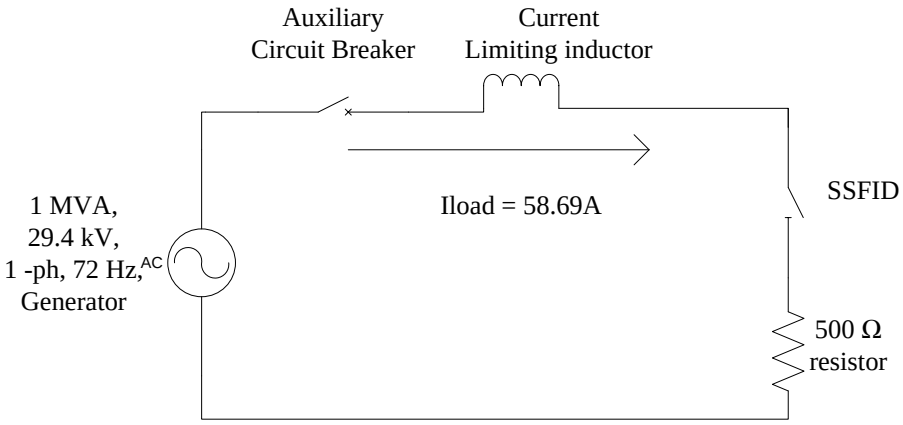


Figure 3.9. Power Frequency Voltage Withstand Test.

The line current flowing through the system and hence the model was as required, i.e.,

$$I_{line} = \frac{41.57kV(peak)}{0.5k\Omega} = 83.14A(peak) = 58.78A(rms) \quad (3.4)$$

The currents in the two IGBTs in the model are shown by continuous and dashed lines in Figure 3.10. Like the continuous current-carrying test, currents through the diode are identical to the currents in the IGBTs

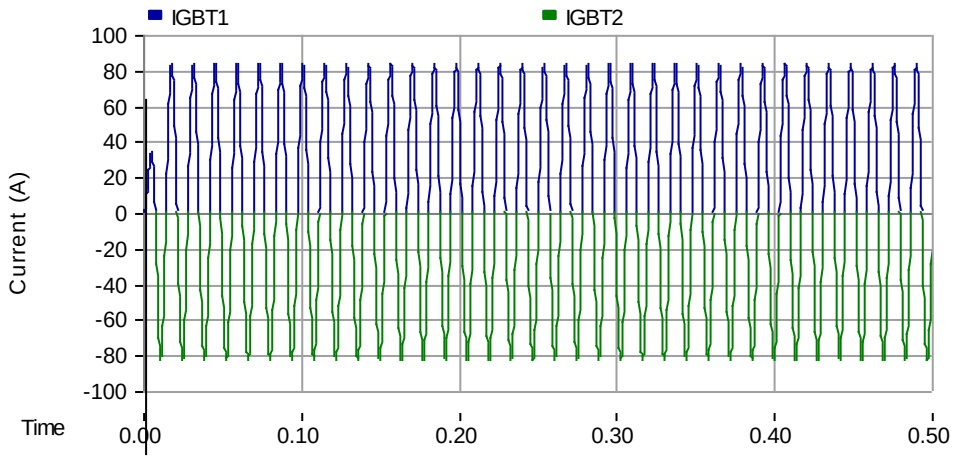


Figure 3.10. IGBT Current in SSFID Model for Power Frequency Voltage Withstand Test.

3.6.3 Short Circuit Current Interrupting Test. This test is one of the synthetic tests that should be used to verify the short circuit current interrupting rating of the SSFID. The rated short circuit interrupting rating of the SSFID will be the maximum symmetrical short circuit current in amperes at primary opening time that the SSFID will be required to interrupt at the rated maximum operating voltage and the standard operating duty cycle [3]. The fault current for the contemporary distribution systems is between 5 to 20 pu of the rated operating current. It is assumed that the system having the SSFIDs will have a peak fault current less than the peak collector current rating of the IGBTs. Hence, the total fault current (symmetrical and asymmetrical components) was assumed to be 10 times the operating current for the first peak of the simulation test i.e.

$$I_{short-circuit} = 10 \times 46.2 = 462A(rms) = 653.3A(peak) \quad (3.5)$$

For this purpose, a current source capable of supplying this current will be needed. The SSFID will be required to withstand the transient recovery voltage (TRV)

that follows current interruption. The magnitude of this TRV for the interrupting short circuit current for a conventional CB is given by

$$E = K_a \times K_f \times 0.816 \times V = 13.57kV \tag{3.6}$$

where

K_a – transient amplitude factor =1.54 [13]

K_f – first-pole –to-clear factor = 1.5 [13]

V –rated maximum voltage = 7.2 kV

However, for test purposes a 4kV source has been used to provide the voltage that occurs after the fault current is interrupted. This can only be synthesized by using synthetic testing methods. Figure 3.11 shows the circuit for the short circuit current-interrupting test using the parallel current injection method [13].

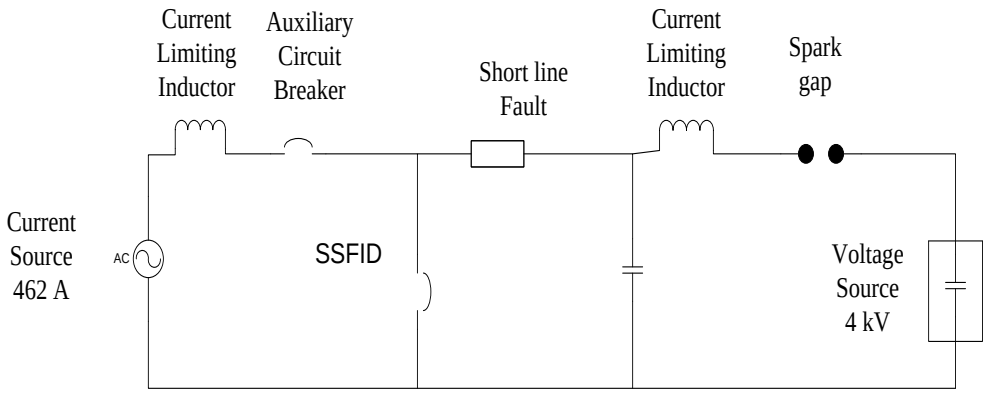


Figure 3.11. Short-Circuit Interrupting Test on a Single-phase Test Circuit.

The auxiliary circuit breaker is required to have its short circuit interrupting rating greater than that of the SSFID. An inductor of 0.001 H is provided for current limiting purposes in the simulation. An impedance consisting of, a resistor of 10 ohm in series with an inductor of 0.026525 H, is connected to simulate a transmission line. The capacitor and the inductor on the right hand part of the circuit are used for voltage support and current limiting purposes respectively. A circuit breaker 'SP' is used to simulate the spark gap shown in the circuit for the test. A dc voltage source having parameters given in Table 3.3 are used for the test. The conditions and the sequence in which the simulation test was carried out are given below.

Table 3.3. Voltage Source Parameters for Short-Circuit Current Interrupting Test.

Initial source magnitude	4 kV
Source power	1.6 MW

Initial Conditions:

(a) The auxiliary circuit breaker is closed. Hence a current of 462 A from the current source directly flows through the SSFID.

(b) Circuit breaker 'SP' is open indicating that the spark gap is open and no current flows through it.

(c) The SSFID model is conducting current flowing from the current source.

Sequence

(a)The circuit breaker ‘SP’ closes at t = 0.2 sec. Thus the DC source injects a dc current through the SSFID model. ‘SP’ remains closed till the end of the simulation.

(b)The auxiliary circuit breaker opens at t = 0.21sec. Hence the current from current source flows through the auxiliary circuit breaker only from t = 0 sec to t = 0.21sec.

(c)The gate signals for the IGBTs are made zero at t = 0.22sec. Hence, the SSFID model stops conducting at t = 0.22sec.

Hence, with this sequence it is guaranteed that the SSFID model is exposed to conditions occurring at the time of circuit interruption. The large current flowing from the current source replicates a fault current while the dc source helps to produce a transient recovery voltage across the model.

Ammeter ‘SSFIDcurrent’ was connected in series with the model. The current flowing through the model during the simulation is shown in Figure 3.12. It was observed that the current before t = 0.2s equals the peak current given by the current source. Also, the current peak starting at t = 0.2s is taller than the previous peaks owing to the injection of current by the voltage source. The increase in current through the SSFID is of

$$I_{increment} = \frac{4kV}{10\Omega} = 400A \tag{3.7}$$

Also, it can be observed in Figure 3.12 that after t = 0.21sec, only the dc current of 400 A flows through the model since the auxiliary circuit breaker opens and stops the flow of current from the current source to the model. The current becomes zero at t = 0.22s when the SSFID model opens.

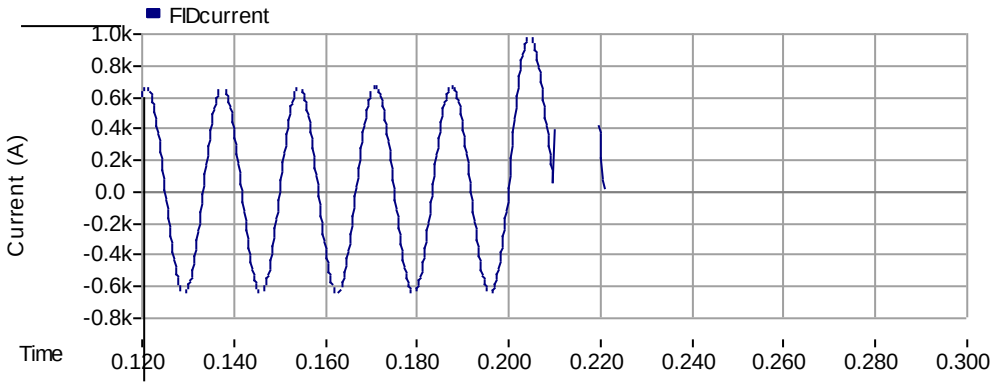


Figure 3.12. Current Through the SSFID for Short-Circuit Current Interrupting Test.

When the model turns off at t = 0.22 sec, it is observed in Figure 3.13 that a peak transient voltage of 6.2 kV appears across the IGBT. Hence, break-over of the IGBT is prevented. After turnoff, the voltage across the IGBT settles down at just less than 1.35 kV. The leakage current through the MOV at t = 0.22sec is 349A (peak) and it settles down to about 0.3A. This is shown in Figure 3.14. The total energy dissipated in the varistor is given by its clamping voltage, peak leakage current and the time-to half for the current [14].

$$E = 1.4 \times V_C \times I_P \times t \tag{3.8}$$

$$= 1.4 \times 6200 \times 349 \times 0.00275 = 8330.63J$$

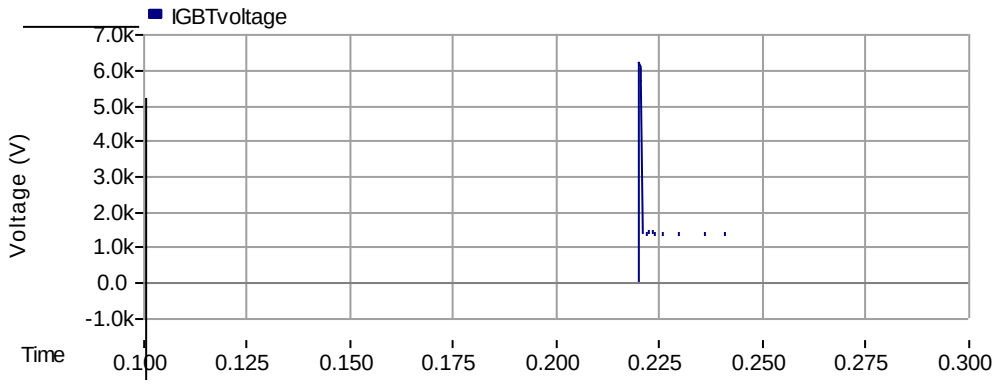


Figure 3.13. Voltage Across IGBT for Short-Circuit Current Interrupting Test.

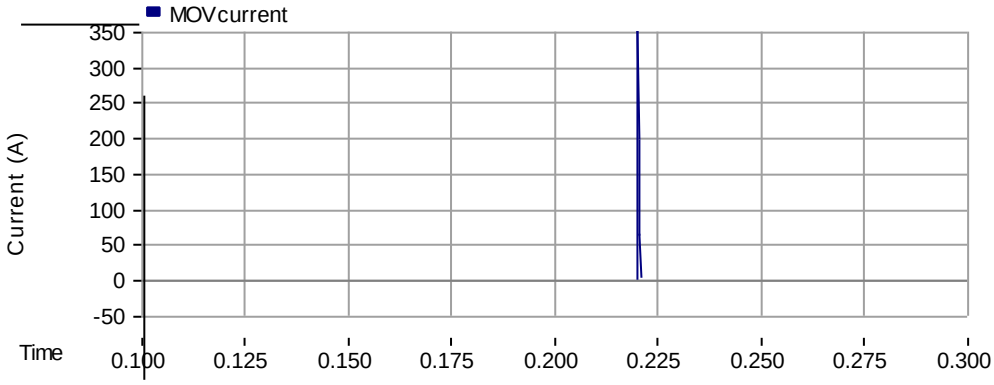


Figure 3.14. MOV Current for Short-Circuit Current Interrupting Test.

3.6.4 Lightning Impulse Voltage Withstand Test. This test will be performed under dry conditions given in [3] to verify the SSFID's ability to withstand its rated full-wave lightning impulse withstand voltage of 95 kV. A standard lightning impulse with a peak voltage of 95 kV with a front time of 1.2 μs and a time to half value of 50 μs is used in the simulation. Figure 3.14 shows the circuit for the lightning impulse test. The

lightning impulse is produced by a dc source controlled by a surge generator model available in PSCAD.

Test Sequence

(a) The impulse rises to 95kV from t = 0 sec to t = 1.2 μsec and decays to zero value at t = 101 μsec.

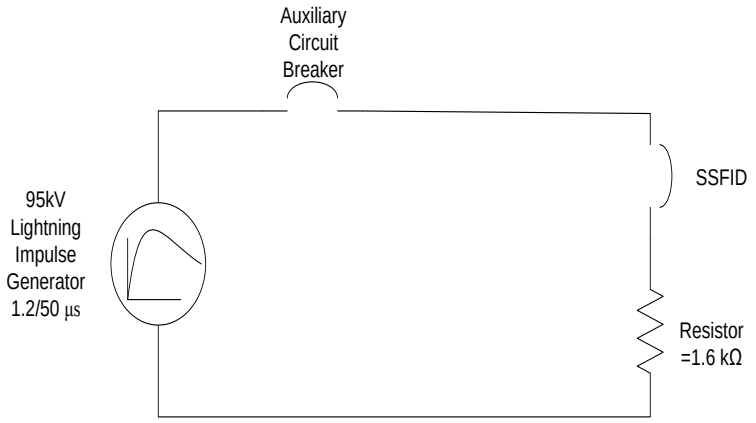


Figure 3.15. Lightning Impulse Voltage Withstand Test Circuit.

The voltages across the IGBTs rise to 300V and 600V respectively. The voltages across the diodes were identical to that across the IGBTs. The MOV operates to limit the voltages across the IGBTs/diodes and keeps them within safe values. The voltages appearing across the IGBTs are shown in Figure 3.16.

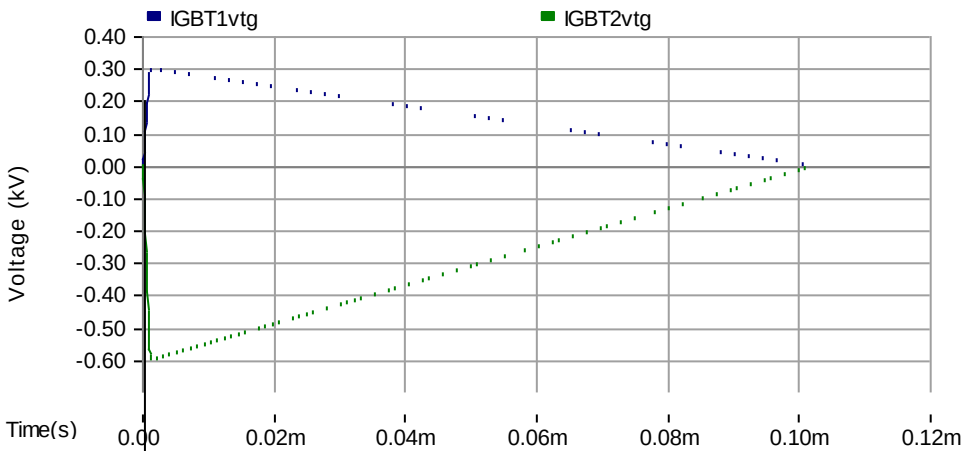


Figure 3.16. IGBT Voltages for Lightning Impulse Withstand Test.

3.7. EFFICIENCY OF THE SSFID

The efficiency of the SSFID is one of the parameters that will decide whether the use of solid state interruption devices is indeed a viable option to replace the conventional circuit breakers. The efficiency will decide the payback time of the breaker and hence it is necessary that it be low or comparable to the contemporary breakers. Since the FREEDM system may have varying loads, the efficiency for the SSFID has been calculated at 100%, 60% and 30% of the maximum loading. All calculations have been made at 125^0C which is assumed to be the maximum operating temperature for the IGBT module.

For 100 % loading

$I_{rms} = I_C = 46.2A$ (Rated rms line current of the system)

$V_{CEO} = 2.4V$ (On–state collector –emitter voltage drop of IGBT at I_{rms} = 46.2 A)

$r_{CE} = 0.02\Omega$ (Internal collector-emitter resistance of IGBT)

$V_F = 1.65V$ (On-state forward voltage of diode)

$T_0 = 16.667ms$

$P_{conductionloss}$ for 1 IGBT+1Diode=

$$\frac{1}{T_0}\int_0^{T_0/2}\left[V_{CEO}\times I\times\sin\omega t + r_{CE}\times I^2\times\sin^2\omega t + V_F\times I\times\sin\omega t\right]dt$$

(I is the peak amplitude of $I_{rms} = I_C = 46.2A$)

$$= \frac{V_{CEO}\times I}{\pi} + \frac{r_{CE}\times I^2}{4} + \frac{V_F\times I}{\pi}$$

$$= 49.9 + 21.34 + 34.31$$

$$= 105.55W$$

Total conduction losses = 105.55×2(2 pairs in each module) $\times 3$(3 modules)

= 633.33 W.

The switching losses will be negligible since each IGBT/diode is shorted out by the other component in the next half cycle.

Power per phase (MW) = $\frac{1MW}{3} = 333333W$

Efficiency for SSFID = $\frac{333333}{333333 + 633.33}$

= 99.81%

For 60 % loading

$I_{rms} = I_C = 27.7A$ (Rated rms line current of the system)

$V_{CEO} = 1.85V$ (On –state collector –emitter voltage drop of IGBT at I_{rms} = 27.7 A)

$r_{CE} = 0.04\Omega$ (Internal collector-emitter resistance of IGBT)

$V_F = 1.3V$ (On-state forward voltage of diode)

$T_0 = 16.667ms$

$P_{conductionloss}$ for 1 IGBT+1Diode =

$$\frac{1}{T_0}\int_0^{T_0/2}\left[V_{CEO}\times I\times\sin\omega t + r_{CE}\times I^2\times\sin^2\omega t + V_F\times I\times\sin\omega t\right]dt$$

(I is the peak amplitude of $I_{rms} = I_C = 27.7A$)

$$= \frac{V_{CEO}\times I}{\pi} + \frac{r_{CE}\times I^2}{4} + \frac{V_F\times I}{\pi}$$

= 23.08 + 15.36 + 16.22

= 54.66 W

Total conduction losses = 54.66×2(2 pairs in each module) $\times 3$(3 modules)

= 327.96 W.

Power per phase (MW) = $\frac{1MW}{3}\times 0.6 = 200000W$

Efficiency for SSFID per each phase = $\frac{200000}{200000+327.96}$

= 99.83%

For 30 % loading

$I_{rms} = I_C = 13.86A$ (Rated rms line current of the system)

$V_{CEO} = 1.25V$ (On–state collector –emitter voltage drop of IGBT at I_{rms} = 13.86 A)

$r_{CE} = 0.07\Omega$ (Internal collector-emitter resistance of IGBT)

$V_F = 1.1V$ (On-state forward voltage of diode)

$T_0 = 16.667ms$

$P_{conductionloss}$ for 1 IGBT+1Diode =

$$\frac{1}{T_0}\int_0^{T_0/2}\left[V_{CEO}\times I\times\sin\omega t + r_{CE}\times I^2\times\sin^2\omega t + V_F\times I\times\sin\omega t\right]dt$$

(I is the peak amplitude of+ $I_{rms} = I_C = 27.7A$)

$$= \frac{V_{CEO}\times I}{\pi} + \frac{r_{CE}\times I^2}{4} + \frac{V_F\times I}{\pi}$$

= 7.762 + 6.66 + 6.83

= 21.252 W

Total conduction losses = 21.252×2(2 pairs in each module) $\times 3$(3 modules)

= 127.512 W.

Power per phase (MW) = $\frac{1MW}{3}\times 0.3 = 100000W$

Efficiency for SSFID per each phase = $\frac{100000}{100000 + +127.512}$

= 99.87%

Hence, it is seen that the efficiency for the FID essentially remains the constant for different loading conditions.

3.8. SPEED OF OPERATION

The primary parameter on which the performance of a SSFID and a conventional circuit breaker can be compared is the interrupting time, i.e., the time taken to interrupt the fault current after the relay time has taken place. The interrupting time for the SSFID

will be a few 100 μs to 5 ms while that for the conventional breaker is in the order of few 10 ms [4]. To verify this, a single-phase 7.2 kV distribution system with four buses was created in PSCAD. The buses were connected by short lines. Two of the four buses were connected to distributed generators (DG) through single-phase 7.2kV/0.48kV transformers. Each line was protected by circuit breakers/SSFIDs indicated as switches at each of its end. A differential scheme was used for protection purposes. A schematic of the distribution system is shown in Figure 3.17.

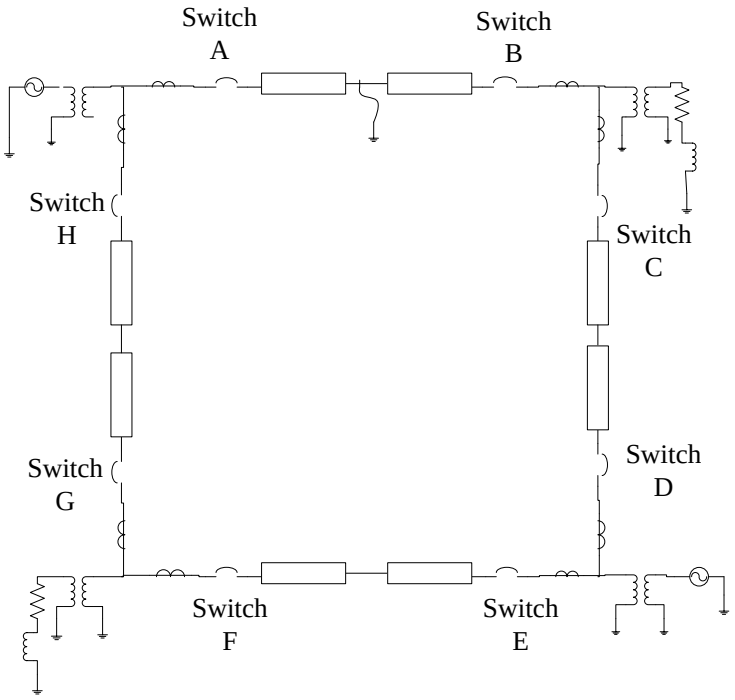


Figure 3.17. Single -phase 7.2kV Distribution System.

To observe the response of the circuit breaker/SSFID, a fault was simulated at the midpoint of the line protected by switches A and B. As a result, current of different magnitudes contribute to the fault current from both sides of the fault location. Peak fault

currents though switches A and B are shown in Figures 3.18 and 3.19, respectively for a particular relay setting.

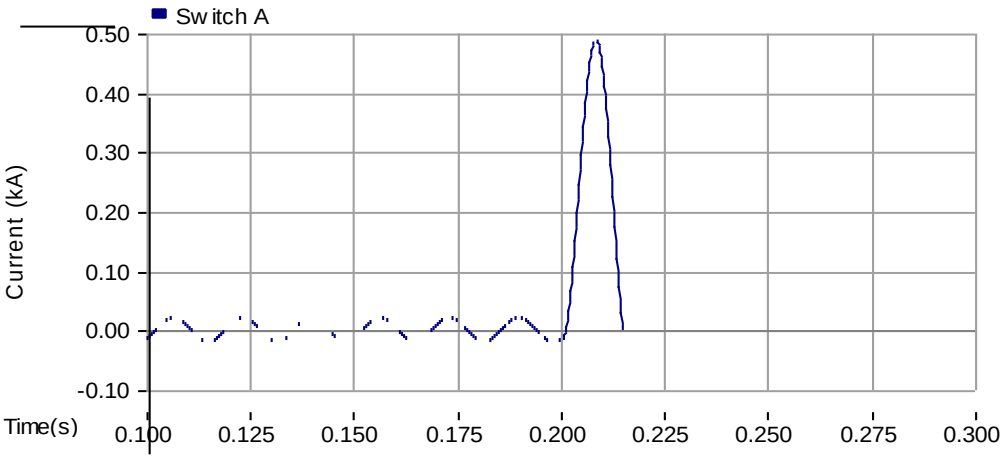


Figure 3.18. Fault Current through Switch A.

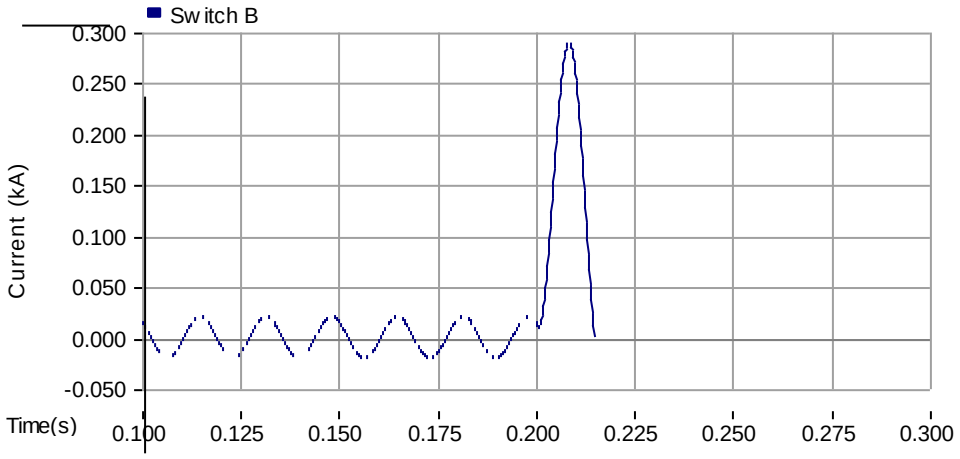


Figure 3.19. Fault Current through Switch B.

When the difference in currents becomes greater than the pickup value of the differential relay, the switches operate and thus isolate the line from the rest of the system. To prevent the fault current from reaching the peak value, the relay settings for the simulation were kept such that the switches opened before the current reached its first peak. The relay trip signal was generated at t = 0.20350s for SSFID models as well as the circuit breakers. For comparison purposes, all system values and relay settings were kept identical for both cases. Current interruption for SSFID models and circuit breakers is shown in Figure 3.20 and Figure 3.23. Figures 3.21and 3.22 show the currents through the IGBT and the MOV that together make up the current through the SSFID during interruption. To give a better idea about interruption time, the trip signal is also plotted.

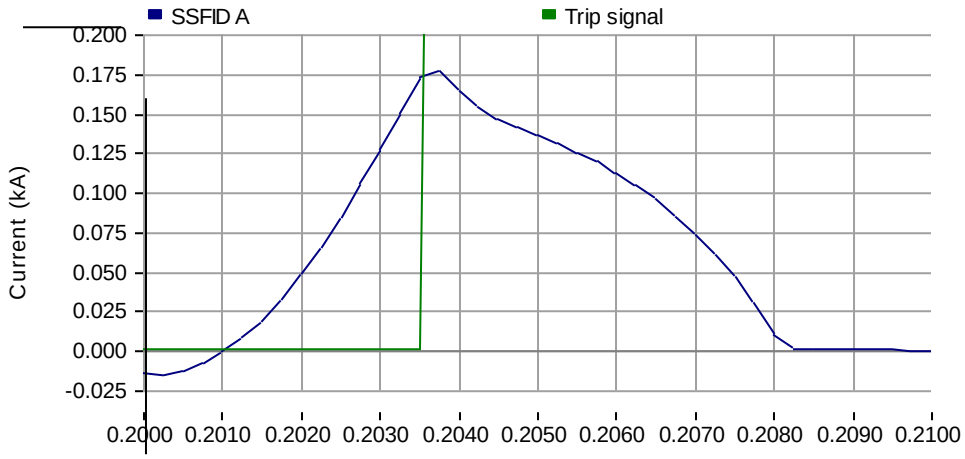


Figure 3.20. Current Interruption in SSFID A.

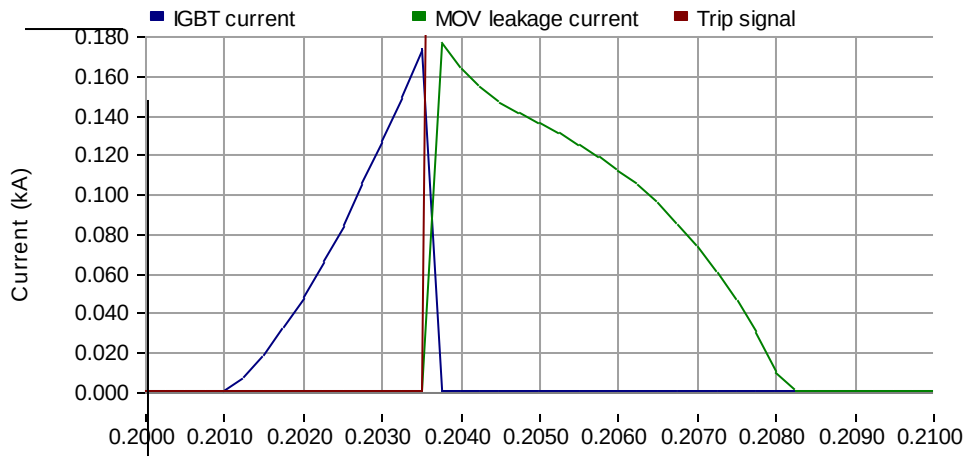


Figure 3.21. IGBT and MOV Current in SSFID A.

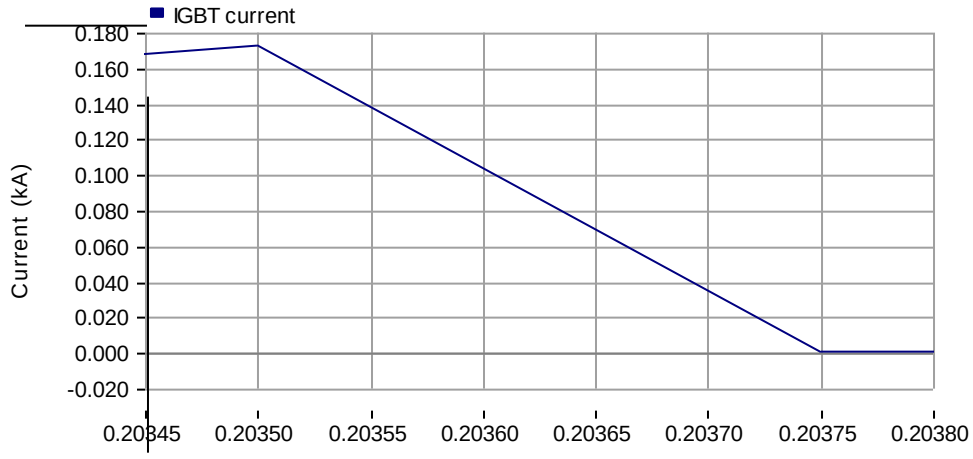


Figure 3.22. Zoomed IGBT Current in SSFID A.

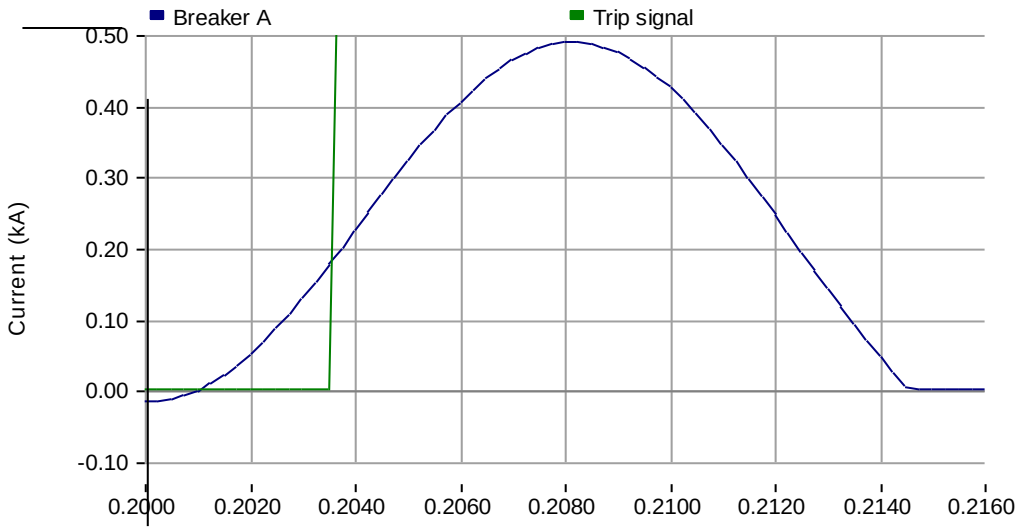


Figure 3.23. Current Interruption in Breaker A.

Thus, from Figures 3.20 and 3.21, it can be observed that after the relay trip signal is generated, current through IGBT is interrupted within 250 µs while the current in the MOV is interrupted within 5ms. From Figure 3.19, it can be observed that the total time taken by the SSFID A to interrupt the fault current is about 5ms. From Figure 3.22, it is observed that the breaker A interrupts the current at the next current zero which requires about 11ms. This indicates a large difference in speed for current interruption by the SSFID as compared to the conventional CB.

To gauge the effect of the interruption time for both cases on system voltages, the voltage at the midpoint of line between switches G and H was measured. It was observed that for the system with SSFIDs, the line voltages recover immediately as soon as the trip signal is given to the SSFID. For the system with a conventional CB, the system experiences a total collapse of the voltage until the time breaker A isolates the fault at the next current zero. The system voltages can be seen in Figures 3.24 and 3.25.

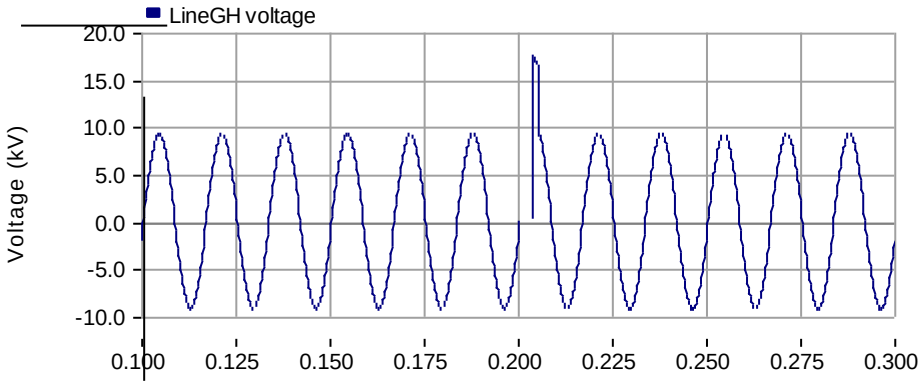


Figure 3.24. Line Voltage for System with SSFIDs.

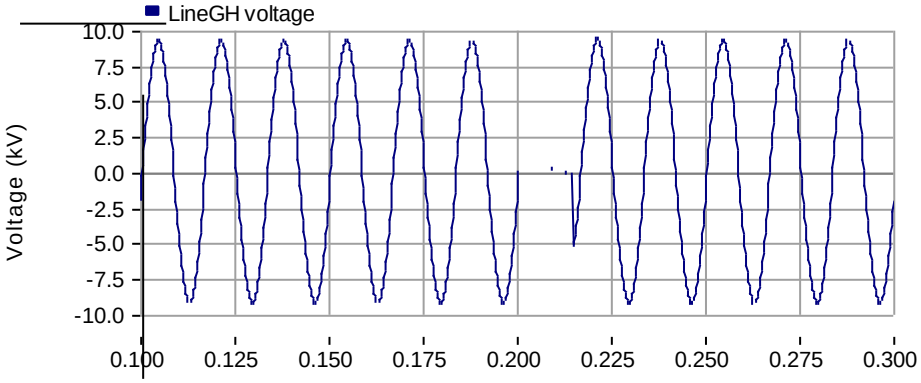


Figure 3.25. Line Voltage for System with CBs.

4. PERFORMANCE COMPARISON AND IMPACT OF SSFIDs ON FAULT STUDIES

4.1. WIND POWER PLANTS AND MICROGRIDS

The increase in generation of electricity from wind power plants (WPP) and their increasing penetration in the legacy grid is imminent. The advantages of being abundant, clean and renewable and the need to reduce emissions from conventional coal power plants makes WPPs an absolute necessity that will complement the contemporary coal and nuclear power plants for sufficing the ever increasing and distributed loads. The different topologies for wind turbine generators that are presently available are given in [15]. For this research, only the Type 1 configuration has been used.

The Type 1 configuration is a constant speed wind turbine, which consists of squirrel cage induction generator (SCIG) directly coupled to the grid [16]. The wind turbine rotor is coupled to the generator through a gearbox. This configuration does not have any power electronic converters or control systems. Hence, the frequency control is achieved through pole changing. The number of poles used is inversely proportional to the speed of the rotor. The power extracted from the wind is limited by using the stall effect. This implies that the efficiency of the wind turbine generator reduces at higher speeds. Since the wind turbine generator is an SCIG, a capacitor bank is needed at its terminals for supplying the excitation for the machine [17].

The experimental FREEDM system will be a microgrid that will be integrated with the legacy grid. A microgrid is a complete electrical system consisting of distributed energy resources (DER) located near loads that may operate independently or in conjunction with the main electrical grid. The FREEDM microgrid system will make use of all available renewable sources of generation namely – micro-turbines, photovoltaic

cells, fuel cells and wind power The FREEDM microgrid may operate in parallel with the main grid to substitute the generation from coal power plants with generation from renewable sources or it may operate as an isolated system to suffice the needs of the loads isolated from the main grid. In parallel operation mode, the legacy grid will control the voltage and the frequency. In an islanded operation of the microgrid, the generators balance the demand to achieve a stable electrical system.

The technical benefits offered by the FREEDM microgrid are that it will help to improve the security, reliability and improve the quality of the electricity available from the legacy grid. During failures in the legacy grid, the FREEDM system will be able to supply electricity from the DERs to the critical loads. Also, during peak demand hours, the FREEDM system will be able to deliver electricity to the legacy grid thus substituting generation by contemporary power plants in the legacy grid.

The economical benefits offered by microgrids are such that the microgrids could be setup where installation or expansion of power plants for meeting future energy growth may not be possible. Further the owner of the DER or the distributed network operator may earn extra revenue by selling electricity to the main electrical grid or to customers within the microgrid during islanded operation. Since microgrids are located close to loads, the cost of losses and congestion are minimal and hence electricity for customers is cheaper than that from the grid.

However, the operations of microgrids such as the FREEDM system face several problems when operating in the islanded mode. In islanded operation, one or more DERs form the grid and prevent the voltage and frequency from collapsing. Non-critical loads may have to be shed to keep frequency within limits. The microgrid has to increase or

decrease their active or reactive power generation according to conditions present prior to going into the islanded mode and according to the needs of the loads present within the microgrid when operating in the islanded mode. Also, a microgrid will most likely maintain the quality of power made available to customers by having energy storage elements to inject or absorb real or reactive power to maintain voltage and frequency. The increased short circuit capacity due to the presence of DERs requires the microgrid to have a level of protection better or comparable to the existing grid.

The objective of this section is to compare the effects when SSFIDs or conventional CBs are used for isolation of microgrids from the main electric grid. Another objective of this section is to demonstrate that the SSFID does not affect the stability of a microgrid having a properly controlled distributed generator unit during planned and unplanned switching and subsequent islanding process. The severity of the transients experienced by the microgrid, subsequent to an unplanned islanding process, is highly dependent on i) the pre-islanding operating conditions, ii) the type and location of the fault that initiates the islanding process, iii) the islanding detection time interval, iv) the post-fault switching actions that are envisioned for the system and, v) the type of DG units within the microgrid [18]. However, this thesis only focuses on the pre-islanding operating conditions and the type of faults. The fault is assumed to be located on the legacy grid. The islanding detection time interval and control/protection methods are not discussed. The SSFIDs open subsequent to the occurrence of a fault and stay open until the end of the simulation. No reclosing action takes place for the SSFIDs. The controller for the DG unit is not optimized. Hence better transient performance could be expected when they are optimized.

4.2. MICROGRID TEST SYSTEM

To observe the impact of SSFIDs on fault studies and subsequent islanding for the FREEDM system, a microgrid test system consisting of a stiff grid representing the legacy grid and a Type 1 wind power plant (WPP), together feeding a constant power load is created. The single-line diagram for the system and the system created in PSCAD are shown in Figures 4.1 and 4.2, respectively. A synchronous generator used as a standby DG to support the load when either of the two sources are forced offline due to faults. The ratings for the grid, the WPP, and the DG are shown in Figure 4.2.

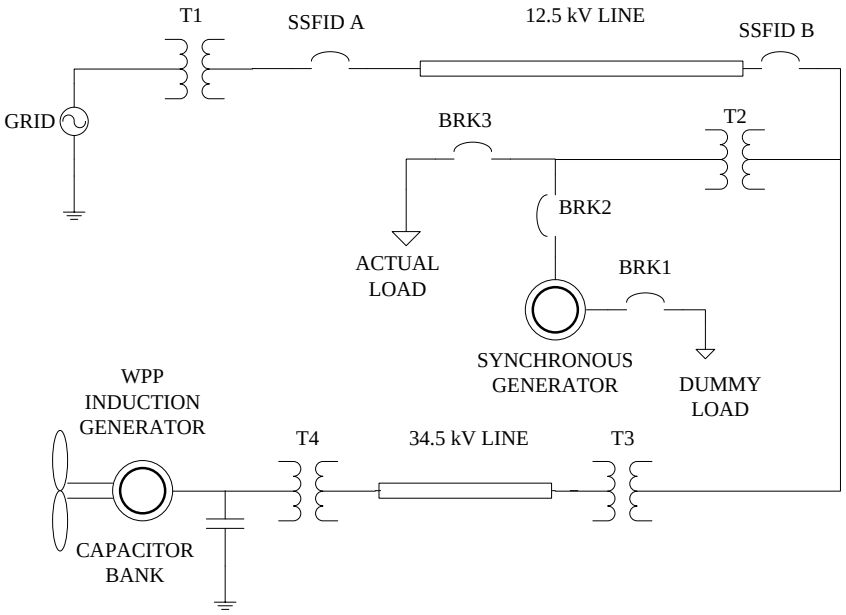


Figure 4.1. Single Line Diagram for Microgrid Test System.

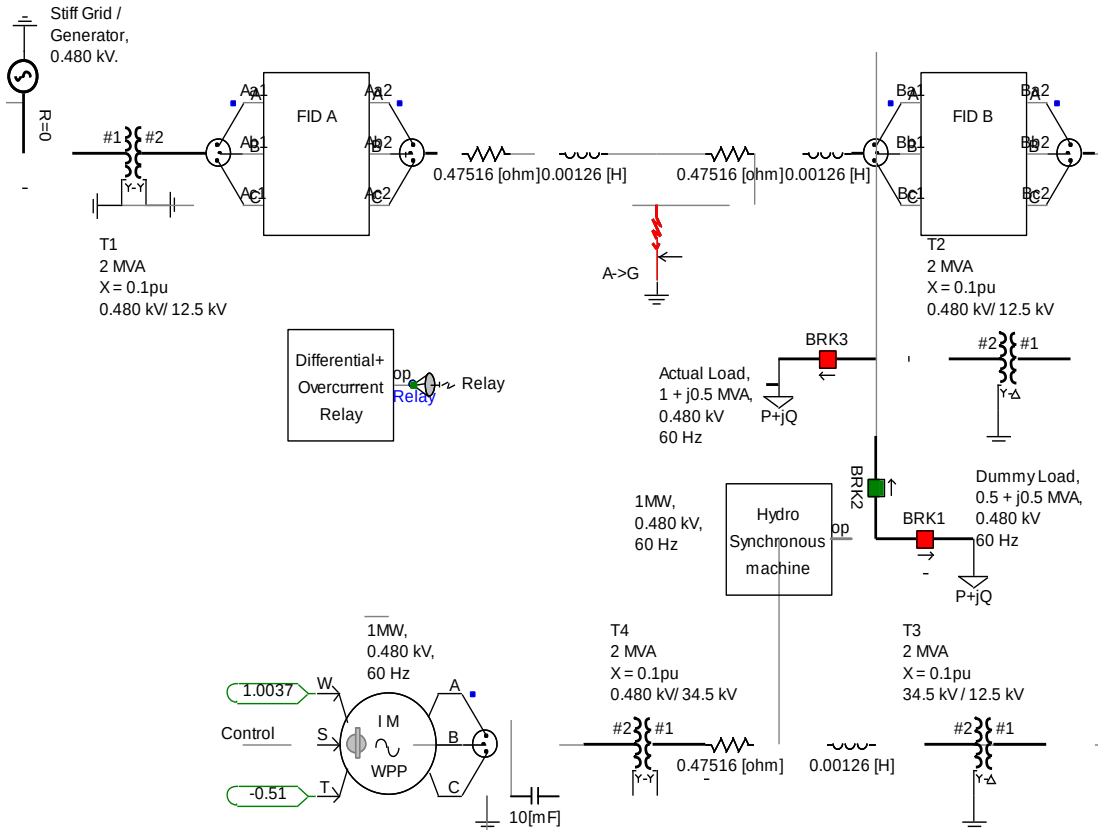


Figure 4.2. Microgrid Test System in PSCAD.

The stiff grid, the WPP, the DG as well as the load are all operating at 480 V. The grid is connected to the load through two 0.480kV/12.5 kV transformers. The SSFIDs are connected on the 12.5kV section. The WPP is connected to the load through a wye ungrounded- wye ungrounded transformer that steps up the voltage from 480 V to 34.5 kV and through another transformer that steps down the voltage from 34.5 kV to 12.5kV. The DG is directly connected to the load bus through a conventional circuit breaker. A combination of a differential and an over-current protection scheme has been provided for the relay that provides gate signals for the SSFIDs.

4.3. SIMULATION SEQUENCE AND RESULTS

At any point of the simulation, a combination of any two of the grid, the WPP and the DG can support the load equally by supplying half of the power. The grid and the WPP together supply the load from the start of the simulation until the point when a fault occurs at time t= 4 sec of the simulation. Following the occurrence of the fault, a large fault current tends to flow into the fault. However, the relay senses this fault current and trips the SSFIDs almost instantaneously. The DG is connected to the load at time t = 4.2 sec by switching the circuit breaker and thereafter the load is sustained by the two sources.

The synchronous machine DG is initially connected to a dummy load in order to keep the machine spinning before connecting to serve the actual load. If the dummy load is not used, the DG fails to pick up the required load fast enough which leads to system instability. A complete synchronous generator system with its exciter control and speed governor control available in the PSCAD library is used for the DG. The model is shown in Figure 4.3.

The WPP is represented as a SCIG compensated by a 10 mF capacitor connected at its terminals. This size of the capacitor is selected such that it supports voltages of 1.06 pu and 0.98 pu at the WPP and the load terminals respectively. For the purpose of simulation, the WPP is operated in a constant torque mode in steady state (from time t = 0 sec to time t = 4 sec) as it helps to control the output power of the WPP. During transients following the occurrence of fault at t = 4 sec, the WPP is immediately switched to the constant speed mode which regulates the torque by itself but keeps the rotor speed constant. In a practical system, this may represent a load change not affecting the speed

of the SCIG because of the high inertia of such generators as well as due to the parallel operation of the WPP which reduces the impact of the load change on a single SCIG. Also, speed governing control systems are able to take an almost immediate corrective action as the time constant for the electrical frequency is much smaller compared to the time constant of the mechanical frequency of the rotor of the SCIG. When the system settles down following the clearing of the fault and subsequent connection of the DG to the load, the WPP is brought back to operate in the torque control mode again at time t = 8 sec.

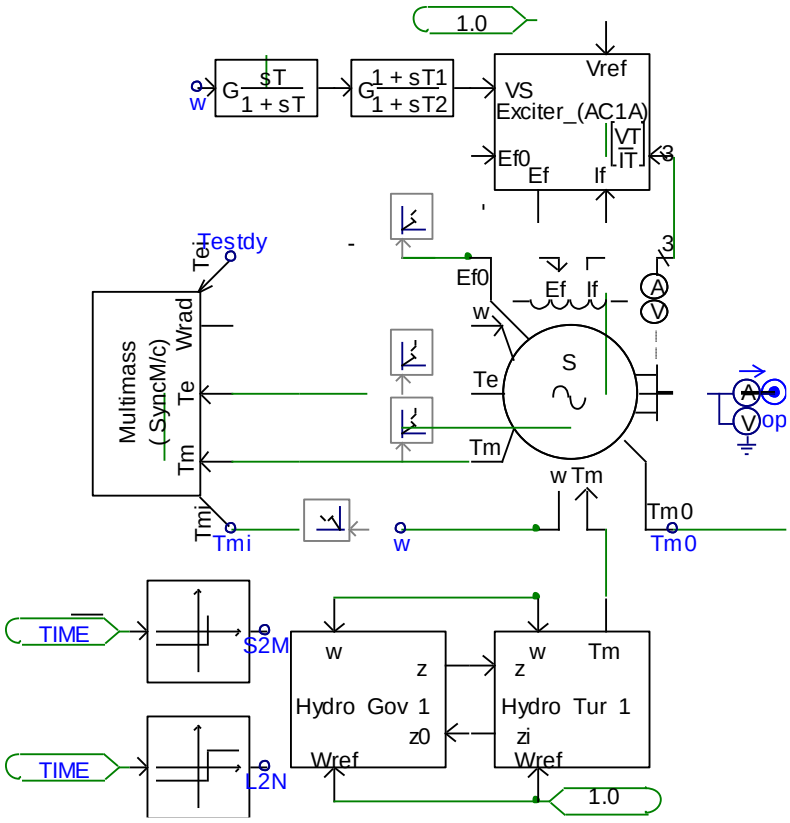


Figure 4.3. PSCAD Synchronous Machine Model as DG.

The different cases studied to demonstrate the stability of the microgrid when SSFIDs are used for the above mentioned simulation sequence for different kinds of faults namely - (i) single line-ground fault (ii) line-line fault (iii) line-line-ground fault (iv) three-phase fault, are -

a) The dummy load is equal to the part of the load taken up by the DG when the microgrid operates in the islanded mode. This case is used for comparing effects of SSFIDs and conventional CBs microgrids are isolated from the main grid..
b) The dummy load is not equal to the part of the load taken up by the DG when the microgrid operates in the islanded mode

Case a)

For faults on the grid side, the SSFIDs are able to limit the fault currents from the grid side to about 25% of values when the conventional CBs are used. The comparisons are shown in Figures 4.4, 4.5, 4.6, 4.7, respectively.

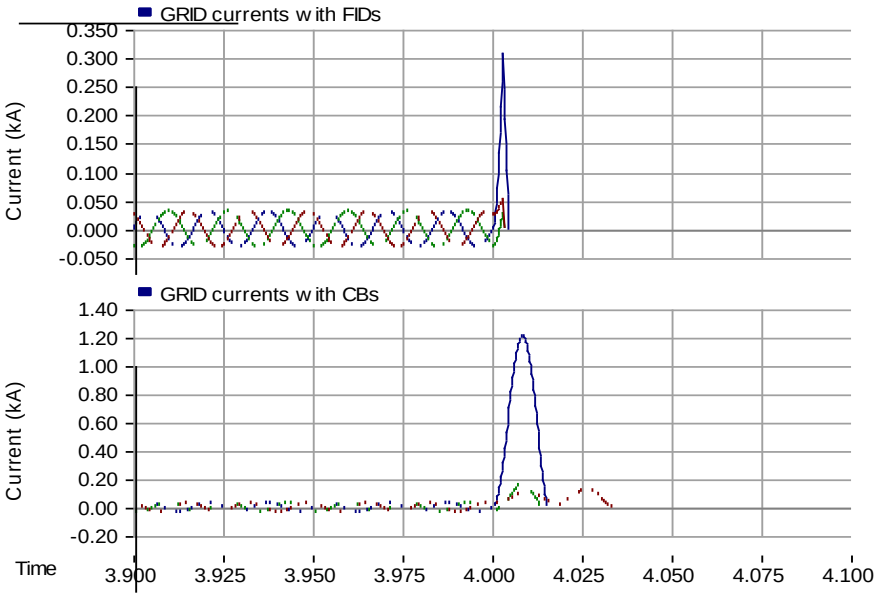


Figure 4.4. Grid Currents with SLG Fault on Grid Side.

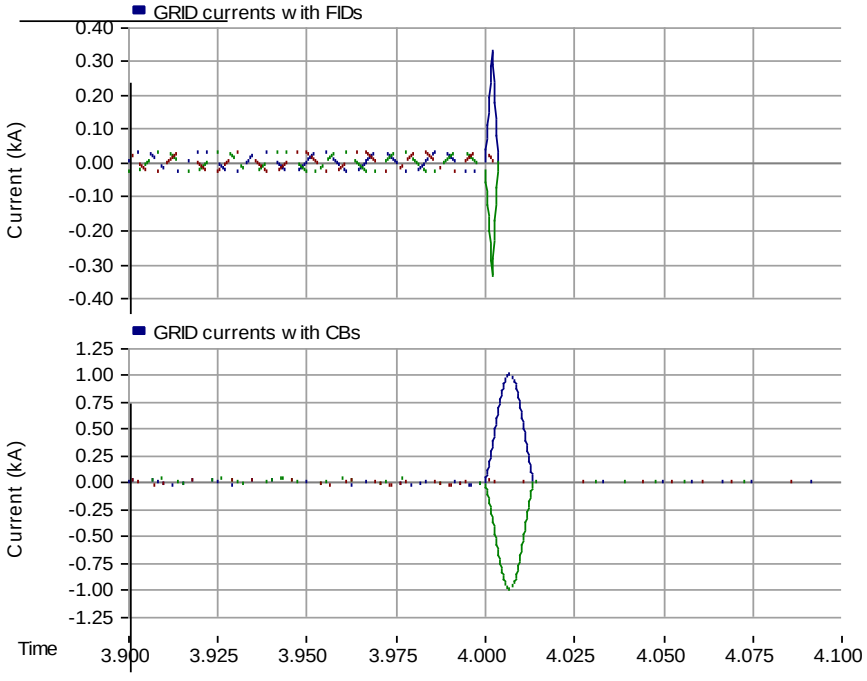


Figure 4.5. Grid Currents with LL Fault on Grid Side.

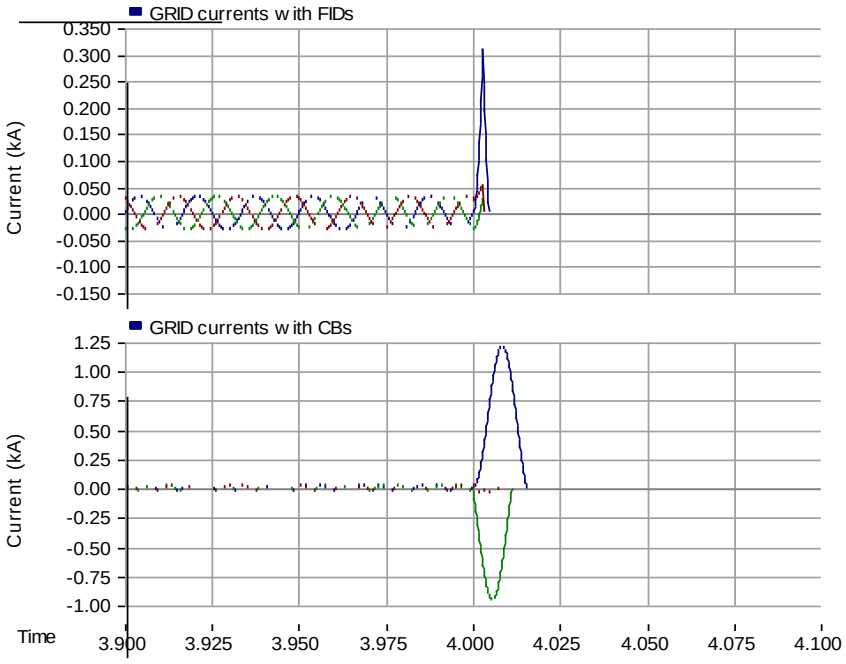


Figure 4.6. Grid Currents with LLG Fault on Grid Side.

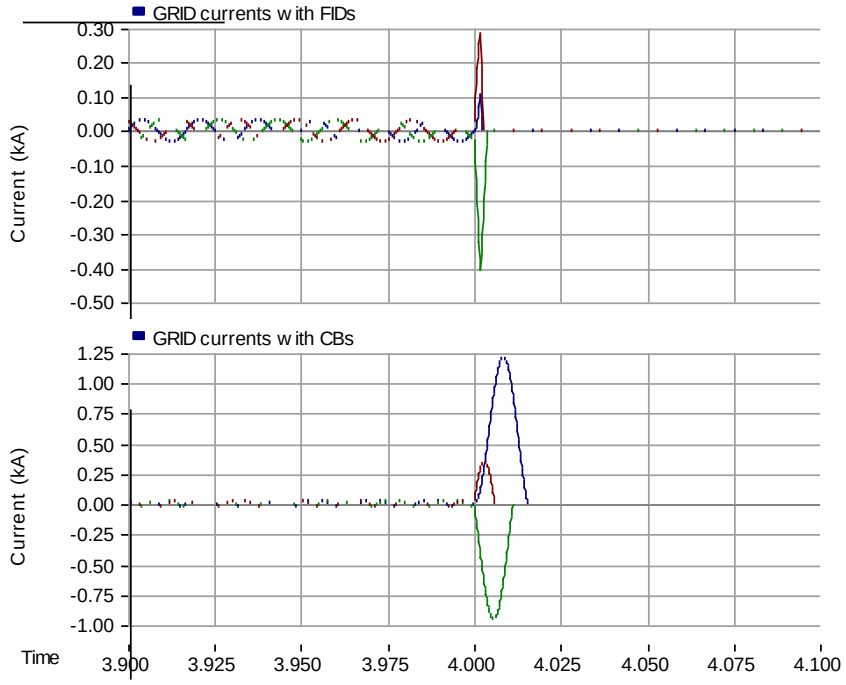


Figure 4.7. Grid Currents with 3 Phase Fault on Grid Side.

Thus, it is observed that the SSFIDs limit the fault current and never let it reach its peak value. The SSFIDs interrupt the fault current before it reaches the first peak. The fault currents are restricted to 25% of values that are observed when conventional circuit breakers are used. Also, other components of the system such as the transformer is subjected to lower stresses developed as a consequence of the lower peak fault currents.

The fast chopping and subsequent interruption of current by the SSFIDs leads to a voltage of 1.8pu on the grid side. The conventional CB interrupts the current at the next current zero and hence the transient voltage is zero. The voltages are shown in Figures 4.8, 4.9, 4.10 and 4.11, respectively.

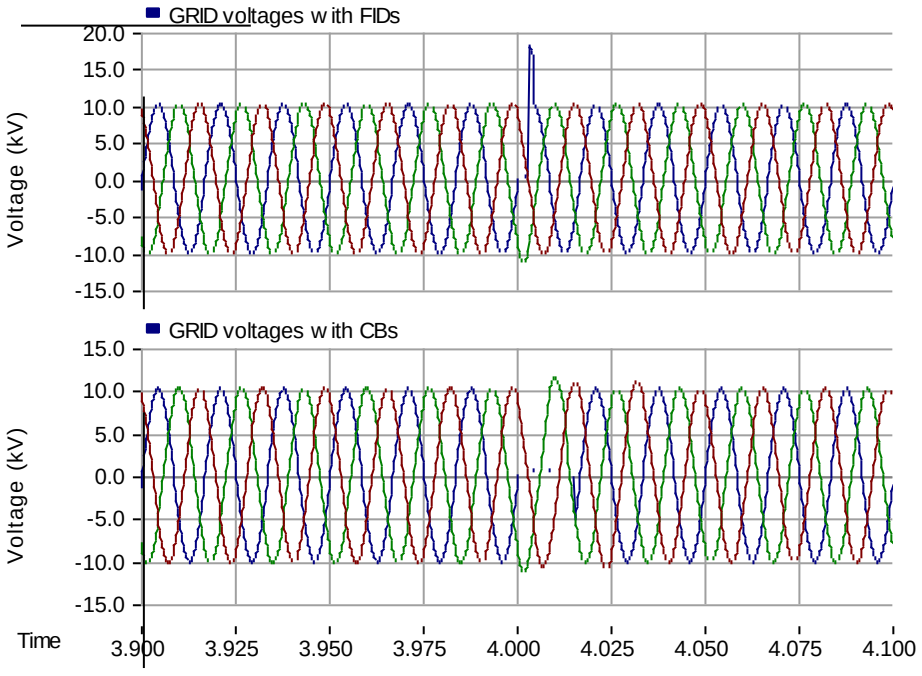


Figure 4.8. Grid Voltage with SLG Fault on Grid Side.

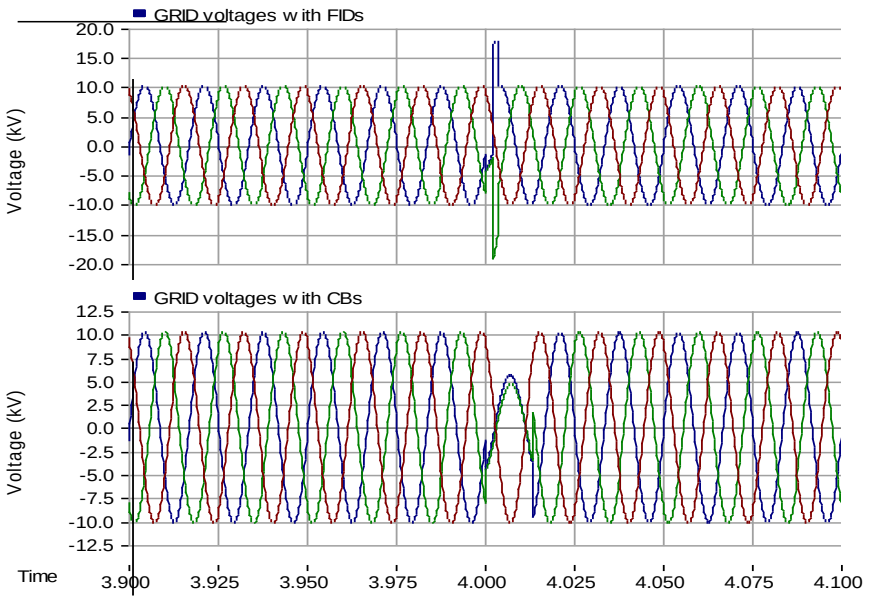


Figure 4.9. Grid Voltage with LL Fault on Grid Side.

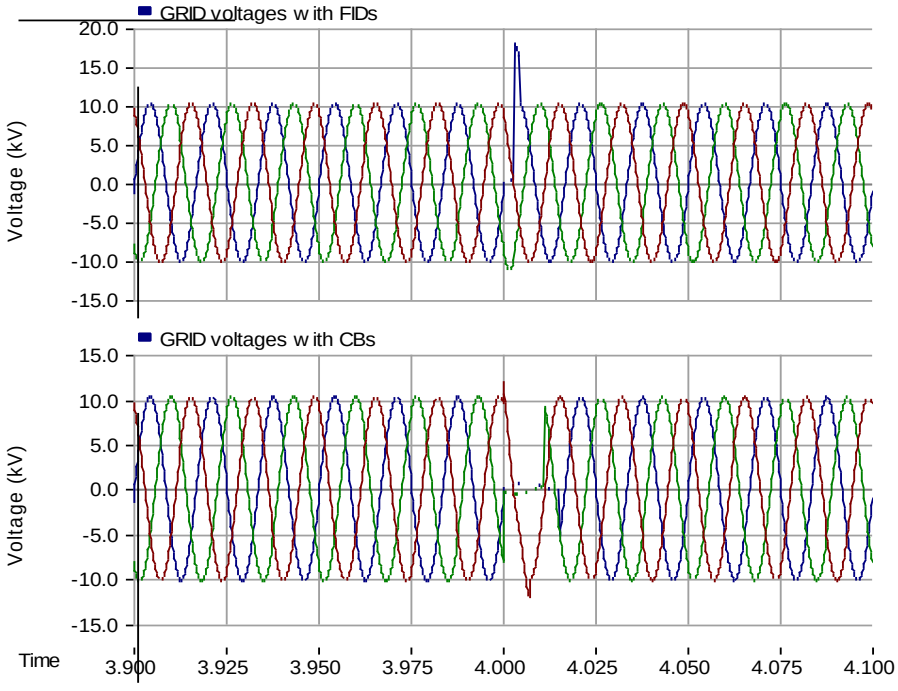


Figure 4.10. Grid Voltage with LLG Fault on Grid Side.

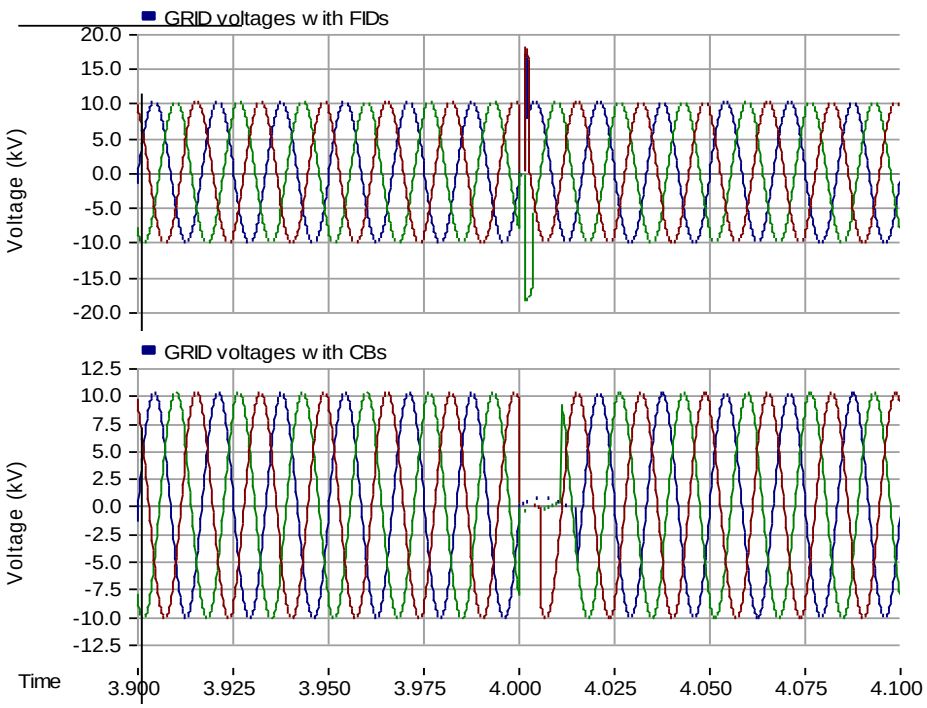


Figure 4.11. Grid Voltage with 3 Phase Fault on Grid Side.

The high transient voltage developed across the grid due to interruption by the SSFIDs can easily be limited by using shunt MOVs. Since the SSFIDs are able to isolate the grid from the islanded microgrid much faster than the conventional CB, the time for which voltage is low due to the fault is negligible as compared to that for the conventional circuit breaker. This shows that power quality is definitely better when SSFIDs are used.

The immediate clearing of the fault by the SSFIDs also obviates the need for the grid to supply MVars to maintain the required voltage profiles on the grid side of the network. Hence, a sudden injection of 1.7pu to 3.5 pu of reactive power supplied by the grid for the different type of faults is not seen on the grid side unlike what is observed

when conventional CBs are used. The powers from the grid for both cases are shown in Figures 4.12, 4.13, 4.14 and 4.15, respectively.

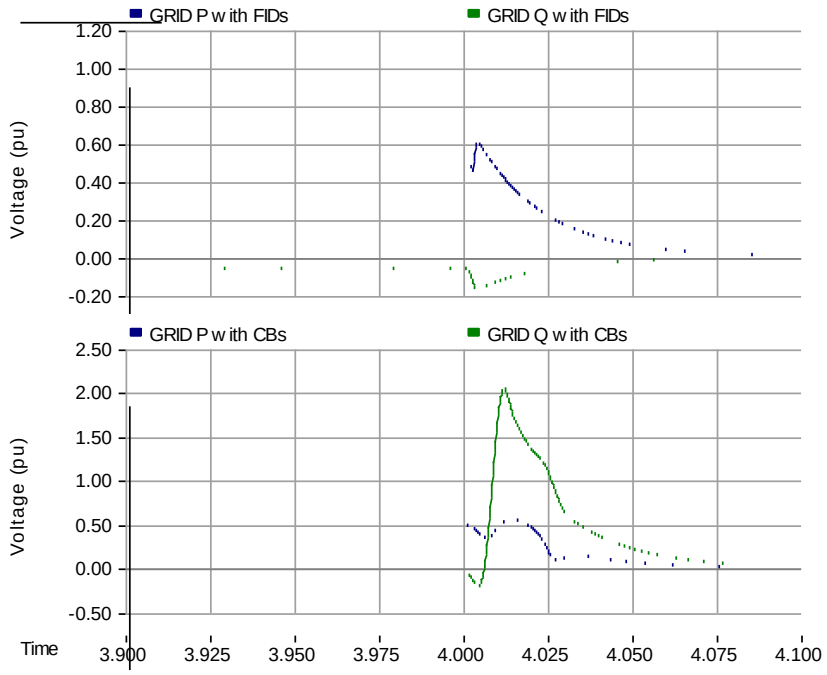


Figure 4.12. Powers from the Grid for SLG Fault on Grid Side.

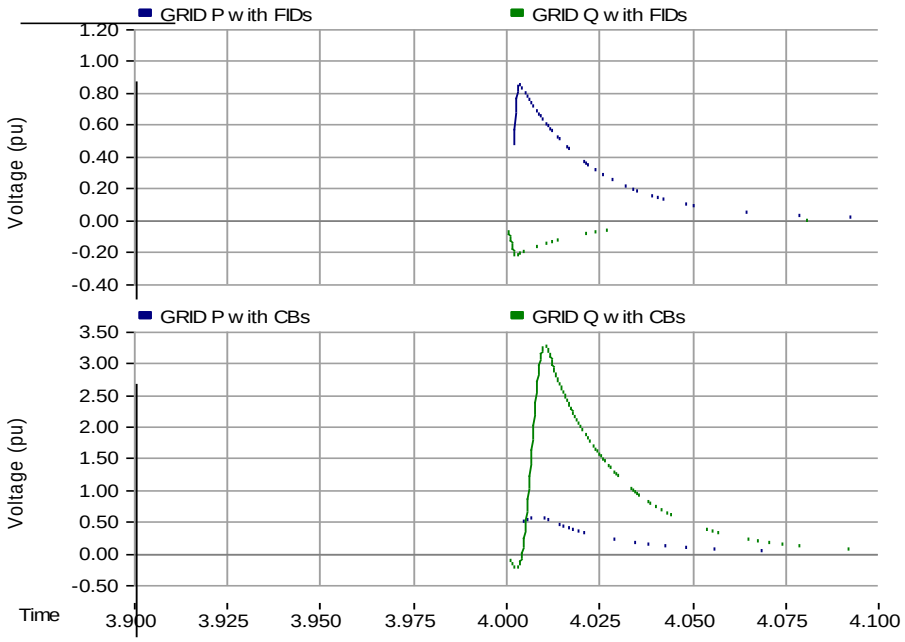


Figure 4.13. Powers from the Grid for LL Fault on Grid Side.

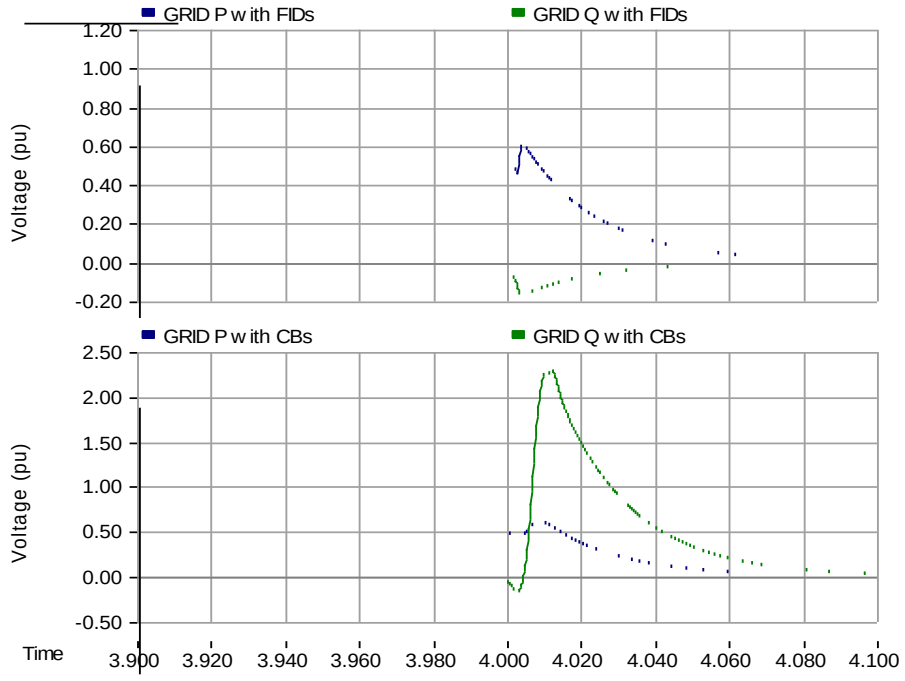


Figure 4.14. Powers from the Grid for LLG Fault on Grid Side.

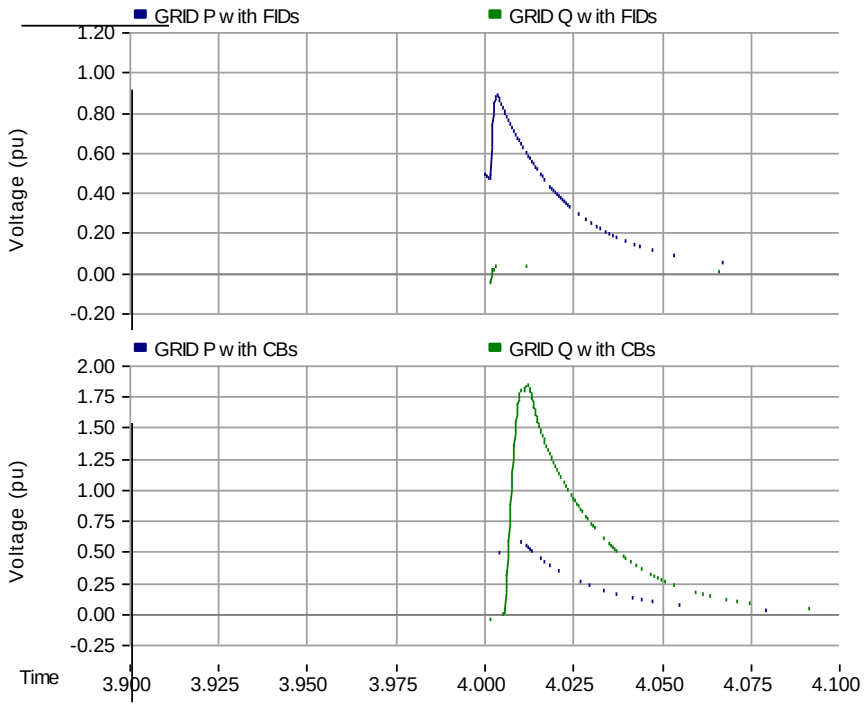


Figure 4.15. Powers from the Grid for 3 Phase Fault on Grid Side.

The effect of any type of fault on the output powers of the WPP is almost the same. For the time interval between the instant of fault occurrence and the instant when the DG is connected to the load, the WPP alone is required to support the load. Hence, the power from the WPP suddenly shoots up at t = 4sec.This is done by increasing the torque of the WPP while keeping the speed of the SCIG constant in the constant speed control mode.

The input torque for an SCIG is negative in the generator mode and positive when it is in the motoring mode. When the DG is connected to the load, the WPP momentarily goes into the motoring mode. Following the transient, the WPP again goes into the generator mode. This is shown in Figure 4.16.

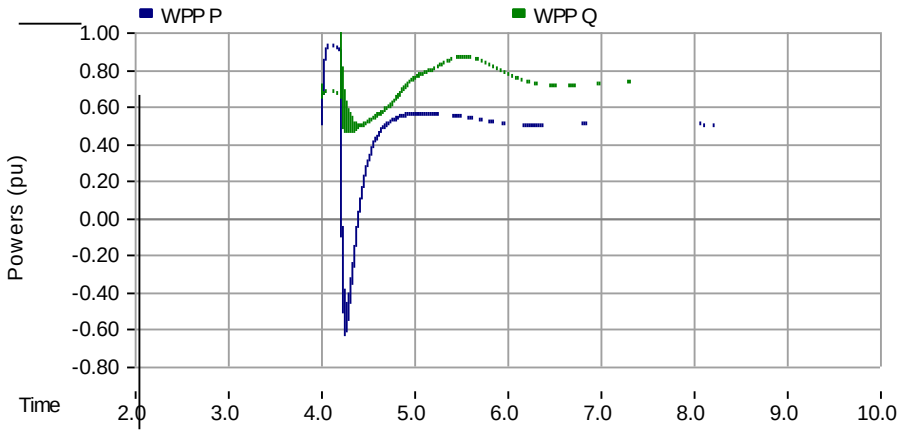


Figure 4.16. Case a WPP Power Output.

The input mechanical torque for the WPP is shown in Figure 4.17. Since the WPP is running in the constant speed mode from time t = 4 sec to time t = 8 sec, the input mechanical torque is variable, and hence it changes negative 1pu to positive 1.5pu during the transient during which the WPP is in the motoring mode. Following the transient, the torque settles down to its pre-fault value of negative 0.5pu and the WPP again runs in the generating mode.

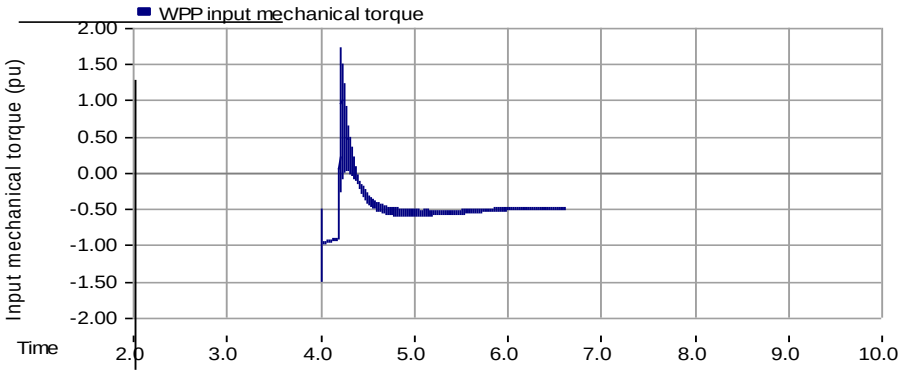


Figure 4.17. Case a WPP Input Mechanical Torque.

For the short interval when the WPP alone supports the load, the voltage at the WPP terminals remains fairly constant. However, if the WPP alone would be made to support the load for an extended period, the capacitor at its terminals would soon discharge making the SCIG inoperable and hence the system will collapse. With the connection of the DG to the load, the capacitor remains charged and the system operates as before. The WPP terminal voltage is shown in Figure 4.18.

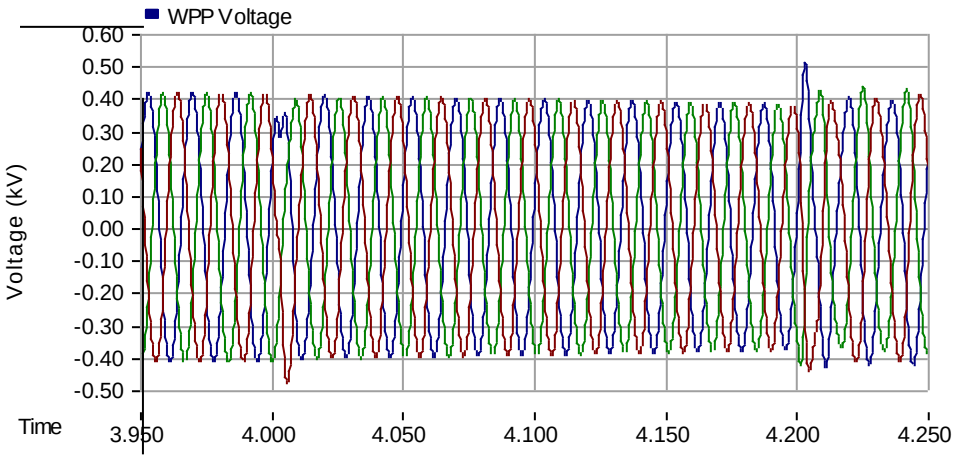


Figure 4.18. Case a WPP Terminal Voltage.

The momentary transition of the WPP into the motoring mode is due to the conditions at the DG terminals. When the DG is synchronized with the actual load, it produces a sharp peak of output power due to a momentary increase in the load angle of the synchronous machine. Like the grid, the DG also acts as a sink for the reactive power from the WPP. The powers at the DG terminals and the load angle are shown in Figures 4.19 and 4.20, respectively.

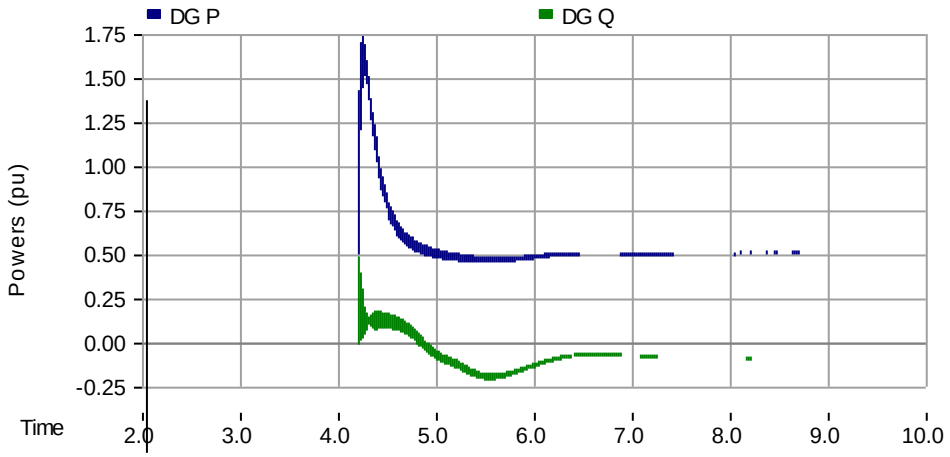


Figure 4.19. Case a Powers at DG Terminals.

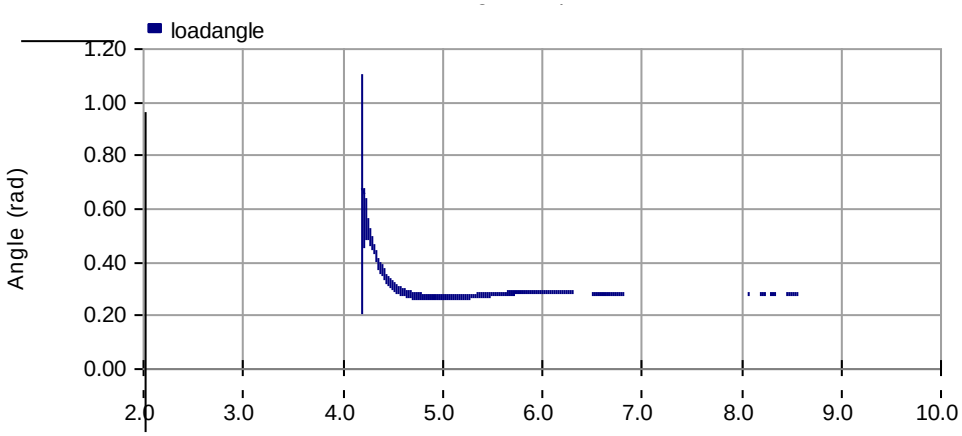


Figure 4.20. Case a Load Angle of DG.

Following the connection of the DG to the load, the DG terminals experience an increase in the voltage due to the change in direction of the DG reactive power during the

transient period. However, they are soon brought back to the rated value by exciter control of the DG. The DG terminal voltage is shown in Figure 4.21.

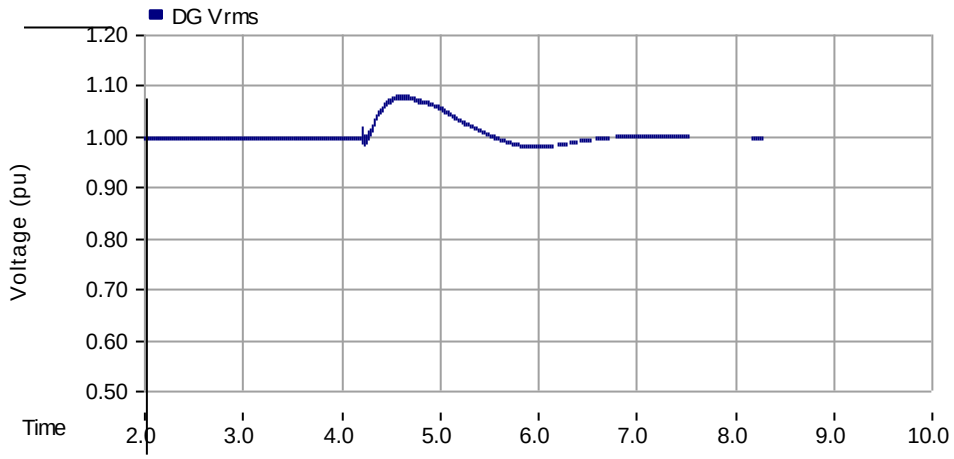


Figure 4.21. Case a DG Terminal rms Voltage.

From the instant of fault occurrence at t = 4sec to the instant the DG is connected to the load at t = 4.2 sec, the power and the voltage at the load terminals follows the powers and voltage at the WPP terminals. Following the connection of the DG, the power and the voltage return back to the pre-fault values after a transient. This is shown in Figures 4.22 and 4.23, respectively.

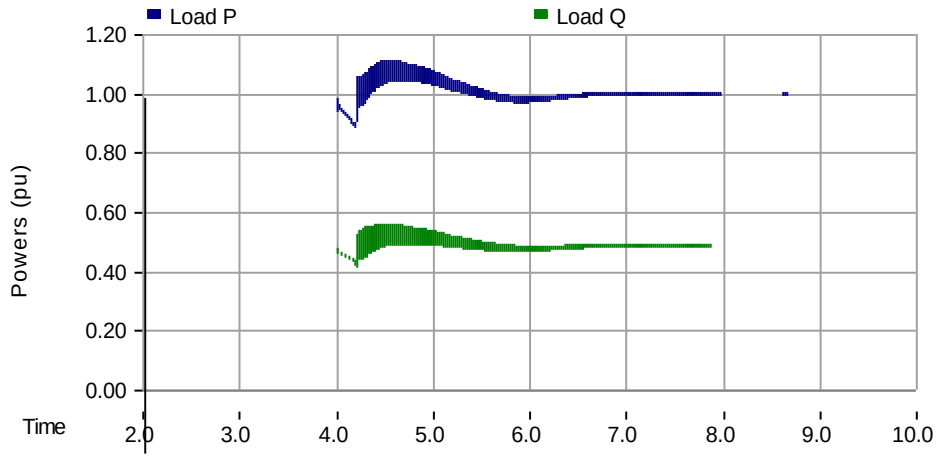


Figure 4.22. Case a Load Powers.

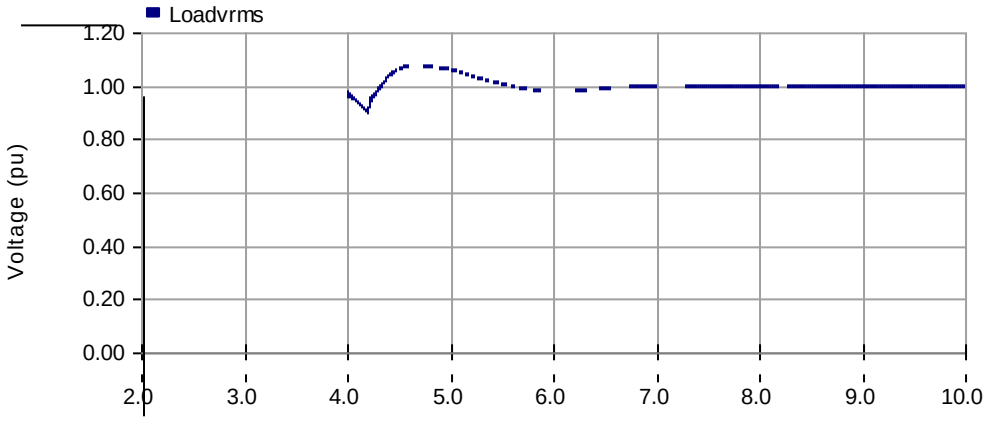


Figure 4.23. Case a Load Voltage.

Case b)

In this case, the dummy load is assumed to be consuming 0.4 MW and 0.4 MVAR respectively. Apart from different load, the behavior of all components essentially

remains the same. From t= 4s to t= 4.2s, the WPP supplies the same amount of power to the load. However, the input torque to the WPP shoots upto positive 2.8 pu during the transient to absorb to inrush of real power from the DG. This is seen in Figures 4.24 and 4.25.

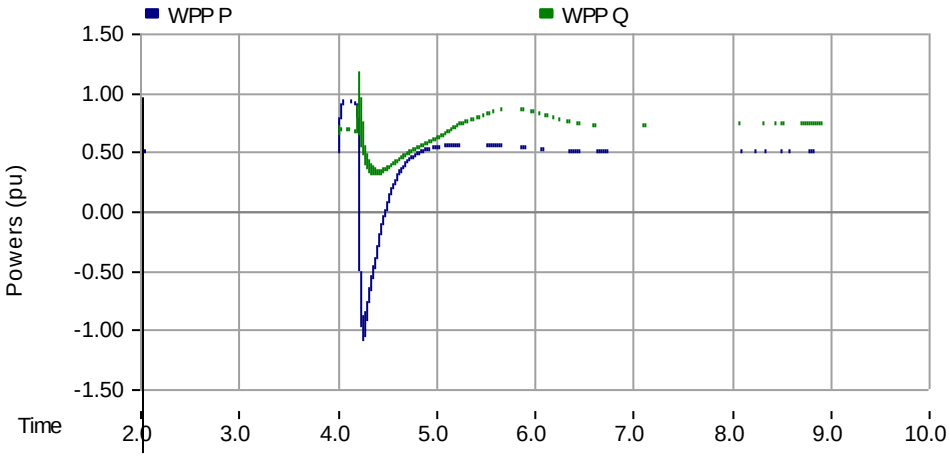


Figure 4.24. Case b WPP Power Output.

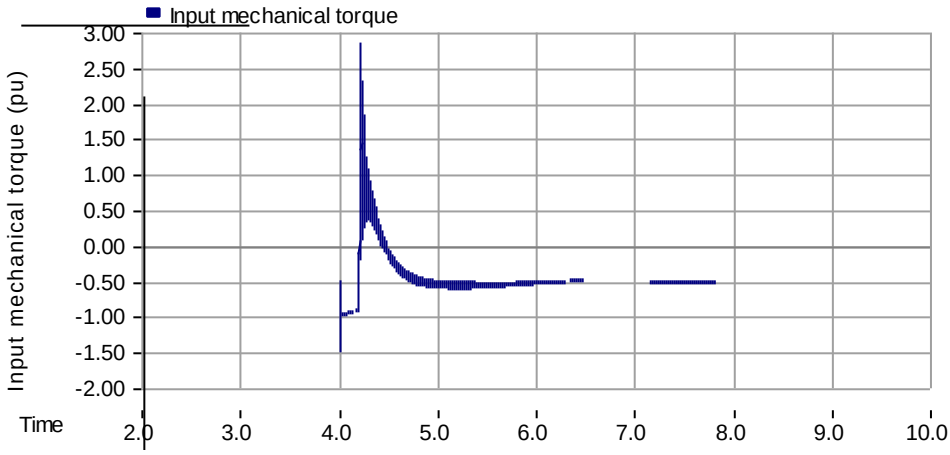


Figure 4.25. Case b WPP Input Mechanical Torque.

When the DG is connected to the load, the combined generation by the WPP and DG is not sufficient to power the load. The DG load angle instantly increases to make up the required power. The DG real power reaches a peak of 2pu as compared to 1.75pu for Case (a) as shown in Figure 4.26.

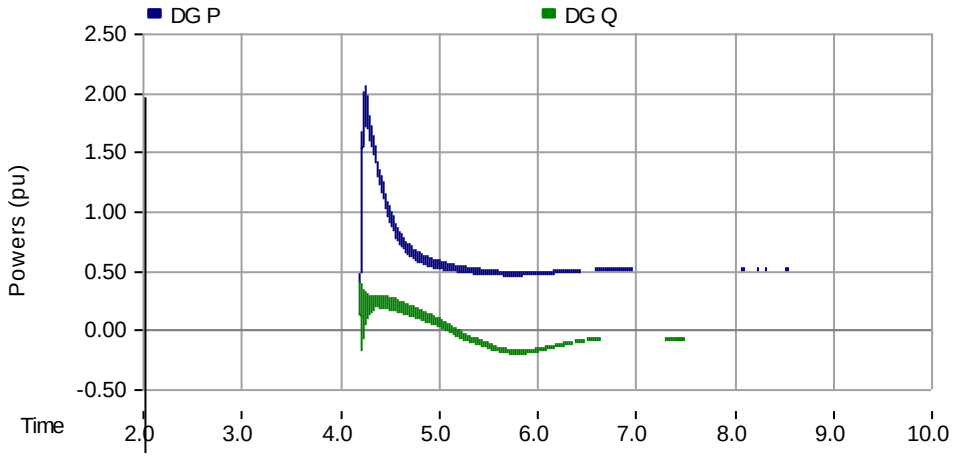


Figure 4.26. Case b Powers at DG Terminals.

Since the DG has a governor control system, it slowly ramps down its output power to match up the load demand. The deficiency in the power supplied at the instant of connection by the DG to the load causes deeper sags at the load. The sag in real power reaches 0.8 pu value as against 0.9pu in Case (a) as shown in Figure 4.27.

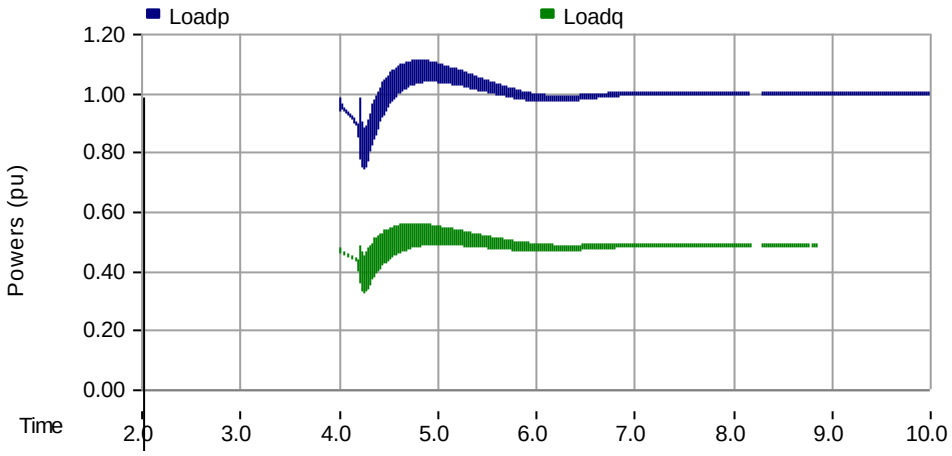


Figure 4.27. Case b Load Powers.

Similarly, the voltage at the load experiences deeper sags. The sag in the measured rms voltage at the load reaches a value of 0.8pu as shown in Figure 4.28.

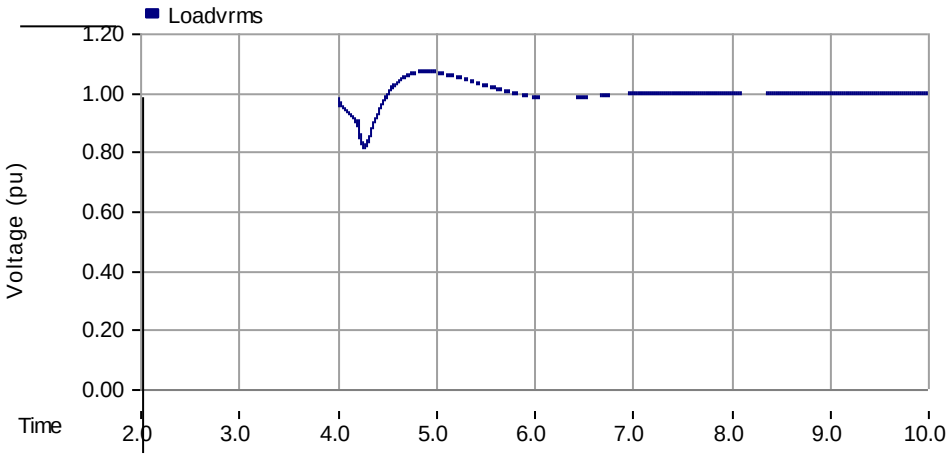


Figure 4.28. Case b Load Voltage.

Hence, unplanned switching with inadequate spinning reserves can cause larger sags in the powers and the voltage at the load. If the need arises, the non-critical loads may have to be shed to maintain system stability and power quality.

5. CONCLUSIONS AND FUTURE WORK

5.1. CONCLUSIONS

The new age digital economy requires a continuous supply of electricity of high quality with minimum frequency and duration of interruptions. To fulfill this need and the need to increase the penetration of electricity from renewable sources, the concept of microgrids has evolved where microgrids will be able to operate in islanded mode or in conjunction with the main electric grid. The main electric grid and the microgrid will both support each other to achieve the common objective of increasing the reliability of the entire network and improving power quality indices.

The interfacing of microgrids with the main electric grid will require the use of state-of-the-start power electronics, semiconductors, control and communications innovations developed in recent times. To demonstrate the possibility of the renewable energy-based microgrid and the main electric grid operating in tandem, the FREEDM system was launched recently. The FREEDM system will serve as a test bed for technologies that could be used for interfacing microgrids with the electric grid. One of those technologies is the solid state fault interruption device (SSFID).

The SSFID is a technology which is slated to replace the mechanical circuit breakers due to their inherent drawback of slow switching. For this thesis, available topologies of SSFIDs have been explored and examined. It was found that all topologies have the same technical behavior. Hence, a comparison on the basis of cost is a must when deciding on the topology to be used for a specific application.

The SSFID is a power electronic circuit breaker. It is composed of a series connection of three modules made up of IGBTs and diodes connected in anti-parallel, and

in common emitter configuration. The SSFID uses an IGBT already available in the market. Each module has a MOV and resistor connected across it to limit over-voltages.

To validate the use of the SSFID in medium voltage distribution systems, it is subjected to four simulated tests. The continuous current carrying test proves that the SSFID will be able to carry the rated current indefinitely when rated conditions are present in the system. The power frequency test proves that the SSFID can carry current with frequency deviations within limits and also withstand the power frequency voltage. The short-circuit current interrupting test proves that the SSFID will be able to withstand the conditions which will be present when it is required to interrupt the fault current during faults. It proves that not only can the SSFID interrupt the fault current but also withstand the transient voltage appearing across its contacts following current interruption. The lightning impulse voltage withstand test proves that the SSFID will be able to withstand the voltage surge that propagates through an electric system when lightning strikes the electric grid.

The efficiency for the SSFID is calculated for different loads and it is found that it essentially remains the same. Hence, the SSFID does not have any detrimental effect on the efficiency of the whole electric system under any conditions. The SSFID and the conventional circuit breaker are compared primarily on their speed of interrupting fault current. For this purpose, a distribution system was simulated and it was found that the SSFID is much faster than the conventional circuit breaker in interrupting fault currents.

To compare the performance and the effects of the SSFID and conventional circuit breakers in the FREEDM system during faults, a system consisting of the main electric grid and a microgrid in parallel, consisting of a wind power plant, a synchronous

generator, and a constant power load was simulated. It was found that the high speed of operation of the SSFID enables a faster interruption of the fault current and an immediate islanding of from the microgrid. The SSFID prevents the fault current from reaching its peak while the mechanical CB only interrupts the fault current at the next current zero irrespective of the type of fault. Also, the line voltage recovers within 3ms of operation of the SSFID thus minimizing the time for which voltage is lost during fault periods. Following the isolation of the grid, the WPP and the DG operate in parallel to supply the load and the microgrid operates in the islanded mode. The DG is capable of making up any shortage of power within a short time for the microgrid to operate in a stable manner.

5.2. FUTURE WORK

The SSFID developed in thesis has been used for a medium voltage distribution system having only WPP and distributed synchronous generator. The SSFID can also be used in microgrids having any other renewable source of electricity like PV cells, fuels cells and battery storage. SSFIDs of lower ratings can also be developed to cater to low voltage systems.

A combination of mechanical CBs and SSFIDs could also be used for extra or ultra high voltage applications. Such applications will require higher ratings for the SSFIDs and novel topologies for the combined fault interrupting system.

APPENDIX

MICROGRID TEST SYSTEM DATA

System frequency: 60 Hz

Grid
Rated L-L Voltage: 480V

Transformer T1
Star grounded- Star grounded
1 MVA, 0.480 kV/12.5 kV, 0.1pu

Transformer T2
Star grounded- Delta
3 MVA, 0.480 kV/12.5 kV, 0.1pu

Transformer T3
Star grounded- Delta
2 MVA, 34.5 kV/12.5 kV, 0.1pu

Transformer T4
Star - Star
2 MVA, 0.480 kV/34.5 kV, 0.1pu

Squirrel Cage Induction Generator
Rated Power: 1340.5 HP
Rated Voltage: 480 V
Rated Current: 1200 A
Input mechanical torque: -0.51pu

Synchronous Machine
Rated Voltage: 480 V
Rated Current: 1200 A

Constant Power Load
Real Power: 1 MW
Reactive Power: 0.5 MVar

IGBT datasheet

V_{CE} = 6500 V
I_C = 400 A

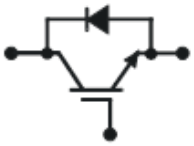


ABB HiPak™

IGBT Module

5SNA 0400J650100

Doc. No. 5SYA 1592-02 Jan 09

- Low-loss, rugged SPT chip-set
- Smooth switching SPT chip-set for good EMC
- High insulation package
- AlSiC base-plate for high power cycling capability
- AlN substrate for low thermal resistance

Maximum rated values [1]

Parameter	Symbol	Conditions	min	max	Unit
Collector-emitter voltage	V_{CES}	V_{GE} = 0 V, $T_{vj} \geq$ 25 °C		6500	V
DC collector current	I_C	T_c = 85 °C		400	A
Peak collector current	I_{CM}	t_p = 1 ms, T_c = 85 °C		800	A
Gate-emitter voltage	V_{GES}		-20	20	V
Total power dissipation	P_{tot}	T_c = 25 °C, per switch (IGBT)		7350	W
DC forward current	I_F			400	A
Peak forward current	I_{FRM}			800	A
Surge current	I_{FSM}	V_R = 0 V, T_{vj} = 125 °C, t_p = 10 ms, half-sinewave		4000	A
IGBT short circuit SOA	t_{psc}	V_{CC} = 4400 V, $V_{CEM CHIP} \leq$ 6500 V $V_{GE} \leq$ 15 V, $T_{vj} \leq$ 125 °C		10	µs
Isolation voltage	V_{isol}	1 min, f = 50 Hz		10200	V
Junction temperature	T_{vj}			125	°C
Junction operating temperature	$T_{vj(op)}$		-40	125	°C
Case temperature	T_c		-40	125	°C
Storage temperature	T_{stg}		-40	125	°C
Mounting torques [2]	M_s	Base-heatsink, M6 screws	4	6	Nm
	M_{t1}	Main terminals, M8 screws	8	10	
	M_{t2}	Auxiliary terminals, M4 screws	2	3	

[1] Maximum rated values indicate limits beyond which damage to the device may occur per IEC 60747
[2] For detailed mounting instructions refer to ABB Document No. 5SYA2039

IGBT characteristic values [3]

Parameter	Symbol	Conditions		min	typ	max	Unit
Collector (-emitter) breakdown voltage	$V_{(BR)CES}$	V_{GE} = 0 V, I_C = 10 mA, T_{vj} = 25 °C		6500			V
Collector-emitter [4] saturation voltage	$V_{CE\,sat}$	I_C = 400 A, V_{GE} = 15 V	T_{vj} = 25 °C		4.2	4.8	V
			T_{vj} = 125 °C		5.4	5.9	V
Collector cut-off current	I_{CES}	V_{CE} = 6500 V, V_{GE} = 0 V	T_{vj} = 25 °C			8	mA
			T_{vj} = 125 °C		35	80	mA
Gate leakage current	I_{GES}	V_{CE} = 0 V, V_{GE} = ±20 V, T_{vj} = 125 °C		-500		500	nA
Gate-emitter threshold voltage	$V_{GE(TO)}$	I_C = 160 mA, V_{CE} = V_{GE}, T_{vj} = 25 °C		6	7.4	8	V
Gate charge	Q_{ge}	I_C = 400 A, V_{CE} = 3600 V, V_{GE} = -15 V .. 15 V			5.3		µC
Input capacitance	C_{ies}	V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz, T_{vj} = 25 °C			95.3		nF
Output capacitance	C_{oes}				4.41		
Reverse transfer capacitance	C_{res}				0.85		
Turn-on delay time	$t_{d(on)}$	V_{CC} = 3600 V, I_C = 400 A, R_G = 5.6 Ω, V_{GE} = ±15 V, L_σ = 280 nH, inductive load	T_{vj} = 25 °C		700		ns
			T_{vj} = 125 °C		630		
Rise time	t_r		T_{vj} = 25 °C		250		ns
			T_{vj} = 125 °C		220		
Turn-off delay time	$t_{d(off)}$	V_{CC} = 3600 V, I_C = 400 A, R_G = 5.6 Ω, V_{GE} = ±15 V, L_σ = 280 nH, inductive load	T_{vj} = 25 °C		1410		ns
			T_{vj} = 125 °C		1700		
Fall time	t_f		T_{vj} = 25 °C		650		ns
			T_{vj} = 125 °C		980		
Turn-on switching energy	E_{on}	V_{CC} = 3600 V, I_C = 400 A, V_{GE} = ±15 V, R_G = 5.6 Ω, L_σ = 280 nH, inductive load	T_{vj} = 25 °C		2250		mJ
			T_{vj} = 125 °C		2800		
Turn-off switching energy	E_{off}	V_{CC} = 3600 V, I_C = 400 A, V_{GE} = ±15 V, R_G = 5.6 Ω, L_σ = 280 nH, inductive load	T_{vj} = 25 °C		1340		mJ
			T_{vj} = 125 °C		2120		
Short circuit current	I_{SC}	t_{psc} ≤ 10 µs, V_{GE} = 15 V, T_{vj} = 125 °C, V_{CC} = 4400 V, $V_{CEM\,CHIP}$ ≤ 6500 V			1800		A
Module stray inductance	$L_{\sigma\,CE}$				20		nH
Resistance, terminal-chip	$R_{CC'+EE'}$		T_C = 25 °C		0.1		mΩ
			T_C = 125 °C		0.15		

[3] Characteristic values according to IEC 60747 – 9
[4] Collector-emitter saturation voltage is given at chip level

Diode characteristic values [4]

Parameter	Symbol	Conditions		min	typ	max	Unit
Forward voltage [6]	V_F	I_F = 400 A	T_{vj} = 25 °C		3.2	3.8	V
			T_{vj} = 125 °C		3.4	4.0	
Reverse recovery current	I_{rr}	V_{CC} = 3600 V, I_F = 400 A, V_{GE} = ±15 V, R_G = 5.6 Ω, L_σ = 280 nH, inductive load	T_{vj} = 25 °C		510		A
			T_{vj} = 125 °C		680		
Recovered charge	Q_{rr}		T_{vj} = 25 °C		450		µC
			T_{vj} = 125 °C		770		
Reverse recovery time	t_{rr}		T_{vj} = 25 °C		1840		ns
			T_{vj} = 125 °C		2120		
Reverse recovery energy	E_{rec}		T_{vj} = 25 °C		670		mJ
			T_{vj} = 125 °C		1380		

[4] Characteristic values according to IEC 60747 – 2
[6] Forward voltage is given at chip level

Package properties [7]

Parameter	Symbol	Conditions	min	typ	max	Unit
IGBT thermal resistance junction to case	$R_{th(j-c)IGBT}$				0.016	K/W
Diode thermal resistance junction to case	$R_{th(j-c)DIODE}$				0.032	K/W
IGBT thermal resistance [3] case to heatsink	$R_{th(c-s)IGBT}$	IGBT per switch, λ grease = 1W/m x K		0.012		K/W
Diode thermal resistance [3] case to heatsink	$R_{th(c-s)DIODE}$	Diode per switch, λ grease = 1W/m x K		0.024		K/W
Partial discharge extinction voltage	V_e	f = 50 Hz, $Q_{PD} \leq$ 10pC (acc. to IEC 61287)	5100			V
Comparative tracking index	CTI			≥ 600		

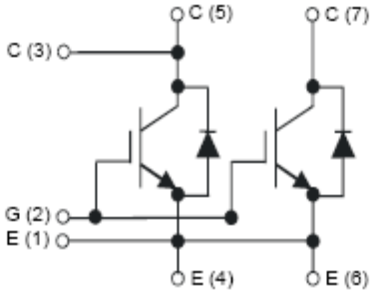
[3] For detailed mounting instructions refer to ABB Document No. 5SYA2039

Mechanical properties [7]

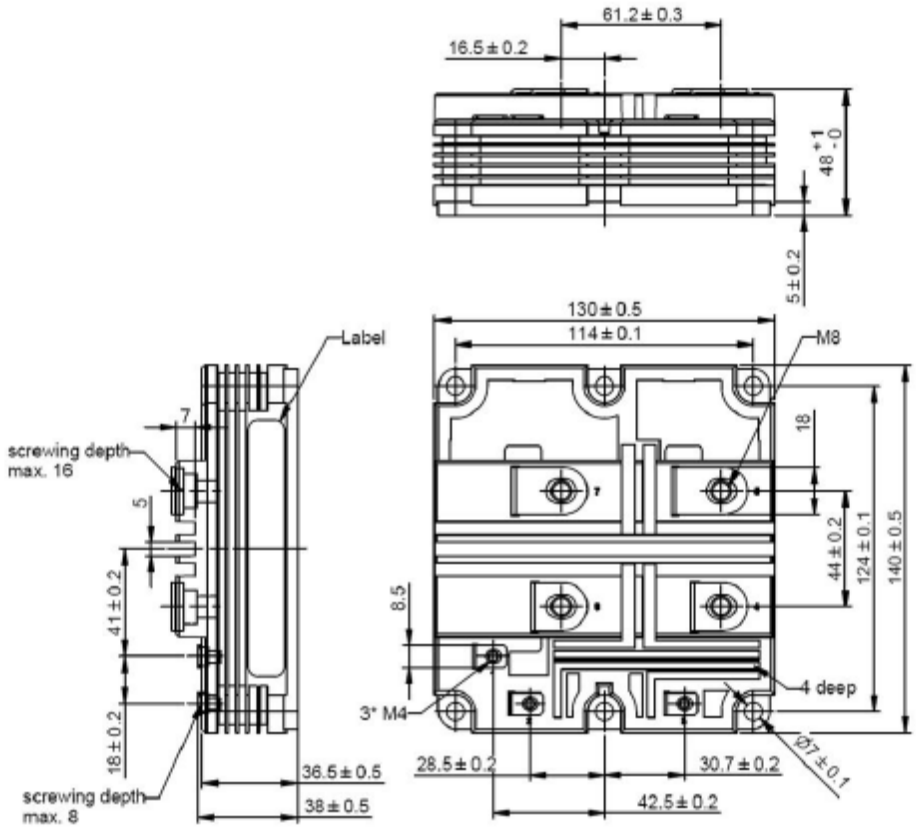
Parameter	Symbol	Conditions		min	typ	max	Unit
Dimensions	L x W x H	Typical , see outline drawing			130 x 140 x 48		mm
Clearance distance in air	d_a	according to IEC 60664-1 and EN 50124-1	Term. to base:	40			mm
			Term. to term:	26			
Surface creepage distance	d_s	according to IEC 60664-1 and EN 50124-1	Term. to base:	64			mm
			Term. to term:	56			
Mass	m				1150		g

[7] Package and mechanical properties according to IEC 60747 – 15

Electrical configuration



Outline drawing [a]



Note: all dimensions are shown in mm

[a] For detailed mounting instructions refer to ABB Document No. 5SYA2039

This is an electrostatic sensitive device, please observe the international standard IEC 60747-1, chap. IX.

This product has been designed and qualified for Industrial Level.

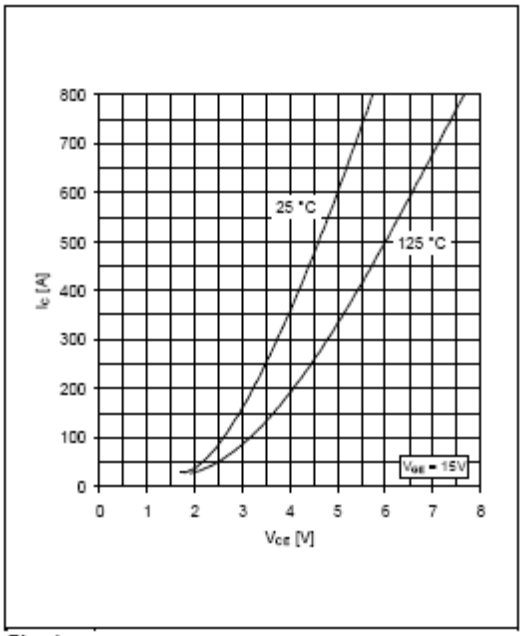


Fig. 1 Typical on-state characteristics, chip level

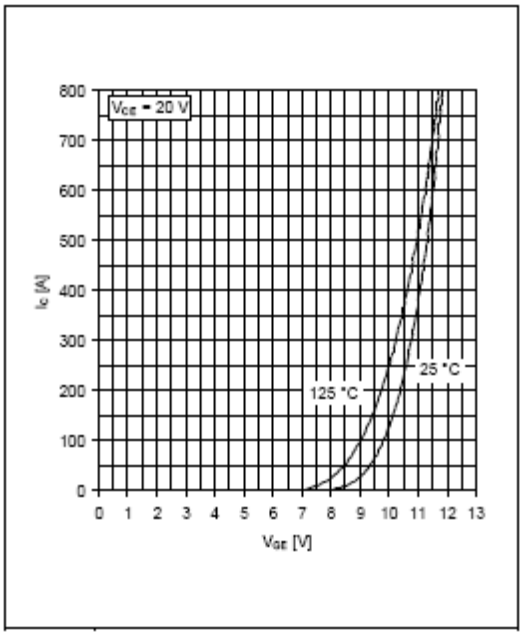


Fig. 2 Typical transfer characteristics, chip level

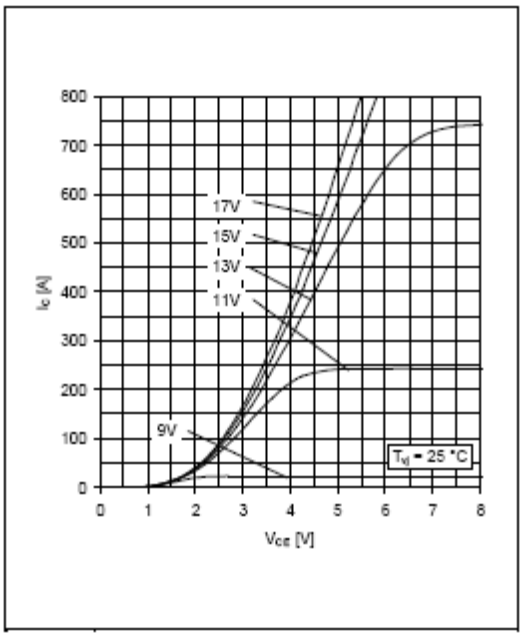


Fig. 3 Typical output characteristics, chip level

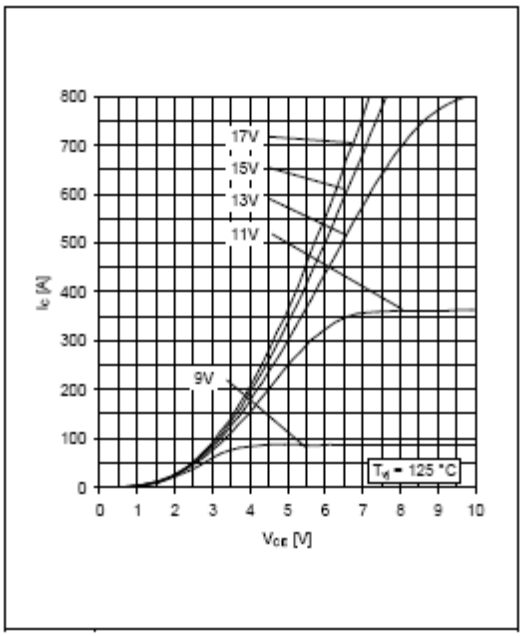


Fig. 4 Typical output characteristics, chip level

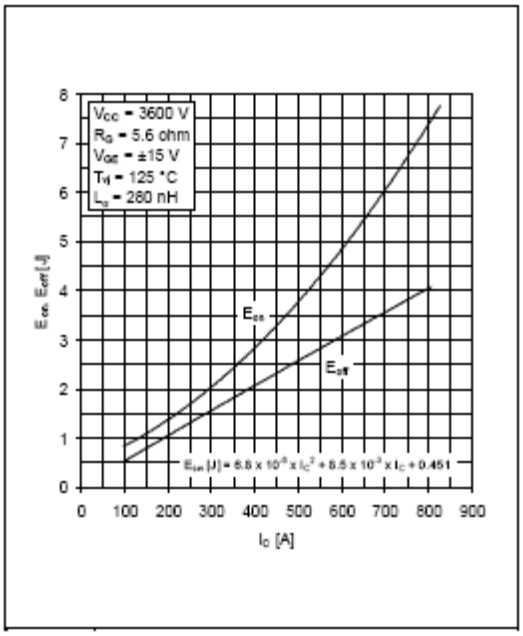


Fig. 5 Typical switching energies per pulse vs collector current

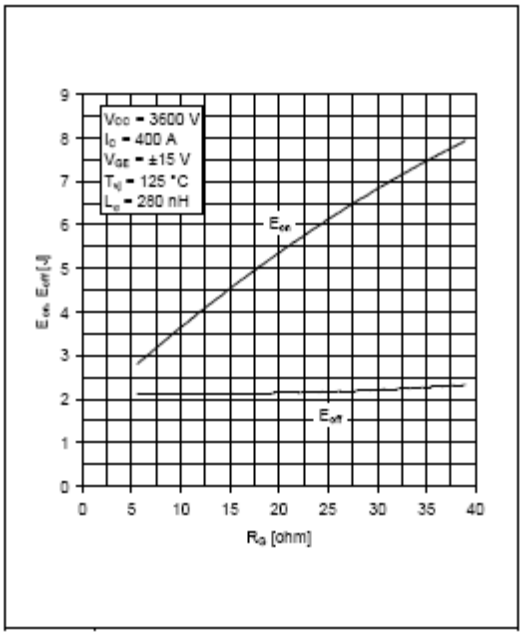


Fig. 6 Typical switching energies per pulse vs gate resistor

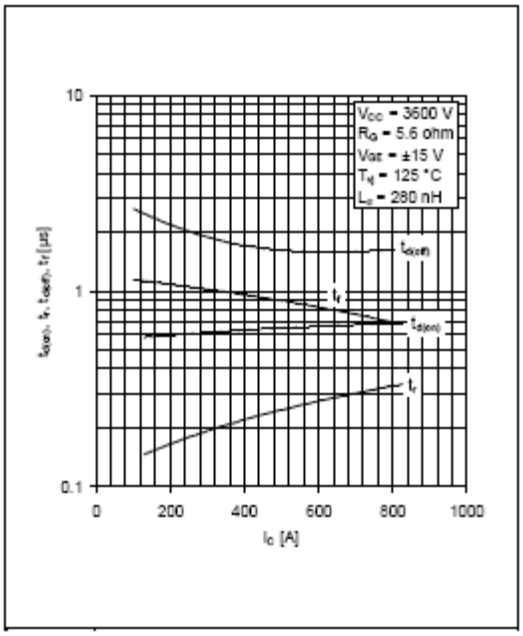


Fig. 7 Typical switching times vs collector current

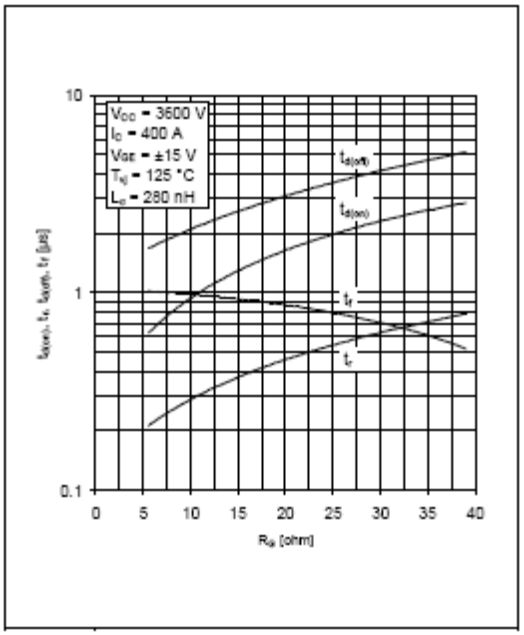


Fig. 8 Typical switching times vs gate resistor

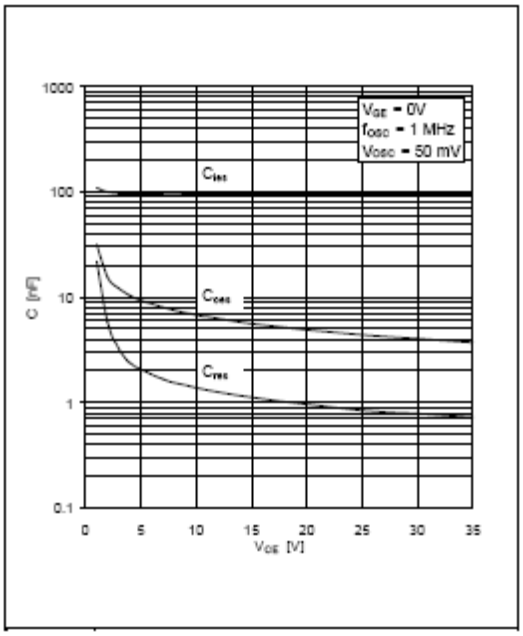


Fig. 9 Typical capacitances vs collector-emitter voltage

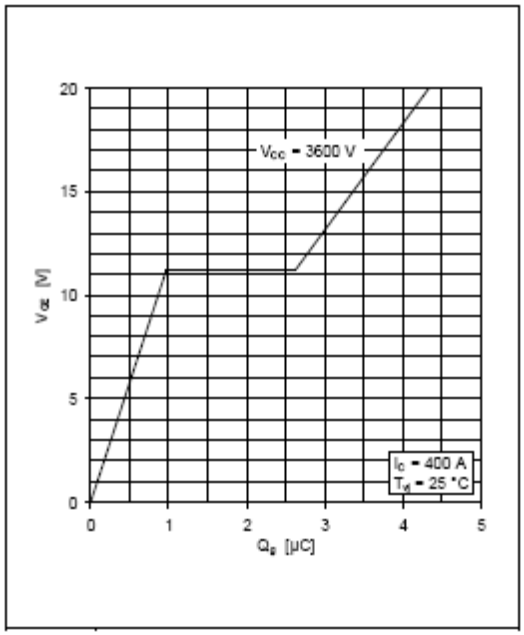


Fig. 10 Typical gate charge characteristics

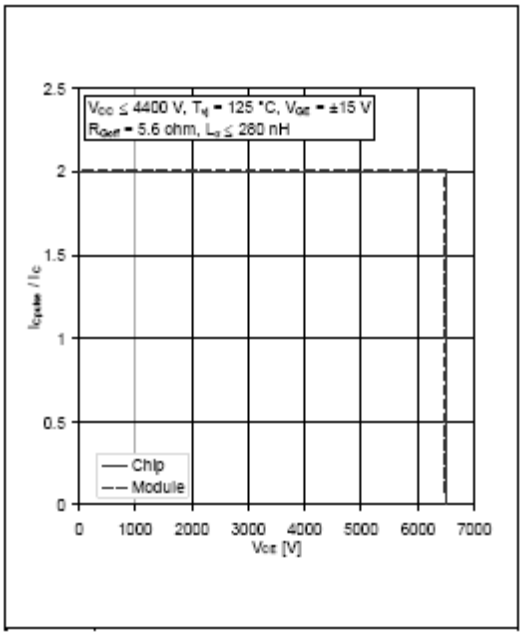


Fig. 11 Turn-off safe operating area (RBSOA)

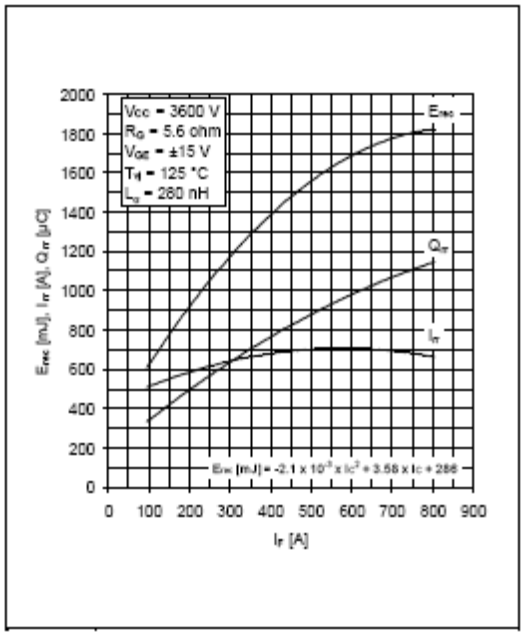


Fig. 12 Typical reverse recovery characteristics vs forward current

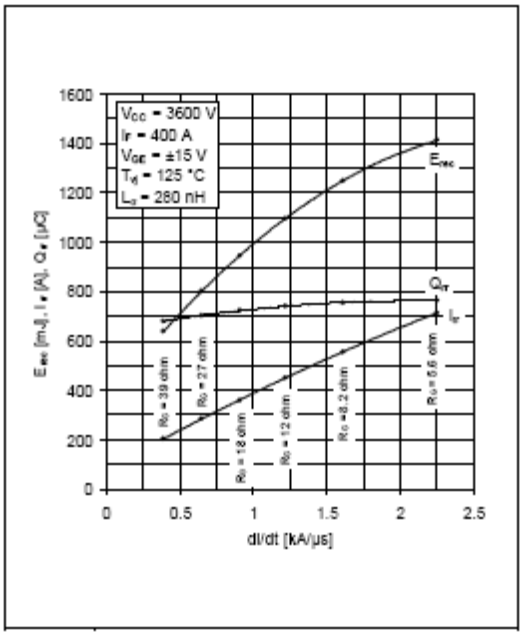


Fig. 13 Typical reverse recovery characteristics vs di/dt

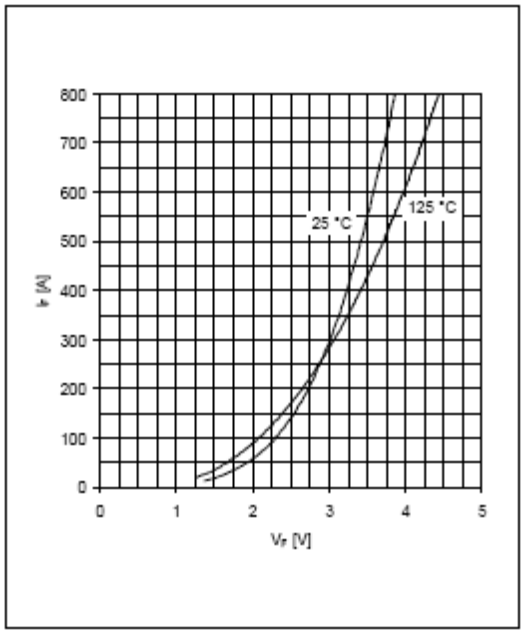


Fig. 14 Typical diode forward characteristics, chip level

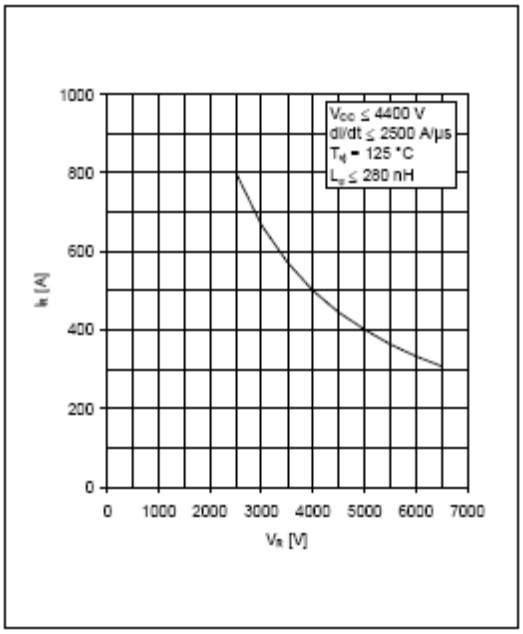


Fig. 15 Safe operating area diode (SOA)

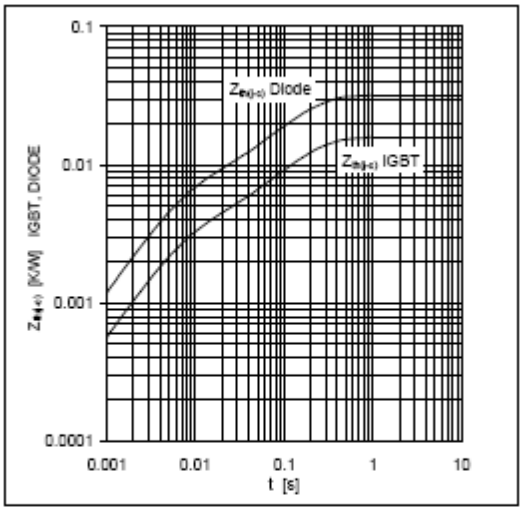


Fig. 16 Thermal impedance vs time

Analytical function for transient thermal impedance:

$$Z_{th\,(j\text{-}c)}(t) = \sum_{i=1}^{n} R_i\left(1 - e^{-t/\tau_i}\right)$$

	i	1	2	3	4	5
IGBT	R_i(K/kW)	12.75	2.99			
	τ_i(ms)	151	5.84			
DIODE	R_i(K/kW)	25.5	6.3			
	τ_i(ms)	144	5.83			

For detailed information refer to:

- 5SYA 2042 Failure rates of HiPak modules due to cosmic rays
- 5SYA 2043 Load – cycle capability of HiPaks
- 5SYA 2045 Thermal runaway during blocking
- 5SYA 2058 Surge currents for IGBT diodes
- 5SZK 9120 Specification of environmental class for HiPak

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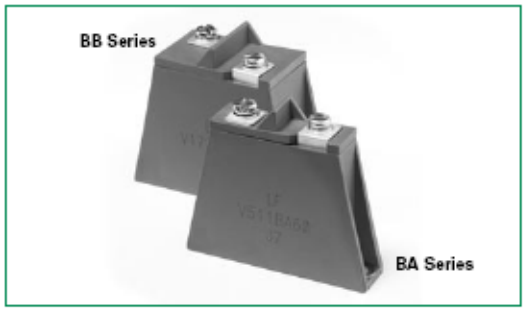
Doc. No. 5SYA 1592-02 Jan 09

MOV Datasheet

Littelfuse
Expertise Applied | Answers Delivered

Varistor Products
Industrial High Energy Terminal Varistors > BA/BB Series

BA/BB Varistor Series



Description

The BA and BB Series transient surge suppressors are heavy-duty industrial Metal-Oxide Varistors (MOVs) designed to provide surge protection for motor controls and power supplies used in oil-drilling, mining, transportation equipment and other heavy industrial AC line applications.

These UL–recognized varistors have similar package construction but differ in size and ratings. The BA models are rated from 130 to 880V_{MIACI}. The BB models from 1100 to 2800V_{MIACI}.

Both the BA and BB Series feature improved creep and strike capability to minimize breakdown along the package surface, a package design that provides complete electrical isolation of the disc subassembly, and rigid terminals to ensure secure wire contacts.

See BA/BB Series Device Ratings and Specifications Table for part number and brand information.

Agency Approvals

Agency	Agency File Number
	E75961-for BA Series only.

Features

- RoHS compliant and Lead–free available
- High energy absorption capability W_{TM}
  BA Series 3200J
  BB Series 10,000J
- Wide operating voltage range $V_{MIACIRMS}$
  BA Series 130V to 880V
  BB Series 1100V to2800V
- Rigid terminals for secure wire contact
- Case design provides complete electrical isolation of disc subassembly
- Littelfuse largest packaged disc 60mm diameter
- No derating up to 85°C ambient

Absolute Maximum Ratings

• For ratings of individual members of a series, see Device Ratings and Specifications chart

Continuous	BA Series	BB Series	Units
Steady State Applied Voltage:			
AC Voltage Range ($V_{MIACIRMS}$)	130 to 880	1100 to 2800	V
DC Voltage Range (V_{MIDC})	175 to 1150	1400 to 3500	V
Transients:			
Peak Pulse Current (I_{TM})			
For 8/20μs Current Wave (See Figure 2)	50,000 to 70,000	70,000	A
Single Pulse Energy Range			
For 2ms Current Squarewave (W_{TM})	450 to 3200	3800 to 10000	J
Operating Ambient Temperature Range (T_A)	-55 to +85	-55 to +85	°C
Storage Temperature Range (T_{STG})	-55 to +125	-55 to +125	°C
Temperature Coefficient (aV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	<0.01	%/°C
Hi-Pot Encapsulation (COATING Isolation Voltage Capability) (Dielectric must withstand indicated DC voltage for one minute per MIL–STD–202, Method 301)	5000	5000	V
COATING Insulation Resistance	1000	1000	MΩ

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

BA/BB Series

Specifications are subject to change without notice.
Please refer to www.littelfuse.com/series/ba or /bb.html for current information.
Revision: January 5, 2009

BA/BB Series Ratings & Specifications

Part Number	Maximum Rating (85°C)				Specifications (25°C)				
	Continuous		Transient		Varistor Voltage at 1mA DC Test Current			Maximum Clamping Volt V_C at 200A Current (8/20μs)	Typical Capacitance f= 1MHz
	V_{RMS}	V_{DC}	Energy (2ms)	Peak Current 8 x 20μs					
	$V_{M(AC)}$	$V_{M(DC)}$	W_{TM}	I_{TM}	Min	$V_{N(DC)}$	Max	V_C	C
	(V)	(V)	(J)	(A)	(V)	(V)	(V)	(V)	(pF)
BA Series									
V131BA60	130	175	450	50000	184	200	228	340	20000
V151BA60	150	200	530	50000	212	240	268	400	16000
V251BA60	250	330	880	50000	354	390	429	620	10000
V271BA60	275	369	950	50000	389	430	473	680	9000
V321BA60	320	420	1100	50000	462	510	561	760	7500
V421BA60	420	560	1500	70000	610	680	748	1060	6000
V481BA60	480	640	1600	70000	670	750	825	1160	5500
V511BA60	510	675	1800	70000	735	820	910	1300	5000
V571BA60	575	730	2100	70000	805	910	1000	1420	4500
V681BA60	680	850	2300	70000	940	1050	1160	1640	4000
V751BA60	750	970	2600	70000	1080	1200	1320	1880	3500
V881BA60	880	1150	3200	70000	1290	1500	1650	2340	2700
BB Series									
V112BB60	1100	1400	3800	70000	1620	1800	2060	2940	2200
V142BB60	1400	1750	5000	70000	2020	2200	2550	3600	1800
V172BB60	1700	2150	6000	70000	2500	2700	3030	4300	1500
V202BB60	2000	2500	7500	70000	2970	3300	3630	5200	1200
V242BB60	2400	3000	8600	70000	3510	3900	4290	6200	1000
V282BB60	2800	3500	10000	70000	4230	4700	5170	7400	800

NOTE: Average power dissipation of transients not to exceed 2.5W. See Figures 3 and 4 for more information on power dissipation.

Power Dissipation Ratings

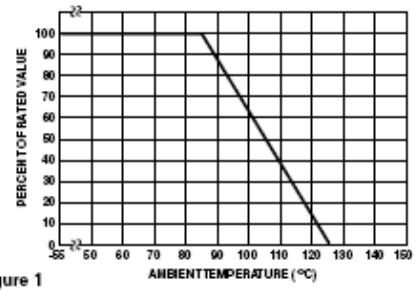


Figure 1

Should transients occur in rapid succession, the average power dissipation required is simply the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Characteristics Table for the specific device. Furthermore, the operating values need to be derated at high temperatures as shown in the above diagram. Because varistors can only dissipate a relatively small amount of average power they are, therefore, not suitable for repetitive applications that involve substantial amounts of average power dissipation.

Peak Pulse Current Test Waveform

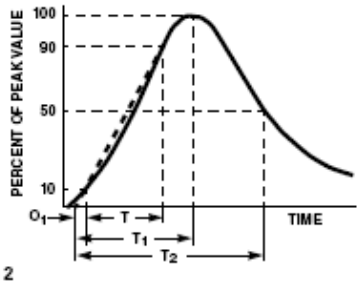


Figure 2

O_1 = Virtual Origin of Wave
T = Time from 10% to 90% of Peak
T_1 = Rise Time = 1.25 x T
T_2 = Decay Time

Example - For an 8/20 μs Current Waveform:
$8\mu s = T_1$ = Rise Time
$20\mu s = T_2$ = Decay Time

Figure 26

Stand by Power Dissipation vs Applied V_{Rms} at Varied Temperatures

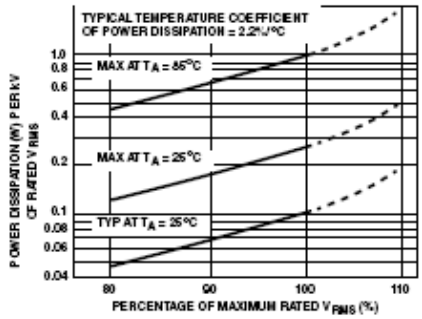


Figure 3

Typical Stability of Standby Power Dissipation at Rated V_{RMS} vs Time

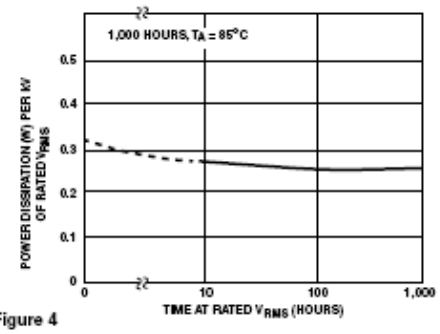


Figure 4

Maximum Clamping Voltage BA Series

V131BA60 - V881BA60

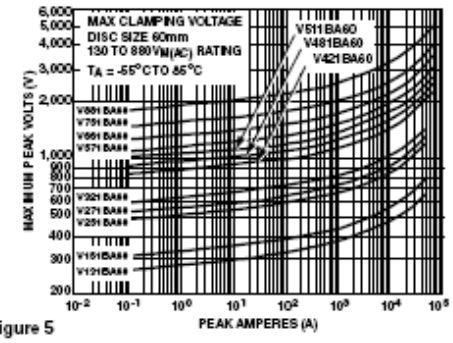


Figure 5

Maximum Clamping Voltage BB Series

V112BB60 - V282BB60

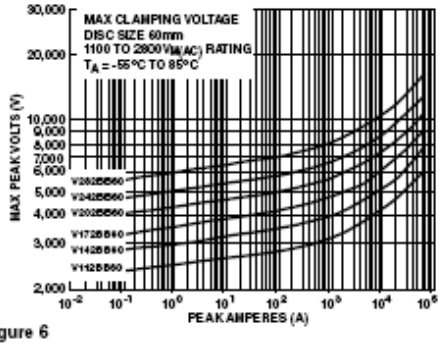


Figure 6

Repetitive Surge Capability BA Series

V131BA60 - V321BA60

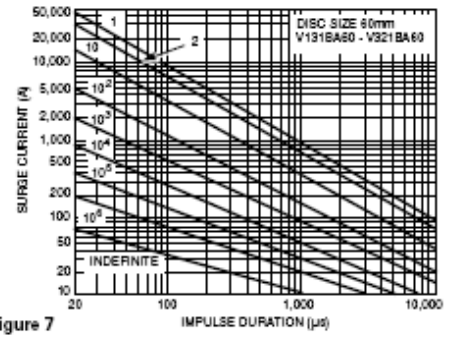


Figure 7

Repetitive Surge Capability BB Series

V421BA60 - V282BB60

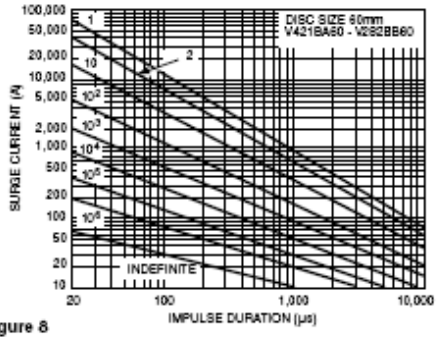


Figure 8

NOTE: If pulse ratings are exceeded, a shift of V_M(DC) (at specified current) of more than +/-10% could result. This type of shift, which normally results in a decrease of V_M(DC), may result in the device not meeting the original published specifications, but it does not prevent the device from continuing to function, and to provide ample protection.

Physical Specifications

Lead Material	BA / BB – Copper with Tin Plating
Insulating Material	Cured, flame retardant epoxy polymer meets UL94V–0 requirements.
Device Labeling	Marked with LF, Part Number and Date code

Environmental Specifications

Operating/Storage Temperature	-55°C to +85°C/ -55°C to +125°C
Humidity Aging	+85°C, 85% RH, 1000 hours +/- 5% typical resistance change
Thermal Shock	+85°C to -40°C 10 times +/- 5% typical resistance change
Solvent Resistance	MIL–STD–202, Method 215F
Moisture Sensitivity	Level 1, J–STD–020C

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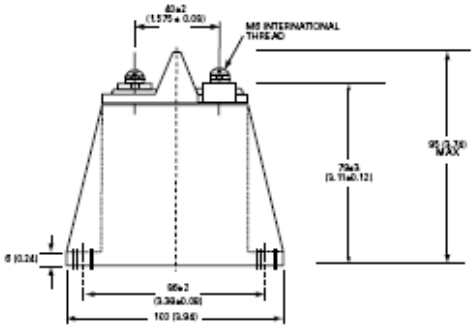
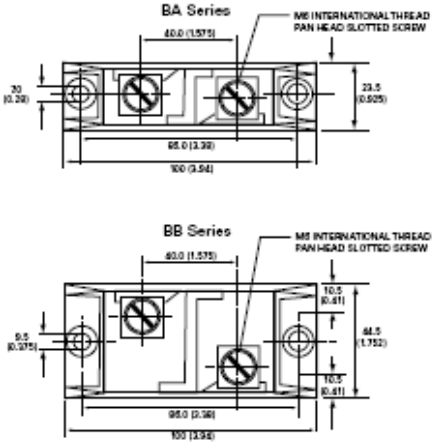
Dimensions





Notes:
Typical weight: BA Series:250g and BB Series: 600g
Dimensions are in mm; inches in parentheses for reference only.

Part Numbering System

V XX X BA 60

- VARISTOR
- $V_{M(AC)}$ — First Two Significant Digits*
- $V_{M(AC)}$ — Decade Multiplier* (1 or 2)
- SERIES DESIGNATOR — BA or BB
- DISC SIZE (60mm)

*Refer to Rating & Specifications table
Examples:
130 $V_{M(AC)}$ = 131
2800 $V_{M(AC)}$ = 282

BA/BB Series

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VITA

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