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Development and validation of a microcontroller emissions model

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Department:

DEVELOPMENT AND VALIDATION OF A MICROCONTROLLER EMISSIONS MODEL

by

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ABSTRACT

A model of the power delivery network of a microcontroller was developed to predict the radiated and conducted emissions from the integrated circuit (IC). A SPICE model of the power delivery network, similar to the ICEM model, was developed for a microcontroller running a typical program and used to predict the noise voltage between the power and return planes of a printed circuit board (PCB). The IC model was generated using the Apache tool suite. A model of the PCB was created using an electromagnetic cavity model and lumped-element models of components on the board. Values of predicted and measured impedance looking into the IC and PCB matched within a few dB up to 1 GHz. The noise voltage between the PCB power and return planes were found using the transfer function between the noise sources in the IC and a measurement port on the PCB. The measured and simulated noise voltages on the PCB matched within several decibels at clock harmonics up to 600 MHz in the frequency domain and were also closely matched in the time domain. Measurement of power pin currents using loops embedded in the PCB show individual pin currents were also predicted well up to 800 MHz.

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to Dr. Daryl G. Beetner for his inspiration, instruction, and encouragement in my graduate research and Dr. James L. Drewniak for his advice, direction and support in a variety of areas. Also, I would like to thank Dr. David J. Pommerenke for his constructive suggestions and help in solving technical problems I encountered and friendship I received. The EMC laboratory provided me with a friendly and convenient research environment and put me on the path to a successful career. I would like to thank all faculty, staff and colleagues in this lab who have helped me and supported me. My special thanks to friends Tun Li, Gang Feng, Francesco De Paulis, Hemant Bishnoi, and Yaojiang Zhang.

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ABSTRACT

A model of the power delivery network of a microcontroller was developed to predict the radiated and conducted emissions from the integrated circuit (IC). A SPICE model of the power delivery network, similar to the ICEM model, was developed for a microcontroller running a typical program and used to predict the noise voltage between the power and return planes of a printed circuit board (PCB). The IC model was generated using the Apache tool suite. A model of the PCB was created using an electromagnetic cavity model and lumped-element models of components on the board. Values of predicted and measured impedance looking into the IC and PCB matched within a few dB up to 1 GHz. The noise voltage between the PCB power and return planes were found using the transfer function between the noise sources in the IC and a measurement port on the PCB. The measured and simulated noise voltages on the PCB matched within about 3 dB at clock harmonics up to 600 MHz in the frequency domain and were also closely matched in the time domain. Measurement of power pin currents using loops embedded in the PCB show individual pin currents were also predicted well up to 800 MHz.

Index Terms **--** Integrated circuits design, modeling; power integrity, electromagnetic compatibility, decoupling, emissions.

I. INTRODUCTION

Electromagnetic noise can be coupled from circuits through radiation or conduction. Although ICs are small and not efficient sources of radiated emissions by themselves below a few GHz, noise from the IC can conducted to other circuits on the PCB or radiated through attached cables to cause EMC problems. In recent years, designers have increasingly focused on reducing EMC problems at the IC level rather than relying entirely on board-level fixes. IC models for power delivery network like ICEM or LECCS [1, 2] have been proposed to better understand the impact of ICs on EMC. Previous research has shown the promise of these models in several scenarios, including prediction of the conducted emissions from ICs [3, 4], of clock jitter [3], of the influence of decoupling capacitors on conducted emissions [3-5], and of substrate noise in mixed-signal designs [6].

Typical models of the power delivery network are composed of two sub-models: a model of the power network with passive elements and a model of the switching activity of the IC. The passive elements may be obtained by using IC development tools that can extract resistive, capacitive and inductive values associated with the IC core and package. The switching currents may be found through tools that predict the time-domain current (or power) consumed by the core [3-7]. Models of the PCB, to date, are typically modeled using lumped elements, where model parameters are found through measurements. Lumped element modeling, however, is only good for low frequencies. At high frequencies, cavity modes and other influences must be taken into account [8,9].

In this paper, models of the IC core, the package, and the printed circuit board are developed separately using different modeling tools, then connected in HSPICE and

processed in MATLAB to predict the noise voltage and current on the power/return planes. Unlike many IC models published in the literature, the model used here includes multiple switching current sources driving a distributed power delivery network through multiple power/return pins, so may describe the pin current more accurately than models using only a single current source. The PCB characterized in a cavity model [8, 9] allows the self and transfer impedance of the board to vary with location and is valid beyond 1 GHz. This modeling approach will lead to better prediction of power integrity issues and better estimation of near-field emissions from the IC, for example to a TEM cell, since the PCB impedance and package currents are better defined.

The following text explains the development of the IC, PCB, and PCB-component (e.g. decoupling capacitor) models in detail. Passive models of impedance are verified through comparison of measurement and simulation of the impedance looking into the IC, PCB, and PCB components, and the transfer impedance between two locations on the PCB. Power plane noise voltage on the PCB is predicted from the models of current sources in the IC using the simulated transfer impedance from the inside of to IC to a location on PCB. Embedded loops built on the PCB were used for the current measurement. Finally, the models of the package and predicted values of pin currents were used to predict the TEM emissions from this IC.

II. IC MODEL

A. Development

The model of the IC activity and impedance was generated using Apache's RedHawk/Sentinal-CPM tool suite. Apache's RedHawk/Sentinel-CPM can generate a

compact HSPICE compatible Chip Power Model (CPM) of a System-On-Chip (SOC). This model is composed of the current demand waveforms along with an effective capacitance and resistance per pin or pin group. These data give an accurate representation of the electrical behavior of the SOC, including precise time-domain and frequency-domain information of the noise source.

RedHawk/Sentinel-CPM simulates the dynamic current behavior of the entire SOC with SPICE-like accuracy, given the layout of a SOC along with the timing of its components and its analog and transistor-based blocks. The current demand of each component is modeled using SPICE to create the Apache Power Library (APL) which is responsive to the power supply variation of each component along with the input transition time and output loading condition. The intrinsic and output loading capacitance of each component, the intentional decoupling capacitance, and the parasitic capacitance of the power/ground network are all accounted for in the model. On-chip inductance can also be considered in the simulation, though was not included in this study. Apache's power/ground network extraction engine includes inter-power-domain coupling to simulate power noise propagation through direct connection or through field coupling. Although a vector-based stimulus such as VCD is preferred, a realistic simulation can be achieved with behavioral specification such as full-chip/block/instance toggle rate and power consumption. Once the simulation is complete, the current signature waveforms can be captured at each pin or pin group.

In order to capture the effective resistance or capacitance per pin or pin group, RedHawk/Sentinel-CPM performs an AC analysis and synthesizes the impedance frequency response using SPICE passive and current-source elements with an error

tolerance of less than 0.2 % compared to the original frequency response. Effectively, it reduces a network of millions of electrical nodes into a compact network of hundreds or thousands. Finally, RedHawk/Sentinel-CPM packages this synthesized network along with the current signature per pin or pin groups into a compact HSPICE compatible CPM.

The final IC model generated by Redhawk/Sentinel-CPM included 9 power and return pin pairs, 8 input and output pin pairs, 34 noise current sources, and many elements to represent internal power bus impedance. In the IC we studied, the noise currents from VCCIO and VSSIO are relatively small compared to those from VCC and VSS, so only noise currents on the power/return bus were considered. The total length of the noise sources is 1 micro-second; it has frequency resolution of 1 MHz.

The IC package model was generated using Optimal Corporation's PakSi-E 3D finite element modeling tool. The tool generates a SPICE model of the resistance, self inductance, and self-capacitance of the lead-frame and bonding wires over a return plane as well as the mutual inductance and capacitance between pins. While a model was developed for the entire package, only the elements associated with the 9 power/return pin pairs were used for the following simulations. Once developed, the package model was incorporate along with the model of the IC core and the two were treated together for the remainder of the analysis.

B. Validation

Models of the IC power delivery network and package were validated by measuring and simulating the impedance looking into individual power pin pairs. Impedance was measured using a network analyzer and a microprobing station as shown

in Fig. 1. Two VSS and VSSIO pins were soldered together to reduce the connection impedance between the two power domains, as would occur on the PCB, and to allow easier bias of each domain. The reset pin was set low by connecting it to a VSS pin in order to minimize chip activity while the IC was biased and to minimize the corresponding influence of that activity on the impedance measurement. Since values of decoupling capacitance will vary with voltage and proper bias of P-N junctions is required for accurate measurements, VCC and VSS pins were biased with 1.5 V DC and VCCIO and VSSIO were biased with 3.3 V DC. The impedance looking into a power/return pin pair was found by placing the signal and return pins of the probe station across the pins and measuring S11 with the network analyzer.

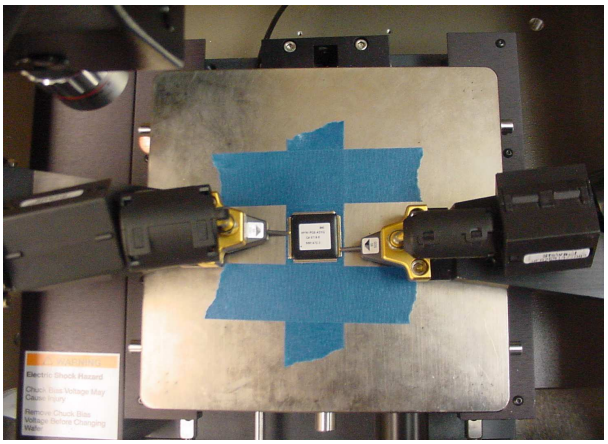

Figure 1. Measurement of the impedance of the IC.

Measured and simulated values of the impedance looking into the IC were compared for all power/return pin pairs. One example is shown in Fig. 2. Simulated values were found using HSPICE. The chip is capacitive below 10 MHz, is primarily inductive above 10 MHz, and is resistive at the resonant point. The simulation and

measurement match well beyond approximately 1 GHz. There is some discrepancy in measured and simulated values at a few 10s of MHz. This problem is likely due to parasitic currents in the biased IC that are not included in the passive model. Reducing the input power of the network analyzer reduces the difference between the measured and simulated curves at low frequencies, which supports this hypothesis. While there is some difference in the measured and simulated values of impedance, as seen around 10 MHz, this difference is not expected to significantly influence prediction of the PCB noise voltage as most energy from the IC is well above this frequency. Measured and simulated values of IC capacitance and package inductance between 1 MHz and 1 GHz match well. Above 1 GHz, the package capacitance becomes important and causes a resonance at a few GHz. The discrepancies in the model resistance at 10 MHz and the resonance at a few GHz are apparently due to problems with the package model and differences between the model and the measurement setup. For this project, we are only interested in noise below 1 GHz, so the high-frequency resonance at a few GHz is not important and we expect the model to work well below 1 GHz. The comparison of measured and simulated impedance at other pin pairs yielded similar results.

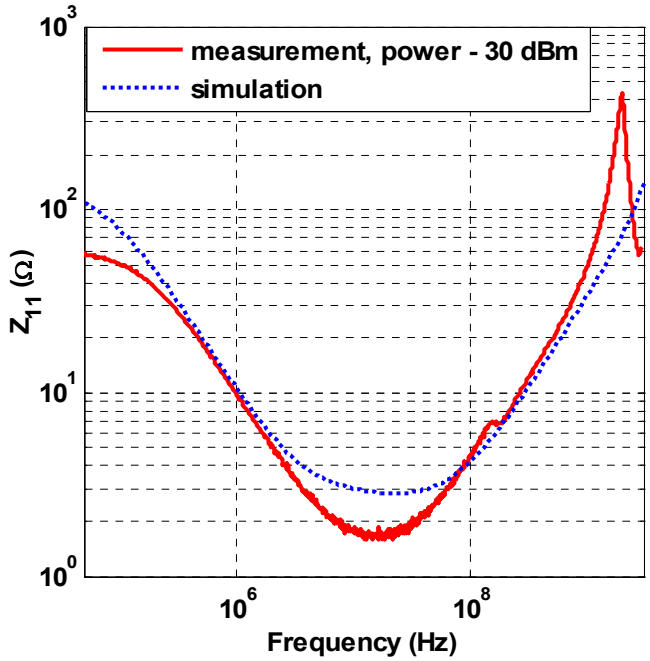

Figure 2. Measured and simulated values of impedance looking into the IC.

III. PCB MODEL

The PCB model includes a model of the power and return planes and of the "other" components attached to the power return planes, like the decoupling capacitors. The self- and transfer-impedance of the power and return planes was found using a cavity model to allow impedance to vary with location and to allow more accurate prediction at frequencies beyond where board resonance becomes important. The IC, decoupling capacitors, and other components connected to the power planes were connected together in simulation through this power plane model.

A. Power Planes

A model of the power plane impedance was found using a program called EZPP (Easy Power Plane) developed at the Missouri University of Science and Technology

(formerly named the University of Missouri – Rolla). The program uses a cavity model [8, 9] solver to find the transfer parameters of a bare PCB. One can add decoupling capacitors at any location on the PCB and simulate to see their effect on Z and S parameters. The software also produces an equivalent SPICE model for the PCB impedance between specific port (i.e. connection) locations.

The test board is shown in Fig. 3. It is 3.88 inch on each side, 28 mils in thickness, and has a dielectric constant of 4.7. Simulated and measured values of the impedance looking into this board at port 1 are found in Fig. 4. Impedance was measured using a network analyzer. The two curves match well below 1 GHz. The peak difference occurs between 600 MHz and 1 GHz and is less than 5 dB. This difference is primarily due to losses in the board that were not part of the model.

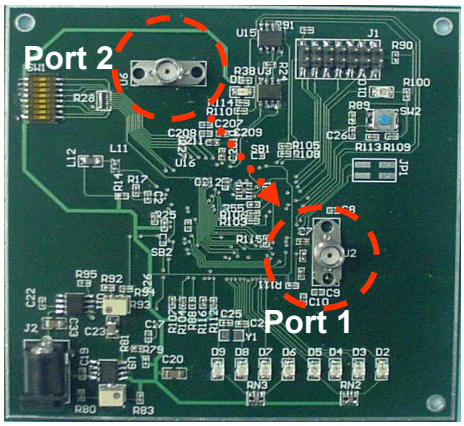

Figure 3. The test board.

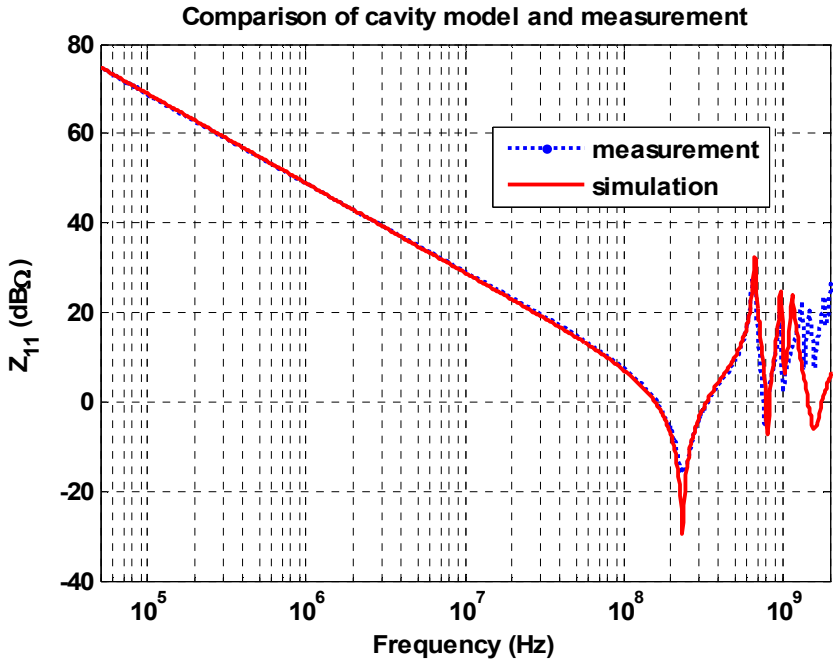

Figure 4. Comparison of cavity model impedance simulation and measurement for the bare PCB.

B. Decoupling Capacitors

On the test board, seven X7R ceramic decoupling capacitors, one 10 µF decoupling capacitor, and six 33 nF decoupling capacitors are directly connected to the power and return planes of the PCB. The decoupling capacitors were characterized using a series RLC model to match the manufacturer data as shown in Fig. 5. Differences in the measured and simulated values of S parameters for these capacitors matched within less than a dB up to several GHz. Additional inductance was added in the PCB model to account for the connection to the power and return planes through the vias.

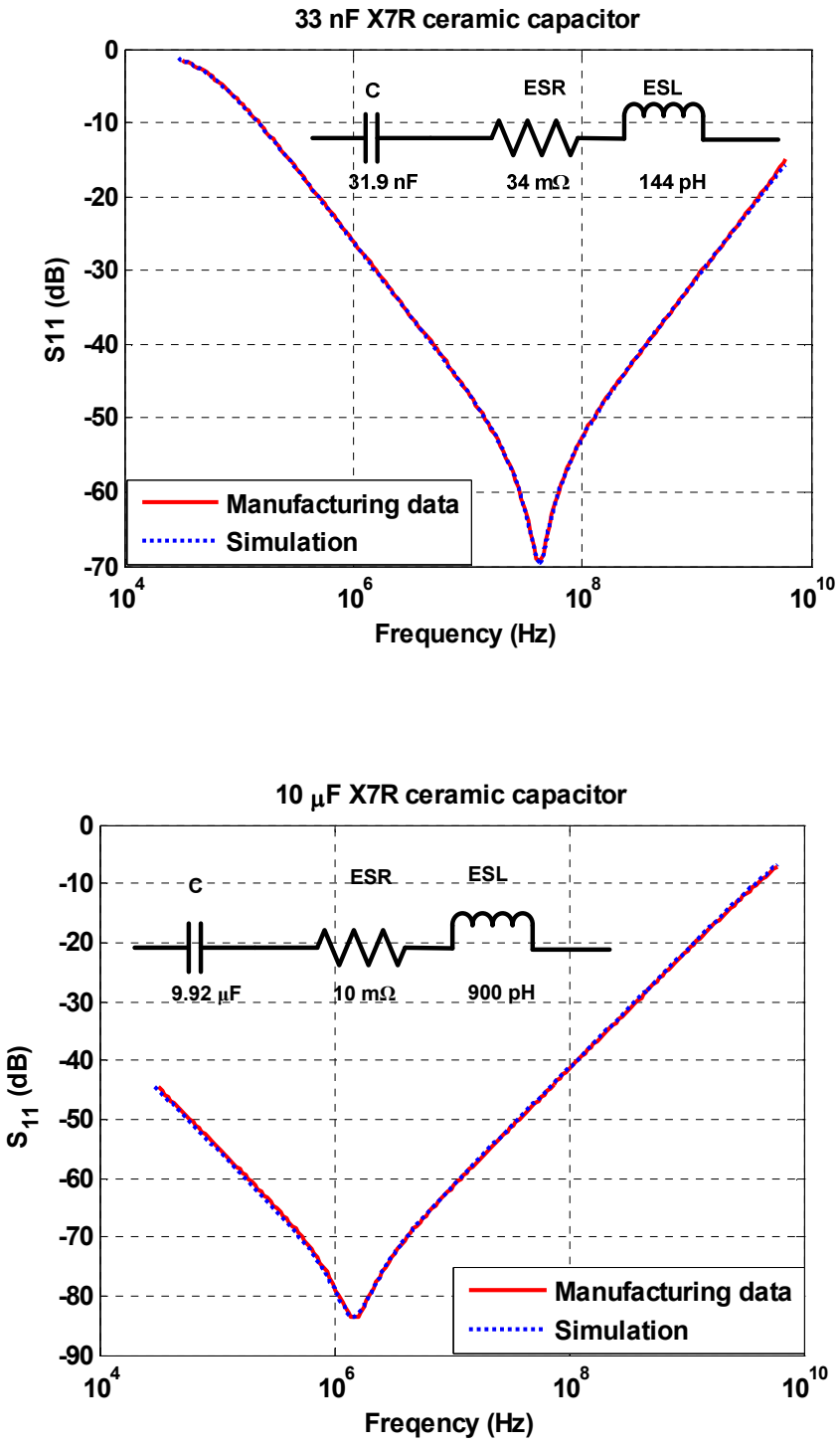

Figure 5. Decoupling capacitor models.

C. Overall PCB Model Validation

EZPP was used to produce a SPICE model of the PCB with 11 ports shown in Fig. 6. Nine of these ports were for the microcontroller's 9 pairs of VCC and VSS pins and two ports were for the SMA connectors connected to the power and return planes on the PCB. Decoupling capacitors were incorporated into the PCB SPICE model during the model generation stage.

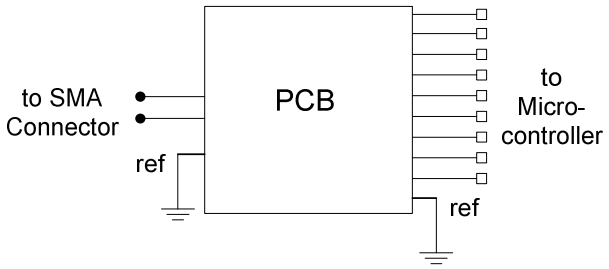

Figure 6. Block model of PCB power/return planes.

The model of the board with all connected components (including decoupling capacitors, voltage regulators, communications ICs, etc) was validated by simulating and measuring the impedance looking into the board at the port locations as well as the transfer impedance between port 1 and port 2 on the PCB (which are shown in Fig. 3). Some discrepancy between the simulated and measured values occurred around 400 MHz, where there was a resonance between the approximately 540 pF of capacitance between the power and return planes and the approximately 400 pH of connection inductance to the decoupling capacitors. This difference of approximately 10 dB at the resonant point is most likely caused by parasitic inductance/capacitance/resistance in the communications ICs on the board that were not modeled, as the PCB model matches well when all other components but these are added to the board. Accounting for these

components using a simple RLC model with an L around 2 nH, C between 10 pF and 80 pF, and R between 200 mΩ and 1000 mΩ resulted in the transfer impedance curve shown in Fig. 7.

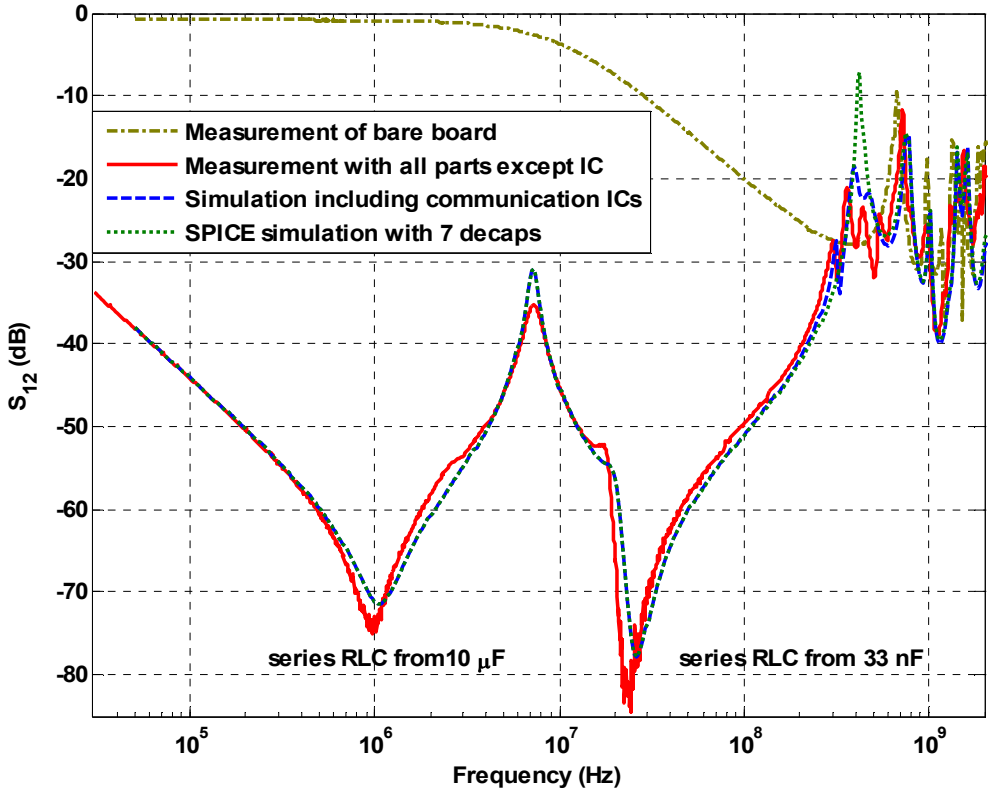

Figure 7. Measured and simulated values of S12 between SMA ports 1 and 2 on the PCB.

The first resonance in the transfer impedance at 1 MHz is mainly due to the 10 μF bulk decoupling capacitor. The second resonance at 7 MHz is due to the six 33 nF local decoupling capacitor resonating with the connection inductance to the bulk decoupling capacitor. The third resonance at 20 MHz is the local decoupling capacitors resonating with their connection inductance. Beyond 600 MHz the resonant modes of the boards

begin to dominate. The final simulated transfer impedance matches the measurement within 6 dB or less up to about 2 GHz.

IV. POWER BUS NOISE

A. Coupled Noise Voltage on PCB

The noise voltage between the PCB power and return planes was calculated from the transfer impedance from the noise sources to the observation point using the models of the IC, package, and PCB shown earlier. The noise voltage in the time- and frequency-domain was predicted using the following equations

$$V_1(j\omega) = \underbrace{Z_{12}(j\omega) I_2(j\omega) + \ldots + Z_{1,19}(j\omega) I_{19}(j\omega)}_{\text{18 current sources inside IC}} \qquad (1)$$

$$V_1(t) = ifft\left(V_1(j\omega)\right) \qquad (2)$$

where Z_{12} to $Z_{1,19}$ are the transfer impedance from the internal noise source to the SMA connector on the PCB, I_2 to I_{19} are noise sources between 18 power/return pin and the reference ground inside IC, and *ifft* is inverse Fourier Transform. The noise currents were originally given in the time-domain by Apache, so were converted to the frequency domain using the Fast Fourier Transform. The transfer impedance were either found through calculation or by cascading S parameter blocks in SPICE as shown in Figure 8. The transfer impedance can be calculated manually as

$$Z_{1\times 18} = Z_{oi}^{PCB}\left(Z_{ii}^{PCB} + Z_{oo}^{IC}\right)^{-1} Z_{oi}^{IC} \qquad (3)$$

where Z_{oi}^{PCB} is transfer impedance of the PCB from nine power ports to one connector, Z_{ii}^{PCB} and Z_{oo}^{IC} are self impedance of PCB and IC on the connector and nine power ports

respectively, and Z_{oi}^{IC} is the transfer impedance of the IC from 18 noise sources to nine power ports.

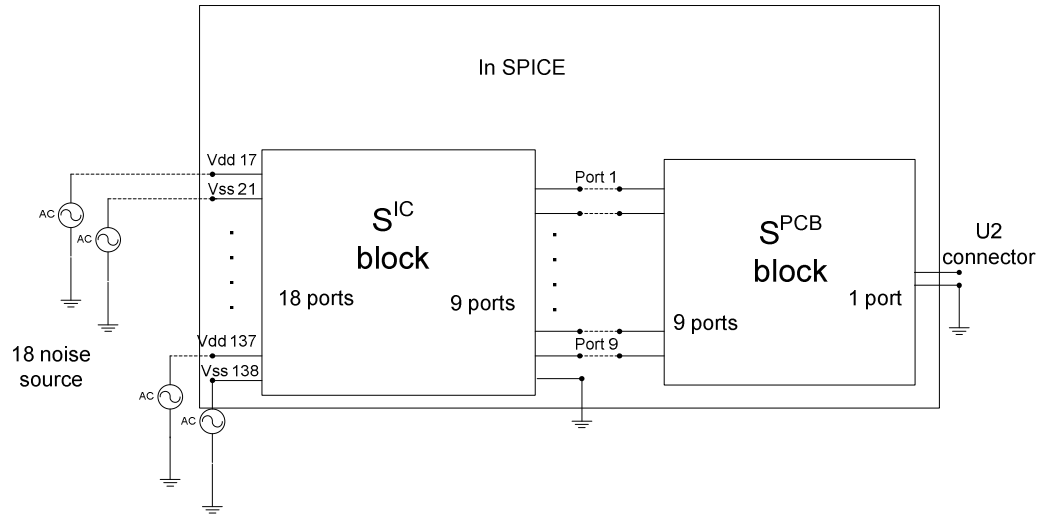

Figure 8. S-parameter blocks of IC and PCB connected in SPICE

Fig. 9 shows the measured and simulated noise voltage in the frequency-domain at one SMA connector (port one in Figure 3). The simulation generally did a good job of predicting the noise voltage at harmonics of the clock up to 600 MHz (72 MHz, 144 MHz, and 288 MHz, etc.), finding the correct value within several decibels. The simulated noise in the time-domain was found using an inverse FFT. Fig. 10 shows a comparison of the simulated and measured noise in the time domain. Measurements were performed using an oscilloscope. Both simulated and measured data were filtered using a high-pass filter with a 20-MHz corner frequency. The simulation and the measurement generally matched well, though the simulation under-estimated the magnitude of the negative (-2 mV) spike. The difference is most likely due to problems with estimating high-frequency noise. Other researchers have found similar problem in predicting high-frequency noise [3, 5, 7].

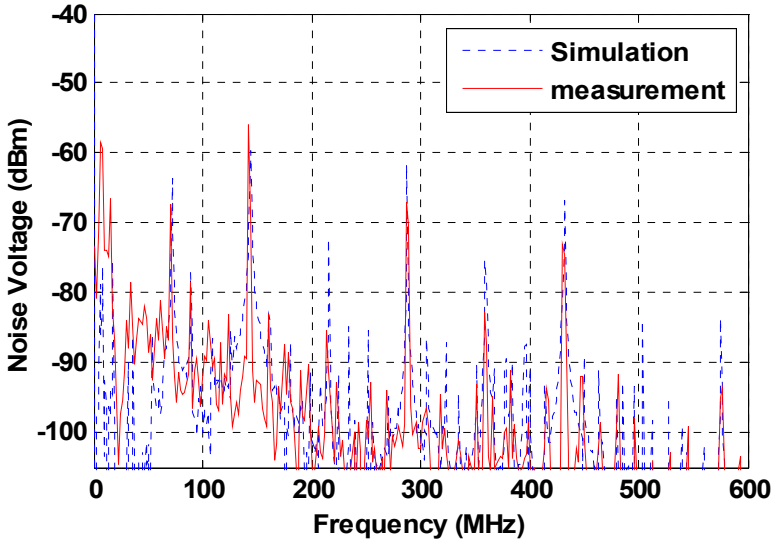

Figure 9. Simulated and measured power bus voltage noise spectrum.

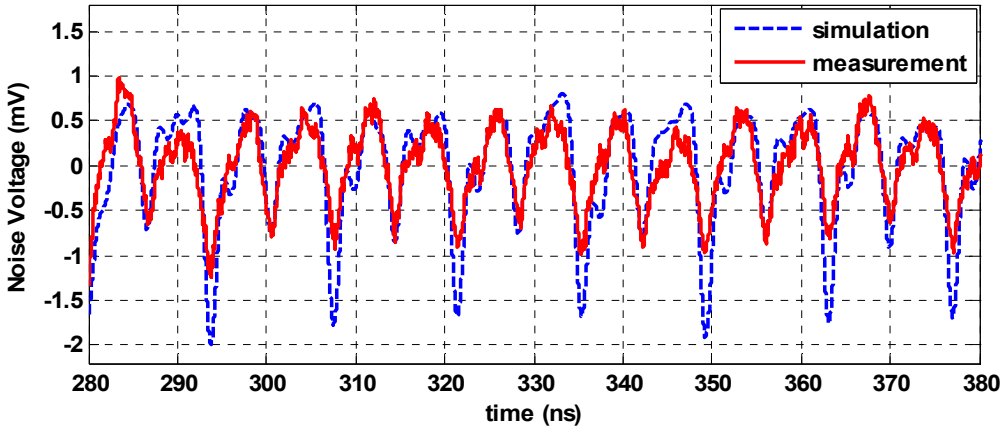

Figure 10. Simulated and measured power bus voltage noise in time-domain.

B. Pin currents

Seven loops were embedded into the PCB to measure noise currents as shown in Figure 11 [10]. The loops were made using traces and vias on the first and third layer of the PCB and were placed under a trace connected between the power or return pins and the power/return places of the PCB. Vias were placed on all sides of the loop to minimize

interference from other currents on the board. The measurement loop was completed by soldering a small-diameter coaxial cable to the board, with the center conductor connected to the via and the shield connected to the bottom trace.

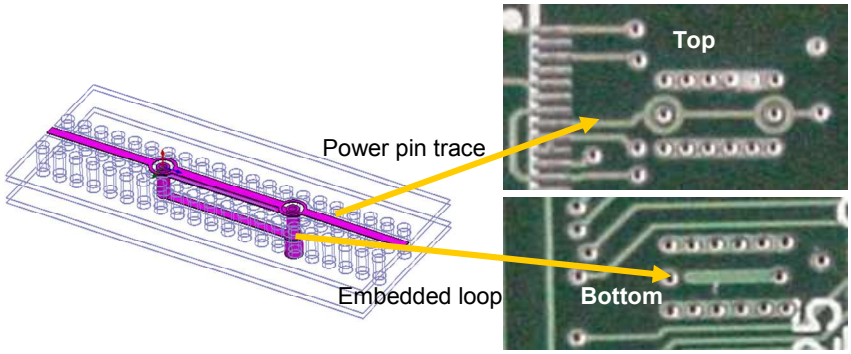

Figure 11. Embedded loop used to measure current.

The equivalent circuit of the embedded loop is shown in Figure 11. The embedded loop is inductively coupled to noise currents on the power trace. The coupled voltage is proportional to frequency over the working range of the loop as shown in Figure 12. The mutual inductance between the loop and trace can be derived from the measurement of S_{21}, when the trace is terminated with a resistance as shown in Figure 11, as

$$Z_{21} = 50 \cdot \frac{2S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} \approx 50 \cdot \frac{S_{21}}{2} = j\omega M \qquad (4)$$

where S_{11}, S_{12}, S_{21}, S_{22} are S parameters measured by network analyzer. For the loops on this board, the mutual inductance was calculated to be 0.55 nH.

The loop has a usable frequency range from 100 KHz to 1 GHz. Below 100 KHz, the coupled voltage was below the noise floor of the measurement setup. Above 1 GHz, the loop impedance is comparable to the system impedance and the frequency response

begins to degrade.

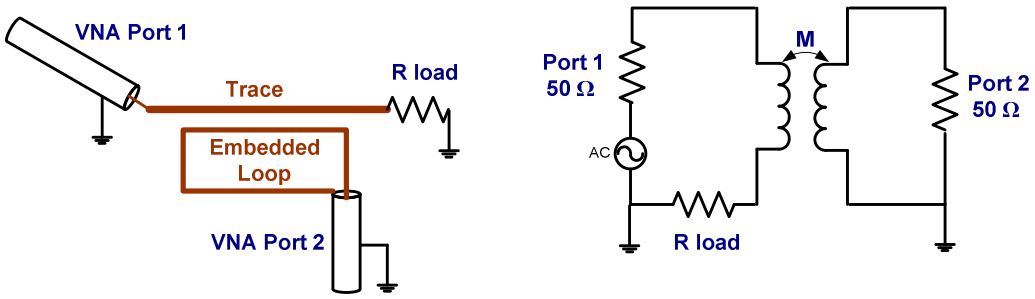

Figure 12. Equivalent circuit of the embedded loop.

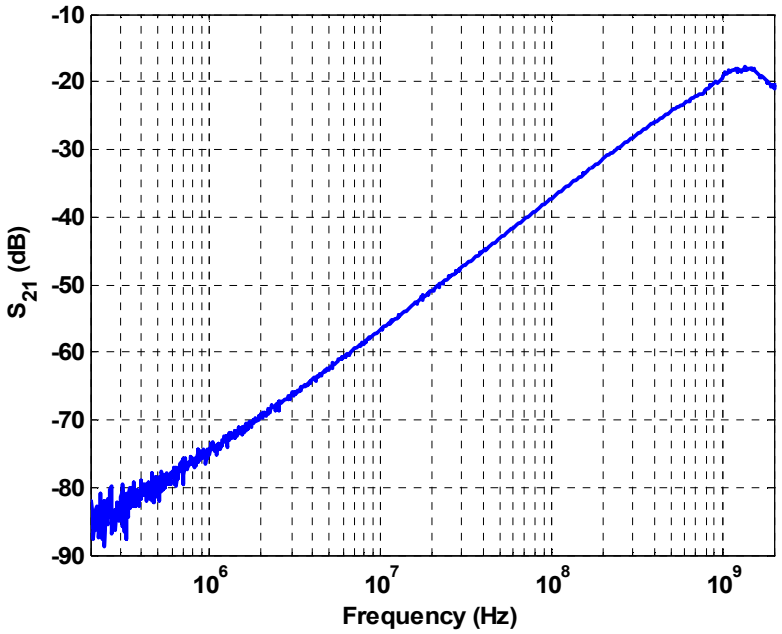

Figure 13. Calibration of the embedded loop.

In order to find the current on power traces in simulations, small resistors (5 mΩ) were inserted between the IC power pins and the PCB power traces in the HSPICE circuit. The comparison between the measured and simulated noise current is shown in Figure 13. The simulation and measurement match well. Similar results were observed on other pins.

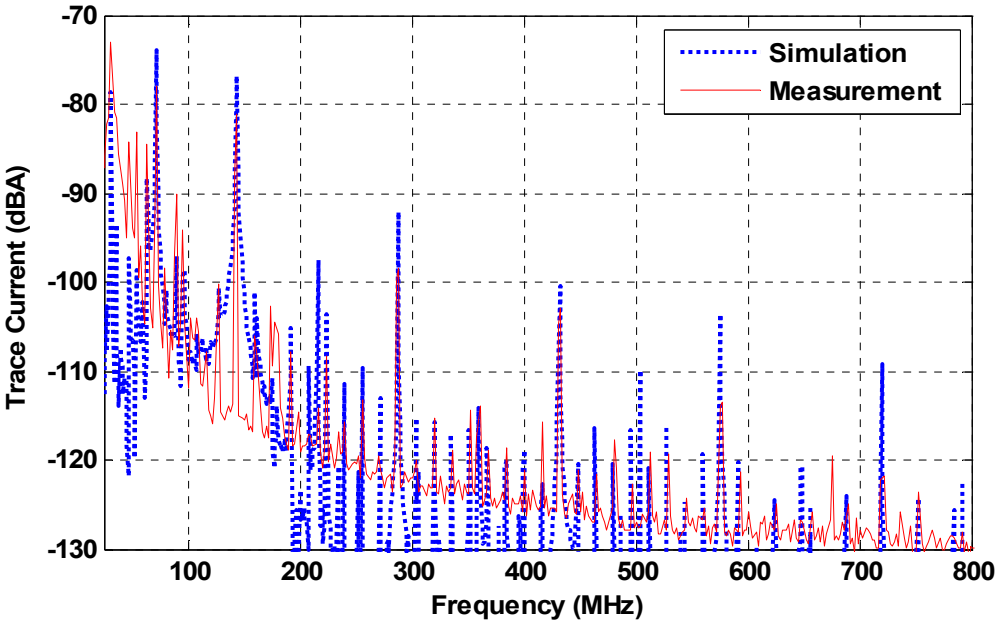

Figure 14. Simulated and measured noise current on the power pin trace.

V. DISCUSSION

The complexity of the IC and PCB model used here posed a significant challenge to simulation and validation. Other studies have typically used simple or measured models of the PCB and have only used a single noise source delivering current to a single pair of power and return pins for the core. Our PCB model was based on a complex cavity model of the power and return planes and our IC model used 34 independent noise sources and 9 power and return pin pairs. The complexity of this model describes the IC and current behavior with more accuracy, but also made it difficult to determine the true cause of simulation errors. Particular difficulties were found when performing simulations in the time-domain. SPICE simulations in the time domain were time consuming and highly susceptible to errors. To avoid these issues, modeling was performed instead in the frequency domain. Modeling of transfer-impedances in the

frequency domain was straightforward and fast. Models of the IC, package, and PCB could be simulated together or separately and could use either lumped SPICE elements or frequency-domain (e.g. S-parameter) specifications for impedance. The time- or frequency-domain noise voltage could then be found easily using a tool like MATLAB.

Modeling of the IC and PCB above 1 GHz is challenging. One difficulty encountered in this study was characterizing the many components attached to the PCB when estimating power bus noise. While the main contributors to the power-bus impedance are the power and return planes and the decoupling capacitors, other components may contribute significantly to the impedance as well, particularly at high frequencies. In this study, these components changed the transfer impedance at resonance by about 10 dB (figure 7). Extra capacitance and resistance had to be added to the PCB model to account for these additional components.

VI. CONCLUSIONS

Models of the IC power delivery network, internal switching currents, the IC package, and the PCB power bus were developed and used to predict noise voltage between the PCB power and return planes and the current through IC power and return pins. Passive impedance models matched measurements well up to 1 GHz. The complete model was able to produce good estimates of the power bus noise voltage in the time domain and at clock harmonics up to 800 MHz in frequency domain and was able to produce good estimates of power-pin currents. Even better results are expected as our ability to accurately model switching currents improves. These models can help IC designers build better ICs as they allow prediction of emissions without manufacturing

the IC and can help PCB designers build better PCBs that anticipate the impact of ICs on emissions and power integrity.

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APPENDIX

TEM CELL PREDICTION

A TEM cell can be used to predict the potential for the board to couple electrically or magnetically to nearby structures. TEM cell emissions are measured by putting the test board in the window of the TEM cell with the chip facing the septum. The magnetic coupling from the test board can be obtained by the setup shown in figure A.1. The magnetic coupling is measured at the port where the voltage at the two ports are subtracted, labeled "A-B". Only a current loop in the same plane of the shown plane can couple magnetically to the TEM cell. The illustration of the configuration and equivalent circuit are shown in figure A. 2(a) and (b).

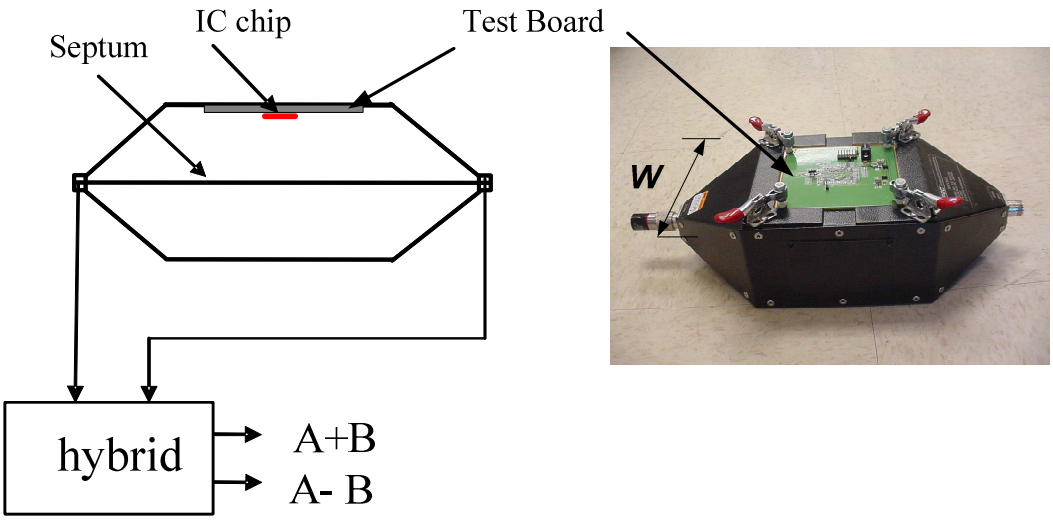

Figure A.1 TEM cell measurement for magnetic coupling

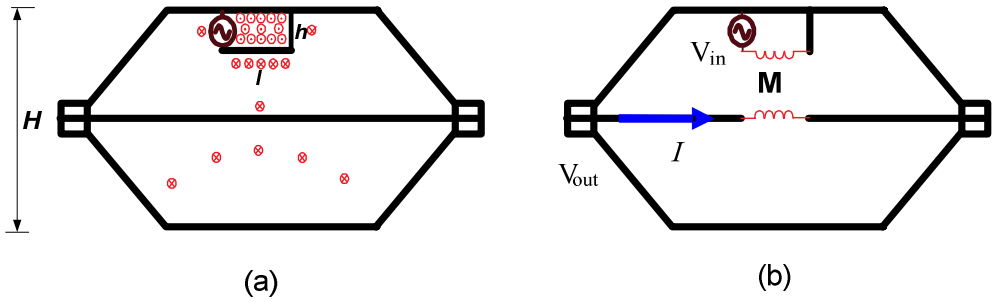

Figure A.2 (a) Illustration of the magnetic coupling
(b) Equivalent circuit for magnetic coupling in the TEM cell

The current loops on the IC and test board that will contribute to magnetic coupling are shown in figure A.3. Suppose the currents on *Vdd* and *Vss* are differential – they may not in fact be differential, but this assumption is implicit in our simulation when we define ports between *Vdd* and *Vss*. In this case, the magnetic fields created by currents on a *Vdd* pin will be largely cancelled by currents on a neighboring *Vss* pin and the IC lead-frame will have few opportunities to cause coupling to the TEM cell. The leads that may cause magnetic coupling to TEM cell are shown in figure A. 3 (when the TEM cell ports are to the left and right of the picture). They are mainly from microstrip line of the power trace on the left and right sides of the IC and the relatively small loop created between *Vdd/Vss* pins at the top and bottom sides of the IC.

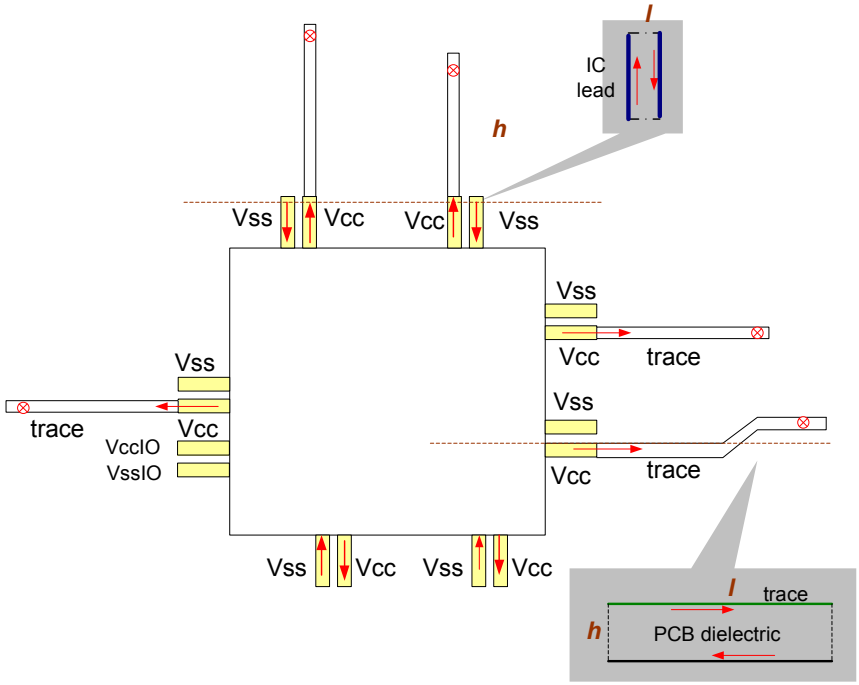

Figure A. 3 Loops that may magnetically couple to the TEM cell

The total voltage coupled to the TEM cell magnetically is the vector summation of the coupling from each loop. The mutual inductance between the TEM cell and a current loop can be approximated by

$$M = \frac{\Phi_{21}}{I} = \frac{\mu_0 \cdot l \cdot h}{2 \cdot (W + H)} \qquad \text{(A1)}$$

where *W, H, l* and *h* are shown in figure A.1 and A.2. More details of the formula can be found in Shaowei Deng's dissertation[1]. Using this mutual inductance and the current on each pin, one can simulate the coupled voltage to the TEM cell, based on the simulated pin currents. Such a simulation is shown in figure A.4. Unfortunately the results from the measurement and simulation have 20 dB differences in the coupled voltage

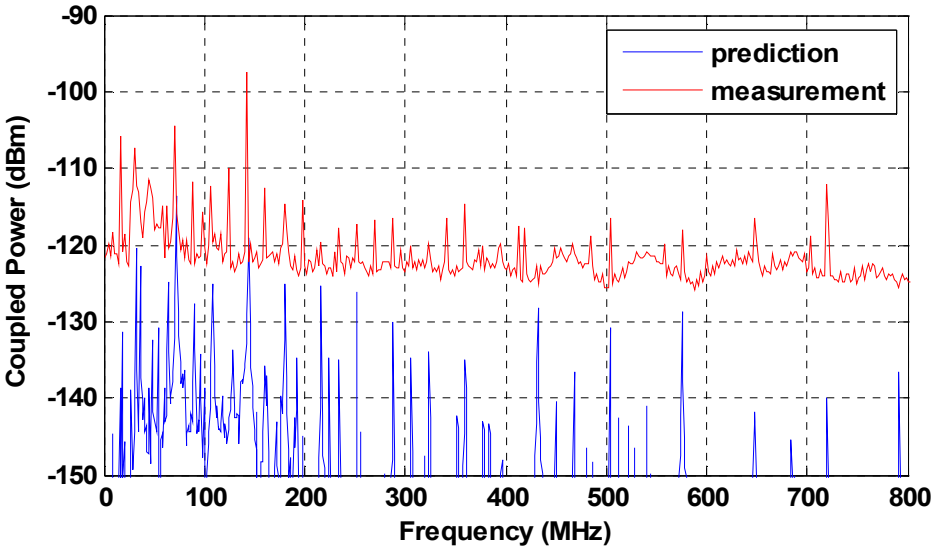

Figure A. 4 Comparison of the simulated and measured magnetic coupling to the TEM cell.

There are several possibilities for this poor results and suggestions for improving it:

1. The assumption of complete differential current on *Vdd* and *Vss* pins may be the main reason for a low simulation result. If currents on the *Vdd* and *Vss* pins are different, the magnetic coupling from the *Vdd* and *Vss* leadframe and bonding wire loops to the TEM cell couldn't be cancelled. One suggestion for this is to define two ports between *Vdd/Vss* and the reference instead of a single port between *Vdd* and *Vss*. The package model needs to be carefully studied to find the appropriate reference for both the IC and PCB. The relative current in

[1] S. Deng, "Innovative Applications of TEM Cell Measurements in Predicting Radiated Emissions due to Common-Mode Current on Printed Circuit Boards," PhD Thesis, University of Missouri – Rolla, 2007.

Vdd and *Vss* pins could be found by performing a near-field scan of the IC package or by hand-probing the pins of the IC to approximate the relative magnitudes of the pin currents. This approach would not tell you the exact size of the currents, but would tell you if they were significantly different.

2. It is possible there was an error calculating the mutual inductance. The mutual inductance between the TEM cell and the IC/board needs to be verified. One possibility is that the height of the bonding wires above the return plan can be different between the *Vdd* and *Vss* pins, causing a change in the associated mutual inductance – and an inability of equal *Vdd/Vss* currents to cancel inductive coupling to the TEM cell. Mutual inductance could be verified by a simple check of the equations or, more carefully, through S-parameter measurements of the coupling from the board to the TEM cell using a network analyzer. Board setup would have to be considered carefully in this case.
3. It is possible there are currents on VddIO and VssIO that need to be considered in the coupling. Other studies have shown that the currents in VddIO and VssIO are not negligible. The amount of current in VddIO and VssIO could be verified using a near-field scan of the IC or by hand probing the VddIO/VssIO pins to get a feel for the magnitude of the currents relative to the current through Vdd/Vss pins. Simulation of the VddIO/VssIO currents would require more ports connected between the IC and PCB for these pins.

VITA

Shaohua Li was born in Jiangsu, China in 1972. She received the B.S. degree in physics from Nanjing Normal University, Nanjing, China, in 1993, the M.S. degree in radio engineering from Nanjing University of Posts and Telecommunications, Nanjing, China, in 1996, and Ph.D. Degree in electrical engineering from the University of Alabama, Tuscaloosa, in May 2005. She was named Outstanding Graduate Student by the University of Alabama in 2005. Between 1996 and 1999 she worked as an Engineer with Nanjing Telecom. In 2006, she enrolled in Computer Engineering program for research on signal integrity and IC electromagnetic compatibility.

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