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COMPARATIVE STUDY OF THREE TYPES OF INVERTERS BASED ON THE OUTPUT TOTAL HARMONIC DISTORTION

by

PATERRSON THOMAS

A THESIS

Presented to the Faculty of the Graduate School of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

2015

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ABSTRACT

In this thesis, three cases of power electronic inverters are taken into consideration to analyze their performance in terms of total harmonic distortion in their output voltage and output current. Firstly, a single H-bridge inverter is simulated. Staircase switching technique is used to generate the gating pulses for the switches. Only one switch is made to toggle for every half cycle. The fundamental harmonic component of the desired output voltage is considered to be 120 V. Secondly, the same topology is used with a Bipolar PWM gating technique. The switching frequency of the carrier wave is 33*60 Hz. Thirdly, a multilevel H-bridge inverter is designed by connecting two H-bridge cells in series - one H-bridge cell with a DC source (main H-bridge inverter) and other with a capacitor (auxiliary inverter). The capacitor voltage regulation method is also proposed to control the voltage of the capacitor. Finally, FFT analysis is performed to understand the total harmonic distortion of output current and output voltage of all the three cases. A comparison study is made between all the three inverters' total harmonic distortion of their output current by keeping the load inductor value as constant and vice versa. Cost, size, no. of components used and design level factors are also taken into consideration to compare the inverters.

ACKNOWLEDGEMENTS

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1. INTRODUCTION

Recent developments in the field of power electronics have paved a way to use inverters in an efficient way. There are many different kinds of inverters, which are being used in various fields. Among them, the cascaded H-bridge structured inverter, diode clamped inverter and flying capacitor inverter are the most common types of multi-level inverters. In this thesis, H-bridge structured inverter is taken into consideration to analyze Total Harmonic Distortion (THD) in various circumstances.

Inverters are widely used in different fields like Uninterruptible Power Supplies (UPS), power grid, renewable energy resources, controlling speed of the electric motor, induction heating and many other fields related to power.

1.1 EFFECTS OF THD

Calculation of the Total Harmonic Distortion is important in the field of power in order to maintain the desired operation. Undesired harmonics cause eddy current losses in transformers, which create a serious problem in the operating temperature of the transformer. They also affect the capacitors by heating the dielectric medium [30].

Due to increase in harmonics in the current, the conductor will be overheated owing to skin effect. They also cause failure of circuit breaker, fuses and generator. Meters used in the utility purpose will show improper measurements due to harmonics present in the supply [28]. Harmonics multiplies the losses in the core of the motor resulting in the temperature increase of the motor windings. Undesired harmonics do not cause immediate

problems in the equipment. However, they slowly overheat the equipment and reduce the overall life span of them.

1.2 THREE CASES OF INVERTERS

In this thesis, three cases of inverters are simulated and analyzed to reduce the Total Harmonic Distortion in the output current. They are:

(i) Single H-bridge Inverter

(ii) Bipolar Pulse Width Modulation (BPWM) Inverter

(iii) Hybrid Multilevel H-Bridge Inverter

1.2.1 Case (i). For the first case, single phase H-Bridge inverter with four switches was considered. Staircase switching pattern is used in this case [3]. The gating pulses for the switches of the inverter are generated based upon the desired output of the single H-bridge inverter. Only one switch is made to toggle for every half cycle. RL load is connected across the output of the inverter.

1.2.2 Case (ii). The topology of the inverter is going to be same as the previous case (with the single phase H-bridge inverter being used in this case also). There is a difference in generating the gating pulse for the inverter in this case. Bipolar Pulse Width Modulation technique is used to control the switches. The triangular waveform is compared with the sinusoidal waveform to create the gating pulses.

1.2.3 Case (iii). In this case, two single H-bridge inverters are connected in series to form a multilevel inverter. Generally, if two H-bridge inverters are used, there will be two independent isolated dc voltage sources [29]. This will increase the cost of the inverter.

This drawback can be resolved by replacing one of the independent dc sources by the capacitor [1,2,4,5]. By this way, the cost of the inverter can be reduced.

If the individual dc source is replaced by the capacitor, the voltage across the capacitor has to be controlled. There are many methods to control the voltage across the capacitor. One of the capacitor voltage regulation methods is discussed in this thesis in section 4.4.

2. SINGLE H-BRIDGE INVERTER

2.1 INVERTER TOPOLOGY

A single H-Bridge inverter consists of four switches with the DC source. A three level AC output is obtained from the single H-Bridge inverter. Figure 2.1 shows the topology of the single H-Bridge inverter. The value of the DC source of the single H-Bridge inverter is assumed to be 2E. The reason for this assumption will be discussed in the chapter 4. The RL load is connected to the output of this inverter.

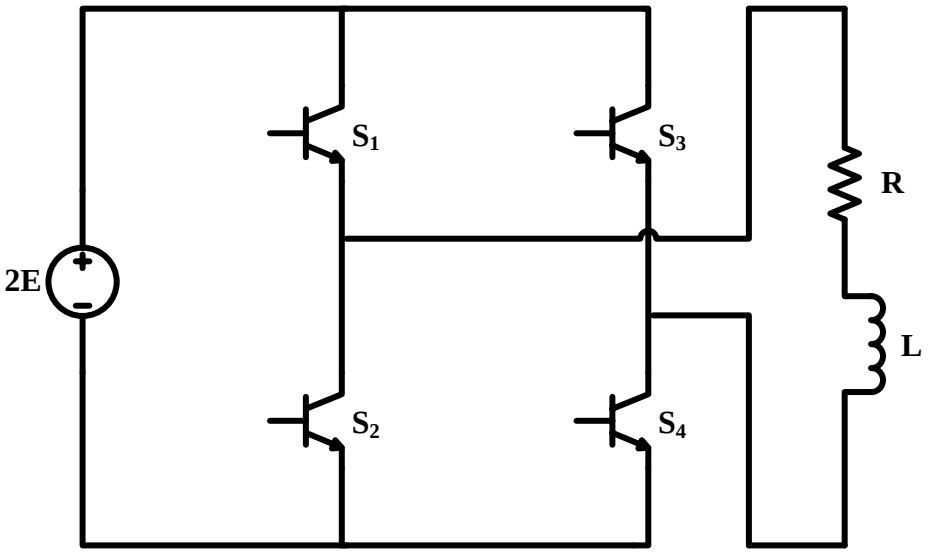

Figure 2.1 Topology of Single H-Bridge Inverter

2.2 GATING TECHNIQUES

The gating signal of this inverter is designed based upon the desired output of this inverter. The firing angle of the inverter [18] is determined by

$$\alpha = \cos^{-1}(\pi V_m/8E) \quad (1)$$

The respective switches are triggered based upon their contribution in generating the desired output. The involvement of the switches in developing the output can be understood from the Figure 2.2.

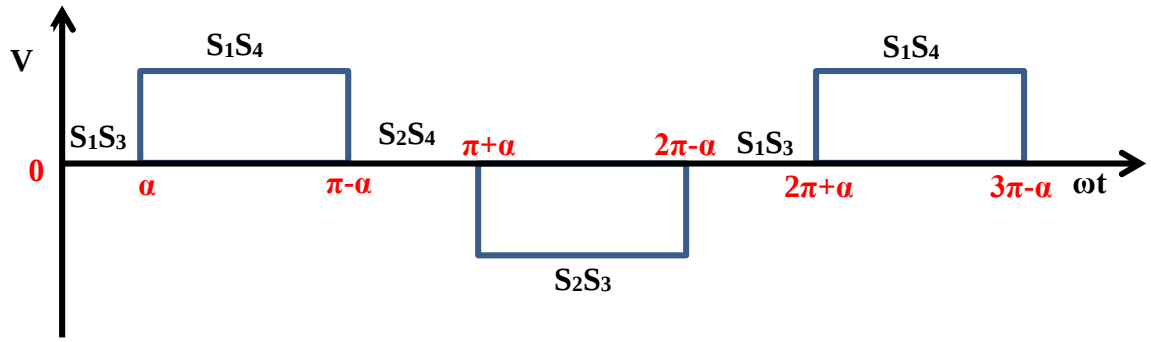

Figure 2.2 Desired output waveform of single H-Bridge inverter

The switch S_1 should be ON in the interval of 0 to π-α and also from 2π-α to 2π. In the interval of 0 to α and from π+α to 2π-α switch S_3 must be ON. Similarly switches S_2 and S_4 should be triggered at the intervals of π-α to 2π-α and from α to π+α respectively. These intervals are repeated in the same order after 2π. From the Figure 2.2, it is clear that

switches S_1 and S_4 are responsible for the positive cycle of the inverter output voltage. Similarly, negative half cycle of the inverter output voltage is created by the switches S_2 and S_3. It is made sure that switches S_1 and S_2 or the switches S_3 and S_4 are not triggered at the same interval in order to avoid short circuit in the inverter. The switching pattern explained above is as follows:

$$\mathbf{S_1} = \{ -\alpha < \omega t < \pi-\alpha \text{ and } 2\pi-\alpha < \omega t < 2\pi \}$$

$$\mathbf{S_2} = \pi-\alpha < \omega t < 2\pi-\alpha$$

$$\mathbf{S_3} = \{ -\alpha < \omega t < \alpha \text{ and } \pi+\alpha < \omega t < 2\pi \}$$

$$\mathbf{S_4} = \alpha < \omega t < \pi+\alpha$$

2.3 SIMULATION

The DC source voltage (i.e. 2E) is chosen to be 100 V. The fundamental harmonic component of the desired AC output voltage is 120. According to these values, using equation (1), the firing angle is calculated. Then the gating pulses for all the switches are generated based upon the technique which is discussed in section 2.2. Figure 2.3 shows the generation of gating pulses for the switches S_1, S_2, S_3 and S_4.

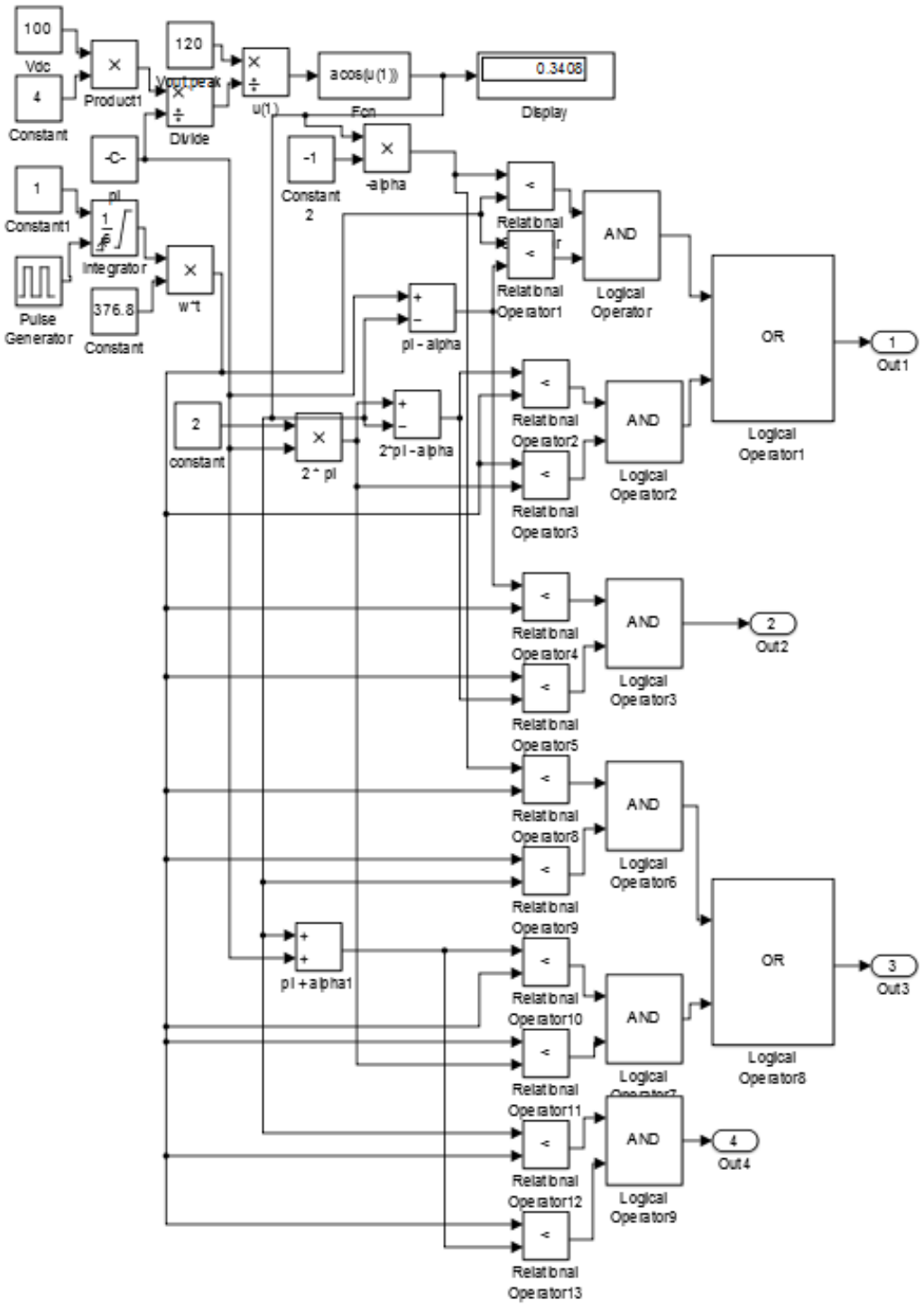

Figure 2.3 Simulink model for gating pulse generator for switches

The values of the load for the inverter is chosen as R=5Ω and L=0.01H. The waveforms of the output voltage and output current of the inverter are obtained as shown in Figure 2.4 and Figure 2.5 respectively.

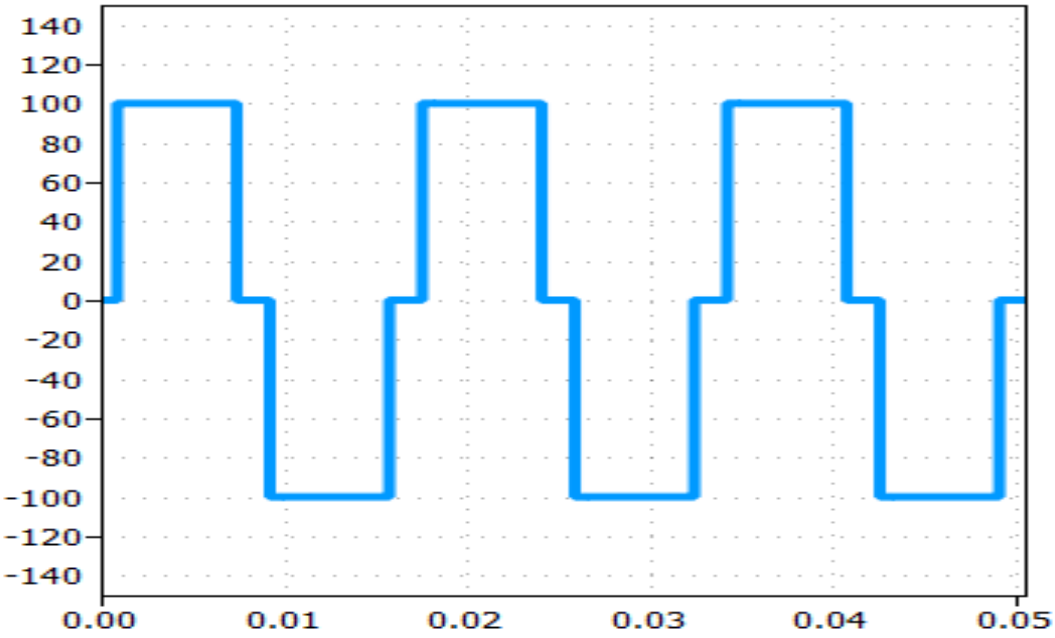

Figure 2.4 Output voltage waveform of single H-bridge inverter

The fundamental harmonic component of the output voltage of the inverter is found to be 120 V as expected.

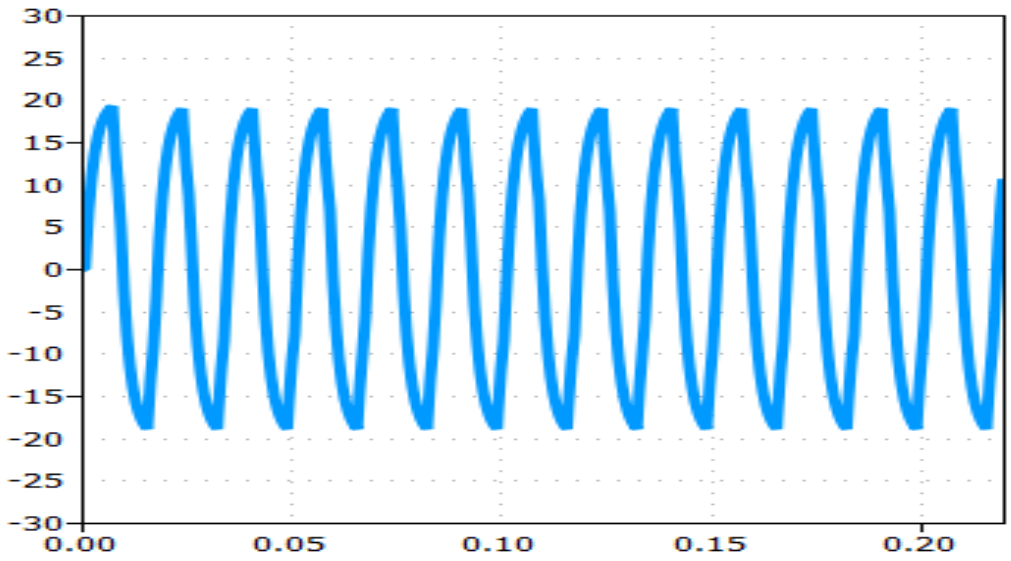

Figure 2.5 Output current waveform of single H-bridge inverter

The fundamental harmonic component of the output current of the inverter is found to be 19.16 A.

2.4 ANALYSIS OF OUTPUT WAVEFORMS

Fast Fourier Transform (FFT) analysis is done in the waveforms of output voltage and current of the inverter in order to know about the Total Harmonic Distortion of the respective waveforms. The results show that THD of the output voltage of the inverter is 29.6% and for the output current of the inverter the THD is 10.10%. These results are shown in the Figure 2.6 and Figure 2.7.

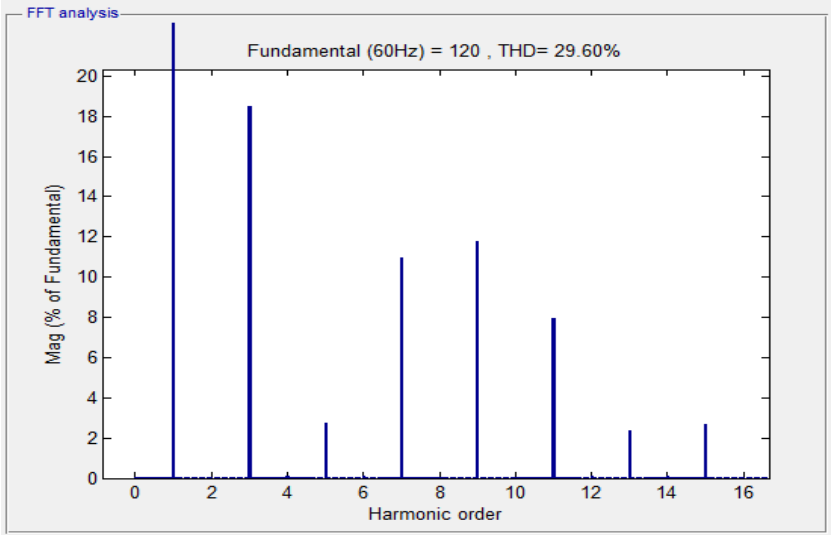

Figure 2.6 FFT Analysis of output voltage of single H-bridge inverter

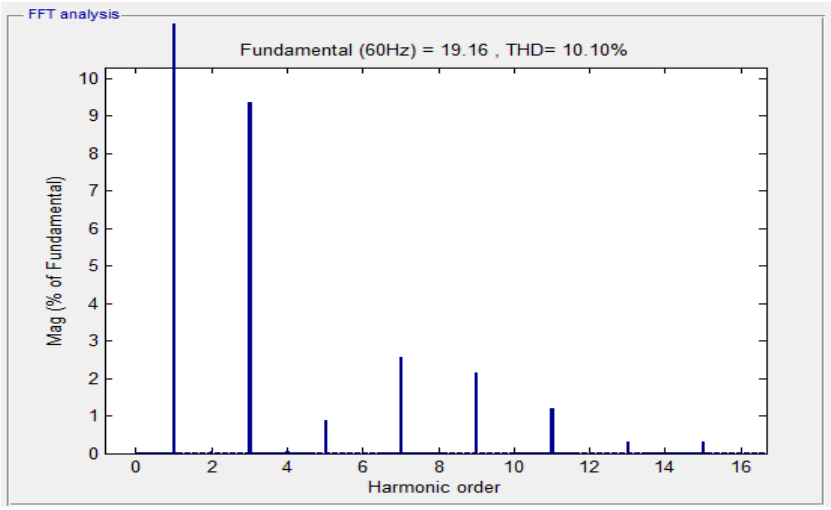

Figure 2.7 FFT Analysis of output current of single H-bridge inverter

3. BIPOLAR PWM INVERTER

3.1 INVERTER TOPOLOGY

The topology of the Bipolar PWM inverter remains same as the single H-bridge inverter discussed in the section 2.1.

3.2 GATING TECHNIQUE

Bipolar Pulse Width Modulation (BPWM) technique is used to generate the gating pulses for the switches in the inverter. This technique is shown is Figure 3.1 [26, 27]. The triangular wave is chosen as the carrier wave. The sinusoidal wave with the same frequency as the desired output waveform is chosen as the reference wave. The sine wave is compared with the triangular wave to generate the gating pulses.

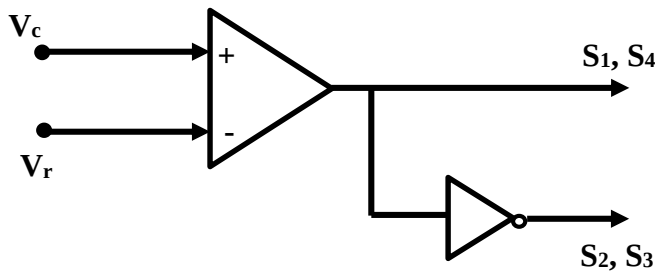

Figure 3.1 Comparison between waves for BPWM

When the value of the triangular wave is greater than the value of the sinusoidal wave, the switches S_1 and S_4 will be ON. Similarly, when the value of the triangular wave is less than the value of the sinusoidal wave, S_2 and S_3 switches will become ON. With the help of these switches, the output voltage waveform is generated. The generation of gating pulses is shown in Figure 3.2.

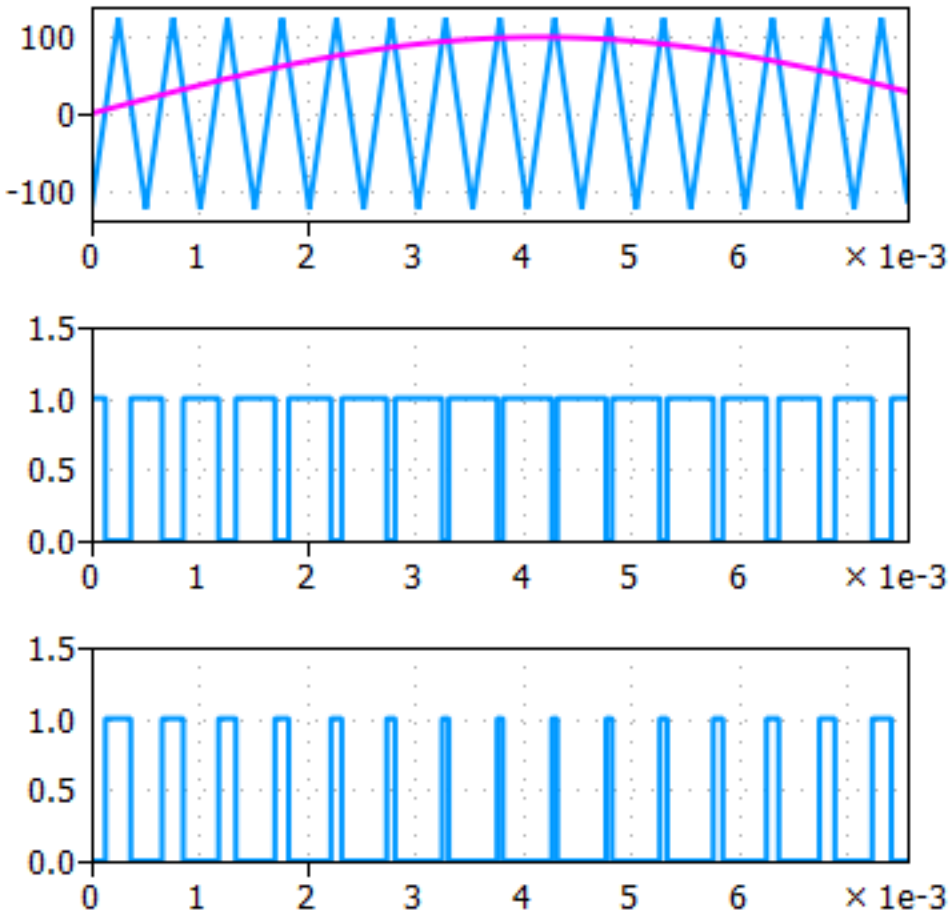

Figure 3.2 Generation of gating pulses for switches

3.3 SIMULATION

The input DC source value of the inverter is taken as 150 V. The desired fundamental harmonic component value of the output voltage is 120 V. Therefore, the chosen value of the modulation index is 0.8. The gating pulses are generated as per section 4.2. The values of the load for the inverter are chosen as R=5Ω and L=0.01H. The waveforms of the output voltage and output current of the inverter are obtained as shown in Figure 3.3 and Figure 3.4 respectively. The fundamental harmonic component of the output voltage and current of the inverter is found to be 119.8 V and 22.45 A respectively.

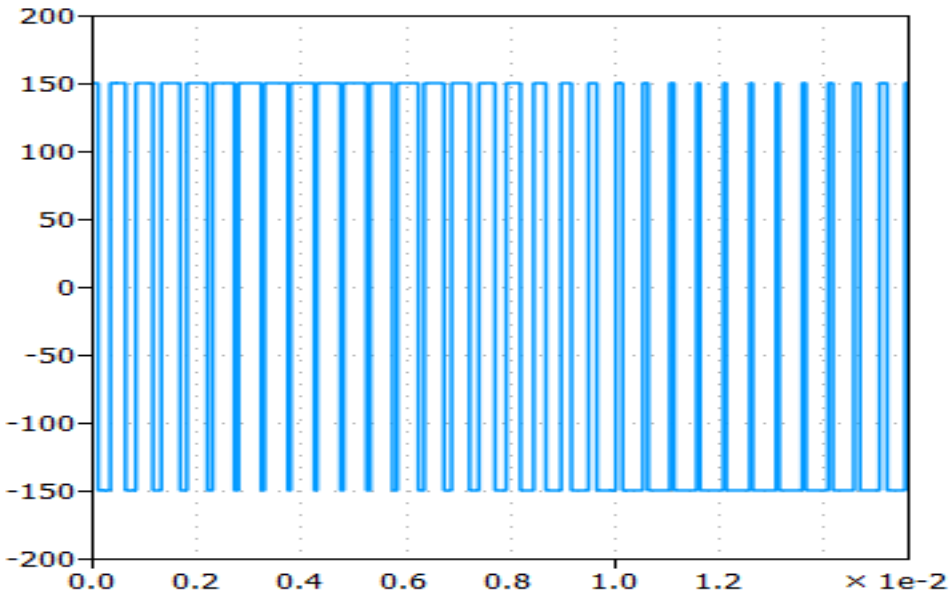

Figure 3.3 Output voltage waveform of BPWM inverter

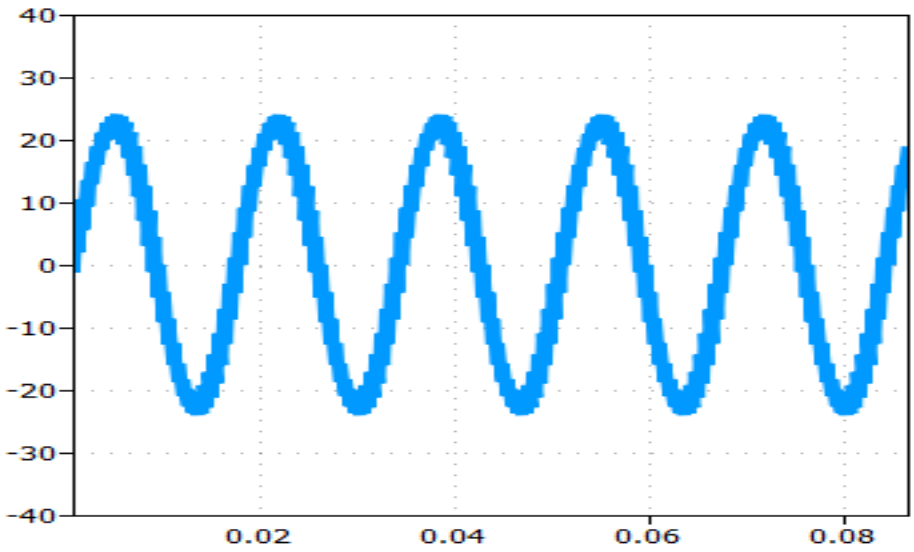

Figure 3.4 Output current waveform of BPWM inverter

3.4 ANALYSIS OF OUTPUT WAVEFORMS

FFT analysis is done in the waveforms of output voltage and current of the inverter; in order to know about the Total Harmonic Distortion (THD) of the respective waveforms. The results show that the THD of the output voltage and output current of the inverter are 146.08% and 9.85% respectively. These results are shown in Figure 3.5 and Figure 3.6.

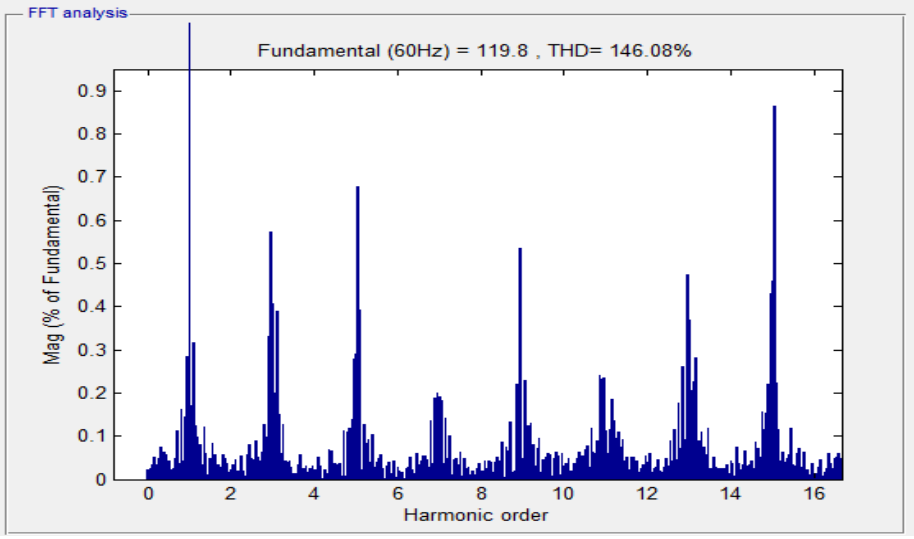

Figure 3.5 FFT Analysis of output voltage of BPWM inverter

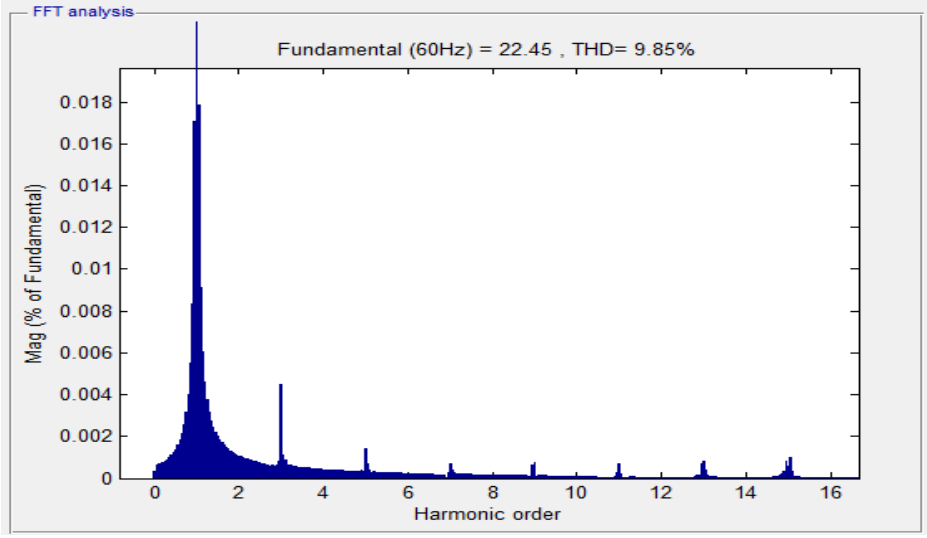

Figure 3.6 FFT Analysis of output current of BPWM inverter

4. HYBRID MULTILEVEL H-BRIDGE INVERTER

4.1 INVERTER TOPOLOGY

This multilevel single phase inverter has two H-Bridge inverters, which are cascaded in series [8,15,17]. One of the inverters would be referred to as the ‘main H-Bridge inverter’ and the other one as the ‘auxiliary H-Bridge inverter’ for easy reference [1]. The topology of the main inverter remains the same as the single H-bridge inverter, which was discussed in chapter 2. The topology of the auxiliary H-bridge inverter is similar to the main inverter; except the DC source. The auxiliary H-bridge inverter is supplied by a capacitor instead of a separate DC source.

Therefore, the overall cascaded H-bridge inverter has eight semi-conductor switches, single DC source and a capacitor. The gating techniques for both main and auxiliary inverters will be different. These techniques will be discussed in detail in section 4.2. The RL load is connected to the cascaded hybrid H-bridge multilevel inverter. The entire topology of the hybrid multilevel H-bridge inverter is shown in Figure 4.1.

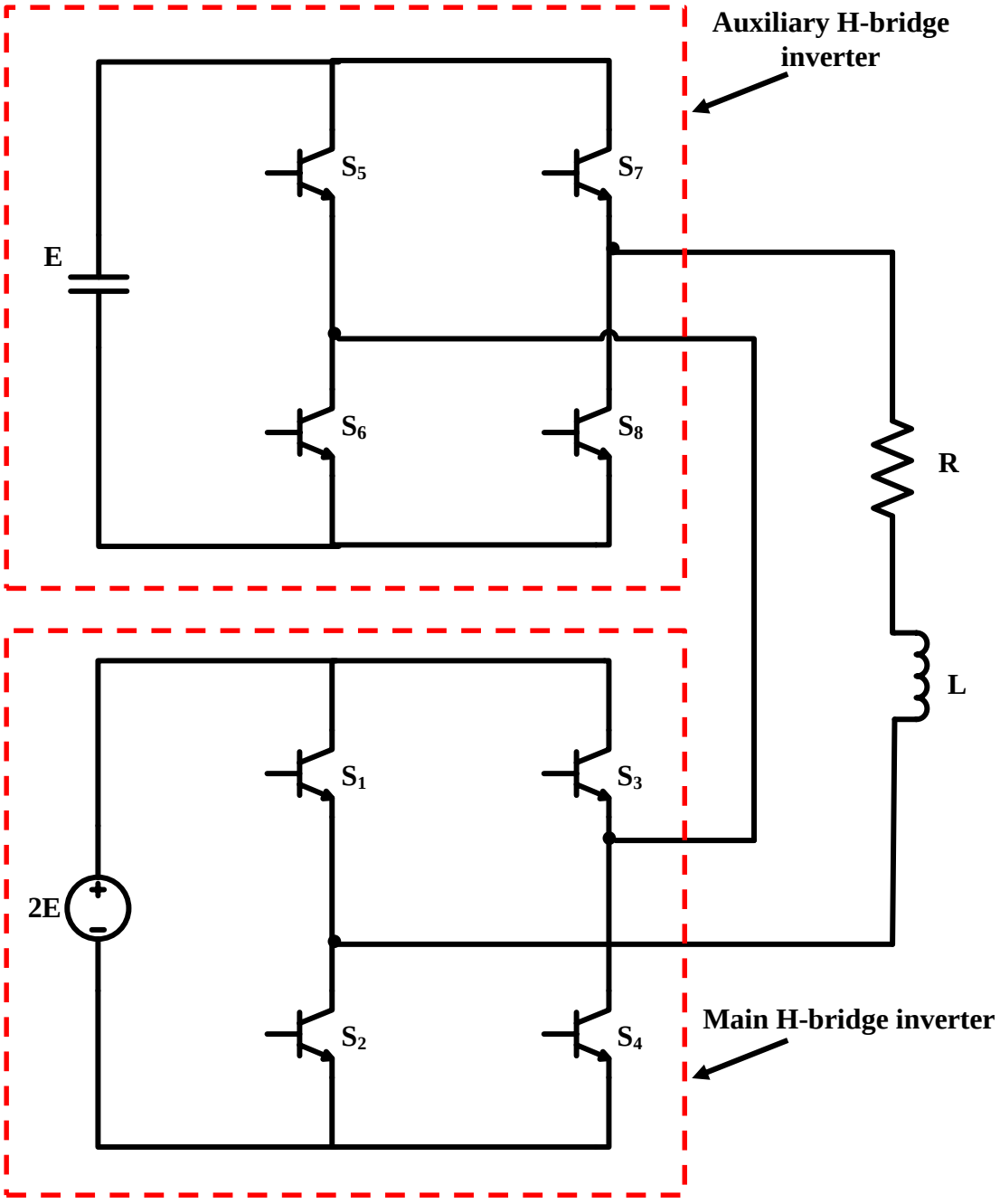

Figure 4.1 Topology of multilevel hybrid H-bridge inverter

As it is discussed in the previous section, the DC voltage source of the main H-bridge inverter is denoted as 2E. The voltage across the capacitor of the auxiliary H-bridge inverter is shown as E, which will be exactly half the value of the main H-bridge inverter DC source. If the DC source is replaced by the capacitor, it is necessary to control the voltage across the capacitor to the desired value [7,22-25]. The capacitor voltage regulation method for controlling the voltage of this inverter is discussed in detail in section 4.4.

4.2 GATING TECHNIQUE OF MAIN H-BRIDGE INVERTER

The gating pulse logic for the main inverter is going to remain the same as the logic followed for the case (i): single H-bridge inverter. But an extra compensation term is involved in calculating the firing angle. The extra compensation term is represented as V_{ma}. This V_{ma} term is added to the desired amplitude of the fundamental harmonic of the inverter output voltage V_m. Due to the operation of the capacitor, there will be a fluctuation in the amplitude of the output voltage waveform. To avoid this, V_{ma} term is added to V_m while calculating the firing angle. This compensation term will be discussed in detail at the end of section 4.4.

Therefore the equation of the firing angle becomes

$$\alpha = \cos^{-1}[\pi(V_m+V_{ma})/8E] \quad (2)$$

The gating pulse logic of the main H-bridge inverter is shown in Figure 4.2.

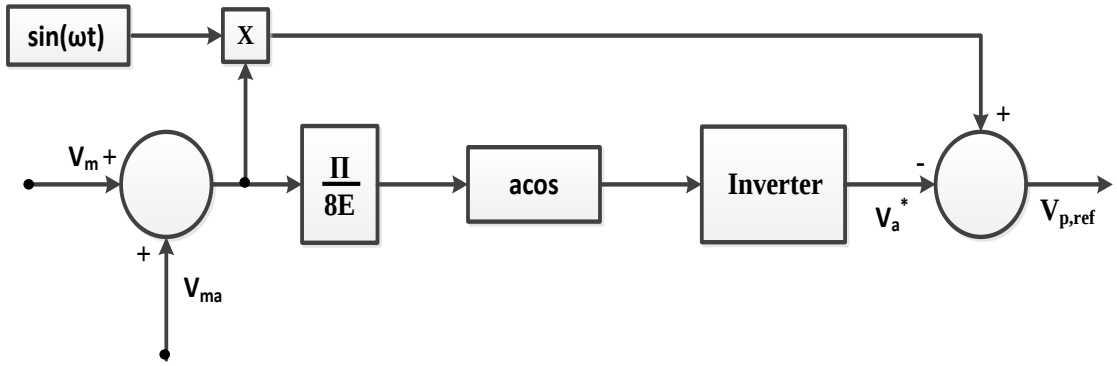

Figure 4.2. Gating pulse logic for main H-bridge inverter [4]

where,

V_m = Amplitude of the desired sinusoidal output waveform

V_{ma} = Extra compensation term

V_a^* = Output of the main inverter

$V_{p,ref}$ = First part of the reference waveform

4.3 GATING TECHNIQUE OF AUXILIARY H-BRIDGE INVERTER

Pulse Width Modulation (PWM) technique is used to generate gating pulses for the auxiliary H-bridge inverter[21]. The reference wave is compared with the carrier wave in order to produce the gating pulses for the switches. This technique is decribed in the Figure 4.3 [26].

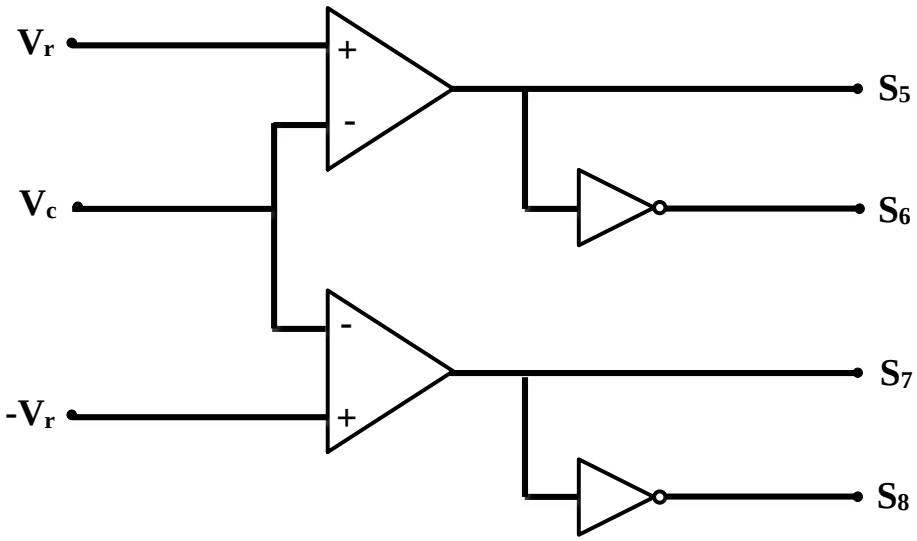

Figure 4.3 Gating pulse logic for auxiliary H-bridge inverter

4.3.1 Carrier Waveform. In this Pulse Width Modulation technique, triangular wave is used as the carrier waveform to be compared with the reference waveform.

4.3.2 Reference Waveform. The generation of reference waveform is splitted into two parts. The first part of the waveform is denoted as $V_{p,ref}$. The output waveform of the main H-bridge inverter (V_a^*) is subtracted from the desired sinusoidal output waveform to generate the first part of the reference waveform [6]. This is shown in Figure 4.4 and Figure 4.5. In Figure 4.5, an inequality in the peak magnitude of the waveform is clearly visible. This is mainly due to the operation of capacitor. The equation of the first part of the reference waveform is derived as:

$$V_{p,ref} = [(V_m+V_{ma}) \sin(\omega t)] - V_a^* \quad (3)$$

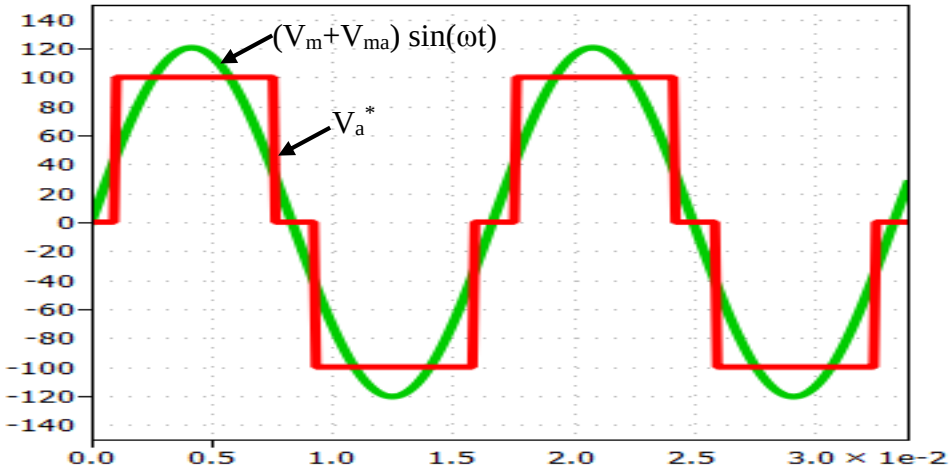

Figure 4.4 Subracting output of main inverter from desired output waveform

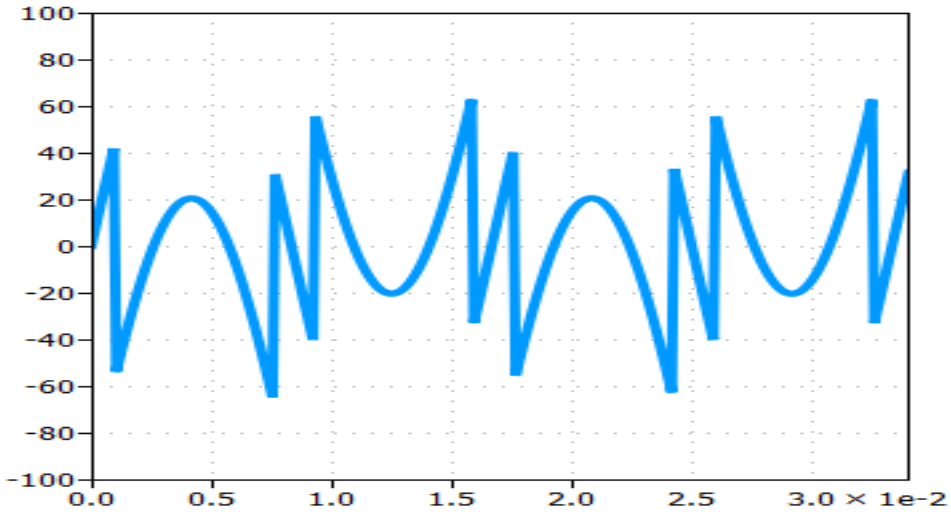

Figure 4.5 Resultant first part of the refernce waveform

The second part of the reference waveform (V_r) is generated by subtracting the output of the PI controller from the first part of the reference waveform ($V_{p,ref}$). This will be discussed in detail in later part of the section 4.4. The final reference waveform is

compared with the triangular waveform to synthesize the gating pulses for switches S_5, S_6, S_7 and S_8. These are depicted in the Figure 4.6.

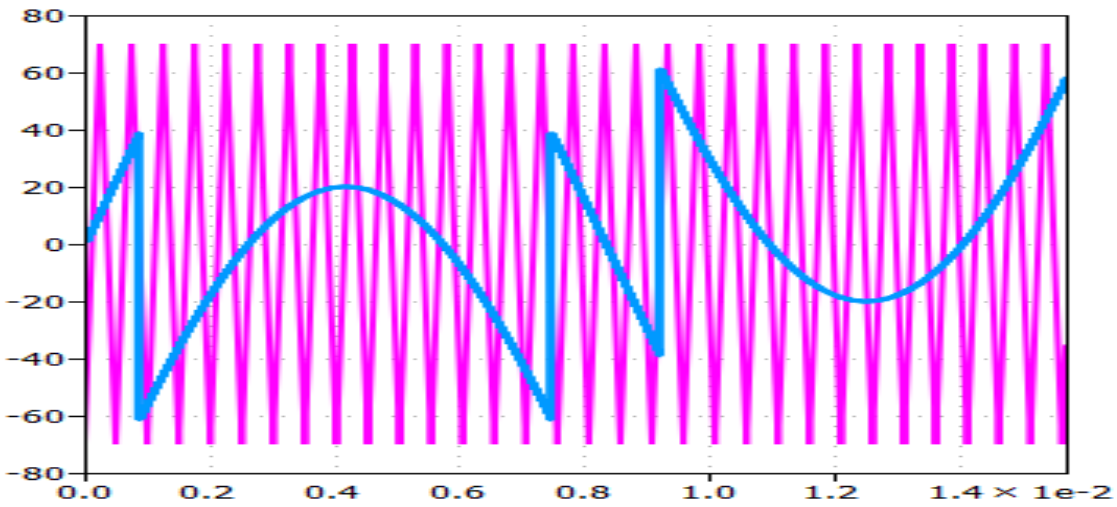

Figure 4.6 Comparing final reference waveform with carier waveform

Whenever the value of reference waveform is greater than the carier waveform, switch S_5 will be triggered and vice versa for the switch S_6. Similarly, if the negative value of the reference waveform is greater than the triangular waveform, the gating pulse will be ON for the switch S_7 and vice versa for S_8 switch.

4.4 CAPACITOR VOLTAGE REGULATION

The voltage across the capacitor has to be maintained at the desired value for the proper functioning of the cascaded H-bridge inverter. There are many methods available

already to control the voltage of the capacitor [9-16,19,20]. One of those methods is dicussed in this section.

The main H-bridge inverter involves in generating fundamental harmonic component of the output voltage of the entire cascaded H-bridge inverter. The auxiliary H-bridge inverter does not involve in producing fundamental harmonic component. This is the main principle used in voltage regulation method [4]. During the fundamental line frequency period, auxiliary H-bridge inverter should not supply the average active power. The capacitor voltage regulation method is depicted in Figure 4.7.

The desired value across the capacitor is denoted as E. The voltage value of the capacitor of the auxiliary H-bridge inverter has to be maintained at half the value of the DC source of the main H-bridge inverter [1,4]. This is the reason for naming the DC voltage source as 2E as per the convenience.

In the reference waveform of the auxiliary H-bridge inverter, a small amount of the fundamental harmonic component is added or subtracted based upon the measured voltage across the capacitor.

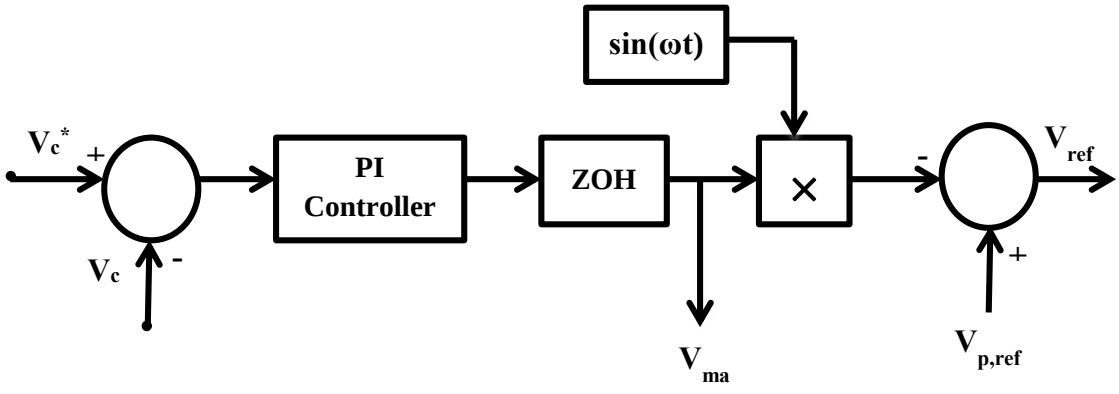

Figure 4.7 Capacitor voltage regulation method [4]

The measured voltage across the capacitor is subtracted from the desired voltage of the capacitor (i.e. E). The resultant value is given to the PI controller. The PI controller design is shown in the Figure 4.8.

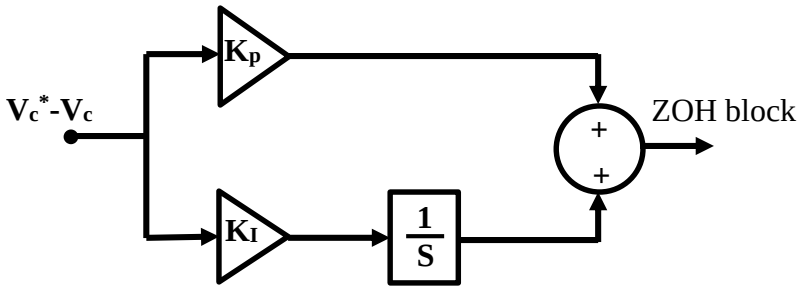

Figure 4.8. PI Controller

Then zero-order hold (ZOH) block is used to sample the output of the PI controller at every period cycle. With the help of this, the fundamental harmonic component added to the reference waveform of the auxialiary H-bridge is kept constant during each line period. This is done to overcome the distortion due to the capacitor voltage regulation in the cascaded H-bridge inverter output voltage. The ouptut of the ZOH block (i.e. V_{ma}) is fedback and added to the desired amplitude of the output sinusoidal waveform (i.e. V_m). The resultant value is used to calculate the firing angle of the main H-bridge inverter. Additionally, it is also used to compare it with the output of the main H-bridge inverter after multiplying it with the sinusoidal waveform of same frequency to create the first part of the reference waveform. This is shown in detail in the Figure 4.2. This feedback is done

to avoid any increase or decrease in the amplitude of the fundamental harmonic companent of the cascaded H-Bridge inverter. The output value of the ZOH block is mulitplied with the sinusoidal waveform and then it is subtracted from the first part of the reference waveform. The resultant will be the final reference waveform which will be used to companre with the carier wave in Pulse Width Modulation technique to generate the gating pulse for the auxiliary H-bridge inverter. The final reference voltage waveform is given in the equation 4.

$$V_{ref} = V_{p,ref} - [(V_c^* - V_c)*(K_p + K_i/s)*\sin(\omega t)] \quad (4)$$

where,

V_c^* = Desired voltage across the capacitor

V_c = Measured voltage across the capacitor

V_{ma} = Extra compensation term

$V_{p,ref}$ = First part of reference waveform

V_{ref} = Final reference waveform

K_p = Proportional gain of PI controller

K_I = Integral gain of PI controller

This entire method depends upon the power supplied by the auxiliary H-bridge inverter. Whenever the value of the measured voltage across the capacitor is greater than

the desired voltage value of the capacitor, a small sinusoidal waveform which has the same fundamental frequency is added to the first part of the reference waveform. This indicates the involvement of auxiliary H-bridge inverter in generating the fundamental harmonic component of the output waveform of the cascaded H-bridge inverter and also produce active power. As the auxiliary H-bridge inverter involves in generating power, the charge of the capactior decreases automatically. Therefore, the measured voltage across the capacitor will come down to the desired voltage value E.

Similarly, if the voltage measured across the capacitor is less than the desired value, a small sinusoidal waveform, which has the same fundamental frequency, is subtracted from the first part of the reference waveform. This makes the auxiliary H-bridge inverter to absorb the power. So, the capacitor gets charged and the measured voltage across the capacitor increases and reaches the desired value. By this way, the voltage across the capacitor is maintained at the desired value.

Under the normal operating condition, auxiliary H-bridge inverter does not involve in generating or absorbing power. But a small amount of active power is supplied or absorbed in order to regulate the capacitor voltage.

4.5 SIMULATION

The DC source voltage (i.e. 2E) of the main inverter H-bridge inverter is chosen to be 100 V. The fundamental harmonic component of the desired AC output voltage is 120 V. According to these values, using equation (2), the firing angle is calculated. Then the gating pulses for all the switches in the main H-bridge inverter are generated based upon the technique which is discussed in 2.2.

Then PWM technique is used to synthesize gating pulses for the auxiliary H-bridge inverter switches as discussed in the section 4.3. The voltage across the capacitor is maintained at 50 V, which is half of the value of DC source of the main H-bridge inverter, with the help of capacitor voltage regulation method discussed in section 4.4. The voltage waveform across the capacitor is depicted in the Figure 4.9.

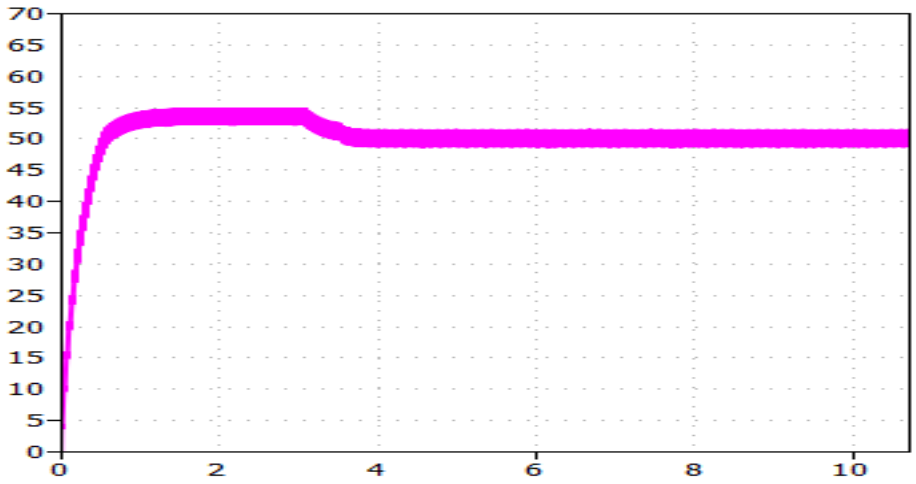

Figure 4.9. Capacitor voltage waveform

The value of the load for the cascaded H-bridge inverter is chosen as R=5Ω and L=0.01H. The waveforms of the output voltage of the auxiliary H-bridge inverter and the waveforms of output voltage and output current of the cascaded inverter are obtained as shown in Figure 4.9, Figure 4.10 and Figure 4.11 respectively.

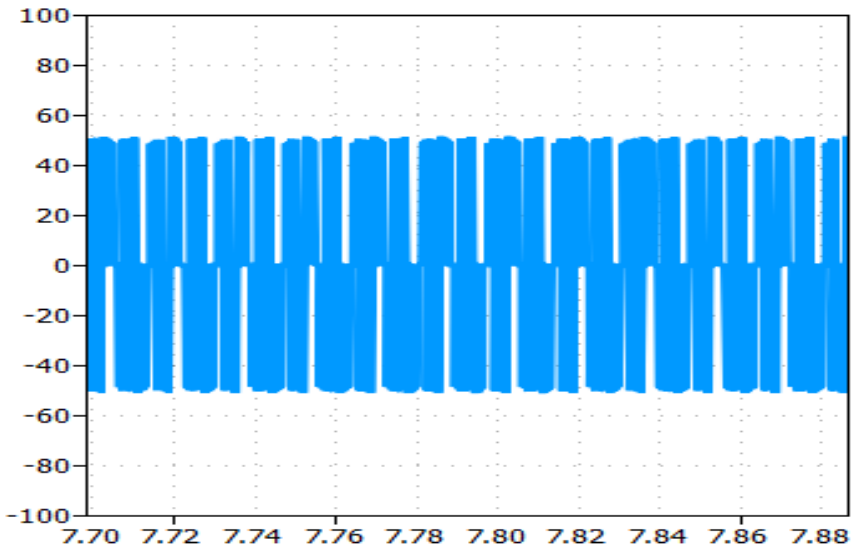

Figure 4.10 Output voltage waveform of auxiliary H-bridge inverter

In the Figure 4.11, there are some spikes in the output voltage waveform of the cascaded H-bridge inverter. It is due to the increase in output voltage of the main inverter and the decrease in output voltage of the auxiliary inverter at the same instant.

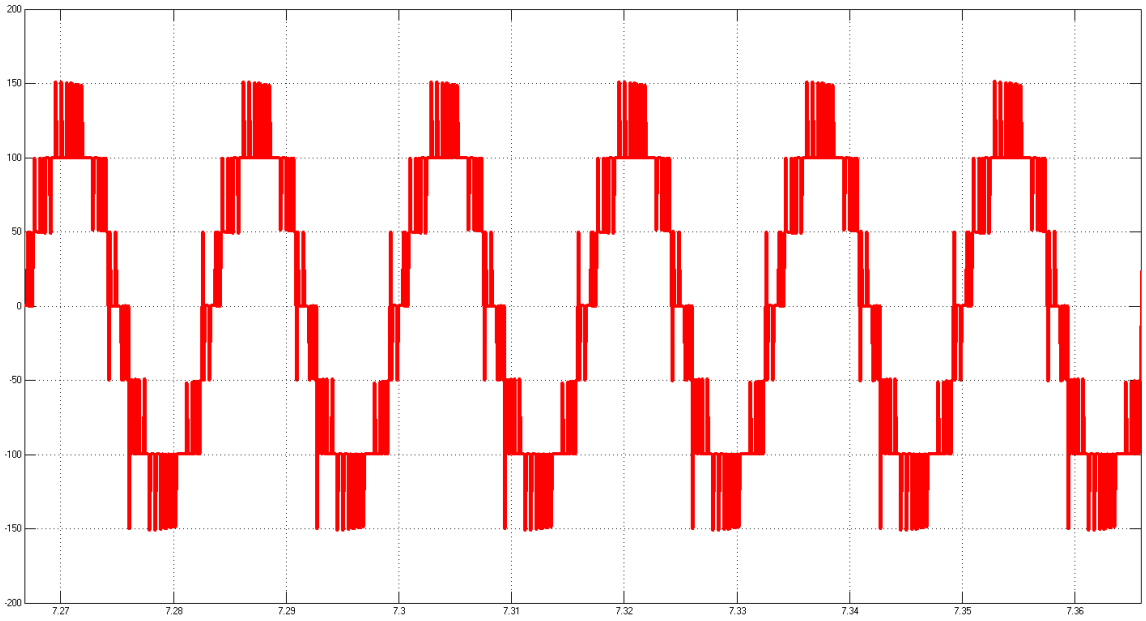

Figure 4.11 Output voltage waveform of cascaded H-bridge inverter

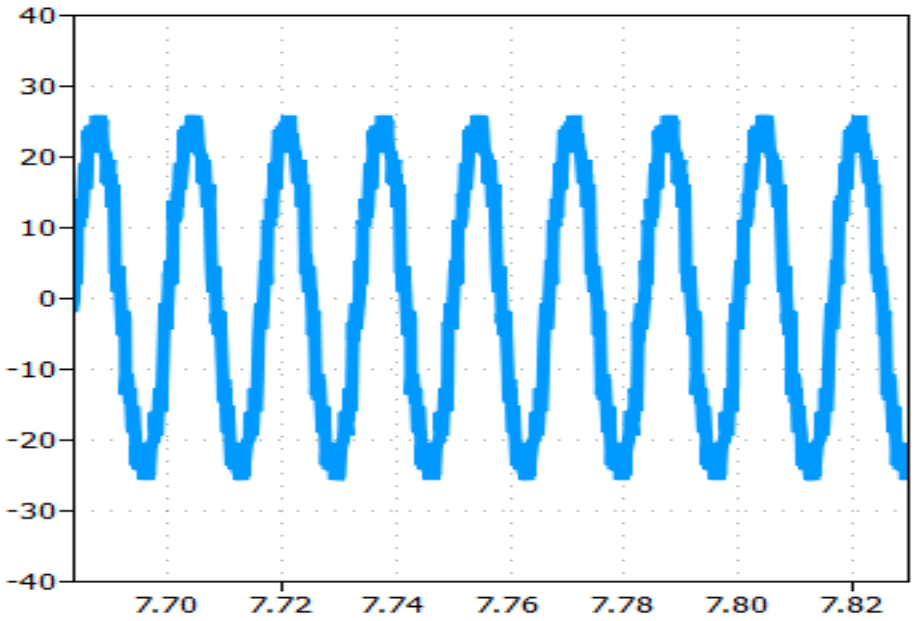

Figure 4.12 Output current waveform of cascaded H-bridge inverter

The fundamental harmonic component of the output voltage and output current of the inverter is found to be 121.3 V and 24.19 A respectively.

4.6. ANALYSIS OF OUTPUT WAVEFORMS

FFT analysis is done in the waveforms of output voltage and current of the cascaded H-bridge inverter to determine about the Total Harmonic Distortion (THD) of the respective waveforms. The results show that THD of the output voltage of the inverter is 22.51% and for the output current of the inverter the THD is 10.31%. These results are shown in the Figure 4.13 and Figure 4.14 respectively.

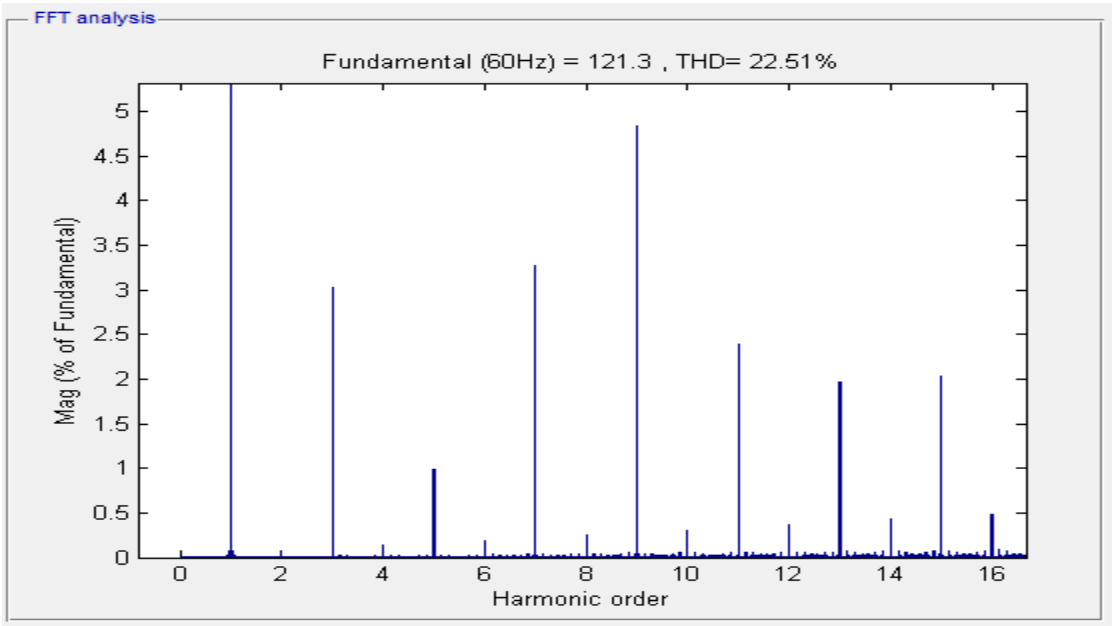

Figure 4.13 FFT Analysis of cascaded H-bridge inverter output voltage

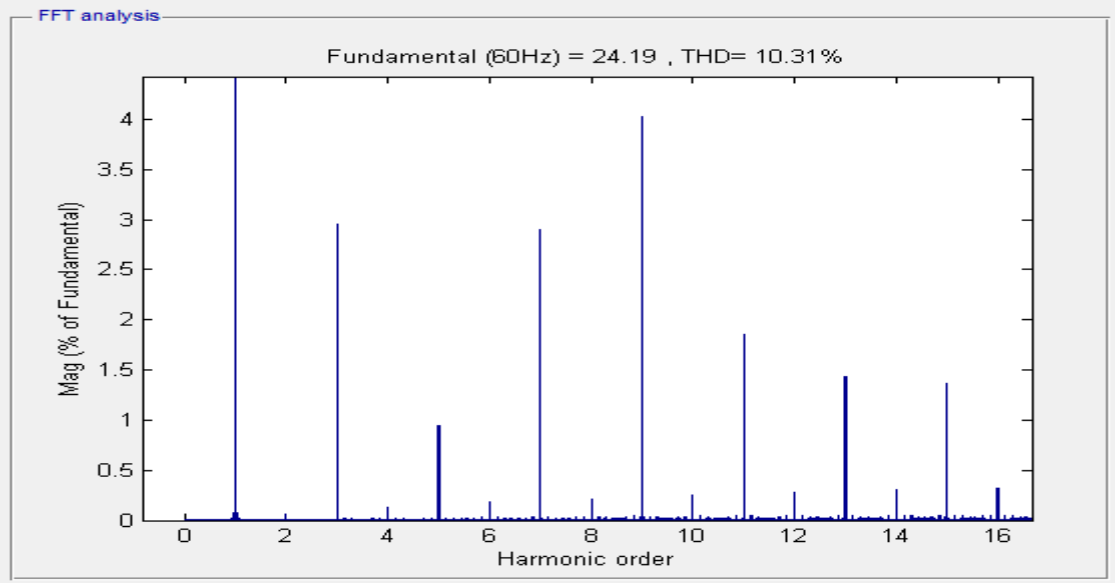

Figure 4.14 FFT Analysis of cascaded H-bridge inverter output current

5. COMPARISON BETWEEN THREE INVERTERS

Here, these three inverters are compared based on the obtained THD values. Firstly, the inductor load which is connected to these inverters is varied in order to get around 10% of THD in the output current. Based upon the chosen inductor values, these three inverters are compared as shown in Figure 5.1.

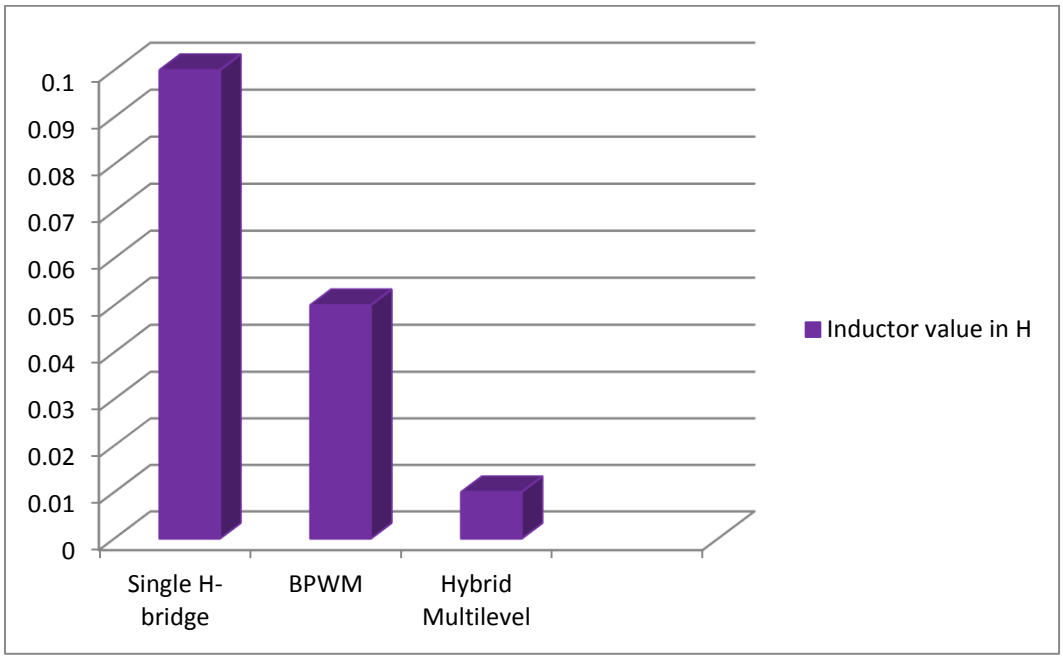

Figure 5.1 Comparison of three inverters based on load inductor value

Then, the load value of all the inverters is kept constant to compare the THD of the output current of the three inverters. The chosen value of the load is R= 5Ω and L= 10mH. This comparison is depicted in the Figure 5.2.

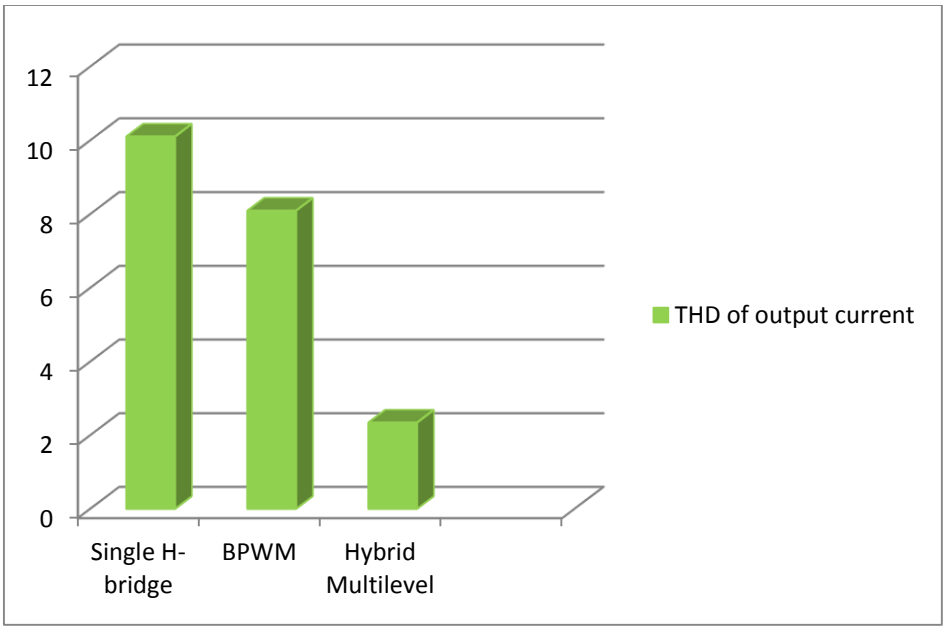

Figure 5.2 Comparison of three inverters based on THD of output current

There are many other considerations, which will be taken in account while choosing an inverter. Based on those constraints, these three inverters are compared and tabulated as in Table 5.1

Table 5.1 Comparison of three inverters

Inverter type	Size	Cost	No. of components used	Design
Single H-bridge	Large	High	Less	Easy
BPWM	Large	High	Less	Easy
Hybrid Multilevel	Small	Low	High	Difficult

Hybrid multilevel inverter shows better performance in THD but the size and cost of the inverter are high; when compared to the other inverters. Therefore, choosing the particular inverter is completely dependent on the user requirements. If the user requires an inverter with less THD and has low cost and size then hybrid multilevel inverter should be an ideal choice. If the no. of components used and the design level are the major constraint of the user, then either a single H-bridge or BPWM inverter can serve better.

6. CONCLUSION

In this thesis, three types of inverters are simulated and analyzed based upon their performance. A single H-bridge inverter is simulated using PLECS software and gating pulses for the switches are generated based on the desired output waveform of the inverter. Then, with the same inverter topology, Bipolar Pulse Width Modulation (BPWM) technique is used to control the operation of the switches in the inverter. A hybrid multilevel cascaded H-bridge inverter is also designed by connecting two H-bridge inverters in series. One of them has a DC source and the other one has a capacitor as its source. PWM technique is used to create the gating pulses for the auxiliary inverter. The capacitor voltage regulation method is proposed to control the voltage across the capacitor at the desired value. The FFT Analysis is performed to calculate the Total Harmonic Distortion (THD) of the inverters' output voltage and current. While analyzing the performance of all the three inverters, hybrid multilevel cascaded H-bridge inverter shows better performance in terms of THD, cost and size of the inverter. In terms of no. of components used and design level, hybrid multilevel inverter is not better than the other two inverters. Therefore, based upon the requirements of the user, the respective inverter is selected.

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