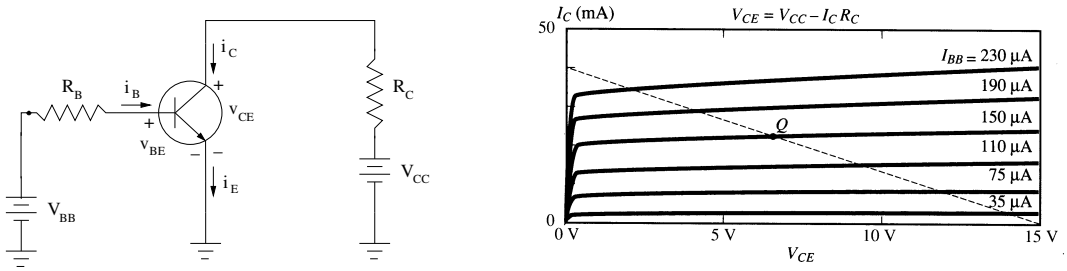
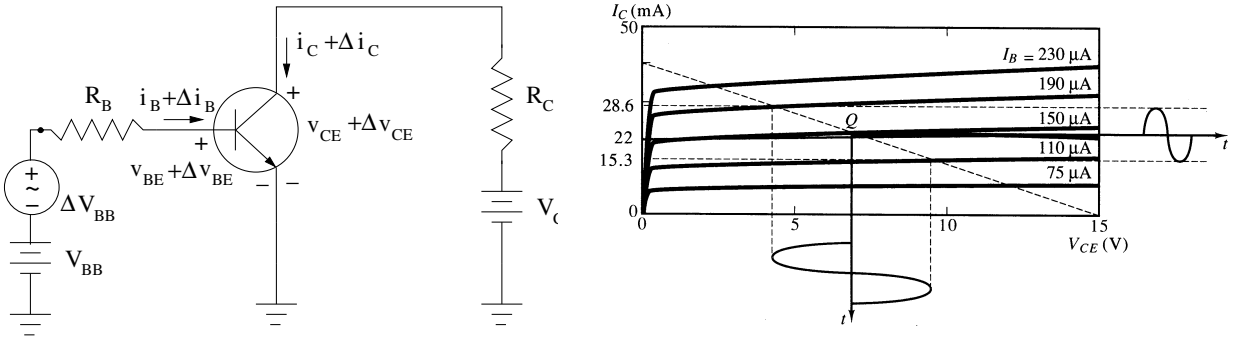
Transistor amplifiers: Biasing and Small Signal Model

Transistor amplifiers utilizing BJT or FET are similar in design and analysis. Accordingly we will discuss BJT amplifiers thoroughly. Then, similar FET circuits are briefly reviewed.

Consider the circuit below. The operating point of the BJT is shown in the $i_C v_{CE}$ space.



Let us add a sinusoidal source with an amplitude of ΔV_{BB} in series with V_{BB}. In response to this additional source, the base current will become $i_B + \Delta i_B$ leading to the collector current of $i_C + \Delta i_C$ and CE voltage of $v_{CE} + \Delta v_{CE}$.



For example, without the sinusoidal source, the base current is 150 μA, $i_C = 22$ mA, and $v_{CE} = 7$ V (the Q point). If the amplitude of Δi_B is 40 μA, then with the addition of the sinusoidal source $i_B + \Delta i_B = 150 + 40\cos(\omega t)$ and varies from 110 to 190 μA. The BJT operating point should remain on the load line and collector current and CE voltage change with changing base current while remaining on the load line. For example when base current is 190 μA, the collector current is 28.6 mA and CE voltage is about 4.5 V. As can be seen from the figure above, the collector current will approximately be $i_C + \Delta i_C = 22 + 6.6\cos(\omega t)$ and CE voltage is $v_{CE} + \Delta v_{CE} = 7 - 2.5\cos(\omega t)$.

The above example shows that the signal from the sinusoidal source ΔV_{BB} is greatly amplified and appears as changes either in collector current or CE voltage. It is clear from the figure that this happens as long as the BJT stays in the active-linear region. As the amplitude of Δi_B is increased, the swings of BJT operating point along the load line become larger and

larger and, at some value of Δi_B, BJT will enter either the cut-off or saturation region and the output signals will not be a sinusoidal function. **Note:** An important observation is that one should locate the Q point in the middle of the load line if we want to have the largest output signal.

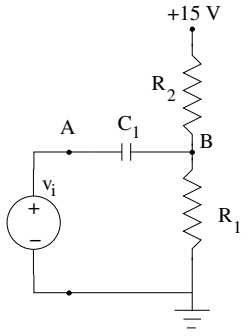
The above circuit, however, has two major problems: 1) The input signal, ΔV_{BB}, is in series with the V_{BB} biasing voltage making design of previous two-port network difficult, and 2) The output signal is usually taken across R_C as $R_C \times i_C$. This output voltage has a DC component which is of no interest and can cause problems in the design of the next-stage, two-port network.

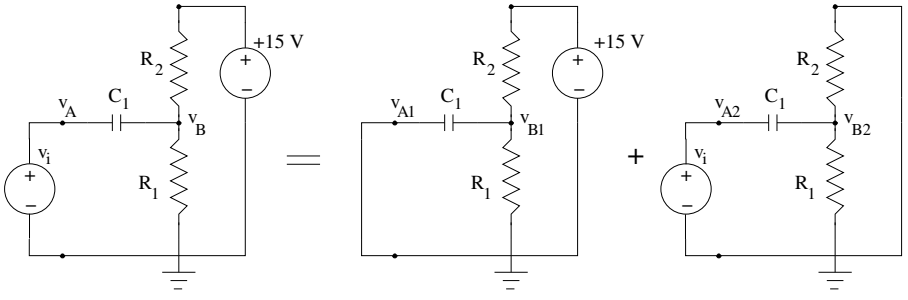
The DC voltage needed to "bias" the BJT (establish the Q point) and the AC signal of interest can be added together or separated using capacitor coupling as discussed below.

Capacitive Coupling

For DC voltages ($\omega = 0$), the capacitor is an open circuit (infinite impedance). For AC voltages, the impedance of a capacitor, $Z = -j/(\omega C)$, can be made sufficiently small by choosing an appropriately large value for C (the higher the frequency, the lower C that one needs). This property of capacitors can be used to add and separate AC and DC signals. Example below highlights this effect.

Consider the circuit below which includes a DC source of 15 V and an AC source of $v_i = V_i \cos(\omega t)$. We are interested to calculate voltages v_A and v_B. The best method to solve this circuit is superposition. The circuit is broken into two circuits. In circuit 1, we "kill" the AC source and keep the DC source. In circuit 2, we "kill" the DC source and keep the AC source. Superposition principle states that $v_A = v_{A1} + v_{A2}$ and $v_B = v_{B1} + v_{B2}$.





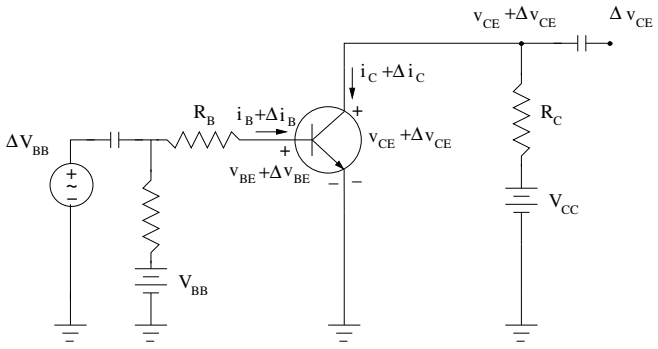
Consider the first circuit. It is driven by a DC source and, therefore, the capacitor will act as open circuit. The voltage $v_{A1} = 0$ as it is connected to ground and v_{B1} can be found by voltage divider formula: $v_{B1} = 15R_1/(R_1 + R_2)$. As can be seen both v_{A1} and v_{B1} are DC voltages.

In the second circuit, resistors R_1 and R_2 are in parallel. Let $R_b = R_1 \parallel R_2$. The circuit is a high-pass filter: $V_{A2} = V_i$ and $V_{B2} = V_i(R_b)/(R_b + 1/j\omega C)$. If we operate the circuit at frequency above the cut-off frequency of the filter, *i.e.,* $R_b \gg 1/\omega C$, we will have $V_{B2} \approx V_{A2} = V_i$ and $v_{B2} \approx v_{A2} = V_i \cos(\omega t)$. Therefore,

$$v_A = v_{A1} + v_{A2} = V_i \cos(\omega t)$$
$$v_B = v_{B1} + v_{B2} = \frac{R_1}{R_1 + R_2} \times 15 + V_i \cos(\omega t)$$

Obviously, the capacitor is preventing the DC voltage to appear at point A, while the voltage at point B is the sum of DC signal from 15-V supply and the AC signal.

Using capacitive coupling, we can reconfigure our previous amplifier circuit as is shown in the figure below. Capacitive coupling is used extensively in transistor amplifiers.



BJT amplifier circuits are analyzed using superposition principle, similar to example above:

1) DC Biasing: Input signal is set to zero and capacitors act as open circuit. This analysis establishes the Q point in the active linear region.

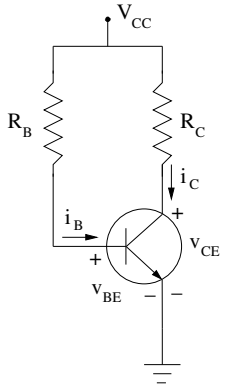
2) AC Response: DC bias voltages are set to zero. The response of the circuit to an AC input signal is calculated and transfer function, input and output impedances, *etc.* are found.

The break up of the problem into these two parts have an additional advantage as the requirement for accuracy are different in the two cases. For DC biasing, we are interested in locating the Q point roughly in the middle of active linear region. The exact location of the Q point is not important. Thus, a simple model, such as large-signal model of page 78 is quite adequate. We are, however, interested to compute the transfer function for AC signals quite accurately. Our large-signal model is not good for the desired accuracy and we will develop a model which is accurate for small AC signals below.

FET-based amplifier are similar. FET should be biased similar to BJT. Analysis method is also similar and broken into DC biasing and AC response.

BJT Biasing

A simple bias circuit is shown. As we like to have only one power supply, the base circuit is also powered by V_{CC}. (To avoid confusion, we will use capital letters to denote DC bias values *e.g.,* I_C.) Assuming that BJT is in active-linear state, we have:



$$\text{BE-KVL:}\quad V_{CC} = I_B R_B + V_{BE} \quad \rightarrow \quad I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B}$$

$$\text{CE-KVL:}\quad V_{CC} = I_C R_C + V_{CE} \quad \rightarrow \quad V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_{CC} - \beta \frac{R_C}{R_B}(V_{CC} - V_{BE})$$

For a given circuit (known R_C, R_B, V_{CC}, and BJT β) the above equations can be solved to find the Q-point (I_B, I_C, and V_{CE}). Alternatively, one can use the above equation to design a BJT circuit (known β) to operate at a certain Q point. (Note: Do not memorize the above equations or use them as formulas, they can be easily derived from simple KVLs).

Example 1: Find values of R_C, R_B in the above circuit with $\beta = 100$ and $V_{CC} = 15$ V so that the Q-point is $I_C = 25$ mA and $V_{CE} = 7.5$ V.

Since the BJT is in active-linear region ($V_{CE} = 7.5 > V_\gamma$), $I_B = I_C/\beta = 0.25$ mA. Writing the KVLs that include V_{BE} and V_{CE} we get:

$$\text{BE-KVL:}\quad V_{CC} + R_B I_B + V_{BE} = 0 \quad \rightarrow \quad R_B = \frac{15 - 0.7}{0.250} = 57.2\ \text{k}\Omega$$

$$\text{CE-KVL:}\quad V_{CC} = I_C R_C + V_{CE} \quad \rightarrow \quad 15 = 25 \times 10^{-3} R_C + 7.5 \quad \rightarrow \quad R_C = 300\ \Omega$$

Example 2: Consider the circuit designed in example 1. What is the Q point if $\beta = 200$.

We have $R_B = 57.2$ kΩ, $R_C = 300\ \Omega$, and $V_{CC} = 15$ V but I_B, I_C, and V_{CE} are unknown. They can be found by writing KVLs that include V_{BE} and V_{CE}:

$$\text{BE-KVL:}\quad V_{CC} + R_B I_B + V_{BE} = 0 \quad \rightarrow \quad I_B = \frac{V_{CC} - V_{BE}}{R_B} = 0.25\ \text{mA}$$

$$I_C = \beta\, I_B = 50\ \text{mA}$$

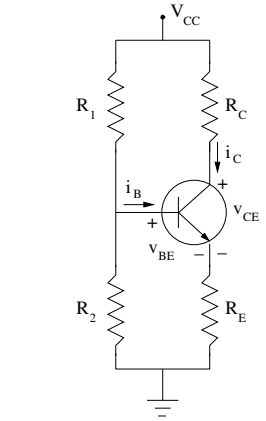
$$\text{CE-KVL:}\quad V_{CC} = I_C R_C + V_{CE} \quad \rightarrow \quad V_{CE} = 15 - 300 \times 50 \times 10^{-3} = 0$$

As $V_{CE} < v_\gamma$ the BJT is not in active-linear region and the above equations are not valid. Values of I_C and V_{CE} should be calculated using the BJT model for saturation region.

The above examples show the problem with our simple biasing circuit as the β of a commercial BJT can depart by a factor of 2 from its average value given in the manufacturers' spec sheet. Environmental conditions can also play an important role. In a given BJT, I_C increases by 9% per °C for a fixed V_{BE}. Consider a circuit which is tested to operate perfectly at 25°C. At a temperature of 35°C, I_C will be roughly doubled and the BJT will be in saturation!

The problem is that our biasing circuit fixes the value of I_B (independent of BJT parameters) and, as a result, both I_C and V_{CE} are directly proportional to BJT β (see formulas in the previous page). A biasing scheme should be found that make the Q-point (I_C and V_{CE}) independent of transistor β and insensitive to the above problems → Use negative feedback!

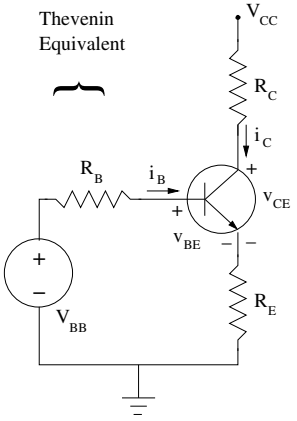
Stable biasing schemes



This biasing scheme can be best analyzed and understood if we replace R_1 and R_2 voltage divider with its Thevenin equivalent:

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \quad \text{and} \quad R_B = R_1 \parallel R_2$$

The emitter resistor, R_E is a sneaky feedback. Suppose I_C becomes larger than the designed value (larger β, increase in temperature, *etc.*). Then, $V_E = R_E I_E$ will increase. Since V_{BB} and R_B do not change, KVL in the BE loop shows that I_B should decrease which will reduce I_C back to its design value. If I_C becomes smaller than its design value opposite happens, I_B has to increase and will increase and stabilize I_C.



Analysis below also shows that the Q point is independent of BJT parameters:

$$I_E \approx I_C = \beta I_B$$

$$\text{BE-KVL:} \quad V_{BB} = R_B I_B + V_{BE} + I_E R_E \quad \rightarrow \quad I_B = \frac{V_{BB} - V_{BE}}{R_B + \beta R_E}$$

$$\text{CE-KVL:} \quad V_{CC} = R_C I_C + V_{CE} + I_E R_E \quad \rightarrow \quad V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Choose R_B such that $R_B \ll \beta R_E$ (this is the condition for the feedback to be effective):

$$I_B \approx \frac{V_{BB} - V_{BE}}{\beta R_E}$$

$$I_C \approx \frac{V_{BB} - V_{BE}}{R_E}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \approx V_{CC} - \frac{R_C + R_E}{R_E}(V_{BB} - V_{BE})$$

Note that now both I_C and V_{CE} are independent of β!

One can appreciate the working of this biasing scheme by comparing it to the poor biasing circuit of page 109. In that circuit, I_B was set by the values of V_{CC} and R_B. As a result, $I_C = \beta I_B$ was directly proportional to β. In this circuit, KVL in BE loop gives $V_{BB} = R_B I_B + V_{BE} + I_E R_E$. If we choose $R_B I_B \ll I_E R_E$ or $R_B \ll (I_E/I_B)R_E \approx \beta R_E$ (feedback condition above), the KVL reduces to $V_{BB} \approx V_{BE} + I_E R_E$, forcing a constant I_E independent of BJT parameters. As $I_C \approx I_E$ this will also fixes the Q point of BJT. If BJT parameters change (different β, change in temperature), the circuit forces I_E to remain fixed and changes I_B!

Another important point follows from $V_{BB} \approx V_{BE} + I_E R_E$. As V_{BE} is not a constant and can change slightly (can drop to 0.6 or increase to 0.8 V), we need to ensure that $I_E R_E$ is much larger than possible changes in V_{BE}. As changes in V_{BE} is about 0.1 V, we need to ensure that $V_E = I_E R_E \gg 0.1$ or $\underline{V_E > 10 \times 0.1 = 1 \text{ V}}$.

Example: Design a stable bias circuit with a Q point of $I_C = 2.5$ mA and $V_{CE} = 7.5$ V. Transistor β ranges from 50 to 200.

Step 1: Find V_{CC}: As we like to have the Q-point to be located in the middle of the load line, we set $V_{CC} = 2V_{CE} = 2 \times 7.5 = 15$ V.

Step 2: Find R_C and R_E:

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \quad \rightarrow \quad R_C + R_E = \frac{7.5}{2.5 \times 10^{-3}} = 3 \text{ k}\Omega$$

We are free to choose R_C and R_E (choice is usually set by the AC behavior which we will see later). We have to ensure, however, that $V_E = I_E R_E > 1$ V or $R_E > 1/I_E = 400\ \Omega$. Let's choose $R_E = 1$ kΩ and $R_C = 2$ kΩ for this example.

Step 3: Find R_B and V_{BB}: We need to set $R_B \ll \beta R_E$. As any commercial BJT has a range of β values and we want to ensure that the above inequality is always satisfied, we should use the minimum β value:

$$R_B \ll \beta_{min} R_E \quad \rightarrow \quad R_B = 0.1\beta_{min} R_E = 0.1 * 50 * 1,000 = 5 \text{ k}\Omega$$

$$V_{BB} \approx V_{BE} + I_E R_E = 0.7 + 2.5 \times 10^{-3} \times 10^3 = 3.2 \text{ V}$$

Step 4: Find R_1 and R_2

$$R_B = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} = 5 \text{ k}\Omega$$
$$\frac{V_{BB}}{V_{CC}} = \frac{R_2}{R_1 + R_2} = \frac{3.2}{15} = 0.21$$

The above are two equations in two unknowns (R_1 and R_2). The easiest way to solve these equations are to divide the two equations to find R_1 and use that in the equation for V_{BB}:

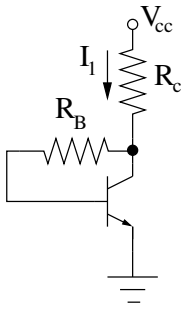
$$R_1 = \frac{5 \text{ k}\Omega}{0.21} = 24 \text{ k}\Omega$$
$$\frac{R_2}{R_1 + R_2} = 0.21 \quad \rightarrow \quad 0.79R_2 = 0.21R_1 \quad \rightarrow \quad R_2 = 6.4 \text{ k}\Omega$$

Reasonable commercial values for R_1 and R_2 are and 24 kΩ and 6.2 kΩ, respectively.

Other Biasing Schemes

As we will see later, value of $R_b = R_1 \parallel R_2$ appears in the formauls for the input resistance (and lower cut-off frequency) of amplifier configuration, greatly reducing the input resistance and increasing the value of the coupling capacitor. A simple, but effective alternative is to use the R_c as the feedback resistor.

We assume that the BJT is in active-linear regime. Since $I_B \ll I_C$, by KCL $I_1 = I_C + I_C \approx I_C$. Then:



BE-KVL: $V_{cc} = R_C I_C + R_B I_B + V_{BE}$

$$V_{cc} = (R_C + R_B/\beta)\, I_C + V_{BE}$$
$$I_C = \frac{V_{cc} - V_{BE}}{R_C + R_B/\beta}$$

If, $R_B/\beta \ll R_C$ or $R_B \ll \beta R_C$, we will have (setting $V_{BE} = V_\gamma$):

$$I_C = \frac{V_{cc} - V_\gamma}{R_C}$$

Since I_C is independent of β, the bias point is stable. We still need to prove that the BJT is in the active linear region. We write a KVL through BE and CE terminals:

$$V_{CE} = R_B I_B + V_{BE} = R_B I_B + V_\gamma > V_\gamma$$

Since $V_{CE} > V_\gamma$, BJT is indeed in active regime.

To see the negative feedback effect, rewrite BE-KVL as:

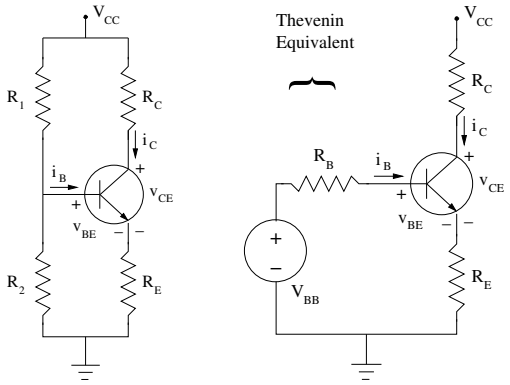
$$I_B = \frac{V_{cc} - V_\gamma - R_C I_C}{R_B}$$

Suppose the circuit is operating and BJT β is increased (*e.g.,* increase in temperature). In that case I_C will increase which raises the voltage across resistor R_C ($R_C I_C$). From the above equation, this will lead to a reduction in I_B which, in turn, will decrease $I_C = \beta I_B$ and compensate for any increase in β. If BJT β is decreased (*e.g.,* decrease in temperature), I_C will decrease which reduces the voltage across resistor R_C ($R_C I_C$). From the above equation, this will lead to an increase in I_B which, in turn, will increase $I_C = \beta I_B$ and compensate for any decrease in β.

Note: The drawback of this bias scheme is that the allowable AC signal on V_{CE} is small. Since $V_{CC} \pm \Delta V_{CC} > V_\gamma$ in order for the BJT to remain in active regime, we find the amplitude of AC signal, $\Delta V_{CC} < R_B I_B = (R_B/\beta) I_C$. Since, $R_B/\beta \ll R_C$ for bias stability thus, $\Delta V_{CC} \ll R_C I_C$. This is in contrast with the standard biasing with emitter resistor in which ΔV_{CC} is comparable to $R_C I_C$.

Other Biasing Schemes

We discussed using an emitter resistor to stabilize the bias point (Q point) of a BJT amplifier as is shown (R_c can be zero). There are two main issues associated with this bias configuration which may make it unsuitable for some applications.

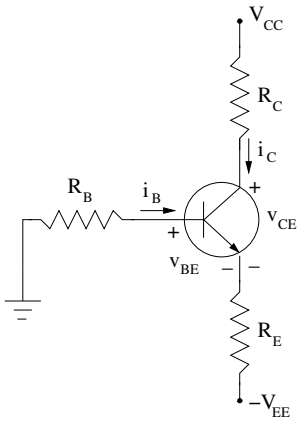


2) Because $V_B > 0$, a coupling capacitor is typically needed to attach the input signal to the amplifier circuit.
The combination of the coupling capacitor and the input resistance of the amplifier leads to a lower cut-off frequency for the amplifier as we discussed before, *i.e.,* this biasing scheme leads to an "AC" amplifier. In some applications, we need "DC" amplifiers. Biasing with two voltage sources, discussed below, will solve this problem.

3) Biasing with one voltage source requires 3 resistors (R_1, R_2, and R_E), a coupling capacitor, and possibly a by-pass capacitor. In integrated circuit chips, resistors and large capacitors take too much space. It is preferable to reduce their number as much as possible and replace their function with additional transistors. For IC applications, "current-mirrors" are usually used to bias the circuit as is discussed below.

Biasing with 2 Voltage Sources:

Consider the biasing scheme as is shown. This biasing scheme is similar to bias with one voltage source. Basically, we have assigned a voltage of $-V_{EE}$ to the ground (reference voltage) and chosen $V_{EE} = V_{BB}$. As such, all of the currents and voltages in the circuit should be identical to the bias with one power supply. We should find that this is a stable bias point as long as $R_B \ll \beta R_E$. This is shown below:



$$\text{BE-KVL:} \quad R_B I_B + V_{BE} + R_E I_E - V_{EE} = 0$$

$$I_E \approx I_C = \beta I_B$$

$$R_B \frac{I_E}{\beta} + R_E I_E = V_{EE} - V_{BE} \quad \rightarrow \quad I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

Similar to the bias with one power supply, if we choose R_B such that, $R_B \ll \beta R_E$, we get:

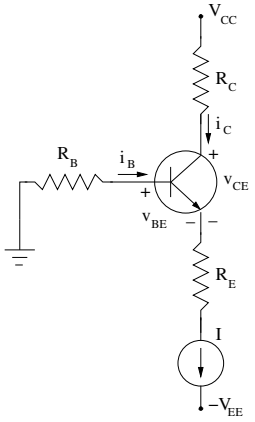
$$I_C \approx I_E \approx \frac{V_{EE} - V_{BE}}{R_E} = const$$

$$\text{CE-KVL:} \quad V_{CC} = R_C I_C + V_{CE} + R_E I_E - V_{EE}$$

$$V_{CE} = V_{CC} + V_{EE} - I_C(R_C + R_E) = const$$

Therefore, I_E, I_C, and V_{CE} will be independent of BJT parameters (*i.e.,* BJT β) and we have a stable bias point. Similar to stable bias with one power supply, we also need to ensure that $R_E I_E \geq 1$ V to account for small possible variation in V_{BE}.

Bias with two power supplies has certain advantages over biasing with one power supply, it has two resistors, R_B and R_E (as opposed to three), and in fact, in most applications, we can remove R_B altogether. In addition, in some configuration, we can directly couple the input signal to the amplifier without using a coupling capacitor (because $V_B \approx 0$). As such, such a configuration can also amplify "DC" signals.



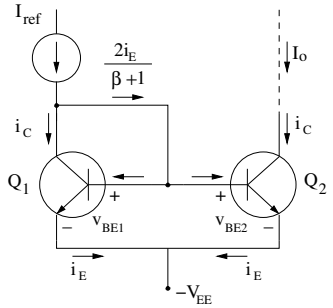
Both stable biasing schemes, with one or two power supplies, use R_E as a negative feedback to "fix" I_E and make it independent of BJT parameters. In effect, any biasing scheme which results in a constant I_E, independent of BJT parameters, will be a stable biasing technique.

Schematically, all these biasing schemes can be illustrated with an ideal current source in the emitter circuit as is shown. For the circuits which include a current source, resistor R_E is NOT needed for stable biasing anymore. For example, R_E can be removed from common emit tor amplifiers with bypass capacitors.

Because of elimination of R_B and R_E (or reducing R_E), biasing with a current source is the preferred way in most integrated circuits. Such a biasing can be achieved with a current mirror circuit.

Biasing in ICs: Current Mirrors

A large family of BJT circuit, including current mirrors, differential amplifiers, and emitter-coupled logic circuits include identical BJT pairs. In most cases, two identical BJTs are manufactured together on one chip in order to ensure that their parameters are approximately equal (Note that if you take two commercial BJTs, *e.g.,* two 2N3904, there is no guaranty that $\beta_1 = \beta_2$, while if they are grown together on a chip, $\beta_1 \approx \beta_2$. For our analysis, we assume that both BJTs are identical.)



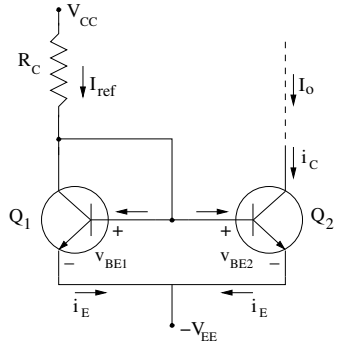
Consider the circuit shown with identical transistors, Q_1 and Q_2. Because both bases and emitters of the transistors are connected together, KVL leads to $v_{BE1} = v_{BE2}$. As we discussed before, BJT operation is controlled by v_{BE}. As $v_{BE1} = v_{BE2}$ and transistors are identical, they should have similar i_E, i_B and i_c:

$$i_B = \frac{i_E}{\beta+1} \qquad I_o = i_c = \frac{\beta i_E}{\beta+1}$$

KCL: $$I_{ref} = i_c + \frac{2i_E}{\beta+1} = \frac{i_E}{\beta+1} + \frac{2i_E}{\beta+1} = \frac{\beta+2}{\beta+1}\, i_E$$

$$\frac{I_o}{I_{ref}} = \frac{\beta}{\beta+2} = \frac{1}{1+2/\beta}$$

(We have used $i_C = \beta i_B$ and $i_E = (\beta+1) i_B$ to illustrate impact of β.) For $\beta \gg 1$, $I_o \approx I_{ref}$ (with an accurancy of $2/\beta$). This circuit is called a "current mirror" as the two transistors work in tandem to ensure that current I_o remains the same as I_{ref} no matter what circuit is attached to the collector of Q_2. As such, the circuit behaves as a current source and can be used to bias BJT circuits.

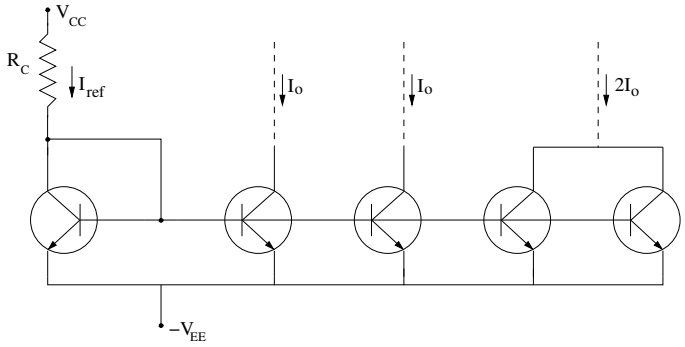


Value of I_{ref} can be set in many ways. The simplest is by using a resistor R_c as is shown. By KVL, we have:

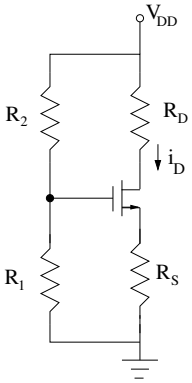
$$V_{CC} = R_C I_{ref} + v_{BE1} - V_{EE}$$
$$I_{ref} = \frac{V_{CC} + V_{EE} - v_{BE1}}{R_C} = const$$

Current mirror circuits are widely used for biasing BJTs. In the simple current mirror circuit above, $I_o = I_{ref}$ with a relative accuracy of $2/\beta$ and I_{ref} is constant with an accuracy of small changes in v_{BE1}. Variation of current mirror circuit, such as Wilson current mirror and Widlar current mirror (See Sedra and Smith) are available that lead to $I_o = I_{ref}$ with a higher accuracy and compensate for $2/\beta$ and changes in v_{BE} effects. Wilson mirror is especially popular because it replace R_c with a transistor.

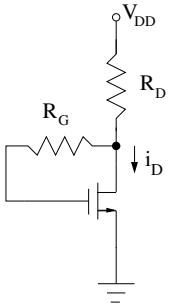
The right hand part of the current mirror circuit can be duplicated such that one current mirror circuit can bias several BJT circuits as is shown. In fact, by coupling output of two of the right hand parts, integer multiples of I_{ref} can be made for biasing circuits which require a higher bias current.



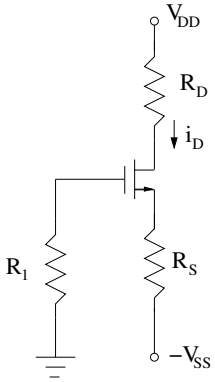
Biasing FETs: Bias circuits for FET amplifiers are similar to BJT circuits. Some examples are shown in below. (**Exercise** Find the bias point of the FET in each of the circuits below.)



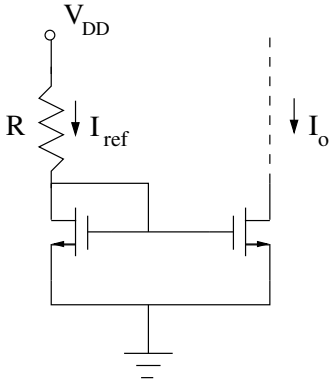
Standard Bias



Bias through R_D



Bias with 2 power supplies

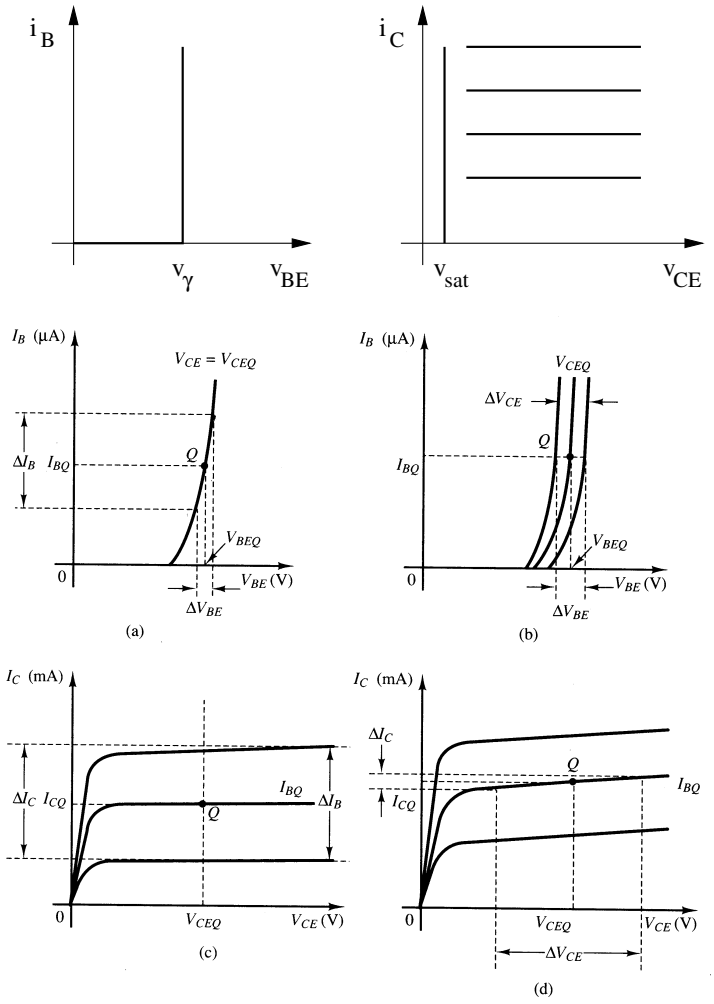


FET Current Mirror

BJT Small Signal Model and AC amplifiers

We calculated the DC behavior of the BJT (DC biasing) with a simple large-signal model as shown. In active-linear region, this model is simply: $v_{BE} = 0.7$ V, $i_C = \beta i_B$. This model is sufficient for calculating the Q point as we are only interested in ensuring sufficient design space for the amplifier, *i.e.,* Q point should be in the middle of the load line in the active linear region. In fact, for our good biasing scheme with negative feedback, the Q point location is independent of BJT parameters. (and, therefore, independent of model used!)

A comparison of the simple model with the iv characteristics of the BJT shows that our simple large-signal model is very crude and is not accurate for AC analysis.



For example, the input AC signal results in small changes in v_{BE} around 0.7 V (Q point) and corresponding changes in i_B. The simple model cannot be used to calculate these changes (It assumes v_{BE} is constant!). Also for a fixed i_B, i_C is not exactly constant as is assumed in the simple model (see i_C vs v_{CE} graphs). As a whole, the simple large signal model is not sufficient to describe the AC behavior of BJT amplifiers where more accurate representations of the amplifier gain, input and output resistance, *etc.* are needed.

A more accurate, but still linear, model can be developed by assuming that the changes in transistor voltages and currents due to the AC signal are small compared to corresponding Q-point values and using a Taylor series expansion. Consider function $f(x)$. Suppose we know the value of the function and all of its derivative at some known point, x_0. Then, value

of the function in the neighborhood of x_0 can be found from the Taylor Series expansion as:

$$f(x_0+\Delta x) = f(x_0) + \Delta x \left.\frac{df}{dx}\right|_{x=x_0} + \frac{(\Delta x)^2}{2}\left.\frac{d^2f}{dx^2}\right|_{x=x_0} + ...$$

Close to our original point of x_0, Δx is small and the high order terms of this expansion (terms with $(\Delta x)^n,\ n=2,3,...$) usually become very small. Typically, we consider only the first order term, *i.e.,*

$$f(x_0+\Delta x) \approx f(x_0) + \Delta x \left.\frac{df}{dx}\right|_{x=x_0}$$

The Taylor series expansion can be similarly applied to function of two or more variables such as $f(x,y)$:

$$f(x_0+\Delta x, y_0+\Delta y) \approx f(x_0,y_0) + \Delta x \left.\frac{\partial f}{\partial x}\right|_{x_0,y_0} + \Delta y \left.\frac{\partial f}{\partial y}\right|_{x_0,y_0}$$

In a BJT, there are four parameters of interest: i_B, i_C, v_{BE}, and v_{CE}. The BJT *iv* characteristics plots, specify two of the above parameters, v_{BE} and i_C in terms of the other two, i_B and v_{CE}, *i.e.,* v_{BE} is a function of i_B and v_{CE} (written as $v_{BE}(i_B, v_{CE})$ similar to $f(x,y)$) and i_C is a function of i_B and v_{CE}, $i_C(i_B, v_{CE})$.

Let's assume that BJT is biased and the Q point parameters are I_B, I_C, V_{BE} and V_{CE}. We now apply a small AC signal to the BJT. This small AC signal changes v_{CE} and i_B by small values around the Q point:

$$i_B = I_B + \Delta i_B \qquad v_{CE} = V_{CE} + \Delta v_{CE}$$

The AC changes, Δi_B and Δv_{CE} results in AC changes in v_{BE} and i_C that can be found from Taylor series expansion in the neighborhood of the Q point, similar to expansion of $f(x_0+\Delta x, y_0+\Delta y)$ above:

$$v_{BE}(I_B+\Delta i_B, V_{CE}+\Delta v_{CE}) = V_{BE} + \left.\frac{\partial v_{BE}}{\partial i_B}\right|_Q \Delta i_B + \left.\frac{\partial v_{BE}}{\partial v_{CE}}\right|_Q \Delta v_{CE}$$

$$i_C(I_B+\Delta i_B, V_{CE}+\Delta v_{CE}) = I_C + \left.\frac{\partial i_C}{\partial i_B}\right|_Q \Delta i_B + \left.\frac{\partial i_C}{\partial v_{CE}}\right|_Q \Delta v_{CE}$$

where all partial derivatives are calculated at the Q point and we have noted that at the Q point, $v_{BE}(I_B, V_{CE}) = V_{BE}$ and $i_C(I_B, V_{CE}) = I_C$. We can denote the AC changes in v_{BE} and i_C as Δv_{BE} and Δi_C, respectively:

$$v_{BE}(I_B + \Delta i_B, V_{CE} + \Delta v_{CE}) = V_{BE} + \Delta v_{BE}$$
$$i_C(I_B + \Delta i_B, V_{CE} + \Delta v_{CE}) = I_C + \Delta i_C$$

So, by applying a small AC signal, we have changed i_B and v_{CE} by small amounts, Δi_B and Δv_{CE}, and BJT has responded by changing , v_{BE} and i_C by small AC amounts, Δv_{BE} and Δi_C. From the above two sets of equations we can find the BJT response to AC signals:

$$\Delta v_{BE} = \frac{\partial v_{BE}}{\partial i_B}\Delta i_B + \frac{\partial v_{BE}}{\partial v_{CE}}\Delta v_{CE}, \qquad \Delta i_C = \frac{\partial i_C}{\partial i_B}\Delta i_B + \frac{\partial i_C}{\partial v_{CE}}\Delta v_{CE}$$

where the partial derivatives are the slope of the iv curves near the Q point. We define

$$h_{ie} \equiv \frac{\partial v_{BE}}{\partial i_B}, \qquad h_{re} \equiv \frac{\partial v_{BE}}{\partial v_{CE}}, \qquad h_{fe} \equiv \frac{\partial i_C}{\partial i_B}, \qquad h_{oe} \equiv \frac{\partial i_C}{\partial v_{CE}}$$

Thus, response of BJT to small signals can be written as:

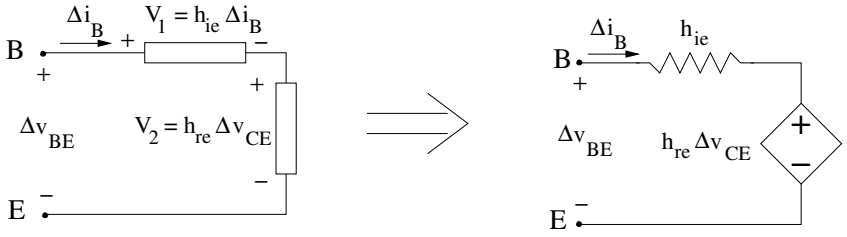
$$\Delta v_{BE} = h_{ie}\Delta i_B + h_{re}\Delta v_{CE} \qquad \Delta i_C = h_{fe}\Delta i_B + h_{oe}\Delta v_{CE}$$

which is our small-signal model for BJT.

We now need to relate the above analytical model to circuit elements so that we can solve BJT circuits. Consider the expression for Δv_{BE}

$$\Delta v_{BE} = h_{ie}\Delta i_B + h_{re}\Delta v_{CE}$$

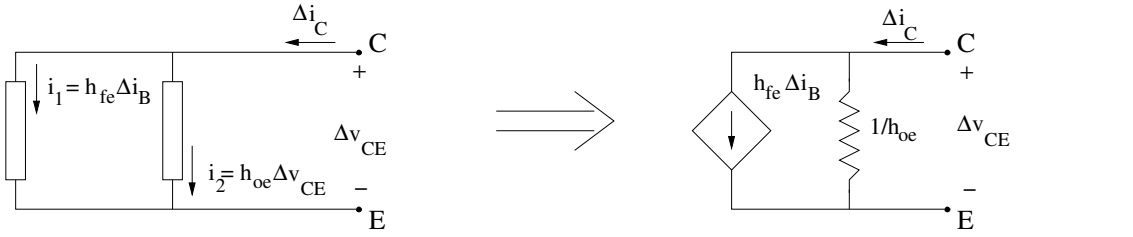
Each term on the right hand side should have units of Volts. Thus, h_{ie} should have units of resistance and h_{re} should have no units (these are consistent with the definitions of h_{ie} and h_{re}.) Furthermore, the above equation is like a KVL: the voltage drop between base and emitter is written as sum of voltage drops across two elements. The voltage drop across the first element is $h_{ie}\Delta i_B$. So, it is resistor with a value of h_{ie}. The voltage drop across the second element is $h_{re}\Delta v_{CE}$. Thus, it is dependent voltage source.



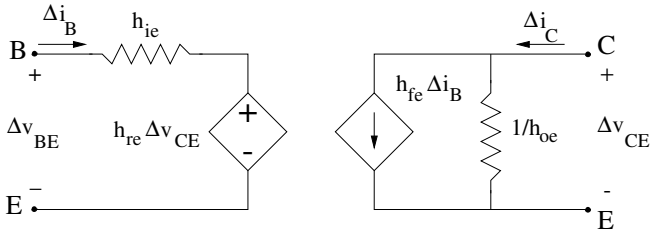
Now consider the expression for Δi_C:

$$\Delta i_C = h_{fe}\Delta i_B + h_{oe}\Delta v_{CE}$$

Each term on the right hand side should have units of Amperes. Thus, h_{fe} should have no units and h_{oe} should have units of conductance (these are consistent with the definitions of h_{oe} and h_{fe}.) Furthermore, the above equation is like a KCL: the collector current is written as sum of two currents. The current in first element is $h_{fe}\Delta i_B$. So, it is dependent current source. The current in the second element is proportional to $h_{oe}/\Delta v_{CE}$. So it is a resistor with the value of $1/h_{oe}$.



Now, if put the models for BE and CE terminals together we arrive at the small signal "hybrid" model for BJT. It is similar to the hybrid model for a two-port network (Carlson Chap. 14).



The small-signal model is mathematically valid only for signals with small amplitude. But the model is so useful that is often used for sinusoidal signals with amplitudes approaching those of Q-point parameters by using average values of "h" parameters. "h" parameters are given in manufacturer's spec sheets for each BJT. It should not be surprising to note that even in a given BJT, "h" parameter can vary substantially depending on manufacturing statistics, operating temperature, *etc.* Manufacturer's' spec sheets list these "h" parameters and give the minimum and maximum values. Traditionally, the geometric mean of the minimum and maximum values are used as the average value in design (see table).

Since $h_{fe} = \partial i_C/\partial i_B$, BJT $\beta = i_C/i_B$ is sometimes called h_{FE} in manufacturers' spec sheets and has a value quite close to h_{fe}. In most electronic text books, β, h_{FE} and h_{fe} are used interchangeably.

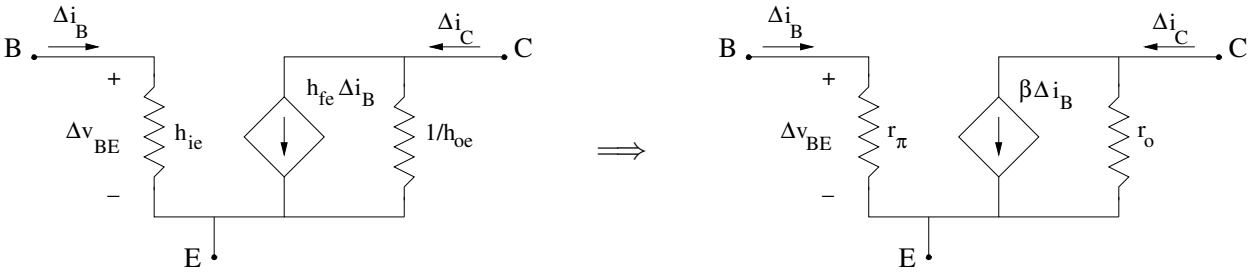
Typical hybrid parameters of a general-purpose 2N3904 NPN BJT

	Minimum	Maximum	Average*
$r_\pi = h_{ie}$ (kΩ)	1	10	3
h_{re}	0.5×10^{-4}	8×10^{-4}	2×10^{-4}
$\beta \approx h_{fe}$	100	400	200
h_{oe} (μS)	1	40	6
$r_o = 1/h_{oe}$ (kΩ)	25	1,000	150
$r_e = h_{ie}/h_{fe}$ (Ω)	10	25	15

* Geometric mean.

As h_{re} is small, it is usually ignored in analytical calculations as it makes analysis much simpler. This model, called the hybrid-π model, is most often used in analyzing BJT circuits. In order to distinguish this model from the hybrid model, most electronic text books use a different notation for various elements of the hybrid-π model:

$$r_\pi = h_{ie} \qquad r_o = \frac{1}{h_{oe}} \qquad \beta = h_{fe}$$

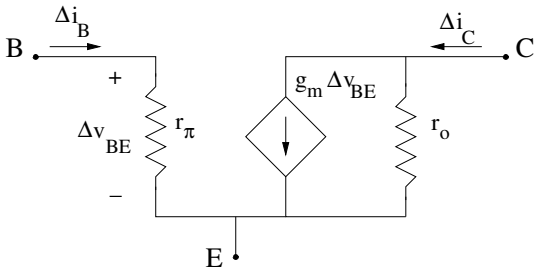


The above hybrid-π model includes a current-controlled current source. This implies that BJT behavior is controlled by i_B. In reality, v_{BE} controls the BJT behavior. A variant of the hybrid-π model can be developed which includes a voltage-controlled current source. This can be achieved by noting it the above model that $\Delta v_{BE} = h_{ie}\Delta i_B$ and

$$h_{fe}\Delta i_B = h_{fe}\frac{\Delta v_{BE}}{h_{ie}} = g_m \Delta v_{BE}$$

$$g_m \equiv \frac{h_{fe}}{h_{ie}} \qquad \text{Transfer conductance}$$

$$r_e \equiv \frac{1}{g_m} = \frac{h_{ie}}{h_{fe}} \qquad \text{Emitter resistance}$$



FET Small Signal Model and AC amplifiers

Similar to BJT, the simple large-signal model of FET (page 94) is sufficient for finding the bias point; but we need to develop a more accurate model for analysis of AC signals. The main issue is that the FET large signal model indicates that i_D only depends on v_{GS} and is independent of v_{DS} in the active region. In reality, i_D increases slightly with v_{DS} in the active region.

We can develop a small signal model for FET in a manner similar to the procedure described in detail for the BJT. The FET characteristics equations specify two of the FET parameters, i_G and i_D, in terms of the other two, v_{GS} and v_{DS}. (Actually FET is simpler than BJT as $i_G = 0$ at all times.) As before, we write the FET parameters as a sum of DC bias value and a small AC signal, *e.g.,* $i_D = I_D + \Delta i_D$. Performing a Taylor series expansion, similar to pages 118 and 119, we get:

$$i_G(V_{GS} + \Delta v_{GS}, V_{DS} + \Delta v_{DS}) = 0$$

$$i_D(V_{GS} + \Delta v_{GS}, V_{DS} + \Delta v_{DS}) = i_D(V_{GS}, V_{DS}) + \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q \Delta v_{GS} + \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q \Delta v_{DS}$$

Since $i_G(V_{GS}+\Delta v_{GS}, V_{DS}+\Delta v_{DS}) = I_G+\Delta i_G$ and $i_D(V_{GS}+\Delta v_{GS}, V_{DS}+\Delta v_{DS}) = I_D+\Delta i_D$, we find the AC components to be:

$$\Delta i_G = 0 \qquad \text{and} \qquad \Delta i_D = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q \Delta v_{GS} + \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q \Delta v_{DS}$$

Defining

$$g_m \equiv \frac{\partial i_D}{\partial v_{GS}} \qquad \text{and} \qquad r_o \equiv \frac{\partial i_D}{\partial v_{DS}}$$

We get:

$$\Delta i_G = 0 \qquad \text{and} \qquad \Delta i_D = g_m \Delta v_{GS} + r_o \Delta v_{DS}$$

This results in the hybrid-π model for the FET as is shown. Note that the FET hybrid-π model is similar to the BJT hybrid-π model with $r_\pi \to \infty$.