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On the design partitioning of 3D monolithic circuits

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ON THE DESIGN PARTITIONING OF 3D MONOLITHIC CIRCUITS

by

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ABSTRACT

Conventional three-dimensional integrated circuits (3D ICs) stack multiple dies vertically for higher integration density, shorter wirelength, smaller footprint, faster speed and lower power consumption. Due to the large through-silicon-via (TSV) sizes, 3D design partitioning is typically done at the architecture-level With the emerging monolithic 3D technology, TSVs can be made much smaller, which enables potential block-level partitioning. However, it is still unclear how much benefit can be obtained by block-level partitioning, which is affected by the number of tiers and the sizes of TSVs. In this thesis, an 8-bit ripple carry adder was used as an example to explore the impact of TSV size and tier number on various tradeoffs between power, delay, footprint and noise. With TSMC 0.18um technology, the study indicates that when the TSV size is below 100nm, it can be beneficial to perform block-level partitioning for smaller footprint with minimum power, delay and noise overhead.

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1. INTRODUCTION

While the semiconductor industry is making every effort to make chips smaller and faster, further scaling of the current 22nm technology has become prohibitively expensive. Accordingly, there has been a groundswell of interest in technologies that offer a path beyond the limits of device scaling. Among all the possible alternatives, the 3D IC is generally considered to be the most promising one, at least in the next decade, for its compatibility with the current technology. Instead of making transistors smaller, it makes use of the vertical dimension for higher integration density, shorter wirelength, smaller footprint, higher speed and lower power consumption. A critical enabling technique in 3D ICs is the TSV, which forms vertical signal, power and thermal paths. Depending on the methods to build chips vertically, there are in general two types of 3D ICs: die stacking and monolithic integration.

Die stacking simply stacks multiple two-dimensional dies fabricated through conventional processes. Despite its full compatibility with existing technologies, due to technology constraints, TSVs in die stacking have to be made large in size (typically 5-50um), which are 5-10x the sizes of standard cells in 32mn technology. This ratio is predicted to increase drastically with the technology scaling in the future by International Technology Roadmap for Semiconductors (ITRS) [1]. The large TSV-to-cell ratio significantly cuts down the benefit that can be achieved by 3D integration. Another issue related to die stacking is heat dissipation. Stacked dies result in higher power density, yet the underfill between adjacent tiers generally has very low thermal conductivity, making vertical heat dissipation a severe problem. Those two issues significantly limit the application of 3D ICs.

Alternatively, monolithic 3D integration involves the direct construction of multiple device layers with ultra-dense vertical connectivity. The biggest advantage of monolithic integration is the miniaturization of TSVs, which can be smaller than 50nm. These high vertical connection densities result in a large number of wires routed in the third dimension, thereby reducing average wirelength. This, in turn, reduces the chip footprint and power. In addition, extremely high bandwidth can be achieved for communication between different tiers. Furthermore, without underfill, much better heat dissipation is achieved. While monolithic 3D ICs can bring significant benefits, they have not been widely adopted in industry so far due to the big challenge in its fabrication process.

Recently, MonolithIC 3D Inc. announced several techniques that leverage an innovative memory technology to fabricate monolithic 3D ICs. They pave the road for large volume production with low cost.

Despite the technology readiness, however, no systematic design flow is available for monolithic 3D designs as of today. Most existing 3D design tools target at die stacking based integration: they partition the design into multiple tiers at architecture level (e.g. memory on logic) during design planning stage, and then apply 2D design flows to handle each tier. While they work fine for die stacking based 3D ICs where TSVs are large in size, they cannot make full use of monolithic 3D integration.

Specifically, TSV miniaturization suggests a possible design paradigm shift, from the current architecture level 3D partition to a potential block level partition for more footprint reduction and performance enhancement. However it is still not clear, in general, what are the tradeoffs in terms of power, delay, noise and footprint if a

functional block is implemented in 3D, and how such tradeoffs are affected by the TSV size and number of tiers. The tradeoffs will eventually decide whether an architecture-level or a block-level 3D partitioning should be adopted. The impact of TSV size and tier number on wirelength and footprint has been studied in literature [24], but only for large-scale circuit placement. The conclusions do not apply to block-level implementation.

In this thesis, an 8-bit ripple carry adder will be used as an example and implement it in 2D and 3D with 2, 3, and 4 tiers. For the 3D designs, the TSV diameter was swept from 50nm to 5um and simulate the designs for power, footprint, delay and noise. Many interesting conclusions are drawn based on the data obtained. Specifically, our preliminary study convincingly demonstrates that when the TSV size is smaller than 100nm, it is indeed beneficial to partition functional blocks in monolithic 3D ICs, as the footprint can be significantly reduced with minimum power, delay and noise overhead.

This thesis is organized as follows. In Section 1, background is given concerning TSVs, what they are, how they are crafted, and other such details. In Section 2, a comprehensive literature review is provided. Section 3 explains the motivation of our work, and Section 4 presents the results on an 8-bit ripple carry adder. Concluding remarks are given in Section 5.

2. LITERATURE REVIEW

According to the International Technology Road for Semiconductors (ITRS) [1], the device feature size is predicted to be 16nm by year 2018. However, the cost associated with the aggressive device scaling also increases drastically.

P. Batude et al. [9] shows that 3D process integration improves density and performance. This work states that the 3D integration technique proposed improves density by 30%. P. Batude et al. [8] goes further to show that the 3D integration can improve gate stack and inter-layer dielectric thickness properties. [7], another work by P. Batude et al. shows that, as technology gets below 22nm, it becomes beneficial to use 3D integration. It is also shown that the top layer can be made without any sheet resistance degradation of the bottom layer. In [3], by P. Batude et al, a 3D monolithic TSV integration method is discussed at length. Figure 2.1 shows the process proposed by which monolithic TSVs are laid out on wafer, and a circuit is crafted using this new technology. It then goes on to show two such circuits that were created using this design process, namely, an inverter, and an SRAM unit.

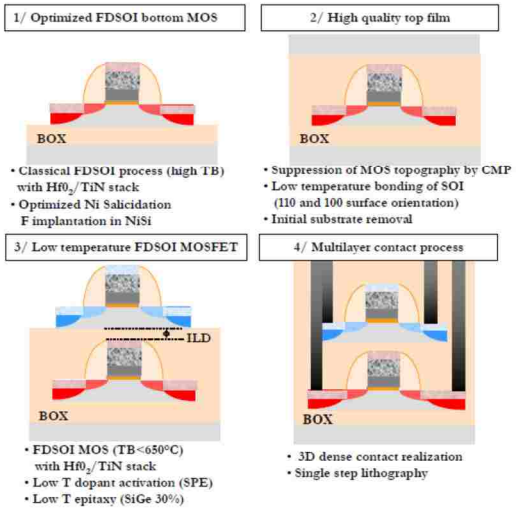


Figure 2.1. Monolithic TSV Integration Design Flow[3]

In [4], S. Wong et al. shows how an FPGA is crafted using the monolithic TSV. They show that the increase in complexity is not as much of a factor as the footprint

and critical path reduction. The benefits of 3D IC and the feasibility of its design were shown by P. Coudrain et al. [5] through the use of submicron pixel creation. According to this work, the 3D approach will increase the photodiode area by 44%. This paper uses a low temperature approach to maintain stability of the lowest layers. [6], also by P. Coudrain et al. seeks to further improve on the idea begun in [5], this time with higher temperatures, direct bonding on SOI, and lower noise margins. In [10] by N. Golshami et al, a fabrication case study was done using 6T SRAM cells and a photodiode array with monolithic TSV. O. Thomas et al[11] shows another case study that shows the potential of monolithic TSV in a 6T SRAM cell. It shows a 20% area improvement.

J. Davis et al[14] brings up all the problems faced by sub-50nm 2D technology such as crosstalk and quantum phenomena, and again iterates that 3D is the way to go and that for the 50nm technologies, a 145% interconnect performance jump happens with the inclusion of TSV.

A method for determining density and size of TSVs was proposed by D. H. Kim and S. K. Lim [16]. This work also shows that there is an upper bound to how many TSVs can be placed in a design and also goes on to explain that 3D may not always shorten the wirelength. It all depends on the technology and the size of the TSV.
In [23], by J. Cong and G. Luo, a systematic design flow for 3D circuits is proposed called 3D-Craft. The idea proposed in [12] by Hai Wei et al. uses carbon nanotubes and carbon nanotube FETs instead of CMOS (or similar to CMOS) to do monolithic integration. This has the benefit of lower process temperatures. Y. T. Lin et al[13] seems to claim that reducing the interlayer dielectric oxide thickness can dramatically lower the

recrystallization temperature to help with keeping the substrate intact after the laser is used to drill the TSV hole.

In [17] by Z. Or-Bach et al, two methods for monolithic fab are proposed, one which allows for higher density, shown in Figure 2.2, which involves using Recessed Channel Transistors (RCATs) which can be fabricated at low temperature. The other achieves fabrication at a low temperature, and without much masking difference using State of the Art (SOA) transistors with a replacement gate process is shown in Figure 2.3.

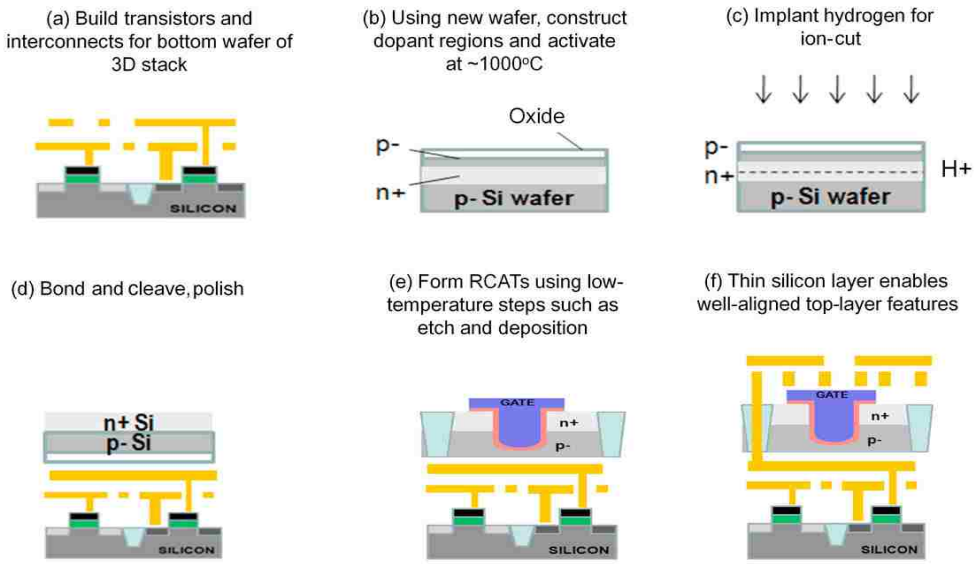


Figure 2.2. Transistor Cover Above Copper Interconnects at < 400°C [17]

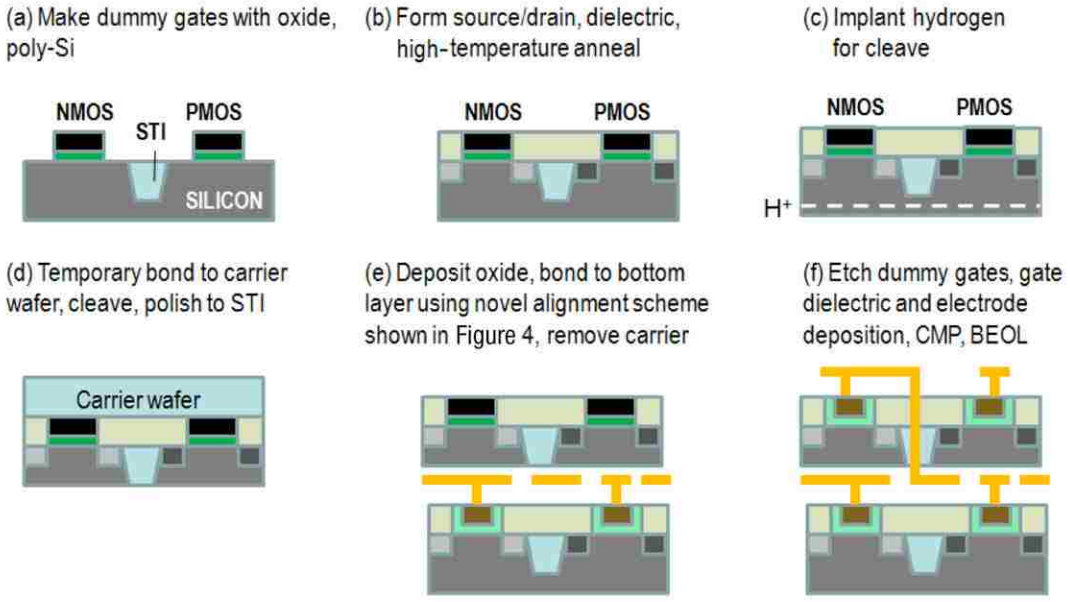
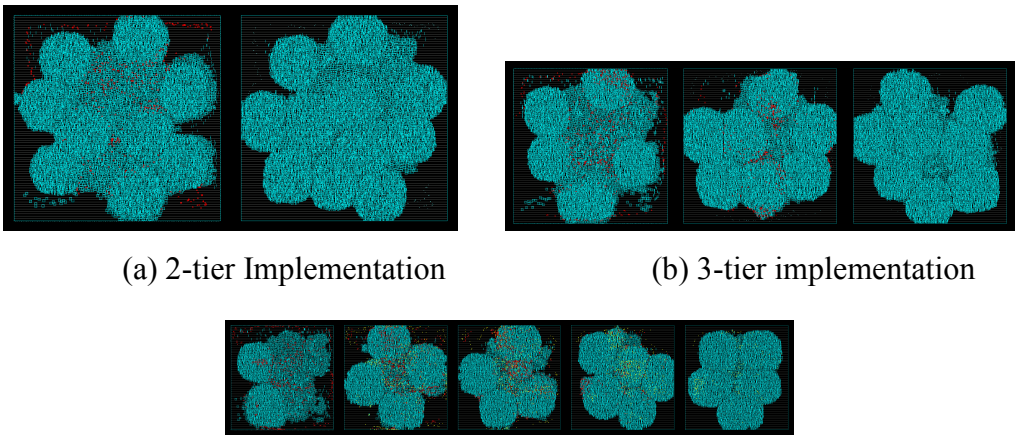


Figure 2.3. State-of-the-Art (SOA) Replacement-Gate Transistor Stacking[17]

3. IMPACT OF TSV SIZE ON DESIGN PARTITIONING

As suggested by several researchers[5-13], a direct impact of miniaturization of TSV is the wirelength and footprint reduction. In addition, another advantage brought by the block level partition is the hierarchical uniformity. As pointed out in [24], in conventional design flows where only architecture level partitioning is allowed, the physical hierarchy does not always follow the logic hierarchy, where the logic hierarchy is the hierarchy of logic modules written by the front-end designers, and the physical hierarchy is the physical proximity of the placeable objects viewed in a top-down fashion by the back-end chip architects. As such, if the design is planned strictly following the logic hierarchy, the planning result is usually suboptimal, because a logic module does not necessarily form a physical cluster of placeable objects in the physical hierarchy. Yet this problem does not exist in monolithic 3D integration: with block level partitioning, the two hierarchies can be unified. To verify this, 3D Craft [23] was used to study the wirelength and footprint comparison for the AES_DES circuit from the IWLS benchmarks. The circuit contains 388 I/O pads, 30K standard cells, and 30K nets. The design was partitioned at block level into 2, 3 and 5 tiers, with various TSV diameters.

With such partition, logic blocks are allowed to spread on multiple tiers. The results are shown in Figures 3.1, 3.2, and 3.3. From the figures two observations can be made: First, both footprint and wirelength reduce rapidly with the decrease of TSV size. Second, only when the TSV diameter is below 1um is there significant improvement over 2D implementation (1-tier), which directly explains why die stacking based 3D integration today does not adopt such partitions. Note that similar results are also reported in [25].



(a) 2-tier Implementation (b) 3-tier implementation

(c) 5-tier implementation

Figure 3.1. Different Implementations of AES_DES (with 1um TSV Diameter)

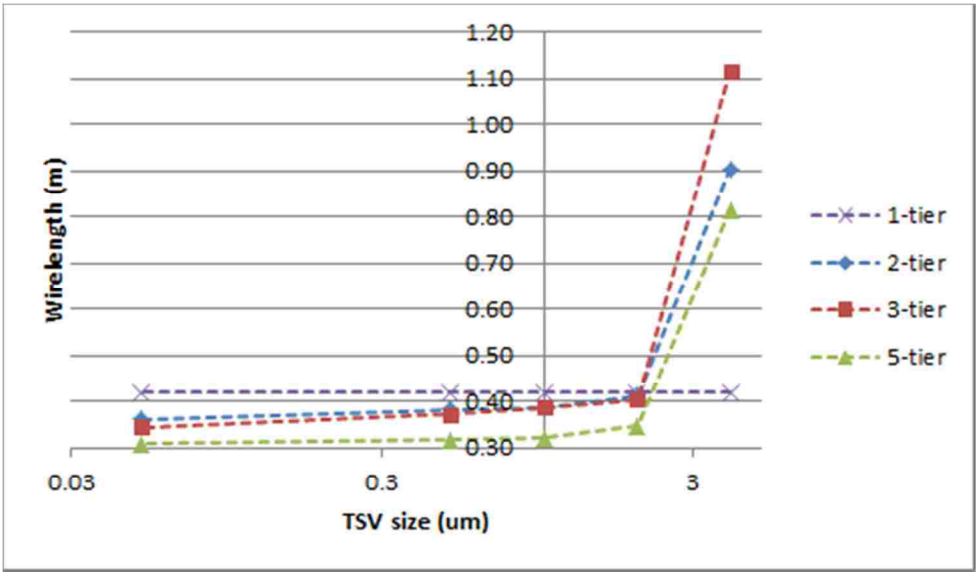


Figure 3.2. Wirelength w.r.t. TSV Diameters

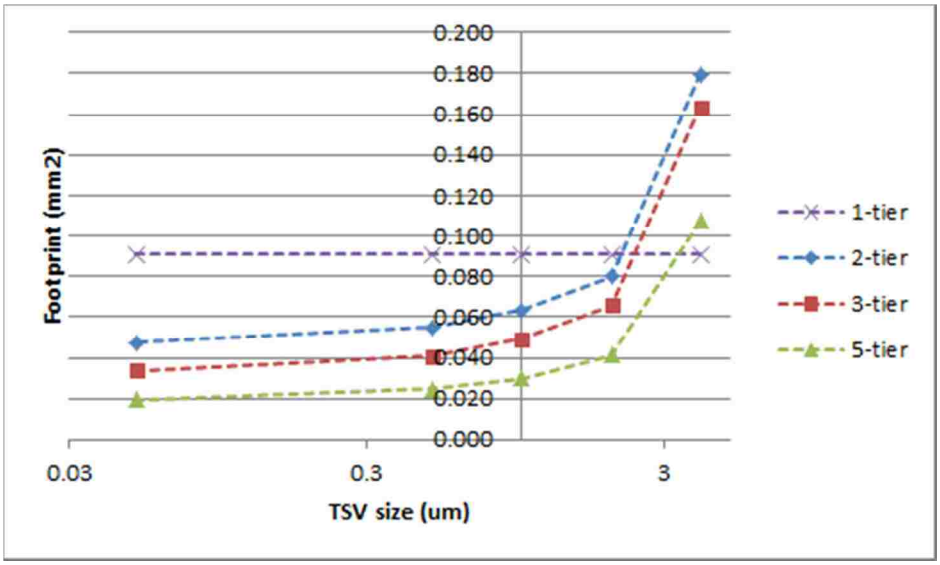


Figure 3.3. Footprint w.r.t. TSV Diameters

4. A CASE STUDY ON AN 8 BIT RIPPLE CARRY ADDER

An 8-bit ripple carry adder was used to study the tradeoffs between delay, footprint, power and noise for block-level partitioning, and how they would be affected by the TSV size and the number of tiers. The fast transmission-gate full adder (TGA) structure, as described in [20] and shown in Figure 4.1, was used to build each single-bit adder. The layout for this design is shown in Figure 4.2. For comparison, four different versions of the design were implemented: a conventional 2D design, two-tier, three-tier and four-tier designs. There are a total of 4 symbols used pictured in Figure 4.3. (a) is the adder, which has already been explained. (b) is the through silicon via which is presented in [20] and whose schematic is shown in Figure 4.4. Note that the TSV described in [20] is for two signals and the one depicted is for three. The major difference is the center. The resistance and inductance connected to SigIn and SigOut and the capacitors connected to the center are all divided by four instead of by two. (c) and (d) are both RC circuits. (d) represents the RC values for the wires in-between two adders on the same tier. (c) is equivalent to the RC values of the wire between the TSV and the tiers. A table in Appendix A will show the values for (c and d) and explain how they were calculated, and Appendix B will show the RLC values used in Figure 4.4.

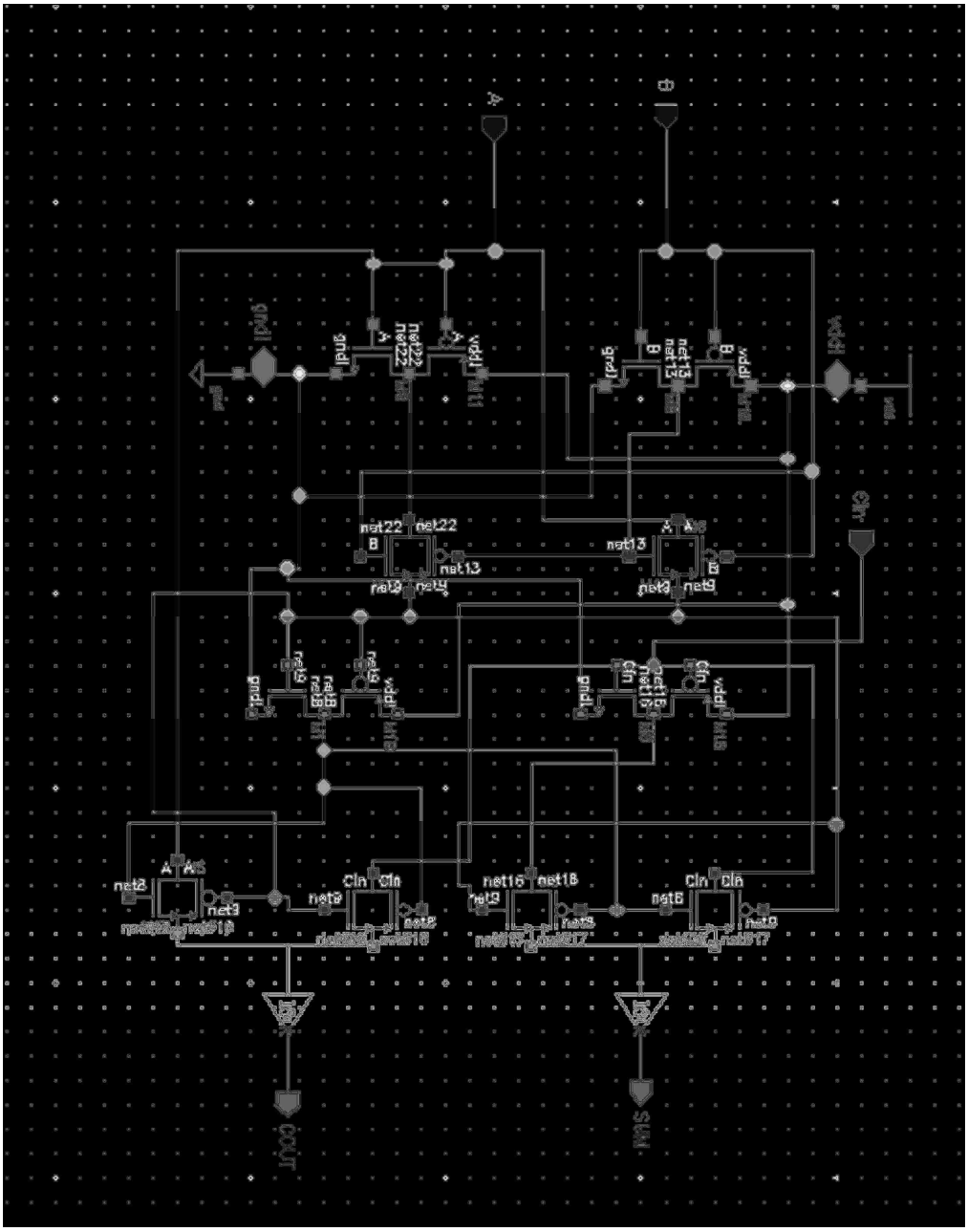


Figure 4.1. TGA Full Adder Schematic

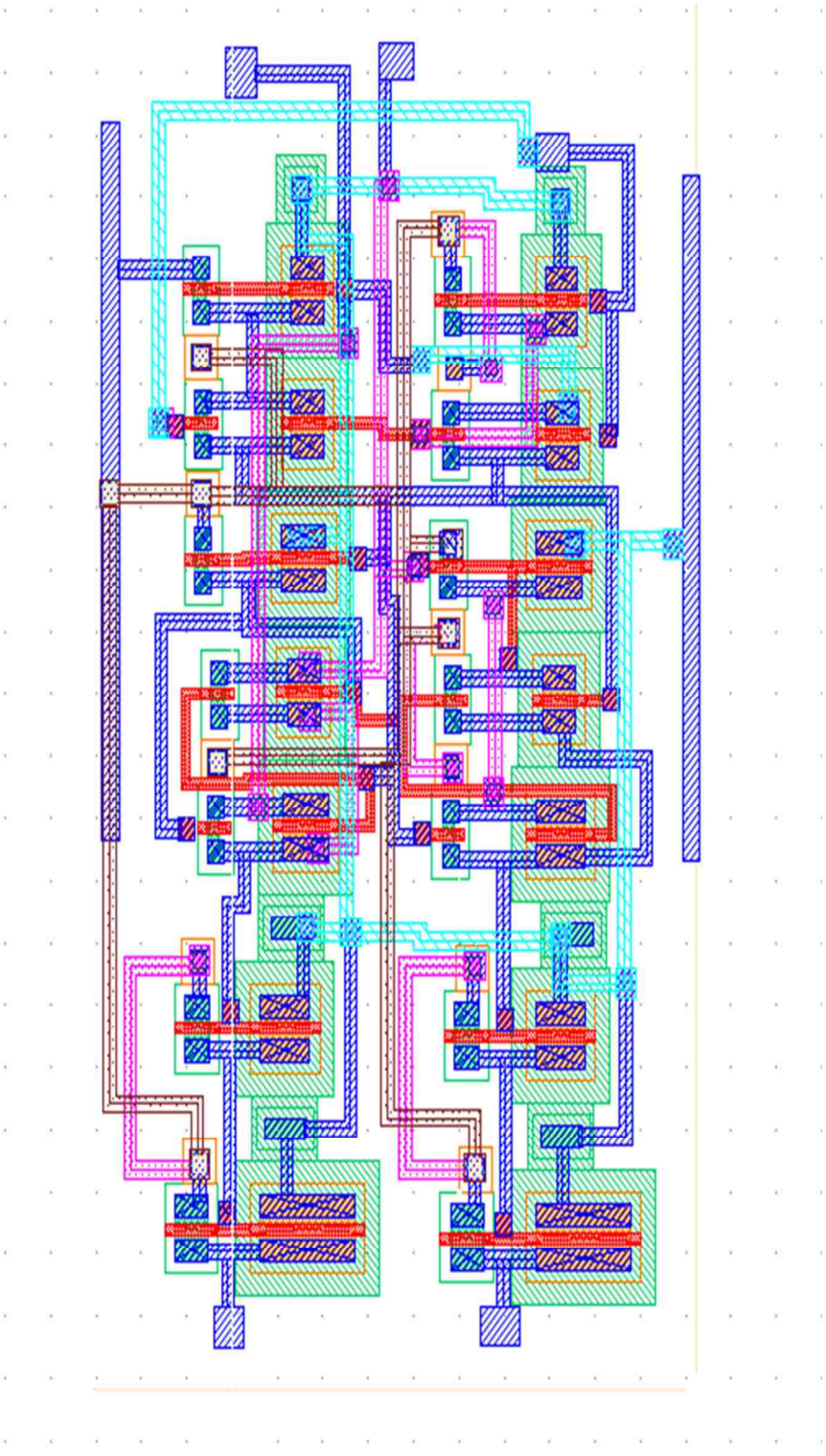


Figure 4.2. TGA Full Adder Layout

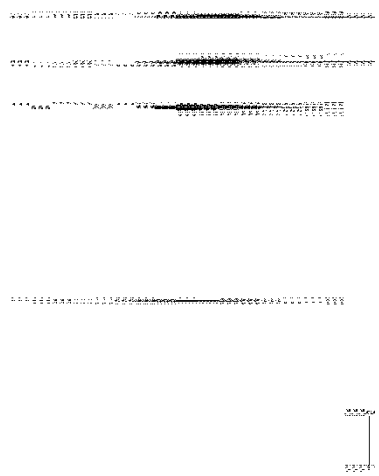


Figure 4.3. Symbols (a) Full Adder (b) TSV (c) RC-2 (d) RC-1

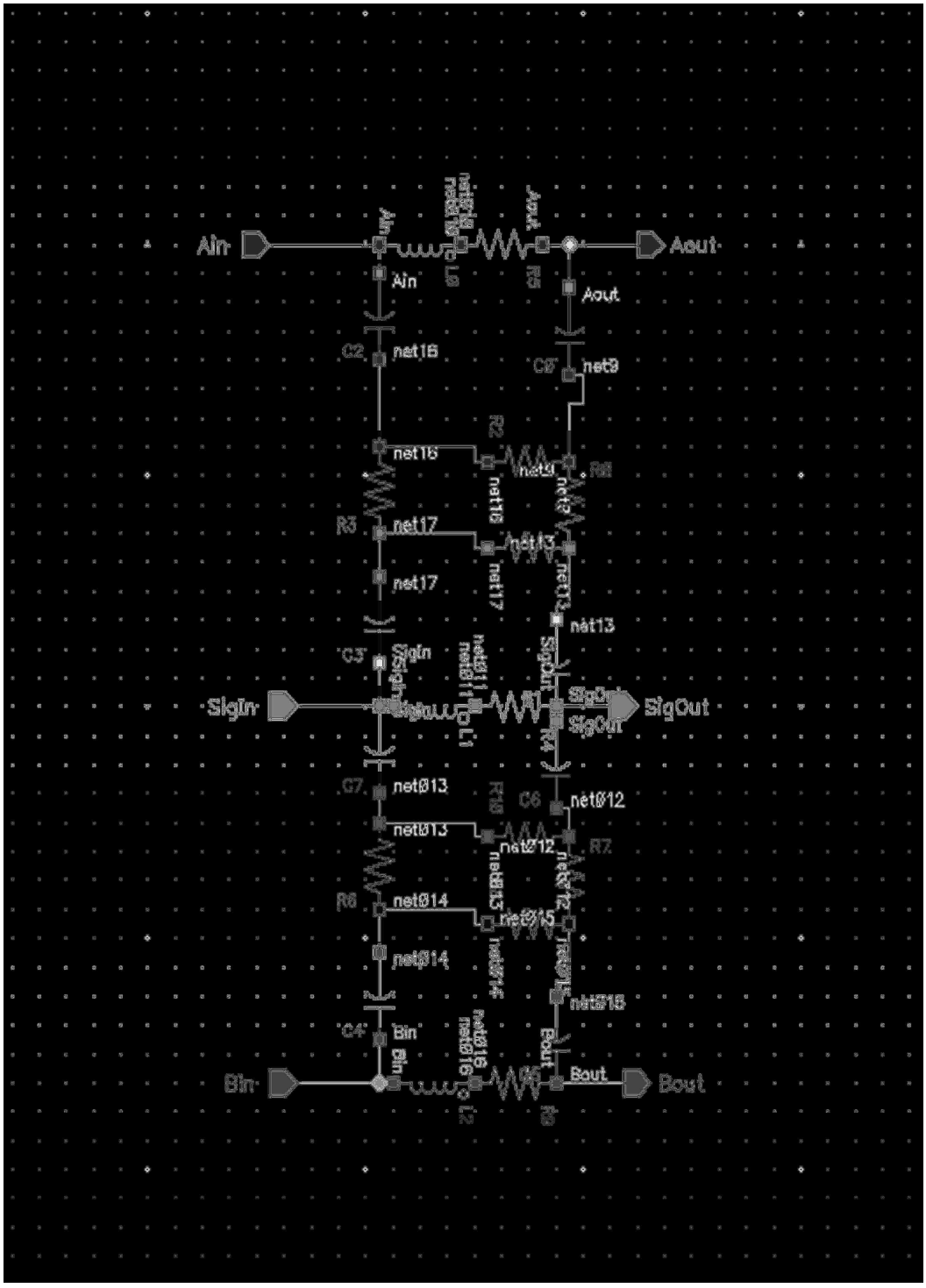


Figure 4.4. TSV Model

4.1 2D DESIGN

The 2D 8-bit full-adder schematic is shown as Figure 4.5, and there are, in total, 8 one-bit full adders. Just as mentioned above, each adder is with simple TGA structure, and they are connected together, and the carry-out of one adder feeds into the carry-in of the next. The layout design is given in Figure 4.6.

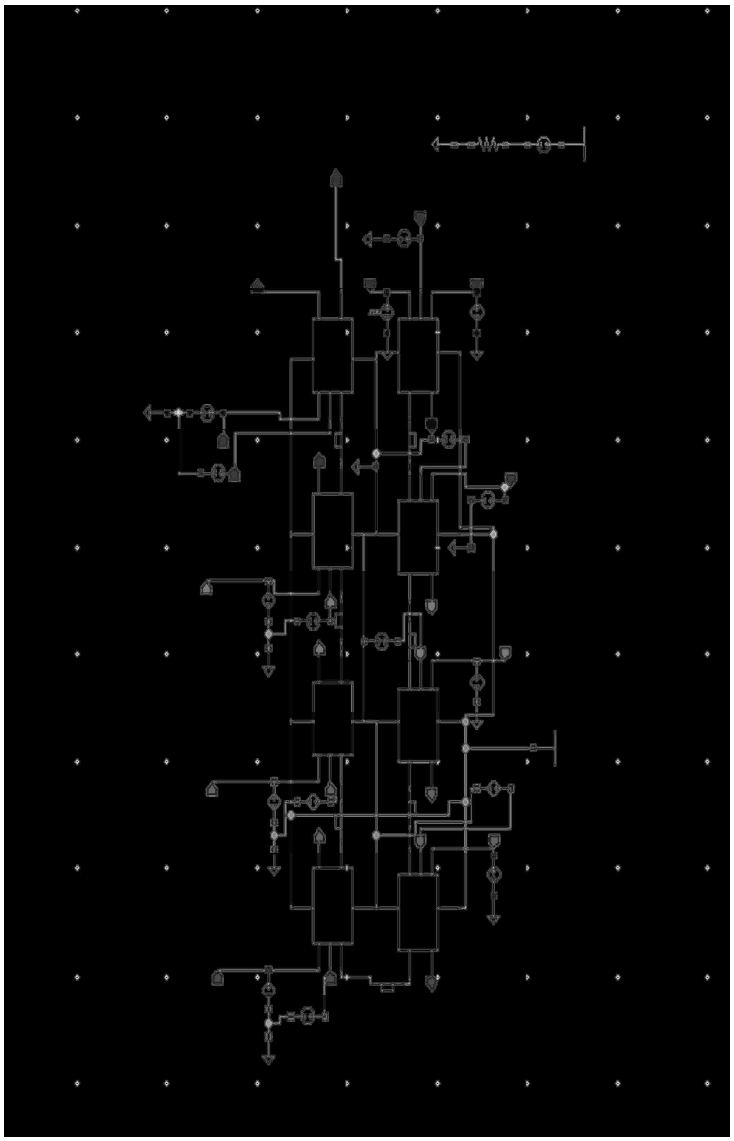


Figure 4.5. 2D Design Schematic

Figure 4.6. 2D Design Layout

4.2 TWO-TIER DESIGN

The two-tier design is shown in Figure 4.7, in which, on each tier, there are four single-bit full adders. In order to align with 2D design, the same single-bit adders are used. The three TSVs are used to deliver power, ground, and signal to the higher tiers. The final carry-out signal of lower tier 1 is transferred to upper tier 2 by a TSV, and the power supply of upper tier 2 is also from the lower tier. There are two separate layouts depending on the size of the TSV. It was found that for the 3um case and above, it was more area efficient to use a TSV-Above-Adder (TAA) Layout instead of a TSV-Beside-Adder (TBA) Layout. The 5um case (TAA) and the 1um (TBA) case are shown in Figures 4.8 and 4.9, respectively. These different layouts were done to save on the footprint area of the circuit. Therefore, the performance of the whole design will be impacted by the TSVs, and the results will be given in Section 4.5.

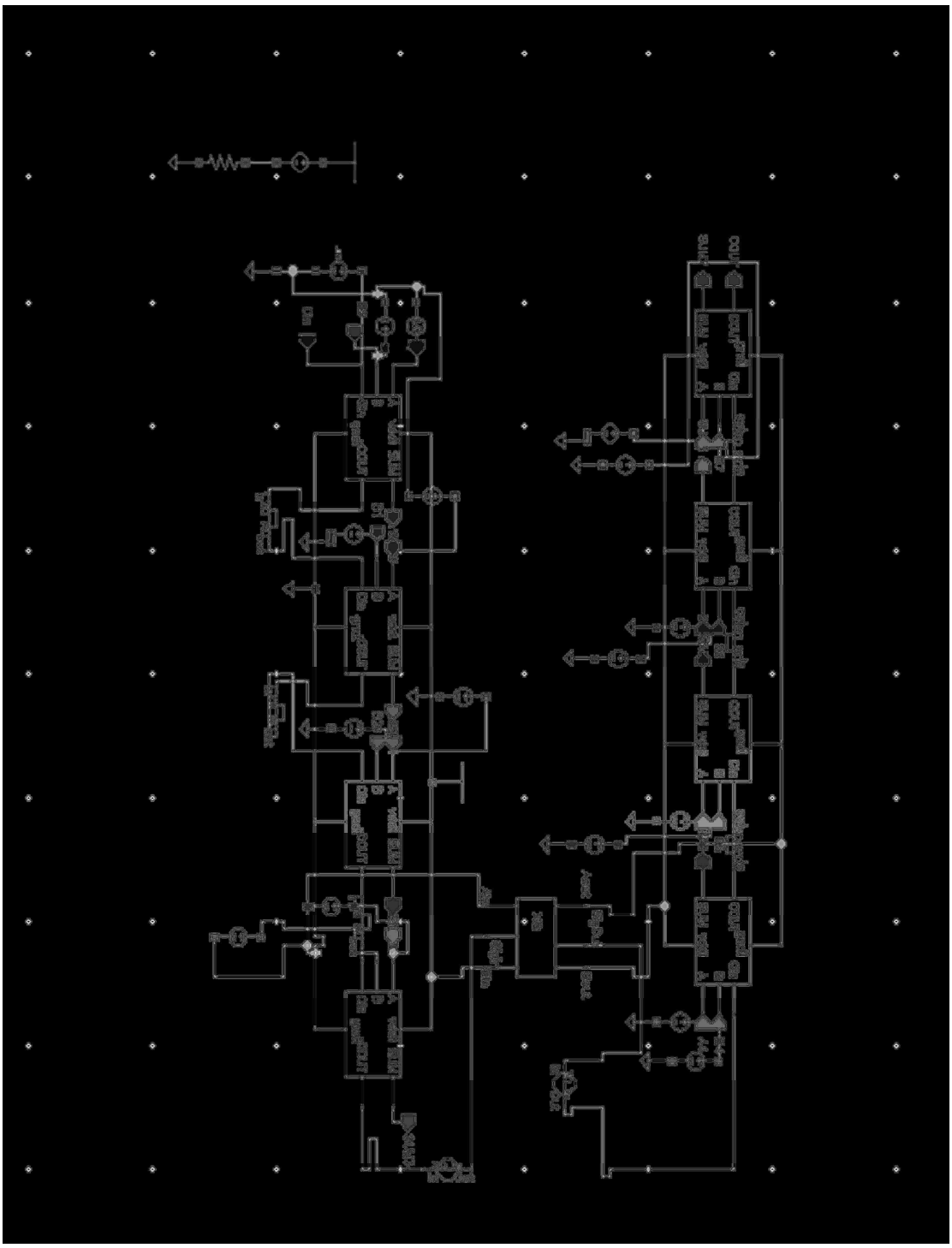


Figure 4.7. Two-Tier Design

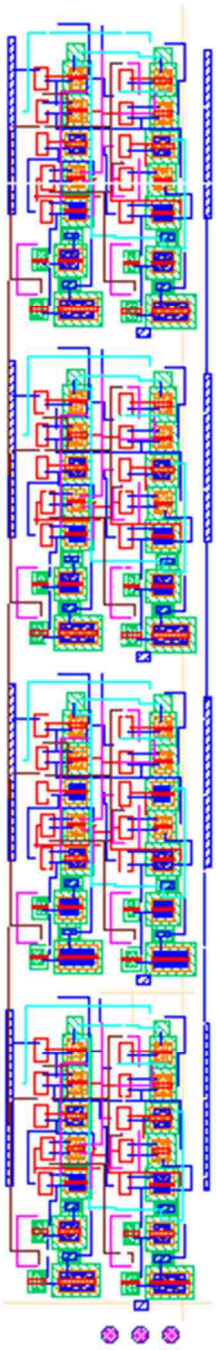


Figure 4.9. Two-Tier TBA Layout

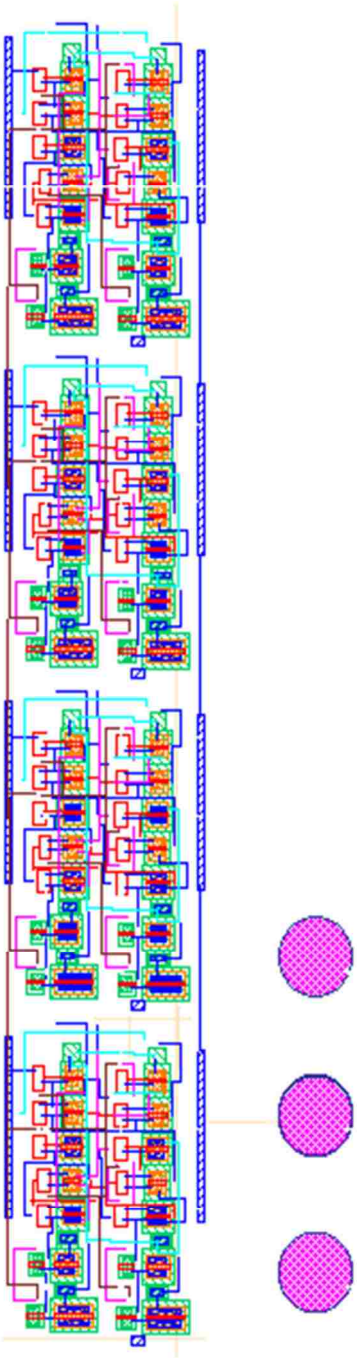


Figure 4.8. Two-Tier TAA Layout

4.3 THREE-TIER DESIGN

Similar to the two-tier design, the three-tier design is connected as shown in Figure 4.10. Three single-bit adders are placed on tier 1 and tier 3, and the remaining two single-bit adders on tier 2 (3-2-3 structure). The power supply and carry-in signals of higher tiers are delivered by TSVs. In Figure 4.11 the TBA layout design is shown for the 1um case. Figure 4.12 shows a different arrangement of the adders into an "L" shape for the three-adder tiers that is used to reduce area in the 2.5um case to the 4um case. Finally the 5um case is shown in Figure 4.13 by use of the TAA. Also note that the two-adder layouts will be presented in the next section.

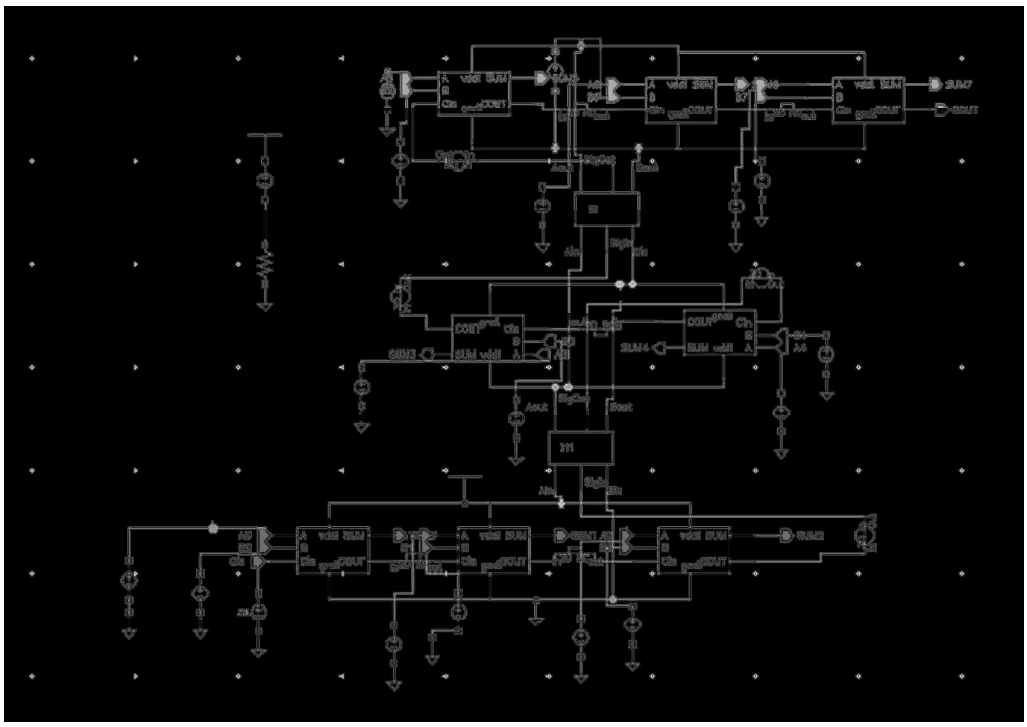


Figure 4.10. Three-Tier Design

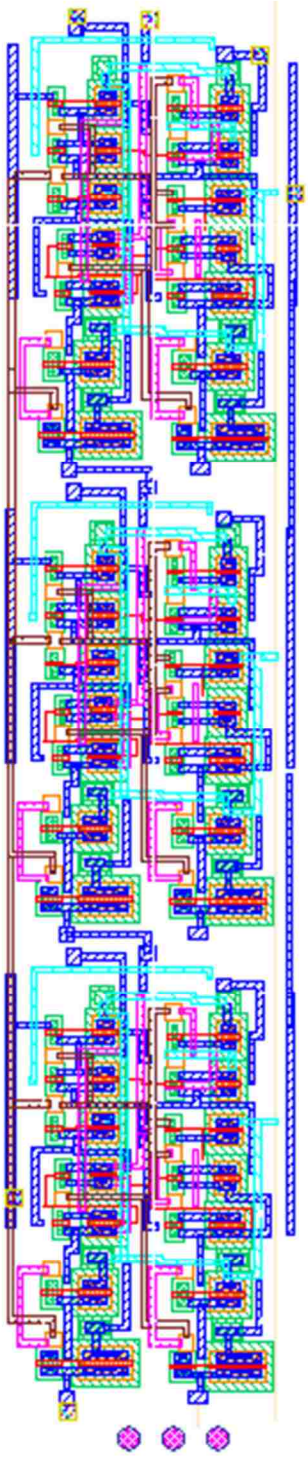


Figure 4.11. Three-Tier TBA Structure

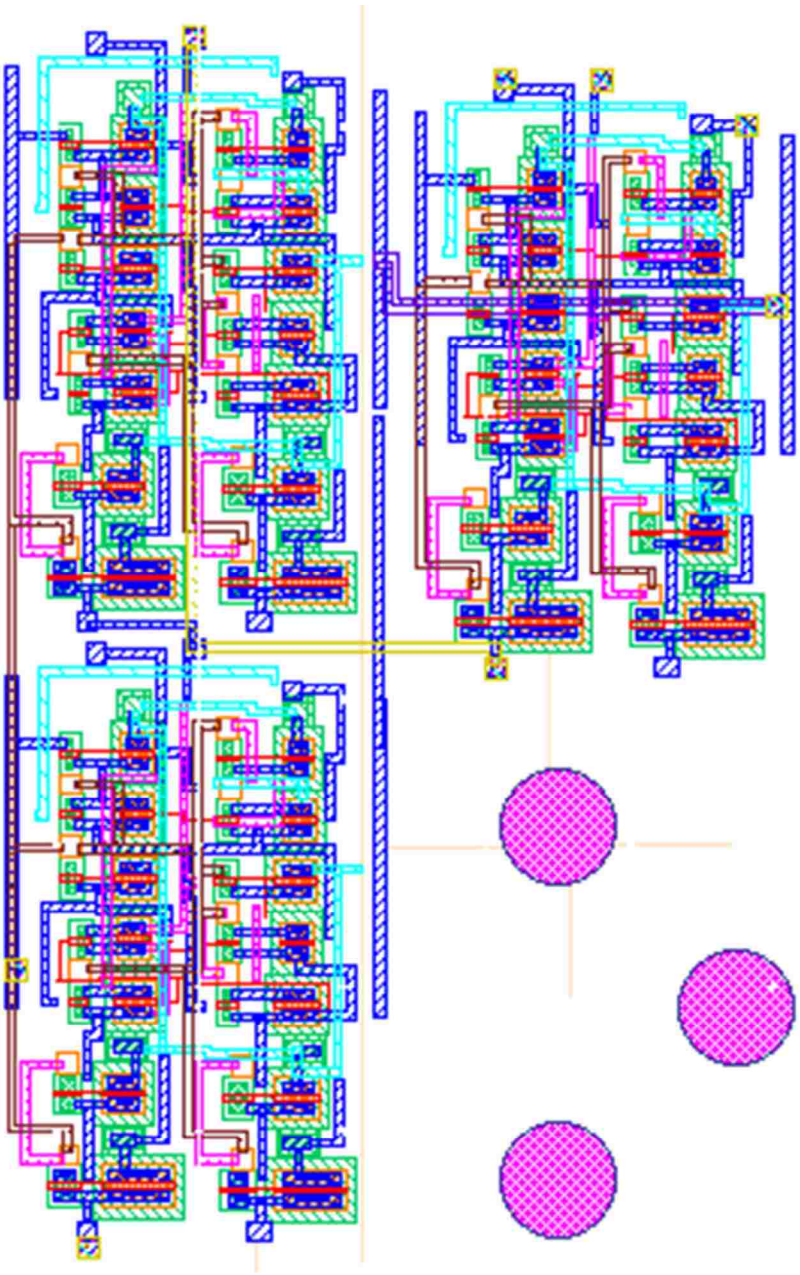


Figure 4.12. Three-Tier “L” Structure

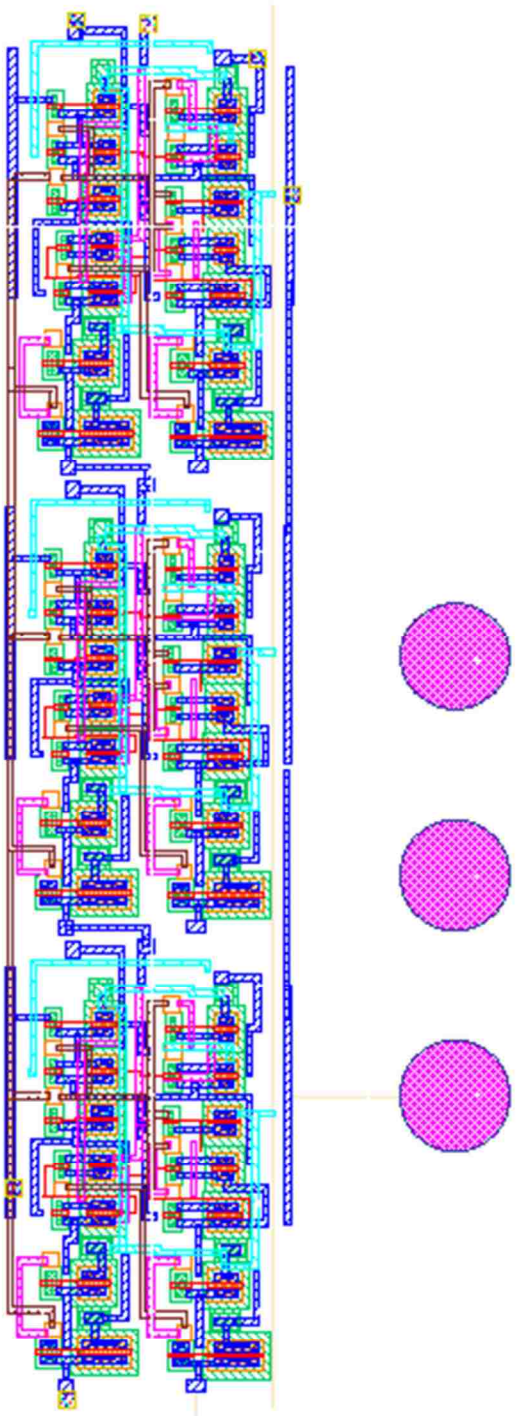


Figure 4.13. Three-Tier TAA Structure

4.4 FOUR-TIER DESIGN

Similar to the two-tier and three-tier design structures, the four-tier structure is depicted in Figure 4.14. There are two adders per tier, with the usual three TSV's connecting the tiers. The power supply and carry-in signals are delivered by the TSVs. The TBA layout was used, as shown in Figure 4.15, until 2.5um then the TAA layout, shown in Figure 4.16.

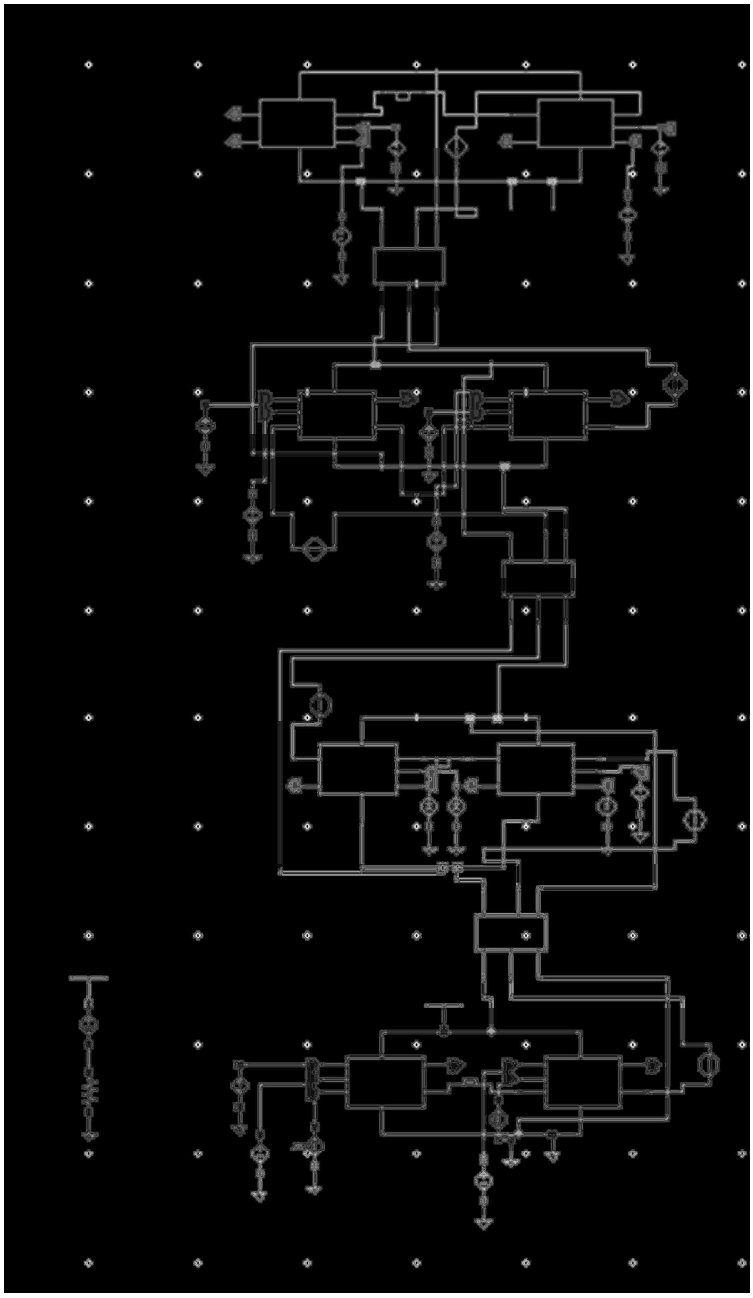


Figure 4.14. Four-Tier Design

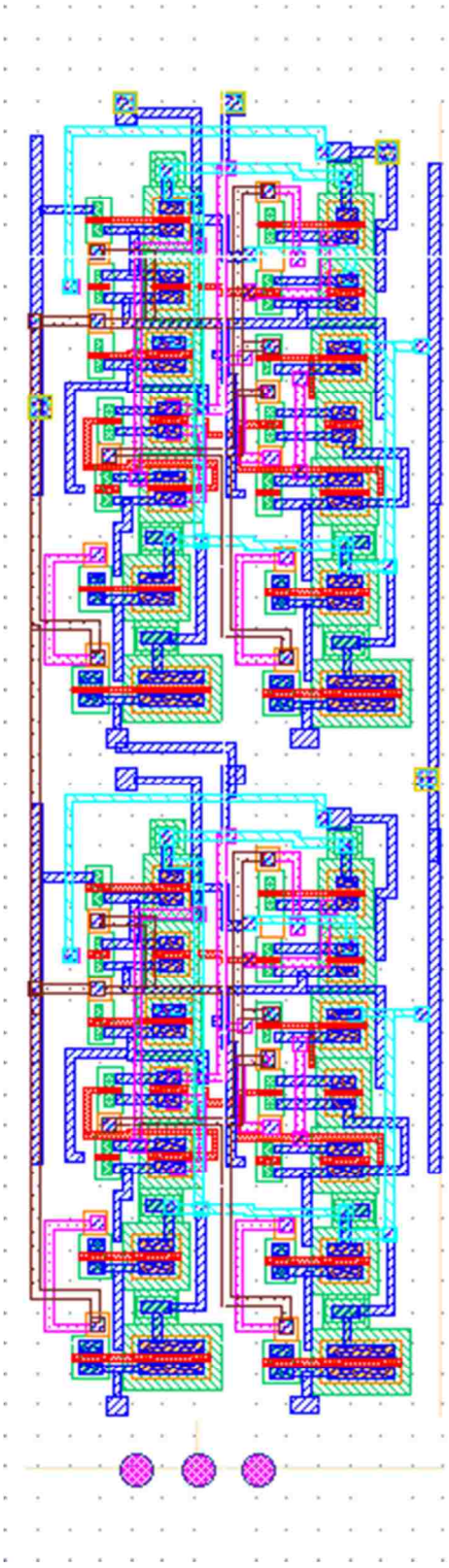


Figure 4.15. Four-Tier TBA Layout

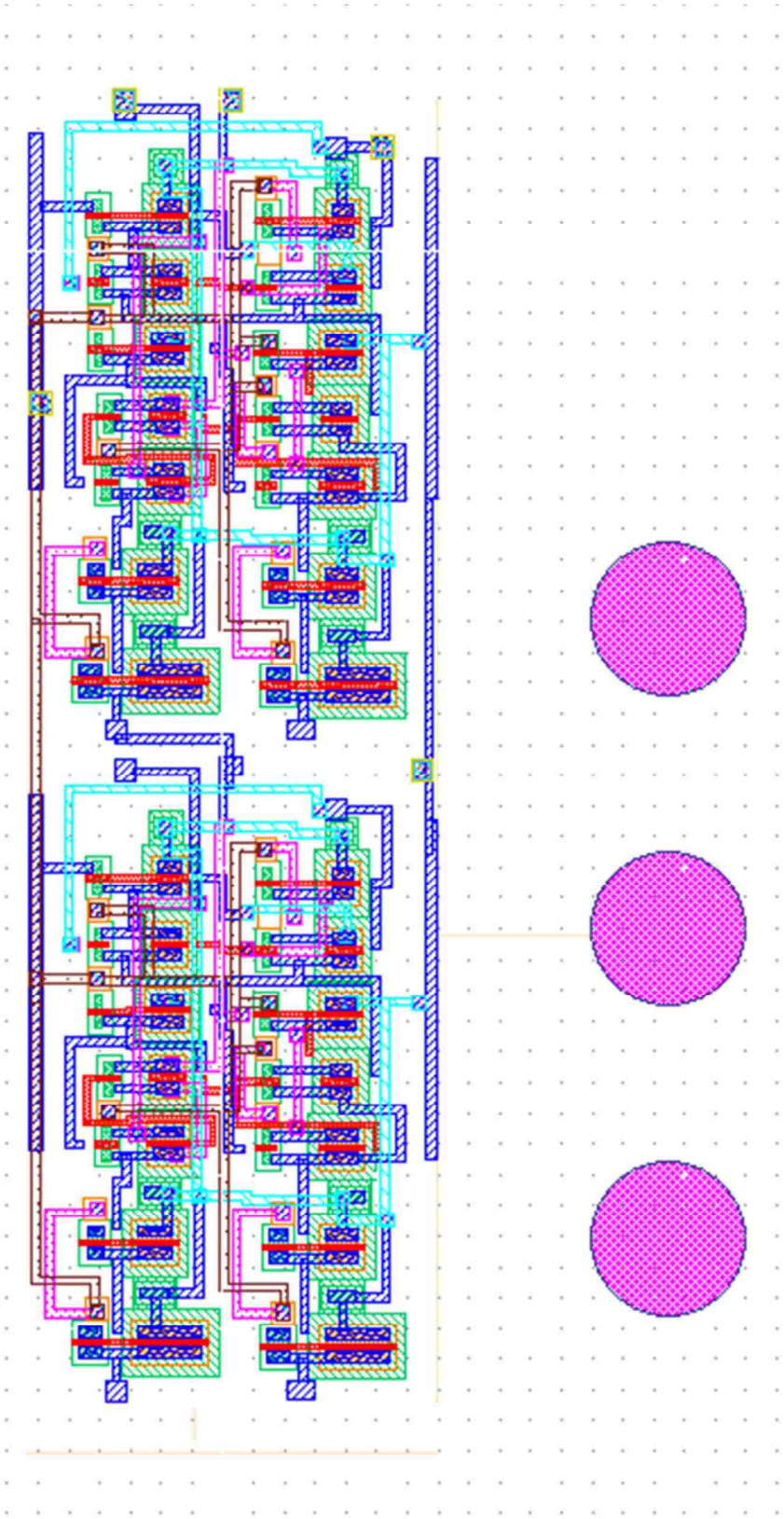


Figure 4.16. Four-Tier TAA Layout

4.5 EXPERIMENTAL RESULTS

The above designs were implemented in Cadence Virtuoso with TSMC 180nm technology library. As the technology library does not contain TSV models, the circuit models described in [20] and shown in Figure 4.17 were used and combined with the extracted parasitics from the layouts of different tiers with SPICE simulation. Note that in the figure, only two TSV's are shown, but in our model, 3 are used. This is due to there being 3 different signals needing to be passed (Vdd, gnd, and COUT). The middle TSV and everything directly connected to it has all values divided by 4 instead of by 2. A 3D technology with a fixed form factor was assumed, as well as TSV dielectric liner that scales with the diameter with the proportions used in [21], and a keep-out-zone from the center of the TSV 2D (D is the diameter of the TSV). The TSV diameter is swept from 5um to 50nm, with 10um height and 0.1um liner thickness at 5um. To capture the power supply noise, the lumped package model described in [22] is used. It is worthwhile to mention that while the simulation data are technology-specific, the overall trends and the conclusions drawn from them are general. The simulations were done with a 5ns period on the Cin Bit and a 15ns overall time. A worst-case input vector was used, i.e., A=[00011010] and B=[11100101].

The impact of the TSV diameter on propagation delay of the 8-bit ripple carry adder as shown in Figure 4.18 was considered first. For all cases, the delay decreases with the TSV diameter, which is natural as the parasitics induced by the TSVs are reduced. When the TSV diameter is reduced by 100x, the delay is reduced by 4.7%, 9.6% and 14.3% for the two-tier, three-tier and four-tier cases, respectively. When the TSV diameter is below 100nm, all designs have no observable difference in delay.

It is also interesting to note that the delay actually increases with the tier number. When the TSV diameter is 5um, the four-tier case has a 4.3% and 9.1% longer delay compared with the three-tier and two-tier cases, respectively.

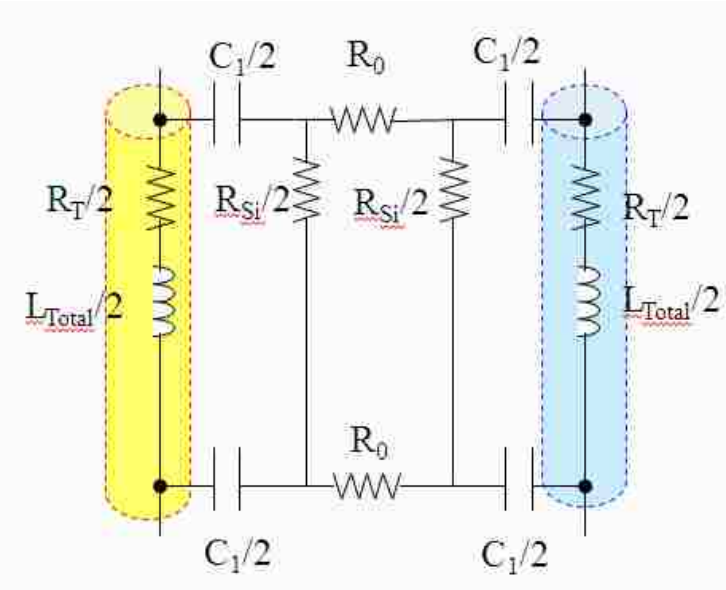


Figure 4.17. TSV Structure

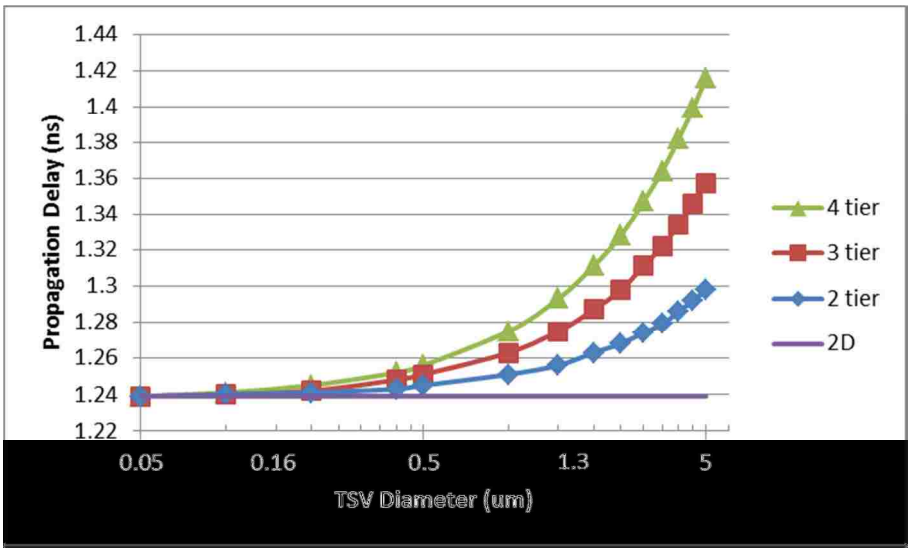


Figure 4.18. Maximum Propagation Delay Comparison Between Different Cases.

The above observations are contrary to the common belief, and the main reason is due to the block-level partitioning: The replacement of short local interconnects with TSVs actually result in a longer delay. To confirm this, a study was done on the RC delay of an M1 interconnect with 0.27um width, as well as that of a TSV with 4.5um diameter. The setup is shown in Figure 4.19 for the local interconnect, and 4.20 for the TSV. The interconnect length is swept from 4.30um to 4.30mm. The result is depicted in Fig. 4.21. From the figure one can clearly see that when the interconnect length exceeds 2.15mm (global interconnect), it would be beneficial to use TSV to replace it. But when the interconnect length gets down to 43um and below (local interconnect), an 18.36% delay overhead is introduced if the interconnect is to be replaced by the TSV.

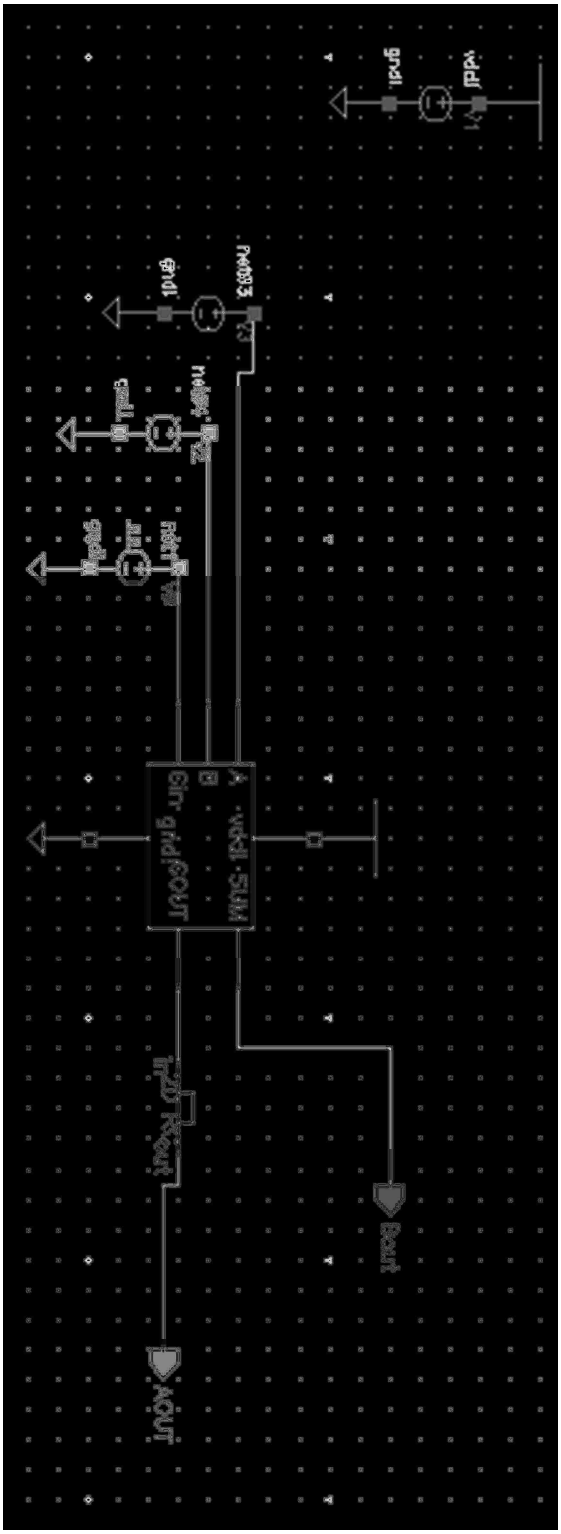


Figure 4.19. Local Interconnect Delay Model

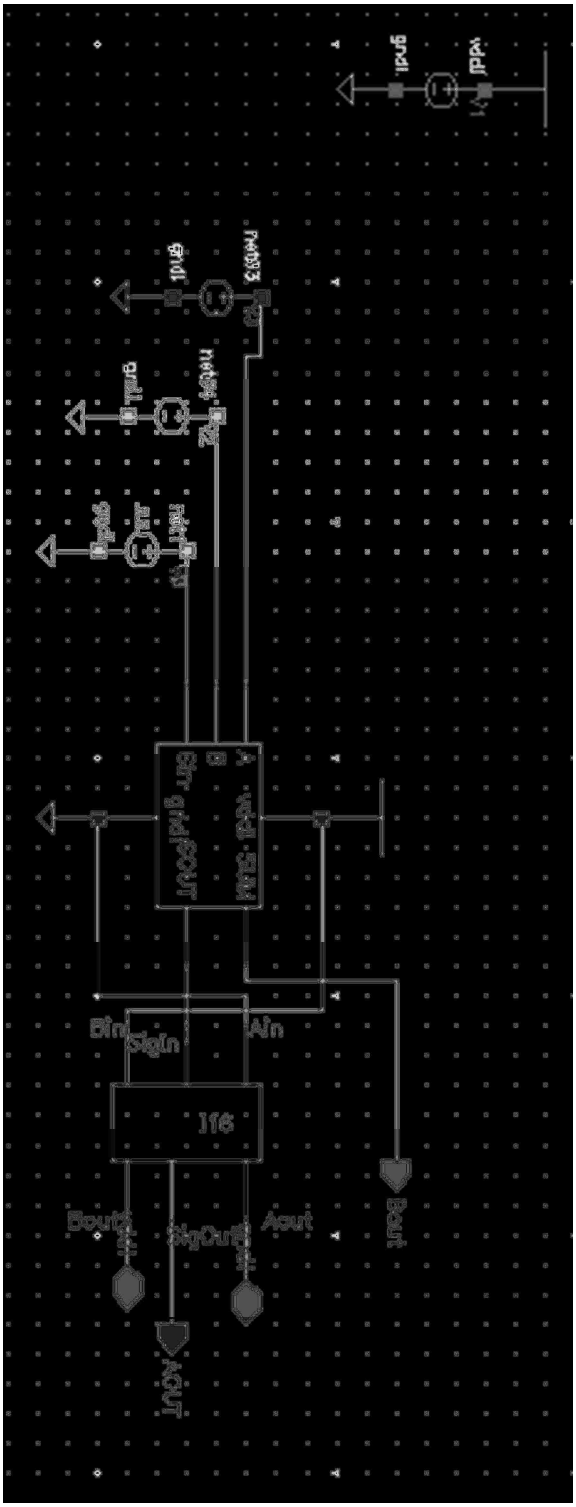


Figure 4.20. TSV-as-Interconnect Model

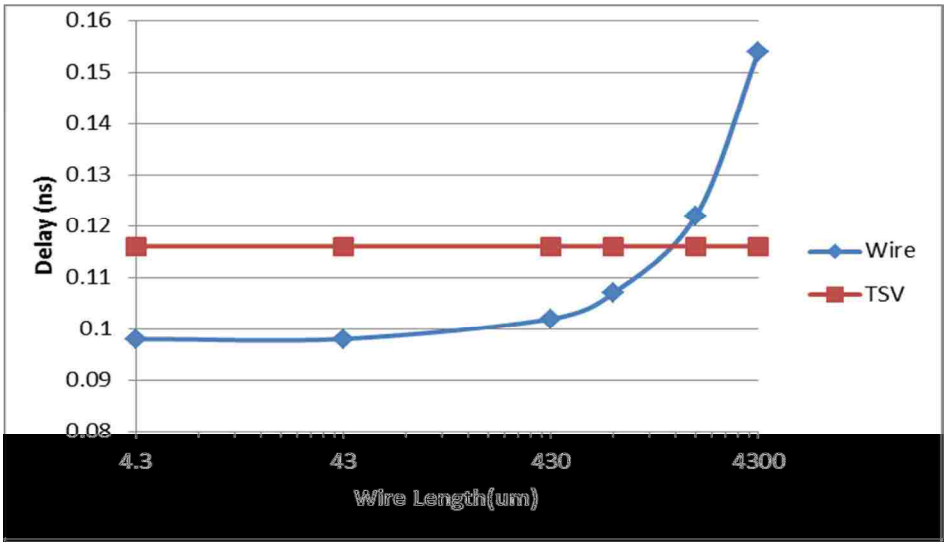


Figure 4.21. Comparison Between Wire Delay and TSV Delay

The average power consumption and power supply noise of the different cases was studied, and the result is shown in Figure 4.22 and Figure 4.23, respectively. Similar trends are observed: When the TSV diameter is reduced by 100x, the power is reduced by 3.9%, 7.9% and 11.8% for the two-tier, three-tier and four-tier cases. It is interesting to note that the power actually increases with the increase in tier number. In terms of the impact of the number of tiers, when the TSV diameter is 5um, the four-tier case consumes 3.6% and 7.6% larger power compared with the three-tier and two-tier cases, respectively. On the other hand, when the TSV diameter is below 100nm, no noticeable difference is found between the different cases.

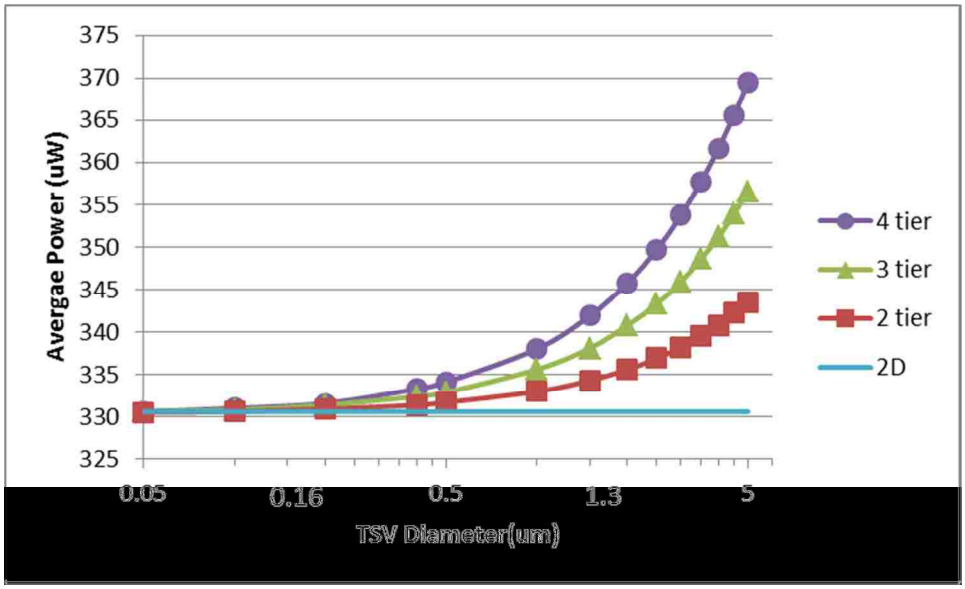


Figure 4.22. Average Power Comparison Between the Different Cases

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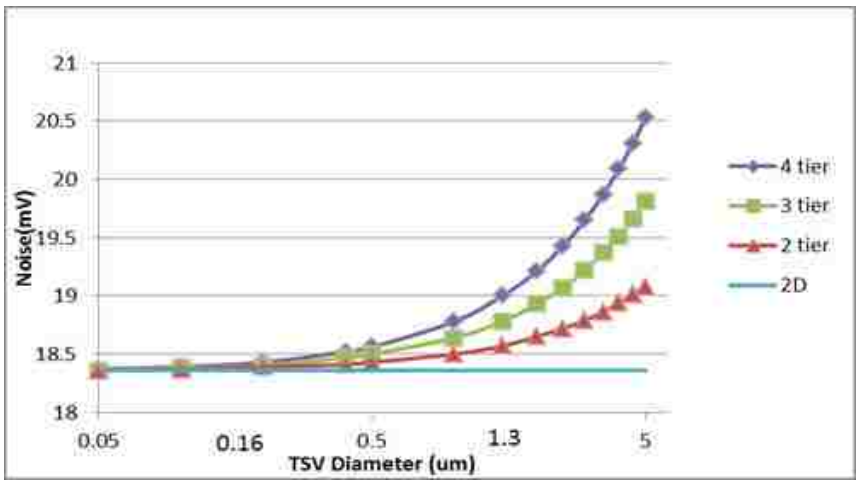

Figure 4.23. Average Noise Ccomparison Between the Different Cases.

Finally, the footprint based on our layouts was compared. The illustration of the layout designs can be found in Sections 4.1, 4.2, 4.3, and 4.4 for the 2D, two-tier, three tier, and four tier , respectively, and the footprint is measured using Virtuoso Layout L.

The result is shown in Figure 4.24. When the TSV diameter exceeds 2.5um, the footprint of the three-tier case levels off for a bit representing a change in the layout. As can be seen in Figure 4.24, when the 5um TSV diameter mark was reached, the two-tier design no longer has an advantage. Whereas when the TSV diameter is below 0.5um, it has a minimum impact on the footprint. The two-tier, three-tier and four-tier cases can achieve an area reduction of 2.0x, 2.6x and 4.0x, respectively.

Combining this result with previous delay, power and noise analysis, it can be concluded that when the TSV diameter is below 100nm, significant area reduction can be achieved with little delay, power and noise overhead. In other words, it is indeed beneficial to perform block-level partitioning for monolithic 3D ICs, where the TSV diameters can be made smaller than 50nm.

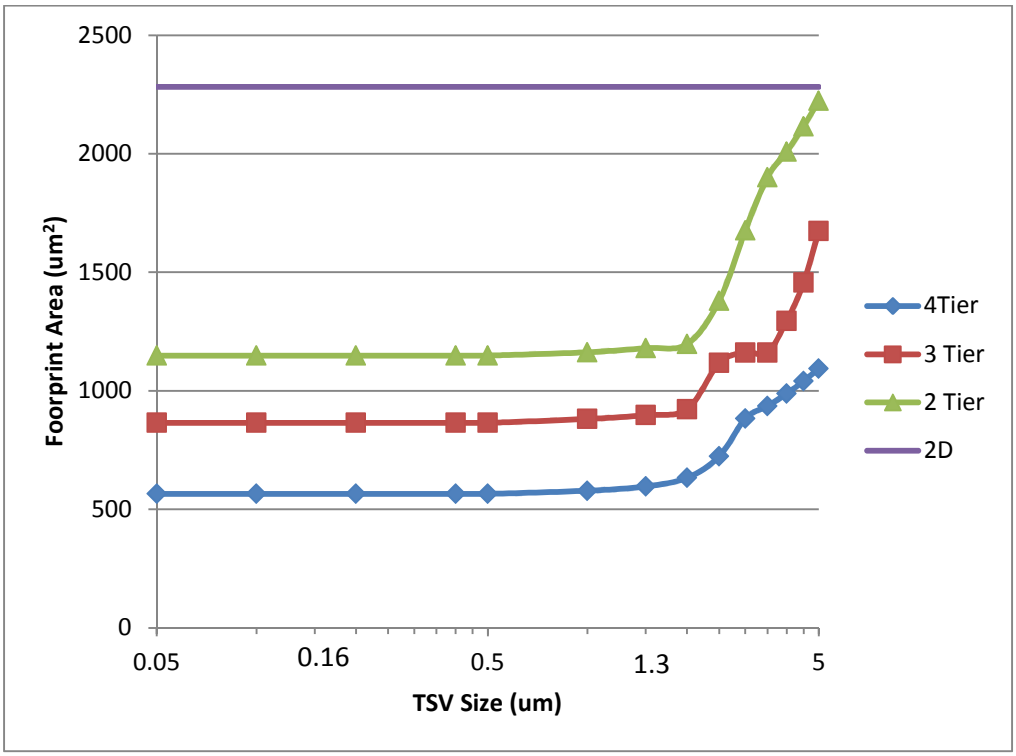

Figure 4.24. Footprint Comparison Between Different Cases.

5. CONCLUSION

An 8-bit ripple carry adder was used as an example to explore the impact of TSV size and tier number on various tradeoffs between power, delay, footprint and noise for monolithic 3D ICs. Experimental results indicate that when the TSV size is below 100nm, it can be beneficial to perform block-level partitioning for smaller footprint with minimum power, delay and noise overhead. It was also shown that for interconnect lengths of greater than 2.15mm for the 4.5um case, it would be beneficial to use monolithic TSV instead.

APPENDIX A
RC VALUES FOR THE RC-2

These values used TSV Diameter (D) to calculate the sheet resistance (R2) for the M1 interconnect and the area capacitance for the M1 region. These values were obtained in [26] for the TSMC 180nm library. The schematic for this is given in Figure A.1. Also of note is that the C values were divided evenly between the two capacitors.

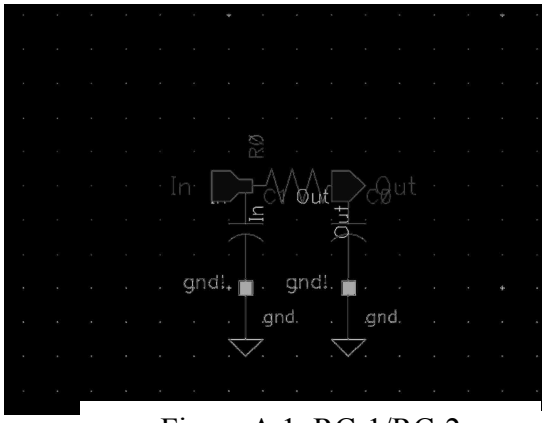

Figure A.1. RC-1/RC-2 Schematic

TSV Diameter(D)	R2	C2
0.05	0.014815	5.265E-19
0.1	0.02963	1.053E-18
0.2	0.059259	2.106E-18
0.4	0.118519	4.212E-18
0.5	0.148148	5.265E-18
1	0.296296	1.0530000E-17
1.5	0.444444	1.5795E-17
2	0.592593	2.106E-17
2.5	0.740741	2.6325E-17
3	0.888889	3.159E-17
3.5	1.037037	3.6855E-17
4	1.185185	4.212E-17
4.5	1.333333	4.7385E-17
5	1.481481	5.265E-17

Table A.1. RC-2 values

APPENDIX B
RLC VALUES FOR THE TSV

This shows the TSV RLC values used. The equations used are those referenced in [20] and the schematic was shown in Figure 4.4.

Diameter(ı	RT	Ltotal	LT	C1	C2	R0	RSi
5E-08	1.709048	1.09203E-12	1.68E-12	5.52933E-16	2.49117E-17	20	0.068795
1E-07	0.854525	1.1224E-12	1.71E-12	1.10587E-15	4.98234E-17	20	0.068795
2E-07	0.427263	1.18315E-12	1.77E-12	2.21173E-15	9.96468E-17	20	0.068795
4E-07	0.213632	1.30464E-12	1.89E-12	4.42346E-15	1.99294E-16	20	0.068795
5E-07	0.170906	1.36539E-12	1.95E-12	5.52933E-15	2.49117E-16	20	0.068795
0.000001	0.085454	1.66912E-12	2.26E-12	1.10587E-14	4.98234E-16	20	0.068795
1.5E-06	0.05697	1.97285E-12	2.56E-12	1.6588E-14	7.47351E-16	20	0.068795
0.000002	0.042728	2.27658E-12	2.86E-12	2.21173E-14	9.96468E-16	20	0.068795
2.5E-06	0.034182	2.58031E-12	3.17E-12	2.76466E-14	1.24558E-15	20	0.068795
0.000003	0.028485	2.88404E-12	3.47E-12	3.3176E-14	1.4947E-15	20	0.068795
3.5E-06	0.024416	3.18777E-12	3.78E-12	3.87053E-14	1.74382E-15	20	0.068795
0.000004	0.021364	3.4915E-12	4.08E-12	4.42346E-14	1.99294E-15	20	0.068795
4.5E-06	0.018991	3.79523E-12	4.38E-12	4.97639E-14	2.24205E-15	20	0.068795
0.000005	0.017092	4.09896E-12	4.69E-12	5.52933E-14	2.49117E-15	20	0.068795
1.00E-05	0.008547	7.13626E-12	7.72E-12	1.10587E-13	4.98234E-15	20	0.068795

Table B.1. RLC Values for the TSV Parameters

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VITA

Luke Maresca was born in Puyallup, WA. He attended St. Charles Borromeo School in St. Charles, MO for his primary, middle, and junior high years. He then went to Duchesne High School in St. Charles, MO for his secondary education. He completed his Bachelor of Science in Computer Engineering at Saint Louis University in St. Louis on May 2010, then his Master of Science in Computer Engineering at Missouri University of Science and Technology in Rolla on August 2012. His passions in the field of computer engineering include computer hardware design, the future of integrated circuits, and quantum computing. He is in the process of publishing one paper in the IEEE Transactions on Circuits and Systems II.