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The influence of printed circuit board design on TEM cell measurements

Vijay Kasturi

Department:

THE INFLUENCE OF PRINTED CIRCUIT BOARD DESIGN ON TEM CELL MEASUREMENTS

by

VIJAY KASTURI

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Dr. Daryl G. Beetner, Advisor	Dr. Todd Hubing

Dr. Thomas P. Van Doren

ABSTRACT

The IEC 61967-2 integrated circuit radiated emissions test standard describes the use of the TEM cell to measure near-field emissions from an IC. This test requires a printed circuit board (PCB) to mount the IC. The IEC guidelines allow for flexibility in the design of this test PCB which may cause variations in the measured emissions. This thesis studies the impact of typical variations in the PCB design on the measured emissions. Two printed circuit boards were designed within the IEC standard specifications; one using what is considered poor PCB design strategies and the other using good PCB design strategies. The two PCBs were designed to allow changes in the PCB design as well. Three pin-for-pin compatible 8051 microcontrollers were tested. Emissions were measured from these three ICs using both PCBs and changing the test configuration by changing the program running inside the IC, changing the rise time of the input clock, and changing the switching of I/O. PCB design variations caused a change of about 3-8 dB in the measured emissions. A change in the test configuration caused a 4-15 dB difference in the measured TEM cell emissions. TEM cell emissions from the three manufacturers were compared for five different board setups. Possible causes for the variations in emissions with the design and among different manufacturers are discussed.

ACKNOWLEDGMENTS

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1. INTRODUCTION

Printed circuit board (PCB) designers want integrated circuit (IC) manufacturing companies to test their new ICs for emissions before they are released to the market, so they can compare ICs among different manufacturers. IC manufacturers use standardized testing methods such as IEC 61967 and SAEJ1752 for measurement of IC radiated emissions [1], [2], [3]. One of the procedures described in the IEC 61967 uses the TEM cell to measure the emissions from an IC. Near electric- and magnetic-field emissions are tested in this procedure by mounting the device under test (the IC) on a test PCB, which is then mounted on the wall of a TEM cell with the IC inside the cell.

The guidelines given by the TEM cell measurement procedure allow for flexibility in the design of the PCB test board. As a result, boards designed by different companies or engineers using the same guidelines might yield different measurements of emissions for the same IC. In this work, the variation of TEM cell emissions with PCB design parameters and test configurations that are not well specified in the IEC standard is studied. PCB design variations that were studied include distance between PCB layers, PCB stack-up, length and width of traces on the IC side of the TEM cell, the placement, connection method, amount, and number of decoupling capacitors, and the presence (or absence) of a ground plane below the IC. Testing configurations that were studied include the clock edge rate, the use of I/O (i.e. inhibiting I/O from switching), the use of external instead of internal memory, and variations in software.

Variations were implemented in a series of PCBs. Each variation was studied through measurements in a TEM cell. The goal of this study was to show the maximum variation in measured emissions that might be expected for typical variations in design parameters, as well as the impact of different testing configurations. To allow study of pin-for-pin compatible ICs from different manufacturers, and allow elimination of the influence of a specific IC from results, a standard 8051 microcontroller IC was used as the device under test (DUT). The affects of PCB design variations and test configurations were tested using three pin-for-pin compatible 8051 ICs from three different manufacturers.

This thesis is arranged as follows. The TEM cell, its advantages, and disadvantages and its applications are discussed in chapter 2. Chapter 3 discusses the experimental approach followed to test the variations in the TEM cell emissions. This chapter includes a detailed discussion of the different parameters tested and how changing these parameters might effect the measured emissions. Details regarding the PCB that was designed for this work are included. Chapter 4 first discusses the measurement setup and the characterization of the noise floor. Measurement results are presented for each test parameter and results are then compared among the different IC manufacturers. Chapter 5 includes a discussion of results and conclusions. This chapter also explains how the results of this work might be scaled to bigger, faster ICs.

2. THE TEM CELL

A TEM cell is a rectangular co-axial transmission line tapered at both the ends to form a closed structure [4]. The inner conductor, called the septum, is wide and flat. The outer conductor of the cell acts as a shield which contains the internal fields and prevents interference from external fields. The TEM cell propagates a TEM mode electromagnetic wave only below its cutoff frequency. Above the cutoff frequency, higher order modes will also exist inside the cell. The cell is tapered at both the ends to adapt to standard 50-ohm co-axial connectors. To avoid reflections, the characteristic impedance of the cell is maintained at 50-ohms throughout the structure. The cell has an opening on the top in which the test PCB with the DUT is mounted. The ground plane of the test PCB attaches to the outer shield to form a completely closed enclosure.

Some advantages of the TEM cell are that it provides a good isolation of the test volume from external fields, the fields inside the cell are well characterized and approximately uniform within the test volume [5], the TEM cell is portable, and all the measurements are easily reproducible within a few dB. The advantages of the TEM cell over OATS and semi-anechoic chambers include that a TEM cell does not need an antenna to establish or measure the EM fields and the TEM cell is portable and easy to handle. The disadvantages of the TEM cell are the relatively low frequency cutoff of the cell because of cavity resonances and higher order modes in the cell [6].

One reason for the low-frequency cutoff is that the cell consists of three differently shaped parts. Due to the tapering of the cell at both the ends, the lengths of the inner and outer conductor differ by Δs as shown in Figure 2.1. This distortion gives rise to propagation of higher order modes inside the TEM cell, making the fields inside the cell non-uniform. The value of Δs limits the maximum frequency up to which the cell can be used. Cavity resonances in the cell also limit the maximum usable frequency. These resonances occur at integer multiples of the frequency at which the dimensions of the cell are half the wave length.

TEM cells are basically used for susceptibility tests and near-field radiated emissions measurements. In the susceptibility tests, one port of the TEM cell is fed with the test signal while the other port is connected with a matched termination (50-ohms). A

uniform EM field propagates in the TEM cell unless the presence of the DUT changes the field. For measuring the radiated emissions, the test PCB is mounted on the TEM cell with the DUT facing towards the septum of the cell. The DUT should be functioning while the measurements are done. One port of the TEM cell is connected to a measuring device (e.g. a spectrum analyzer). The other port is connected with a matched termination. This setup allows one to measure the amplitude of the signal coupled to the septum. Measuring the coupled noise at both the ports allows one to determine the phase information, which is useful for determining the cause (electric- or magnetic-field) for the emissions [7]. The measurements do not directly give the far-field radiation from the DUT, but give the near E-field and H-field coupling from the DUT to the septum. While this measurement does not give the far-field emissions, it does give a feel for the tendency of this DUT to couple to nearby antennas and in some cases, can be used to predict the maximum radiated field with sufficient information about the PCB and attached cables [7], [8].

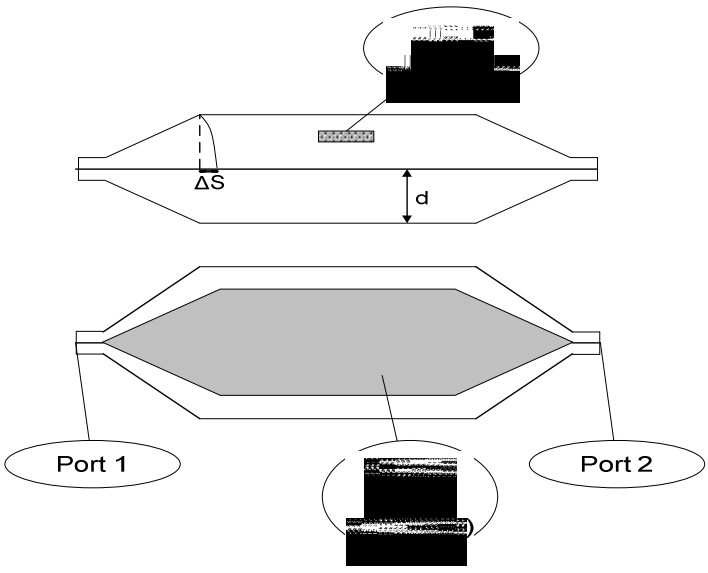


Figure 2.1. Cut-away diagram of the TEM cell showing the septum, DUT, and the difference in the length between inner and outer conductors. Top: side view. Bottom: top view.

3. METHODS

3.1. PARAMETERS TESTED

IEC standard 69167-2 for TEM cell emissions allows for many variations in the test PCB design and the test configuration which may influence the outcome of the test. Parameters that might be varied to impact TEM cell measurements are presented in the following sections and hypotheses are made as to how these parameters will effect emissions.

3.1.1. PCB Design Variations

3.1.1.1 Distance between PCB Layers. Distance between layers in the PCB stack-up is one parameter that may affect measured emissions in a TEM cell. Figure 3.1 and Figure 3.2 show two different PCB designs that illustrate this case. The PCB in Figure 3.2 uses a greater distance between layers than the one in Figure 3.1. Assuming no change in the decoupling capacitor placement, an increase in the thickness of the board increases the inductance to the decoupling capacitor. Inductance increases because of a greater overall loop area in one PCB design over the other. An increase in the inductance to the decoupling capacitor increases the impedance of the power delivery network at high frequencies, as seen by the IC, which in turn may increase the noise voltage between the IC and septum and decrease conducted currents. Hence, increasing distance between power planes may increase capacitive coupling to the TEM cell and reduce inductive coupling to the cell.

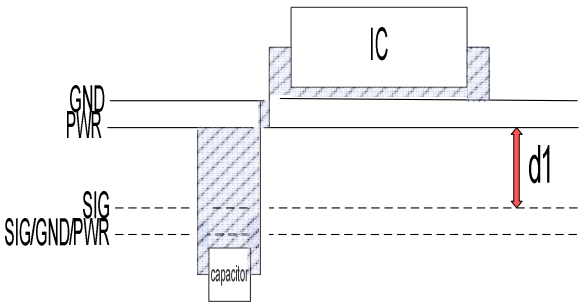


Figure 3.1. PCB with distance d1 between power and signal layers

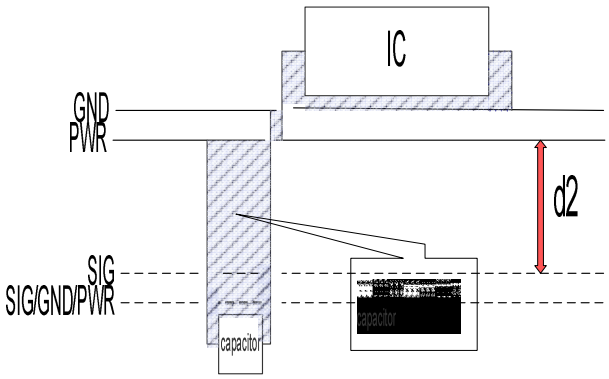


Figure 3.2. PCB with distance d2 (>d1) between power and signal layers

3.1.1.2 Stack-up. Changing the stack-up of the PCB may also affect TEM cell measurements. For example, for the connections shown in Figure 3.1 if the power and the signal layers are swapped, as shown in Figure 3.3, inductance to the decoupling capacitor decreases assuming the vias to power and ground planes from the IC and capacitor, respectively, are closely spaced. Hence, capacitive coupling may decrease and inductive coupling may increase at high frequencies for the configuration in Figure 3.3 compared to Figure 3.1 . If the vias to the power and ground planes are widely spaced, then the inductance may increase with a change in stack-up. For widely spaced power and ground planes as shown in Figure 3.4, placement of the decoupling capacitor matters more than when power and ground layers are close, so placement may have a greater influence on emissions when the separation between power and ground layers is increased. Switching the power and signal layers as in Figure 3.3 and connecting the decoupling capacitor badly may result in an overall increase in capacitive coupling and decrease in inductive coupling, more so than for the case where power and ground layers are close.

3.1.1.3 Traces in the TEM Cell. The tendency of a trace to couple to the septum of the TEM cell changes with the length and width of the trace on the IC side of the board. The greater the trace area, the greater the capacitive coupling. The longer and skinnier the trace, the greater the inductive coupling. Changing trace length or area may also change the impedance from the IC to PCB, but that change should be relatively small for the changes in trace design that are allowed by the standard.

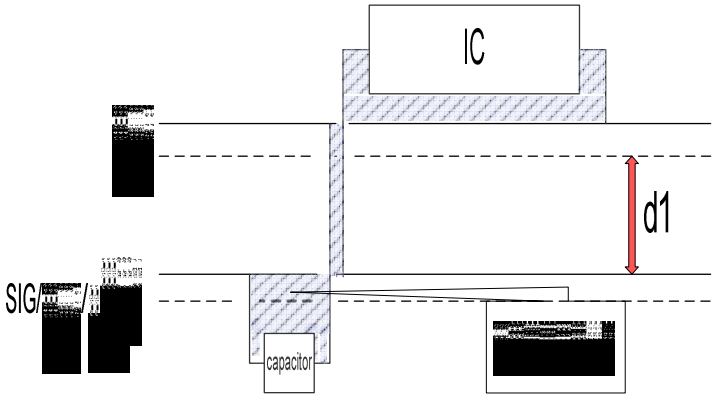


Figure 3.3. PCB with power and signal layers swapped (closely spaced vias)

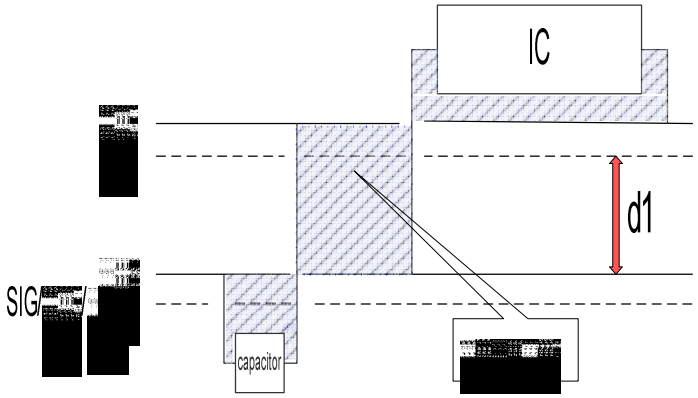


Figure 3.4. PCB with power and signal layers swapped (widely spaced vias)

3.1.1.4 Decoupling Strategy. The number, value, location, connection method and package style of decoupling capacitors may be varied. An increase in the value of the decoupling capacitors decreases the impedance of the power bus at low frequencies, potentially decreasing noise voltage (as shown in Figure 3.5), and hence the voltage between the IC and the septum, and possibly increasing noise current (due to lower power bus impedance). As a result, capacitive coupling may decrease and inductive coupling may increase at low frequencies.

Increasing the distance between the IC and the decoupling capacitor (as shown in Figure 3.6) can increase connection inductance between the IC and decoupling capacitor. Distance has a small effect on the impedance of the power bus for closely placed PWR

and GND planes, but may have a measurable effect for widely spaced planes. Increasing power bus impedance may increase capacitive coupling and reduce inductive coupling.

The method used to connect to the decoupling capacitor may change the series inductance to the capacitor (as shown in Figure 3.7 and Figure 3.8), changing the power bus impedance at high frequencies (as shown in Figure 3.9). Increasing the trace length to the decoupling capacitor or using via connections to the power and return planes that have high associated inductance may increase capacitive coupling and decrease inductive coupling at high frequencies.

Decoupling capacitors in large packages may have a higher equivalent series inductance (ESL) associated with them than smaller packages. The impact of package size should generally be small among surface mount components compared to inductance added elsewhere, for example by the connection method.

Using a large number of decoupling capacitors decreases the overall inductance to the capacitor, decreasing the power bus impedance at high frequencies. Increasing the number of decoupling capacitors may decrease capacitive coupling and increase inductive coupling.

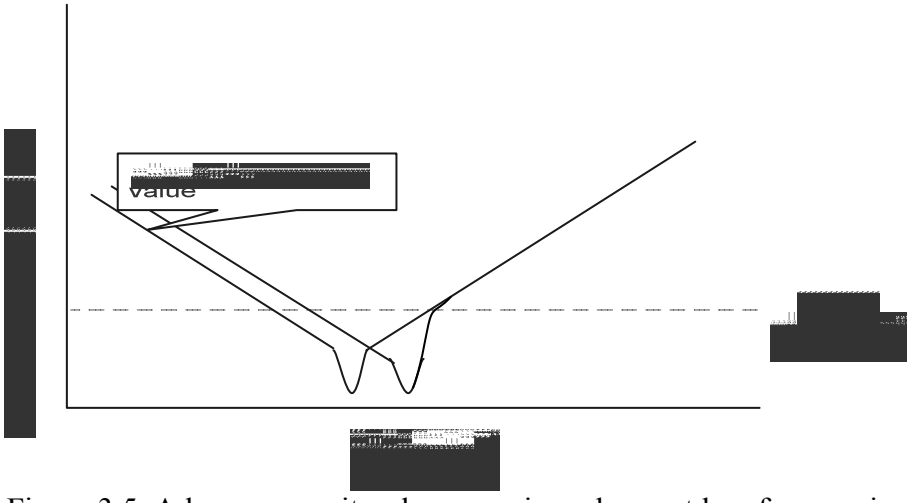


Figure 3.5. A larger capacitor decreases impedance at low frequencies

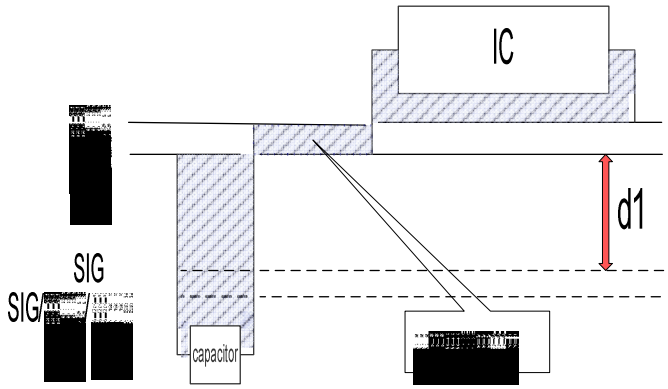


Figure 3.6. Increasing the distance between the decoupling capacitor and IC can increase the impedance between them

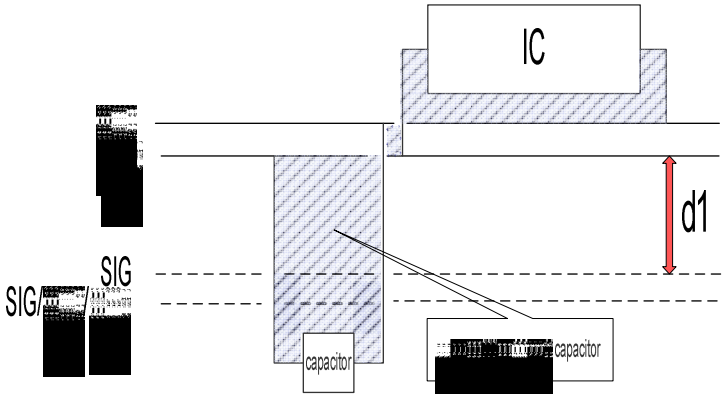


Figure 3.7. Decoupling capacitor with longer connection trace than in Figure 3.1

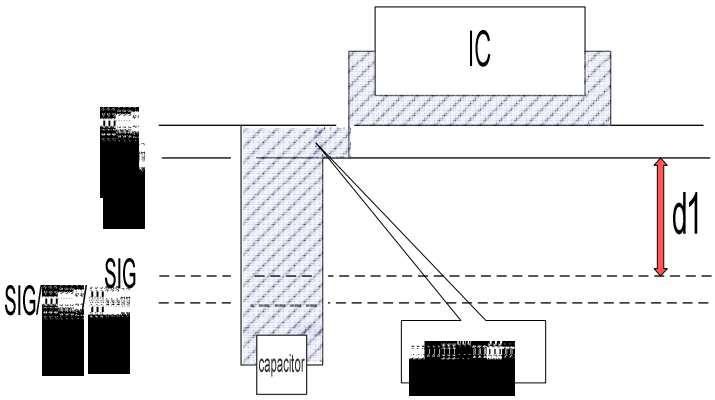


Figure 3.8. Poor placement of vias to power and ground planes

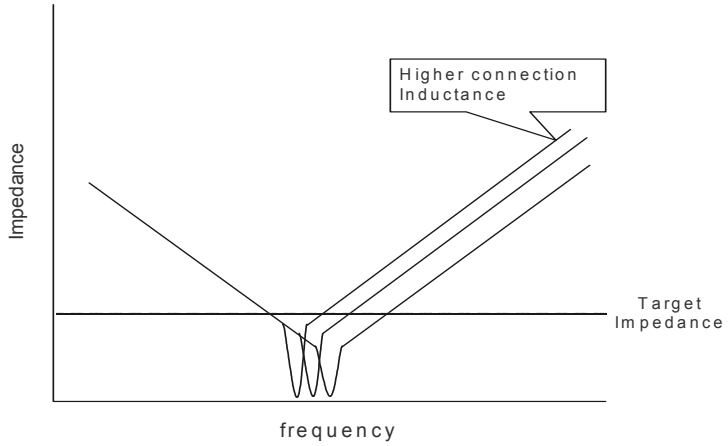


Figure 3.9. Increasing connection inductance increases the effective impedance to decoupling capacitors at high frequencies

3.1.1.5 Ground Plane below IC. The TEM cell standard allows a gap in the ground plane under the IC since some ICs may have too many pins to allow a contiguous ground plane. With a gap in the ground plane under the IC (as shown in Figure 3.10), some current return paths may be forced around the IC, increasing loop area for some pins and possibly redistributing current. In this case capacitive coupling may increase with increasing power bus impedance and inductive coupling may go up or down depending on whether the "gap" creates or fixes asymmetries in the pin current distribution.

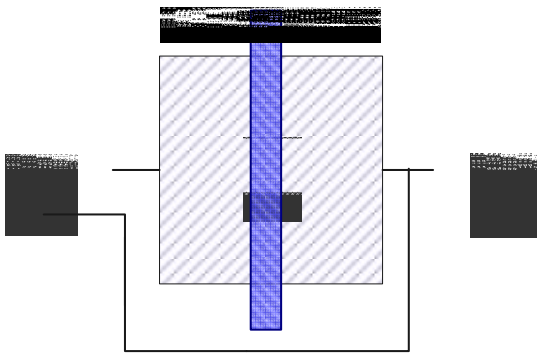


Figure 3.10. Current must flow around the gap in the ground plane below the IC

3.1.2. Test Configuration Variations

3.1.2.1 Clock Edge Rate. ICs may be fed by an external clock driver. This external clock may also couple to the TEM cell. The higher the clock edge rates, the more energy that may be coupled, as we see more high frequency harmonics in the signal spectrum. Capacitive as well as inductive coupling to the septum may increase with the edge rate. The overall impact of the clock driver may be small, however, as most emissions are, at least ideally, driven directly by the IC, rather than by signals to the IC.

3.1.2.2 Memory Location. Many ICs may use either external or internal memory. Using external memory forces repetitive use of I/O signals, which may switch at close to (or even above) the clock frequency. These signals may couple inductively or capacitively to the TEM cell, increasing measured emissions over the internal memory case.

3.1.2.3 Unused I/O. Switching of unused I/O may also affect the measured emissions in the TEM cell. If the IC is tested when these unused I/O are switched OFF it should be mentioned in the test report. Address Latch Enable (ALE) is one such I/O in many 8051 microcontrollers which can be inhibited if internal memory is being used, as it is switched at close to the clock frequency. These microcontrollers are often advertised as "low emissions" parts because the measured emissions with ALE OFF may be lower than with ALE switching.

3.1.2.4 Software. Software may change the emissions, depending on the actions performed by the instructions. Codes that produce better or worse emissions can be found with the help of the IEC-69167 standard.

3.1.3. Other Parameters. Other parameters that may be varied but are expected to have minimal effect on the TEM cell measurements are the amount of layer 4 used as GND, the distance between vias connecting return planes, via size, I/O configuration (input/output/bidirectional), and the way I/O are loaded.

3.1.4. Summary. The hypothesized influence of the different parameters is summarized in Table 3.1. In the table, L_{cap} represents inductance to the decoupling capacitor; L_{IC} represents inductance to the IC; $V_{N,\,IC}$ represents power bus noise voltage in the IC; $I_{N,\,IC}$ represents power bus noise current in the IC; TEM_C represents capacitive coupling to the TEM cell; TEM_L represents inductive coupling to the TEM cell. The

terms “big” and “small” are used as a relative comparison in this table. Overall, little effect is expected from PCB variations above a few hundred megahertz, since the IC package should dominate the impedance seen by the IC looking into the board. Differences above a few hundred megahertz will most likely be due to other effects, like the clock edge rate, the switching of I/O, and use of external memory.

RANK	VARYING PARAMETER	L_{cap}	L_{IC}	$V_{N,IC}$	$I_{N,IC}$	TEM_C	TEM_L	POTENTIAL EFFECT
	PCB Design Variation							
1	Increase distance between PCB layers	↑	–	↑	↓	↑	↓*	big (below few hundreds of MHz)
2	Change stackup from G/P/S/S to G/S/P/S							
	2a) Closely spaced vias to PWR and GND planes	↓		↓	↑	↓	↑*	big (below few hundreds of MHz)
	2b) Widely spaced vias to PWR and GND planes	↓		↑	↓	↑	↓	big (below few hundreds of MHz)
3	Decoupling capacitor							
	3a) Increase value of decoupling capacitor	–	–	↓	↑	↓	↑*	big (at low freq.)
	3b) Increase # of decoupling capacitors	↓	–	↓	↑	↓	↑	big (below few hundreds of MHz)
	3c) Increase decoupling capacitor placement distance	–	↑	↑	↓	↑	↓*	small (below few hundreds of MHz)
	3d) Increase decoupling capacitor connection inductance	↑	–	↑	↓	↑	↓*	big (below few hundreds of MHz)
4	Remove GND plane below DUT	–	↑	↑	↓↑	↑	↓↑	small (at high freq.)
5	Signal traces on IC side							
	5a) Increase length of the trace	–	↑	–	–	↑	↑	small (at high freq.)
	5b) Increase width of the traces	–	–	–	–	↑	–	small (at high freq.)
	Test Configuration Variation							
1	Increased clock edge rate	–	–	↑	↑	↑	↑	small
2	Inhibit ALE, other I/O	–	–	–	–	↓	↓	big
3	Use external memory rather than internal	–	–	–	–	↑	↑	big
4	Program running	–	–	–	–	↓↑	↓↑	big
	* small amount							

Table 3.1. Summary of anticipated influence of the test parameters

3.2. PRINTED CIRCUIT BOARD DESIGN

Two different 4-layer printed circuit boards were designed to test the influence of the design parameters listed in Table 3.1. Both boards were designed within the IEC Standard specifications, as discussed below.

3.2.1. IEC Standard Specifications for PCB Design. General guidelines for designing the integrated circuit test PCB are given in IEC 61967-1 [2] and IEC 61967-2 [3]. These standards state that the test PCB can be of any size or shape that mates with the slot (the opening) on the TEM cell. The number of layers in the PCB is not restricted. The minimum design requirements for a nominal 100 mm square 4 layer PCB and a nominal 100 mm square mating wall port are shown in the IEC standard and are repeated in Figure 3.11.

The standards state that only the device under test (the IC) should be mounted on the TEM-side of the test PCB (no other conductors or components are allowed to be mounted on this side except for conductors connecting to the IC, which should generally be minimized). All other supporting circuitry required for the proper functionality of the IC should be mounted on the other side of the board. The test PCB is to be mounted on the TEM cell in such a way that the IC is placed inside the TEM cell. Unused area on the IC side should be filled with metal in order to complete the TEM cell or GTEM cell wall over the port opening. The periphery of the IC side layer should be plated with tin, gold or silver to facilitate contact to the edge of the wall of the TEM cell. The area under the IC should be covered with ground whenever it is practical. Power bypass capacitors for the IC and terminations for different pins can be chosen according to manufacturers' recommendations.

3.2.2. PCB Designed for the Study. As shown in the previous section, the IEC standard allows many variations in the PCB design parameters, like the decoupling strategy, the number of layers in the PCB, the PCB stack-up, the ground plane under the IC, the thickness of the PCB, etc. As a result, boards designed by different engineers may give different emissions for the same IC. To test the influence of these parameters, two test boards were designed. The test PCBs were designed after careful review of the IEC standard to make sure they comply with the standard. Each PCB was built to test specific design parameters.

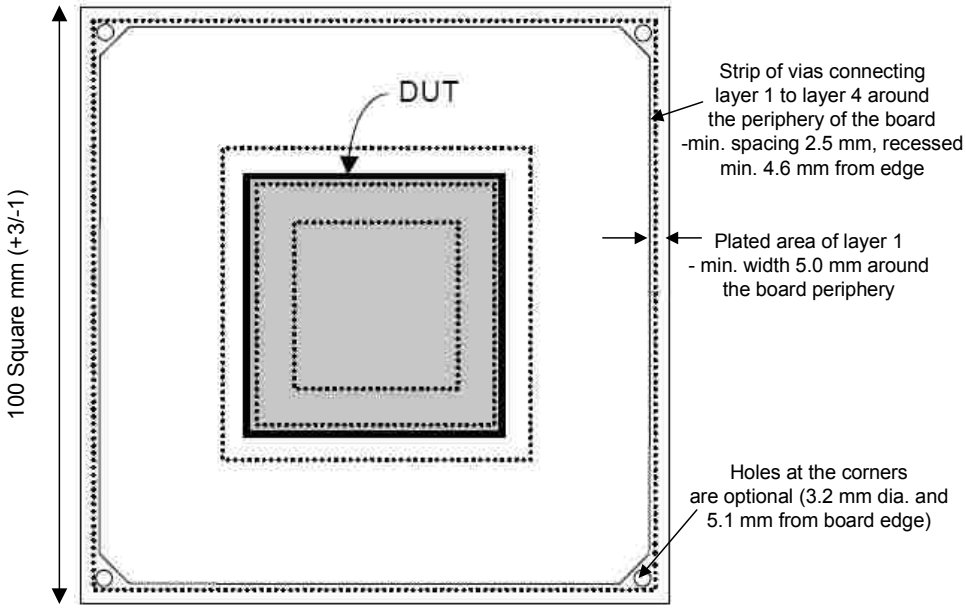


Figure 3.11. PCB design requirements-I (from [3] without permission)

3.2.2.1 8051 Compatible Microcontrollers Selected for Study. Three pin-for-pin compatible 8051 microcontrollers were chosen for the study. The useful specifications of the three microcontrollers as given in the data sheets are as follows. Appendix C shows the complete specifications of these ICs.

ATMEL (AT89C51RB2)

• 80C52 Compatible
  – 8051 Pin and Instruction Compatible
  – Four 8-bit I/O Ports
  – Three 16-bit Timer/Counters
  – 256 Bytes Scratch Pad RAM
• ISP (In-system Programming) Using Standard VCC Power Supply
• High-speed Architecture
  – In Standard Mode:
    40 MHz (Vcc 2.7V to 5.5V, both Internal and external code execution)
  – 16K/32K Bytes On-chip Flash Program/Data Memory
  – Byte and Page (128 Bytes) Erase and Write
• On-chip 1024 Bytes Expanded RAM (XRAM)
  – Software Selectable Size (0, 256, 512, 768, 1024 Bytes)
  – 256 Bytes Selected at Reset for TS87C51RB2/RC2 Compatibility
• Dedicated Baud Rate Generator for UART
• Low EMI (Inhibit ALE)

• Power Control Modes
  – Idle Mode
  – Power-down Mode
  – Power-off Flag
• Power Supply:
  – 2.7 to 3.6 (3V Version)
  – 2.7 to 5.5V (5V Version)
• Packages: PDIL40, PLCC44, VQFP44

PHILIPS (P89V51RB2)

• 80C51 CPU
• 5 V operating voltage from 0 MHz to 40 MHz
• 16 kB of on-chip flash user code memory with ISP and IAP
• SPI and enhanced UART
• Four 8-bit I/O ports with three high-current port 1 pins (16 mA each)
• Three 16-bit timers/counters
• Programmable watchdog timer
• Low EMI mode (ALE inhibit)
• Low power modes
  – Power-down mode with external interrupt wake-up
  – Idle mode
• DIP40, PLCC44 and TQFP44 packages

MAX-DALLAS (DS89C430)

• High-Speed 8051 Architecture
  – One Clock-Per-Machine Cycle
  – DC to 33MHz Operation
  – Single Cycle Instruction in 30ns
• On-Chip Memory
  – 16kB/64kB Flash Memory
  – In-Application Programmable
  – In-System Programmable Through Serial Port
  – 1kB SRAM for MOVX
• 80C52 Compatible
  – 8051 Pin and Instruction Set Compatible
  – Four Bidirectional, 8-Bit I/O Ports
  – Three 16-Bit Timer Counters
  – 256 Bytes Scratchpad RAM
• Power-Management Mode
  – Programmable Clock Divider
  – Automatic Hardware and Software Exit
• Peripheral Features
  – Two Full-Duplex Serial Ports
  – Electromagnetic Interference (EMI) Reduction

3.2.2.2 PCB Schematic Design. The PCBs were designed with the test parameters in mind, as well as other restrictions. The microcontrollers should be able to be programmed in-system so that the ICs do not have to be unsoldered to change the software. There should be a provision to be able to program the external flash memory in-system and for the IC to fetch instructions from the external flash memory. The PCB should be flexible enough to test all three microcontrollers. Application notes and data sheets for all three IC manufacturers were carefully reviewed before coming up with the schematics [9], [10], [11]. The final schematic was designed using Altium Designer 6 [12].

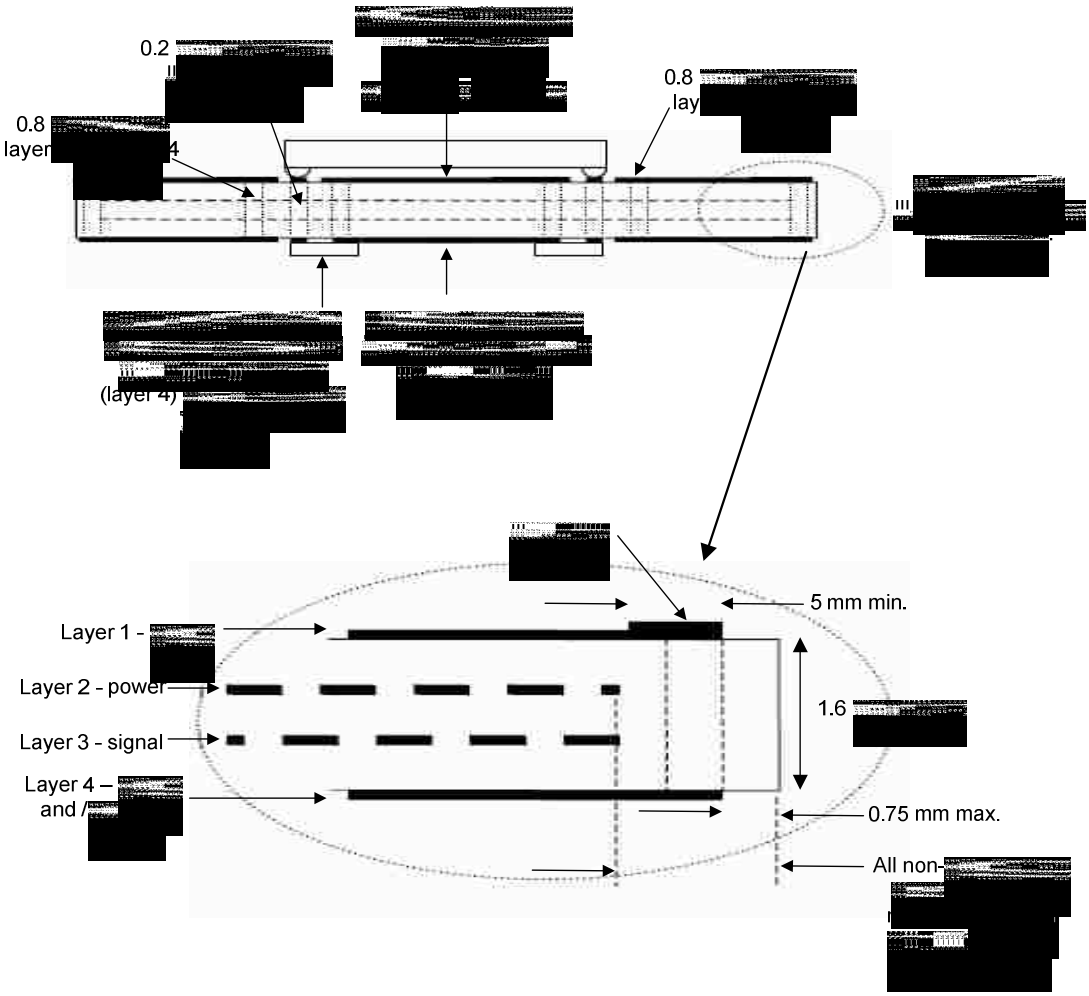


Figure 3.12. PCB design requirements-II (from [3] without permission)

Figure 3.13 shows the schematic diagram of one test board. The schematic contains a voltage regulator module in order to supply a constant voltage of 5V to all the components on the board. The purpose of the Zener diode in the voltage regulator module is to protect the components from over voltage and negative voltage. The regulator module also has two bulk decoupling capacitors and an LED that glows when there is a 5V supply to the board. The schematic uses a D connector and a MAX 232 IC (MAX232CSE) for in-system programming of the microcontroller. There is also circuitry for software reset of the microcontroller while programming [13], [14]. A dip-4 switch is used to set the voltage levels of control pins of the microcontroller and external access circuitry (PSEN, ALE, EA and ISP). A buffer (74AC573SJ) is used to latch the lower 8-bits of the address while accessing external memory. The presence of the latch also facilitates the use of those 8-bits as data bits while transferring data to and from the external memory (AT29C512-70TI) when they are not used as address bits. The NOT (MM74HCT04SJ) and NAND (MM74HC00SJ) ICs were used for implementing the glue logic required for external flash programming [15], [16], [17]. LEDs are connected to port pins of the IC to confirm the program works. An LED is also connected at the output of the MAX232 which glows whenever the IC is being programmed. Another LED is connected to the ALE pin for debugging. Decoupling capacitors are placed near each and every component. Extra decoupling capacitors are placed near the microcontroller to implement different decoupling strategies which vary the number, amount, connection length, location and connection method of the decoupling capacitors. The schematic also has provisions to allow compatibility with the particular ICs being used. For example, the Max-Dallas IC has two Vcc pins and three Vss pins in comparison to the other two ICs who have one Vcc pin and one Vss, with the other pins unconnected. To account for this difference the unconnected pins are connected to ground/Vcc through a resistor in the schematic. When the IC which has two Vcc pins and three grounds is being used these pins are connected to either Vcc or ground using a zero ohm resistor; otherwise, the pins are left unconnected.

3.2.2.3 PCB Layout. Before laying-out the board, the PCB design guidelines discussed in the IEC standard were carefully studied. The layout of the components was chosen so that it was convenient to connect the components together. A strip of vias were

placed at the edge of the board, and on the inner and outer sides of the pins of the IC where ever possible as specified in the IEC standard shown in Figure 3.11.

Two different four layer PCBs were designed which have stack-ups GND/PWR/SIG/SIG (starting from the IC side of the PCB) and GND/SIG/PWR/SIG. Except for the stack-up, these two PCBs are the same. It was assumed that varying the thickness of the PCB will have nearly the same effect on emissions as varying the stack-up so an additional board with different thickness was not built. Pads for the decoupling capacitors were arranged such that some capacitors are far away from the IC, some are as near as possible to the IC, some have long connection trace lengths, and so forth, covering all the planned decoupling capacitor arrangements. To give provision for testing the effect of the traces on the IC side, each ground pin of the IC was connected to a long trace and these traces could be connected to the ground either near the IC (short trace) or at the far end of the trace (long trace). Provisions for wide traces were achieved by placing another trace right beside these ground traces (in parallel) and providing pads to connect these traces to the ground trace at both ends. Extending/not extending the ground plane below the IC was achieved by placing a copper fill below the IC, which was not connected to the usual ground. This copper fill has seven pads which could be used to connect to the ground when ever the ground plane was to be extended below the IC; otherwise, the pads were left unconnected. Pads are also provided near the clock input of the board to mount a low pass filter when needed. The completed layout of the PCB is shown in Figure 3.14. The arrangement of the decoupling capacitors, the traces on the IC side, and the ground fill below the IC are shown in Figure 3.15. The finished thickness of the PCB was approximately 62 mils, with core approximately 42 mils thick. The length and width of the trace used on the IC side was approximately 6 mm and 1 mm respectively.

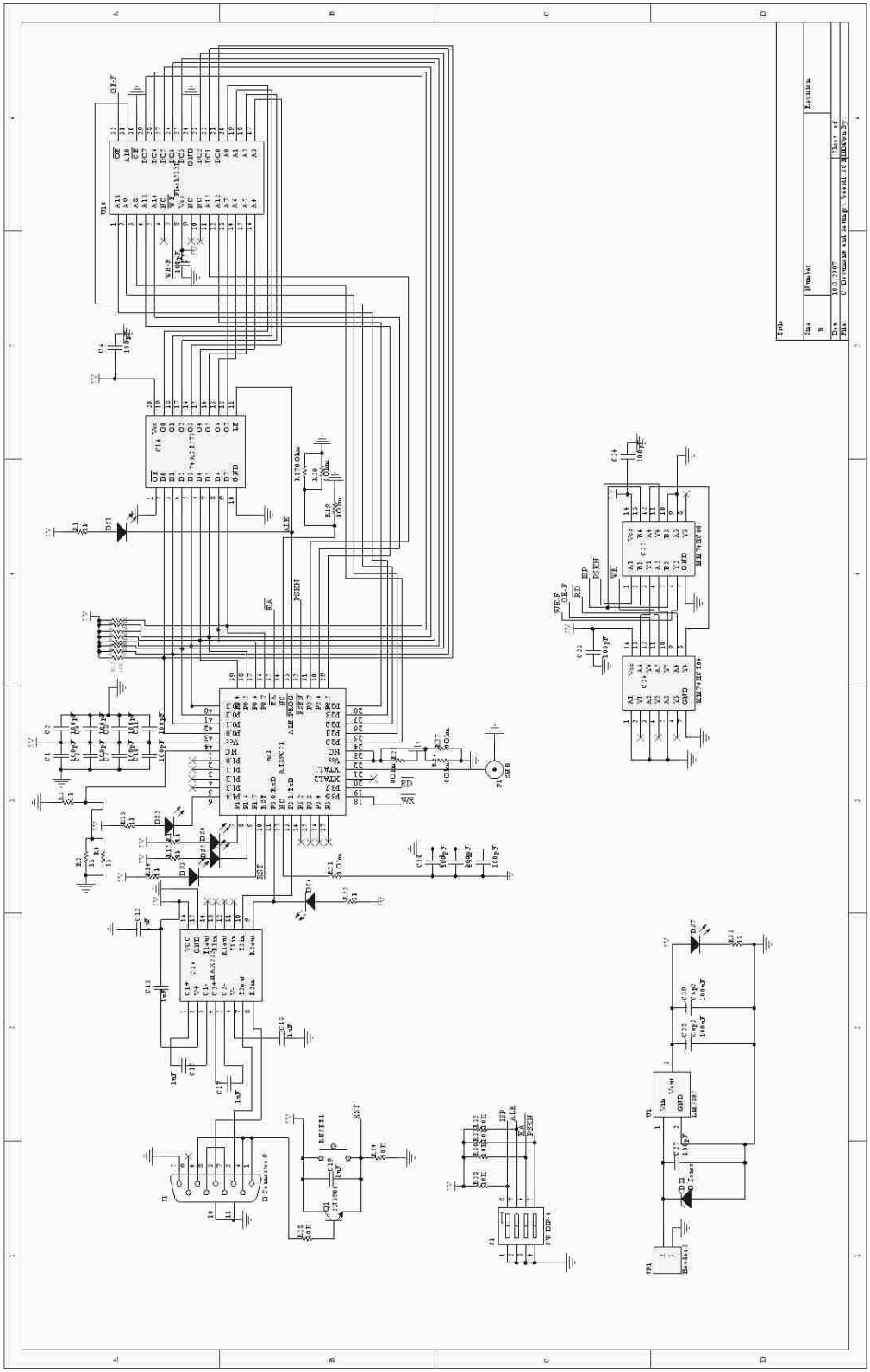


Figure 3.13. Completed Schematic of the printed circuit board

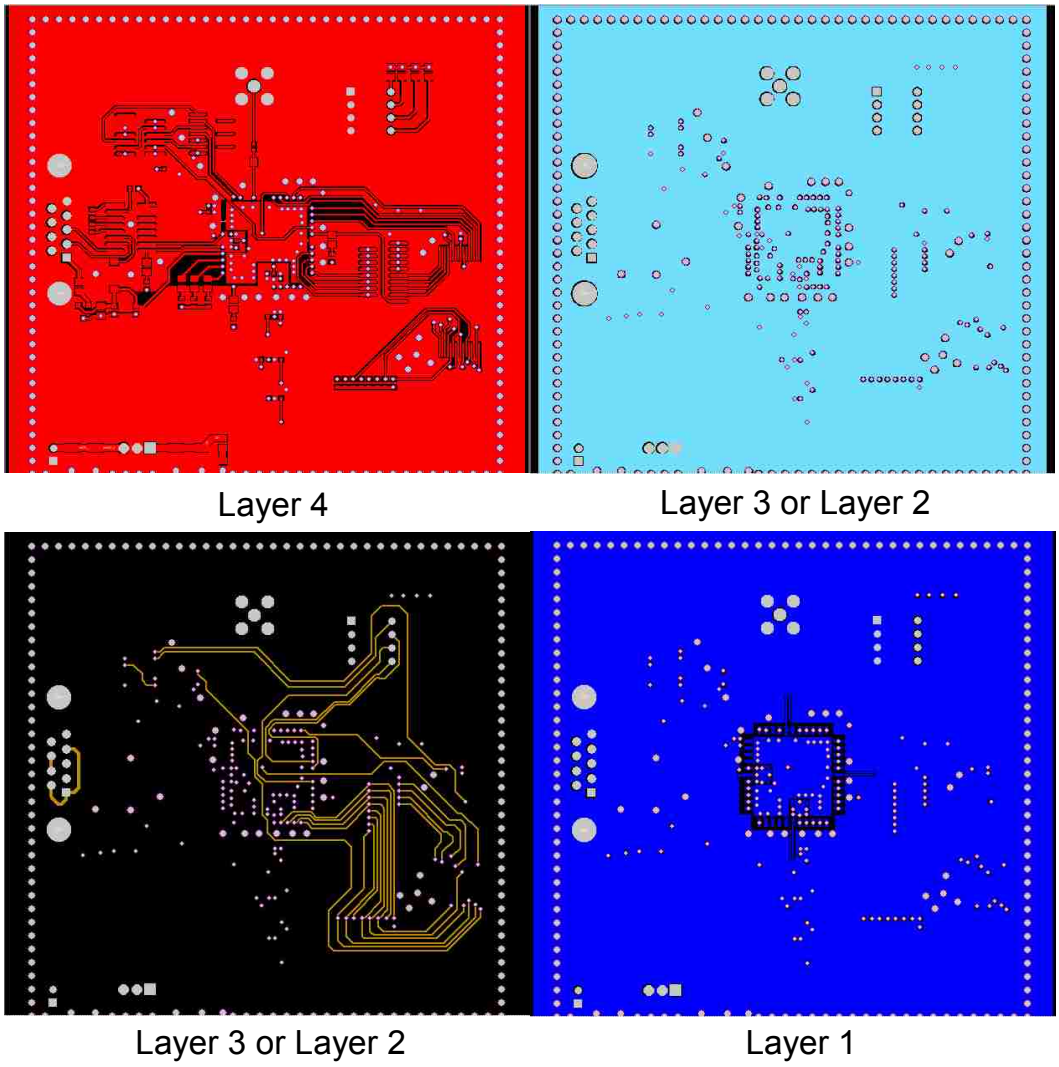


Figure 3.14. Completed layout of the printed circuit board

3.2.2.4 Completed PCB. The completed system is shown in the Figure 3.16. The completed PCB generally worked as designed; however, the external flash memory could not be programmed. The reason might be an error in the in-application programming software or the schematic design. The cause is unknown. For this reason, emissions were not tested when using external memory.

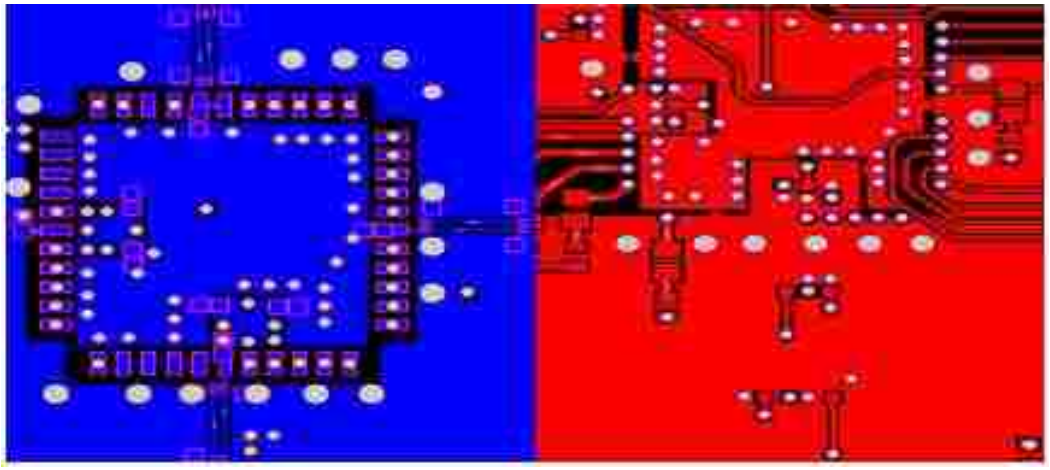


Figure 3.15. Layout used to achieve long wide traces (in the DUT layer (left)), decoupling capacitor connections (right) and ground pad under the IC

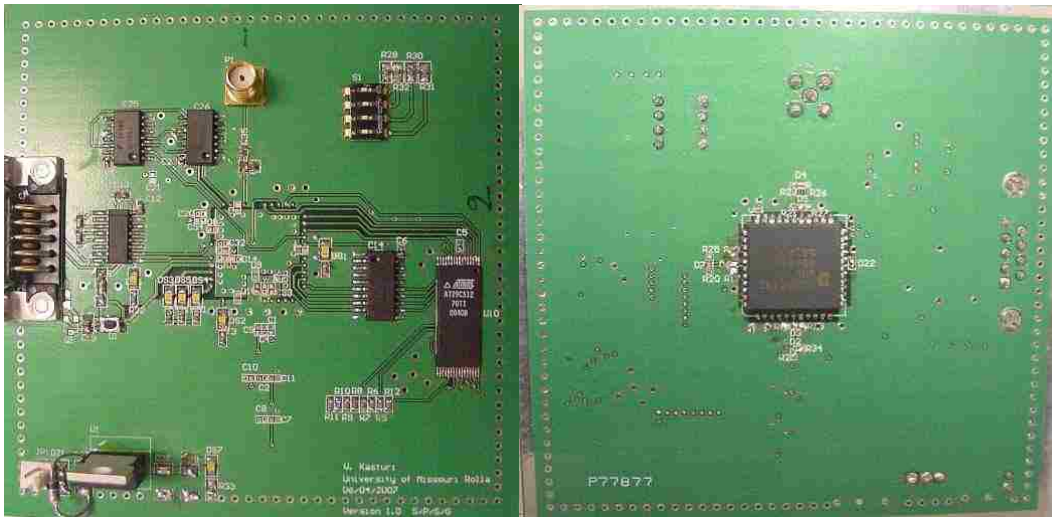


Figure 3.16. Completed Printed Circuit Board, Top view (left); bottom view (right)

4. RESULTS

Measurements were performed using two different boards, board 1 with stack-up GND/PWR/SIG/SIG and board 2 with stack-up GND/SIG/PWR/SIG. Except for the stack-up, these two boards were the same. The measurement setup is explained in the first section of this chapter. The Noise floor is characterized in the second section. The results obtained from measurements of the boards are shown in Section 4.4 to Section 4.8. The results show the effect of variations in PCB design, switching of unused I/O, clock edge rate and software on the TEM cell emissions. Finally, emissions are compared among the three manufacturers for all five different board setups.

4.1. MEASUREMENT SETUP

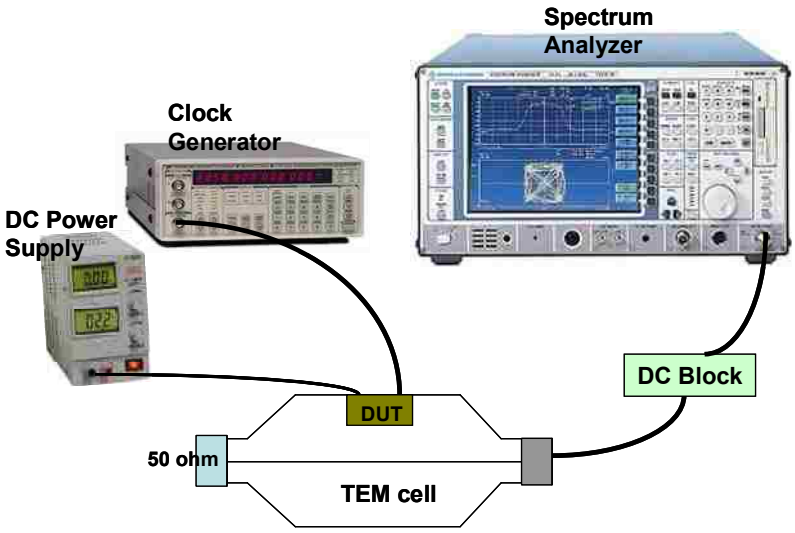


Figure 4.1. Measurement setup

The measurement setup is shown in Figure 4.1. One port of the TEM cell was connected to a 50-ohm matched load. The other port was connected to the spectrum analyzer to view the power coupled to the septum of the TEM cell as a function of frequency. The IC test printed circuit board was powered by an external power supply.

The clock signal for the operation of the IC was supplied from an external clock generator. The operating frequency was 33 MHz for each IC tested.

The spectrum analyzer was set in peak detect mode and for max hold. Resolution bandwidth and video bandwidth were set to 10 KHz and 30 KHz respectively. RF attenuation was set at 10 dB, giving a noise floor of approximately 12 dBμV, as discussed in section 4.3. Start and stop frequencies were set at 1 MHz and 1 GHz respectively, with 500 points sampled in the total range. The sweep time was 25 sec. Three measurements were taken at different times for each set-up and averaged, with each measurement taken for approximately 7 minutes.

4.2. ACCURACY OF MEASUREMENTS

To define how much variation might be expected in measurements of the same set-up, measurements were taken at three different times for a board setup implemented on board 2 such that there were no decoupling capacitors (both bulk and local), there was no ground plane under the IC, IC side uses long and wide traces, program 2 was used, and an RC low-pass filter (R = 100 Ohm, C = 100 nF) was present in the path of the clock trace. A difference plot for the three measurements is shown in Figure 4.2. Measurement accuracy among any two measurements was always better than approximately 2.5 dB. Since, results are presented using the average of three results taken at different times, if error is assumed to be Gaussian distribution, accuracy of the results should generally be better than approximately $2.5/\sqrt{3} \approx 1$ dB.

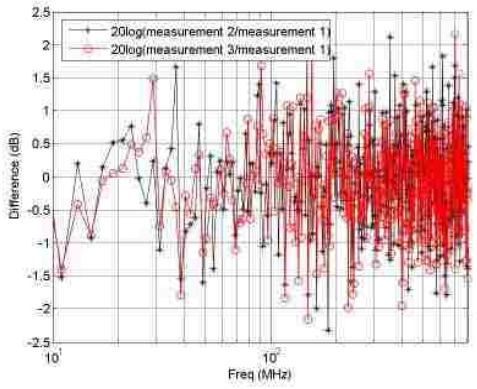


Figure 4.2. Accuracy of measurements

4.3. NOISE FLOOR CHARACTERIZATION

The noise floor of the measurement setup is shown in Figure 4.3. This measurement was performed with the measurement setup shown in Figure 4.1, except that the clock generator and the DC power supply were switched OFF. The noise floor of the setup was approximately 12 dBμV.

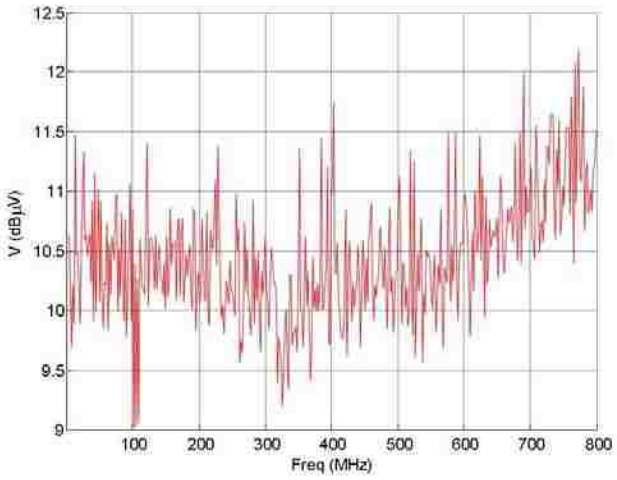


Figure 4.3. Noise floor of the measurement setup

4.4. EFFECT OF PRINTED CIRCUIT BOARD DESIGN VARIATIONS

As outlined earlier, the design variations that were studied include the distance between the PCB layers, the decoupling strategy, stack-up, the width and length of traces in the TEM cell, and the presence of a ground plane below the IC. The parameters tested in this section can be divided into two sets. set 1 includes parameters which dominate the variations in the emissions in the low frequency range (below a few hundred MHz) and set 2 includes parameters which dominate the variations in the emissions in the high frequency range (above a few hundred MHz). Set 1 includes the decoupling strategy as it is only effective up to a few hundred MHz [18]. Set 2 includes the presence of a ground plane under the IC and the presence of wide and long traces to the IC, stack-up, and

distance between the layers. These parameters cause variations in the loop area of power return currents, which may increase coupling at high frequencies.

Initially, the idea was to study the variation of each parameter individually. The influence of changing the value, number, and location was studied by a series of measurements. Different combinations of the above were tested. The measured emissions did not seem to change significantly from one case to another among these combinations. One such result is shown in Figure 4.4. In the figure, the case 1 setup includes one decoupling capacitor connected far away from the IC. The case 2 setup includes three decoupling capacitors connected right below the IC. The change in the emissions at low frequencies was approximately 1dB, which is below the accuracy of the measurement. At high frequencies, variations were generally less than 2 dB. This result indicates that the decoupling strategy alone has little effect on the TEM cell emissions. At this stage, the idea of testing the influence of parameters individually was ruled out and the idea to study the typical variation in the emissions from a board using what are typically bad design strategies and a board using typically good design strategies was pursued. Two different test boards were designed, which were named the case 1 and case 2 setups:

- Case 1: Using board 1, the ground plane is extended under the IC, decoupling capacitors (both local and bulk) are present, very short traces on the IC side are used, and an RC low-pass filter (R = 100 Ohm, C = 100 nF) is present in the path of the clock trace.
- Case 2: Using board 2 with no decoupling capacitors (both bulk and local), no ground plane under the IC, long and wide traces on the IC side, and an RC low-pass filter (R = 100 Ohm, C = 100 nF) is present in the path of the clock trace.

Emission measurements were performed on both these boards while running a program that thoroughly exercised the software, later called program 2in this thesis. The results plotted in Figure 4.5 through Figure 4.16 show the impact of variations of these parameters on the measured emissions from the three ICs tested.

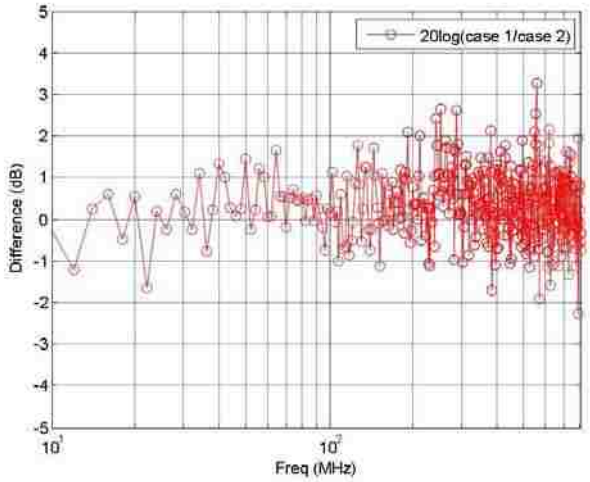


Figure 4.4. Difference plot for emissions measured with decoupling capacitors connected near and far away from the IC

4.4.1. Atmel. As we can see in Figure 4.5 and Figure 4.6, PCB design variations between the boards typically change emissions at low frequencies (up to 60 MHz) in the orientation 1 measurement by approximately 3 dB, with case 2 yielding higher emissions. For orientation 2 (Figure 4.7and Figure 4.8) the emissions are changed at low frequencies (from 30 MHz to 150 MHz) by approximately 2 dB. While orientations 3 and 4 are not shown here (see Appendix A), they are similar to orientations 1 and 2 respectively. Peak emissions are due to harmonics of the clock (spread through out the frequency range) which are multiples of 33 MHz and harmonics from another source apparently operating at one-half the clock frequency. While emissions at clock harmonics may vary by as much as 5 dB with design variations at high frequencies, PCB design variations do not uniformly harm the emissions as the emissions will increase for one case in some orientations and decrease in other orientations. The fact that results differ among orientations indicates that inductive or a combination of inductive and capacitive coupling dominates, though the coupling mechanism was not carefully studied.

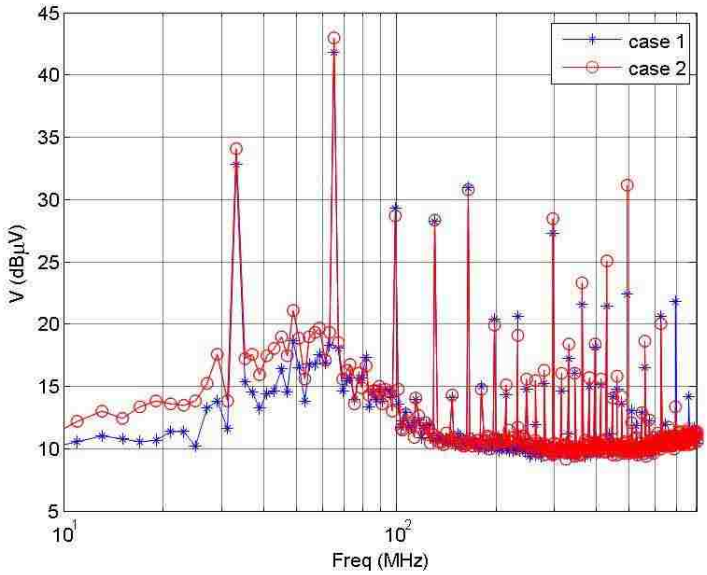


Figure 4.5. Comparison between TEM cell emissions for case 1 and case 2 (orientation 1, Atmel)

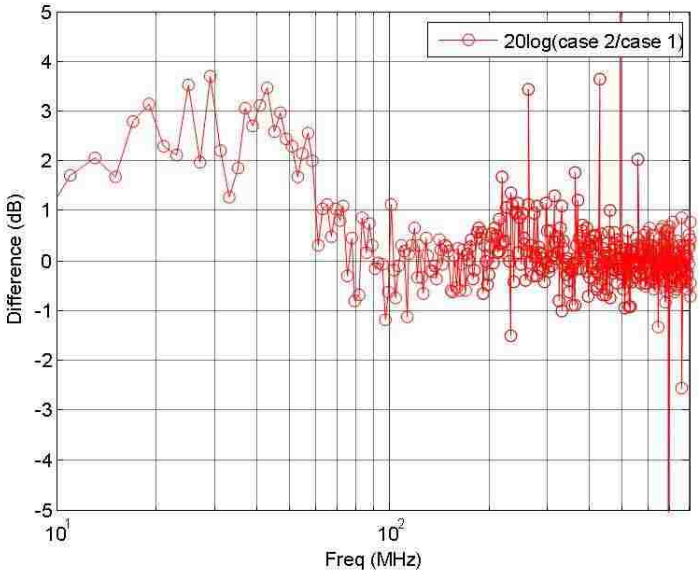


Figure 4.6. Difference between emissions for case 1 and case 2 (orientation 1, Atmel)

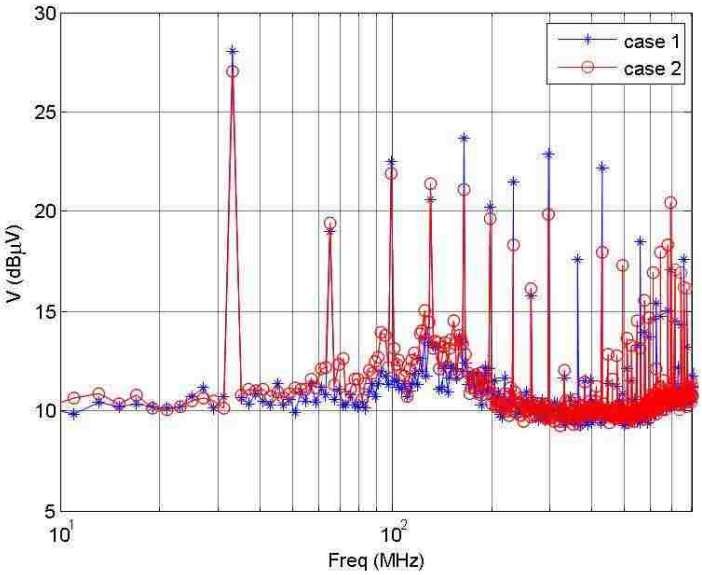


Figure 4.7. Comparison between TEM cell emissions for case 1 and case 2 (orientation 2, Atmel)

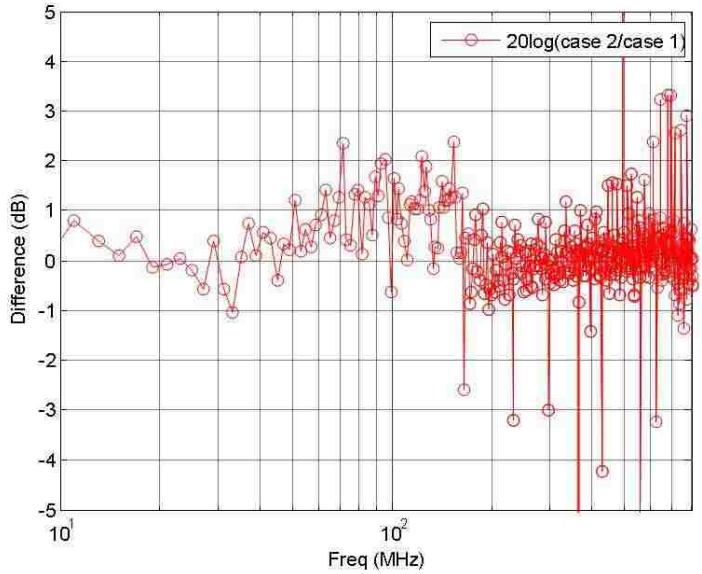


Figure 4.8. Difference between emissions for case 1 and case 2 (orientation 2, Atmel)

4.4.2. Philips. Similar to the Atmel IC the emission levels for the Philips IC in the low frequency range (below 70 MHz) is approximately 3 dB stronger in orientation 1 for case 2 than for case 1 as shown in Figure 4.9 and Figure 4.10. Orientation 2 does not show a similar increase as seen in Figure 4.11 and Figure 4.12. Orientation 3 and 4 results are similar to orientations 1 and 2 respectively (see Appendix A). For the Philips IC, the peak emissions only occur at harmonics of the clock. There are no large contributions at other frequencies (i.e. at harmonics of half the clock) as seen for the Atmel IC. The high frequency behavior is otherwise similar to the Atmel IC. Similar to the Atmel IC, neither case 1 nor case 2 shows better overall emissions, as emissions are higher for one case in some orientations and lower in the other orientations. The fact that results differ among orientations indicates that inductive or a combination of inductive and capacitive coupling dominates, though the coupling mechanism was not carefully studied.

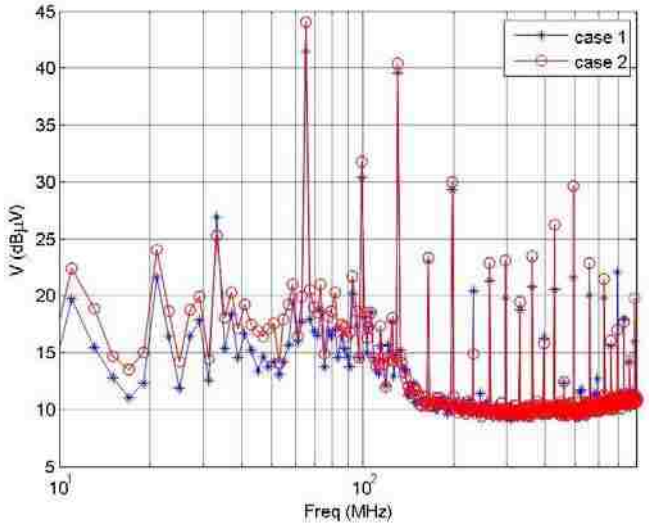


Figure 4.9. Comparison between TEM cell emissions for case 1 and case 2 (orientation 1, Philips)

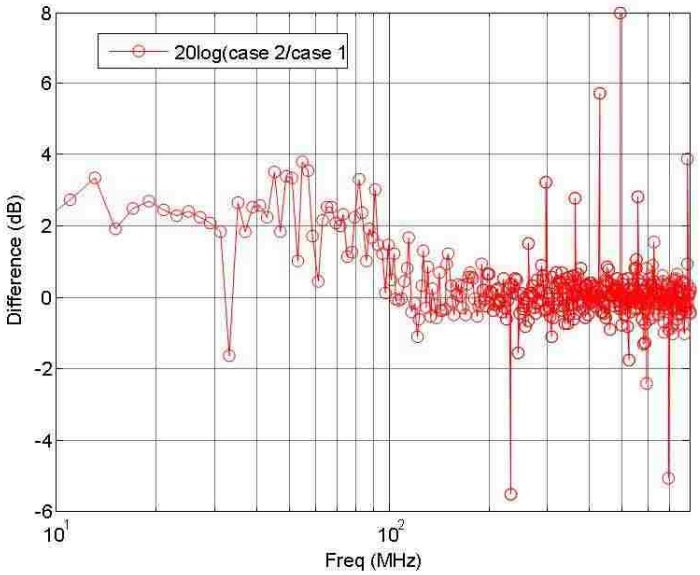


Figure 4.10. Difference between emissions for case 1 and case 2 (orientation 1, Philips)

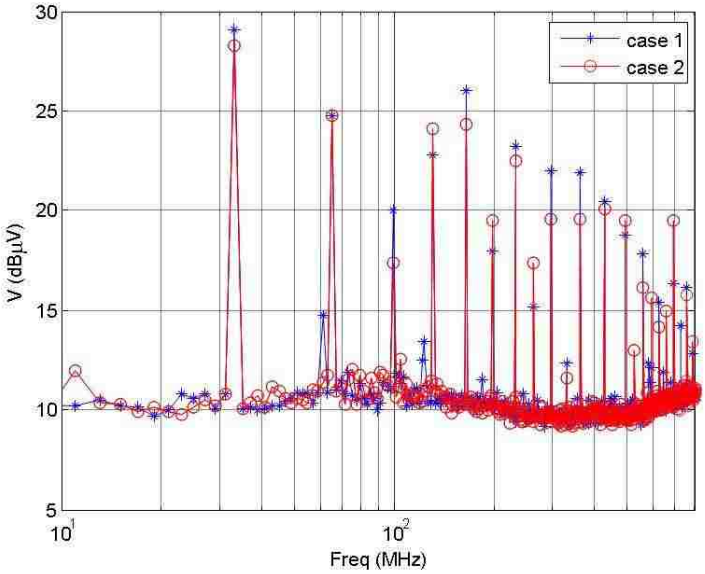


Figure 4.11. Comparison between TEM cell emissions for case 1 and case 2 (orientation 2, Philips)

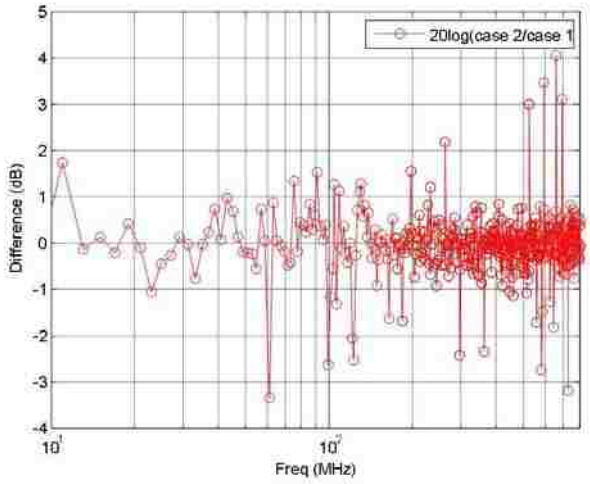


Figure 4.12. Difference between emissions for case 1 and case 2 (orientation 2, Philips)

4.4.3. Max-Dallas. Figure 4.13 through Figure 4.16 show the measurements for the Max-Dallas IC. Measurements for case 2 were generally higher than for case 1 by up to 6 dB up to about 500-600 MHz for all the orientations, though case 1 was higher at some frequencies. Beyond 600 MHz, neither case dominated. Other orientation results are shown in Appendix A.

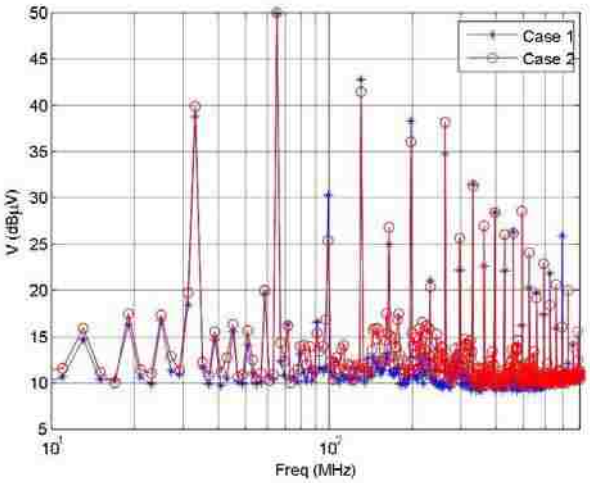


Figure 4.13. Comparison between TEM cell emissions for case 1 and case 2 (orientation 1, Max-Dallas)

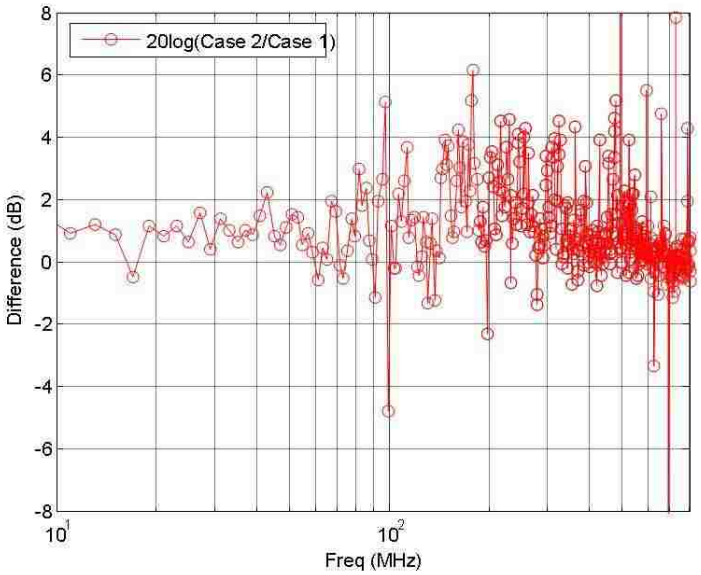


Figure 4.14. Difference between emissions for case 1 and case 2 (orientation 1, Max-Dallas)

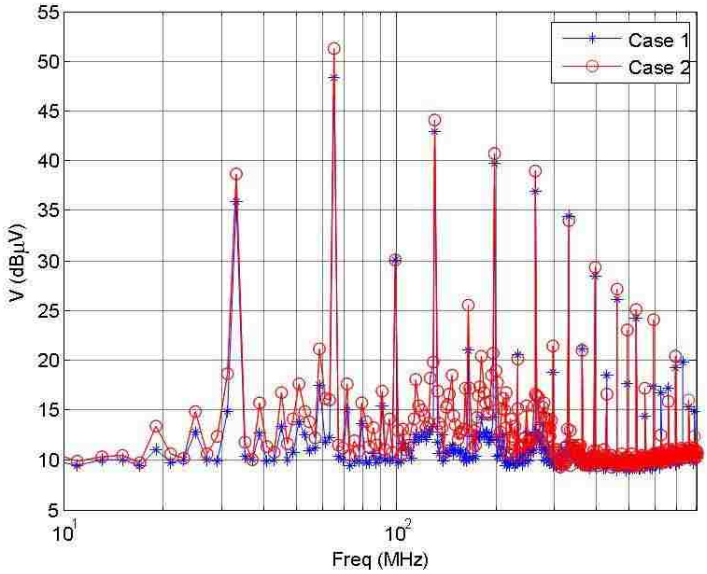


Figure 4.15. Comparison between TEM cell emissions for case 1 and case 2 (orientation 2, Max-Dallas)

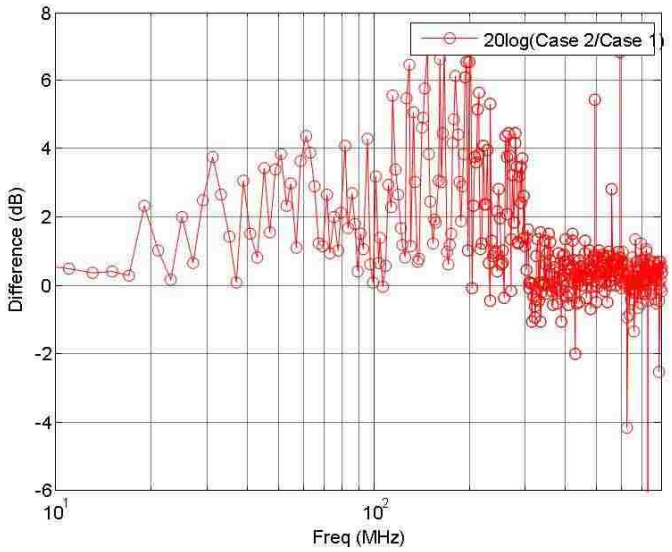


Figure 4.16. Difference between emissions for case 1 and case 2 (orientation 1, Max-Dallas)

4.5. EFFECT OF CLOCKING OF UNUSED I/O PINS

The switching of I/O may also effect emissions, and may be particularly important when switching is optional. The effect of switching I/O pins on the measured emissions was studied for the three ICs. This test was performed using the setup from case 1, which has the ground plane extended under the IC, uses both local and bulk decoupling capacitors, uses very short traces on the IC side, runs program 2, and uses an RC low-pass filter (R = 100 Ohm, C = 100 nF) in the path of the clock trace on board 1. The address latch enable (ALE) pin was tested here because this pin is only used when the microcontroller accesses the external memory. In the standard 8051 microcontroller, this pin switches at a constant rate close to the clock frequency, even when external memory is not being accessed by the microcontroller. Many microcontroller IC manufacturers provide an option to turn off this ALE pin when the microcontroller is not accessing external memory, by setting a control bit in the software code. Two configurations were tested. In one case the ALE pin is turned OFF so it switches only when the IC excesses external memory or expanded RAM and in the other case the ALE

is switching all the time. Since our test setup did not use external memory, the ALE was never required to switch.

4.5.1. Atmel. The effect of switching the ALE pin on the measured emissions of the Atmel IC is shown in Figure 4.17 through Figure 4.20. Only orientations 1 and 2 are shown as the results of orientation 3 and 4 are similar to orientations 1 and 2 respectively (see Appendix A). The emissions are increased by about 5 to 20 dB throughout the frequency range when the pin was switching than when it was not though little change was observed at the peak emissions. Peak emissions occurred at the clock frequency harmonics. The ALE pin was switching at $1/6^{th}$ the clock frequency. By observing all the orientations it can be said that both capacitive and inductive coupling increase when the ALE pin was switching. At high frequencies (above few hundred MHz) the dominant coupling mechanism was inductive. We see higher emissions in orientation 1 figure for the ALE switched off case than the ALE switched on for frequencies below 100 MHz. This is due to frequency spreading because of ALE pin switching occasionally while the program running inside the (program 2) IC is accessing the expanded RAM.

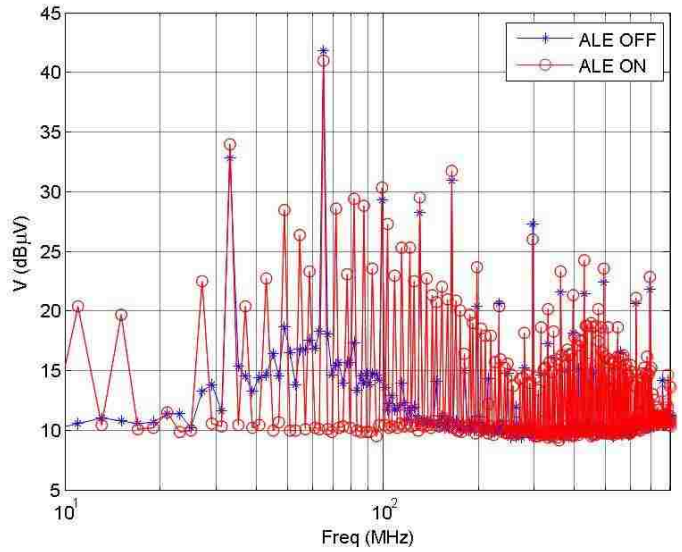


Figure 4.17. TEM cell emissions with and without ALE switching (orientation 1, Atmel)

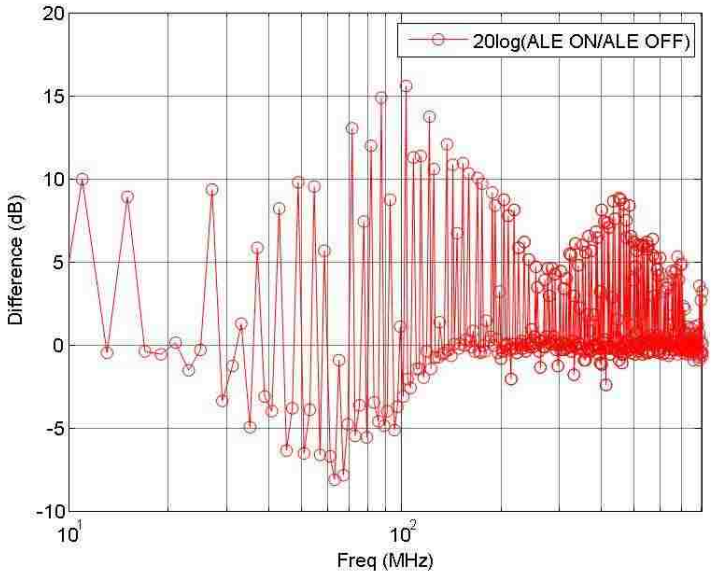


Figure 4.18. Difference in TEM cell emissions with and without ALE switching (orientation 1, Atmel)

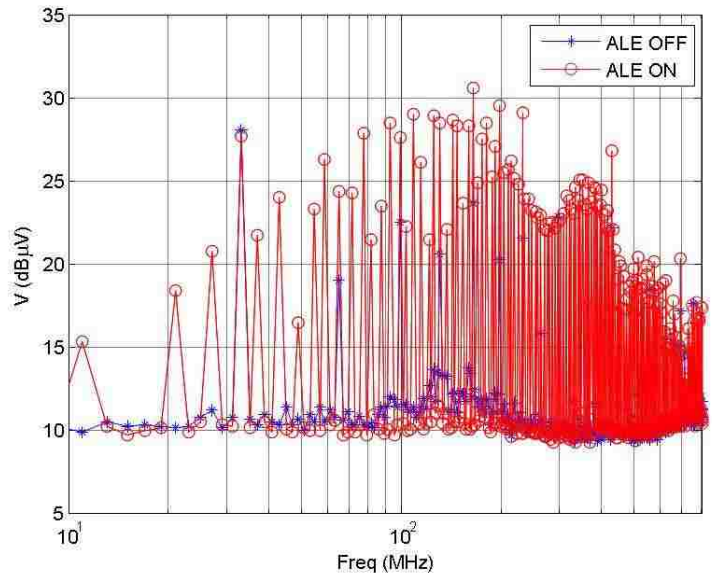


Figure 4.19. TEM cell emissions with and without ALE switching (orientation 2, Atmel)

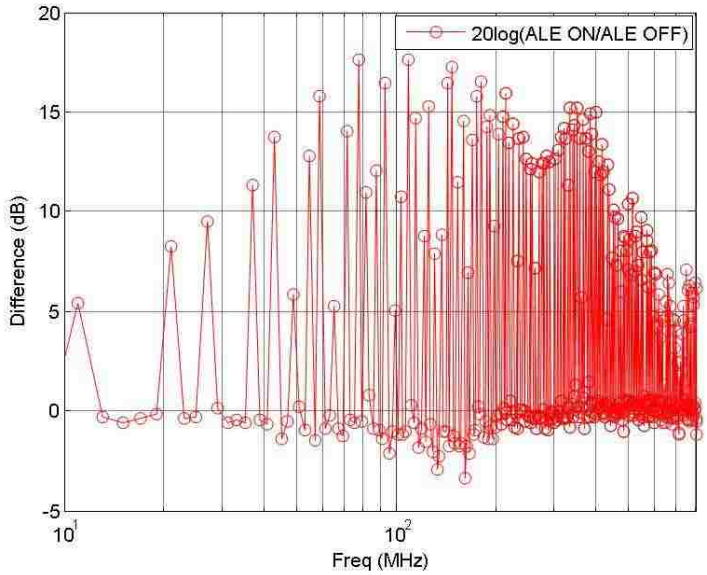


Figure 4.20. Difference in TEM cell emissions with and without ALE switching (orientation 2, Atmel)

4.5.2. Philips. Figure 4.21 through Figure 4.24 show the effect of switching the ALE pin on the measured emissions of the Philips IC. Results from orientations 1 and 2 are similar to 3 and 4 respectively. Use of ALE pin caused a 5 to 15 dB increase in the emissions up to 200-400 MHz in both the orientations. As before, however, the peak emissions at clock frequency harmonics did not change significantly. The switching frequency of the ALE pin was $1/6^{th}$ the clock frequency. Both capacitive and inductive coupling increased when the ALE pin was switching. In the high frequencies (above 200 MHz) inductive coupling was dominant. In orientation 1, similar to the Atmel IC the emissions from ALE switched off case are higher than from ALE switched on case at low frequencies due to frequency spreading because of ALE pin switching occasionally while the program running inside the (program 2) IC is accessing the expanded RAM.

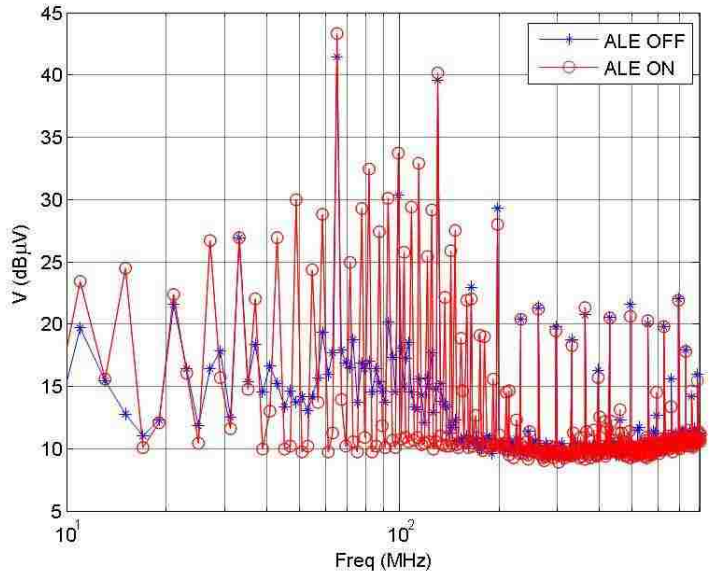


Figure 4.21. TEM cell emissions with and without ALE switching (orientation 1, Philips)

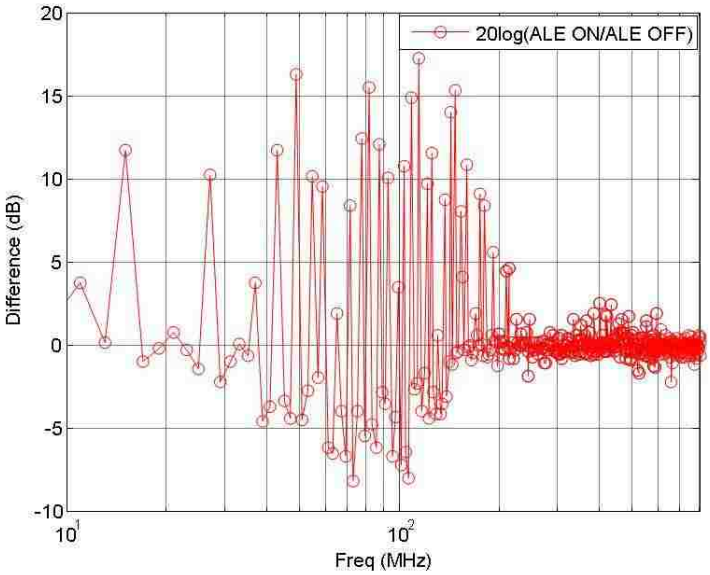


Figure 4.22. Difference in TEM cell emissions with and without ALE switching (orientation 1, Philips)

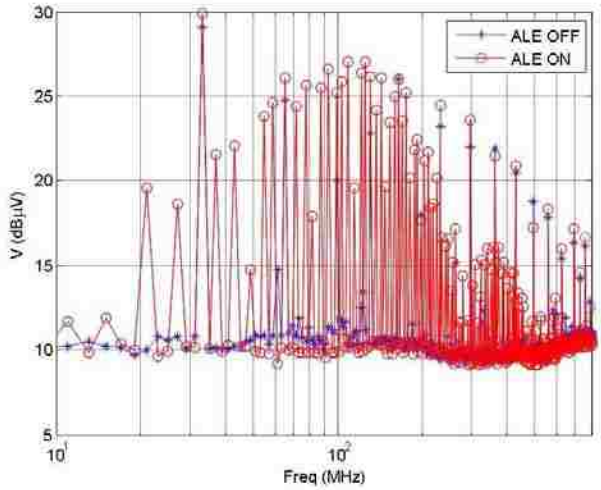


Figure 4.23. TEM cell emissions with and without ALE switching (orientation 2, Philips)

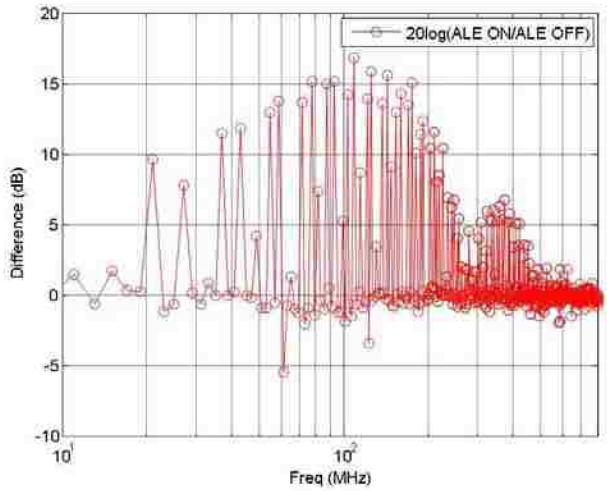


Figure 4.24. Difference in TEM cell emissions with and without ALE switching (orientation 2, Philips)

4.5.3. Max-Dallas. Switching of the ALE pin increased the emissions above 100 MHz by approximately 10-25 dB for both the orientations of the Max-Dallas IC as shown in Figure 4.25 through Figure 4.28. Contrary to the Atmel and Philips ICs the Max-Dallas ALE pin is switching at approximately the clock frequency. Below 100 MHz there is no significant difference between the cases with and without the ALE pin

switching and there are no new harmonics produced in the spectrum due to ALE switching. There was a noticeable change in the peak emissions at clock harmonics. A careful review of all four orientations shows that both capacitive coupling and inductive coupling increased when the ALE pin is turned on.

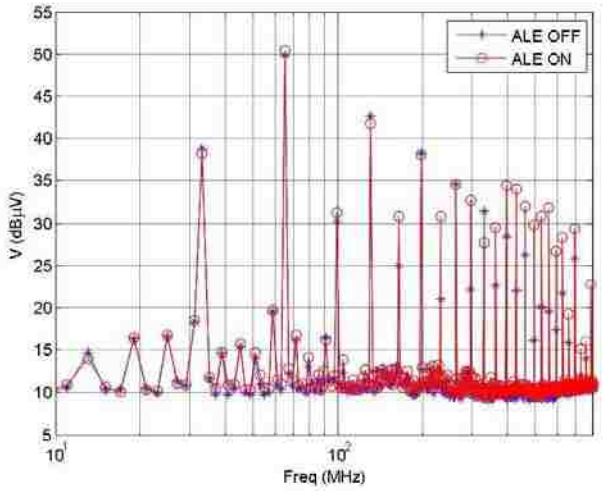


Figure 4.25. TEM cell emissions with and without ALE switching (orientation 1, Max-Dallas)

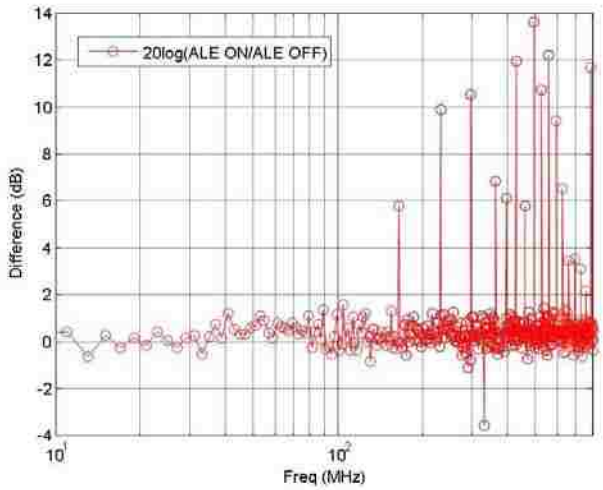


Figure 4.26. Difference in TEM cell emissions with and without ALE switching (orientation 1, Max-Dallas)

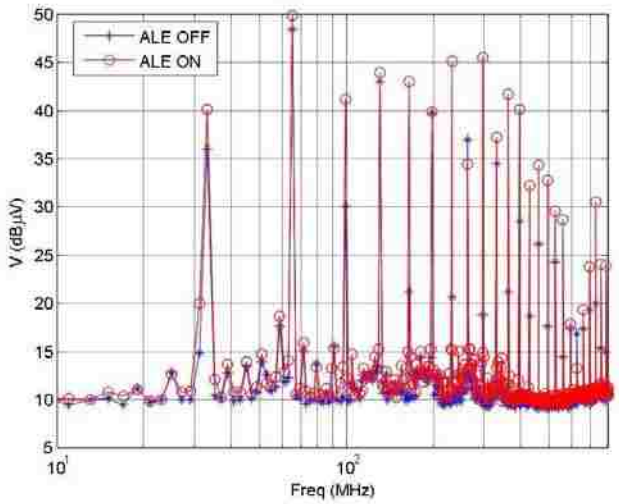


Figure 4.27. TEM cell emissions with and without ALE switching (orientation 2, Max-Dallas)

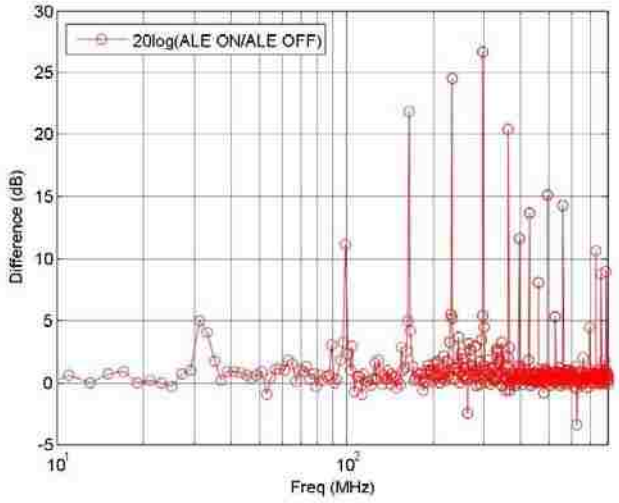


Figure 4.28. Difference in TEM cell emissions with and without ALE switching (orientation 2, Max-Dallas)

4.6. EFFECT OF CLOCK EDGE RATE

While the TEM cell test is intended to only measure emissions related to an IC and not the clock fed to the IC, there is a chance that the clock may couple directly to the TEM cell, independent of the IC. To test this possibility the effect of the input clock edge

rate on the measured emissions was studied for the three ICs tested. This test was performed using the setup for case 1, which has the ground plane extended under the IC, uses both local and bulk decoupling capacitors, uses very short traces on the IC side, runs program 2, and uses an RC low-pass filter (R = 100 Ohm, C = 100 nF) in the path of the clock trace on board 1. The RC low-pass filter in the path of the clock was removed for this test. In one case the clock signal was directly connected to the IC from the clock generator and measurements were performed with this relatively fast rise-time signal (the rise time of the signal directly coming out of the clock generator was approximately 1 ns). In the other case a low-pass filter (R=100 Ohm, C= 100 pF) was placed in the path of the clock trace to increase the rise time of the signal to approximately 22 ns before it was passed to the IC. Increasing the clock edge rate caused an increase in the measured emissions at high frequencies for all orientations of the three ICs. The overall increase in the emissions was approximately 5-20 dB as shown in Figure 4.29 through Figure 4.40. A careful review of all four orientations shows that both capacitive and inductive coupling increased for the three ICs when a clock with fast edge rate was used.

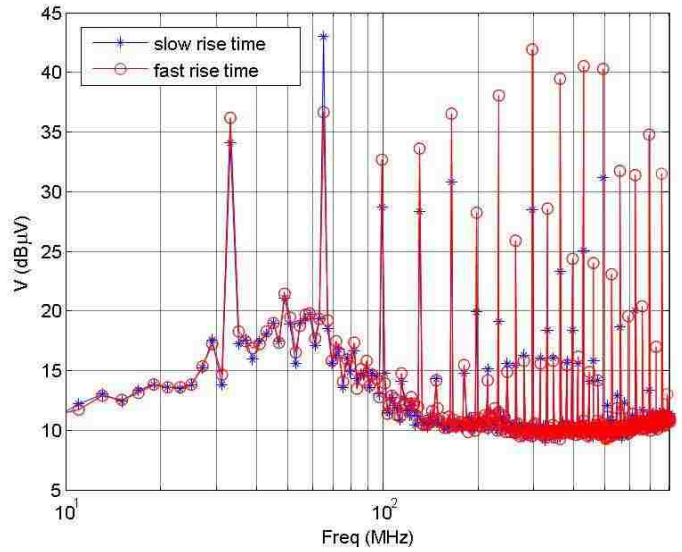


Figure 4.29. TEM cell emissions when using a fast- and slow- rise-time clock (orientation 1, Atmel)

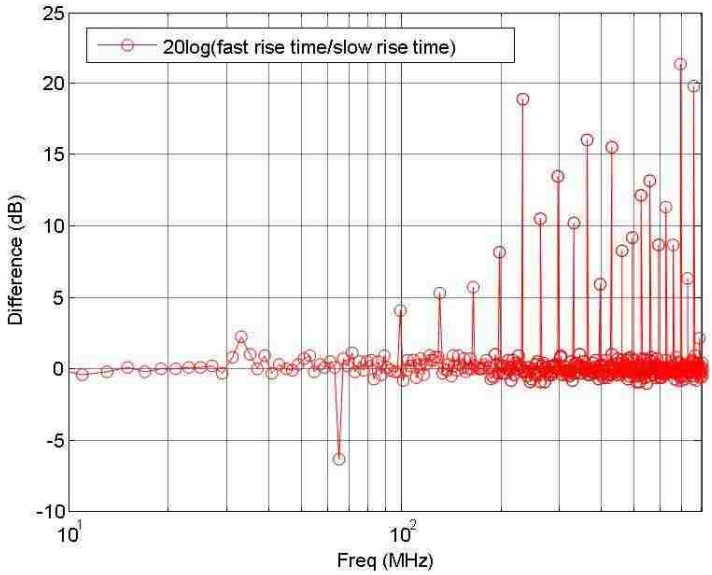


Figure 4.30. Difference in TEM cell emissions when using a fast- and slow- rise-time clock (orientation 1, Atmel)

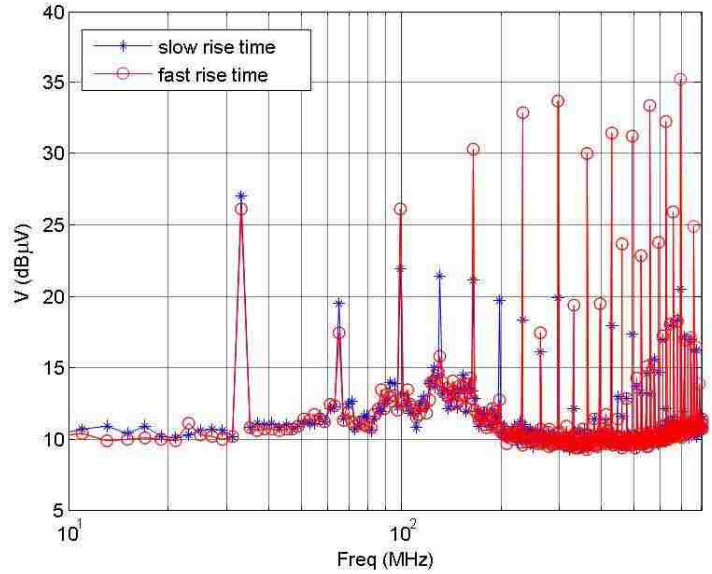


Figure 4.31. TEM cell emissions when using a fast- and slow- rise-time clock (orientation 2, Atmel)

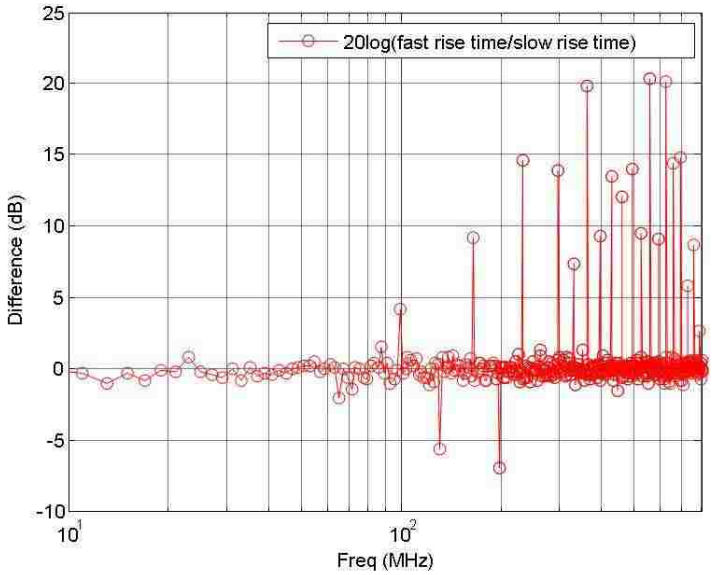


Figure 4.32. Difference in TEM cell emissions when using a fast- and slow- rise-time clock (orientation 2, Atmel)

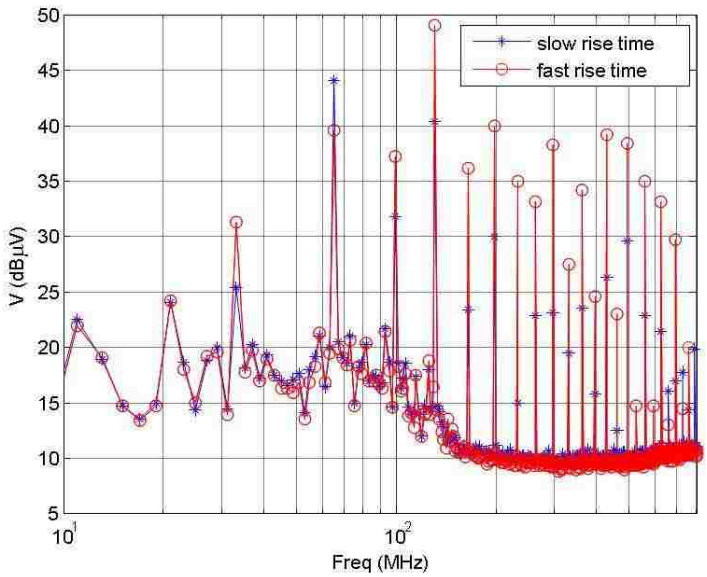


Figure 4.33. TEM cell emissions when using a fast- and slow- rise-time clock (orientation 1, Philips)

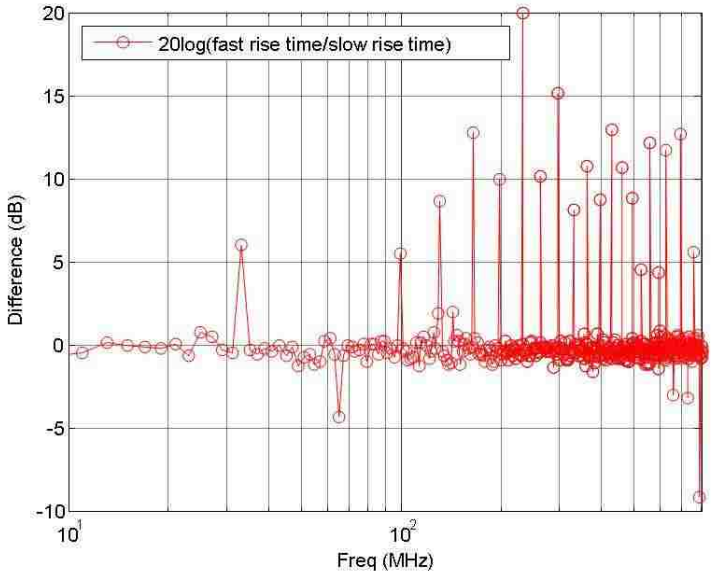


Figure 4.34. Difference in TEM cell emissions when using a fast- and slow- rise-time clock (orientation 1, Philips)

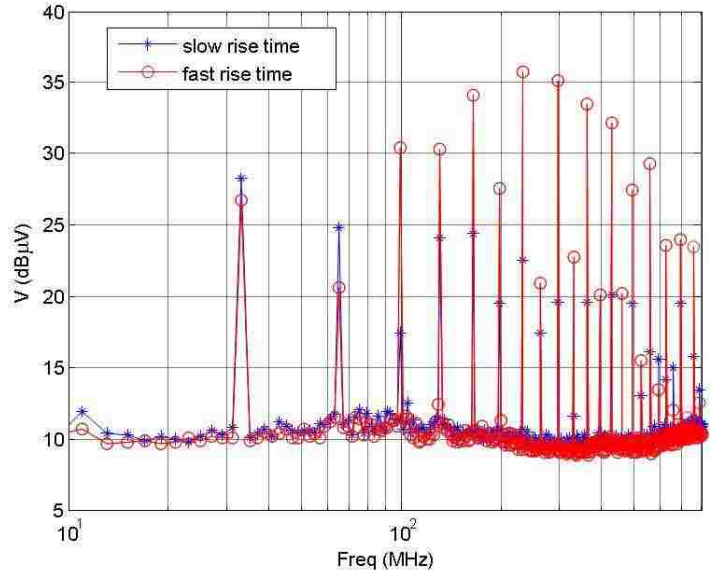


Figure 4.35. TEM cell emissions when using a fast- and slow- rise-time clock (orientation 2, Philips)

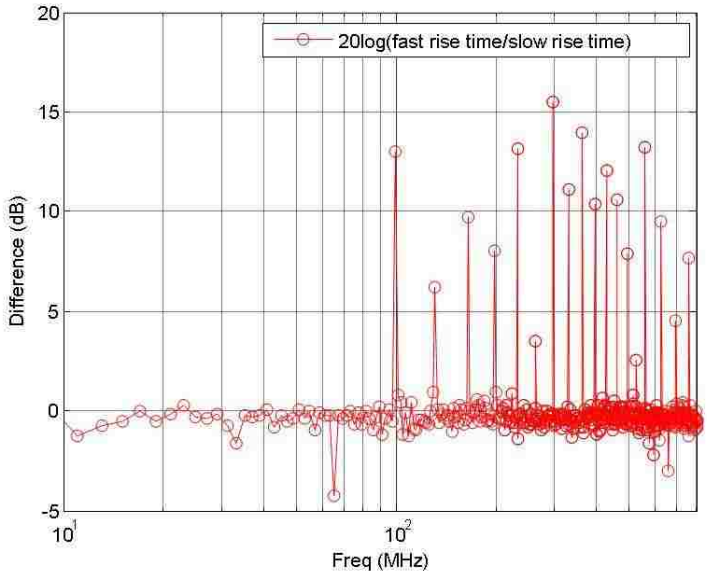


Figure 4.36. Difference in TEM cell emissions when using a fast- and slow- rise-time clock (orientation 2, Philips)

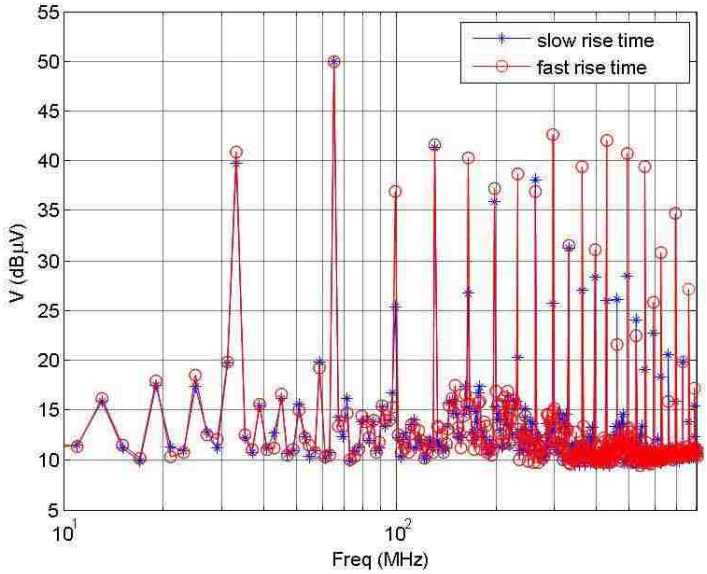


Figure 4.37. TEM cell emissions when using a fast- and slow- rise-time clock (orientation 1, Max-Dallas)

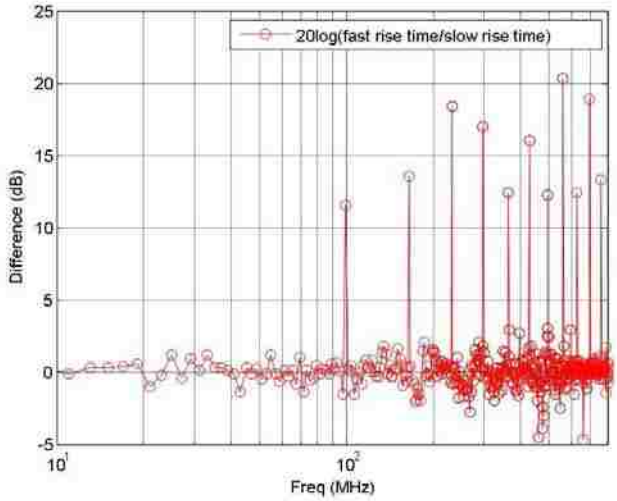


Figure 4.38. Difference in TEM cell emissions when using a fast- and slow- rise-time clock (orientation 1, Max-Dallas)

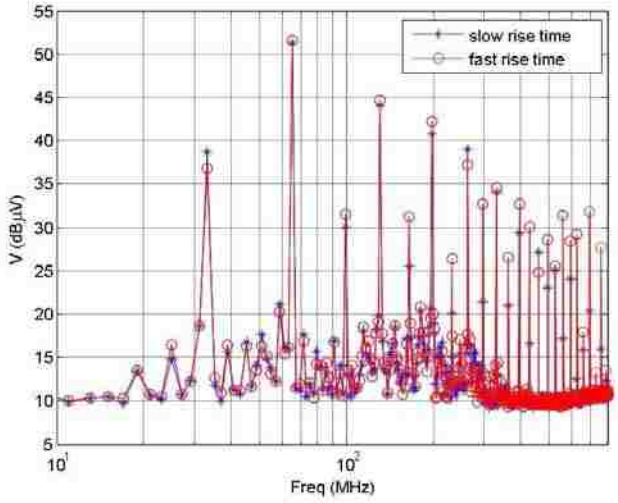


Figure 4.39. TEM cell emissions when using a fast- and slow- rise-time clock (orientation 2, Max-Dallas)

4.7. EFFECT OF SOFTWARE

As the current drawn by the IC may depend on the instruction or operation performed, the software run by the IC may also influence TEM cell emissions. The effect

of software was tested using the setup for case 1, which had the ground plane extended under the IC, used local and bulk decoupling capacitors, used short traces on the IC side,

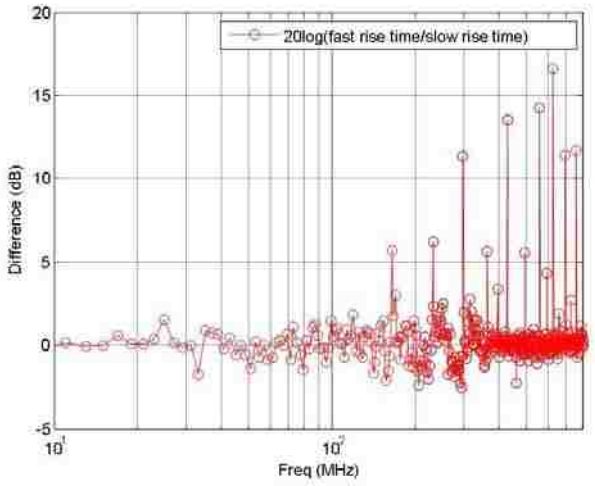


Figure 4.40. Difference in TEM cell emissions when using a fast- and slow- rise-time clock (orientation 2, Max-Dallas)

and used an RC low-pass filter (R = 100 Ohm, C = 100 nF) in the path of the clock trace on board 1. Two different programs called program 1 and program 2 were written to perform this test. Program 1 repeatedly blinks four LEDs on the test board in a binary number pattern. This program does not access different internal memory areas nor exercise many instructions, so there is no significant activity in the core of the microcontroller. Program 2 accesses different internal memory areas, performs arithmetic operations, logical operations, and many other instructions, goes into power-down mode, returns to normal mode through an interrupt, and then blinks the LEDs in a binary pattern. The above list of tasks is done repeatedly. Emissions measurements were performed when each of these programs was executing in the microcontroller. The code for program 1 and 2 is shown in Appendix B.

4.7.1. Atmel. The effect of software on the measured emissions for orientation 1 is shown in Figure 4.41 and Figure 4.42. The emissions are 4-8 dB higher for program 2 than program 1 at low frequencies (25 to 100 MHz). At higher frequencies, the emissions

for program 1 and program 2 are almost the same. Orientation 2 measurements show an increase in the emissions by 1-4 dB in the frequencies up to 200 MHz as shown in Figure 4.43 and Figure 4.44.

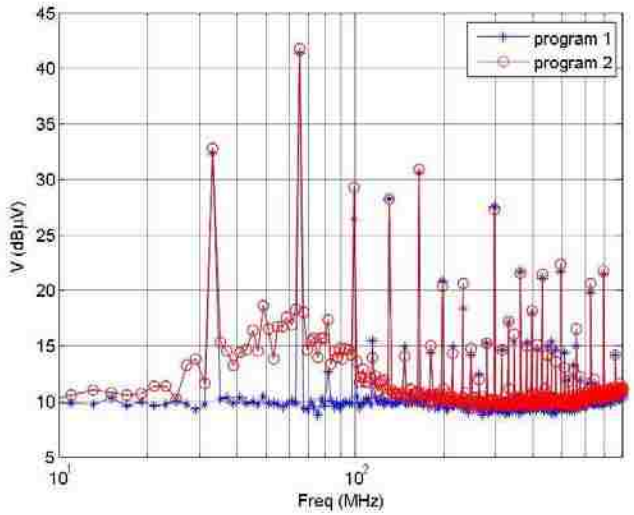


Figure 4.41. TEM cell emissions using program 1 and program 2 (orientation 1, Atmel)

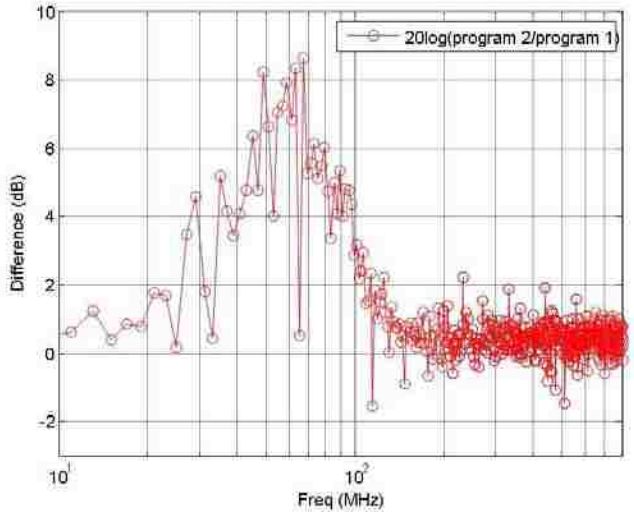


Figure 4.42. Difference in TEM cell emissions using program 1 and program 2 (orientation 1, Atmel)

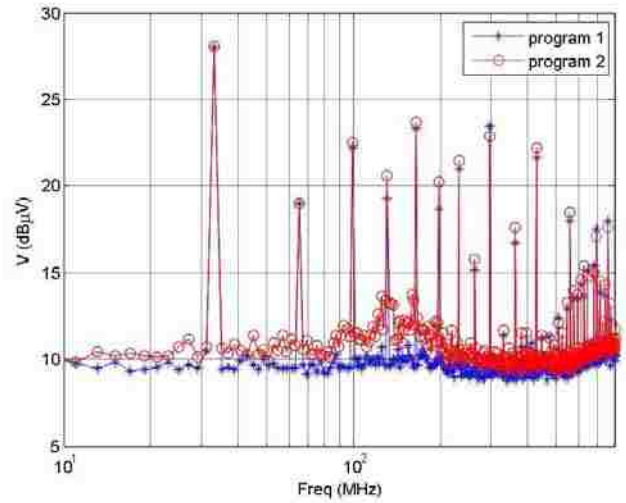


Figure 4.43. TEM cell emissions using program 1 and program 2 (orientation 2, Atmel)

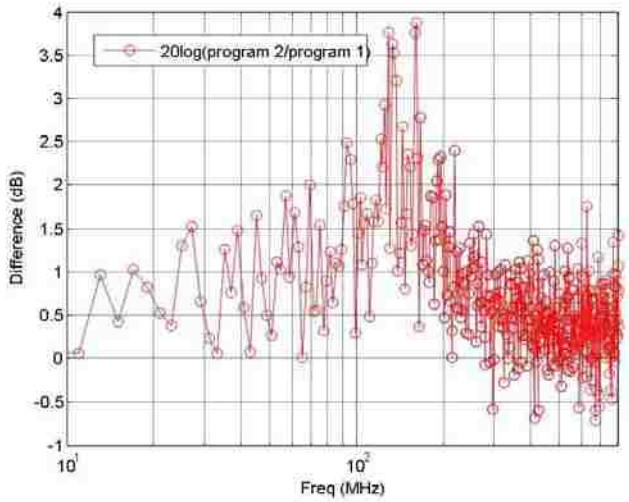


Figure 4.44. Difference in TEM cell emissions using program 1 and program 2 (orientation 2, Atmel)

4.7.2. Philips. As shown in Figure 4.45 through Figure 4.48, running program 2 on the Philips IC caused a 2-7 dB increase in the emissions between 20 and 150 MHz compared to program 1. There was no significant change in the emissions with software at higher frequencies.

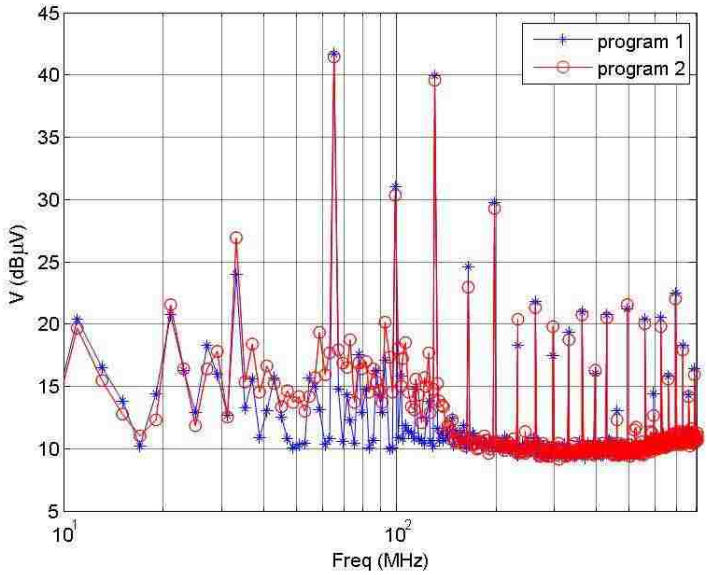


Figure 4.45. TEM cell emissions using program 1 and program 2 (orientation 1, Philips)

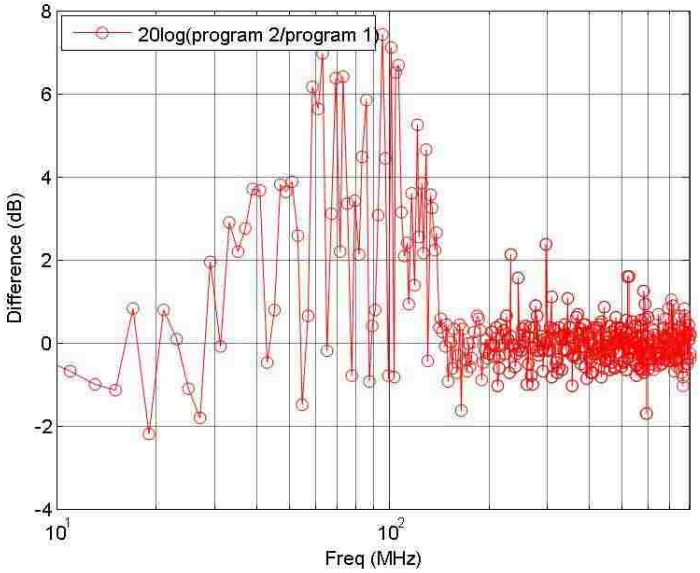


Figure 4.46. Difference in TEM cell emissions using program 1 and program 2 (orientation 1, Philips)

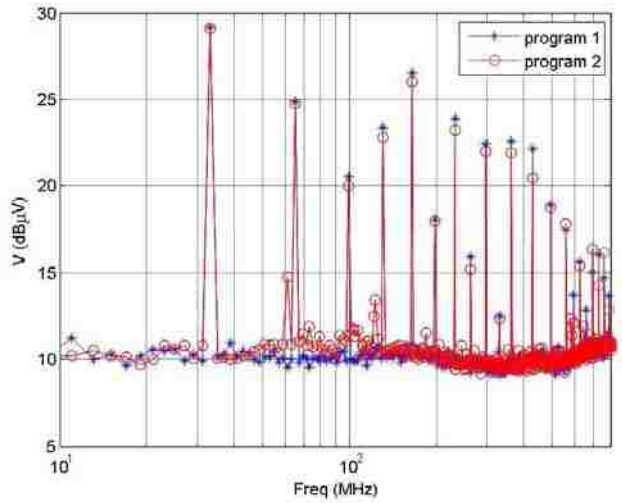


Figure 4.47. TEM cell emissions using program 1 and program 2 (orientation 2, Philips)

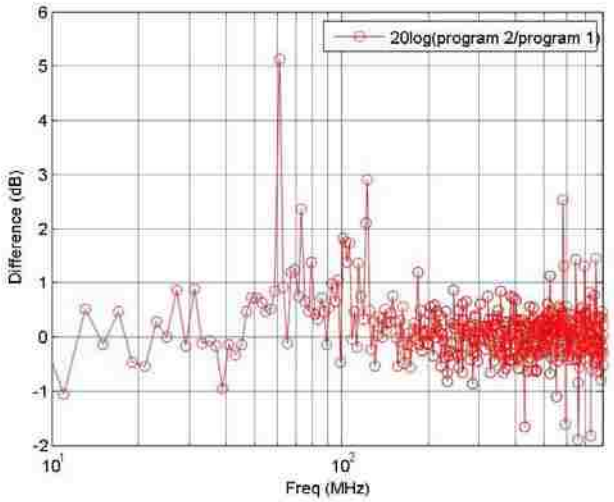


Figure 4.48. Difference in TEM cell emissions using program 1 and program 2 (orientation 2, Philips)

4.7.3. Max-Dallas. Unlike the Atmel and Philips ICs, the Max-Dallas IC showed an overall decrease in emissions when running program 2 compared to program 1. Measured emissions are shown in Figure 4.49 (difference plot shown in Figure 4.50) and Figure 4.51 (difference plot shown in Figure 4.52). There is a decrease in the emissions

by 10-15 dB when running program 2 in both orientations. It may be possible that even though program 2 might increase emissions due to more activity in the core of the IC, the emissions are dominated by the switching of port pins to blink the LEDs. Since program 2 executes more instructions than program 1, the LEDs blink more slowly with this code. Other manufacturers may also see emissions from the switching of the I/O, but that change may be too small to see at the measured frequencies, since instructions are executed at 1/12 the rate or slower. The Max-Dallas switches the LEDs faster than the other two manufacturers, since an instruction is executed in one clock cycle for this IC (12 to 48 times faster than the other ICs). It is also possible that one of the instructions executed by program 1 happens to be a particularly high-energy instruction for the Max-Dallas part, so that program 1, which calls this instruction more often than program 2, has higher emissions.

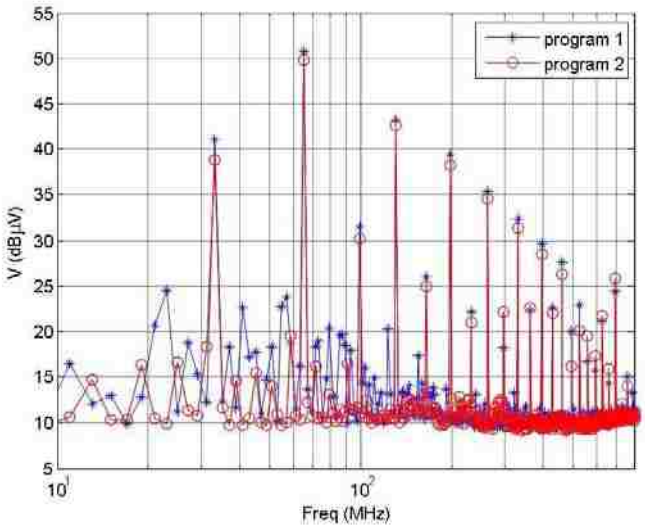


Figure 4.49. TEM cell emissions using program 1 and program 2 (orientation 1, Max-Dallas)

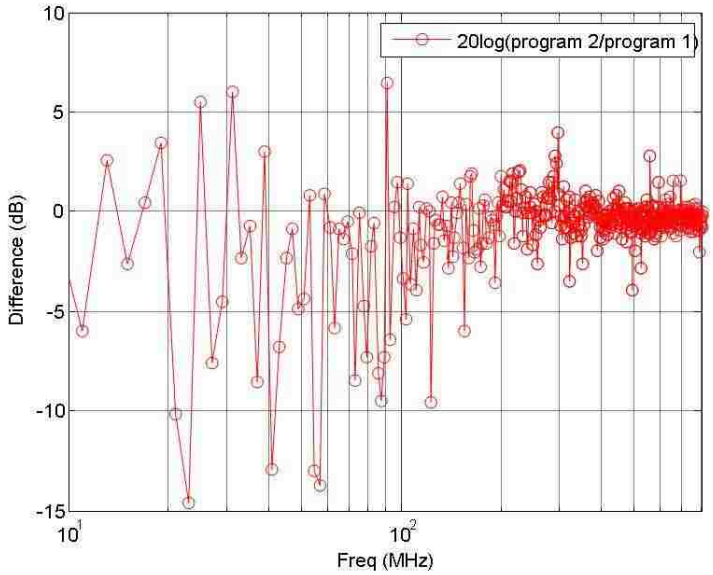


Figure 4.50. Difference in TEM cell emissions using program 1 and program 2 (orientation 1, Max-Dallas)

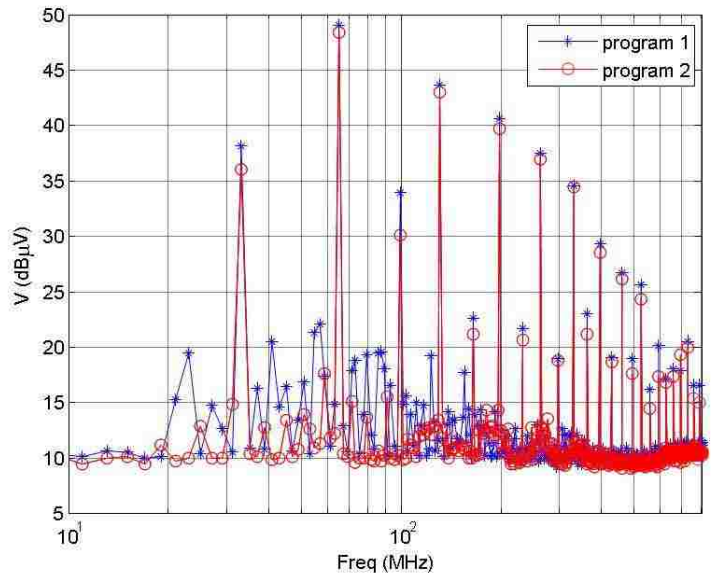


Figure 4.51. TEM cell emissions using program 1 and program 2 (orientation 2, Max-Dallas)

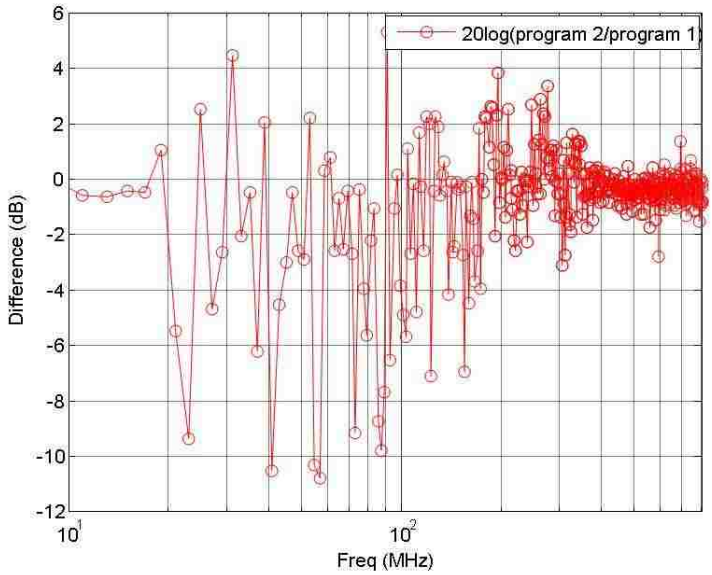


Figure 4.52. Difference in TEM cell emissions using program 1 and program 2 (orientation 2, Max-Dallas)

4.8. COMPARISION OF EMISSIONS AMONG MANUFACTURERS

Based on the data in the previous sections, the emissions from the ICs from the three manufacturers were compared for five different test board setups. The main purpose is to determine which IC performs best (or worst) under which test conditions. The general trend was that the Max-Dallas IC had the highest emissions among the three ICs at the harmonics of the clock frequency for all five test setups. Max-Dallas's higher emissions might be due to the fact that the Max-Dallas IC operates approximately twelve times faster than the other two ICs for the same input clock frequency [11]. That is, the Max-Dallas IC completes an instruction in one clock cycle, while the other two ICs complete an instruction in 12, 24 or 48 clock cycles. As a result, the Max-Dallas IC likely has more gates switching in any particular clock. While emissions were not generally as large at frequencies that were *not* clock harmonics, at those frequencies the general trend was that the Atmel IC caused more emissions at high frequencies (above a few hundred MHz) and the Philips IC caused more emissions at low frequencies (below a few hundred MHz). The Atmel may have caused more emissions at high frequencies because this IC had a faster internal rise-time than the Philips IC [19], [20]. Max-Dallas IC always had

low emissions outside of the clock harmonics, since switching always occurs periodically with the clock and not at a sub-frequency of the clock, as with the other ICs. Results obtained for each test setup are presented in the following sub-sections.

4.8.1. Case 1. The setup for case 1 had a ground plane extended under the IC, used both local and bulk decoupling capacitors, used very short traces on the IC side of the board, used an RC low-pass filter (R = 100 Ohm, C = 100 nF) in the path of the clock trace, and ran program 2 on the IC, and was implemented on board 1. Figure 4.53 through Figure 4.56 show the TEM cell emissions from the ICs of the three manufacturers for this setup. Only results from orientation 1 and orientation 2 are shown as orientations 3 and 4 show similar results. At high frequencies (above 150 MHz) the emissions from the Atmel IC was generally higher than the others by approximately 5 dB at odd harmonics of the clock. At even harmonics of the clock frequency, the Max-Dallas IC had the highest emissions by 10-20 dB. The peak emissions occurred at even harmonics of the clock. The Philips IC, which generally had the lowest emissions at clock frequencies, appears to generate more emissions over a wide band of low-frequencies, up to about 150 MHz, though these emissions were much smaller than at clock harmonics. The Atmel IC also generated emissions at harmonics of ½ the clock frequency. A possible source for the emissions at harmonics of half the clock frequency is the clock divider (divide by 2) between the XTAL1 input and main clock input of the core of the IC [9]. The purpose of this clock divider is to supply clock signal to the CPU when the IC is in X2 mode (X2 mode is generally useful for power saving).

In orientation 2, the emissions from the Max-Dallas IC were generally higher than the emissions from the three ICs throughout the frequency range at harmonics of the clock. Differences of 10-30 dB in the emissions were observed at the even harmonics of the clock frequency. The maximum difference between the emissions from the Atmel and Philips ICs was about 5 dB above 500 MHz. Below 500 MHz the difference in emissions from the Atmel and Philips ICs was small.

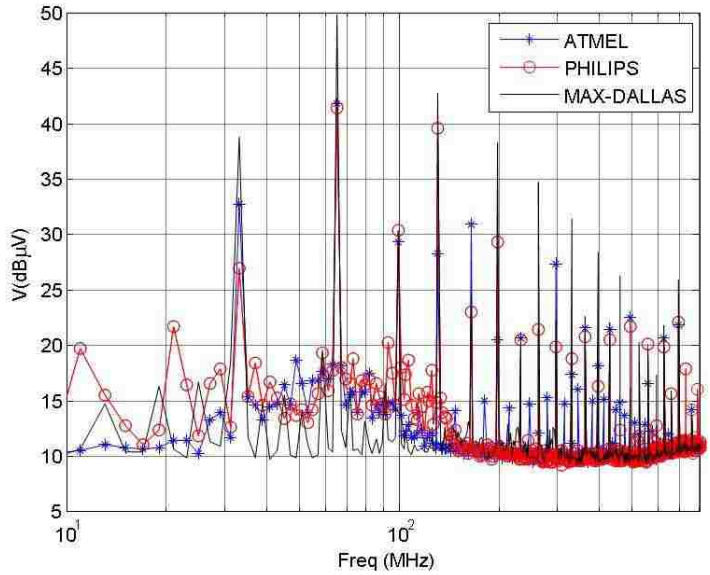


Figure 4.53. TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs using the case 1 setup (orientation 1)

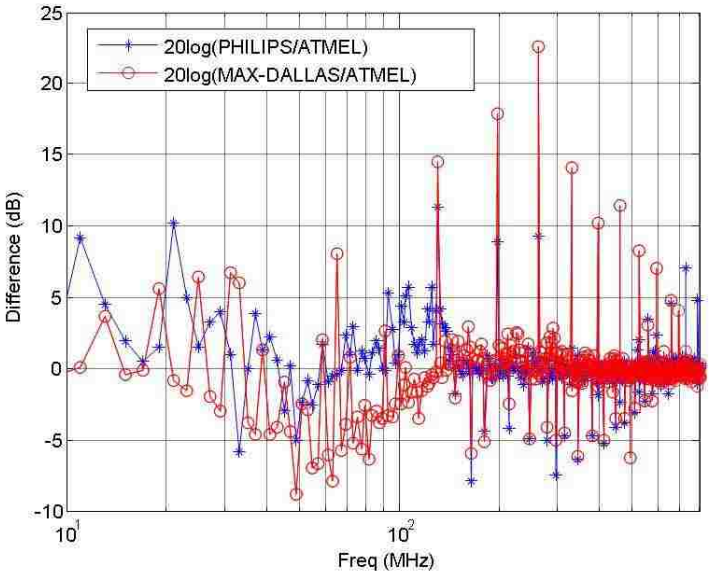


Figure 4.54. Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs using the case 1 setup (orientation 1)

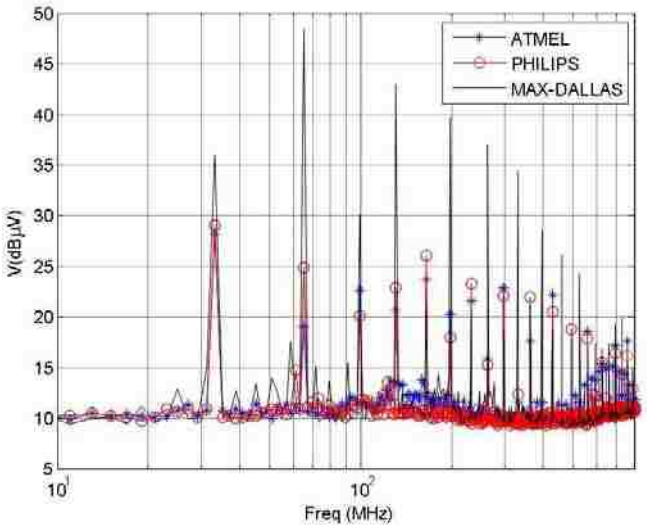


Figure 4.55. TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs using the case 1 setup (orientation 2)

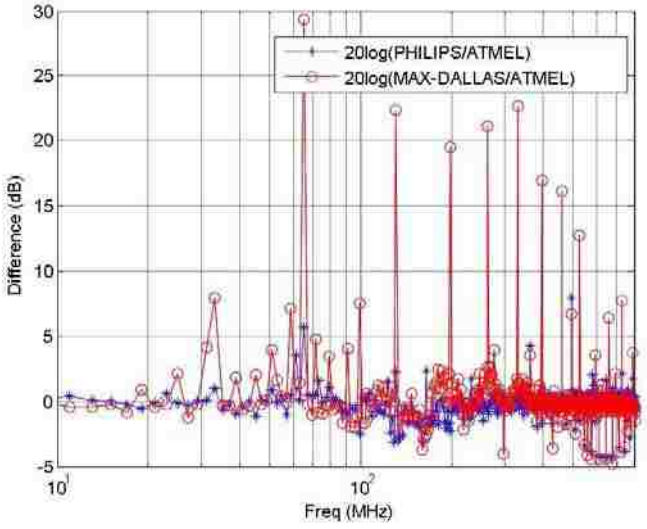


Figure 4.56. Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs using the case 1 setup (orientation 2)

4.8.2. Case 2. The setup for case 2 was implemented on board 2 such that there were no decoupling capacitors (both bulk and local), there was no ground plane under the IC, the IC side of the board used long and wide traces, an RC low-pass filter (R = 100

Ohm, C = 100 nF) was placed in the path of the clock trace, and program 2 was run on the IC. Figure 4.57 through Figure 4.60 show the TEM cell emissions from the ICs from the three manufactures for this setup. Only results from orientation 1 and orientation 2 are shown as results from orientations 3 and 4 are similar to orientation 1 and 2 respectively. Similar to case 1 at high frequencies (above 150 MHz), the Max-Dallas IC generally dominated the emissions among the three ICs by 5-15 dB. Emissions from the Max-Dallas IC dominated at the even harmonics of the clock frequency (similar to case 1) and also at other frequencies. Between the Philips and Atmel ICs, the emission from the Atmel IC was approximately 5 dB higher than the emissions from the Philips IC at high frequencies. In orientation 2 the Max-Dallas IC dominated the emissions by 5-30 dB. Above 500 MHz Atmel dominated emissions by approximately by 5-8 dB.

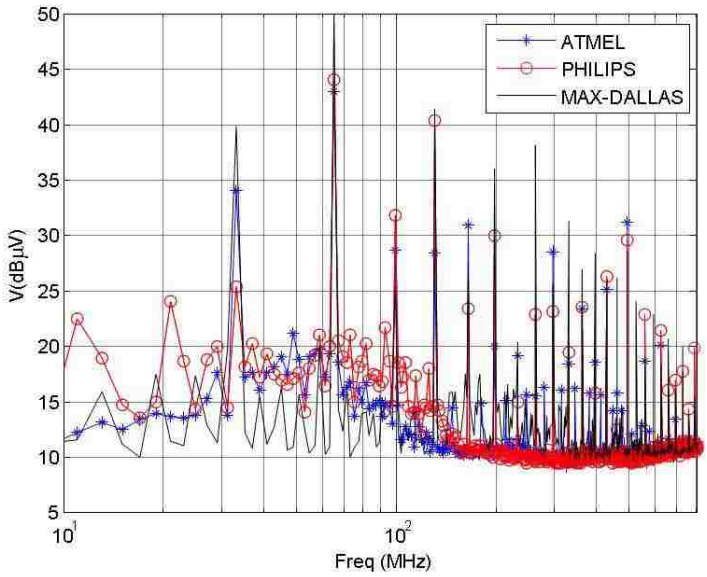


Figure 4.57. TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs using the case 2 setup (orientation 1)

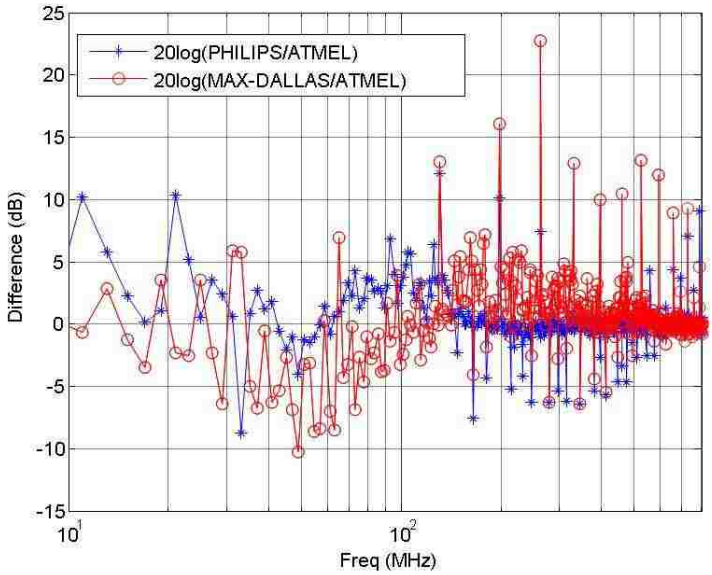


Figure 4.58. Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs using the case 2 setup (orientation 1)

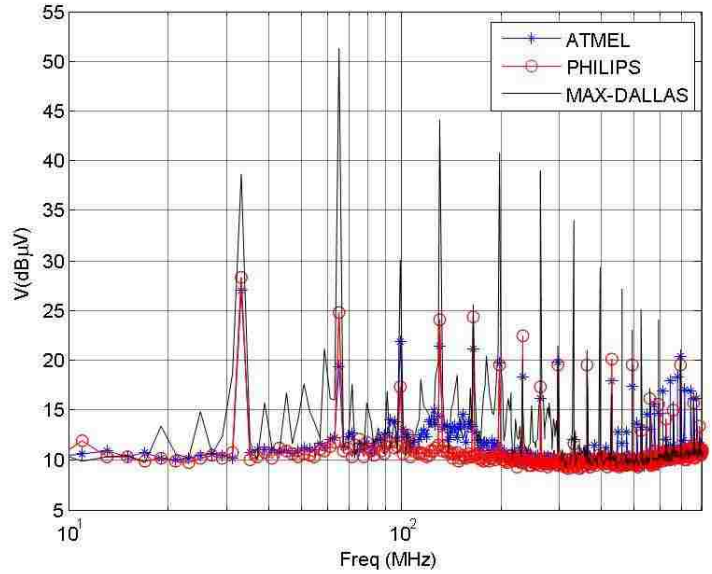


Figure 4.59. TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs using the case 2 setup (orientation 2)

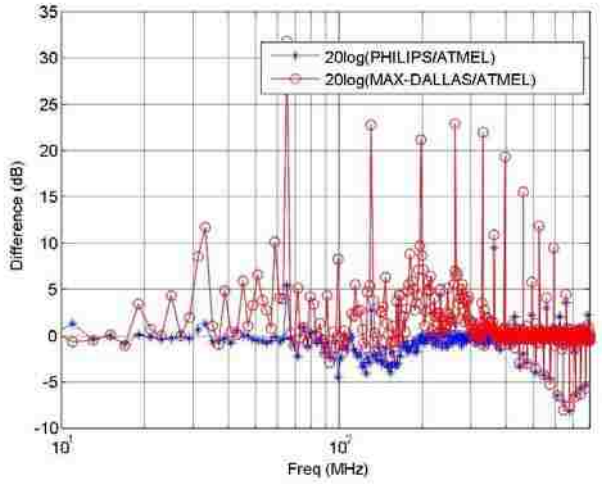


Figure 4.60. Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs using the case2 setup (orientation 2)

4.8.3. Clocking of Unused I/O Pins. Figure 4.61 through Figure 4.64 show the emissions from the three manufacturer's ICs when the ALE was switching. The PCB setup had a ground plane extended under the IC, used both local and bulk decoupling capacitors, used very short traces on the IC side of the board, used an RC low-pass filter (R = 100 Ohm, C = 100 nF) in the path of the clock trace, ran program 2 on the IC, and was implemented on board 1. Results are shown only for orientations 3 and 2 since orientations 1 and 4 are similar to 3 and 2, respectively. Orientation 3 is shown rather than 1 as the variation in the emissions among the manufacturers was more profound in this case. As shown in Figure 4.61 and Figure 4.62 the Philips IC dominated emissions at frequencies below 30 MHz. At high frequencies (above 30 MHz) at harmonics of the clock frequency, the Max-Dallas IC dominated the emissions among the ICs by 10-15 dB. At other frequencies, the Atmel IC dominated emissions by approximately 5 dB. In orientation 2, the Max-Dallas IC dominated the emissions at clock frequency harmonics by 10-15 dB. The Atmel and Philips ICs have approximately the same emissions at low frequencies (below 150 MHz). Above 150 MHz, the Atmel IC had higher emissions than the Philips part by approximately 10-15 dB and had higher emissions than the Max-Dallas IC by 10-20 dB at frequencies other than the clock harmonics. For the Atmel and Philips ICs emissions are seen at harmonics of $1/6^{th}$ the clock frequency when ALE is on.

For the Atmel IC the ALE on effected the emissions throughout the frequency range whereas, for the Philips IC the emissions are effected only in the low frequencies. This might be due to faster rise time of the ALE pin of the Atmel IC when compared to the Philips IC. The Max-Dallas IC saw an increase in the emissions at the clock frequencies.

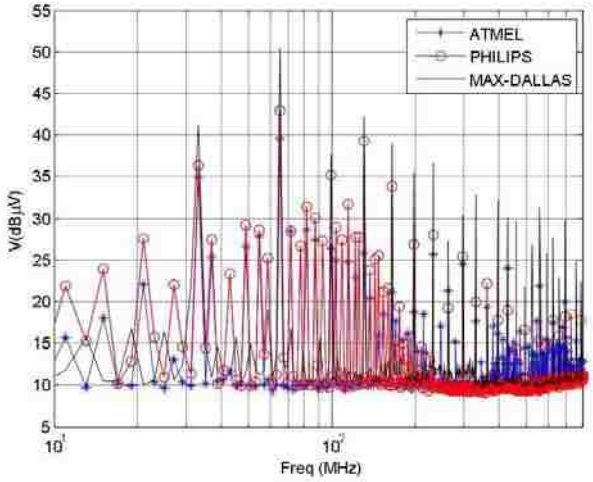


Figure 4.61. TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs with ALE switching (orientation 3)

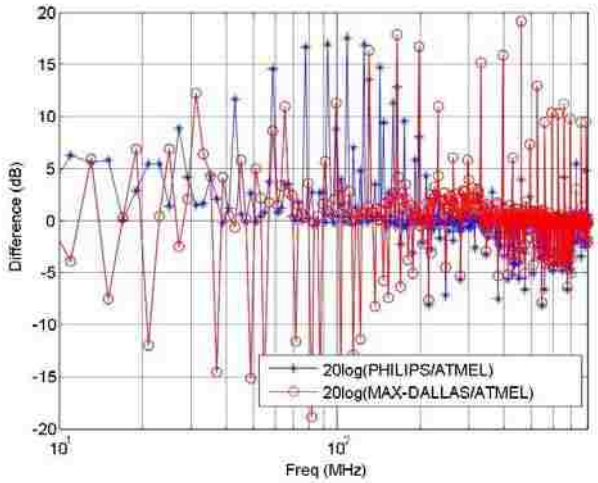


Figure 4.62. Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs with ALE switching (orientation 3)

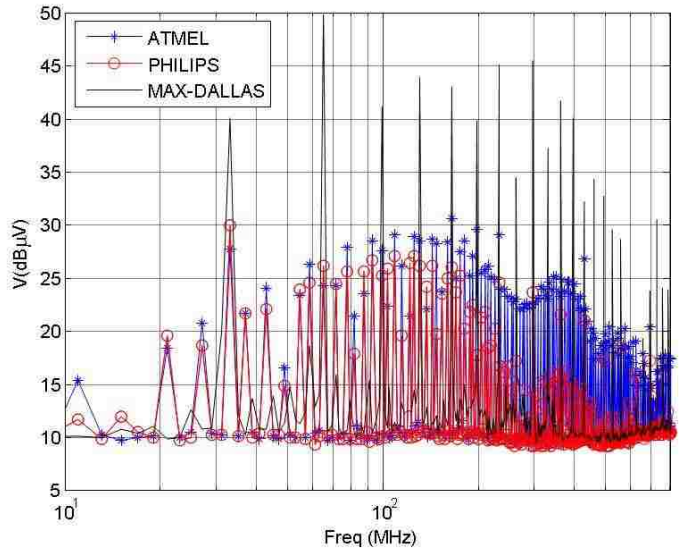


Figure 4.63. TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs with ALE switching (orientation 2)

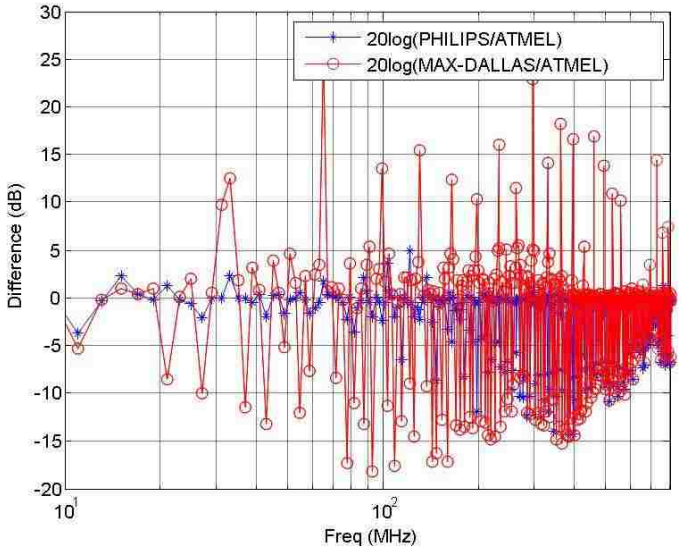


Figure 4.64. Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs with ALE switching (orientation 2)

4.8.4. Fast Clock Edge Rate. Figure 4.65 through Figure 4.68 show the emissions from the ICs from the three manufacturers when using a fast rise-time clock. These experiments were implemented on board 2 using the setup for case 2, except the RC low-pass filter in the path of the clock input trace was not included, giving a fast rising edge on the clock. As in the previous cases, only orientation 1 and 2 are shown as the other two orientations are similar. The results show that for both orientations 1 and 2, the emissions at clock harmonics were increased above about 130 MHz by 10 dB or more over the case with a slow clock edge rate for all the three ICs. As a result, the difference between the emissions from the Max-Dallas and the other two ICs was reduced by about 10 dB. The Max-Dallas IC emissions are still highest, but the difference among the ICs is smaller.

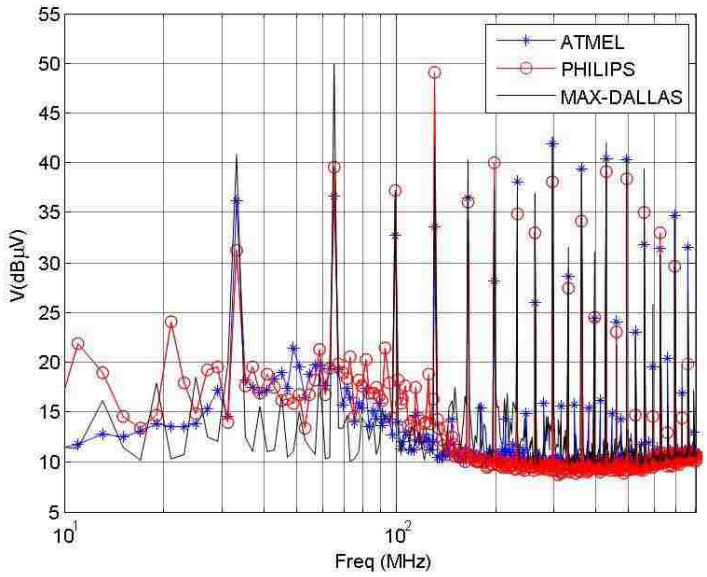


Figure 4.65. TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs for a fast rise-time clock (orientation 1)

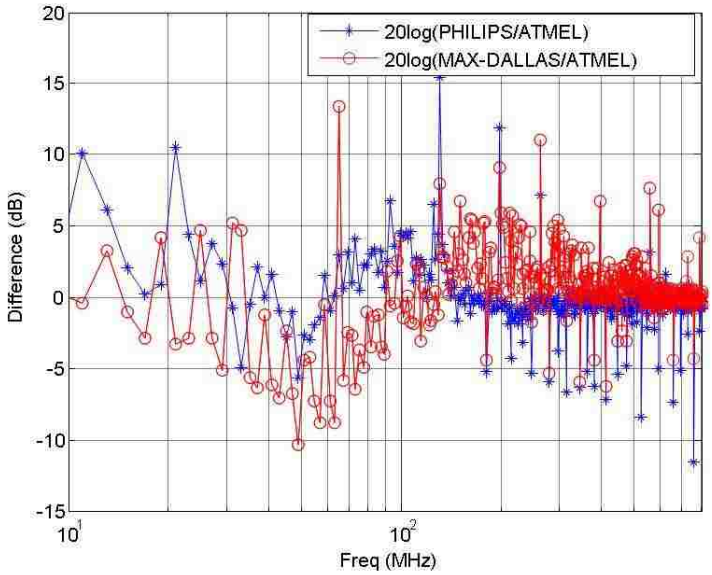


Figure 4.66. Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs for a fast rise-time clock (orientation 1)

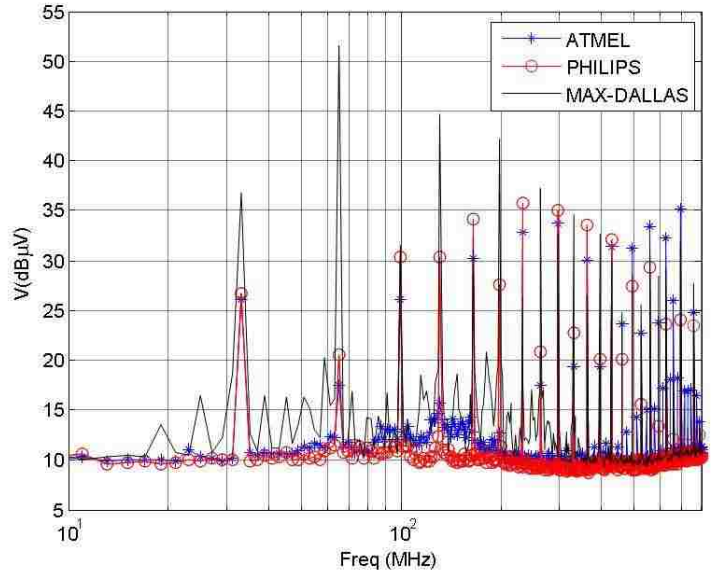


Figure 4.67. TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs for a fast rise-time clock (orientation 2)

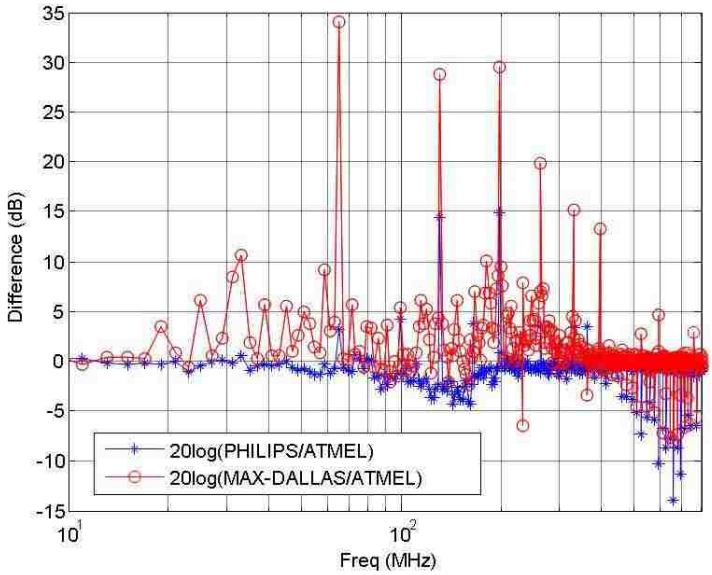


Figure 4.68. Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs for a fast rise-time clock (orientation 2)

4.8.5. Change of Software. Previous emissions were measured while the ICs were running program 2. Another test was implemented using the setup used for case 1, except the program was changed to program 1. Figure 4.69 through Figure 4.72 show the emissions of three manufacturer's ICs when program 1 was used. In orientation 1 the Max-Dallas IC generally dominated emissions below 100 MHz, even at frequencies other than clock harmonics. Above 150 MHz at clock frequency harmonics, the Max-Dallas IC dominated the emissions among the ICs by 10-20 dB. At other frequencies, the Atmel IC dominated the emissions by approximately 5 dB. In orientation 2, the Max-Dallas IC dominated the emissions at clock harmonics by 10-25 dB over the entire frequency range. Below 500 MHz, the Philips and Atmel ICs had approximately the same emissions. Above 500 MHz at frequencies other than the clock harmonics, the Atmel IC dominated the emissions among all ICs by approximately 5 dB.

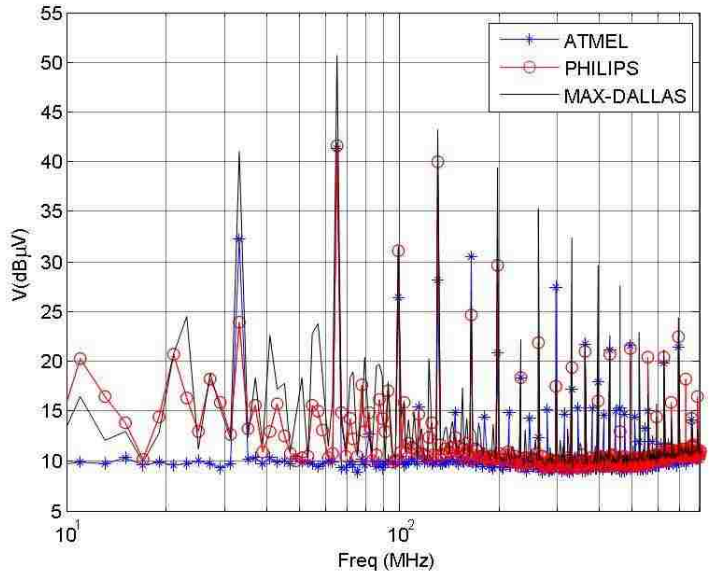


Figure 4.69. TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs while running program 1 (orientation 1)

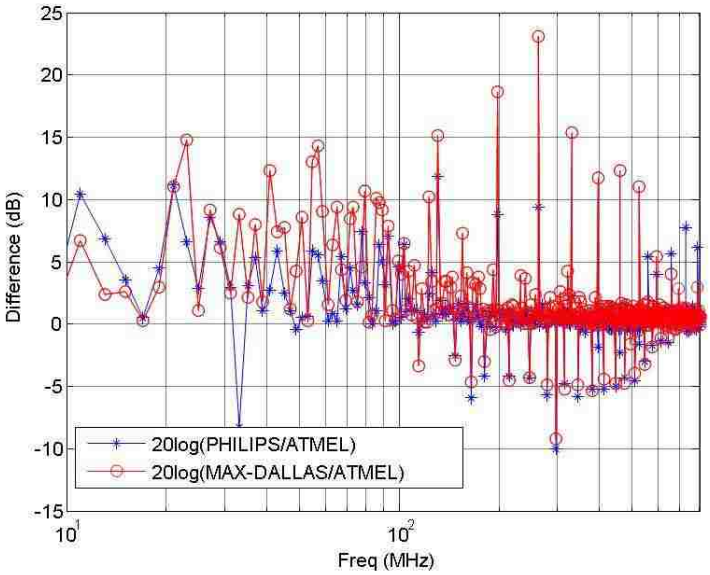


Figure 4.70. Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs while running program 1 (orientation 1)

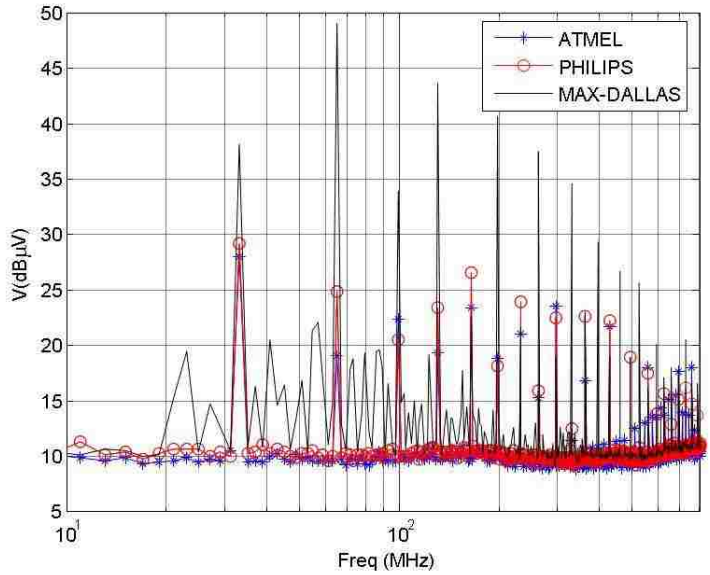


Figure 4.71. TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs while running program 1 (orientation 2)

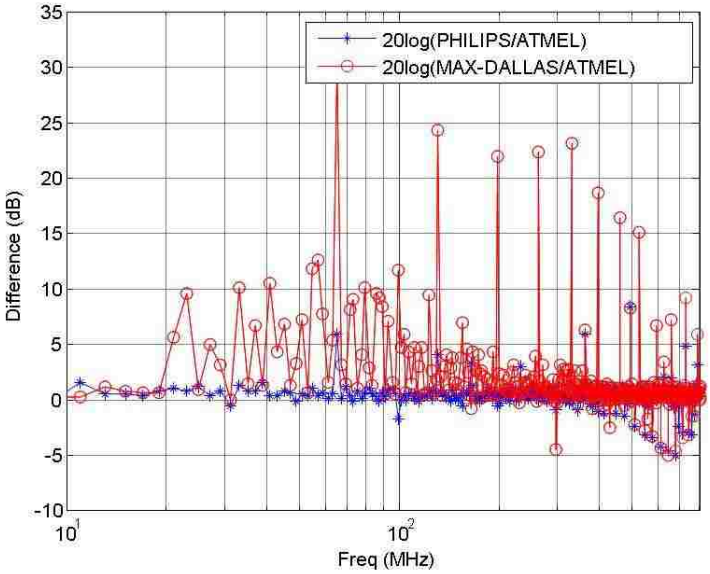


Figure 4.72. Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs while running program 1 (orientation 2)

5. DISCUSSION AND CONCLUSIONS

The effect of PCB design variations on the TEM cell emissions can be explained better by dividing the total frequency range into two sub ranges: low frequencies (below a few hundred MHz) and high frequencies (above a few hundred MHz). The emissions variations at low frequencies are influenced by the decoupling strategy of the test PCB. Emissions variations at high frequencies are most influenced by PCB design parameters such as presence or absence of the ground plane under the IC, the width and length of the traces on the IC side, the distance between the layers, and the stack-up of the test PCB. In the ICs tested, the increase in the emissions observed by changing the test PCB design from with decoupling capacitors (both bulk and local) and closely spaced power and ground planes to a test PCB without any decoupling capacitors (local or bulk) and widely spaced power and ground planes was approximately 3-4 dB. Considering the +/-1 dB accuracy of the measurement, there was a measurable but not significant increase in the emissions between these two cases. A more advanced IC with more transistors and higher working frequencies, however, may see a larger change in emissions with decoupling capacitors and power plane spacing, since they require significantly more current, increasing the noise voltage on the power delivery network. Decoupling strategy plays an important role for the ICs consisting of synchronous circuitry than the ICs with asynchronous circuitry as the synchronous ICs draw huge amount of current at the transition because of large number of transistors switching at the same time creating more noise voltage in the power delivery network.

At high frequencies, it was observed that there was a change of approximately 5-8 dB in the emissions when the PCB design was changed from a design with a ground plane under the IC, which used very short traces on the IC side, and had closely spaced power and ground planes to a design which had no ground plane under the IC, which used long wide traces to connect the ground pin to the board ground, and had widely spaced power and ground planes (some orientations saw an increase and some saw a decrease). In the test PCB, the ground pin is the only pin which used a long, wide trace to connect to the PCB ground. ICs with more power and ground pins and/or increased switching current may see a larger or smaller change in emissions with these same

variations. More power and ground pins may allow more potential return paths and possibly create loops with opposing flux, potentially reducing the impact of larger traces or a ground plane beneath the IC [21]. Higher switching currents, however, will likely increase the impact of these variations.

Clocking of unused I/O pins - in this case the ALE pin - caused a significant increase in the emissions from all three ICs tested. The ALE pin caused variations either through the entire frequency range, only at low frequencies, or only at high frequencies, depending on the IC. Not surprisingly, switching of unused I/O pins has a large influence on the TEM cell emissions. In the ICs tested, when the ALE pin was off emissions were lower by about 10 dB than when the ALE pin was on. The switching off of the ALE pin caused frequency spread in the low frequencies because of less frequent switching of the ALE pin. The results support the manufacturer's typical contention that an 8051 IC with the option to turn off the ALE pin is a "low-emissions" IC. In any case, because of the importance of I/O, an IC should be tested in the configuration it will be used in the end application as recommended by the IEC standard. Testing with more I/O switching at a higher speed than in the end application may give artificially high emissions. Similarly, ignoring I/O may ignore potentially significant emissions sources. Different manufacturers should be compared with similar test configurations.

Although emissions were not tested when the IC accessed the external memory it might be reasonable to assume that the impact of accessing the external memory on the emissions will be similar to that of ALE switching. Since accessing the external memory toggles multiple pins at a time at different rates the emissions might be spread over wide range of frequencies.

It was observed in all three IC test measurements that there was an increase in the strength of clock frequency harmonics by up to 10 dB at high frequencies when the rise time of the input clock was decreased from 22 nsec to 1 nsec. For this setup the emissions from the three ICs were all almost equally bad. This indicates that the Atmel and the Philips ICs are most affected by the faster clock edge rate. The clock input can have a significant influence on the emissions. While the influence may not be as large for bigger, faster ICs with more switching current, the effect of the clock input should be accounted

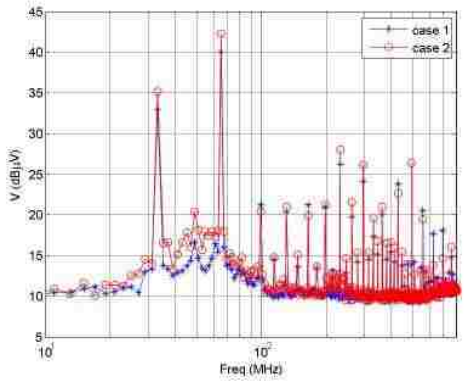
for when comparing emissions among different ICs. In general ICs should probably be tested and used with as slow a clock edge as is required for operation.

Changing the software also caused variation in the measured TEM cell emissions among the ICs tested. The IEC 61967 standard specifically discussed the possible influence of software on the TEM cell emissions. Two different programs were written and tested for emissions in this study. A difference of approximately 4-8 dB in the measured TEM cell emissions was observed between the programs, supporting the IEC's contention that software should be considered when comparing the emissions from different ICs. For the Max-Dallas IC there was a decrease in the emissions by 10-15 dB when running program 2 in both orientations. This may be caused by the switching of port pins to light LEDs. Other manufacturers may also see emissions from the switching of the I/O, but that change may be too small to see at the measured frequencies, since instructions are executed at 1/12 the rate or slower. The Max-Dallas switches the LEDs faster than the other two manufacturers, since an instruction is executed in one clock cycle for this IC (12 to 48 times faster than the other ICs). It is also possible that one of the instructions executed by program 1 happens to be a particularly high-energy instruction for the Max-Dallas part, so that program 1, which calls this instruction more often than program 2, has higher emissions. Emissions variations with software were only seen at low frequencies for the three ICs tested. Other investigators have found, however, that the program used in an IC changes emissions only at high frequencies [22]. The reason for not seeing any variations at high frequencies for the ICs tested may be the high noise floor of the measurement or the 1 GHz upper frequency limit of the measurement (if the variations occur at more higher frequencies). Change in the software may cause vary the measured TEM cell emissions also at low frequencies. This may be caused by repeated execution of the same program.

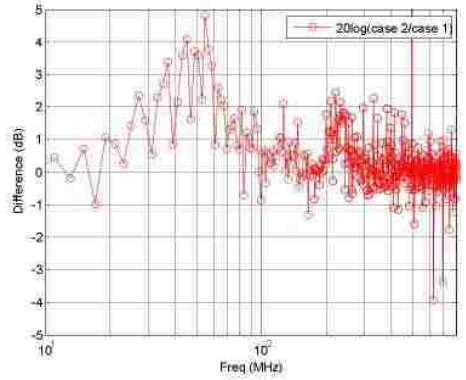
Max-Dallas IC had the highest emissions among the three ICs at the harmonics of the clock frequency for all five test setups because it operates approximately twelve times faster than the other two ICs for the same input clock frequency. At *non* clock harmonics, Atmel IC caused more emissions at high frequencies (above a few hundred MHz). It may be because the Atmel IC has faster internal rise time.

To summarize the above discussion a PCB designer should be careful about using more traces on the IC side of the test PCB as it might cause significant variations in the measured emissions. The ground plane should be extended under the IC when ever it is possible. Decoupling strategy changes from one board to another may not have much influence until there is some decoupling on the board. For fast and dense ICs decoupling strategy may also have significant influence on the measured TEM cell emissions. The test configuration of the PCB may also influence the measured TEM cell emissions. For comparison of emissions among different ICs the PCBs used for testing should be setup with similar configuration. The ICs should be tested in the configuration it will be used in the end application to get a good idea on its emissions.

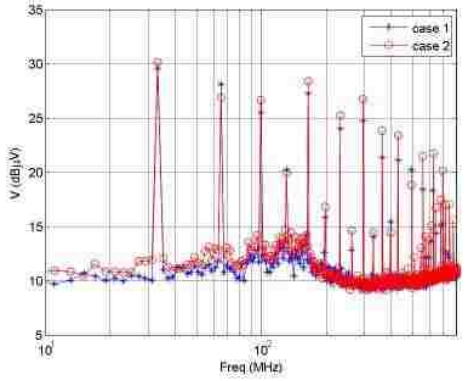
APPENDIX- A
PLOTS FOR REMAINING ORIENTATIONS



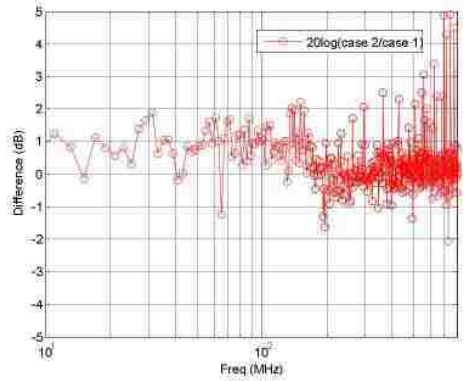
Comparison between TEM cell emissions for case 1 and case 2 (orientation 3, Atmel)



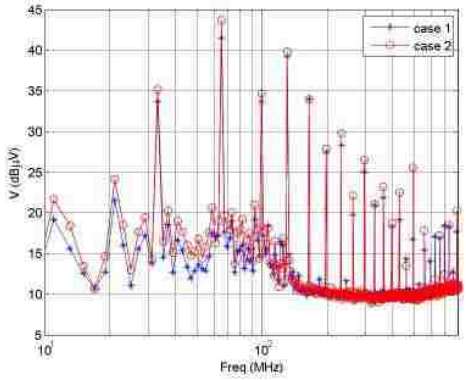
Difference between emissions for case 1 and case 2 (orientation 3, Atmel)



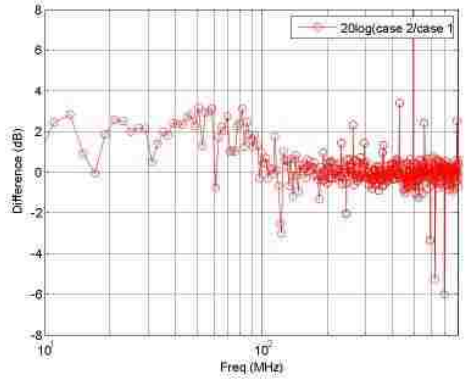
Comparison between TEM cell emissions for case 1 and case 2 (orientation 4, Atmel)



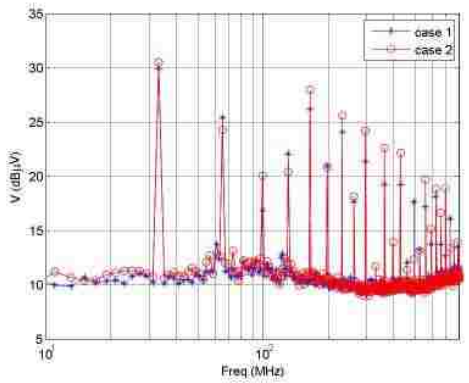
Difference between emissions for case 1 and case 2 (orientation 4, Atmel)



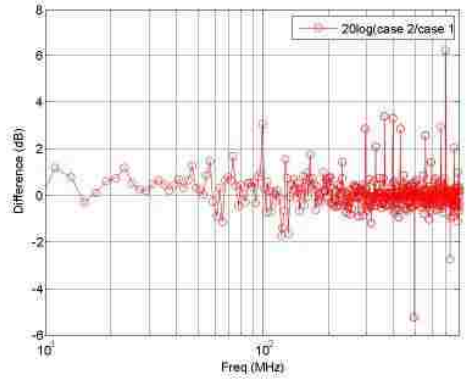
Comparison between TEM cell emissions for case 1 and case 2 (orientation 3, Philips)



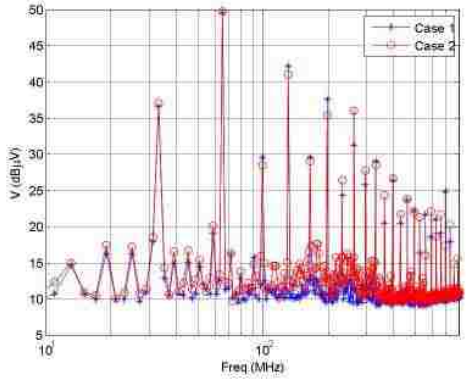
Difference between emissions for case 1 and case 2 (orientation 3, Philips)



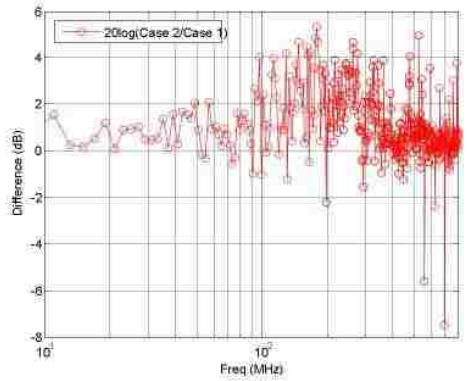
Comparison between TEM cell emissions for case 1 and case 2 (orientation 4, Philips)



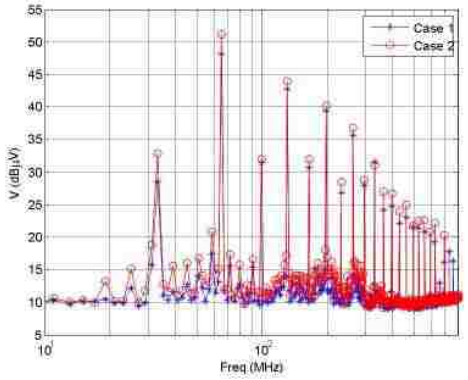
Difference between emissions for case 1 and case 2 (orientation 4, Philips)



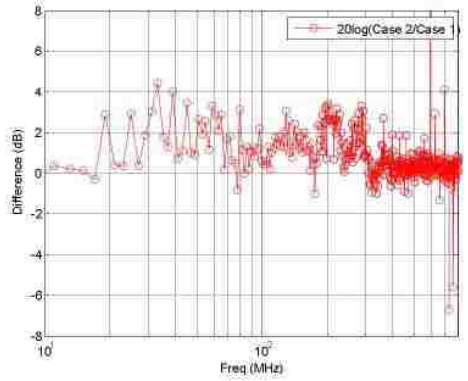
Comparison between TEM cell emissions for case 1 and case 2 (orientation 3, Max-Dallas)



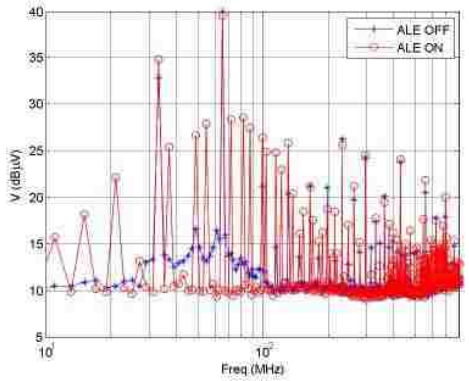
Difference between emissions for case 1 and case 2 (orientation 3, Max-Dallas)



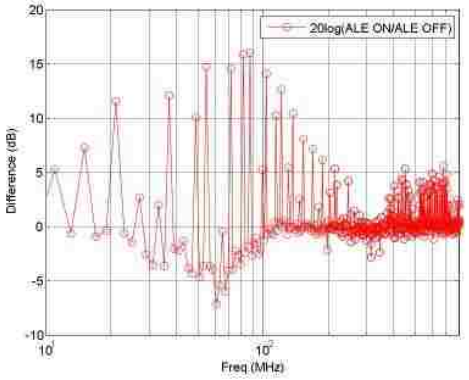
Comparison between TEM cell emissions for case 1 and case 2 (orientation 3, Max-Dallas)



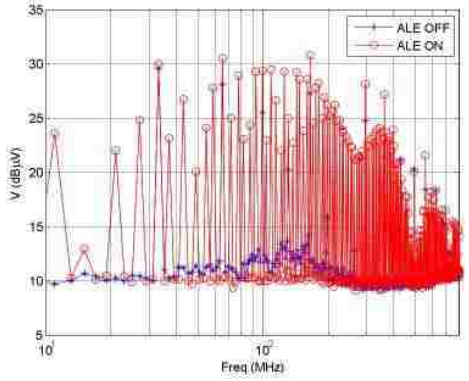
Difference between emissions for case 1 and case 2 (orientation 4, Max-Dallas)



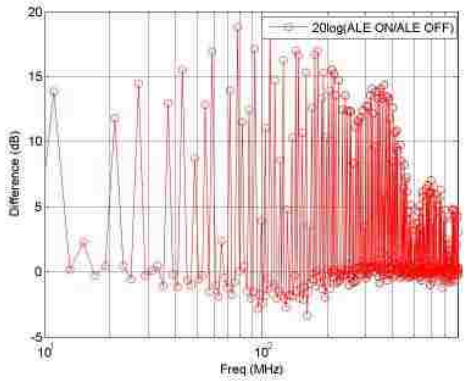
TEM cell emissions with and without ALE switching (orientation 3, Atmel)



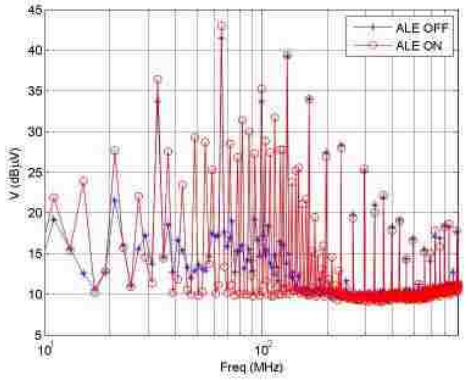
Difference in TEM cell emissions with and without ALE switching (orientation 3, Atmel)



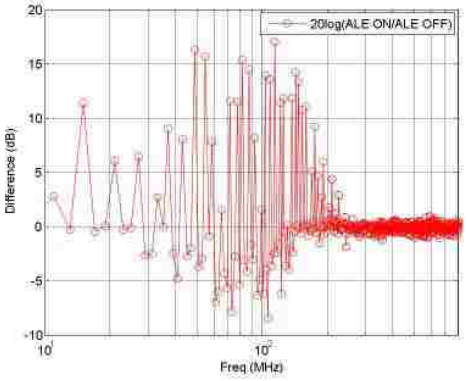
TEM cell emissions with and without ALE switching (orientation 4, Atmel)



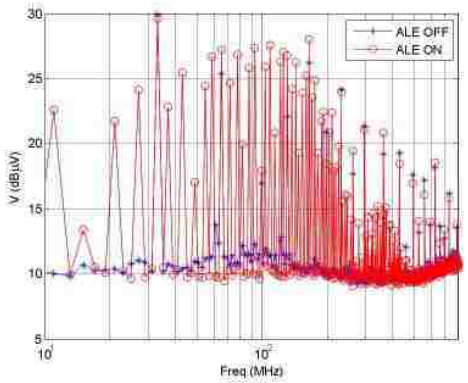
Difference in TEM cell emissions with and without ALE switching (orientation 4, Atmel)



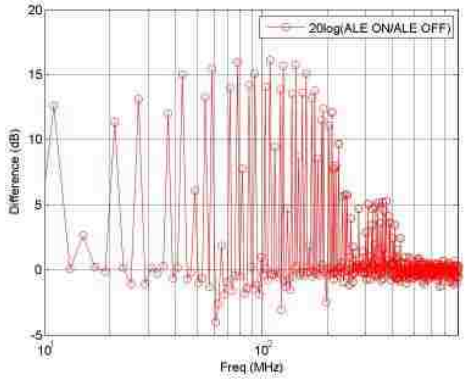
TEM cell emissions with and without ALE switching (orientation 3, Philips)



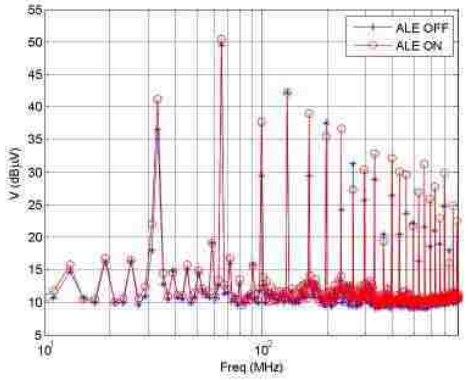
Difference in TEM cell emissions with and without ALE switching (orientation 3, Philips)



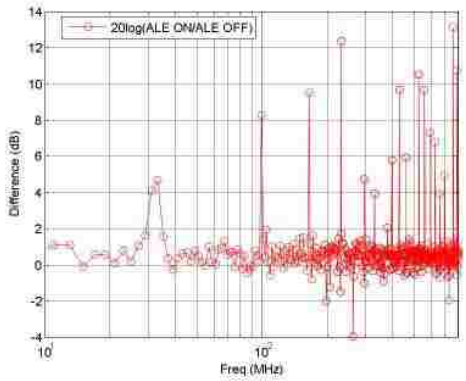
TEM cell emissions with and without ALE switching (orientation 4, Philips)



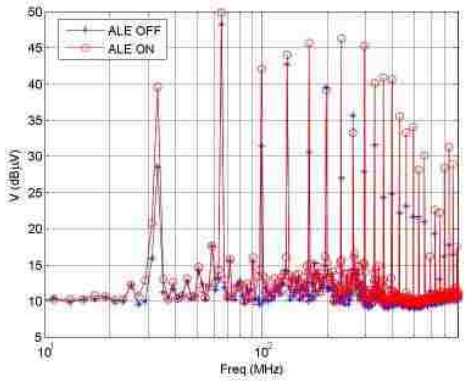
Difference in TEM cell emissions with and without ALE switching (orientation 4, Philips)



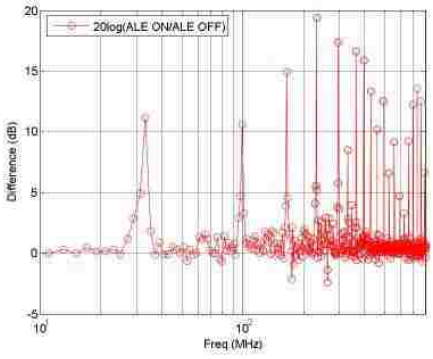
TEM cell emissions with and without ALE switching (orientation 3, Max-Dallas)



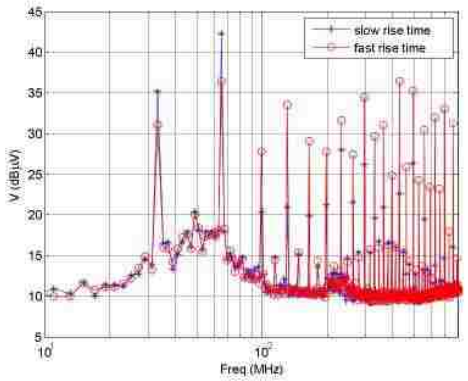
Difference in TEM cell emissions with and without ALE switching (orientation 3, Max-Dallas)



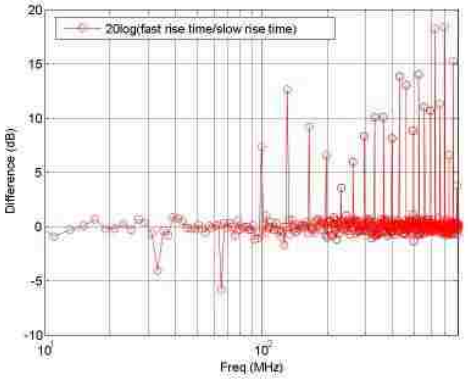
TEM cell emissions with and without ALE switching (orientation 4, Max-Dallas)



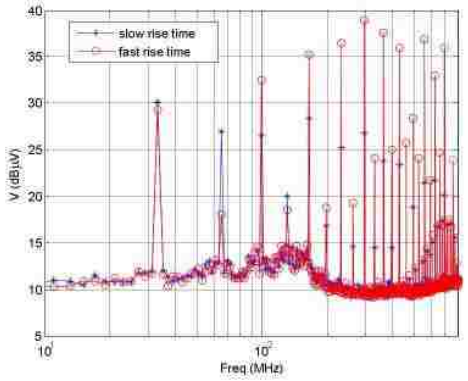
Difference in TEM cell emissions with and without ALE switching (orientation 4, Max-Dallas)



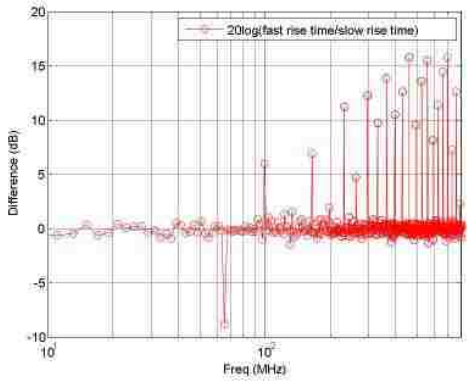
TEM cell emissions when using a fast- and slow- rise-time clock (orientation 3, Atmel)



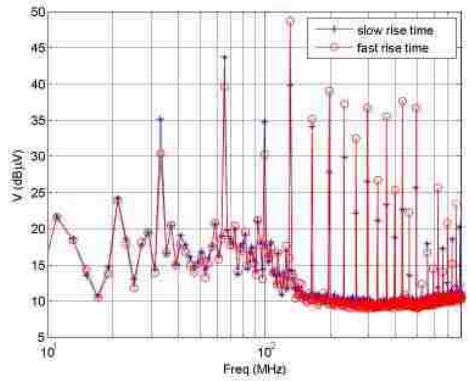
Difference in TEM cell emissions when using a fast- and slow- rise-time clock (orientation 3, Atmel)



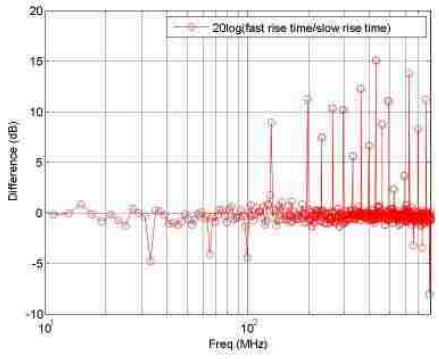
TEM cell emissions when using a fast- and slow- rise-time clock (orientation 4, Atmel)



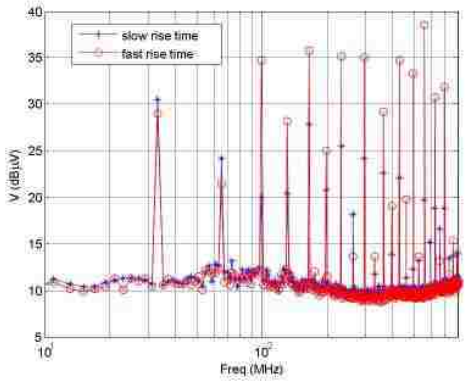
Difference in TEM cell emissions when using a fast- and slow- rise-time clock (orientation 4, Atmel)



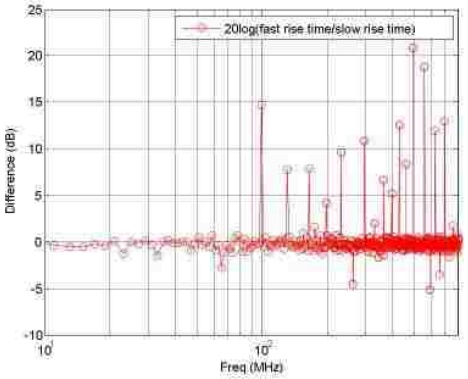
TEM cell emissions when using a fast- and slow- rise-time clock (orientation 3, Philips)



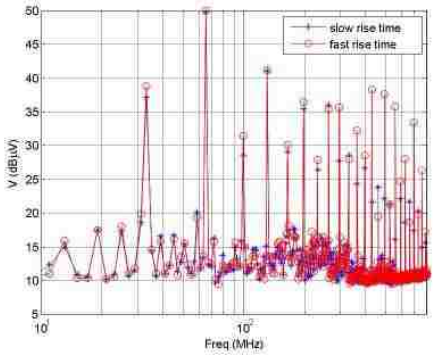
Difference in TEM cell emissions when using a fast- and slow- rise-time clock (orientation 4, Philips)



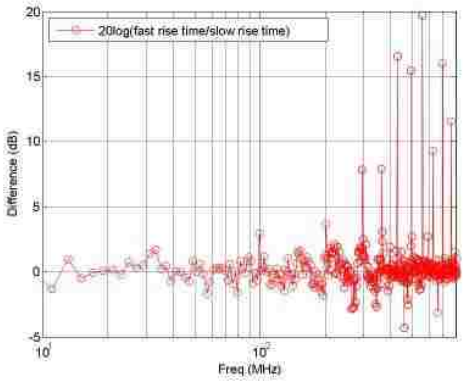
TEM cell emissions when using a fast- and slow- rise-time clock (orientation 4, Philips)



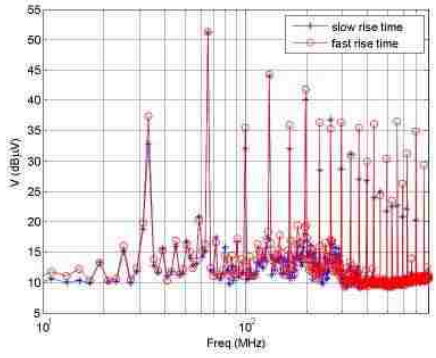
Difference in TEM cell emissions when using a fast- and slow- rise-time clock (orientation 4, Philips)



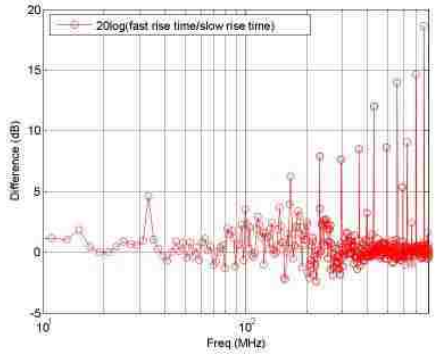
TEM cell emissions when using a fast- and slow- rise-time clock (orientation 3, Max-Dallas)



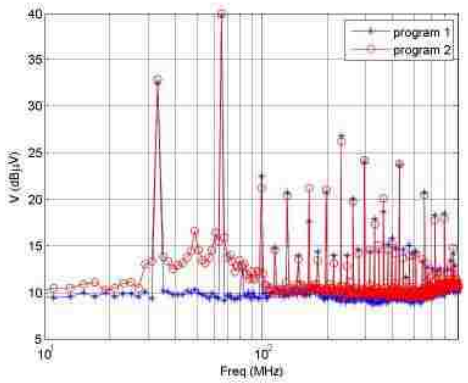
Difference in TEM cell emissions when using a fast- and slow- rise-time clock (orientation 3, Max- Dallas)



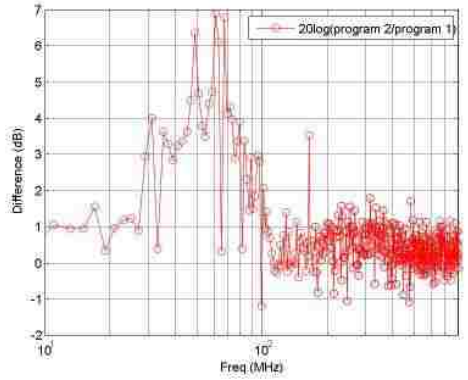
TEM cell emissions when using a fast- and slow- rise-time clock (orientation 4, Max-Dallas)



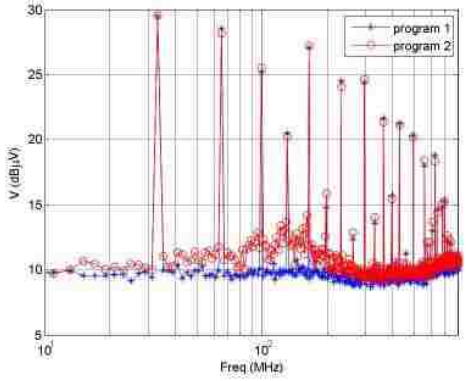
Difference in TEM cell emissions when using a fast- and slow- rise-time clock (orientation 4, Max- Dallas)



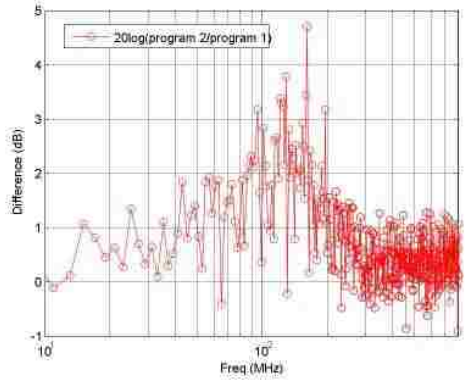
TEM cell emissions using program 1 and program 2 (orientation 3, Atmel)



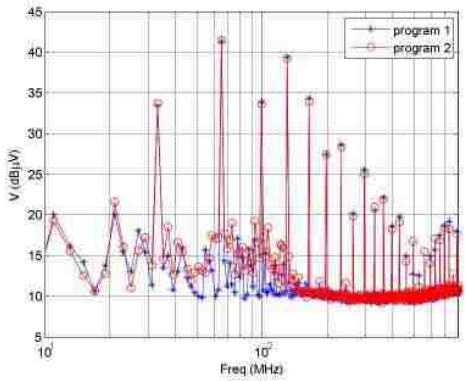
Difference in TEM cell emissions using program 1 and program 2 (orientation 3, Atmel)



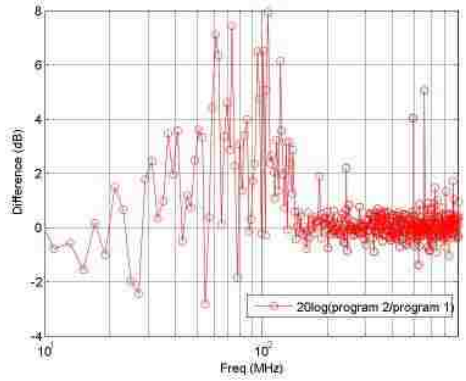
TEM cell emissions using program 1 and program 2 (orientation 4, Atmel)



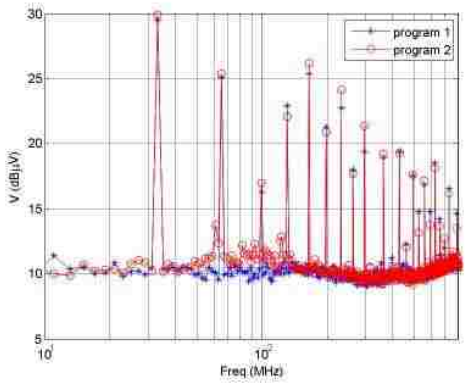
Difference in TEM cell emissions using program 1 and program 2 (orientation 4, Atmel)



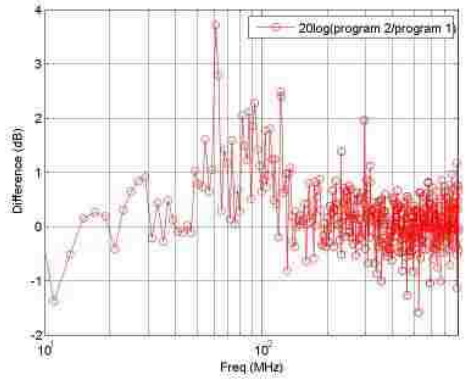
TEM cell emissions using program 1 and program 2 (orientation 3, Philips)



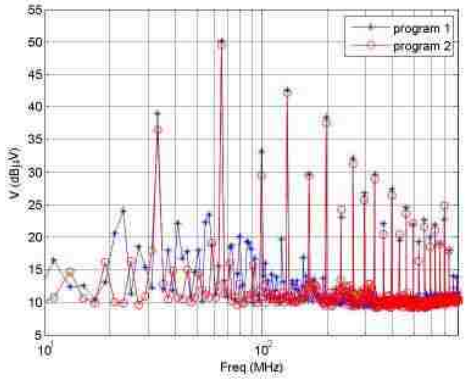
Difference in TEM cell emissions using program 1 and program 2 (orientation 3, Philips)



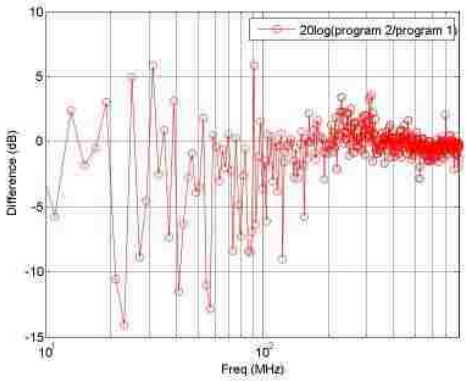
TEM cell emissions using program 1 and program 2 (orientation 4, Philips)



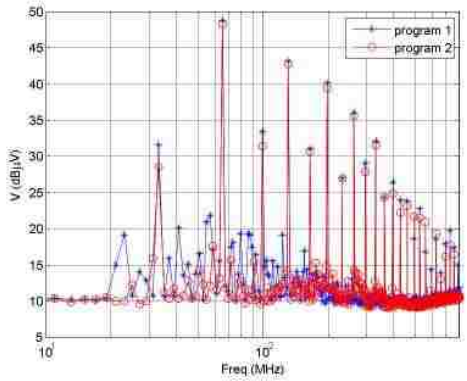
Difference in TEM cell emissions using program 1 and program 2 (orientation 4, Philips)



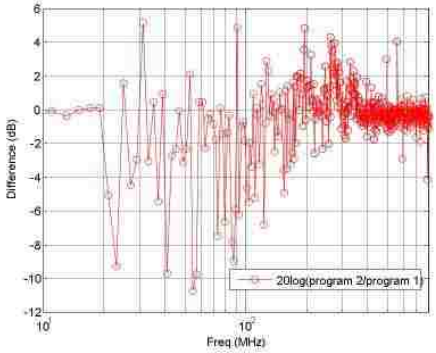
TEM cell emissions using program 1 and program 2 (orientation 3, Max- Dallas)



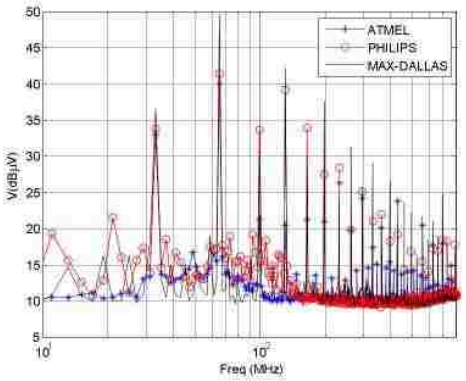
Difference in TEM cell emissions using program 1 and program 2 (orientation 3, Max-Dallas)



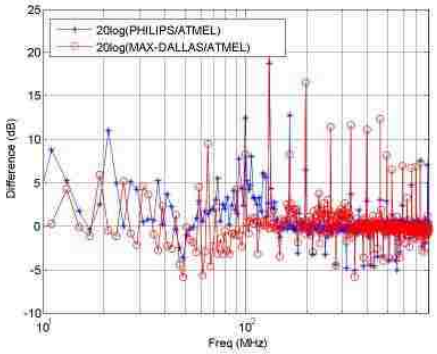
TEM cell emissions using program 1 and program 2 (orientation 4, Max- Dallas)



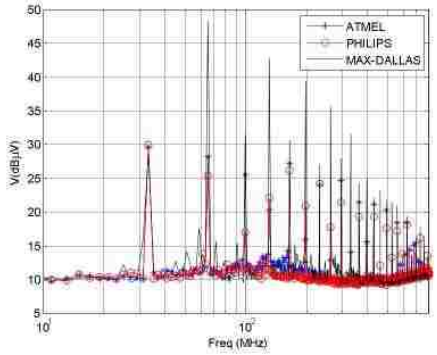
Difference in TEM cell emissions using program 1 and program 2 (orientation 3, Max-Dallas)



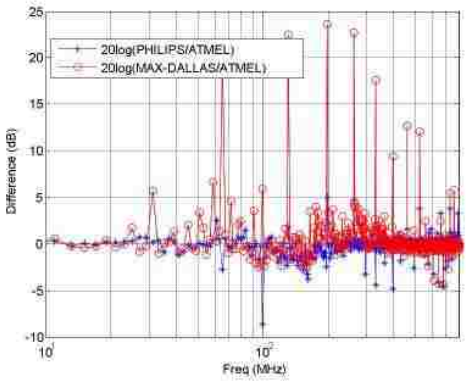
TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs using the case 1 setup (orientation 3)



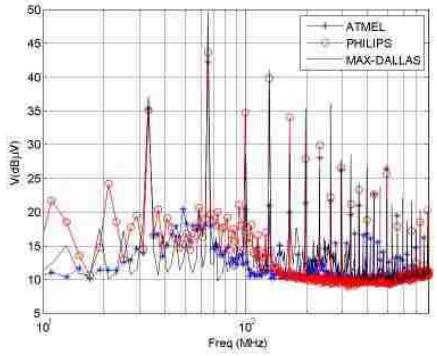
Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs using the case 1 setup (orientation 3)



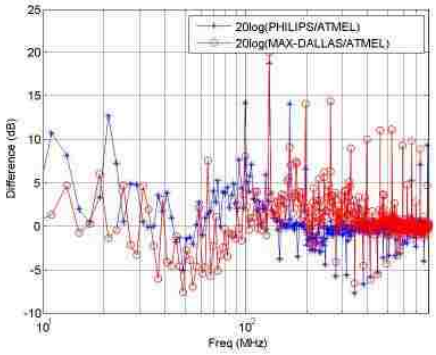
TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs using the case 1 setup (orientation 4)



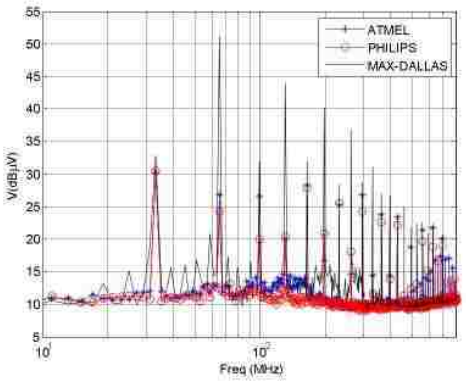
Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs using the case 1 setup (orientation 4)



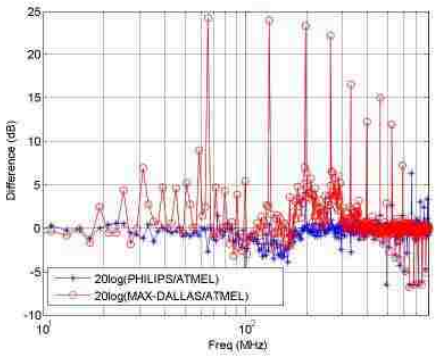
TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs using the case 2 setup (orientation 3)



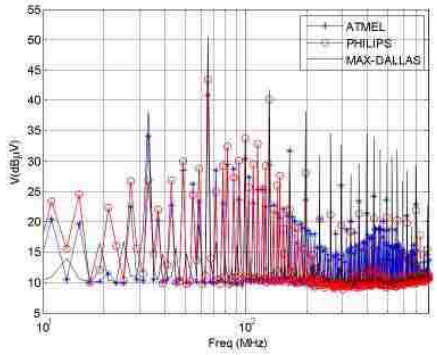
Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs using the case 2 setup (orientation 3)



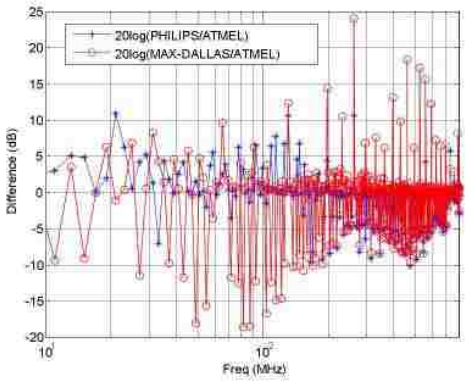
TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs using the case 2 setup (orientation 4)



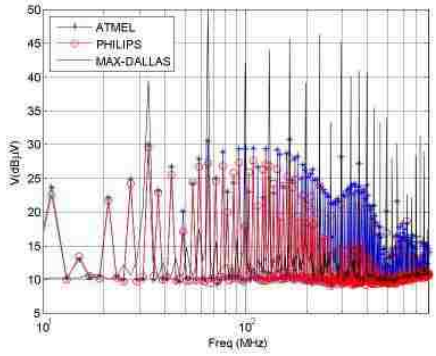
Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs using the case 2 setup (orientation 4)



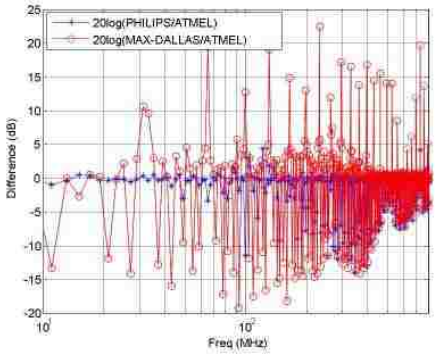
TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs with ALE switching (orientation 1)



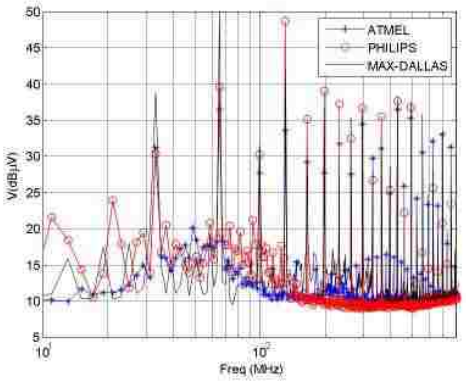
Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs with ALE switching (orientation 1)



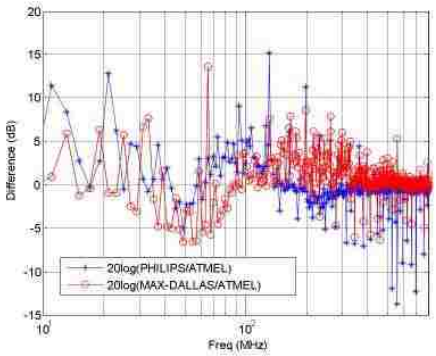
TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs with ALE switching (orientation 4)



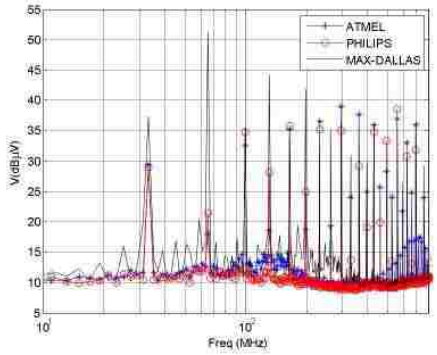
Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs with ALE switching (orientation 4)



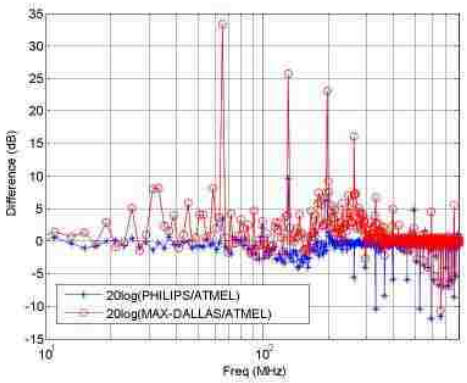
TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs for a fast rise-time clock (orientation 3)



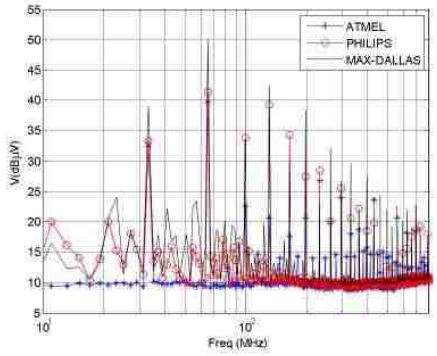
Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs for a fast rise-time clock (orientation 3)



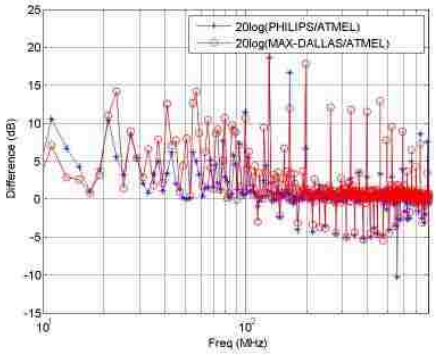
TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs for a fast rise-time clock (orientation 4)



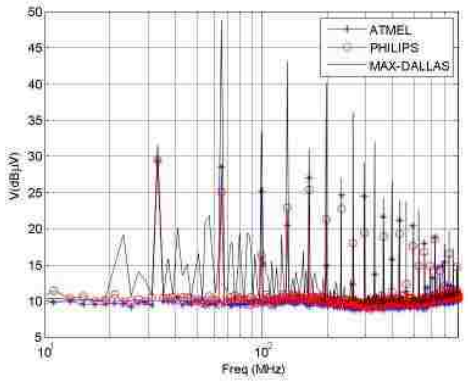
Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs for a fast rise-time clock (orientation 4)



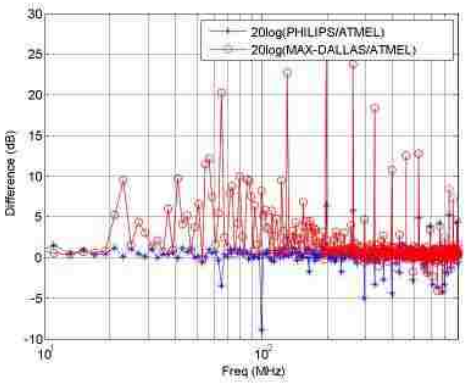
TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs while running program 1 (orientation 3)



Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs while running program 1 (orientation 1)



TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs while running program 1 (orientation 4)



Difference between TEM cell emissions from the Atmel, Philips, and Max-Dallas ICs while running program 1 (orientation 4)

APPENDIX- B
PROGRAM 1 AND PROGRAM 2

Two programs, program 1 and program 2, were written using C- language to test the ICs. Codes for the programs are as follows.

PROGRAM 1

```
#include <INTRINS.H>
#include <REG51F.H>
void one_second_delay()
{int x;
 int y;
  for(x=0;x<15;x++);
   for(y=0;y<15;y++); }
 void main()
{
    while(1)  {
   AUXR= 0x03;
   P1 = 0xFF;
   one_second_delay();
   P1 = 0xEF;
  one_second_delay();
 P1 =0xDF;
   one_second_delay();
              P1 = 0xCF;
              one_second_delay();
   P1 = 0xBF;
   one_second_delay();
   P1 = 0xAF;
  one_second_delay();
   P1 = 0x9F;
   one_second_delay();
   P1 = 0x8F;
   one_second_delay();
  P1 = 0x7F;
   one_second_delay();
   P1 = 0x6F;
   one_second_delay();
   P1 = 0x5F;
   one_second_delay();
   P1 = 0x4F;
   one_second_delay();
   P1 = 0x3F;
   one_second_delay();
   P1 = 0x2F;
   one_second_delay();
   P1 = 0x1F;
   one_second_delay();
   P1 = 0x0F;
```

```
  one_second_delay();
 }
}
```

PROGRAM 2

```
#include <INTRINS.H>
#include <REG51F.H>
unsigned char go;
void timer_ISR (void) interrupt 1
{
 go=1;
} /* this exits IDLE Mode */
void main()
{
            signed int x1;
            signed int y1;
            idata signed int x;
            idata signed int y;
            xdata signed int x2;
            xdata signed int y2;
            xdata signed int z2;
            idata signed int z;
            signed int z1;
             while(1)   {
  AUXR= 0x03;/* For ATMEL and PHILIPS parts AUXR= 03h (02h) for ALE
  P1= 0xAF; OFF (ON); for Max-Dallas part AUXR is replaced by PMR. PMR
  x=0x0019; = 80h (84h) for ALE OFF (ON) */
  x1=0x0018;
  x2=0x0017;
                        y=0x1070;
  y1=0x1070;
 y2=0x1070;
 z= (x1+(y1*y2))/((x1*x2)+y1+(x*x1*y2));
 z1= (x1+(y1*y2))/((x1*x2)+y1+(x*x1*y2));
  z2= (x1+(y1*y2))/((x1*x2)+y1+(x*x1*y2));
 y2= x2& ~(0xFF >> 4);
 y= x1^~(0xFF >> 4);
                        P1= 0x5F;
                        TR0 = 0;        /* Stop Timer 0 */
 TMOD=0x01;
  TL0=-10;
  ET0 = 1;        /* Enable Timer0 Interrupt */
  TR0 = 1;        /* Start Timer 0 */
  EA = 1;/* Enable Global Interrupts */
```

```
 PCON = 0x01;
 TR0=0;
  TMOD=0x02;
  TH0=-10;
 TL0=-10;
  ET0 = 1;          /* Enable Timer0 Interrupt */
  TR0 = 1;
  EA=1;
                          P1 = 0xFF;
 go=0;
while(go==0){}
 P1 = 0xEF;
 go=0;
 while(go==0){}
 P1 =0xDF;
  go=0;
 while(go==0){}
P1 = 0xCF;
  go=0;
 while(go==0){}
 P1 = 0xBF;
 go=0;
 while(go==0){}
 P1 = 0xAF;
 go=0;
 while(go==0){}
 P1 = 0x9F;
 go=0;
 while(go==0){}
 P1 = 0x8F;
 go=0;
 while(go==0){}
 P1 = 0x7F;
 go=0;
                          while(go==0){}
 P1 = 0x6F;
 go=0;
while(go==0){}
P1 = 0x5F;
 go=0;
 while(go==0){}
 P1 = 0x4F;
 go=0;
 while(go==0){}
 P1 = 0x3F;
 go=0;
```

```
  while(go==0){}
  P1 = 0x2F;
  go=0;
  while(go==0){}
  go=0;
 P1 = 0x1F;
  while(go==0){}
  P1 = 0x0F;
  go=0;
  while(go==0){}
  TR0=0;
   EA=0;
   x=0x0000;
   x1=0x0000;
   x2=0x0000;
  y=0x0000;
  y1=0x0000;
   y2=0x0000;
  }
}
```

APPENDIX- C
SPECIFICATIONS OF THE THREE MICROCONTROLLERS

ATMEL (AT89C51RB2)

• 80C52 Compatible
  – 8051 Pin and Instruction Compatible
  – Four 8-bit I/O Ports
  – Three 16-bit Timer/Counters
  – 256 Bytes Scratch Pad RAM
  – 9 Interrupt Sources with 4 Priority Levels
  – Dual Data Pointer
• Variable Length MOVX for Slow RAM/Peripherals
• ISP (In-system Programming) Using Standard VCC Power Supply
• Boot ROM Contains Low Level Flash Programming Routines and a Default Serial Loader
• High-speed Architecture
  – In Standard Mode:
    40 MHz (Vcc 2.7V to 5.5V, both Internal and external code execution)
    60 MHz (Vcc 4.5V to 5.5V and Internal Code execution only)
  – In X2 mode (6 Clocks/machine cycle)
    20 MHz (Vcc 2.7V to 5.5V, both Internal and external code execution)
    30 MHz (Vcc 4.5V to 5.5V and Internal Code execution only)
  – 16K/32K Bytes On-chip Flash Program/Data Memory
  – Byte and Page (128 Bytes) Erase and Write
  – 100K Write Cycles
• On-chip 1024 Bytes Expanded RAM (XRAM)
  – Software Selectable Size (0, 256, 512, 768, 1024 Bytes)
  – 256 Bytes Selected at Reset for TS87C51RB2/RC2 Compatibility
• Keyboard Interrupt Interface on Port P1
• SPI Interface (Master/Slave Mode)
• 8-bit Clock Prescaler
• Improved X2 Mode with Independent Selection for CPU and Each Peripheral
• Programmable Counter Array 5 Channels
  – High-speed Output
  – Compare/Capture
  – Pulse Width Modulator
  – Watchdog Timer Capabilities
• Asynchronous Port Reset
• Full Duplex Enhanced UART
• Dedicated Baud Rate Generator for UART
• Low EMI (Inhibit ALE)

• Hardware Watchdog Timer (One-time Enabled with Reset-out)
• Power Control Modes
  – Idle Mode
  – Power-down Mode
  – Power-off Flag
• Power Supply:
  – 2.7 to 3.6 (3V Version)
  – 2.7 to 5.5V (5V Version)
• Temperature Ranges: Commercial (0 to +70°C) and Industrial (-40°C to +85°C)
• Packages: PDIL40, PLCC44, VQFP44

PHILIPS (P89V51RB2)

• 80C51 CPU
• 5 V operating voltage from 0 MHz to 40 MHz
• 16/32/64 kB of on-chip flash user code memory with ISP and IAP
• Supports 12-clock (default) or 6-clock mode selection via software or ISP
• SPI and enhanced UART
• PCA with PWM and capture/compare functions
• Four 8-bit I/O ports with three high-current port 1 pins (16 mA each)
• Three 16-bit timers/counters
• Programmable watchdog timer
• Eight interrupt sources with four priority levels
• Second DPTR register
• Low EMI mode (ALE inhibit)
• TTL- and CMOS-compatible logic levels
• Brownout detection
• Low power modes
  – Power-down mode with external interrupt wake-up
  – Idle mode
• DIP40, PLCC44 and TQFP44 packages

MAX-DALLAS (DS89C430)

• High-Speed 8051 Architecture
  – One Clock-Per-Machine Cycle
  – DC to 33MHz Operation
  – Single Cycle Instruction in 30ns
  – Optional Variable Length MOVX to Access Fast/Slow Peripherals

  – Dual Data Pointers with Automatic Increment/Decrement and Toggle Select
  – Supports Four Paged Memory-Access Modes

• On-Chip Memory
  – 16kB/64kB Flash Memory
  – In-Application Programmable
  – In-System Programmable Through Serial Port
  – 1kB SRAM for MOVX

• 80C52 Compatible
  – 8051 Pin and Instruction Set Compatible
  – Four Bidirectional, 8-Bit I/O Ports
  – Three 16-Bit Timer Counters
  – 256 Bytes Scratchpad RAM

• Power-Management Mode
  – Programmable Clock Divider
  – Automatic Hardware and Software Exit

• ROMSIZE Feature
  – Selects Internal Program Memory Size from 0 to 64kB
  – Allows Access to Entire External Memory Map
  – Dynamically Adjustable by Software

• Peripheral Features
  – Two Full-Duplex Serial Ports
  – Programmable Watchdog Timer
  – 13 Interrupt Sources (Six External)
  – Five Levels of Interrupt Priority
  – Power-Fail Reset
  – Early Warning Power-Fail Interrupt
  – Electromagnetic Interference (EMI) Reduction

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VITA

Vijay Kasturi was born on March 18, 1984, in Kakinada, Andhra Pradesh, India. In June 2001, he received his Bachelor's of Technology in Electronics and Communication Engineering from Vallurupalli Nageswara Rao Vignana Jyothi Institute of Engineering and Technology (affliated to Jawharlal Nehru Technological University), Hyderabad, India. He joined the Master's program in Electrical Engineering at the University of Missouri-Rolla in Fall 2005. While pursuing his graduate degree, he was supported by the department of Electrical Engineering as a Graduate Research Assistant in the Electromagnetic Compatibility Laboratory.