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Time-domain thru-reflect-line (TRL) calibration error assessment and its mitigation and modeling of multilayer printed circuit boards (PCB) with complex area fills

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TIME-DOMAIN THRU-REFLECT-LINE (TRL) CALIBRATION ERROR ASSESSMENT AND ITS MITIGATION AND MODELING OF MULTILAYER PRINTED CIRCUIT BOARDS (PCB) WITH COMPLEX AREA FILLS

by

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ABSTRACT

Part 1 for this thesis is on the error assessment of a time-domain (t-TRL) calibration technique. Application of the “Thru-Reflect-Line” (TRL) calibration to time-domain measurements of S-parameters (t-TRL) can be used for the characterization of the printed circuit boards (PCBs). However, t-TRL calibrated results still have deviations from the reference frequency-domain vector network analyzer (VNA) calibrated results. There are two main sources of errors in the t-TRL calibration. They are random errors, such as an additive noise and jitter, and systematic errors associated with cables, connectors, and port mismatches. This work addresses these two types of errors by proper selection of the number of sampling points, waveform averages, and time record. Methods tried out to eliminate or reduce these errors are detailed in this work. Measurements and simulations were performed for implementing these methods, and the results are explained. A t-TRL calibration automation tool based on TDR/TDT measurements has been developed.

Part 2 of this thesis is on the modeling of multilayer PCBs with complex area fills and floating planes. Noise on the power distribution network (PDN) and between the power area fills in multilayer PCBs with complex geometries is a significant concern. Modeling of such PCBs can be done with a cavity model approach. Correlation of a 3D EM solver results with the Multilayer Via Transition Tool (MVTT) results based on cavity model is explained here. Additional modeling and validation was done using the equivalent inductance method.

ACKNOWLEDGMENTS

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Finally, I thank my parents and fiancée for their constant emotional support and encouragement. I wish to dedicate this work to them.

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1. INTRODUCTION TO TIME-DOMAIN CALIBRATION

Measurements are subject to uncertainty. These uncertainties characterize the deviation of the measured values from the actual values. Un-corrected measurements or measurements without any calibration technique applied will have less accuracy but can be very fast and easy. In the case of S-parameter measurements using vector network analyzers (VNA), the device under test (DUT) measured will have the effects of the cables, connectors, measurement errors and port mismatches. The true response of the DUT can be obtained if these effects are removed or characterized.

Interconnect and printed circuit board (PCB) characterization using conventional calibration methods are widely used in high-speed digital systems. Accurate wideband characterization of PCB dielectric materials is becoming increasingly important for the high-speed digital designs as the data rates are raising. The material properties governing the performance of the signal passing through a transmission line are frequency-dependent. The characterization implies measuring S-parameters of the transmission line and extraction of the dielectric substrate parameters, such as relative permittivity or dielectric constant Dk and loss tangent or dissipation factor Df [1]. The measurements can be performed using a conventional VNA in the frequency-domain.

Application of the "Thru-Reflect-Line" (TRL) calibration technique to the VNAs allows for calibrating the instrument to take into account the discontinuities associated with the cable and on-board connectors [2]. However, the cost of a VNA is high. At the same time, time-domain reflection/transmission measurements can be a cheaper alternative to the VNA. Time-domain Reflectometry (TDR) allows for cost effective and faster ways to characterize the PCBs for high-speed digital design. In this work, time-domain calibration using TDR is studied and the errors associated with the calibration is identified. Methods for eliminating these errors are in the literature. These methods were implemented and the results are analyzed.

Application of the TRL calibration technique to time-domain measurements (t-TRL) assumes the calculation of TDR/TDT waveform spectra using the complete-fast-

Fourier-transform (CFFT) [4], and application of the TRL algorithm in the frequency-domain.

In reference [5], a complete step-by-step t-TRL calibration procedure has been detailed and compared to VNA measurements up to 25 GHz. It has been shown that the t-TRL technique is widely used for the characterization of the PCBs. However, t-TRL calibrated results still deviate from the reference frequency-domain VNA calibrated results. A block diagram of the time-domain calibration process is shown below in Figure 1.1. In reference [5], design of a complete TRL calibration pattern is explained. The design is based on the requirements of the TRL calibration standards [6].

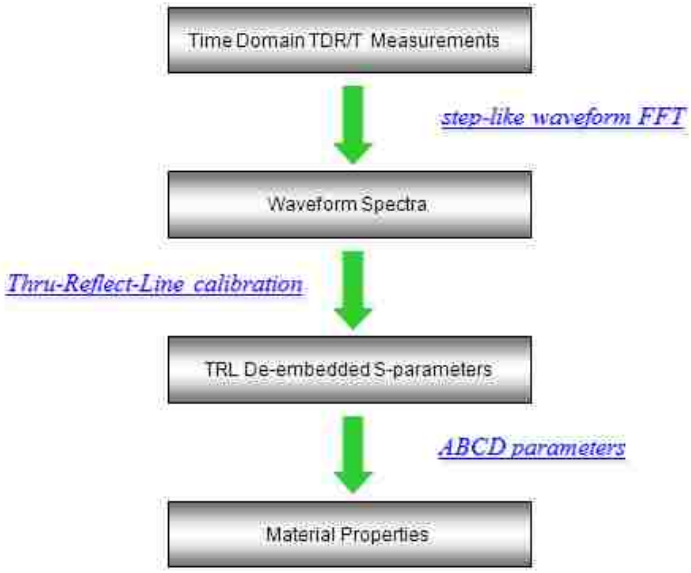

Figure 1.1: Block diagram of different stages of the time-domain calibration

The errors associated with the time-domain S-parameter measurements are analyzed in this work. The time-domain calibrated results are compared with the corresponding frequency-domain VNA measurements. Also, the material parameter extraction algorithm to the S-parameter measured in the time-domain is applied.

1.1. ERROR MODELS AND CALIBRATION METHODS

The TRL technique takes into account the discontinuities caused by the connector transitions and the connector-via transitions on the board. Figure 1.2 shows a block diagram of a similar connection to a PCB from a connector. There is cable to connector transition and then a connector to via transition. The DUT which is red in color, is a stripline structure as shown in the Figure 1.2. A Short-Open-Load-Thru (SOLT) calibration which is applied at the cables ends, does not take into account the connector to via transition. This transition is taken as a part of the DUT. The SOLT calibration leads to inaccurate measurement of the DUT. By applying a TRL calibration, the reference plane is shifted as shown in the Figure 1.4 and a more precise measurement can be made.

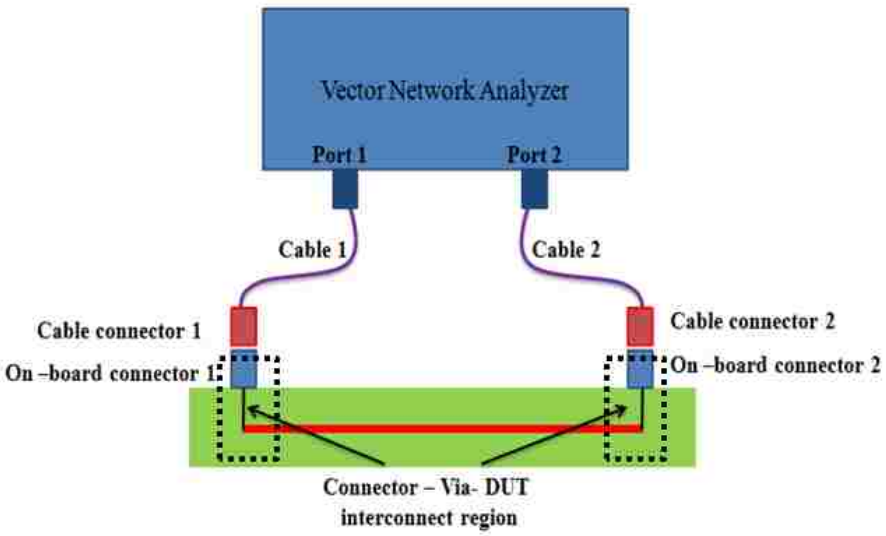

Figure 1.2: Block diagram representation of a two-port measurement system

The SOLT calibration reference plane is the blue line shown in the Figure 1.3. Here the DUT measurement will include the responses from the DUT along with the response from the unwanted interconnect region. The TRL calibration reference plane with respect to the DUT is shown in Figure 1.4, and will give the response of the DUT alone.

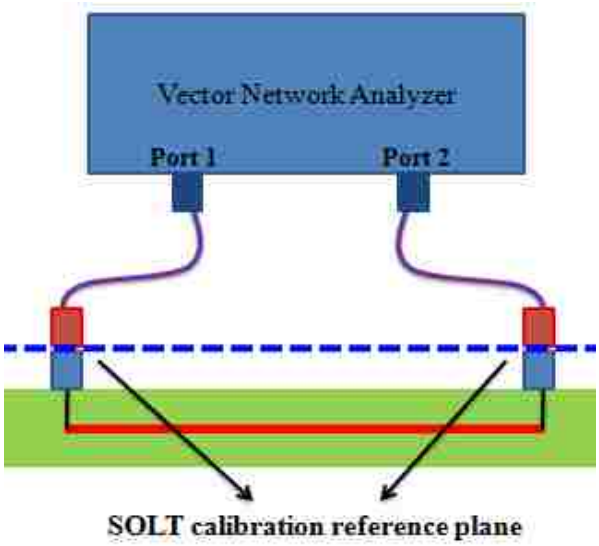

Figure 1.3: Block diagram showing the SOLT calibration reference plane with respect to the DUT for a two port measurement setup

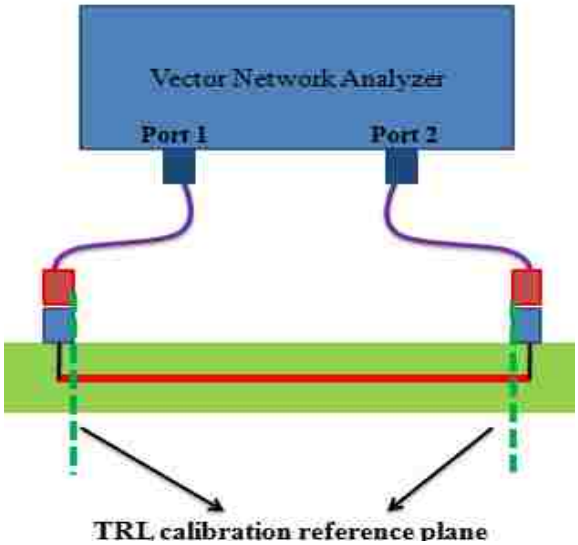

Figure 1.4: Block diagram showing the TRL calibration reference plane with respect to the DUT for a two port measurement setup

The calibration procedures make a marked improvement when measuring two port systems with adaptors, cables and other connectors. Some of the common errors that

are there in the two port calibration are directivity errors, frequency response errors and port mismatch errors. The calibration procedures will combine all the effects caused by the cables, connectors and ports into error terms or boxes. The number of error terms in general is the square of the number of ports. The error terms can be measured and by using the signal flow graph, a complete error model can be obtained. Depending upon the measurement which can be coaxial or non coaxial, and the measurement setup, different error models can be adopted for two port calibration.

It is important to understand the error models adopted. It is easy to explain the error models from a VNA perspective. The error models of the frequency-domain VNAs are similar to that of the time-domain VNAs. It is shown that general VNA calibration techniques apply directly in time-domain VNAs [9]. The difference is only in the internal circuitry of the VNA and TDR that measures the signals. A block diagram for a two port time-domain system and its signal flow graph are shown in Figure 1.5.

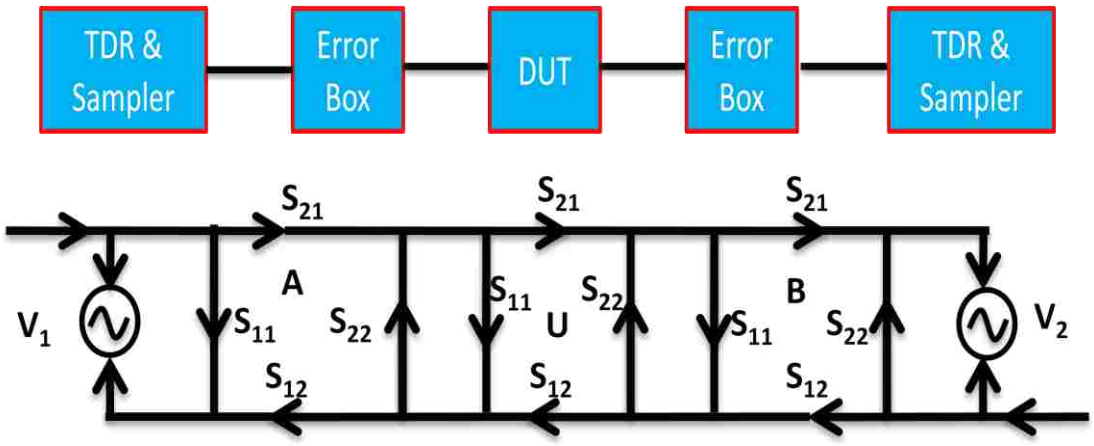

Figure 1.5: Block diagram and signal flow graph of a two port time-domain VNA system

The 12-term error model is widely used in calibration. As seen from Figure 1.6, the error model for the forward and reverse direction measurements has 12 error terms each [12]. There are 24 error terms in total. Out of these error terms, some primary error terms are taken into consideration and the 24-term error model is simplified.

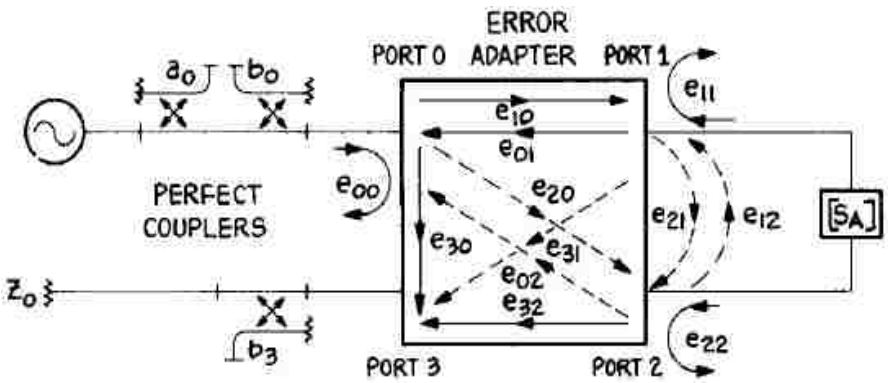

Figure 1.6: 12-term error model for the forward measurement direction

The error terms for the forward direction are:

- Port mismatch e_{11} when Port 1 is not terminated with a matched impedance and e_{22} when Port 2 is not terminated with a matched impedance
- Directivity e00 which is the ratio of the leakage of the incident signal to the reflected signal.
- Reflection tracking $e_{10}e_{01}$ and transmission tracking $e_{32}\, e_{10}$
- Leakage e_{30}, e_{20}, e_{02}, e_{31}, e_{21} and e_{12} which are the crosstalk terms between the ports.

There are a total of 12 terms each for forward and reverse direction. Thus there is a sum total of 24 error terms. Certain error terms are not significant in terms of the signal strength when compared to the other terms. These terms can be neglected and a simpler error model with fewer error terms results. After neglecting the insignificant error terms, the 24-term error model reduces to a 12-term error model, with primary error terms:

- Port mismatch e_{11} and e_{22}
- Directivity e_{00}
- Reflection tracking $e_{10}e_{01}$ and transmission tracking $e_{32}\, e_{10}$
- Leakage e_{30}

Solving the 12 term error model can give four simultaneous measured S parameter equations [12]. Signal flow graphs for the forward and reverse measurements are shown in Figure 1.7 and Figure 1.8.

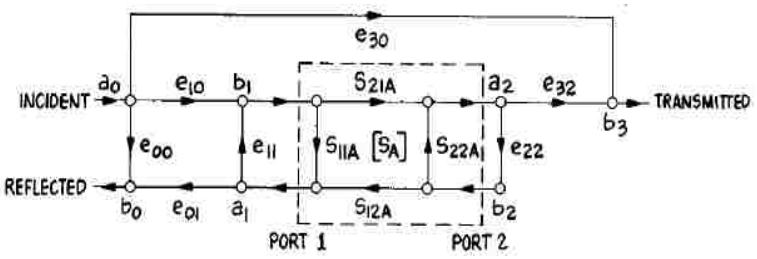

Figure 1.7: Error model for forward measurements with excitation on Port 1

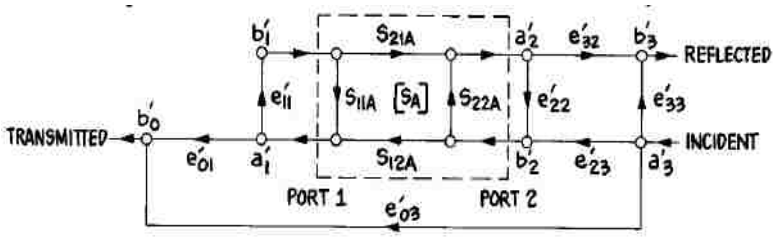

Figure 1.8: Error model for reverse measurements with excitation on Port 2

Each actual S-parameter calculated from a DUT measurement needs all four S-parameters as well as the 12 error terms. Two measurements each can be made for the forward where the excitation is on Port 1 and the reverse directions where the excitation is on Port 2. Each of them is a function of the four S-parameters of the DUT as well as the error terms. Error terms can be obtained from the calibration procedure. The signal flow graphs can be solved to get the actual S-parameters of the DUT.

An eight term error model can be derived from the 12-term model. The basic assumption is that the VNA switch is prefect and has same S-parameters for both forward and reverse direction measurements [12]. The error adaptor is separated into an X-error adapter and Y-error adapter as shown in Figure 1.9. There will be no leakage between the adapters. Here the measurement is modified with error adapter X on one side for Port 1

and error adapter Y on the other side for Port 2 as shown in Figure 1.10. The well known calibration using the 8 term error model is the TRL calibration [2]. The eight error terms are e_{10}, e_{01}, e_{00} and e_{11} for Port 1and e_{32}, e_{23}, e_{22} and e_{33}. The error model of the 8 term model is shown in Figure 1.11

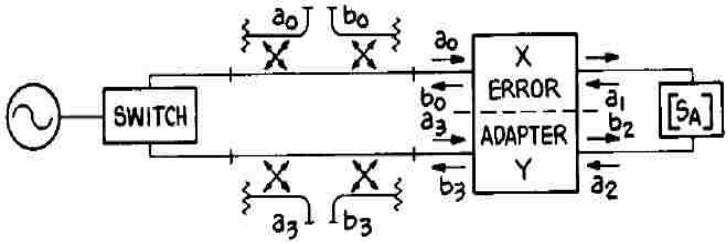

Figure 1.9: 8-term error adapter for two port measurements

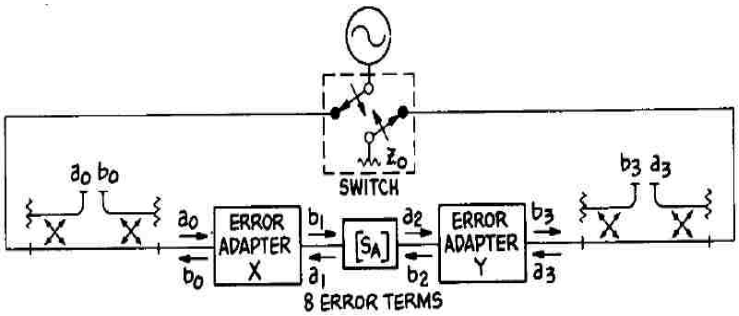

Figure 1.10: Two separate error adapters with 8 error terms in total

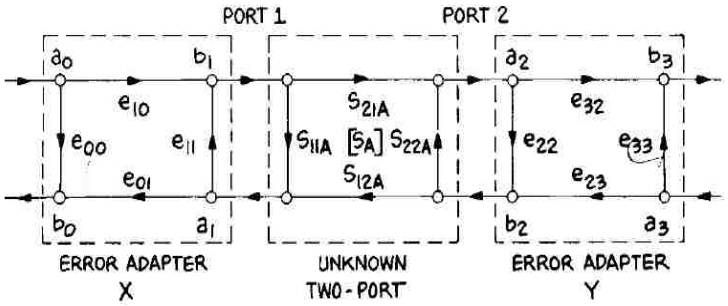

Figure 1.11: 8-term error model for two port measurements

For calculating the error terms, there are different calibration methods. There are mainly two calibration procedures for two port systems. An SOLT calibration, which is fast and has good accuracy but is problematic to use for non-coaxial measurements and the TRL calibration, which is time consuming and has very good accuracy and is suitable for non-coaxial media.The SOLT calibration is a widely used calibration method [12]. One set of measurements is used for the forward direction on Port 1 and same set of measurements is used for reverse direction on Port 2. It is very important to accurately know the terminations used for the measurements. The first set of measurements is done with a Short, an Open, and a Load on Port 1. These measurements allow characterization of these three error terms for one measurement direction which are the equivalent directivity e_{00}, the port mismatch e_{11}, and the reflection tracking e_{l0e01} as shown in Figure 1.12. 12-term error model has a leakage term. SOLT calibration allows considering this leakage term too [12]. Leakage term (e30) is measured by placing matched terminations on both ports as shown in Figure 1.13. The final part is connecting port 1 and port 2 together. This is the THRU connection as shown in Figure 1.14.

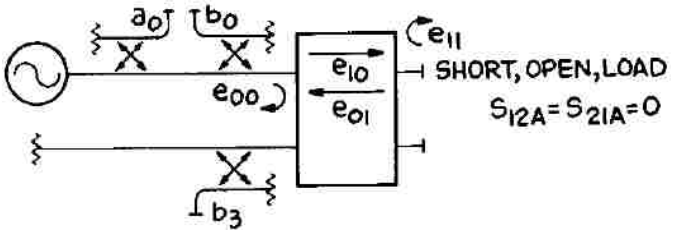

Figure 1.12: Setup to measure the directivity, port match and frequency response

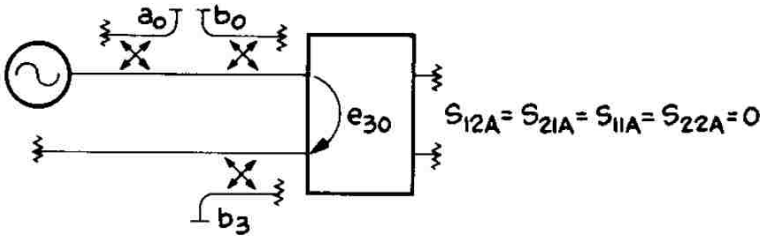

Figure 1.13: Setup to measure the leakage term

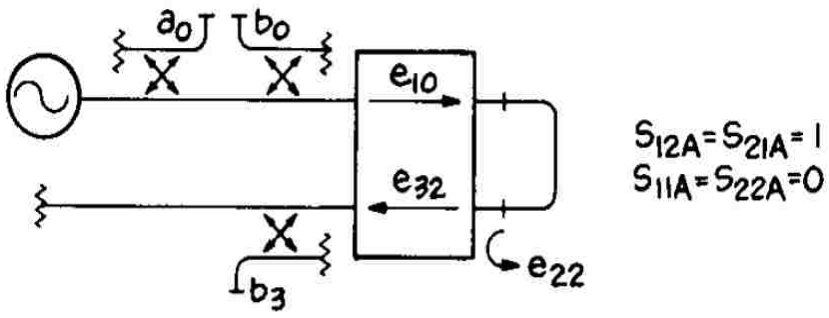

Figure 1.14: Thru measurement setup

These three sets of measurements can yield six error terms for the forward directions. Another set for the reverse directions, then all the 12 error terms can be measured. The SOLT calibration is based on the known short, open and matched standards. One of the main disadvantages of the SOLT calibration is that the standards used are always imperfect to some degree. It is practically difficult to make a perfect open. A short standard will have some inductance associated with it, and the open standard will have some fringing capacitance. These imperfections lead to errors in the measurements. These errors will be significantly larger at higher frequencies.

The TRL calibration does not rely on known standards. It needs three connections such as a Thru, Reflect and Line. The reflect connection can be a short or open which basically has a large reflection coefficient. These connections are applied at the reference plane and the S-parameters are measured. The error boxes are characterized by S-parameters. Using equations obtained from the signal flow graphs; measured S-parameters are obtained at the measurement plane in terms of the S-parameters of the error boxes. S-parameters of the DUT can be measured and then corrected using the TRL error boxes to get the S-parameters at the reference planes. Basic TRL requirements of the standards are noted below. The TRL Calibration standard selection is as follows.

For the Reflect standard, the reflection coefficient (Γ) magnitude need not be known and the phase of the Γ must be known within ± ¼ wavelengths. For non-zero length THRU, the characteristic impedance Z_0 of the THRU and LINE must be same, and the attenuation of the THRU is assumed to be zero. For the LINE standard, the Attenuation of the LINE need not be known, the phase need to be specified within ¼

wavelengths, the bandwidth of the single THRU/LINE pair is 8:1 and the TRL calibration references the DUT S-parameters to the impedance of the LINE standard. For the Match standard, it assumes matched terminations on both ports.

A network analyzer measures S-parameters as the ratios of complex voltages. The reference plane is at some point inside the VNA, so the measurement will include losses and phase delays caused by the effects of connectors, cables, port mismatch, via transitions etc. A calibration method can include these effects as error boxes placed between the measurement plane and the desired reference plane. A calibration technique can then characterize these error boxes and the error corrected S-parameters of the DUT can be obtained.

1.2. ERROR ASSESSMENT OF THE T-TRL CALIBRATION TECHNIQUE

One of the major goals of the t-TRL project is to assess the errors associated with the TRL implementation and the measurement process. The instrument used in the beginning of the work was the Agilent DCA-J 86100C TDR module with 35ps rise time. The receiver bandwidth of this model is 18GHz. The second instrument used was a Tektronix DSA 8200 with E10 TDR modules. The maximum bandwidth of E10 modules is 50GHz. The entire measurement procedure is automated into a calibration wizard tool, which is explained later. A calibration wizard works as a standalone application and lets the user to do the measurement/t-TRL calibration easily.

The measurement test setup is shown below in Figure 1.15. The cables used for the measurements are from Gore Associates and are very low loss cables. The connectors are 3.5mmm precision. The connectors on the board are 3.5 mm female SMA Molex connectors. Most of the measurements were taken after one or one and half hours after switching on the instrument. This was done to make sure that the instrument is warmed up and in stable working condition. THE time-domain measurements are performed using t-TRL calibration tool. The tool measures and save the time-domain waveforms and process the waveforms using the TRL calibration technique to give the calibrated S-parameters of the DUT.

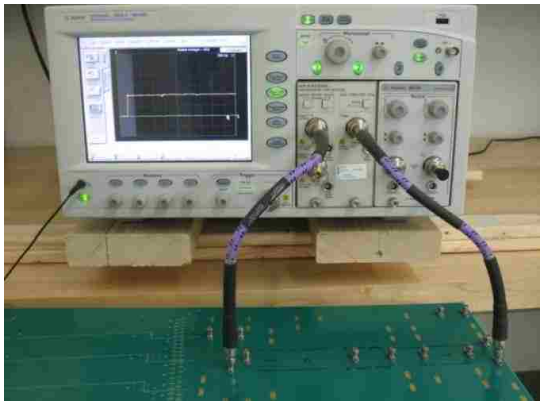

Figure 1.15: TRL calibration measurement setup using Agilent DCA-J 86100C

There are two kinds of errors associated with t-TRL measurements. They are random errors and systematic errors. Random errors are due to the noise of the TDR receiver and generator, as well as time jitter and calibration imperfections because of connector inconsistency and cable bend. Systematic errors are caused by cable and connector effects, port mismatches, and nonlinearities of the instrument. These systematic errors, associated with the instrument ports, cables and connectors, can be effectively eliminated by the proper TRL calibration, as VNA measurements show. At the same time, application of the t-TRL calibration to the measurements by two TDR instruments with different bandwidths results in residual errors, illustrated by Figure 1.16 and Figure 1.17. TDR 1 has 18 GHz bandwidth and TDR 2 has 50 GHz bandwidth. Parameters of the TRL kits 1 and 2 applied for calibrating these two TDR instruments and VNAs are explained in the paper [5].

These TRL kits were manufactured using standard PCB technology with copper-clad FR-4 type dielectric substrates. The VNA results are used as reference. Magnitude of S_{11} measured by t-TRL using TDR 1 for calibration Kit 1 and 2 are shown in Figure 1.16 and Figure 1.17. The phase of S_{21} measured by t-TRL using TDR 1 for calibration Kit 1 and 2 are shown in Figure 1.18 and Figure 1.19 and the magnitude of S_{11} measured by t-TRL using TDR 1 for calibration Kit 1 and 2 are shown in Figure 1.20 and Figure 1.21.

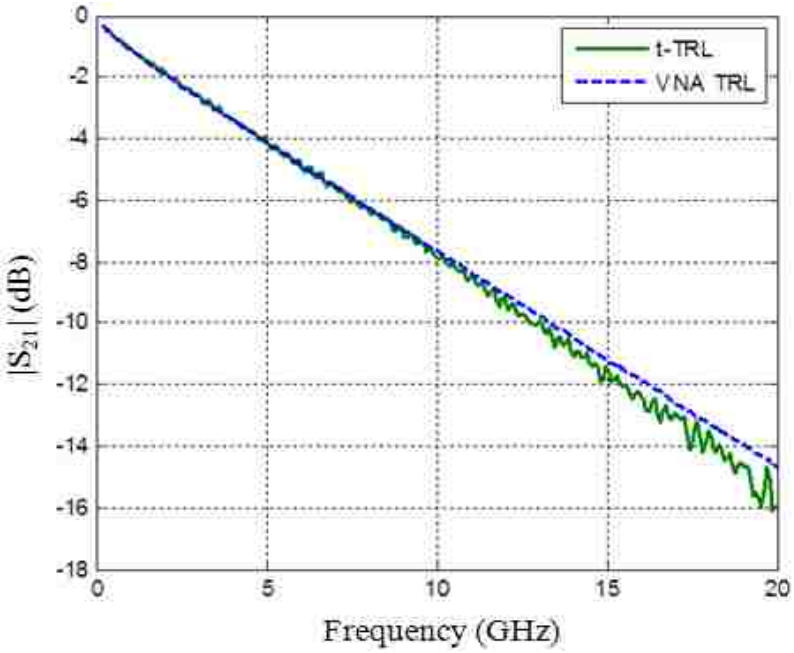

Figure 1.16: S_{21} magnitude comparison of the Test Line 1 of the Calibration Kit 1 measured by t-TRL using the TDR 1 and VNA TRL

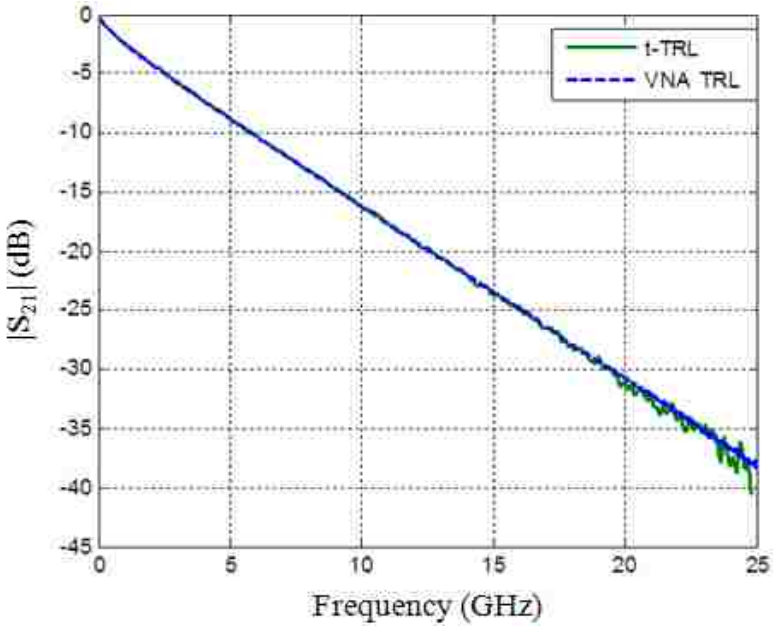

Figure 1.17: S_{21} magnitude comparison of the Test Line 1 of the Calibration Kit 2 measured by t-TRL using the TDR 2 and VNA TRL

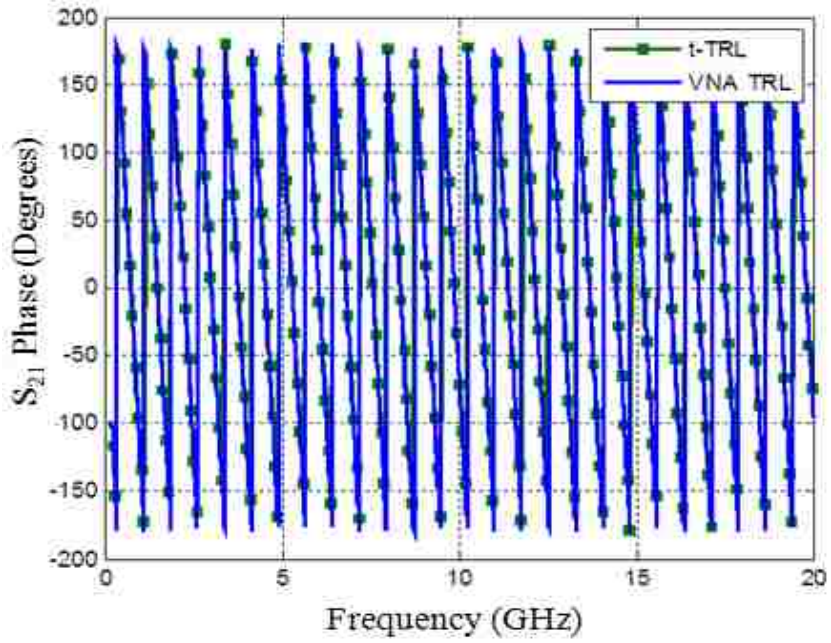

Figure 1.18: Phase of the S_{21} comparison of the Test Line 1 of the Calibration Kit 1 measured by t-TRL using the TDR 1 and VNA TRL

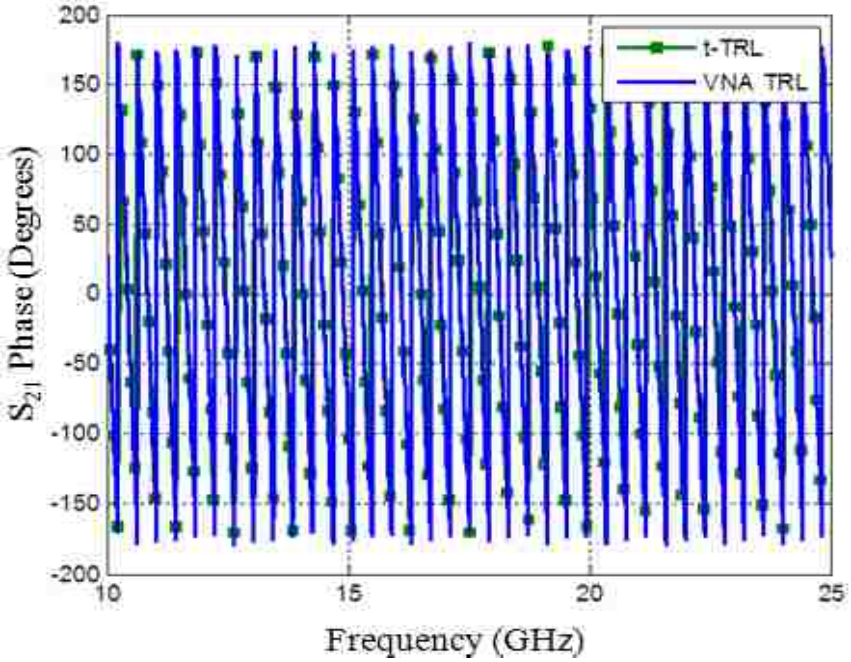

Figure 1.19: Phase of the S_{21} comparison of the Test Line 1 of the Calibration kit 2 measured by t-TRL using the TDR 2 and VNA TRL

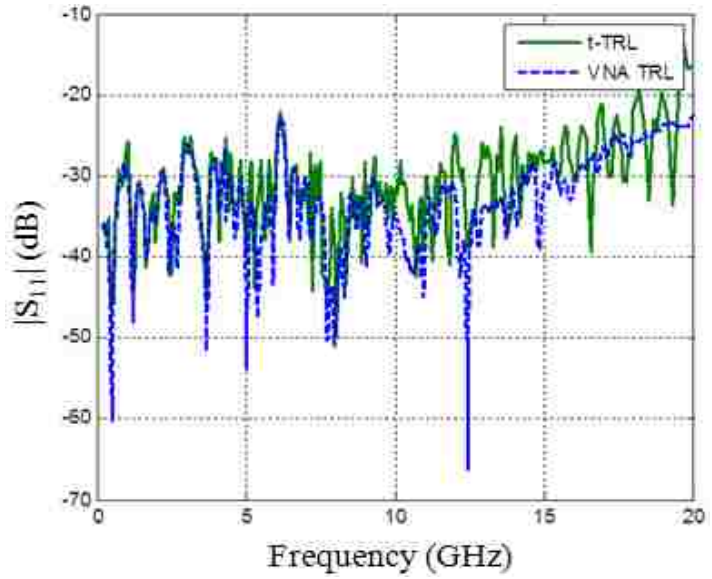

Figure 1.20: S_{11} magnitude comparison of the Test Line 1 of the Calibration Kit 1 measured by t-TRL using the TDR 1 and VNA TRL

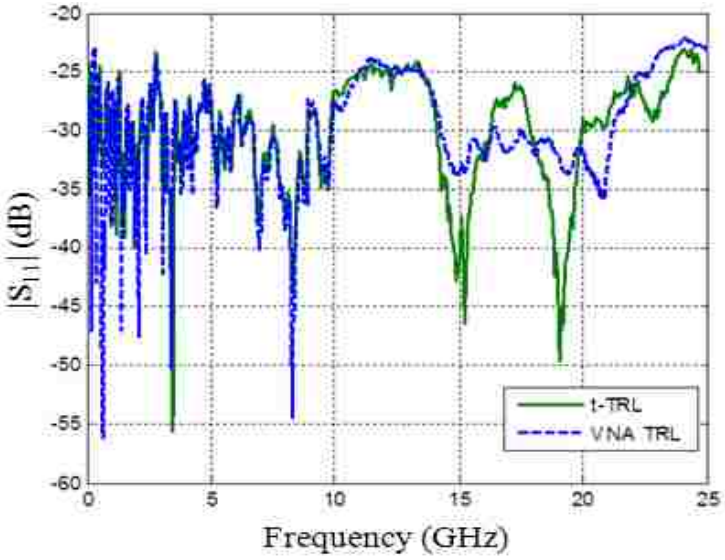

Figure 1.21: S_{11} magnitude comparison of the Test Line 1 of the Calibration Kit 2 measured by t-TRL using the TDR 2 and VNA TRL

The error in S_{21} measurement is approximately 1.5 dB for TDR 1 and 1 dB for TDR 2 at 20 GHz. The phase error is 4 degrees for TDR 1 and 7 degrees for TDR 2 at 20 GHz which is a minor value considering the electrical length of the line. The accuracy of

the S_{11} measurement of the transmission lines is not critical for most applications. A statistical analysis was performed in order to determine the nature of errors in the S_{21} measurements. Magnitude of S_{21} of the test transmission line was measured by TDR 1 ten times, and the standard deviation σ was calculated which is shown in Figure 1.22. The discrepancy between the t-TRL TDR measurement and frequency-domain VNA TRL measurement of S_{21} is about 1.5 dB at 20 GHz as shown in Figure 1.16.

At the same time, the standard deviation σ of t-TRL S_{21} measurement is less than 0.4 dB at the same frequency. This indicates that the systematic component in the S_{21} measurement error dominates. The same conclusion can be made by estimating the signal-to-noise ratio (SNR) of the transmitted signal for the test line. The TDT signal was measured for test line 1 of the cal kit 1 using TDR 1. The spectrum of the TDT signal is shown on Figure 1.23. The curve in Figure 1.23 can be used to roughly estimate signal-to-noise ratio in the frequency range of interest. For this purpose, the noise was approximated as having a uniform spectrum in the frequency range, and the signal spectrum was assumed to be a uniformly decreasing function. The estimation gives the value of 0 dB SNR at approximately 25 GHz, which is higher than the highest frequency in Figure 1.16. For this reason, the random noise may be not the dominating factor for the error in the S_{21} measurement for frequencies below ~25 GHz for the settings of the instrument indicated in the caption for Figure 1.23.

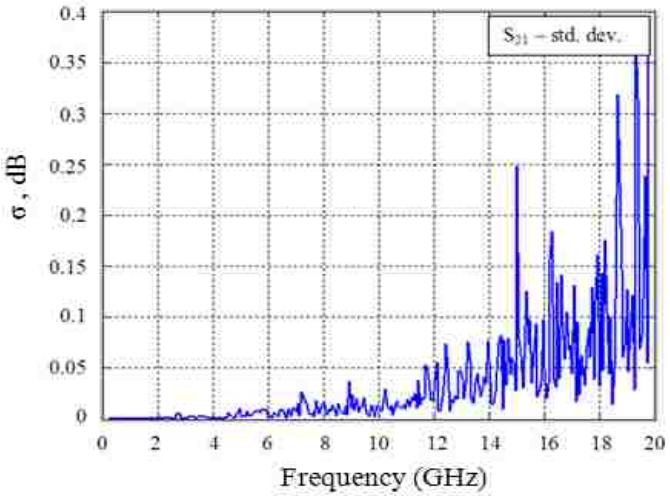

Figure 1.22: Estimation of the standard deviation of the S_{21} measurements

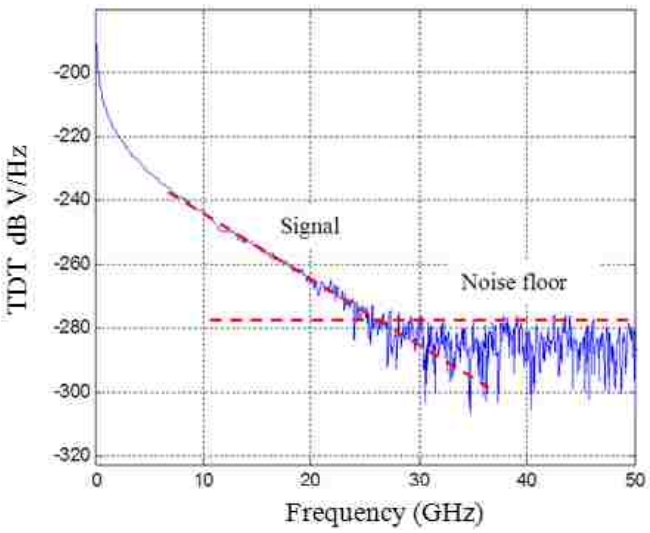

Figure 1.23: Spectrum of the TDT signal (TDR 1, 4096 samples, 10 ns time window, 256 averages)

Usually it is possible to achieve the SNR of at least 15 dB at 20 GHz for the used DUTs (10 or 16 inch test lines). In fact, the SNR can be further increased by varying the number of averages and the number of sampling points. According to [7], if all random errors are modeled as white noise, and the signal is modeled as an ideal step function, the SNR is defined as the ratio of the power spectral densities of signal and noise

$$SNR(f) = \frac{P_{sig}(f)}{P_{noise}(f)} = \frac{a^2}{2\pi^2} \frac{N_{pts}}{T^2 f^2} \frac{N_{avg}}{n^2}, \quad (1)$$

where N_{avg} is the number of waveforms averaged, N_{pts} is the number of samples, a is the signal amplitude, T is the time record, and n^2 is the white noise power. In order to increase the SNR, the number of samples and the number of averages should be increased, while the time record should be decreased. Theoretically, N_{pts} and N_{avg} do not have upper limits, and in practice they are limited by technical capabilities of the instrument and the acceptable measurement time. In contrast, the time record T has a lower limit determined by the DUT response. The choice of the minimum time record is illustrated below in Figure 1.24.

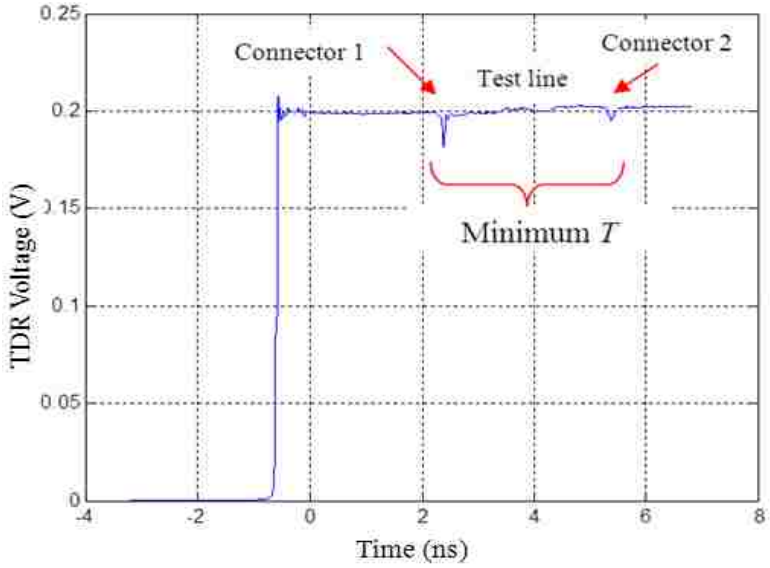

Figure 1.24: Minimum time record for TDR measurements

Therefore random noise cannot be a major factor limiting the performance of the t-TRL calibration, and SNR can be easily increased if needed by increasing N_{pts} and N_{avg}.

The interpolation of the frequency-domain results is explained now. The frequency resolution of the discrete Fourier transform is

$$\Delta f_{fft} = 1/N\Delta T, \tag{2}$$

where N is the number of time samples, and ΔT is the sampling period. The TDR/TDT signal spectra are computed by CFFT, which uses separate calculation procedures for odd and even frequency samples. Hence, the frequency resolution of the CFFT is doubled [4],

$$\Delta f_{cfft} = \frac{1}{2N\Delta T}, \tag{3}$$

For the time record of 10 ns, the frequency resolution of CFFT is 50 MHz. In practice, the part of the signal, which contains the incident TDR pulse and cable

response, is discarded, and the waveforms are windowed to eliminate the diode state error. This results in a reduced frequency resolution (however if the response of the DUT isn't affected by this windowing procedure, the useful information is not lost). At the same time, some applications may require an interpolation of the measured discrete S-parameters, and it can be done prior to the application of the TRL calibration by padding measured waveforms.

The usual way to interpolate discrete spectra is the use of zero-padding [10]. However, since the CFFT is intended to work with step-like functions, the waveform padding with zeros results in an error. To retain the step-like shape of a waveform, it is reasonable to pad it not with the zero, but with the value at its last sampling point. Figure 1.25 illustrates this interpolation technique in frequency-domain for the phase of S_{21}. The interpolated frequency resolution of the padded waveform is

$$\Delta f_i = \frac{1}{2(N + N_p)\Delta T}, \tag{4}$$

where N_p is the number of added samples.

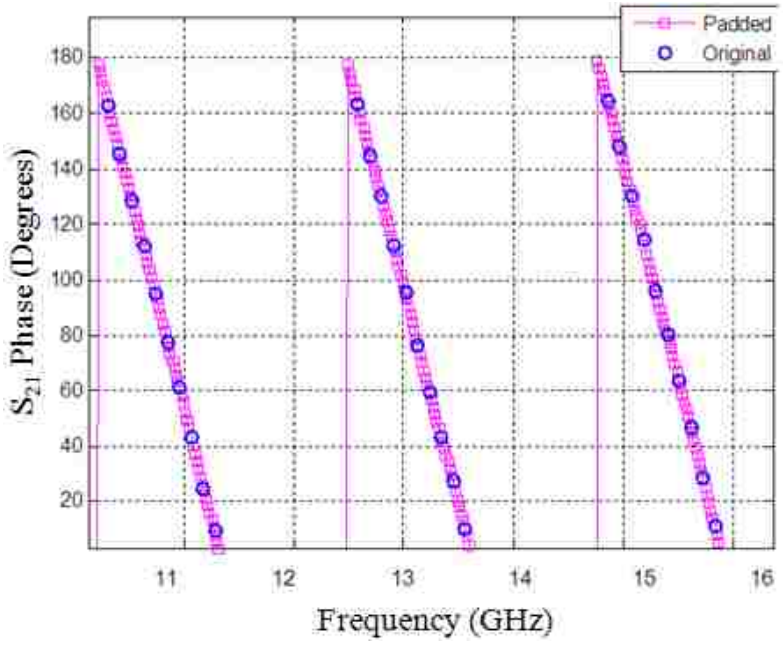

Figure 1.25: Result of padding – phase (10,000 points added).

1.2.1. ANALYZING RANDOM ERRORS. Experiments were done to analyze random errors. The measurement board used along with the calibration standards is shown below in Figure 1.26. The effect of the number of acquisition points was studied first. A firmware update was done on DCA-J 86100C which increased the number of acquisition points to 16834 points from 4096 points.

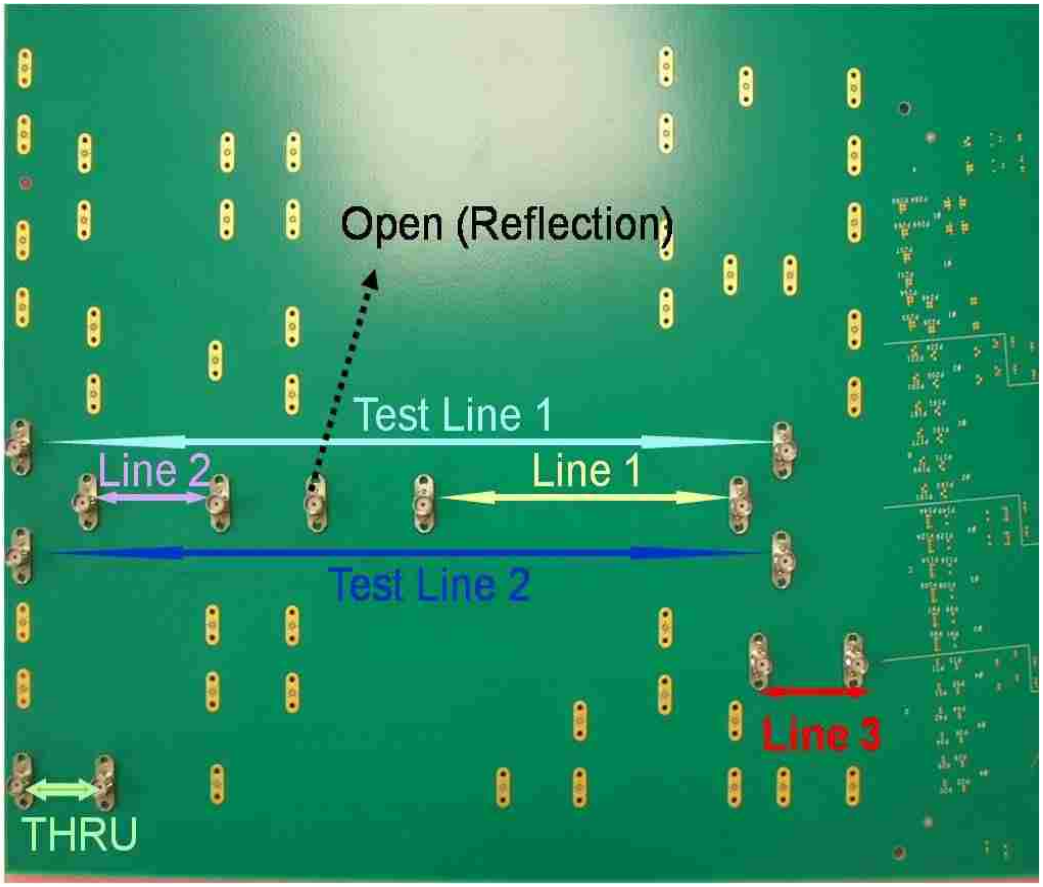

Figure 1.26: Test board used for the measurements

The timespan and the number of averages were fixed and the numbers of points were changed. Timespan was fixed at 1ns/div or 10 ns in total and the number of averages were 256. Magnitude of S_{11} and magnitude and phase S_{21} were plotted for this measurement setup as shown in Figure 1.27, Figure 1.28 and Figure 1.29.

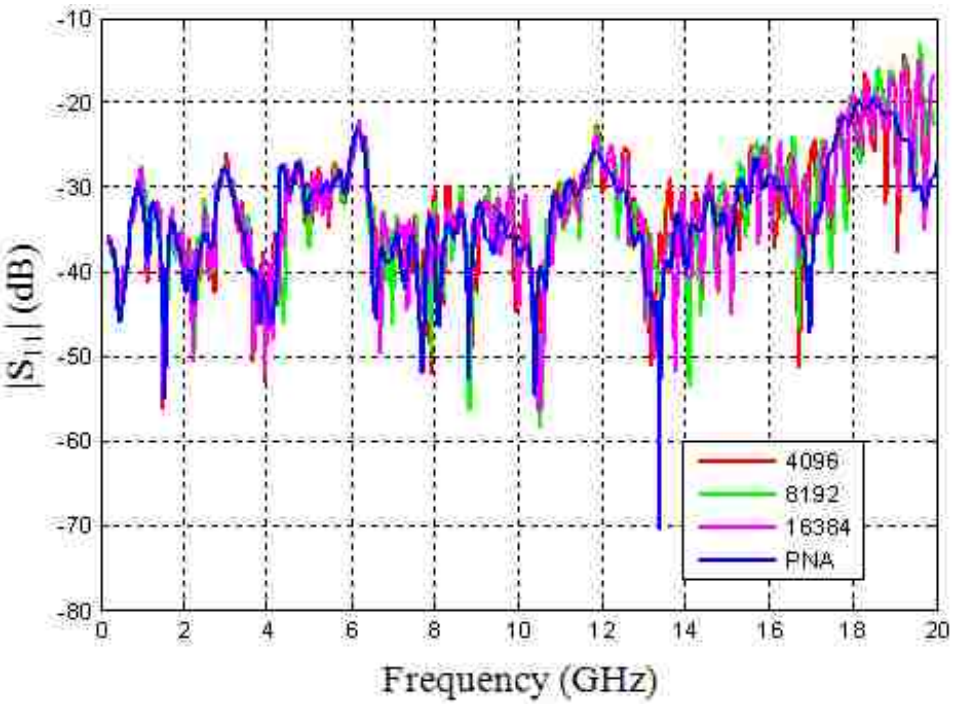

Figure 1.27: S_{11} magnitude comparison with VNA for different points

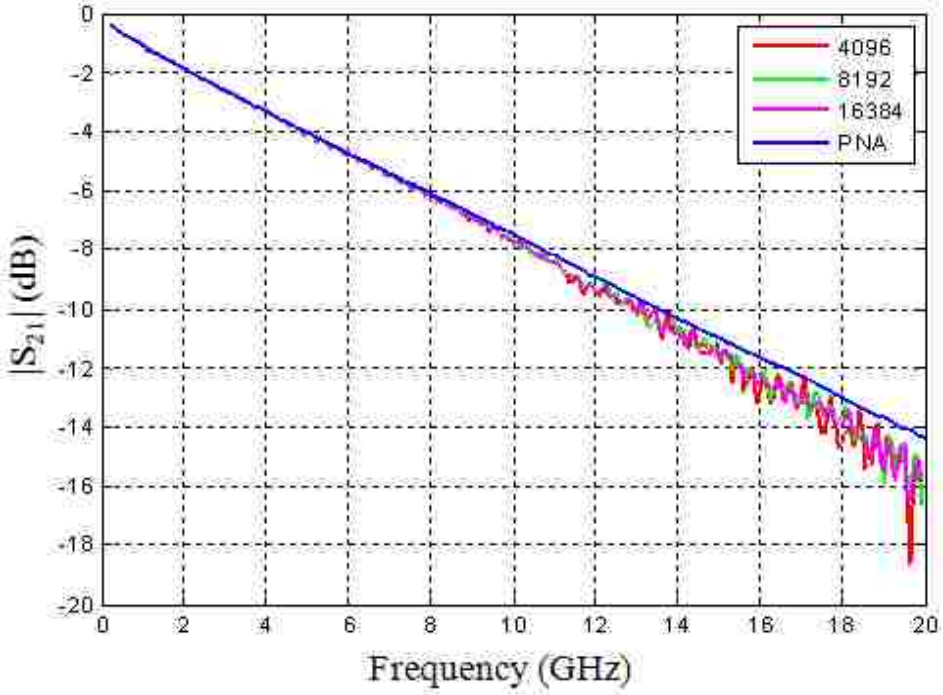

Figure 1.28: S_{21} magnitude comparison with VNA for different points

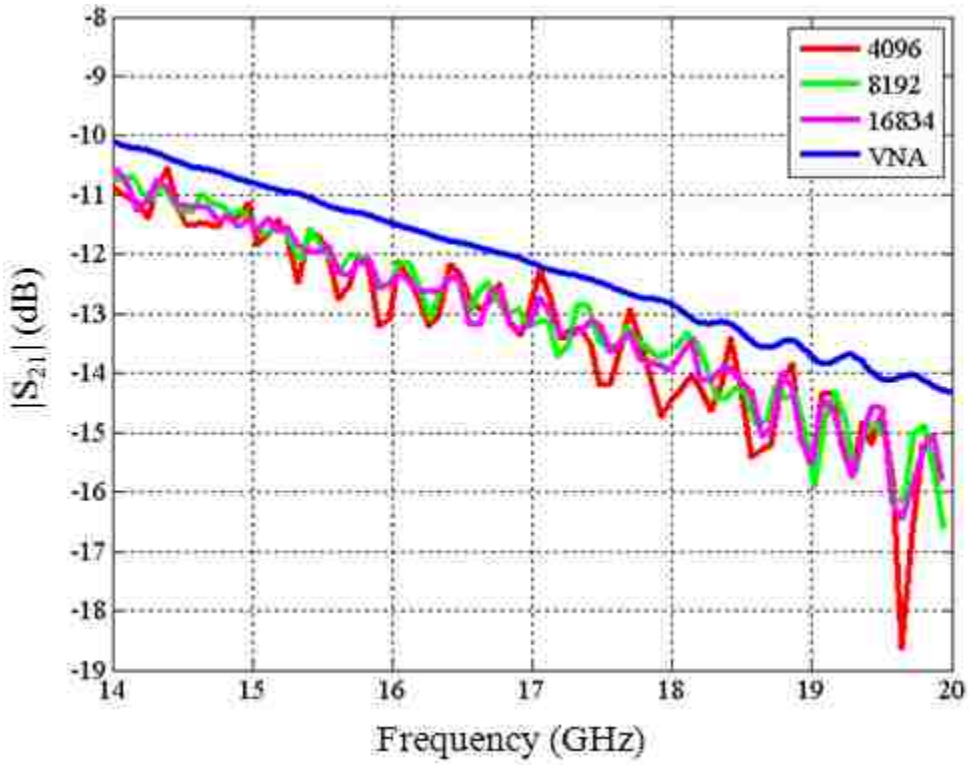

Figure 1.29: S_{21} magnitude comparison with VNA for different points – zoomed

The increase in number of acquisition points in the measurements is preferred as the SNR increases with the number of points/samples especially at higher frequencies. The time record or the timespan of the measurement was changed to study the effect of long waveforms. In this case the averages and the number of points were fixed at 256 and 16834 respectively and the time record was changed. Due to the large number of averages and points, the measurements can take long time. The magnitude of S_{11} and magnitude and phase of S_{21} were plotted for this measurement setup as shown in Figure 1.30, Figure 1.31, Figure 1.32 and Figure 1.32. The graphs show that the increase in time record decreases the SNR. S_{21} graph shows better correlation of the t-TRL result with the VNA measurement for 10ns time record than for the 40ns time record. The phase of S_{21} shows noise like undulations at higher frequencies. For better understanding of the correlation of the t-TRL results with the frequency-domain VNA for different time record results the difference between the t-TRL and VNA TRL are plotted in dB scale which are shown in figure 1.34 and figure 1.35.

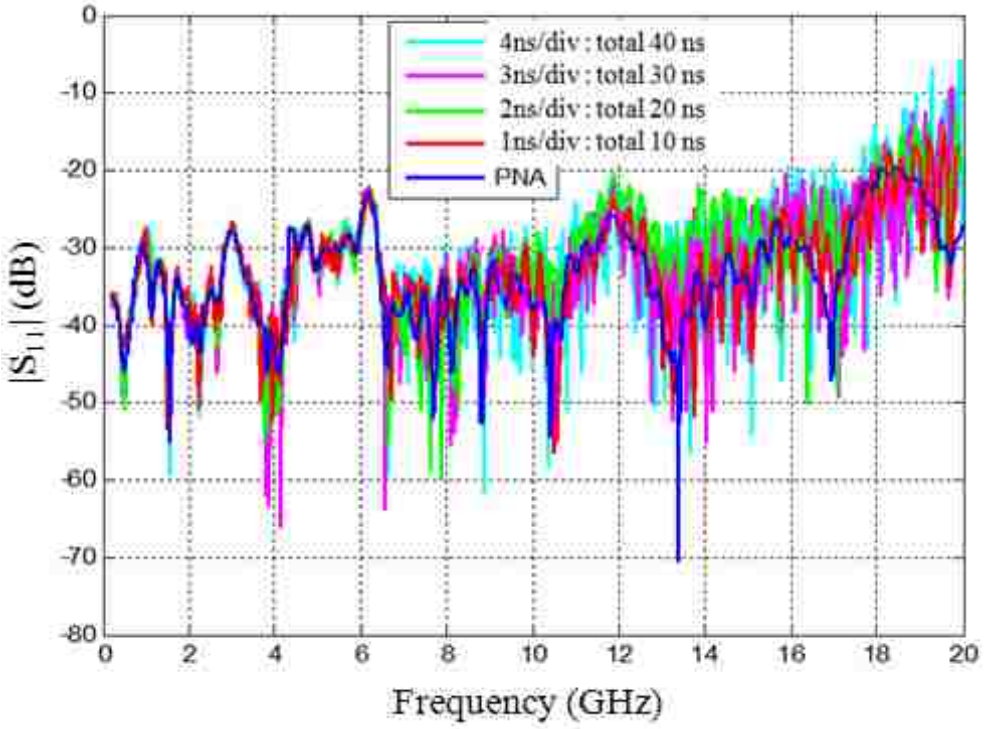

Figure 1.30: S_{11} magnitude comparison for different time record

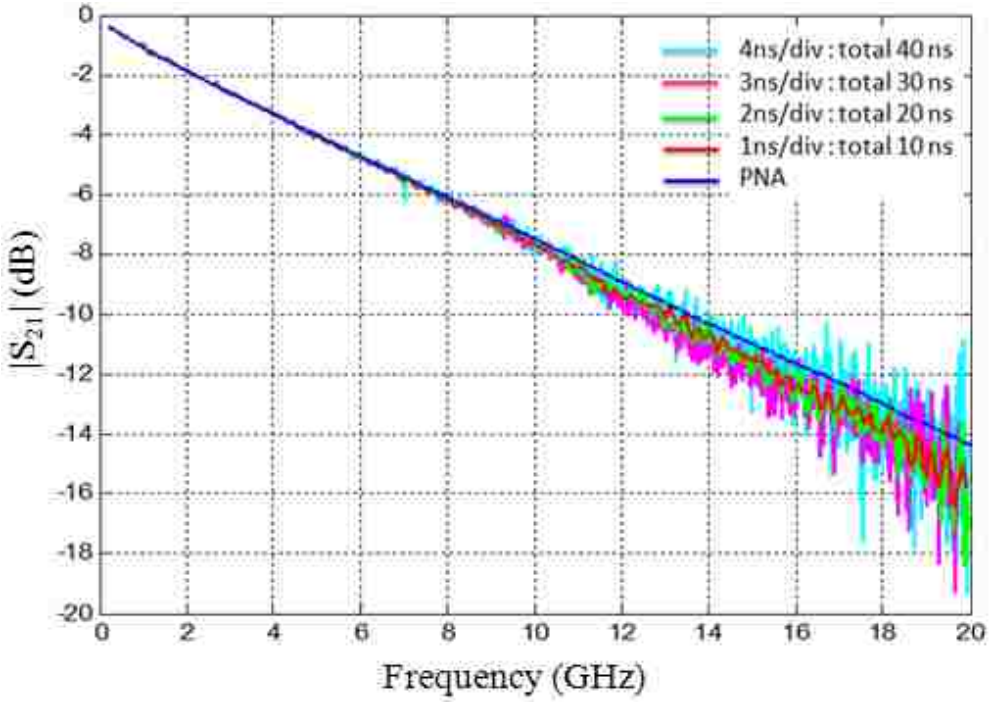

Figure 1.31: S_{21} magnitude comparison for different time record

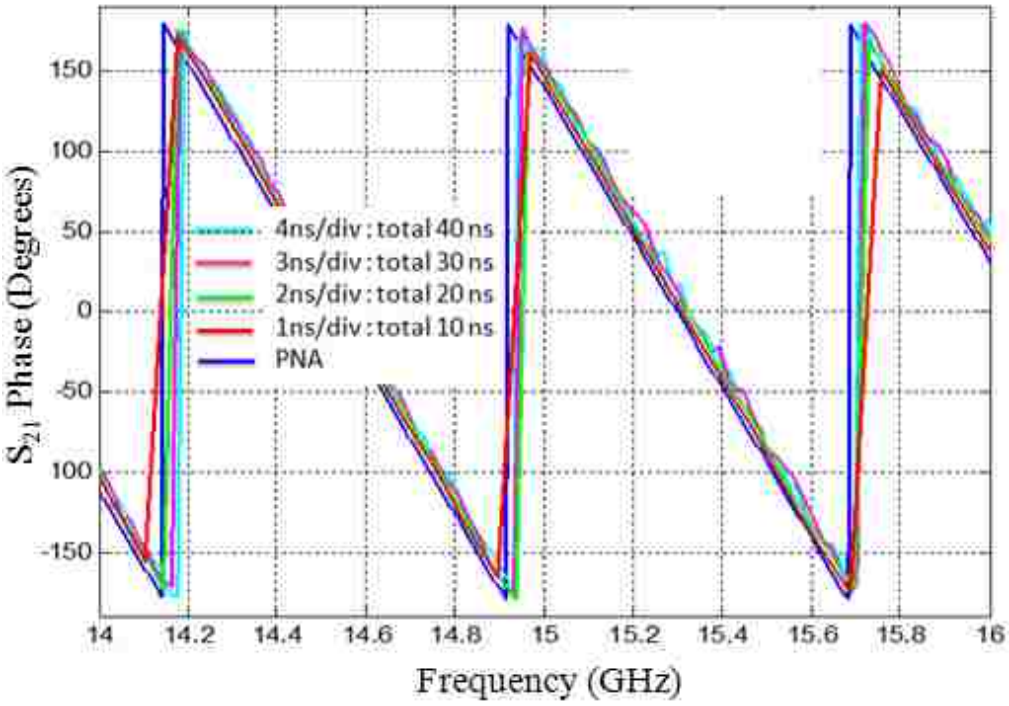

Figure 1.32: Phase of S_{21} comparison zoomed

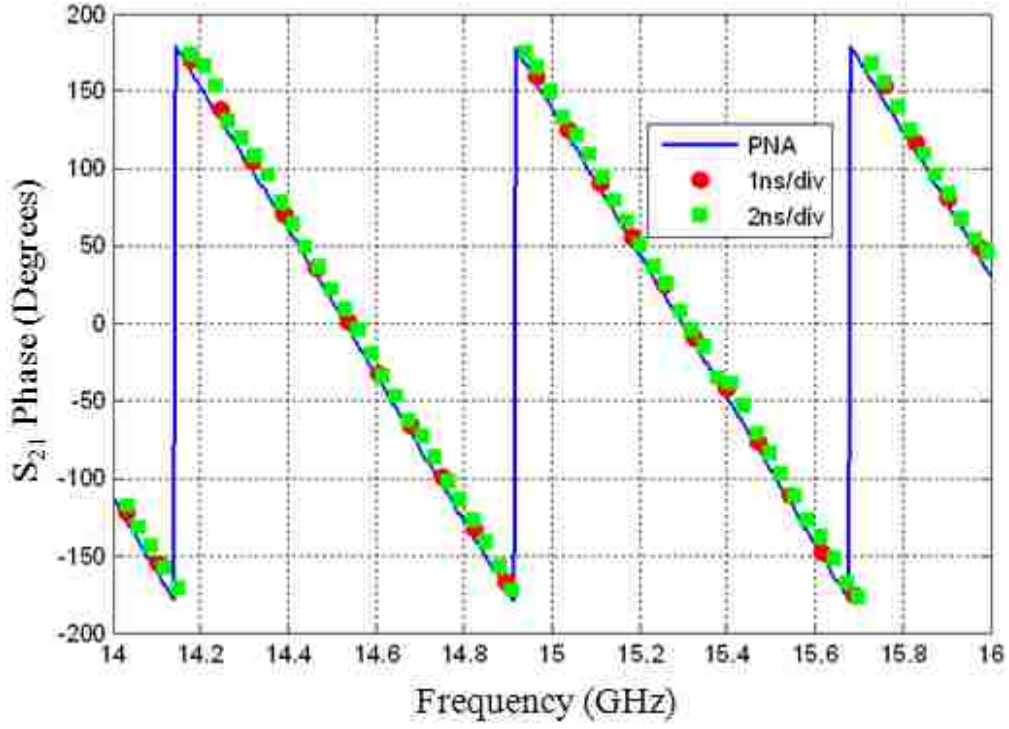

Figure 1.33: Increase in time record will increase the frequency resolution

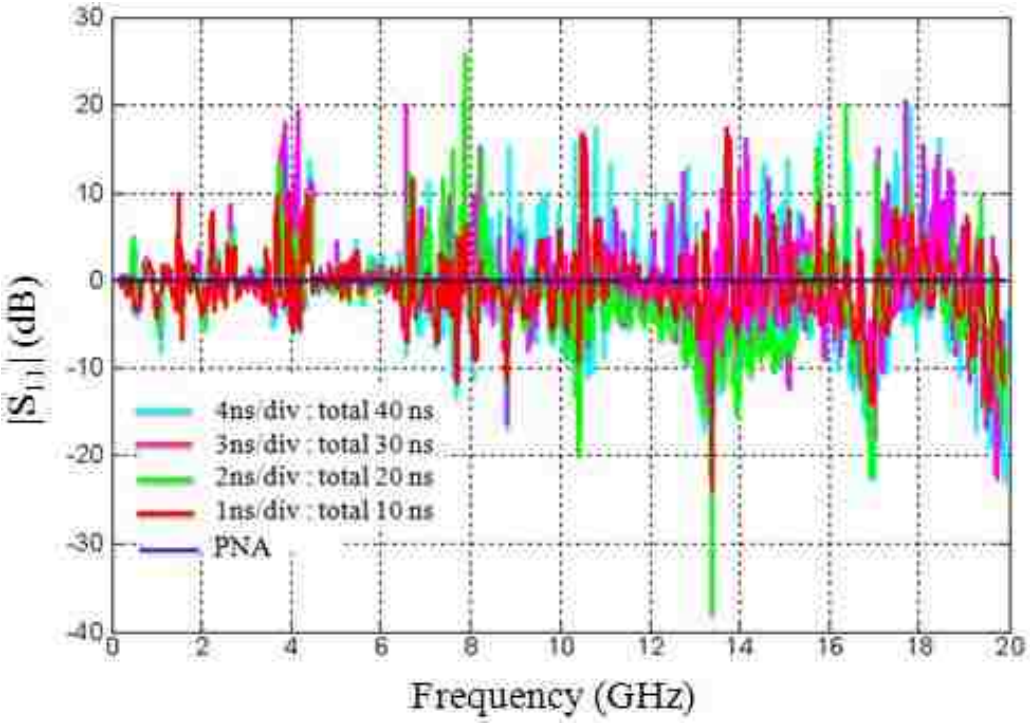

Figure 1.34: Difference in the S_{11} magnitude for different time record

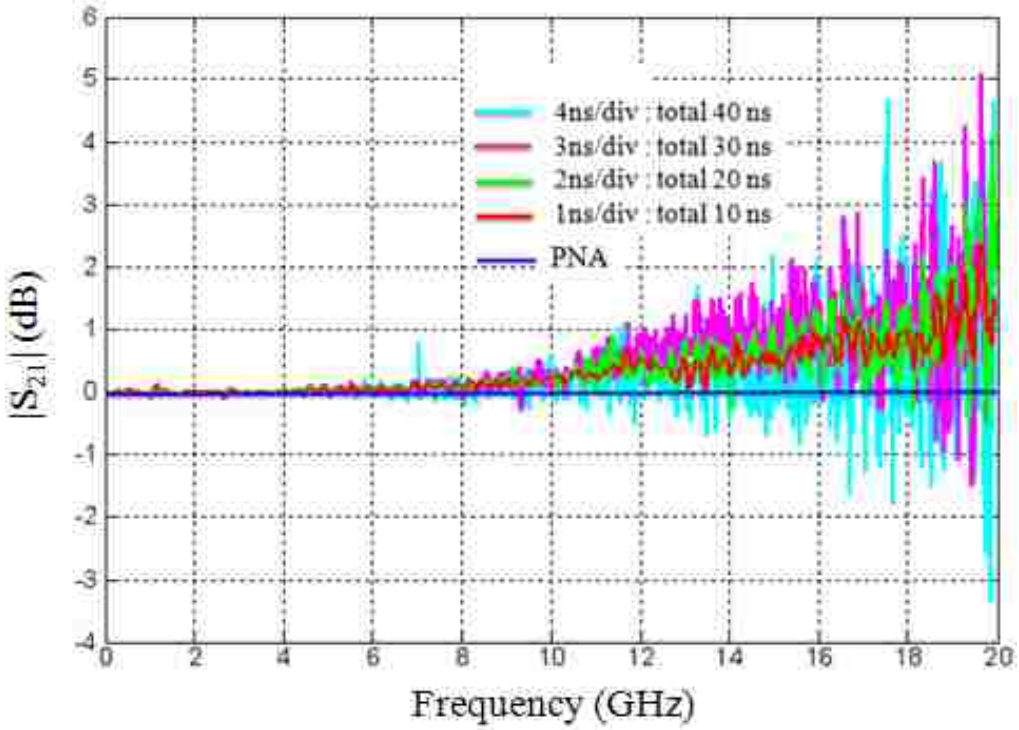

Figure 1.35: Difference in the S_{21} magnitude for different time record

From the formula (1), SNR is proportional to the number of points and inversely proportional to the square of the time record. The increase in time record reduces the SNR, but this can be solved by increasing the number of averages. Also by measuring a long time record it is ensured that the multiple reflections that occur at the ports and the connections are always captured. So another method can be considered to improve the measurement results. This method stitches many short waveforms together to create a long waveform. By stitching these waveforms, for each waveform section the SNR is preserved and the higher order reflections are captured. Generally as the time record increases the noise also increases which can be further reduces by taking larger number of averages.

The error assessment and study was now conducted on a new instrument, Tektronix DSA 8200 Digital Serial Analyzer. The measurement setup is similar to the previous setup done for the Agilent TDR. Tektronix has a rise time of 18ps. Here one end of the precision cables was connected to the sampling heads and the other end to the connectors on the boards as shown in Figure 1.36. One of the main advantages of the external E10 sampling heads is that they can be kept away from the instrument mainframe. The t-TRL calibration is performed with the new instrument and S_{11} magnitude and S_{21} magnitude and phase were plotted.

Figure 1.36: Measurement setup for the Tektronix DSA 8200

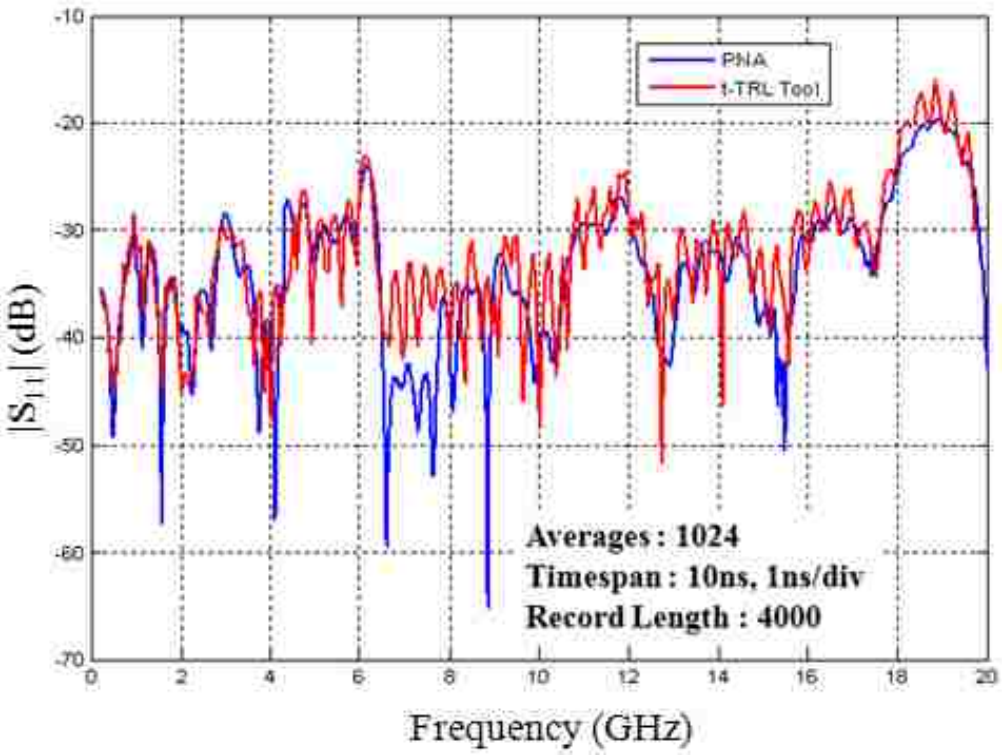

Figure 1.37: S_{11} magnitude comparison with VNA

The S_{11} magnitude as shown in figure 1.37 has a good correlation with the VNA measurement results at the low frequencies. But after about 6GHz, they graphs tend to fall apart. Random errors and systematic errors were analyzed to understand this effect. The magnitude and phase of S_{21} were plotted as shown in Figure 1.38 and Figure 1.39. The Tektronix DSA8200 analyzer is a relatively new instrument with higher bandwidth and faster rise time. Hence it is expected that the results are better than the Agilent DCA-J 86100C. It also has an option for setting the bandwidth to 20GHz or 30GHz or 50GHz. For all the measurements here, the maximum bandwidth of 50GHz was used. The results obtained from Tektronix are better than the ones from the Agilent. This can be due the facts that:

- The Tektronix signals reach steady state earlier due to the faster rise time.
- The Tektronix port connectors seem to be better.
- Faster rise time provides better spatial resolution

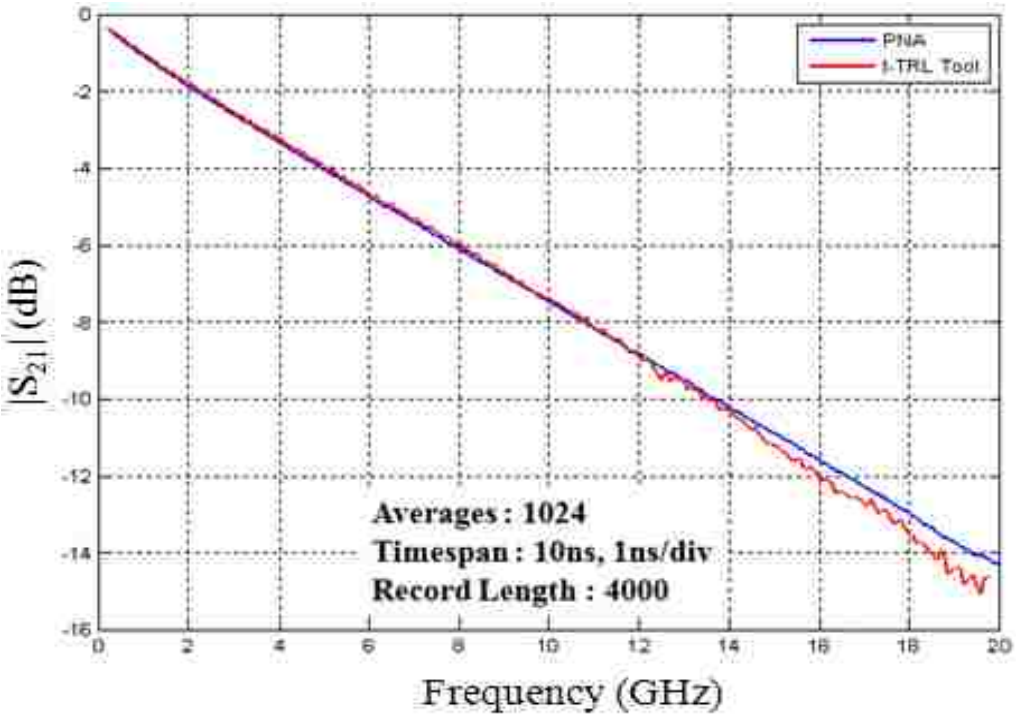

Figure 1.38: S_{21} magnitude comparison with VNA

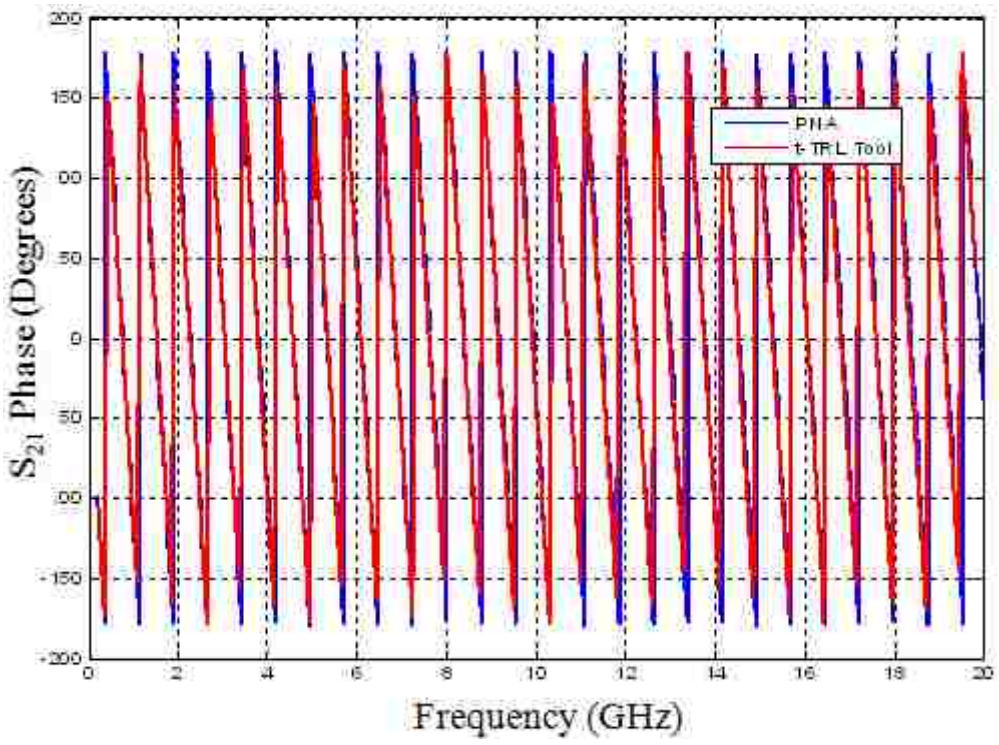

Figure 1.39: S_{21} phase comparison with VNA

The same process was repeated for a slightly different measurement setup. Here the E10 sampling heads were connected directly to the connectors on the measurement board as shown in Figure 1.40. No cables were used for this setup. Channel 1 was used as port 1 and channel 2 was used as port 2. Time record was fixed at 10ns and 512 averages was used. Also maximum (4000) number of points was used.

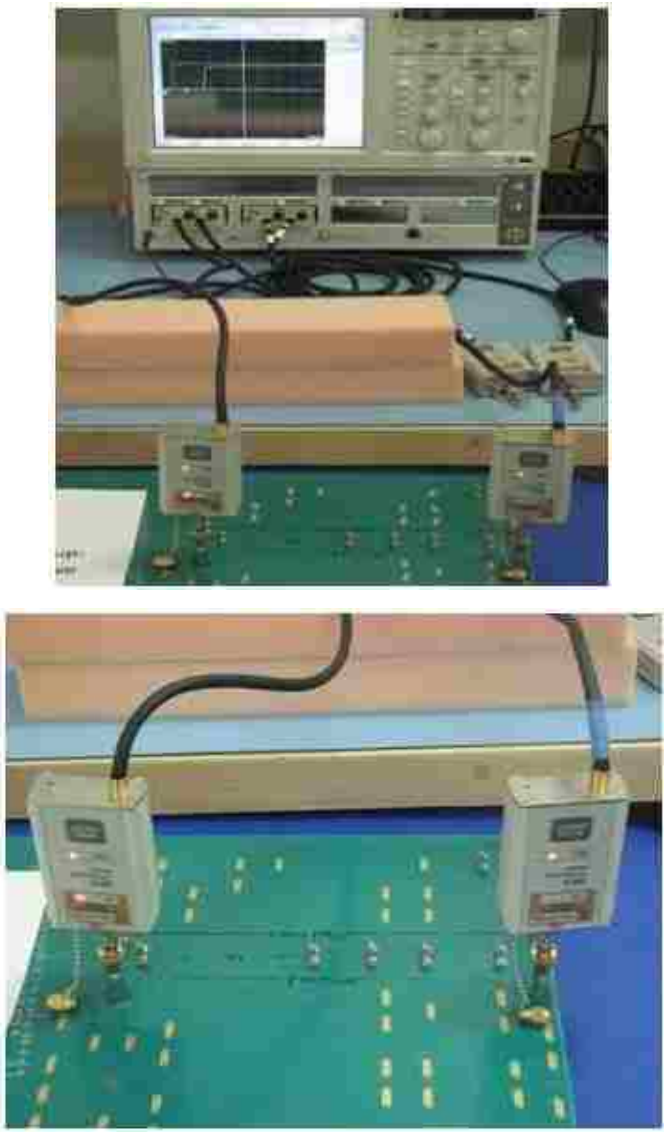

Figure 1.40: Measurement setup with sampling heads connected directly to the board

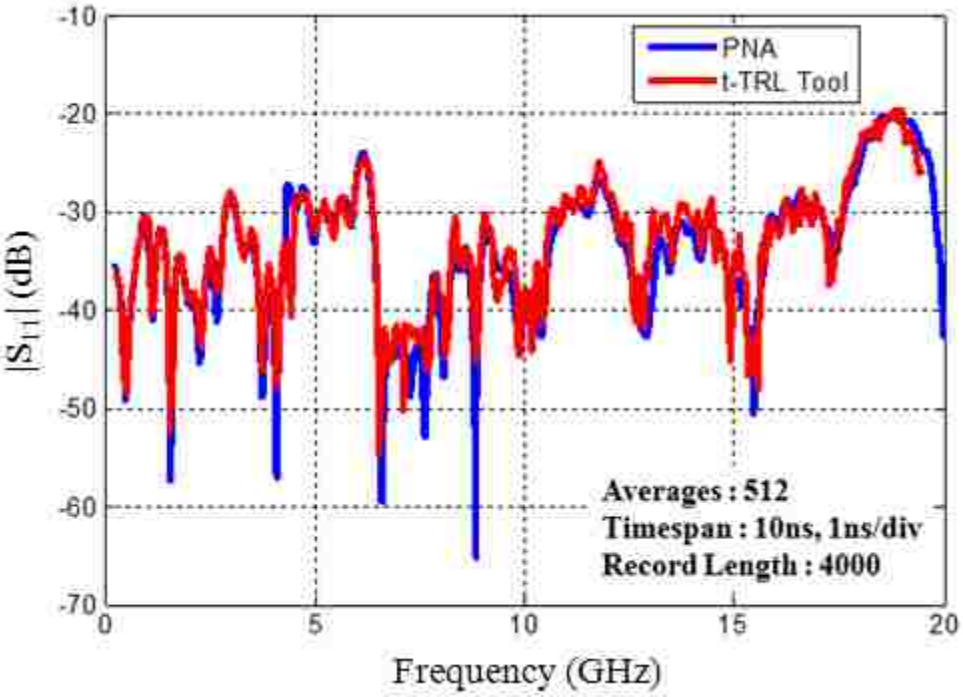

Figure 1.41: S_{11} magnitude comparison for measurements without cables.

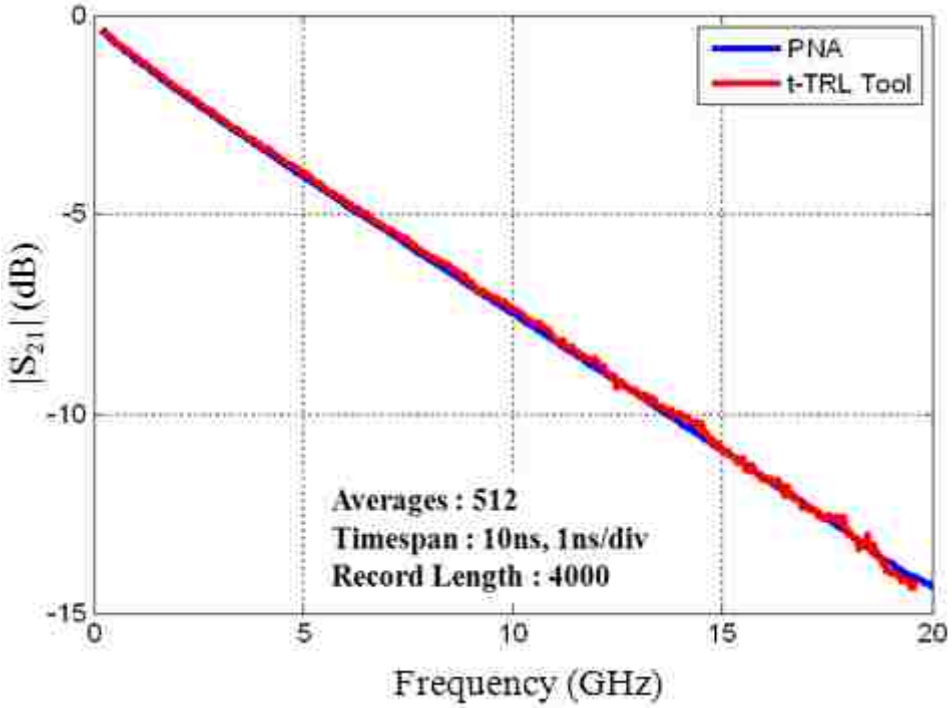

Figure 1.42: S_{21} magnitude comparison for measurements without cables

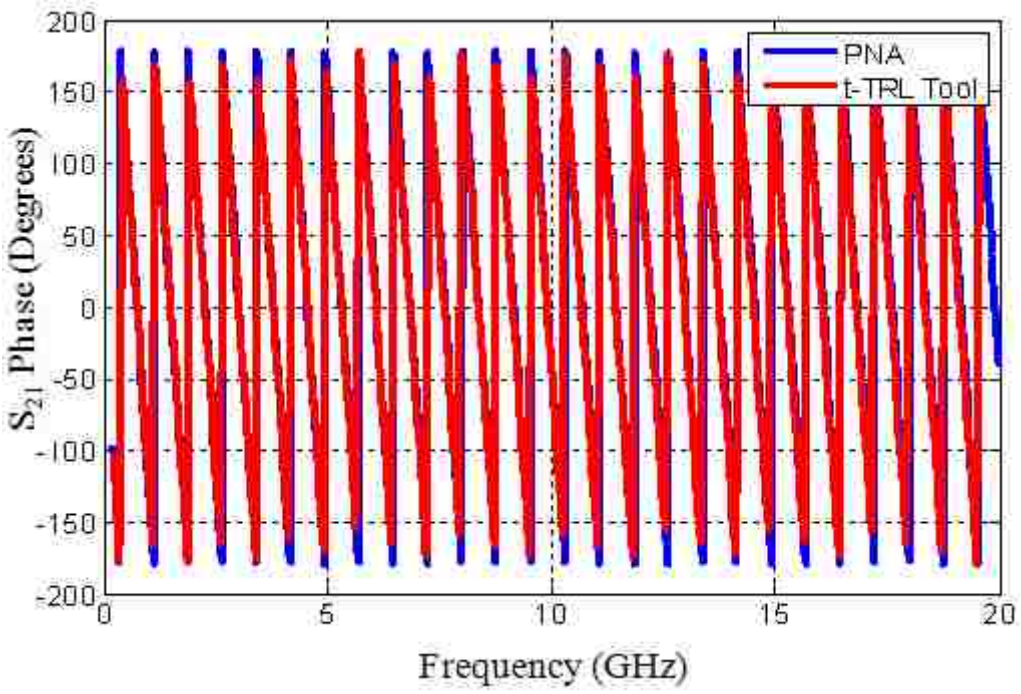

Figure 1.43: S_{21} phase comparison with VNA for measurement without cables

The t-TRL calibration results without the cables gave much better results when compared with the ones with the cables. The TRL technique by itself should have taken care of the influence of the cables. Interestingly, the calibration without cables always yielded better correlation with PNA calibration results. The t-TRL calibration effectively reduces reflections caused by the connector mismatches. The ripples in S_{21} and S_{11} are caused by extra reflections from the internal TDR load (most likely from the pulse generator of another channel).

Another concern while performing the time-domain TRL calibration was the repeatability of the calibration. It was observed that the t-TRL calibration was very sensitive to the way the measurement is done. Each measurement with respect to the connections and setups should be absolutely identical to get the same results again and again. The t-TRL calibration was done several times on the same DUT to check the repeatability of the measurement. S_{11} magnitude and S_{21} magnitude and phase were plotted.

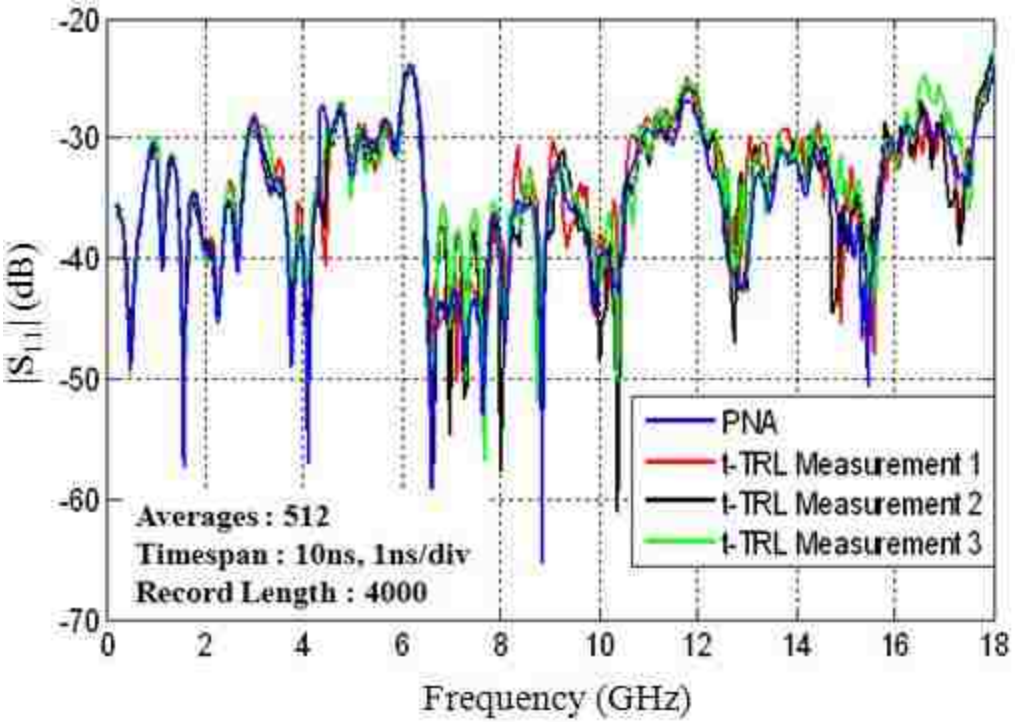

Figure 1.44: S_{11} magnitude comparison with VNA

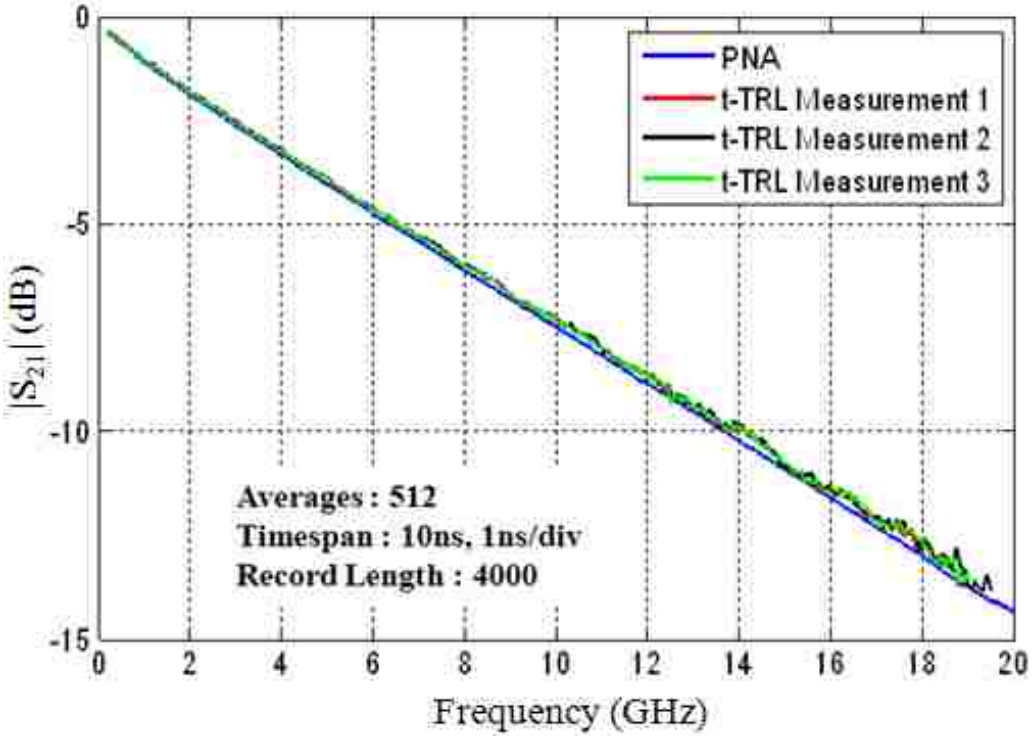

Figure 1.45: S_{21} magnitude comparison with VNA

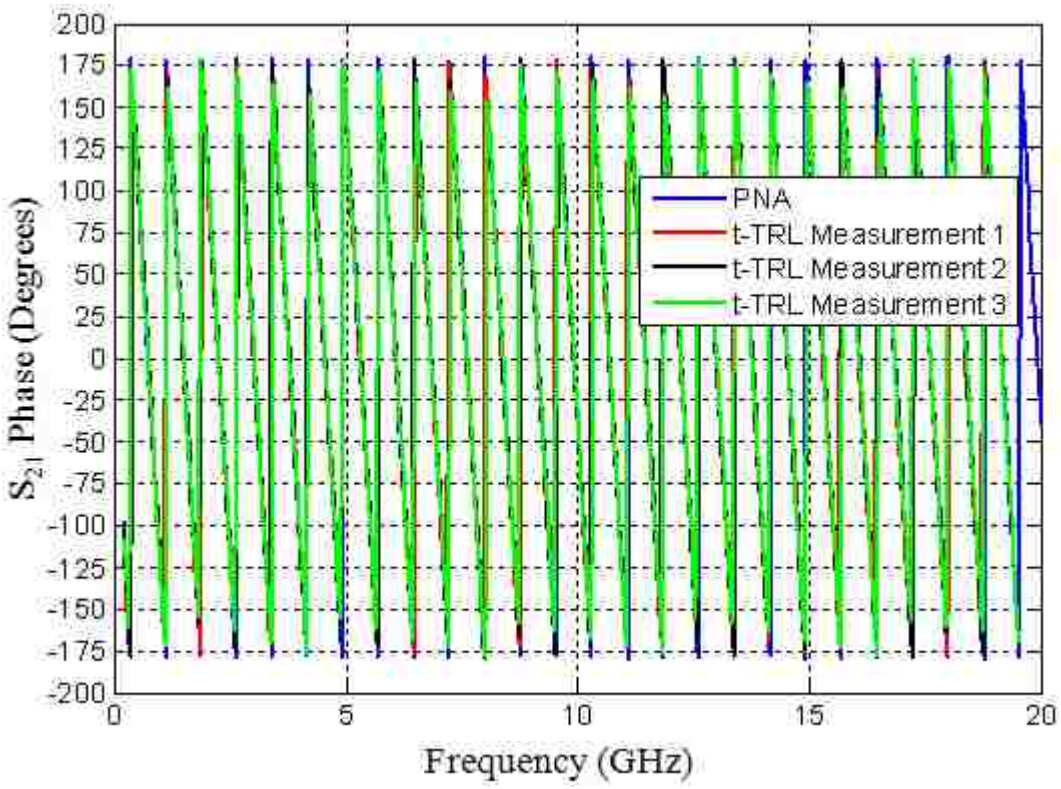

Figure 1.46: S_{21} phase comparison with VNA

1.2.2. Analyzing Systematic Errors. After analyzing the random errors, systematic errors are studied. The TRL calibration is based on an 8 term error model for two port systems. VNAs with two measurement ports are based on 24 term error models (12 terms for forward and 12 terms for reverse measurements). Taking only the terms that are important this 24 term error model reduces to a 12 term error model as shown in Figure 1.47.

The TRL calibration does not consider the leakage terms. It assumes that the error adapter X and error adaptor Y as shown in figure 1.11 are identical. That means the error adapters are the same for both forward and reverse measurements. One of the requirements for the TRL calibration is that the error terms should be the same for forward and reverse measurements. Unfortunately, this is not true for TDR instruments since their port impedances depend on the state of the port generator, i.e. whether the generator is turned on or switched off. In [8], this effect was described as a diode state error, and is illustrated herein in Figure 1.48[8].

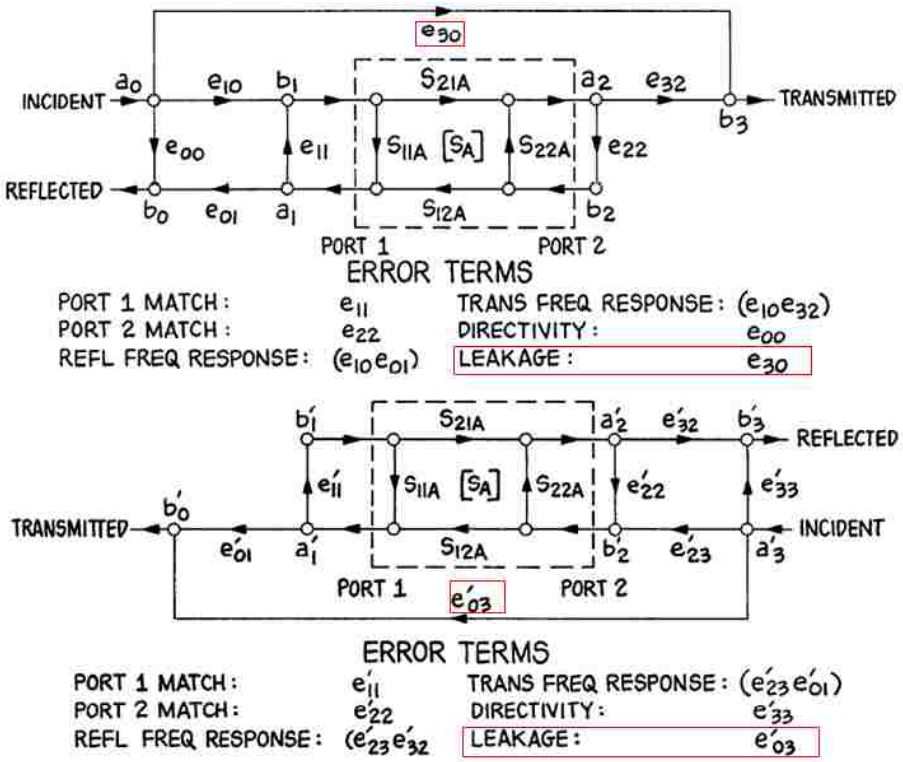

Figure 1.47: 12-term error model for forward and reverse measurements

A simple experiment was done to analyze the diode state error. The ports of the TDR 1 were connected with the 12-inch precision cable, and the TDR response of the port 2 was recorded for enabled and disabled generator of the port 2. The left zoomed part of Figure 1.48 shows the difference in TDR responses of the port 2 depending on the state of generator 2. Figure 1.49 shows the spectrum of the signal showing the diode state error.

The difference in reflections from port 2 means that it has different impedance depending on whether the port's generator is "on" or "off" which results in the asymmetry of the system (i.e. dependence of the result from the measurement direction). The diode state error creates a 10 term error model when the isolation terms are not considered. The asymmetry introduces additional term into calibration procedure error model which cannot be compensated by TRL according to [8]. The error can be reduced by windowing waveforms in such a manner that the reflection from the port is excluded, as is seen from figure 1.50[8]. By the windowing procedure, the port reflections are

eliminated after making sure that the response of the DUT is inside the time window selected. The windowing technique was applied to the TDR 1 instrument. It led to the improvement of the transmission coefficient magnitude measurements at 20 GHz, as is indicated in Figure 1.51. In this particular case, the error was reduced from 10% to 5%.

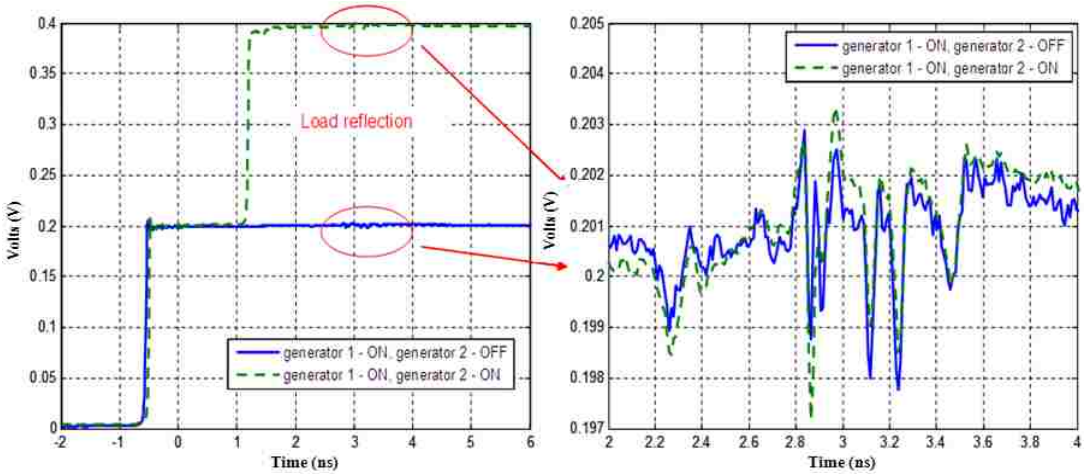

Figure 1.48: Measurement results showing the corresponding generator state

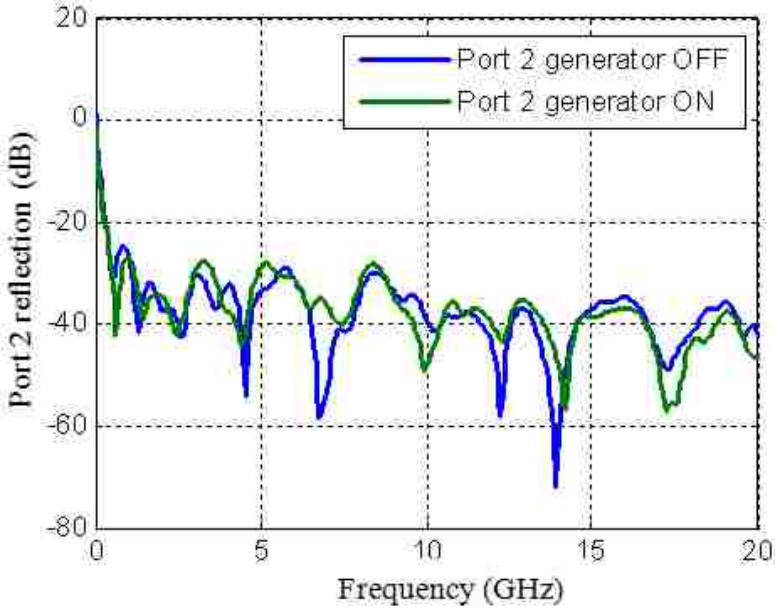

Figure 1.49: Spectrum of the signal showing diode state error

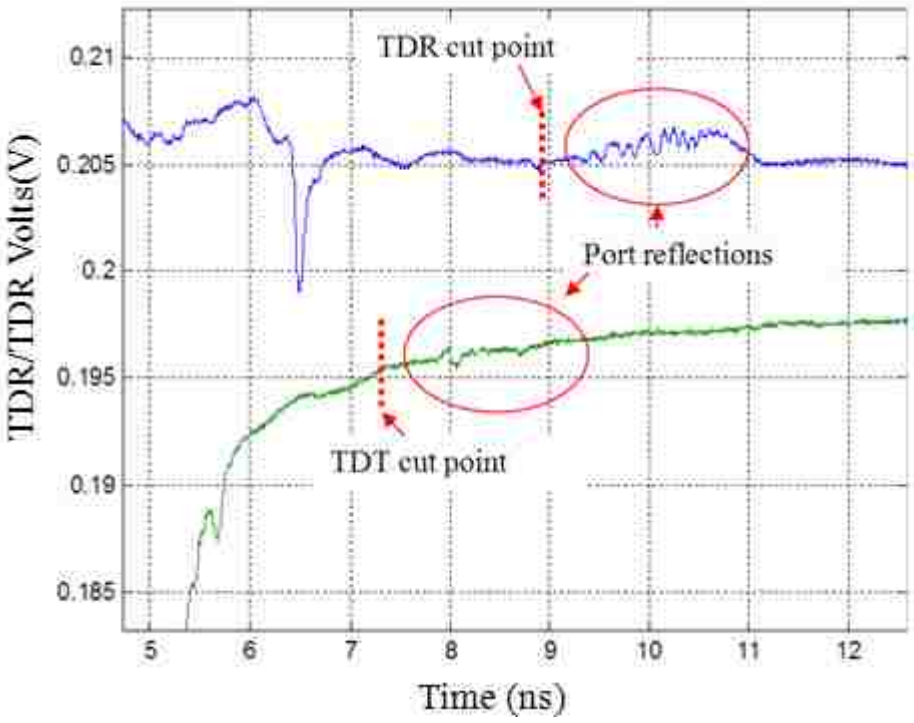

Figure 1.50: Windowing of the TDR/TDT waveforms to eliminate the effect of the diode state error

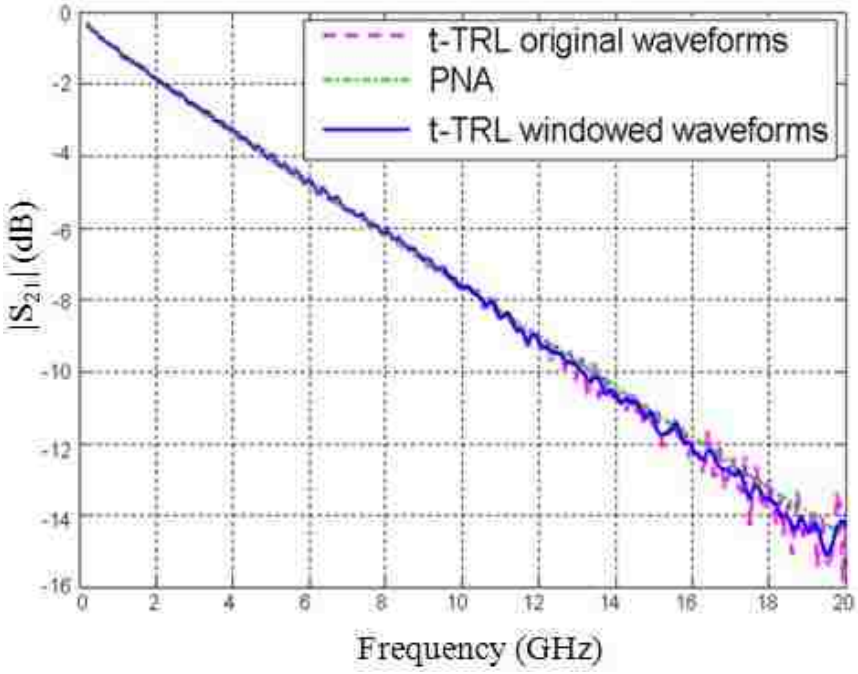

Figure 1.51: Improvement by applying waveform windowing

However, the windowing procedure does not allow for eliminating the overall error completely. This is because the reflection form the far-end port in the TDT measurement arrives at the same time at the incident edge of the TDR pulse and they cannot be separated. The circuit model below in the Figure 1.52 illustrates this effect. It contains of the model of the measurement cables, transmission line DUT, on board connectors (modeled by capacitors C1 and C2) and a reflective load.

The reflective load is modeled by a combination of capacitors, inductors and transmission lines. The simulated waveforms are shown in the Figure 1.53. It clearly shows the higher order reflections in both TDR and TDR waveforms. The reflection can be separated from the DUT response only in TDR waveform. In the TDT waveform the reflection and the incident edge overlap.

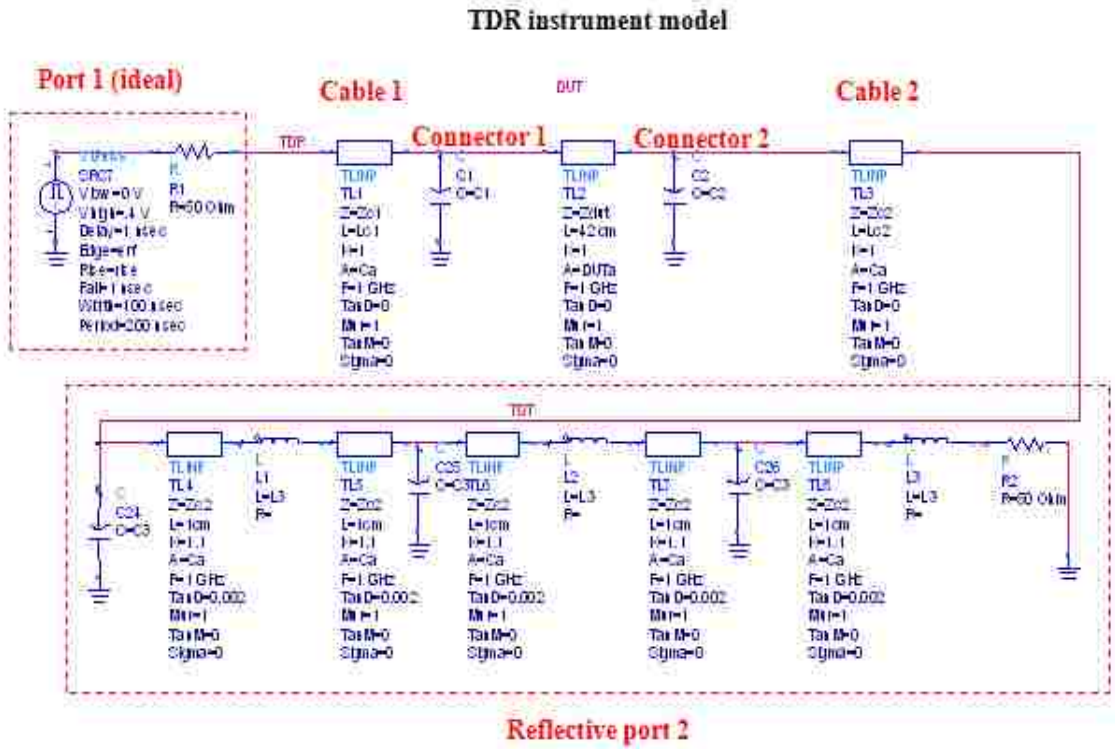

Figure 1.52: ADS model for TDR with reflective port

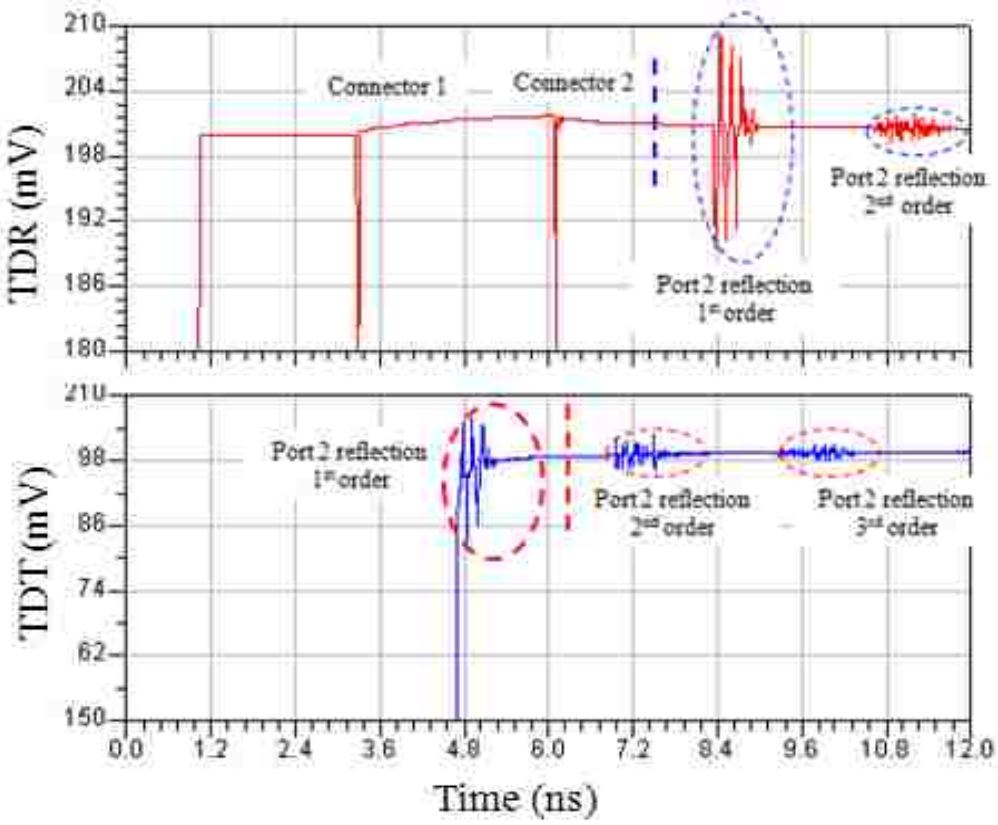

Figure 1.53: Simulation results showing higher order reflections

The VNAs with two measurement ports and one source have switching error. This can be very similar to the state error associated with the TDR samplers in the ON and OFF positions. The samplers have diodes which has different impedances in different states. The switching errors can be considered if separate models for forward and reverse measurements are used. This helps to measure the entire incident and reflected signals at the ports. A majority of the modern frequency-domain VNAs are four-sampler instruments, capable of measuring incident and reflected waves on both ports simultaneously. A switch changes direction of the incident power to the unknown 2 port for forward and reverse direction measurements and at the same time terminates the unknown 2 port in impedance Z_0. In such instruments, the switching error can be compensated in the course of the normal calibration and measurement procedure without the use of any additional calibration standards.

In the frequency-domain VNAs there are two ways of eliminating the switching error. If the VNA has 4 samplers/mixers, then the switching error can be mathematically removed without any additional measurements. Figure 1.54 shows how the S-parameters can be measured from the incident and reflected signals. If the VNA has only 3 receivers, the switching error is removed by applying the SOLT calibration prior to the TRL calibration. This is called the two-tier calibration procedure [12] as shown in figure 1.55. The same approach can be applied to the time-domain VNAs too.

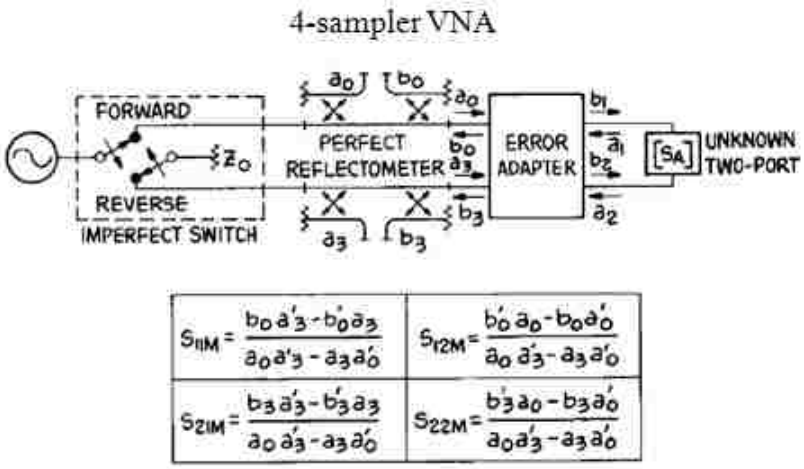

Figure 1.54: 4 sampler VNA and the measurement of S-parameters

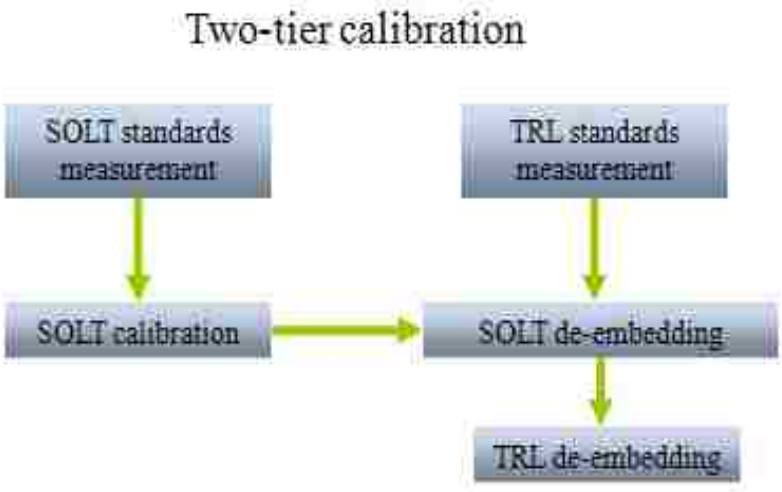

Figure 1.55: Two tier calibration for 3 sampler VNA

1.3. TWO TIER CALIBRATIONS

In two tier calibrations [12], SOLT calibration is performed as the 1st tier calibration. The SOLT calibration takes into account of the switching error. Time-domain waveforms are measured and SOLT calibration is performed on these waveforms. The SOLT calibrated data is given to the TRL technique to yield two-tier calibrated results. A block diagram below shows the methodology that is used. To make sure that this method works, first the 1st tier SOLT calibration is done in the frequency-domain. This is sanity check before doing the experiment in the time-domain. 1st tier calibration can be a manual SOLT calibration or an Electronic calibration done in the VNA. Figure 1.56 shows the block diagram representation of two tier calibration.

These frequency-domain results are then compared to the time-domain SOLT calibration results. The measurements for both forward and reverse directions are taken. The correlation between time-domain SOLT calibration and frequency-domain VNA calibration are shown in Figure 1.57 and Figure 1.58.

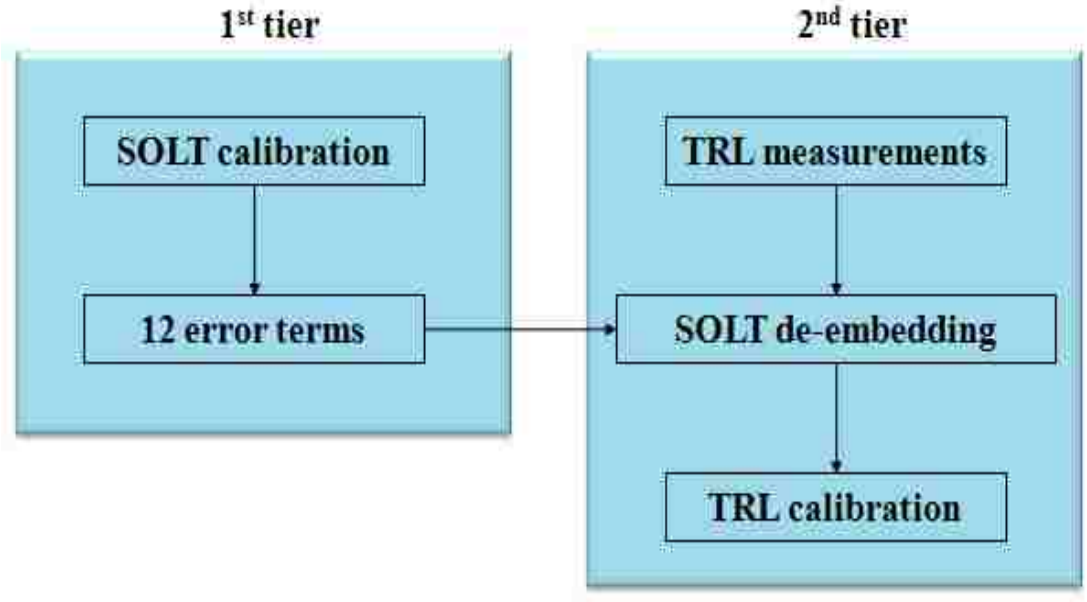

Figure 1.56: Two tier calibration block diagram

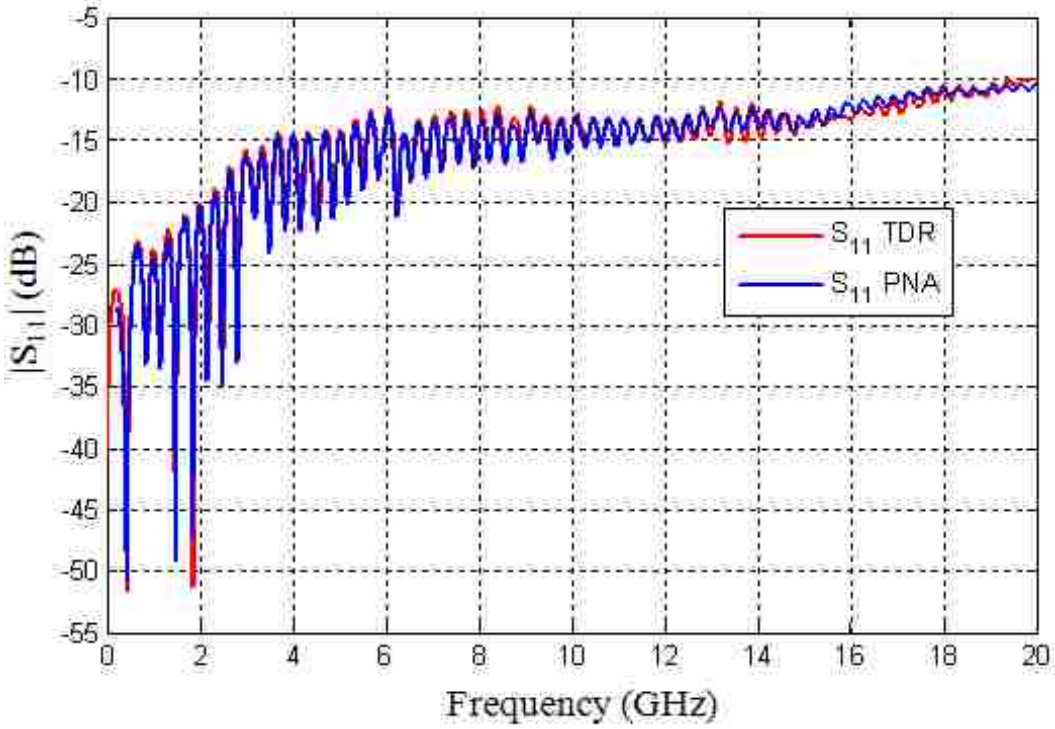

Figure 1.57: SOLT calibration comparison of S_{11} magnitude with the VNA

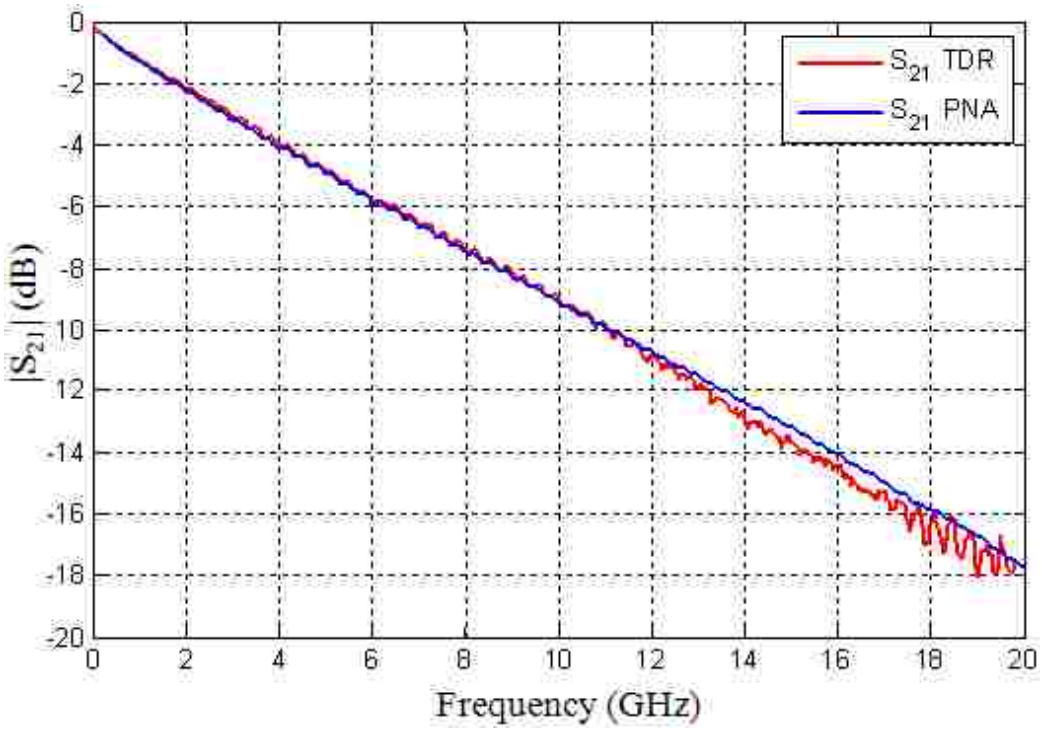

Figure 1.58: SOLT calibration comparison of S_{21} magnitude with the VNA

The forward measurements are S_{21} data and the reverse measurements are S_{12} data. The VNA S-parameters for forward and reverse measurements are identical. Hence time-domain results are compared to just the forward VNA measurements. Similarly the TRL technique is applied to the SOLT calibrated data from the frequency-domain. All the standards used in the TRL calibration is measured and calibrated using the Agilent VNA. For the particular measurement board three line standards were used. The block diagram of the two tier calibration performed on the frequency-domain data is shown below in the Figure 1.59. The Figure 1.60 and Figure 1.61 show the results of two tier calibrations on frequency-domain data.

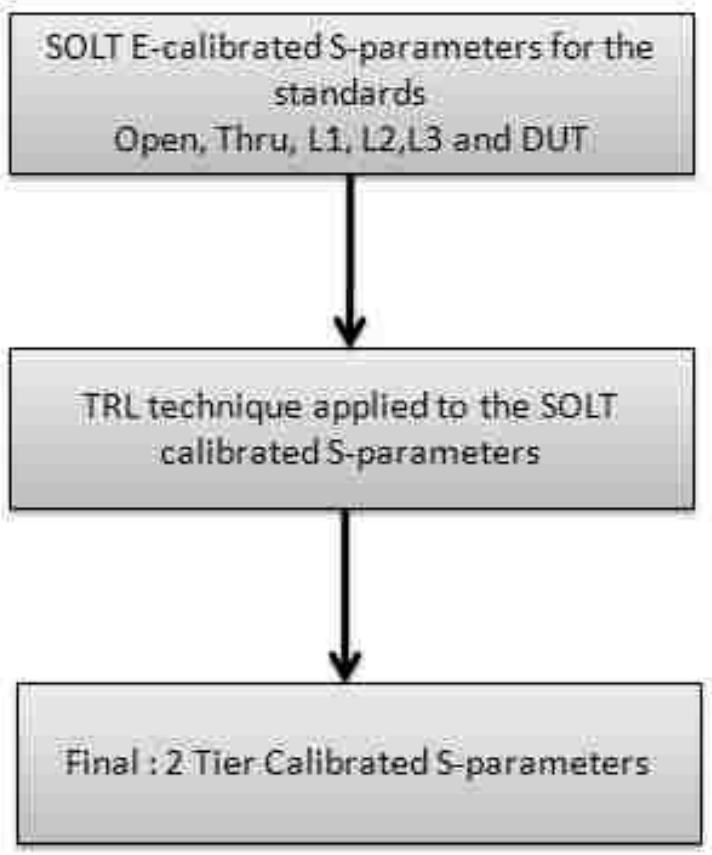

Figure 1.59: Two tier calibration with 1st tier calibrated by E-calibration

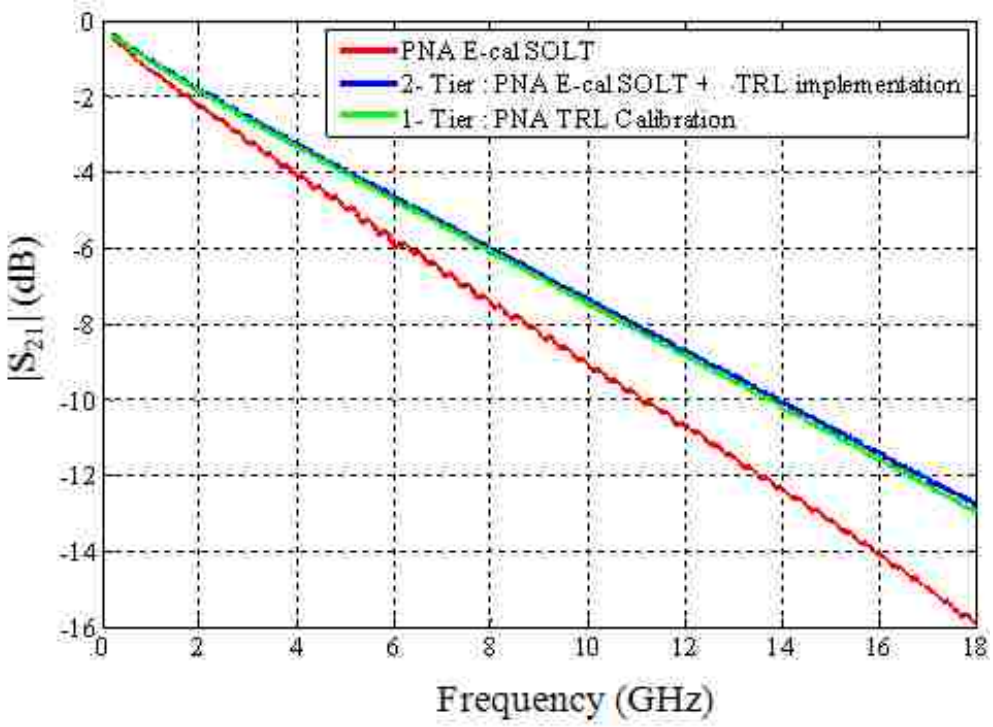

Figure 1.60: Two tier calibration on frequency-domain data, S_{21} magnitude

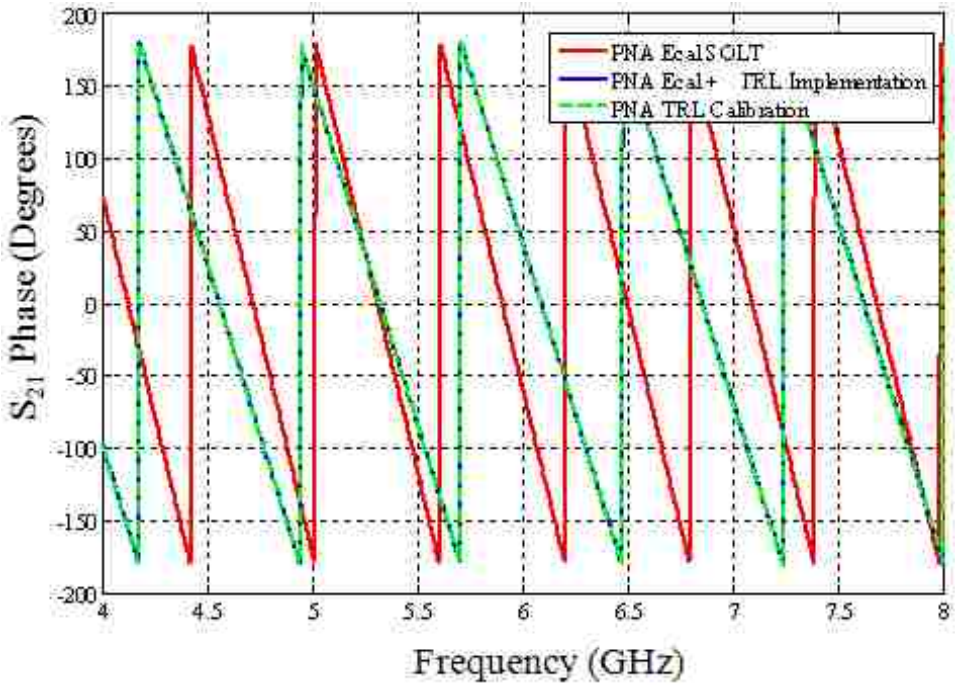

Figure 1.61: Two tier calibration on frequency-domain data, S_{21} phase

The graphs shows that when the E-calibrated data is given to the TRL technique it gives calibrated results similar to that of the frequency-domain TRL VNA calibrated results. This validates that the two tier calibrations on frequency-domain data works well. This method is now applied to the time-domain waveforms. SOLT calibrated data from the time-domain measurements were fed to the TRL calibration technique and the magnitude of the S_{21} and S_{11} are plotted as shown in Figure 1.62 and Figure 1.63. The correlation with the reference VNA data is not good as seen from the figures below. The two tier calibration measurements in time-domain were unsuccessful. Even though the 1st tier calibration (SOLT) results were comparable to the frequency-domain results, when the 2nd tier calibration was applied to the SOLT calibrated S-parameters yielded unsatisfactory results. By theory [12] it is possible to eliminate the switching error by the proposed two tier calibration. One possible reason for the uncorrelated results is that the errors in the 1st tier calibration may be exaggerated when the 2nd tier calibration is performed.

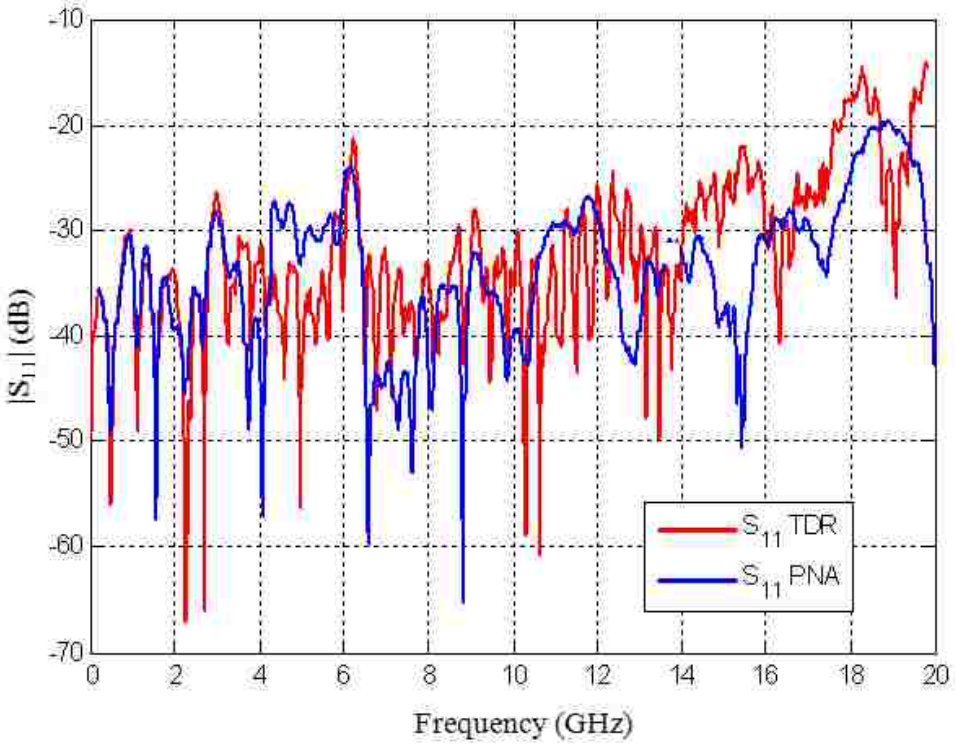

Figure 1.62: Two tier calibration on time-domain data, S_{11} magnitude

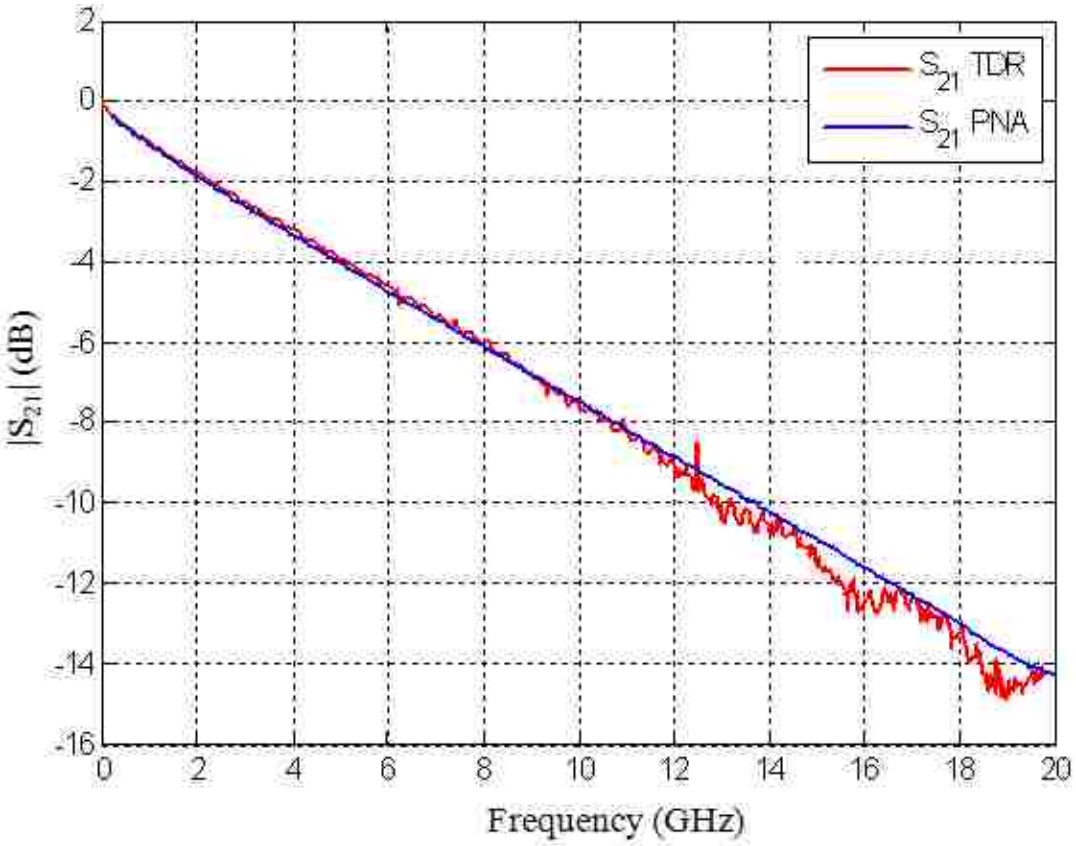

Figure 1.63: Two tier calibration on time-domain data, S_{21} magnitude

1.4. t-TRL CALIBRATION WITH SPLITTERS

Another method to eliminate the switching error in time-domain VNA is by the use of splitters in time-domain measurements. The switching error can be simulated using a circuit model for the time-domain VNA. The figure below shows the time-domain model for the TRL calibration in the forward direction (excitation at port 1). The same model is there for the reverse direction too. They are shown in Figure 1.64 and Figure 1.65. The excitation is modeled as a RC circuit. The capacitance of the port models the reflection. The capacitance is given slightly different values for the forward and reverse direction simulations. Simple transmission line models are used for the cables. The connectors on the boards were also modeled as capacitors. The Figure 1.66 shows the correlation of the circuit model with the actual TDR measurement.

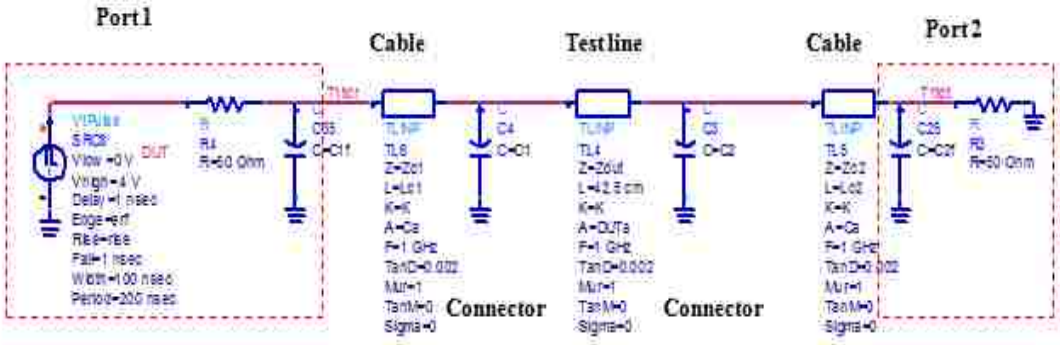

Figure 1.64: ADS model for TDR forward measurement

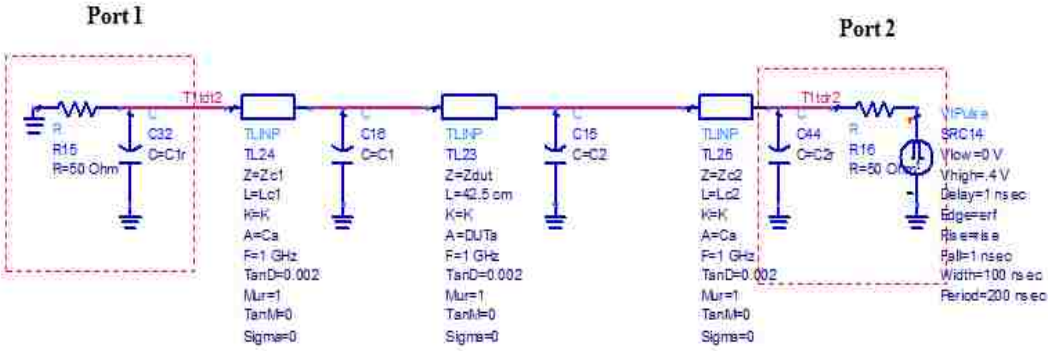

Figure 1.65: ADS model for TDR reverse measurement

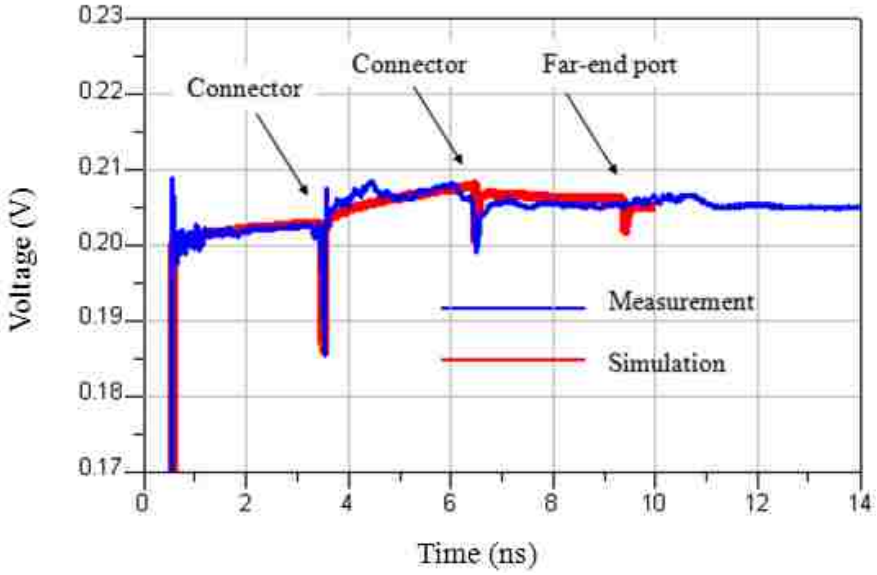

Figure 1.66: TDR pulse comparison

This circuit model is used for the TRL calibration. For the forward measurement the capacitance at the port 1 is given a value of 0.1pF and for the reverse measurement this capacitance is given a value of 0.11 pF. This small difference in capacitance can emulate the switching error. Similarly, the same change in capacitor values were made to the port 2 too. Here the values were 0.12 pF and 0.1 pF respectively. Figure 1.67 below shows the simulation results.

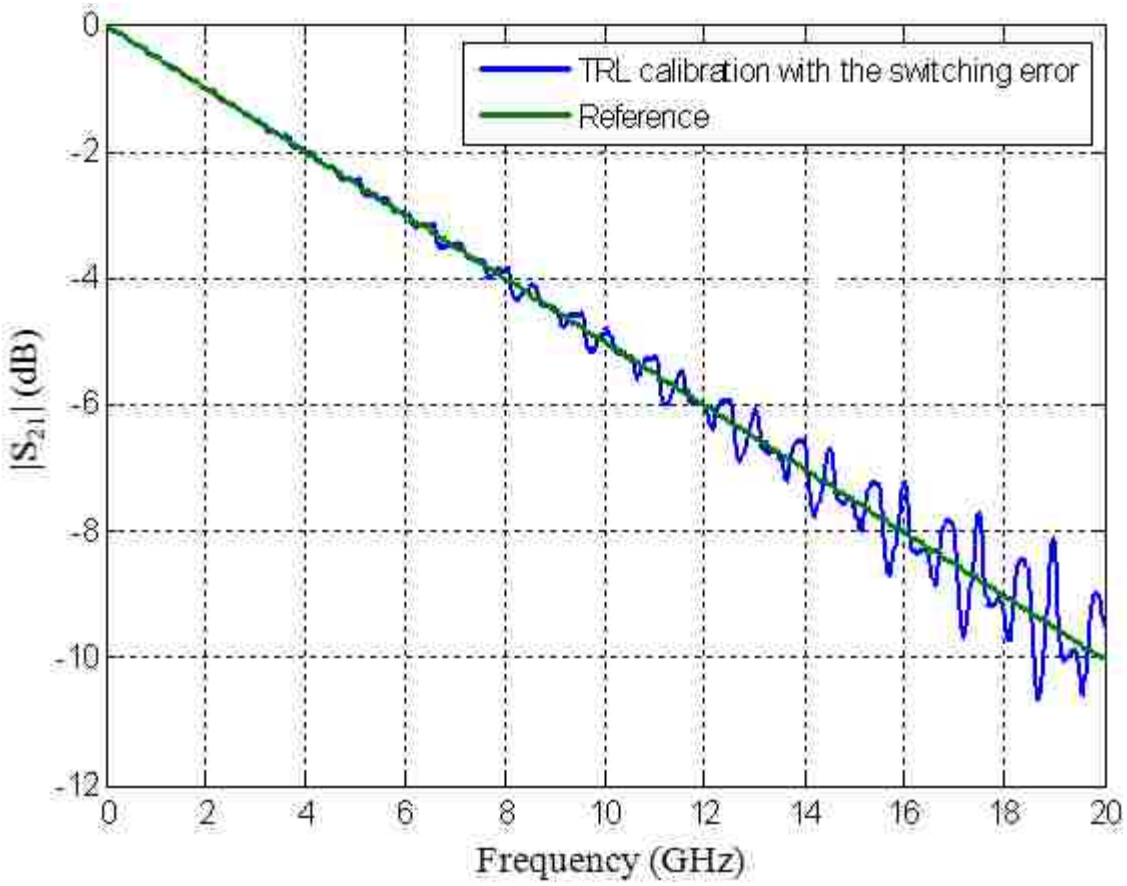

Figure 1.67: Switching error simulation using the ADS model

The reference is the frequency-domain VNA results. The Figure 1.67 above shows that the switching error can be visualized by a circuit model. To minimize the switching error a new method was tried. Power dividers were used to reduce the reflected wave. Here by using power dividers, the reflected wave and the transmitted wave are

measured separately. The reflections from the ports are attenuated more than the reflections from the DUT. Power dividers from mini-circuits are used for this experiment. The isolation between the inputs is about 20 dB till 10GHz and about 16dB at 20GHz. The transmission is about 10dB at 20GHz. The S-parameters of the splitters are shown in Figure 1.68. Port 1 and 2 are the inputs and port 3 is the output of the splitters.

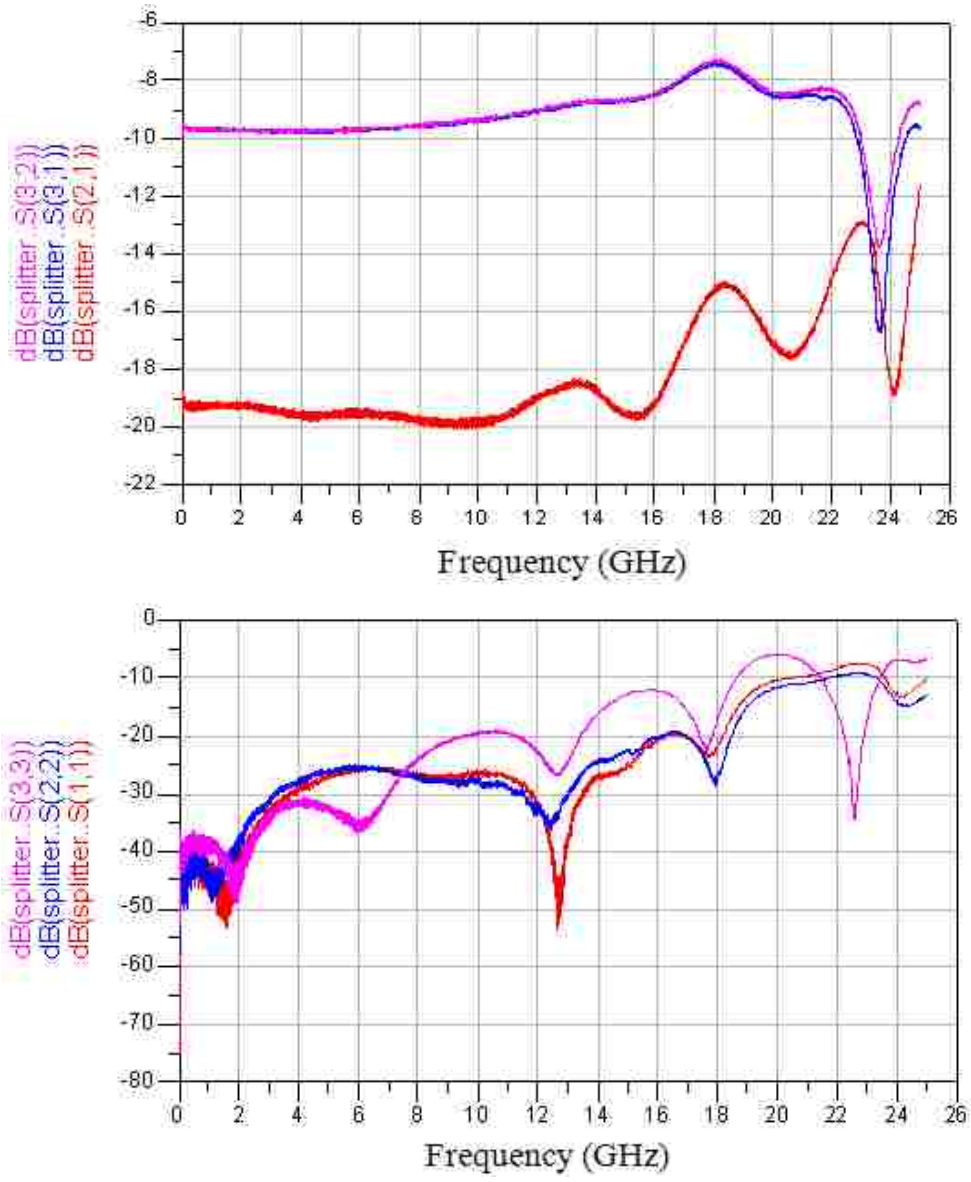

Figure 1.68: S-parameters of the splitters showing isolation, transmission and reflection

The circuit model for the splitter simulation is shown in Figure 1.69. The excitation at TDR Port 1. The excitation can be given by Agilent DCA-J or Tektronix DSA 8200. In this case the other module is used in the oscilloscope mode to measure the TDR/TDT waveforms. The simulated results are shown below in Figure 1.70. The graph clearly shows with increased isolation, the undulations are greatly reduced. It was decided that 20 dB isolation is enough to get good results.

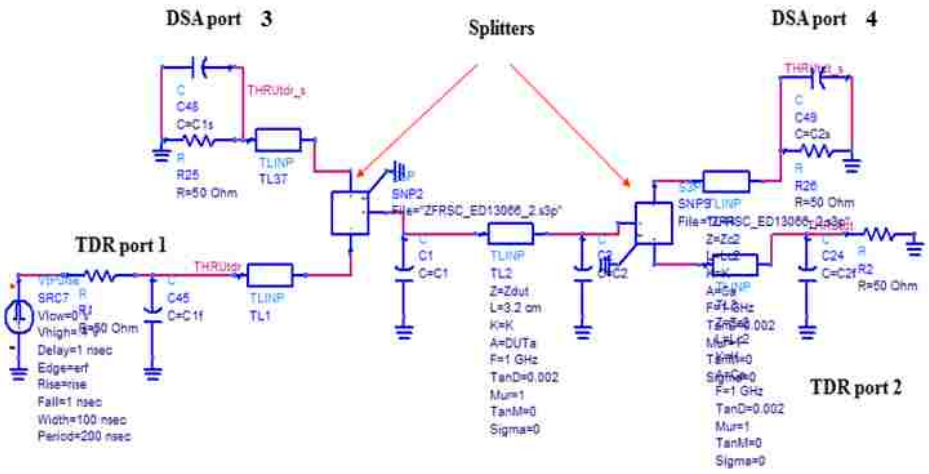

Figure 1.69: ADS model for the TDR measurement setup with splitters

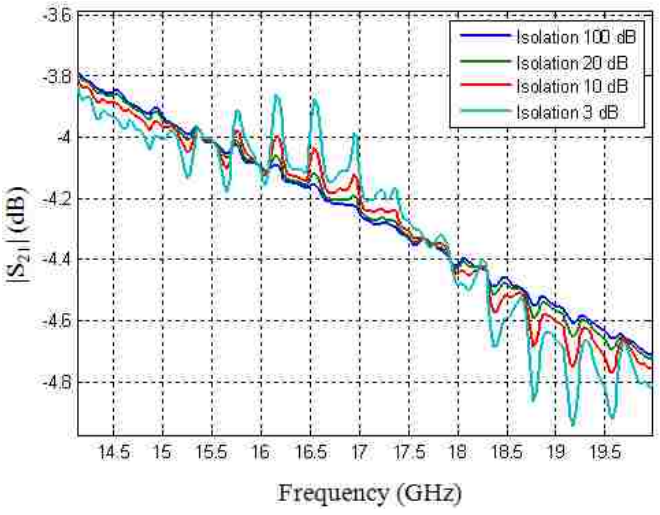

Figure 1.70: Simulated results showing fewer undulations with more isolation

Different configuration were tried to do this experiment. These configurations are shown in the figures below. Setup 1 of the measurement uses Agilent as TDR and Tektronix as scope and is shown in the Figure 1.71 and Figure 1.72. In this setup, DSA 8200 is the TDR and the Agilent DCA-J is in the scope mode. The two instruments must be synchronized to be able to measure the signals properly. Trigger output from the DSA 8200 is given as trigger input to the Agilent scope. The trigger level too was adjusted to enable the measurement. The time-domain waveforms were measured for each port excitation for the entire TRL calibration pattern.

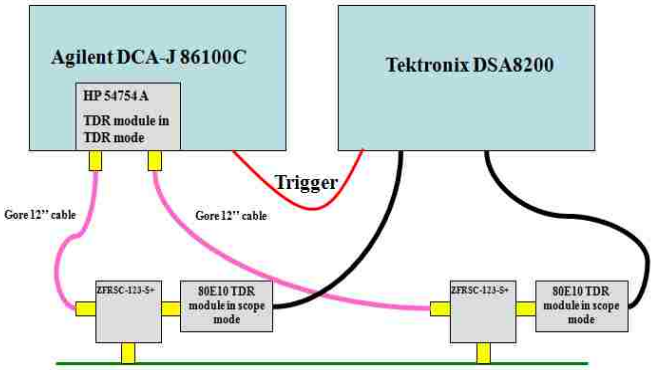

Figure 1.71: Block diagram for measurement setup 1

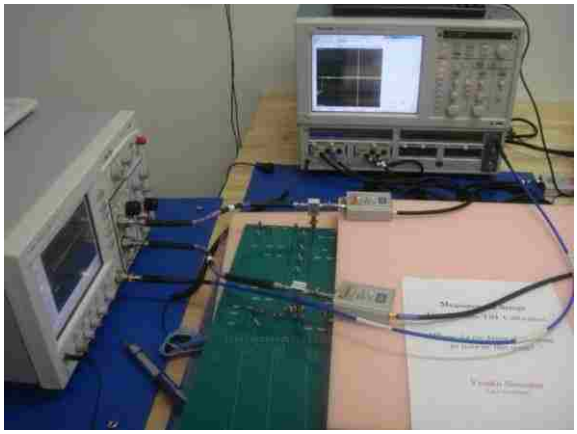

Figure 1.72: Measurement setup 1

After measuring all the time-domain waveforms, the TRL calibration is applied to the measured waveforms at the scope. The results are shown in Figure 1.73. S_{11} and S_{21} magnitude and S_{21} phase are plotted. The results are not good when compared to the reference VNA results. The reason for this error is the sampling pulse from the generator.

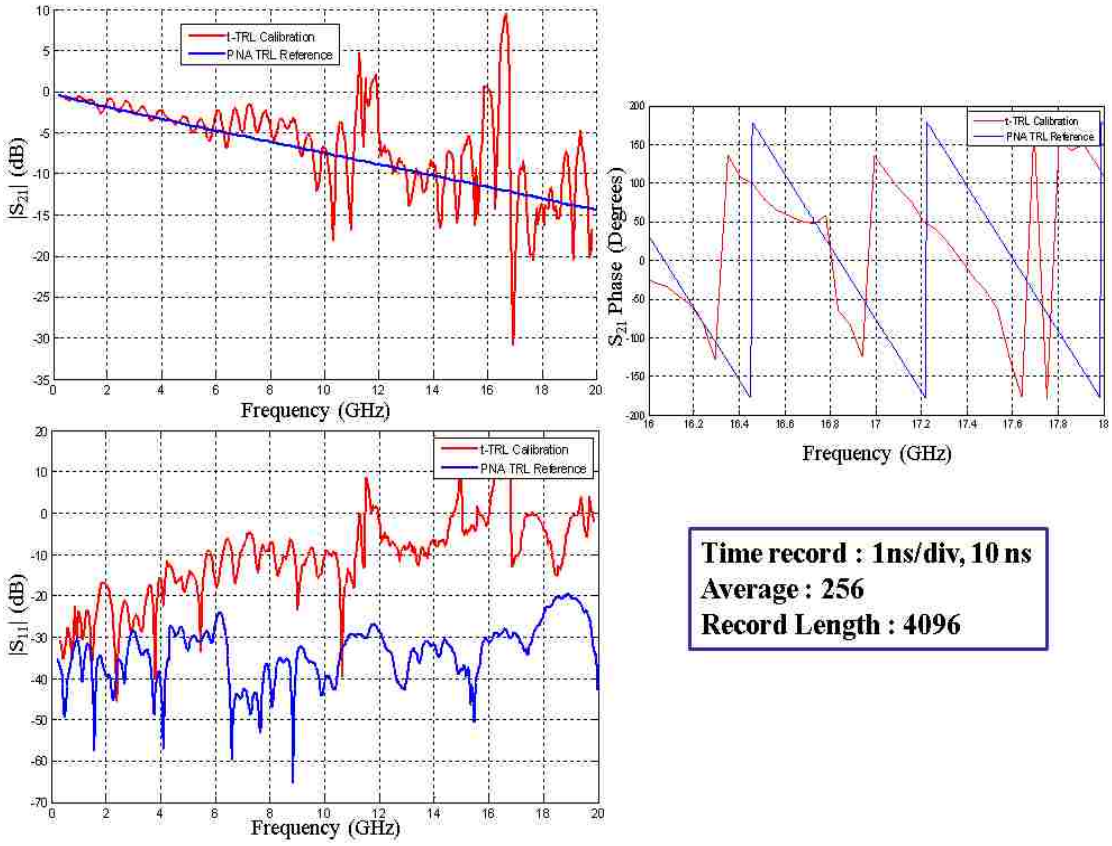

Figure 1.73: Results from the measurement setup 1

The measured TDR and TDT waveforms are shown in Figure 1.74. The TDT waveform clearly shows the parasitic sampler pulse. This pulse arrives at the same time as the incident pulse. It is believed that this parasitic signal may be the reason for the calibration error. To avoid the effect of this unwanted signal due to external trigger, only DSA 8200 is used for the experiment.

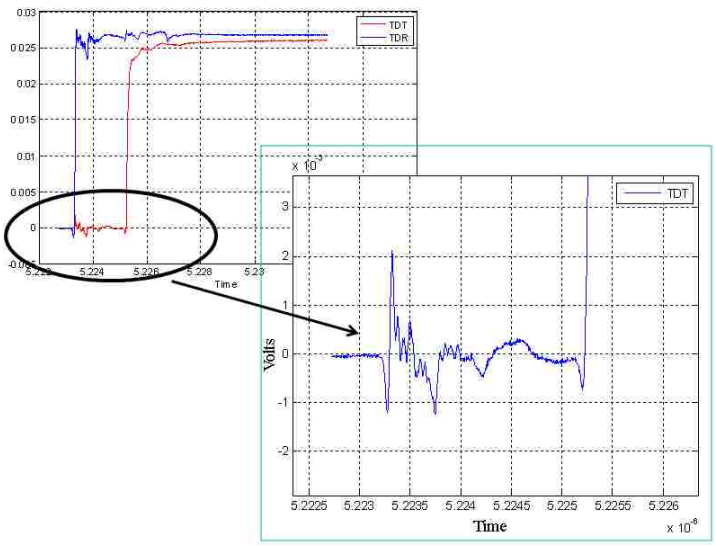

Figure 1.74: Sampler pulse causing parasitic waveforms

The setup 2 of the experiment used Tektronix DSA 8200 as both TDR and scope as shown in Figure 1.75. Two channels of the analyzer were used as the TDR generator and the other two channels were used as the receivers. Here twelve inch cables were attached between the generator heads and the splitters as shown in Figure 1.76. The input to the splitters is connected to the sampler heads acting as the scope. Similar time-domain measurements were made using this setup.

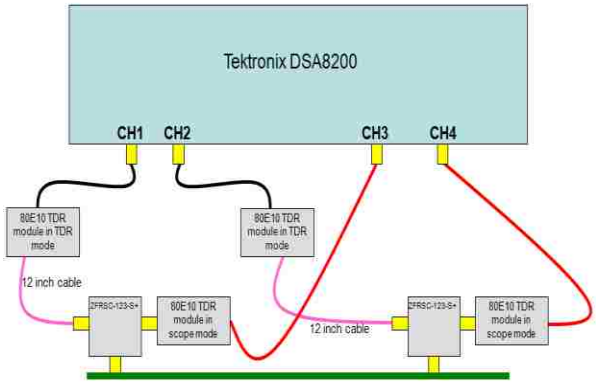

Figure 1.75: Block diagram for measurement setup 2

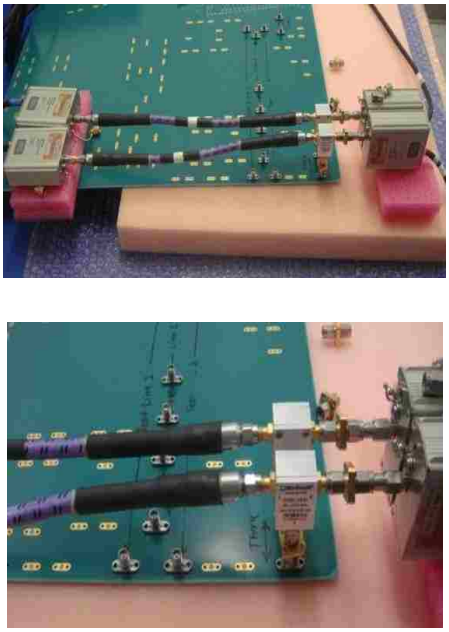

Figure 1.76: Using short cables to connect TDR generators to splitters

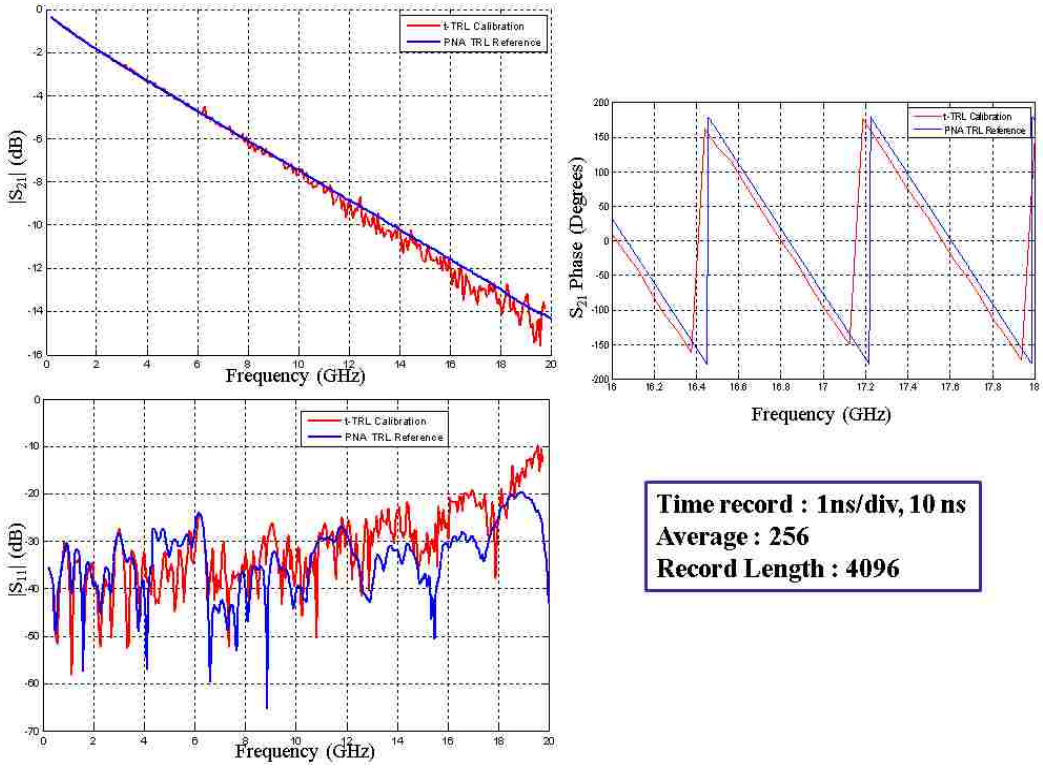

Figure 1.77: Results from the measurement setup 2

S_{11} and S_{21} magnitude and S_{21} phase are plotted in Figure 1.77. The results shown did not improve the results compared to the measurements without the splitters. The graphs were worse than the measurement without splitters. The setup 3 of the measurement also uses Tektronix DSA 8200 as both TDR and scope. Here no cables are attached between the generator heads and the splitters. The block diagram of this setup is shown in figure 1.78. S_{11} and S_{21} magnitude and S_{21} phase are plotted in Figure 1.80. For connecting the generator heads to the splitters, 3.5 mm precision adaptors were used. Because of the use of many adaptors, the setup is very rigid and good care had to be taken for the getting good proper connections.

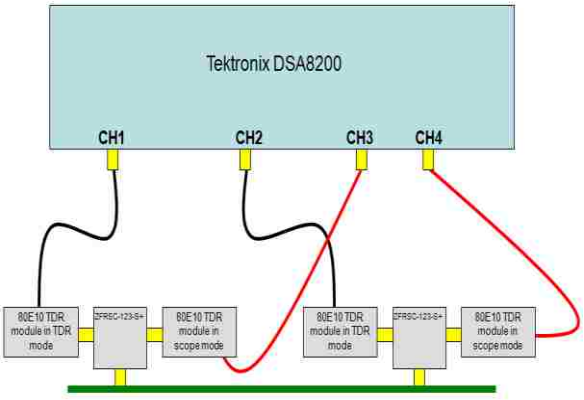

Figure 1.78: Block diagram for measurement set up 3

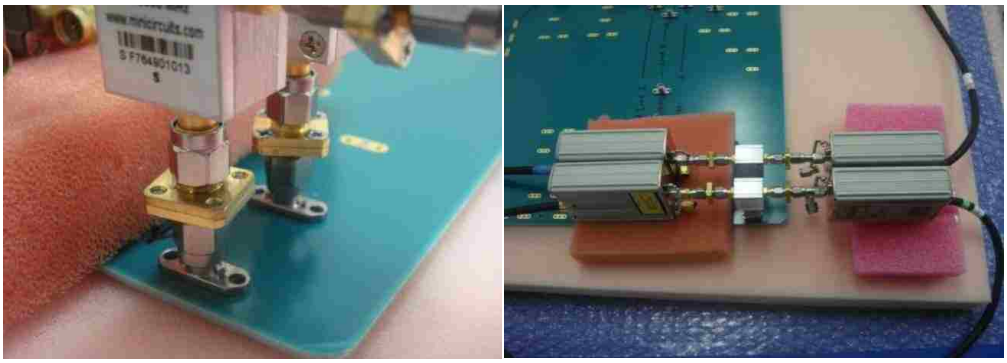

Figure 1.79: Connecting TDR generators directly to splitters

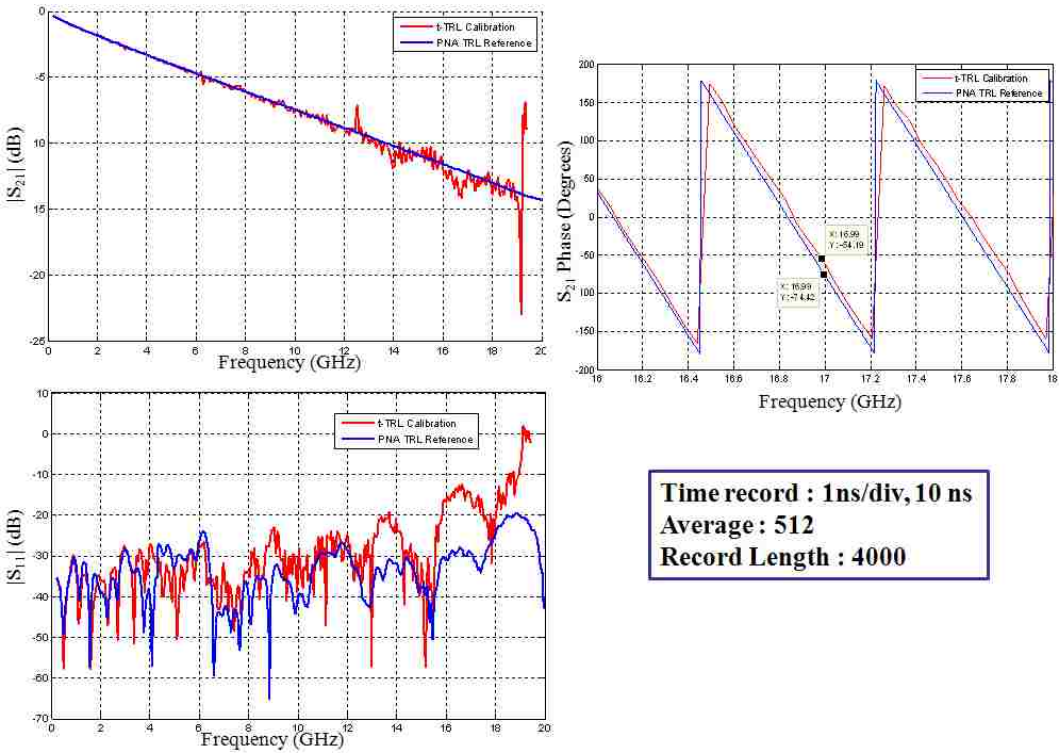

Figure 1.80: Results from the measurement setup 3

The results were not better than the results from the setup 2. The normal t-TRL calibration without cables and splitters gave much better results than the one with splitters and without cables. The entire experiment with power dividers did not give the improvements as expected from the circuit model simulation. Different measurement setups were tried. By theory and by simulation results, the switching errors can be eliminated by the procedures mentioned above. But the measurement done in the time-domain VNA did not give the expected results.

1.5. APPLICATION OF T-TRL CALIBRATION

The PCB substrate dielectric characterization tool based on TDR/TDT measurements together with the t-TRL calibration has been developed. This tool allows for efficient and frequency wideband extraction of two major parameters of a PCB FR-4

type dielectric substrate: its real part of relative permittivity ε_r', or dielectric constant (Dk), and its loss tangent $\tan\delta = \varepsilon_r'' / \varepsilon_r'$, which is also known as a dissipation factor (Df). In the t-TRL tool, the t-TRL calibrated time-domain responses are measured and converted to frequency-domain S-parameters. Then the extraction technique developed in Missouri S&T is applied to determine Dk and Df data. This procedure was initially proposed for frequency-domain measurements obtained using VNA [1], and its flowchart is shown in figure 1.81. However, the same procedure can be successfully used for S-parameters independently whether they were obtained through frequency-domain, or through time-domain measurements [9].

The very first step in this procedure is an application of the MS&T Link Path Analyzer tool to the input S-parameter data for checking the network passivity, causality, and reciprocity. Then the corresponding ABCD transmission matrix parameters are calculated. For a passive and reciprocal system, the complex propagation constant γ is calculated from the known A and D parameters, and the phase β and attenuation α constants are obtained as the corresponding imaginary and real parts of the complex propagation constant. Dielectric constant and loss tangent are then calculated from these phase and attenuation constants, as is shown in flow-chart. Though conductor surface roughness on the test vehicles substantially affects the extracted dissipation factor (Df) over the frequency range of interest [14, 15], the conductors were considered as smooth, and the conductor frequency behavior was assumed to be as $\sim P\sqrt{\omega}$, while dielectric loss behaves as $\sim Q\omega + R\omega^2$ to follow the Debye-like behavior [1], where $P, Q,$ and R are constant coefficients that depend on the PCB dielectric and copper foil. Once the dielectric loss is determined, the Df values can be calculated [1].

The test board with the TRL calibration pattern was chosen for comparison of the extracted dielectric parameters from the measurements of S-parameters obtained using two different methods - the frequency-domain VNA technique and the t-TRL method using TDR 2. The board has an FR-4 type dielectric with the standard copper foil conductors. The extracted data for Dk and Df parameters using both methods are shown in Figure 1.83 and Figure 1.84.

There is a good agreement between the results obtained using these two methods. The discrepancy for the extracted Dk value does not exceed 0.3%, and the average over the frequency range Df values do not differ more than by 2%, which serves as a validation of the t-TRL calibrated TDR measurements. The PCB used for the material parameter extraction is shown here. It is designed to work till 50GHz. Measurements were taken till 20GHz.

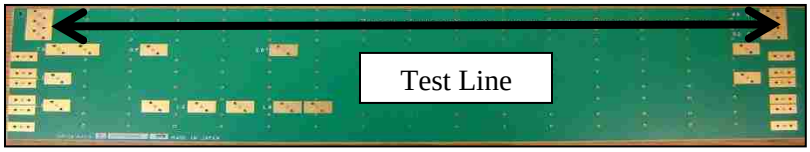

Figure 1.81: PCB board used for material extraction

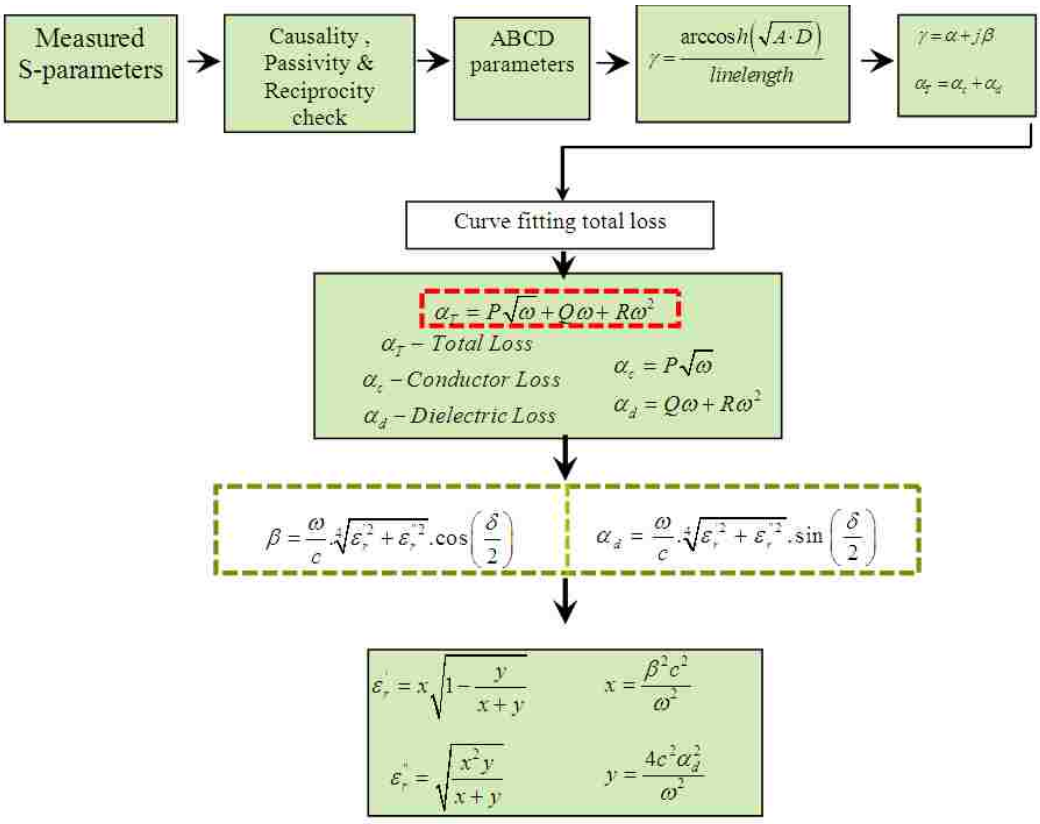

Figure 1.82: Flow-chart for the dielectric parameter extraction procedure

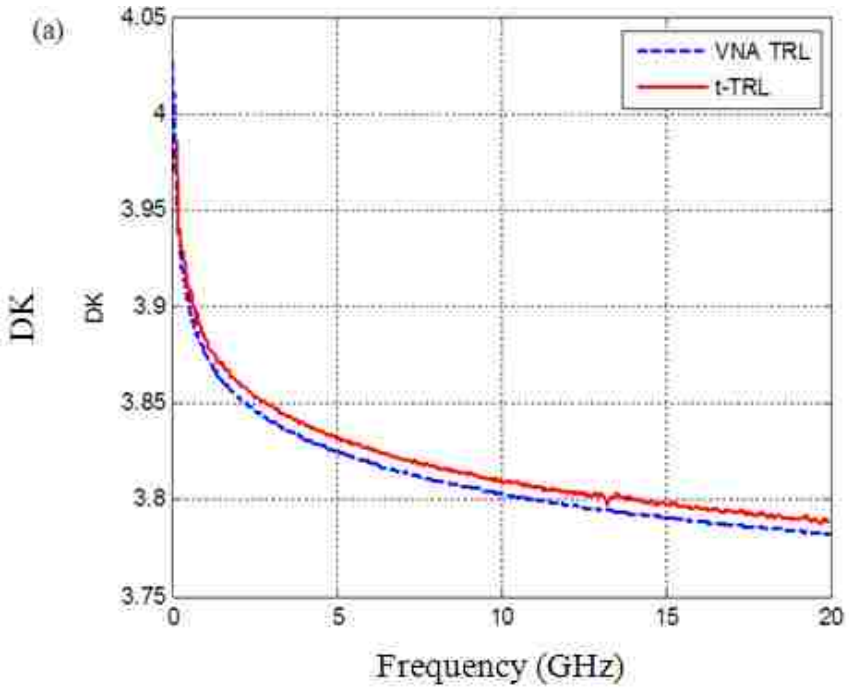

Figure 1.83: Dielectric constant extracted comparison

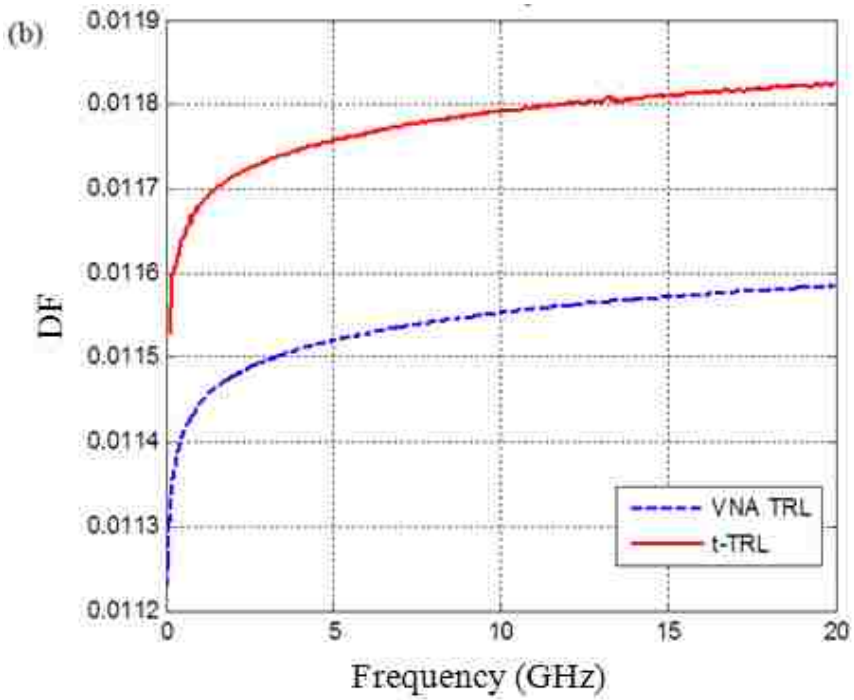

Figure 1.84: Loss tangent extracted comparison

1.6. TIME-DOMAIN TRL CALIBRATION AUTOMATED TOOL

The time-domain calibration is automated into a standalone tool. The tool was developed in Matlab. Graphical user interface (GUI) design is done in Matlab and a complete calibration tool is developed. The calibration tool is designed to work like a calibration wizard in frequency-domain VNAs. The tool is compiled into an executable. User can run the Main window to start the calibration tool. Before running the tool, it should be made sure that the instrument is switched on and it is connected to the computer (where the tool runs) through a GPIB interface. When the Main window is started it opens up as shown in Figure 1.85.

The Main window gives the user the option to setup the TDR and also shows the type of calibration options available in the tool. The user has to setup the TDR instrument properly before proceeding to the calibration methods. Other tabs are grayed out and will appear in time once the user goes through the calibration procedures. The Setup TDR option will call the TDR Setup Window as shown in Figure 1.86.

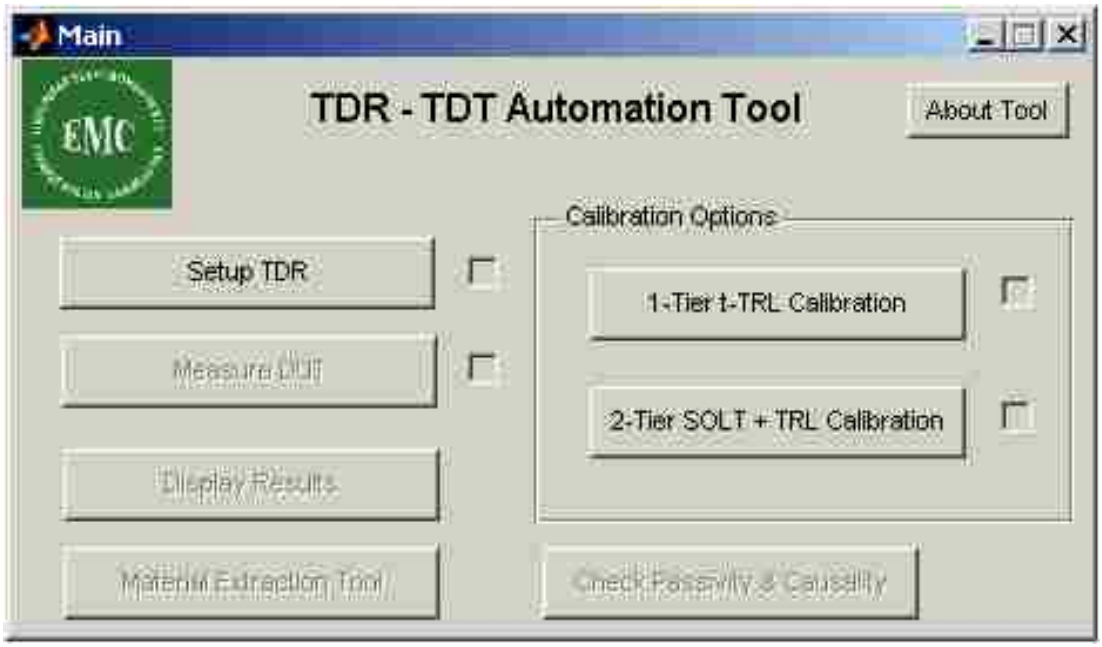

Figure 1.85: Main Window

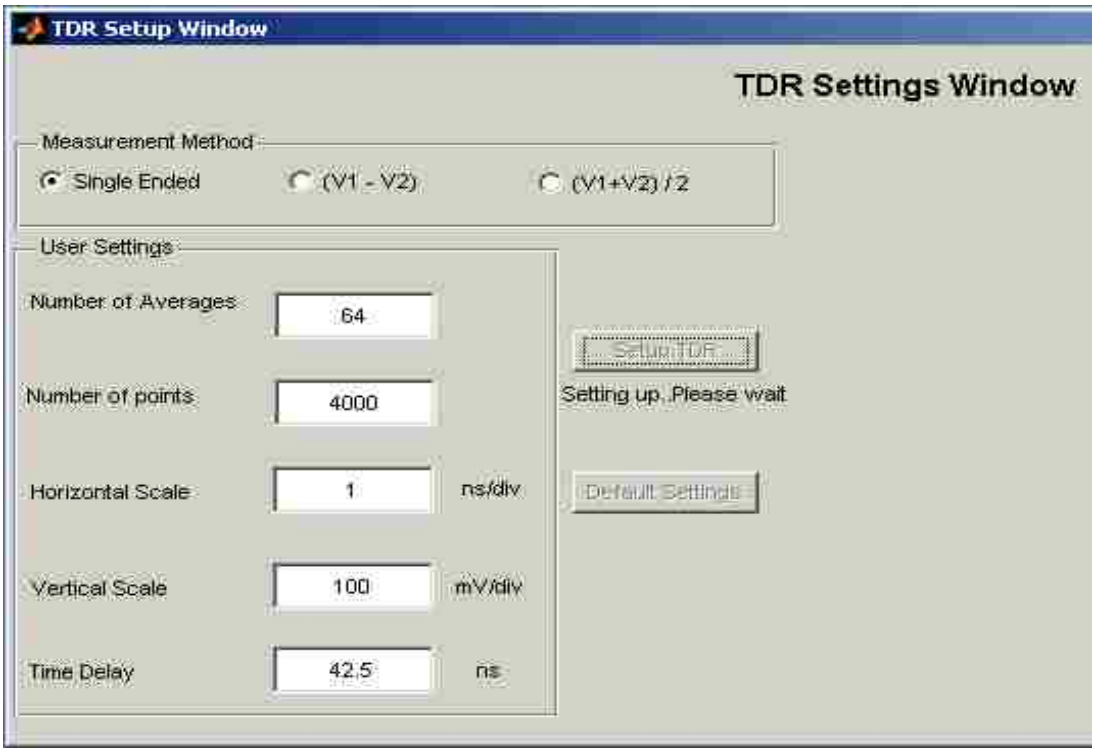

Figure 1.86: TDR setup options

The Setup window has the following options to setup the TDR. The number of averages, number of points, horizontal scale, vertical scale and the time delay. The user can use the default settings option in the tool to setup the TDR or can input user defined values. The tool will automatically check any errors in the user input. Once the values are entered the user can setup the TDR. Once the TDR is setup, the tool provides an option to view the TDR waveform as shown in Figure 1.87. This option is useful for the user for observing the DUT transitions. This will give an idea to the user about the connections on the DUT. The user can save the TDR waveform for future use. Tool will retain the values used to set up the TDR each time the user goes to the Setup Window.

Other user friendly options added to this window are the Zoom and Pan option. This helps the user to clearly view the TDR waveform. The figure below shows the TDR setup with an open transition at the port. Once the setup is complete the tool allows the user to go back to the Main window or setup the TDR again.

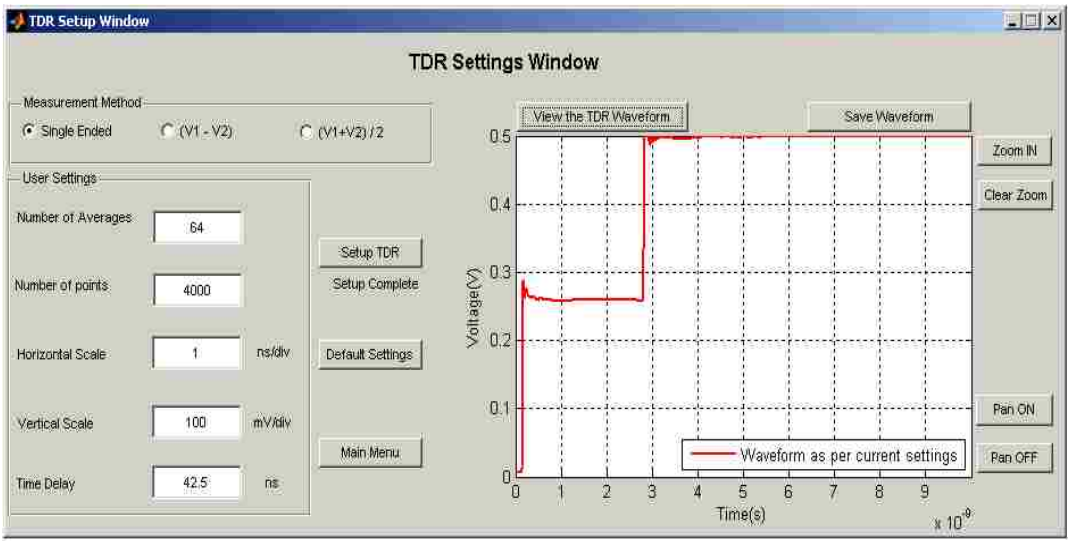

Figure 1.87: TDR setup with user defined parameters (single ended)

There are 2 more additional options available in the Setup window. The user can also setup the TDR in even mode or odd mode configuration. This option allows the user to view and save the even mode and odd mode waveforms. TDR setup to view the even mode configuration is shown in Figure 1.88. Though, the calibrations using the even mode and odd mode TDR setup is not programmed up in the tool. The Figure 1.89 shows the even mode TDR waveform zoomed in.

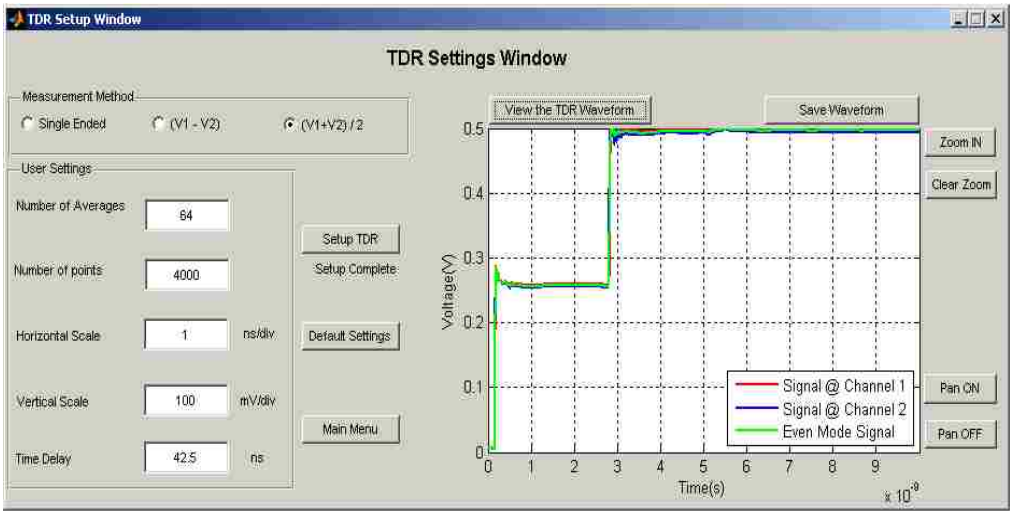

Figure 1.88: TDR setup with user defined parameters (even mode)

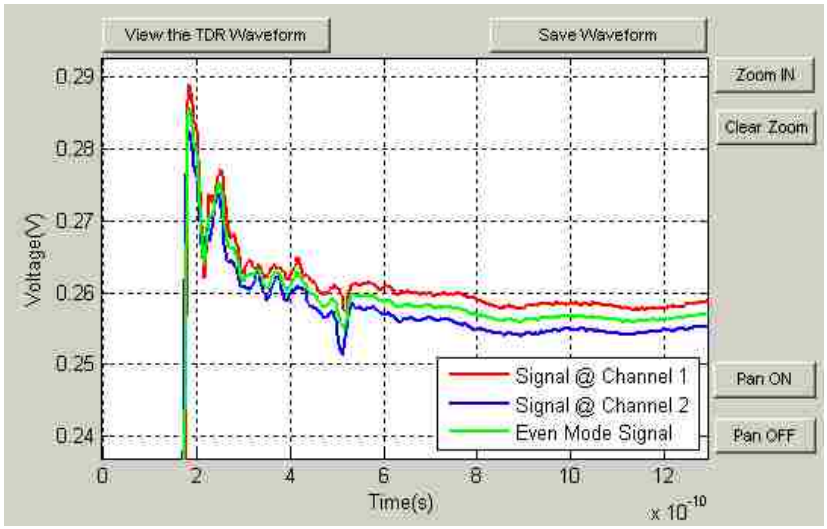

Figure 1.89: Zoom in and Pan options

Once the setup is complete, the user can go back to the Main window and select either two tier calibration or one tier calibration. If the user wants to do the 2 Tier calibration, SOLT calibration window pops up. This window allows the user to measure the time-domain TDR waveforms of the Short, Open, Load standards for both ports and the THRU standard. The Figure 1.90 shows the initial SOLT waveform measurement window.

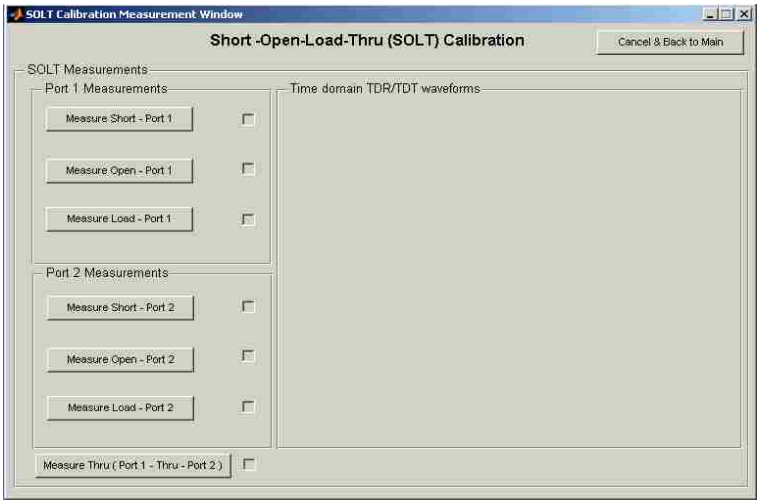

Figure 1.90: SOLT calibration measurement window

The user can connect the standards and measure the waveforms. The real time waveforms will be displayed on the window while measurements are taken. Once the standards are measured, the checkboxes will be checked to notify the user about the measurements taken as shown in Figure 1.91. After all the measurements are done, the tool will give an option to go the two tier calibration window.

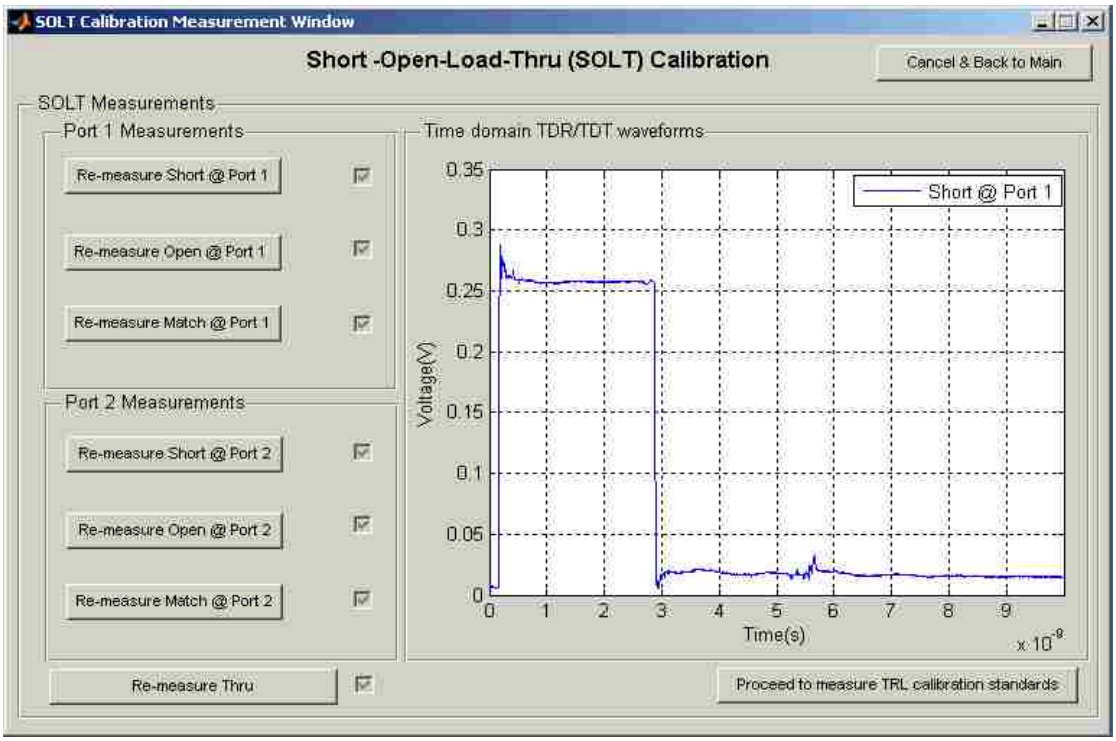

Figure 1.91: Measuring SOLT standards

The 2nd tier t-TRL calibration definition window gives the user two options. One is to input a user defined calibration pattern and the other one is to calculate the TRL pattern. If the user knows the frequency range for TRL calibration Line standards, then the user can define the pattern. If the user knows the frequency range of the measurement only, the tool can calculate the TRL pattern based on the frequency range and the length of the THRU. Loading a pre defined TRL pattern is a future addition to the tool. These options are shown in Figure 1.92.

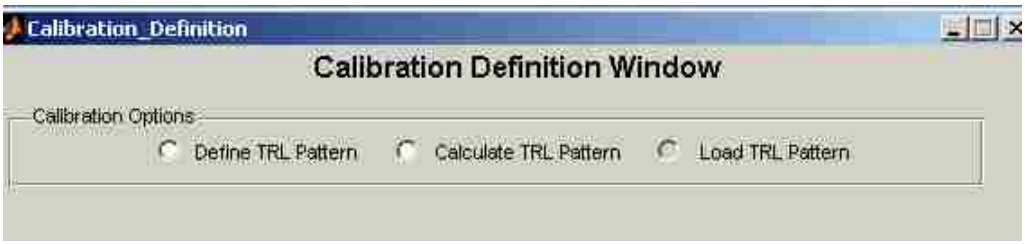

Figure 1.92: TRL calibration pattern options

While defining the TRL pattern, the user can enter the start and stop frequency and also the number of line standards. Then the user can define the TRL pattern. The tool guides the user to go through the calibration standards one by one as shown in Figure 1.93. Once all the standards are fed to the tool, the control goes to the measurement window for the TRL standards. This window allows the user to make the TRL calibration standard's time-domain TDR/TDT waveform measurements. TDR and TDT waveforms are measured at the ports as shown in Figure 1.94 and saved. The time taken for the measurements depends on the number of averages and the number of points.

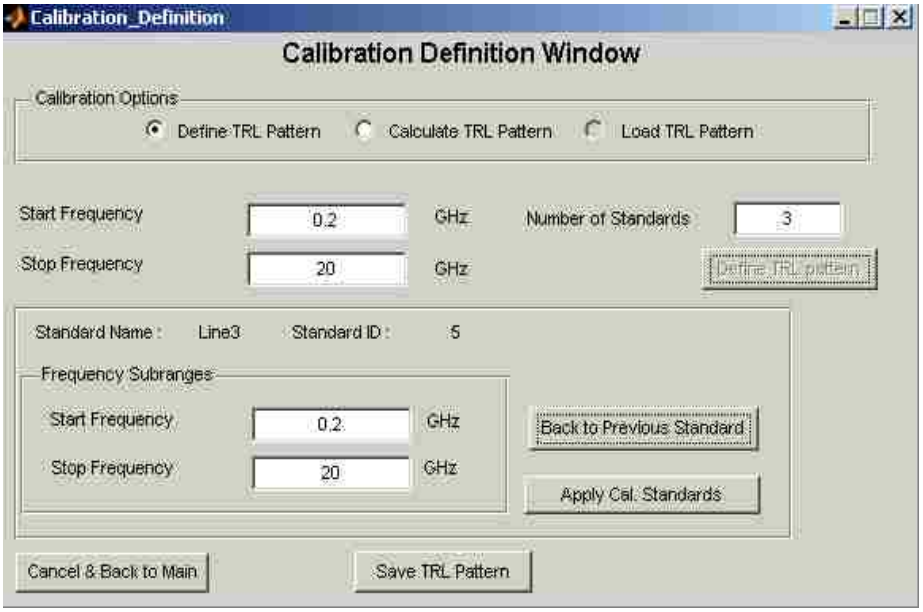

Figure 1.93: Defining a TRL pattern

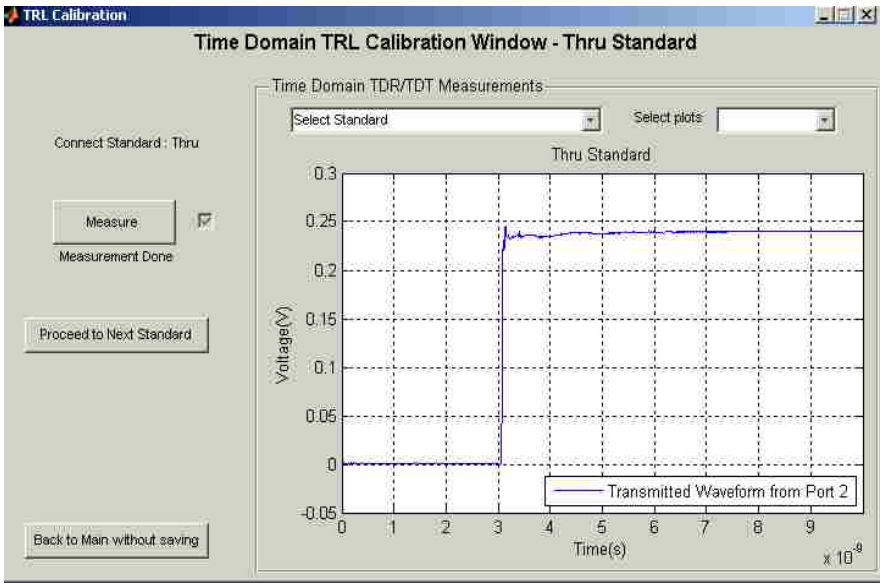

Figure 1.94: Measuring the TRL standard

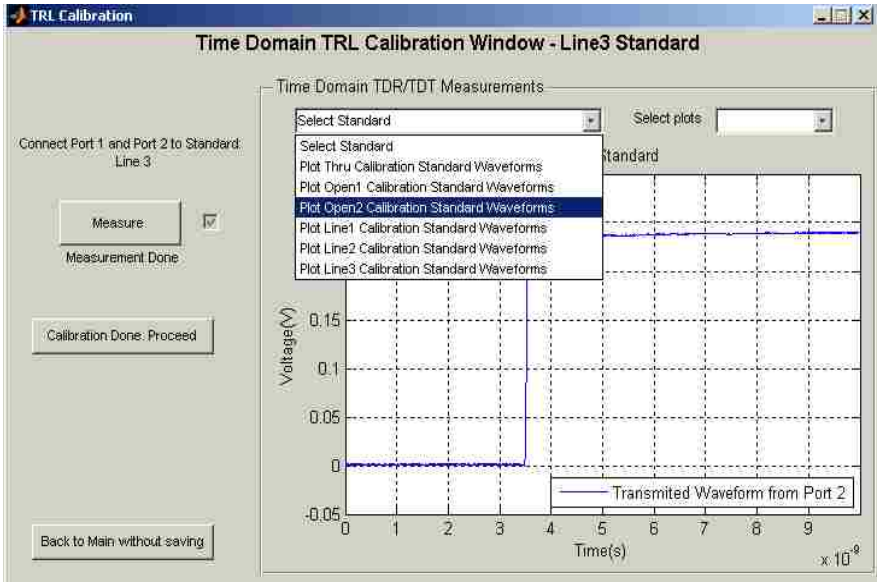

Figure 1.95: Options for viewing all the measured time-domain waveforms

After the measurements, user can view all the time-domain waveforms by selecting the particular calibration standard as shown in Figure 1.95. After all the standards are measured the tool is ask the user to proceed. Tool will pass the control to the Cut point selection window shown in Figure 1.95, where it automatically calculates

the point where the incident pulse is cut away from the waveform. It will ask the user to disconnect all the connections made to the TDR ports and measure. Once measured, the tool will display the Cut point calculated. The user can also input the cut point of his/her choice. The control now passes back the Main window where the tool guides the user to connect the DUT. Once the DUT is connected, user can click the OK button to start the time-domain TDR/TDT measurement of the DUT as shown in Figure 1.97.

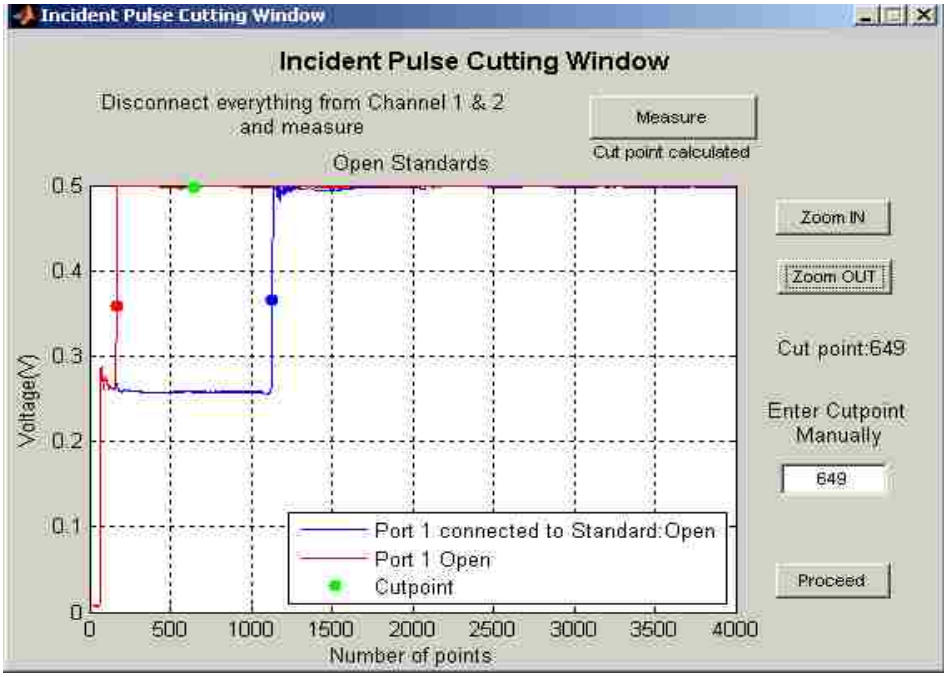

Figure 1.96: Cut point selection/calculation window

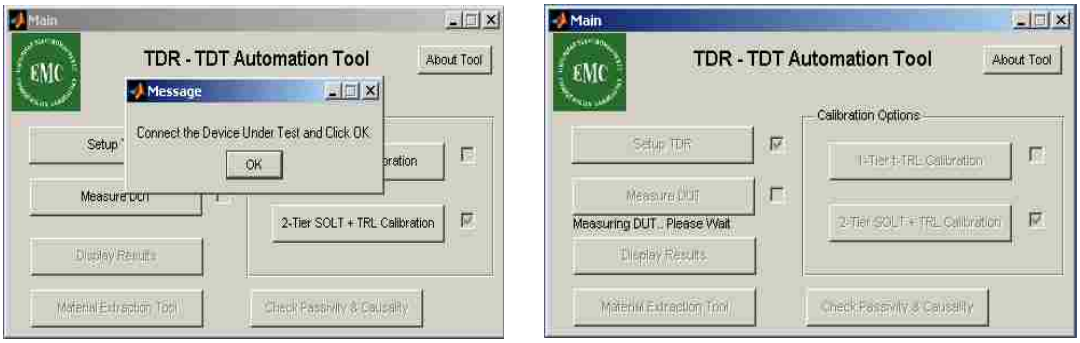

Figure 1.97: Measuring the DUT once calibration is defined

Tool will process all the time-domain waveforms measurements and apply the TRL calibration technique. Once the calibration is successful the tool displays option for displaying the calibrated results, material extraction tool and also additional option for checking passivity and causality as shown in Figure 1.98.

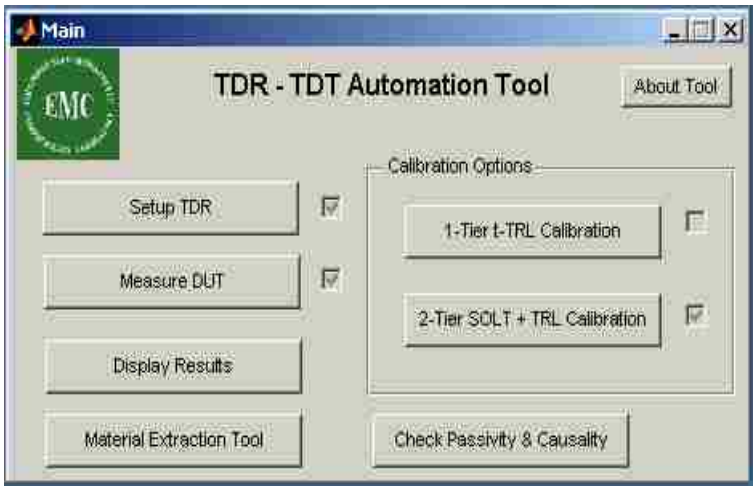

Figure 1.98: Main window giving options to view the calibrated results

1.7. CONCLUSIONS ON T-TRL ERROR ASSESSMENT

The random and systematic errors associated with t-TRL S-parameter measurements on printed circuit boards using TDR/TDT instrument have been assessed. It is shown that the random errors are not the main contributor to the overall error of S_{21} measurement of practical PCB transmission lines with FR-4 type copper-clad substrates in the frequency range up to ~ 20 GHz. The random errors can be further reduced, if needed, by the proper choice of the number of waveform averaged, the number of samples, and the time record.

The interpolation of the t-TRL frequency-domain dependencies can be performed by the padding of waveforms with the value of the last sampling point. The systematic error due to the TDR asymmetry can be eliminated by waveform windowing. Experiments were performed to eliminate the switching errors in time-domain VNAs.

Simulations showed that both two –tier calibration and measurements using power dividers can eliminate/reduce the switching errors. The results from time-domain measurements did not yield the expected results.

The PCB characterization tool based on TDR/TDT measurements together with the t-TRL calibration has been developed, and the material parameter extraction results have been compared with those measured using the frequency-domain VNA measurements. Good agreement of the results obtained through these two measurement techniques validates the t-TRL calibration application for accurate extraction of PCB substrate dielectric parameters.

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2. INTRODUCTION TO MODELING OF MULTILAYER PCBS

Power Distribution Network (PDN) design is one of the most challenging jobs in the high speed PCB industry. As the data rates are going high and the integrated circuits (ICs) are performing very fast, the power distribution through the entire circuit is becoming difficult. The size of the digital components is also getting smaller. Smaller components are forced to perform at a higher voltage level. It is the responsibility of the PDN to deliver proper power (current) to the ICs. Most of the printed circuit boards that are currently being designed and used in the industry are multilayer PCBs. These multilayer PCBs have thousands of vias and power area fills. Power area fills can be split planes. That means, even on the same layer of a PCB, there can be area fills with different logic levels. Add to that, differential signals that transition through the entire PCB. All these elements make the PCB really complex from the power delivery point of view.

Purpose of the work explained here is to understand how to effectively analyze and design a PDN and at the same time to anticipate the problems in the multilayer PCBs. The noise developed in the stackup of the PCBs can propagate to all direction. This noise can couple with some the critical signals in the stackup and creates incorrect signal levels. An effective PDN design can reduce the amount of noise generated and its propagation. Anticipating the noise propagation through the stackup allows designing better PDN design. The work explains the effort taken to analyze multilayer PCB taken from the industry to study and understand the PDN design. Simpler stackup is modeled and validated using a 3D solver.

2.1. MULTILAYER PCB STACKUP ANALYSIS

The analysis of multilayer PCBs with complex area fills numerous power and power return and large via counts is difficult. Modeling the entire PCB in a 3D solver is not practical. The problem arise from coupling between different power (PWR) layer pairs as well as exceeding a target impedance for a given logic level. Noise propagates between the PWR/Ground (GND) layers throughout PCB stackup. The fundamental

physics involves the tracing of the current paths. This helps to develop physical intuition and a relatively simple model that will include the critical currents.

2.1.1. PCB study. In an effort to understand the noise propagation through multilayer PCBs with complex area fills and to simplify the complex design by the application of simple physics, a particular PCB from the industry was selected. The PCB has 28 layers with GND/PWR planes and single/differential signal routing. Size of the PCB is 13 inch x 18 inch. The PWR planes are all area fills. They are designed to supply the required power levels to the active components place on the PCB.

The study was done in steps. The stackup was complex; hence it was divided into parts and analyzed. The aggressor (which is the main noise source) and the victim (which is affected) are identified first. Voltage Regulator Module (VRM) is on the top of the board and is the aggressor as shown in Figure 2.1. An IC that is connected to different layers in the board is the selected as the victim. There can be many active devices on the board. But for the start of the analysis, only the VRM and the IC is considered. IC is located on the right bottom of the board.

Figure 2.2 shows the path of the power draw of the IC from the VRM. The current from the VRM travels through the stackup in different directions before reaching the IC. The footprint of the victim IC looking from the top plane is shown in Figure 2.1. The path the current takes to reach the IC and back to the source can be complex and confusing. The aim is to trace the current path from the aggressor to the victim. Due to the complexity of the board the path is not a direct path. It follows so many transitions through the entire board before reaching the IC. The current is also made to pass through some passive devices (ferrite beads).

As the signal transition through the board, it couples with the other signals produced from other aggressors. These coupling can cause unwanted signal propagation through the stackup and can even result in the IC malfunction. The goal is to minimize the effect of this coupling. To do this, the path through which most of the current passes has to be identified. This process was performed first.

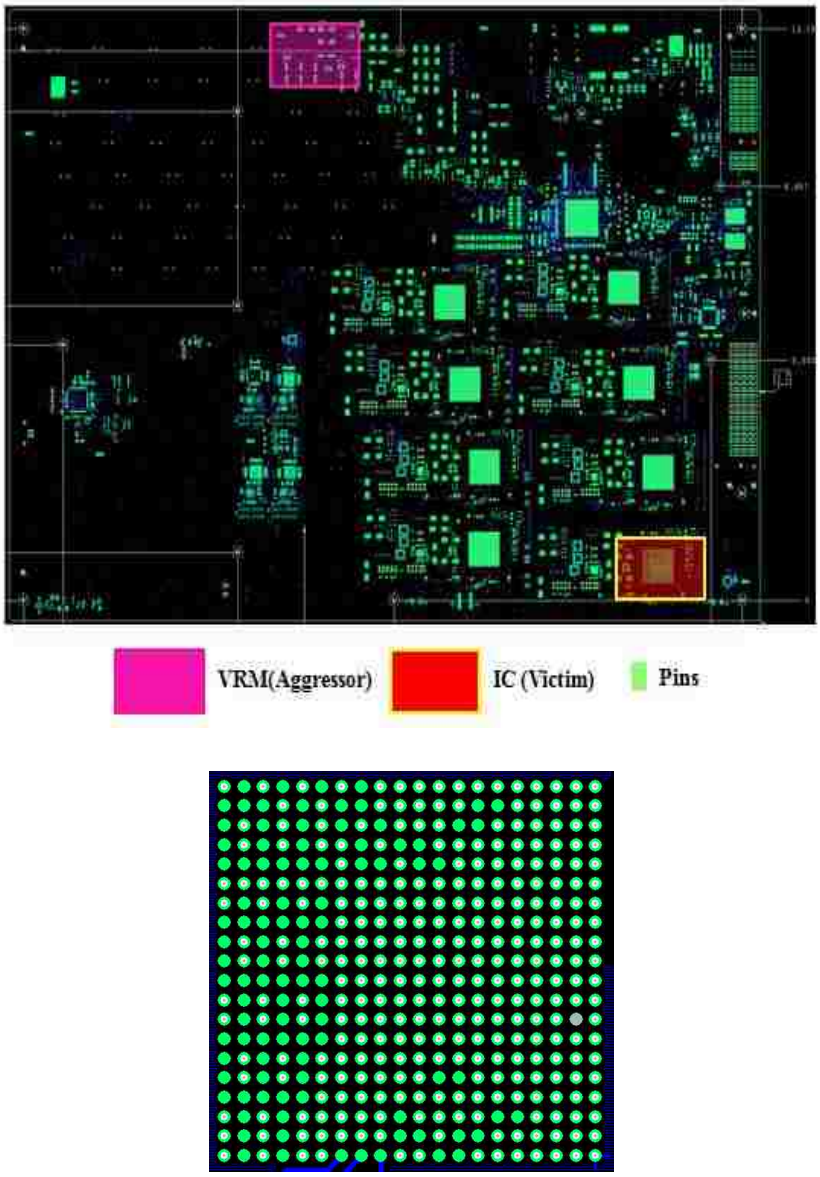

Figure 2. 1: PCB top view showing aggressor and victim IC footprint on top layer

Since the work is about analyzing the PCB stackup for better stackup design, it is often recommended validating the analysis by correlating with 3D FEM solver simulations. Multilayer Via Transition Tool (MVTT) developed in Missouri S&T is based on cavity model approach. 3D FEM solver results are compared with the analytical formulation in MVTT. High frequency simulation software (HFSS) is used as the 3D

solver. Therefore it is necessary to perform the validation at the very beginning of the study itself.

2.1.2. Analyzing the stackup in parts. First three layers were considered in the beginning. Top plane (TOP) is a full plane and is GND. The second plane is power plane (PWR02) and has different nets. The VRM is directly connected to this layer. The third layer is again a full GND plane. The current from the VRM will look for any conductive path to reach the load(IC). As the frequency goes up, the displacement current dominates. But as low frequencies, it is easy to trace the current as conduction current. If that is the case, then the other area fills nearby the area fills to which the VRM is connected directly can be neglected to simplify the design. Again the distance between the areas fills were compared to the height of the dielectric. If the gap-height ratio is more than 4, then that particular area fill was neglected. There are two ferrite beads connecting the PWR02 layer to the lower layers and then to the IC. These ferrites beads have the main purpose to provide noise isolation between the area fills. They also function as a path for the signal to reach the IC.

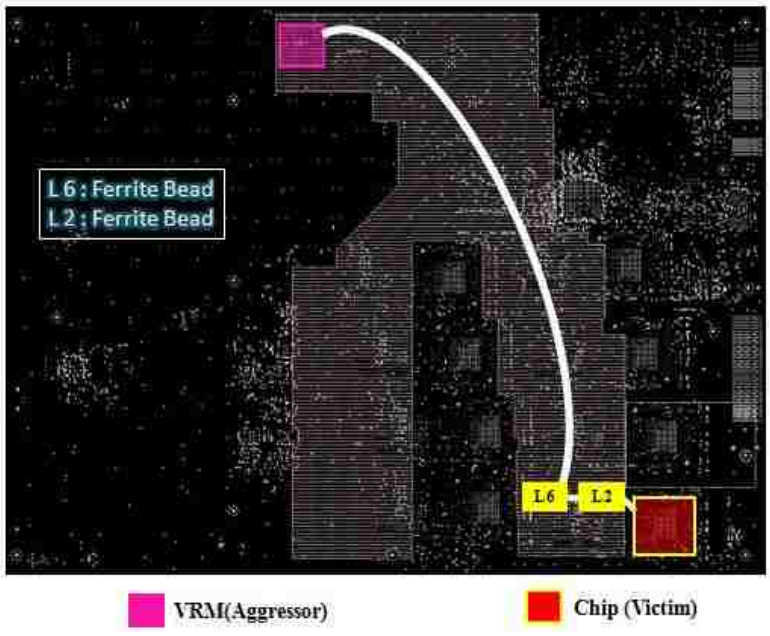

Figure 2. 2: Current path from the VRM to the chip

The white line shown in Figure 2.2 is the main current path from the aggressor VRM to the victim IC. Hence while trying to simplify the complex geometry; it is important to take into consideration, this particular area fill and its main signal propagation path. To be more precise, only the area fill shown in the figure below needed to be considered. The selection of the area fill shape is critical while simplifying the complex geometry. The capacitances associated with these shapes are important. The PDN is usually designed with specific target impedance. Ideally this target impedance profile should have flat response over a frequency range and they should be as low as possible. Parallel plate capacitance formed by the area fills influence the low frequency behavior of the impedance profile. But the impedance profile will not have a flat frequency response on a real PCB. It will have poles and zeros alternatively. As the TOP and the GND03 are full planes, effect of current below GND03 is not likely to affect the current through the top two cavities. The fringing fields from the edges of the PCB are neglected in the modeling process. It is made sure that the boundary conditions (BC) used for MVTT and HFSS are same. The PWRO2 plane is modeled as the same shape in the board and two full planes are kept above and below it as shown in Figure 2.3.

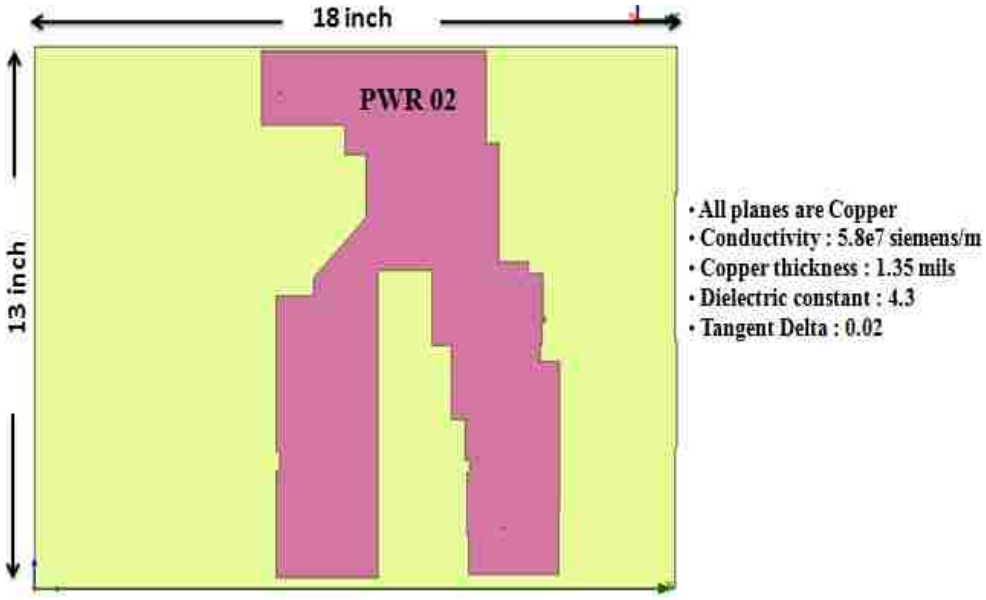

Figure 2. 3: HFSS model for the 3 layer PCB showing area fill

To see the effect of the couple between two areas in the PCB, two ports are selected. Port 1 is the location of the power pin of the VRM and port 2 is an arbitrary via location on PWR02 very near to the actual position of the victim IC. The modeled geometry is shown in the figure 2.3. The PWR02 area fill is highlighted and the light yellow region is the cavity between TOP and GND03. The conductor and dielectric properties of the model are shown in the figure too. The shape and the dimensions of the planes are maintained while modeling the PCB. The shapes of the first three planes are shown below in the Figure 2.4. Two ports shown in the Figure 2.4 are the two power (PWR) vias penetrating the geometry.

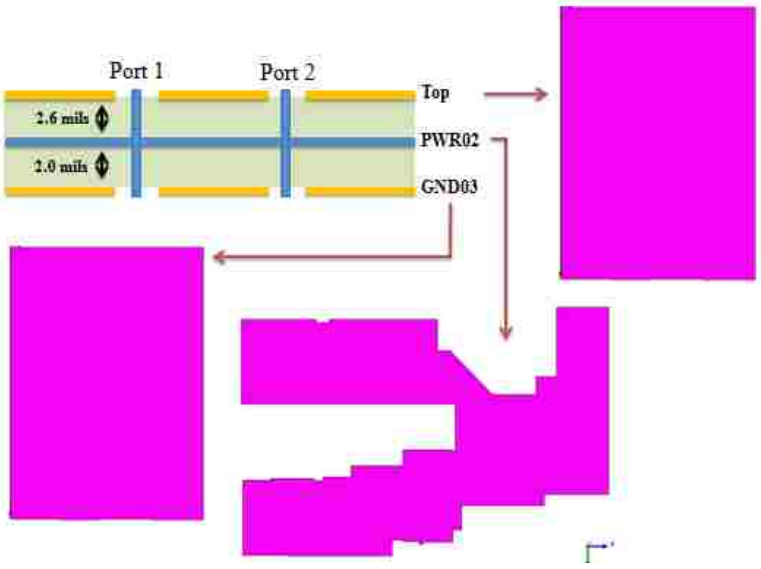

Figure 2. 4: Shapes of the planes modeled in HFSS

It is necessary to understand how cavities are formed in the PCB stackup. The figure below helps to visualize the cavities formed by the top three planes of the stackup. The top cavity is formed between the TOP and the PWR02 planes. Similarly another cavity is formed between the PWR02 and the GND03 planes. These two cavities are of the same shape. The third cavity is formed between the TOP and GND03 planes. The cavities are shown in Figure 2.5.

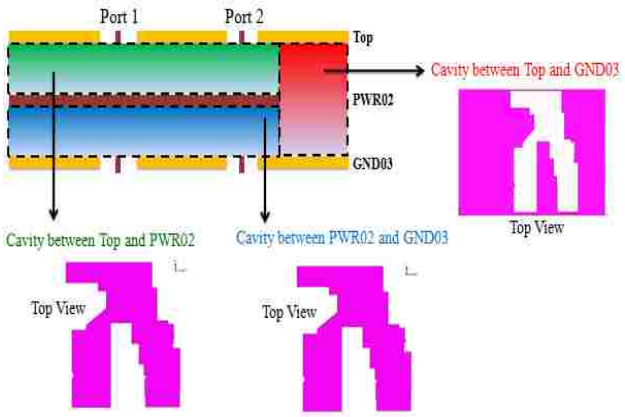

Figure 2. 5: Cavity formation in the stackup

The cavities formed by the planes are divided into rectangle and triangles. This geometry information is given to MVTT as an input text file. Same geometry is modeled in HFSS too. Padstack information is obtained from the real PCB board and the same pad stack is used for the modeling too. The HFFS model shown in Figure 2.6 shows the geometry creation with the pad stack information. Once the geometry (cavity) information is given to the MVTT engine, it reads the cavity information for analytical processing as shown in Figure 2.7.

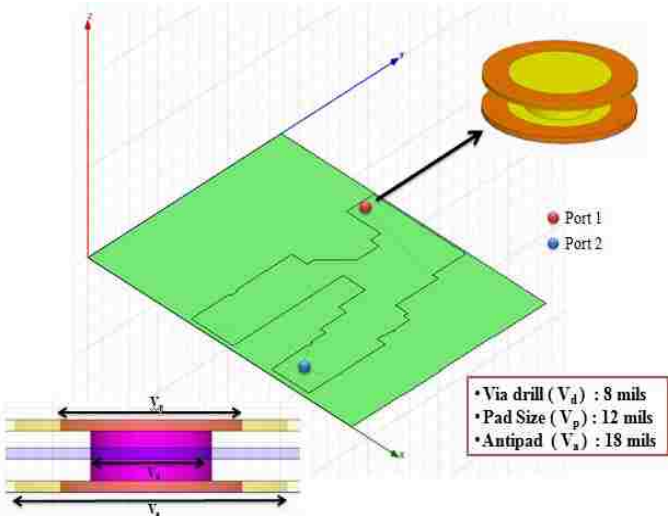

Figure 2. 6: HFSS model showing ports and padstack

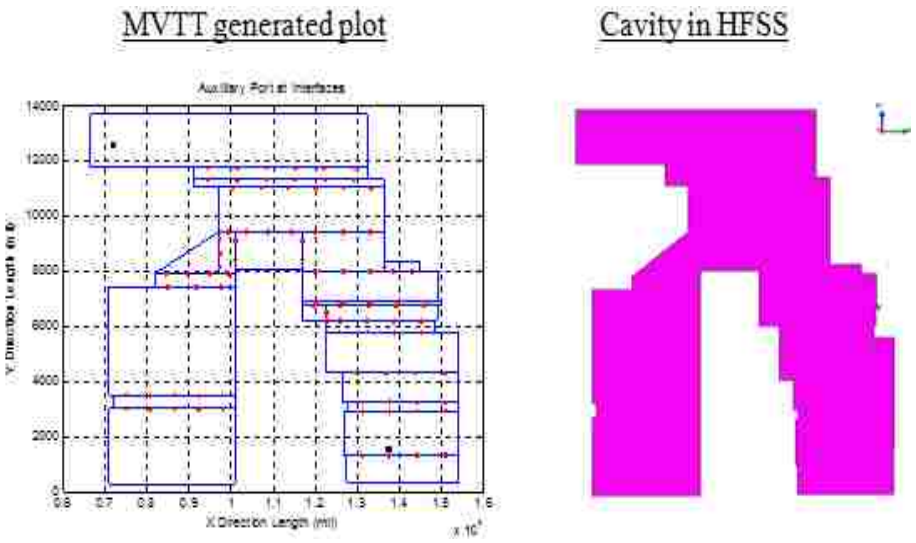

Figure 2. 7: MVTT created plane shape and HFSS model

The simulations were done in both MVTT and HFSS. The transfer parameter will give an idea about the noise coupling between two ports in the PCB. Here S_{21} is looked into to see the coupling between two ports. The magnitude and phase of S_{21} are plotted below in Figure 2.8 and Figure 2.9.

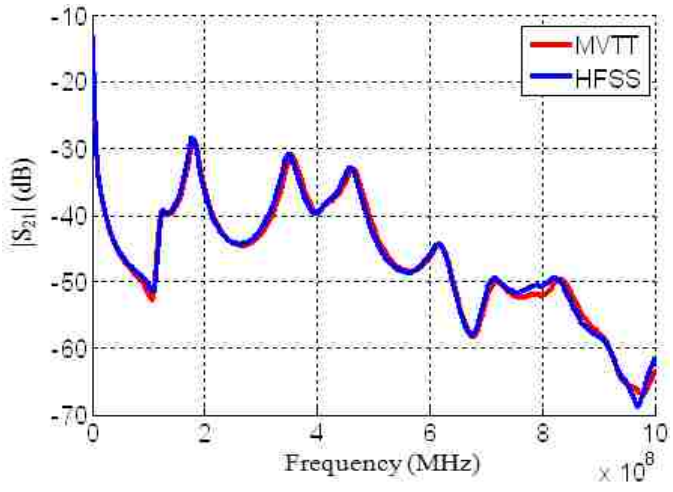

Figure 2. 8: S_{21} Magnitude simulation results comparison

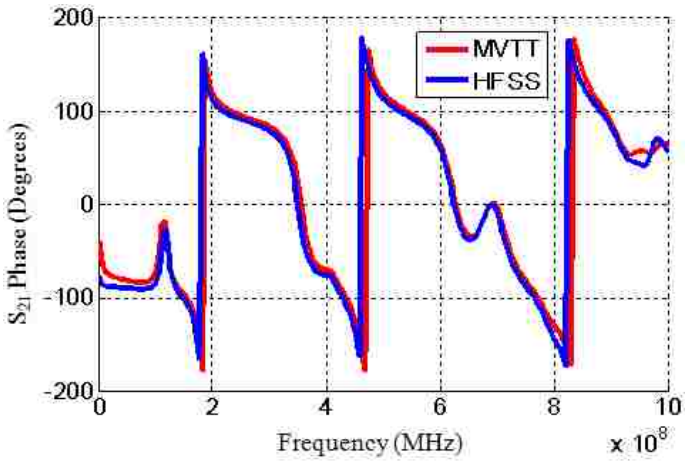

Figure 2. 9: S_{21} Phase simulation results comparison

The graphs show very good correlation between MVTT cavity model analysis and HFSS. Now the same procedure is applied to the entire stackup. The signal layers are not considered here. The PDN design has little to do with the signal traces where it is single ended or differential routing. It is often how the noise created in the PDN affects these signal traces and the critical through them. From the PCB stackup, there are full GND planes till layer twelve. The stackup till GND12 is shown below in Figure 2.10.

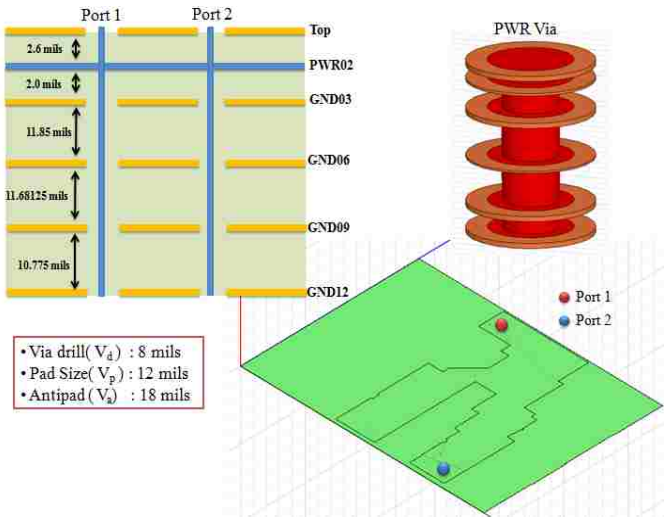

Figure 2. 10: 12 layer stack and padstack

As the planes GND06, GND09 and GND012 are full, not much difference is expected in the coupling between two ports. The results comparison for the 12 layer stackup is shown below in Figure 2.11 and Figure 2.12. S_{21} magnitude and phase shows very god correlation with the HFSS simulation. S_{21} magnitude starts from near zero which indicates that there is direct current path from Port 1 to Port 2.

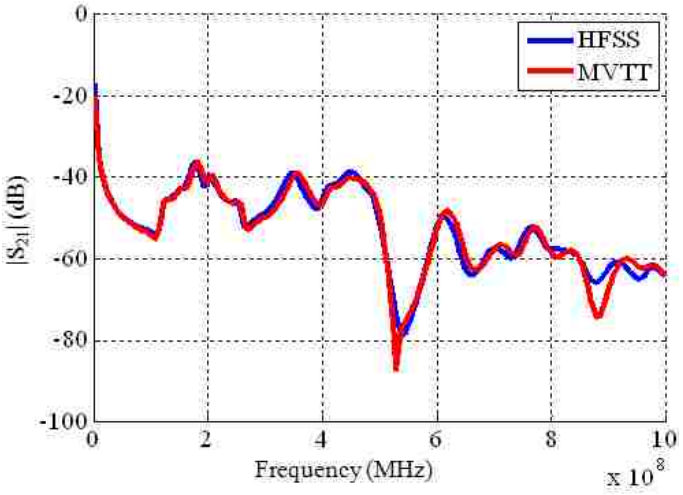

Figure 2. 11: S_{21} Magnitude simulation results comparison

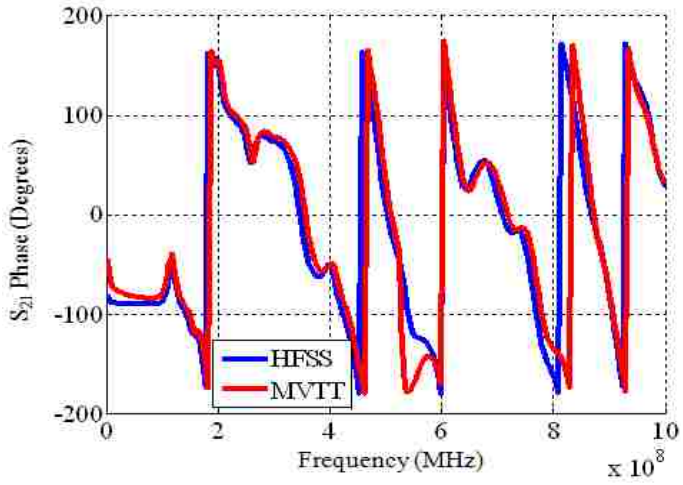

Figure 2. 12: S_{21} Phase simulation results comparison

Now it is confirmed that the cavity model approach in MVTT is a good alternative to the 3D FEM solver for PDN analysis. It is also good to know the amount of time required to simulate this 12 layer stack in MVTT and HFSS. Time taken for simulation is:

MVTT (200 Freq points) : 1 hour 40 minutes

HFSS (200 Freq points) : 9 hours 20 minutes

The MVTT simulation time is almost 8 times faster than HFSS simulation time for obtaining satisfactory results. Now the number of frequency points in MVTT simulations is changed and the results are potted as shown in Figure 2.13.

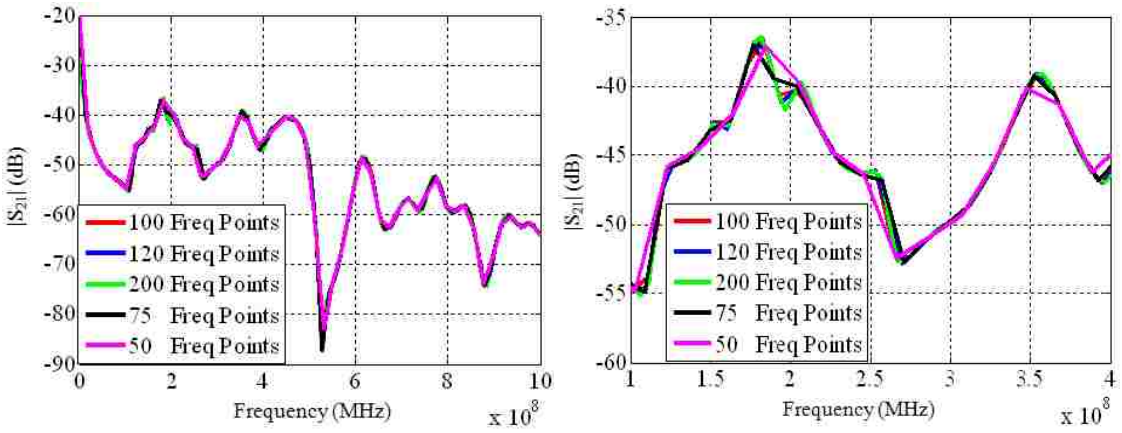

Figure 2. 13: Simulation with different frequency points

The MVTT simulation with 50 frequency points still gave good results and is comparable to the one with 200 frequency points. Some peaks and nulls are missed with fewer points, but the overall profile of the graph remains the same. The time taken for 50 frequency points is just 23 minutes, which when compared to the 9 hours 20 minutes taken by HFFS; is pretty fast.

2.1.3. Identifying return path. The PCB stackup was studied for return path. The PCB stackup is filled with thousands of vias of which some of them function as return vias for the power current flowing through the PCB.

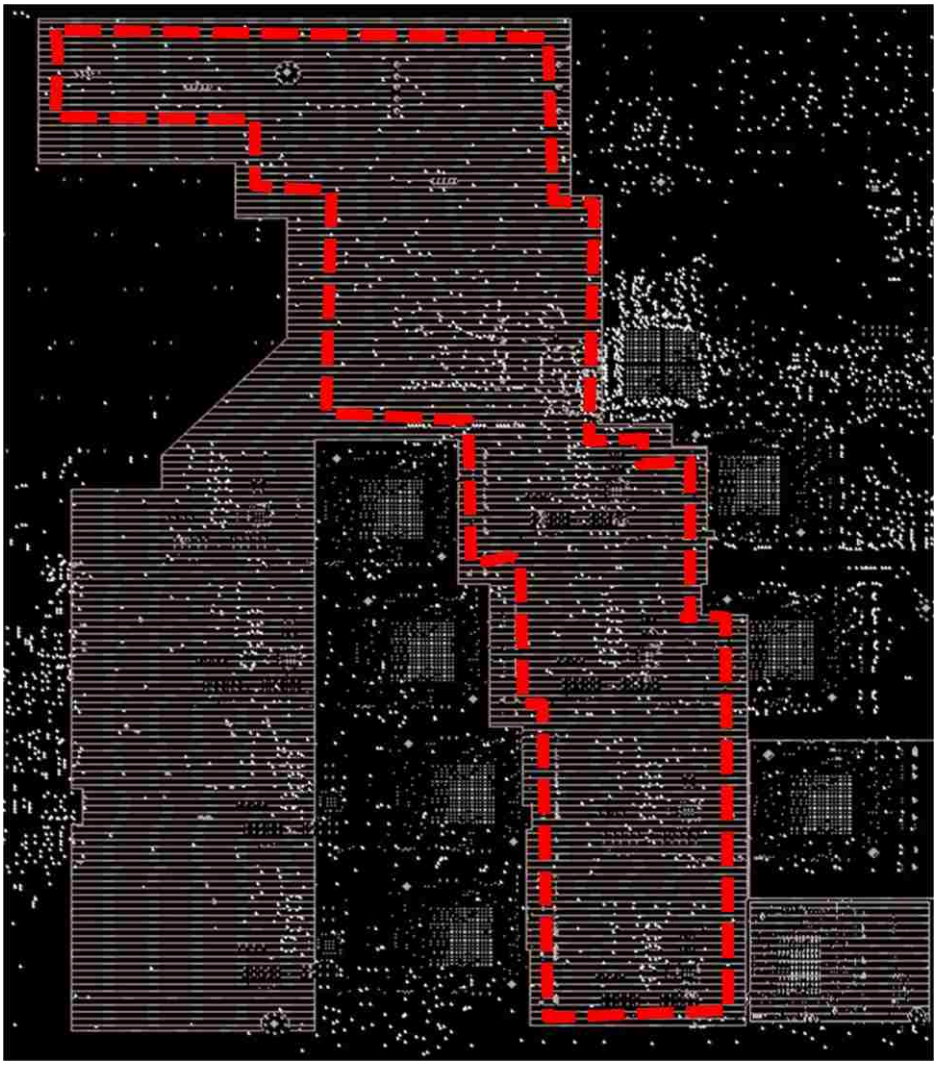

Figure 2. 14: PWR02 plane area fill

For modeling the PCB it is necessary to estimate the right amount of return vias and also its location. For example, the Figure 2.14 shows the PWR02 area fill. The area shown in red has 157 GND vias that were connected to all the GND layers in the stackup. Including all these 157 GND vias for a single layer will make the geometry complex. Therefore, it was decided that one power via should have only the nearest power return via (GND via). This simplifies the model a lot. This method was adopted for the entire PCB. As the current is traced from the VRM to IC, the return path is also looked into and the PWR return vias (GND vias) close by the PWR vias were selected. The areas near the

ferrite beads were closely studied to indentify the closest PWR return vias. Figure 2.15 shows the GND vias selected for the current return path for ferrite beads L6 and L2.

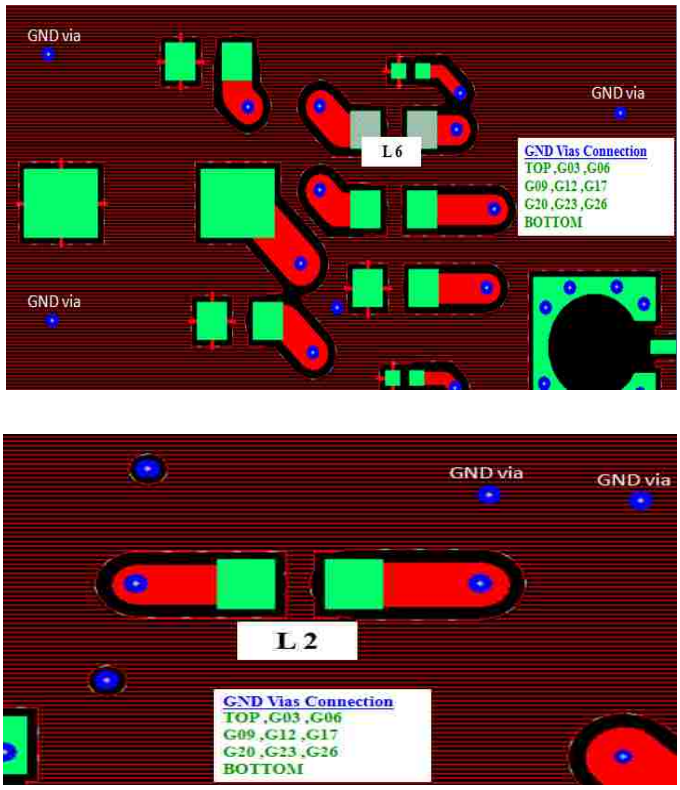

Figure 2. 15: GND vias nearby ferrite beads

The layers below G12 to G17 are power planes with complex area fills. They are floating planes having no connections to the main PWR vias carrying the PWR current. The return current while returning to the source has to pass through these floating planes. Since these are no direct contacts to these planes, the return current will propagate as displacement current through the plane cavities. This propagation is a potential noise coupling problem. The displacement current can take any path back to the source. Since the current and the current return have to see each other, the path of the displacement current through the complex area fills is critical. As the frequency increases the current takes the path of least impedance. In this case, the case tends to take the path of least

inductance. Therefore it is important to have nearby return vias for the PWR vias. Nearby vias can reduce the overall inductance associated with the current loop and this facilitates the design of a PDN with low target impedance.

2.1.4. IC pin configuration and connections. When building up the simplified geometry, the IC pin configuration was studied. The IC has 400 pins connected to different logic levels in different layers. The main path of the current from the VRM to reach the IC is through the area fill in layer P16. Figure 2.16 shows the particular area fill which has 17 PWR via connections to the IC. The GND vias near to the IC location is also marked.

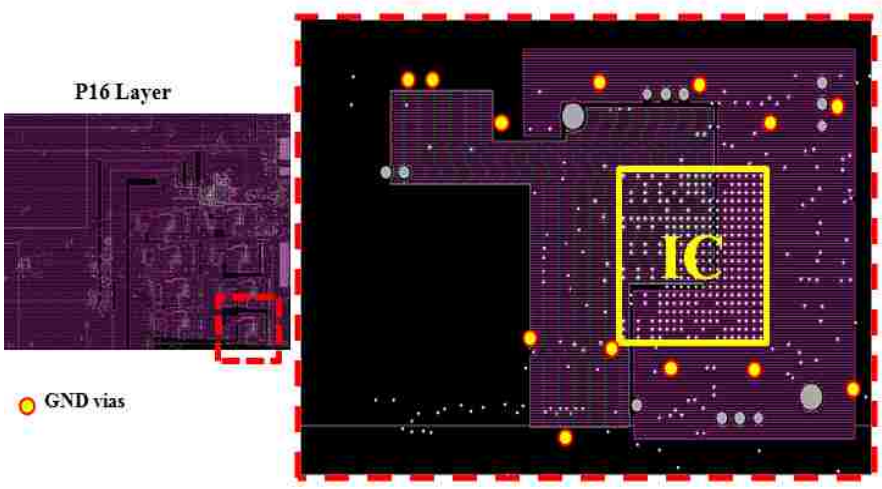

Figure 2. 16: P16 Layer area fill and nearby GND vias

The IC has 24 PWR return vias connected to the same area fill on P16. Therefore out of the 400 pins of the IC, only 41 vias (17 PWR vias and 24 GND vias) are considered for modeling. At this point it is necessary to study the importance of these 41 vias in modeling. These vias are concentrated on a small location on the PCB. Simulating the 28 layer PCB in HFSS with 41 vias is itself a big overhead for the solver in terms of the simulation time and computer resources. To conclude this, 28 layer PCB was created

in HFSS as shown in Figure 2.17. All layers were considered full plane as putting the actual area fills into the model will make it more complex.

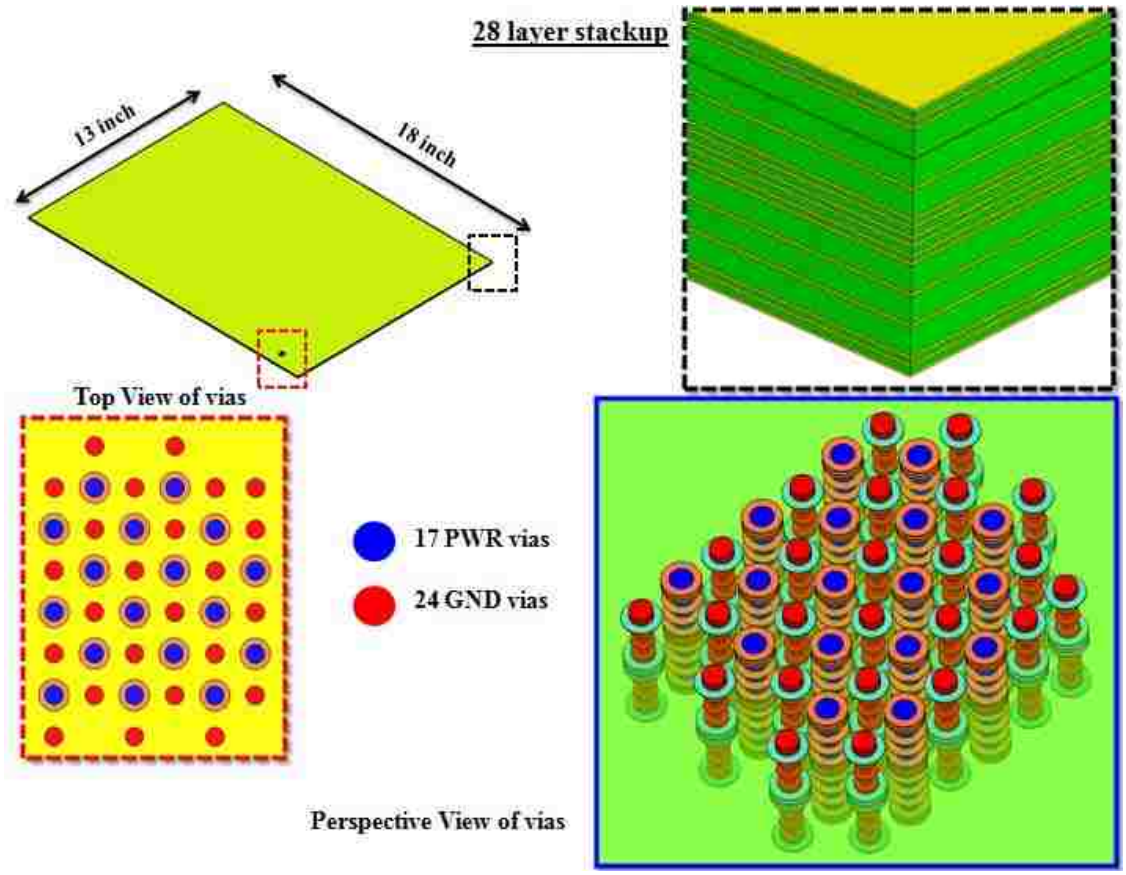

Figure 2. 17: HFSS model for the 28 layer PCB with 41 vias

17 power vias out of the 41 vias selected are connected to the P16 layer which is more than half way down the boards. The 24 GND (power return) vias are all connected to the GND planes. The inductance associated with the vias that are close by is important because inductance is a function of length. The return current from the IC can flow through all these 24 GND vias or through some of them. The impedance the IC sees looking into the board will depend on the number of vias penetrating these planes and also on the via connections. When the current flows through these vias, it can create noise

propagation through the cavities. This noise can couple with signals on some other part of the PCB. Hence it is important to model the correct amount of vias for a better PDN impedance profile. In the HFSS model, to see the effect of these 41 vias penetrating, ports were assigned to the all the 17 PWR vias. This 17 port model was simulated to compare with the same MVTT model.

As all the 17 PWR via are only connected to the P16 layer, the return path is through the displacement current through PCB cavities. It is often handy, to have an estimate the response of such a geometry when simulating. Because of no direct conduction path, the low frequency behavior of the geometry will be capacitive in nature. The capacitance value can be calculated from the Z_{11} impedance profile for a single port simulation. The capacitance created by the cavities till P16 (C_{upper}) is in parallel with the sum of the capacitance creates by cavities from P16 to Bottom layer (C_{lower}). C_{upper} and C_{lower} are the parallel sum of the individual parallel plate capacitance formed by the planes. The parallel sum of these capacitances is the total capacitance (C_{total}). This is shown in the Figure 2.18. Port is assigned to the PWR vias which have connection to layer P16 only.

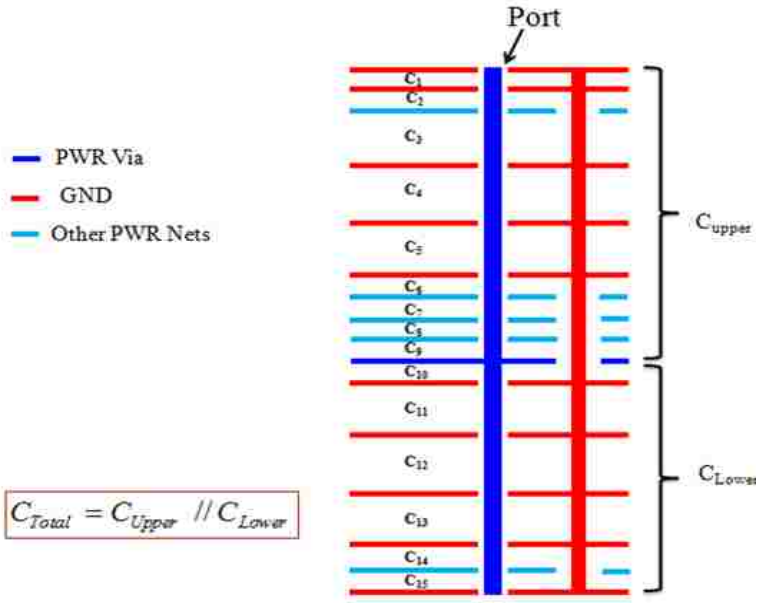

Figure 2. 18: Stackup side view and calculation of low frequency capacitance

The HFSS and MVTT model were simulated with 17 ports. The simulation gave a 17 port S-parameter result. These S-parameters were exported as an s17p file (touchstone file) to ADS and post processed to yield a single port result. ADS model used for post processing is shown in Figure 2.19. The 17 ports of the s17p file were connected together and this will be similar to looking down the PCB from a single port of the IC. Figure 2.20 and Figure 2.21 shows the comparison of the HFSS and MVTT results for both Z_{11} magnitude and phase.

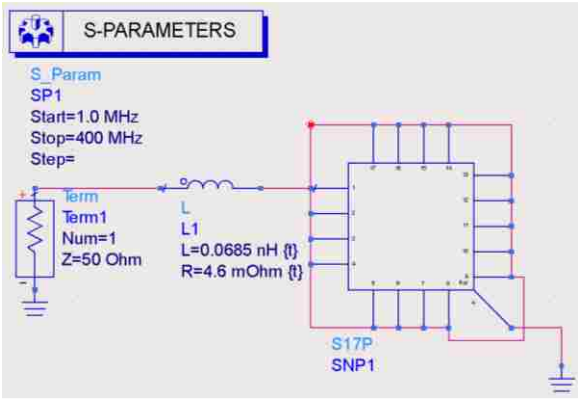

Figure 2. 19: ADS model used for post processing

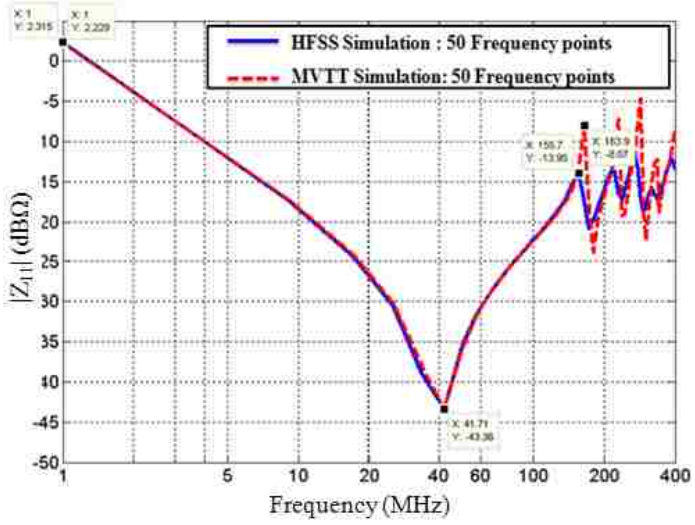

Figure 2. 20: Phase of Z_{11} comparison

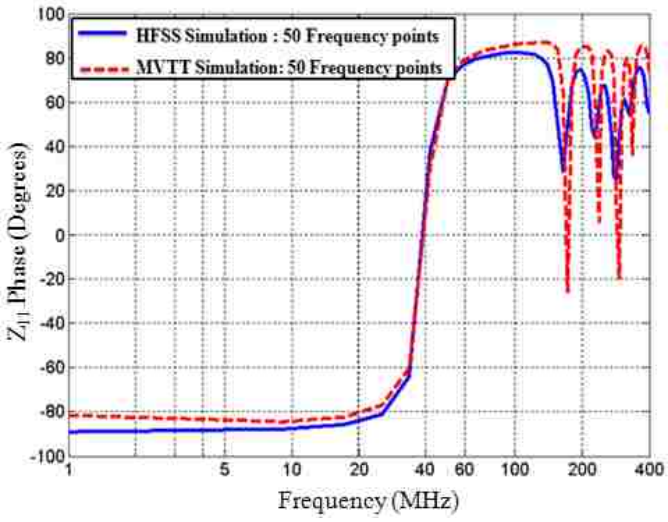

Figure 2. 21: Phase of Z_{11} comparison

The HFSS and MVTT simulation matched very well. The post processing needed a small lossy inductance in series with the Port. Using this inductance the results matches well. This may be due to the inductance associated with the port definition in HFSS. Waveguide ports were used for all the 17 ports in HFSS.

2.1.5. Current propagation through PCBs with floating planes. The PCB studied here has a lot of floating planes. When there are floating planes, the current path especially the return current path is confusing. It is because the return current flows as displacement current and has to penetrate these floating planes to reach back to source. Tracing the current through the entire PCB is difficult. But to design a simpler and better stackup design it is an essential burden. Tracing the current involves tracing both conduction and displacement current. Here it is critical to identify the nearest return vias as explained earlier. The current path through the 28 layer stack is shown below in Figure 2.22.

The component 1 and 2 are the ferrite beads L1 and L6. From the Figure 2.22 the current makes lots of transition through the stackup before reaching the IC. These via transitions have to minimize as they can propagate noise through the cavities. Once the current reaches the IC it will look to go back to the source. The PWR return current will try to see the PWR current while returning and this makes the return current to penetrate

the floating planes. If these floating planes are full planes, the current penetrate through the via holes. But if they are floating planes with area fills, then there is a chance of these current penetrating the via holes, spreading across the area fills and coupling to the other area fills nearby. This makes the return path very complex to analyze.

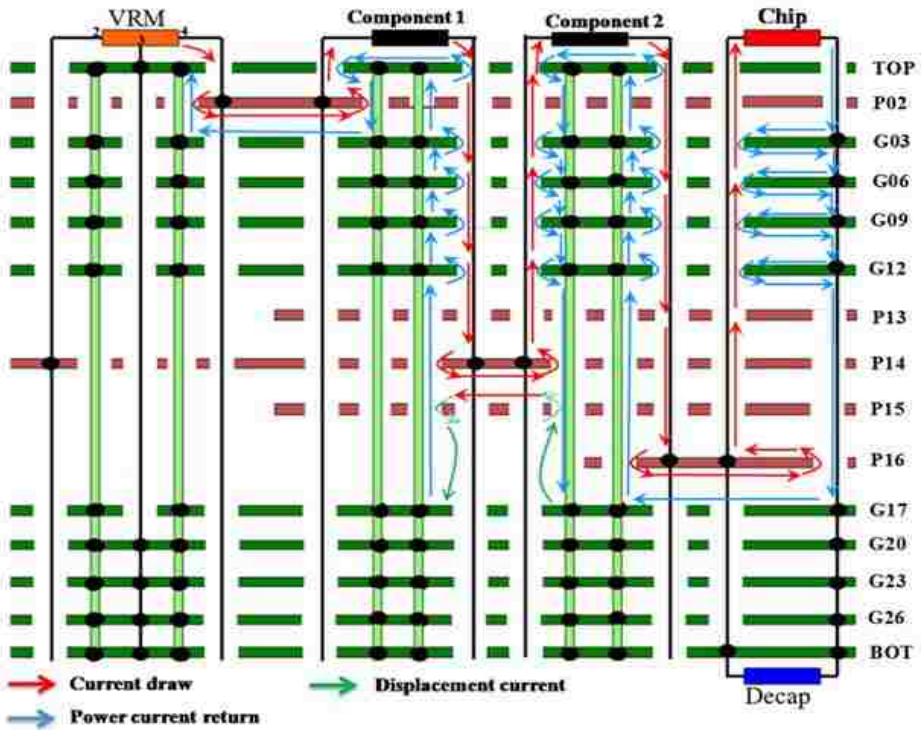

Figure 2. 22: Tracing current through PCB stackup

Here the return current reaches the IC and look for the nearest GND (PWR return) via nearby. It will flow down the stackup by spreading through the planes and via holes to reach GND17 layer. Here will be flow on the top surface of the GND17 to reach the nearest GND via of the ferrite bead. As the current looks up, it will see the floating planes above it. The return current will now flow as a combination of conduction and displacement current.

To understand the current path through the geometry with floating planes a simpler geometry (model) is created in HFSS. The model has 4 planes with one floating

plane. Top and bottom planes are full GND planes and middle ones are full PWR planes. Two PWR via are kept to simulate a two port geometry. For these two PWR vias, two GND (PWR return) vias are placed nearby. The size of the board is 4000 x 4000 mils and the cavity thickness is 2 mils. The GND vias are placed 50 mils away from the PWR vias. PWR via 2 and GND via 2 are shorted together. This is similar to that of the way the IC sit on the 28 layer board. Here the short models the IC connection.

Current through the stackup is now traced. Since there is a short at one side of the board, there is always a direct conduction current path through the geometry. But as the frequency increases, the current will also take other path looking for a path of least impedance. Therefore, in this case also the current will flow as a combination of conduction and displacement current. Figure 2.23 below shows the geometry under consideration and the figure 2.24 shows the current path. The displacement currents are shown in blue and the conduction currents are shown in red. It is difficult to visualize and conclude that the current will through the directions shown here by HFSS simulation. Therefore another approach was proposed to trace the current through the geometry.

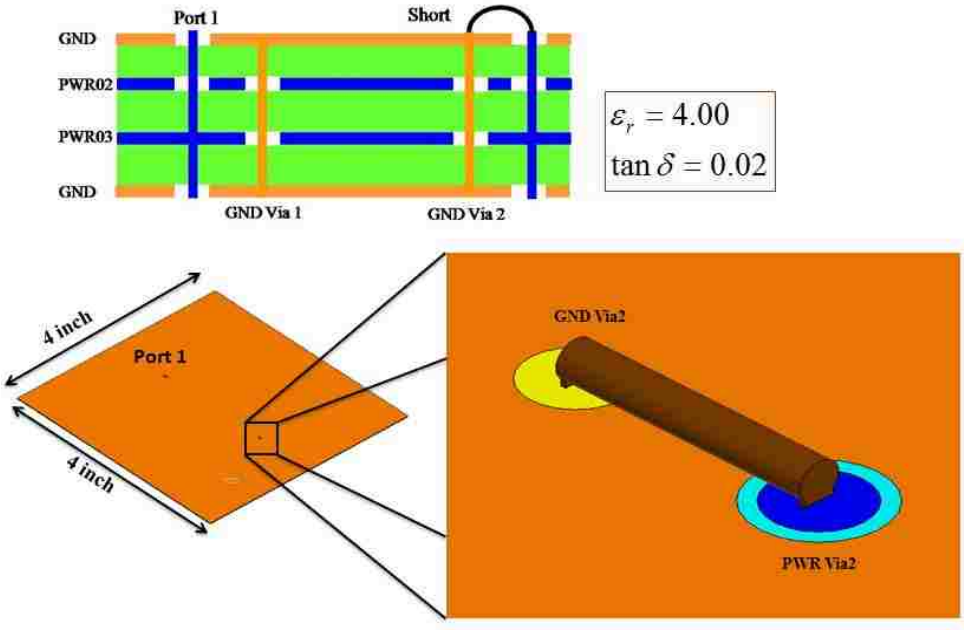

Figure 2. 23: 4 layer geometry with floating plane

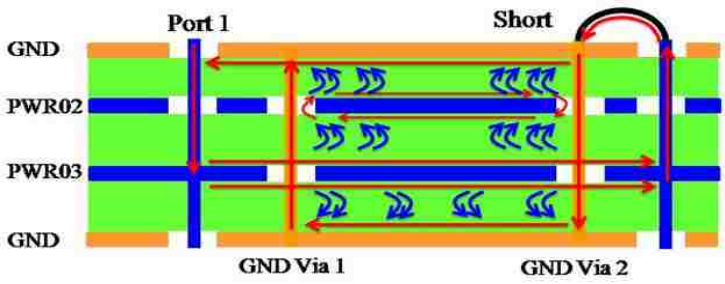

Figure 2. 24: Tracing current through 4 layer stackup

2.1.6. Circuit model using equivalent inductance method. From reference [2], the inductance associated with the vias penetrating PCB stackup can be calculated accurately. Equivalent inductance method can be used to study the PCB geometry with floating planes. If the self and the mutual inductance of the vias are calculated, then a simple physics based circuit model can be made to resemble the PCB stackup. Capacitance of the cavities can be found out from the parallel plate formula. Figure 2.25 shows the circuit model for the four layer stackup.

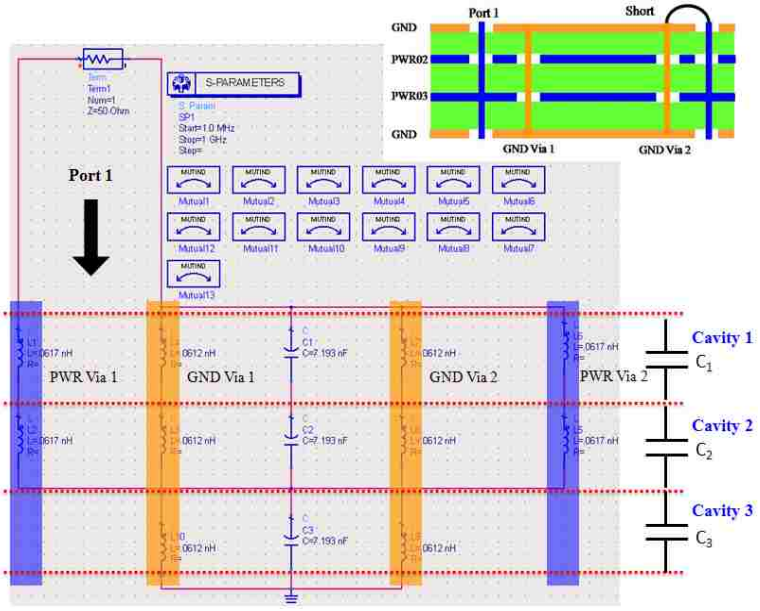

Figure 2. 25: Circuit model for 4 layer stackup

The inductance of the via is just a single value for each cavity. The method [2] takes into account the current flowing through the via, current necking down and spreading across the plane and lumps all the inductance associated with it into a single physics based inductance. The EZ Power Plane (EZPP) tool developed in MS&T uses this approach and gives the inductance values based on the text based input file with cavity information as shown in Figure 2.26. The input file for the four layer geometry is given below. The results of the circuit model simulation compared to the HFSS results are shown below in the Figure 2.27 and Figure 2.28.

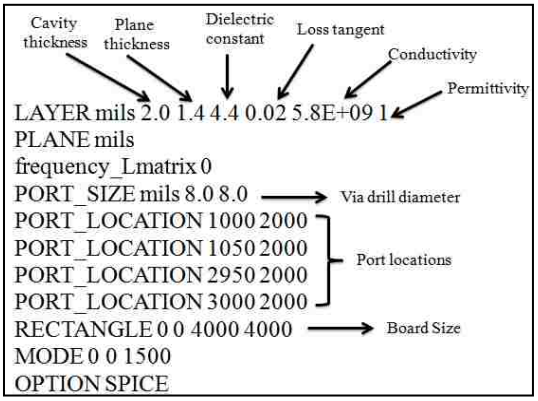

Figure 2. 26: EZPP sample input file

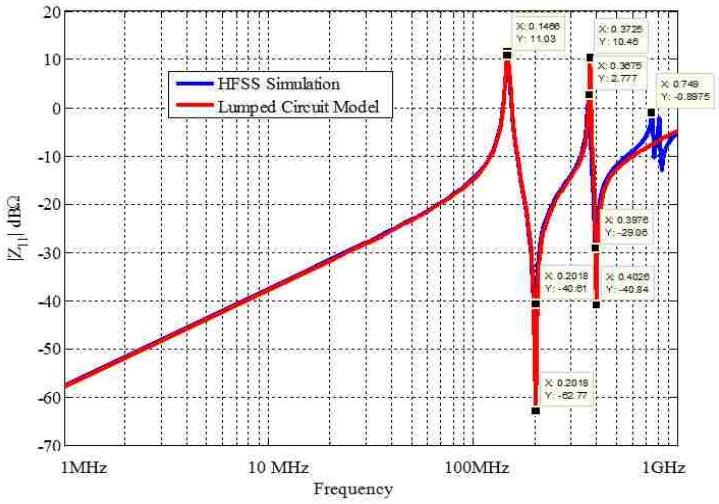

Figure 2. 27: Z_{11} magnitude comparison

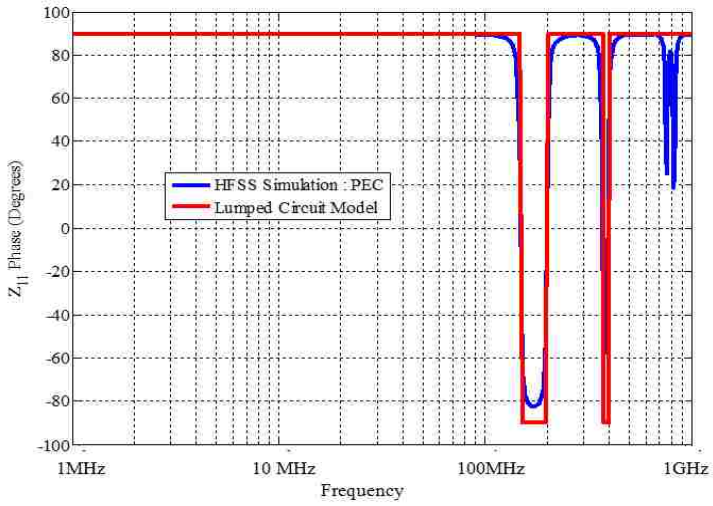

Figure 2. 28: Z_{11} phase comparison

The results show very good correlation with the HFSS results. The peaks and the nulls are perfectly matched. The Z_{11} magnitude is inductive in nature as there is a direct conduction path. As the correlation is good, it is possible to calculate the current through the geometry from the circuit model. Current probes are placed across the inductors and capacitors. The circuit models with current probes are shown in Figure 2.29.

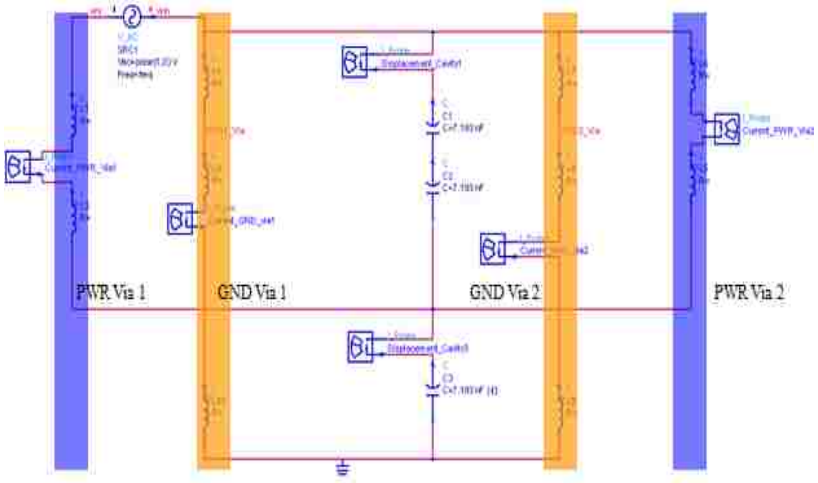

Figure 2. 29: Calculating current through stackup by circuit model

Once the current through the vias and the cavity are calculated, it is easy to analyze what inductance (L) and capacitance (C) causes the parallel and series resonance as seen from the Figure 2.30. Looking at the impedance profile, it is often the peaks that are causing the problem. It means that at these parallel resonance peaks, the impedance is very high and the current available for the IC switching is low. The 1st parallel LC resonance is shown below in Figure 2.30. The current through the inductors (blue path) and the current through the capacitance formed by the cavity 3 resonate at a particular frequency. The total current through the PWR via 2 decreases as the frequency increases and the displacement current through the cavity 3 increases. At a particular frequency they both cancel each other and the net current reduces. Here the impedance goes very large .The phase of the conductance current and displacement current are out of phase at that particular frequency.

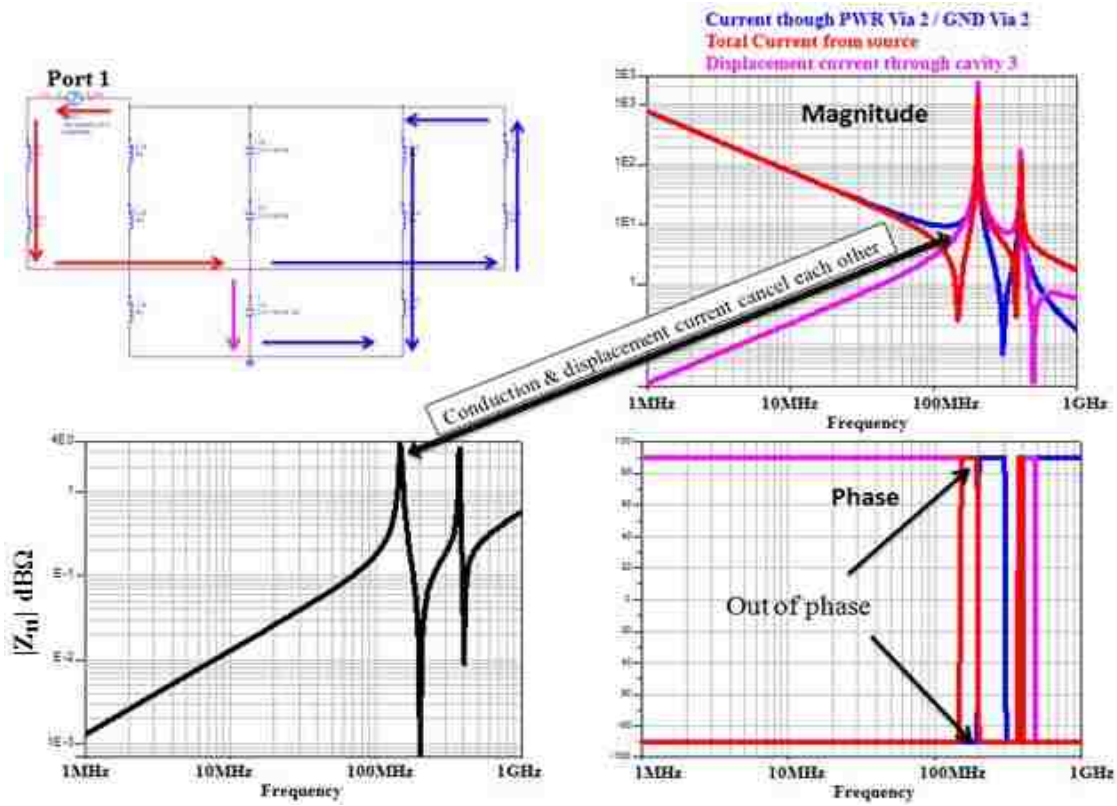

Figure 2. 30: 1st parallel resonance

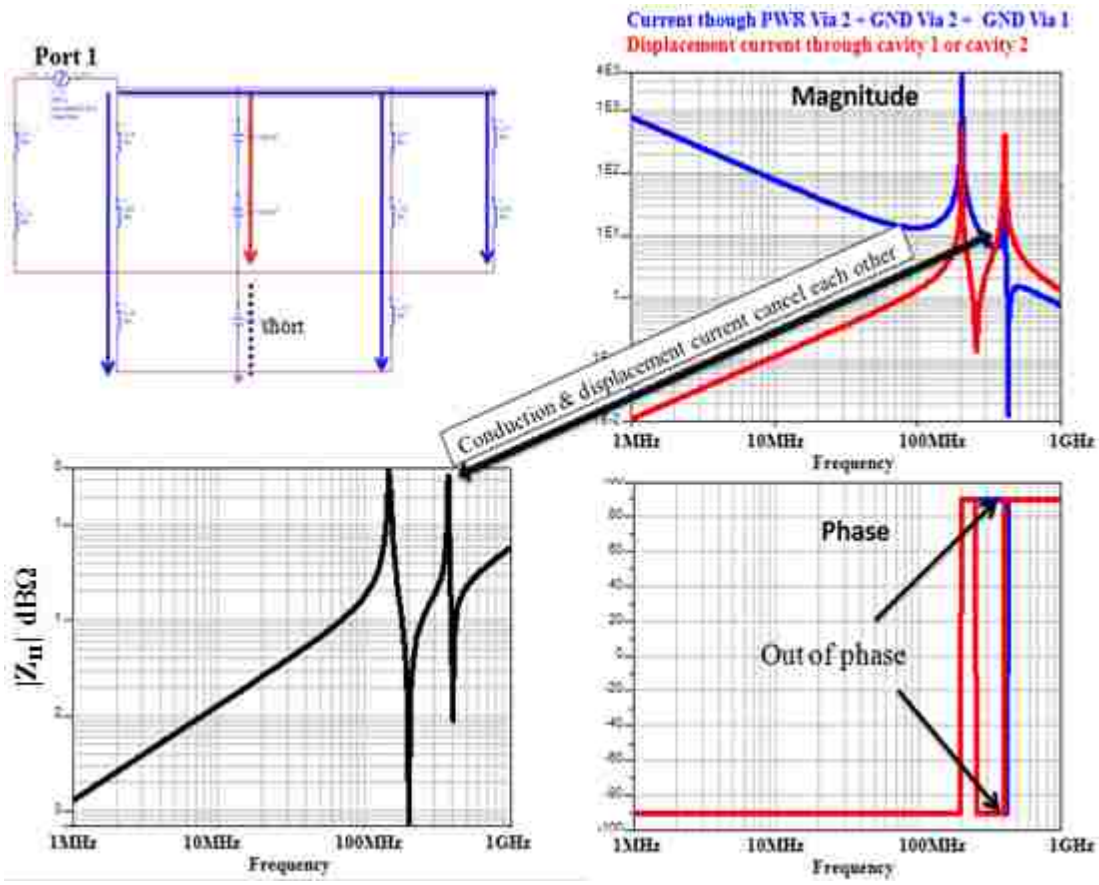

Figure 2. 31: 2nd parallel resonance

Similarly the 2nd parallel resonance can also be analyzed. The results from the circuit model are shown in Figure 2.31. For the 2nd parallel resonance the cavity 3 capacitance is shorted and the current through the cavities 1 and 2 increases. This approach can be now extended to the full geometry to analyze and study the current propagation through the stackup. Full planes can then be replaced with the complex area fills and the same process can be followed again.

2.2. CONCLUSIONS ON PDN MODELING AND DESIGN

The MVTT analytical formulation correlates very well with a 3D FEM solver with much faster solution. An understanding of current paths in multilayer PCBs with

multiple power and power return layers is being developed in conjunction with a physics based equivalent circuit model using the MVTT based on a full-wave formulation. The fundamental physics involves the tracing of the current paths. This helps to develop physical intuition and a relatively simple model that will include the critical currents. A physics based equivalent inductance method helps understanding of the current path in complex multilayer PCBs with multiple PWR and PWR return (GND) layers.

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[1] Zhenwei Yu, Jun Fan, Samuel Connor, Bruce Archambeault and James L. Drewniak, "Modeling of Noise Coupling inside Multilayer Printed Circuit Boards Using Cavity Model and Segmentation Technique", 2010 Asia-Pacific Symposium on Electromagnetic Compatibility, 12-16 April, 2010 Beijing.

[2] J. Kim, J. Kim, L. Ren, J. Fan, J. Kim, and J. L. Drewniak, “Extraction of equivalent inductance in package- PCB hierarchical power distribution network”, in *Proc. of 2009 IEEE 18th Conference on Electrical Performance of Electronic Packaging and Systems*, pp 109-112, Oct. 2009.

VITA

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