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VIA TRANSITION MODELING AND CHARGE REPLENISHMENT OF THE

POWER DELIVERY NETWORK IN MULTILAYER PCBs

by

MATTEO COCCHINI

A THESIS

Presented to the Faculty of the Graduate School of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

2008

Approved by

James L. Drewniak, Advisor
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Daryl Beetner

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PUBLICATION THESIS OPTION

This thesis consists of the following five articles that have been published or submitted for publication as follows:

Pages 1-16 have been published in the IEEE International Symposium on EMC, pp. 1–6, Honolulu, Hawaii, July 2007

Pages 17-29 have been accepted for publication to the 2008 IEEE EMC Detroit Symposium

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Pages 41-71 have been published in the Proceedings of Design Conference East, Santa Clara, CA, Feb 2007

Pages 72-85 are intended for submission to the 2008 IEEE EMC Detroit Symposium

ABSTRACT

In the first article of this thesis, the charge delivery in the power distribution network for printed circuit board has been analyzed in the time-domain. Performing all the simulations and analyzing the PDN physics and modeling, I contributed to a better understanding of the time-domain decoupling mechanism.

The second paper studies the noise coupling sing a segmentation approach combined with a via-to-antipad capacitance model and a plane-pair cavity model. Building equivalent circuit models as well as analyzing design strategies, I contributed to a new approach for the PDN analysis in multilayer PCBs.

The third article discusses how to estimate the amount of current needed for large ICs and how to evaluate the amount of noise voltage due to this current draw. After accurate discussion of the design strategies, I modeled and simulated the free evolution of a charged PCB with and without decoupling capacitors.

The depletion of charges stored between the power buses in time and frequency-domain has been investigated as a function of the plane thickness, SMT decoupling closeness in the fourth paper. With my contribution, the time and frequency-domain in the PDN have been related using circuit approach.

In the fifth paper, I analyzed a 26-layer printed circuit board performing milling, measurements and building circuit models. It is the first time that the segmentation approach has been used for differential geometry. In addition, Debye materials have been implemented in the cavity model.

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1. EARLY TIME CHARGE REPLENISHMENT OF THE POWER DELIVERY NETWORK IN MULTI-LAYER PCBS

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1.1. ABSTRACT

The investigation of decoupling issues has been extensively treated in the literature in both the frequency and the time domain [1-9]. The two domains describe from different perspectives the same physical phenomenon, being related by a Fourier transform. In this article, well known decoupling issues usually addressed in the frequency domain [1,2] are discussed in the time domain. Moreover, some modeling issues related to the cavity model approach are discussed and, in particular, the circuit extraction feature associated with this methodology is utilized throughout the article to carry out the time domain simulations within a SPICE based-tool. The depletion of charges stored between the power bus is investigated in the time domain as a function of the plane thickness, SMT decoupling closeness and interconnect inductance values.

Keywords

Decoupling Issues, Power Delivery Network, Charge Depletion, Cavity Model

1.2. INTRODUCTION

Understanding decoupling issues in both the frequency and the time domain is important for effective design of the power distribution network for printed circuit boards (PCB) for high-speed signaling. Many contributions can be found in the literature [1-9] dealing with PDN decoupling aspects to ensure the functionality of PCB systems.

Different schools of thoughts exist regarding the utilization of decoupling capacitors, typically in terms of a target impedance of the power/ground plane pair (power bus). The ability to perform circuit extraction when describing the power bus in terms of cavity modes [10-17] is used in this paper to investigate these issues mainly in the time domain by means of SPICE-based tools. Firstly, a couple of modeling problems are discussed in order to explain some intricacies associated with the circuit models and the choice of the observation points. Then, well known decoupling, issues that are usually addressed in the frequency domain, are investigated in the time domain. Design tips and conclusions drawn are consistent regardless of whether frequency or time domains are examined [1,2].

1.3. MODELING ISSUES AND IMPLEMENTATION

The circuit extraction feature of the cavity model approach [10-17] can be utilized to model the power delivery network. The circuit models extracted are run in a SPICE-based tool allowing for the possibility to investigate the same issues from a time domain prospective. The circuit interpretation of the cavity model approach is given below:

$$Z_{ij} = \frac{1}{j\omega C_p} + \sum_{n=0}^{N}\sum_{m=0}^{M} \frac{N_{nmi}N_{nmj}}{\underset{n=m\neq 0}{j\omega C_p + \frac{1}{j\omega L_{nm}} + G_{nm}}} + j\omega L_{ij}^{HM} \quad (1)$$

is divided into three terms. The first term corresponds to the interplane capacitance of the plane pair. It represents the impedance of the board at low frequencies, i.e., when the impedance declines at -20 dB/dec. The third term is the higher order interconnect inductance. This term comprises all the contributions of the modes, whose resonant frequencies fall above the maximum frequency of interest. It is well- known that each resonant mode can described in terms of an equivalent R-L-C parallel circuit [11-14]. Hence, all the inductive contributions of those higher order modes are grouped together to create the inductive behavior. Also, this inductance resonates with the interplane capacitance creating the characteristic first dip seen in any self-impedance profile. If no additional terms were to be considered in the impedance formula, a characteristic

impedance rise of 20 dB/dec would be observed in the self-impedance profile at higher frequencies. The second term of the summation consists of a double summation of all the resonant modes considered for the board geometry. The maximum number of those modes for each propagating direction is chosen according to the formulas provided in [12-13]. All these modes superimpose their characteristic R-L-C behavior on top of the underlying $j\omega L_{ij}$ behavior as the frequency is increased. Figure 1.1 illustrates the equivalent circuit realized by equation (1).

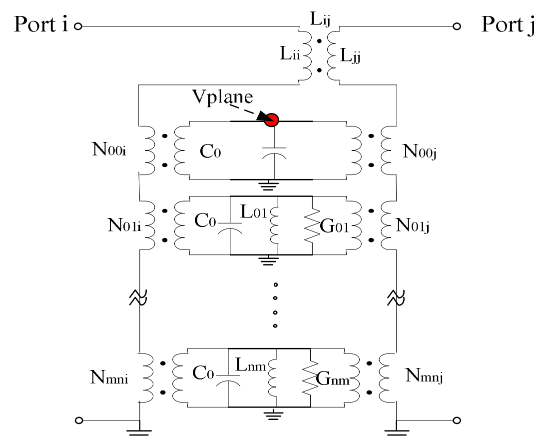

Figure 1.1. Equivalent circuit model corresponding to (1).

The original summation of equation (1) consists of a double infinite summation, which is replaced by two finite N by M summations and the inductive term. The inductive term is obtained as the number which the double infinite summations converges, once the N by M terms - still explicitly present in the formulation (1) - are subtracted from it.

Further considerations need to be added regarding the investigation of decoupling issues in the time domain and in particular the charge depletion of the planes. As a repetitive triangular current waveform is drawn from a given location on the board, the sagging of the voltage is observed at the node specified in Figure 1.1 as Vplane. By placing a current source at Port i and leaving Port j open, the voltage observed at the driver port, or Port i, corresponds to the summation of all the voltage drops observed across the higher order mode inductance L_{ii}, the capacitance of the plane C_0 and all the R-L-C circuits associated with the resonant modes, coupled to the driver Port i by means of

the ideal transformers N_{mni}. The quantity of interest is the voltage sag as a function of the charge depleted from the planes by the current drawn at the driver location, or Port i. Hence, the voltage, which is monitored and correlated to the amount of charge associated with the triangular current pulse, is the one specified in Figure 1.1 as Vplane.

An alternative representation of the power delivery network, other than the equivalent circuit model shown in Figure 1.1, would not allow monitoring the voltage Vplane and relate its decrease the amount of charge depleted from the planes themselves.

The effectiveness of a decoupling capacitor is an important issue when designing a decoupled power bus. Often, effectiveness is defined as the ability to lower the power bus impedance. From studies in the frequency domain, this effectiveness is determined as a function of two frequency independent parameters [2,6], the coefficient of mutual coupling k and the ratio of the interconnect inductance above the plane over the interconnect inductance below the planes L_3/L_2. The coefficient of mutual coupling quantifies the amount of magnetic energy coupled between an IC-pin via and the connection via of a decoupling capacitor [2,6,8]. The farther away the capacitor via from the IC via, the lower the local decoupling effectiveness, the closer the k to zero. It is also desirable to have the ratio of the inductance above the plane over the inductance below the plane to be smaller than one when the mutual coupling coefficient is much larger than zero, in order to benefit from local decoupling effects [2,6]. This is usually achievable when the plane pair is thick, i.e., 35 mils plane spacing, and the interconnect inductance above the planes is minimized by choosing the decoupling capacitors with low ESL and properly designing the decoupling capacitor pads on the top or bottom sides of the PCB.

Finally, the two frequency independent quantities can be grouped into the formula (2) [6], which quantifies the reduction, namely $|Z_{deacrease(dB)}|$, of the impedance.

$$\left|Z_{decrease(dB)}\right| = \left|20\log_{10}\left(\frac{(1-k)+\left(\frac{L_3}{L_2}\right)}{1+\left(\frac{L_3}{L_2}\right)}\right)\right| \tag{2}$$

1.4. TIME DOMAIN BEHAVIOR – EARLY TIME

The equivalent circuit models extracted by means of the cavity model approach are used in this article to perform the investigation of power delivery issues as a function of various parameters such as decoupling capacitor distance and inductance above the planes. The inductance above the plane is varied in a range between 0.5 nH and 3 nH to observe the variations in the voltage noise excited between the power planes. On the other hand, the decoupling capacitor distance form Port 2, i.e., the point at which the current is drawn, is varied in a range between 50 mils to 5000 mils in order to observe the effects of the distance in reducing or increasing the power bus noise voltage. The two layer board of interest is shown in Figure 1.2.

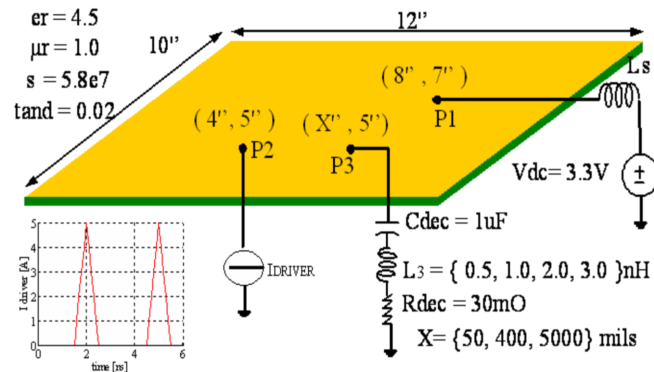

Figure 1.2. Geometry under test and triangular current waveform source connected at Port 2

A constant DC voltage is connected at Port 1 through a interconnect inductance L_s of 50nH, a periodic triangular current waveform of 500 ps rise time and 3 ns repetition , also shown in Figure 1.2, is hooked up at Port 2 in order to draw charges at a given rate and observe the PDN reaction to this disturbance. Also, a 1 μF decoupling capacitor with 30Ω ESR and a variable L_3 is connected to Port 3, whose location is at a variable distance along the x direction from the driver, i.e., 50, 400, and 5000 mils. The peak value of the current waveform is chosen to be 5 A so that every cycle approximately 20% of the overall plane charge is drawn from the driver. Finally, two values of plane separation are chosen, i.e., 35 and 10 mils.

A first comparison between the two aforementioned configurations is shown in Figure 1.3 and Figure 1.4. The current waveform of Figure 1.2 is applied at Port 2 and the interconnect inductance of the decoupling capacitor, located 400 mils away from the driver, is varied in the following range, i.e., 0.5 nH, 1 nH, 2 nH, and 3 nH.

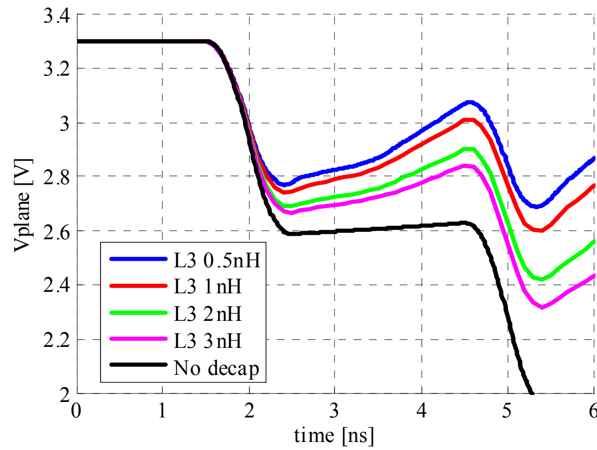

Figure 1.3. Configuration with 35 mils plane separation and decoupling capacitor 400 mils away from the driver.

It is important to observe that the time domain results agree with the frequency domain expectations [2,6] associated with the two configurations considered. The plane voltage reported in Figure 1.3 and Figure 1.4 is associated with the voltage across the plane capacitance, as indicated in Figure 1.1. By relating circuit models to the geometry, each point on the board would experience this voltage sag and each point would also have additional voltage terms associated with their positions with respect to the spatial variation of the resonant modes. Hence, the Vplane is the first order approximation of the voltage variation observed at any location. The reduction in the voltage sag observed in Figure 1.3 as a function of the decoupling capacitor interconnect inductance can be explained in terms of the impedance decrease formula given in equation (2) [2,6,8]. Since the distance between the decoupling capacitor and the driver is constant for all the four different cases, the only variable in equation (2) is the ratio between the inductance above the plane L_3 and L_2 which is constant for all the cases. As the L_3 is increased becoming

the dominant factor, the L_3/L_2 ratio also increases. Hence, the impedance-decrease factor is reduced or, the voltage swing is increased. This is true when examining results in the frequency domain, or in the time domain. The plane voltage sag lowers the plane voltage during the time when the current draw is increasing. During the time in which the current draw decreases, the plane voltage increases, but it doesn't return to the level at which it started, i.e., 3.3 V. Hence, when the second current pulse begins, the plane voltage sags again and later in the current cycle, when the current draw decreases, again, the voltage rises, but it cannot reach the value it had achieved after the first triangular pulse. This phenomenon reflects the physics of charge replenishment, or lack thereof in this case. The decoupling capacitor is not able to respond quick enough to meet the charge demand from the driver.

The negligible reduction in the voltage sag associated with the 10 mils configuration as a function of the decoupling interconnect inductance can also be explained in terms of equation (2). The mutual coupling coefficient k is the same as the 35 mils case. However, the value of L_2 is 3.5 time smaller, hence the ratio of L_3/L_2 is 3.5 time larger, making this term the dominant one in equation (2).

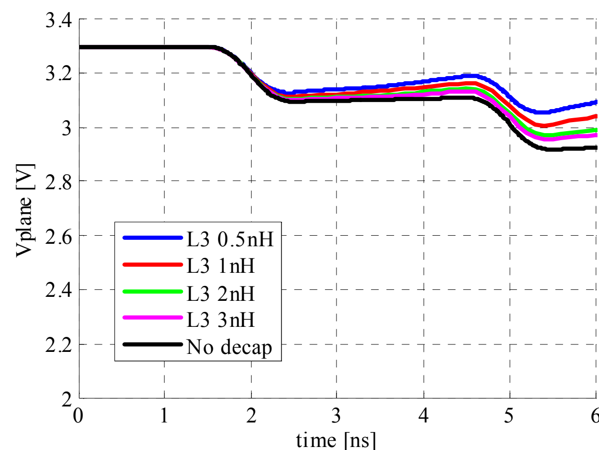

Figure 1.4. Configuration with 10 mils plane separation and decoupling capacitor 400 mils away from the driver.

The overall difference in the voltage swing observed when comparing the curves in Figure 1.3 and Figure 1.4 is also explained by considering that the interplane capacitance of the 10 mils case is also 3.5 larger than the interplane capacitance of the 35 mils case. Hence, the thin configuration is more effective in terms of decoupling by supporting the same amount of charge draw with a smaller voltage sag. Two additional comparisons of the decoupling capacitor effectiveness, as a function of the distance of the decoupling capacitor itself to the driver, are given in Figure 1.5 and Figure 1.6, for the 35 mils case and the 10 mils case, respectively. The reduction in the voltage sag in Figure 1.5 can be again explained in terms of equation (2) [2,6,8]. As the decoupling capacitor is moved far away from the driver, the coupling coefficient k decreases, making equation (2) in value close to one.

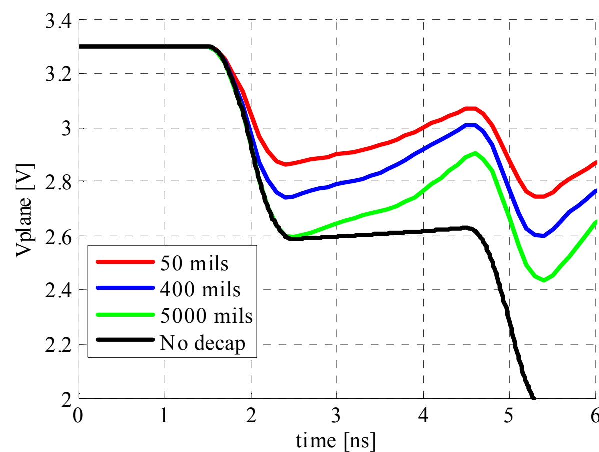

Figure 1.5. Plane separation 35 mils and 1nH decoupling capacitor interconnect inductance

This effect is less important, hence the location of the decoupling capacitors with respect to the driver, is less important when considering thin parallel plane pair, as shown in Figure 1.6. As already mentioned in the previous paragraph, when reducing the plane separation from 35 mils down to 10 mils, the coupling coefficient is reduced of about 3.5 times and the plane capacitance is increased accordingly. Hence, the voltage swing is not significantly affected by the physics described in equation (2) and the overall voltage

level is higher since the plane can provide the same amount of charges with a smaller voltage sag.

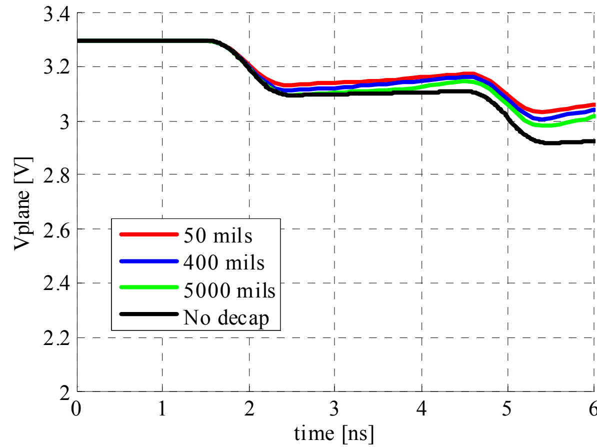

Figure 1.6. Plane separation 10 mils and 1nH decoupling capacitor interconnect inductance

The values associated with the two frequency independent quantities constituting equation (2), i.e., the coupling coefficient k and the ratio of inductances L_3/L_2 are reported in Table 1.1, Table 1.2 , Table 1.3 and Table 1.4 and for all the curves shown in Figure 1.3, Figure 1.4, Figure 1.5 and Figure 1.6. The value of the $|Z_{decrease}|$ is also shown in the two tables and it is possible to devise the correlation described in the previous paragraphs between the curves in the aforementioned plots and the values obtained from equation (2) [6].

Table 1.1. k, L_3/L_2 and $|Z_{decrease(dB)}|$ factor for the curves in Figure 1.3

35 mils L_2 = 1.0nH & k = 0.38 @ 400 mil		
L_3 = 0.5nH	L_3/L_2 = 0.5	$|Z_{decrease(dB)}|$ = 2.62
L_3 = 1.0nH	L_3/L_2 = 1.0	$|Z_{decrease(dB)}|$ = 1.83
L_3 = 2.0nH	L_3/L_2 = 2.0	$|Z_{decrease(dB)}|$ = 1.21
L_3 = 3.0nH	L_3/L_2 = 3.0	$|Z_{decrease(dB)}|$ = 0.92

Table 1.2. k, L_3/L_2 and $|Z_{decrease(dB)}|$ factor for the curves in Figure 1.4.

10 mils L_2 = 0.28nH & k = 0.38 @ 400 mil		
L_3 = 0.5nH	L_3/L_2 = 1.78	$\|Z_{decrease(dB)}\|$ = 1.31
L_3 = 1.0nH	L_3/L_2 = 3.5	$\|Z_{decrease(dB)}\|$ = 0.82
L_3 = 2.0nH	L_3/L_2 = 7.1	$\|Z_{decrease(dB)}\|$ = 0.45
L_3 = 3.0nH	L_3/L_2 = 10	$\|Z_{decrease(dB)}\|$ = 0.25

Table 1.3. k, L_3/L_2 and $|Z_{decrease(dB)}|$ factor for the curves in Figure 1.5.

35 mils - L_3 = 1.0nH & L_2 = 1.0nH (~ same for all cases)			
50 mils	L_3/L_2 = 1.0	k = 0.74	$\|Z_{decrease(dB)}\|$ = 4.00
400 mils	L_3/L_2 = 1.0	k = 0.38	$\|Z_{decrease(dB)}\|$ = 1.83
5000 mils	L_3/L_2 = 1.0	k = 0.09	$\|Z_{decrease(dB)}\|$ = 0.45

Table 1.4. k, L_3/L_2 and $|Z_{decrease(dB)}|$ factor for the curves in Figure 1.6.

10 mils - L_3 = 1.0nH & L_2 = 0.28nH (~ same for all cases)			
50 mils	L_3/L_2 = 3.5	k = 0.74	$\|Z_{decrease(dB)}\|$ = 1.51
400 mils	L_3/L_2 = 3.5	k = 0.38	$\|Z_{decrease(dB)}\|$ = 0.82
5000 mils	L_3/L_2 = 3.5	k = 0.09	$\|Z_{decrease(dB)}\|$ = 0.18

Four additional comparisons are finally presented in Figure 1.7 and Figure 1.8 in the timed domain and in Figure 1.9 and Figure 1.10 and in the frequency domain. A 400 mils radius ring of eight capacitors centered around the driver is compared against a single capacitor, 8 times larger also 400 mils away from the driver along one direction.

The conclusions to be drawn when comparing each set of curves within each plot is that the ring of decoupling capacitor acts by improving the speed of charge delivery from the capacitors themselves to the plane, where the voltage across the plane starts sagging. It is also seen, by comparing Figure 1.7 and Figure 1.8, that the value of decoupling capacitor is not important in the very early instants of time during the plane charge depletion. An array of decoupling capacitors, presenting a lower interconnect inductance, is superior to a single capacitor of much greater value.

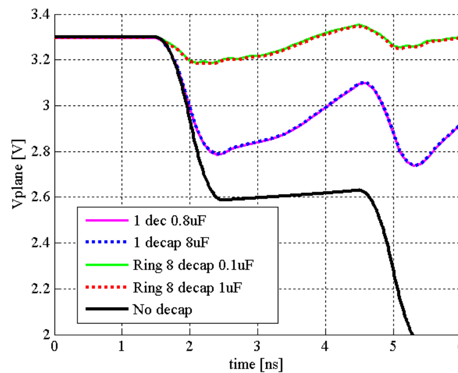

Figure 1.7. Early instants of time comparison between a ring of eight 0.1 μF decoupling capacitor 400 mils away from the driver *vs.* a single 0.8 μF decoupling capacitor at 400 mils away from the driver (L_3 = 0.5 nH and ESR 30 mΩ) and a ring of eight 1μF decoupling capacitor 400 mils away from the driver *vs.* single 8uF decoupling capacitor at 400 mils away from the driver for a 35 mils plane separation (L_3 = 0.5 nH and ESR 30mΩ)

There is a definitive improvement when compared with the case of no decoupling, but also the improvement with respect to the single capacitor is remarkable and it amount to approximately 400mV in the case of 35 mils. The smaller voltage swing associated with the 10 mils cases is again explained by considering that the interplane capacitance is 3.5 times higher.

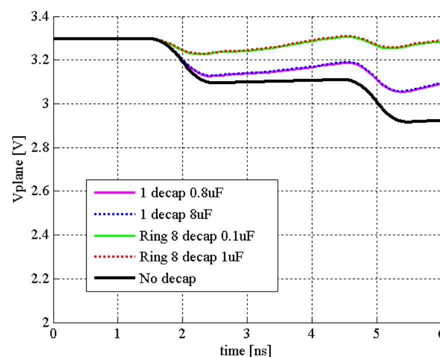

Figure 1.8. Early instants of time comparison between a ring of eight 0.1 μF decoupling capacitor 400 mils away from the driver *vs.* a single 0.8 μF decoupling capacitor at 400 mils away from the driver (L_3 = 0.5 nH and ESR 30 mΩ) and a ring of eight 1 μF decoupling capacitor 400 mils away from the driver *vs.* a single 8 μF decoupling capacitor at 400 mils away from the driver for 10 mils plane separation (L_3 = 0.5 nH and ESR 30mΩ).

This rationale is also confirmed by looking at the frequency domain plots given Figure 1.9 and Figure 1.10 corresponding to the time domain graphs of Figure 1.7 and Figure 1.8, respectively. First of all, the self-impedance observed across the driver port, when the plane separation is 35 mils, is approximately 10 dB higher with respect to the 10 mils case above approximately 50 MHz. This improvement is well documented in the literature [1-9] and also confirmed by the timed domain simulations presented in the previous paragraph. Also, above 20-30 MHz, both graphs confirm the greater importance of the interconnect inductance over the values of the decoupling capacitance utilized. The two ring configurations as well as the single decoupling configurations exhibit the same frequency domain behavior, respectively, in both the 35 mils case and the 10 mils case.

It is important to note that different nodes are monitored when the pair of curves given in Figure 1.7 and Figure 1.8 and the pair of curves shown in Figure 1.9 and Figure 1.10 are obtained. In fact, the time domain curves were observed at the node Vplane shown in Figure 1.1. This node provides a first order approximation of the plane voltage noise and it is not affected by the $L_{ii}di/dt$ voltage drop, which is large compared to the one across the plane in the configuration of Figure 1.2. On the other hand, the input impedance plots were both observed from Port 2, or the driver port, hence the port inductance is considered and it prevails at higher frequencies. This is the reason why the self impedance in both the cases of the ring of decoupling capacitors and the single decoupling capacitor exhibits the same impedance behavior above 100 MHz, while the plots of early instants of time show significant differences. The difference between the ring and the single capacitors is more visible in the range between 10 MHz and approximately 100 MHz, where the effect of the interconnect inductance of the decoupling capacitors play a role in reducing the plane impedance.

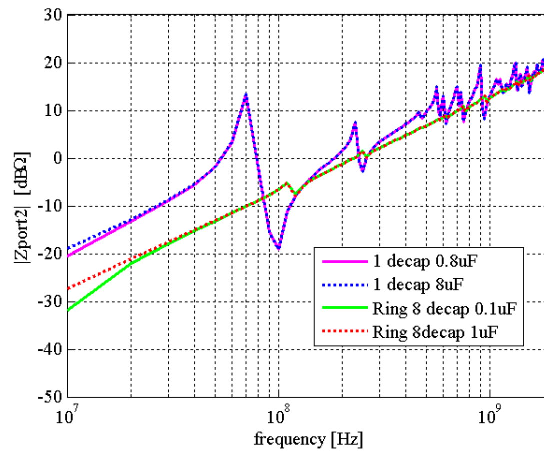

Figure 1.9. Frequency domain comparison between a ring of eight 0.1 μF decoupling capacitor 400 mils away from the driver *vs.* a single 0.8 μF decoupling capacitor at 400 mils away from the driver (L_3 = 0.5 nH and ESR 30 mΩ) and a ring of eight 1 μF decoupling capacitor 400 mils away from the driver *vs.* single 8 μF decoupling capacitor at 400 mils away from the driver for a 35 mils plane separation (L_3 = 0.5 nH and ESR 30mΩ).

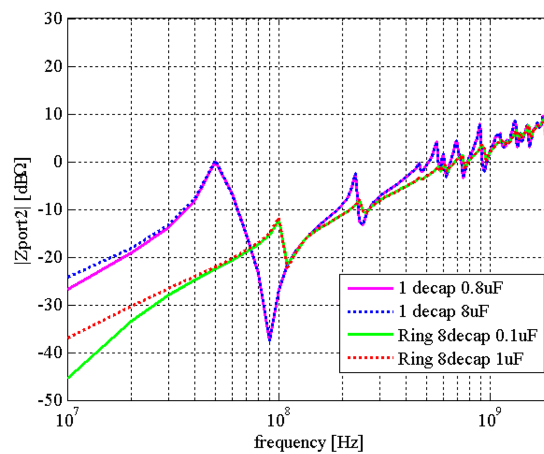

Figure 1.10. Frequency domain comparison between a ring of eight 0.1 μF decoupling capacitor 400 mils away from the driver *vs.* a single 0.8 μF decoupling capacitor at 400 mils away from the driver (L_3 = 0.5 nH and ESR 30 mΩ) and a ring of eight 1 μF decoupling capacitor 400 mils away from the driver *vs.* a single 8 μF decoupling capacitor at 400 mils away from the driver for 10 mils plane separation (L_3 = 0.5 nH and ESR 30mΩ).

1.5. CONCLUSIONS

Modeling problems issues, as well as, some important design issues are in this paper. In particular, it is been shown the importance of the higher order mode self and mutual inductances, which are crucial parameters to represent correctly when dealing with decoupling issues. A reduction in the impedance, in the frequency domain, or a reduction in the voltage swing, in the time domain can be achieved for some PDN designs by placing the decoupling capacitors close to the drivers and minimizing their interconnect inductance. The PDN associated with thin power planes, i.e., 10 mil and below, are not significantly affected by the decoupling placement as shown in the time domain plots given in the previous paragraph. It is very interesting to note that the value of the decoupling capacitors themselves do not make a difference in the early instants of time. In this time frame, it is of more importance achieving a configuration with a low parasitic interconnect inductance rather than increasing the value of decoupling capacitors.

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2. NOISE COUPLING BETWEEN SIGNAL AND POWER/GROUND NETS DUE TO SIGNAL VIAS TRANSITIONING THROUGH POWER/GROUND PLANE PAIR

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2.1. ABSTRACT

Signal vias are often used to move a signal from one PCB layer to another. As a result, these vias can penetrate power/ground plane pair and cause noise coupling (crosstalk) between signal and power/ground nets. This paper studies the noise coupling mechanism using a segmentation approach combined with a via capacitance model and a plane-pair cavity model. Noise coupling from signal to power/ground, and vice versa, is demonstrated in the modeling results.

Keywords: Differential signal, noise coupling, signal and power/ground nets, signal via transition, via capacitance, cavity model, ground vias.

2.2. INTRODUCTION

In modern multi-layer printed circuit boards (PCBs), signal vias are extensively used to route signals from one layer to another. The high density and small package size of today's high-speed integrate circuits (ICs) force signal nets to be routed on multiple layers to facilitate access to all the pins/balls in the device's dense pin field. Further, the number of layers can be a big factor in PCB cost. By transitioning signals among multiple layers PCB real estate may be used more efficiently, possibly reducing the number of signal layers required in the PCB.

Vias used for signal layer transitions are likely to penetrate one or more power and/or ground planes, Power/ground plane pair are commonly used in multi-layer high-speed PCB designs as a power distribution network. Previous work found the signal penetration through power and ground plane pair was a mechanism that can result in power bus noise, in addition to the more commonly understood simultaneous switching noise (SSN)[1-2].

This noise coupling phenomenon can be explained using the return current for the signal penetrating the power and ground plane pair. Even if there are many decoupling capacitors placed between the power and ground plane pair, not all the return current will take the capacitor paths because of the interconnect inductance associated with these decoupling capacitors. A portion of the return current will jump between the planes in the form of a displacement current, and hence excite the power and ground plane pair. The same phenomenon can occur between two power planes with different logic levels.

The noise coupling mechanism described above works in the reverse as well. A signal via transitioning through a power and ground plane pair can pick up the noise in the power and ground planes that may be caused by other mechanisms such as SSN. The noise from the power and ground planes may affect the integrity (quality) of the high-speed signal that propagates through the via.

This paper studies the noise coupling problems between the signal and power/ground nets due to via transition, using a segmentation method combined with a via capacitance model and a plane-pair cavity model. Section 2 introduces the modeling approach, while two typical coupling cases are modeled and discussed in Sections 3 and 4.

2.3. MODELING APPROACH

The modeling approach used in this paper is based on the segmentation method [3]. First, the entire geometry is divided into multiple blocks. Then, each block is modeled using an equivalent circuit model. All the blocks are finally connected together by enforcing the current and voltage continuity conditions. This approach has many advantages over the traditional full-wave modeling approaches. It extracts an equivalent circuit model that is physics-based, so that geometry features are linked with circuit

parameters for meaningful engineering design and optimization. The equivalent circuit allows the further integration of the model with other circuit components such as decoupling capacitors and IC devices, and it can be run in both the frequency and time domains. Compared to the full-wave methods, this approach is very fast and efficient. It can handle tens of plane pair and hundreds of vias, which can be the case in practical PCB designs.

The entire PCB geometry is divided at the middle of every power or ground plane. The underlying reasoning for this is that only the TEM mode exists in the anti-pad regions that are coaxial structures in the frequency range of interest. Thus well-defined voltages and currents exist at every interface between the blocks. Figure 2.1 illustrates a typical block except the top and bottom ones that are often microstrip structures. As clearly shown in Figure 2.1(a), the geometry of every block includes a pair of planes and multiple via portions that may or may not be connected to the planes. The corresponding equivalent circuit model is shown in Figure 2.1(b), where a capacitor exists between a via portion and a plane if the via portion is not connected to the plane. The capacitance values can be calculated using a quasi-static EM tool or a closed-form expression [4]. The pair of the planes is modeled as a multi-port impedance matrix that is obtained using a cavity method [5]. The inductances associated with the via portions including the mutual ones are accounted for in the impedance matrix, as well as the dimension-dependent distributed behaviors of the plane pair.

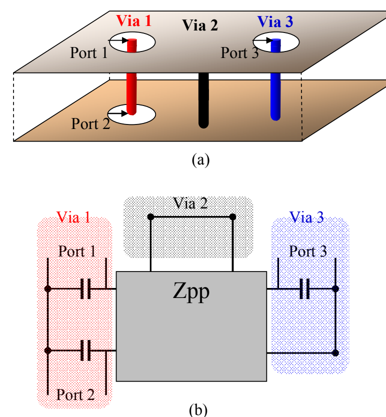

Figure 2.1. A typical building block.

Trace/via transitions, including both microstrip/via and stripline/via transitions, can be combined with the fundamental blocks, as well as other circuit components such as decoupling capacitors and IC devices. This segmentation approach combined with the via capacitance model and the plane-pair cavity model has been validated to be effective and efficient for common PCB structures [4, 6].

2.4. NOISE COUPLING FROM SIGNAL TO POWER/GROUND

The approach was first applied to study the noise coupling from signal to power/ground nets. The test geometry is shown in Figure 2.2. It includes a multi-layer printed circuit board and a signal via transitioning a signal from the microstrip line on the top to another microstrip line on the bottom of the board. The printed circuit board has four solid planes for power supply and current return (ground planes). The signal via penetrates all the four planes.

The dimensions of the printed circuit board are 14″×10″, and the two 50 Ω microstrip lines are both 5″ long. All the dielectric layers are assumed to have a dielectric constant of 4.5, and a loss tangent of 0.02. The signal via is located at (6″, 4″) from the left bottom corner of the board, and the via radius is 11 mils. Two ports (Ports 3 and 4) between the two middle planes are chosen to monitor the noise coupled from the signal via. Ports 1 and 2 are located at the end of the top and bottom microstrip traces, respectively.

The equivalent circuit model for the test geometry was extracted using the previously introduced segmentation approach, and is shown in Figure 2.3. Notice that the middle plane pair is modeled as a three port impedance matrix, where one port is at the signal via and the other two are at the two observation ports.

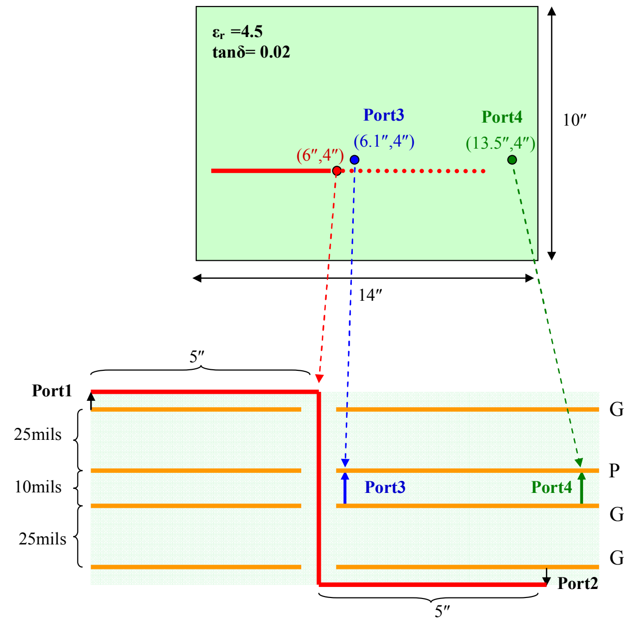

Figure 2.2. Test geometry to study noise coupling from signal to power/ground nets.

The circuit model is first investigated in the frequency domain, and the modeled S-parameters among Ports 1, 2, 3, and 4 are shown in Figure 2.4. The $|S_{21}|$, which indicates the transmission of the signal from the top microstrip line to the bottom one, is close to 0 dB up to approximately 1 GHz. The signal can be effectively transmitted with a very small loss. The $|S_{21}|$ starts to decrease rapidly from 1 GHz due to both the dielectric and skin-effect losses.

The $|S_{31}|$ and $|S_{41}|$ reflect the noise coupling at Ports 3 and 4 from Port 1, respectively. At most of the frequencies, the magnitude of these two transfer functions ranges from -60 to -30 dB. If the signal voltage at Port 1 is strong enough, a relatively high noise voltage at Ports 3 and 4 due to the signal via transition could be generated. This is consistent with the previous work reported in [1-2].

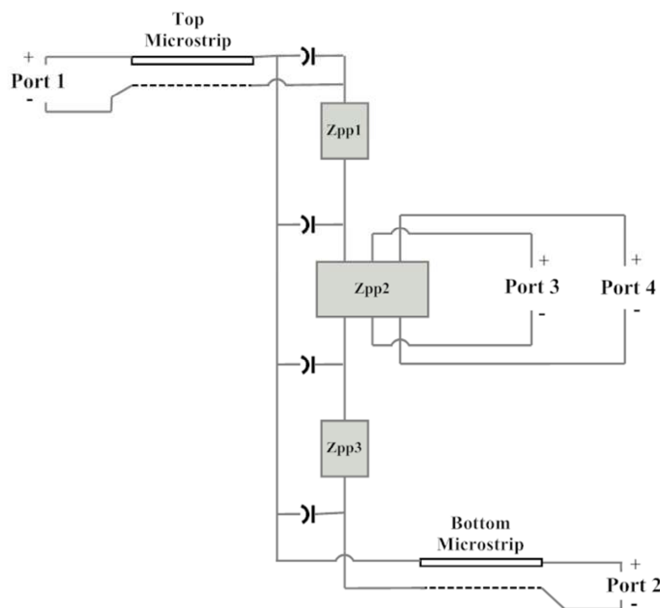

Figure 2.3. Equivalent circuit model for the test geometry shown in Figure 2.2.

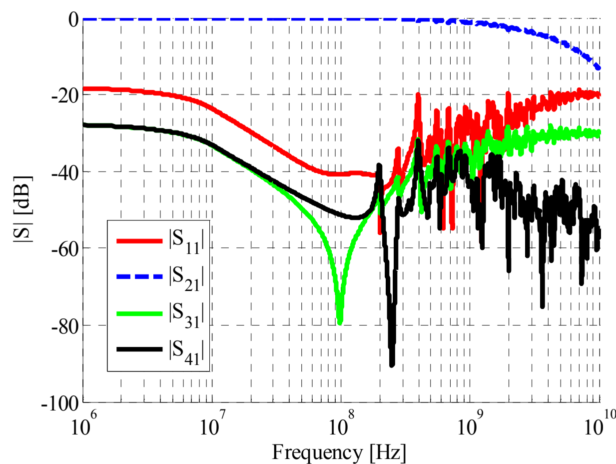

Figure 2.4. Frequency-domain transfer functions including the noise transfer functions from signal to power/ground.

Figure 2.5 shows the time-domain waveforms when Port 1 is exited with a 5V voltage source with a 50 Ω matching source impedance. The source data rate is 2.5 Gb/s, and the rise/fall time is 100 ps. The data pattern is “010010001” in repetition. Port 2 is terminated with a 50 Ω load impedance. As clearly seen in Figure 2.5, the voltage at Port 2 has a magnitude close to 5 V, indicating the signal transmission loss is relatively small

at the fundamental frequency. However, the waveform at Port 2 is significantly rounded due to the high-frequency loss, consistent to the frequency-domain result discussed before. The noise voltages at Ports 3 and 4 are much smaller, compared to the Port 2 signal voltage. However, if they are examined more carefully in the zoomed-in plots as shown in Figure 2.6, their magnitude gets as high as 120 mV. Obviously these noise voltages cannot be neglected.

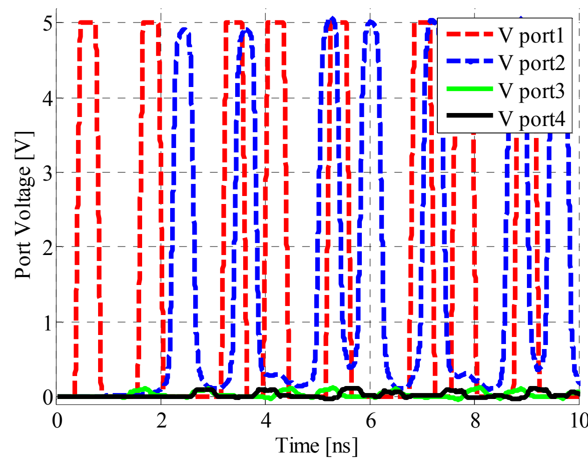

Figure 2.5. Time-domain transfer functions including the noise transfer functions from signal to power/ground.

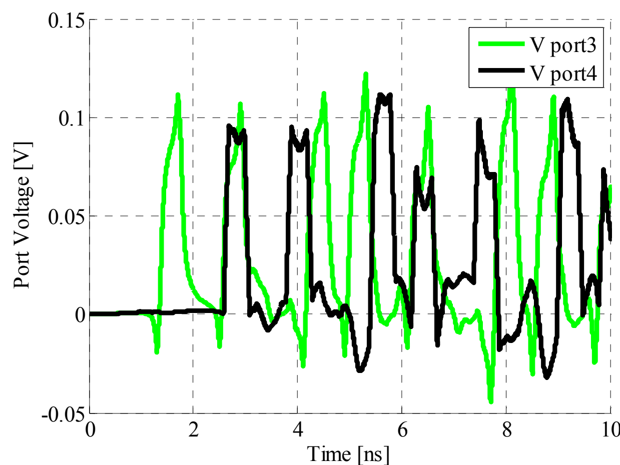

Figure 2.6. Noise voltages generated in the power/ground plane pair due to the signal transition.

2.5. NOISE COUPLING FROM POWER/GROUND TO SIGNAL

The signal via can also pick up power bus noise when it penetrates a power and ground plane pair. Figure 2.7 shows a test geometry used to study this noise coupling mechanism. Similar to the previous example, it includes a multi-layer printed circuit board and a signal via transitioning a signal from the top microstrip line to the bottom one. The PCB stackup, dimensions, the microstrip lines, and the signal via location are the same as in the previous example. Additionally, an IC and a decoupling capacitor are added in the geometry. The coordinates shown in the figure are the power via locations for these two components. Their ground vias are placed 50 mils away from the corresponding power vias. Ports 1 and 2 are located at the end of the top and bottom microstrip traces, respectively. Port 3 is set at the IC, looking into its power and ground vias. The equivalent circuit model for this test geometry is shown in Figure 2.8. The decoupling capacitor is modeled as a series RLC circuit.

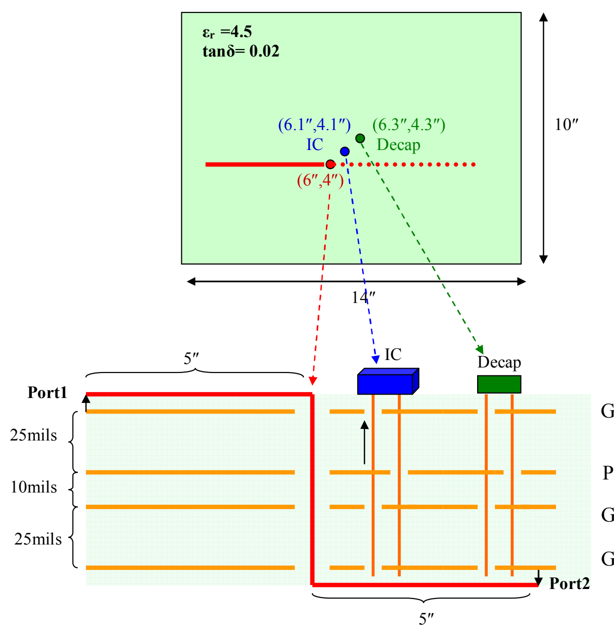

Figure 2.8. Test geometry to study noise coupling from power/ground to signal nets.

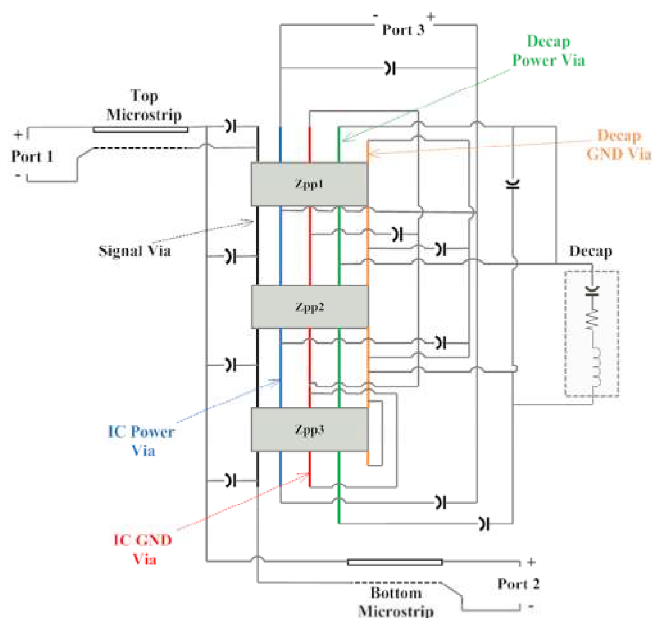

Figure 2.9. Equivalent circuit model for the test geometry shown in Figure 2..

Figure 2.9 shows the frequency-domain transfer functions. As illustrated by the $|S_{13}|$ and $|S_{23}|$, noise voltage can be generated at the end of the microstrip traces when the power bus noise is coupled to the signal via that penetrates the power and ground plane pair. Since the geometry is symmetric, the magnitudes of the noise voltages at Ports 1 and 2 are the same.

The corresponding time-domain results are shown in Figure 2.10. When the IC (Port 3) draws current (triangular pulses) from the power and ground plane pair, noise voltage pulses are observed at Ports 1 and 2. Notice that these two noise voltages are out-of-phase. In other words, the dominant coupling is inductive coupling between the signal and power vias.

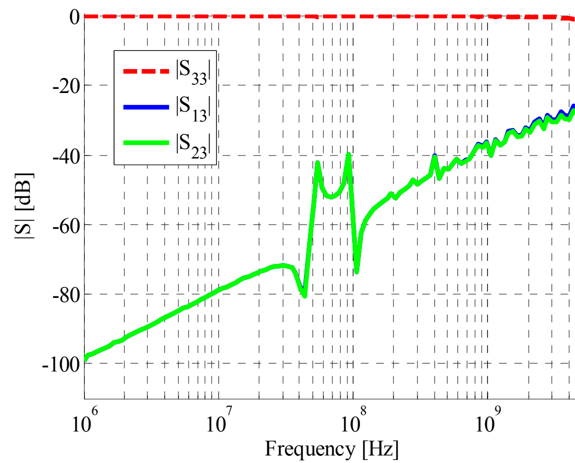

Figure 2.9. Frequency-domain transfer functions including the noise transfer functions from power/ground to signal.

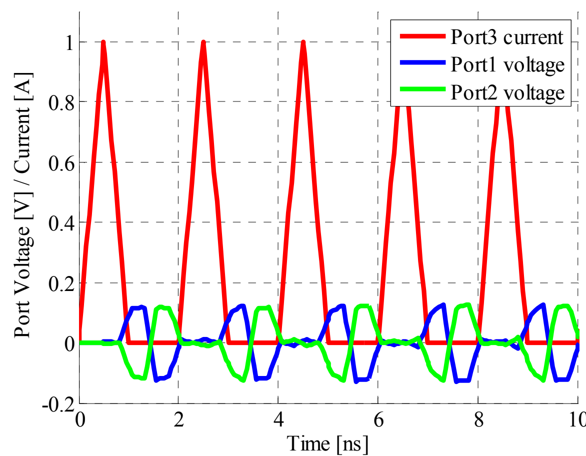

Figure 2.10. Noise voltages generated in the signal trace caused by power bus noise due to the signal transition.

If the signal via location is further away from the IC and the decoupling capacitor, as illustrated in Figure 2.11, the noise coupling from the power and ground plane pair to the signal traces is weakened, as shown in both Figure 2.12 and Figure 2.13. In the frequency domain, the $|S_{13}|$ and $|S_{23}|$ magnitudes, generally speaking, are a few dB lower than those in Figure 2.9, except close at the two resonant frequencies of 55 MHz and 90 MHz. Due to nature of the transfer functions, this indicates a lower noise coupling from the power and ground plane to the signal traces. The trend is more intuitive in the time

domain. As shown in Figure 2.13, the magnitude of the noise voltage at Ports 1 and 2 is much lower than in Figure 2.10.

2.6. CONCLUSIONS

This paper studies the noise coupling between signal and power/ground nets due to signal vias penetrating power and ground plane pair. A segmentation approach combined with a via capacitance model and a plane-pair cavity model is used. The modeled results demonstrate that noise can be coupled from the signal to the power and ground plane pair, and vice versa, with a magnitude of as high as -30 dB in the frequency-domain transfer functions. Therefore, the noise magnitude can be significant enough and careful design is required to achieve the noise mitigation and signal integrity objectives in high-speed digital circuits. The segmentation approach provides a suitable tool for effective and efficient engineering designs and optimization.

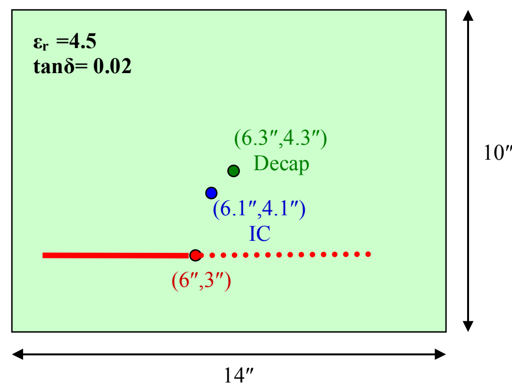

Figure 2.11. Signal via is further away from the power/ground vias, compared to the test geometry shown in Figure 2.7.

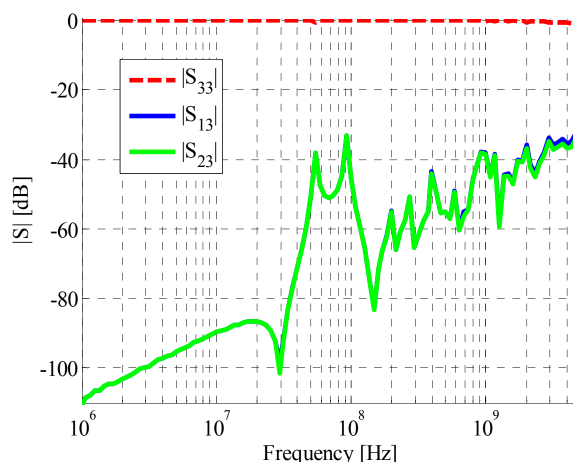

Figure 2.12. Frequency-domain transfer functions including the noise transfer functions from power/ground to signal, for the geometry shown in Figure 2.11.

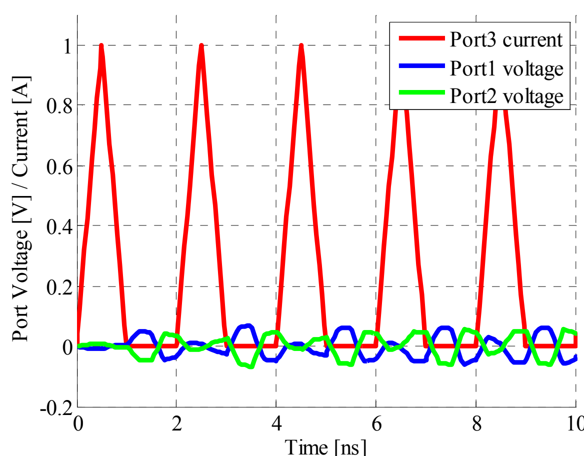

Figure 2.13. Noise voltages generated in the signal trace caused by power bus noise due to the signal transition, for the geometry shown in Figure 2.11.

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3. DESIGN METHODOLOGY FOR PDN SYNTHESIS ON MULTI-LAYER PCBS

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3.1. ABSTRACT

This paper discusses a fast and accurate design methodology for real world design of power distribution networks on printed circuit boards. The designer is shown how to estimate the amount of current needed for large ICs, how to estimate the amount of noise voltage due to this current draw, and the effect of decoupling capacitor distance from the IC's power/ground pins.

Keywords: EMI, Power Integrity, Signal integrity, PDN, decoupling, cavity resonance.

3.2. INTRODUCTION

Proper decoupling of printed circuit board (PCB) power distribution networks (PDN) is very important for proper operation of the PCB. Decoupling of the PDN is important in (a) reducing radiated and conducted noise levels from the PCB (EMI), (b) reducing the noise level on the PCB that active components tolerate (EMC), and, (c) providing current (charge) to ICs that is timely and sufficient (usually an issue with large digital ICs). Because these three areas are broad in scope, yet distinct, there are many published design rules, but because of the breadth of decoupling requirements and the distinct character is each of the three requirements, these published design rules can contradict each other. The designer can be faced with evaluating a plethora of design rules often without the benefit of a sound understanding of the physics involved with a well designed decoupling strategy. The common result is an over design where a larger number of decoupling capacitors are used than may be required. This paper focuses on

the third area of importance in decoupling, i.e., ensuring timely and sufficient charge supply to major ICs on the PCB.

The designer faces three basic questions:

(1) what is the maximum amount of noise between the power and ground-reference plane desired,

(2) how much current is needed by the IC, and

(3) how many capacitors are required to meet the goal with the variation in distance to the capacitor and capacitor connection inductance.

Recent publications [1,2,3,4] study different aspects of decoupling design including overall PCB noise levels, noise sources and charge delivery to ICs. For overall noise level studies frequency domain analysis is usually the most appropriate. These analyses focus on global (distributed) decoupling analysis for EMI/EMC resonance control since a low impedance between the power and ground-reference plane is needed across PCB to minimize the potential emissions. Global (distributed) decoupling capacitors and/or thin separation between power and ground-reference plane have been shown to have significant impact on the ability to achieve this low impendence.

Time domain analysis is usually more appropriate when the charge supply to the IC is the concern, since the charge must be supplied during the switching time of the IC. There can be significant delay in the movement of charge from its stored location (in a decoupling capacitor or between the planes) to the IC power pin. This delay is due to propagation delay and/or inductance of the current path. Regardless of the reason for the delay, if the replenishment charge is delayed too long, a larger than normal voltage supply droop can occur which may interfere with proper operation of the IC.

The purpose of this paper is to help designers go through a step-by-step process to design the decoupling strategy for the charge supply. The distance to the decoupling capacitors, the number of decoupling capacitors, and the inductance associated with the connection of the decoupling capacitor to the power and ground-reference planes will all influence how much charge is delivered. This paper will not discuss global (distributed) decoupling, since the approach and concerns are different, and they have been addressed in previous work [1, 2, 3].

3.3. HOW MUCH CURRENT IS REQUIRED BY THE IC?

The first step is to determine how much current is required by the IC. If the IC is a simple clock buffer then a fairly straightforward approach can be used [5]. However, the larger ICs are usually the dominant current drain for the PDN and will be the focus of this paper.

If specialized knowledge of the inner workings of the IC is available from the IC vendor, then a good analysis of the required time domain current is available and should be used. Often, however, this specialized knowledge is not available to the PCB designer, and so some estimation must be made.

A rough rule-of-thumb that is often used to estimate power current requirements is to assume that one-third of the total power consumption for that ASIC is associated with the time-varying current. For example, if the ASIC is a 60 watt device operating with a supply voltage of 2.5 volts, we would estimate that 20 watts of the power is time-varying. For a first-order estimate, from a simple triangle current waveform (as in Figure 3.1) with the total pulse width equal to the ASIC driver voltage output rise time we can find the average current using the following relationship:

$$I_p = 2 * \frac{I_{AVE} * T}{t_r} \tag{1}$$

$$I_{AVE} = \frac{P_{noise}}{V_{\sup ply}} \tag{2}$$

and t_r is the rise time of the output voltage. As an example, assume that P_{noise}, the power consumption associated with the time-varying current, is 20 watts and V_{Supply} is 2.5 Volts. With a 200 Mb/s waveform, the period, T, is 5 ns and the rise time, t_r, is 1 ns. Using these values in equations 1 and 2 above, the result is I_p = 80 A.

3.4. PURPOSE OF LOCAL DECOUPLING CAPACITORS

It has been shown [2, 3, 4] that the inductance associated with the capacitor's connection to the planes and the inductance associated with the distance between the IC and the capacitor (except in cases with large separation between planes) results in the

capacitor not being able to deliver charge directly to the IC during the time required. All the charge delivered to the IC in the time period immediately after switching states is delivered from the capacitance formed by the planes.

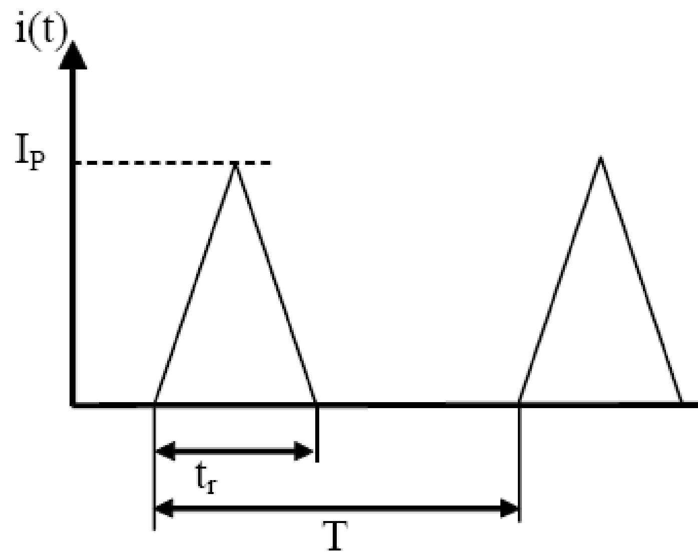

Figure 3.1. Simple triangle current waveform

If the charge between the planes is not replenished, the voltage between the planes will continue to droop and the overall result is increased noise propagating between the power and ground-reference planes. The decoupling capacitor's purpose is therefore to assist in the replenishment of the charge between the planes to mitigate this voltage droop at the power pin of the IC. The distance to the decoupling capacitor and the inductance associated with the capacitor's connection are both very important to this charge replenishment.

First, consider the amount of inductance associated with the capacitor's connection to the planes. Figures 3.2a and Figure 3.2b illustrate a low inductance connection and a high inductance connection, simply based on the distance down to the associated planes within the PCB stackup.

In addition to the distance to the planes, the distance between the vias must also be included. This inductance can be calculated [2] by an extensive formula. Table 1 shows some typical connection inductances calculated using this formula. The distance

between the pads for 0805 (8 mils x 5 mils) and 0603 (6 mils x 3 mils) standard size surface mount technology (SMT) capacitors are added to the additional trace lengths on each side to find the total distance between the vias.

Table 3.1 Calculated Connection Inductance for various dimensions

Spacing between Vias	20 mils to planes	10 mils to planes
0805 + 2*10mil	3.0 nH	2 nH
0805 + 2*100mil	4.1 nH	3 nH
0805 + 2*160mil	5.1 nH	3.5 nH
0603 + 2*10mil	2.3 nH	1.1 nH
0603 + 2*100mil	3.3 nH	2.1 nH
0603 + 2*160mil	4.2 nH	2.4 nH

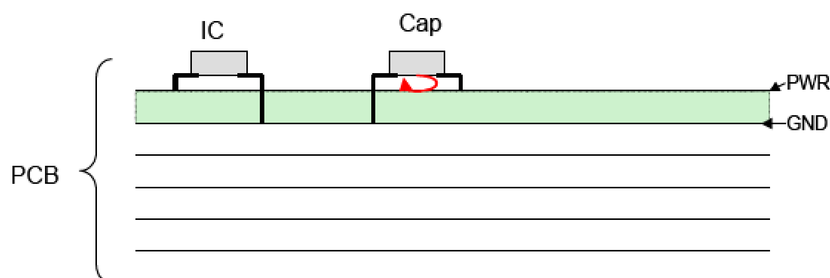

Figure 3.2a. Low connection inductance configurations

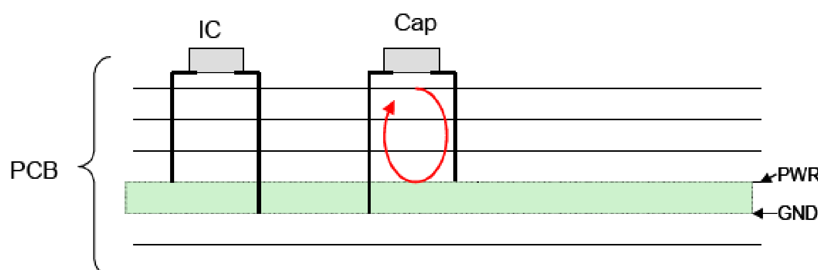

Figure 3.2b. High connection inductance configuration

Clearly, there is significant connection inductance that must be added to the nominal equivalent series inductance (ESL) specified by the capacitor vendors.

3.5. INITIAL PULSE VOLTAGE DROOP

It is important to know how much the voltage between the planes will droop for each IC current draw. If all the charge must come from the planes, the total available charge is:

$$Q = C * V \tag{3}$$

where:
Q = charge,
C = board capacitance, and
V = supply voltage

The charge drawn by each current pulse from the IC is given by:

$$Q_p = \frac{1}{2} * I_p * t_r \tag{4}$$

where:
Q_p = charge drawn in the pulse,
I_p = the peak current, and
t_r = current pulse width
Using these expressions, the voltage droop for each pulse can be found.

3.6. TIME FOR CHARGE RESTORATION TO THE PLANES

The time for the charge to travel from the capacitor to the area of the planes where it is needed can be broken into two parts (1) delay associated with the connection inductance, and (2) propagation delay associated with the distance the charge must travel. This can be modeled with a simple circuit that includes resistance, inductance and a transmission line as shown in Figure 3.3.

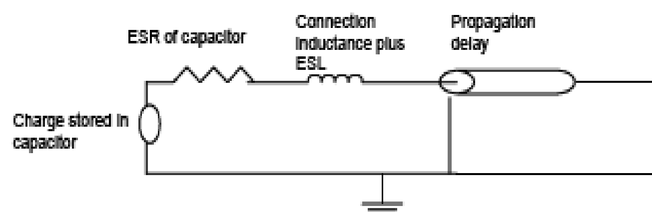

Figure 3.3. Equivalent circuit

3.7. SIMULATION CONFIGURATION

The cavity resonance technique was used to create an HSPICE equivalent circuit [6, 7] and then the HSPICE circuit was used in a time domain analysis to produce the following results. The circuit was initially charged to 3.3 volts (planes and decoupling capacitor, then the DC supply was removed and a 1 A peak triangle pulse of current with a 0.5 ns base width, and a cycle time of 1 ns was drawn repeatedly from the planes. The dimensions of the planes were 20” x 24” with 35 mils separation between the planes. The decoupling capacitor was moved to various distances from the IC power pin port which was located asymmetrically in one quadrant of the board. The voltage at the IC power pin was observed for various distances to the decoupling capacitor to observe the speed of charge replenishment.

Two separate effects were observed, i.e., effects within a cycle and the effects over many cycles.

3.8. EFFECTS WITHIN A CYCLE

The within-cycle effects are due directly to the current draw. The IC draws current predominately from between the planes, and the inductance associated with this current and the rate of change of the current (di/dt) combine as a noise voltage V_L=L*di/dt. This is shown in Figure 3.4. The impulsive noise voltage that occurs during each 1 ns cycle is caused by the inductance and di/dt. There is little difference between the various capacitor distances, with the exception of the closest capacitor distance (at 50 mils). In this case, the very close placement allows the mutual inductance between the vias to significantly lower the loop inductance, thus lowering the noise voltage swing.

The only other way to reduce this noise is to lower the inductance by making the power/ground layers closer to the surface of the board (as in Figure 3.2), or by slowing the rate of change of the current (probably not possible).

3.9. EFFECTS OVER MANY CYCLES

There is another voltage noise effect that takes place over many cycles. When the within-cycle noise is filtered out to show the (relatively) slower effects, a damped oscillation is seen in Figure 3.5. This oscillation has a period of about 34 ns corresponding to a resonant frequency of 29.4 MHz. This is due to the inductance of the port and the inter-plane capacitance. When using the interplane capacitance of 13.8 nF and the port inductance of 2.2 nH (1 nH between the planes and 1.2 nH above the planes), the resulting LC resonant frequency is 28.8 MHz.

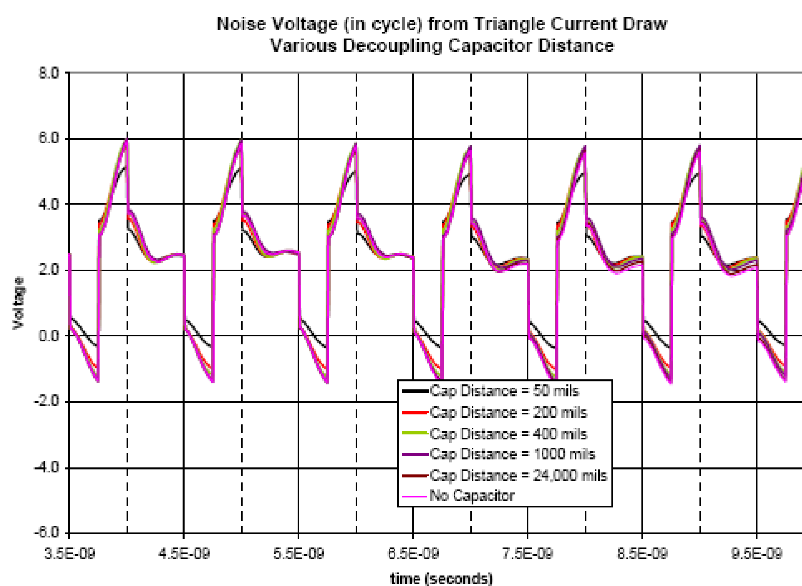

Figure 3.4. Within cycle noise voltage from IC current draw

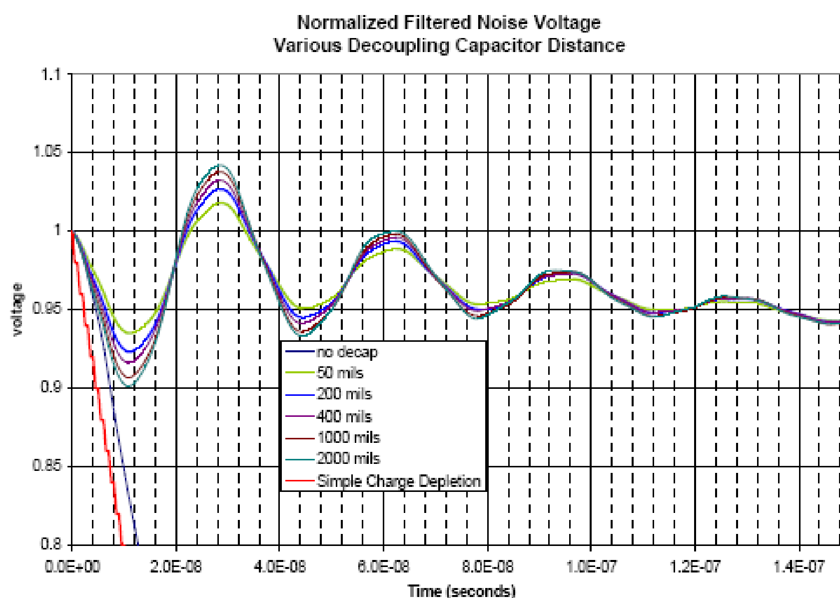

Figure 3.5. Noise voltage across many cycles

The configuration with no decoupling capacitor is also displayed in Figure 3.5. Since the DC supply was removed from the circuit when the IC current draw began, once the charge stored between the planes is depleted, the voltage will continue to decrease until it is zero.

If equations 3 and 4 are used to calculate the amount of charge removed during each current pulse, and then calculate the remaining voltage calculated, the curve in Figure 5 labeled 'Simple Charge Depletion' shows the voltage decrease. It is observed that the slope of the curve is the same as the no capacitor case for the first 15-20 ns. After that time, the actual voltage decrease slows due to the longer delay required for the charge to travel from the remote portions of the board.It can also be observed from Figure 3.5 that the amplitude of the damped oscillation is lower when the decoupling capacitor is placed close to the IC power pin.

Figure 3.6 shows the percentage deviation from the nominal voltage as the decoupling capacitor distance increases. Once the capacitor is about 20 times the distance between the planes, the deviation increases only slightly, indicating that the distance to the decoupling capacitor is too great for it to provide charge to the IC during the time of need during switching.

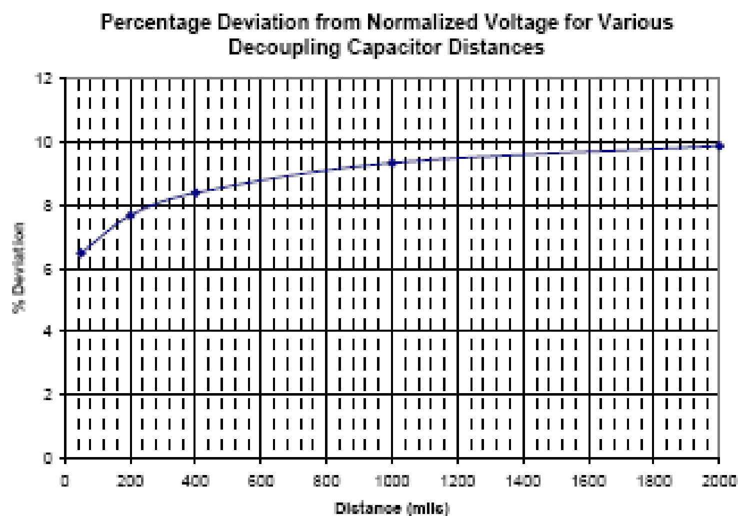

Figure 3.6. Deviation Vs. decoupling capacitor distance

3.10. SUMMARY

This paper has provided PCB designers with an approach to estimate the noise between power and ground planes. Noise created during each cycle is due to the amount of connection inductance associated with the IC as well as the rate of change of the IC's current draw. Noise that occurs over much longer periods (mid frequency noise) is associated with the resonance between the PCB planes and the connection inductance of the IC. The position of a decoupling capacitor has little impact on the within-cycle noise, but can impact the midfrequency noise significantly. However, once the decoupling capacitor gets far enough away, it will not have a significant impact on the amplitude of this noise.

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4. COMPARING TIME-DOMAIN AND FREQUENCY DOMAIN TECHNIQUES FOR INVESTIGATION ON CHARGE DELIVERY AND POWER-BUS NOISE FOR HIGH-SPEED PRINTED CIRCUIT BOARDS

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4.1. ABSTRACT

The performance of power distribution network is critical to high-speed digital circuits in terms of both signal integrity and radiated emission. This paper studies charge delivery of a power distribution network, as well as power bus noise resulting from device switching, in the time domain as well as the frequency domain. Some of the PDN performance analysis is easier to understand when analyzed in the time domain. The effects of capacitor location, capacitor value, power/ground plane pair location within the stackup, board size, as well as dielectric material, are discussed.

4.2. INTRODUCTION

In high-speed digital circuit designs, the PDN associated with the PCB plays a vital role in maintaining signal integrity (SI), i.e., necessary fidelity of signal and clock wave shapes, and minimizing electromagnetic noise generation. Yet, the design of the power distribution system presents an increasingly difficult challenge for digital circuits employing active devices. As integrated circuit (IC) technology is scaled downward to yield smaller and faster transistors, the power supply voltage must decrease. As clock rates rise and more functions are integrated into microprocessors and application specific integrated circuits (ASICs), the power consumed must increase, meaning that current levels, i.e., the movement of electrical charge, must also increase [1-2].

One category of design engineer who confronts this design challenge is the signal integrity (SI) engineer, whose goal is to ensure adequate fidelity of the individual signal and clock waveshapes on the PCB [2-4]. Another category of engineer who faces similar design challenges is the electromagnetic interference/compatibility (EMI/EMC) engineer, whose goal is to minimize electrical noise generated by the circuitry to prevent interference with other systems and within the same system [5-8]. While both engineers wrestle with the same physics of the dc PDN on a digital PCB, practitioners of different design disciplines may view the same physical phenomena differently. For instance, the SI engineer may be more familiar with circuit behavior and analysis expressed in the time domain than with the behavior of electromagnetic waves and analysis expressed in the frequency domain. The EMI engineer's experience is likely just the reverse. Therefore these engineers may employ different methodologies and approaches to PCB design. These different design methodologies may sometimes seem contradictory and/or incompatible, but both engineers have similar goals of assuring adequate charge transfer between active devices and the PDN with minimum noise generation. This paper is intended to review the state of knowledge of dc power distribution design, offer practical design advice, and address schools of design that appear to offer conflicting advice.

The PDN for modern medium-to-high-speed digital PCBs is usually formed from one or more pair of conducting planes used as power and ground (power return). The PDN for digital circuitry has evolved over time, as signal and clock speeds have increased, from discrete power supply wires, to discrete traces, to area fills and ground islands on single/two-layer slow-speed boards, to the planar power bus structure used extensively in today's multi-layer high-speed PCBs. The low inductance associated with charge delivery from the plane to circuit element allows for the storage of relatively easy-to deliver charge available all over the board. Often the term power bus is used to identify an individual plane pair, whereas the term PDN is used for the entire system of supplying power to circuits placed on the PCB. As speeds of active devices have increased, digital data rates have escalated and signal rise and fall times dropped so that the frequency regime of operation on the PCB has risen into the gigahertz (GHz) band. Operation at high frequencies can blur the boundaries between circuit behavior and electromagnetic behavior.

Noise is generated in the power bus when a digital active device (integrated circuit or transistor) switches between its high and low logical states (switching noise) [5], or it can be coupled to the power bus when a high-speed signal transits through the power bus by signal vias (transition noise) [9,10]. Noise generated in the power bus can be easily propagated throughout the board. Propagated noise can affect the operation of other active devices (signal integrity) as well as radiate from the PCB (EMI). At the printed circuit board (PCB) level, there is no way to eliminate the production of noise by IC devices. However, a good PCB design can ensure that the generated noise be constrained to a level that permits successful circuit operation and the resulting low levels of radiation produced do not violate regulatory requirements. The use of decoupling capacitors are one of the key elements in achieving this goal, along with the board stack up design, power/ground plane pair, usage of losses, power islands, board edge termination, etc.

4.3. THE POWER DELIVERYNETWORK

There are two primary purposes of the PDN. The first purpose of the PDN is functionality. The PDN is a charge storage and delivery system that supplies charge (current) when an IC switches state and requires additional current. If sufficient current is not provided, the IC may experience a functional failure.

A second purpose of the PDN is to reduce or minimize the noise injected into the power and ground-reference plane pair and thus reduce the potential of noise propagation in the board and EMI emissions from the circuit board. The mechanisms for EMI emissions are several. For instance, the edge of a board may be near the seams of a metal enclosure or near an air vent area, allowing this noise to escape the enclosure. Alternatively, PDN noise may couple onto input/output (I/O) connector pins or onto a grounded cable shield and be directly coupled out of the metal enclosure through any of the cables. There are a variety of coupling mechanisms that are possible once this noise is created. To avoid undesirable consequences from noise on the PDN, the impedance of the PDN should be low over a wide frequency range that includes the spectrum of the critical signals and their harmonics.

4.3.1. THE DECOUPLING CAPACITORS

A PDN is comprised of several elements, including the VRM module, bulk capacitors, SMT decoupling capacitors, and power/ground plane pairs (power bus). The effectiveness of each element in delivering sufficient charge with adequate speed is not uniform. A charging hierarchy exists based on the rate of charge delivery (usually impeded by distance and inductance) and charge storage capacity [2].

The VRM (Voltage Regulator Module, i.e., dc/dc converter), the largest source of charge, is able to store and release a lot of charge but it cannot meet demands to rapidly deliver charge due to the large inductance connecting it to the PDN. It cannot keep up with charge demands that vary or oscillate with rapidity greater than a MHz. Hence, it cannot deliver charge in a timely manner when the circuits demanding charge have time constants that are much shorter than one microsecond.

Bulk capacitors constitute the second largest source of charges in this hierarchy and are typically capacitors whose values range between a few hundred microFarads to as high as a few milliFarads. These components are able to supply charge with sufficient speed to meet the demands by systems characterized by time constants as low as a few hundreds of nanoseconds and even shorter.

Decoupling capacitors, sometimes referred to as “high-frequency ceramic capacitors”, are the second to last category of components in this charging hierarchy [2]. Decoupling capacitors usually exhibit capacitance values from a few tens of nanoFarads to as high as a few microfarads. These capacitors can usually support charge demand from circuits with time constants as low as a few tens of nanoseconds.

The PWR/GND planes form the last component in the charging hierarchy and can usually deliver charge to circuits whose time constants are shorter than a few tens of nanoseconds, i.e., a charge demand frequency above several hundreds of MHz.

The VRM and the bulk capacitors are usually few in number and are located in specific areas of the PDN due to their dimensions and other constraints. High-frequency decoupling capacitors are usually large in number and are typically easily located with a greater flexibility. Figure 4.1 shows a typical impedance profile of a decoupled PDN.

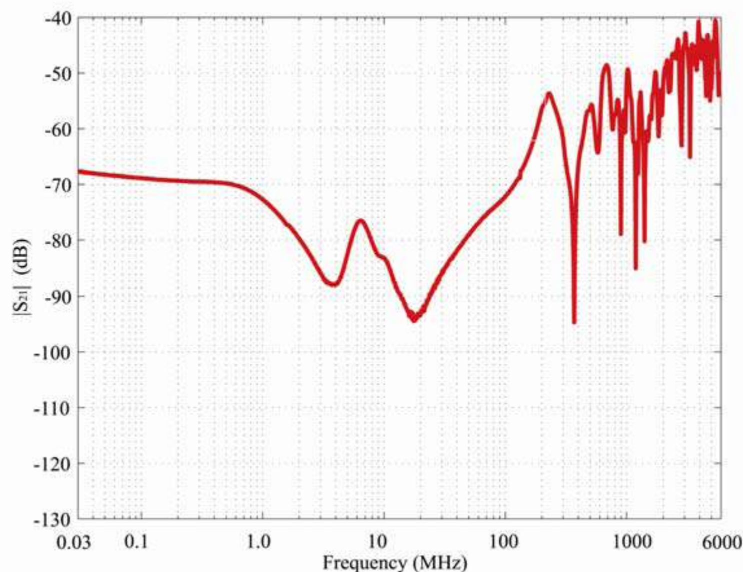

Figure 4.1. Typical Impedance Profile for PDN.

Self impedance, or Z_{11}, provides an indication of the voltage created by the injection of noise current. Z_{21} indicates the noise transmission from noise source to anywhere on the board. Z_{21} is very useful for circuit susceptibility and radiated emission studies. Zij is a vector quantity in that it has both magnitude and phase. For these types of studies, often just the magnitude is examined. The effect of phase will be discussed later.

The decoupling capacitor exhibits parasitic inductance and resistance in addition to its capacitance. The parasitic inductance consists of an inductance associated with the capacitor itself (equivalent series inductance, or ESL) and inductance associated with the means of connecting the capacitor between power and ground planes (inductances associated with the solder pads used to secure the capacitor to the PCB and any traces and/or vias used to make the electrical connections). The parasitic inductance impedes changes in the current; hence, it impedes the prompt availability of charge. The parasitic subsection heading and is indented ½" over from the left hand margin, and it's text is inductance and resistance when combined with the device's capacitance, form a series resonant circuit whose impedance dips to a minimum at the frequency where the inductive and capacitive reactance cancel. Low values in interconnect inductance can often be achieved by careful attention to the design of solder pads lands with low inductance properties along with having no traces in the ideal case, or in the realistic

case, very short traces connecting them to the planes [4]. The parasitic inductance of the interconnects can be several nH to less than 1 nH. In brief, a good PDN design is characterized by a low interconnect inductance between each decoupling capacitor and the PDN itself. Figure 4.2 illustrates the connection of an SMT capacitor to a power bus which provides a parasitic inductive component from the current path above the plane (Loop 2) and a parasitic inductive component associated with current flow between the planes, first in the via and then returning as displacement current (Loop 1). As stated earlier, the parasitic inductance associated with current flow above the plane also includes effects from the solder pads that connect to the capacitor and any traces used to connect solder pads to the vias. The lower the value of the inductance, the faster the capacitor can supply and store charge and the more importance that is attached to the distance of the decoupling capacitor from an IC in achieving effective decoupling capacitor behavior.

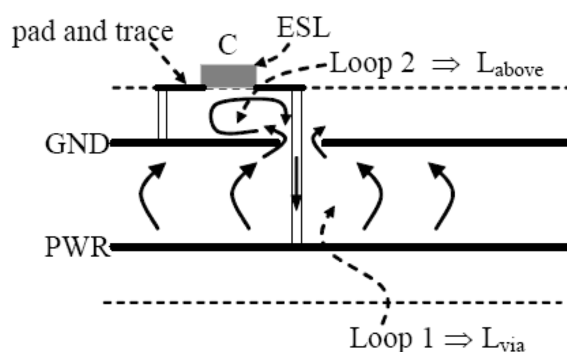

Figure 4.2. Connection Inductance Associated with Capacitor Mounting on PCB.

The ESL of the decoupling capacitors is a function of the length, width, height and manufacturing technology of the capacitor itself. Due to improvements in the material selection and manufactory technology, the size of SMT decoupling capacitors have been shrunk from the early 1206 package size (120 mils length x 60 mils width) down to the more recent 0201 (20 mils length x 10 mils width) package size, allowing a significant reduction of the equivalent series inductance, which is always less than 1 nH.

The equivalent series inductance (ESL) as well as the equivalent series resistance (ESR) is usually measured by employing impedance analyzers and/or network analyzers.

In both cases, special fixtures are utilized along with calibration procedures and measurement techniques in order to minimize the parasitic elements associated with the measurement setup itself [11]. Values reported by capacitor manufacturers are influenced by the specific measurement techniques employed and should be viewed critically when the use of the specific values of parasitic elements is desired. Typically, the interconnect inductance is significantly larger than the ESL, making the ESL a small portion of the overall inductance.

4.3.2. DETERMINING INDIVIDUAL DECOUPLING CAPACITORS VALUES – DIFFERING APPROACH

Approach A: The SI community. Two general approaches have developed in the design community on how to deploy decoupling (high-frequency ceramic) capacitors in order to reduce the impedance of the PDN between frequencies in the range of approximately 1 MHz to a few hundred MHz. A prominent approach, referred to here as Approach A, is used in the SI community and has developed out of the experience of server motherboard design and other high performance digital PCBs [2-3]. This approach uses an array of values of decoupling capacitors. This technique generally uses three capacitor values per decade to achieve the flattest PDN impedance vs. frequency profile to maintain an upper bound “target impedance” to provide an upper bound on the AC ripple voltage on the PDN [4, 11].

In Approach A, the capacitor values are typically chosen so that they are logarithmically spaced (i.e. 10, 22, 47, 100 nF, etc). The effectiveness of this approach is somewhat dependant on the value of ESR of the capacitors and the resulting series/parallel resonant (resonant/anti-resonant) frequencies of the decoupling capacitors to maintain the impedance to be below the desired target impedance over the frequency range of interest.

Approach B: The EMI community. On the other hand, a prominent view in the EMI community for PDN design for highspeed digital PCBs is that the specific values of decoupling capacitors need not be as carefully chosen as in the previous approach [5]. This design methodology, Approach B, addresses the high-frequency ceramic decoupling specifically and employs the largest value of capacitance available in the specific surface

mount technology (SMT) package size to yield a PDN impedance profile that is acceptably flat. For the same number of high-frequency ceramic decoupling capacitors, more total capacitance is often achieved in Approach B than with Approach A.

A comparison of the two approaches in the frequency range between 1 KHz and 1 GHz using a 2-D cavity model method, allowing parallel plane characteristics to be included[12, 13]. The PDN dimensions correspond to a PCB that is 6 in. x 9 in. with a single power/ground plane pair power bus of thickness 10 mils. The PCB material is chosen to exhibit a dielectric constant of 4.5, and a loss tangent of 0.02; a relative permeability of unity; and a plane capacitance of 2.426 nF. For each example with this PCB, one bulk decoupling capacitor and 60 ceramic decoupling capacitors were chosen. In addition, it was assumed that the power bus was located at the center of the 62 mil PCB stackup and that all decoupling capacitors were placed on the board's surface, allowing for inclusion of the via interconnect inductance in the simulation. A target impedance of -20 dB_ was chosen. For each capacitor type, typical values of ESR and ESL were selected from typical values from a specific vendor's catalog for X7R MLC capacitors. [14]

A third approach, Approach B1, a subset of Approach B, was included to investigate the effects of making all of the smaller decoupling capacitors in the 0402 package size, instead of dividing them between the 0603 (60 x 30 mils) and the 0402 (40 x 20 mils) package sizes. Figure 4.3 shows the driving point impedance, _Z_{11}_ of the PDN. While there are differences between the three approaches shown in the Figure, all three provide an impedance well below the target impedance up to frequencies in the range of 100 MHz. At low frequencies, Approaches B and B1 provide a lower impedance, which is a manifestation of the higher capacitance used. It is also interesting to note that there is very little difference between Approaches B and B1, except near 1 MHz, where the impedance is already very low compared to the target impedance. Above a few MHz, when the impedance rises proportional to frequency, i.e., at a rate of 20 dB/decade, there is virtually no difference between any of the methods. In this example, above 100 MHz, the discrete decoupling capacitors do not do a good job of maintaining a low PDN impedance, regardless of the design strategy.

In these examples, it is clear that either approach can achieve the design goal on PDN transfer impedance and have nearly identical performance above frequencies of a few hundred MHz. Use of a single value of capacitance in the largest value in the package size may provide the benefit of simplicity of design and manufacture [7]. Changing the design parameters (PCB characteristics, power bus characteristics, capacitor characteristics, etc.) will alter the impedance curves regardless of the design approach used, but will not change the overall conclusion that there is little difference in the PDN impedance profiles between Approaches A and B (and B1).

Although the values of the decoupling capacitors employed are different in the two strategies, the need of lowering the parasitic inductance associated with the decoupling capacitors is consistent [2,3,5,8]. In fact, lowering this inductance shifts all the series/parallel resonant frequencies higher and in particular the last one, allowing the PDN to meet the design specifications on the target impedance in a broader frequency band.

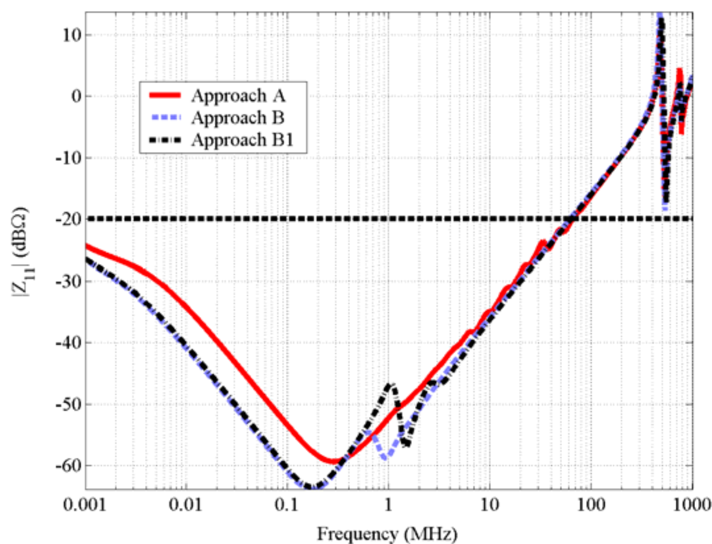

Figure 4.3. PDN Impedance from Comparison of Decoupling Approaches.

4.3.3. THE IMPORTANCE OF CAPACITORS LOCATION

The significance of decoupling capacitor location has been extensively studied in the EMI design community [16, 17]. In the early days of digital electronics on PCBs consisting of only a few layers (and perhaps without power and ground planes), the

conventional wisdom was that decoupling capacitors should be placed as close as possible to the major active components. Within the past decade, the conventional wisdom for digital electronics on multilayered PCBs with planes (which is the model for modern high-speed digital design) has been that it is not generally necessary to relate the effectiveness of the decoupling capacitors to their distance with respect to the IC's, i.e., the decoupling capacitors behave in a global manner [18]. More recent work indicates that there are specific situations where the proximity of the decoupling capacitor to the IC can have a strong affect of the effectiveness of the capacitor [19]. Hence, there is a growing acceptance that there are specific design situations where it is beneficial for the capacitor to be placed "close" to an IC power pin.

Figure 4.4 shows a conceptual configuration of an IC and a decoupling capacitor attached to a power bus. The current loop formed by the IC drawing current from the power bus and capacitor has three distinct regions of magnetic flux that define the inductance of this loop. The regions labeled Labove represent the inductance of the connection between IC and plane and between capacitor and plane. (The two Labove regions are not necessarily identical, but they are treated as such in this discussion.) The region labeled Lbelow represents the inductance of the portion of the current loop that exists between the power and ground planes. L_{below} has a self inductance component and a mutual inductance component which represents mutual coupling (transformer–like) between the two vias. The mutual inductance acts in opposition to the self-inductance and reduces the overall value of Lbelow. The total loop inductance encountered by the current flow from IC to capacitor is the sum of these inductances,

$$L_{Total} = 2 * L_{Above} + 2 * L_{Below} \tag{1}$$

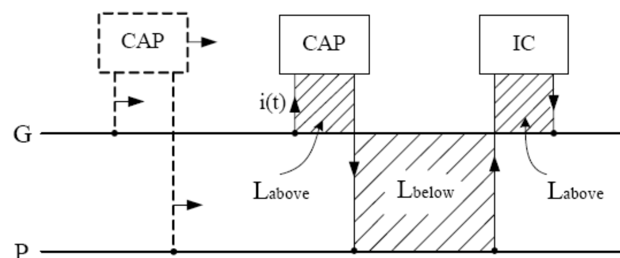

Figure 4.4. Inductance "Above" and "Below" for connection to PDN.

If the capacitor were moved closer to the IC, as indicated by the dashed lines in Figure 4.4, then the vias that form the boundaries of L_{below} become closer, the increased mutual magnetic coupling between these vias decreases Lbelow causing Ltotal to decrease. (The decrease in L_{below} due to mutual coupling is explained in the discussion of Figure 4.5, later in this paper.) As stated earlier, the lower the inductance value, the faster the capacitor can supply and store charge and the more importance is attached to the distance of the decoupling capacitor from an IC in achieving effective decoupling capacitor behavior. Therefore, this decrease in inductance should enhance the effectiveness of the decoupling capacitor and render decoupling effectiveness that is more apt to be location-dependant.

Magnetic Coupling between Vias Can Affect Decoupling. The ability for rapid behavior is directly related to the inductance of the capacitor's interconnect and its ESL. However, two identical capacitors with identical interconnect may still differ in their abilities to exhibit local decoupling behavior. The reason for this is the degree of magnetic coupling that exists between the vias of the power/round connections of the IC and the decoupling capacitor, as shown in Figure 4.5. The mutual coupling between the vias reduces the overall interconnect inductance that determines the magnitude and rapidity of the charge supplied by the capacitor. (The reduction of overall inductance can be seen in Figure 4.2, where the directions of the currents in the two vias produce magnetic flux in opposite directions in the region of mutual magnetic flux between the planes, thereby decreasing the total magnetic flux and the total inductance.) This mutual inductance can also increase the capacitor's effectiveness in reducing the PDN impedance and increase the maximum frequency for which this decoupling capacitor can be effective. A circuit representation of Figure 4.2 is shown in Figure 4.3.

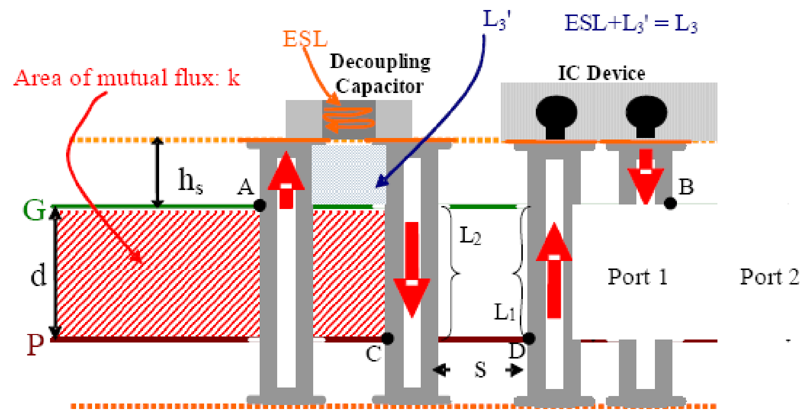

Figure 4.5. Local Decoupling Inductance and Mutual Inductance.

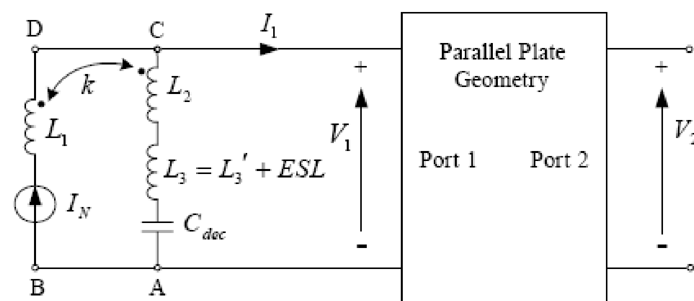

Figure 4.6 Schematic Representation from Figure 4.5.

The via pins connected to the same power layer (as seen in Figure 4.5) are coupled through an area of mutual magnetic flux, resulting in a mutual inductance. The mutual inductance is seen in the equivalent circuit representation of the power delivery network in Figure 4.6. This mutual inductance is a function of the IC/decoupling capacitor spacing (s), ground/power layer spacing, or thickness (d), and the proximity of both components to the edges of the board [16].

4.3.4. LOCAL DECOUPLING AS SEEN IN THE FREQUENCY DOMAIN

A majority of PCB PDN analysis has been done in the frequency domain. As an example, a PCB configuration that is a rectangle of dimensions 10 x 12 inches is analyzed. Port 1 simulates the location of a switching IC power pin. A movable decoupling capacitor is placed a distance, s, from Port 1. The capacitor has a value of 1_F, an ESL of 0.5 nH, and an ESR of 0.03_. Port 2 represents a somewhat random location at which the voltage of the power bus may be observed. SPICE models for this

PCB were extracted by means of a cavity model analysis tool with a circuit extraction feature [12, 13,]. This yields a lumped element model that includes the planes, ports and capacitors. The comparisons of the transfer impedance, |Z21|, between Ports 1 and 2 for different capacitor distances from Port 1 are shown in Figure 4.7 and Figure 4.8, for frequencies above 1 GHz and for separation distances between power and ground planes of 10 and 35 mils, respectively. In this figure, $L_3' = 0$, which is an exaggeratedly low value, but which accentuates the effect of the mutual coupling. (L3' is the interconnection inductance of the capacitor above the power bus planes, excluding the ESL of the capacitor, as indicated in Figure 4.2.) The greater decreases in $|Z_{21}|$ in the 35 mil structure, than in the 10 mil structure, implies that the 35 mils structure is a better structure for supportino capacitor location dependent local decoupling. Thicker power bus structures inherently provide more mutual coupling between vias, hence better support for local decoupling effects.

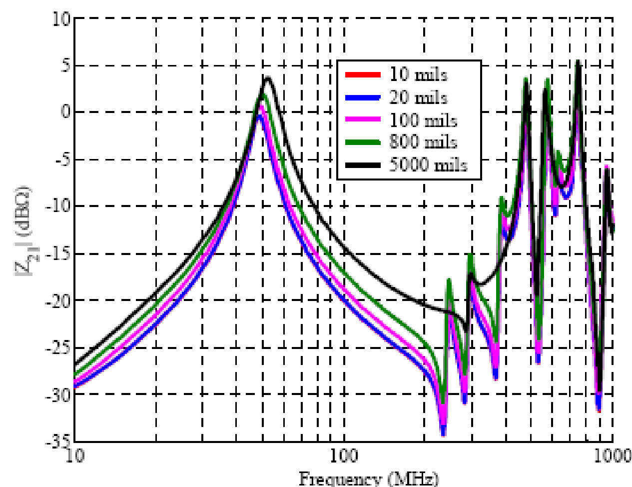

Figure 4.7. Transfer Impedance for Dielectric Thickness = 10 mils.

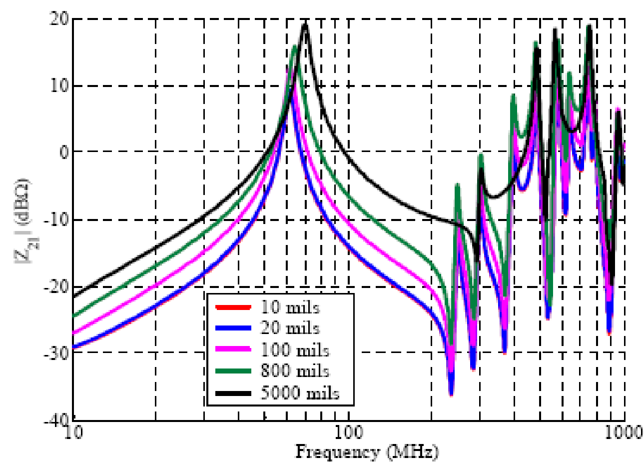

Figure 4.8. Transfer Impedance for Dielectric Thickness = 35 mils.

Two factors play an important role in expression (2), i.e., the ratio L3/L2 and the coupling factor k. The decrease in |Z21| is negligible if the vias are so loosely coupled that there is no mutual coupling, or if L3 is much greater than L2, i.e., the interconnect inductance of the via within the power/ground pair is much smaller than the sum of the interconnect inductance above the power/ground plane and the ESL. A relatively large ratio of L3/L2 is easily achieved when the distance between the power and the round plane is small; therefore thin power/ground PDN's often receive few benefits from a local decoupling strategy.

4.3.5. LOCAL DECOUPLING AS SEEN IN THE TIME DOMAIN

A different and possibly more intuitive way to examine PCB decoupling is to esamine the phenomenon in the time domain. As discussed earlier, as an IC power pin switches very quickly from a high impedance state to a low impedance state (drawing current), the initial current must come from the portion of the power bus that is able to deliver charge in a nearly instantaneous manner. This part of the power bus is either a local decoupling capacitor or the stored charge between the power/ground-reference plane pair, or some combination of the two. If sufficient current is not available quickly enough from the decoupling capacitor (due to the inductance associated with the current path) then the voltage will dip substantially, causing a noticeably higher ripple voltage and EMI 'noise'. As the decoupling capacitor is moved farther away from the IC, the

inductance associated with any current from the capacitor increases, resulting in less current provided and a higher noise level.

As shown in the previous section, the magnitude of the impedance in the frequency domain varied slightly as the capacitor is moved further away. However, this is only examining half the overall data and ignores the phase information. The time domain combines magnitude *and* phase, allowing a more complete picture of the real-world effects. To examine decoupling from the perspective of the time domain, the PCB configuration from earlier is re-examined. The simulated IC power pin, represented by Port 1, is represented by a time-dependent current source. This may not be the highest fidelity simulation of the switching power pin, but it is sufficiently accurate to be illustrative. In this case, the current source with an isosceles triangular shape that has 2 ns duration with the peak reached at 1 ns.

Figure 4.9 shows the resulting voltage at Port 2 versus time for various decoupling capacitor locations. The voltage waveforms shown are for the case of a power bus thickness of 35 mils and L3' =0 (no interconnect inductance), an ESL value of 0.5 nH, and an ESR of 0.03 Ohms. The lack of interconnect inductance is unrealistic and exaggerates the effect of capacitor location but is used in this figure for illustrative purposes. The voltage peak at Port 2 during the first cycle of disturbance is much greater when the local decoupling capacitor is very far from Port 1 than it is when the capacitor is close to Port 1. This demonstrates that the location of the capacitor is important in determining the voltage swing, ripple voltage, at Port 2 as a result of state changes at Port 1. The initial cycle of the voltage disturbance is the time period during which the IC is in most need of rapidly delivered charge. The smaller voltage swing during the initial disturbance when the decoupling capacitor is located close to the IC (s is small) is indication that the IC's initial thirst for charge is more easily satisfied when the capacitor is close to the IC pin than when it is far away. This is consistent with the previous discussion. The values of the coupling coefficient, k, are noted for each value of distance between the vias.

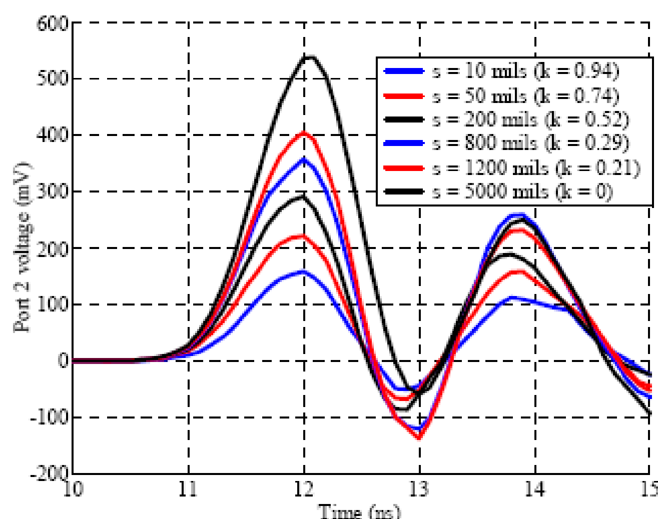

Figure 4.9. Time Domain Noise Pulse for Different Decoupling Capacitor Distances.

The thirst for charge during the initial cycle of disturbance is important to the functionality of the IC. This time dependency of the voltage disturbance that comprises the power bus ripple is not so intuitively apparent when examining decoupling in the frequency domain [20]. It should also be noted that although the power bus planes and decoupling capacitor values and locations may be designed to supply charge to the IC and lower the power bus impedance, it can also be simultaneously true that insufficient charge is available to meet the demand of a particularly charge-thirsty IC. In this case, functional difficulties may result as the device may experience output waveform distortion. This is a topic beyond the scope of this paper.

Figure 4.10 shows the change in peak voltage, ΔV_p, in this initial disturbance period at Port 2 vs. distance between the capacitor and Port 1 (simulated IC power pin. The capacitor has an ESL of 0.5 nH and an ESR of 0.03 Ohms. A larger change in peak voltage indicates a larger dependency on location of the capacitor. From Figure 4.11, it is clear that for the thicker power bus, d = 35 mils, the power bus voltage at Port 2 has a greater dependency on the proximity of the decoupling capacitor than the thinner power bus.

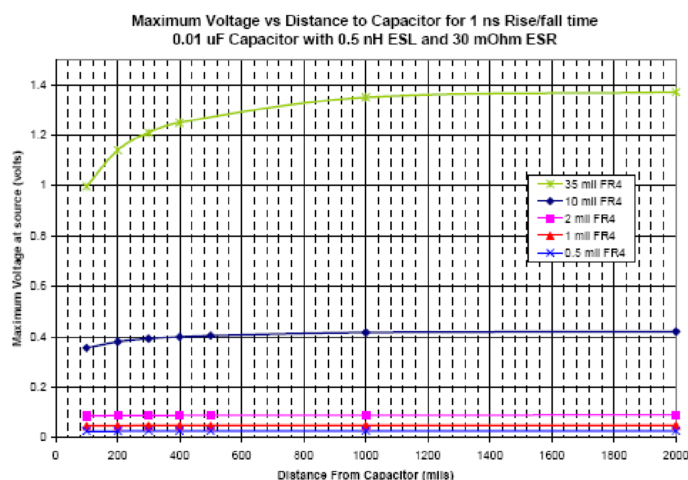

Figure 4.10. Comparison of Maximum Time Domain Voltage for Different Decoupling Capacitor Distances and Dielectric Thicknesses.

Table 4.1 shows interesting effects when the power bus is not centered in the PCB stackup as shown in Figure 4.11. When positioning a power bus off-center in the stack-up, two power buses must be used in order to maintain PCB symmetry, or at least an identical two plane structure. The figure shows such a PCB with two power buses, each with a thickness of 10 mils. The IC is mounted on the obverse surface of the PCB with decoupling capacitors mounted on either observe or reverse sides of the board. The table shows the effects of moving a 10 mil power bus near the obverse surface of the PCB in terms of the L3/L2 ratio. The decoupling capacitor on the obverse surface of the PCB has relatively short via lengths that form L3'. The capacitor on the reverse side requires relatively long via lengths to reach the power bus connected to the IC. Table 4.1 shows that the ratios of L3/L2 are vastly different depending on the surface upon which the capacitor is mounted. A capacitor ESL value of 0.5 nH was used when calculating L3. When the capacitor is mounted on the obverse surface L3/L2 is less than three, indicatine the potential for effective local decoupling. However, when the capacitor is mounted on the reverse surface, L3/L2 is greater than nine, indicating slim possibility of effective local decoupling. Hence, the position of the power bus in the PCB stack-up, along with placement of the capacitor can be very important in achieving effective local decoupling.

Figure 4.12 shows the proper ways to place SMT decoupling capacitors near IC power pins in order to increase the mutual inductance between capacitor and IC vias,

hence to take best advantage of local decoupling behavior. The four examples include all combinations of capacitors on top or bottom and power plane above or below the ground plane. (The terminology “top’ and “bottom” refer to the obverse and reverse sides of the PCB, which is often characterized by layer numbers in the PCB stack-up, layer 1 is near the top, etc.). The conclusion is that the IC power or ground pin and SMT capacitor should be placed so that the longer vias are proximate (regardless of there label as “power” or “ground”). This increases the mutual coupling and gives greatest weight to local decoupling behavior [21].

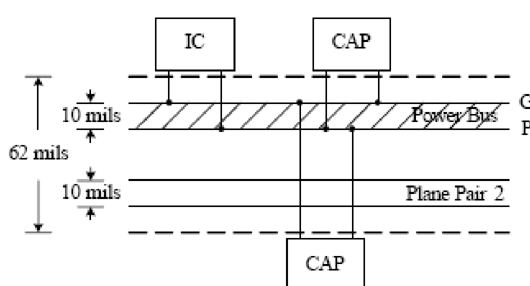

Figure 4.11. Capacitor Mounting on Top/Bottom of PCB.

Table 4.1 Inductance from Capacitor Mounting on Top/Bottom of PCB.

DeCap Placement	L3' (nH)	L3/L2
Obverse	0.45	2.96875
Reverse	2.56	9.5625

Figure 4.13 shows the “wrong” ways that one could place the decoupling capacitor, corresponding to Figure 4.12(a). From this one can extrapolate the configurations shown in Figure 4.13 to obtain the “wrong” ways to place the decoupling capacitor in those configurations. The rule is that if the longer vias are not proximate, the placement is wrong in the sense that the mutual inductance between the vias is not maximized; hence the potential for local decoupling is not maximized [16].

So, how close must a decoupling capacitor be to the IC pin to achieve effective local decoupling? No simple answer can be given to this question because the performance of a local decoupling capacitor depends on the power bus thickness, d, the

inductance ratio, L3/L2, and the IC/capacitor spacing, s. As a rule of thumb, however, for a 35 mil thick power bus structure with a favorable L3/L2 ratio (3, or less), a 3 dB decrease in both port voltage and power bus transfer impedance requires a capacitor to be within approximately 200 mils, or less of the IC power/ground pin.

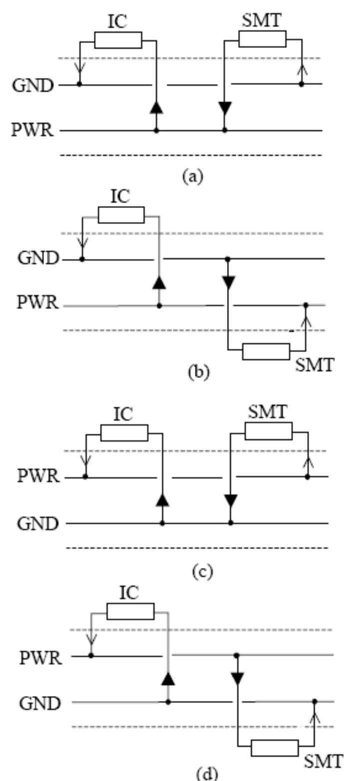

Figure 4.12. Proper Capacitor Mounting Configurations.

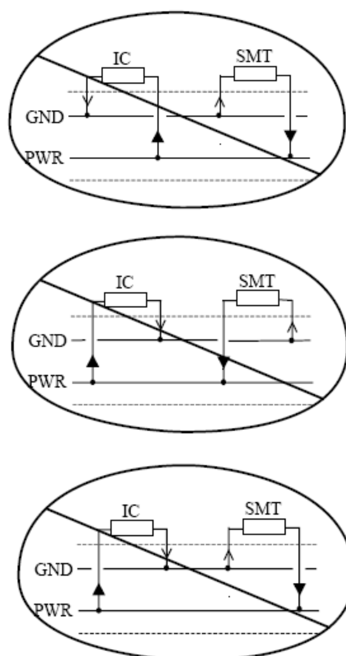

Figure 4.13. Incorrect Capacitor Mounting Configurations.

4.4. CHARGE DEPLETION AS SEEN IN THE TIME DOMAIN

The charging hierarchy described in the first paragraph ranks the effectiveness of the storage elements constituting a power delivery network in terms of speed of charge delivery and amount of charge available for delivery. While the magnitude plots of measured or simulated S or Z-parameter data provide good insights regarding the frequency range of effectiveness for each of these charging elements, as shown in Figure 4.1, these plots always provide only half of the information, the other half being contained in the phase plots. More over, the charging-discharging cycles among the storage elements, hence the time constants associated with them, can be truly appreciated the time domain. Therefore, SPICE-based time-domain simulations are used in this section to provide the same insights shown in Figure 4.1 from a time domain prospective.

A concise sketch of the charging hierarchy described in the first paragraph is given in Figure 4.14. Although, the PWR/GND plane model is represented only with the plane capacitance and inductance and all the storage elements seem to be connected to the same node, the circuit models employed in the time domain simulations take into account the distributed behavior and the relative locations of each charging element with respect to the others, as shown in Figure 4.15. Without loss of generality, the bulk

capacitor is neglected and the IC driver is replaced by a triangular current source sinking charge from the plane with a rise time of approximately 500 ps and a repetition of approximately 3 ns.

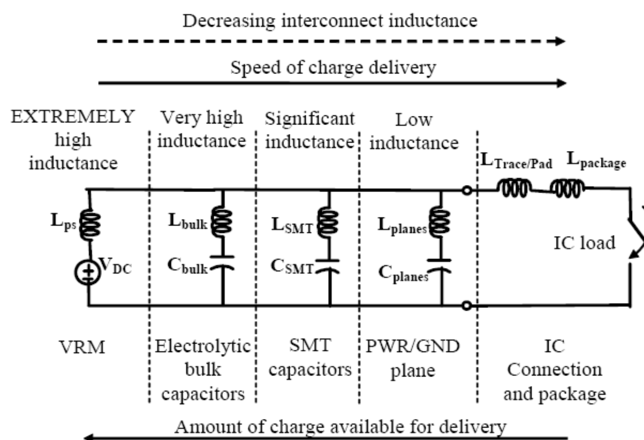

Figure 4.14. Charging hierarchy of a power delivery network.

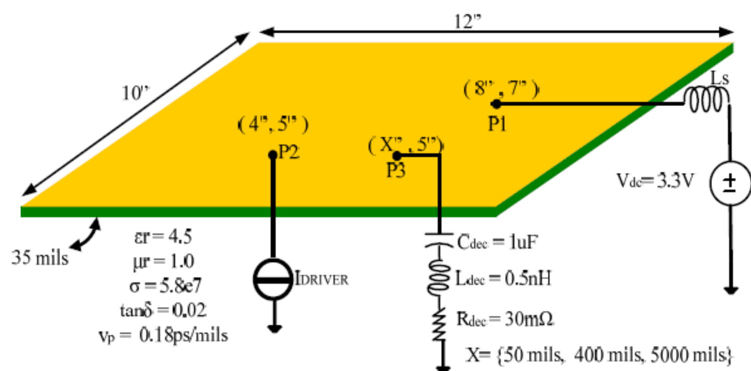

Figure 4.15. Board model under investigation.

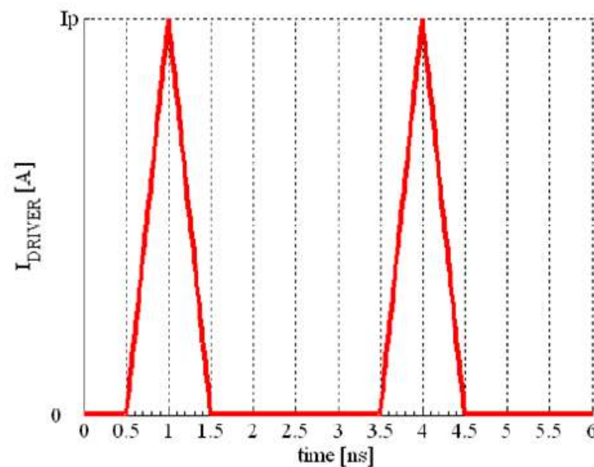

Figure 4.16. Current waveform sunk at Port 2. The peak current is chosen accordingly to the required time domain simulation settings.

The Inductance of the Port. The first set of time domain simulations deals with a phenomenon always observed in the frequency domain at high frequencies, and appreciated in the time domain during the early instants of time, i.e., the inductive behavior of a port connected between a pair of parallel planes. First of all, this frequency-domain time-domain duality is explained in terms of Fourier theory. The frequency domain voltage observed at Port 2 of Figure 4.15 is equal to the Fourier Transform of the current waveform exciting Port 2 multiplied by the impedance seen looking into the pair of plane at the same port. This self-impedance is shown in Figure 4.17 and it is characterized by a distinctive 20 dB/dec slope. This behavior corresponds to an inductive element and not to a capacitive element and a distinctive L di/dt behavior is observed in Figure 4.18(a) and (b), when simulating the circuit for the board model of Figure 4.15 in the time domain. In this set of simulations, the peak current Ip is chosen to be approximately 120 mA, the base of the triangles are 1ns and 2ns, and the repetition are 3ns and 4ns, respectively. These values are chosen to ensure a charge demand from the current source at every cycle of approximately 5‰ and 1% of the overall charge available, respectively. Hence, the pair of planes are not stressed the inductive behavior becomes the most relevant feature to be observed. The amount of charge available from the plane is about 12nC (3.3V x 3.5nF), whereas the amount of charge depleted from the

planes each cycle is about 60pC and 120pC, respectively. Finally, the decoupling capacitor is disconnected during this first set of simulations.

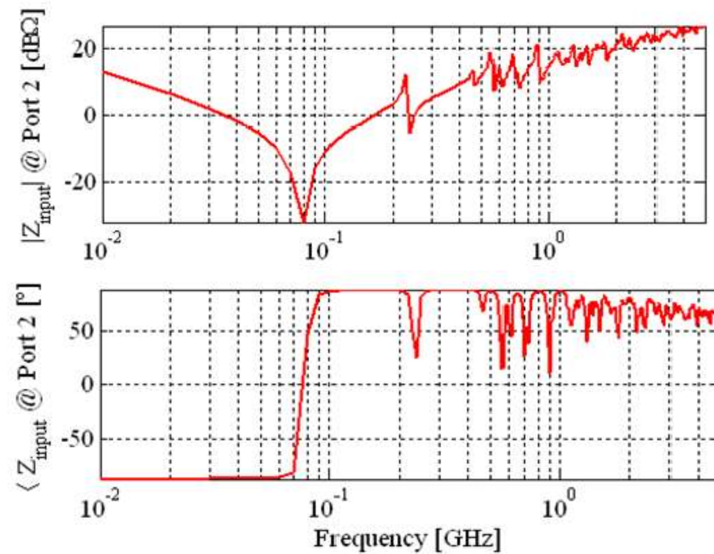

Figure 4.17. Self-impedance, magnitude and phase, looking into Port 2 of Figure 4.15.

As soon as the voltage across the planes is settled to about 3.3 V, the current (noise) source is switched on with the shape and the repetition shown in Figure 4.18(a) and (b) – lower red curves. The amount of charges depleted from the plane is very small, hence the mean value of the voltage does not deviate significantly from the steady state value of about 3.3V. On the other hand, the amount of charge per unit time, i.e., the current flowing into Port 2 is able to create an Ldi/dt type of voltage drop. When the current is on the rising edge, the voltage decreases, when the current is on the falling edge, the voltage swings back overshooting above the mean value of 3.3V. The inductive behavior of the port is further demonstrated by observing halved voltage dips and peaks, when the triangle base is doubled from 1 ns to 2 ns, Figure 4.18(b) *vs.* Figure 4.18(a).

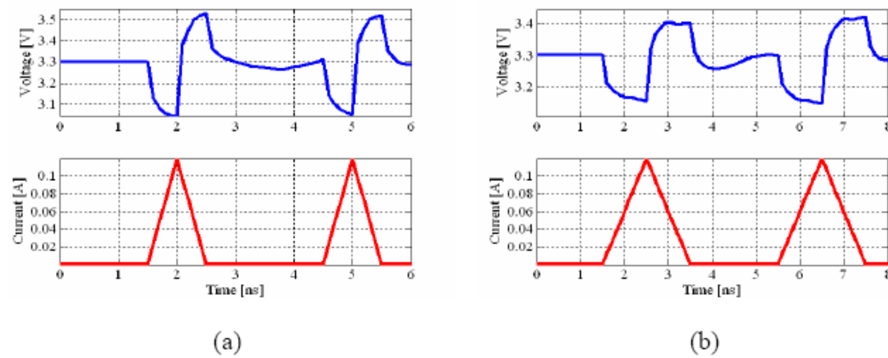

Figure 4.18. Triangular current at Port 2 for (a) 1 ns base; (b) 2 ns base. The corresponding inductive voltage drop is observed at the terminals of Port 2.

The Effect of the Inductance Ls. The second set of time domain simulations deals with the charge/discharge issues associated with only the voltage supply and current source, connected at Port 1 and Port 2, respectively. The charge depletion from the plane needs to be large, now, in order to appreciate the charge/recharge mechanism. The peak current is then increased to 5A and each triangle of 1 ns encloses approximately 22% of the overall charge available between the pair of planes. When the current driver is switched on, the voltage across the plane starts decreasing from 3.3 V. Every cycle the voltage decrease due to a constant drawing of charge at Port 2. The voltage sag stops when the voltage supply senses this reduction and it starts supplying charges to restore the 3.3V steady state voltage. An oscillation is then triggered due to the series inductance of the voltage supply and the capacitance of the planes. This oscillation is slowly damped until a new steady state is reached again. The voltage across the planes for three configurations characterized by three different values of voltage supply series inductance are shown in Fig.19. The oscillation frequencies for each of the cases given in Fig.19 are calculated and reported in Table 4.2.

Table 4.2. Resonant frequencies associated to oscillations observed in Figure 4.19.

L_s (C_p = 3.5nF)	$f_{res} = \frac{1}{2\pi\sqrt{L_s C_p}}$	$\tau = \frac{1}{f_{res}}$
1nH	~ 83MHz	~ 12ns
10nH	~27MHz	~37ns
50nH	~12MHz	~83ns

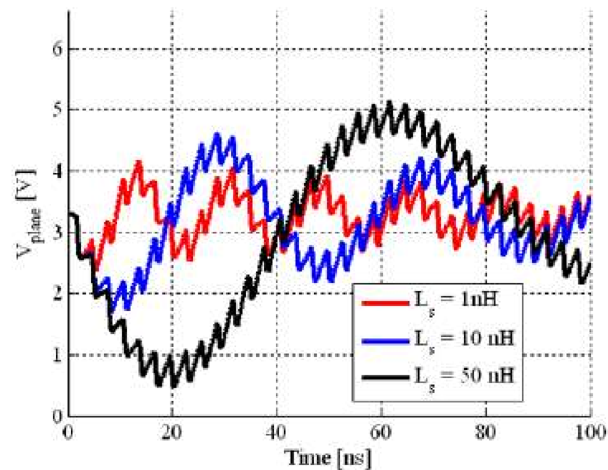

Figure 4.19: Voltage observed across the plane pair of the board model given in Figure 4.15 for different voltage supply series inductance.

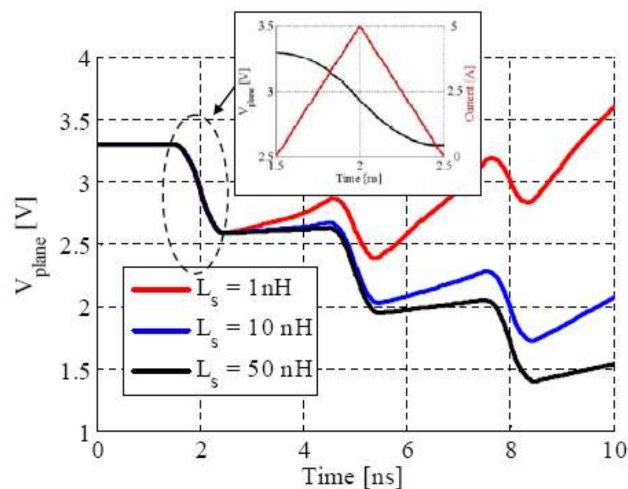

Figure 4.20. Close up of the voltage given in Figure 4.19.

The close up view shown in Figure 4.20 provides additional insights on the charge depletion mechanism due to the current sunk from the driver. When the current driver is switched on at *t* equal to 1.5 ns, the voltage between the planes (at this location) starts decreasing in a quadratic fashion. During the duration of the first current pulse - 1ns – the voltage must sag of about 22%, since the charge associated with each triangle is about 22% of the total plane charge and there are no other source of charges in a radius of 1 ns in proximity of the driver. The level reached by the voltage across the plane at *t* equal to 2.5 ns is in fact 2.58V, which is approximately 22% smaller than the steady state value of 3.3V.

As soon as the disturbance reaches the voltage supply, this storage elements reacts by supplying charges in order to re-establish an equilibrium. Depending upon the value of series source inductance, this charge supply is slowed down and the voltage across the plane continues to sag especially for the configurations characterized by large values of series inductance. On the other hand, when the voltage supply has a low value of series inductance, this storage element can supply charge as fast as the velocity of propagation allows it.

The Benefits of Decoupling. The conclusions drawn from the previous sections are very helpful to introduce the final set of time domain simulations. These are carried out by employing a current driver with a triangular pulse of 5A peak current and a base of 1 ns with 3 ns repetition, a 3.3V voltage supply with a 50nH series inductance and a decoupling capacitor of 1 uF with 30mΩ ESR and 0.5nH ESL at 50 mils, 400 mils and 5000 mils from the current source along the x direction as shown in Figure 4.15. The system is charged up until all the components connected to the planes have reached a steady state voltage of about 3.3V, then the time varying current (noise) source is started.

A first comparison between the case with no decoupling capacitor and decoupling capacitors at different locations is shown in Figure 4.21. As expected, placing a decoupling capacitor across the pair of planes helps maintaining the voltage swing within tighter bounds. Several charge/discharge mechanisms are now possible, i.e., from the voltage supply to the planes, from the voltage supply to the decoupling capacitor from the decoupling capacitors to the planes. More over, each of these mechanisms has its own characteristic time constant. For instance, the voltage supply – plane pair charge exchange mechanism is characterized by the same time constant described before for a 50nH source inductance, i.e., approximately 83 ns. The voltage supply – decoupling capacitor charge exchange mechanism is characterized by a time constant of about 1400ns (freq = 0.7 MHz from C = 1 uF and L = 50 nH). Finally the decoupling capacitor plane pair charge exchange mechanism is going to be characterized by a time constant in the order of 13 ns, due to the inductance of the full capacitance interconnection, approximately 1.2 nH, and the plane capacitance, approximately 3.5 nF. The capacitance ratio between the decoupling capacitor and the pair of planes is about 300, hence the

charged decoupling capacitor is like a constant voltage source with a small interconnect inductance for the parallel plane.

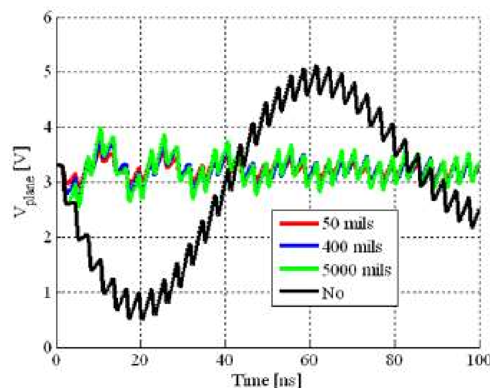

Figure 4.21. Voltage observed across the plane pair of the board model given in Figure 4.15 for different locations of the decoupling capacitor or no decoupling capacitor.

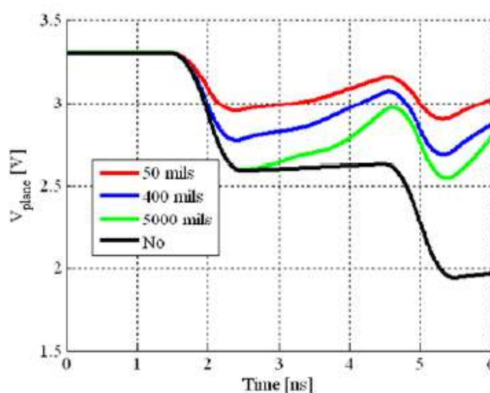

Figure 4.22. Close up of the voltage given in Figure 4.21.

The expanded view of the early time (first few current pulses) shown in Figure 4.22 provides additional insights regarding the effectiveness of the decoupling capacitor location to replenish the charge locally across the pair of planes. For instance, when the decoupling capacitor is located within 50 mils it is able to begin to replenish the charge within the first few hundreds of picoseconds, and the nominal voltage only decreases to about 2.95 volts. As another example, when the decoupling capacitor is located five inches away, it can begin to replenish the local charge only after a much longer time, and the voltage decreases to approximately 2.6 volts and only raises to about 2.95 volts bifore the next current pulse occurs. If the second current pulse had occurred sooner, then the

voltage would have not risen as high. In the case of no decoupling capacitor, the charge must be replenished from the supply (which is highly inductive), and the charge never reaches this point in the planes before the second current pulse occurs, further depleting the local charge.

4.5. CONCLUSION

This paper has provided a discussion of the various aspects of the decoupling capacitor and how it relates to providing charge to ICs on PCBs. Signal integrity engineers and EMC engineers often view the role of a decoupling capacitor from different points of view, but the capacitor actually functions to serve both purposes. The importance of the value of the decoupling capacitor and more importantly, the amount of inductance introduced by physically connecting the capacitor to the PCB planes is examined. This connection inductance dominates the performance of the capacitor, making the actual value of capacitance of small importance for most real-world PCBs.

The role of the capacitor as a charge storage device, and the amount of time needed to provide that charge is examined to indicate if the location of the decoupling capacitor is important. Again, the connection inductance dominates the capacitor's ability to provide the charge to an IC *during the time it is needed*, making the location of the decoupling capacitor seem unimportant, since the inductance associated with the capacitor's charge will usually be significantly higher than the charge stored between the planes.

And finally, the role of the capacitor as a charge source to recharge the depleted planes is discussed, and the location of the decoupling capacitor is shown to be very important to maintaining a small noise voltage fluxuation in the local area near the IC drawing the current.

4.6. REFERENCES

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5. DIFFERENTIAL VIAS TRANSITION MODELING IN A MULTILAYER PRINTED CIRCUIT BOARD

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5.1. ABSTRACT

In this paper a 26-layer printed circuit board including several test sites has been analyzed. All the sites have a transition from coupled microstrips to coupled striplines through signal vias. Differential measurements have been performed on some of these test sites to estimate the effect on S-parameters and eye diagrams due to via and antipad radius variation, and different lengths of via stub. At the same time, a physics based circuit model has been assembled in a spice-based simulation tool and a full-wave model has been generated as well. The simulation results have been compared with the measurements for both differential and single ended cases. A brief discussion about possible issues associated with fabrication tolerances is presented in the last chapter.

Keywords—Differential signal, noise coupling, signal and power/ground nets, signal via transition, via capacitance, cavity model, ground vias.

5.2. INTRODUCTION

The main purpose of this paper is to show how a complex geometry with several layers can be simulated quickly using a combination of cavity model and circuit based tools as ADS or HSPICE. It will also be shown that fabrication tolerances can have a very large effect on the resultant S-parameters. The increasing complexity of modern PCBs with a larger and larger number of layers and very thin dielectric often creates problems in modeling these structures with full-wave tools. The minimum mesh step to

represent all the particulars in the structure with good detail should be very small; this means that for a large PCB several million cells are probably needed. Of course, this will likely lead to many hours of simulation time; if the goal is to perform parametric simulations it is better to avoid large memory usage and computational resources. A circuit model can be made based on the geometry to get very quick results and, therefore, control quickly parametric variation of some variable to more easily manage tolerance variations.

Cisco Systems and the UMR EMC Lab have realized the test board used in this article. The test board is a 10x10 inches PCB with several small test sites where differential via transitions are present. The backplane is divided into 5 main areas based on via and antipad diameter, via pad diameter, microstrips and striplines shapes and ground via location and shows a 26 layers stack-up with 12 solid copper planes. First, a series of sites having the same via diameter and without ground vias close to the signals have been milled to show the microstrips and striplines pads. Next, a series of differential measurements were performed using microprobe station and network analyzer to extract S-parameters. At the same time the circuit model has been made. A current signal propagating between top and inner layers and coming back to the source meets several "obstacles" so that the S-parameters show many resonances meaning that the signal propagation depends strictly on the frequency.

After the model realization, an S-parameters comparison was done between differential measurements, circuit model and Microwave Studio.

5.3. PCB TEST GEOMETRY AND MEASUREMENT SETUP

In Figure 5.1, the PCB area with the sites of interest is shown. The label "P" visible on each site is related to the via-to-via distance, the "D" is associated with via diameter and the "L" is followed by the layer where striplines are connected. Although many sites have been milled, only P2-D1 test sites have been studied in this paper; the nominal via diameter for these geometries is 22 mils with an antipad diameter of 50mils. The distance between the two vias, center to center, is 60 mils.

The PCB stack-up is shown in Figure 5.2. The geometry consists of 26 layers with 12 copper solid planes and 12 possible positions to connect the traces; four via stub lengths are visible in Figure 5.3.

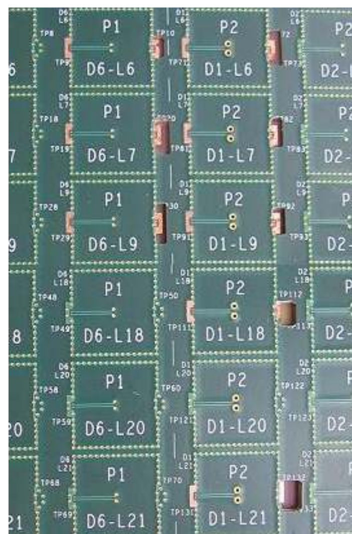

Figure 5.1. Top view of P2-D1 series of test sites

With these test structures, it is possible to study only microstrip to stripline transitions and not stripline to stripline. All the test sites are separates each other by means of several ground vias those limit the field propagation inside a confined small region 500x500 mils large.

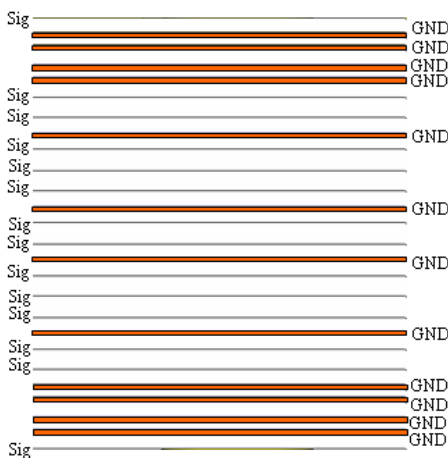

Figure 5.2. Board Stack-up

To perform differential measurements an Agilent 8720ES with an ATN 4110 test set operating at 40 GHz was utilized. The maximum frequency selected to compare measurements and simulations was 18GHz due to the maximum frequency allowed by the microprobes.

The microprobes used are Cascade 500um pitch ACP probes and the microprobe station is a Cascade analytical probe station.

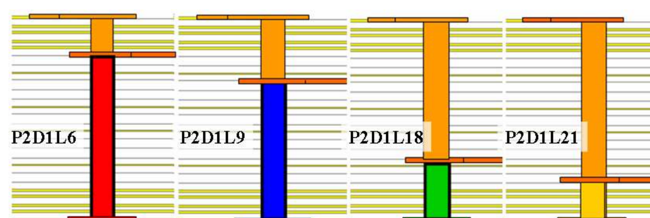

Figure 5.3. P2-D1 test sites for different stub lengths

The test sites were milled out to expose the launching structures and allow the signal to smoothly transition from the probe to the device under test. Figure 5.4 shows a cross-section of one of the sites that has been milled from top to 21st layer

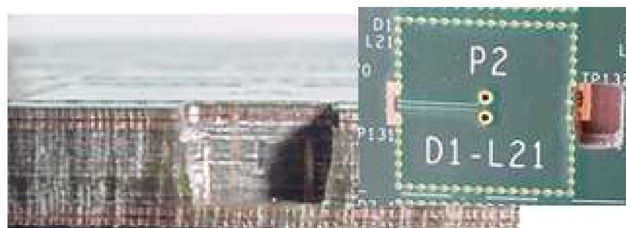

Figure 5.4. Detail of test site P2-D1-L21and cross-section on launching structure

5.4. MODELING APPROACH

The segmentation method is the approach used in this paper. The main idea is to divide the whole stack-up into several subsections, each corresponding to one solid power/ground plane pair [1,2]. Each block is then modeled using the cavity model theory; this method has been widely validated in previous publications and allows an accurate evaluation of the power-plane impedances [3]. At the end, the blocks are linked by enforcing current and voltage continuity conditions across the via-to-antipad region. This assumption is valid since it is possible to define interconnection ports across the antipads: in the antipad region the field is considered purely TEM since it shows a coaxial

geometry. Using this approach saves time and computational resources compared to the classical full-wave models. Furthermore, a physics-based circuit model relates geometric features to circuit elements in a manner that it is easy to optimize the design and integrate the whole structure with external components as ICs or decoupling capacitors. With this kind of circuit, it is possible to perform simulations in both frequency and time-domain; complex structures where tens of power plane pairs and vias are supported as imposed by modern PCB design.

The differential circuit model is composed of four main parts: transmission lines (coupled miscrostrips and striplines), transmission line-to-via transition, antipad capacitances and cavities as shown in Figure5.5. Coupled microstrips and striplines have be represented using a cascade of Π cells since the coupled transmission lines model implemented in ADS does not consider a reference for the return path and the maximum frequency of interest does not allow to represent the traces as simple single lumped element. As for the transition from traces to via, different effects as capacitive and inductive coupling between the non-TEM part of the traces, the two via pads and pad-solid plane have been computed for the geometries P2-D1 (related to a via radius of 11 mils and antipad radius of 22 mils nominal) using full wave methods. The capacitances across the antipad between vias and copper solid planes were calculated using an empirical formula based on curve fitting.

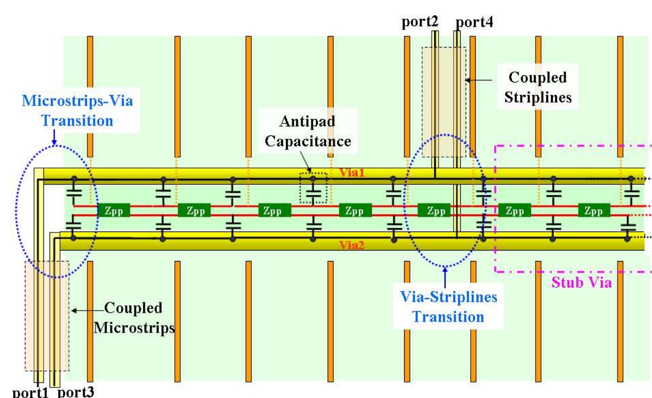

Figure 5.5. Geometry and equivalent circuit model

To represent the power-plane impedance, including frequency dependent metal and dielectric losses, reflection at boundaries and mutual inductive effects between the two vias, a tool based on cavity model has been utilized.

During the process of modeling and measurements, several difficulties have been encountered due to the complexity of the board. In this geometry, within the same power-plane pair more than one dielectric is present. In addition, those dielectrics have frequency-dependent properties. In the simple cavity model approach those aspect are not included so a model that take into account a series of Debye material in the same cavity has been developed. In Figure 5.6 the effect of implementing frequency dependent material on the simulated insertion loss is shown for test site P2D1L6.

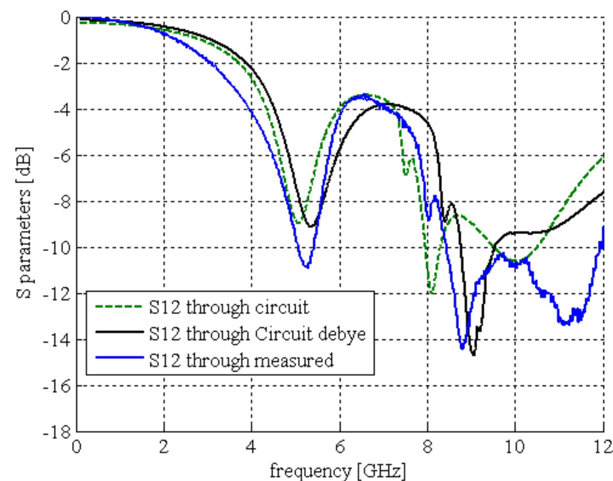

Figure 5.6. $|S_{12}|$ including Debye materials

Another problem is related to measurement. The S-parameters data violated passivity in almost the entire frequency range, especially above 5 GHz, possibly due to calibration errors or bad contacts.

5.5. MEASUREMENTS AND SIMULATIONS COMPARISON

First, the test site P2-D1-L6, with a transition from top to layer 6, was modeled using the circuit approach and with CST Microwave Studio. The amplitude of the S_{12} (thru) parameter is shown in Figure 5.7.

It can be seen form the curves that there is a good agreement between circuit model and measurements to about 10GHz.

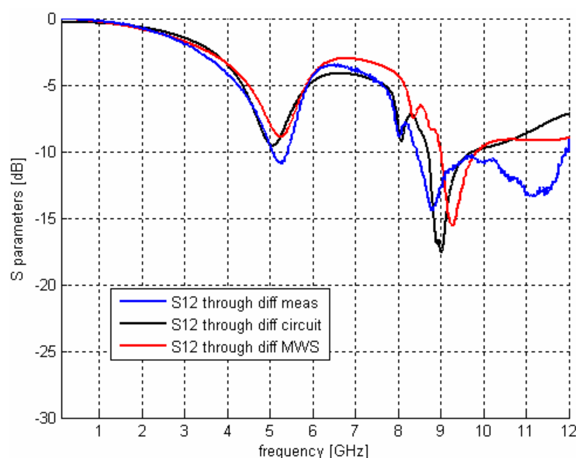

Figure 5.7. $|S_{12}|$ Measurements vs. simulations

The full-wave model is able to get more precisely the 5 GHz resonance than the circuit but above 6 GHz the black curve seems closer to the measured values. At those relatively high frequencies is evident from the Microwave Studio model that the model used for the material does not represent correctly the real physics.

Another interesting thing to notice is the big resonance at about 5GHz, a frequency where the actual bit-rates can easily show some harmonics. In Figure 5.8, all the power plane impedances $|Z_{11}|$, where port 1 is referred to one of the vias in the single cavity, are shown in the same plot of the simulated $|S_{12}|$, where port 1 and 2 are the ports shown in Figure 5.5. Notice that in the plot the $|S_{12}|$ curve is shifted 40dB up for the sake of visualization.

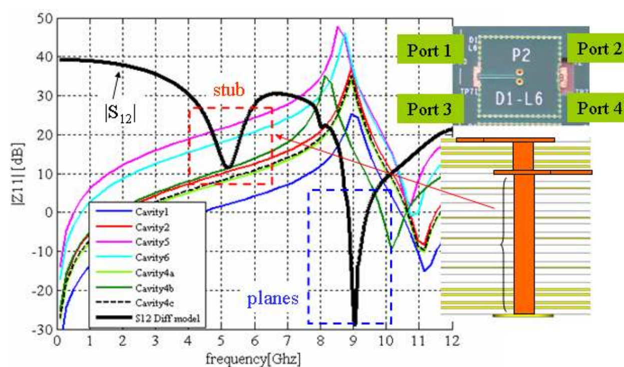

Figure 5.8. $|S_{12}|$ overlapped with all the plane impedances $|Z_{11}|$

Since all the resonances associated to the reflection at the boundaries (colored curves) are between 8 and 9 GHz, it can be concluded the big dip at 5GHz in the global $|S_{12}|$ (black curve) is due to the via stub length, about 70 mils in this particular case.

Figures 5.9 and 5.10 are associated with four test sites where only the length of the stub was varied. Figure 5.9 is associated with circuit simulations and Figure 5.10 with measured results. The red curve is a top to layer 6 transition, the blue a top to layer 9, the green top to layer 18 and the orange a top to layer 21. In both model and measurement there is a noticeably large shift toward higher frequencies when the stub length decreases. In particular, a huge difference of about 2.5GHz is observable when the stub length decreases from 70mils (site P2D1L6) to 20mils (site P2D1L21).

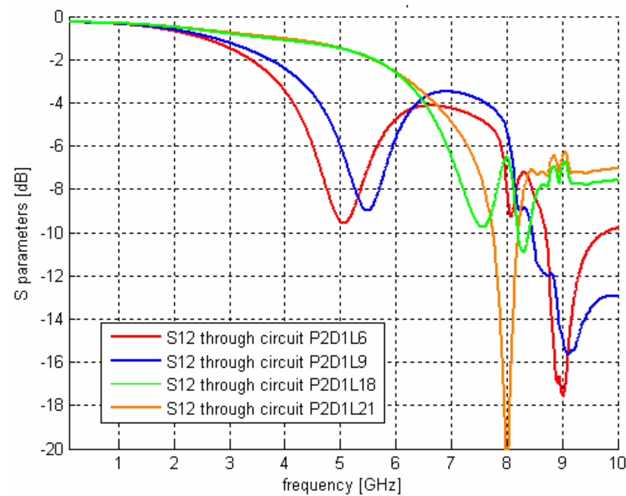

Figure 5.9. $|S_{12}|$ simulations varying stub length

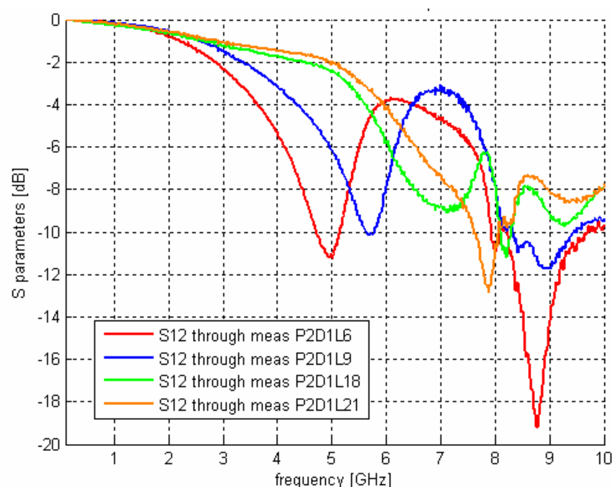

Figure 5.10. $|S_{12}|$ measurements varying stub length

Examining the differential mode |SDD12|, the effect on the stub resonance is strongly reduced and only the plane resonances are evident.

In Figure 5.11, for the P2D1L6 case, this effect is clearly visible: in the measurement there is only some residual stub effect at about 5.5GHz. In the model results, where the conditions are ideal, the low frequency dip disappears completely.

Examining the phase of the differential mode in Figure 5.12, a discrepancy can be observed between the model and measurement starting at relatively low frequencies. This means possible large differences when a time-domain analysis is performed.

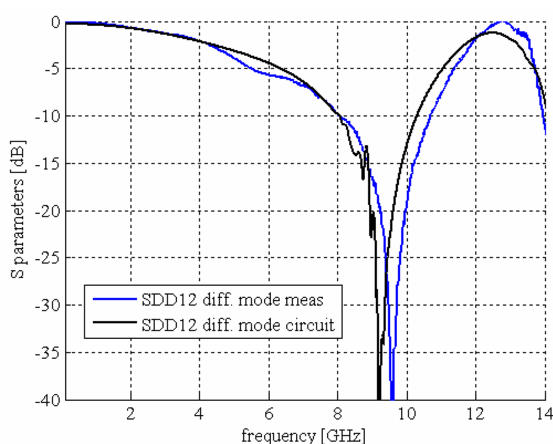

Figure 5.11. $|S_{DD12}|$ measurements vs. equivalent circuit model

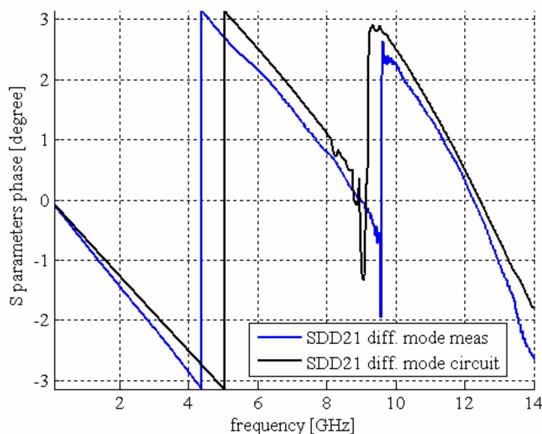

Figure 5.12. Phase of SDD_{12} measurements vs. equivalent circuit

To demonstrate this effect, the S-parameter files associated with measurements and simulations have been loaded in a Link Path Analyzer tool to simulate eye diagrams [5].

A data pattern K28.5 with two different data-rates was used, 50 samples per bit and a rise-time of 10 ps have been set. In Figure 5.13 the model and simulation eye diagrams are shown for a 3.5 Gbit/s bit-rate corresponding to the 5th harmonic of the input signal going into the 9GHz dip.

The same pattern was used as the input in Figure 5.14; however, the bit-rate was increased to 6.3Gbit/s so that the third harmonic is delivered to the 9 GHz dip.

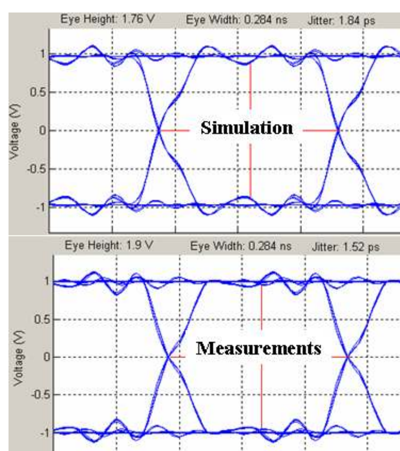

Figure 5.13. Eye diagram for a 3.5Gbit/s pattern based on simulated and measured S-parameters

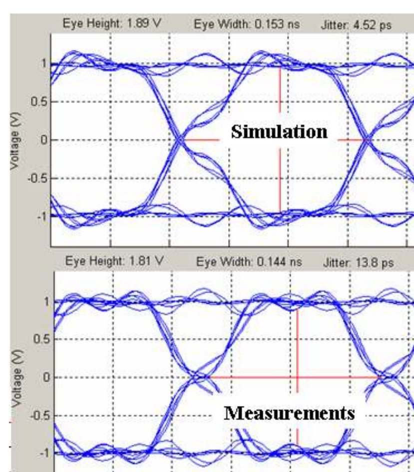

Figure 5.14. Eye diagram for a 6.3Gbit/s pattern based on simulated and measured S-parameters

It can be seen in Figure 5.13 that the model and measurement are consistent in terms of height, width and jitter. For the higher data-rate case, however, a large difference in jitter is present: 4.52 ps in the simulated data and 13.8 ps in the measured data. This discrepancy is most likely a result of the phase difference previously shown in Figure 5.12.

5.6. EFFECTS OF TOLERANCES ON MODELING

The impact of a +/- 20% variation in the dielectric constant is shown in figure 15 and a +/- 20% variation of via-to-antipad capacitance in Figure 5.16. This has been done to study the effect of possible fabrication tolerances in the material and especially in the via placement process. Observation of the geometry cross-section shows relevant changes in the via geometry compared to the nominal values. An offset with respect to the vertical axis has been observed, as well as a large offset with respect to the nominal via center. Obviously, these geometric variations strongly affect the results since even a 20% variation in the via-to-antipad capacitance can generate an approximate 200MHz shift of the 5GHz stub-related dip as shown in Figure 5.16.

Figure 5.15 shows that modification of the dielectric constant has a relevant impact on the plane-related 9.5 GHz resonance in the amplitude of the differential mode $|S_{DD12}|$. It is apparent from the model results that the resonances always occur at lower frequencies compared to the measurements, but a dielectric constant decrease of 20% can

improve the accuracy of the circuit model, thus reducing the discrepancy with measurements from about 400 MHz to 200 MHz . This effect can be explained considering the formula relating resonant frequencies and dielectric constant in a rectangular cavity:

$$f_{res} = \frac{1}{2\pi\sqrt{\varepsilon\mu}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \quad (1)$$

where a and b are the largest and smallest dimensions of the rectangular parallel-plates, respectively; ε and μ are the dielectric constant and permittivity of the dielectric material respectively. In formula (1), the resonant frequency and the dielectric constant are inversely proportional [4].

In Figure 5.16 it can be seen that a variation in the antipad capacitance causes a shift in the 5 GHz resonance in the insertion loss S_{12} but not around 9 GHz.

5.7. CONCLUSIONS

In this paper measurements related to differential vias transitions are presented and compared with a physics-based equivalent circuit model. The impact of stub length and plane resonances on insertion loss, differential modes and eye patterns has been evaluated showing that, even in the fairly complex geometry of a 26-layer board, this approach can give acceptable results. The effect of fabrication tolerances on the S-parameters has been shown as well.

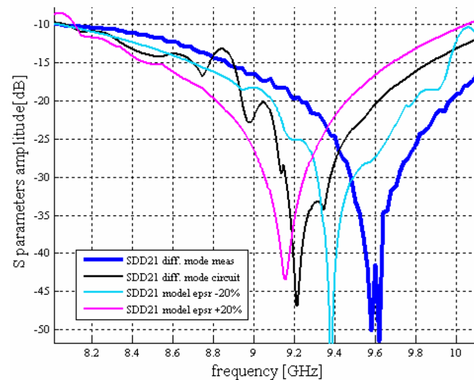

Figure 5.15. $|S_{DD12}|$ measurement vs. model varying dielectric constant value

This is additional verification that the resonances at 5GHz are directly related to the stub length. In fact, the stub resonance in the circuit model depends on the thicknesses of the cavities and port inductances but also on the antipad capacitances, calculated externally to the power plane impedances.

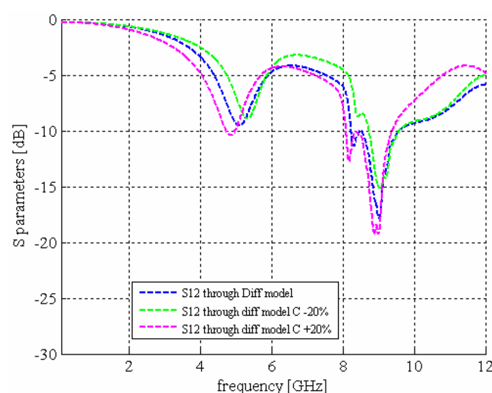

Figure 5.16. $|S_{12}|$ model varying via-to-antipad capacitance

5.8. REFERENCES

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VITA

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