Summer 2010

Control and applications of double input DC-DC power electronic converters

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Department:

CONTROL AND APPLICATIONS OF DOUBLE INPUT DC-DC POWER ELECTRONIC CONVERTERS

by

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A THESIS

Presented to the Faculty of the Graduate School of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

2010

Approved by

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ABSTRACT

Multi-input power electronic converters (MIPEC) are increasingly gaining interest in the fields of renewable energy systems and hybrid electric vehicles (HEV). The main advantage of MIPECs is their ability to interface several energy sources and storage devices using a single power conversion stage. Therefore, they provide simpler control and smaller parts count. In this thesis, various aspects of the utilization of double-input (DI) converters in solar and HEV applications are explored. For instance, a DI buckboost topology is proposed for a photovoltaic (PV)/battery energy system. The converter is controlled in a way that maximum power is drawn from the PV array using maximum power point tracking (MPPT) techniques and the additional power is drawn from the battery while keeping the output voltage constant. The capability of MIPECs to process bi-directional power in battery/ultra-capacitor hybrid system is also investigated. In addition, in order to analyze system stability and to design optimal controllers, the small signal model of the DI buck converter is developed. The developed model can also be used for the implementation of different control strategies based on the particular application. In order to effectively share power in a DI buck converter, two new control methods called the coupling control and the dead-time control have been proposed. It has been proven analytically and through small signal analysis that these methods have better dynamic performance compared to conventional methods. Power sharing in a DI buckboost converter using the offset-time control method has been implemented and experimentally verified where the offset-time between the switch commands is controlled to achieve effective power sharing.

ACKNOWLEDGMENTS

First and foremost I offer my sincerest gratitude to my advisor, Dr. Mehdi Ferdowsi, who has supported me throughout my thesis with his patience and knowledge. It has been a great experience to work under his guidance and I attribute the level of my Masters degree to his encouragement and effort. One simply could not wish for a better or friendlier supervisor.

I would also like to thank Dr. Badrul Chowdhury and Dr. Jonathan W. Kimball for serving on my committee and for being such a great source of inspiration. Especially Dr. Kimball for all the guidance and help he provided me during my thesis work. I would like to thank Dr. Mariesa L. Crow and Dr. Keith A. Corzine for being such great instructors. I am grateful to the Department Secretary Mrs. Kohout Regina for always being there and taking care of all the formalities.

I would like to thank my project partners Deepak Somayajula and Mostafa Khazraei for their valuable contribution towards the thesis. I would also like to thank my friends in the Power Group and my roommates Krutik Patel, Pankaj Pai, Nishant Chouhan, Hossien Sepahvand, Vennela Yadhati, Ajay Pappu, Mehul Madan, and Murali Baggu for their constant support and help.

I want to dedicate my thesis to my father Prabhala Narasimham Murty and mother Prabhala Vijaya Lakshmi and my late grandparents Prabhala Venkata Narasimham and Prabhala Kameswari. They have taught me the importance of education and supported all my endeavors. I would also like to thank my brother Prabhala Ravi Prasad and sister Prabhala Ratna Kameswari for being part of my support system and always encouraging me. I would like to thank all my friends and well wishers for their love and blessings.

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1. INTRODUCTION

1.1. NEED FOR MULTI-INPUT CONVERTERS

The limited supply of fossil fuels and conventional energy sources has prompted a thrust on the development of renewable energy and hybrid systems. The main advantages of renewable energy systems are that the sources are not depleted and they provide a clean alternative to the fossil fuels. However, one of the disadvantages of renewable energy sources is they are intermittent and not reliable thus limiting the optimal utilization of these sources. For example, in solar and wind based renewable energy generating systems the generation depends on the amount of solar insolation available and the weather which is highly uncertain. For this purpose, these sources are needed to be combined or hybridized with more reliable sources of energy and energy storage devices (e.g. batteries). In addition, a storage element is required to act as an energy buffer during transients in the system thus improving the dynamics of the overall system. Again the storage element compensates the mismatch in power between the source and load.

Thus, for a hybrid energy system, it is highly beneficial to develop a power management system which integrates different power sources and storage elements and combines their advantages through a single power conversion stage. Multi-input power electronic converters (MIPEC) find applications in these types of hybrid systems where they interface several power sources and storage devices. A battery source combined with a PV (photovoltaic) source can be one such application. In hybrid electric vehicles (HEV), it is desired for the energy source to have high power density as well as high energy density to cater for sudden changes in the load demand. Batteries have high

energy density but have low power density while ultra-capacitors have high power density but have low energy density, thus an ideal source for HEV would be the combination of both these sources. A MIPEC can be used to combine both these sources to utilize the high energy density of the battery as well as the high power density of the ultra-capacitor. A bi-directional MIPEC can be utilized for recharging the ultra-capacitor during regenerative braking.

1.2. CONVENTIONAL APPROACH VS. THE NEW APPROACH

Several topologies have been explored to interface multiple energy sources with a common load. The authors in [17-24] propose several converter stages in parallel with separate dc-dc converters for individual sources. The converters are connected to a common dc bus and have to be controlled independently. Several such converters like the interleaved boost converters [1], phase-shifted full-bridge converter [2], three-phase converter [3], current-fed push–pull converter [4] have been developed. The main disadvantage of these systems is that they are complex and have high cost due to several converter stages. They need a common dc bus and have separate control for each conversion stage making it much more difficult to control. Figure 1.1 shows the conventional structure for interfacing multiple energy sources.

Instead of using several power stages, it is more advantageous to use a single power processing stage which integrates several inputs to form a hybrid source. A MIPEC can be used to interface several power sources and storage devices (shown in Figure 1.2). In this structure, the system voltage is regulated and the power flow between the energy sources and storage devices can be controlled. This structure removes the need

for redundant power stages of the conventional structure and thus results in lesser parts count. MIPECs have integrated power management, efficient thermal management, and centralized control compared to a conventional structure. The overall system efficiency is increased due to the elimination of the redundant elements and their associated losses.

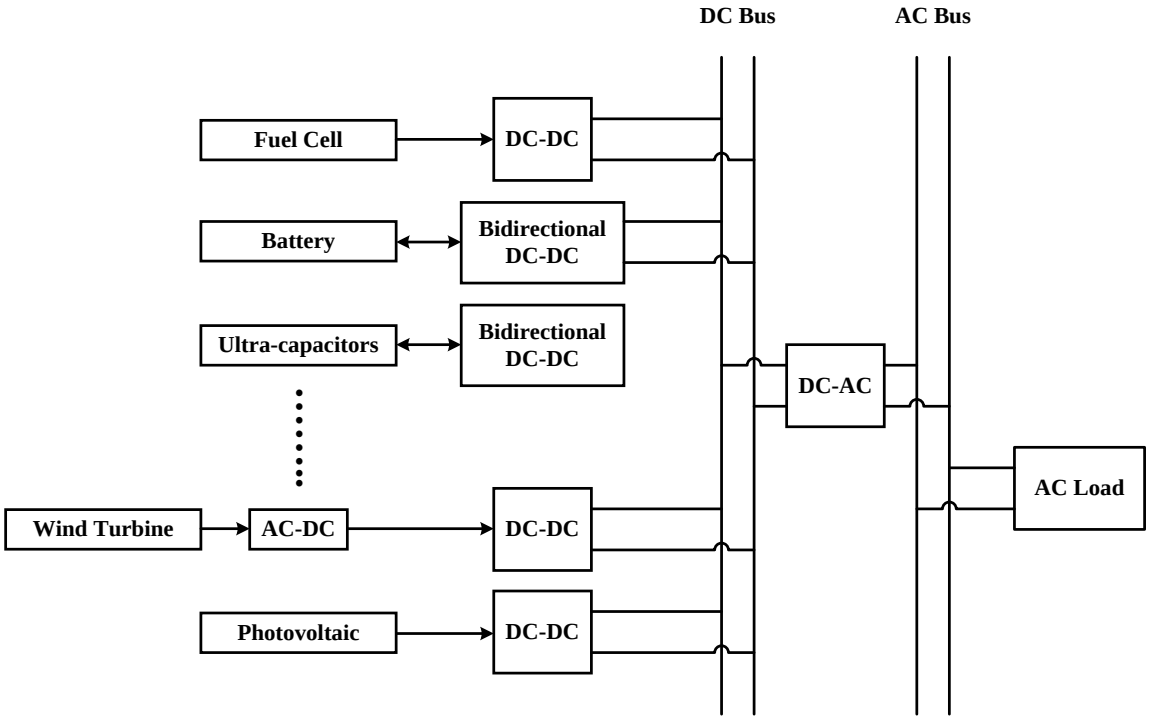


Figure 1.1. Conventional structure for interfacing multiple energy sources.

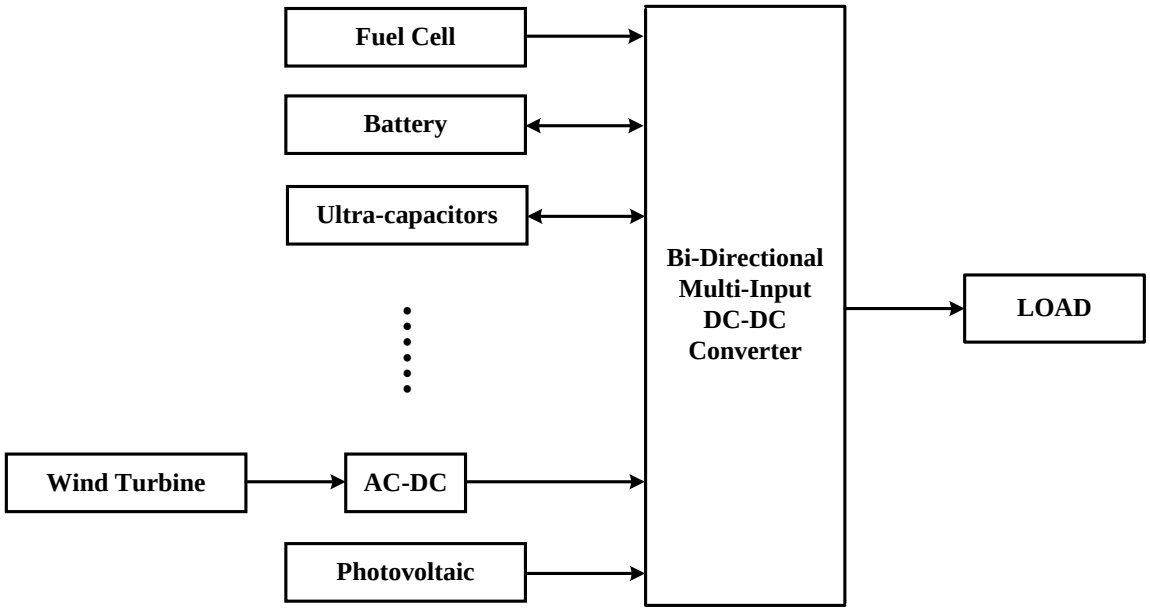


Figure 1.2. Multi-input (MIPEC) power electronic converter for interfacing for hybrid systems.

Control of converters connected in parallel is difficult and they have limited operating region. For example, in a multi-input parallel buck converter (shown in Figure 1.3) with two input voltages V_1 = 100 V, V_2 = 80 V, and constant output voltage V_0 = 40 V, the duty ratio for input source 1 has to be D_1 = 0.4 and for input source 2, the duty ratio is D_2 = 0.5 given by equation (1.1). Whereas, for a double-input (DI) buck converter (shown in Figure 1.4) with output to input voltage relationship given by equation (1.2), the duty ratios D_1 and D_2 can vary over a wide range to keep the output voltage constant.

$$V_0 = D_1V_1 \text{ and } V_0 = D_2V_2 \tag{1.1}$$

$$V_0 = D_1V_1 + D_2V_2 \tag{1.2}$$

In HEV applications with one of the sources as battery and the other being the ultra-capacitor, the battery supplies constant power and the additional load demand is supplied by the ultra-capacitor while regulating the output voltage. The power supplied

by the batteries depend on the state of charge (SOC) of the battery, thus, for change in power drawn from the battery the power supplied by the ultra-capacitors should also be changed while keeping the output voltage constant. With parallel interleaved converters this is not possible as both the sources have to supply constant power to regulate the output voltage. Thus, effective power sharing can be achieved by MIPECs depending on the control strategies. Moreover, the control of parallel converters is complex and small imbalances in circuit parameters associated with voltage loop gains can cause large differences in the output current as discussed in [44]. The individual converters would interact with each other and try to regulate the output voltage, inducing oscillations in the output voltage. Thus, there should be some current sharing control that makes individual converters to equally share currents.

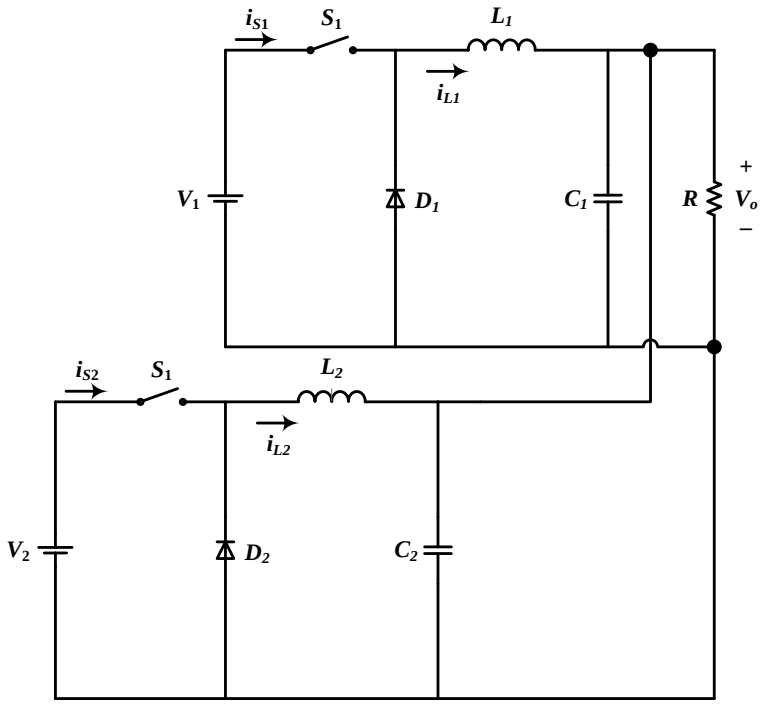


Figure 1.3. Parallel connected double-input buck converter.

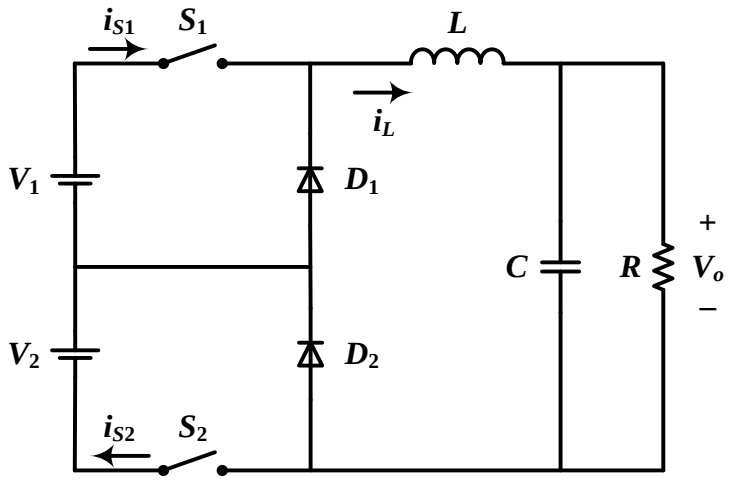


Figure 1.4. Double-input (DI) buck converter.

1.3. PREVIOUS WORK

Several MIPEC topologies have been reported in the literature based on non-isolated direct link [5-8], magnetically coupled structure [9-11], and magnetic coupling through a high frequency transformer [12]. Again, some topologies have been developed using flux additivity by a multiwinding transformer [13], putting sources in series [14], time-sharing concept [15], dc-link coupling via a dc bus [16], and a three switch boost topology [17]. Several non-isolated topologies have been explored in [5, 15, 16, 25-27] and a comparative study of several MIPEC topologies based on cost, application suitability, modularity, and flexibility has been presented in [28]. Several applications of MIPECs in renewable energy sources comprising of wind and solar have been discussed in [8, 9, 29-35]. In [36] maximum power point tracking is used to get maximum power out of the photovoltaic array while regulating the output voltage in a double-input buckboost converter. The authors in [6, 7, 13, 21, 26, 37-40] discuss the applications of

bi-directional MIPECs in HEVs where the energy sources are batteries and ultra-capacitors (shown in Figure 1.5).

For analysis, control, and design of MIPECs, it is important to have some models that describe the behavior of the system. These models are also necessary for designing voltage and current compensators for the converter containing multiple loops to achieve various control objectives. The control objectives in a hybrid system can vary depending on the type of the sources. For example, in solar applications with one of the sources as a PV array and the other being the battery, the objective is to draw maximum power from the PV array. The battery is used to meet the additional load demand while regulating the output voltage. In an HEV with batteries/ultra-capacitors, the control objective is to provide constant power from batteries and ultra-capacitors are used to meet the additional load demand. A multifrequency, time-invariant model of multi-input buckboost converter has been reported in [41]. In [42], a parametric average value model of multi-input buck converter which utilizes corrected full-order state space averaged model has been presented. The small signal model of double-input buckboost converter has been developed and subsequently analysis and compensator design has been discussed in [43]. Therefore modeling these systems becomes necessary for analyzing system stability and designing optimal controllers.

1.4. THESIS ORGANIZATION

In this thesis, the application of several MIPEC topologies and different control strategies are discussed. The future developments and widespread applications of MIPECs depend on the implementation of new control methods. To develop these control

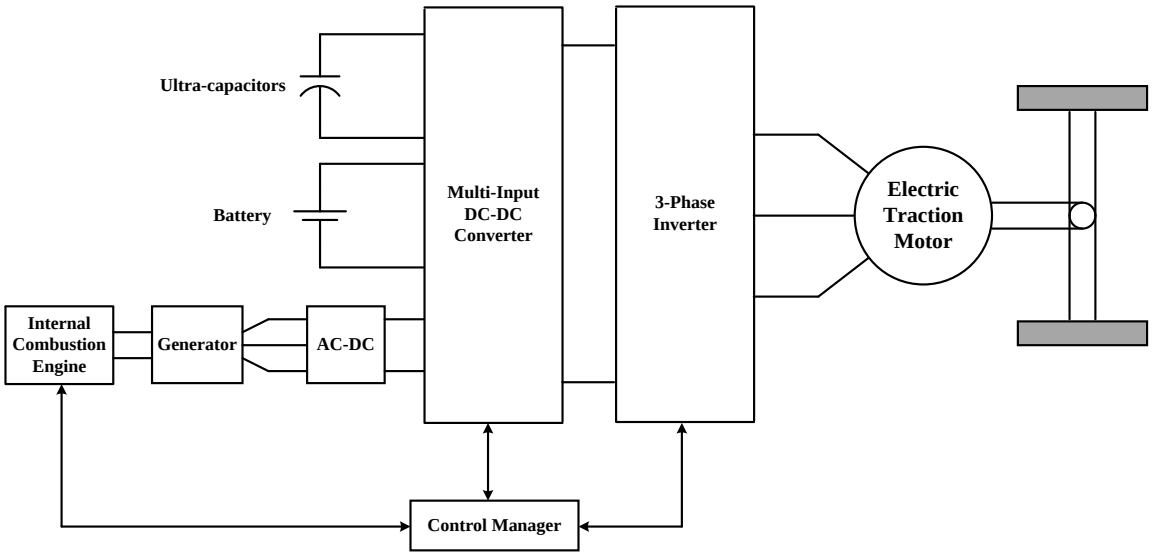


Figure 1.5. MIPEC application in HEV.

methods and to predict the dynamic behavior of the system, it is important to develop some models of these converters. In Section 2, detailed procedure for deriving the small signal model of a DI buck converter has been explained.

The small signal models are extremely useful for designing optimal controllers for the system and do stability analysis for the system. In Section 3, a new control method called the coupling control method for the DI buck converter has been proposed. The small signal model developed in the previous section has been used to analyze the system and establish the superiority of the proposed control method to conventional methods. In Section 4, another control method called dead-time control has been proposed which uses the dead time between the switch commands as the third variable apart from switch commands D_1 and D_2 to control the power sharing in the DI buck converter. In Section 5, the offset-time control of DI buckboost converter [45] has been implemented and verified.

Several applications of MIPECs in renewable energy sources have been discussed in the literature [31-35], still a lot needs to be done in terms of exploration of new non-isolated topologies for possible applications in renewable energy and HEVs. In Section 6, application of bi-directional DI buck converter topology in HEVs with regenerative operation has been discussed. By employing this method, the high power density and high energy density of the battery/ultra-capacitor system has been utilized and during deceleration the energy is fed back to the system. In this system, current-mode control technique is utilized to regulate the dc link voltage. In Section 7, a DI buckboost converter has been used to develop a system where one of the sources is a PV array and the other source is a battery. Perturb and observe (P&O) maximum power point tracking has been utilized to draw maximum power out of the PV array and the additional load demand is supplied by the battery, while keeping the output voltage constant. Conclusion and future work has been presented in Section 8.

2. SMALL SIGNAL MODEL OF DI BUCK CONVERTER

Small signal analysis is done to predict the dynamic behavior of power electronic converters for variations in source, load and circuit parameters. For developing a small signal model, first an averaged model is developed and it is linearized about a quiescent operating point. Various controllers of the control system are then designed based on this linear time invariant (LTI) model to meet the control objective. The small signal modeling of the DIPEC converters and the design of the controllers based on this model is yet to be explored. In this section a small signal model is developed for a DI buck converter and the subsequent analysis of control strategies based on this small signal model is explained in the following sections.

2.1. DI BUCK CONVERTER

Two different topologies for the DI buck converter are discussed in [14-16, 42]. The non-restricted topology is selected for the small signal analysis. The circuit diagram of a DI buck converter, which has no mode restriction, is shown in Figure 2.1 [15]. The modes of operation of this topology, along with inductor and diode voltages, are shown in Table 2.1. It can be seen that both of the switches can be ON at the same time and thus there is no mode restriction. The steady-state input-output voltage relationship, inductor current and input currents are given by -

$$V_0 = D_1 V_1 + D_2 V_2 \tag{2.1}$$

$$I_L = \frac{V_0}{R} \tag{2.2}$$

$$I_{S1} = D_1 I_L \tag{2.3}$$

$$I_{S2} = D_2 I_L \tag{2.4}$$

where D_1 and D_2 are the on-time duty ratios of switches S_1 and S_2, respectively. V_1, V_2, V_0, I_L, I_{S1}, and I_{S2} are the steady state input voltages, output voltage, inductor current and input currents at the operating point. The small signal model is developed by perturbing and then linearizing the system about a steady state operating point. By this method a non-linear power electronic converter system is converted to an LTI system.

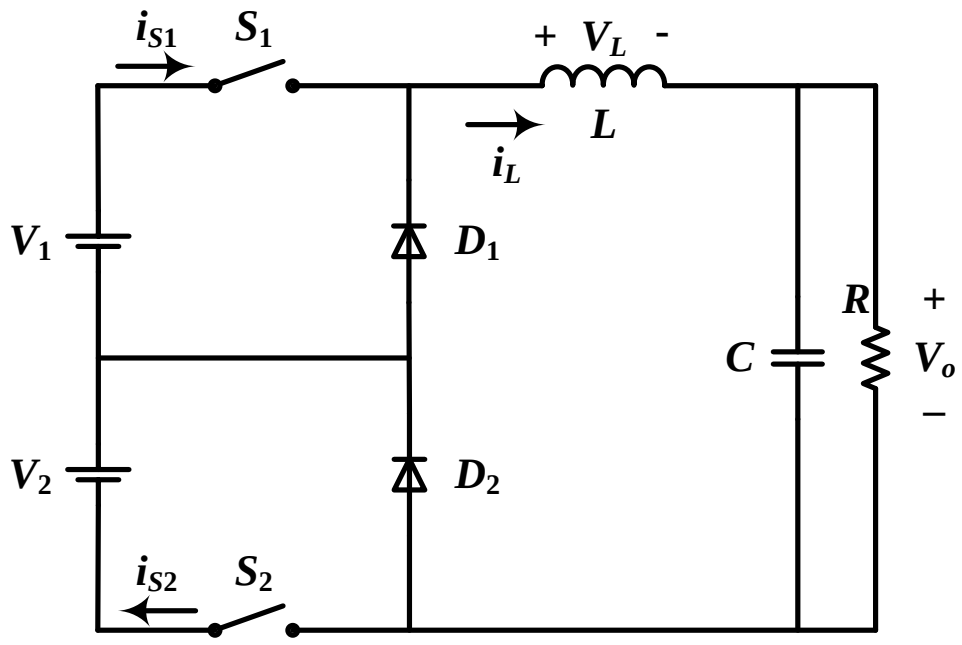


Figure 2.1. Circuit diagram of the DI buck converter.

Table 2.1. Modes of Operation of a DI Buck Converter

Mode	S_1	S_2	V_L	V_{D1}	V_{D2}
I	On	Off	V_1-V_0	-V_1	0
II	Off	On	V_2-V_0	0	V_2
III	Off	Off	-V_0	0	0
IV	On	On	V_1+V_2-V_0	-V_1	-V_2

2.2. DEVELOPMENT OF THE SMALL SIGNAL MODEL

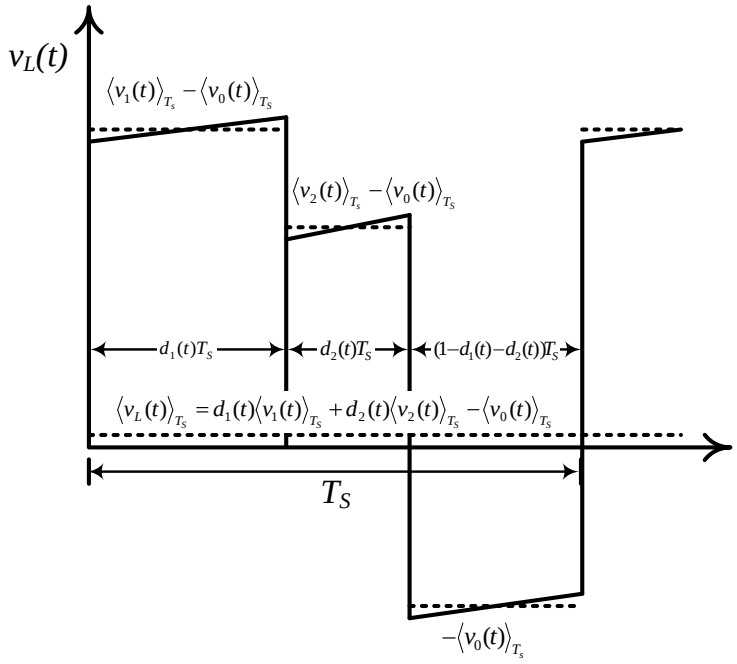
The small signal model of any power electronic converter is developed by first determining the inductor voltage, capacitor current, and input currents. The inductor voltage and input current waveforms are shown in Figure 2.2, with the dotted lines giving the averaged values of the currents and voltages. Equations (2.5) to (2.8), derived from these waveforms, give the low frequency averaged equations for inductor voltage, capacitor current and input currents for the DI buck converter. These equations neglect the switching ripple and only contain the low frequency components.

$$\langle v_L(t)\rangle_{T_S} = L\frac{d\langle i_L(t)\rangle_{T_S}}{dt} = d_1(t)\langle v_1(t)\rangle_{T_S} + d_2(t)\langle v_2(t)\rangle_{T_S} - \langle v_0(t)\rangle_{T_S} \tag{2.5}$$

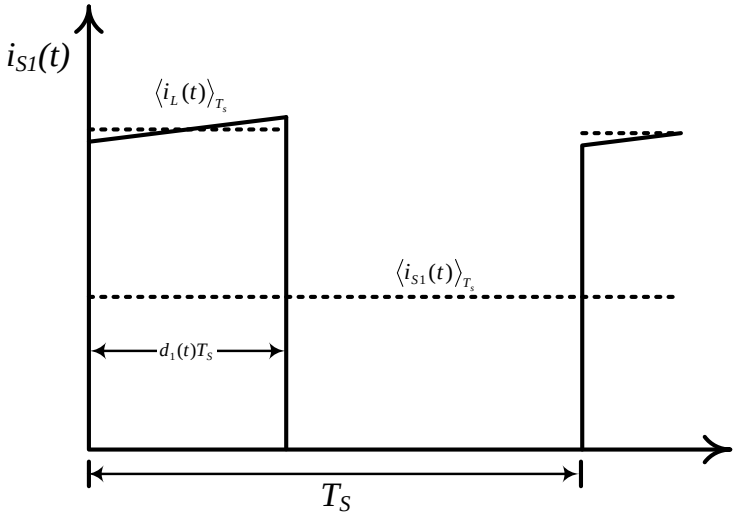
$$\langle i_C(t)\rangle_{T_S} = C\frac{d\langle v_0(t)\rangle_{T_S}}{dt} = \langle i_L(t)\rangle_{T_S} - \frac{\langle v_0(t)\rangle_{T_S}}{R} \tag{2.6}$$

$$\langle i_{S1}(t)\rangle_{T_S} = d_1(t)\langle i_L(t)\rangle_{T_S} \tag{2.7}$$

$$\langle i_{S2}(t)\rangle_{T_S} = d_2(t)\langle i_L(t)\rangle_{T_S} \tag{2.8}$$

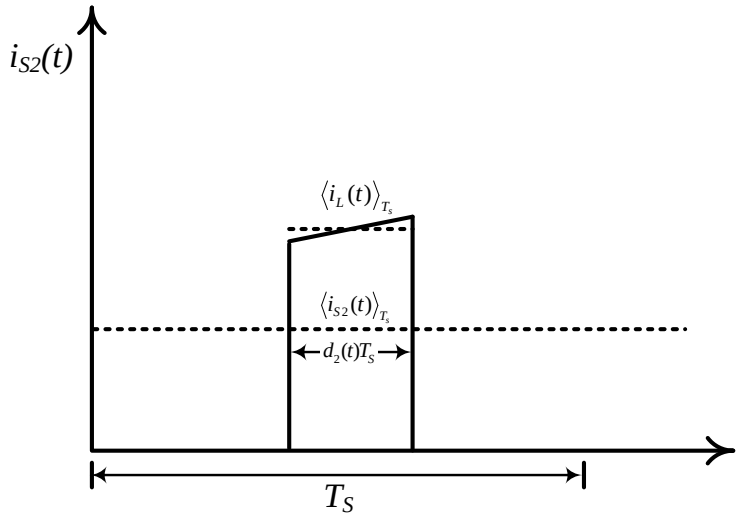


(a)



(b)

Figure 2.2. DI Buck converter waveforms: (a) inductor voltage, (b) input current due to source 1 (c) input current due to source 2.



(c)

Figure 2.2. DI Buck converter waveforms: (a) inductor voltage, (b) input current due to source 1 (c) input current due to source 2. (cont.)

The detailed procedure for deriving these equations has been described in [43, 48]. The voltages and currents are averaged over one switching period T_S, where switching period T_S is equal to inverse of switching frequency f_S. These equations are nonlinear as they involve multiplication of two time varying quantities, so they have to be linearized about the operating point. For developing the small signal model small ac variations are superimposed about the operating point. The time varying quantities along with the superimposed ac variations are given by -

$$\begin{aligned} \langle i_L(t)\rangle_{T_S} &= I_L + \hat{i}_L(t) \\ \langle v_0(t)\rangle_{T_S} &= V_0 + \hat{v}_0(t) \\ \langle v_1(t)\rangle_{T_S} &= V_1 + \hat{v}_1(t) \end{aligned} \tag{2.9}$$

$$\langle v_2(t)\rangle_{T_S} = V_2 + \hat{v}_2(t)$$

$$\langle i_{S1}(t)\rangle_{T_S} = I_{S1} + \hat{i}_{S1}(t)$$

$$\langle i_{S2}(t)\rangle_{T_S} = I_{S2} + \hat{i}_{S2}(t)$$

$$d_1(t) = D_1 + \hat{d}_1(t)$$

$$d_2(t) = D_2 + \hat{d}_2(t)$$

Where all the quantities in upper case are the steady state values at the operating point. The magnitudes of the ac variations are considered to be very small compared to the steady state values. First step for developing the small signal model is to perturb the equations about an operating point by substituting equation (2.9) in (2.5) to (2.8). The next step is to linearize the non-linear equations by neglecting the non-linear second order terms containing the product of the ac variations. This procedure leads to -

$$L\frac{d\hat{i}_L(t)}{dt} = D_1\hat{v}_1(t) + D_2\hat{v}_2(t) + \hat{d}_1(t)V_1 + \hat{d}_2(t)V_2 - \hat{v}_0(t) \tag{2.10}$$

$$C\frac{d\hat{v}_0(t)}{dt} = \hat{i}_L(t) - \frac{\hat{v}_0(t)}{R} \tag{2.11}$$

$$\hat{i}_{S1}(t) = \hat{d}_1(t)I_L + D_1\hat{i}_L(t) \tag{2.12}$$

$$\hat{i}_{S2}(t) = \hat{d}_2(t)I_L + D_2\hat{i}_L(t) \tag{2.13}$$

Equations (2.10) to (2.13) give the linearized model of the DI buck converter about a steady state operating point.

Figure 2.3 shows the circuit equivalent of the small signal model based on equations (2.10) through (2.13). The input side of the model has independent current sources with control signal perturbations $\hat{d}_1(t)$ and $\hat{d}_2(t)$ and dependent current sources

with inductor current perturbations $\hat{\imath}_L(t)$. The output side of the model has the independent voltage sources with control signal perturbations $\hat{d}_1(t)$ and $\hat{d}_2(t)$ and dependent voltage sources with input voltage perturbations $\hat{v}_1(t)$ and $\hat{v}_2(t)$. The small signal model is used for deriving the voltage and current compensators that can realize the control objective of keeping the output voltage constant while drawing constant power from one of the sources.

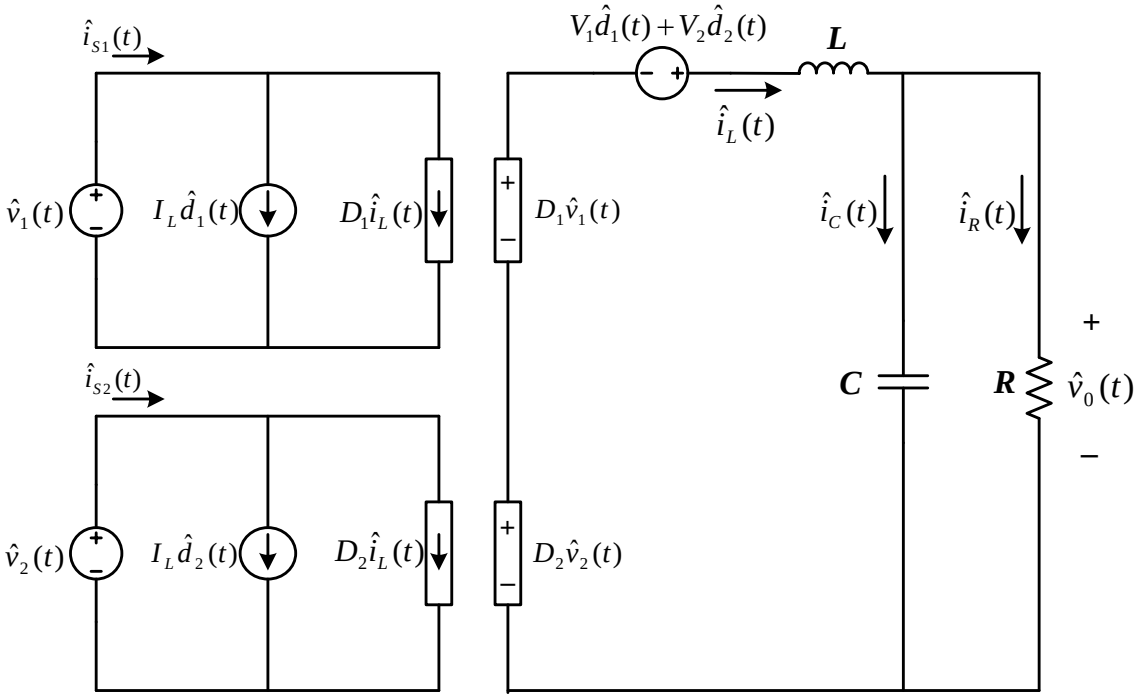


Figure 2.3. Small signal model for DI buck converter.

2.3. DI BUCK CONVERTER TRANSFER FUNCTIONS

The equivalent small signal circuit model developed (as shown in Figure 2.3) in the previous section is used for deriving the transfer functions of the converter. The

analysis is done in the frequency domain with bode plots by converting equations (2.10) to (2.13) to frequency domain using the Laplace Transformation. The equations in frequency domain are as follows -

$$sL\hat{i}_L(s) = D_1\hat{v}_1(s) + D_2\hat{v}_2(s) + \hat{d}_1(s)V_1 + \hat{d}_2(s)V_2 - \hat{v}_0(s) \tag{2.14}$$

$$sC\hat{v}_0(s) = \hat{i}_L(s) - \frac{\hat{v}_0(s)}{R} \tag{2.15}$$

$$\hat{i}_{S1}(s) = \hat{d}_1(s)I_L + D_1\hat{i}_L(s) \tag{2.16}$$

$$\hat{i}_{S2}(s) = \hat{d}_2(s)I_L + D_2\hat{i}_L(s) \tag{2.17}$$

The small signal model has four input variables – (i) two control input perturbations $\hat{d}_1(s)$ and $\hat{d}_2(s)$, and (ii) two input voltage perturbations $\hat{v}_1(s)$ and $\hat{v}_2(s)$. The transfer functions of the converter describe the behavior of the system for variations in the input. In some topologies, like DI buckboost converter toplogy, they also explain the right-half-plane zeroes and resonances in a converter system, and can also be used to derive the output and input impedances of the system.

From equations (2.14) and (2.15) the control to output transfer functions $G_{v0d1}(s)$ and $G_{v0d2}(s)$ due to inputs 1 and 2, respectively, are derived by setting other inputs to zero. These transfer functions describe the variations in output voltage $\hat{v}_0(s)$ for variations in control inputs $\hat{d}_1(s)$ and $\hat{d}_2(s)$.

$$G_{v0d1}(s) = \left.\frac{\hat{v}_0(s)}{\hat{d}_1(s)}\right|_{\hat{d}_2(s)=\hat{v}_1(s)=\hat{v}_2(s)=0} = \frac{V_1}{s^2LC + s\frac{L}{R} + 1} \tag{2.18}$$

$$G_{v0d2}(s) = \left.\frac{\hat{v}_0(s)}{\hat{d}_2(s)}\right|_{\hat{d}_1(s)=\hat{v}_1(s)=\hat{v}_2(s)=0} = \frac{V_2}{s^2LC + s\frac{L}{R} + 1} \tag{2.19}$$

Similarly the control to inductor current transfer functions $G_{iLd1}(s)$ and $G_{iLd2}(s)$ are derived by setting the control input variations of the other input and the input voltage variations to zero in (2.14) and (2.15). The transfer functions hence derived describe the variations in inductor current due to variations in control inputs.

$$G_{iLd1}(s) = \left.\frac{\hat{i}_L(s)}{\hat{d}_1(s)}\right|_{\hat{d}_2(s)=\hat{v}_1(s)=\hat{v}_2(s)=0} = \frac{V_1(\frac{1}{R}+sC)}{s^2LC + s\frac{L}{R}+1} \tag{2.20}$$

$$G_{iLd2}(s) = \left.\frac{\hat{i}_L}{\hat{d}_2}\right|_{\hat{d}_1(s)=\hat{v}_1(s)=\hat{v}_2(s)=0} = \frac{V_2(\frac{1}{R}+sC)}{s^2LC + s\frac{L}{R}+1} \tag{2.21}$$

Again by substituting (2.20) and (2.21) in (2.16) and (2.17), the control to input current transfer functions are derived as

$$G_{is1d1}(s) = \left.\frac{\hat{i}_{s1}(s)}{\hat{d}_1(s)}\right|_{\hat{d}_2(s)=\hat{v}_1(s)=\hat{v}_2(s)=0} = I_L + \frac{D_1V_1(\frac{1}{R}+sC)}{s^2LC + s\frac{L}{R}+1} \tag{2.22}$$

$$G_{is2d2}(s) = \left.\frac{\hat{i}_{s2}(s)}{\hat{d}_2(s)}\right|_{\hat{d}_1(s)=\hat{v}_1(s)=\hat{v}_2(s)=0} = I_L + \frac{D_2V_2(\frac{1}{R}+sC)}{s^2LC + s\frac{L}{R}+1} \tag{2.23}$$

2.4. SIMULATION RESULTS

The small signal model is verified by simulating the DI buck converter and measuring the small signal variations in the input currents and output voltage for small ac variations in control inputs $\hat{d}_1(s)$ and $\hat{d}_2(s)$. The measured values are then compared with the bode plots of the transfer functions derived from the small signal model. The DI buck

converter is simulated with V_1 = 75 V, V_2 = 60 V, f = 50 kHz, D_1 = 0.4, D_2 = 0.4, V_0 = 54 V, L = 100 µH, C = 50 µF, and R = 15 Ω. Small ac variations are introduced in one of the control inputs while the other is kept constant. The ac variations that are introduced is $\hat{d}(t) = 0.01\sin(2\pi ft)$, where f is the frequency of the ac variations that is introduced in the control input. The frequency is varied and the variations in various currents and voltages are recorded and converted into dB to be compared with that obtained from the bode plots of the transfer functions derived from the small signal model. In Figure 2.4, G_{v0d1_sim} shows the recorded values, of the both magnitude and phase, from the simulation and it is matched with the bode plot of $G_{v0d1}(s)$ transfer function obtained from the small signal model. Figures 2.4 to 2.7 show that the simulated results match the bode plots of all the transfer functions obtained from the developed small signal model.

In this section the small signal model has been developed for a DI buck converter and has been verified by simulations. The small signal model provides us a powerful tool in determining the dynamic behavior of the system. The developed model is used in the design of optimal compensators for stable closed-loop operation. In the following section the small signal model is used to analyze a new control method.

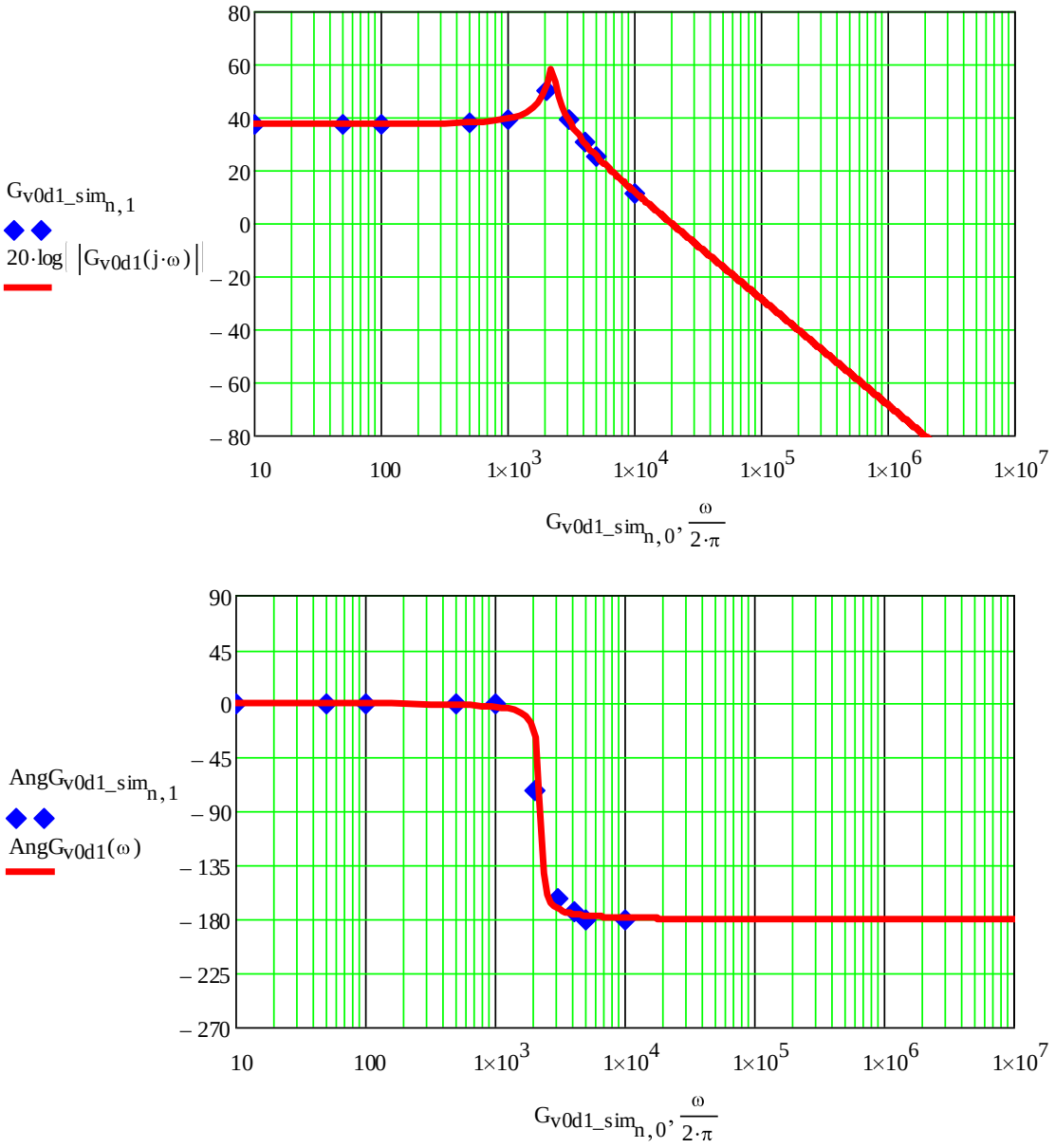


Figure 2.4. Bode magnitude and phase plots for $G_{v0d1}(s)$.

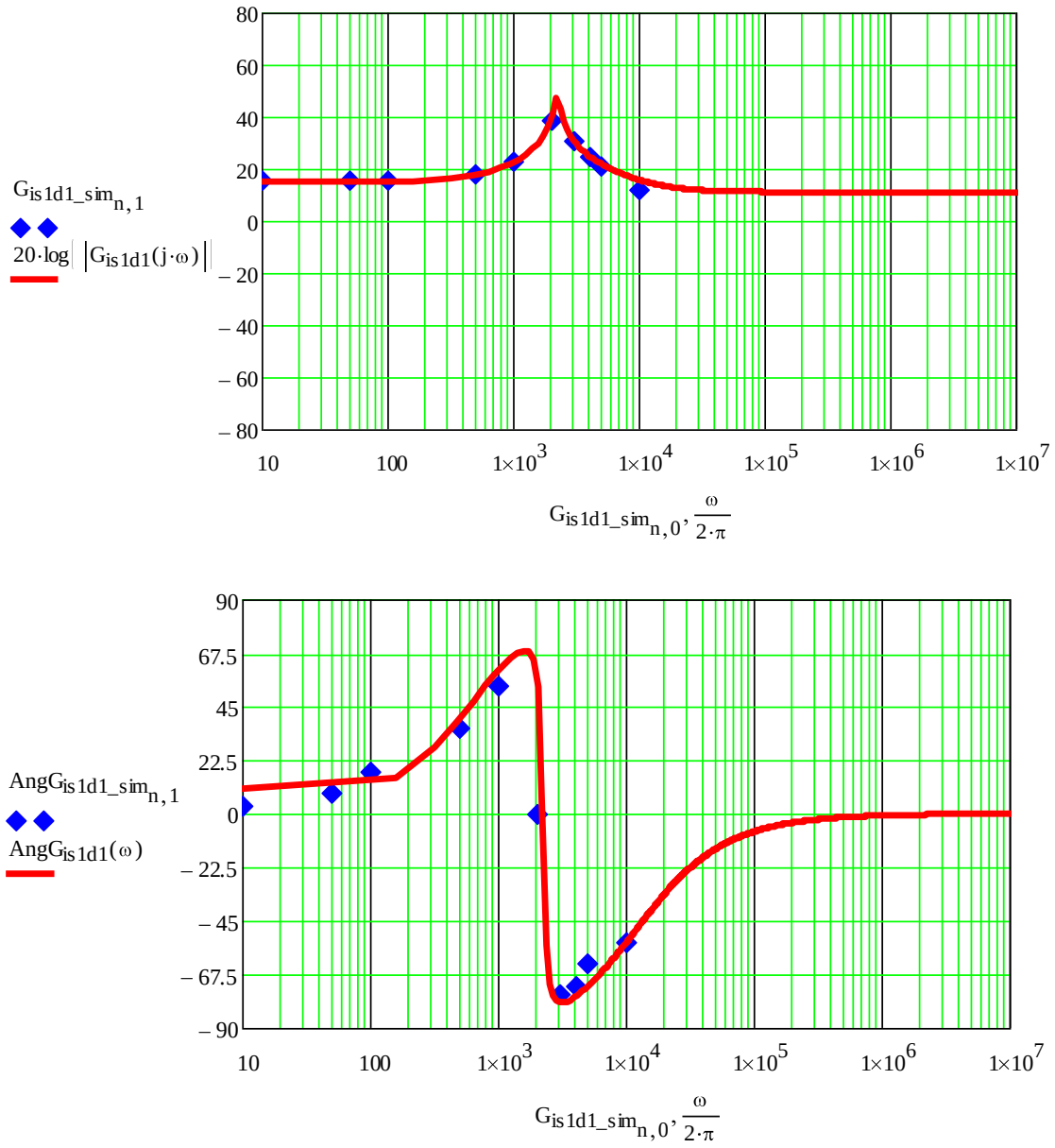


Figure 2.5. Bode magnitude and phase plots for $G_{is1d1}(s)$.

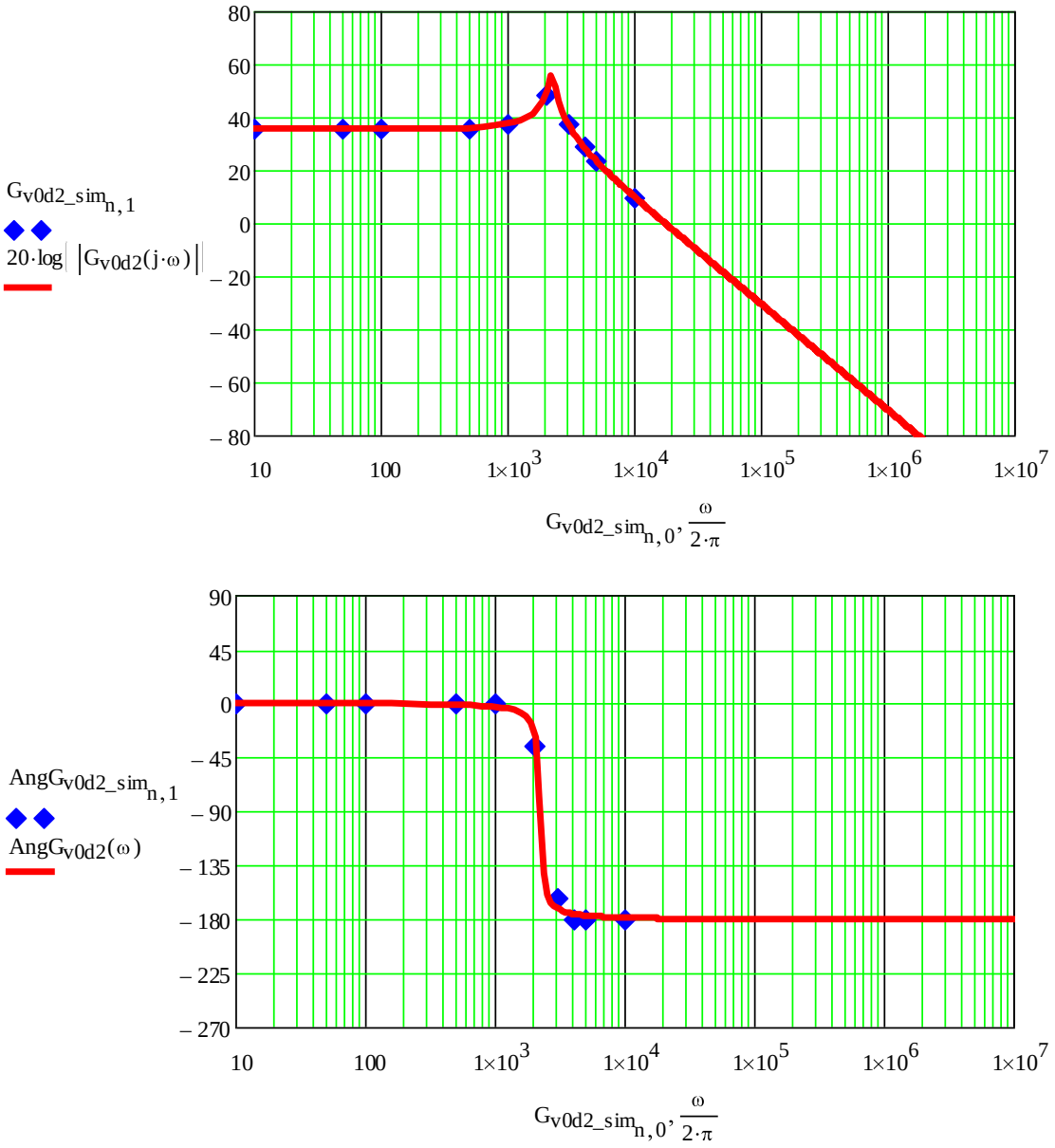


Figure 2.6. Bode magnitude and phase plots for $G_{v0d2}(s)$.

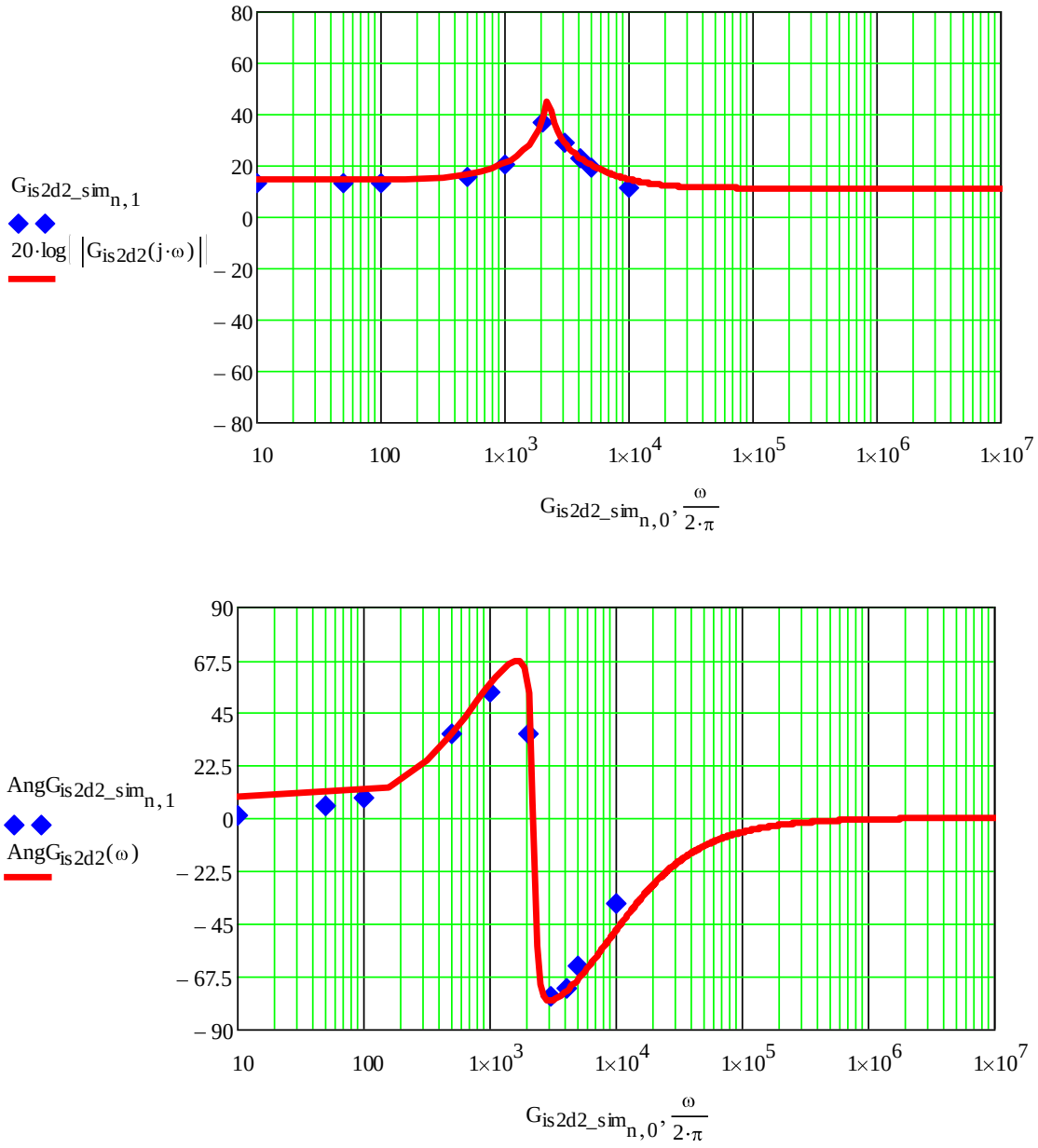


Figure 2.7. Bode magnitude and phase plots for $G_{is2d2}(s)$.

3. COUPLING CONTROL METHOD FOR DI BUCK CONVERTER

The conventional method to control DIPECs is based on the control of one of the switch currents while maintaining constant output voltage [43]. The most straightforward control structure is based on having independent current and voltage control loops. However, the conventional control does not exhibit good dynamic response when a sudden change in the switch current reference or load happens. In this section a new control method called the coupling control method is introduced which is based on the coupling of current and voltage loops of the conventional control structure. Since the output from the current loop is combined with the output of the voltage loop and vice-versa the dynamic response is improved significantly. The small signal model developed in the previous section is used to analyze both the control methods to show the superiority of the new control method over the conventional method.

3.1. COUPLING CONTROL STRATEGY

Figure 3.1 shows the block diagram of the conventional control method for a DI buck converter. According to the control strategy, one of the input currents is controlled keeping the output voltage constant. Figure 3.1 shows the conventional control method where a current compensator is used to control one of the input currents and a voltage compensator is utilized to control the output voltage. It can be seen that the control signal from the voltage compensator is used to generate d_2, the switch command for switch S_2. It can also be observed that control signal from the current compensator is used to generate d_1, the switch command for switch S_1.

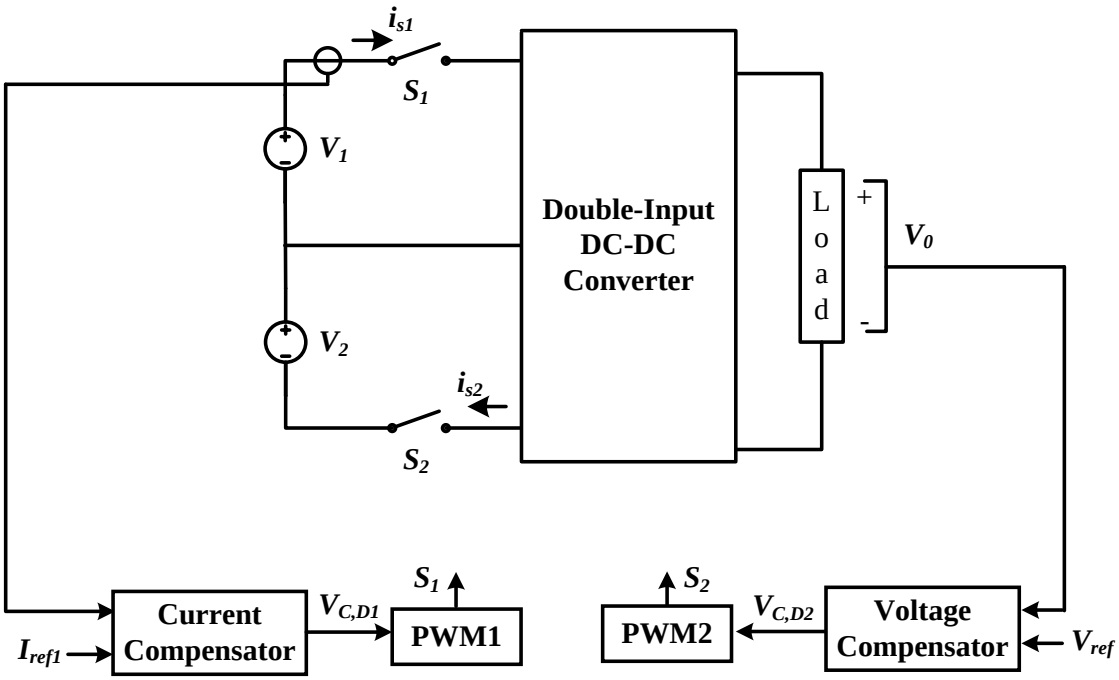


Figure 3.1. Conventional control method for DIPEC.

In many applications, the fast dynamics of i_{s1} is desirable. Hence, a new modified method is introduced called the coupling method which can help improve the dynamic response of the converter even with large load variations. As shown in Figure 3.2, this method is based on coupling the output of the voltage and current compensators. This coupling makes both the compensators to participate in the regulation of the input current and output voltage. When i_{ref1} is decreased the output of current compensator is decreased and hence d_1 is decreased and it reduces i_{s1}. Moreover, based on a negative sign in the coupling method, the output of current compensator will make d_2 to increase and hence

i_{s2} increases faster. Since the load is constant, the increase in i_{s2} helps to decrease i_{s1} faster. The similar phenomenon happens for the voltage loop as well.

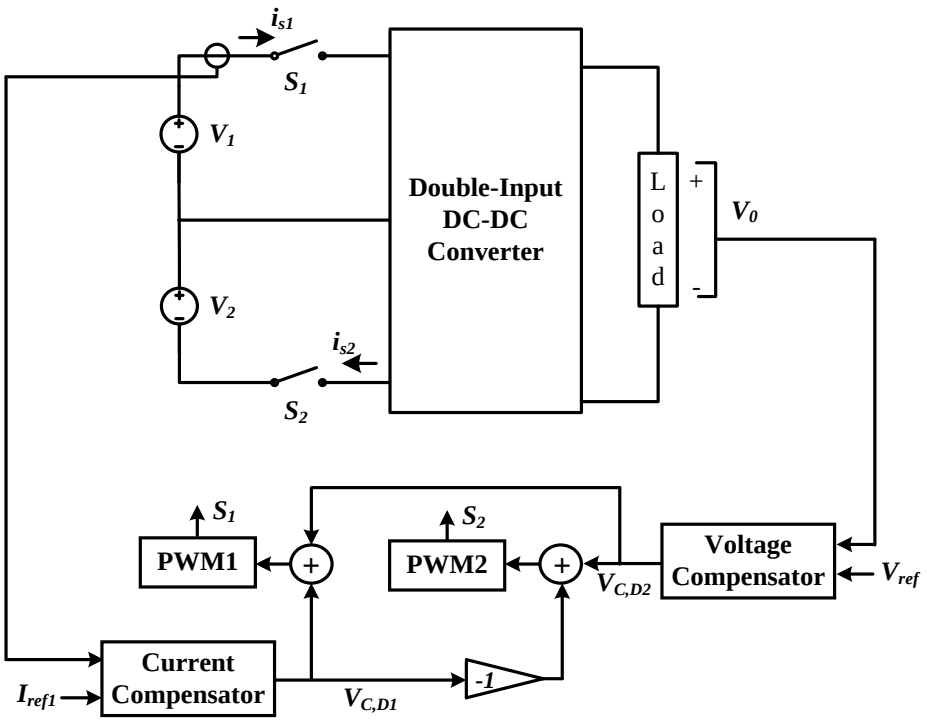


Figure 3.2. Proposed coupling control method for DIPEC.

The small signal model developed in the previous section is used to design the current and voltage compensators. In the conventional method, the current and the voltage loops are considered to be independent and the voltage and current compensators are designed accordingly.

Figures 3.3 and 3.4 show the voltage and current loops of the converter. $G_{vc}(s)$ and $G_{ic}(s)$ are designed to get desired phase and gain margins for the loop gains $T_v(s)$ and $T_i(s)$. Transfer functions $G_{v0d2}(s)$ and $G_{is1d1}(s)$ are derived in the previous section from the

small signal model of the DI buck converter. The voltage compensator is Type III and the current compensator is Type II. The designed compensators given in equations (3.3) and (3.4) are used for the proposed method also.

$$T_v(s) = G_{vc}(s)G_{v0d2}(s) \tag{3.1}$$

$$T_i(s) = G_{ic}(s)G_{is1d1}(s) \tag{3.2}$$

$$G_{vc}(s) = \frac{100\left(1+\frac{s}{2\pi 1000}\right)\left(1+\frac{s}{2\pi 1000}\right)}{s\left(1+\frac{s}{2\pi 50000}\right)\left(1+\frac{s}{2\pi 50000}\right)} \tag{3.3}$$

$$G_{ic}(s) = \frac{650\left(1+\frac{s}{6\pi 500}\right)}{s\left(1+\frac{s}{6\pi 8000}\right)} \tag{3.4}$$

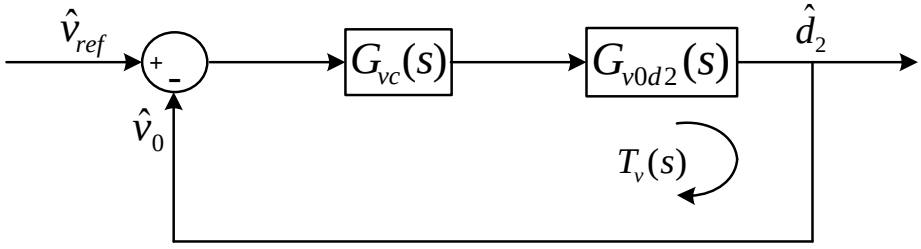


Figure 3.3. Voltage loop of the DI buck converter.

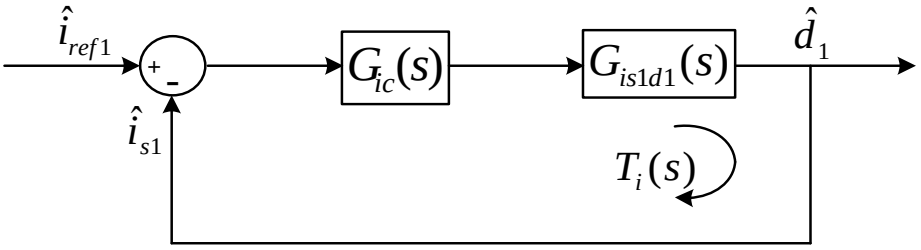


Figure 3.4. Current loop of the DI buck converter.

From Figures 3.5 and 3.6, it can be observed that the voltage and current loop gains $T_v(s)$ and $T_i(s)$ have improved phase and gain margins compared to open loop gains $G_{v0d2}(s)$ and $G_{is1d1}(s)$.

Figure 3.7 shows the small signal model for the coupling method. The model is used to derive $G_{v0is1}(s) = \hat{v}_0/\hat{\imath}_{s1}$ and output impedance $Z_0(s)$. By doing some mathematical manipulation the $G_{v0is1}(s)$ for both conventional and coupling methods can be obtained as follows -

$$G_{v0is1\_conv}(s) = G_{ic}(s)G_{v0d1}(s) \tag{3.5}$$

$$G_{v0is1\_coup}(s) = \frac{G_{ic}(s)G_{v0d1}(s)}{(1+G_{v0d1}(s)G_{vc}(s))} \tag{3.6}$$

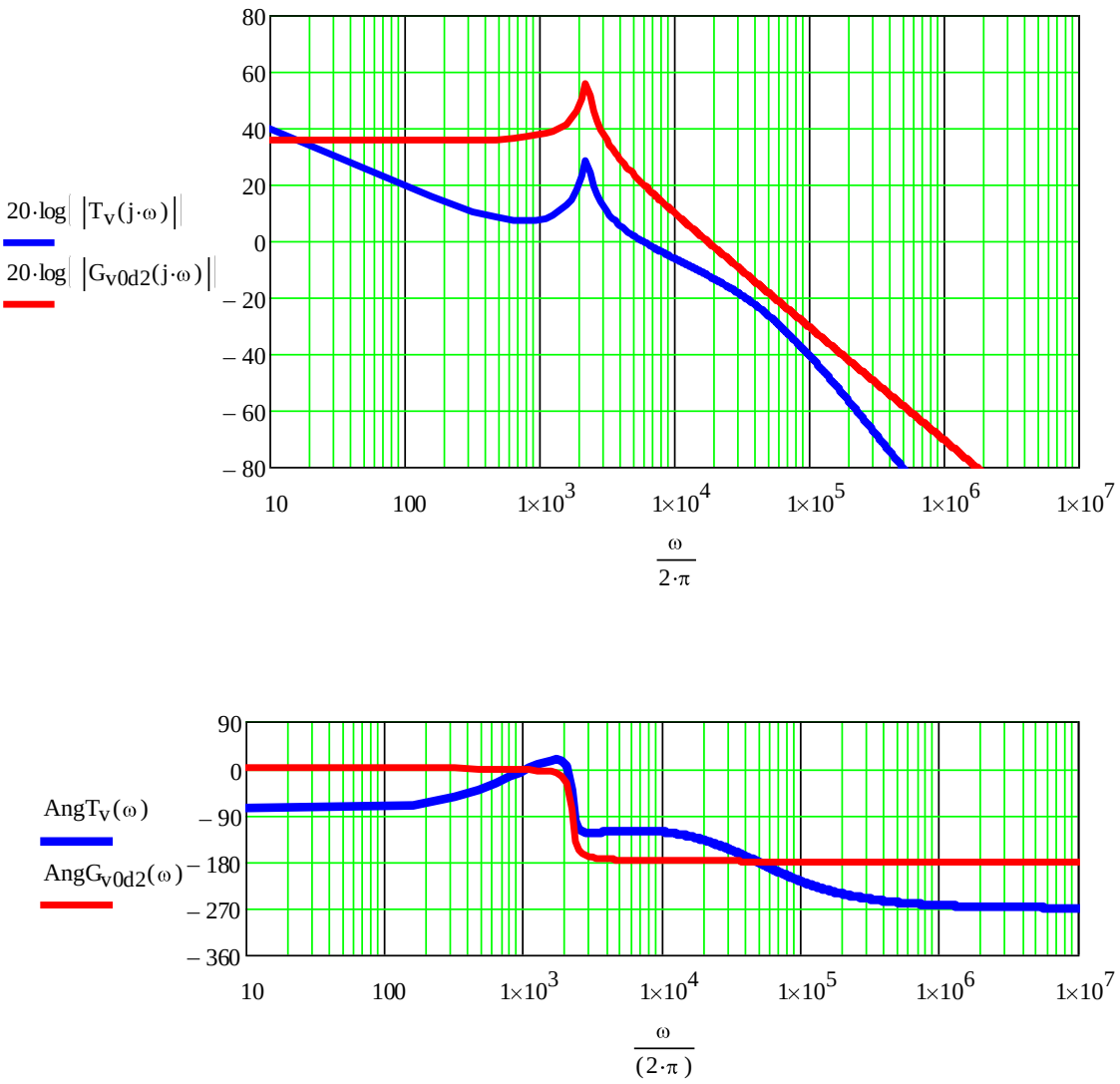


Figure 3.5. Bode magnitude and phase plots of $G_{v0d2}(s)$ and $T_v(s)$.

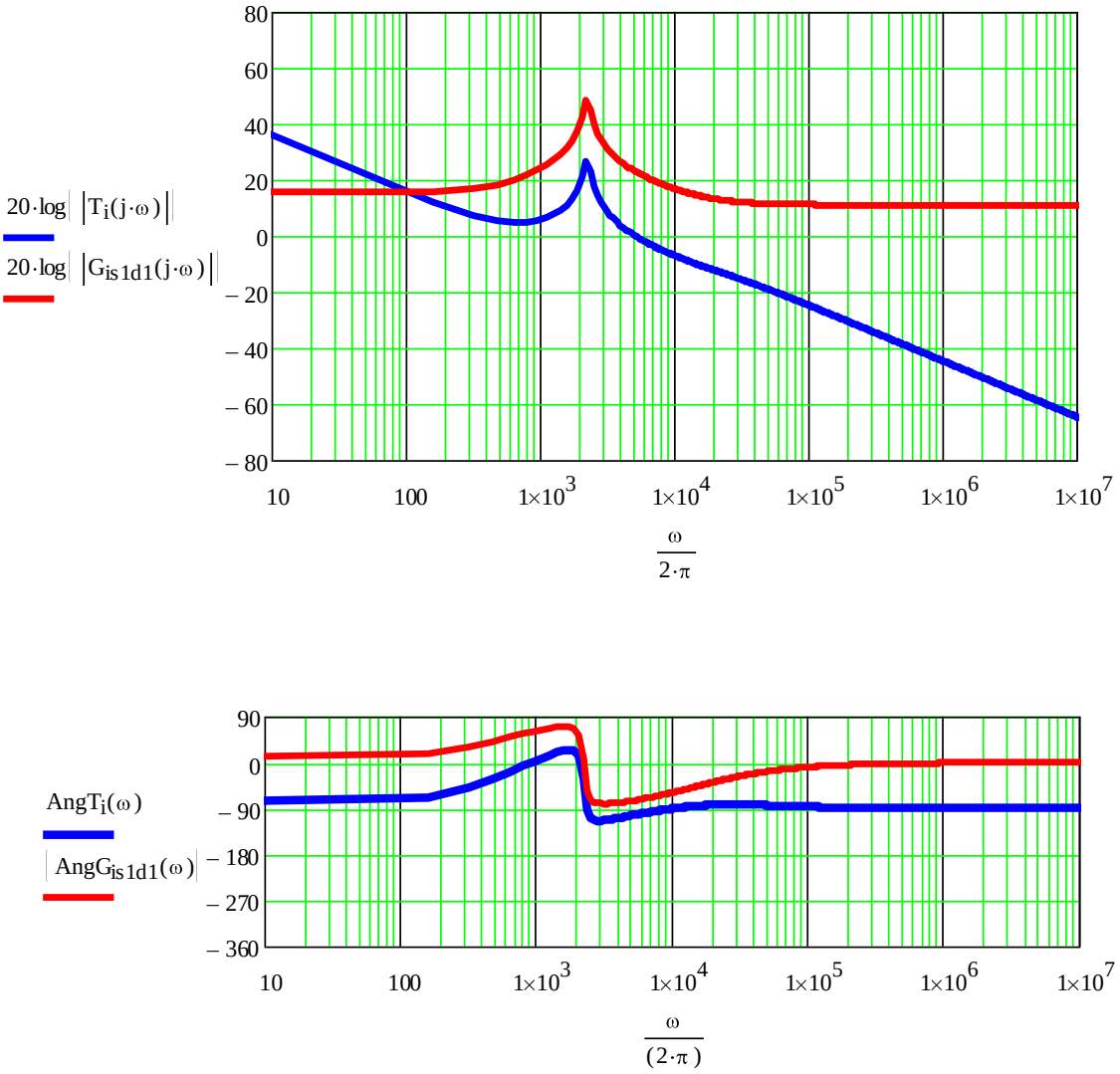


Figure 3.6. Bode magnitude and phase plots of $G_{is1d1}(s)$ and $T_i(s)$.

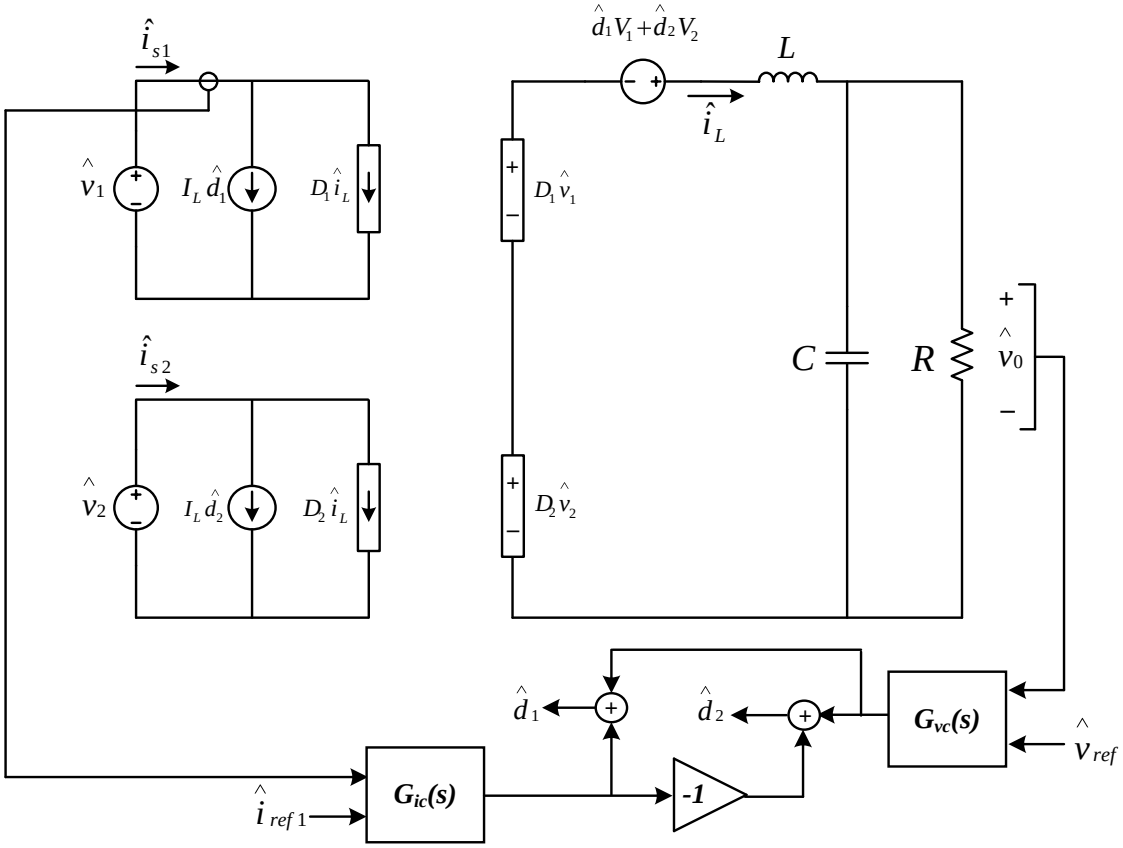


Figure 3.7. Small signal model for the coupling method.

Figure 3.8 shows the bode plots of $G_{v0is1}(s)$ transfer function for both the conventional and coupling control methods. As seen the gain of the transfer function for the new control method is less than the gain for the conventional method. It shows that the sensitivity of the output voltage to changes in i_{s1} for the new method is less than the conventional method. Hence, the dynamic response of the output voltage due to change in input current is faster for the proposed method.

To get the output impedance transfer function an ac current source is added to the circuit in Figure 3.7. Again, by doing some mathematical manipulation the $Z_0(s) = \hat{v}_0/\hat{\imath}_0$ for both conventional and coupling method can be obtained as follows -

$$Z_{0\_conv} = \frac{sL + \dfrac{G_{ic}(s)D_1V_1}{(1+G_{ic}(s)I_L)}}{\dfrac{sL(1+sRC)}{R} + 1 + V_2G_{vc}(s) + \dfrac{G_{ic}(s)D_1V_1(1+sRC)}{R(1+G_{ic}(s)I_L)}} \tag{3.7}$$

$$Z_{0\_coup}(s) = \frac{A}{B} \tag{3.8}$$

$$Where,\quad A = \frac{R}{(1+sRC)}[sL(1+I_LG_{ic}(s)) - (V_2 - V_1)G_{ic}(s)D_1]$$

$$B = \frac{R}{(1+sRC)}(1+I_LG_{ic}(s))\{1+G_{vc}(s)(V_1+V_2)\} + sL(1+I_LG_{ic}(s))$$
$$-(V_2-V_1)G_{ic}(s)D_1 + \frac{R}{(1+sRC)}(V_2-V_1)G_{ic}(s)I_LG_{vc}(s)$$

Figure 3.9 shows the output impedance $Z_0(s)$ transfer function for the converter with both the control methods. As seen the output impedance for the new method is less than the conventional one. It shows that the sensitivity of the output voltage to change in the load for the new control method is less than the conventional method. Hence, the output voltage disturbance due to changes in load current is rejected sooner for the new method compared to the conventional method. Simulation results which are presented in the following section completely validate the small signal analysis.

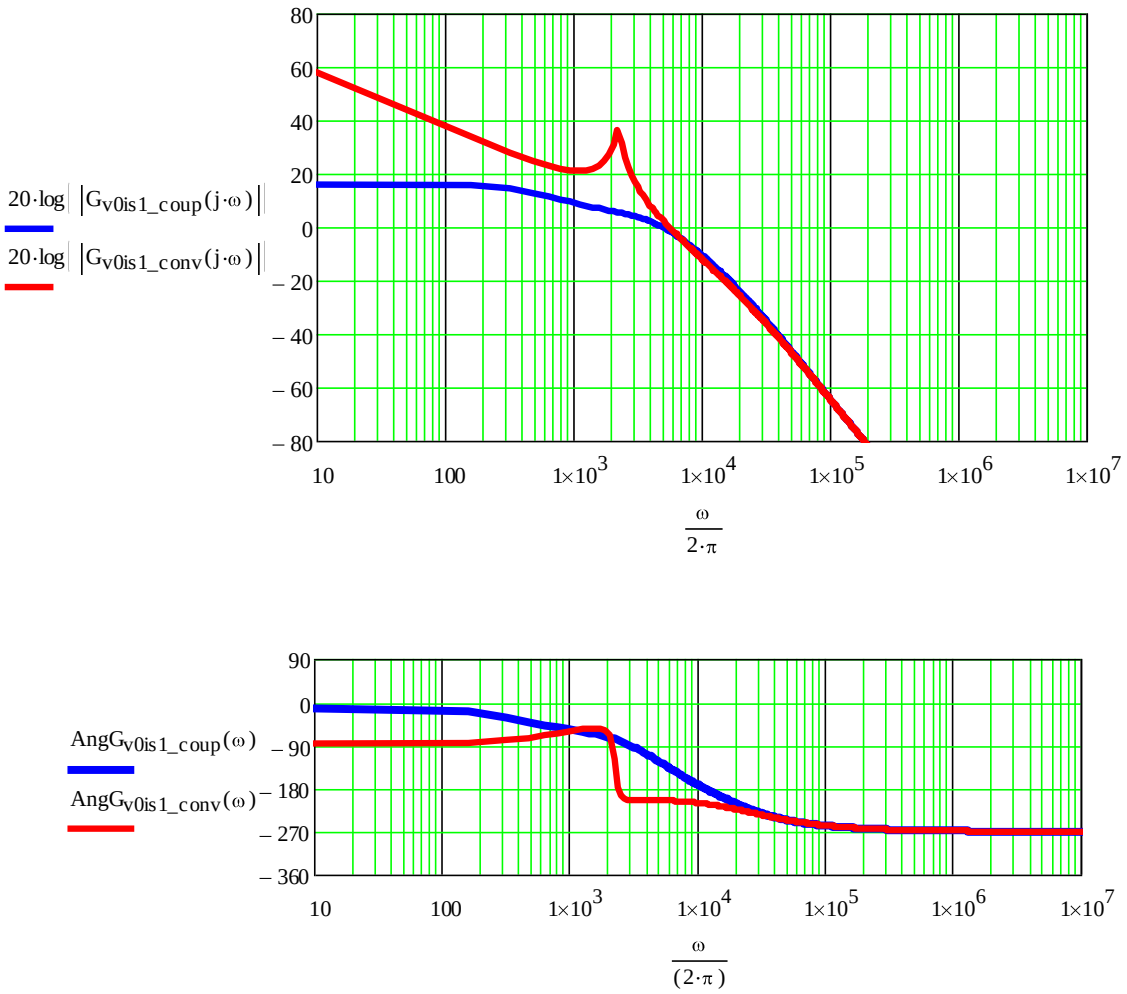


Figure 3.8. Bode magnitude and phase plots of $G_{v0is1}(s)$ for both the methods.

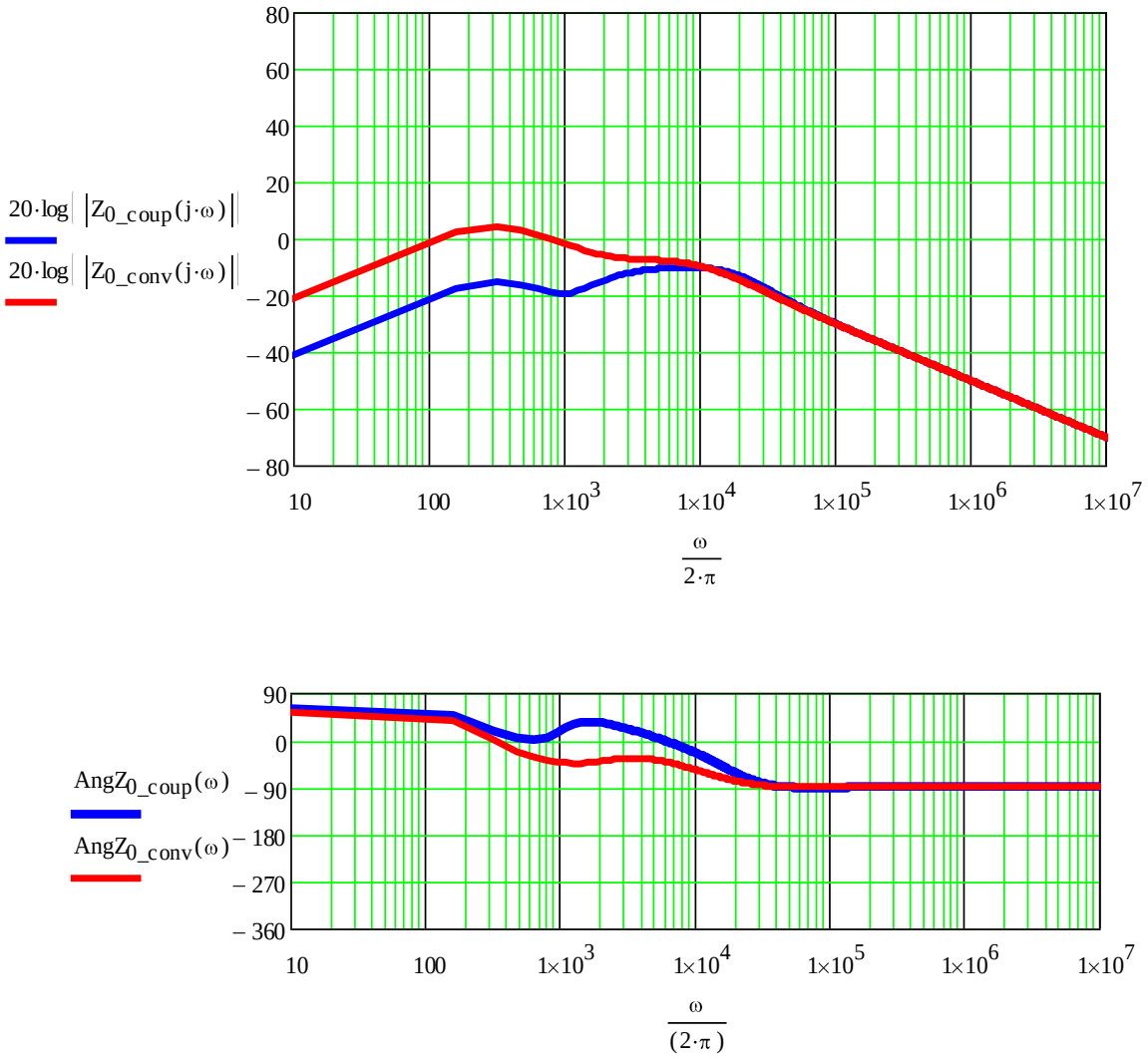


Figure 3.9. Bode magnitude and phase plots of $Z_0(s)$ for both the methods.

3.2. SIMULATION RESULTS

A DI buck converter with V_1 = 75 V, V_2 = 60 V, f = 50 kHz, V_0 = 54 V, L = 100 µH, C = 50 µF is simulated with both the control methods. At $t = 0.01$ *s*, there is a step change in i_{ref1} from 2 A to 1 A. Figure 3.10 shows the output voltage v_0 for both the conventional and coupling methods. As predicted based on the small signal analysis, the output voltage disturbance when current reference i_{ref1} changes is negligible in the case of

coupling method. Figures 3.11 and 3.12 show the results for i_{s1} and i_{s2}, respectively. Both the figures clearly show that the coupling method has a better performance compared to the conventional method.

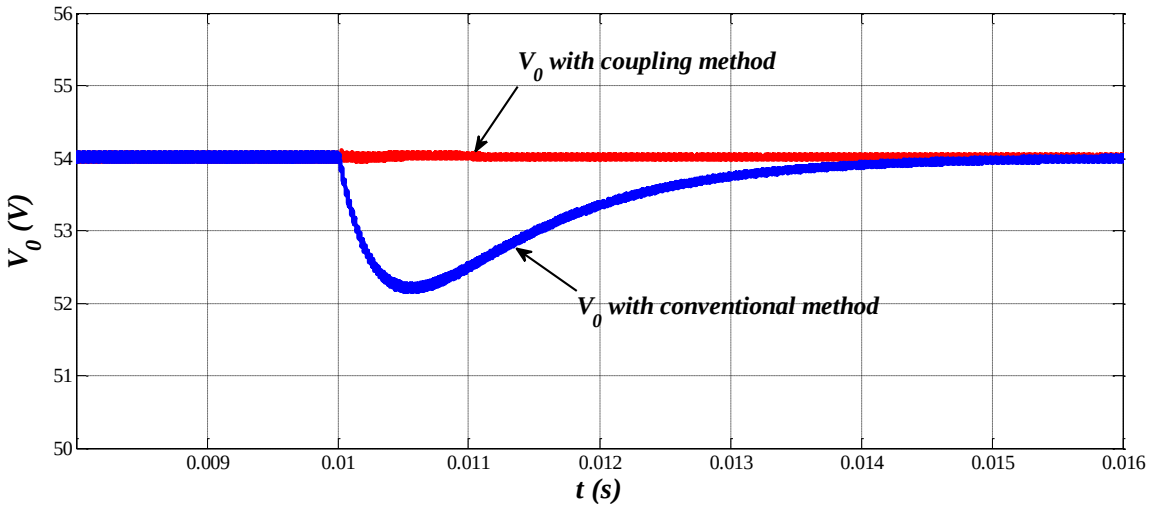


Figure 3.10. Output voltage v_0 waveform for both conventional and coupling methods for step change in i_{ref1} from 2 A to 1 A.

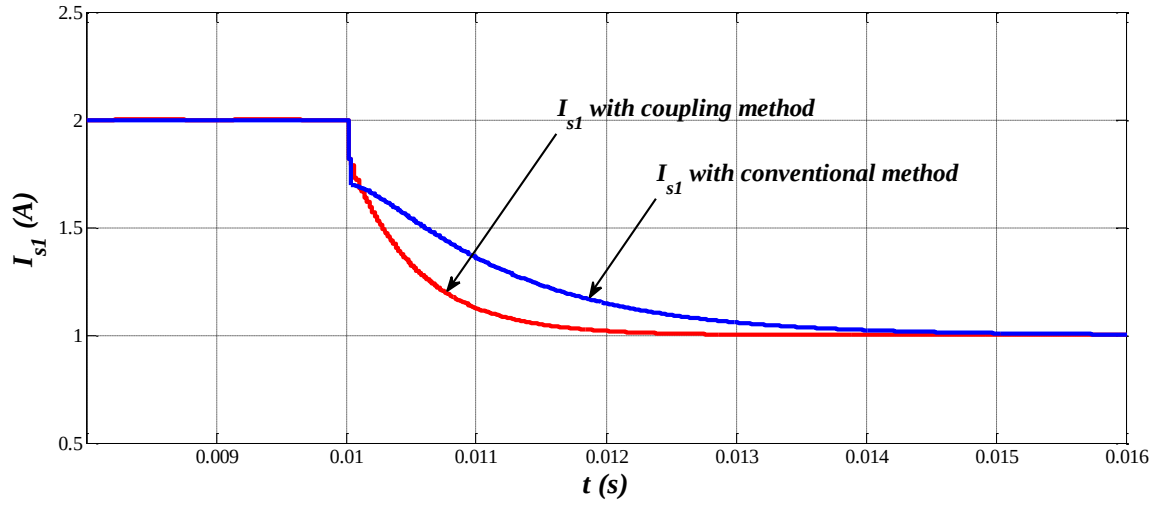


Figure 3.11. Average current from input source 1 i_{s1} for both conventional and coupling methods for step change in i_{ref1} from 2 A to 1 A.

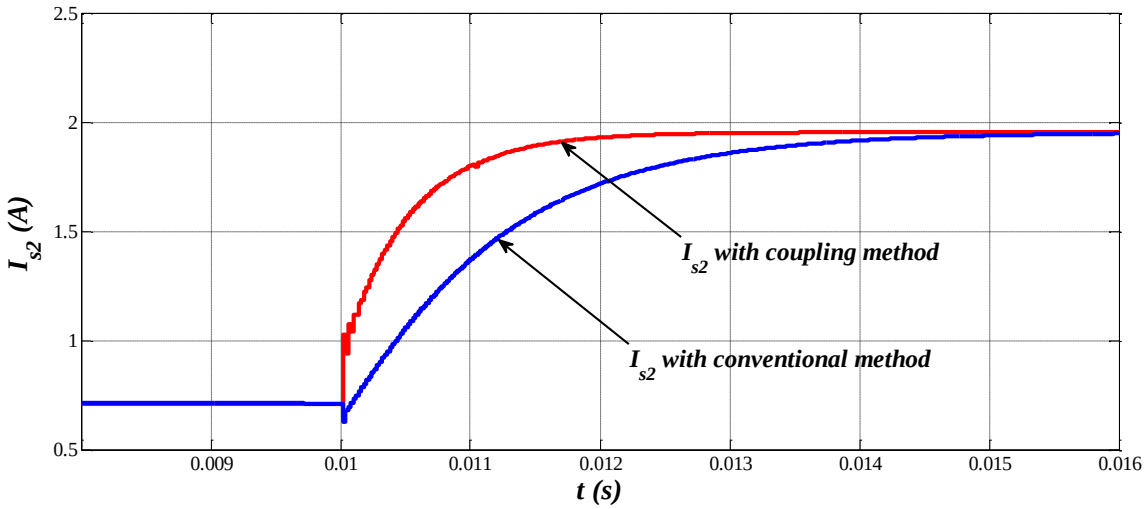


Figure 3.12. Average current from input source 1 i_{s2} for both conventional and coupling methods for step change in i_{ref1} from 2 A to 1 A.

Again at $t = 0.01\ s$ step change in load from 10 Ω to 15 Ω is introduced. Figure 3.13 shows output voltage v_0 for the both conventional and coupling methods. As predicted based on small signal model, the output voltage disturbance when the load changes is less for coupling method compared to the conventional method. Figures 3.14 and 3.15 show the results for i_{s1} and i_{s2} currents respectively. It can be seen that the coupling method shows better performance compared to the conventional method.

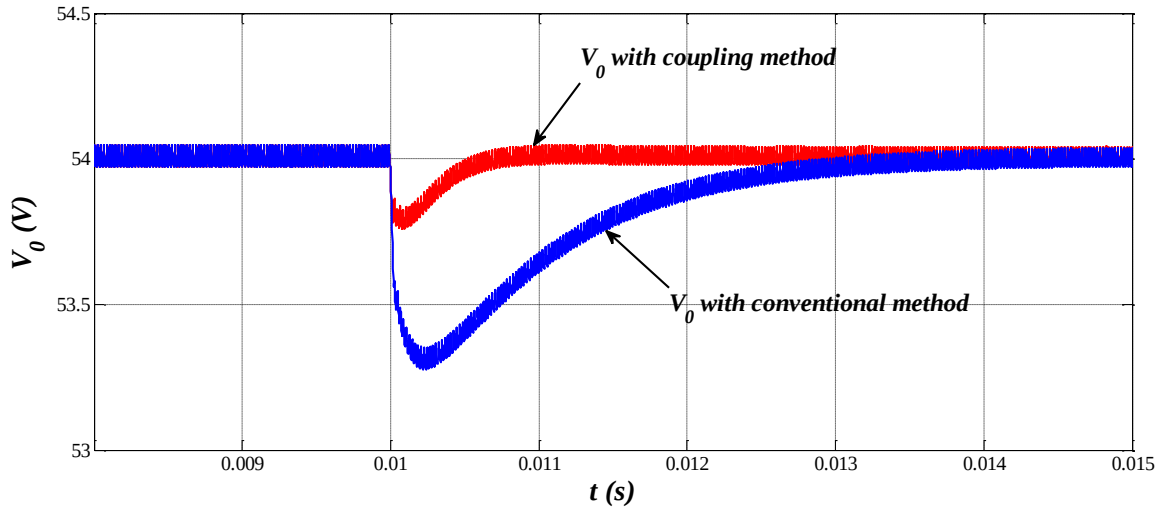


Figure 3.13. Output voltage v_0 waveform for both conventional and coupling methods for step change in load from 10 Ω to 15 Ω.

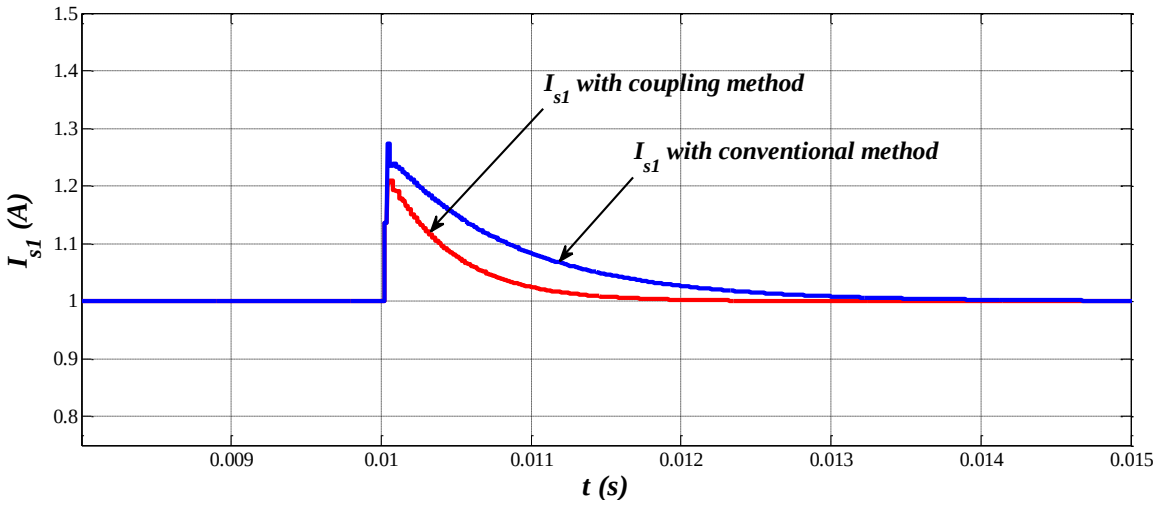


Figure 3.14. Average current from input source 1 i_{s1} for both conventional and coupling methods for step change in load from 10 Ω to 15 Ω.

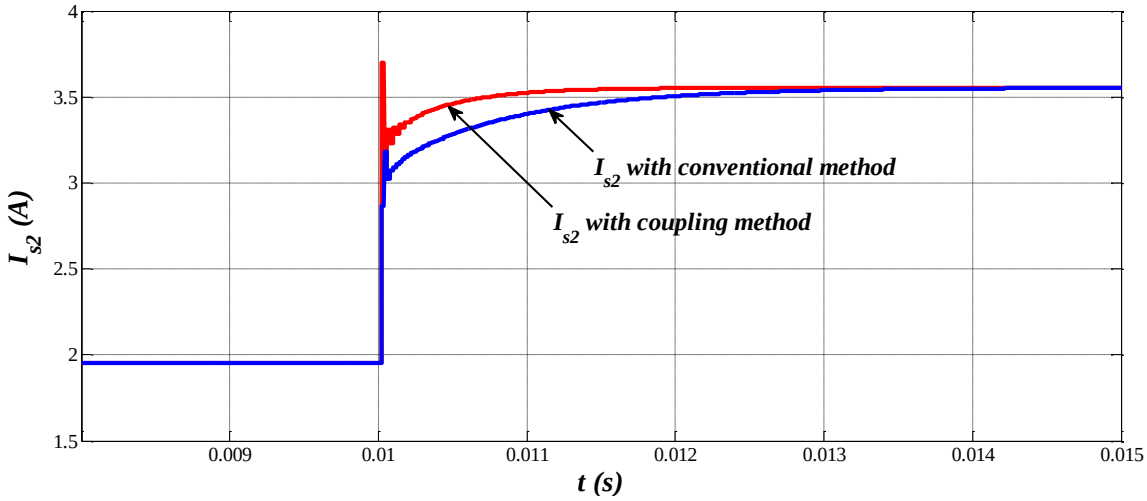


Figure 3.15. Average current from input source 1 i_{s2} for both conventional and coupling methods for step change in load from 10 Ω to 15 Ω.

In this section a new control method has been proposed for power sharing in DI buck converter. The proposed method shows better dynamics for changes in input reference current or load compared to the conventional method with independent control of voltage and current loops. Small signal analysis has been done to validate the proposed method.

4. DEAD TIME CONTROL FOR DI BUCK CONVERTER

In this section, it is shown that in a DI buck converter the dead-time between the two switching commands directly affects the input currents. Therefore, this dead-time can be used as the third control input in addition to the two duty ratios. Using this additional control input, improves the dynamic performance of the system. The newly devised control method hereinafter is called dead-time control.

4.1. DI BUCK CONVERTER MODES OF OPERATION

Two different topologies for the DI buck converter are discussed in [14-16, 25, 42]. The circuit diagram of a restricted DI buck converter is shown in Figure 4.1 [15, 42]. This topology has a mode restriction and the inductor cannot be energized by both of the sources at the same time. In other words, both switches S_1 and S_2 cannot be ON at the same time [42]. The modes of operation of the restricted DI buck converter are shown in Table 4.1. In Figure 4.2, the circuit diagram of the non-restricted DI buck converter topology is presented [16, 25]. The modes of operation of this topology are shown in Table 4.2 and it can be seen that both of the switches can be ON at the same time [25]. In this section, the non-restricted DI buck converter is considered for the development of the dead-time control scheme. The results can easily be extended to the restricted topology as a special case.

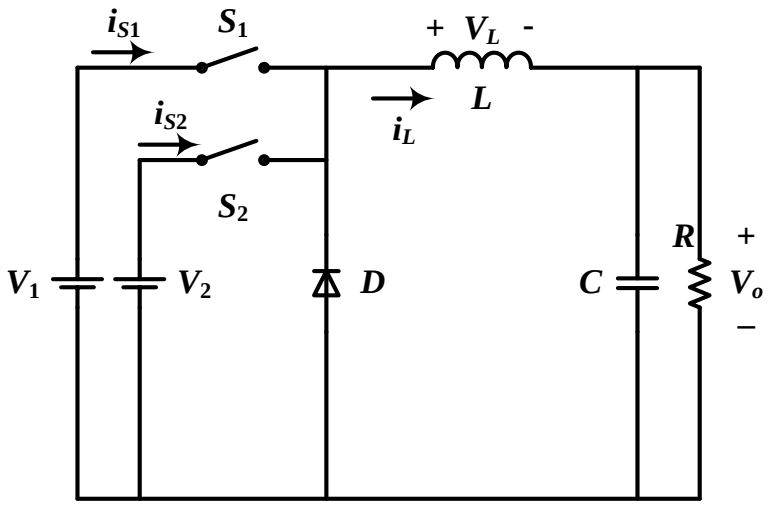


Figure 4.1. Circuit diagram of the restricted DI buck converter.

Table 4.1. Modes of Operation of a DI Restricted Buck Converter

Mode	S_1	S_2	V_L	V_D
I	On	Off	V_1-V_0	-V_1
II	Off	On	V_2-V_0	-V_2
III	Off	Off	-V_0	0
IV	On	On	Not allowed	

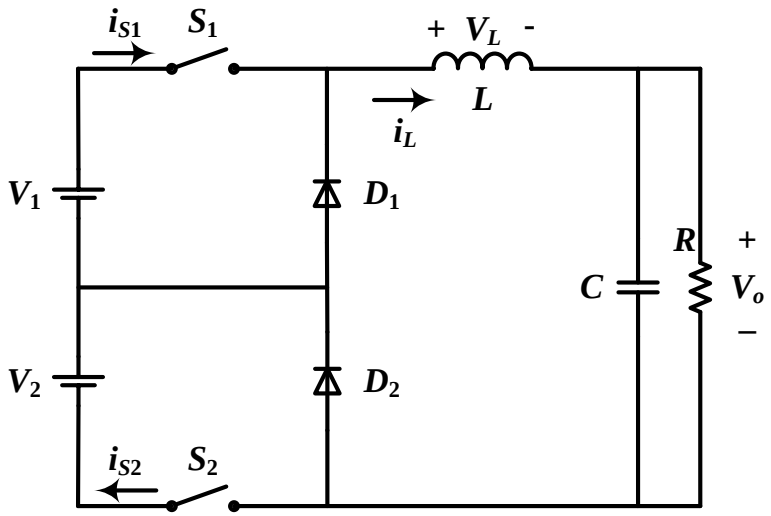


Figure 4.2. Circuit diagram of the non-restricted DI buck converter.

Table 4.2. Modes of Operation of a DI Non-Restricted Buck Converter

Mode	S_1	S_2	V_L	V_{D1}	V_{D2}
I	On	Off	V_1-V_0	-V_1	0
II	Off	On	V_2-V_0	0	-V_2
III	Off	Off	-V_0	0	0
IV	On	On	V_1+V_2-V_0	-V_1	-V_2

For both topologies, the steady-state input-output voltage relationship is

$$V_0 = D_1V_1 + D_2V_2 \tag{4.1}$$

where D_1 and D_2 are the on-time duty ratios of switches S_1 and S_2, respectively.

4.1.1. Dead-Time Control Scheme Considering Modes I, II, and III. Modes I, II and III are common in both topologies. The equations in this sub-section are developed based on the assumption that the operation of the converters is restricted to these three modes. The steady-state inductor current waveform in this case is shown in Figure 4.3. It is clear that $D_1+D_{12}+D_2+D_{21}=1$. Using this figure and Table 4.1 one can write

$$i_{\max 1} = i_{\min 1} + \frac{(V_1 - V_0)}{L} D_1 T \tag{4.2}$$

$$i_{\max 2} = i_{\min 1} + \frac{V_0}{L} D_{21} T \tag{4.3}$$

$$\begin{aligned} i_{\min 2} &= i_{\max 2} - \frac{(V_2 - V_0)}{L} D_2 T \\ &= i_{\min 1} + \frac{V_0}{L} D_{21} T - \frac{(V_2 - V_0)}{L} D_2 T \end{aligned} \tag{4.4}$$

Equations (4.2), (4.3), and (4.4) describe i_{max1}, i_{max2}, and i_{min2} as functions of i_{min1} which is the inductor current at the beginning of the switching cycle.

If one tries to find the average inductor current in Figure 4.3, they should find the area of the four trapezoids. Using equations (4.2), (4.3), and (4.4) in this procedure leads to

$$\begin{aligned} i_{\min 1} = \langle i_L \rangle - \frac{T}{2L} [& (V_1 - V_0)(D_1^2 + D_1 D_{12}) + (V_2 - V_0)(D_2^2 - D_2 D_{12}) \\ & + V_0 (D_{12} D_{21} + 2 D_2 D_{21} + D_{21}^2] \end{aligned} \tag{4.5}$$

Again average inductor current I_L for a resistive load R is equal to

$$\langle i_L \rangle = I_L = V_0 / R \tag{4.6}$$

Equations (4.2), (4.3), (4.4), (4.5) indicate that i_{max1}, i_{max2}, i_{min1}, and i_{min2} all depend $D_{21}T$ which is named as the dead-time. Now, the average current equations for sources V_1 and V_2 can be derived.

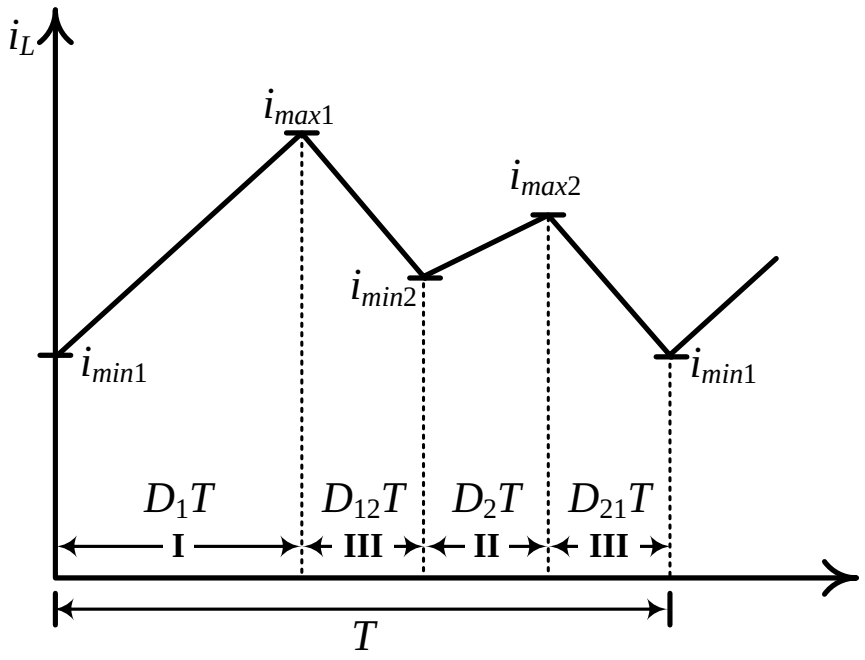


Figure 4.3. Steady-state inductor current waveform for Modes I, II, and III.

Average switch currents $\langle i_{s1} \rangle$ and $\langle i_{s2} \rangle$ can be described by the following equations

$$\langle i_{s1} \rangle = (i_{\max 1} + i_{\min 1}) \frac{D_1}{2} \tag{4.7}$$

$$\langle i_{s2} \rangle = (i_{\max 2} + i_{\min 2}) \frac{D_2}{2} \tag{4.8}$$

Considering equations (4.7) and (4.8), it can be concluded that dead-time $D_{21}T$ can be used to control the average value of input currents $\langle i_{s1} \rangle$ and $\langle i_{s2} \rangle$. The ratio

between average switch current i_{s1} and i_{s2} is defined as α. Or

$$\alpha = \frac{\langle i_{s1} \rangle}{\langle i_{s2} \rangle} \tag{4.9}$$

Consequently, α can be controlled as well. Therefore, it can be concluded that D_{21} can be used as a control variable when the ratio between the input currents is desired to be controlled.

4.1.2. Dead-Time Control Scheme Considering Modes I, II, III, and IV. The inductor current waveform when Mode IV is also included is depicted in Figure 4.4. Mode IV only takes place in the non-restricted DI buck converter when the conduction of the switches overlaps. In this mode, both of the switches are ON for the overlap time $D_{12}T$. The average current equations are derived from the inductor current waveform. It is clear that $D_1+D_{12}+D_2+D_{21}=1$. Using Figure 4.4 and Table 4.2, one can write

$$i_{\min 2} = i_{\min 1} + \frac{(V_1 - V_0)}{L}(-D_{21} - D_2)T \tag{4.10}$$

$$\begin{aligned} i_{\max 1} &= i_{\min 2} + \frac{(V_1 + V_2 - V_0)}{L} D_{12} T \\ &= i_{\min 1} + \frac{(V_1 - V_0)}{L}(-D_{21} - D_2)T + \frac{(V_1 + V_2 - V_0)}{L} D_{12} T \end{aligned} \tag{4.11}$$

$$i_{\max 2} = i_{\min 1} + \frac{V_0}{L} D_{21} T \tag{4.12}$$

Equations (4.10), (4.11), and (4.12) describe i_{min2}, i_{max1}, and i_{max2} as functions of i_{min1} which is the inductor current at the beginning of the switching cycle.

Similar to the previous sub-section, one can find i_{min1} by attempting to find the average inductor current using equations (4.10), (4.11), and (4.12).

$$i_{\min 1} = \langle i_L \rangle - \frac{V_0 (-D_1)}{2L} T + \frac{V_2 D_2 (2 - D_1 - D_2)}{2L} T + \frac{V_2 D_2 D_{21}}{L} T \tag{4.13}$$

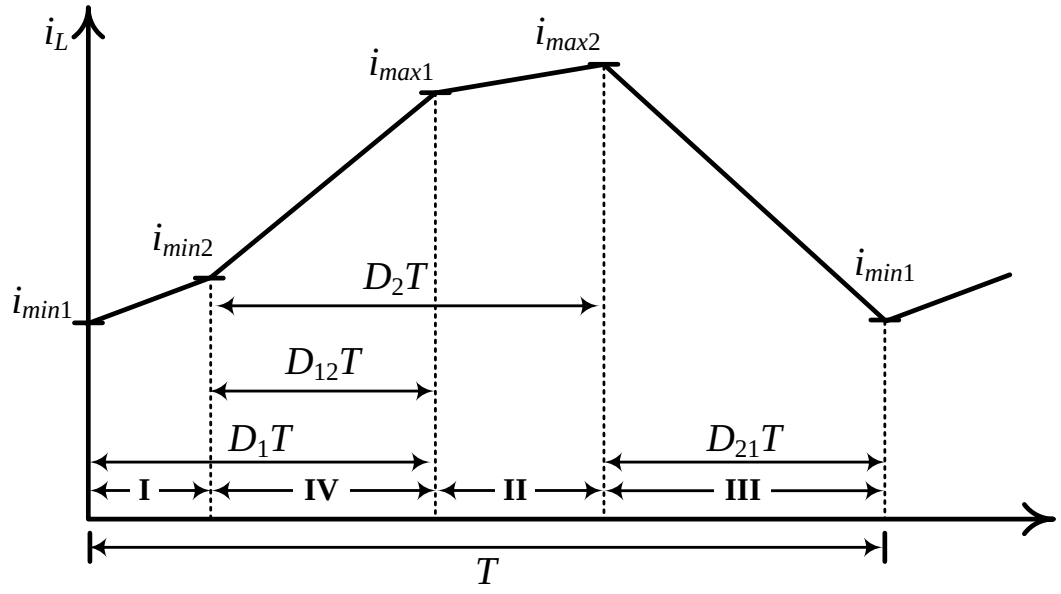


Figure 4.4. Steady-state inductor current waveform when Mode IV is also included.

Also, the average current supplied by each voltage source can be described as

$$\langle i_{s1} \rangle = i_{\min 1} D_1 + \frac{(V_1 - V_0) D_1^2}{2L} T + \frac{V_2}{2L} (D_1 + D_2 + D_{21} - 1)^2 T \tag{4.14}$$

$$\langle i_{s2} \rangle = i_{\min 1} D_2 + \frac{(V_2 - V_0) D_2^2}{2L} T + \frac{(V_1 - V_0) D_1 D_2}{L} T + \frac{V_0 D_2 (D_1 + D_2 + D_{21} - 1)}{L} T - \frac{V_1}{2L} (D_1 + D_2 + D_{21} - 1)^2 T \tag{4.15}$$

From equations (4.13), (4.14), and (4.15), it can be observed that average switch currents $<i_{s1}>$ and $<i_{s2}>$ are related to i_{min1} which in turn is related to dead-time $D_{21}T$. Thus, it can be concluded that average switch currents are dependent on the dead-time $D_{21}T$ even in Mode IV. From Figure 4.5, it can be observed that the range of α w.r.t $D_{21}$is increased due to Mode IV. The non-overlap region corresponds to Modes I, II, III and the overlap region corresponds to Mode IV. Thus the non-restricted topology (Figure 4.2) has greater range of α compared to restricted topology (Figure 4.1).

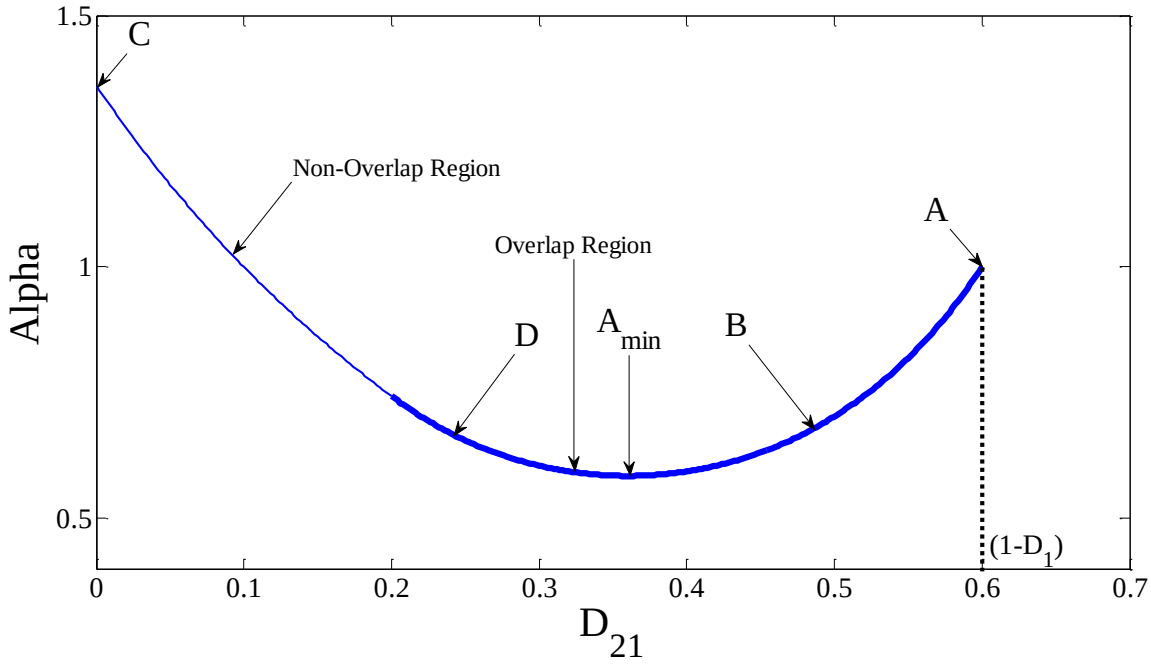


Figure 4.5. α vs. D_{21} for the non-restricted DI buck topology.

4.2. IMPLEMENTATION OF DEAD-TIME CONTROL

The dead-time control scheme for the non-restricted DI buck converter is implemented by using D_{21} as an extra control variable. The control objective of regulating output voltage V_0 while average source currents $\langle i_{s1} \rangle$ and $\langle i_{s2} \rangle$ are controlled can be achieved with the help of a voltage compensator, a current compensator, and a dead-time compensator which will regulate the dead-time $D_{21}T$. The block diagram of the system is shown in Figure 4.6. Switch currents i_{s1} and i_{s2} are sensed and fed to the current compensator and the dead-time compensator. In the dead-time compensator, the measured current values are converted into average values $\langle i_{s1} \rangle$ and $\langle i_{s2} \rangle$. Alpha (α) is calculated for each cycle as $\langle i_{s1} \rangle / \langle i_{s2} \rangle$ and compared with the α_{ref} value which is $I_{ref1} / \langle i_{s2} \rangle$. The current compensator is used to regulate the average current $\langle i_{s1} \rangle$ to the

reference value of I_{ref1} through the control of duty ratio D_1 and the value of I_{ref1} is varied by a system level controller when the power supplied by the second source varies. The voltage compensator is used to regulate output voltage V_0 to a constant value through the control of duty ratio D_2. Initially phase delay (*PD*) control was explored. In this control method the delay in phase between switch commands S_1 and S_2 is used to vary the dead-time. From Figure 4.5 it can be observed that α vs D_{21} plot is parabolic, α first decreases for increase in D_{21} and attains a minimum value A_{min} and again starts increasing. From Figure 4.5, it can also be observed that initially the *PD* is zero i.e. D_{21} is maximum, which corresponds to point A in the plot. The operating points of Figure 4.7 and Figure 4.8 correspond to points A and B of Figure 4.5, respectively, which is in the unrestricted region of the plot. When the *PD* is increased, the transition of the operating point happens from point A to B. It is observed that the range of α is limited due to the parabolic nature of α vs D_{21} plot. Thus the main drawback of *PD* control is that it operates in the region where the range of α is limited and it gets saturated.

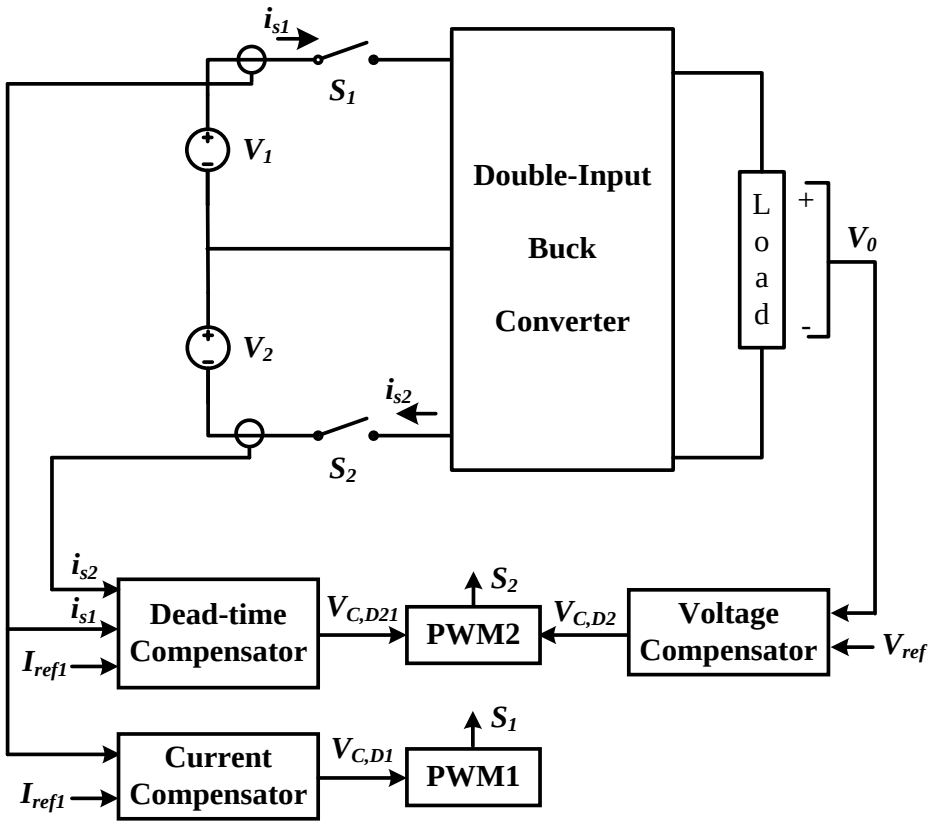


Figure 4.6. Block diagram of the overall system.

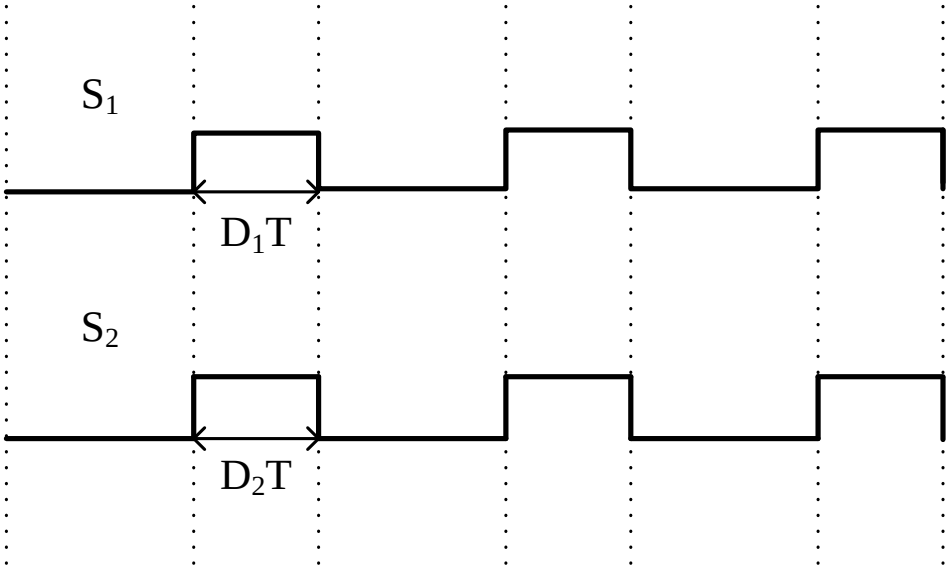


Figure 4.7. Switch commands S_1 and S_2 when $PD.T = 0$.

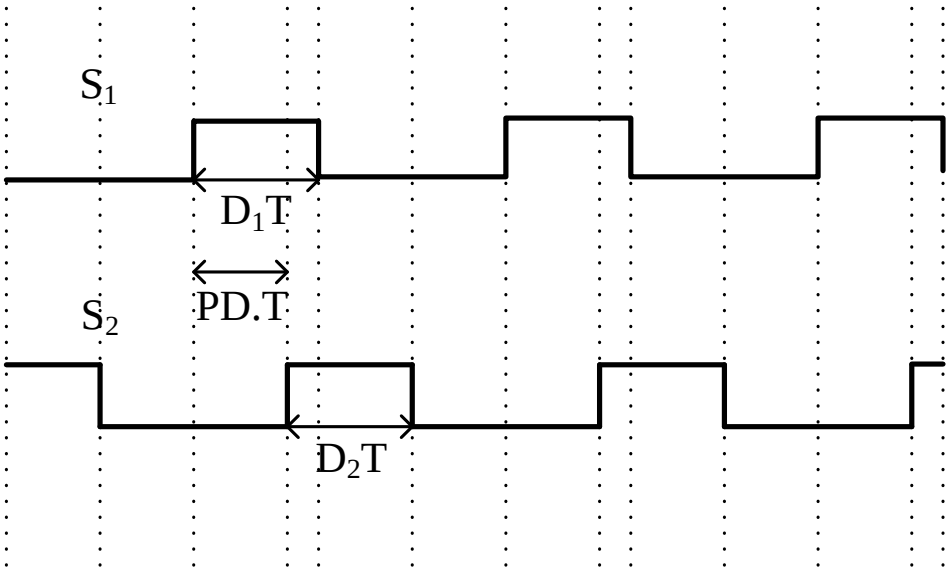


Figure 4.8. Switch commands S_1 and S_2 when $PD.T \neq 0$.

Dead-time control is implemented to utilize the maximum range of α. In this method D_{21} starts from zero, as shown in Figure 4.9, and varies till α reaches A_{min}, thus α varies in the entire extended range (shown in Figure 4.5). Figure 4.9 and 4.10 correspond to points C and D of Figure 4.5, respectively. The PWM implementation of dead-time control is shown in Figure 4.11. The control signals for D_2 and D_{21} are passed through PWM2 block in which a negative-slope ramp is used to generate the pulses S_2 and S_{21}. However, PWM1 block is a conventional PWM block with a positive-slope ramp being compared with the control voltage of D_1 to generate the switch command S_1.

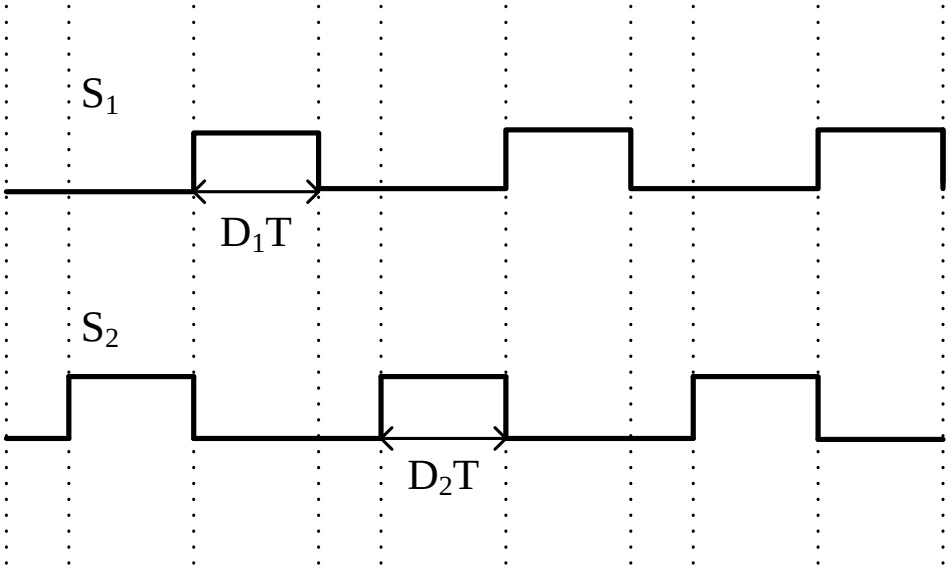


Figure 4.9. Switch commands S_1 and S_2 when $D_{21}.T = 0$.

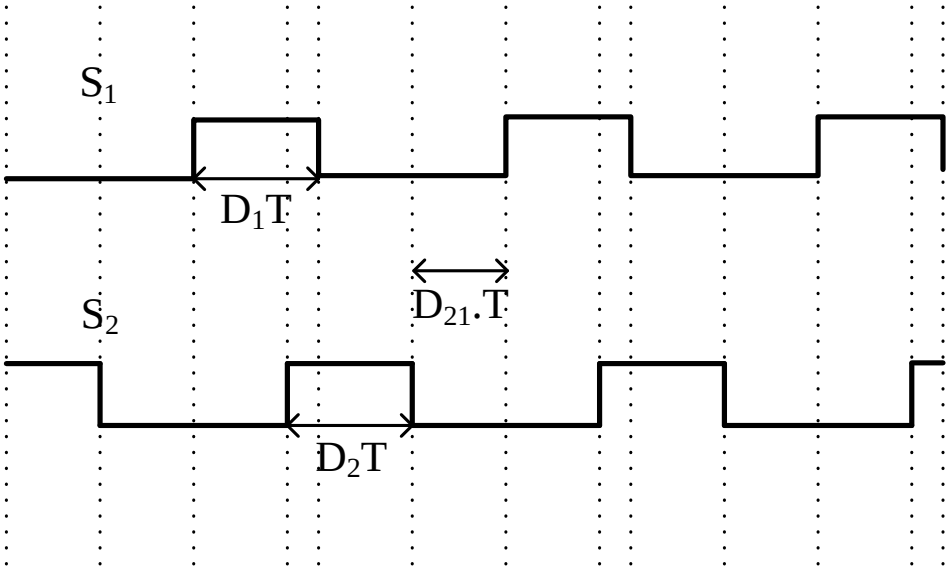


Figure 4.10. Switch commands S_1 and S_2 when $D_{21}.T \neq 0$.

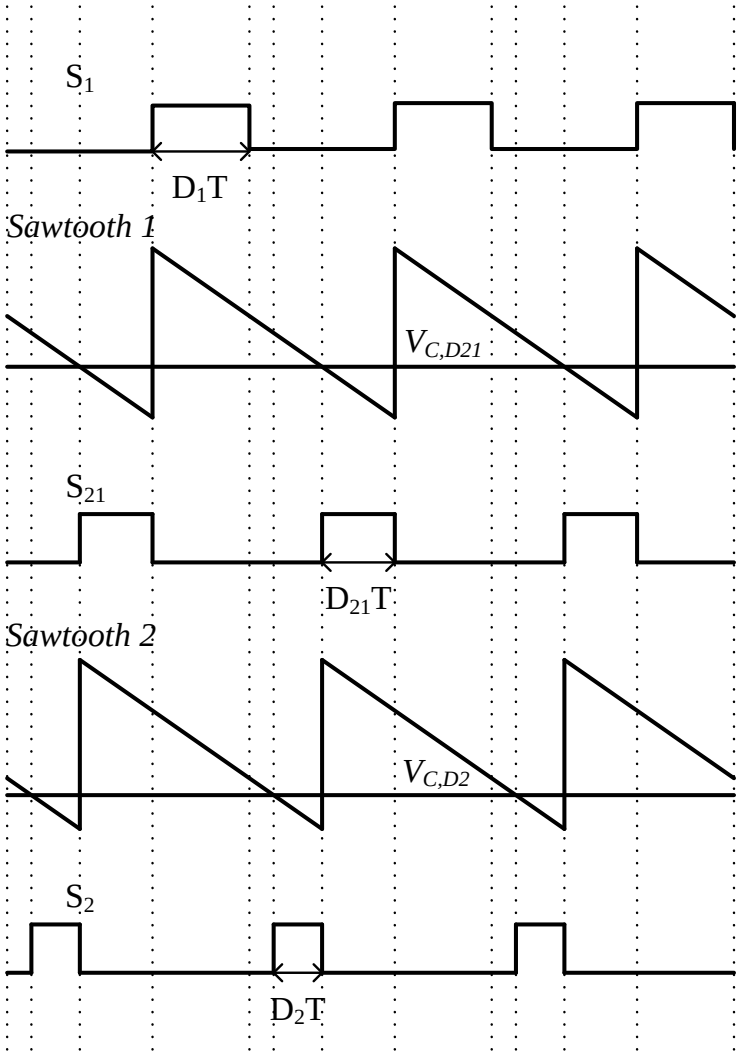


Figure 4.11. PWM implementation of dead-time control.

4.3. SIMULATION RESULTS

The relationship between α and dead-time D_{21} is depicted in Figure 4.12. In this figure, the duty ratios are selected in a way that the output voltage remains constant. It can be observed that the profile of the curve depends on the input voltages and duty ratios and α can be greater than or less than 1 depending on the operating point. It can also be observed that there are two regions of operation which are 1) the restricted (non-overlap)

region which is represented by the thin curve and 2) the non-restricted (overlap) region which is represented by the thick curve. In the non-overlap region, the system operates in Modes I, II, and III and the relation between α and D_{21} are based on the equations derived in sub-section 4.1.1. In the overlap region, the system operates in Modes I, II, III, and IV and the relation between α and D_{21} derived in sub-section 4.1.2. It must be noted that when the dead-time control scheme is used for the non-restricted DI buck converter, shown in Figure 4.2, the system can operate in both overlap and non-overlap regions. Therefore, the dead-time control benefits from an extended range.

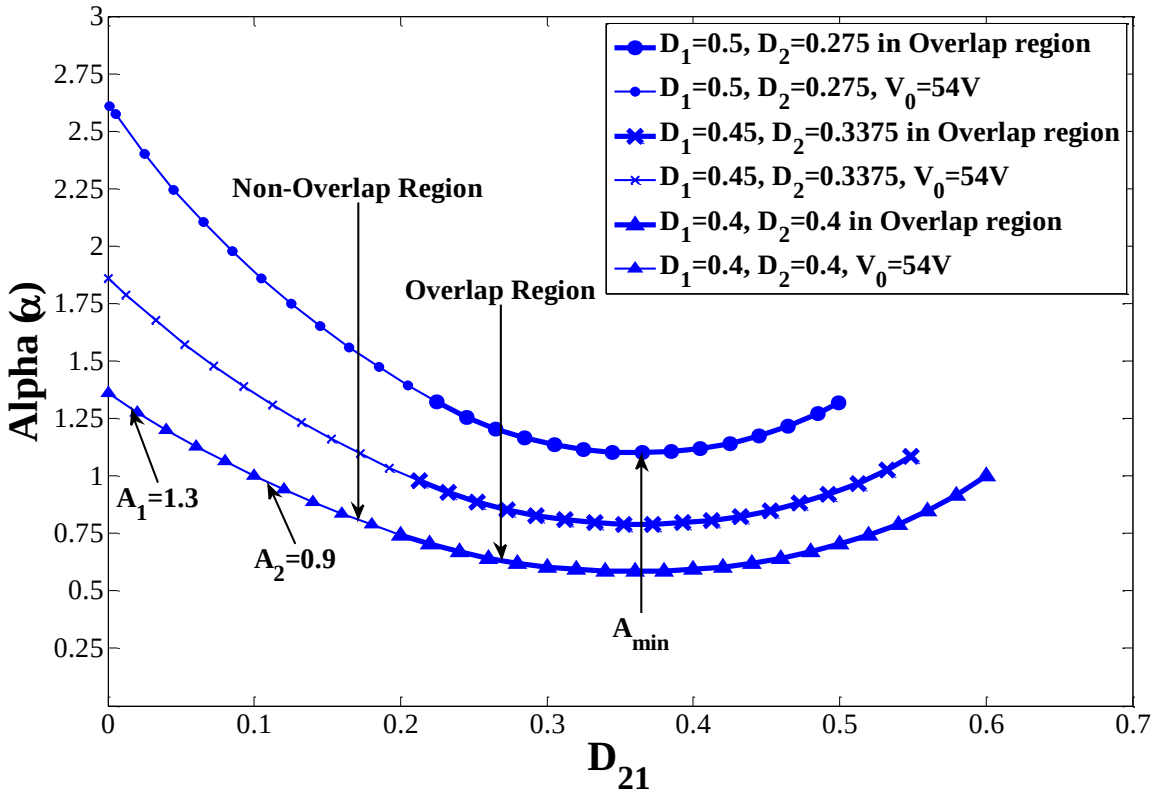


Figure 4.12. α vs. D_{21} for the non-restricted DI buck topology for different duty ratios.

Only the negative slope regions of the curves in Figure 4.12 are used in control implementation. This negative slope is the reason that a negative-ramp PWM scheme is chosen for PWM2 block. The following compensators are used to control the system: dead-time compensator (28,000/s), a current compensator $G_{c1}(s)$ and a voltage compensator $G_{c2}(s)$ are used whose transfer functions are -

$$G_{c1}(s) = \frac{6000}{s}\left(\frac{1+\frac{s}{6\pi*500}}{1+\frac{s}{6\pi*8000}}\right)$$

$$G_{c2}(s) = \frac{400}{s}\left(\frac{1+\frac{s}{2\pi*1000}}{1+\frac{s}{2\pi*50000}}\right)\left(\frac{1+\frac{s}{2\pi*1000}}{1+\frac{s}{2\pi*50000}}\right)$$

First, the converter is simulated with only dead-time control loop closed and V_1 = 75 V, V_2 = 60 V, f = 50 kHz, D_1 = 0.4, D_2 = 0.4, V_0 = 54 V, L = 100 µH, C = 50 µF, and R = 15 Ω remain constant. For a step change in α_{ref} from points α_2 (α_{ref} = 0.9) to point α_1 (α_{ref} = 1.3) as shown in Figure 4.12, the response of α is depicted in Figure 4.13. The system is then simulated with only two of the three control variables D_1 and D_2 being controlled for a constant load of 25 Ω, V_{ref} = 54 V and for a partial shading or decrease in state of charge situation where the I_{ref1} decreases from 1 A to 0.5 A.

The same test is carried out with all the three control variables controlled, i.e., D_1, D_2 and D_{21} and in this case also V_{ref} = 54 V and I_{ref1} decreases from 1 A to 0.5 A. The average switch currents I_{s1}, I_{s2} and the output voltage V_0 waveforms for the system with and without dead-time control are compared in Figures 4.14, 4.15, and 4.16, respectively. It can be clearly seen from Figures 4.14 and 4.15 that the I_{s1} is settling at the commanded currents of 1 A and 0.5 A and the other current I_{s2} is changing accordingly to meet the

load demand. It can also be observed from Figures 4.15 and 4.16 that the I_{s2} and V_0 are settling much faster when dead-time control scheme is included in the system. And it can also be observed from Figure 4.16 that the output voltage V_0 has a lower overshoot for the case with dead-time control when compared to the case without dead-time control which clearly indicates that the dynamic performance of the system is improved when dead-time D_{21} is also controlled along with the switch commands D_1 and D_2. Therefore, though the control objective is achieved in both the cases including the dead-time control scheme speeds up the system and gives an extra degree of freedom in controlling the input currents of the system.

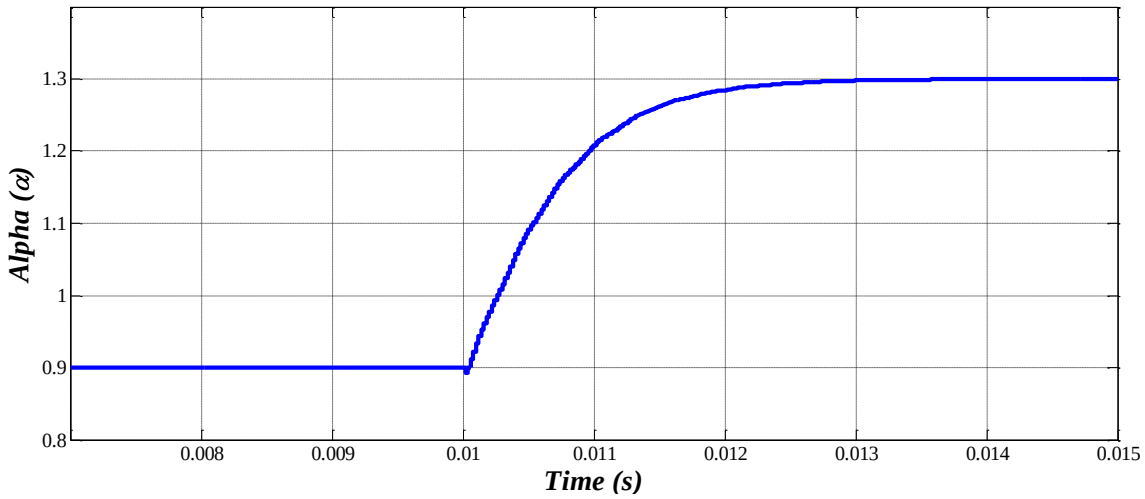


Figure 4.13. Dead-time D_{21} control for step change in α_{ref} from 0.9 to 1.3.

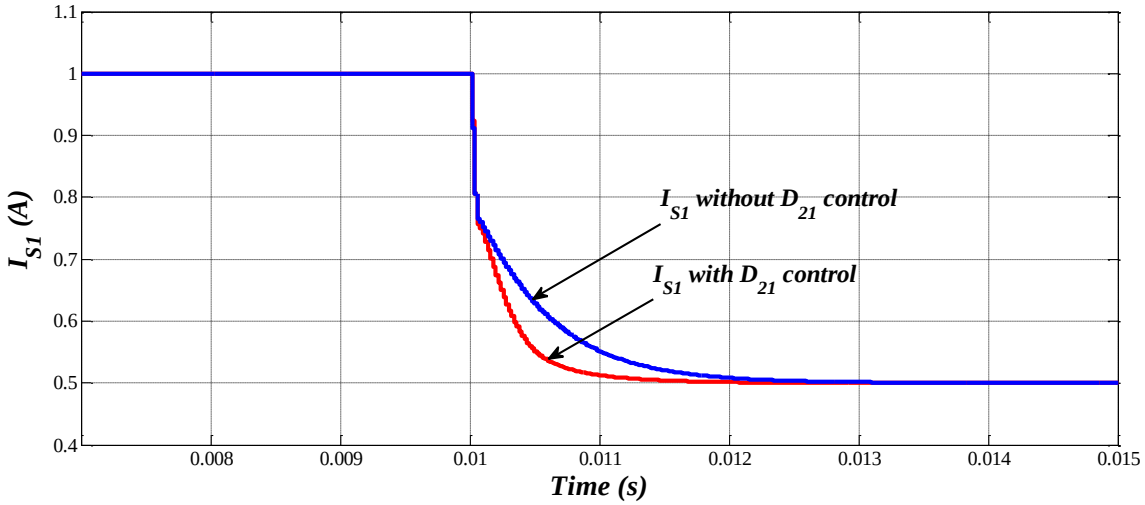


Figure 4.14. Average current of switch 1 I_{s1} waveform with and without dead-time D_{21} control.

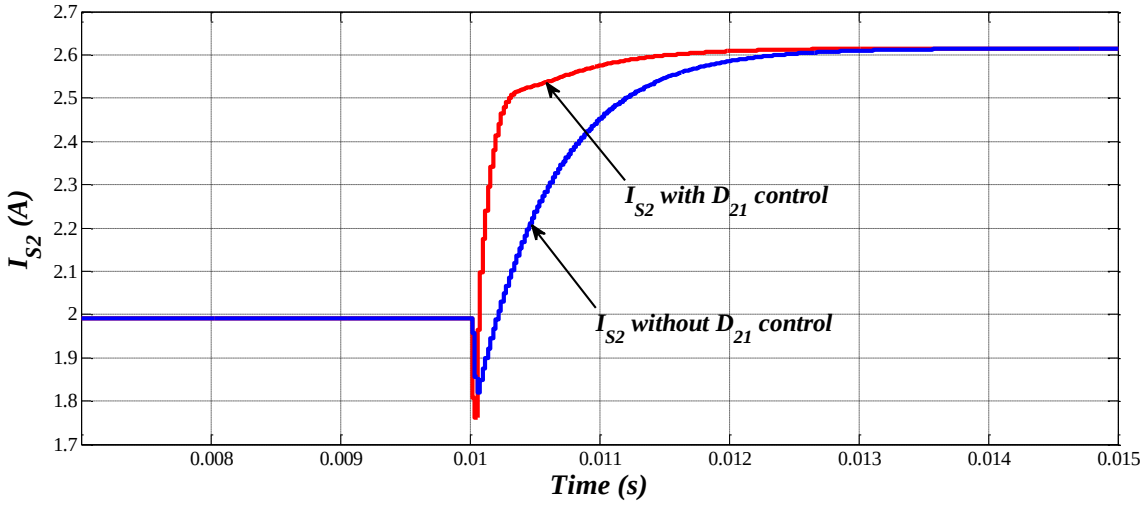


Figure 4.15. Average current of switch 1 I_{s2} waveform with and without dead-time D_{21} control.

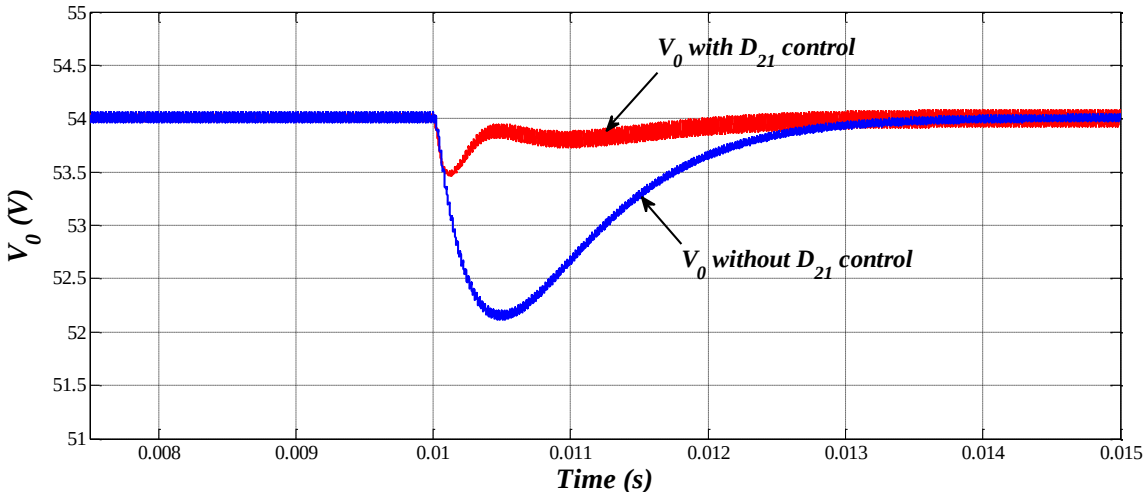


Figure 4.16. Output voltage V_0 waveform with and without dead-time D_{21} control.

Another control method called the dead-time control has been introduced in this section. It is shown that the dead-time between switch commands has a direct impact on the input currents and can be used as an additional variable for control. In this control method the dead-time between the switch commands D_{21} is used as a third variable apart from the switch commands D_1 and D_2 to improve the dynamic performance of the system.

5. EXPERIMENTAL RESULTS

In hybrid systems, it is important to control the amount of power drawn from each of the sources. When the power supplied by one of the sources decreases, the power drawn from the other source must be effectively managed to meet the load demand. Power sharing is necessary in hybrid energy systems like the wind-solar or battery/ultra-capacitor combinations. In [45], the author proposes the offset-time control for the closed loop control of the converter. It has been analytically proven that the offset-time control has better dynamics compared to the conventional method of independent control of control variables D_1 and D_2. In this method, the offset time $D_{12}T$ (see Figure 5.2) or the delay between switch commands is utilized as an additional control variable in addition to the actual control variables D_1 and D_2. The offset-time control method has been implemented for DI buckboost converter.

5.1. DI BUCKBOOST CONVERTER

Figure 5.1 shows the circuit diagram of the DI buckboost converter. This topology has mode restriction and both the switches S_1 and S_2 cannot be ON at the same time. Table 5.1 shows the modes of operation and inductor voltage of the converter. Figure 5.2 shows the typical inductor current waveform for the converter, where D_1 and D_2 are the ON time duty ratios of switches S_1 and S_2. Again, D_{12} and D_{21} are the offset-time duty ratios or the delay between the switch commands. The input to output voltage relationship is given by equation (5.1).

$$V_0 = \frac{D_1 V_1}{(1 - D_1 - D_2)} + \frac{D_2 V_2}{(1 - D_1 - D_2)} \tag{5.1}$$

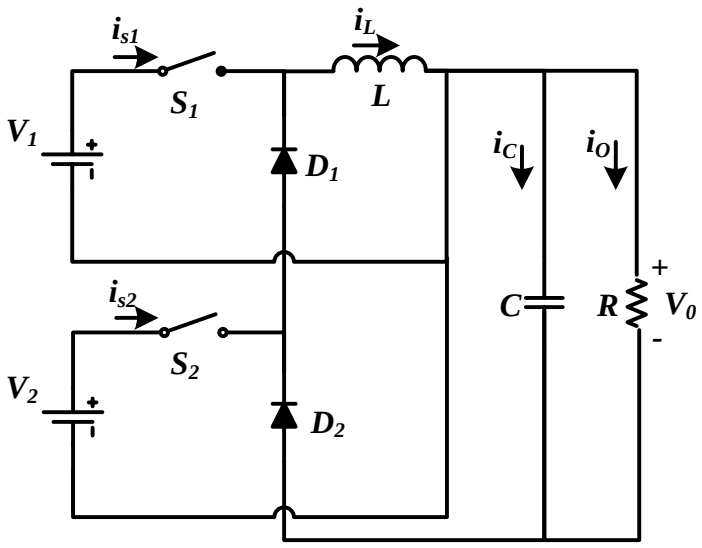


Figure 5.1. Circuit diagram of DI buckboost converter.

Table. 5.1. Modes of Operation of a DI Buckboost Converter

Mode	S_1	S_2	V_L
I	ON	OFF	V_1
II	OFF	ON	V_2
III	OFF	OFF	$-V_O$
IV	ON	ON	Not Allowed

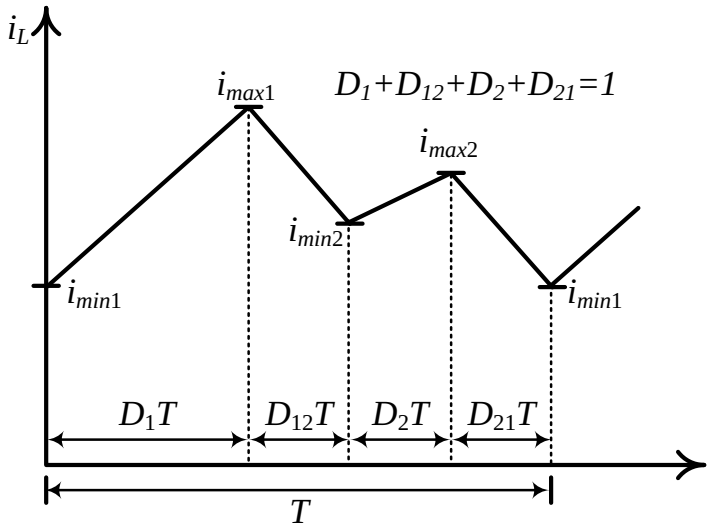


Figure 5.2. Inductor current waveform in the steady state operation.

5.2. OFFSET-TIME CONTROL

Figure 5.3 shows the block diagram of the overall system. The output voltage of the converter v_0 is regulated to a reference voltage V_{ref} by controlling D_1 through a voltage compensator. The input current from source 2 (i_{s2}) is regulated to a reference current I_{ref2} by controlling D_2 through a current compensator. In Figure 5.4, offset-time controller is shown where the average input currents i_{s1} and i_{s2} are calculated by integrating the switch currents over one switching cycle. The ratio of these currents gives α which is proportional to D_{12}. The relationship between α and D_{12} can be obtained by substituting equations (5.3) and (5.4) into (5.5). Figure 5.5 shows the typical plot between α and D_{12}, it can be observed that they almost have a linear relationship. The offset time duty ratio can be obtained by integrating the error between α and α_{ref} , which is the ratio of i_{s1} and i_{ref2}. Therefore a third loop is added to the system that controls the delay

between switch commands. Figure 5.6 shows the PWM implementation of the proposed control.

$$\alpha = \frac{\langle i_{s1} \rangle}{\langle i_{s2} \rangle} \tag{5.2}$$

$$I_L = \langle i_L \rangle = \frac{V_0}{R(1 - D_1 - D_2)} . \tag{5.3}$$

$$i_{\max 1} = \frac{1}{2Lf} \frac{[2V_0 D_2 D_{12} - V_2 D_2^{\,2} - \frac{V_1 D_1^{\,2}}{\alpha}]}{[D_2 - \frac{D_1}{\alpha}]} \tag{5.4}$$

$$\langle i_L \rangle = i_{\max 1} - \frac{1}{2Lf}[D_1 V_1 - D_2 V_2 + D_1 D_2 (V_2 - V_1) + 2D_2 (V_2 + V_0) D_{12}] \tag{5.5}$$

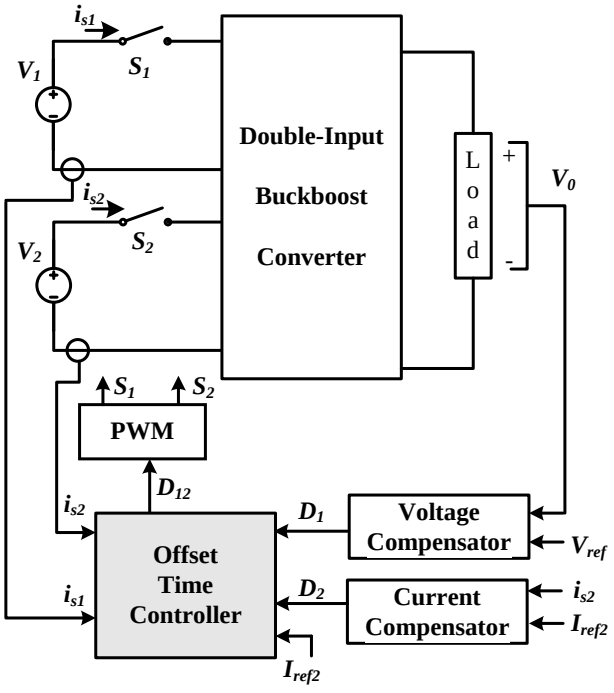


Figure 5.3. Block diagram of the overall system.

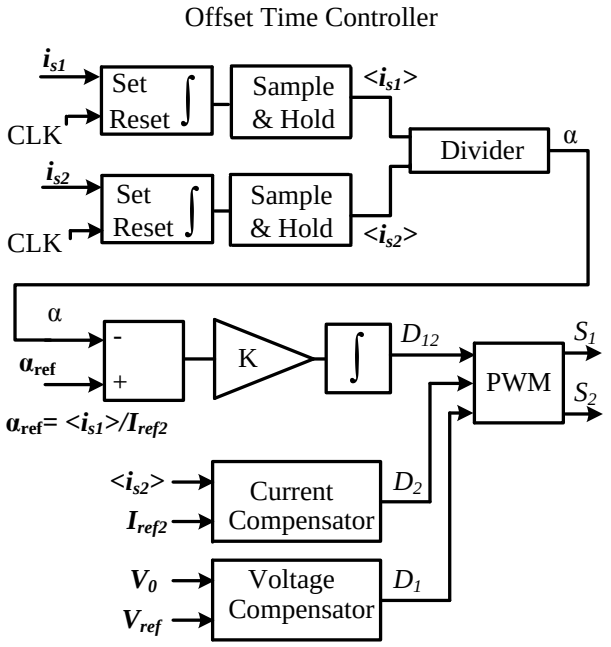


Figure 5.4. Block diagram of the power sharing controller.

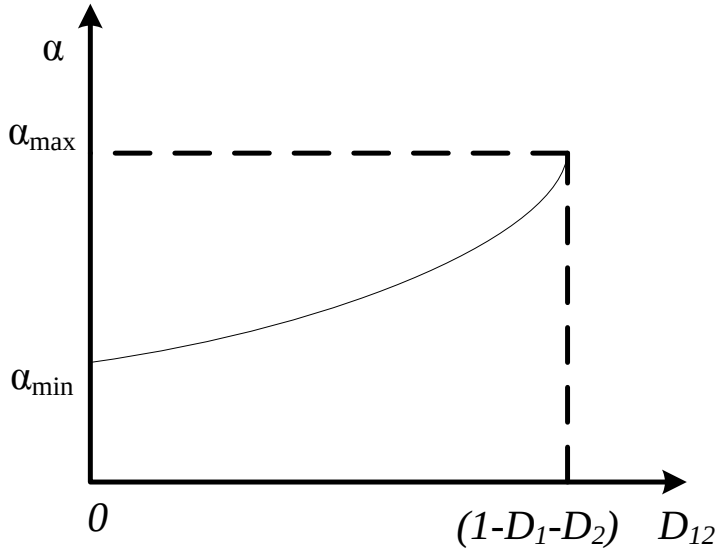


Figure 5.5. Typical plot of α vs D_{12}.

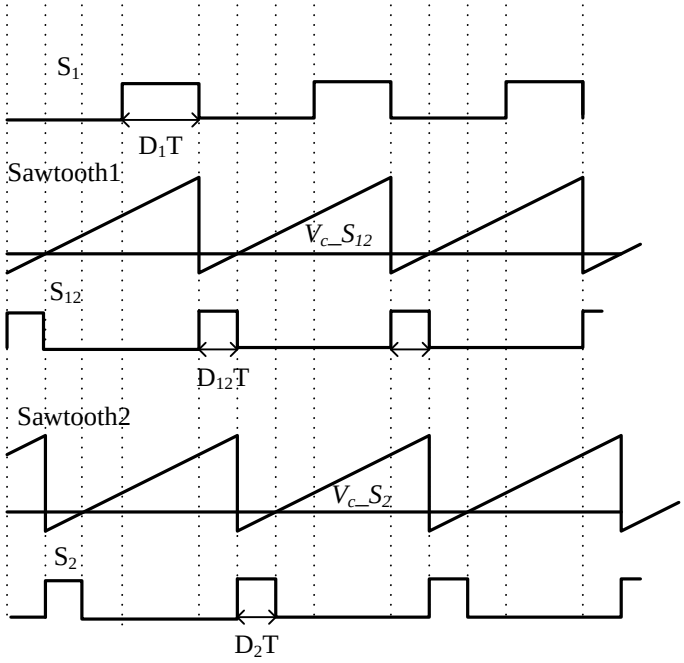


Figure 5.6. Pulse width modulation block and delay D_{12} between S_1 and S_2.

5.3. IMPLEMENTATION OF OFFSET-TIME CONTROL

The DI buckboost converter is designed and implemented for frequency of 30 KHz. A dual DC supply BK Precision 1761 DC Power Supply is used for the isolated voltage sources with 820μF input capacitors. Switches S_1 and S_2 are realized by N-channel MOSFETs STP20NF20. Schottky diodes MBR40250G are used for D_1 and D_2, the same diodes are used as blocking diodes for negating the effect of the anti-parallel diodes of the MOSFETs. To remove the high frequency oscillations in the switch currents RC-snubbers are used across the switches. Inductor of 180μH is used which is rated for a current of 11.4 A and has dc resistance of 0.045 Ω. Output capacitor of 47 μF is used with a constant load resistance of 15 Ω.

The converter was initially implemented without any closed loop control with the source voltages V_1 = 8.6 V and V_2 = 6.8 V, a dual supply signal generator was used to generate the duty ratios D_1 and D_2. The switch commands were applied to the MOSFETs through optocoupler drivers FOD3180. The inductor current is sensed by a sensing resistor R_{SENSE}. The value of R_{SENSE} used is 0.1667 Ω and the sensed current is then amplified by a factor of 6 to get the actual waveform. Figure 5.7 shows the output voltage V_0, inductor current I_L, and switch commands S_1, S_2 waveforms. It can be seen that for D_1 = 0.3, D_2 = 0.4, and f = 30 kHz the measured output voltage V_0 = 11.2 V.

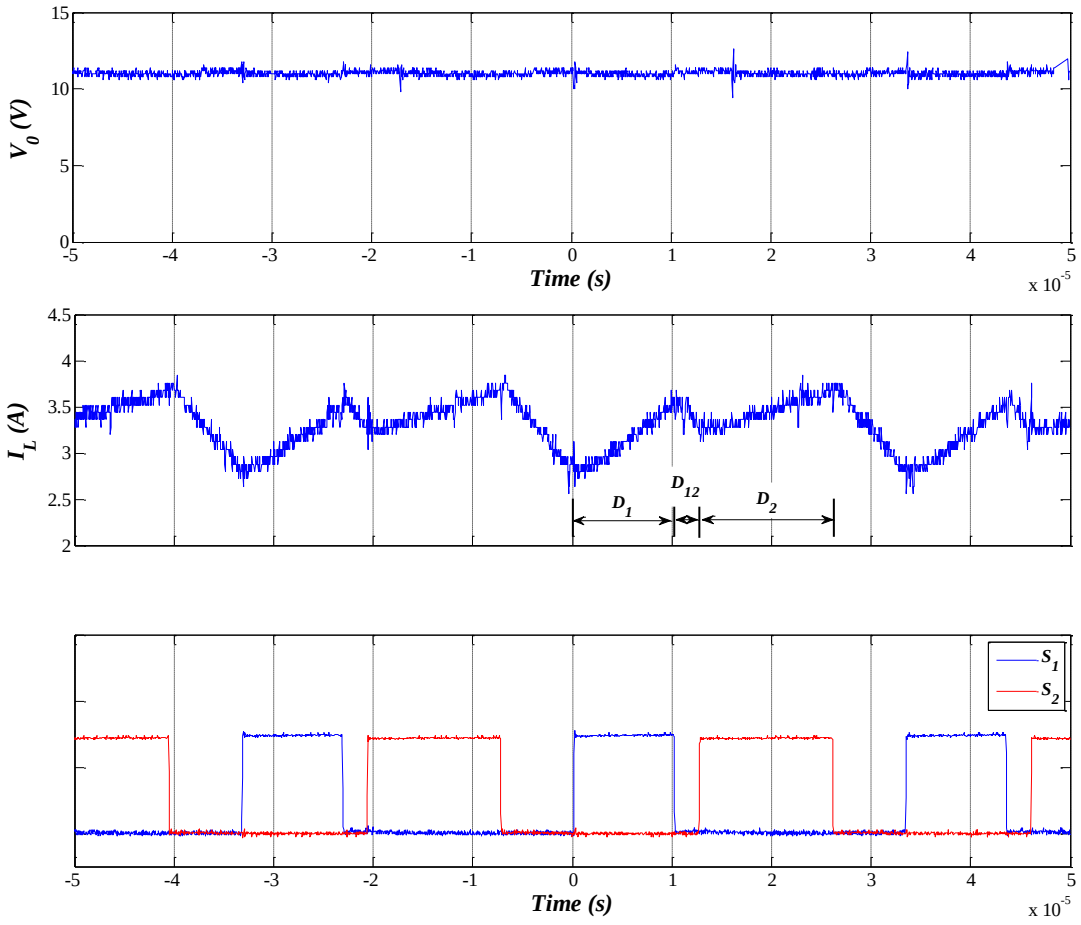


Figure 5.7. Output voltage V_0 and inductor current I_L waveforms for open loop operation with different D_{12}.

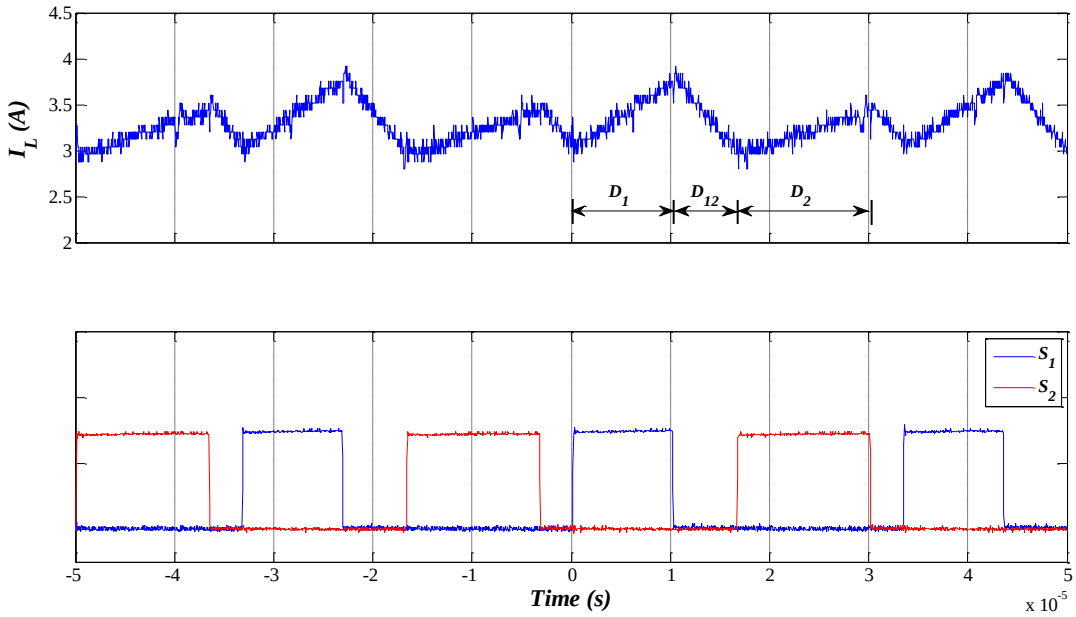


Figure 5.7. Output voltage V_0 and inductor current I_L waveforms for open loop operation with different D_{12}. (cont.)

The converter was then implemented with only voltage mode control; the circuit diagram for the same is shown in Figure 5.8. The voltage mode controller UC3526AN is used for generating the switch commands which are synchronized at the leading edges. Duty ratios D_1 and D_2 are always equal for this control. The output voltage of the converter is set by a 100 KΩ potentiometer across the output resistor. The frequency of the converter is set by selecting suitable values of C_T, R_T and R_D values for the oscillator of the controller UC3526AN. V_{ref} is 5.1 V which is obtained from the 18th pin of the controller. The voltage compensator is realized by the error amplifier of the controller as shown in Figure 5.9. The voltage compensator (G_{VC}) is given by –

$$G_{VC} = \frac{0.068s + 133.33}{s} \tag{5.6}$$

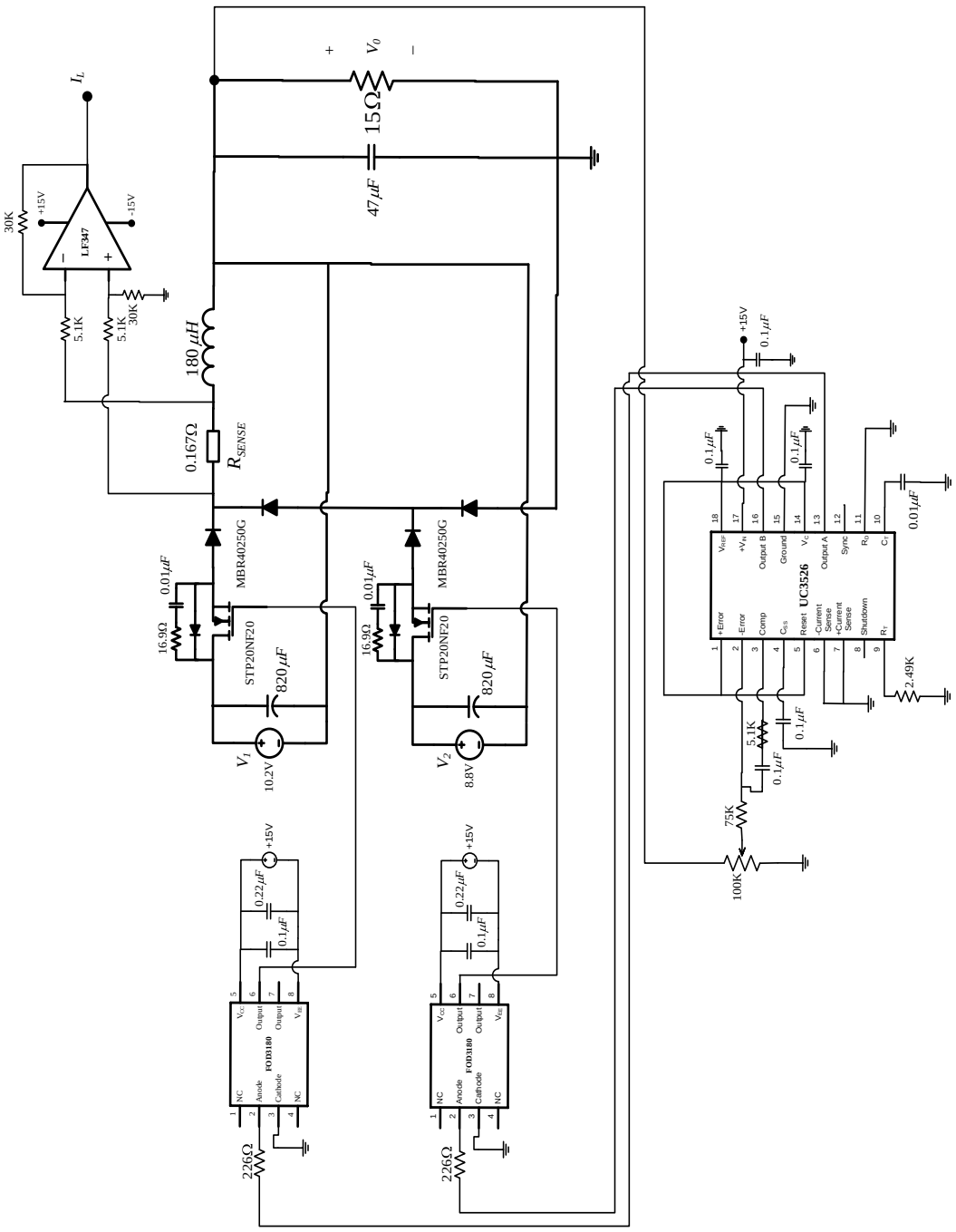


Figure 5.8. Circuit diagram for DI buckboost converter with voltage mode control.

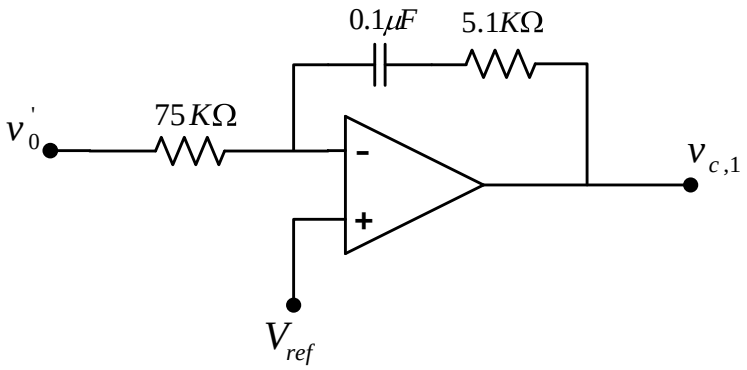


Figure 5.9. Voltage compensator using the error amplifier of UC3526AN.

From Figure 5.10, it can be seen that for V_1 = 10.2 V, V_2 = 8.8 V, and f = 30.3 kHz, output voltage V_0 is maintained at the reference voltage V_{ref} = 9.3 V and V_0 is kept regulated at V_{ref} for a step change in input voltage V_1 from 10.2 V to 14.5 V.

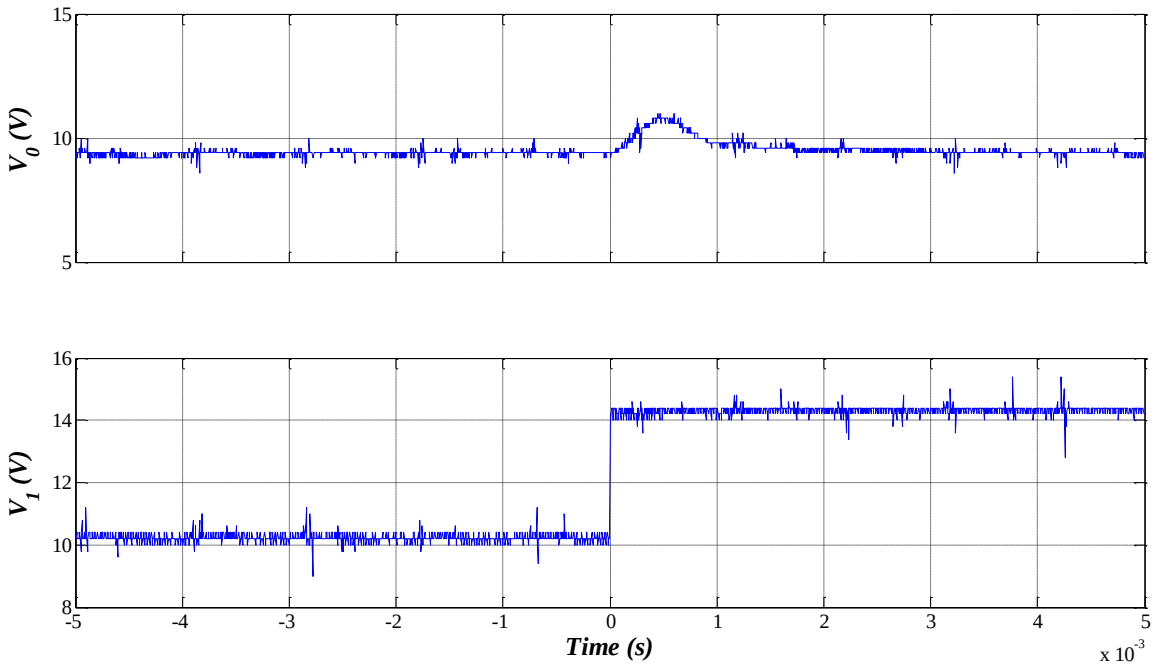


Figure 5.10. Output voltage V_0 for a step change in input voltage V_1 from 10.2 V to 14.5 V.

Average currents $<i_{s1}>$ and $<i_{s2}>$ are calculated by integrating the input currents i_{s1} and i_{s2} over one switching cycle using the dual switched integrator ACF2101 and then sampling the current at the end of the switching cycle using sample and hold amplifier AD783. The ratio of input currents α and α_{ref} is calculated by using the divider circuit of multiplier AD532 (see Figure 5.11).

Switch commands D_1, D_{12} and D_2 are synchronized at the falling edge. The synchronizing is done by connecting the differentiated signals of D_1 pulses to the 12^{th} pin (SYNC) of voltage controller UC3526AN that produces D_{12} (as shown in Figure 5.12). Similarly, D_{12} and D_2 are synchronized with each other; D_{12} then becomes the delay between switch commands D_1 and D_2 (see Figure 5.13).

The offset-time controller (see Figure 5.4) with current compensator (G_{IC}) and α-compensator (G_{OC}) is implemented by the error amplifier of the controller UC3526AN. The current compensator and offset-time compensators are given by -

$$G_{IC} = \frac{0.013s + 666.67}{s} \tag{5.7}$$

$$G_{OC} = \frac{6666.67}{s} \tag{5.8}$$

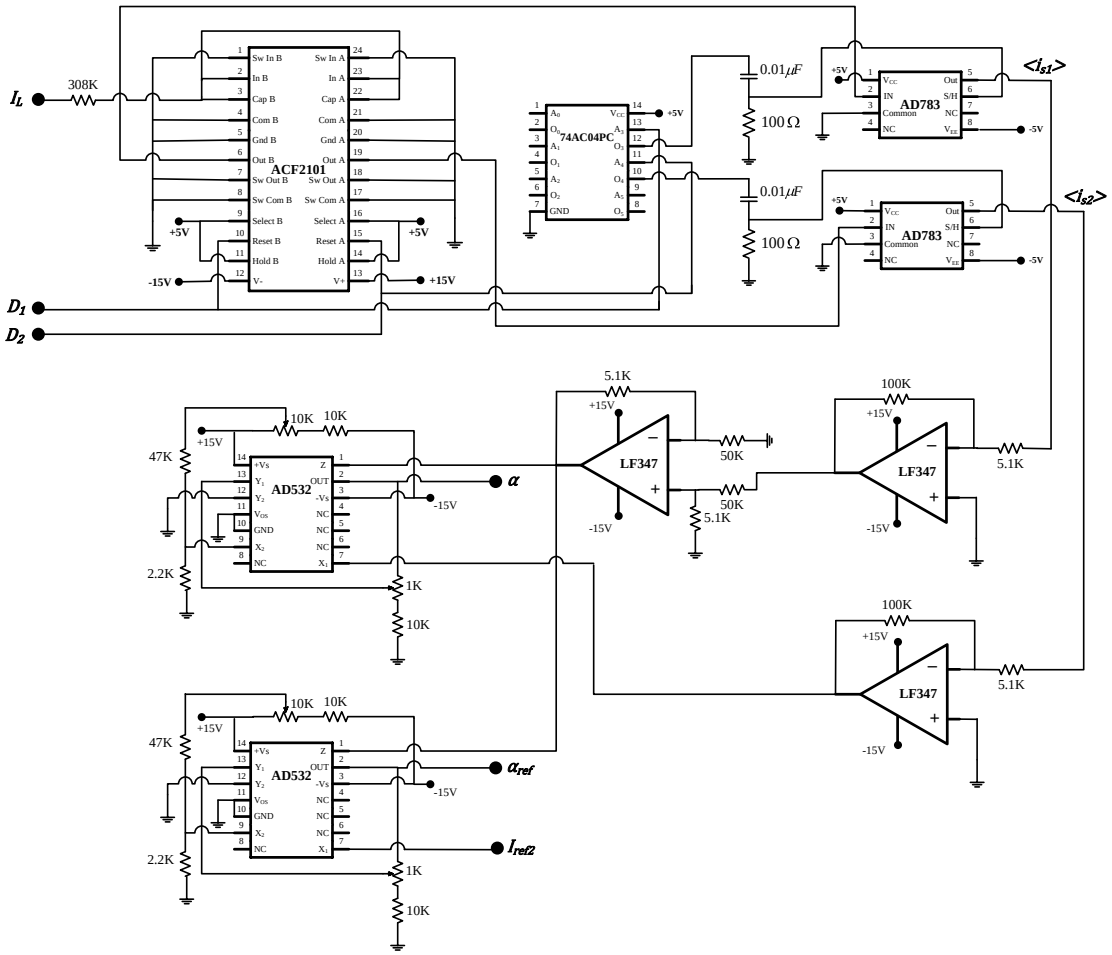


Figure 5.11. Circuit diagram for calculation of average currents $<i_{s1}>$ and $<i_{s2}>$ and ratio of input currents α and α_{ref}.

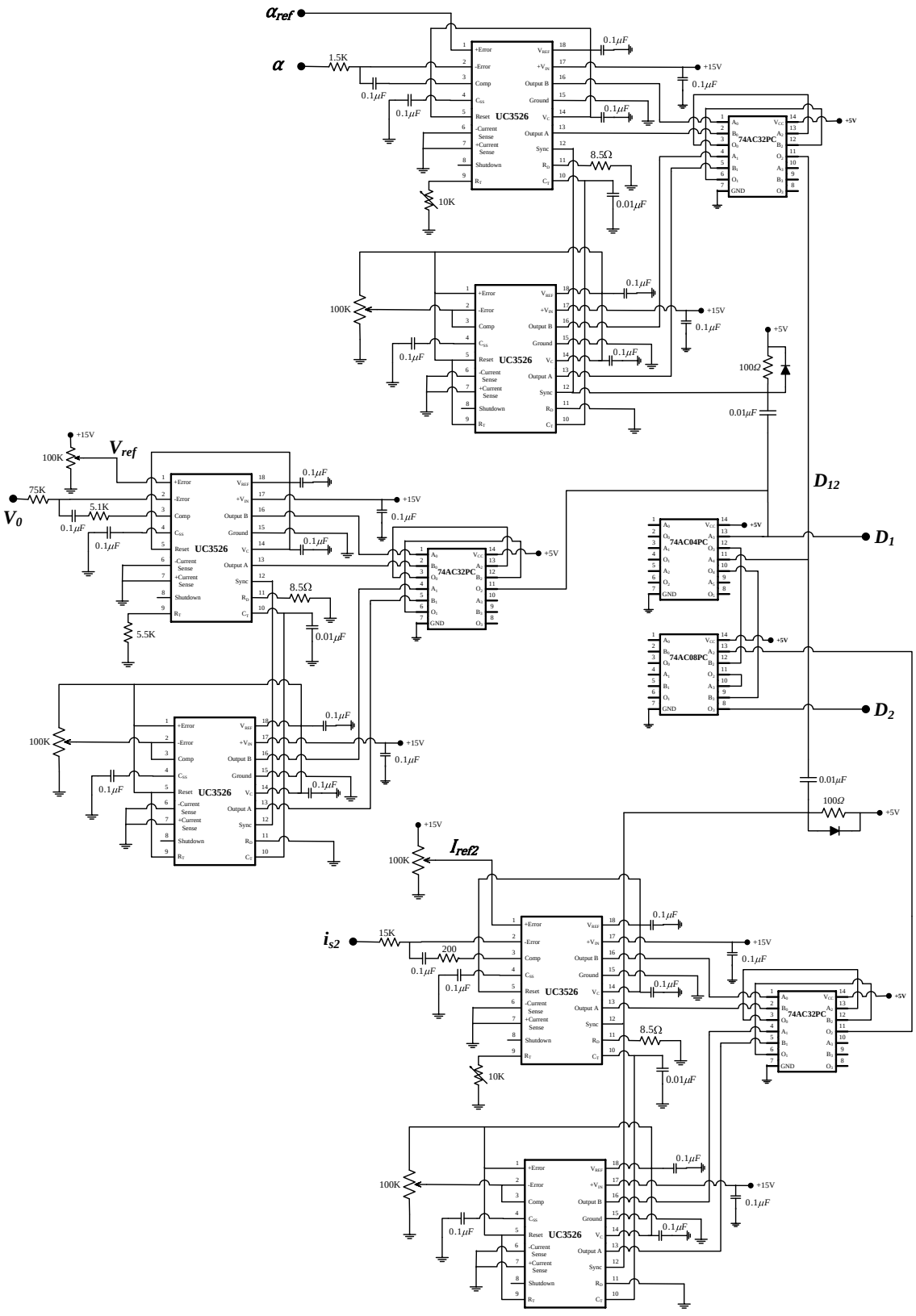


Figure 5.12. Circuit diagram for synchronizing D_1, D_{12} and D_2.

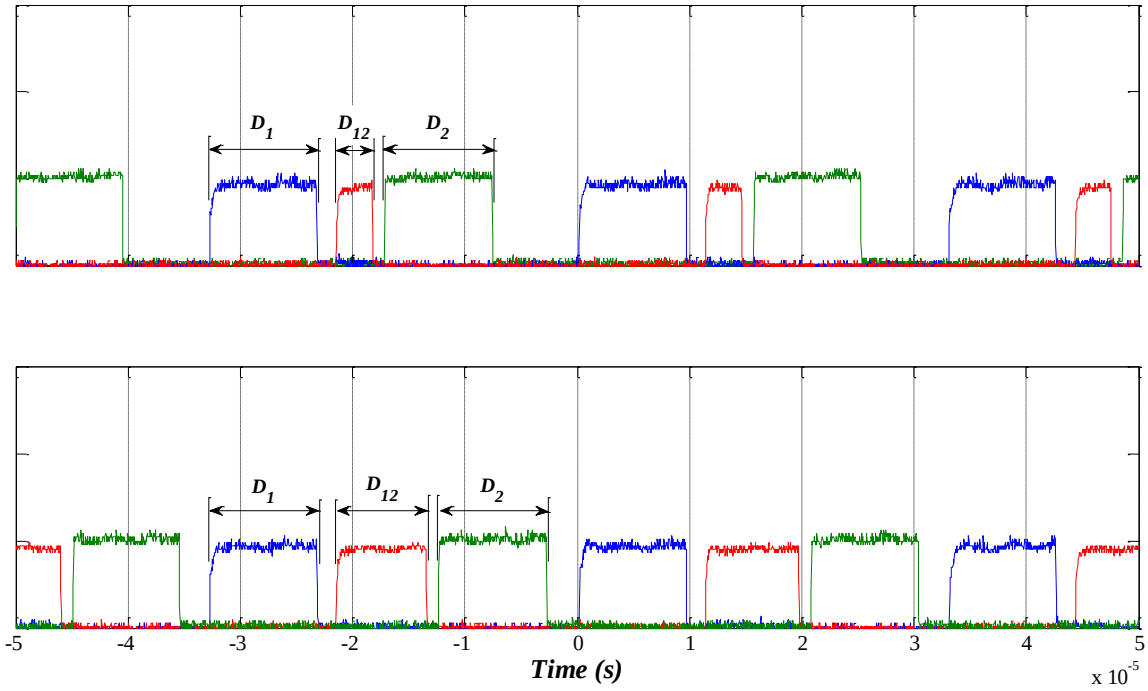


Figure 5.13. Synchronized D_1, D_{12} and D_2 pulses.

Figure 5.14 shows the V_0, I_{S1}, I_{S2}, and I_{ref2} waveforms with all the three loops closed. The input voltages V_1 = 10.2 V, V_2 = 8.8 V, and f = 30.3 KHz. Again, V_{ref} and I_{ref2} are set at 9.3 V and 0.3 A, respectively. The measured I_{S1}, I_{S2}, and I_{ref2} are amplified by a factor of 20 to reject measurement noise. From Figure 5.14, it can be seen that V_0 is regulated at 9.3 V, I_{S2} at 0.3 A, and I_{S1} is 0.275 A. For a step change in I_{ref2} from 0.3 A to 0.225 A, I_{S2} follows I_{ref2} and I_{S1} increases to cater the load while keeping the output voltage V_0 regulated at 9.3 V.

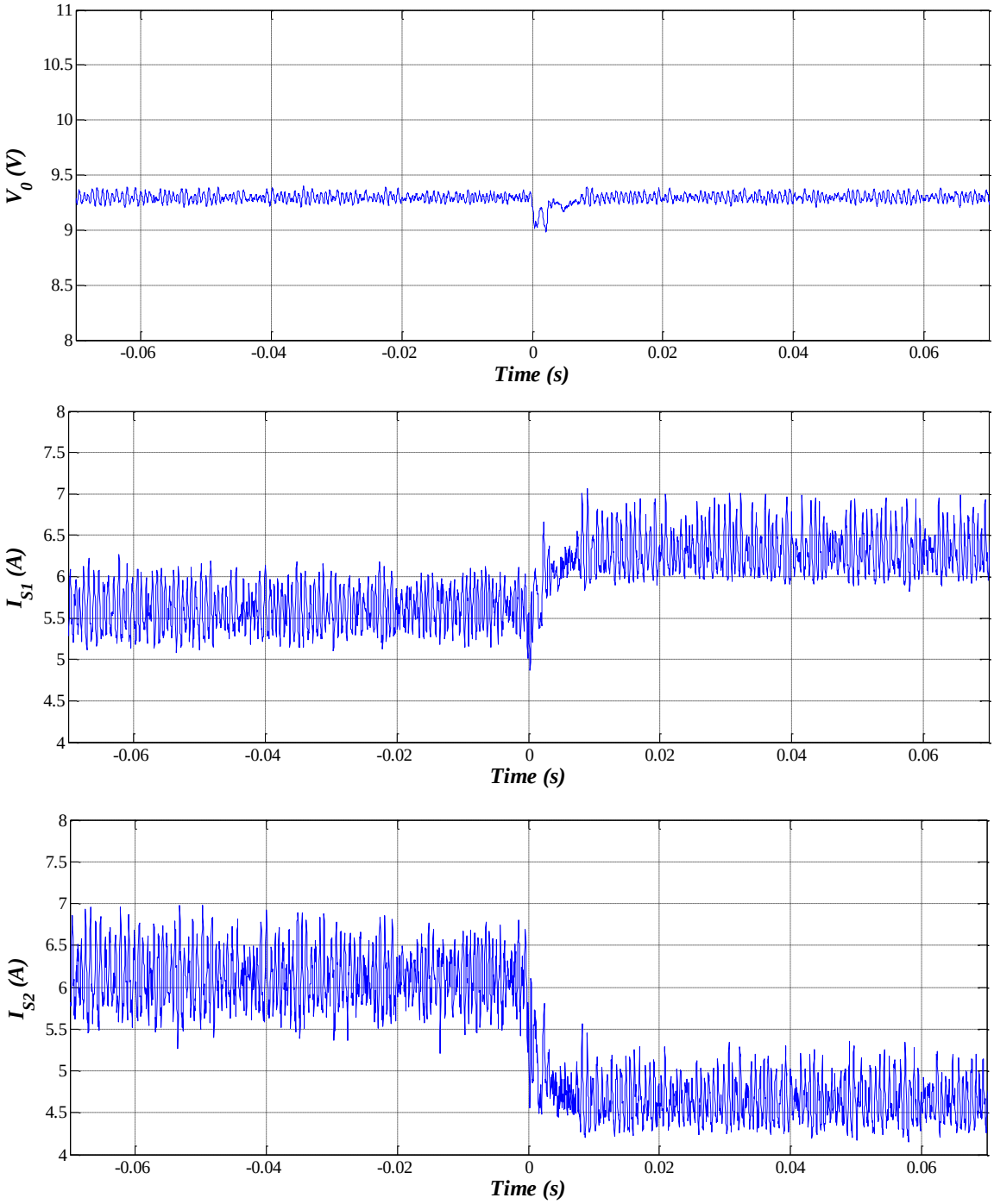


Figure 5.14. V_0, I_{S1}, I_{S2}, and I_{ref2} waveforms with offset-time control.

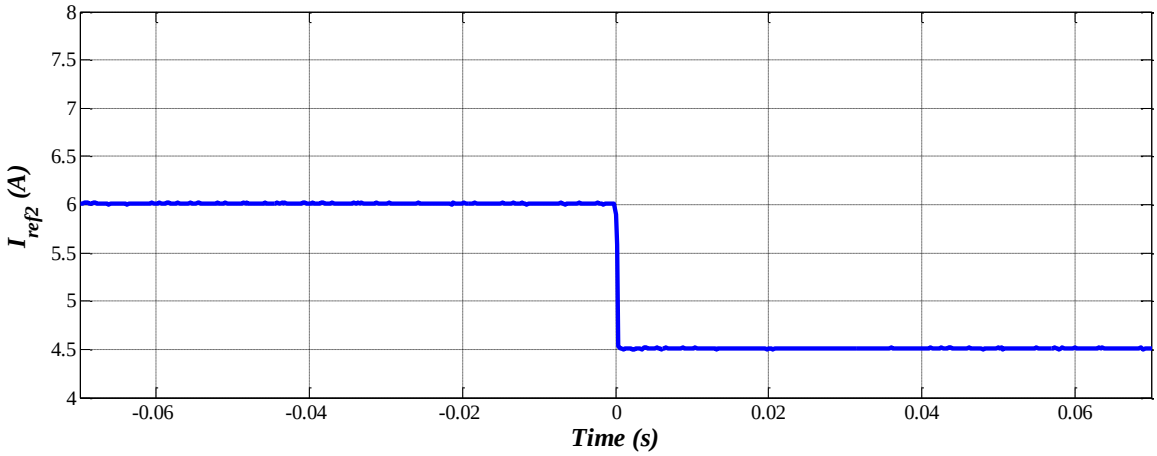


Figure 5.14. V_0, I_{S1}, I_{S2}, and I_{ref2} waveforms with offset-time control. (cont.)

It has been experimentally verified that effective power sharing can be achieved in a DI buckboost converter by offset-time control method. In this method, the ratio of input currents is used to control the offset-time between the switch commands for better dynamic performance. The offset-time has a near linear relationship with the ratio of input currents and hence can be used as a third variable for achieving the control objective.

6. BI-DIRECTIONAL DI BUCK CONVERTER FOR HYBRID ELECTRIC VEHICLES

MIPECs can find applications in hybrid electric vehicles where the objective is to integrate sources which have high power density (e.g. ultra-capacitors) with other sources that have high energy density (e.g. Batteries). This way the advantages of both types of sources can be obtained [39]. In these types of applications the control objective is to supply the peak load demand from the source having the higher power density while the base load is supplied by the other source having higher energy density, thus the ultra-capacitors can be used to supply the peak load demands and the battery can be used to supply the base load. During regenerative braking, the energy can be stored back in the ultra-capacitors (as shown in Figure 6.1).

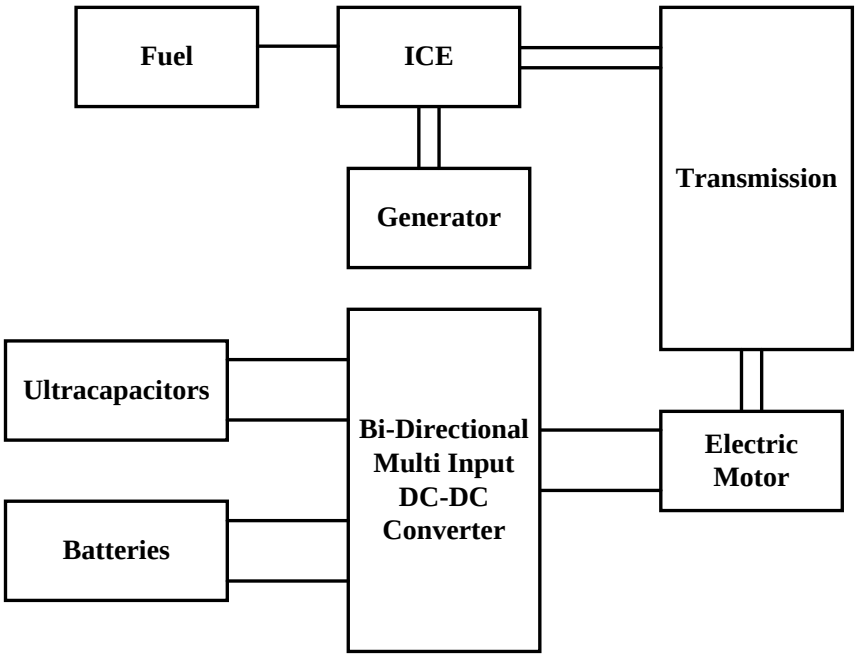


Figure 6.1. Block diagram of a bi-directional MIPEC in hybrid electric vehicle.

6.1. BI-DIRECTIONAL DI BUCK CONVERTER

The DI buck converter (shown in Figure 6.2) is connected to a permanent magnet synchronous machine (PMSM) to implement the scheme shown in Figure 6.1. In this topology, switches S_1 and S_2 cannot be ON simultaneously.

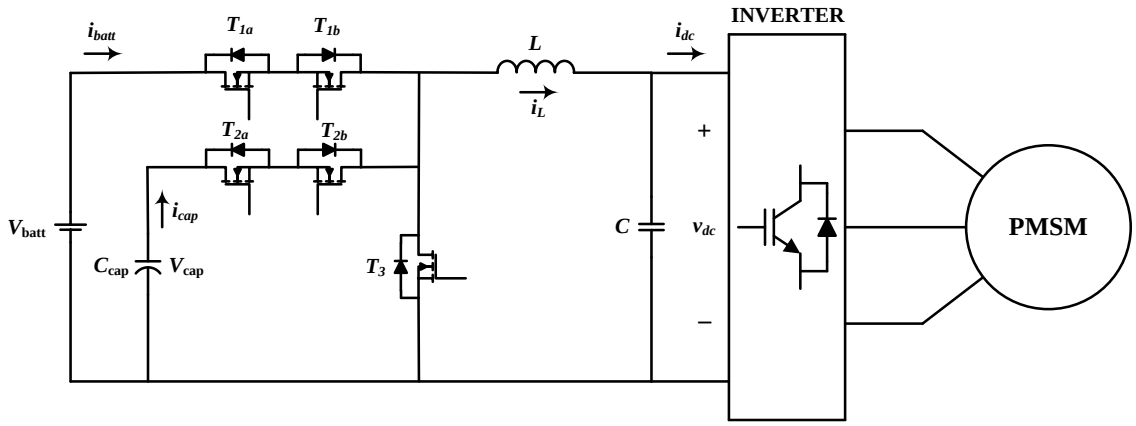


Figure 6.2. Circuit diagram of the bi-directional DI buck converter with a PMSM load.

This topology is bi-directional and for achieving the control objective the transistors are needed to be switched in a manner so that in the motoring mode the capacitor supplies the load whenever its voltage is greater than v_{dc} otherwise the load is supplied by the battery. When the motor is decelerating then the energy is stored in the capacitor. This is called the regenerative mode. The different modes of operation of the system are described below.

6.1.1. Mode I (Capacitor Discharging Mode). In this mode, the PMSM is running as a motor and the ultra-capacitor supplies the power to the motor till the voltage of the ultra-capacitor V_{cap} falls to dc link capacitor voltage v_{dc}. In this mode, transistors T_{1a}, T_{1b}, T_{2b}, and T_3 are OFF. The converter acts as a buck converter with a current mode controller used to generate switch command d_2 for transistor T_{2a} to regulate v_{dc} at the commanded voltage v_{dc}* (shown in Figure 6.3). When the capacitor discharges to the commanded dc link voltage, it will not be able maintain v_{dc} at the commanded value since the converter is acting as a buck converter. So the minimum voltage to which the ultra-capacitor is to be discharged is kept equal to or slightly greater than the commanded dc link voltage v_{dc}*.

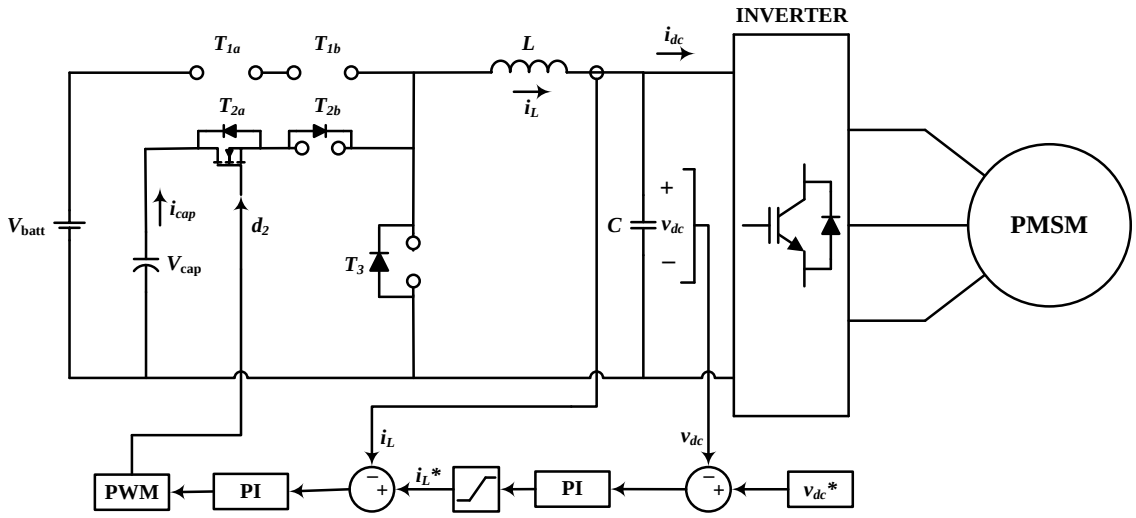


Figure 6.3. Circuit diagram for Mode I (capacitor discharging mode).

6.1.2. Mode II (Battery Only Mode). Once the ultra-capacitor is discharged and its voltage becomes minimum, the source is switched from the ultra-capacitor to the battery to supply the motor load. In this mode, transistors T_{1b}, T_{2a}, T_{2b} and T_3 are OFF (shown in Figure 6.4). The converter is operating as a buck converter and the current mode controller is used to generate switch command d_1 for transistor T_{1a} to maintain the dc link voltage at commanded value v_{dc}*.

6.1.3. Mode III (Regenerative Mode). In this mode the PMSM is decelerating and starts acting as a generator. The objective of this mode is to store the generated energy in the ultra-capacitor. In this mode, transistors T_{1a}, T_{1b}, and T_{2a} are OFF and switch T_{2b} is always ON and transistor T_3 is controlled by the current mode controller to maintain the dc link voltage v_{dc}. The PMSM acts as a source and the ultra-capacitor is the load and the converter operates as a boost converter charging the ultra-capacitor. Thus the bi-directional operation of DI buck converter is achieved.

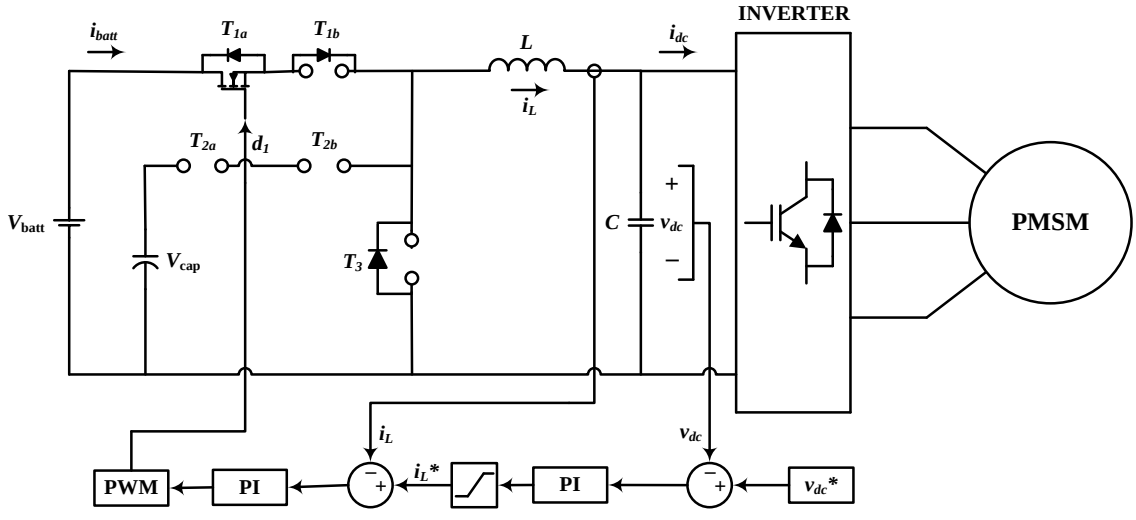


Figure 6.4. Circuit diagram for Mode II (battery only mode).

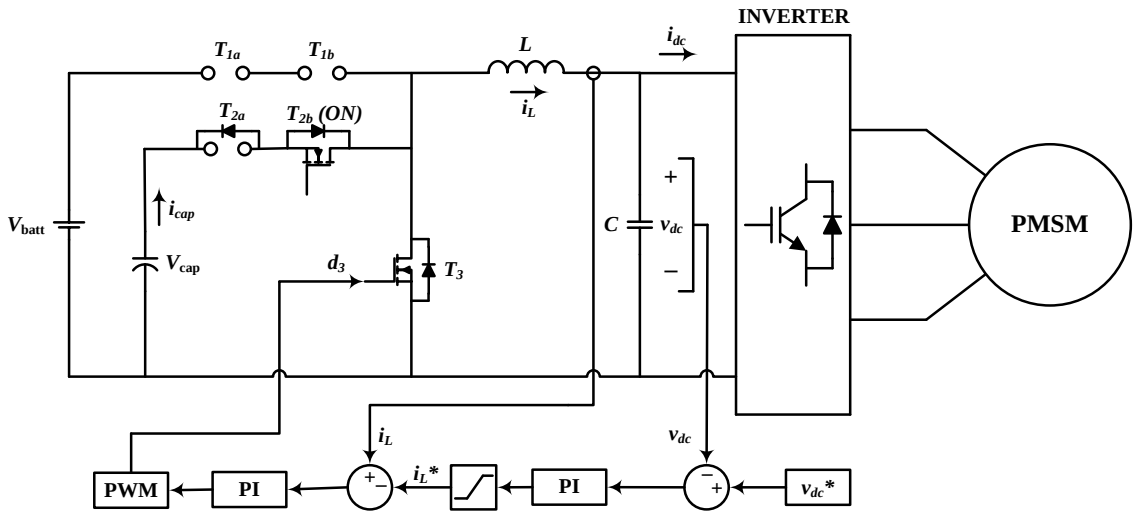


Figure 6.5. Circuit diagram for Mode III (regenerative mode).

6.2. SIMULATION RESULTS

The brushless DC drive with the hysteresis current regulation is implemented with an ideal battery source connected to a round rotor PMSM through an inverter (as shown in Figure 6.6). The PMSM has P = 4, r_s = 0.11 Ω, L_s = 0.25 mH, J = 0.38 kgm^2, B_m = 10^{-5} kgm^2/s and λ'_m = 1.3 Vs. The commanded torque T_e* is applied and the commanded currents i_{abc}* are generated by the torque control equations (6.1) to (6.3).

$$i_{qs}^{r*} = \frac{2}{3}\frac{2}{P}\frac{T_e^*}{\lambda'_m} \tag{6.1}$$

$$i_{ds}^{r*} = 0 \tag{6.2}$$

$$i_{abcs}^{*} = (K_s^r)^{-1} i_{qd0s}^{r*} \tag{6.3}$$

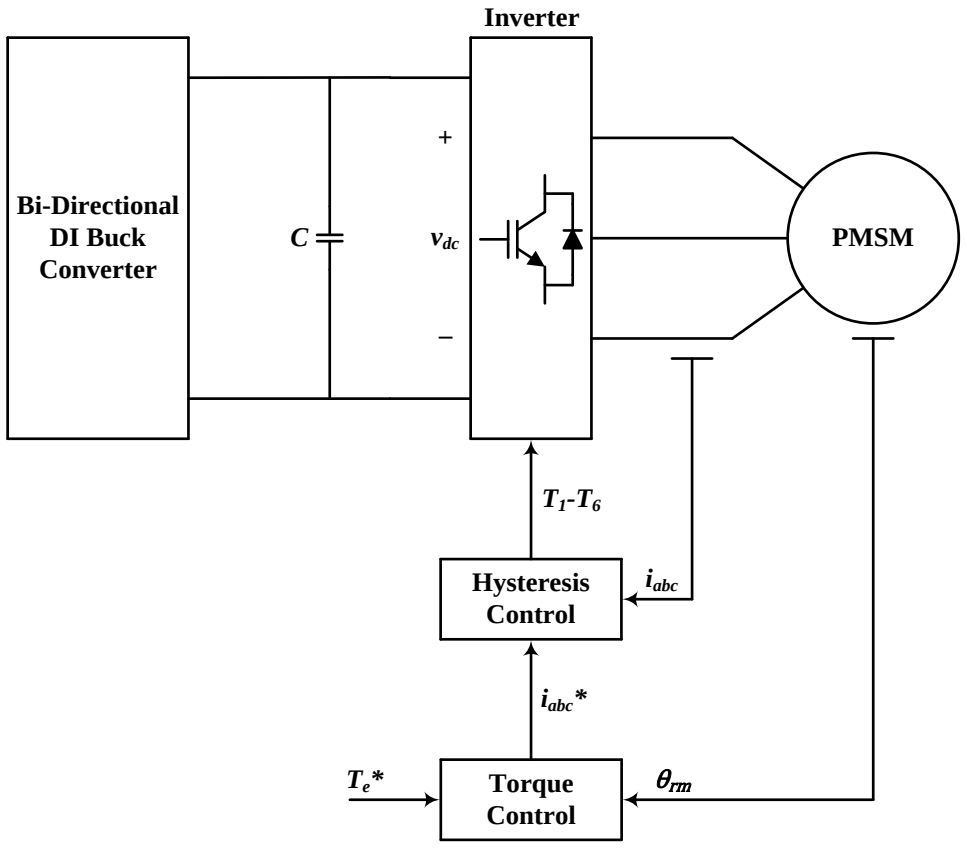


Figure 6.6. Brushless dc drive with hysteresis current regulation connected to bi-directional DI buck converter.

The bidirectional DI buck converter with the battery voltage V_{batt} = 600 V, capacitance of the ultra-capacitors is C_{cap} = 1 mF with initial voltage V_{cap} = 500 V, L = 20 mH and the dc link capacitor C = 10 mF is simulated with the PMSM load (as shown in Figure 6.2). The ultra-capacitor value has been chosen such that the capacitor charging and discharging can be observed. The hysteresis control is used with hysteresis limits h = ±1 A. The commanded torque T_e* is obtained from the PI controller of the speed control (as shown in Figure 6.7). In the simulation, the speed control gains are set to K_p = 5000 and K_i = 1000. The current mode control is employed to achieve better control of

inductor current. The PI controller used for generating the inductor reference current i_L* is $G_{vc}(s) = (20s+2)/s$ and the PI controller used for maintaining the inductor current to i_L* is $G_{ic}(s) = (s+0.1)/s$. The v_{dc}* is set to 300 V and the minimum voltage to which the ultra-capacitors are discharged to is set at 310 V. The simulated waveforms are shown in Figure 6.8.

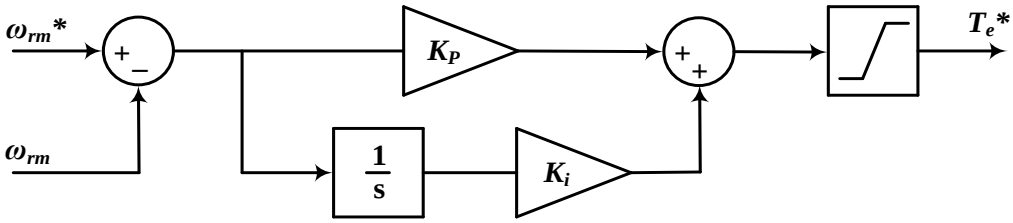


Figure 6.7. Commanded torque T_e* obtained from speed control.

At t = 0.005 s the commanded speed ω_{rm}* is increased and the machine runs in the motor mode. The speed is increased to 20 rad/s and a positive torque is commanded, it can be observed from Figure 6.8 that the ultra-capacitors are discharging. For this mode the i_{cap} and i_L are positive and V_{cap} reduces which shows that the power is flowing from the ultra-capacitors to the machine. V_{cap} reduces to 310 V and remains constant, at this time the machine is supplied only from the batteries. At t = 0.045 s, the commanded speed is reduced to zero which means the machine is decelerating and a negative torque is commanded, the machine is now operating in the regenerative mode and charges the ultra-capacitors. It can be seen from Figure 6.8 that V_{cap} is increasing and reaches 466.5 V. The ultra-capacitor voltage reached during the regenerative mode is less than the initial voltage of 500 V because there are some losses in the armature resistance and

windage losses. Also, the i_{cap} and i_L are negative during the regenerative mode which clearly indicate that power is flowing back to the ultra-capacitors.

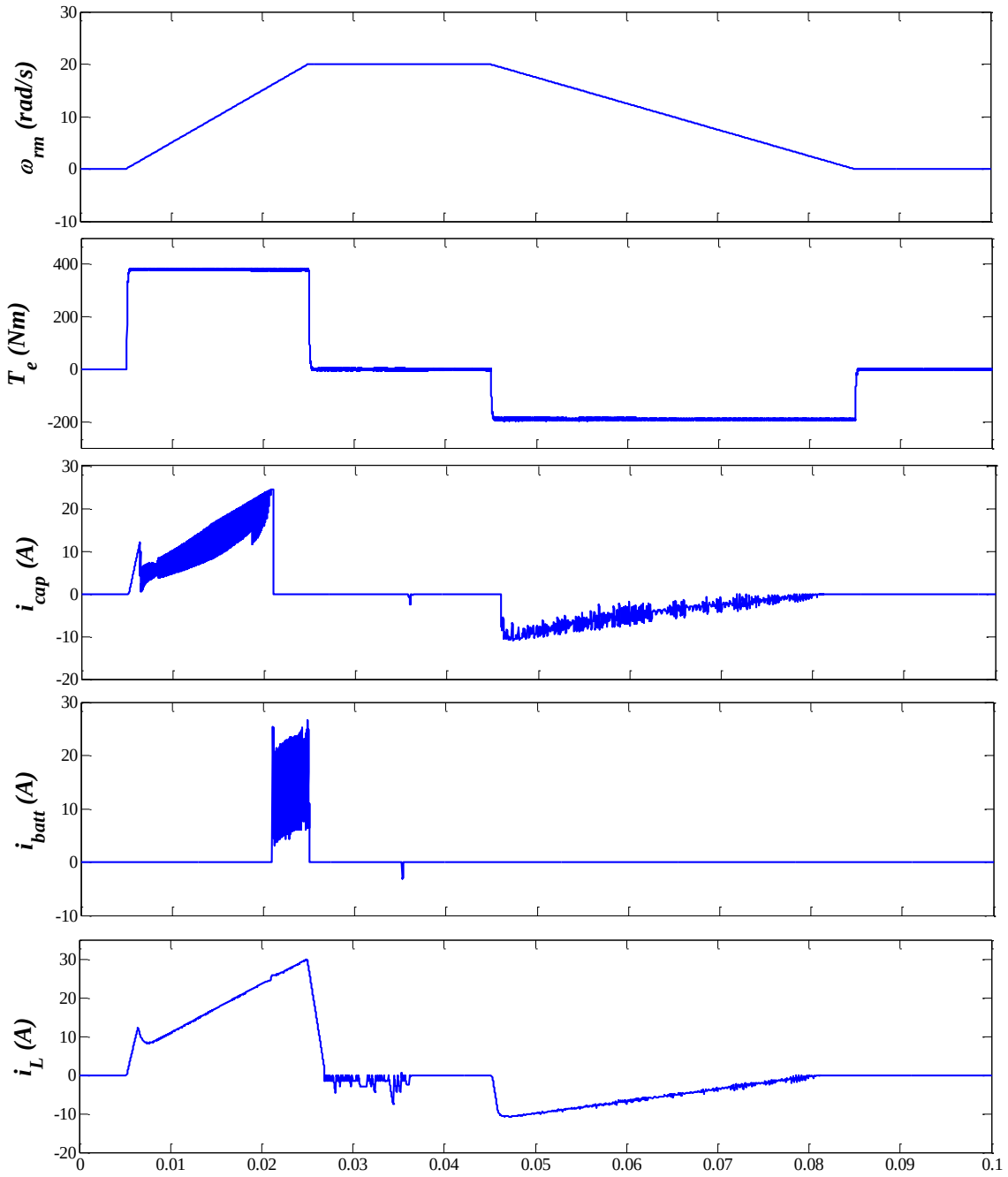


Figure 6.8. Simulated waveforms for bidirectional DI buck converter connected to PMSM load.

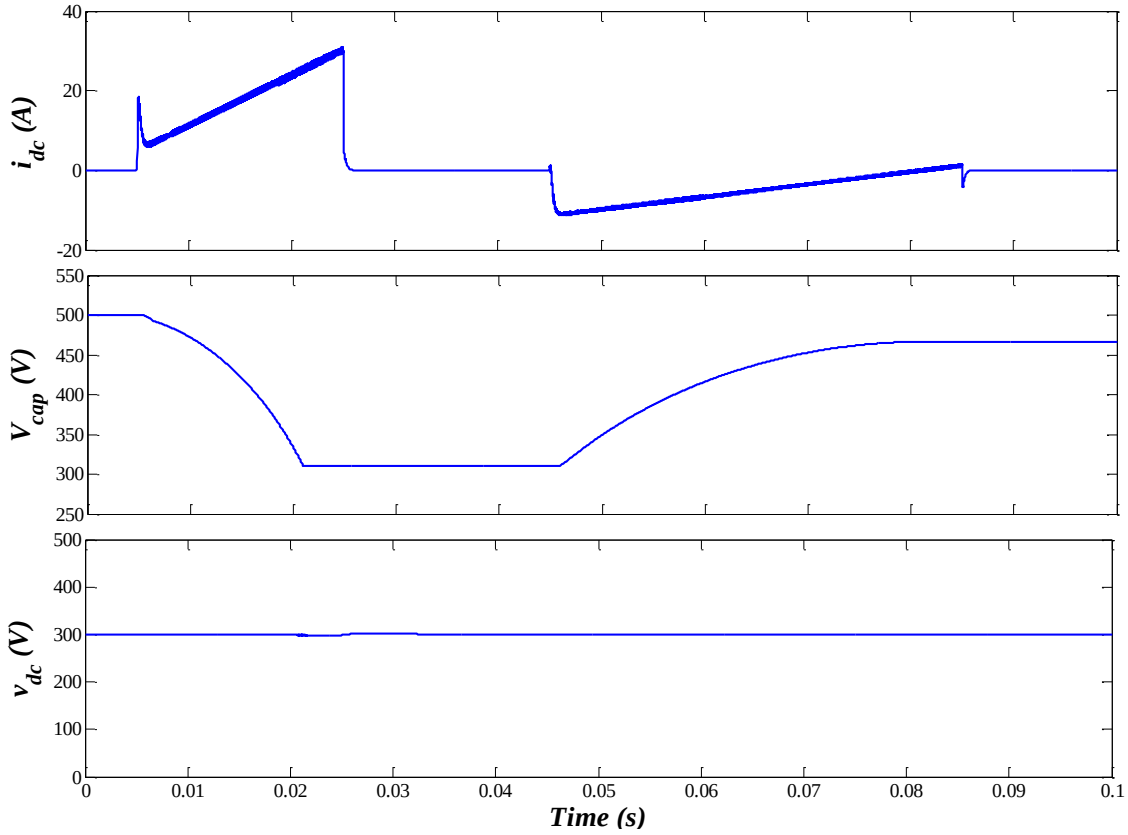


Figure 6.8. Simulated waveforms for bidirectional DI buck converter connected to PMSM load. (cont.)

In this section the bi-directional power flow in MIPECs and its potential applications in HEVs have been explored. The bi-directional DI buck converter has been simulated using battery/ultra-capacitor sources. During acceleration the power flows from the battery/ultra-capacitors to the machine and the ultra-capacitors are discharged and during regenerative braking they are again recharged.

7. DI BUCKBOOST CONVERTER FOR SOLAR APPLICATIONS

In this section, an application of multi-input converters for renewable energy sources is discussed. Renewable energy sources like wind, solar etc. are generally unreliable and intermittent and therefore need to be integrated with more reliable energy sources such as battery with multi-input converters. One such application is combining the PV (photovoltaic) array with the battery using a DI buckboost converter. It is required that the PV array delivers the maximum power, which may or may not cater for the load, and the remaining power is supplied by the battery or another reliable energy source.

7.1. PERTURB AND OBSERVE MAXIMUM POWER POINT TRACKING ALGORITHM

Figures 7.1 and 7.2 show the typical PV array characteristics. It can be observed that there is a nonlinear relationship between PV power and current as well as PV voltage and current. Therefore for getting the maximum power out of the PV array, maximum power point tracking (MPPT) techniques are utilized. The MPPT techniques make the system converge at a voltage (V_{MPP}) and current (I_{MPP}) such that the PV array supplies maximum power P_{MPP}. Many MPPT algorithms such as perturb and observe (P&O), incremental conductance, ripple correlation technique, fractional open-circuit voltage, fractional short-circuit current etc. have been developed to get maximum power out of the PV array [51]. The tracking techniques are selected based on the cost, complexity, speed of convergence, and implementation. Due to its simplicity and straightforward implementation, P&O method is used for this application [51].

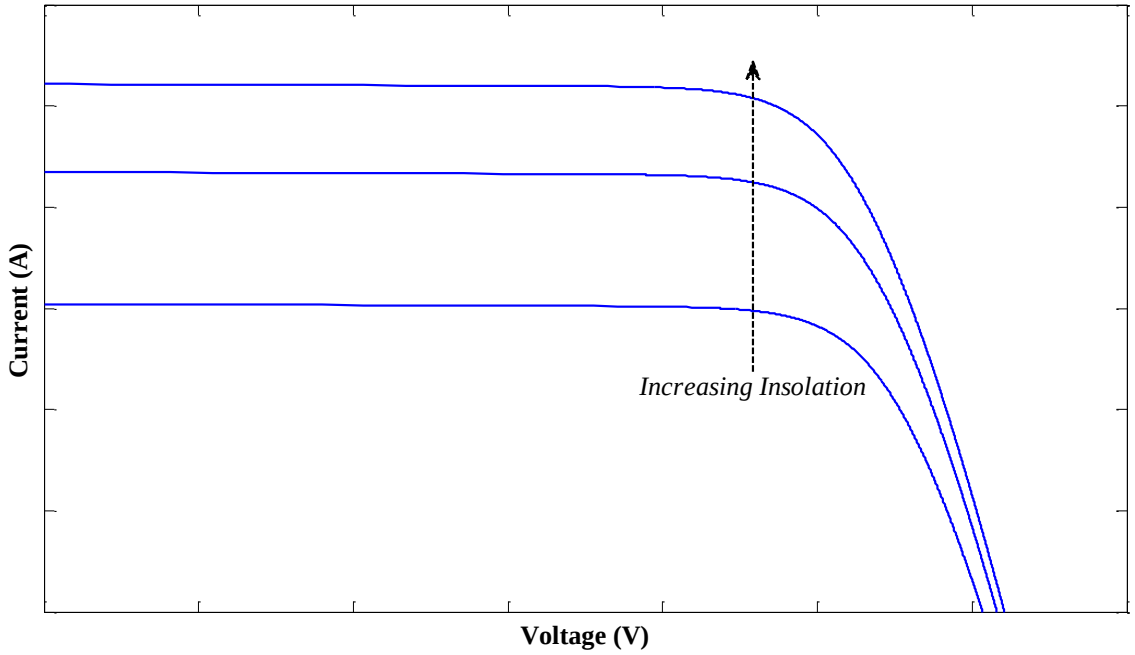


Figure 7.1. I-V characteristics of a PV array.

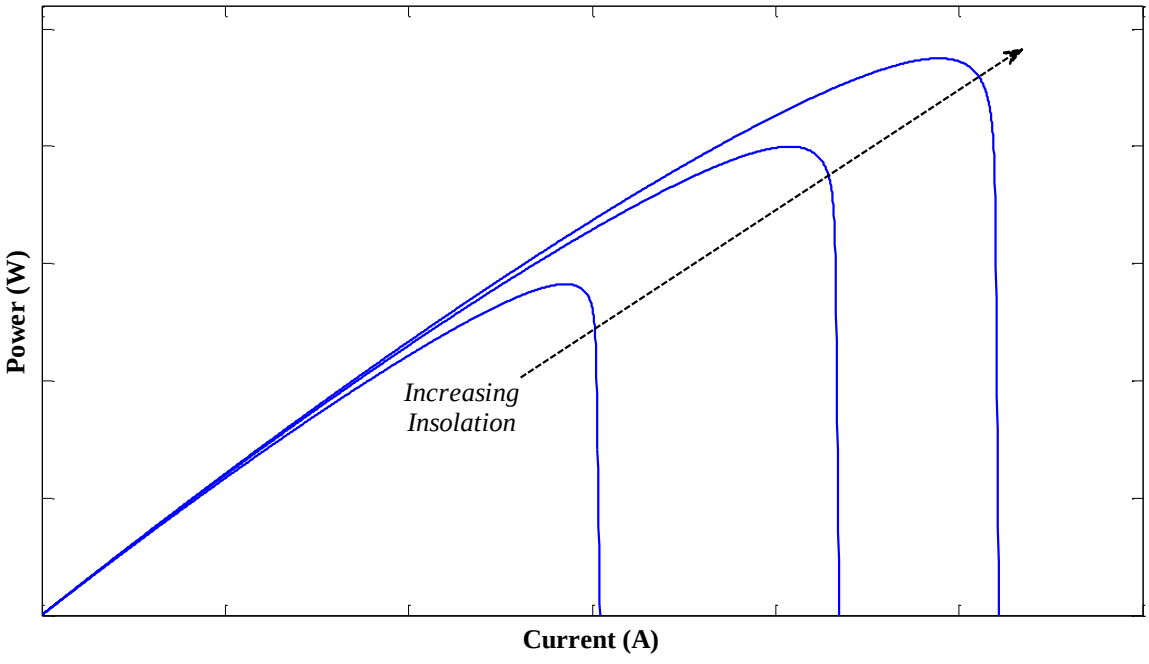


Figure 7.2. P-I characteristics of a PV array.

In the P&O MPPT algorithm (shown in Figure 7.3), PV current I_{PV} is perturbed by a step size of C and the PV voltage V_{PV} and output power P_{PV} is observed, if the power increases then incremental power ΔP_{PV} is positive or if the power decreases it is negative. If ΔP_{PV} is positive, current I_{PV} is increased in the same direction by setting the *inc* to 1 and incrementing I_{PV} by a constant step size of C. If incremental power ΔP_{PV} is negative then the direction of increment is reversed by setting the *inc* to -1, i.e., decreasing I_{PV} by C. The method is repeated until the MPP is reached.

The speed and accuracy of the algorithm depends on the step size of the increments, sampling frequency, and the points at which the V_{PV} and I_{PV} samples are taken. The main disadvantage of this method is that the system oscillates around the MPP. The oscillations can be reduced by setting a smaller step size but that would compromise the speed of the system. The other drawback of this method is that the system diverges from the MPP for sudden change in irradiance.

7.2. INTEGRATING PV ARRAY WITH DI BUCKBOOST CONVERTER

The P&O MPPT algorithm is implemented for a DI buckboost converter, as shown in Figure 7.4, with one of the sources as the PV array and the other source as the battery. samples are taken at the lower peak of the PV voltage and the upper peak of PV current with sampling time as t_s, as shown in Figure 7.5. In this case the MPPT algorithm does not converge to the actual maximum power point (MPP) and oscillates around point A with an offset from the actual MPP (as shown in Figure 7.6). The same is true when we take samples at the upper peak of voltage and lower peak of current. In both these cases

the algorithm converges at a point with an offset from the actual MPP and oscillates around point B as shown in Figure 7.6.

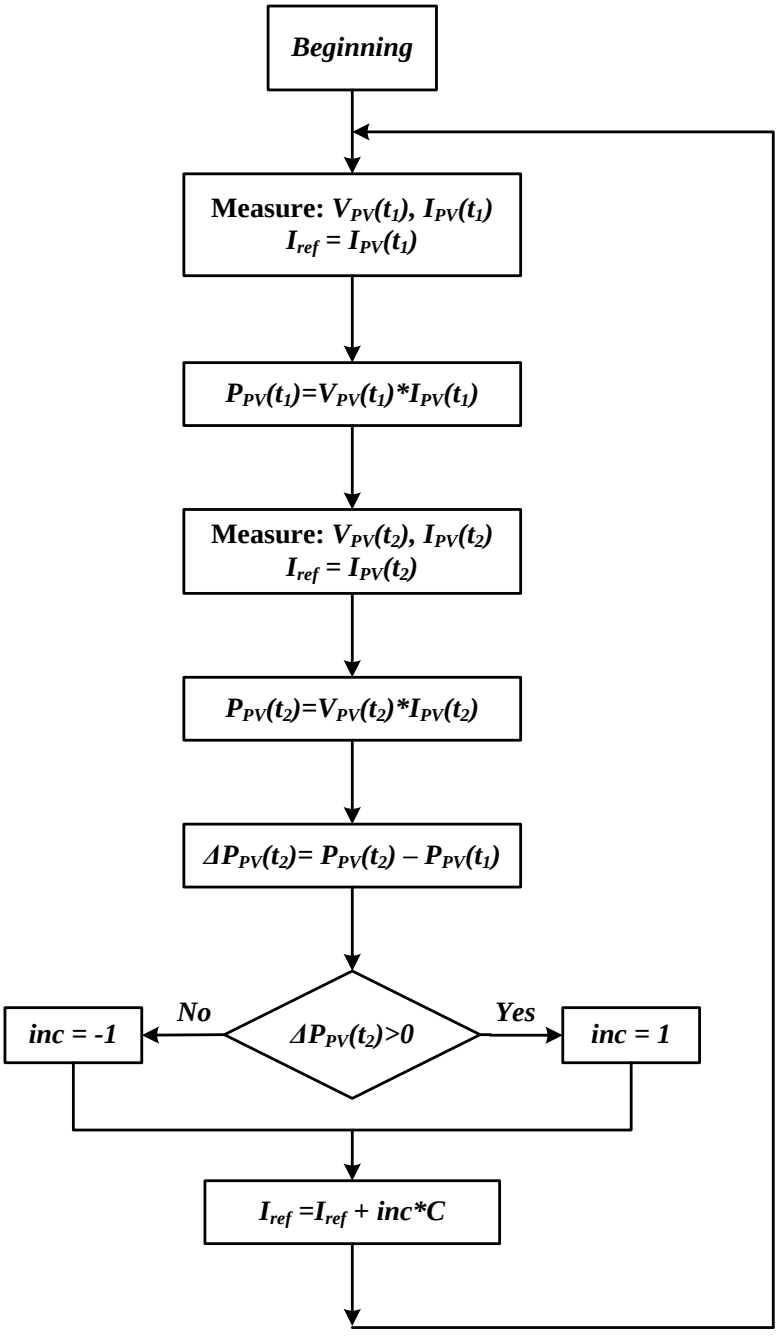


Figure 7.3. P&O (Perturb and Observe) MPPT algorithm.

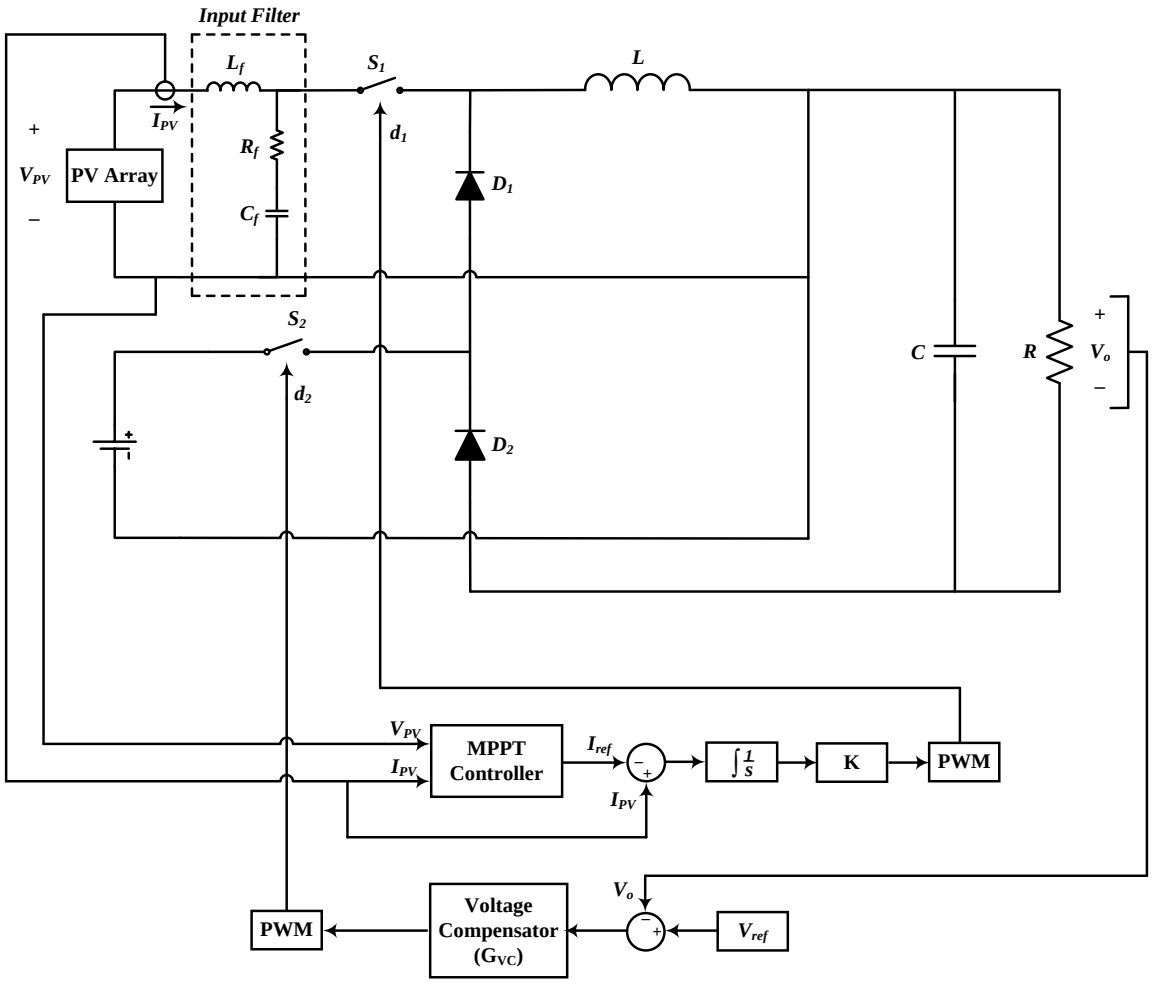


Figure 7.4. P&O MPPT algorithm implemented for a DI buckboost converter.

The input current of the DI buckboost converter is discontinuous, so to draw a continuous current out of the PV array, a low pass LC filter is introduced at the PV array source. To reduce the oscillations in the input current a damping resistor is inserted in series with the filtering capacitor.

The accuracy of the MPPT algorithm depends on the points at which the voltage and current samples are taken. Samples are taken at three different points. At first, the samples are taken at the lower peak of the PV voltage and the upper peak of PV current

with sampling time as t_s, as shown in Fig. 7.5. In this case the MPPT algorithm does not converge to the actual maximum power point (MPP) and oscillates around point A with an offset from the actual MPP (as shown in Fig. 7.6). The same is true when we take samples at the upper peak of voltage and lower peak of current. In both these cases the algorithm converges at a point with an offset from the actual MPP and oscillates around point B as shown in Fig. 7.6.

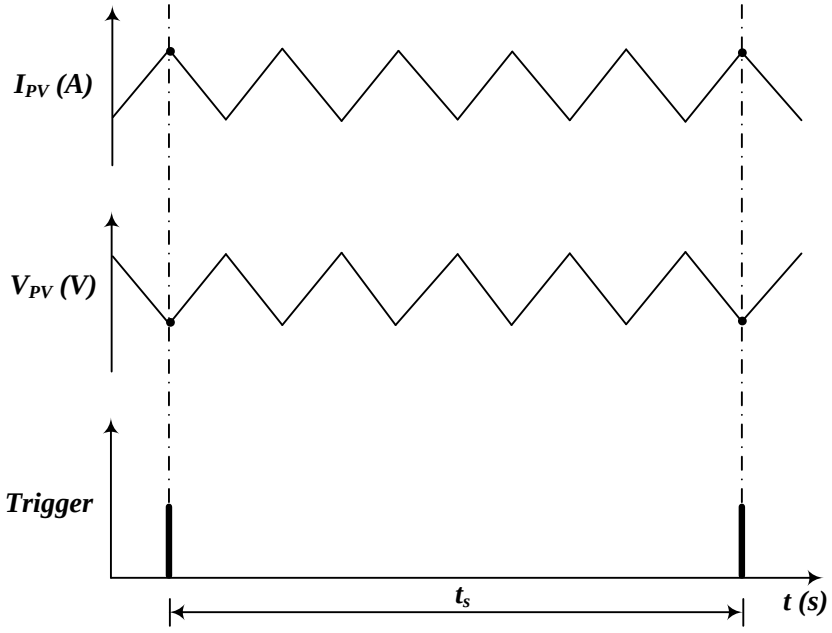


Figure 7.5. Samples taken at upper peak of I_{PV} and lower peak of V_{PV}.

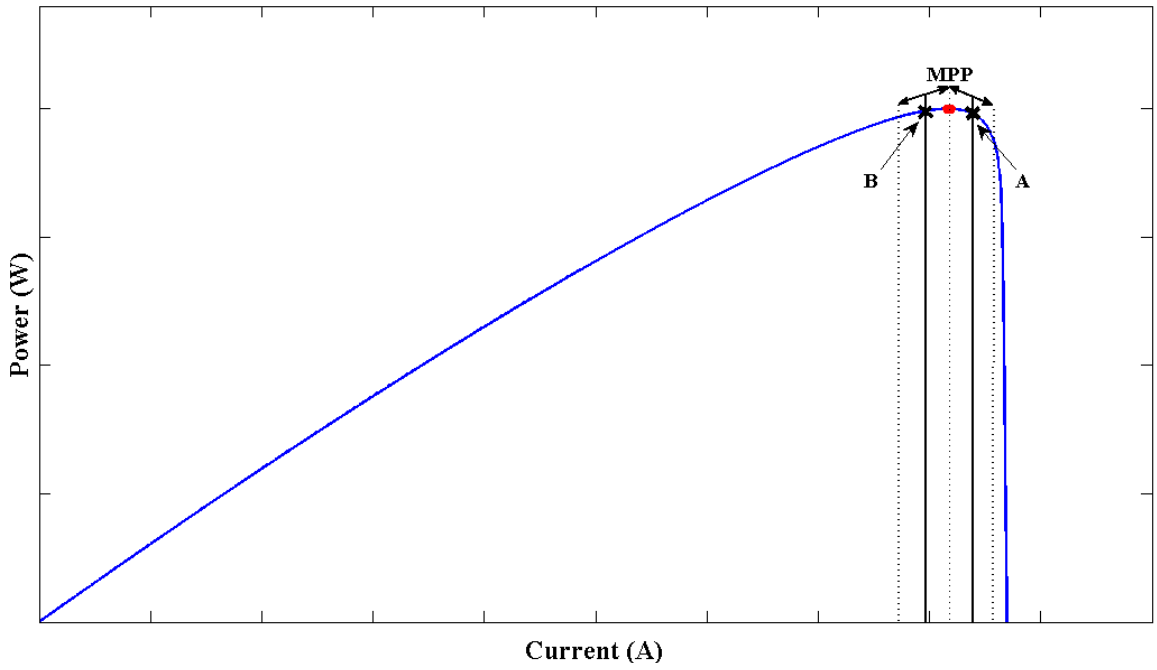


Figure 7.6. P&O MPPT algorithm oscillating around points A and B for samples of peak values of I_{PV} and V_{PV}.

Taking samples of the average values of voltage and current (as shown in Figure 7.7) ensures accurate tracking of the MPP. It can be observed from Figure 7.8 that the MPPT algorithm converges to the actual MPP and oscillates around it. The amplitude of the oscillation depends on the value of step size C by which the I_{ref} is increased or decreased.

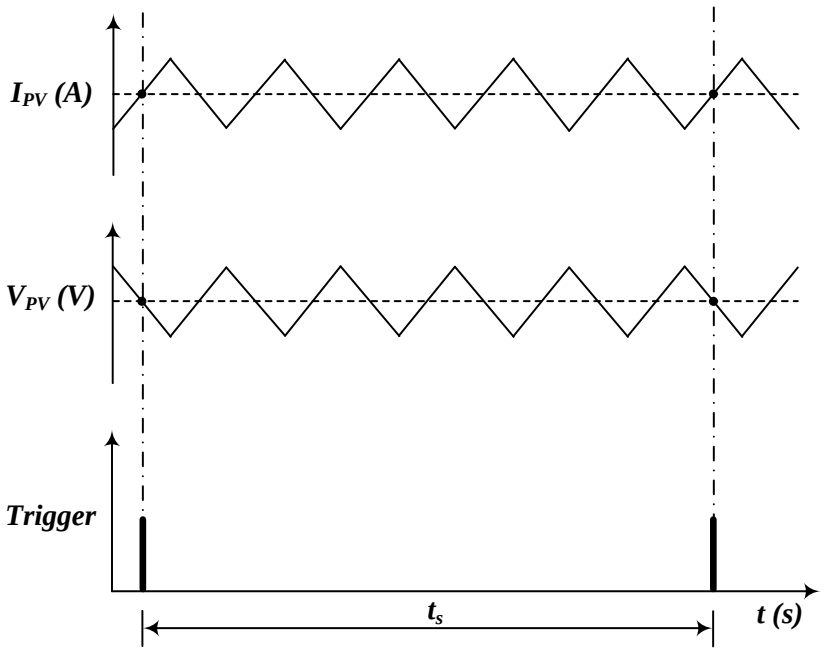


Figure 7.7. Samples taken at average values of I_{PV} and V_{PV}.

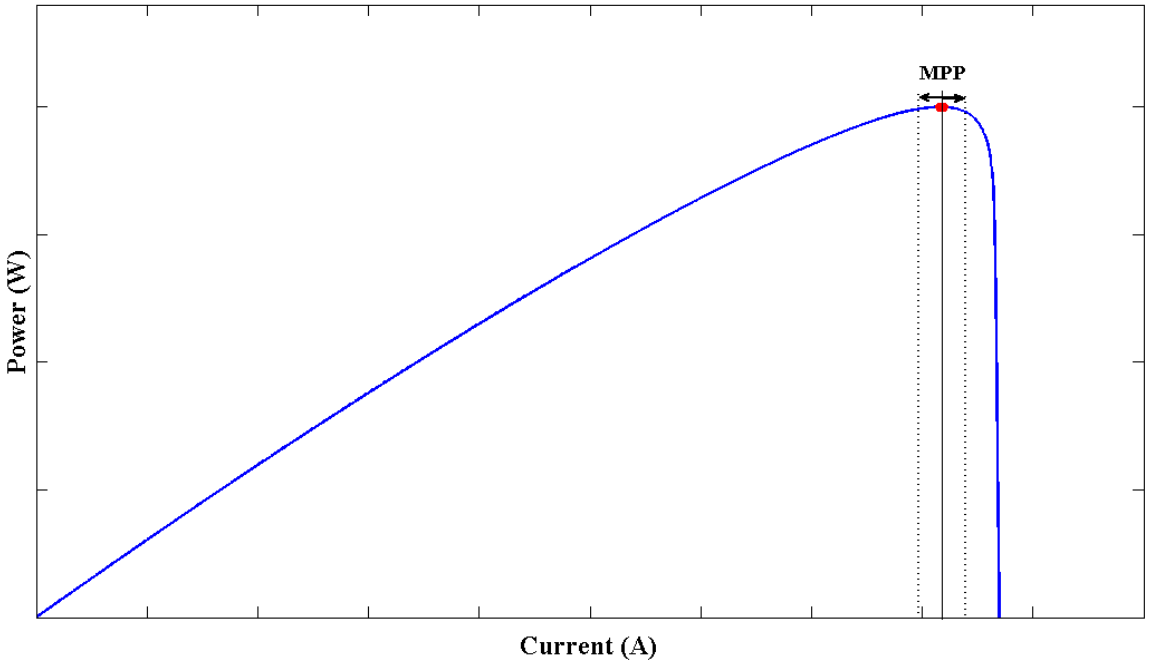


Figure 7.8. P&O MPPT algorithm oscillating around MPP for samples of average values of I_{PV} and V_{PV}.

7.3. SIMULATION RESULTS

The converter is simulated with first source V_1 as the PV array and the second source being a constant voltage source V_2 = 70 V, f = 50 kHz, L = 1 mH, C = 100 µF, R = 20 Ω, insolation is kept constant at 1000 W/m^2. The PV array [47] used for the simulation has an open circuit voltage of 30.8 V and short circuit current of 8.7 A. For an insolation of 1000 W/m^2 the maximum power supplied by the PV array is 200 W and the V_{MPP} is 24.5 V and I_{MPP} is 8.16 A. The input current of the DI buckboost converter is discontinuous; therefore the input filter is used (as shown in Figure 7.4) so that the PV array supplies continuous current. The damping resistor R_f is used to reduce the oscillations in the current. The input filter used in this simulation has L_f = 1 µH, C_f = 150 µF, R_f = 1 Ω.

The sampling frequency for taking the I_{PV} and V_{PV} samples for the MPPT algorithm is decided based on the settling time of the system for a step change in I_{ref}. The speed of the system also depends on the sampling frequency. It is important to choose the sampling time such that the dynamics of the system gets settled. Initially I_{ref} is set to 7 A and the integrator gain K = 1400 (see Figure 7.4), keeping duty ratio D_2 of the switch command S_2 constant at 0.4, the system is allowed to settle, after the system is settled I_{ref} is increased to 7.1 A at 0.03 s and the settling time is observed. It can be observed from Figure 7.9 that the system settles in approximately 2 ms, therefore, the sampling time t_s is set to 2 ms.

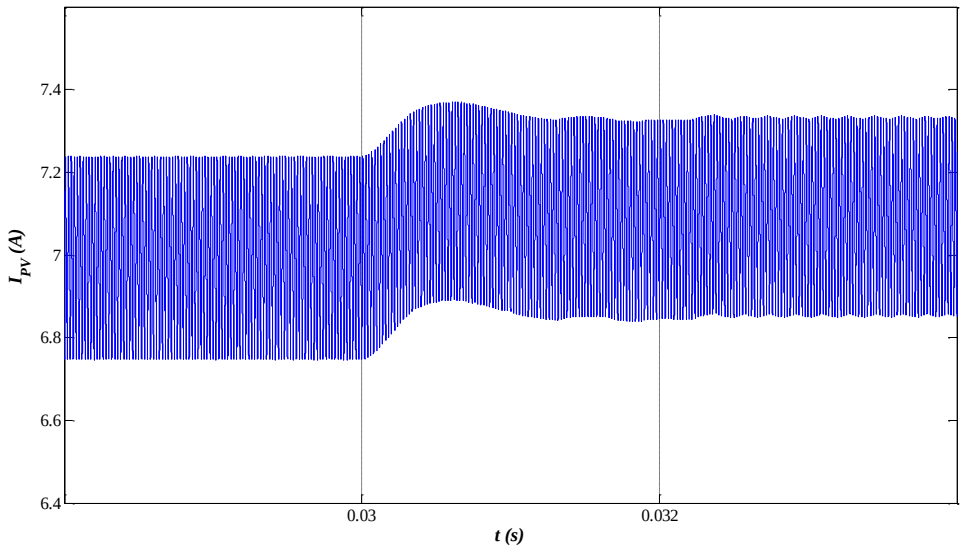


Figure 7.9. I_{ref} increased from 7 A to 7.1 A at 0.03 s.

The system is supposed to maintain a constant voltage across the load while drawing maximum power from the PV array. For this purpose, a voltage compensator is used to generate the switch command S_2. The system is simulated with G_{vc}(s) = (0.005s+1.3)/s (see Figure 7.4) and output voltage V_0 is kept constant at 150 V. The initial value of I_{PV} is set to 7.9 A and the step size C by which the I_{ref} is incremented is set to 0.1 A. Figure 7.10 shows the simulated waveforms for the system and it can be observed that the output voltage is held constant at 150 V while drawing maximum power of 200 W from the PV array for insolation of 1000 W/m^2. At t = 0.05 s, there is a step change in insolation from 1000 W/m^2 to 1100 W/m^2. It can be seen from Figure 7.10 that the PV array settles to the new MPP with I_{PV} and P_{PV} increasing to 8.8 A and 219 W, respectively, while the system voltage is regulated at 150 V. The insolation levels have been chosen to show the application of DI buckboost converter in solar energy systems and may not be a realistic estimation.

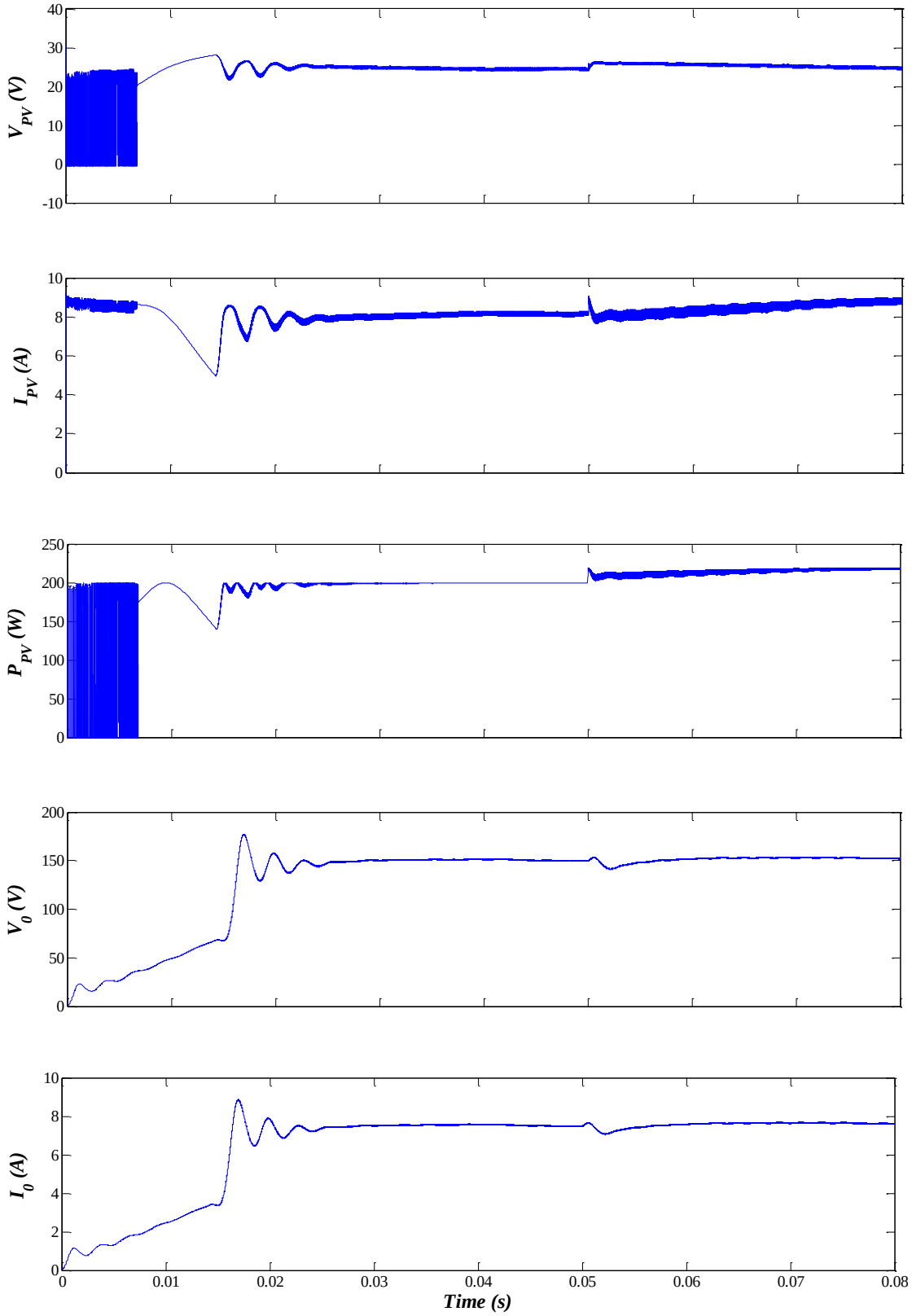


Figure 7.10. Simulated waveforms for the PV array integrated with DI buckboost converter.

MIPECs have been used to integrate PV array and battery, thus, making the system more reliable. Optimal utilization of the solar energy can be done by drawing the maximum available energy. Due to their non-linear characteristics, MPPT algorithms are used to extract maximum power out of the PV array. In this section, P&O MPPT algorithm has been used to explain the application of DI buckboost converter in a PV/battery hybrid energy system. In this system, maximum power is drawn from the PV array and the additional load is supplied from the battery, while keeping the output voltage constant.

8. CONCLUSION

In this thesis, the application and control aspects of various DIPEC topologies have been discussed. The application of MIPECs in solar energy systems have been demonstrated using the P&O MPPT algorithm. The utilization of bi-directional MIPECs in HEVs has also been shown. For any converter design, modeling of these converters is necessary for predicting the transient stability and for optimal controller design for stable closed loop operation. Small signal modeling is done for the DI buck converter and voltage and current compensators have been designed using these models. New control methods namely coupling control and dead-time control have been proposed for effective power sharing in DI buck converter. Small signal analysis of the coupling control method has been done to prove the superiority of the proposed method over conventional methods. In dead-time control, it has been shown that the dead-time between the switch commands directly affect the input currents. It has been proposed that in addition to controlling the switch commands, control of the dead-time as an additional variable can be done to achieve the control objective. It has been proven theoretically and by simulations that the proposed control methods have a better dynamic performance compared to conventional methods. Simulation results are in line with what has been predicted by the small signal models. Offset-time control method for power sharing in the DI buckboost converter has been experimentally verified. Results from the implementation show that effective power sharing is achieved by controlling the offset-time between the switch commands.

BIBLIOGRAPHY

[1] Huang, X., Wang, X., Nergaard, T., Lai, J.S., Xu, X., and Zhu, L., "Parasitic ringing and design issues of digitally controlled high power interleaved boost converters," in *IEEE Trans. Power Electron.*, vol. 19, pp. 1341–1352, Sep. 2004.

[2] Xu, H., Kong, L., and Wen, X., "Fuel cell power system and high power DC-DC converter," in *IEEE Trans. Power Electron.*, vol. 19, pp. 1250–1255, Sep. 2004.

[3] Liu, C., Johnson, A., and Lai, J.S., "Modeling and control of a novel six-leg three-phase high-power converter for low voltage fuel cell applications," Proc. *IEEE Power Electronics Specialists Conf. (PESC)*, Aachen, Germany, June 2004, pp. 4715–4721.

[4] Gopinath, R., Kim, S., Hahn, J.H., Enjeti, P.N., Yeary, M.B., and Howze, J.W., "Development of a low cost fuel cell inverter system with DSP control," *IEEE Trans. Power Electron.*, vol. 19, pp. 1256–1262, Sep. 2004.

[5] B. G. Dobbs and P. L. Chapman, "A multiple-input DC-DC converter topology," *IEEE Power Electronics Letters*, vol. 1, pp. 6–9, Mar. 2003.

[6] A. D. Napoli, F. Crescimbini, S. Rodo, and L. Solero, "Multiple input DC-DC power converter for fuel-cell powered hybrid vehicles," in Proc. *IEEE 33rd Power Electronics Specialists Conference (PESC'02)*, Cairns, Jun. 2002, pp. 1685–1690.

[7] L. Solero, A. Lidozzi, and J. A. Pomilio, "Design of multipleinput power converter for hybrid vehicles," in Proc. *IEEE Applied Power Electronics Conference and Exposition (APEC'04)*, Anaheim, California, Feb. 2004, pp. 1145–1151.

[8] L. Solero, F. Caricchi, F. Crescimbini, O. Honorati, and F. Mezzetti, "Performance of a 10 kW power electronic interface for combined wind/PV isolated generating systems," in Proc. *IEEE Power Electronics Specialists Conference (PESC'96)*, Jun. 1996, pp. 1027–1032.

[9] Y. M. Chen, Y. C. Liu, and F. Y. Wu, "Multi-input DC/DC converter based on the multiwinding transformer for renewable energy applications," *IEEE Trans. Ind. Appl.*, vol. 38, no. 4, pp. 1096–1104, Jul./Aug. 2002.

[10] M. Michon, J. L. Duarte, M. Hendrix, and M. G. Simoes, "A three-port bi-directional converter for hybrid fuel cell systems," in Proc. *IEEE Power Electronics Specialists Conference (PESC'04)*, Aachen, Germany, Jun. 2004, pp. 4736–4742.

[11] H. Matsuo, W. Lin, F. Kurokawa, T. Shigemizu, and N. Watanabe, "Characteristic of the multiple-input DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 625–631, Jun. 2004.

[12] J. L. Duarte, M. Hendrix, and M. G. Simoes, "Three-port bidirectional converter for hybrid fuel cell systems," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 480–487, Mar. 2007.

[13] M. Marchesoni and C. Vacca, "New DC-DC converter for energy storage system interfacing in fuel cell hybrid electric vehicles," in *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 301–308, Jan. 2007.

[14] K. Gummi, "Derivation of new double-input dc-dc converters using Building Block Methodology," *M. S. Thesis, University of Missouri-Rolla*, Dec. 2006.

[15] K. Gummi and M. Ferdowsi, "Synthesis of double-input dc-dc converters using single pole triple throw switch as a building block," in *Proc. IEEE Power Electronics Specialists Conf. (PESC)*, Greece, Jun. 2008.

[16] K. Gummi and M. Ferdowsi, "Derivation of new double-input converters using H-Bridge cells as Building Blocks," in Proc. *IEEE Industrial Electronics Conf.*, Orlando, FL, USA, Nov. 2008.

[17] B. Ozpineci, L. M. Tolbert, D. Zhong, "Multiple input converters for fuel cells," in Proc .*IEEE Industry Applications Conference*, vol. 2, pp. 791-797, Oct. 2004.

[18] R. U. Haque, M. T. Iqbal, J. E. Quaicoe, "Sizing, Dynamic Modeling and Power Electronics of a Hybrid Energy System," in *IEEE Canadian Conference on Electrical and Computer Engineering*, Ottawa, May 2006, pp. 1135-1138.

[19] A. D. Napoli, F. Crescimbini, F. G. Capponi, L. Solero, "Control strategy for multiple input DC-DC power converters devoted to hybrid vehicle propulsion systems," in *IEEE Industrial Electronics International Symposium*, vol. 3, pp. 1036-1041, May 2002.

[20] L. Solero, A. Lidozzi, J. A. Pomilio, "Design of multiple-input power converter for hybrid vehicles," in *IEEE Trans. on Power Electronics*, vol. 20, pp. 1007-1016, Sep. 2005.

[21] A. Lidozzi, L. Solero, "Power balance control of multiple-input DC-DC power converter for hybrid vehicles," in *IEEE Industrial Electronics International Symposium*, 2004, vol. 2, pp. 1467-1472.

[22] M. Amirabadi, S. Farhangi, "Fuzzy Control of a Hybrid Power Source for Fuel Cell Electric Vehicle using Regenerative Braking Ultracapacitor," in *IEEE International Power Electronics and Motion Control Conference*, 2006, pp. 1389-1394.

[23] M. B. Camara, H. Gualous, F. Gustin, A. Berthon, "Control strategy of Hybrid sources for Transport applications using super capacitors and batteries," in Proc. *IEEE Power Electronics and Motion Control Conf.*, 2006, vol. 1, pp. 1-5.

[24] H. Tao, A. Kotsopoulos, J. L. Duarte, M. A. M. Hendrix, "Family of multi-port bidirectional DC-DC converters," in *IEEE Proc. on Electric Power Applications*, vol. 153, pp. 451-458.

[25] K. P. Yalamanchili, M. Ferdowsi, and K. Corzine, "New double input dc-dc converter for automotive applications", in Proc. *IEEE Vehicle Power and Propulsion Conf.*, 6-8 Sept. 2006, pp 1-6.

[26] K. P. Yalamanchili and M. Ferdowsi, "Review of multiple input DCDC converters for electric and hybrid vehicles," in Proc. *IEEE Vehicle Power and Propulsion Conf.*, 7-9 Sept. 2005, pp. 160-163.

[27] A. Khaligh, J. Ciao and Y. J. Lee, "A Multiple-input dc-dc converter topology," *IEEE Power Electronic Letters*, vol. 24, pp. 862-868, Mar 2009.

[28] S. H. Choung and A. Kwasinki, "Multi-input dc-dc converter topologies comparison," in Proc. *IEEE Industrial Electronics Conf.(IECON)*, Nov. 2008, pp. 2359-2364.

[29] Caricchi, F., Crescimbini, F., Napoli, A.D., Honorati, O., Santini, E., "Testing of a new DC/DC converter topology for integrated wind-photovoltaic generating systems," in Proc. *IEEE Power Electronics and Applications*, vol. 8, pp. 83–88, Sep. 1993.

[30] Matsuo, H., Kobayashi, K., Sekine, Y., Asano, M., Lin Wenzhong, "Novel solar cell power supply system using the multiple-input DC-DC converter," in Proc *IEEE Telecommunications Energy Conf. (INTELEC)*, pp. 797–802, Oct. 1998.

[31] Chen, Y. M., Liu, Y. C., Hung, S. C., Cheng, C.S., "Multi-Input inverter for grid-connected hybrid PV/wind power system," in *IEEE Trans. On Power Electronics*, vol. 22, pp. 1070-1077, May 2007.

[32] Yaow-Ming Chen, Yuan-Chuan, Liu, "Development of multi-port converters for hybrid wind-photovoltaic power system," in Proc. *IEEE Electrical and Electronic Tech. International Conf. (TENCON)*, 2001, vol. 2, pp. 804-808.

[33] Vazquez, Nimrod, Hernandez, Alvaro, Hernandez, Claudia, Rodriguez, Elias, Orosco, Rodolfo, Arau, Jaime, "A double input DC/DC converter for photovoltaic/wind systems," in *Proc. IEEE Power Electronics Specialists Conf. (PESC)*, 15-19 June 2008, pp. 2460-2464.

[34] Crescimbini, F., Carricchi, F., Solero, L., Chalmers, B.J., Spooner, E., Wu Wei, "Electrical equipment for a combined wind/PV isolated generating system," in Proc. *IEEE Opportunities and Advances in International Electric Power Generation, International Conference*, pp. 59-64, 18-20 Mar. 1996.

[35] Das, D., Esmaili, R., Xu, L., Nichols, D., "An optimal design of a grid connected hybrid wind/photovoltaic/fuel cell system for distributed energy production," in Proc. *IEEE Industrial Electronics Society (IECON)*, 6-10 Nov. 2005.

[36] Benavides, N.D., Esram, T., Chapman, P.L., "Ripple correlation control of a multiple-input DC-DC converter," in Proc. *IEEE Power Electronics Specialists Conf.(PESC)*, 2005, pp. 160-164.

[37] Stienecker, A.W., Stuart, T., Ashtiani, C., "A combined ultracapacitor-lead acid battery storage system for mild hybrid electric vehicles," in Proc. *IEEE Vehicle Power and Propulsion Conf. (VPPC)*, 7-9 Sep. 2005.

[38] Carpaneto, M., Ferrando, G., Marchesoni, M., Vacca, C., "The average switch model of a new double-input DC/DC boost converter for hybrid fuel-cell vehicles," in Proc. *IEEE International Symposium on Industrial Electronics (ISIE)*, vol. 2, pp. 601-607, Jun. 2005.

[39] Di Napoli, A., Crescimbini, F., Solero, L., Caricchi, F., Capponi, F.G., "Multiple-input DC-DC power converter for power-flow management in hybrid vehicles," in Proc. *IEEE Industry Applications Conference (IAS)*, vol. 3, pp. 1578-1585, Oct. 2002.

[40] Marchesoni, M., Vacca, C., "A new DC-DC converter structure for power flow management in fuel-cell electric vehicles with energy storage systems," in Proc. *IEEE Power Electronics Specialists Conf. (PESC)*, vol. 1, pp. 683-689, June 2004.

[41] Yongxiang Chen,, Davoudi, Ali, Chapman, Patrick L., "Multifrequency modeling of a multiple-input DC-DC converter," in Proc. *IEEE Power Electronics Specialists Conf. (PESC)*, pp. 4604-4610, June 2008.

[42] Davoudi, A., Jatskevich, J., Chapman, P.L., "Parametric average-value modeling of multiple-input buck converters," in Proc. *IEEE Canadian Conf. on Electrical and Computer Engineering (CCECE)*, 22-26 Apr. 2007, pp. 990-993.

[43] Somayajula, D., Ferdowsi, M., "Small-signal modeling and analysis of the double-input buckboost converter," in Proc. *IEEE Applied Power Electronics Conf. and Exposition (APEC)*, 2010, pp. 2111-2115.

[44] J. Rajagopalan, K. Xing, Y. Guo, F. C. Lee and B. Manners, "Modeling and dynamic analysis of paralleled dc/dc converters with master-slave current sharing control," in *Proc. IEEE Applied Power Electronics Conf. (APEC)*, Mar. 1996, pp. 678-684.

[45] D. Somayajula and M. Ferdowsi, "Power sharing in a double-input buckboost converter using offset time control," in *Proc. IEEE Applied Power Electronics Conf.* (APEC), Feb. 2009, pp. 1091-1096.

[46] http://dataweek.co.za/news.aspx?pklNewsId=31635&pklCategoryID=46 Loop compensation of voltage-mode boost converters (last accessed on May 15, 2010).

[47] http://ecee.colorado.edu/~ecen2060/energyprogram.html (last accessed on May 10, 2010).

[48] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, M. A. Kluwer, 2001.

[49] J. G. Kassakian, M. F. Schlecht, and G. C. Verghese, *Principles of Power Electronics*, 2nd ed, Addison Wesley, 1991.

[50] N. D. Benavides and P. L. Chapman, "Power budgeting of a multiple-input buck-boost converter," *IEEE Trans. Power Electronics,* vol. 20, pp. 1303-1309, Nov. 2005.

[51] Esram, T.; Chapman, P.L., "Comparison of Photovoltaic Array Maximum Power Point Tracking Techniques," *IEEE Trans. Energy Conversion*, 2007, vol. 2, pp. 439-449.

[52] Y. M. Chen, Y. C. Liu, and S. H. Lin, "Double-input pwm DC/DC converter for high/low-voltage sources," *IEEE Trans. Industrial Electronics,* vol. 53, pp. 1538-1545, Oct. 2006.

[53] Prabhala, V.A.K.; Somayajula, D.; Ferdowsi, M., "Power sharing in a double-input buck converter using dead-time control," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, 2009, pp. 2621 – 2626.

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