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Printed circuit board (PCB) loss characterization up-to 20 GHz and modeling, analysis and validation

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PRINTED CIRCUIT BOARD (PCB) LOSS CHARACTERIZATION UP-TO 20 GHz

AND

MODELING, ANALYSIS AND VALIDATION

by

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ABSTRACT

Dielectric properties and losses are increasingly more important in signal link path characterization, as data rates increases. High-frequency effects such as dielectric losses, dispersion and skin-effect losses need to be considered. For ensuring signal integrity, it is important to characterize losses of printed circuit board (PCB) dielectrics. To extract dielectric properties of a stripline transmission medium, an analytical technique was used as described in [1]. Two test materials were studied, and the extraction procedure was refined. This technique was applied to microstrip transmission lines. Two analytical solutions were derived for extracting practical material parameters. A microstrip test vehicle was designed and the two extraction methods were applied to a set of test boards. A standard measurement protocol was developed. Results were analyzed and documented.

An approach to characterize losses in printed circuit board (PCB) materials as a single value was studied. It was analytically proven that the theory was meaningful. Time-domain and frequency-domain techniques were developed to characterize the single value loss parameter. Measurements were taken with stripline test vehicles. Results validated the method to be a potential standard for characterizing losses.

Several tools are available in the market for design and discovery related to signal integrity issues. Some of these tools were considered to model two simple validation problems. Propagation of a plane wave through a dielectric slab was analyzed with two different tools and results were also validated using calculations. A simple PCB was modeled with decoupling capacitors using several tools to see the effects of decoupling on impedance.

ACKNOWLEDGMENTS

I express my deep and sincere gratitude to Dr. James L. Drewniak for his constant guidance and mentoring throughout the pursuit of my Master's degree. I thank Dr. Pommerenke for his support and enlightening discussions. I thank all my fellow students of the UMR EMC laboratory who I have been working with during these years. I also want to thank the committee members of my thesis defense, and I'm grateful for the financial support of research assistantship from the UMR EMC Laboratory. Finally, I would like to thank my family and dedicate this work to them, for their unconditional love, support, and encouragement throughout my education and life.

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1. INTRODUCTION

Digital systems require signals to be transmitted from drivers to receivers. Signal propagates through several discontinuities like connectors, transitions, lossy transmission lines etc. along its path to the receiver. These discontinuities degrade the signal quality and may even distort the original signal. So, the receiver may miss a bit if it does not fall on a certain threshold level. Noise could also couple into the system from external sources and degrade the signal. Some problems of this sort are solved using parity checking. But, they are not practical in terms of cost and performance. Data rates are going higher in modern digital systems and the requirement to achieve sufficient signal integrity is increasing. Sufficient power integrity should also be maintained for proper functioning of the device.

1.1. PCB MATERIAL PARAMETER EXTRACTION

Signals propagating in modern digital systems are getting progressively faster. Traces on printed circuit boards which transmit signals from source to destination no longer behave as simple conductors. As the data rates are going higher, these conductors exhibit high frequency effects and have to be considered as transmission lines. Hence, it becomes necessary to deal with high frequency effects such as skin effect loss, dielectric loss, as well as dispersion. It is not just the conductor which exhibits loss, but as frequency goes higher the dielectric used between the conductors also play an important role. The timing issues relating to transmission lines are also becoming important in today's high speed digital designs. Hence, it becomes important to characterize the materials for efficient signal integrity analysis.

Conventional single valued representation of dielectric constant and loss tangent are becoming invalid because they are dependant on frequency. Several simulation tools take in the material properties as a single valued number. But, as frequencies go as high as 20 GHz, single valued representation no longer holds true. So, frequency dependent models for dielectric constant and loss tangent are necessary to represent the actual properties of the material. Several techniques are available in the literature to extract material parameters. Cavity resonance method, two-line measurement method, etc are different techniques used to extract material properties from raw measurements. A method for extracting dielectric constant and loss tangent as a function of frequency was proposed [1] using TRL calibrated S-parameters for stripline structures. Two methods for extracting material parameters for a microstrip structure are presented in this thesis. This section of thesis starts off with analyzing two stripline structures and then recreates the measurement procedure suggested by J. Ziang [1]. Measurements and results are also discussed. A Microstrip test board with TRL calibration patterns was designed. Test boards made of 32 different materials were measured, analyzed and extracted for material study.

1.2. ROOT IMPULSE ENERGY (RIE) LOSS

A method for characterizing loss in time and frequency domain is presented in this section. Several methods are available to extract losses in terms of frequency [2-6]. But, it will be very useful to have a single valued number to specify losses in terms of limits. Also, several frequency domain techniques could be used to characterize losses since losses are functions of frequency. It would also be useful to have a time domain

technique to characterize losses so that measurements could be made using simple, less costly instruments like TDR. This section of the thesis provides a novel technique to characterize losses in time domain. Frequency domain characterization based on the same concept is also done to validate time domain method.

RIE loss is a single valued energy loss used to represent losses in a transmission line. A step signal is injected into a transmission line and energy is lost when the signal propagates through the transmission line. Characteristics of losses in a transmission line can be determined by comparing RIE of the injected wave to the RIE of the received wave. For avoiding the effects of losses due to cables, connectors and transitions, a calibration trace is also used to deal with unwanted energy loss. The received step signal is converted into an impulse response to encompass the widest possible frequency range. Then the area under the impulse response is integrated over time to get the energy associated with each trace. The ratio of energies of test trace to calibration trace gives the RIE loss. Measurements are results are also analyzed in this section.

1.3. ANALYSIS, MODELING AND VALIDATION

Several tools are available in the market for analyzing and modeling signal integrity issues. This section deals with modeling two common geometries and validating the results with different tools. The first section considers the propagation delay through a dielectric slab. The velocity through a medium is inversely proportional to the square root of the permeability of the material. So, as the permeability goes higher, velocity decreases. An electromagnetic wave takes longer to pass through a medium with higher permeability. This time delay and the reflections from the boundaries are calculated in

this section of the thesis. This geometry is then modeled in different tools to validate the results.

Design of dc power distribution networks (PDN) on a printed circuit board (PCB) plays a vital role in maintaining power integrity. Several techniques are available to ensure that the PDN provides necessary charge to the devices in the PCB [14-17]. Yet, the design presents an increasingly difficult challenge for digital circuits with active devices. The sizes of the circuits are getting smaller with more devices added to the same board. This makes the power consumption levels go high. More devices are switching and they are getting current starved. For the proper functioning of the devices, it is necessary to have sufficient charge when it is required. As switching speeds go higher, a simple PDN might not be enough to supply enough charge for the devices. PDN have to be designed carefully with sufficient decoupling capacitors to provide the charge in a timely manner. The study of PDN design with emphasis on the value of the decoupling capacitors used was analyzed in one among a series of papers on PDN design strategies [14]. The location of the decoupling capacitors was analyzed in the second paper [15]. The third paper deals with importance of the planes and the choice of material parameters [16]. Fourth, among the series of papers studies the sources of PDN noise [17].

The study presented on this thesis is analyzing the location and value of capacitors on a PDN design. Several values of capacitors were used on different locations to see its effect on the impedance. Increasing decoupling capacitors on the board decreases the impedance. Reducing the PDN impedance would allow current to flow freely into the IC device when needed. Several cases were modeled using three different signal integrity analysis tools. Validation of the results is also presented in this section.

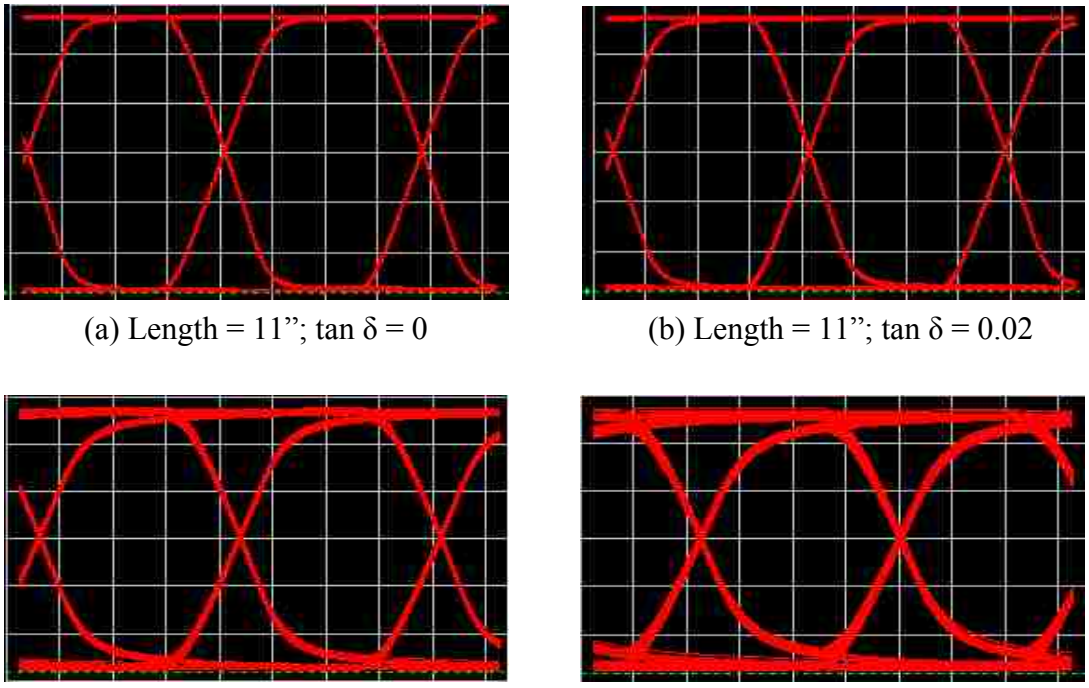
2. PRINTED CIRCUIT BOARD (PCB) MATERIAL PARAMETER EXTRACTION UP TO 20 GHz

The correct estimation of material properties is very critical when dealing with signal link path characterization. As data rate increases, it is important to consider high frequency effects such as skin effect and dielectric losses, as well as dispersion. For such cases, dielectric constant and loss tangent become functions of frequency. These losses could significantly degrade the signal quality and close the eye in an eye diagram. Furthermore, losses increase as the length of the transmission line increases, and these losses degrade the rise time. The effects of losses and length on an eye diagram generated in Hyperlynx, is shown in Figure 2.1. An eye pattern was generated using PRBS data, which was passed through a stripline transmission line. This line was terminated with matched load impedance.

Figure 2.1(a) shows the eye diagram, when there are no losses on 11" stripline transmission line. A prefect eye is obtained in this case because there are no other discontinuities considered here except losses. The line is terminated with a matched impedance so there are no reflections either. Figure 2.1(b) is almost similar to Figure 2.1(a) because only loss tangent was increased to 0.02. But, the effects of losses are very clear in Figure 2.1(c) and Figure 2.1(d). The rise time is degraded as the losses become significant and the eye is starts to close. This will generate jitter which is undesirable for applications with high data rates. The eye opening becomes much narrower for a 20" long line which is shown in Figure 2.1(d).

So, it becomes important to characterize material properties of printed circuit boards (PCBs) to do an effective signal integrity analysis. Several methods for extracting

material properties are reported in the literature [1-6]. Each has its own advantage depending on the material or the band of frequencies.



(a) Length = 11”; tan δ = 0

(b) Length = 11”; tan δ = 0.02

(c) Length = 11”; tan δ = 0.2

(c) Length = 20”; tan δ = 0.2

Figure 2.1. Channel performance degradation in several cases due to length dependent losses in transmission lines.

A resonant cavity technique is available for single or narrow band frequencies, which provides dielectric parameters at higher frequencies with good accuracy [2]. A coaxial technique is also available but the material has to be in powder form and it is hard to use de-embedding techniques, which becomes critical at higher frequencies [4]. Direct measurements can be done using impedance analyzer to obtain dielectric constant and loss tangent, though it is limited to lower frequencies [6]. A method for the extraction of

material parameters such as dielectric constant and loss tangent as a function of frequency based on measured S-parameters is also available [1], and is of interest to the study in this Section. In this method [1], a stripline geometry was considered and measurements were made only on a single FR-4 material.

There are several FR-4 materials available in the market from different vendors and suppliers. They differ based on their resin content and different methodologies are adopted by vendors to extract material properties. So, it becomes difficult for a board designer to choose which material to use, and from where. Knowledge of the material properties from a set of materials available in the market could help a designer choose between materials for specific applications. Some high speed applications with long traces require the use of low loss materials, and there are some applications where sufficient loss is required for the proper functioning of devices. For example, for reducing the power plane impedance for power integrity issues, increasing dielectric loss can be beneficial. This Section deals with generating a parameter matrix of different materials from different vendors using an S-parameter measurement technique [1]. To validate the technique, two new materials of stripline construction were studied in the first section of this Section and the procedure was refined. stripline structures were measured using SMA connectors. This proved troublesome for high frequency measurements. Therefore, a new, simple, two-layer microstrip test board was designed. The absence of additional via stubs in the microstrip geometry also proved beneficial in designing a new microstrip test board for the material study. This also facilitated the use of high precision microprobes to reduce high-frequency imperfections. The work flow adopted for this Section is shown in Figure 2.2.

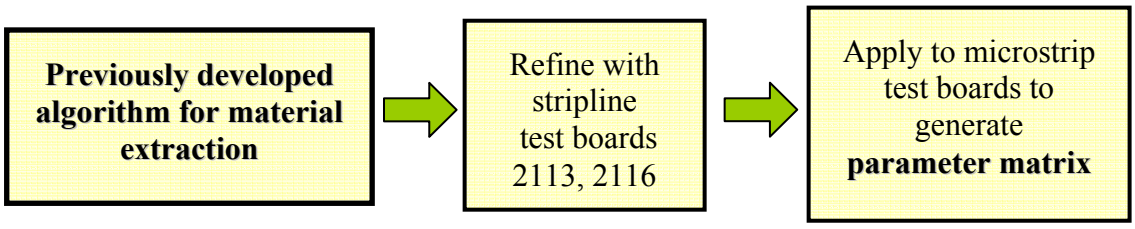


Figure 2.2. General flow diagram for generating a new material parameter matrix.

The previously developed S-parameter extraction technique needed modification, since for microstrip geometry, TEM wave propagation can no longer be assumed. This is because of the presence of both air and the dielectric material as the propagation medium. A quasi-TEM model [7] has to be used, which combines both dielectric mediums as a single effective medium. Hence, only effective values of material properties could be obtained from the normal extraction procedure. The algorithm was modified to obtain practical values of material parameters. Two algorithms are presented in this Section for extracting material parameters from a microstrip geometry. Both adopt the same procedure as for stripline [1], but differ in the method of approximating conductor losses. The general procedure explained in [1] is as shown in Figure 2.3. The S-parameters of the test board is required to calculate the material properties of the material. It is important to exclude the effects of discontinuities from the measurement equipment to the test trace for accurate extraction of material properties. The propagation constant is extracted from the measured S-parameters. Conductor losses and dielectric losses are separated from the propagation constant. A good estimation of the material properties could be obtained from the phase constant and dielectric loss. Frequency dependant values of dielectric

constant and loss tangent are obtained in this way. This work flow was used for the extraction of material parameters from the designed microstrip test vehicles.

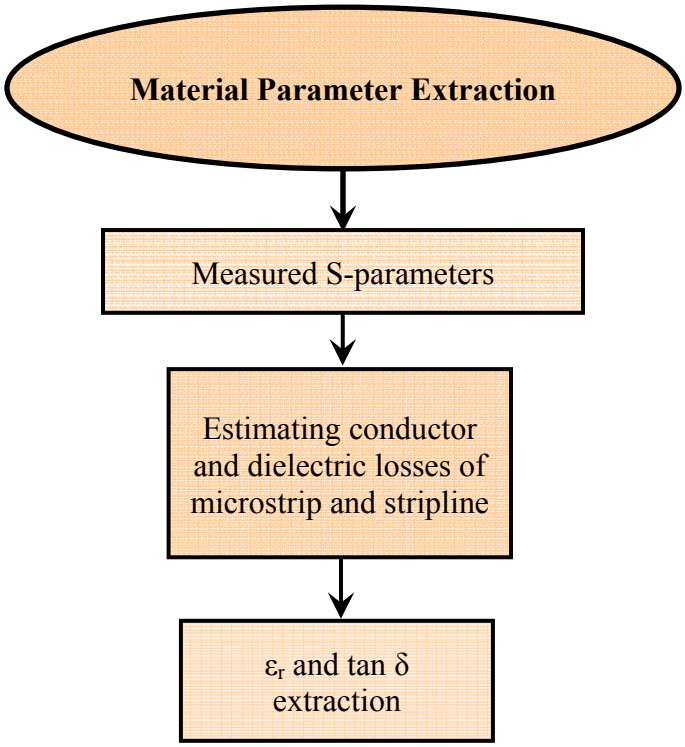


Figure 2.3. General procedure for extracting material parameters.

2.1. EXTRACTION OF MATERIAL PARAMETERS FROM STRIPLINE

Previously developed S-parameter algorithm for material extraction is revisited in this section. Geometry is defined and traces were selected for measurements. S-parameter and TDR measurements are taken. Data is analyzed and material properties are extracted.

2.1.1. Description of Geometry. A perspective view of a 7-layer board under test is shown in Figure 2.4. The board consists of stripline structures that are connected

through SMA connectors. The board has three distinct sections of lines arranged in three different orientations: vertical, horizontal and 10^{o} rotated from horizontal. The 10^{o} trace, facilitate the study of the effects of orientation of fiber in the material, on losses. The layout of a single section is shown in Figure 2.5. Only single-ended traces of different lengths, marked in colors as shown in Figure 2.5 are used for this study. Differential traces present in this board were not used for this study. The stack up and dimensions of a single-ended trace on the board is shown in Figure 2.6. Thru-Reflect-Line (TRL) calibration patterns were designed in each base structure to take care of the effects of cables, vias, connectors, etc. in the launch [7]. They are ST, SO, SL1, SL1, SL2 and SL3 which are marked in colors on Figure 2.5. There are two additional test traces ST1 and ST2 having the same length on the board, which are only used for test purposes.

Figure 2.4. Perspective view of the stripline test board.

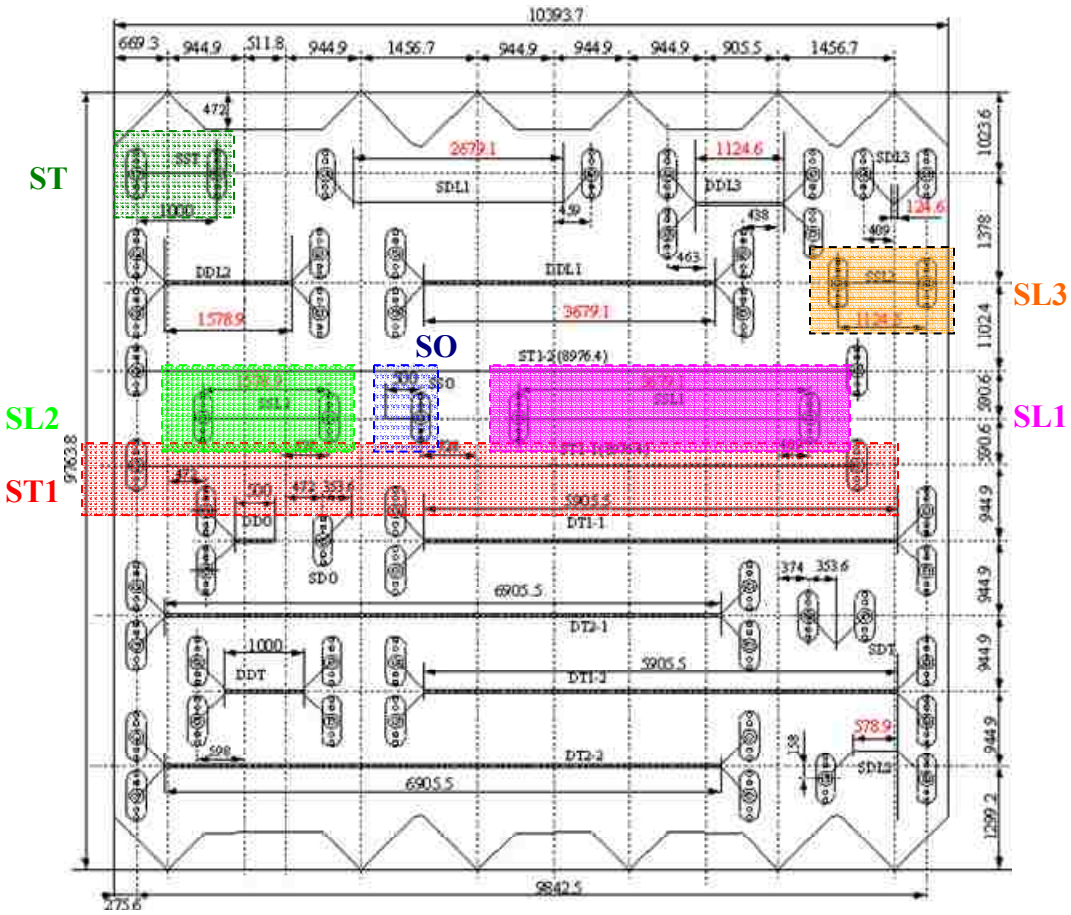


Figure 2.5. Layout of a base structure with TRL cal patterns and test traces (all dimensions are in mils).

Traces are considered as ideal rectangular cross sections, but they are not in real practice due to process variations. But, considering these effects are beyond of the scope of this thesis. The dimensions shown in Figure 2.6 are used for extraction algorithms.

2.1.2. Material Extraction Procedure for Stripline. The extraction procedure for stripline geometry has been previously developed [1]. The material properties are extracted from TRL calibrated, measured S-parameters. The measured S-parameters are converted to ABCD parameters. The complex propagation constant can be calculated from the measured 'ABCD' parameters as

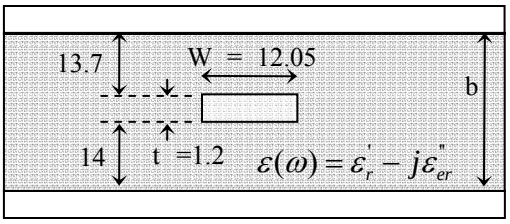


Figure 2.6. Stack up of a single stripline structure (all dimensions are in mils).

$$\gamma = \frac{\cosh^{-1}(A)}{L}. \tag{2.1}$$

where 'L' is the length of the trace under test, and 'γ' is the propagation constant. The real part of propagation constant is the total attenuation loss, and the imaginary part is the phase constant. The total attenuation loss is given in (2.3).

$$\gamma = \alpha + j\beta. \tag{2.2}$$

$$\alpha = \alpha_c + \alpha_d. \tag{2.3}$$

where 'α' is the total attenuation loss, 'β' is the phase constant, 'α_c' is the conductor loss and 'α_d' is the dielectric loss. Conductor loss is a function of geometry and can be approximated as [7]

$$\alpha_c = \begin{cases} \dfrac{2.7\times10^{-3} R_s \varepsilon_r^{'} Z_c}{30\pi(b-t)} A & for\ \sqrt{\varepsilon_r^{'} Z_c} \le 120. \\ \dfrac{0.16 R_s}{Z_c b} B & for\ \sqrt{\varepsilon_r^{'} Z_c} \succ 120. \end{cases} \tag{2.4}$$

$$A = 1 + \frac{2W}{b-t} + \frac{b+t}{\pi(b-t)} \ln\left(\frac{2b-t}{t}\right). \tag{2.5}$$

$$B = 1 + \frac{b}{0.5W + 0.7t} + \left(0.5 + \frac{0.414t}{W} + \frac{1}{2\pi} \ln\left(\frac{4\pi W}{t}\right)\right). \tag{2.6}$$

where ε_r' is the real part of permittivity, 'Z_c' is the characteristic impedance of the line, 'W' is the width of the trace, 'b' is the thickness of the dielectric medium, 't' is the thickness of the trace, which could be observed in Figure 2.6. Surface resistance, 'R_s' is given by

$$R_s = \sqrt{\frac{\omega\mu}{2\sigma}}. \tag{2.7}$$

where 'μ' is the permeability and 'σ' is the conductivity of the stripline conductor material. Then, from the measured S-parameters total loss can be extracted. Conductor loss can be approximated using (2.4). Therefore, dielectric loss can be calculated as

$$\alpha_d = \alpha - \alpha_c. \tag{2.8}$$

The real and imaginary part of permittivity is related to the phase constant and dielectric loss as

$$\varepsilon' = \frac{c^2}{\omega^2}\left(\beta^2 - \alpha_d^2\right). \tag{2.9}$$

$$\varepsilon'' = \frac{c^2}{\omega^2}\left(2\alpha_d\beta\right). \tag{2.10}$$

$$\varepsilon(\omega) = \varepsilon' - j\varepsilon''. \tag{2.11}$$

The loss tangent is defined as

$$\tan\delta(\omega) = \frac{\varepsilon''}{\varepsilon'}. \tag{2.12}$$

The material extraction procedure explained above is shown in detail on Figure 2.7. The corresponding geometry is also shown in Figure 2.7, for the calculation of conductor loss.

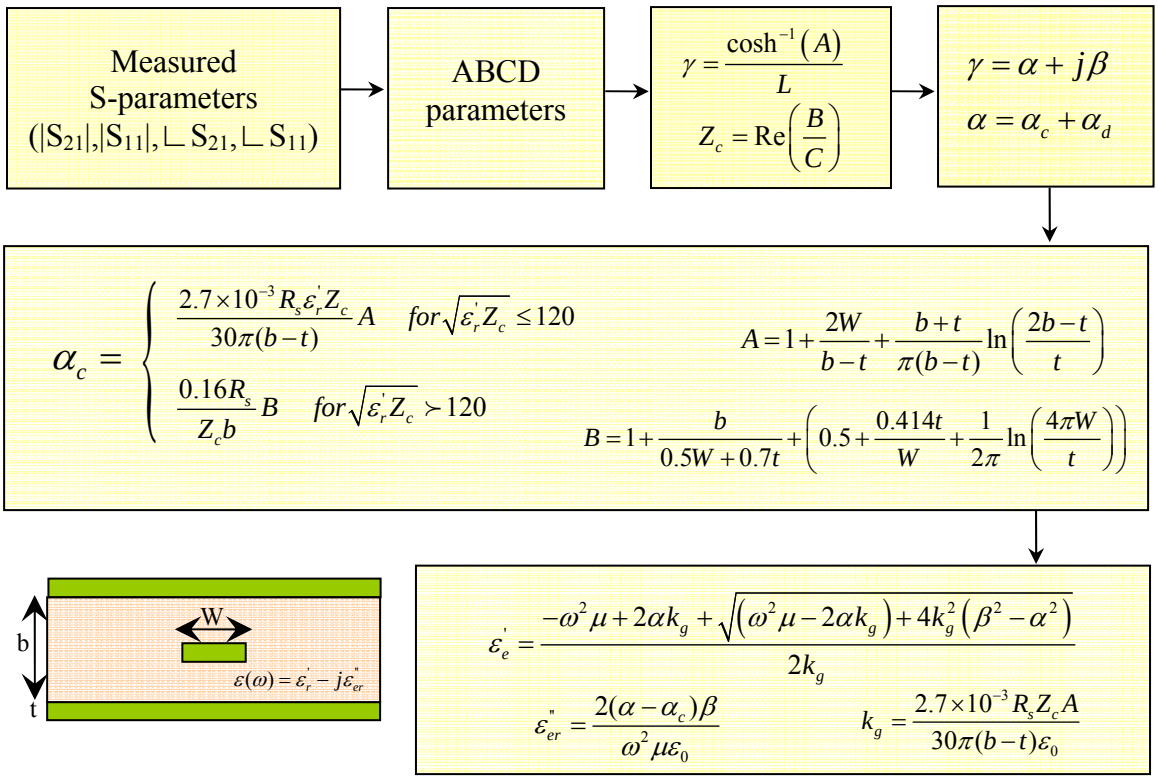


Figure 2.7. Material extraction procedure for stripline.

2.1.3. Test Setup, Calibration and Measurements. Calibration used for this study was TRL calibration for accurate extraction of material properties. In the measurement of S-parameters, for the purpose of extracting material parameters, non-ideal effects such as cable losses, via effects, connector losses should not be included. The best way to exclude those effects is using a TRL calibration. The design of calibration patterns depends on the frequency range of interest. For this study, the frequency range of interest was 200 MHz – 20 GHz. The frequency range was split into three separate ranges for effective TRL calibration [7]. They were 200 MHz – 930 MHz, 930 MHz to 4.3 GHz and 4.3 GHz to 20 GHz. The designed TRL calibration patterns

lengths are shown in Table 2.1. The purpose and procedure for designing TRL calibration patterns for microstrip is explained later in Section 2.2.4.

Table 2.1. TRL calibration lengths and other trace lengths for patterns on the PCB.

ST (mils)	SO (mils)	SL1 (mils)	SL2 (mils)	SL3 (mils)	ST1(mils)	ST2(mils)
1000	500	3679.1	1578.9	1124.6	8976.4	8976.4

S-parameter measurements need to be taken for the test boards under consideration. Two test boards with different dielectric material were studied. The dielectric materials used in the board construction varied based on their resin content. They were named Board 2113 and Board 2116. The stripline traces were extended outside using SMA connectors for measuring S-parameters. The purpose of this measurement is to extract dielectric constant and loss tangent as a function of frequency. The boards have three different orientations of a base structure as shown in Figure 2.4.

The test setup involves an HP8270D network analyzer, high-precision microwave cables, and test boards. Molex, press fit connectors were used to connect to the stripline. Torque wrench was used as a part of measurement protocol to tighten the screws. This helped to make sure that the same pressure is provided to the connectors each time the connection was made. This is very important while considering TRL calibration. Figure 2.8 shows a typical measurement setup. High-precision microwave cables are used to reduce the losses that accrue due to the cable itself. TRL calibration assumes that both ports are identical so it is also important that the cables have identical characteristics.

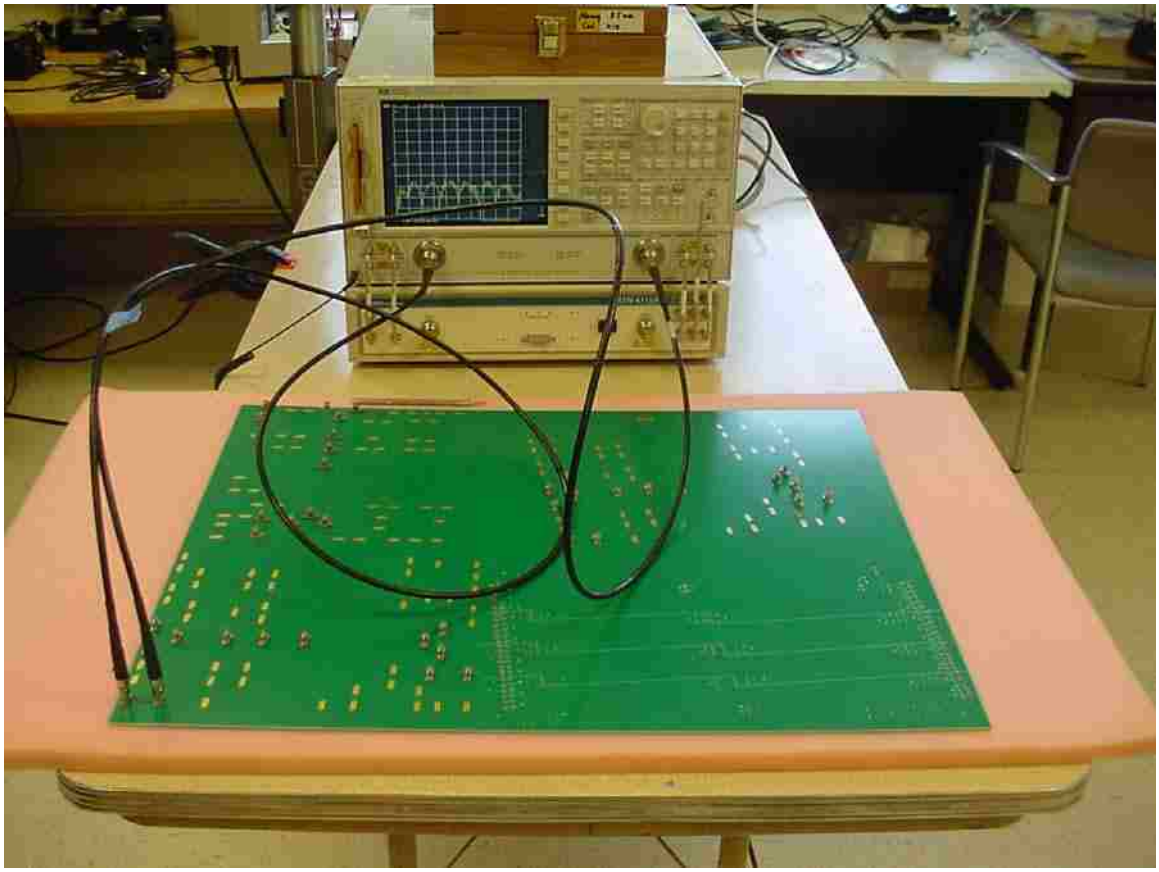
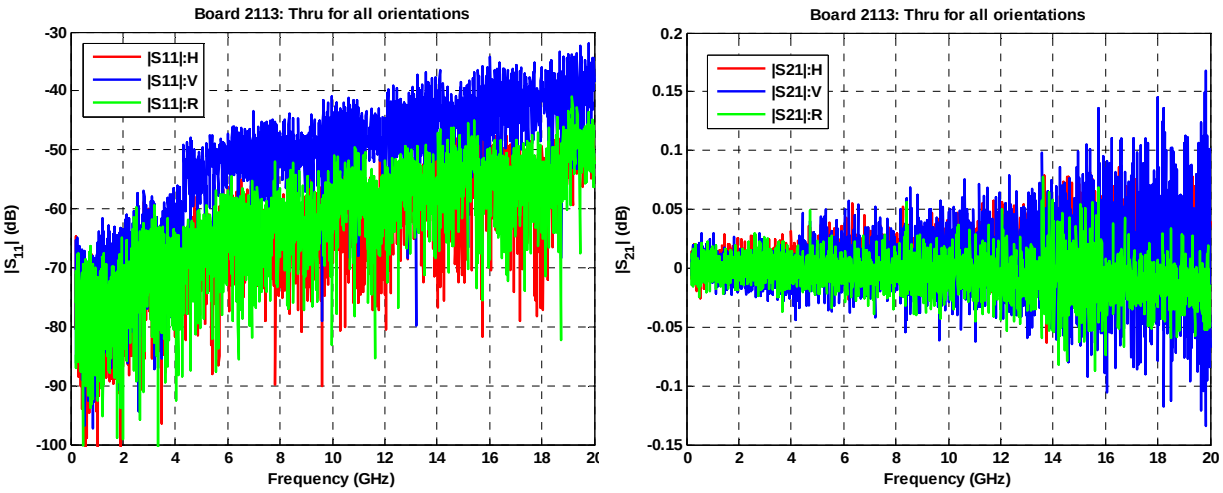


Figure 2.8. Test setup used for stripline measurements.

TRL calibration was done on all three test pattern orientations. Calibration included separate measurements on three different frequency ranges. All the data obtained after measurements on the three frequency ranges were combined to span the entire frequency range. S-parameters of Board 2113 and Board 2116 were measured and the measured data were analyzed for errors as shown below. As a part of measurement protocol, a sanity check for effective calibration was done. $|S_{11}|$ and $|S_{21}|$ were analyzed for the "Thru" calibration standard. The expected and observed results are discussed below. This protocol was used for all the measurements but only $|S_{11}|$ and $|S_{21}|$ data for three orientations for Board 2113 are shown in Figure 2.9.



(a) (b)

Figure 2.9. VNA measurement results for "Thru" standard. (a) $|S_{11}|$ with "Thru" calibration standard measurement. (b) $|S_{21}|$ with "Thru" calibration standard measurement.

For a frequency range of 200 MHz – 20 GHz, return loss seem to be well below -30 dB and $|S_{21}|$ remains almost 0 dB at low frequencies and spreading out to a range of <0.2 dB at higher frequencies. This proves that the calibration was done correctly and measurements could be taken with reasonable levels of accuracy. Figure 2.10 shows measurements on trace ST1. Above 18 GHz, non-ideal artifacts are visible. This is due to the non-ideal effects of two non-identical ports. Figure 2.11 shows the return loss of the two boards for the test trace ST1. At approximately 18 GHz, the return loss goes above -20 dB which is unacceptable for this analysis. If return loss goes above -20 dB, $|S_{21}|$ is affected as shown in Figure 2.10. A sudden dip in $|S_{21}|$ is observed after 18 GHz for horizontal trace ST1 on Board 2116. The physics underlying this phenomenon is beyond the scope of this thesis. Thus, the extraction of parameters above 18 GHz is considered inaccurate.

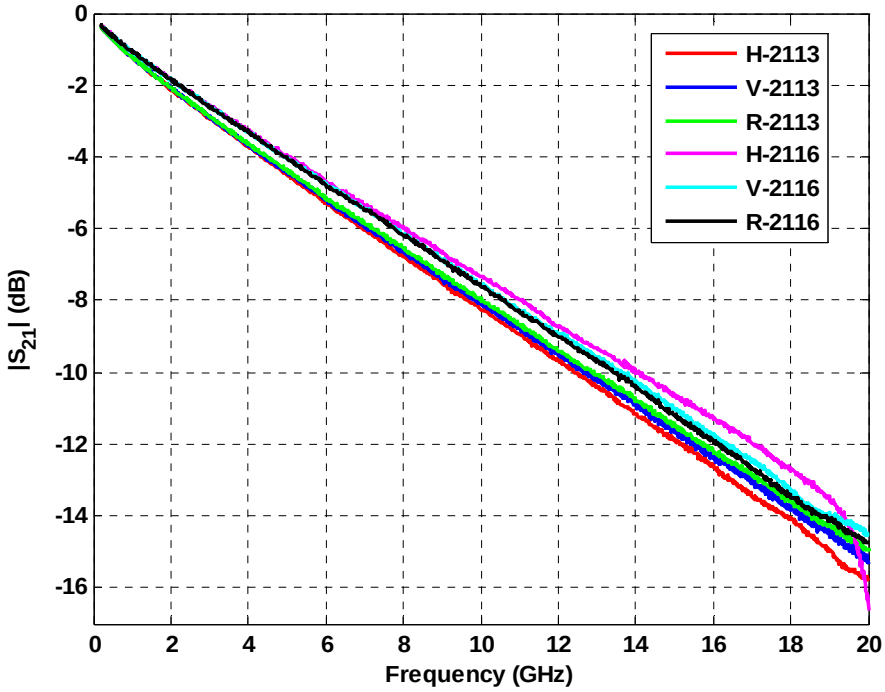


Figure 2.10. Measured $|S_{21}|$ of the test trace ST1.

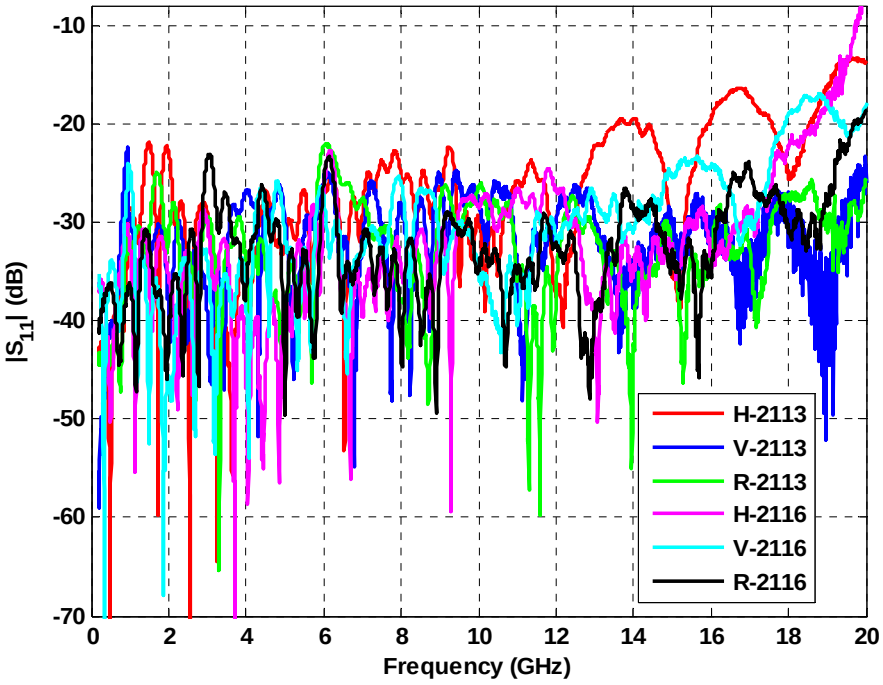


Figure 2.11. Measured $|S_{11}|$ of the trace ST1.

As mentioned earlier, the test board consisted of three different orientations: vertical, horizontal and 10^{o} rotated from horizontal. Each section had its own calibration patterns because for TRL calibration results may vary even with the different weave effects of the fiber in the material. Measurements were done on all three orientations to study the effects due to orientation of the traces in the board. Figure 2.10 shows some difference in the $|S_{21}|$ due to orientation of traces. But, the analysis of the underlying physics is beyond the scope of this thesis.

Ideally, the measurements taken after switching port locations should be the identical. This was true in measurements, because $|S_{12}|$ and $|S_{21}|$ were always almost equal. But, in real world, none of the ports will be exactly the same. So, measurements were taken after switching the ports to see if there are any variations. Figure 2.12 shows that $|S_{12}|$ and $|S_{21}|$ are same even after switching ports.

In the extraction procedure, it is assumed that the impedance of the trace stays constant, along the length of the trace. Ideally it should be constant. Because of the change in width and dielectric thickness due to process variations, the impedance varies at different locations along the trace. So, it becomes important to observe if the impedance variation is small and is close to 50Ω. Cross-sections of these geometries could provide us a better understanding of the variation. But it is a painful and hard process. Time domain reflectometry (TDR) measurements are a good way to analyze the impedance variation along the length of a trace. Every single trace on the board was analyzed using TDR measurements and the impedance variation stayed within 48-53Ω. Though, for extraction procedure, the mean value of the impedance is taken into consideration for calculations. The test setup and procedure is explained below.

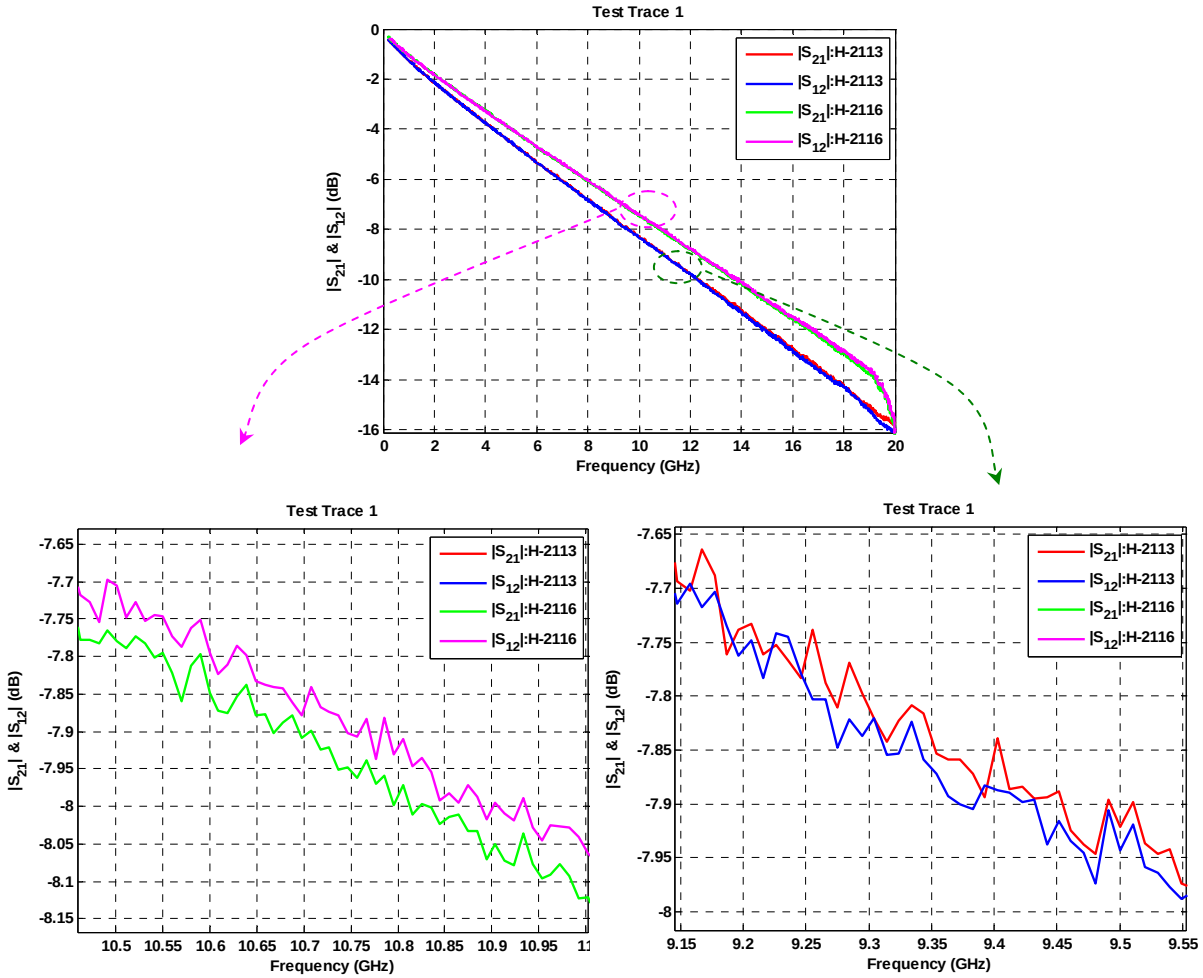


Figure 2.12. $|S_{21}|$ and $|S_{12}|$ comparison after ports were switched manually.

The test setup used to measure impedance along the trace is shown in Figure 2.13. One port of TDR was connected to the trace and the other end of the trace was shorted using a "Short" calibration standard. TDR sends out a pulse through the transmission line which was reflected from the other end of the trace with a reflection coefficient of -1 (short). The impedance was calculated based on the reflection coefficient at various locations on the trace. These measurements were taken on all the traces including the calibration traces, on all three orientations of boards 2113 and 2116. This was done to

observe if the impedance variation was close to 50Ω, and also to determine if any of the traces are damaged or if three was any discontinuity along the length of the trace. Figure 2.14 shows the impedance measurements on trace ST1.

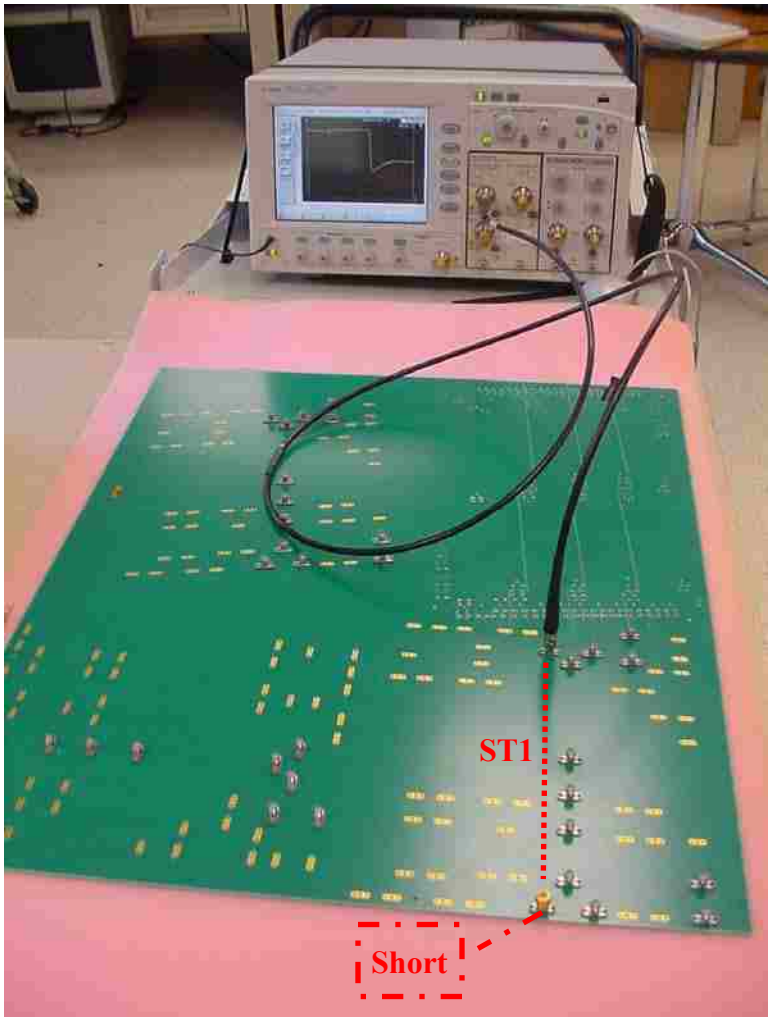


Figure 2.13. Test setup used to measure impedance along the length of a trace.

All orientations were compared on Board 2113 and Board 2116. The impedance variation along the trace was only ±3 Ω of the desired impedance. Figure 2.14 shows the

actual measurements. Enlarged views of capacitive connector discontinuity and impedance variation along the trace are also shown in Figure 2.14.

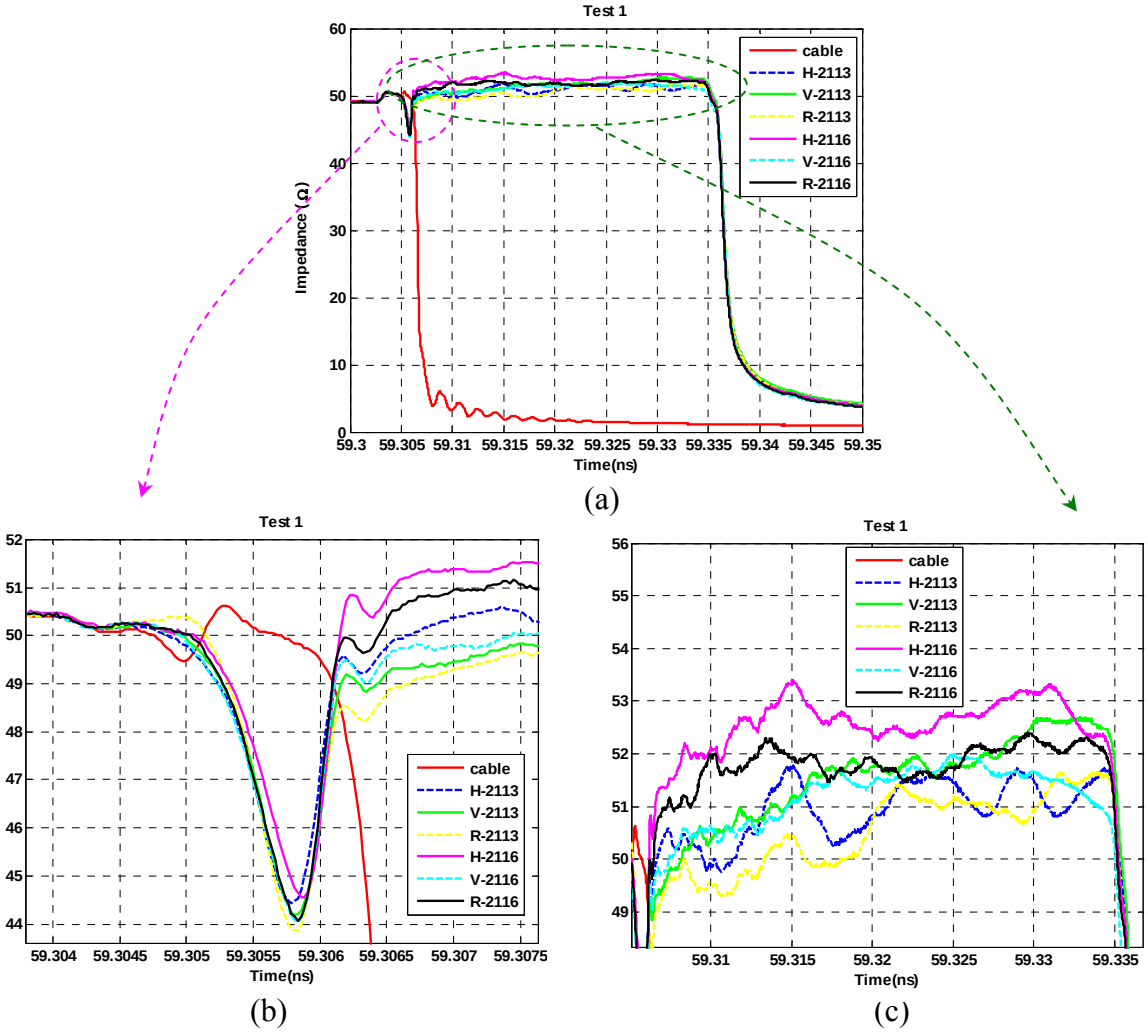


Figure 2.14. TDR measurements on trace ST1. (a) TDR Impedance measurement along the trace length of ST1. (b) Capacitive connector discontinuity (c) Enlarged view of impedance variation along the trace.

2.1.4. Extracted Results and Analysis. The measured data was analyzed with a TDR for its discontinuity. The $|S_{21}|$ and $|S_{11}|$ of the "Thru" calibration standard was within

acceptable limits as discussed in Section 2.1.3. The $|S_{21}|$ and $|S_{11}|$ of the measured test traces were also in acceptable limits as discussed in Section 2.1.3. Then, measurement data was used for extracting the material properties using the algorithm detailed in Section 2.1.2. Measured S-parameters were used to calculate dielectric constant and loss tangent as a function of frequency. Figure 2.15 shows the dielectric constant as a function of frequency. It is clear from the extractions that the conventional representation of dielectric constant as a mere constant no longer holds. The dielectric constant is high at lower frequencies and gradually decreases as frequency increases. The real behavior of materials at lower frequencies can be explained using polarization loss and Debye behavior, which is beyond the scope of this thesis. The variation of dielectric constant for different orientations can also be seen in Figure 2.15. Ideally, there should be no difference in the dielectric constant for any orientation in the same board because it is made of the same material. However, some variation is observed because of the weave effects of fiber causing variations in the actual measurements itself. The sensitivity of weave effects on the measurements is not reported in this thesis [8]. Figure 2.16 shows the loss tangent as a function of frequency. This also includes a comparison of boards, 2113 and 2116, on all orientations.

As discussed in Section 2.1.3, the return loss of horizontal trace in Board 2116 goes beyond limits when the frequencies are above 18 GHz. Hence, extraction results above 18 GHz cannot be trusted. However, it is shown here to demonstrate the effects of return loss on the extraction procedure. Same low frequency behavior is observed here on loss tangent curves as in dielectric constant curves. At lower frequencies, the loss tangent values are high and they gradually reduce to be a constant over higher frequency ranges.

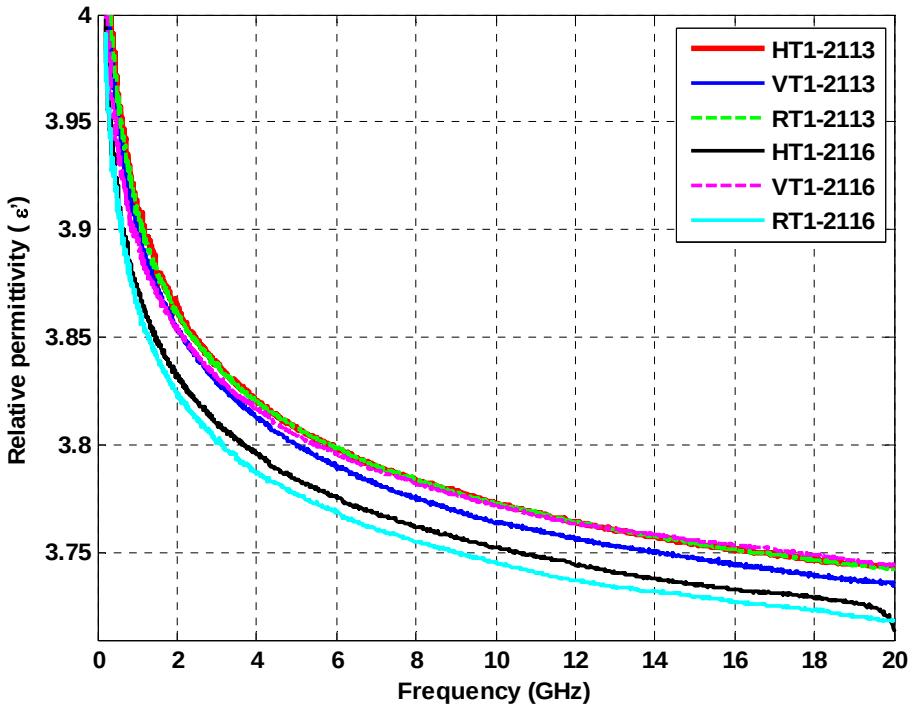


Figure 2.15. Dielectric constant as a function of frequency for boards 2113 and 2116.

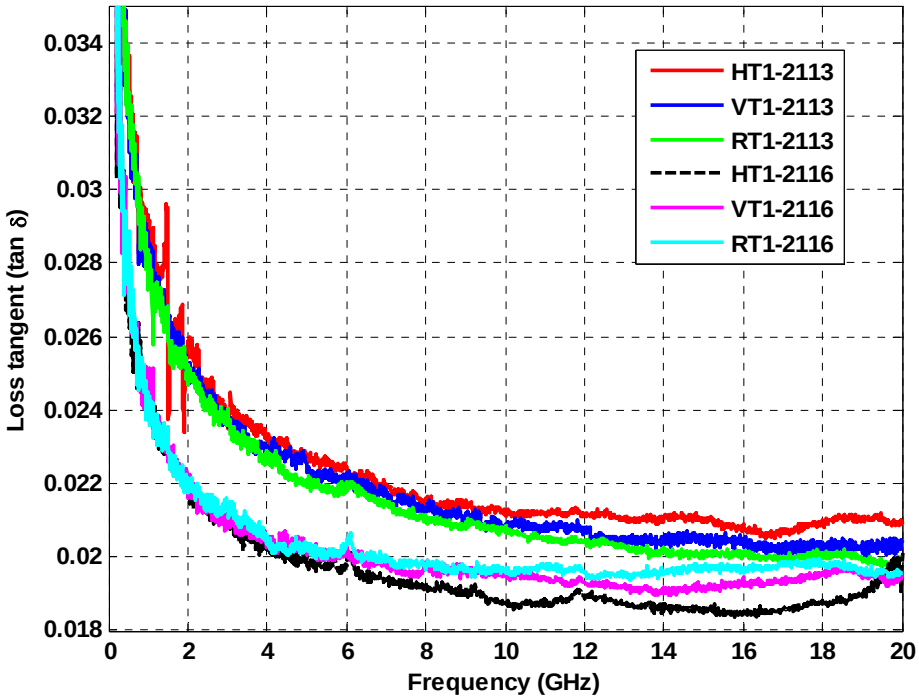


Figure 2.16. Loss tangent as a function of frequency for boards 2113 and 2116.

2.2. EXTRACTION OF MATERIAL PARAMETERS FROM MICROSTRIP

As discussed in Section 2.1, the material properties of stripline geometry can be extracted directly from S-parameter measurements. This is fairly a straight forward process for stripline structure, since the field is contained and there is only one dielectric medium. Therefore, TEM mode of wave propagation can be assumed. But, when microstrip geometry is considered, mode of propagation of the waves is not TEM anymore. The dielectric material and air act as medium of propagation. For most of the operating frequency range of microstrips, the longitudinal components of the fields for the dominant mode are very much smaller than the transverse components. So, the transverse components can be neglected. The dominant mode then behaves like TEM mode and this approximation is called the Quasi-TEM approximation [7]. An effective permittivity and effective loss tangent as function of frequency were considered in this case. Literature also provides closed form expressions to calculate the practical values of material properties which will be discussed later.

2.2.1. Geometry and Test Vehicle Design. As discussed earlier, for microstrip geometry, Quasi TEM approach is used and the new geometry would be represented as shown in Figure 2.17.

In order to validate the new microstrip extraction procedure, specific microstrip test vehicles were designed. To design a test vehicle for material parameter extraction, several characteristics needs to be analyzed. Only the material is of interest and other non-ideal artifacts should be avoided to the greatest extent. Some of the important characteristics are analyzed in detail below. This analysis helps in building up geometry with approximate dimensions.

To make the trace compatible with the measurement equipment, both instrument and the device under test should have the same impedance i.e. 50Ω. This was used to avoid unnecessary reflections due to port mismatch. The impedance of microstrip geometry is dependent on the width, thickness of the trace and also the thickness of the dielectric medium. So, the dimensions have to be carefully chosen to obtain a final impedance of 50Ω.

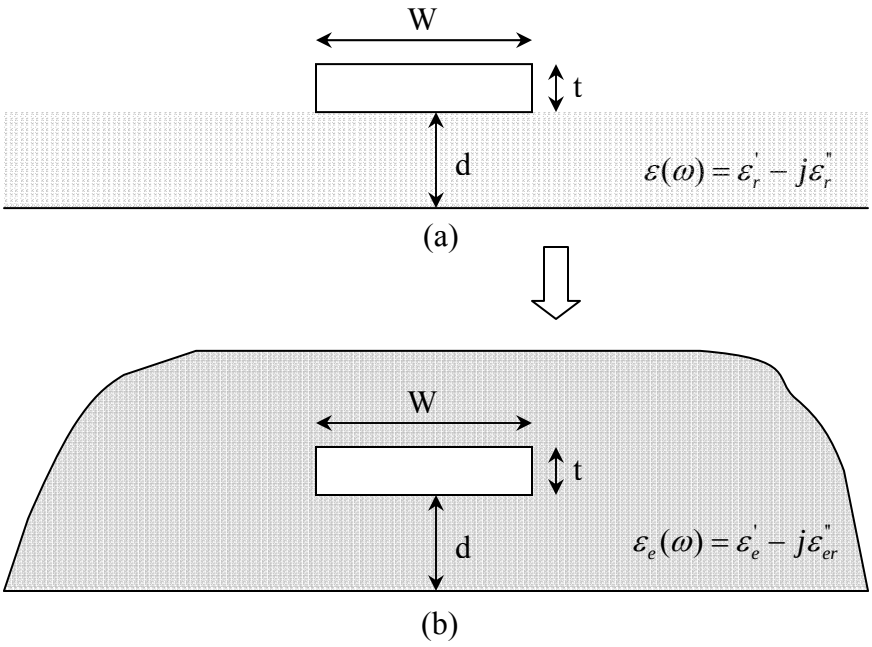


Figure 2.17. Microstrip geometry. (a) Cross sectional geometry of a microstrip trace. (b) Quasi TEM approximation of microstrip geometry.

The impedance constraint of 50Ω can be met by choosing several width and thickness combinations. But, the other important consideration was to make conductor losses as small as possible. The purpose of this test vehicle design was to extract the

material properties of the dielectric material between the conductors. So, it became important to make the dielectric loss dominate over the frequency range of interest. This was achieved by doing the cross-over point analysis. The cross-over point is the frequency at which there is equal contribution of conductor loss and dielectric loss. The ratio of dielectric loss to conductor loss is 1 at the cross over point.

$$\frac{\alpha_d}{\alpha_c} = 1. \tag{2.13}$$

where 'α_d' is the dielectric loss and 'α_c' is the conductor loss.

So, the idea was to choose the dimensions in such a way that the cross over point appears at very low frequencies. This analysis can be done using two methods. One was to use analytical expressions of loss parameters to calculate the cross over point [9]. The other method was to use static solvers such as Hyperlynx which calculates the loss curves directly.

Taking the impedance and cross over point into consideration the following geometry parameters were chosen for the design of microstrip traces. Figure 2.18 shows the loss curves and the cross over point.

Width of the trace (W) = 9.5 mils

Thickness of the trace (t) = 1.2 mils

Thickness of the dielectric medium (d) = 5 mils

Approximate εr used for calculation = 3.9

Approximate tan δ used for calculation = 0.02

The impedance of the line calculated with these geometry parameters was 50Ω. And the cross-over point was obtained to be approximately 0.6 GHz.

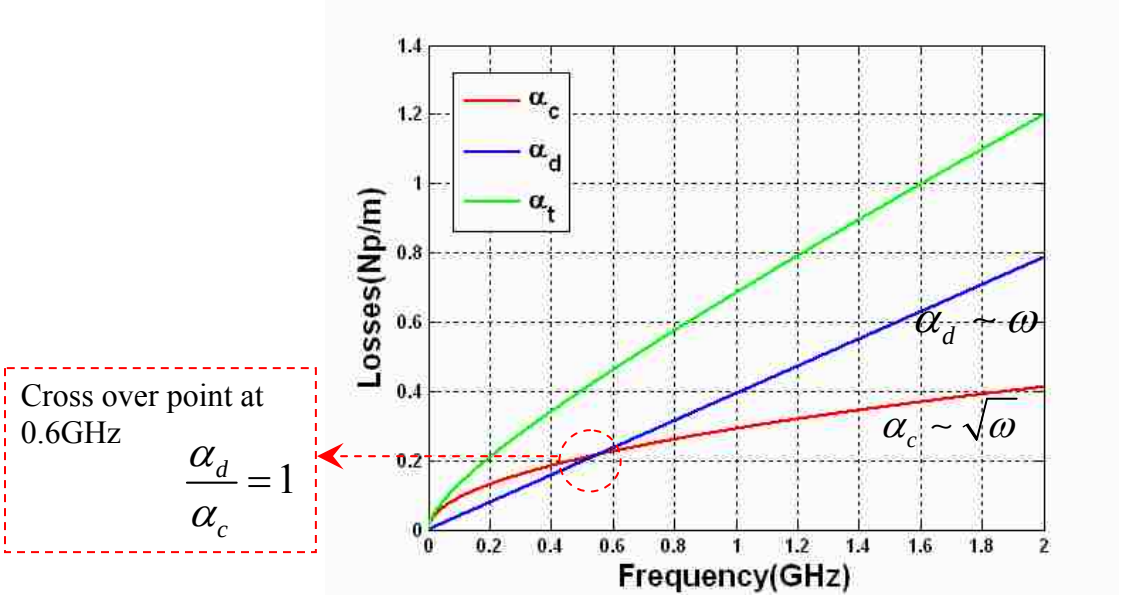


Figure 2.18. Loss curves obtained after using the current geometry parameters with the cross over point at 0.6 GHz.

The frequency range of interest for this project was 0-20 GHz. However, it was important to make sure that the design was compatible for such high frequency range. The following are three frequency considerations that were taken into account. These considerations were also used in the design of stripline test vehicles [11] discussed in Section 2.1.1.

Three mechanisms may limit the application frequencies of microstrip lines: higher-order modes, surface wave propagation in the planar metal-dielectric-air structure, and radiation effects in the open structure [10]. It is reasonable to estimate the upper frequency limit based on the three mechanisms, and take the lowest value as the upper-bound of the interest frequency. The cutoff frequency for the first higher-order mode was estimated as

$$f_c = \frac{c_0}{\sqrt{\varepsilon_e'}\left(2W + 0.8d\right)}. \tag{2.14}$$

where 'c_o' is the speed of light in free space. The lowest TM surface mode has no cutoff frequency, but its coupling to the quasi-TEM mode becomes significant only when their phase velocities are nearly matched. This occurs at the frequency

$$f_s = \frac{c_0 \arctan\left(\varepsilon_e^{'}\right)}{\sqrt{2}\pi d\sqrt{\varepsilon_e^{'}-1}}. \tag{2.15}$$

An approximate relation for the frequency where the radiation becomes significant was

$$f_r > \frac{2.14\sqrt[4]{\varepsilon_e^{'}}}{d}. \tag{2.16}$$

where f_r is in GHz, and *d* is in millimeters.

For the test board considered, Table 2.2 provides the values of frequencies mentioned on (2.14), (2.15), and (2.16). It is clear from Table 2.2 that the required frequency range of 0-20 GHz opposes no limitations.

Table 2.2. Frequency limitations for the microstrip test vehicle design.

f_c	260 GHz
f_s	412 GHz
f_r	24 GHz

The purpose of this test vehicle was to provide information of the dielectric material used for its construction. Hence, the measurements should only depict effects of the dielectric. It was not desirable to have non-ideal effects of cables, vias and connectors on measurements. Thus, TRL calibration technique was used to de-embed the effects of

such non-idealities. With the conventional measurement setup, the reference plane can only be set within the measurement equipment. The actual measurement will include effect of vias, probes, connectors etc. which will degrade the measurement results. But, with TRL calibration technique [7], the reference plane can be set at a desired point on the device under test. This calibration procedure characterizes the error boxes associated with the discontinuities till the device under test, setting the reference plane at a desired point. The TRL calibration patterns were designed the following way.

To achieve a good TRL calibration kit, the useable bandwidth of a single THRU/LINE pair was less than 8:1 (frequency span/start frequency) [11]. The frequency span was 19.8 GHz, and the start frequency was 0.2 GHz, which means three THRU/LINE pairs are needed. The next step was to separate the frequency span 19.8 GHz into three segments. The optimal break-frequency points are the geometric mean frequency

$$f_j = \sqrt{f_1 \bullet f_2} \tag{2.17}$$

For this case, the lowest frequency was $f_1 = 0.2$ GHz and the highest frequency was $f_4 = 20$ GHz. Then there will be two equations for the two unknown frequencies

$$f_2 = \sqrt{f_1 \bullet f_3} \tag{2.18}$$

$$f_3 = \sqrt{f_2 \bullet f_4} \tag{2.19}$$

Solving the above two equations, the frequencies were found to be $f_2 = 0.93$ GHz and $f_3 = 4.3$ GHz. Then, the frequency range based on the calibration requirement was separated into three segments, 0.2-0.93 GHz, 0.93-4.3 GHz, and 4.3-20 GHz.

Another condition for designing a good TRL calibration was that the insertion phase difference between the THRU and LINE must be between (20˚ and 160˚) ±n × 180˚ for a quarter wavelength [11]. Otherwise, the measurement uncertainty will increase significantly when the insertion phase nears 0˚ or an integer multiple of 180˚. The quarter wavelength at center frequency can be calculated from

$$\lambda q = \frac{1}{4} \bullet \frac{c \big/ \sqrt{\varepsilon_e}}{\left(f_i + f_{i+1} \right) \big/ 2} = \frac{c}{2\sqrt{\varepsilon_e}\left(f_i + f_{i+1} \right)} = \frac{1.5 \times 10^8}{\sqrt{\varepsilon_e}\left(f_i + f_{i+1} \right)} \tag{2.20}$$

where 'c' is the light speed in free space. 'ε_e' is the effective dielectric constant given by

$$\varepsilon_e = \left(\frac{\varepsilon_r + 1}{2} \right) + \left(\frac{\varepsilon_r - 1}{2} \right) \left(1 + \frac{12d}{W} \right)^{-0.5} \tag{2.21}$$

Then the phases for the quarter wavelength at the frequency f_i and f_{i+1} are evaluated as

$$P_i = \frac{360^0 \, f_i \lambda_q}{c \big/ \sqrt{\varepsilon_e}} = \frac{180^0 \, f_i}{f_i + f_{i+1}} \tag{2.22}$$

and

$$P_{i+1} = \frac{360^0 \, f_{i+1} \lambda q}{c \big/ \sqrt{\varepsilon_e}} = \frac{180^0 \, f_{i+1}}{f_i + f_{i+1}} \tag{2.23}$$

Then the phases at lower and upper frequency points for each frequency segment are calculated, and the values are given below. It is clear that all the calculated phases in (2.24) meet the insertion phase requirements since the phase always remain between (20˚ and 160˚) ±n × 180˚ for a quarter wavelength. Thus, the picked frequency break points are optimized in this case. Now, the other parameters in TRL calibration kits are calculated.

$$\begin{cases} P_{11} = \dfrac{180^0 \times 0.2}{0.2 + 0.93} = 31.86^0 \\ P_{12} = \dfrac{180^0 \times 0.93}{0.2 + 0.93} = 148.14^0 \\ P_{21} = \dfrac{180^0 \times 0.93}{4.3 + 0.93} = 32^0 \\ P_{22} = \dfrac{180^0 \times 4.3}{4.3 + 0.93} = 148^0 \\ P_{31} = \dfrac{180^0 \times 4.3}{4.3 + 20} = 31.85^0 \\ P_{32} = \dfrac{180^0 \times 20}{4.3 + 20} = 148.15^0 \end{cases} \tag{2.24}$$

Since the difference between LINE and THRU must be equal to quarter wavelength

$$L - T = \lambda q \tag{2.25}$$

where 'T' indicates the length of THRU, and 'L' is the length of LINE. Substituting (2.20) into (2.25),

$$L = T + \frac{1.5 \times 10^8}{\sqrt{\varepsilon_e}\,(f_i + f_{i+1})} \tag{2.26}$$

Choosing the length of OPEN was equal to half of the THRU, then,

$$O = T / 2 \tag{2.27}$$

where 'O' indicates the length of OPEN. Since the dielectric permittivity of the test board is 3.9, or $\sqrt{\varepsilon_e}$ was calculated from (2.23) to be 1.728. The (2.26) was simplified to

$$L = T(mils) + \frac{3417.543}{(f_i + f_{i+1})_{GHz}}(mils) \tag{2.28}$$

The values given in Table 2.3 are available for the TRL calibration kit geometries shown in Figure 2.19, which was used for single-ended microstrip calibration. The actual

board manufactured is shown in Figure 2.20. The landing pattern for each trace is also shown in Figure 2.21.

Table 2.3. Parameters of single-ended microstrip TRL calibration kit.

ST (mils)	SO (mils)	SL1 (mils)	SL2 (mils)	SL3 (mils)
1000	500	4024	1653	1141

The test board was a simple two layer board with the material under test used as dielectric. Dimensions chosen for microstrip traces were shown in Section 2.2.1. The lengths of those traces are shown in Table 2.3. The next step was to lay those traces on to a printed circuit board (PCB). Figure 2.19 shows the overall layout for the microstrip test vehicle. Figure 2.21 shows the landing pad layout for the microprobes. Microprobes are used for measurement to achieve accurate results. Similar to the design of stripline boards, three orientations, Vertical, Horizontal and 10^{o} Rotated from horizontal traces, were considered with its own calibration patterns. Apart from the calibration traces, there are two test traces, ST1 and ST2 available on all three orientations. ST1 was 6000 mils long and ST2 was 9000 mils long. The overall size of the board was 11100x11100 mils. Figure 2.20 shows the actual board. Copper was filled on the top layer of the board separating the traces. This was done to avoid warping of the board which could break the traces. Analysis was done using static solver tool, Hyperlynx, to make sure that there was not coupling between copper fill and the traces on the top layer. Proper spacing was provided according to the analysis.

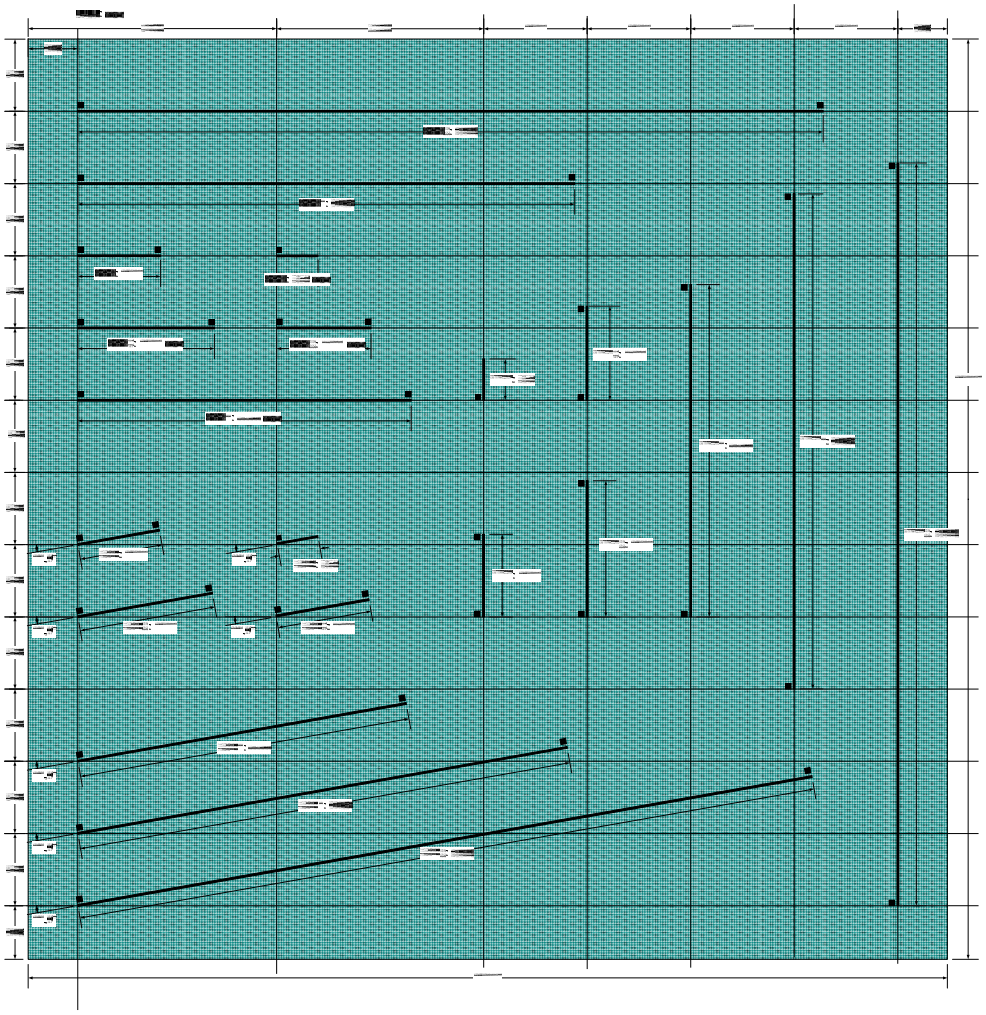


Figure 2.19. Microstrip test vehicle design including TRL calibration and test traces.

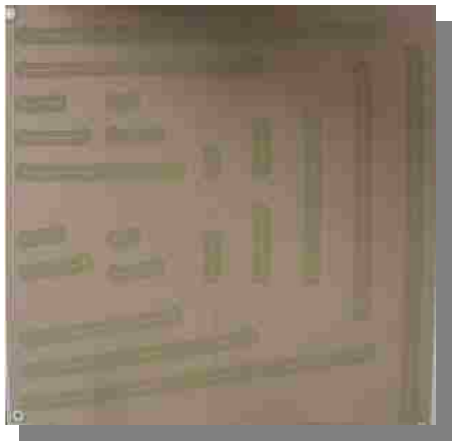


Figure 2.20. Actual board: microstrip test vehicle design.

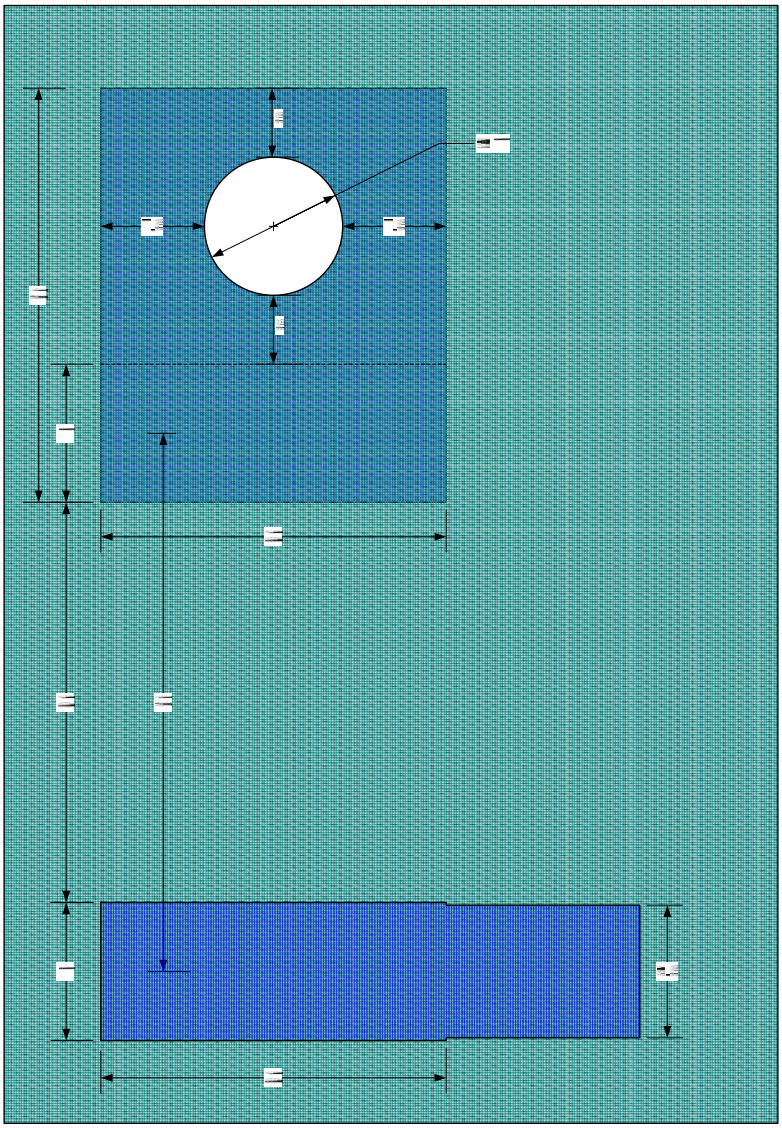


Figure 2.21. Landing pad design for each trace.

A small section of the trace is shown at the bottom of Figure 2.21. The width of the trace was increased at the edges to accommodate the probe tips. The pad includes a via hole connected to the bottom copper layer. Enough room was also given there for landing the probe tips. The probe pitch was chosen to be 1000μm. This probe turned out to be very fragile and hard to use. But, there were also long traces in the design which

cannot be viewed through the high resolution microscope of the probe station. So, external microscope was used which had lower resolution. In this case, it would be hard to view the probe tips when landing the probes. For this reason, it was not possible to go for a lesser probe tip pitch than 1000μm.

2.2.2. Material Extraction Procedure for Microstrip. Two methods are suggested here for the extraction of material properties from microstrip structure. First one is approximation method, which is very similar to the stripline material extraction procedure explained in Section 2.1.2. The other method is called the Curve-fitting method, where the losses are curve fitted to a loss expression to obtain individual contribution of losses.

2.2.2.1. Approximation method. This method is almost the same as the extraction procedure for stripline structure. However, it should be noted that microstrip structures are evaluated as Quasi-TEM models. The extracted parameters would not be the actual material parameters but are obtained as effective material parameters. The effective values can be converted back to the practical values with closed form expressions, which will be explained later. The procedure flow diagram is shown in Figure 2.22. S-parameter measurements are taken for the device under test after TRL calibration was done. The measured S-parameters are converted to ABCD parameters. The propagation constant and total loss is represented as shown in (2.1), (2.2) and (2.3). From (2.3), it is assumed that the total loss is a contribution of conductor loss and dielectric loss. But, conductor loss is a function of geometry and can be calculated using analytical expressions [9]. (2.31) shows the expression for conductor loss.

$For \quad \frac{1}{2\pi} < \frac{W}{d} \leq 2 .$

where ‘W’ is the width of the trace, ‘d’ is the dielectric thickness and effective width is

$$W' = W + \Delta W \,. \tag{2.29}$$

where ‘ΔW’ is the correction term added to take into account of the thickness of the trace [9] given by

$$\Delta W = \frac{t}{\pi}\ln\left(\frac{2d}{t}+1\right). \tag{2.30}$$

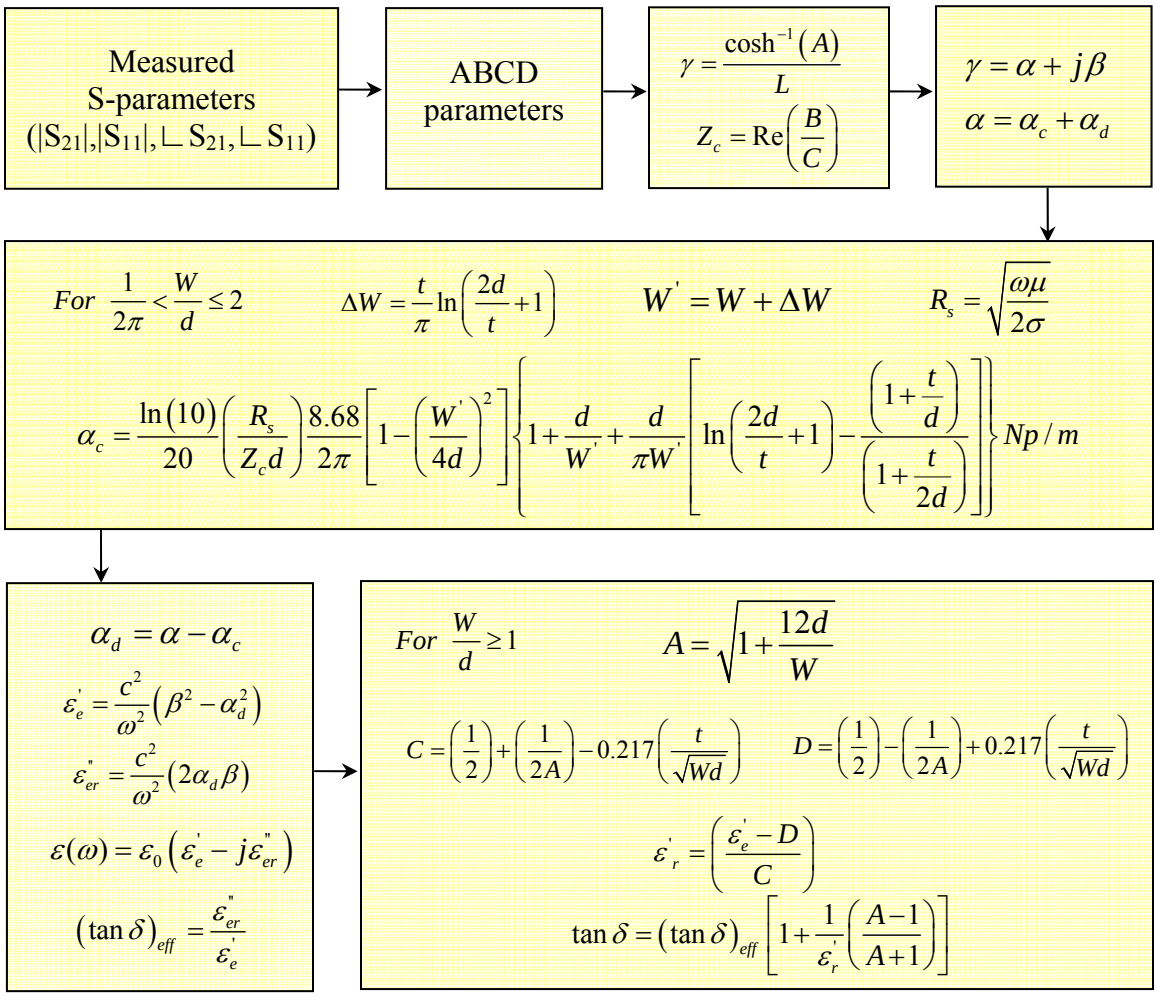


Figure 2.22. Material extraction algorithm (approximation technique) for microstrip.

Thus, the conductor loss can be calculated as

$$\alpha_c = \frac{\ln(10)}{20}\left(\frac{R_s}{Z_c d}\right)\frac{8.68}{2\pi}\left[1-\left(\frac{W'}{4d}\right)^2\right]\left\{1+\frac{d}{W'}+\frac{d}{\pi W'}\left[\ln\left(\frac{2d}{t}+1\right)-\frac{\left(1+\frac{t}{d}\right)}{\left(1+\frac{t}{2d}\right)}\right]\right\} Np/m\,. \tag{2.31}$$

where 'R_s' is the surface resistance given by (2.7), and 'Z_c' is the mean impedance of the trace. Thus, dielectric loss can be calculated using (2.8). The real and imaginary part of effective permittivity of the Quasi-TEM model can be calculated using expressions (2.9) and (2.10). Effective loss tangent could then be calculated using (2.12).

Once the effective dielectric constant and loss tangent is calculated, closed form expressions can be used to calculate the real practical value of dielectric constant and loss tangent of the material [12]. Equations (2.32) and (2.33) shows the relationship.

$$For\ \frac{W}{d}\geq 1;\ \ \varepsilon_r' = \left(\frac{\varepsilon_e' - D}{C}\right). \tag{2.32}$$

$$\tan\delta = (\tan\delta)_{eff}\left[1+\frac{1}{\varepsilon_r'}\left(\frac{A-1}{A+1}\right)\right]. \tag{2.33}$$

where A, C and D are

$$A=\sqrt{1+\frac{12d}{W}};\ C=\left(\frac{1}{2}\right)+\left(\frac{1}{2A}\right)-0.217\left(\frac{t}{\sqrt{Wd}}\right);\ D=\left(\frac{1}{2}\right)-\left(\frac{1}{2A}\right)+0.217\left(\frac{t}{\sqrt{Wd}}\right) \tag{2.34}$$

It should be noted that both dielectric constant and loss tangent are functions of frequency. It should also be noted that the practical values of material parameters are also weak functions of geometry. So, for this approximation method, reasonable estimates of geometry parameters are required.

2.2.2.2. Curve-fitting method. The procedure for this method is same till the extraction of total loss and phase constant. After the total loss is extracted, a Genetic Algorithm [13] (GA) is used to curve-fit the total loss using an expression relating conductor loss and dielectric loss which is shown in (2.35). The overall flow diagram is shown in Figure 2.23.

Measured, TRL calibrated S-parameters are converted to ABCD parameters. Propagation constant is found using (2.1). The real part of propagation constant, total loss is estimated from (2.2). Total loss is related to conductor loss and dielectric loss as in (2.3). But, conductor loss varies as square root of frequency and dielectric loss varies linearly with frequency. Since, the only variable in the expressions is frequency, the total loss can be represented using (2.35).

$$\alpha = A\sqrt{\omega} + B\omega . \tag{2.35}$$

$$\begin{aligned} \alpha_c &= A\sqrt{\omega}. \\ \alpha_d &= B\omega. \end{aligned} \tag{2.36}$$

where ‘A’ and ‘B’ are constants.

So, conductor loss can be approximated by using (2.36). Therefore, measured dielectric loss can be calculated using (2.8). From dielectric loss and phase constant, the effective material properties can be calculated using (2.9), (2.10), (2.11) and (2.12). The method till here is same as the procedure used for stripline structures. Then, the same equations are used as in approximation technique of microstrips to calculate the practical values of material properties. Equations (2.32) and (2.33) shows the expressions for the calculation of the practical values of material parameters from effective material parameters.

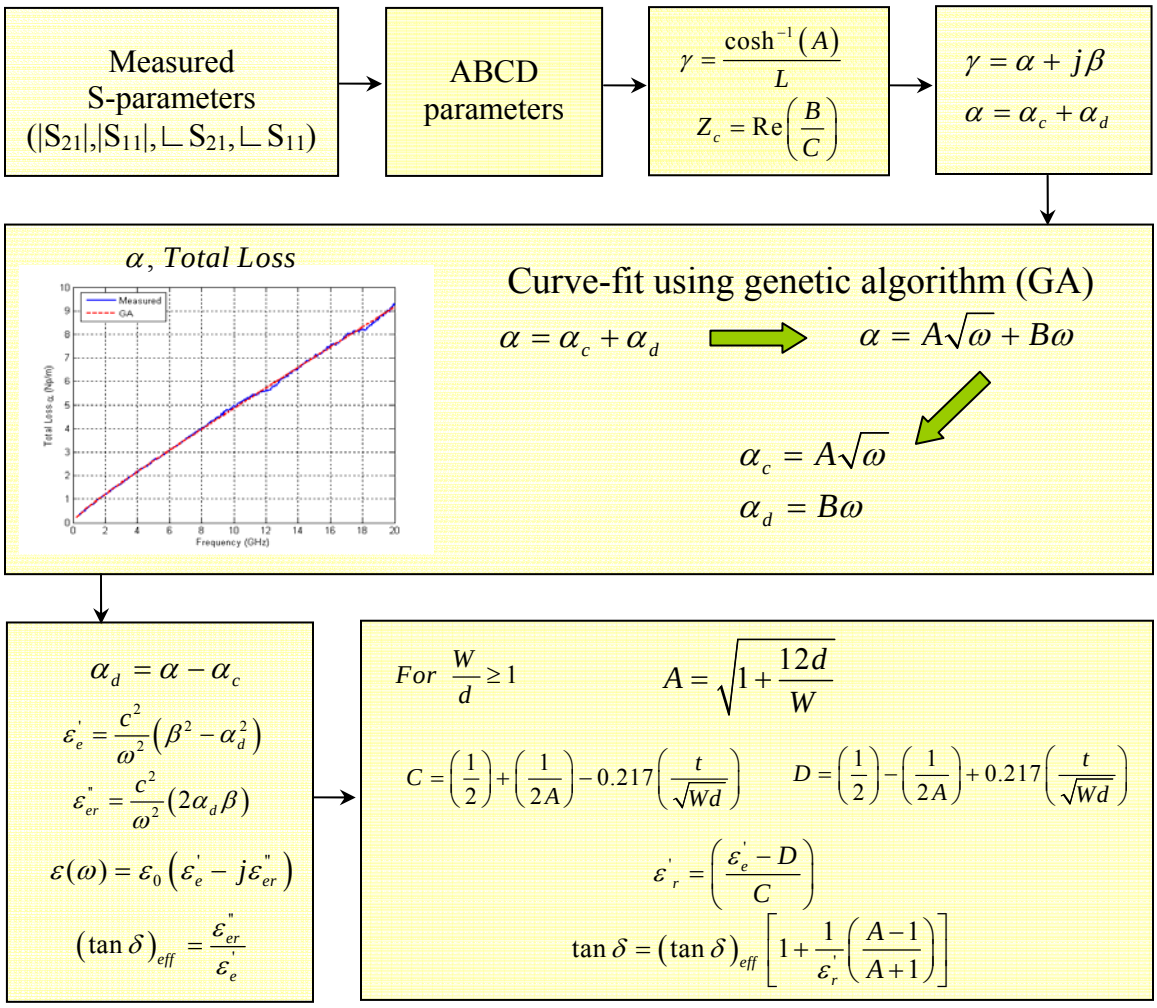
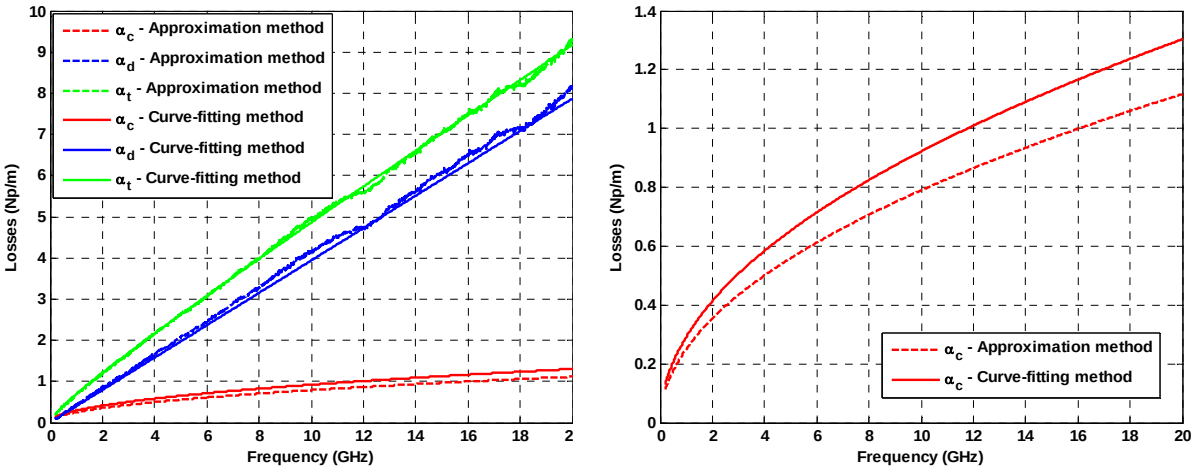


Figure 2.23. Material extraction procedure (curve-fitting) for microstrip.

2.2.2.3. Comparison of two methods. Both methods are very similar and are only different in the way conductor loss was evaluated. Approximation technique, uses analytical expression to calculate conductor loss while curve-fitting method uses GA. But, both methods provide almost the same results with a maximum deviation of 2 dB. Figure 2.24 shows the conductor loss estimated using two methods. In Figure 2.24(b), the difference at higher frequencies is always less than 2 dB.



(a) (b)

Figure 2.24. Extraction method comparison. (a) Comparison of all losses extracted with two proposed methods. (b) Conductor loss variation with frequency for two methods.

This analysis was shown for only one specific material, but the same trend was seen for all the materials which were studied. Though both methods give almost the same answer, the curve-fitting method proves to be much friendlier because the geometry parameters are not required to calculate the conductor loss. Thus, even without the absolute knowledge of the geometry information, the material parameters can be extracted using the curve-fitting method. But, it has to be noted that the conversion of effective properties to practical parameters are still a weak function of geometry.

2.2.3. Test Setup, Settings and Measurements. Measurement for the microstrip test vehicles were more complicated than stripline test vehicles because of the use of Model 9000 Cascade Microtech microprobe station and Fixed Pitch Compliant (FPC) microprobes to measure S-parameters of microstrip traces. Measurements had to be taken carefully because of the fragility of the probes.

The overall test setup consisted of a HP8270D network analyzer, high precision microwave cables, 1000µm pitch Cascade microprobes on the microprobe station, and the microstrip test board. Figure 2.25 shows the real time test setup used for measuring S-parameters of microstrip traces.

Figure 2.25. Test setup for microstrip test board measurement.

The monitor was used to display the microscope's view to better observe the landing pad and probe tips. High precision cables were connected to the VNA and to the two microprobes. The microprobes were mounted on a Model 9000 Cascade microprobe station. The test board was fixed on the probe station with suction control. Microscope was turned ON and the image was viewed through the monitor. The board was adjusted so that the pad was clearly visible on the screen. The probes were adjusted with horizontal x and y knobs to position the probe right above the pad. Then the vertical knob was adjusted so that the probe touches the pad. Utmost care had to be given while

bringing the probe down to made sure that the probe touches the pad. After it touches the pad, the probe slides forward (skating). Enough pressure had to be given to the probe so that it slides at least 0.1mm forward to make proper contact. This had to be done on both sides of the trace. Once properly connected, calibration and measurements were done.

TRL calibration procedure explained in Section 2.1.3 was used for microstrip test board also. The frequency range of interest for this study was 200 MHz – 20 GHz. But, this frequency range was split into three different sections and the corresponding traces in the test board were used for calibration. Each frequency range has to be calibrated separately because each involves different instrument settings. Once calibrated, the instrument settings and calibration data were stored in the VNA for further measurements. For the first frequency range 200 MHz – 930 MHz, the trace SL1 in Figure 2.19 was used as calibration "Line". For second frequency range 930 MHz – 4.3 GHz, the trace SL2 was used as "Line" calibration standard and for the third frequency range 4.3 GHz – 20 GHz, SL3 was used as "Line" calibration standard.

Each frequency range was calibrated separately with different number of points. VNA was set to auto power mode. The first frequency range was set from 200 MHz – 930 MHz with 201 points. The number of averages was set over 16 averages. This was used to reduce the noise in the calibration and measurements. Setting the averages would also set the return loss of the "Thru" standard to as low as -60 dB. First "Thru" standard called ST in Figure 2.19 was connected to VNA for calibration, then "Open" standard called SO was connected for calibration. Then "Line" standard SL1 was connected for calibrating the first frequency range. Isolation was omitted. Once all the standards were measured, the calibration was finished and it was saved for actual measurements.

Similarly, calibrations were done for second frequency range, 930 Mhz – 4.3 GHz with 801 points using the "Line" standard SL2. Calibration was also done for third frequency range 4.3 GHz – 20 GHz with 1601 points using "Line" standard SL3. Once all three frequency ranges were calibrated, measurements were taken on ST1 and ST2. These were very long traces which cannot be viewed through the microscope in the probe station. External microscopes had to be used to view the pads.

The microprobes used for these measurements were 1000μm pitch probes. Two different probes had to be used because of the Ground-Signal configuration of the pad design. Figure 2.26 shows the pads and the corresponding probe configurations used on both sides. The pads for the ground vias were located at the same side of the trace. This required the use of two different configurations of probes.

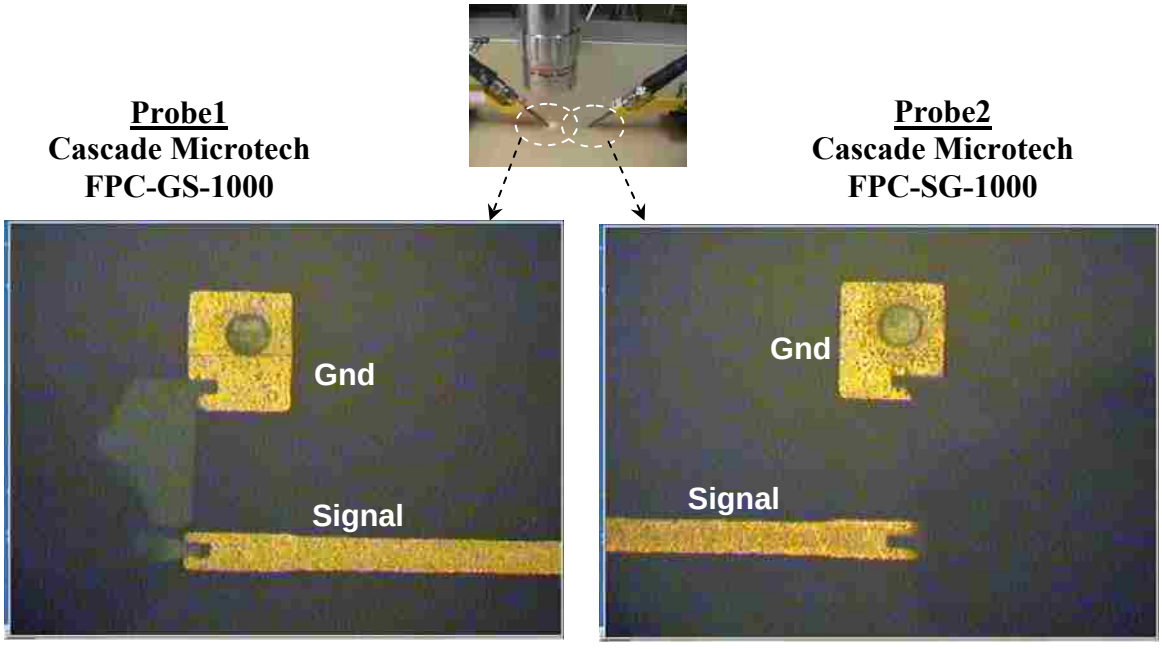


Figure 2.26. View of pads configuration and probe configuration at the edge of traces on the test boards.

The microprobes used were FPC-GS-1000 and FPC-SG-1000 from Cascade Microtech. These probes were very fragile and utmost care had to be taken for reuse. Pressurized air was used to clean the tips of the probe after measurements. This removed the copper debris accumulated at the tips after several measurement cycles. The pads are clearly visible on Figure 2.26. The Ground-Signal configuration is different on both sides. Each probe could only handle a certain number of landing procedures and eventually the tips break off. The probes were very costly and hard to maintain. Other disadvantage of the 1000µm probe was its large tip inductance. TDR measurements were taken to see the impedance of the traces. Figure 2.27 shows the large peak on both sides of the trace showing its large tip inductance. But, with our calibration technique, these effects are taken off in part, assuming that both probes are identical.

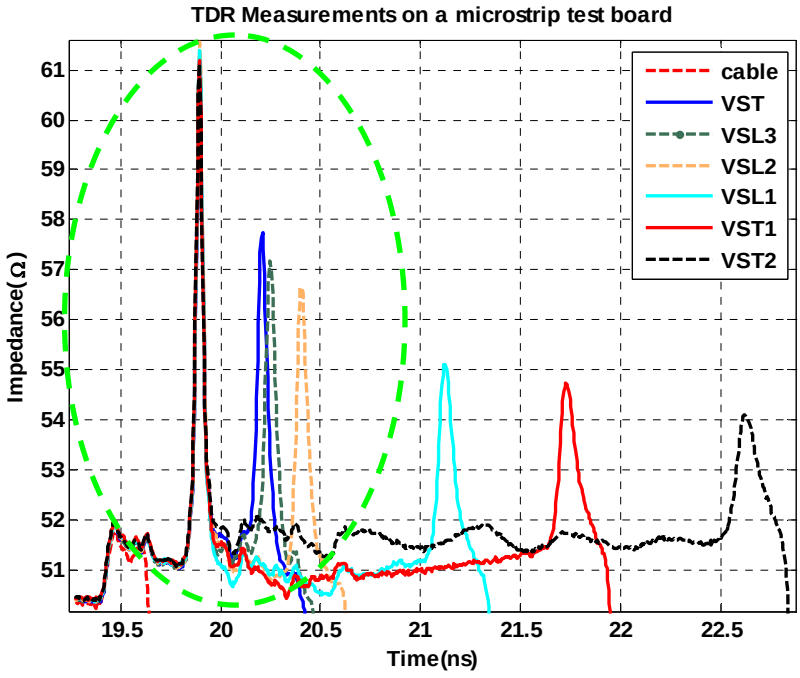
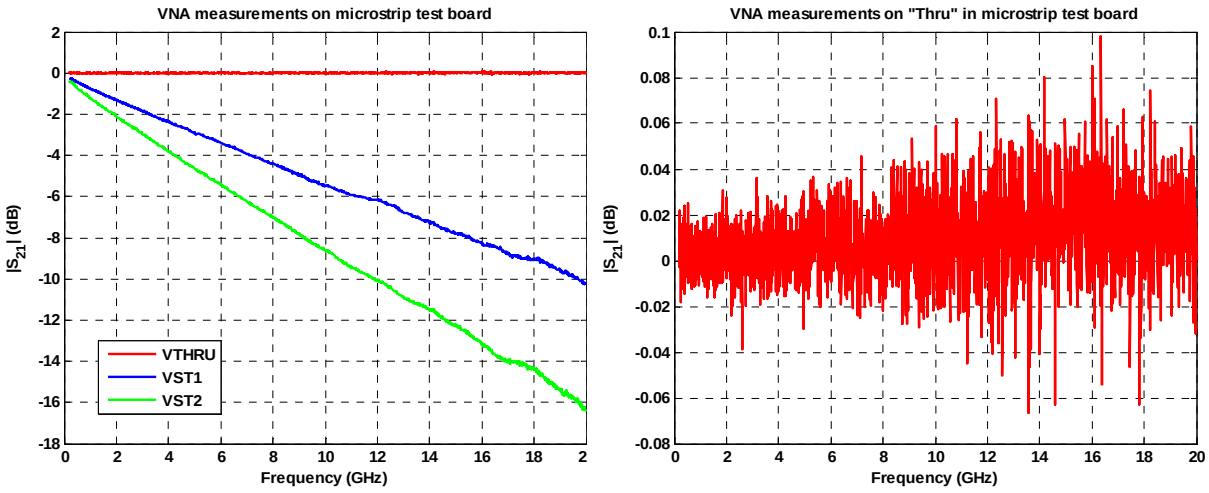


Figure 2.27. TDR measurements on the traces showing the large inductance on both sides of the trace associated with the tips.

2.2.4. Measurements and Analysis. After the TRL calibration was done and saved for all three frequency ranges, the setup was all set for measurements. For this project, 32 test boards made of different FR-4 materials from different vendors and suppliers were studied for its material properties. Orientation analysis study was also done for 3 sets of test boards.

After TRL calibration, test traces VST1 and VST2 from Figure 2.19 were measured and saved in touchstone format. While taking measurements, it was important to analyze how good the measurements are. The simplest way of doing it is to measure the calibration standards again to see if reasonable results are observed as discussed in Section 2.1.3. For example, after calibration, "Thru" standard was showing a return loss ($|S_{11}|$) of less than -50 dB over the entire frequency range. This is because after calibration, the effective length of "Thru" which contributes to the losses is ideally zero. Figure 2.28 shows the $|S_{21}|$ for "Thru" standard, VST1 and VST2 for a sample board.



(a) (b)

Figure 2.28. VNA measurements on microstrip board. (a) $|S_{21}|$ for "Thru" standard, VST1 and VST2. (b) $|S_{21}|$ for "Thru".

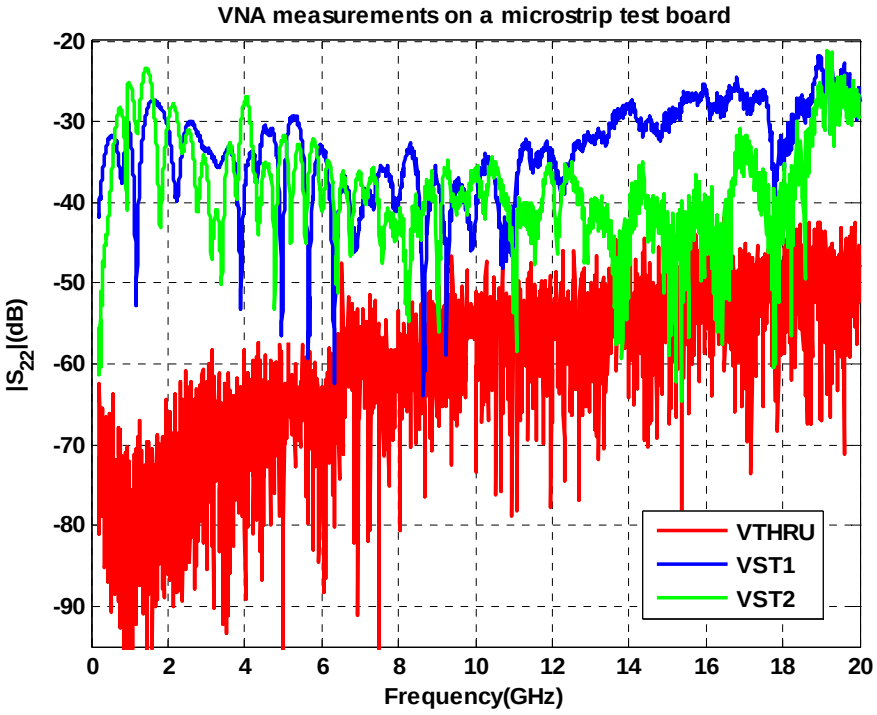


Figure 2.29. Return loss for "Thru" standard, VST1 and VST2.

$|S_{21}|$ should ideally be 0 dB but since the calibration would never be perfect, the variation in magnitude of S_{21} at high frequency was always less than 0.05 dB. The other sanity check was to check the return loss for the "Thru" standard. It was always less than -50 dB even at higher frequencies as shown in Figure 2.28. The next sanity check was to check the return loss for longer traces. It always stayed less than -15 dB which was reasonable. If the return loss goes above -15 dB, the results would be inaccurate. In Figure 2.28 and Figure 2.29, when the return loss become close to -15 dB, the $|S_{21}|$ becomes inaccurate. These sanity checks were done for all the samples calibrated and measured. The $|S_{21}|$ of trace VST2 for all the board measured are given in Figure 2.30, showing varying loss for different FR-4 materials. Figure 2.31 shows the return loss for all the sample board for trace VST2.

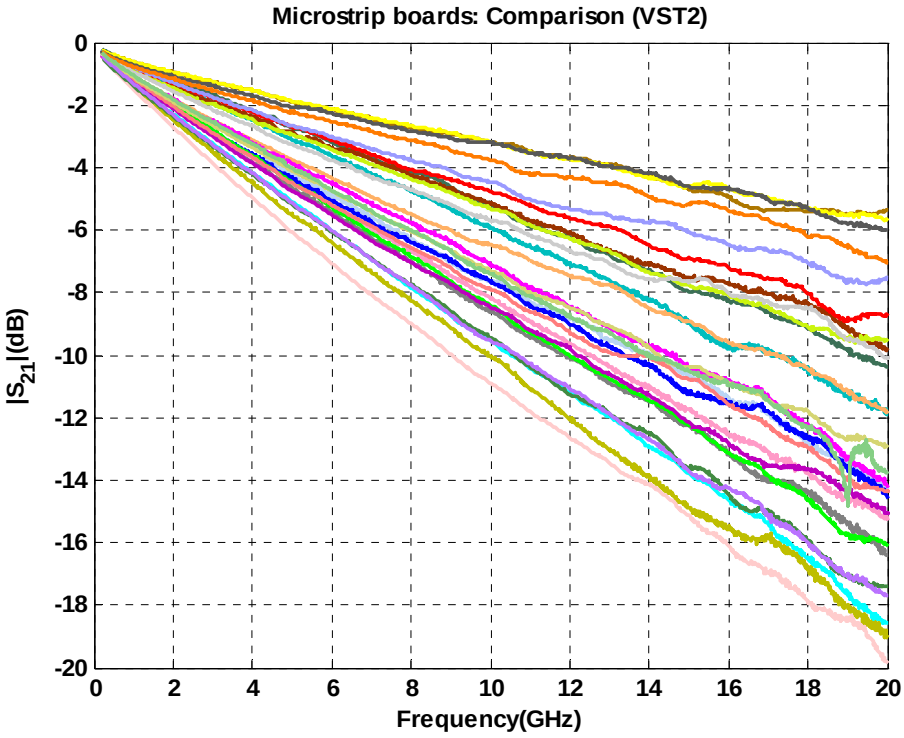


Figure 2.30. $|S_{21}|$ of trace VST2 for all TRL calibrated samples.

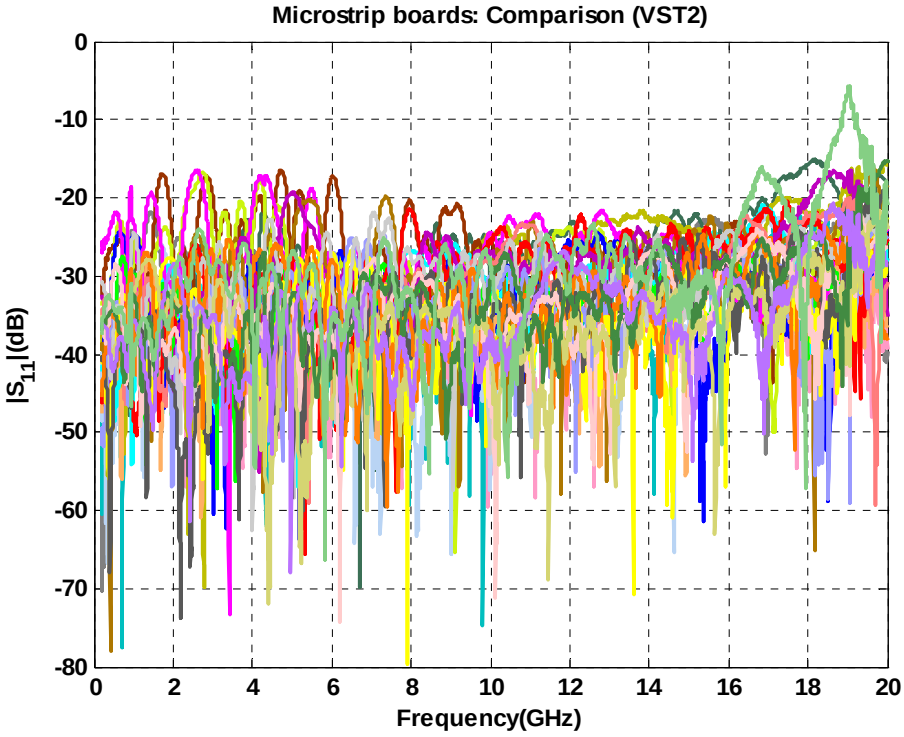


Figure 2.31. $|S_{11}|$ of trace VST2 for all TRL calibrated samples.

From Figure 2.31, most of the sample board satisfies the return loss criteria as discussed earlier. Only the light green curve goes above -15 dB. This was due to measurement or calibration error. The impact of this is shown in Figure 2.30. There is a sudden dip in $|S_{21}|$ at about 19 GHz, which implicates that when return loss goes higher, the results become inaccurate. It was mentioned earlier that separate measurements were taken for three different frequency ranges because there were three different calibration ranges. So, after measurements the data was processed to combine all the three frequency ranges. Figure 2.30 and Figure 2.31 are combined version of all three frequency ranges.

Similar to the discussion in Section 2.1.4, it was important to check for large impedance variations along the length of the trace. Any discontinuity could change the impedance and also could lead to inaccurate results while taking measurements. A break in the calibration standard could give us a wrong calibration. TDR measurements were used to check the impedance with the test setup shown in Figure 2.32.

Figure 2.32. Test setup used for TDR measurements on microstrip test boards.

Figure 2.33 shows a typical TDR measurement from one of the sample boards. It was important to measure the continuity of all the traces in the sample board. This is similar to the setup shown in Figure 2.13. The only difference being that, the traces were probed using microprobes instead of connectors. All samples were analyzed using TDR measurements and were proved to be nearly 50Ω.

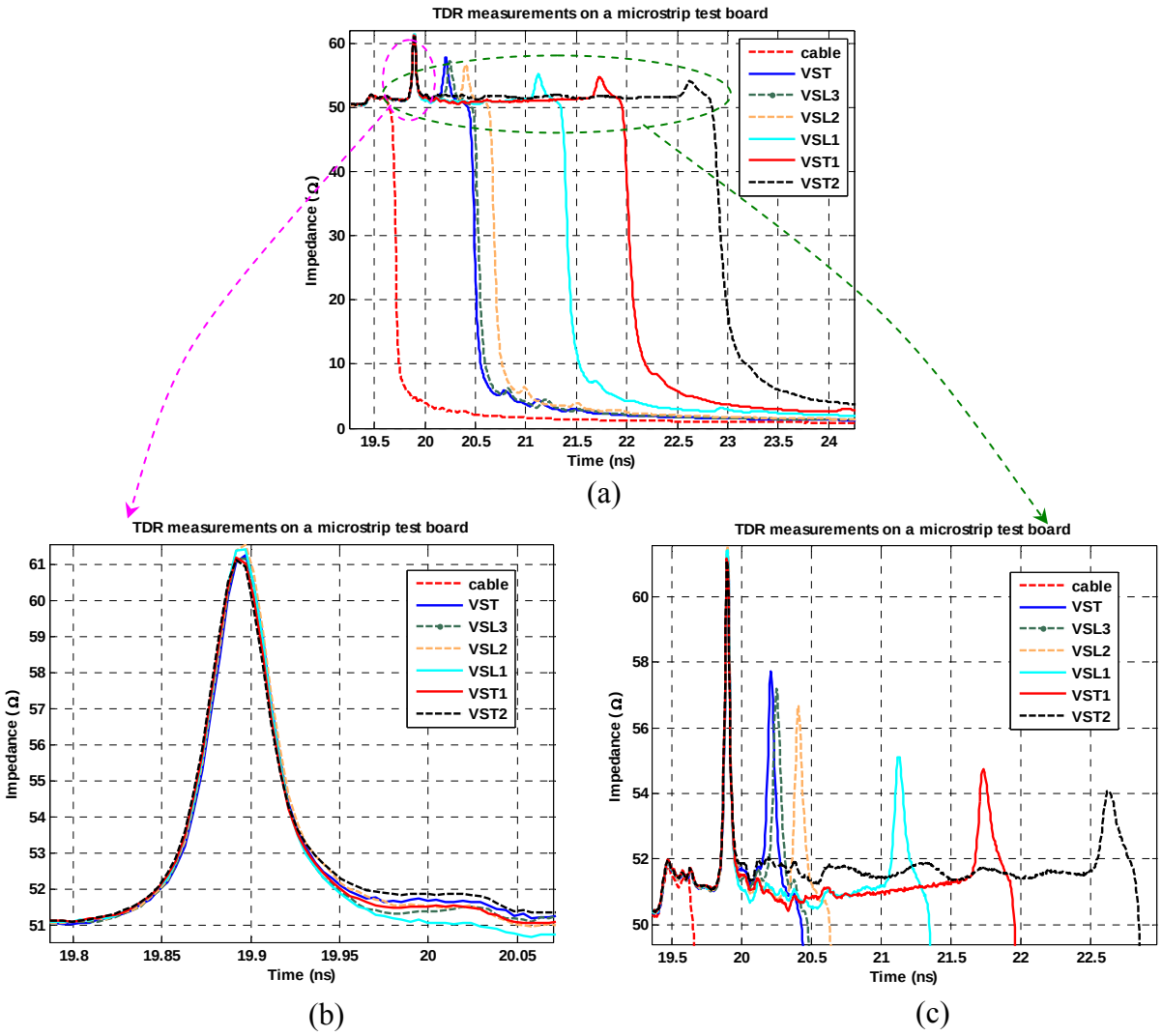


Figure 2.33. Impedance measurements on microstrip board. (a) TDR Impedance measurement along the trace length (b) Inductive connector discontinuity (c) Enlarged view of impedance variation along the trace.

2.2.5. Comparison and Analysis. Measurements were taken on 32 different samples and the results were compared. Figure 2.30 and Figure 2.31 gives the comparison of measurements on trace VST2 for all the sample boards analyzed. Several different sanity checks were done as discussed earlier, to ensure that the measurement results were reasonable.

As a common practice, before measurements, all the traces were cleaned with Isopropyl alcohol swabs. After several measurement cycles, dust particles gets deposited on the surface of the board. It was important to make sure that this does not pose any change in measurement results. So, the effects of cleaning were also studied on one of the samples. Figure 2.34 shows the comparison of measurements before and after cleaning.

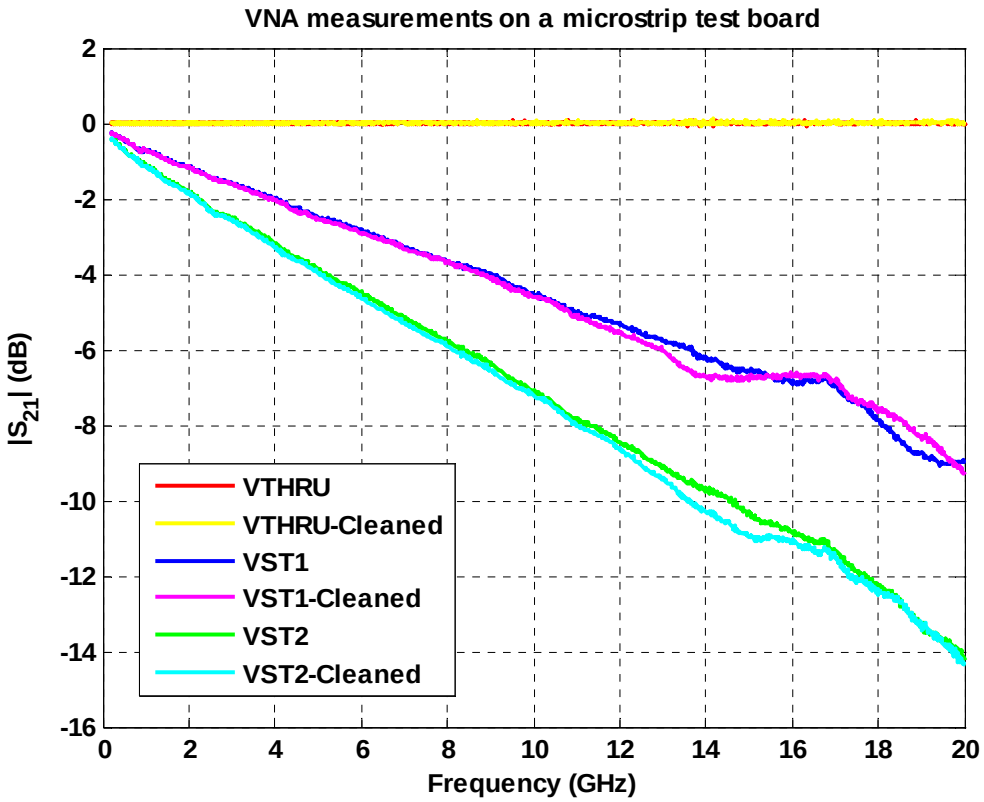


Figure 2.34. $|S_{21}|$ measurement comparison before and after cleaning the trace surface.

From Figure 2.34, it is clear that not much of difference was seen when the board was cleaned or not cleaned. This shows that small amount of dust deposition on the surface of the trace would not really affect the measurement results. But, the practice of cleaning the boards before measurements was continued as a part of measurement protocol.

Variation of trace width along a trace is inevitable because perfect traces could not be produced because of manufacturing limitations. But, this trace width could change the characteristic impedance significantly as discussed in Section 2.2.1. TDR measurements were taken to study this effect. But this information does no provide us the variation in width in particular. So, width measurements were taken at different locations of the trace using a high resolution, HIROX microscope. Table 2.4 shows the measurement results.

Table 2.4. HIROX measurements for width variation along a trace.

#(From Port 1)	Width(mils)	Impedance
1	9.968	51.772
2	9.926	51.904
3	9.863	52.104
4	9.841	52.174
5	9.776	52.382
6	9.883	52.040
7	9.345(small break)	53.809
8	9.669	52.729
9	9.757	52.443
10	9.694	52.647
11	9.694	52.647
12	9.715	52.579
13	9.482	53.347
14	9.546	53.133
15	9.715	52.579

From Table 2.4, it is clear that the impedance was varying by a small amount because of the variation in width. But, it is evident that not much change in impedance is seen in any case. However, reading #7 in Table 2.4 had a small break in the trace which reduced the width much less than the other readings. These made the impedance go as high as 54Ω. TDR measurements were also taken to verify the discontinuities along a trace which was discussed in Section 2.2.4. These measurements were much easier to make sure that there were no significant discontinuities along the trace. From this study, it was concluded that even though the trace width varies, it was not significant enough to change the impedance by large values. So, the results were not affected.

Similar analysis done in Section 2.1.4 was also done for the microstrip test boards. It is important to make sure that the non-ideality of two ports is not evident in the measurement results. Figure 2.34 shows the effects of manually switching the ports. Both ports look different in a TDR, which clearly demonstrates of the non-ideality of the ports. Figure 2.35 shows that the difference is not huge after manually shifting the ports. This effect was taken off in part when TRL calibration was done.

Another factor which affected the impedance of the trace was the thickness of the trace. According to process variations, the surface of the copper will never be flat. It will have a certain surface roughness associated with the manufacturing process. So, measurements were taken using a Profilometer to see how much variation in thickness is seen on a typical test board. Table 2.5 shows the average value of thickness across the trace, for the vertical “Thru” trace in a sample test board. The tip of the Profilometer measures the roughness of the trace along the dashed line in Figure 2.36. Measurements were taken at different locations and are shown in Table 2.5.

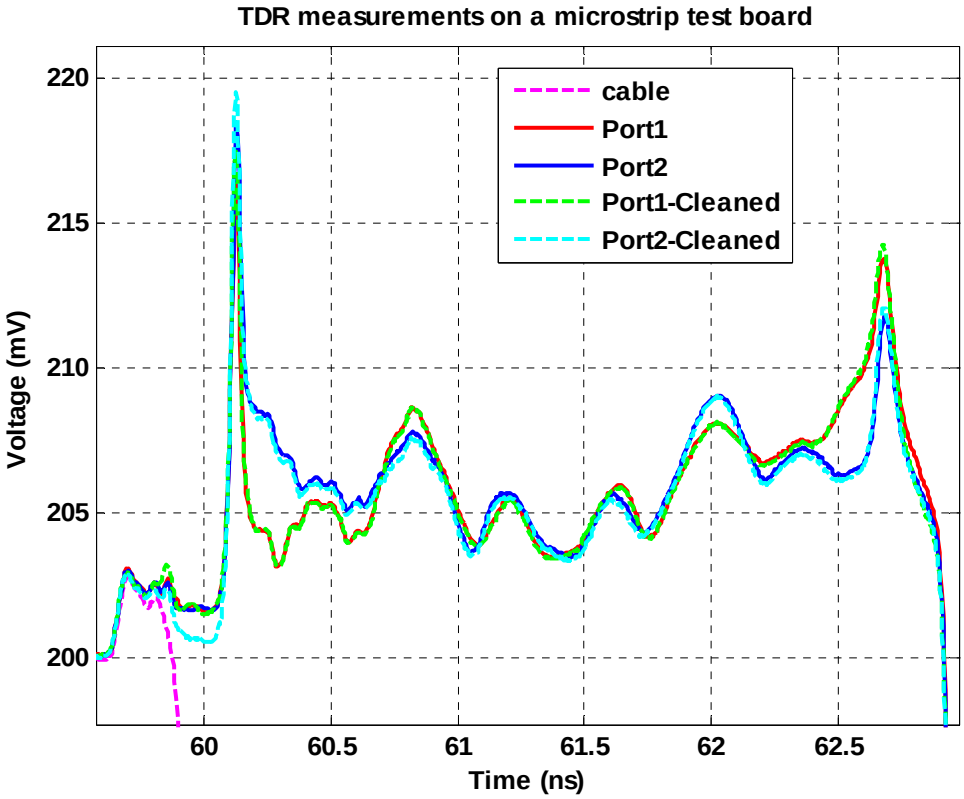


Figure 2.35. TDR measurements after manual switching of ports and also the comparison before and after cleaning the trace surface.

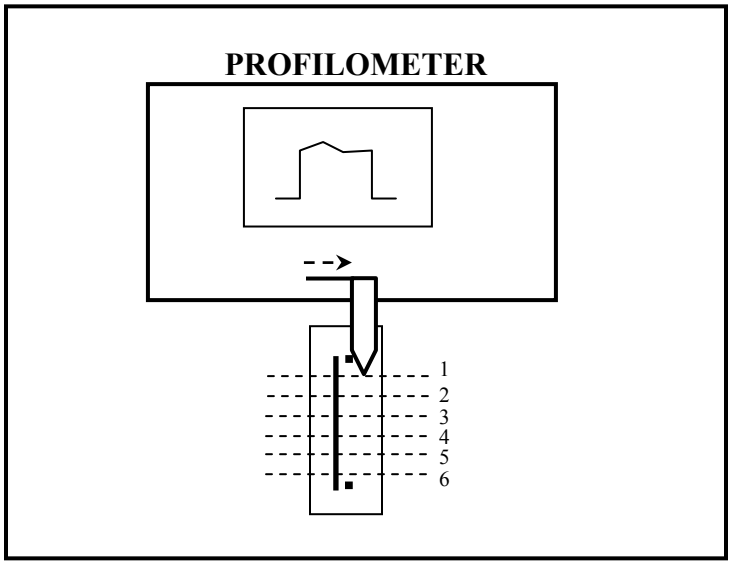


Figure 2.36. Surface roughness measurement using Profilometer.

Table 2.5. Profilometer measurements for surface roughness along a trace.

S.No	Thickness(μm)	Thickness(mils)
1	35.55	1.326
2	34.23	1.277
3	36.04	1.345
4	36.06	1.345
5	36.12	1.348
6	36.26	1.353

Measurements on the same location produced an error of about ±1.5μm (±0.056mils). So, the measurement was not accurate enough to measure the surface roughness along the dashed line. The average value along the width of the trace was taken. From Table 2.5, the surface roughness won't affect the thickness of the trace much and it won't be affecting the measurements significantly.

One of the samples tested had an extra via in the "Open" Standard as shown in Figure 2.37.

Open standard (Incorrect)
(Extra via)
(a)

Open standard (Correct)
for TRL Calibration
(b)

Figure 2.37. Geometry of "Open" standard. (a) Extra via error made on a sample board. (b) Correct geometry for a "Open" calibration standard (without the via at one end).

The purpose of this analysis was to study the effects of the extra via on the calibration standard. Calibration and measurements were done on the board with via.

Measurements were also taken after milling out via using a milling machine. Figure 2.38 shows the comparison of measurements with and without via. The results indicate that the added via was not showing much effect on the measurements.

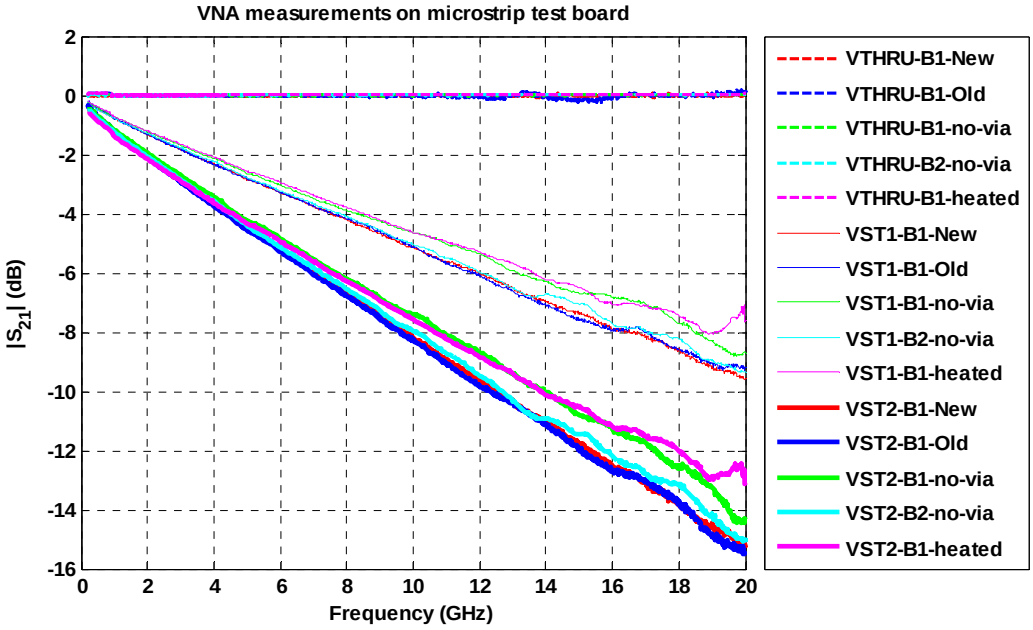
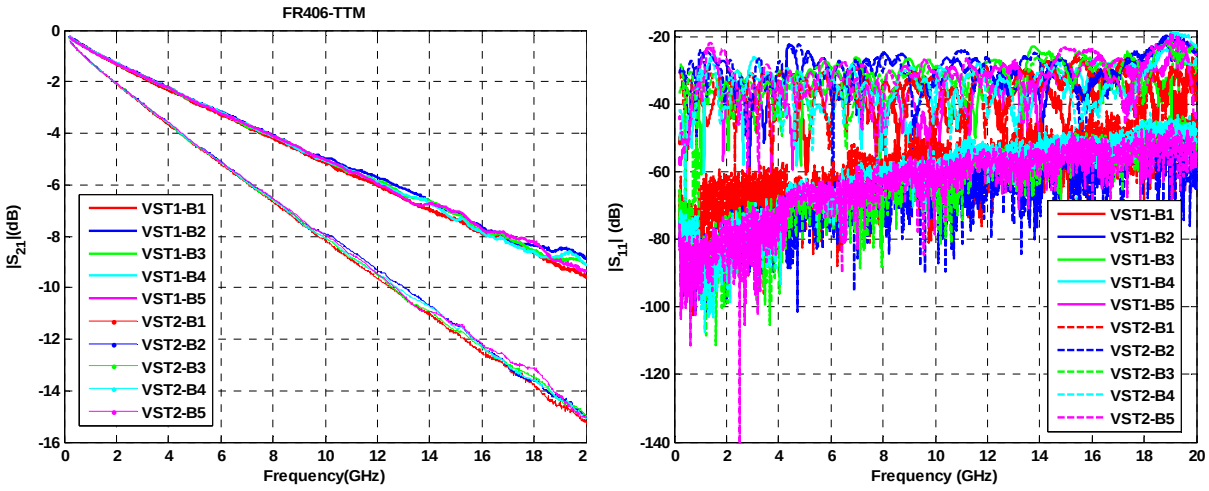


Figure 2.38. Comparison of $|S_{21}|$ with and without via in the "Open" standard.

A sample board was heated up to 150^{o}C for 4 hours in an oven to remove the moisture off the board. Calibration and measurements were done and compared with old measurements. The comparison is shown in Figure 2.38. Even after heating the samples, much difference is not observed in measurement results.

Five samples of same material from the same supplier were chosen for accuracy analysis. Even though the samples were different, the material and construction for all samples are same. So, ideally the measurements should show the same $|S_{21}|$ and $|S_{11}|$. Figure 2.39 shows the measurement results for trace VST, VST1 and VST2. They all

match very well. This proved that the measurement results and calibration coefficients would be comparable even when measured using different samples of the same board.



(a) (b)

Figure 2.39. Measurement comparison for five samples of same material. (a) $|S_{21}|$ measurements of all samples of same material. (b) $|S_{11}|$ measurements of all samples of same material.

2.2.6. Extracted Results. S-parameter measurements were taken. TDR measurements were done to observe the discontinuities along the trace. Calibration standards were measured to see if the range of $|S_{21}|$ and $|S_{11}|$ are in acceptable limits as discussed in Section 2.2.4. The test traces were measured using VNA and $|S_{11}|$ was checked to see if it is in acceptable limits as discussed in Section 2.2.4. After the sanity checks were done, it was used for the extraction procedure explained in Section 2.2.2. For the data used for the extraction procedure, the Curve-fitting method was chosen. The benefits of using the Curve-fitting method were also analyzed in Section 2.2.2. Figure 2.40 shows the dielectric constant values as a function of frequency for all the material

samples that were analyzed. Figure 2.41 shows the loss tangent values as a function of frequency for all the material samples that were analyzed. The materials that were used for the test boards were variants of FR-4 material. They were different based on their resin content. Figure 2.40 shows that the dielectric constant varies from 4.4 to 4.6 for different FR-4 materials. Figure 2.41 shows that the loss tangent varies from 0.005 to 0.03 for different FR-4 materials. Loss tangent is almost seen constant over the entire frequency range. But, dielectric constant does vary with frequency. It is high at low frequencies and reduces and settles down at higher frequencies. The physics underlying the behavior of dielectric constant and loss tangent with frequency is beyond the scope of this thesis.

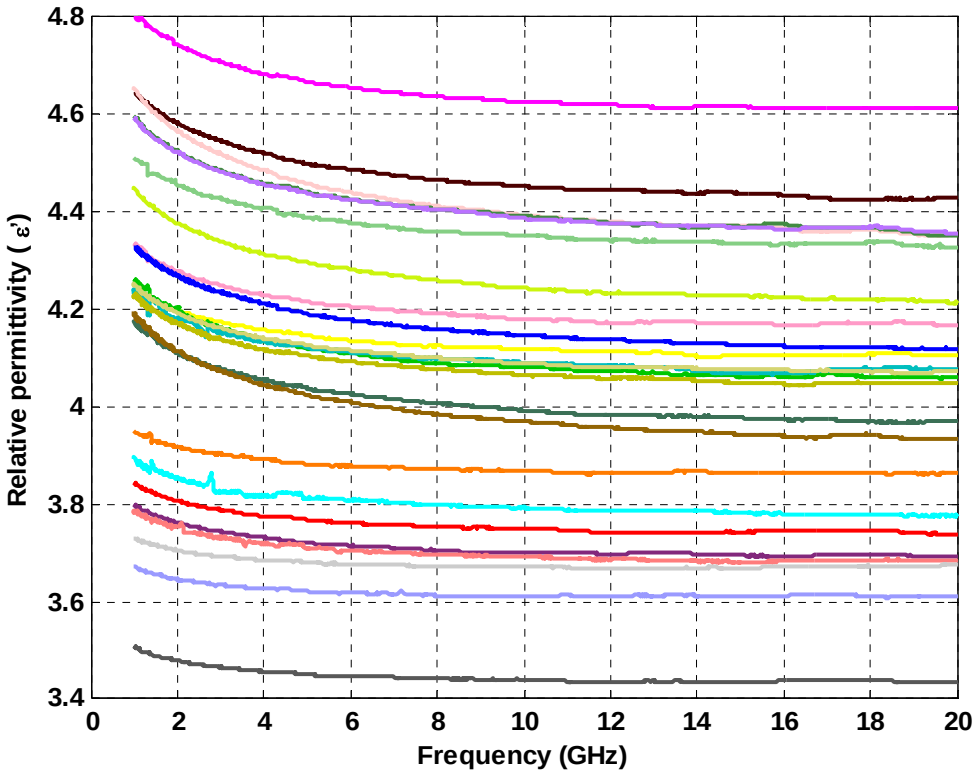


Figure 2.40. Comparison of dielectric constant for all the samples tested.

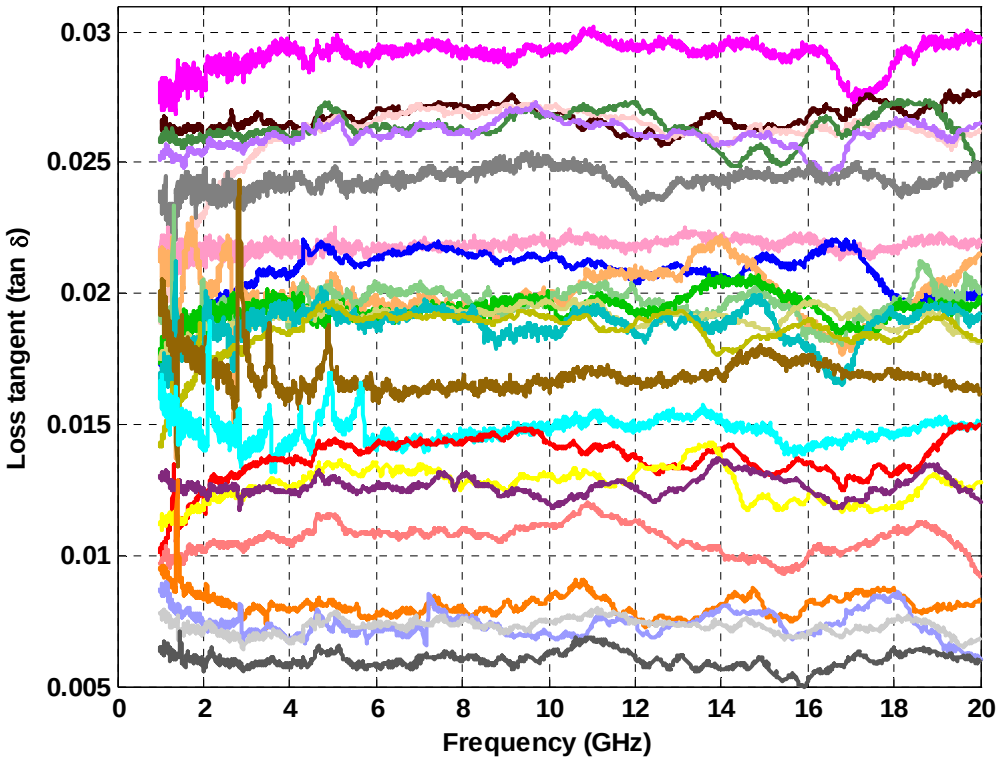


Figure 2.41. Comparison of loss tangent for all the samples tested.

With the information of the extracted results, it is possible to do accurate signal integrity analysis where material properties are not just considered as constants but as functions varying with frequency. This will help to provide accurate modeling strategies for full wave modeling. This could significantly influence the signal link path budget. With the information obtained, decisions could be made on choosing the appropriate material for the particular application when designers will have to trade-off quality for cost.

3. ROOT IMPULSE ENERGY (RIE) LOSS

Loss characterization is always preferred to be done in frequency domain because the loss information is embodied in information rich S-parameters from a Vector Network Analyzer (VNA). Also, dielectric properties of a material are frequency dependant parameters. But, VNA is a very costly equipment and measurement procedure is complicated to be used in board houses for quick measurements. Board houses which manufacture such boards require an easy robust technique to characterize losses so that they can provide a good estimate of the losses to its supplier.

Time Domain Reflectometer (TDR), is a time domain equipment which sends out a pulse to a device under test and measures the reflected signal. It is less costly when compared to VNA and could be easily used in board houses for measurements. So, this is the motivation of the technique discussed in this Section is to build a time domain technique to characterize losses easily and produce a single valued number for losses which is representative of the entire frequency range under consideration. TDR losses have shown correlation to VNA measurements, but have a much simpler representation which is more suitable to specification and ease of measurement.

The observed edge of a TDR waveform is related to energy lost in the transmission line attached to the TDR unit. The intent of Root Impulse Energy (RIE) loss is to represent losses as a single valued energy loss of a transmission line on a printed circuit board (PCB) which is representative of its losses as a function of frequency. A step signal is injected into the transmission line. Energy is lost as the wave travels through the transmission line. The loss characteristics of a transmission line can be

determined by comparing the RIE of the injected wave to the RIE of the reflected wave. This is called RIE loss.

First, a time domain technique is defined in this Section and then a frequency domain technique is analyzed, both analytical and measurement wise, on a stripline structure. This was done to compare the RIE loss numbers with the standard VNA measurements and correlate to see how well they agree.

3.1. TIME DOMAIN CHARACTERIZATION

One of Newton's fundamental laws of physics states that "energy must be conserved." This is true for systems viewed in the both the time and frequency domain because, frequency domain is nothing but a mathematical manipulation of numbers to allow easier solutions to everyday problems. To satisfy conservation, the energy can be transmitted, reflected, radiated, or absorbed and turned into heat. The energy not delivered to the load is considered lost. The loss can be measured as a ratio of received (Rx) energy to the injected (In) energy.

Insertion loss is a parameter that is roughly the square root of the ratio of received energy to injected energy and is a function of frequency. Since loss is not a single value, it is difficult and complicated to specify it, in terms of limits. The purpose of the RIE method is to define a single energy loss value as a quality factor. Insertion loss, S_{21} is,

$$S_{21} \approx \sqrt{\frac{V_{rx}}{V_{in}}} . \tag{3.1}$$

where the received and injected voltages are functions of frequency. The purpose of this method is to define and utilize a single energy loss value, called the Root Impulse Energy (RIE) loss.

From an electrical perspective, energy is simply product of voltage, current, and time. Considering that the measurement equipment source impedance and load impedance is 'R', Ohm's law reveals the following

$$E = \frac{V^2}{R} * T \,. \tag{3.2}$$

Total energy is the integral of (3.2) over time.

$$E = \int \frac{V(t)^2}{R} * dt \,. \tag{3.3}$$

With (3.3), it is possible to define the RIE loss as a ratio of the received energy with the injected energy.

$$RIE_{loss} = \frac{E_{rx}}{E_{in}} = \frac{\sqrt{\int V_{rx}(t)^2 * dt}}{\sqrt{\int V_{in}(t)^2 * dt}} \,. \tag{3.4}$$

The above equation (3.4) shows the RIE loss associated with a single trace with injected and received energies. But, this RIE loss includes losses in edges, cables, launch pad, and a small section of transmission line. To calculate the energy loss of just the trace, those effects should be omitted. So, a calibration trace is used, which is only shorter than the original test trace. Then with the ratio of energies of the test trace to the calibration trace, it is possible to get the RIE loss number and the unwanted effects are also eliminated.

An impulse response is required to encompass the widest possible frequency range so that all the energy associated with the trace is considered. TDR utilizes a step response. Differentiating the step response would yield an impulse response.

Therefore, considering the impulse response in the RIE loss (in dB) expression, the following expression (3.5) is derived.

$$RIE_{loss\_dB} = 10 * \log\left(\frac{\sqrt{\int\left(d\frac{V_{test\_tdr}(t)}{dt}\right)^2 * dt}}{\sqrt{\int\left(d\frac{V_{cal\_tdr}(t)}{dt}\right)^2 * dt}}\right) = 10 * \log\left(\frac{IE_{test}}{IE_{cal}}\right). \quad (3.5)$$

3.2. FRQUENCY DOMAIN CHARACTERIZATION

RIE loss in dB can be also be calculated by a frequency domain technique. This can be considered as a standard to compare with the time domain technique because the frequency domain measurements are accurate. The S_{21} parameter obtained from the VNA can be used to calculate the RIE_{loss_dB} with the following equation

$$RIE_{loss\_dB} = 20 * \log\left(\frac{\sqrt{\int\left|S_{21test\_vna}\right|^2 * df}}{\sqrt{\int\left|S_{21cal\_vna}\right|^2 * df}}\right) = 10 * \log\left(\frac{IE_{test}}{IE_{cal}}\right). \quad (3.6)$$

To understand this, it becomes important to consider S-parameters of a two port network [7]. Figure 3.1 shows the power across two ports. The parameters in Figure 3.1 can be explained as, $|a_i|^2$ = power wave traveling towards the two-port gate; $|b_i|^2$ = power wave reflected back from the two-port gate; and $|S_{21}|^2$ = power transmitted from port2 to port1.

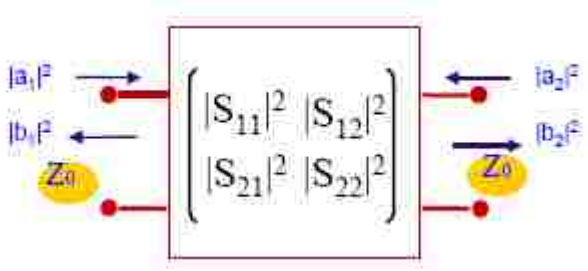


Figure 3.1. S-parameter block of a two port network.

So, the definition of insertion loss S_{21} is

$$\left|S_{21}\right|^2 = \frac{\left|b_2\right|^2}{\left|a_1\right|^2},\ where\ \left|a_2\right|^2 = 0\,. \tag{3.7}$$

Therefore, to get the total energy transmitted from port2 to port1 could be obtained by integrating (3.7) over the entire frequency range.

$$E = \int \left|S_{21}\right|^2 * df\,. \tag{3.8}$$

So, considering the calibration trace and the test trace, the Root Impulse Energy loss is the ratio of both energies which is shown in the following equation

$$RIE_{loss} = \sqrt{\frac{\int \left|S_{21test}\right|^2 * df}{\int \left|S_{21cal}\right|^2 * df}}\,. \tag{3.9}$$

Therefore, the RIE loss in dB can be expressed as

$$RIE_{loss\_dB} = 10 * \log\left(\sqrt{\frac{\int \left|S_{21test}\right|^2 * df}{\int \left|S_{21cal}\right|^2 * df}}\right). \tag{3.10}$$

(3.10) can also be represented as

$$RIE_{loss\_dB} = 10 * \log\left(\frac{\sqrt{\int \left|S_{21test}\right|^2 * df}}{\sqrt{\int \left|S_{21cal}\right|^2 * df}}\right) = 10 * \log\left(\frac{IE_{test}}{IE_{cal}}\right). \tag{3.11}$$

3.3. ANALYTICAL EXPRESSION ANALYSIS OF RIE LOSS FOR STRIPLINE

To better understand RIE loss definition, a stripline structure was chosen for analysis. In later sections, RIE loss would be derived from basic principles of losses in a transmission line. Losses will be represented in terms of frequency by selecting a particular configuration of stripline structure.

3.3.1. Description of the Geometry and Losses. Stripline geometry was chosen for analyzing the RIE loss. Figure 3.2 shows the general stripline stack up. A stripline test board was already developed for material extraction study which was discussed in Section 2. Same geometry was chosen for this analysis too. Table 3.1 gives the geometry parameters used for the stripline test board.

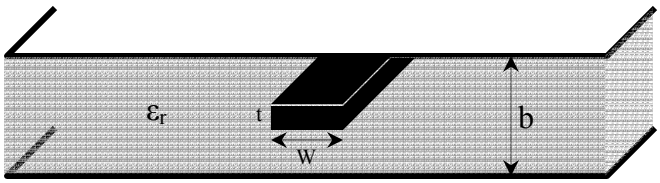


Figure 3.2. Stripline geometry chosen for RIE loss calculations.

The dielectric constant and loss tangent were extracted using the technique explained in Section 2. Even though they are dependent on frequency, mean values were chosen for the purpose of calculation.

Table 3.1. Geometry parameters used for the stripline test board.

W	12.05 mils
b	28.9 mils
t	1.2 mils
ε_r	3.8
tan δ	0.017

The losses associated with a transmission line were derived from basic voltage equations. For a transmission line with characteristic impedance, Zo and reflection coefficient, Γ, the voltage at any length (l) is given by the equation

$$V(l) = V_0(1+\Gamma)e^{-\gamma l}. \tag{3.12}$$

Assuming that there is no reflection, (Γ) = 0, i.e. when the load is matched, then

$$\frac{V(l)}{V_0} = e^{-\gamma l}. \tag{3.13}$$

But, the insertion loss can be represented using (3.14).

$$\frac{V(l)}{V_0} = \text{Transmission coefficient } (S_{21}). \tag{3.14}$$

Therefore, from Equations (3.13) and (3.14)

$$S_{21}(l) = e^{-\gamma l}. \tag{3.15}$$

where 'γ' is the propagation constant and 'l' is the length of the transmission line. But, propagation constant can be represented as

$$\gamma = \alpha + j\beta. \tag{3.16}$$

where 'α' is the total loss of the transmission line and 'β' is the phase constant. Therefore, (3.15) could be written as

$$S_{21}(l) = e^{-(\alpha+j\beta)l}. \tag{3.17}$$

$$S_{21}(l) = e^{-\alpha l}.e^{-j\beta l}. \tag{3.18}$$

The magnitude of (3.18) is shows as

$$\left|S_{21}(l)\right| = e^{-\alpha l}. \tag{3.19}$$

Squaring (3.19) would provide

$$\left|S_{21}(l)\right|^2 = e^{-2\alpha l}. \tag{3.20}$$

But, attenuation is due to dielectric (α_d) and conductor losses (α_c). Therefore, the total attenuation (α) is

$$\alpha = \alpha_d + \alpha_c . \tag{3.21}$$

3.3.2. Attenuation Due to Dielectric Loss (α_d). Assuming TEM mode of wave propagation, the dielectric loss can be expressed the following way[7]

$$\alpha_d = \frac{k \tan \delta}{2}. \tag{3.22}$$

where 'k' is the wave number and is given by

$$k = \frac{\omega \sqrt{\varepsilon_r}}{c}. \tag{3.23}$$

3.3.3. Attenuation Due to Conductor Loss (α_c). For the stripline geometry, closed form expressions are derived for conductor loss using perturbation method. This is because conductor loss is just a function of geometry and it depends upon skin effect losses [7]. Assuming TEM mode of wave propagation, the impedance of the transmission line can be approximated using the following expression

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_r}} \frac{b}{W_e + 0.441b}. \tag{3.24}$$

where

$$\frac{W_e}{b} = \frac{W}{b} - \begin{cases} 0. & for\ \frac{W}{b} \rangle 0.35. \\ (0.35 - W/b)^2. & for\ \frac{W}{b} \langle 0.35. \end{cases} \tag{3.25}$$

When designing stripline circuits, one needs to find the stripline width, given the characteristic impedance with inverse formulas. Such formula is derived as

$$\frac{W}{b} = \begin{cases} x. & for\ \sqrt{\varepsilon_r} Z_0 \langle 120. \\ 0.85 - \sqrt{0.6 - x}. & for\ \sqrt{\varepsilon_r} Z_0 \rangle 120. \end{cases} \tag{3.26}$$

where

$$x = \frac{30\pi}{\sqrt{\varepsilon_r} Z_0} - 0.441. \tag{3.27}$$

The attenuation due to conductor loss can be approximated for the stripline geometry using perturbation method or Wheeler's incremental inductance rule [7]. The approximated result is

$$\alpha_c = \begin{cases} \dfrac{2.7 \times 10^{-3} R_s \varepsilon_r Z_0}{30\pi(b-t)} A. & for\ \sqrt{\varepsilon_r} Z_0 \langle 120. \\ \dfrac{0.16 R_s}{Z_0 b} B. & for\ \sqrt{\varepsilon_r} Z_0 \rangle 120. \end{cases} \tag{3.28}$$

where A and B is

$$A = 1 + \frac{2W}{b-t} + \frac{1}{\pi}\frac{b+t}{b-t}\ln\left(\frac{2b-t}{t}\right). \tag{3.29}$$

$$B = 1 + \frac{b}{(0.5W + 0.7t)}\left(0.5 + \frac{0.414t}{W} + \frac{1}{2\pi}\ln\frac{4\pi W}{t}\right). \tag{3.30}$$

3.3.4. Losses in Terms of Frequency for the Selected Stripline Structure. Substituting dimensions and values shown in Table 3.1, in (3.22), the dielectric loss can be written in terms of frequency as

$$\alpha_d = (3.468 \times 10^{-10})\, f\ . \tag{3.31}$$

Substituting dimensions and values shown in Table 3.1, in (3.24), the impedance of the transmission line was calculated as

$$Z_0 = 55.2\Omega\,. \tag{3.32}$$

Substituting dimensions in (3.28), the conductor loss can be calculated in terms of frequency as

$$\alpha_c = (7.31\times10^{-6})\sqrt{f}\,. \tag{3.33}$$

Therefore, total attenuation is obtained by substituting (3.31) and (3.33), in (3.21)

$$\alpha = \left\{(3.468\times10^{-10})\,f\right\} + \left\{(7.31\times10^{-6})\sqrt{f}\right\}. \tag{3.34}$$

This equation was programmed in MATLAB and the attenuation was plotted with varying frequency. Figure 3.3 shows the loss curves and gives an idea about the cross-over point. Cross over point occurs when

$$\alpha_d = \alpha_c\,. \tag{3.35}$$

Therefore,

$$(3.468\times10^{-10})\,f = (7.31\times10^{-6})\sqrt{f}\,. \tag{3.36}$$

Evaluating (3.36) gives the frequency where cross-over point occurs

$$f = 444.3MHz\,. \tag{3.37}$$

From this cross-point study, it is clear that the dielectric loss dominates conductor loss at low frequencies. Therefore, it is meaningful to consider this geometry for loss characterization.

3.3.5. Derivation of Analytical Expression for RIE Loss. From the above sections, the conductor loss and dielectric loss were calculated for the stripline test board. Now it is possible to substitute (3.34) in (3.20).

$$\left|S_{21}(l)\right|^2 = e^{-2l\left\{\left((3.468\times10^{-10})\,f\right)+\left((7.31\times10^{-6})\sqrt{f}\right)\right\}}\,. \tag{3.38}$$

Integrating (3.38) over frequency

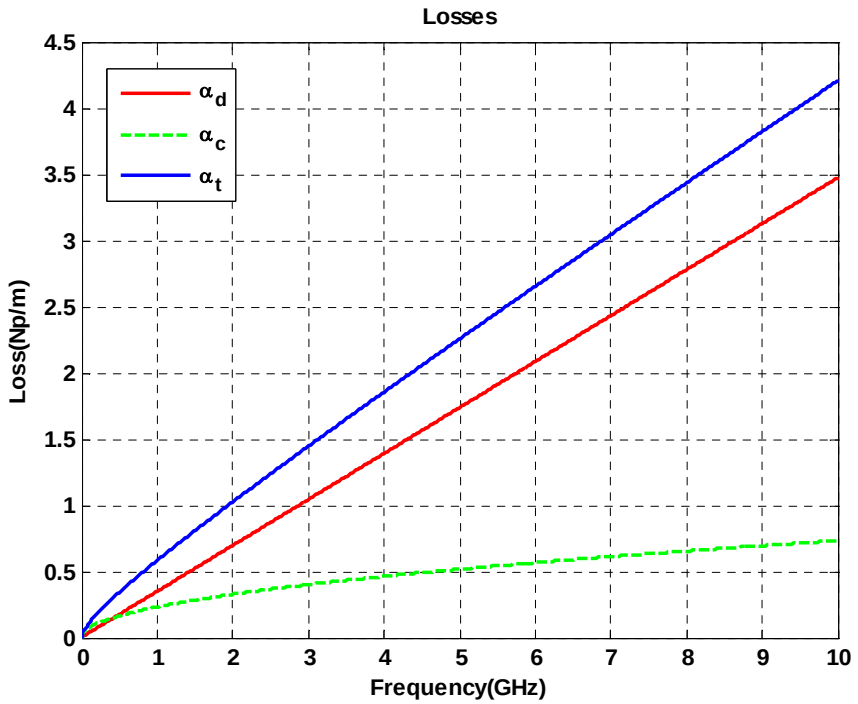


Figure 3.3. Loss curves plotted from loss equation for the stripline test board.

$$\int \left|S_{21}(l)\right|^2 df = \int e^{-2l\left\{\left((3.468\times10^{-10})f\right)+\left((7.31\times10^{-6})\sqrt{f}\right)\right\}} df \,. \tag{3.39}$$

Equating the constants to a and b

$$a = 3.468\times10^{-10}. \tag{3.40}$$

$$b = 7.31\times10^{-6}. \tag{3.41}$$

Then the solution to the integral in (3.39) would be

$$\int e^{-2l(af+b\sqrt{f})} df = -\left[\frac{be^{\frac{b^2 l}{2a}}\sqrt{\frac{\pi}{2}} \bullet erf\left(\frac{\sqrt{l}\left(2\sqrt{f}a+b\right)}{\sqrt{2a}}\right)}{2a^{\frac{3}{2}}\sqrt{l}}\right] - \left[\frac{e^{\left(-2afl-2b\sqrt{fl}\right)}}{2al}\right]. \tag{3.42}$$

where the error function can be evaluated as

$$erf(x)=\frac{2}{\sqrt{\pi}}\sum_{n=0}^{\infty}\left(\frac{(-1)^n x^{2n+1}}{n!(2n+1)!}\right) \tag{3.43}$$

So, calculating the RIE loss using (3.11)

$$\frac{\sqrt{\int_{f_1}^{f_2}\left|S_{21}(l_{test})\right|^2 df}}{\sqrt{\int_{f_1}^{f_2}\left|S_{21}(l_{cal})\right|^2 df}}=\frac{\sqrt{-\left[\frac{be^{\left(\frac{b^2 l_{test}}{2a}\right)}\cdot\sqrt{\frac{\pi}{2}}\cdot erf\left(\frac{\sqrt{l_{test}}\left(2\sqrt{f_2}a+b\right)}{\sqrt{2a}}\right)}{2a^{\frac{3}{2}}\sqrt{l_{test}}}\right]-\left[\frac{e^{-2af_2 l_{test}-2b\sqrt{f_2}l_{test}}}{2al_{test}}\right]}+\left[\frac{be^{\left(\frac{b^2 l_{test}}{2a}\right)}\cdot\sqrt{\frac{\pi}{2}}\cdot erf\left(\frac{\sqrt{l_{test}}\left(2\sqrt{f_1}a+b\right)}{\sqrt{2a}}\right)}{2a^{\frac{3}{2}}\sqrt{l_{test}}}\right]+\left[\frac{e^{-2af_1 l_{test}-2b\sqrt{f_1}l_{test}}}{2al_{test}}\right]}}{\sqrt{-\left[\frac{be^{\left(\frac{b^2 l_{cal}}{2a}\right)}\cdot\sqrt{\frac{\pi}{2}}\cdot erf\left(\frac{\sqrt{l_{cal}}\left(2\sqrt{f_2}a+b\right)}{\sqrt{2a}}\right)}{2a^{\frac{3}{2}}\sqrt{l_{cal}}}\right]-\left[\frac{e^{-2af_2 l_{cal}-2b\sqrt{f_2}l_{cal}}}{2al_{cal}}\right]}+\left[\frac{be^{\left(\frac{b^2 l_{cal}}{2a}\right)}\cdot\sqrt{\frac{\pi}{2}}\cdot erf\left(\frac{\sqrt{l_{cal}}\left(2\sqrt{f_1}a+b\right)}{\sqrt{2a}}\right)}{2a^{\frac{3}{2}}\sqrt{l_{cal}}}\right]+\left[\frac{e^{-2af_1 l_{cal}-2b\sqrt{f_1}l_{cal}}}{2al_{cal}}\right]}} \tag{3.44}$$

Therefore, the RIE loss in dB can be calculated as

$$RIE_{loss\_dB} = 5 \bullet \log \left[\begin{array}{l} - \left[\dfrac{be^{\left(\frac{b^2 l_{test}}{2a}\right)} \bullet \sqrt{\dfrac{\pi}{2}} \bullet erf\left(\dfrac{\sqrt{l_{test}}\left(2\sqrt{f_2}a + b\right)}{\sqrt{2a}} \right)}{2a^{\frac{3}{2}}\sqrt{l_{test}}} \right] - \left[\dfrac{e^{-2af_2 l_{test} - 2b\sqrt{f_2} l_{test}}}{2al_{test}} \right] \\ + \left[\dfrac{be^{\left(\frac{b^2 l_{test}}{2a}\right)} \bullet \sqrt{\dfrac{\pi}{2}} \bullet erf\left(\dfrac{\sqrt{l_{test}}\left(2\sqrt{f_1}a + b\right)}{\sqrt{2a}} \right)}{2a^{\frac{3}{2}}\sqrt{l_{test}}} \right] + \left[\dfrac{e^{-2af_1 l_{test} - 2b\sqrt{f_1} l_{test}}}{2al_{test}} \right] \end{array} \right]$$

$$- 5 \bullet \log \left[\begin{array}{l} - \left[\dfrac{be^{\left(\frac{b^2 l_{cal}}{2a}\right)} \bullet \sqrt{\dfrac{\pi}{2}} \bullet erf\left(\dfrac{\sqrt{l_{cal}}\left(2\sqrt{f_2}a + b\right)}{\sqrt{2a}} \right)}{2a^{\frac{3}{2}}\sqrt{l_{cal}}} \right] - \left[\dfrac{e^{-2af_2 l_{cal} - 2b\sqrt{f_2} l_{cal}}}{2al_{cal}} \right] \\ + \left[\dfrac{be^{\left(\frac{b^2 l_{cal}}{2a}\right)} \bullet \sqrt{\dfrac{\pi}{2}} \bullet erf\left(\dfrac{\sqrt{l_{cal}}\left(2\sqrt{f_1}a + b\right)}{\sqrt{2a}} \right)}{2a^{\frac{3}{2}}\sqrt{l_{cal}}} \right] + \left[\dfrac{e^{-2af_1 l_{cal} - 2b\sqrt{f_1} l_{cal}}}{2al_{cal}} \right] \end{array} \right]. \quad (3.45)$$

RIE loss number is dependent on the length of the transmission line. It varies based on the length. But, from (3.46) it is clear that a per unit length RIE loss number could not be obtained since length of both test and calibration traces are embedded in the expression. So, the following analysis was done to make the equation less complicated to bring the length factor out. From the loss curves in Figure 3.3 it is observed that dielectric loss is dominating after 400 MHz. It is prudent to assume that losses are only due to dielectric loss and now, RIE loss expression would be less complicated as shown below.

If α_d dominates,

$$\int_{f_1}^{f_2} \left|S_{21}(l)\right|^2 df = \int_{f_1}^{f_2} e^{-2l\alpha_d} df \ . \tag{3.46}$$

$$\int_{f_1}^{f_2} \left|S_{21}(l)\right|^2 df = \int_{f_1}^{f_2} e^{-2l\left(3.468\times10^{-10}\right)f} df \ . \tag{3.47}$$

Evaluating the integral in (3.47)

$$\int_{f_1}^{f_2} \left|S_{21}(l)\right|^2 df = \left(\frac{e^{-l\left(6.936\times10^{-10}\right)f_2}}{-l\left(6.936\times10^{-10}\right)}\right) - \left(\frac{e^{-l\left(6.936\times10^{-10}\right)f_1}}{-l\left(6.936\times10^{-10}\right)}\right). \tag{3.48}$$

Therefore, square root of (3.48) gives

$$\sqrt{\int_{f_1}^{f_2} \left|S_{21}(l)\right|^2 df} = \sqrt{\left(\frac{e^{-l\left(6.936\times10^{-10}\right)f_2}}{-l\left(6.936\times10^{-10}\right)}\right) - \left(\frac{e^{-l\left(6.936\times10^{-10}\right)f_1}}{-l\left(6.936\times10^{-10}\right)}\right)}. \tag{3.49}$$

To calculate RIE loss it is required to consider a test trace (l_{test}) and a calibration trace (l_{cal}). Then the expression for RIE loss would be

$$\frac{\sqrt{\int_{f_1}^{f_2} \left|S_{21}(l_{test})\right|^2 df}}{\sqrt{\int_{f_1}^{f_2} \left|S_{21}(l_{cal})\right|^2 df}} = \frac{\sqrt{\left(\frac{e^{-l_{test}\left(6.936\times10^{-10}\right)f_2}}{-l_{test}\left(6.936\times10^{-10}\right)}\right) - \left(\frac{e^{-l_{test}\left(6.936\times10^{-10}\right)f_1}}{-l_{test}\left(6.936\times10^{-10}\right)}\right)}}{\sqrt{\left(\frac{e^{-l_{cal}\left(6.936\times10^{-10}\right)f_2}}{-l_{cal}\left(6.936\times10^{-10}\right)}\right) - \left(\frac{e^{-l_{cal}\left(6.936\times10^{-10}\right)f_1}}{-l_{cal}\left(6.936\times10^{-10}\right)}\right)}}. \tag{3.50}$$

Further simplification of (3.50) and converting it to dB provides leads to

$$RIE_{loss\_dB} = 10\bullet\log\left(\sqrt{\frac{l_{cal}}{l_{test}}}\right) + 10\bullet\log\left(\sqrt{\frac{e^{-6.936\times10^{-10} f_2 l_{test}} - e^{-6.936\times10^{-10} f_1 l_{test}}}{e^{-6.936\times10^{-10} f_2 l_{cal}} - e^{-6.936\times10^{-10} f_1 l_{cal}}}}\right). \tag{3.51}$$

$$RIE_{loss\_dB} = 5\bullet\log\left(\frac{l_{cal}}{l_{test}}\right) + 5\bullet\log\left(\frac{e^{-6.936\times10^{-10} f_2 l_{test}} - e^{-6.936\times10^{-10} f_1 l_{test}}}{e^{-6.936\times10^{-10} f_2 l_{cal}} - e^{-6.936\times10^{-10} f_1 l_{cal}}}\right). \tag{3.52}$$

From (3.53) it is clear that, even now the length is embedded in the equation and it is impossible to extract a per unit length RIE loss parameter.

3.4. MEASUREMENTS AND RESULTS

From the previous section, three sets of comparisons were detailed to verify the RIE loss number: frequency domain method, time domain method and the analytical expression. Frequency domain measurements were made on the stripline test board with HP8270ES Network Analyzer and time domain measurements were done with Agilent Infiniium DCA 86100B. Analytical calculations were done in MATLAB.

3.4.1. Frequency Domain Measurements. Calibration is important for this study to quantify the loss of the trace and it is required to avoid effects of via, transitions etc. TRL calibration was used which was explained in Section 2.1.3. Three different frequency ranges were used and calibrated separately. Once calibration was done, measurements were taken on the traces shown in Table 3.2. The test board was the same as shown in Figure 2.5. And the test setup used was the same as the one shown in Figure 2.8. S-parameters of all the traces shown in Table 3.2 were measured and plotted for further analysis. Figure 3.4 shows the measurement results.

Table 3.2. Length of traces used in the stripline test board.

Traces	Length (inches)
SSL3 (Calibration)	0.125
SSL2 (Calibration)	0.579
SSL1 (Test)	2.679
ST1-2 (Test)	7.976

Among the traces, SSL3 and SSL2 are chosen as calibration traces because they are short. The test traces are SSL1 and ST1-2.

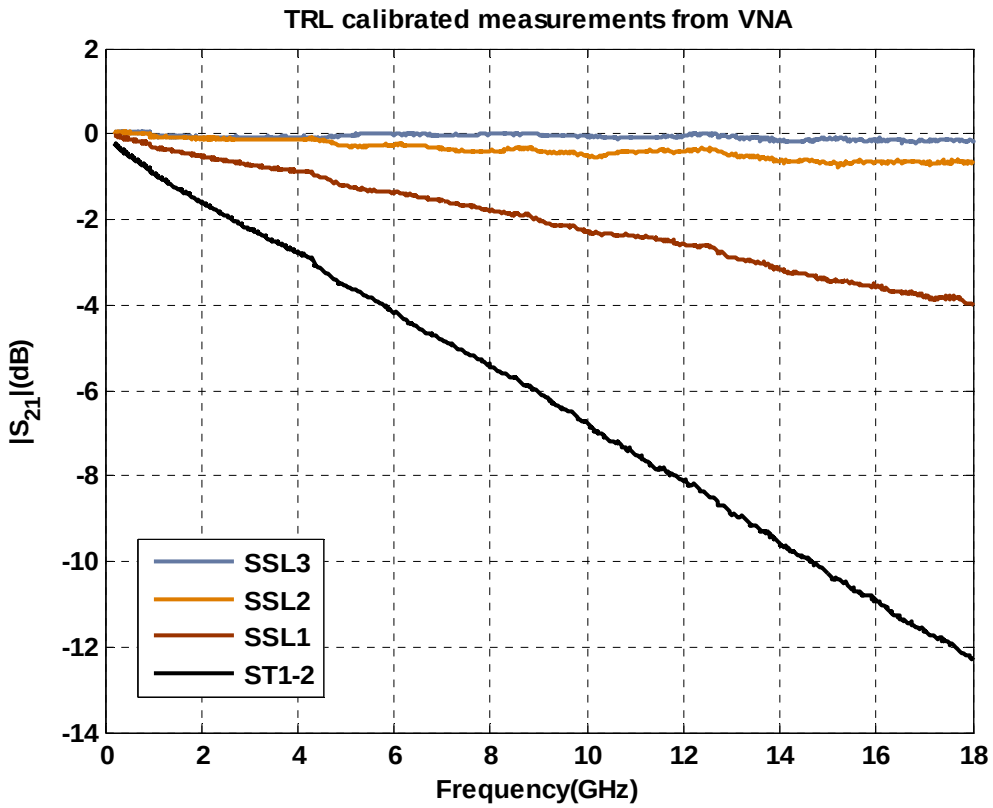


Figure 3.4. S-parameter measurements taken after doing TRL calibration.

Though the measurements were taken with three different frequency ranges, all the measurements were combined to span the entire frequency range.

3.4.2. Time Domain Measurements. Agilent TDR was used to make the time domain measurements. The test setup used is shown in Figure 3.5. The wide bandwidth oscilloscope had a TDR module which sends out a step signal through its output port. The signal traverses through the cable to the trace. The other end of the trace was kept open so

that the whole signal was reflected back because the reflection co-efficient was 1. This was measured back at the TDR module so the effective voltage seen at the oscilloscope would be twice the value of the signal send out. The bandwidth of the TDR was less than 12 GHz.

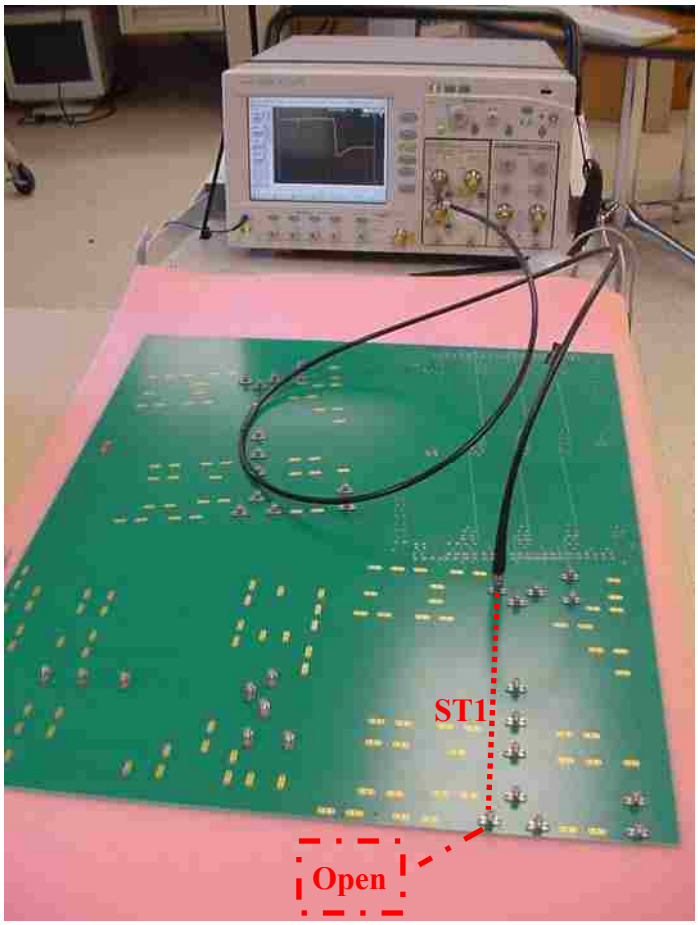


Figure 3.5. Test setup used to measure step response of the reflected wave.

The step response received after reflection was captured and saved. Figure 3.6 shows the measured results. All the traces mentioned in Table 3.2 were measured. The step response was averaged over 1000 averages to reduce noise. Several measurements

were taken with and without averages to understand the effect of averages on measurements. It was found out that the noise was reduced significantly with the use of averaging. Once the step response was obtained, the data was differentiated to get an impulse response. Figure 3.7 shows the impulse response of the measurements shown in Figure 3.6.

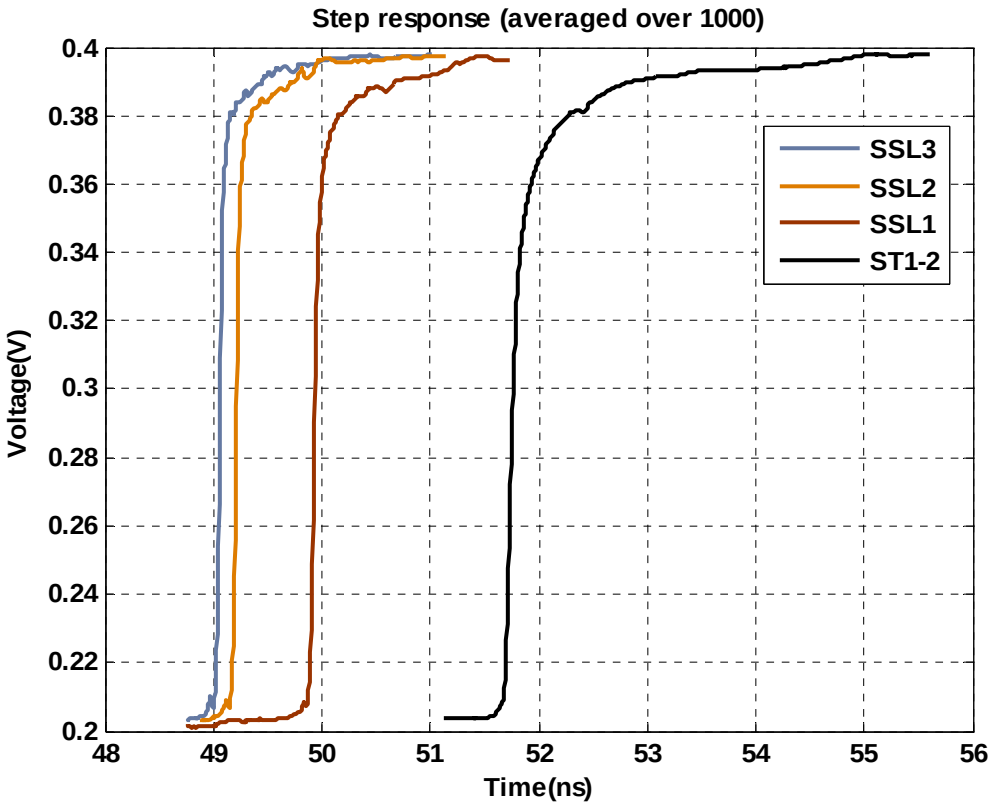


Figure 3.6. Measured TDR step response after reflection.

Root impulse energy is the area under the impulse response and could be found by integrating the impulse response over time. The range of integration did have an effect on the final results, but it was later proved that the effect of range of integration was

insignificant. If the data was really noisy, then the range of integration becomes important because the area under all those noisy segments will also be added up when integrated. But, with sufficient averaging, the noise was be filtered away which made the effect of range of integration insignificant.

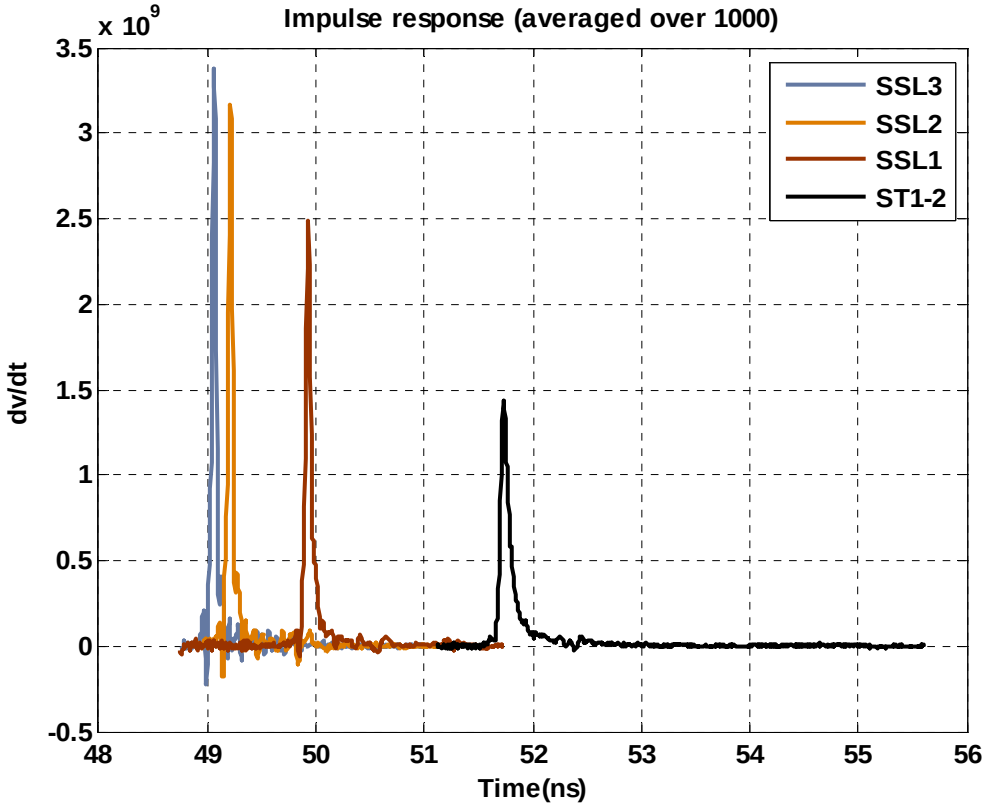


Figure 3.7. Impulse response obtained by differentiating the TDR step response.

3.4.3. RIE Loss Comparison and Analysis. Once the measurements were taken, the data was processed to calculate the RIE loss number. For the frequency domain measurements, (3.6) was used to calculate RIE loss number. (3.5) was used for time domain, and (3.45) was used for analytical calculation for RIE loss for this specific test

board. Table 3.3 shows the results and comparison for all the methods. From Table 3.3, it was observed that the results compare very well. Two sets of results were analyzed by taking two different calibration lengths, SSL3 and SSL2. The VNA and TDR RIE loss numbers match pretty well especially when a long test-trace and short calibration-trace was used.

Table 3.3. RIE loss results and comparison.

RIE loss (dB)	SSL3 (Calibration Trace)			SSL2 (Calibration Trace)		
	Measured VNA	Measured TDR	Calculated tan δ = 0.017	Measured VNA	Measured TDR	Calculated tan δ = 0.017
SSL1 (Test trace)	**0.9135**	**0.9374**	**0.8852**	**0.7614**	**0.7469**	**0.6942**
ST1-2 (Test trace)	**2.4535**	**2.4662**	**2.1825**	**2.3014**	**2.2757**	**1.9914**

The calculated RIE loss really depends on the value of loss tangent and the geometry parameters used for calculation. Table 3.4 provides the percentage difference between TDR and VNA numbers. It is observed that the percentages are less than 12% in all cases.

Table 3.4. Percentage difference of RIE loss between VNA and TDR methods.

Test trace / Cal trace	(VNA - TDR)	%Diff
ST1-2 / SSL3	0.2710	11%
ST1-2 / SSL2	0.2843	12.3%
SSL1 / SSL3	0.0283	3.1%

With the RIE loss number, the loss tangent value can be estimated by plotting the RIE loss number as a function of loss tangent. The RIE loss number is given by (3.45) which was derived under the assumption that loss tangent is a constant value. But, plotting (3.45) by assuming a varying loss tangent in (3.22) would provide the curves in Figure 3.8.

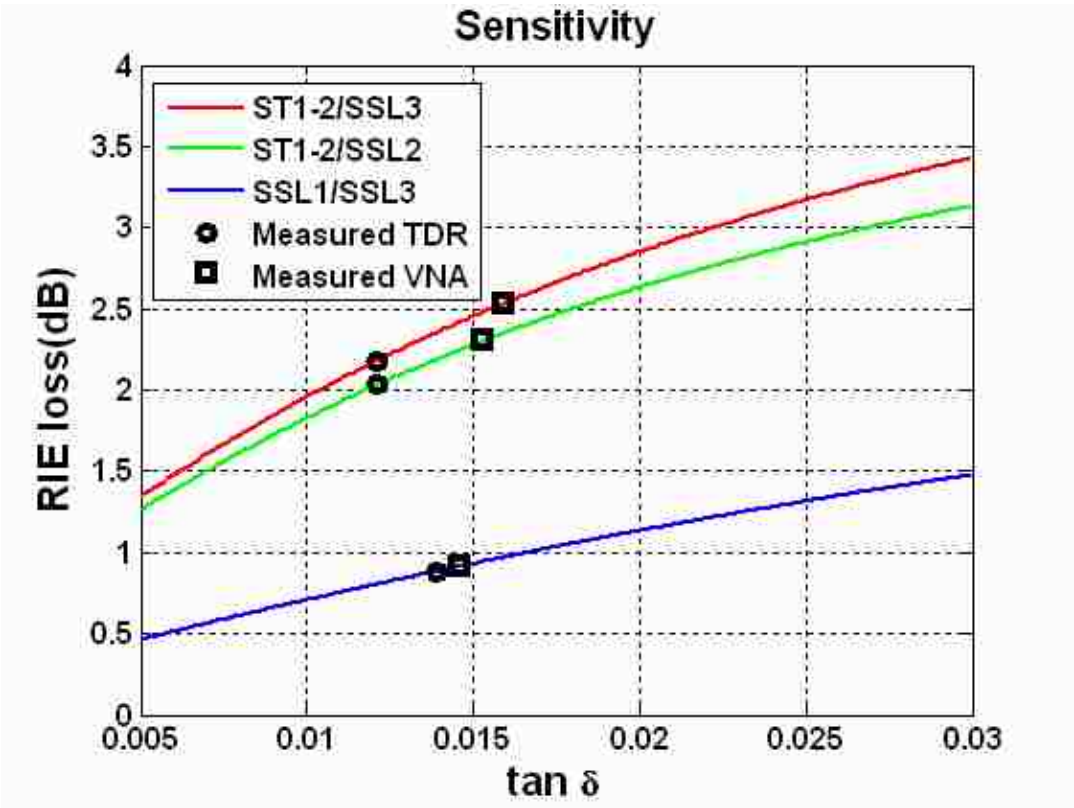


Figure 3.8. RIE loss number calculated analytically as a function of loss tangent.

The red, green and blue curves are analytical RIE loss numbers with varying loss tangent for the corresponding combination of test trace and calibration trace. By plotting the numbers calculated from measurements, which is shown by square and circular

points, approximate value of loss tangent can be obtained from measurement results. Table 3.5 shows the projected value of loss tangent for each measurement.

Table 3.5. Projected value of loss tangent from RIE loss curves.

Test trace / Cal trace	tan δ (VNA)	tan δ (TDR)
ST1-2 / SSL3	0.0159	0.0121
ST1-2 / SSL2	0.0153	0.0121
SSL1 / SSL3	0.0146	0.0139

From Table 3.1, VNA measurements, which was our standard, is giving loss tangent values close to what was extracted. The extracted value for this material was 0.017 and VNA RIE loss number corresponds to almost 0.016. But, TDR RIE loss number, which were not very accurate correspond to a value close to 0.012. More research is needed to make sure that TDR measurements are much more accurate and corresponding RIE loss values, because the TDR measurements are dependent on the bandwidth of the equipment. Once it is made sure that VNA and TDR are providing comparable measurement results, this method could prove to be a standard in extracting the loss parameters with the help of time domain equipments like TDR. Thus, RIE loss number could be used as a standard to estimate losses in a printed circuit board (PCB).

4. ANALYSIS, MODELING AND VALIDATION

Cost-effective, efficient, and fast signal link path designs require careful modeling strategies. Several tools are available in the market to do time and frequency domain simulations for signal integrity analysis. Static time domain solvers provide us quick results while full wave simulations take longer. But, full wave simulations provide us with more accurate results. But, modeling is not an easy task. The user not only has to understand the problem very well but also needs to understand how to use the tool effectively. Simple problems also need careful modeling to assure that the results obtained are correct. Once modeling is done, it is very important to make sure that the results are meaningful and corresponds to what was expected. Experience with signal integrity analysis and tools, could solve this problem easily. But, for a beginner, he could try to validate the results by developing analytical solutions. As the problem becomes complex, developing analytical solutions become tedious. Then, the best way to validate the results would be to use several different tools available in the market. Comparisons will lead to a better understanding of modeling and more accurate solutions. This Section deals with two simple signal integrity modeling problems.

First, the problem considers a dielectric slab placed in an air-medium. A plane wave passes through this dielectric slab. The time delays for the plane wave traveling through air and through a dielectric medium will be different because of the material properties. Those time delays and reflections, at air and dielectric boundaries are analyzed using two different tools.

Design of power distribution networks (PDNs) on a printed circuit board (PCB) is very important for proper charge delivery to the devices on the board. Lowering the

impedance is the key for efficient PDN design. Second problem deals with the modeling of a large PCB with a source at the center. Effects of using decoupling capacitors on transfer impedance are analyzed. Location and value of capacitors were changed to see how it affects the transfer impedance. The results are validated using three tools.

4.1. PROPAGATION DELAY THROUGH A DIELECTRIC SLAB

The problem considers the propagation of a plane wave through a dielectric slab. The dielectric constant of the slab is varied to see the effects of it on the propagation delay. As the plane wave passes through the dielectric medium, the time it takes to pass depends on the dielectric constant of the slab. If dielectric constant is increased, the plane wave takes more time to pass through the medium since time delay is directly proportional to the square root of dielectric constant. The problem here compares a thin slab with dielectric constants 2.5, 5 and 10.

4.1.1. Geometry Description. The problem as shown in Figure 4.1, considers a 5 cm thick dielectric slab with width and length large enough to be considered as infinite. This is to avoid the boundary effects that could possibly be a part of the end results. A Gaussian plane wave source is considered here which is approaching from x = minus infinity direction. So, the plane wave is propagating along the x-axis.

4.1.2. Time Delay Calculation. The velocity of propagation (v_p) of a wave traveling through the slab with dielectric constant (ε_r) is given by

$$\text{Velocity of propagation}, v_p = \frac{c}{\sqrt{\varepsilon_r}}. \tag{4.1}$$

$$\text{Time delay}, t_d = \frac{d}{v_p}. \tag{4.2}$$

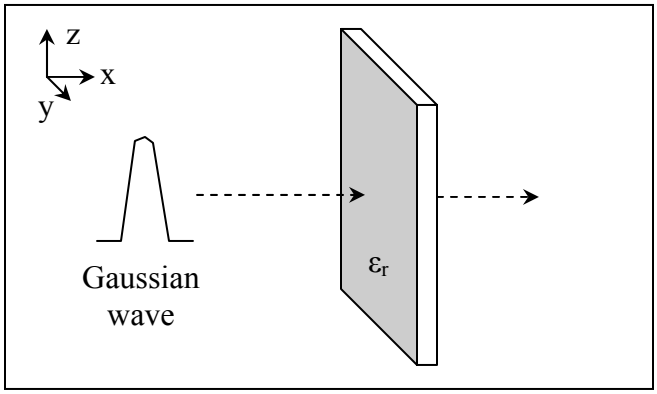


Figure 4.1. Gaussian wave propagating through a dielectric slab.

where $c = 3\times10^{8}\, m/s$; $d = 5\times10^{-2}\, m$.

Therefore,

$$\text{Case 1: } \varepsilon_r = 2.5\,; t_d = 0.263\times10^{-9}\, s\,. \tag{4.3}$$

$$\text{Case 2: } \varepsilon_r = 5\,; t_d = 0.37\times10^{-9}\, s\,. \tag{4.4}$$

$$\text{Case 3: } \varepsilon_r = 10\,; t_d = 0.527\times10^{-9}\, s\,. \tag{4.5}$$

Calculation of time delay is very simple. But, the following sections show the difficulty in modeling such a simple problem.

4.1.3. Modeling Geometry using EZ-FDTD. The simulation was done in a full wave tool called EZ-FDTD developed by UMR, EMCLab. The overall cell domain was defined as x = 200 cells, y = 200 cells, z = 200 cells. The cell size was defined as x = 1 mm, y= 6 cm, z = 6 cm. The cell size is the smallest dimension in the problem where the fields are calculated. Increasing the number of cells provides better accuracy but at the cost of time. The dimensions of y-cell and z-cell were chosen to be greater than x-cell because of the need to make width and height of the slab large enough to be considered infinite. Then the dielectric slab is defined. The geometry can be seen in the Figure 4.2.

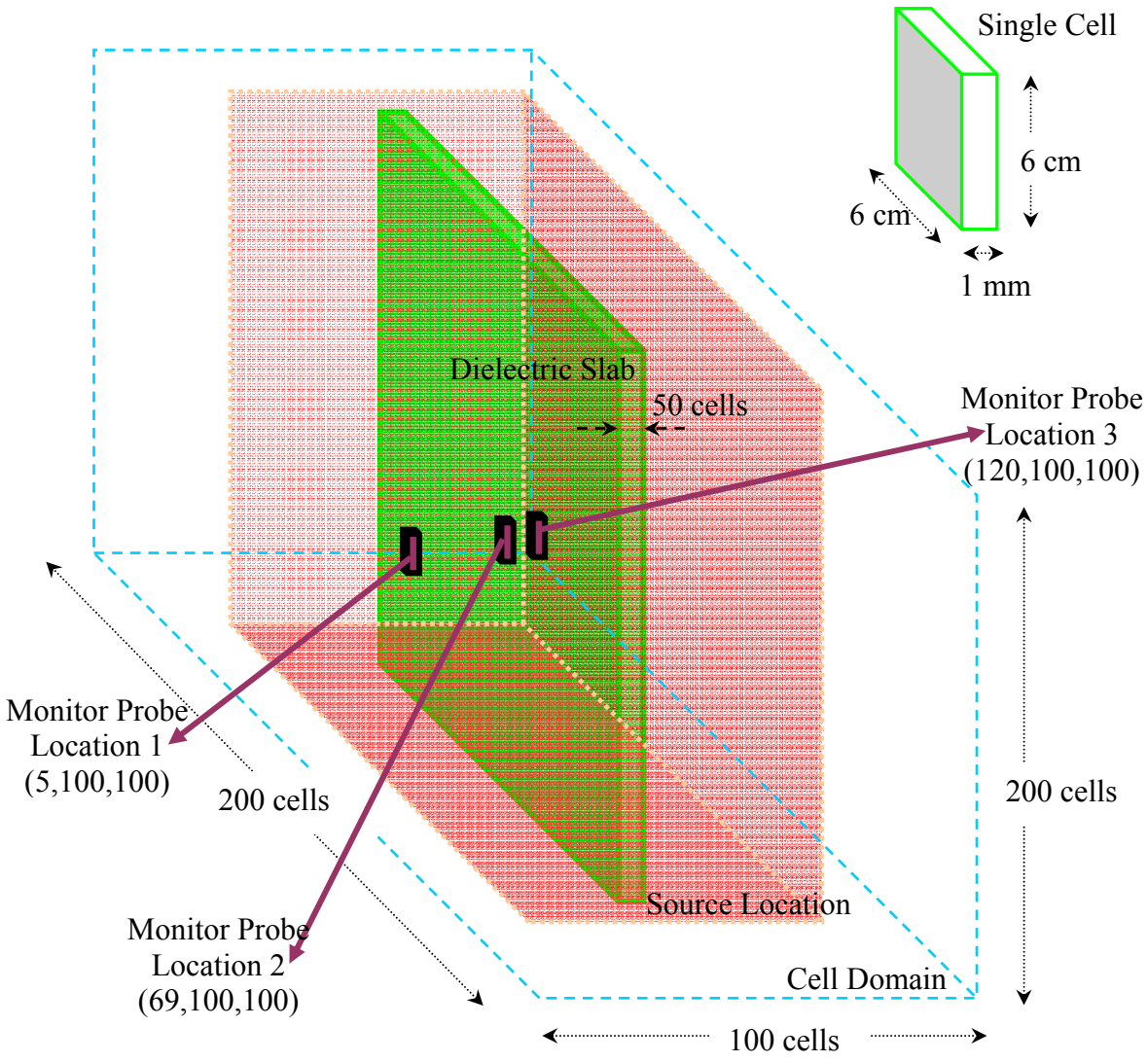


Figure 4.2. Cell domain for EZFDTD simulation with three monitor probes at different locations before and after the dielectric slab.

A custom material is defined with the specific dielectric constant. Then a plate is created with a thickness of 5 cm. The width and height almost equals to the source location size. A monitor probe was placed to observe the fields at the source location. Then two monitor probes were placed at the cell before and after the slab. The total time

step was chosen to be 10000. Simulation was not run till the total time step was reached because, only the first wave to pass through our monitor locations to calculate the time delay. This saved a lot of time. Boundary condition scheme was also specified to be PML with six white spaces and eight absorbing layers. The PML scheme has the best absorbing effectiveness and the number of white spaces is chosen so that there is a trade off between simulation time and absorbing effectiveness. More white spaces mean, better absorption, but more simulation time.

The source was chosen to be a Gaussian plane wave with a temporal width 100 which is propagating in the positive x-direction. The components of electric field is chosen to be $E_x = 0$, $E_y=1$ and $E_z=0$. Electric field direction is in the yz plane since wave is passing in the positive x-direction. Source amplitude was chosen to be 1V. The source location was also specified and can be seen in Figure 4.2.

4.1.4. Simulation and Analysis using EZ-FDTD. The simulation was done in EZ-FDTD and results were generated. The simulation was stopped before it reached the final step size because the data for the first wave to pass through the slab is needed for this study. The data files were loaded in MATLAB and E_y component of electric field was plotted against time. The peak value of E_y component that reaches the monitor probe 1 is taken as t_1. The peak value of E_y component that reaches monitor probe 2 is taken as t_2. Thus, propagation delay is $t_d = t_2 - t_1$. Figure 4.3 shows a diagrammatic view of the incident waves and reflected waves. Time delay is also depicted in Figure 4.3. The monitor probes are placed before and after the slab and are shown as red squares in Figure 4.3. The parallel polarization of a plane wave incident on a dielectric medium can be explained using the electric field that lies in the xz plane.

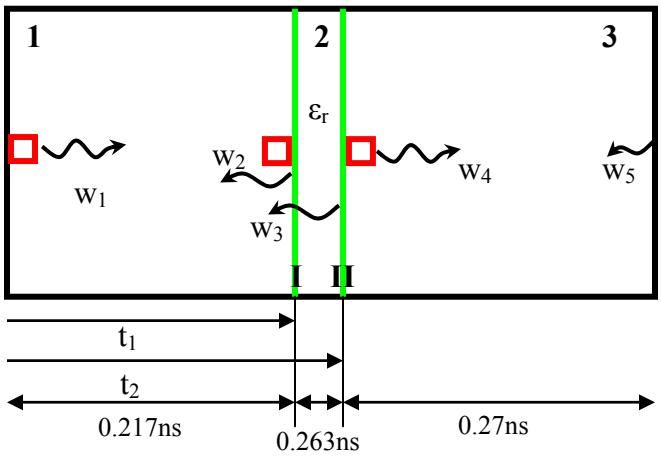


Figure 4.3. Location of monitor probes and wave behavior at boundaries.

The incident wave can be written as

$$E_i = E_0 \hat{x}\, e^{-jzk_1}. \tag{4.6}$$

where $k_1 = \omega\sqrt{\mu_0 \varepsilon}$, is the wavenumber of the region 1 shown on Figure 4.3.

The reflected and transmitted waves can be written as

$$E_r = E_0 \Gamma\ e^{-jzk_1} \hat{x}. \tag{4.7}$$

$$E_t = E_0 \mathrm{T}\ e^{-jzk_2} \hat{x}. \tag{4.8}$$

where $\Gamma = \dfrac{\eta_2 - \eta_1}{\eta_2 + \eta_1}$ .and $\mathrm{T} = \dfrac{2\eta_2}{\eta_2 + \eta_1}$., are the reflection and transmission coefficients, respectively. η_1 and η_2 are the impedances of medium 1 (377Ω) and medium 2 (284.43), respectively. Therefore, transmission and reflection coefficients can be calculated.

The example case chosen was the one where ε_r = 2.5, The reflection and transmission coefficients when the wave travels from region 1 to region 2 are

$$\Gamma_1 = \frac{\eta_2 - \eta_1}{\eta_2 + \eta_1} = \frac{238.43 - 377}{238.43 - 377} = -0.2252. \tag{4.9}$$

$$\mathrm{T}_1 = \frac{2\eta_2}{\eta_2 + \eta_1} = \frac{2*238.43}{238.43 + 377} = 0.7748 . \tag{4.10}$$

The reflection and transmission coefficients when the wave travels from region 2 to region 3 are

$$\Gamma_2 = \frac{\eta_2 - \eta_1}{\eta_2 + \eta_1} = \frac{377 - 238.43}{377 + 238.43} = 0.2252 . \tag{4.11}$$

$$\mathrm{T}_2 = \frac{2\eta_2}{\eta_2 + \eta_1} = \frac{2*377}{238.43 + 377} = 1.2252 . \tag{4.12}$$

For monitor probe 1 (at the source), the magnitude of E_y when E_o = 1 V/m is the wave reflected from surface 1 and is seen at probe 1

$$E_{y1} = E_0 \cdot \Gamma_1 = 1(-0.2252) = -0.2252 V/m . \tag{4.13}$$

Wave transmitted from surface 1, reflected from surface 2 and transmitted back from surface 1 is calculated as

$$E_{y121} = E_0 \cdot \mathrm{T}_1 \cdot \Gamma_2 \cdot \mathrm{T}_2 = 1*(0.7748*0.2252*1.2252) = 0.2138 V/m . \tag{4.14}$$

The wave observed at probe 1 are w1 and the reflected waves w2, w3. There will also be reflections from w5, but they will be quite small. It takes, t = 0.93ns for the wave to reach monitor probe 1. Then it passes through free space and reaches the monitor probe 2(just before the dielectric slab) which is 0.065m away. The time of travel is

$$t = \frac{0.065}{3\times10^8} = 0.217 ns . \tag{4.15}$$

w2 reaches monitor probe 1 in

$$t = (0.93 + 0.217 + 0.217) ns = 1.364 ns . \tag{4.16}$$

To calculate the reflected waves, the time the wave takes to pass through the dielectric slab with ε_r = 2.5,

$$t = \frac{0.050 \times 2.5}{3 \times 10^8} = 0.263ns\,. \tag{4.17}$$

Therefore, w3 reaches monitor probe 1 in

$$t = (0.93 + 0.217 + 0.217 + 0.263 + 0.263)ns = 1.89ns\,. \tag{4.18}$$

For monitor probe 2, the magnitude of E_y when E_o = 1V/m, is the wave reflected from surface 1 and is seen at probe 2

$$E_{y2} = E_0 - E_{y1} = \left(1 - 0.2252\right) = 0.7748V/m\,. \tag{4.19}$$

Wave transmitted from surface 1, reflected from surface 2 and transmitted again from surface 1 can be calculated as

$$E_{y21} = E_{y2} \cdot \Gamma_2 \cdot \mathrm{T}_2 = \left(0.7748 * 0.2252 * 1.2252\right) = 0.2138V/m\,. \tag{4.20}$$

The total time it takes w1 to reach monitor probe 2 is

$$t = (0.93 + 0.217)ns = 1.147ns\,. \tag{4.21}$$

The w3 is coming back to monitor probe 2 in

$$t = (0.93 + 0.217 + 0.263 + 0.263)ns = 1.673ns\,. \tag{4.22}$$

For monitor probe 3, the magnitude of E_y when E_o = 1V/m, is the wave reflected from surface 1 and is seen at probe 3 (wave transmitted from surface II)

$$E_{y3} = E_0 \cdot \mathrm{T}_1 \cdot \mathrm{T}_2 = 1 * 0.7748 * 1.2252 = 0.9493V/m\,. \tag{4.23}$$

The wave reaches monitor probe 3 in

$$t = (0.93 + 0.217 + 0.263)ns = 1.41ns\,. \tag{4.24}$$

The monitor probe 2 is showing much lesser amplitude for E_y as that of the source because some of the field components reflected from the slab boundary is out of phase with the incident wave and cancels off (as shown in (4.19)). There are reflections from the end of the source location too, but the value is quite small. The time delay values and

magnitude of E_y are proved to be correct in Figure 4.4. The times and magnitudes of E_y vary for different dielectrics but the calculation done above is only for slab with $\varepsilon_r = 2.5$. Figure 4.4 shows the waves and the time delays at all probe locations.

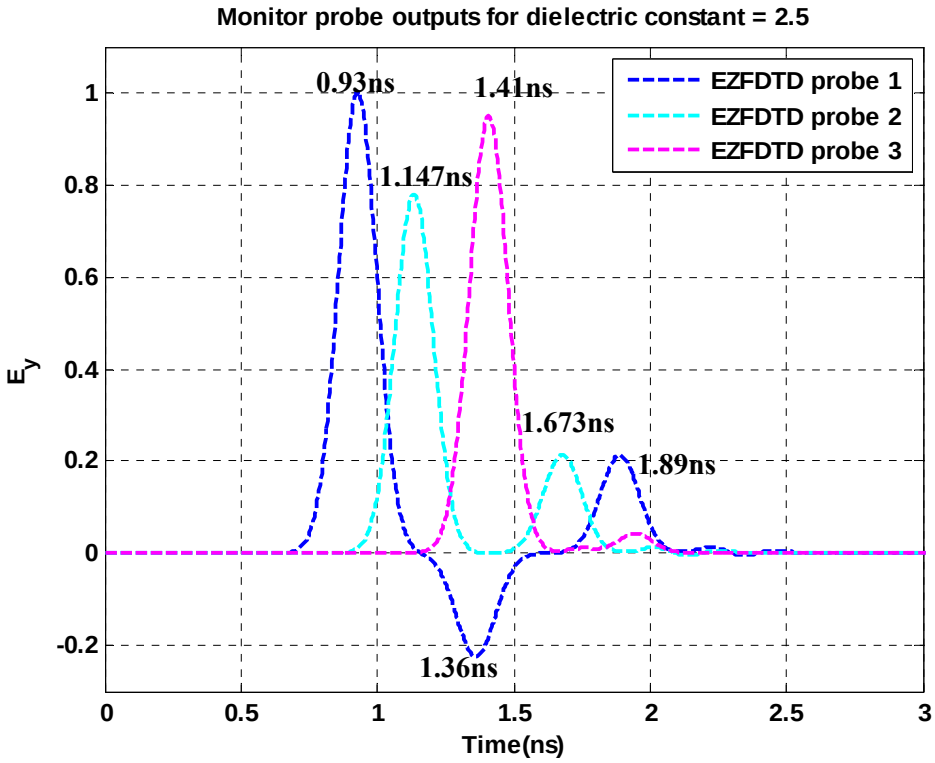


Figure 4.4. Calculated and observed time along the wave propagation.

With the help of EZFDTD, the time delays for all the different dielectric constants could be found out. Following values were extracted from EZFDTD output. These values compare very well with calculated time delays in (4.3), (4.4), and (4.5).

Case 1: (see Figure 4.5) when $\varepsilon_r = 2.5$, $t_d = 0.27$ ns.

Case 2: (see Figure 4.6) when $\varepsilon_r = 5$, $t_d = 0.39$ ns.

Case 3: (see Figure 4.7) when $\varepsilon_r = 10$, $t_d = 0.54$ ns.

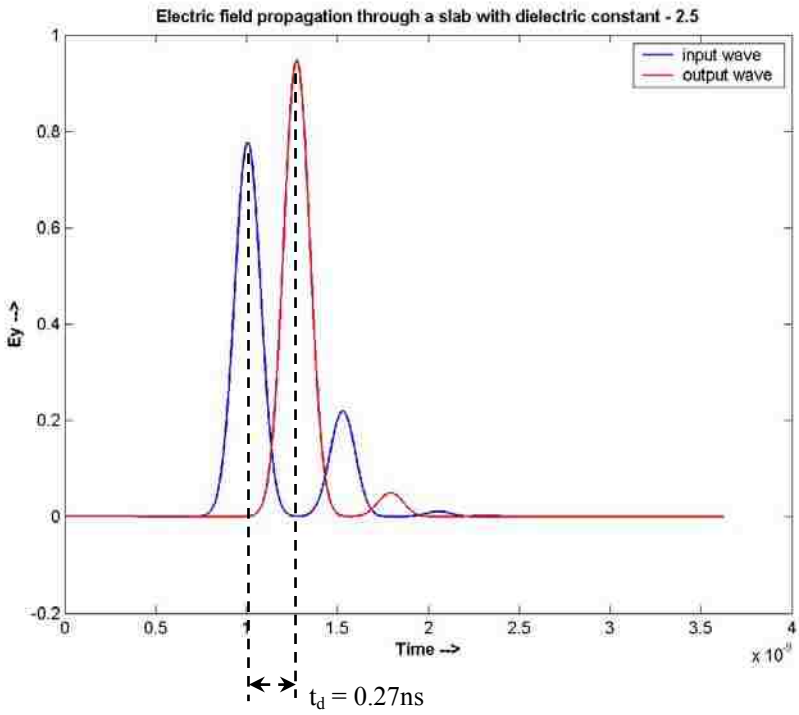


Figure 4.5. Propagation delay through the slab with dielectric constant 2.5.

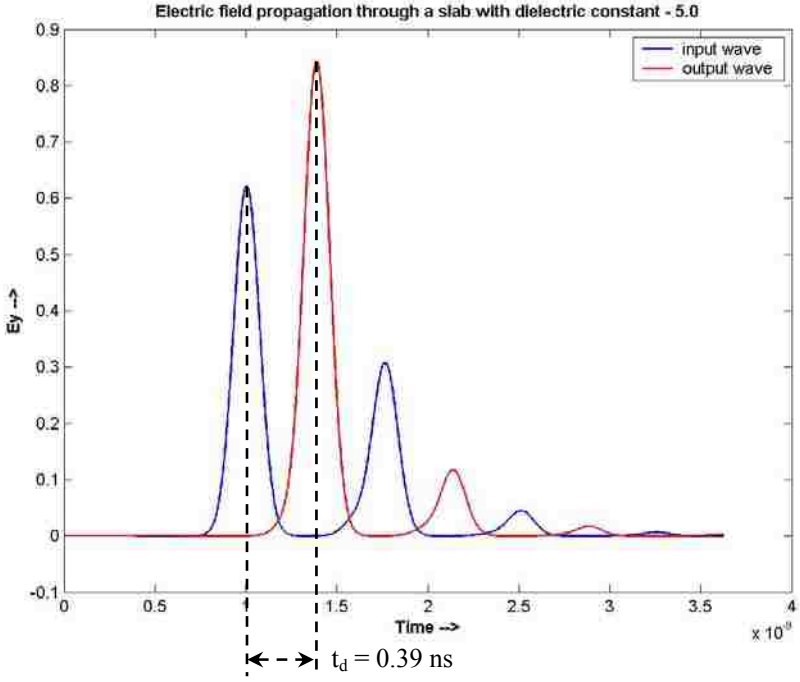


Figure 4.6. Propagation delay through the slab with dielectric constant 5.

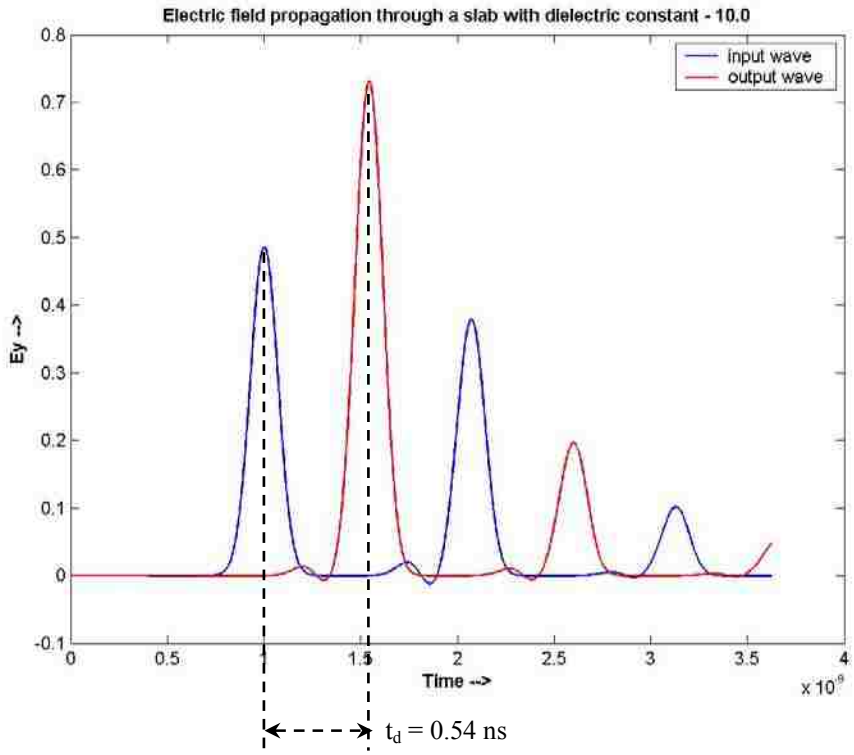


Figure 4.7. Propagation delay through the slab with dielectric constant 10.

4.1.5. Modeling and Simulation using PSPICE. The same structure was modeled in PSpice using transmission lines models. There are three sections of transmissions lines modeled. The first and last being free space and the center one being the dielectric slab. The characteristic impedance for the first and last section is chosen to be $Z_0 = 377\Omega$ since its free space. The time delays of each transmission line are obtained from calculations done on Section 4.1.2 (depending on the distance the wave traveled and the wave speed). The center section has a characteristic impedance of

$$Z_0 = \frac{377}{\sqrt{\varepsilon_r}}. \tag{4.25}$$

Here, have a value of $Z_0 = 238.44\Omega$ for $\varepsilon_r = 2.5$. The input Gaussian wave was created using a V_{PWL} function in PSpice. To smoothen out this sharp wave, an RC filter was

designed. I had to play around with the values to get an exact match with the EZFDTD input Gaussian wave. The circuit was terminated with the characteristic impedance of 377Ω. The circuit diagram in shown in Figure 4.8.

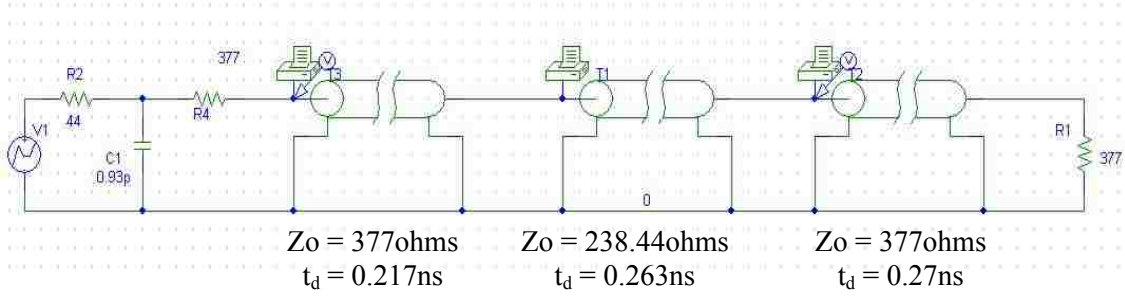


Figure 4.8. Circuit diagram in PSpice for $\varepsilon_r = 2.5$.

The output curve for one of the cases is shown in Figure 4.9.

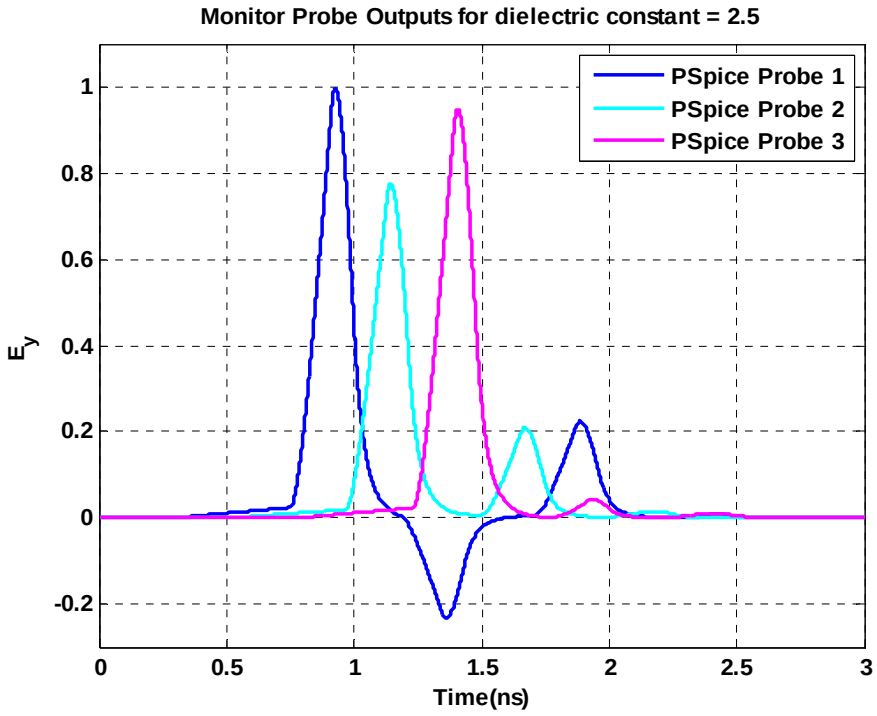


Figure 4.9. The dielectric slab simulated in PSpice for $\varepsilon_r = 2.5$.

4.1.6. Comparison and Validation. After generating results from both tools, they are compared to see how well they agree. Figure 4.10 shows the comparison between EZFDTD and PSpice for the case where dielectric constant is 2.5. Calculations are also done for the comparison and are shown in Table 4.1.

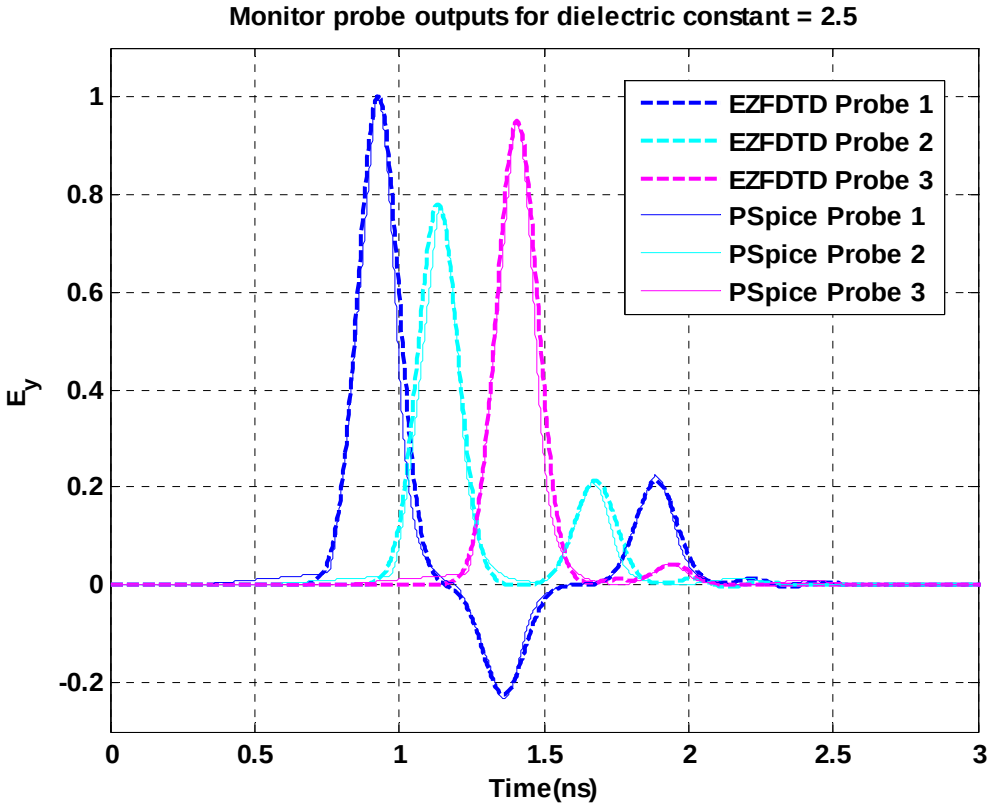


Figure 4.10. Comparison of EZFDTD data with PSpice simulated data for $\varepsilon_r = 2.5$.

The comparison is done for dielectric constants 5 and 10 also. Figure 4.11 and Figure 4.12 gives the comparison plots. The calculations for those are not done because it is almost similar to the calculations with dielectric constant 2.5. The calculated values of time delay and field at the peaks of the Gaussian wave is shown in Table 4.1. However,

both EZFDTD and PSpice results match for both dielectric constants 5 and 10. All methods agree very well.

Table 4.1. Comparison between calculations and tools of values at wave peaks.

$\varepsilon_r = 2.5$		Calculated			EZFDTD			PSpice		
P_1	t_d(ns)	0.930	1.364	1.890	0.927	1.363	1.888	0.927	1.363	1.887
	E_y(V/m)	1.000	-0.225	0.214	1.000	-0.225	0.213	0.997	-0.232	0.224
P_2	t_d(ns)	1.147	1.673		1.135	1.678		1.144	1.671	
	E_y(V/m)	0.773	0.214		0.780	0.213		0.776	0.209	
P_3	t_d(ns)	1.410			1.408			1.407		
	E_y(V/m)	0.949			0.949			0.949		

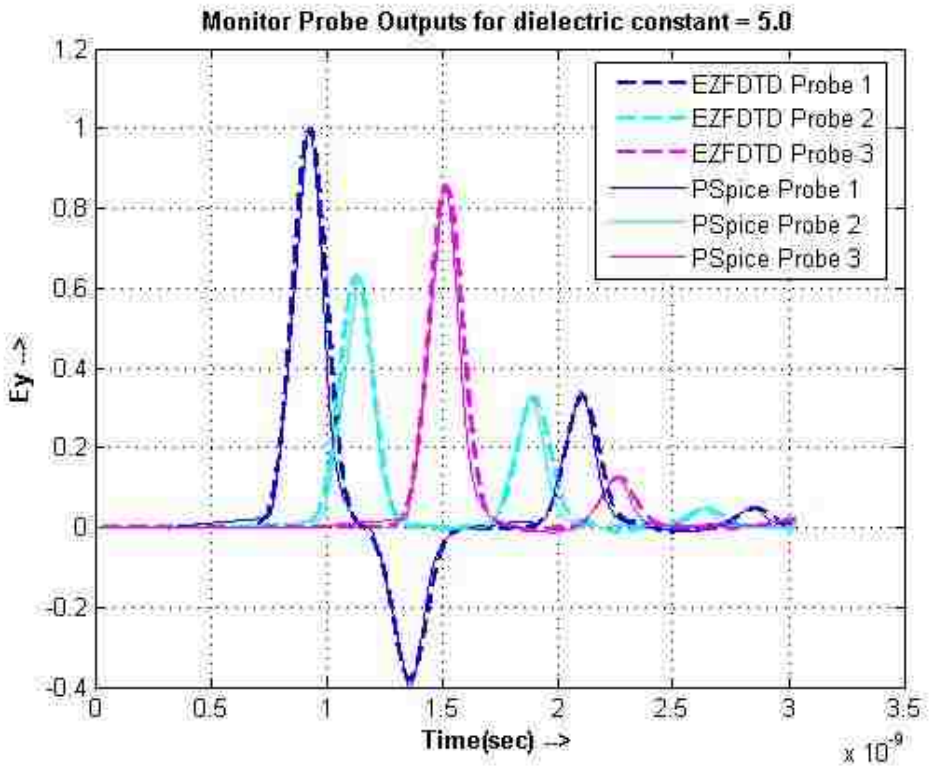


Figure 4.11. Comparison of EZFDTD data with PSpice simulated data for $\varepsilon_r = 5.0$.

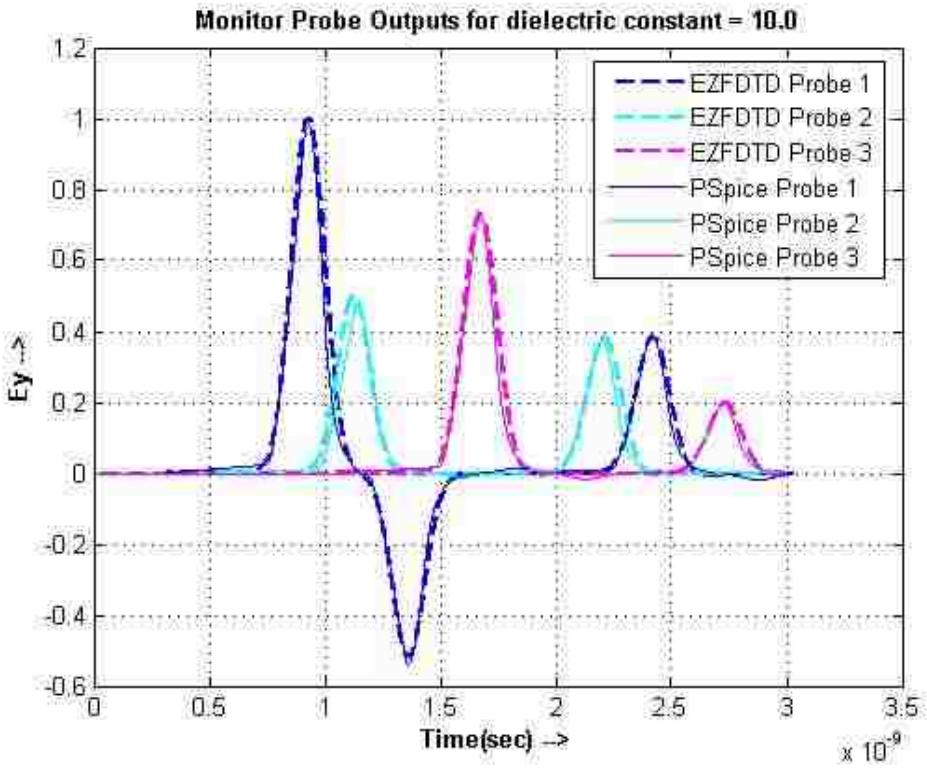


Figure 4.12. Comparison of EZFDTD data with PSpice simulated data for $\varepsilon_r = 10.0$.

Thus, propagation delay across a dielectric slab was studied and the models were created in EZFDTD and PSpice to verify the propagation delay across dielectric slabs with different dielectric values were verified and these results were validated with calculations. It was also seen that the reflections at different discontinuities were also matching in all cases.

4.2. DECOUPLING POWER/GROUND PLANES IN PCBs

In high speed digital circuit designs, the design of power distribution networks (PDNs) play a very important role in maintaining signal integrity. In EMC and signal integrity applications, proper decoupling strategies are very important because of the

requirement of sufficient current for a digital device on the printed circuit board (PCB) for switching the transistors [14-17]. The problem considered here is a realistic-sized printed circuit board with a power and a ground plane separated by FR4. Different decoupling strategies are applied to see its effect on impedance at different locations on the printed circuit board (PCB).

4.2.1. Geometry Description. The problem considers a printed circuit board, with capacitors distributed across the entire board. The specifications are given below and a diagram is provided in Figure 4.13. This problem includes a wide range of frequencies, resonance effects, and the effects of lumped circuit elements.

General Board Description: 4-layer board with 2 solid planes in inner layers, solid planes are separated by 40 mils dielectric FR4 (relative dielectric constant = 4.5).

PCB size: 10” x 12” inches.

Capacitors: 95 capacitors evenly spaced 1” apart, includes 30 mohms series resistance and 2 nH series inductance.

Source: Located in center of board, 1-volt sine wave, frequency scanned from 10-1000 MHz.

Figure-of-merit: Impedance at output #1, #2, and #3

Following cases are considered for decoupling analysis:

1. Board with no capacitors.
2. Board with four capacitors only around source.
3. Board with fully loaded 95 capacitors.
4. Use capacitor values of 0.01 μF, 0.1 μF and 100 pF.

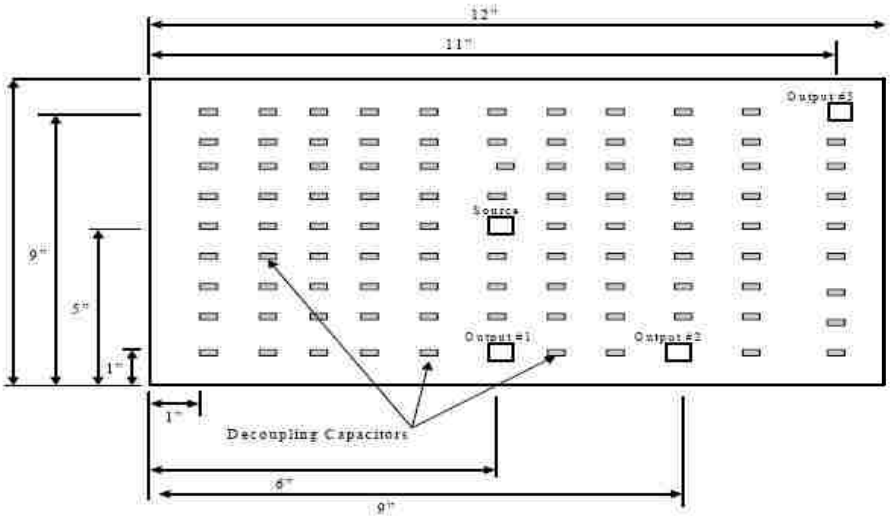


Figure 4.13. Geometry information for decoupling on a printed circuit board (PCB).

4.2.2. Modeling using Cavity Resonance Tool (EZPP). The geometry was setup in EZPP software. The source was provided at the center of the board. Three voltage probes were placed at the locations as shown in Figure 4.13. All the cases with different value of capacitors were modeled. Figure 4.14 shows a sample layout for 95 capacitor case.

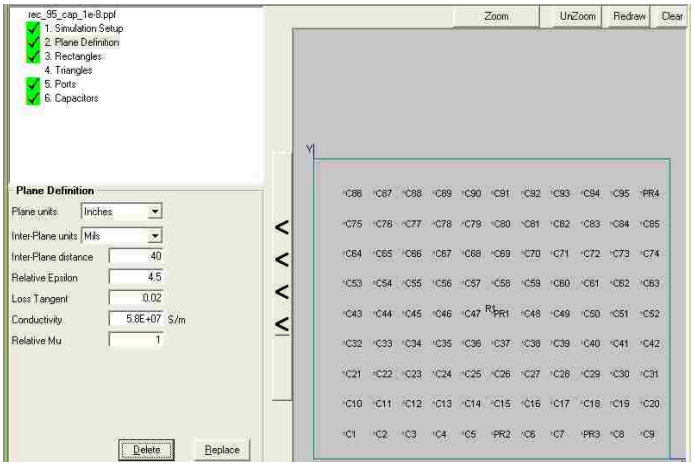


Figure 4.14. Screenshot of EZPP tool with 95 capacitor case.

The simulations were done and results were taken which would be explained in Section 4.2.5. For the case in Figure 4.14, the parameter settings used in the tool are shown in Figure 4.15. The number of X and Y modes were defined as 10. Port size was chosen to be 1mm. All the geometry information was defined as shown in Figure 4.15. Decoupling capacitors were also defined with ESR=3mΩ and ESL=2nH.

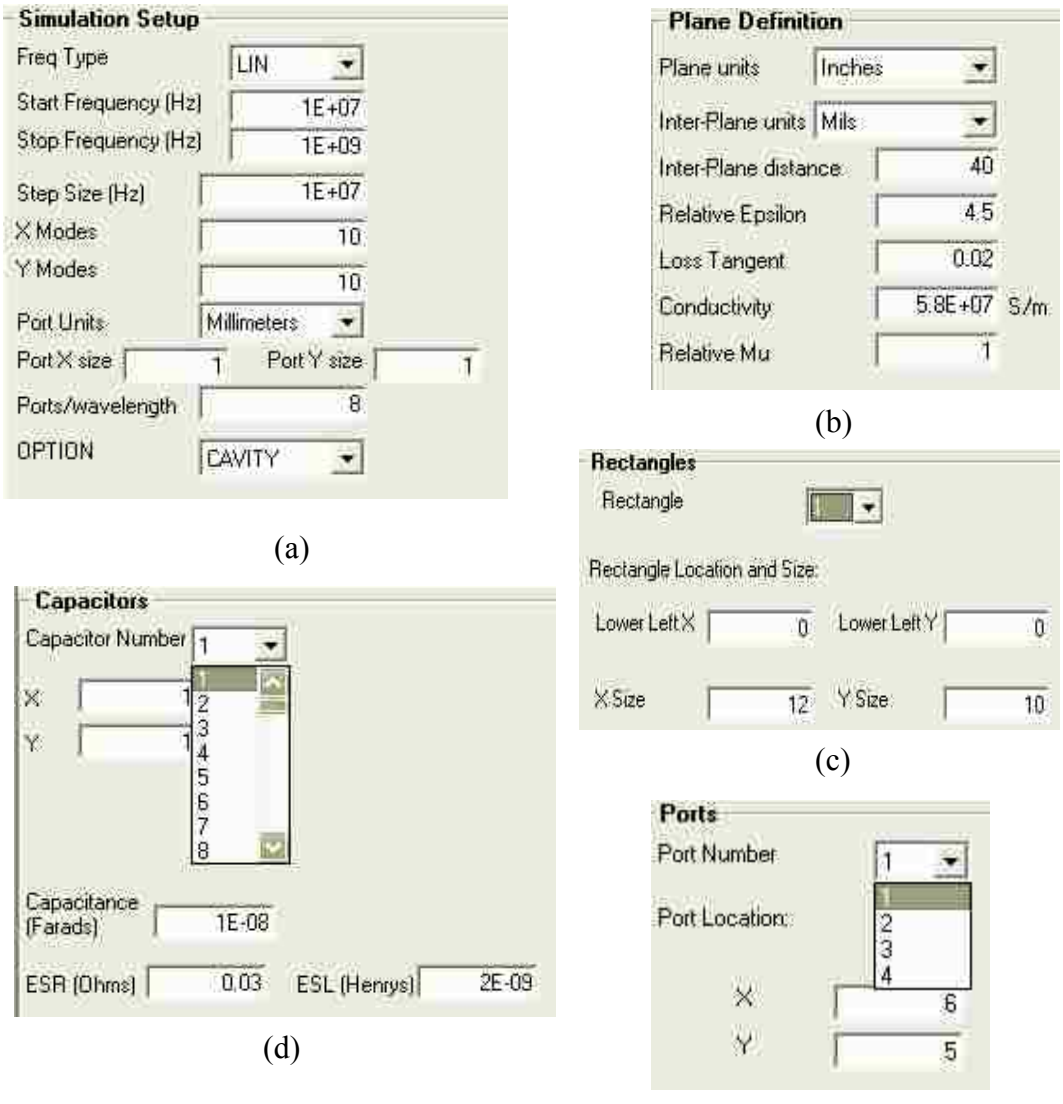


Figure 4.15. EZPP parameter setup. (a) Simulation parameters, (b) Plane definition, (c) Rectangle definition, (d) Capacitor definition, (e) Port definition.

4.2.3. Modeling using Full Wave Tool (EZFDTD). Modeling was also done in a full wave tool called EZFDTD. The model laid out for this particular problem is as shown in Figure 4.16. The size of the board is 10x12 inches. So, y-axis needs to cover a distance of 0.254m (10 inches). The cell size for y-direction was calculated to be 0.00254m. Therefore, the number of cells needed was calculated to be 100 cells in y-direction. Extra 5 cells are added on both ends. So, a total of 110 cells are needed in y-direction. Similarly, a distance of 0.3048m (12 inches) in x-direction was needed and the cell size was defined to be 0.00254m. So, the total number of cells required was found to be 120 cells. An addition of 5 cells on both sides makes a total of 130 cells in x-direction. Now, a power and ground plate with a dielectric FR-4 ($\varepsilon_r = 4.5$) is sandwiched between them. FR4 is 40 mils thick. Decoupling capacitors have to be connected from power to ground. Three components (ESR, ESL and C) are needed to represent a decoupling capacitor. In order to connect all of them in series, 40 mils is divided into three cells so that three different cells could be used to connect all the lumped elements (as shown in Figure 4.16). So, the cell size should be (40mils/3) 0.003387m. So, there are 3 cells and an addition of 5 cells on both sides which makes a total of 13 cells in z-direction. Therefore, the cell domain was defined as x = 110 cells, y = 130 cells and z = 13 cells. And the cell sizes are given as x = 0.00254m, y = 0.00254m, z = 0.003387m. The total time step was chosen to be 1000000. The time was kept so long because to resolve lower frequencies in 95 capacitor case. The source was located at the center of the board which is at the location (65, 55, 6-7). Since the plates are at 5^{th} and 8^{th} cell the source is connected to those plates with thin wires. The source (1V) was chosen to be mod-Gaussian with a min frequency of 10 MHz and a maximum frequency of 1000 MHz. The

source type was chosen to be resistive with a resistance of 50ohms. Then, the FR-4 plate was defined which is 40 mils thick which covers 3 cells in z-direction. The two power planes are also defined. Voltages are probed at three locations in the plates as shown in Figure 4.16. A size of a cell is also shown in Figure 4.16.

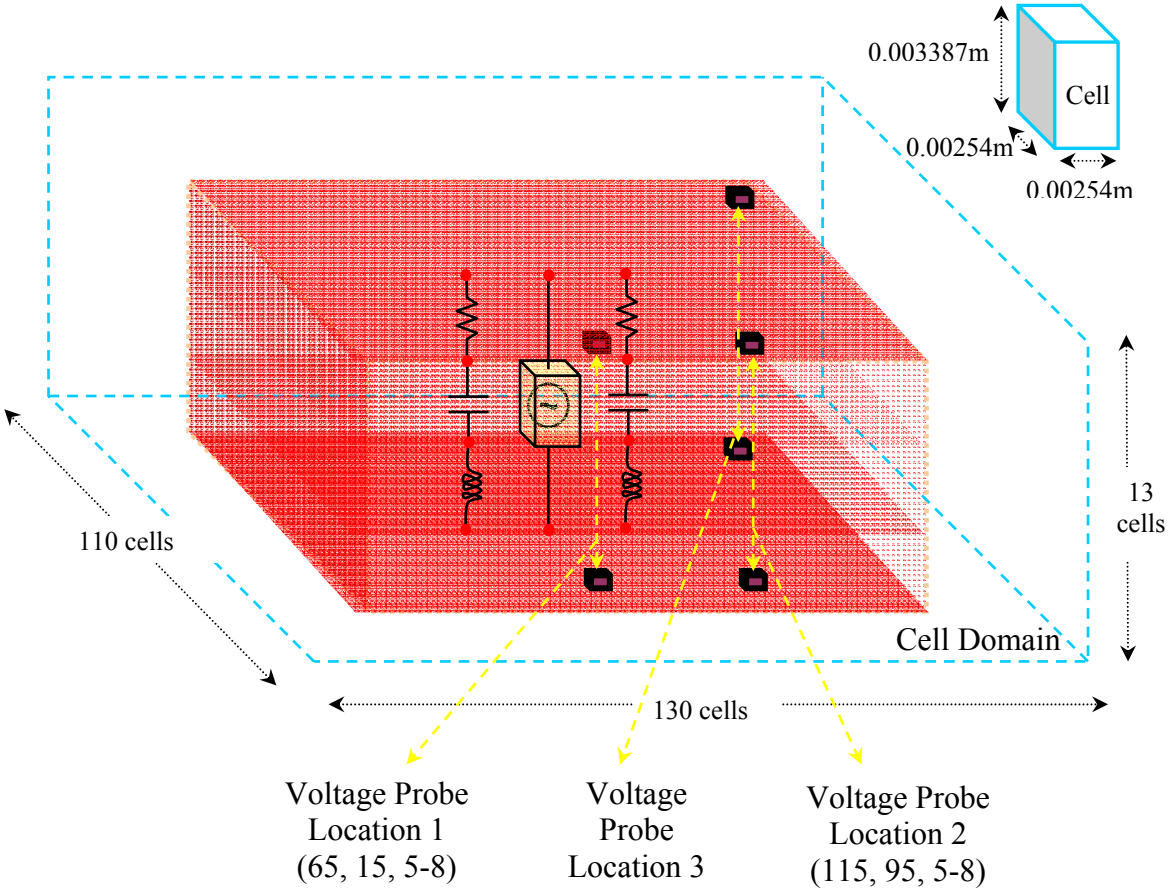


Figure 4.16. Geometry defined in EZ-FDTD.

EZFDTD requires specification of conductivity of the material instead of specifying the tan δ. Since loss tangent was used to specify losses in other two tools, it was a bit of difficulty to match all the Q values. Finally, an approximation was derived to

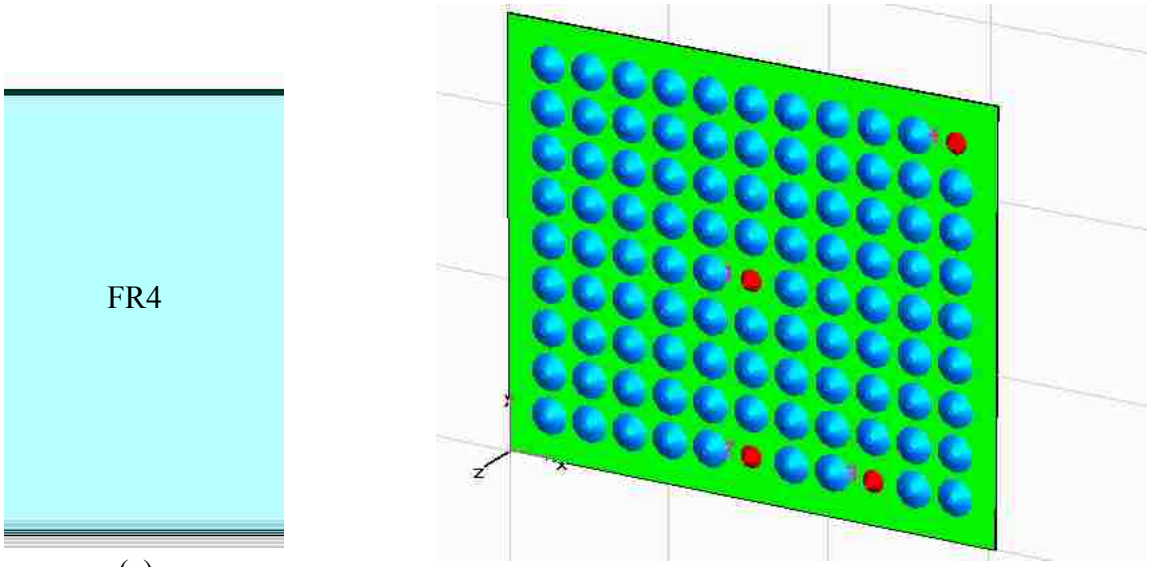
calculate the conductivity for a particular tan δ. The following equation was used to calculate the conductivity

$$\sigma = \omega\varepsilon' \tan\delta \,. \tag{4.26}$$

where σ = conductivity; ω = 2*π*f, f = frequency; ε' = $\varepsilon_0\varepsilon_r$; tan δ = loss tangent.

By choosing an approximate middle frequency of 700 MHz, the conductivity was calculated to be 0.0035. All cases as mentioned in the geometry description were modeled and simulated.

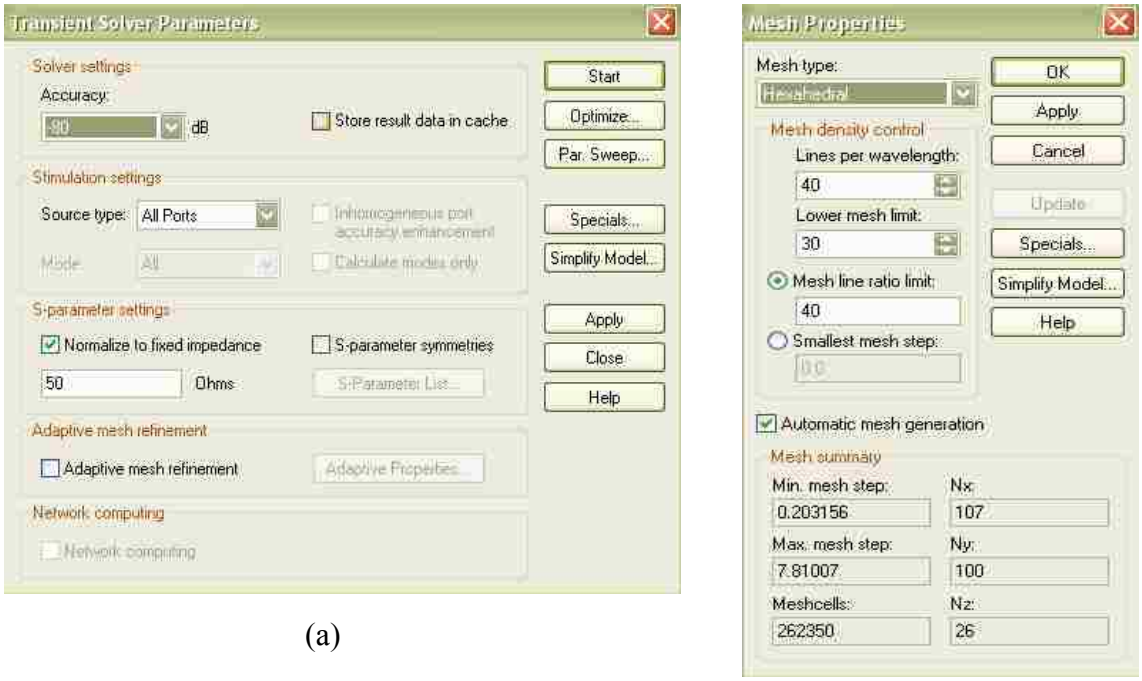
4.2.4. Modeling using Full Wave Tool (Microwave Studio). Modeling using CST Microwave Studio was also done for this geometry. Figure 4.17 shows the stack up and the top view of a case where the board is laid out with 95 capacitors. Figure 4.17(a) shows an FR4 material separated by copper layers. Figure 4.17(b) shows the port locations and also decoupling capacitor locations.



(a) (b)

Figure 4.17. Geometry modeled in CST. (a) Stackup for the geometry. (b) Layout (blue: capacitors, red: ports).

The thickness of copper chosen was 0.4mm. FR-4 is 40 mils thick. The ports were also defined in the locations shown on Figure 4.13. A Gaussian excitation signal with Fmin = 10 MHz and Fmax = 100 MHz was provided for analysis. A transient solver was used with parameters shown in Figure 4.18. By choosing the mesh properties shown in Figure 4.18, sufficient number of cells was generated for full wave analysis. Accurate results could be obtained by increasing the number of cells for the cost of time.



(a) (b)

Figure 4.18. Modeling parameters in CST. (a) Transient solver parameters. (b) Mesh properties.

Higher lines per wavelength were given for the 95 capacitor case to get accurate results at lower frequencies. The accuracy of the transient solver was also set to -80 dB for maximum accuracy.

4.2.5. Results and Comparison. All the cases mentioned in Section 4.2.1 were modeled and simulated using three different tools. This section provides the results of simulation and the validation of results between different tools. Figure 4.19, shows the transfer impedance from the source of the board to Output 1 with no decoupling capacitors on. There is some shift in resonances if Output 2 and 3 are observed. They are shown in Figure 4.20 and Figure 4.21, respectively.

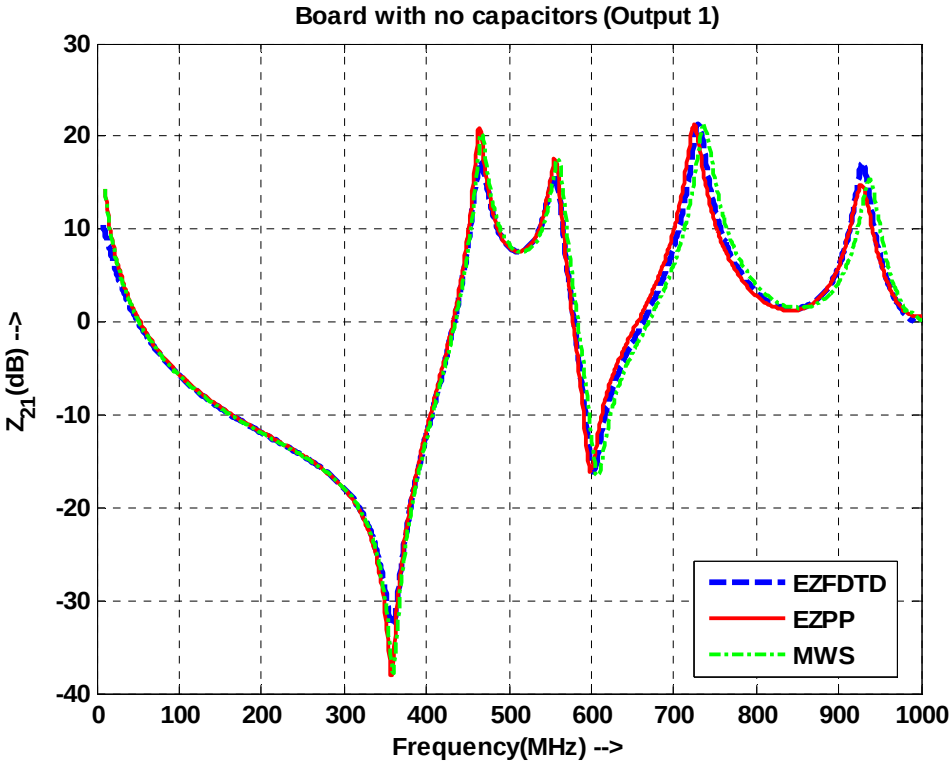


Figure 4.19. Transfer impedance from source to Output 1 for the board with no capacitors.

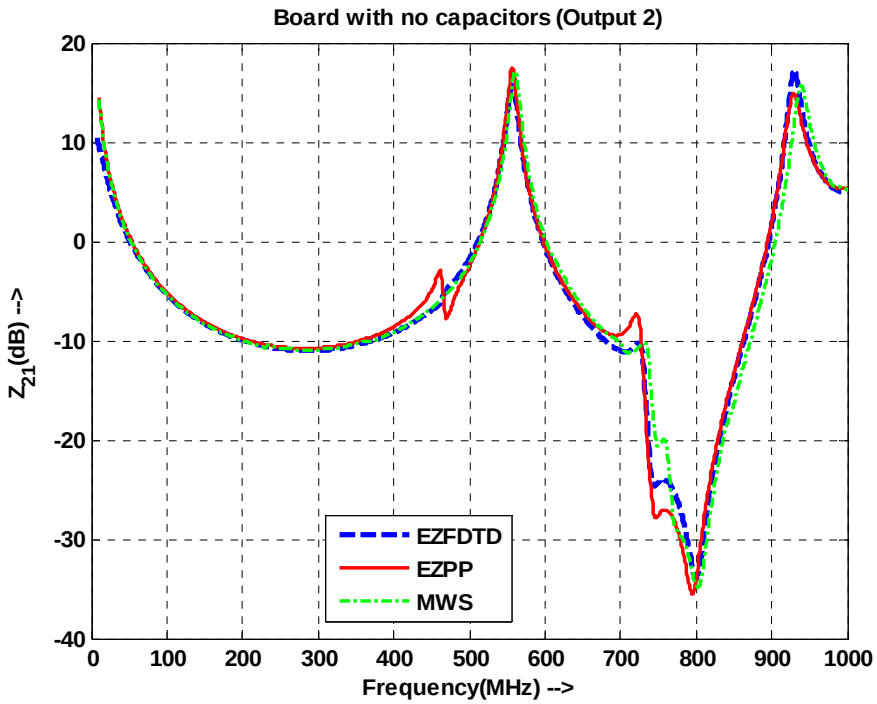


Figure 4.20. Transfer impedance from source to Output 2 for the board with no capacitors.

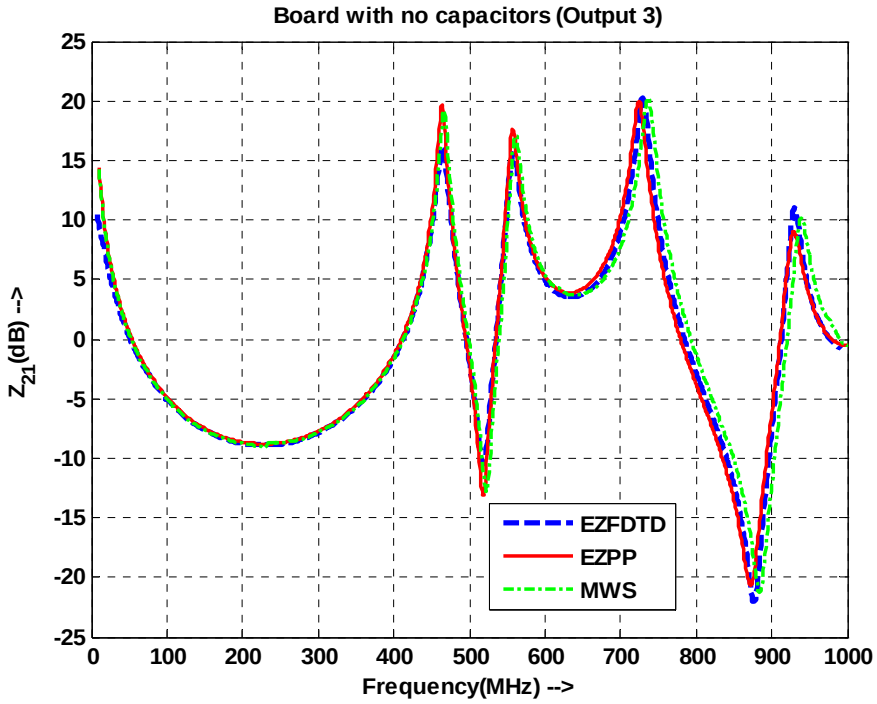


Figure 4.21. Transfer impedance from source to Output 3 for the board with no capacitors.

For further results, only transfer impedances from source to output 1 are shown for different values and numbers of capacitors used. Figure 4.22, shows the case at Output 1 when only four capacitors of value 0.01µF were used. The shift in first resonance was seen at low frequency which is indicative of the added decoupling capacitance. But, this really did not bring the impedance down a lot except at very low frequencies. Figure 4.23 shows the case where four 0.1µF capacitors were used. Figure 4.24 shows the case where four 100pF capacitors were used. Figure 4.23 shows that, as the capacitor value were increased, the first resonance shifted to lower frequencies. No appreciable difference was seen in lowering of transfer impedance when four capacitors were used.

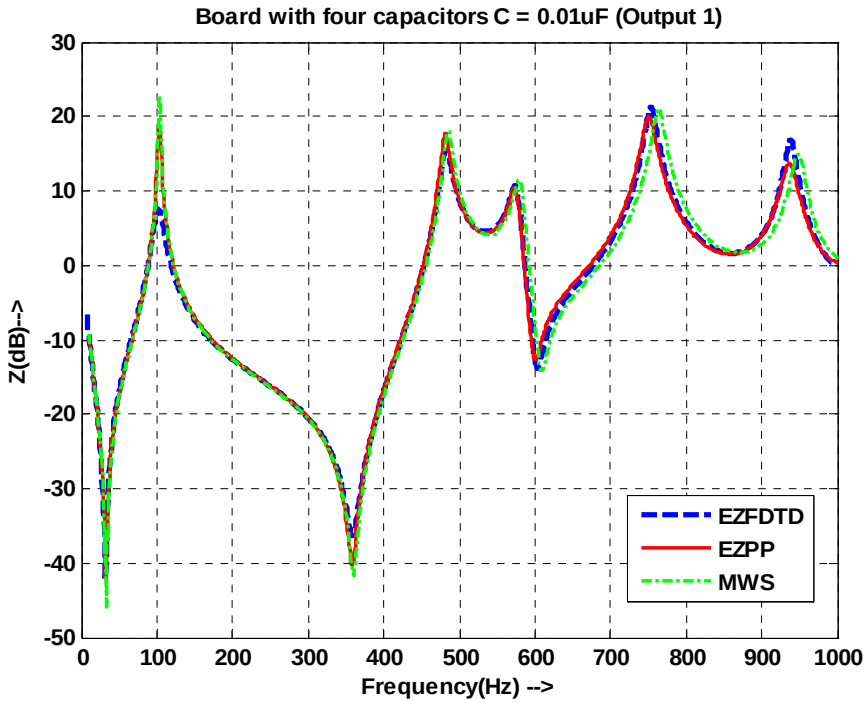


Figure 4.22. Transfer impedance from source to Output 1 for the board with four capacitors (0.01µF) around the source.

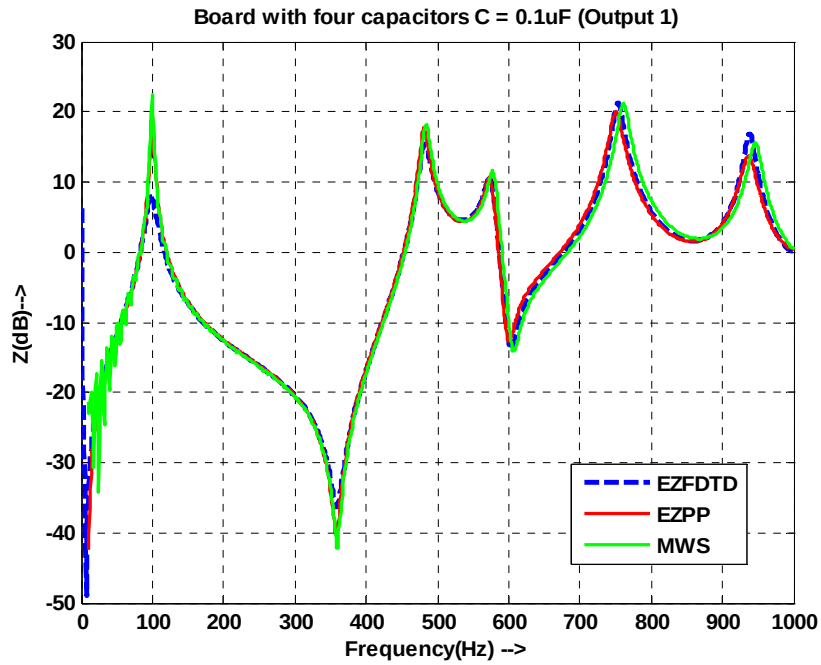


Figure 4.23. Transfer impedance from source to Output 1 for the board with four capacitors (0.1μF) around the source.

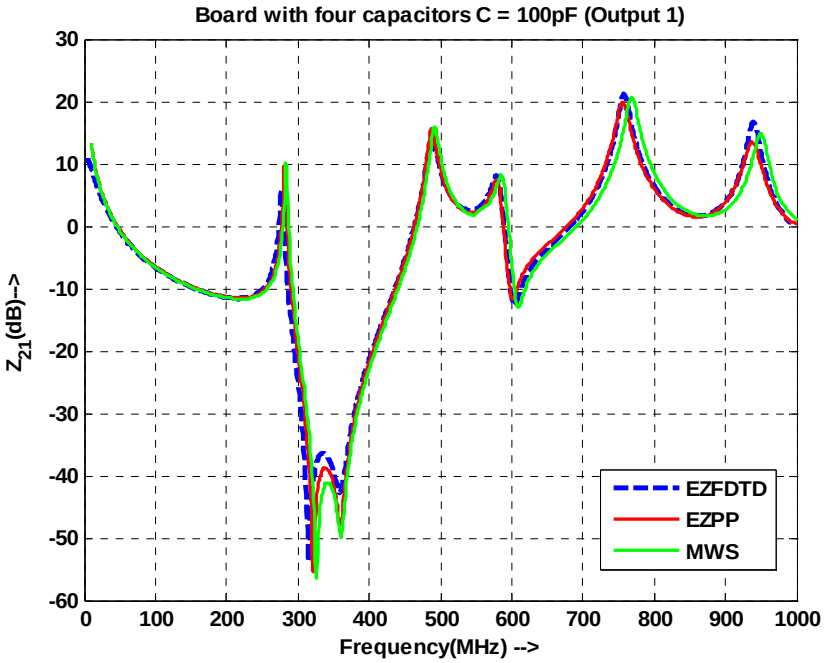


Figure 4.24. Transfer impedance from source to Output 1 for the board with four capacitors (100pF) around the source.

In Figure 4.23, a discrepancy is observed at the low frequency for MWS simulations. This is because the full wave simulation was not run long enough to resolve the components are lower frequencies. Usage of full wave tools, results in accurate results but the disadvantage is that it take very long time to execute. But, cavity resonance tools like EZPP executes in a few minutes for simple cases like these. EZFDTD took 2 days of simulation time for the board with no capacitors. Processing the data after simulation would also be difficult because of the oversized data files.

Similar cases with 95 capacitors were also done. Figure 4.25 shows the case where the entire board is filled with 95 capacitors. Appreciable lowering of transfer impedance can be seen at low frequencies for these cases. Figure 4.26 and Figure 4.27 shows the same using different values of capacitors.

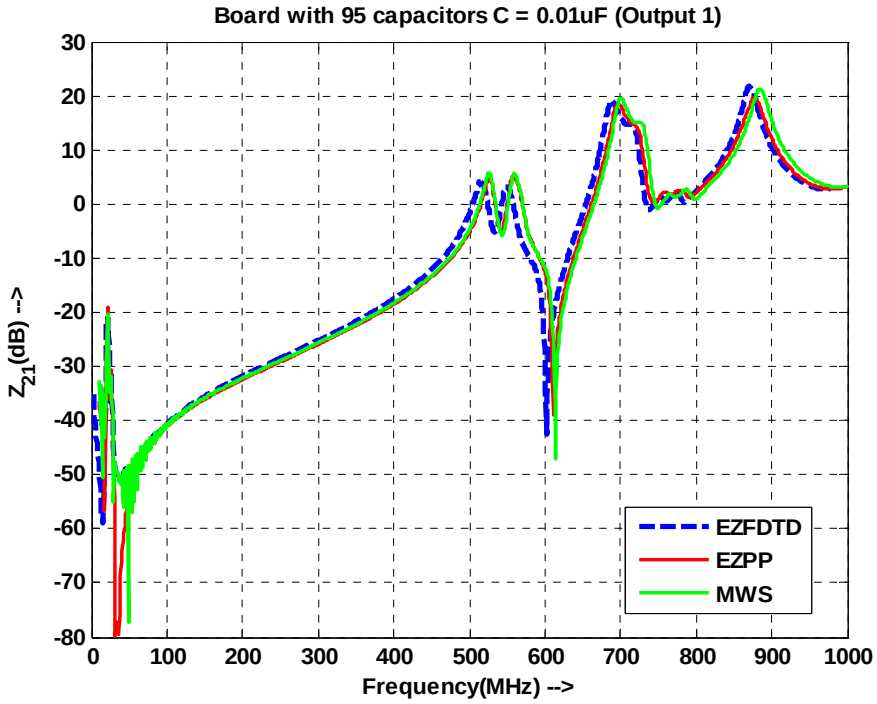


Figure 4.25. Transfer impedance from source to Output 1 for the board with 95 capacitors (0.01μF) around the source.

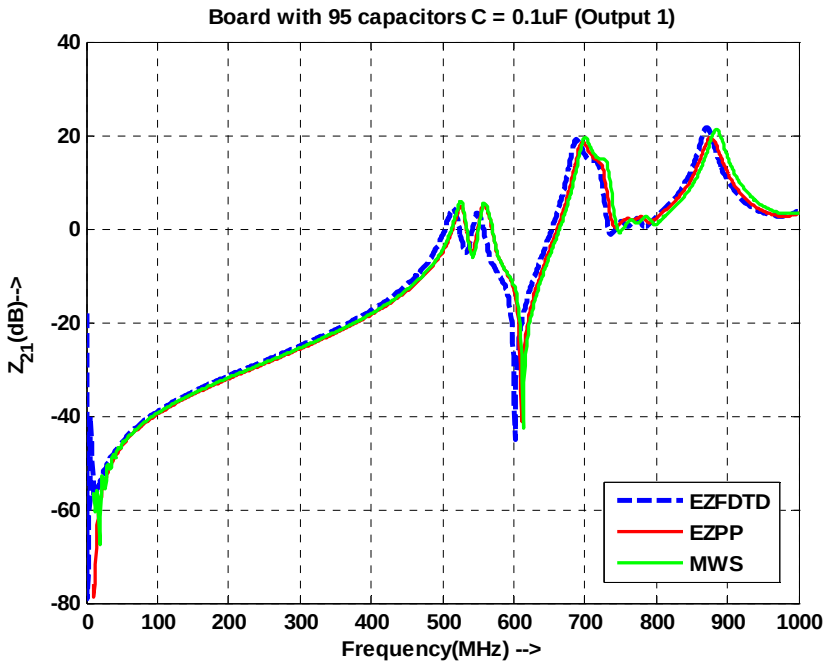


Figure 4.26. Transfer impedance from source to Output 1 for the board with 95 capacitors (0.1μF) around the source.

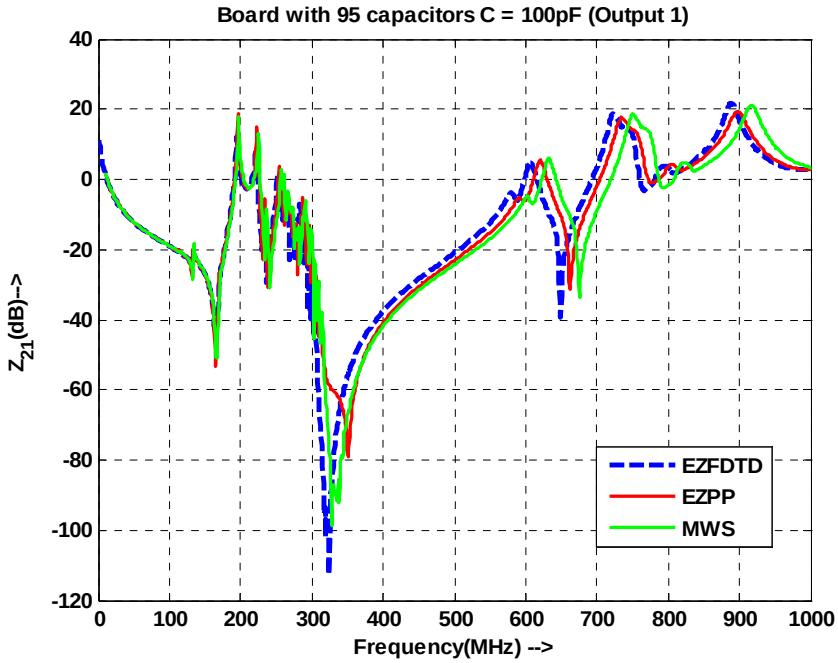


Figure 4.27. Transfer impedance from source to Output 1 for the board with 95 capacitors (100pF) around the source.

The use of 95 capacitors works pretty well in reducing the impedance at lower frequencies. Figure 4.26 shifts lowest resonance to very low frequencies and the impedance is low up to about 650 MHz. At higher frequencies, the series inductance (ESL) starts to dominate and take over. So, the decoupling strategies should also be considering the reduction of the package inductance when the frequency of interest is high. Studies of this sort are very important when considering power integrity issues. It becomes very important to supply enough charge for switching the transistors in digital devices. Otherwise the device will fail to operate.

5. SUMMARY

The material extraction procedure for a stripline geometry was refined using two sample test boards. A measurement protocol was developed to be applied for microstrip test vehicles. Two different techniques were developed to extract material parameters from microstrip transmission lines. A new microstrip test board was designed. Several variants of FR-4 samples were manufactured from different printed circuit board (PCB) suppliers. All samples were measured and material parameters were extracted.

RIE loss was analytically shown to be a potential standard for loss characterization. Stripline test boards were used to characterize losses. Measurements were done in both the frequency-domain and time-domain. RIE loss numbers were extracted and compared. Calculated RIE loss numbers were also obtained for comparison. The comparison proved that the numbers from TDR measurements agree to numbers from VNA measurements with about 12% of accuracy.

Propagation delay through a dielectric slap was analyzed analytically. EZFDTD and PSpice were used to model the geometry and validate the calculated results. A large PCB was modeled with decoupling capacitors to study effects of decoupling on the reduction of impedance. The usage of a large number of capacitors spread across the board was adequate to reduce the impedance to an acceptable level at lower frequencies. The results were validated using three different CAD tools.

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