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WIDEBAND CHARACTERIZATION OF PRINTED CIRCUIT BOARD MATERIALS

UP TO 50 GHZ

by

ALEKSEI RAKOV

A THESIS

Presented to the Faculty of the Graduate School of the  
MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

2013

Approved by

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## ABSTRACT

A traveling-wave technique developed a few years ago in the Missouri S&T EMC Laboratory has been employed until now for characterization of PCB materials over a broad frequency range up to 30 GHz. This technique includes measuring S-parameters of the specially designed PCB test vehicles. An extension of the frequency range of printed circuit board laminate dielectric and copper foil characterization is an important problem. In this work, a new PCB test vehicle design for operating up to 50 GHz has been proposed.

As the frequency range of measurements increases, the analysis of errors and uncertainties in measuring dielectric properties becomes increasingly important. Formulas for quantification of two major groups of errors, repeatability (manufacturing variability) and reproducibility (systematic) errors, in extracting dielectric constant (DK) and dissipation factor (DK) have been derived, and computations for a number of cases are presented.

Conductor (copper foil) surface roughness of PCB interconnects is an important factor, which affects accuracy of DK and DF measurements. This work describes a new algorithm for semi-automatic characterization of copper foil profiles on optical or scanning electron microscopy (SEM) pictures of signal traces. The collected statistics of numerous copper foil roughness profiles allows for introducing a new metric for roughness characterization of PCB interconnects. This is an important step to refining the measured DK and DF parameters from roughness contributions. The collected foil profile data and its analysis allow for developing “design curves”, which could be used by SI engineers and electronics developers in their designs.

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## TABLE OF CONTENTS

	Page
ABSTRACT .....	iii
ACKNOWLEDGMENTS .....	iv
LIST OF ILLUSTRATIONS .....	vii
LIST OF TABLES .....	xi
SECTION	
1. INTRODUCTION .....	1
1.1. METHODS FOR PCB MATERIAL MEASUREMENTS & CHARACTERIZATION .....	2
1.2. LAMINATE DIELECTRICS AND PCB STACKUP .....	8
1.3. TYPES OF COPPER FOILS USED IN PCBs .....	12
1.4. LIMITATIONS ON FREQUENCY OF MEASUREMENTS DUE TO CONNECTORS .....	18
2. MAJOR ERROR AND SENSITIVITY ANALYSIS FOR PCB MATERIALS CHARACTERIZATION .....	21
2.1. REPEATABILITY, OR MANUFACTURING VARIABILITY, ERRORS .....	23
2.2. SYSTEMATIC, OR REPRODUCIBILITY, ERRORS .....	29
2.3. SYSTEMATIC AND REPEATABILITY ERRORS AT LOWER FREQUENCIES .....	32
2.4. DERIVATION OF SENSITIVITY FORMULAS .....	36
2.5. SUMMARY .....	38
3. CHARACTERIZATION OF COPPER FOIL SURFACE ROUGHNESS FROM MICROSECTION PHOTOGRAPHS .....	40
3.1. PREVIOUS TOOL TO CHARACTERIZE SIGNAL TRACE GEOMETRY AND SURFACE ROUGHNESS .....	41
3.2. GENERAL STRUCTURE AND PECULIARITIES OF THE NEW SURFACE ROUGHNESS EXTRACTION PROCEDURE .....	47
3.3. IMAGE PROCESSING PART IN THE NEW ALGORITHM .....	48
3.4. COMPUTER VISION PART IN THE NEW ALGORITHM .....	52
3.4.1. Profile Coding and Extrema Search .....	56
3.4.2. De-trending and Cutoffs .....	60
3.4.3. Removal of False Maxima and Minima .....	63
3.5. ROUGHNESS QUANTIFICATION .....	65

3.6. MORPHOLOGICAL PROCESSING OF THE ROUGHNESS PROFILE.....	69
3.7. AUTOMATIC COLLECTION OF STATISTICS AND DATABASES .....	71
3.8. FURTHER IMPROVEMENT OF ROUGHNESS CHARACTERIZATION.....	74
4. DEVELOPMENT OF DESIGN CURVES .....	80
4.1. EXPERIMENTAL SAMPLES AND SETUP .....	84
4.2. IMPROVED DIFFERENTIAL EXTRAPOLATION MEASUREMENT TECHNIQUE (DERM2) .....	85
4.3. ADDITIONAL SLOPE OF INSERTION LOSS AS A FUNCTION OF FREQUENCY DUE TO FOIL ROUGHNESS .....	90
4.4. MODEL USING EFFECTIVE ROUGHNESS DIELECTRIC .....	93
4.5. SUMMARY .....	104
5. A 50-GHZ TEST VEHICLE DESIGN OPTIMIZATION .....	106
5.1. DESCRIPTION OF THE 30-GHZ TEST VEHICLE AS A PROTOTYPE.....	106
5.2. FIRST ATTEMPT TO DESIGN A 50-GHZ TEST VEHICLE.....	108
5.3. MOLEX PROTOTYPE OF 50-GHZ VIA TRANSITION.....	111
5.4. A NEW VIA TRANSITION DESIGN FOR 50-GHZ SI TEST VEHICLE.....	113
5.5. A NEW GROUND VIA WALL DESIGN.....	116
5.6. TRL PATTERN .....	117
5.7. NEW 50-GHZ SI TEST VEHICLE DESIGN AND ALLEGRO FILES FOR MANUFACTURING .....	117
5.8. NEW FABRICATED 50-GHZ SI TEST VEHICLE.....	122
6. CONCLUSION AND FUTURE SCOPE.....	126
BIBLIOGRAPHY .....	129
VITA .....	136

## LIST OF ILLUSTRATIONS

Figure	Page
1.1. Flowchart of the PCB material extraction procedure from measuring S-parameters [22]. .....	6
1.2. SEM picture of the PCB stripline cross-section .....	8
1.3 Typical multilayer stackup.....	9
1.4. Structure of a copper foil on a dielectric surface [37].....	13
1.5. Electrodeposition copper manufacturing process [38]. .....	14
1.6. SEM pictures of roughness on the treated size of the 0.5 oz ED and rolled copper foils [38]. .....	18
2.1. Measured return loss and insertion loss for three samples of the same set of test vehicles; line length is 15,410 mils .....	24
2.2. DK and DF extracted using “root-omega” procedure for three samples of the same set.....	25
2.3. Actual “measured” and calculated maximum repeatability errors in DK and in DF for three samples of the same set.....	27
2.4. Acceptable and unacceptable levels of measured return loss, insertion loss, and systematic error for DF .....	31
2.5. Effect of the removal of the $\sqrt{\omega}$ component from $\beta$ on the extracted DK and DF values for three samples .....	33
2.6. Effect of the removal of the $\sqrt{\omega}$ component from $\beta$ on the repeatability error in DK and in DF .....	34
2.7. Difference between the measured and fitted $\beta$ , relative errors between the measured and fitted $\beta$ with and without the $\sqrt{\omega}$ term, and the difference for $\alpha$ .....	35
3.1. Flowchart for copper roughness extraction tool .....	42
3.2. Input data for original GUI: SEM and optical microscope images .....	43
3.3. Copper roughness extraction tool and output data.....	44
3.4. User interface of <i>Trace Geometry Extraction Tool</i> .....	45
3.5. Flowchart of the new surface roughness extraction procedure.....	47
3.6. Flowchart of the image processing part.....	49
3.7. Artifacts in images and errors in image processing .....	50
3.8. Image manipulations according to the new image processing algorithm .....	50



3.9. Image to vector conversion .....	53
3.10. Image artifacts.....	55
3.11. Profiles first derivative coding.....	56
3.12. Profiles second derivative coding .....	57
3.13. Profile coding example .....	58
3.14. Extrema search example .....	59
3.15. An example of a profile processing using the improved non-linear de-trending.....	62
3.16. Surface roughness profile, peak and valley cutoffs, and selecting significant peaks and valleys .....	63
3.17. Examples of the artifacts removal.....	65
3.18. Surface roughness impact to insertion losses.....	67
3.19. Morphological operation.....	69
3.20. Examples of the morphological processing of the roughness profile image .....	70
3.21. Roughness profile is the same along the trace width and along the trace length.....	73
3.22. Extracted profile with non-flat envelope around valleys .....	75
3.23. Enforcement of flat base for roughness profile.....	75
3.24. An example of the validation of automatically detected peaks .....	76
3.25. Average shape of the peaks along the roughness profile.....	78
3.26. Flowchart of the new surface roughness extraction procedure based on the new approach .....	79
4.1. Two sets of test vehicles under study .....	85
4.2. Extrapolation to zero roughness in DERM2 procedure applied to total loss on two sets of test vehicles with different foil roughness levels .....	86
4.3. Extrapolation to zero roughness in DERM2 procedure applied to total phase constant on two sets of test vehicles with different foil roughness levels.....	87
4.4. Refined from surface roughness dielectric parameters of laminate dielectrics in two sets of test vehicles.....	89
4.5. Dielectric loss, smooth conductor loss, and rough conductor loss as functions of frequency for both sets of test vehicles .....	89
4.6. Slopes of insertion loss for all test vehicles .....	90
4.7. Additional slopes in insertion loss due to roughness of foils.....	92
4.8. Cross-section of stripline in the numerical Q2D modeling setup .....	95

4.9. DK and DF for all three sets of test vehicles .....	97
4.10. Measured and modeled insertion loss $ S_{21} $ in the STD test vehicle.....	98
4.11 Measured and modeled insertion loss $ S_{21} $ in the VLP test vehicle.....	98
4.12. Measured and modeled insertion loss $ S_{21} $ in the HVLP test vehicle .....	99
4.13. Measured and modeled insertion loss in Set I -STD foil and Set II - STDR foil ...	100
4.14. Measured and modeled insertion loss in Set I and Set II, both RTF foils .....	101
4.15. Measured and modeled insertion loss in Set I -HVLP foil and Set II - HVLP foil .....	102
4.16. Total roughness loss tangent as a function of roughness parameter QR .....	103
4.17. Additional slope in $ S_{21} $ as a function of the total roughness loss tangent .....	103
5.1. Layout of the 30-GHz SI Test Vehicle .....	106
5.2. Stackup of the 30-GHz SI Test Vehicle.....	107
5.3. CST-model of the modified signal via-to-signal trace transition and footprint for of the 50-GHz SI Test Vehicle .....	109
5.4. CST-modeled S-parameters for the modified signal via-to-signal trace transition ..	109
5.5. S-parameters of the fabricated PCB. The presence of strong resonances prevent from using this board for material parameter measurements. ....	110
5.6. Conversion of HFSS Molex's signal via-to-signal trace transition model to CST model.....	111
5.7. Via transition structure and footprint.....	112
5.8. CST modeled S-parameters for Molex structure .....	112
5.9. CST- via transition model and footprint for the new 50-GHz SI test vehicle design .....	113
5.10. Backdrill and new optimized via transition structure .....	115
5.11. Simulated connector-via-trace S-parameters and TDR response for a new designed 50-GHz test vehicle .....	115
5.12. Normal distribution of the ground via generated along the test trace.....	116
5.13. A segment of the schematic file for new 50-GHz SI Test Vehicle.....	118
5.14. PCB drawing for new 50-GHz SI Test Vehicle.....	118
5.15. Connectors insertion in the new 50-GHz SI Test Vehicle.....	119
5.16. Implementation of footprint and padstacks in Allegro PCB Editor.....	120

5.17. Stackup manufacture drawing for the new 50-GHz SI Test Vehicle.....	121
5.18. New fabricated 50-GHz PCB SI test vehicle with removable connectors.....	123
5.19. Measured S-parameters and TDR response of the new fabricated 50-GHz PCB SI test vehicle.....	123
5.20. Extracted DK and DF.....	124
5.21. Evaluated systematic errors for DK and DF extracted on the 50-GHz test board.....	125

**LIST OF TABLES**

Table	Page
3.1. Statistical Data for Various Types of Test Vehicles and Foils .....	72
4.1. Geometrical and Roughness Data for Two Sets of Test Vehicles .....	85
4.2. Curve-fitting Coefficients for Two Sets of Test Boards .....	87
4.3. Geometrical and Roughness Data for Set of Test Vehicles .....	96
4.4. Curve-fitting Coefficients for Set of Test Vehicles .....	96
4.5. Effective Roughness Dielectric.....	99
5.1. Target Impedance Table .....	122

## 1. INTRODUCTION

Today, more functionality, higher speed, smaller features, and lighter weight are required for numerous end-products of consumer, industrial, medical, avionics, and automotive electronics. Signal data rates are reaching tens Gbps, while electronic devices still use multilayer printed circuit boards (PCBs) with copper interconnects. However, the problem with copper interconnects is the frequency-dependent loss, which significantly affects signal integrity and degrades the rise time. If special attention is not paid, problems may be encountered when transmitting high-speed serials links at data rates of even 1 Gbps or more over lengths longer than 20". SI specialists consider that the ultimate limit for copper interconnects may be around 40 Gbps [1], and beyond that optical interconnects are needed.

However, as is stated in [1], copper itself does not pose a fundamental, near-term limit to backplane data rates. Instead, there are cost/performance tradeoffs. Every feature that increases the data rate through copper interconnect will add to the cost of the backplane. Wider traces mean thicker boards. Lower dissipation factor laminates cost more. Higher bandwidth connectors, IC packages and termination components are more expensive. For higher data rates, it is not a question of whether a copper-based interconnects can be applicable, but how much it will this cost. Designers always search for the most cost-effective system approaches, and each system will have a different set of tradeoffs between data rate, cost, risk, and time-to-market.

## 1.1. METHODS FOR PCB MATERIAL MEASUREMENTS & CHARACTERIZATION

Both high-speed digital electronics designers and manufacturers of PCBs are interested in accurate characterization of PCB materials - laminate dielectric substrates and copper foils. The parameters of interest are the dielectric constant  $DK = \epsilon_r'$ , associated with phase constant of the waves propagating on the line, or time delay, and loss tangent, or dissipation factor  $DF = \tan \delta = \frac{\epsilon_r''}{\epsilon_r'}$  for dielectric substrates. The dielectric properties of all PCB dielectrics change with frequency. Dielectric constant  $DK = \epsilon_r'$  typically slowly goes down as frequency increases. Loss tangent, or dissipation factor  $DF = \tan \delta = \frac{\epsilon_r''}{\epsilon_r'}$ , on the contrary, typically increases with frequency increase over the microwave frequency range. This is consistent with the Debye relaxation behavior of dipole polarization dynamics in dielectrics exposed to high-frequency electromagnetic field [2]. Loss due to conductors on PCB transmission lines is also frequency-dependent. Designers must know this loss. Loss due to the rough conductor-dielectric interfaces is of a special interest, since conductors on laminate substrates are always rough for adhesion purposes [3].

Currently, the frequency range for PCB laminate dielectric characterization is from 50-60 Hz [4] to 110 GHz [5]. The most low-frequency characterization of unclad laminate dielectrics used for PCBs is done by applying capacitor-loading (LCR meter) techniques and impedance analyzer [6], and the most high-frequency techniques use resonances in cavities with appropriate numerical modeling [4]. There are some resonator methods of measuring dielectric properties of thin unclad laminate dielectrics, including split-post dielectric resonator (SPDR) technique [7], and split cylinder resonator (SCR)

technique [8]. All resonator techniques are narrowband. To conduct measurements in a number of discrete frequency points over a wide frequency range, a number of test fixtures of different dimensions are needed. This makes narrowband measurements time-consuming, expensive, and not always realizable.

Wideband measurement techniques, either in time domain, or in frequency domain, are preferable. To characterize unclad laminate dielectrics, one can use, for example, Nicolson-Ross-Weir technique [9] and [10]. In this case, samples of dielectric materials of special shape (washers or rectangular bars) should be cut out. Incident electromagnetic waves in a coaxial line or a waveguide are normally incident on a sample, which should precisely fit (with no gaps) the cross-section of a coaxial air line or an appropriate waveguide test fixture. Still, frequency range of measurements using a coaxial line or a waveguide of each cross-section is limited by the cut-off frequency at the lower end (for waveguides), and higher-order mode excitation at the upper end of the frequency band.

Various standard techniques to characterize different unclad dielectric materials are described in NIST reports [11], [12], and [13].

However, characterization of unclad PCB laminate dielectrics is not sufficient for SI engineers, high-speed electronics designers, and PCB manufacturers. Conductor loss characterization is also important, especially for the rough conductor and dielectric interface, existing in real PCBs. Moreover, the majority of PCB dielectrics exhibit anisotropy. For this reason, measured dielectric properties when the electric field is in-plane cannot be directly used when analyzing PCB structures with electric field being out-of-plane. Eventually, engineers need to know the behavior of dielectrics “in situ”, *i.e.*,

directly on a transmission line - a single-ended or coupled stripline, or on a microstrip. For this reason, measurements of PCB dielectric parameters in industry are typically conducted using stripline resonator techniques. These are either Bereskin method [14], or as proposed by the IPC [15]. The disadvantage of these techniques is that they provide narrowband results in discrete frequency points over a given frequency range of operation. Wideband measurements require building of a set of tuned test samples, and the measurement results then should be interpolated to build continuous frequency dependence. Another important shortcoming is the decrease of accuracy of measurements with an increase of resonance peak order, especially for samples with increased loss, *e.g.*  $> 5 \text{ Np/m}$ , or a  $D_f > 0.01$  [16].

“In-situ” measurement techniques, when transmission lines are directly built on the PCB laminate dielectric substrates, are preferable. Striplines have an advantage over microstrip lines because of the better electromagnetic field containment and less exposure of dielectrics and conductors to possible environmental humidity changes.

Since early 1990s, short-pulse propagation (SPP) technique has been used for broadband dielectric characterization of PCB materials. SPP technique uses time-domain oscilloscope in time-domain transmission mode on two identical lines of different lengths. SPP technique can be applied over a broad band up to 70 GHz, and even higher, when using very fast source excitations, low-loss transmission lines, and proper probes [17], [18], and [19]. However, the SPP technique has limited accuracy, especially at higher frequencies, because of the noise floor of time-domain detectors. When all frequencies are simultaneously used to reconstruct time-domain waveforms, the time-



domain pulses will contain embedded errors. In addition, it is difficult to separate losses due to conductors and dielectric.

For this reason, the frequency-domain technique using VNA is preferable for implementation of the traveling-wave method on PCB striplines. This technique has been described in [16], [20], and [21]. Conventionally, this technique has been called *S3*, and is based on measuring the full set of complex S-parameters of a test board with an appropriate “through-reflect-line” (TRL) calibration pattern. TRL calibration allows for eliminating port effects on measurements of S-parameters. Flow-chart of the algorithm to extract material parameters on single-ended PCB striplines is given in Figure 1.1 [22].

The algorithm as is shown in Figure 1.1 contains separation of conductor loss from dielectric loss. This separation is done by applying a simple “root-omega” procedure based on curve-fitting the total loss on the transmission line to  $\alpha_T = K_1\sqrt{\omega} + K_2\omega + K_3\omega^2$ , where  $\omega=2\pi f$  is the angular frequency. Then it is assumed that the  $\sqrt{\omega}$  part is associated with the conductor loss only. As is shown in the same paper [22], this assumption is no longer correct, if conductor surface roughness starts playing an important part, especially at frequencies above a few gigahertz. To employ any other techniques which takes into account surface roughness, cross-sectional analysis and at least preliminary information on the foil type used to build a particular test vehicle is required. However, for PCB test vehicles with *a priori* unknown cross-sectional geometries and conductor surface roughness profiles, this “in situ” S3 traveling-wave technique with “root-omega” procedure can be quite reasonable and effective way to extract DK and DF of laminate dielectrics. The problem with this technique is that an accuracy of extracting DK and DF reduces as frequency increases mainly due to

conductor surface roughness effects. This may lead to ambiguity of extracted dielectric data on the test vehicles with exactly the same dielectric, but different types of foil. However, this is the cost for lack of information about the cross-sectional geometry and roughness on the transmission line.

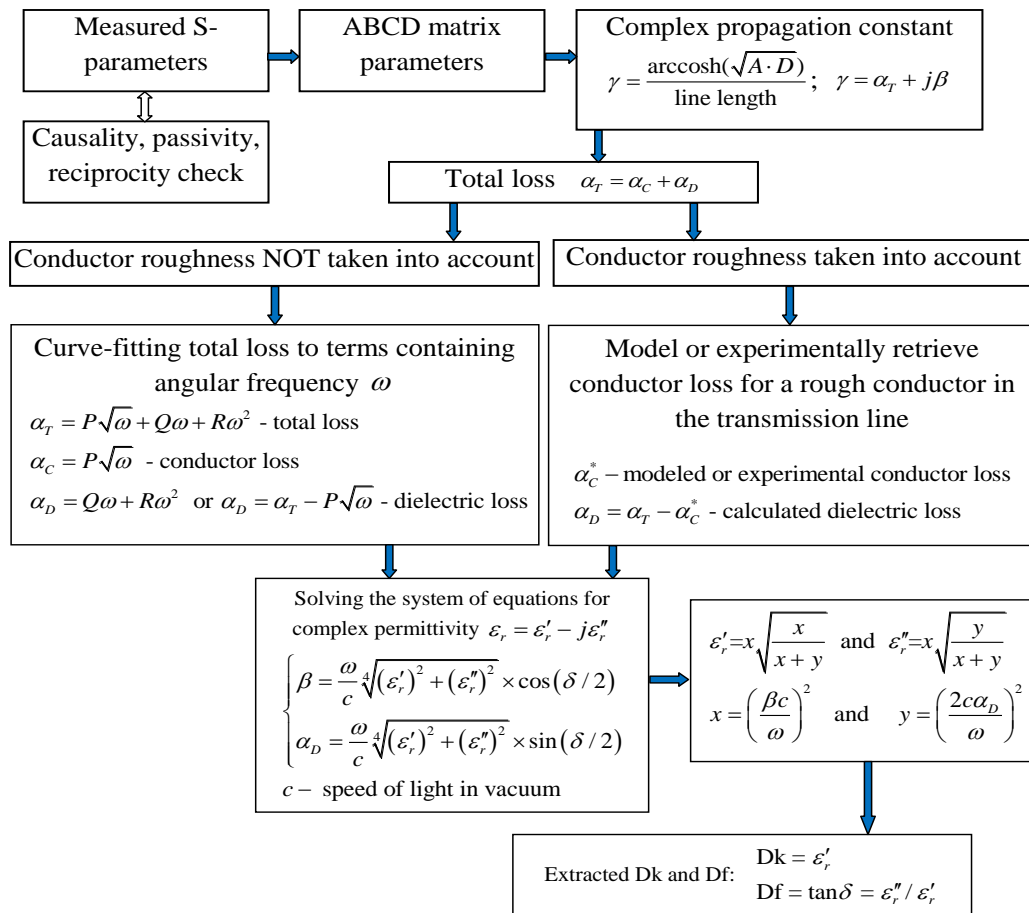


Figure 1.1 Flowchart of the PCB material extraction procedure from measuring S-parameters [22]

The frequency range of the *S3* technique currently is from 10 GHz to 30 GHz. These frequency limits are associated with the test vehicle layout, including TRL

calibration pattern design, and types of connectors used. The latter determines the specifics of connector footprint and via-to-trace transition design. The initial layouts of test boards with TRL calibration patterns and connector-via-trace transitions allow for conducting measurements in the frequency range below  $\sim 30$  GHz with 3.5-mm and 2.4-mm SMA connectors. Recently, a layout for a new test vehicle operating up to  $\sim 50$  GHz has been developed [23] and [24]. This test vehicle design had some modifications regarding connector-via-trace transition, ground via wall structure, and TRL calibration pattern design. However, practical realization of this design did not provide return loss and insertion loss on the line acceptable for accurate measurements of dielectric and conductor parameters over the entire frequency range up to 50 GHz. An extension of frequency range of measurements up to 50 GHz needs further serious improvements in the layout of the test vehicle. Herein, a new test vehicle design will be proposed based on the detailed analysis of possible sources of artifacts and errors leading to reduced accuracy of measurements, and optimizing the performance of the proposed design using electromagnetic numerical modeling (CST Microwave Studio, in particular).

The *objective of the present work* is to improve the S3 material parameter extraction technique. The improvement means obtaining more wideband measurements than available now on test vehicle with a new re-designed layout, and making this material extraction procedure more accurate even in the case of preliminary unknown cross-sectional geometries and roughness of foils. The latter challenge could be solved by collecting statistics on different types of foils and stripline geometries and developing “design curves”, which will allow a user for getting correct DK and DF data of the dielectrics under test by removing properly quantified roughness effects.

## 1.2. LAMINATE DIELECTRICS AND PCB STACKUP

Laminate dielectrics used in PCBs are typically intrinsically inhomogeneous composite dielectrics. They contain resin matrix, glass, and other, typically inorganic, reinforcement ingredients. PCB dielectric materials can be divided into *two major classes* based on the type of reinforcement used. The first group is comprised of *woven fiber-glass reinforced* dielectrics, and the second group is *dielectrics with non-woven glass reinforcements*. Woven glass reinforced laminates are less expensive than non-woven laminates, they are cheaper to manufacture, and hence they are more widespread. [25] and [26].

A scanning electron microscopy (SEM) picture of a cross-section of one of the striplines on the PCB is shown in Figure 1.2. One can see fiber-glass weaves embedded in a resin matrix. Additional crumbs are ceramic particles to enhance mechanical strength of the laminate dielectric.

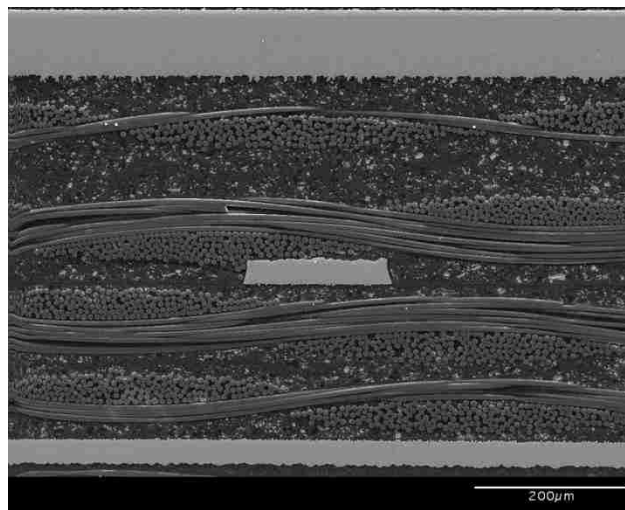


Figure 1.2 SEM picture of the PCB stripline cross-section

The glass used in laminates has a relative dielectric constant of around 6, while resin has dielectric constant around 3. Dielectric constants of PCB dielectrics differ depending on the glass/resin ratio. Because of the amount of glass in the woven glass cloth, the dielectric constants of laminates based on it are higher than of laminates based on other reinforcements.

Typical multilayer PCB stackup (see Figure 1.3) contains alternating layers of core and prepreg dielectrics.

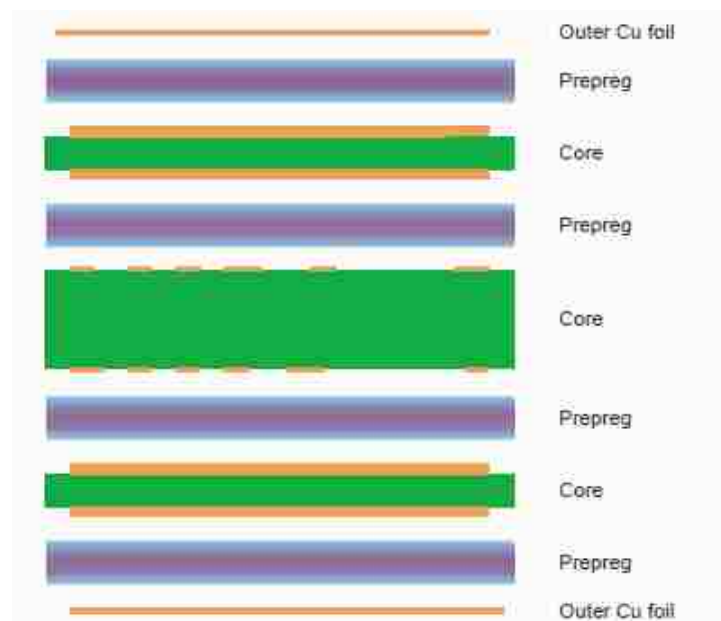


Figure 1.3 Typical multilayer stackup

Currently, a PCB may contain up to 20 layers or even more; most popular are the boards with 4-8 signal layers plus 4-8 ground layers. A core is a thin layer of a laminate dielectric with copper foil bonded to both sides of this layer, and this is a cured (hard)

fiber-glass resin composite. *Prepregs* are pre-impregnated fiber reinforcements or cloths that are used to manufacture composites. Prepreg in a multilayer PCB is typically the same fiber-glass resin composite, but uncured. Prepreg will cure, *i.e.*, harden when heated and pressed. Prepreg in striplines is used for dielectric to completely surround a signal trace. Signal trace typically has a shape close to trapezoidal. The wider (typically rougher) side lies on the core, while the narrower (which is typically smoother or of the different roughness) side of the conductor is in the prepreg

[27].

There are many different dielectrics that can be chosen depending on the requirements of the circuit. Some of these dielectrics are polytetrafluoroethylene (PTFE=Teflon), containing glass fibers and ceramic particles, and fire retardant dielectrics FR-4, FR-1, CEM-1 or CEM-3. Well-known prepreg materials used in the PCB industry are FR-2 (phenolic cotton paper), FR-3 (cotton paper and epoxy), FR-4 (woven glass and epoxy), FR-5 (woven glass and epoxy), FR-6 (matte glass and polyester), G-10 (woven glass and epoxy), CEM-1 (cotton paper and epoxy), CEM-2 (cotton paper and epoxy), CEM-3 (non-woven glass and epoxy), CEM-4 (woven glass and epoxy), CEM-5 (woven glass and polyester). Thermal expansion is an important consideration especially with ball grid array (BGA) and naked die technologies, and glass fiber offers the best dimensional stability. FR-4 is currently the most common material used. However, since 2000s, adoption of high-frequency thermoset materials (hydrocarbon resin/ceramic/woven glass) began to take place in the market, and available bond films (prepregs) that follow traditional epoxy/woven glass (FR-4) processing techniques made building multi-layer boards less complex [28].

PCB fibers are typically made of D-glass (DK =4.1-4.2 and DF=0.0025 @ 10 GHz); E-glass (DK=6.6-6.8 and DF=0.0070 @ 10 GHz), L-glass (DK< 5.0 and DF<0.005 and DF=0.0005 @ 10 GHz), NE-glass (DK=4.4-4.7 and DF=0.0035 @ 10 GHz), Li glass (DK=5.61 and DF=0.0034 @ 1 MHz), Silica Quartzel (DK=3.78 and DF=0.0001 @ 1 MHz and 10 GHz), S-glass, LTE-glass, and some others [29]. Glasses differ by their chemical composition, density, intrinsic porosity, elastic modulus, and thermal expansion coefficient. Physical and chemical properties of chosen glass affect morphology of fibers and the dielectric properties of glass and fiber-glass-filled composites.

Currently, there is much interest to an anisotropy and glass-weave effects in laminates containing woven glass, upon performance of high-speed interconnects. It has been shown that the frequency dispersion and loss of propagating signals depend on the signal trace routing with respect to the glass-weave orientation [30], [31], [32], and [33].

Because fiber-glass bundles lay almost in the layer plane, in-plane and out-of-plane dielectric properties of most laminates differ, causing anisotropy of dielectric properties. This may lead to significant discrepancy in the results obtained by techniques with different orientation of electric field with respect to the sample plane. When TEM wave propagates in a PCB stripline or microstrip line, the electric field is normal to the dielectric plane. For this reason, the data obtained by measurement techniques, where electric field lies in the sample's plane (*e.g.*, SPDR and SCR techniques, Nicolson-Ross-Weir technique in coaxial airline or a waveguide), cannot be directly used to PCB transmission lines, unless corrections due to anisotropy effects are made [34].

### 1.3. TYPES OF COPPER FOILS USED IN PCBs

The pressure to improve both dielectric substrates and copper foils to meet quality standards and better performance over as broad as possible frequency range has been constant, because data rates of electronic designs are steadily increasing. Greater uniformity and quality of materials comprising PCBs are demanded, and cost effectiveness is an important issue.

It is well-known nowadays that copper foil roughness greatly affects signal integrity, while signal integrity issues impact modeling, design, and material selection [16], [22], and [35]. At frequencies greater than  $\sim 2$  GHz the skin depth approaches the value of the copper foil roughness, and the measured conductor loss in PCB traces no longer conforms to the classical skin resistance models, so that signal integrity deteriorates. If designers knew how the frequency components may be degraded, some signal processing in the silicon could be done to compensate this degradation.

Copper foils used in PCB applications must be adhesively attached to a dielectric on the PCBs. Foils are typically either rolled, or electro-deposited with various treatments, and they differ greatly by their grain structure and surface roughness profiles [36]. The copper foil roughness contributes loss and dispersion on the line, leads to signal integrity problems, and affects eye-diagram closure, especially over GHz frequency range. Nowadays, it is obvious for designers of high-speed digital devices that copper foil roughness must be properly measured, quantified, and taken into account at the design stage [3]. Indeed, any numerical or analytical model of a realistic PCB transmission line requires accurate input DK and DF data of the laminate dielectric used, cross-sectional geometry of the line, its length, conductivity of smooth conductors, and conductor



roughness profile characterization. If dielectric properties of a laminate dielectric are measured using a transmission line technique, using a stripline or microstrip line, where the dielectric under study is adhesively attached to conductors, the parameters of the dielectric should be “cleaned” from the effects of coupling with the conductors.

Copper foil itself is inhomogeneous. It consists of the base copper layer (base, or drum foil) and treatment layers that are applied to the surfaces of the base foil to improve adhesion of the base foil to dielectrics and provide corrosion resistance. A typical structure of a foil is shown in Figure 1.4.

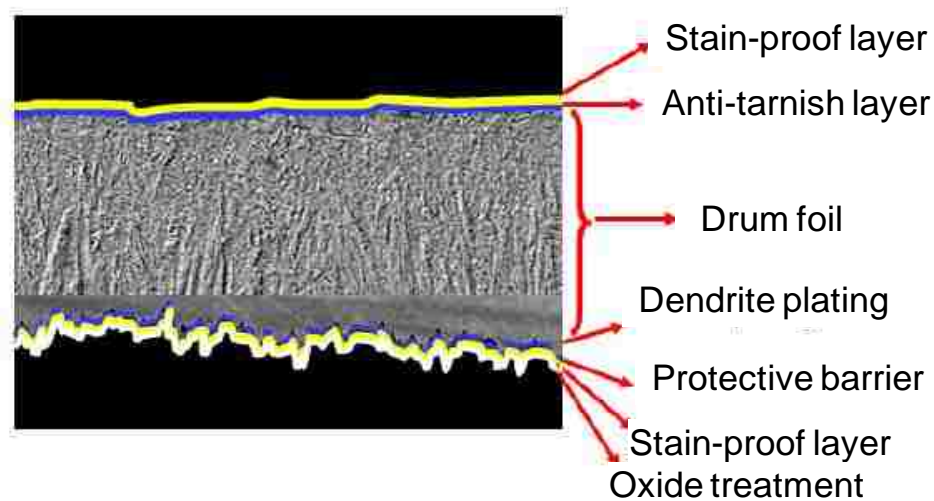


Figure 1.4 Structure of a copper foil on a dielectric surface [37]

As is mentioned above, base copper can be electrodeposited or rolled. The majority of PCBs are fabricated using electrodeposited copper foil. Electrodeposition (ED), schematically shown in Figure 1.5, produces high-purity copper, above 99.8% pure, which leads to high conductivity. The grain size and grain morphology, which

determine the strength and ductility of the copper, are controlled during the electrodeposition process. The copper is accumulated on the cathode surface of the titanium drum. The slower the drum speed, the thicker the copper gets. The copper surface on the drum side is smooth, while the opposite side is rough. The matte and drum side of the copper foil go through different treatment cycles so that the copper would be suitable for PCB fabrication. The treatments enhance adhesion between copper and dielectric interlayer during copper clad lamination. Treatments also act as anti-tarnish agents to stop or slow down copper oxidation [38].

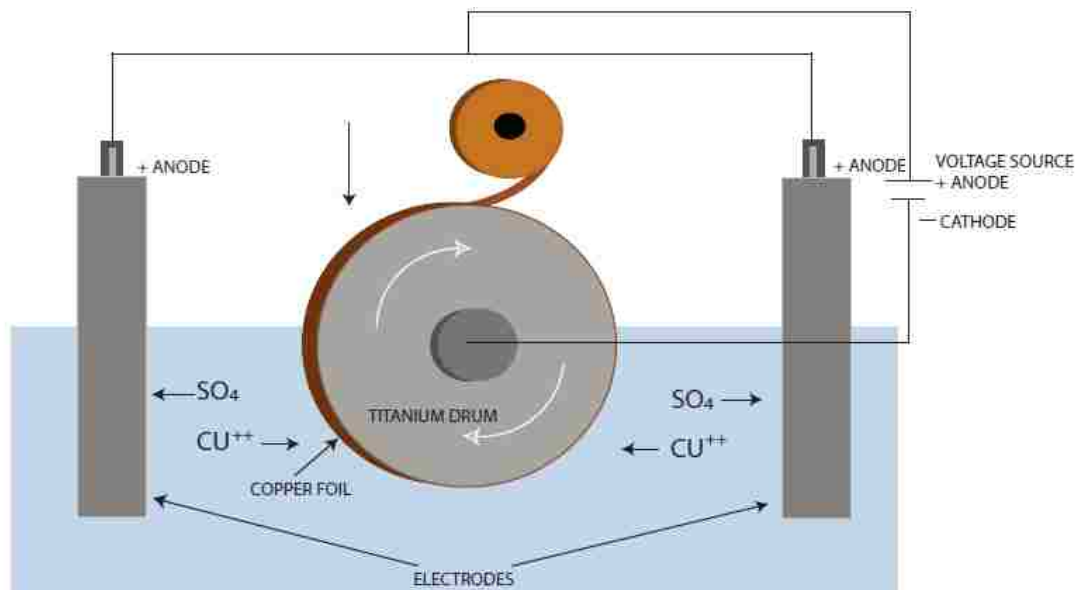


Figure 1.5 Electrodeposition copper manufacturing process [38]

The modern foil has small grain sizes, a couple of tenths of a micron or so on average. The grain size distribution is relatively narrow and the grains are equiaxed.

Another feature of the modern foil is the relatively smooth surface topography. Freestanding copper foils with thickness down to 7  $\mu\text{m}$  are already available. The thin copper, along with smooth surface topography, facilitates the fine-line etching of small features required to increase PCB functionality. On the other hand, thicker copper foils, which can be as thick as 400 microns, have good adhesion to high loss-tangent epoxies and polyimides. Application of thicker foils reduces the likelihood of delamination and cracking during thermal cycling. The thicker copper foils provide greater conductivity and improved thermal transport for some applications that have higher power requirements. Several copper foil treatments promote adhesion of the dielectric resin to the conductor in PCBs. The primary adhesion promoting treatment is micro-roughness added in the form of microscopic granules of copper metal plated onto the copper foil surface. Typically, less surface treatment is used to provide a smoother interface for etchability and electrical performance at high frequencies. Additional treatment is often used to enhance adhesion for more brittle and higher loss-tangent dielectrics that have intrinsically poor adhesion. A chemical adhesion promoter, typically a silane, is applied to the bond micro-roughened surface, which serves as a bridge between the resin and the base foil. A barrier layer is another treatment applied to copper foil to promote adhesion. It consists of a brass or zinc layer 800-1200 angstroms thick that is applied immediately after the nodule treatment. The barrier layer inhibits diffusion and contact of copper metal with certain dielectric components such as dicyandiamide. When the laminate is heated, dicyandiamide can interact with copper causing adhesion loss. The barrier layer inhibits the interaction and the associated adhesion loss. Finally, stabilization treatment is applied to both surfaces of the copper foil. This layer, 25 to 50

angstroms thick, is typically an oxide of chromium or chromium alloys, such as zinc-chromium [38].

Copper foil surface topography depends upon the base foil and treatments and plays a critical role in the performance of a PCB. The base foil roughness component (profile) is present on the side of the foil opposite the plating drumside surface. It is influenced by drum surface topography, additive adsorption, deposit defect structure, and mass transfer limitations. Thicker foils typically have greater profile. The treatment component is the nodule treatment described above and can be present on either or both foil surfaces.

There are several groups of foils depending on their roughness profiles. Standard foil (**STD**) is the roughest one. Its average peak-to-valley amplitude  $R_z$  may range from 5 to 20  $\mu\text{m}$  on the roughest *foil side*, which directly penetrates a dielectric in both striplines and microstrips. The foil side has maximum treatment for better adhesion with a dielectric. The opposite *oxide side* of an STD foil is typically very smooth ( $R_z < 1 \mu\text{m}$ ).

Very-low-profile (**VLP**) and hyper/super-very-low-profile (**HVLP/SVLP**) foils with the minimum treatment required for adhesion have been developed to address signal integrity issues. Roughness levels on both sides of these foils are lower than those on the foil side of STD foil. For VLP, the roughness amplitude  $R_z$  typically ranges from 2 to 5  $\mu\text{m}$ , and for HVLP, it is less about 1-3  $\mu\text{m}$  on either foil or oxide side. These foils use some additives to suppress profile growth during electrodeposition. Thinner foils, which are made possible by advances in producing higher foil strength, yield lower profiles, since roughness has less time to develop.

Reverse treated foils (**RTF**) involve the treatment of the smooth side of the electrodeposited copper. Thin treatment layers improve adhesion of the base foil to dielectric and provide corrosion resistance, which makes the shiny side rougher than it was before. This treated side of copper is laminated to the dielectric material. The fact that the treated drum side is rougher than the other side constitutes a greater adhesion to the dielectric, which is advantageous over the standard ED copper. The matte side does not require any mechanical or chemical treatment before applying a photoresist – it is already rough enough for good adhesion.

Electrodeposited copper crystals (dendrites) tend to grow perpendicular to the foil plane, and they form spikes, as is shown in Figure 1.6. Rolled copper, if untreated, is the smoothest, because copper crystals are broken during rolling process, and their shape is spherical or hemispherical. Shape of copper roughness profile is important for loss and frequency dispersion analysis on the line, since it affects interaction of electromagnetic waves in the transmission line with the inhomogeneous copper-dielectric interface.

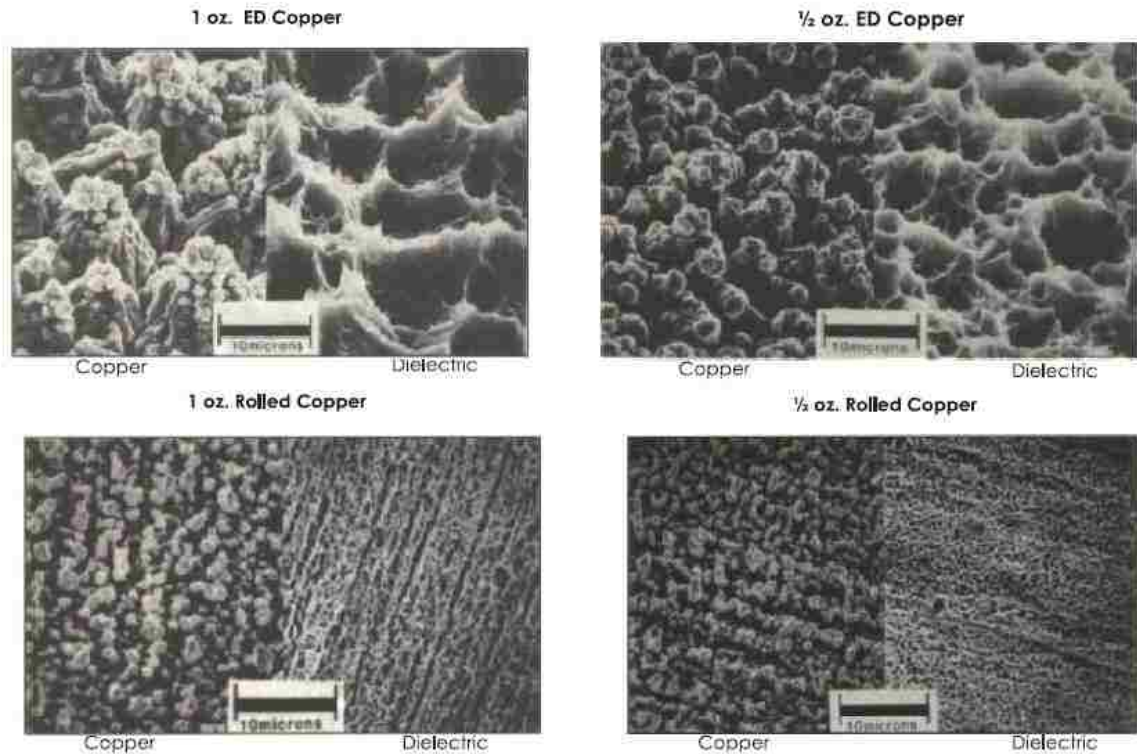


Figure 1.6 SEM pictures of roughness on the treated size of the 0.5 oz ED and rolled copper foils [38]

#### 1.4. LIMITATIONS ON FREQUENCY OF MEASUREMENTS DUE TO CONNECTORS

Currently, “in-situ” characterization of both laminate dielectrics and copper foils using travelling-wave techniques on PCB transmission lines can be done only up to about 50 GHz. The upper frequency limit is associated with the problems of effective signal launch to the PCB lines and the necessity of using special wideband low-loss SMA connectors and their matching with PCB transmission lines, which requires special connector-via-trace design [39] and [40]. The advantage of SMA connectors is that they are easy to attach a precision 50-Ohm coaxial cable to, and once attached, they are robust.

However, they have a number of significant drawbacks. Though the bandwidth of an SMA connector itself maybe in excess of 50 GHz, the artifacts it introduces in the test board can often be seen at much lower frequency. This is usually due to the vias required in the board to plug in the SMA. If this structure is not optimized, the SMA can introduce artifacts of either inductive or capacitive nature. The SMA is physically large in size and with cable attached, there is a limit to how closely spaced they can be mounted to a board. An SMA, in the best case, looks like a 50-Ohm stub about 0.5 inches long, but at Gbps rates it may cause the performance of the test board to degrade.

The problems with SMA connectors can be eliminated by using microprobes and special RF/microwave microprobe stations for testing losses on PCBs. Microprobing can dramatically increase quality of material characterization measurements. However, a test board should be specifically designed for microprobing so that there will be adjacent return connections to all signal paths. The physical dimensions of the probe can be very small, and hence its parasitics very low. Microprobes can have either 50-Ohm or controlled high impedance for active probing [41]. They are commonly used for probing high-speed PCBs, including motherboards and backplanes, where mechanical constraints like size, SMT components, connectors, and daughtercards present measurement and probing challenges. Accurate measurement of losses on PCBs, connectors and ICs require careful set-up of high frequency probes when using VNA or TDR. Probe stations contain a probing stage and a micro-positioner that can be adjusted on the X-Y-Z-theta directions, and can probe samples of various shapes and sizes. Microprobe stations may be used over wide frequency range up to 110 GHz, provided that the proper microprobes and millimeter-wave network analyzers are employed [42]. The main problems with

microprobing stations are their cost, relative complexity of using, which needs special training of personnel, and availability at test facilities.

In this work, the design of a 50-GHz test vehicle for “in-situ” dielectric and copper foil characterization is considered. This is a test board with 2.4-mm SMA connectors for using VNA to conduct two-port S-parameter measurements on PCB single-ended striplines. Similar to its 20-GHz and 30-GHz prototypes, it contains TRL calibration pattern [20], [21]. However, its connector-via-signal trace transitions are optimized to assure for the most broadband performance.

The structure of the work is the following. Section 2 of this thesis contains the analysis of the major errors and uncertainties, which may occur at the measurements of dielectric parameters of PCB laminate dielectrics. Since surface roughness is one of the important artifacts affecting accuracy of measurements, it is important to have a metric to take it into account. The new procedure and algorithm to capture and quantify cross-sectional geometry of PCB transmission lines and conductor surface profile on the signal trace are described in Section 3. Based on the statistics of the cross-sectional analysis of numerous test vehicles and measuring their S-parameters, “design curves” to correlate geometrical roughness parameters with the effective roughness dielectric layer, have been identified and built in Section 4. These “design curves” can be used in the models of PCB designs. Section 5 describes the new design of the 50-GHz test vehicle. Conclusions are summarized in Section 6.



## 2. MAJOR ERROR AND SENSITIVITY ANALYSIS FOR PCB MATERIALS CHARACTERIZATION

Systematic and random errors are always present in measurements. To provide reliable measurement results of dielectric properties (DK and DF) of PCB dielectrics, it is important to identify sources of the major errors and determine sensitivity of measurements to various artifacts on printed circuit boards, peculiarities of measurement methodology, and instruments used. Impact of these factors on accuracy of measurements of dielectric properties must be quantified.

PCB designers prefer to use low-loss dielectric materials in PCBs to achieve better performance of their designs at data rates over 10 Gbps. However, an accuracy of measurements of DK and DF may become a serious issue for broadband measurements as frequency increases. Achieving satisfactory accuracy of measurements is especially difficult for short test lines and when measuring dielectric materials with very low loss.

Some sources of trouble regarding errors in DK and DF measurements have been listed in [23]. To name a few sources, these are

- an imperfect TRL calibration pattern and procedure;
- non-identical mounting of connectors on the test board, which may lead to TRL calibration failure;
- non-ideal connector-via-trace transitions on the test board, which may cause parasitic resonances and limit frequency range;
- conductor surface roughness if not properly taken into account;
- presence of parasitic resonances, *e.g.*, due to periodic structure of ground via walls;

- and intrinsic test fixture artifacts, *e.g.*, inhomogeneous width of a trace, which causes significant variation of impedance along the propagation path.

It was stated in [23] that the systematic and random errors arising from the measurements using TRL-calibrated test vehicles over the frequency range below 20 GHz are comparatively low and almost do not affect the quality of designs using such PCBs. However, as the upper frequency limit of measurements is increased from 20 GHz to 50 GHz, errors and uncertainties, associated with the measurement technique, may become significant.

Two groups of errors associated with the “in-situ” travelling-wave *S3* method have been identified [43]. The first group includes *repeatability (manufacturing variability)* errors, and the second includes *systematic (or reproducibility)* errors. Repeatability errors are quantified for the tests performed on multiple test boards with the same dielectric taken from the same manufacturer and the same batch. Systematic errors of measurements occur when testing a single test vehicle, and are associated with the peculiarities of the test vehicle design and methodology of measurements.

The *objective of this Section* of the work is to present quantification and analysis of the major errors and uncertainties in the test vehicles with currently existing layout and 2.4-mm connectors up to at least 30 GHz.

## 2.1. REPEATABILITY, OR MANUFACTURING VARIABILITY, ERRORS

Repeatability, or manufacturing variability, errors arise due to physical difference between the boards. There are always some manufacturing variations within some tolerance ranges in the signal trace width and thickness, dielectric thickness, in copper surface roughness (both on foil and oxide sides), and in resin/fiber contents. Therefore the extracted data (DK and DF) may differ from sample to sample within the same set of PCBs, even if the same measurement and material parameter extraction methodology is applied.

Figure 2.1 shows the measured magnitudes of  $S_{11}$  and  $S_{21}$  (in dB) for three test boards (“samples”) with the line length of 15,410 mils (391.41 mm). All three samples are from the same manufacturer and from the same batch, *i.e.*, have the same dielectric, the same foil, and identical geometry, as this is possible within manufacturing tolerances (<10% variation for any dimension). Slight differences in the measured S-parameters translate into some differences in the extracted DK and DF data, as shown in Figure 2.2. At 10 GHz, the discrepancy in DK is 0.69%, and in DF is 2.8%.

Causality and passivity of S-parameters are important for eye diagram formation and jitter analysis. Therefore, before doing any extraction of DK and DF, the measured S-parameters are checked for passivity and causality. All samples exhibit passivity. They also comply with causality for the entire frequency range of measurements (10 MHz – 30 GHz), but within some predetermined error limits. Non-causality errors are determined through the difference between the measured  $\text{Im}(S_{21})$  and the causal  $\text{Im}(S_{21})_c$ , reconstructed from  $\text{Re}(S_{21})$  based on the procedure described in [44]. Thus, for Samples 1, 2, and 3, the calculated average non-causality errors are 1.5%, 0.6%, and 0.25%,

respectively, and the maximum non-causality errors are 8.9%, 4.5%, and 3.7%, respectively. These errors allow for passing the causality tests, if the average error limit is set as 2%, and the maximum error is 10%.

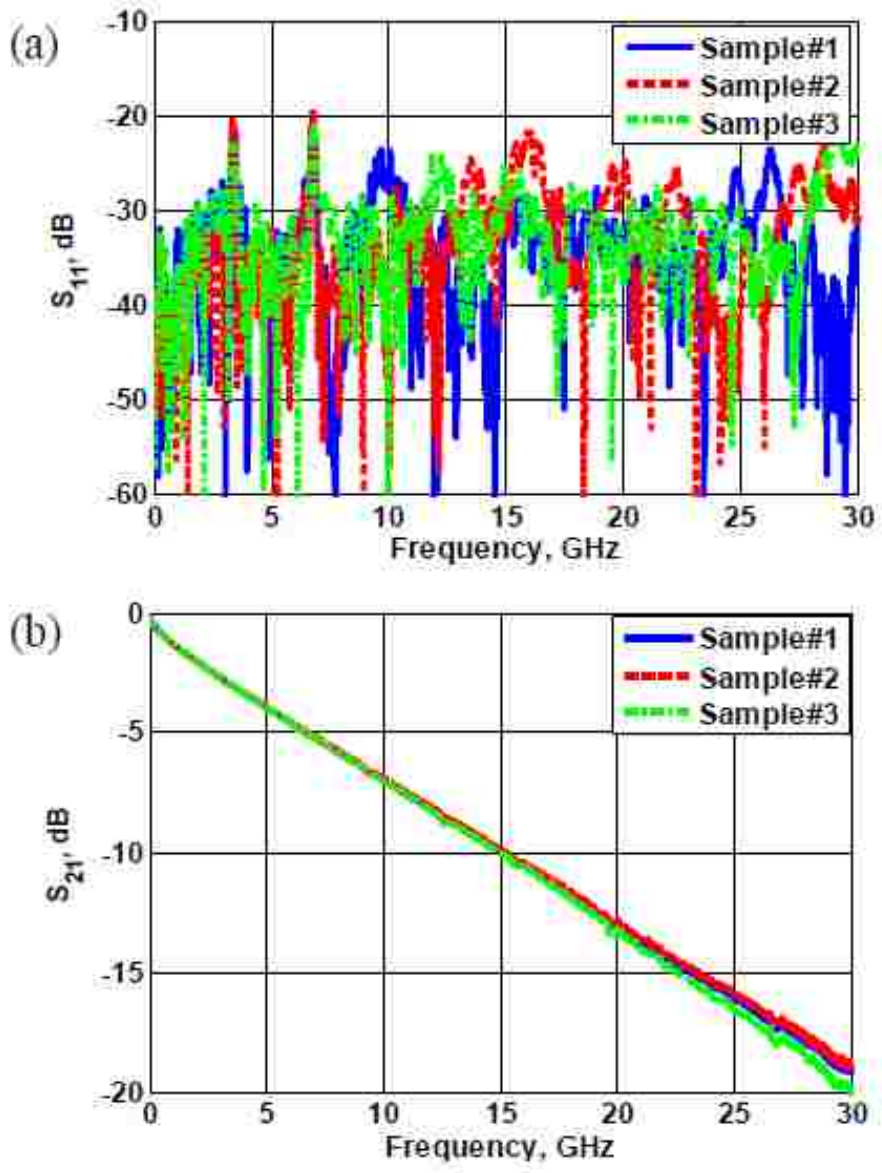


Figure 2.1 Measured return loss (a) and insertion loss (b) for three samples of the same set of test vehicles; line length is 15,410 mils

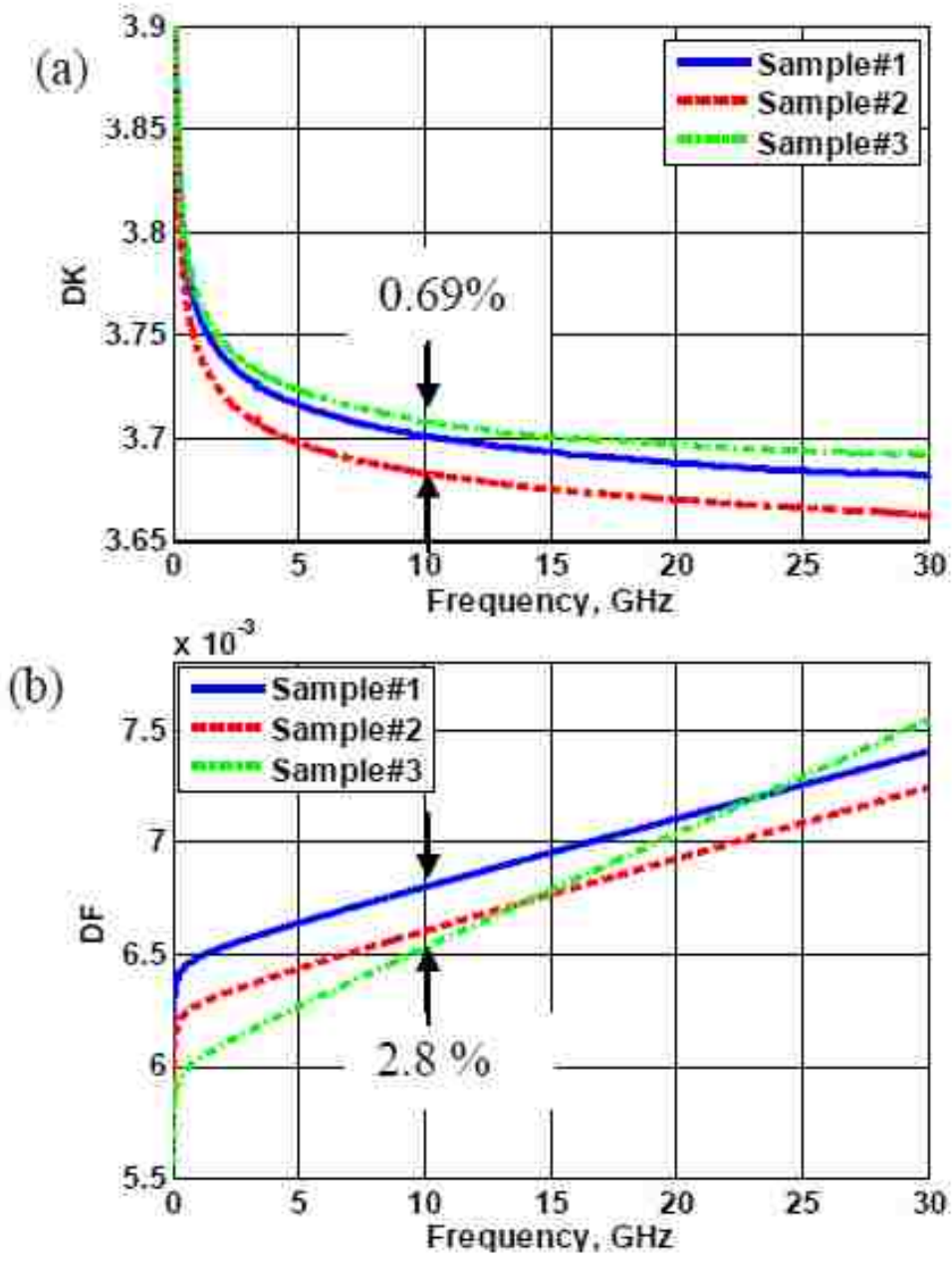


Figure 2.2 DK (a) and DF (b) extracted using “root-omega” procedure for three samples of the same set

The maximum (upper-bound) repeatability errors in DK and DF can be evaluated starting from the definitions:

$$DK = \varepsilon'_r = \left( \frac{c}{2\pi} \right)^2 \left( \frac{[\varphi_{21}]}{l \cdot f} \right)^2 \quad (2.1)$$

and

$$DF = \tan \delta = \frac{\varepsilon''_r}{\varepsilon'_r} = \frac{-|S_{21}^{dB}|_D}{4.343 \cdot [\varphi_{21}]}, \quad (2.2)$$

where  $[\varphi_{21}]$  is the measured unwrapped phase of  $S_{21}$  in radians,  $l$  is the length of the test line,  $c$  is the free space velocity, and  $f$  is the frequency in Hz. In (2.2), the value  $|S_{21}^{dB}|_D$  is the insertion loss associated with only dielectric part.

Then the increment (variation) in DK is obtained through the differential with respect to phase  $[\varphi_{21}]$

$$\Delta DK = \frac{\partial DK}{\partial([\varphi_{21}])} \Delta[\varphi_{21}], \quad (2.3)$$

resulting in

$$\Delta DK = \left( \frac{c}{2\pi} \right)^2 \cdot \frac{2}{(l \cdot f)} \cdot [\varphi_{21}] \cdot \Delta[\varphi_{21}]. \quad (2.4)$$

Similarly, the increment (variation) in DF is obtained through the corresponding partial derivatives as

$$\Delta DF = \left( \frac{\partial DF}{\partial(-|S_{21}^{dB}|_D)} \Delta(|S_{21}^{dB}|_D) \right) + \left( \frac{\partial DF}{\partial([\varphi_{21}])} \Delta[\varphi_{21}] \right), \quad (2.5)$$

resulting in

$$\Delta DF = \frac{1}{4.343} \cdot \left( \frac{\Delta|S_{21}^{dB}|}{[\varphi_{21}]} + \frac{\Delta[\varphi_{21}]}{[\varphi_{21}]^2} \right). \quad (2.6)$$

The parameters  $\Delta|S_{21}^{dB}|$  and  $\Delta[\varphi_{21}]$  herein are the maximum differences of the corresponding measured values for all the boards within the same test set.

The repeatability errors are quantified for the set of three boards with the measured S-parameters as in Figure 2.1. Figure 2.3 shows the maximum repeatability errors calculated using (2.4) and (2.6) together with the actual “measured” deviations directly obtained from the extracted DK and DF as in Figure 2.2.

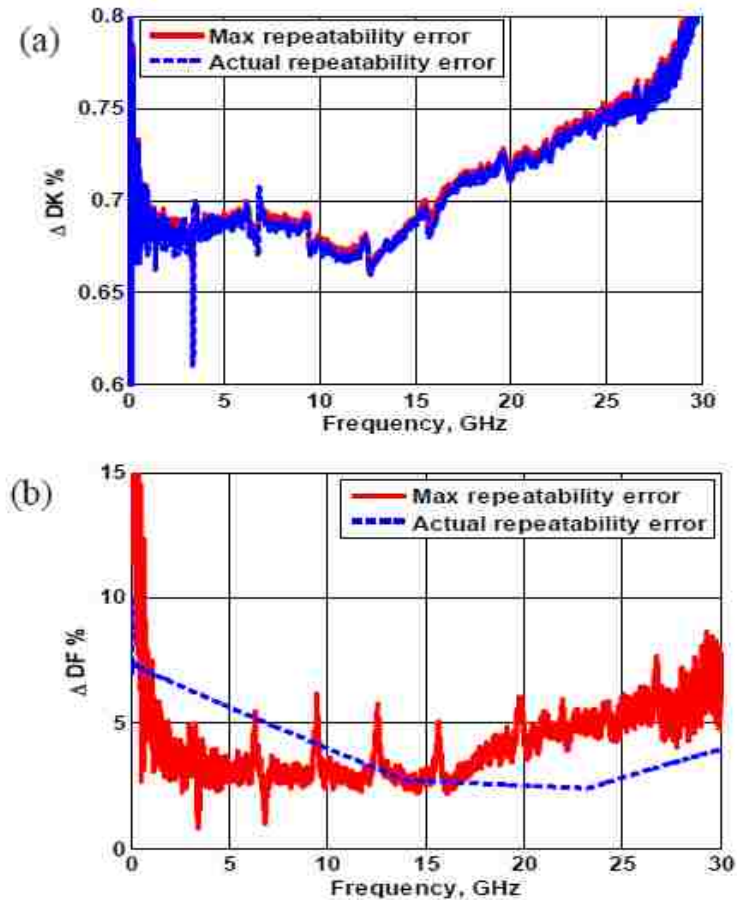


Figure 2.3 Actual “measured” and calculated maximum repeatability errors in DK (a) and in DF (b) for three samples of the same set

The repeatability error for DK extraction in this case is comparatively low (<0.8%) over the entire frequency range of measurements, except for the most low-frequency part (<300 MHz), as is seen from Figure 2.3 (a). The low-frequency systematic error is associated with the conductor-dielectric interface effect, and will be discussed in sub-section 2.3.

Figure 2.3 shows the presence of periodic peaks in the maximum repeatability errors. They are most likely due to the periodic via walls at every 2.5 cm (~ 1 inch) along the test line on each board. These via walls cause periodic enhanced reflections, which affect the measured return loss and insertion loss as in Figure 2.1. The calculation of maximum repeatability errors employs the measured  $S_{11}$  and  $S_{21}$ , and hence, via wall effects are incorporated in the maximum repeatability errors. The actual repeatability error for DF is comparatively smooth, because it is obtained after DF values are extracted in “root-omega” procedure, which uses curve-fitting.

It is important to note that various *artifacts* in one or a few boards within a set, *e.g.*, connector-via transition defects, violation of translational invariance (trace defects), TRL calibration imperfectness, may also affect measured S-parameters and curve-fitting to  $\sqrt{\omega}$ ,  $\omega$ , and  $\omega^2$  in the *S3* method [22].

As a result, the actual “measured” repeatability error may be higher than the maximum evaluated one. Therefore, if possible, such artifacts should be eliminated, and S-parameters re-measured.



## 2.2. SYSTEMATIC, OR REPRODUCIBILITY, ERRORS

Systematic, or reproducibility, errors are associated with the chosen measurement technique and instrumentation, and peculiarities of test board design, *e.g.*, imperfect TRL calibration pattern. These errors in the current work depend on the quality of SMA connectors, including variation in resistance at pad-connector interface; identical mounting of SMA connectors, including variation in mounting torque; positional variation of cables, which may lead to phase shift; and zero drift of VNA. These errors are calculated through sensitivity of indirectly measured values of DK and DF to the directly measured S-parameters as

$$\delta(DK) = \left(\frac{c}{2\pi}\right)^2 \frac{2}{(l \cdot f)^2} \cdot [\phi_{21}] \cdot \delta[\phi_{21}] \quad (2.7)$$

and

$$\delta(DF) = \frac{c}{\omega \cdot l \sqrt{\epsilon'_r}} \left( \frac{|S_{11}|^2}{1 - |S_{21}|^2} + \frac{|-S_{21}^{dB}|}{8.686} \cdot \frac{\delta(DK)}{\epsilon'_r} \right). \quad (2.8)$$

The formula (2.7) for the systematic error of DK is similar to (2.1), but  $\delta[\phi_{21}]$  term in (2.7) is the systematic error of measuring phase of  $S_{21}$  in the travelling-wave method. The derivation of the systematic error for DF (2.8) is given Section 2.4. The accuracy of measuring DF mainly depends on the reflection loss: the higher loss results in the higher error. According to (2.8), if loss on the line is low ( $|S_{21}| \rightarrow 1$ ), the error of determining DF would increase. This is obvious: it is always more difficult to measure accurately

materials with very low loss. The systematic error also increases if frequency is low, DK is low, and the test line is short.

The question is how well the test board should be matched so that the reflection loss should be acceptable for accurate measurements of DF? The sensitivity analysis should be done to answer this question.

Figure 2.4 illustrates the maximum acceptable level of the magnitude of  $S_{11}$ , which provides the given limit of  $\Delta DF$  error. Figure 2.4 (a) shows the actual measured return loss (thick red curve); the “unacceptable” return loss, artificially elevated by 6 dB (thin black curve); and the trial  $|S_{11}|$  limit set to -19 dB (dashed magenta line). The corresponding  $|S_{21}|$  curves are given in Figure 2.4 (b). The  $|S_{21}|$  curves calculated from the elevated  $|S_{11}|$  and from the trial  $|S_{11}|$  limit are obtained from the power balance

$$|S_{11}|^2 + |S_{21}|^2 + \kappa_P = 1 , \quad (2.9)$$

where  $\kappa_P$  is the power absorption coefficient, which depends only on the loss in the dielectric.

Figure 2.4 (c) shows the corresponding calculated  $\Delta DF$  levels for the actual measurements (thick red line); for the elevated  $|S_{11}|$  (thin black line); for the trial  $|S_{11}| = -19$  dB level (dashed magenta line); and the acceptability limit for  $\Delta DF$  defined as 10%. Figure 2.4 (c) shows, that if  $|S_{11}|$  trial limit of -19 dB is exceeded, unacceptable systematic errors may occur at some frequencies. The low-frequency ( $f < 300$  MHz) error will be discussed below.

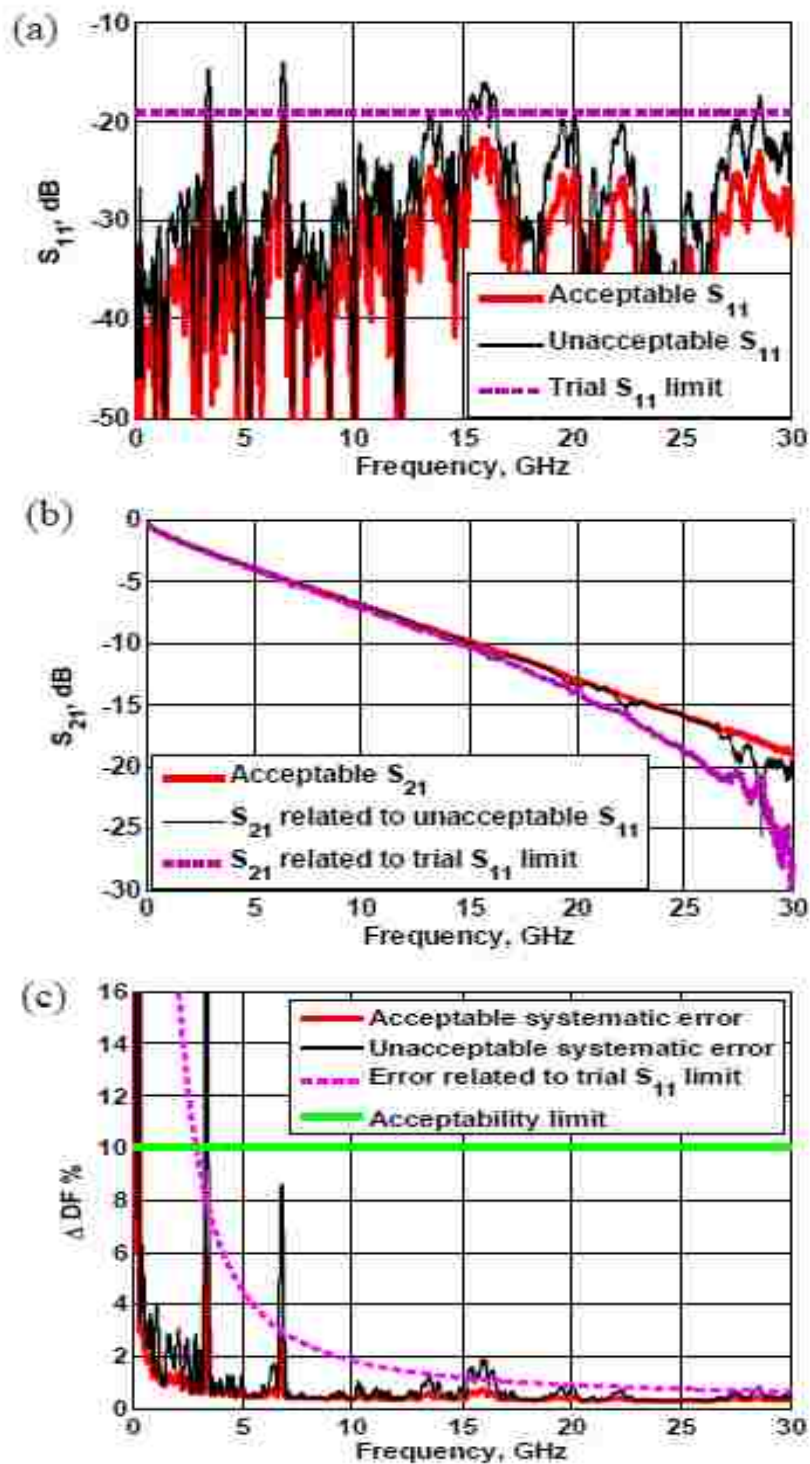


Figure 2.4 Acceptable and unacceptable levels of measured return loss (a), insertion loss (b), and systematic error for DF (c)

### 2.3. SYSTEMATIC AND REPEATABILITY ERRORS AT LOWER FREQUENCIES

Low-frequency extraction of dielectric properties using the simple “root-omega” procedure gives an incorrect increase in DK as frequency decreases. It can be shown that this is a *systematic error due to the presence of the  $\sqrt{\omega}$  component in the phase constant  $\beta$*  on the line. This component appears because of the dielectric-metal interface.

The  $\sqrt{\omega}$  term should be removed in future extractions of DK and DF data. This is illustrated by Figure 2.5. When  $\sqrt{\omega}$  is removed, the lines of DK become flatter, following the Debye-like behavior with a slight decrease of DK as frequency increases. The DF curves do not change significantly, except for the lower frequencies (<5 GHz).

As is mentioned above, the repeatability errors are also affected by the  $\sqrt{\omega}$  term in  $\beta$ . If this term is removed, the repeatability errors in DK and DF shown in Figure 2.6 may be different from those in Figure 2.3. The blue dashed line corresponding to the actual measured repeatability error in DK in Figure 2.6 (a) is smoother than the corresponding curve in Figure 2.3 (a). This smoothening is caused by the curve-fitting of the total measured phase constant as

$$\beta = B_1\sqrt{\omega} + B_2\omega + B_3\omega^2. \quad (2.10)$$

The removal of  $\sqrt{\omega}$  from  $\beta$  results in a straight dash-dot line in the DK error frequency dependence shown in Figure 2.6 (a). The error for DF turns out to be almost unaffected by the  $\sqrt{\omega}$  term in  $\beta$ , and Figure 2.6 (b) and Figure 2.3 (b) are almost identical.

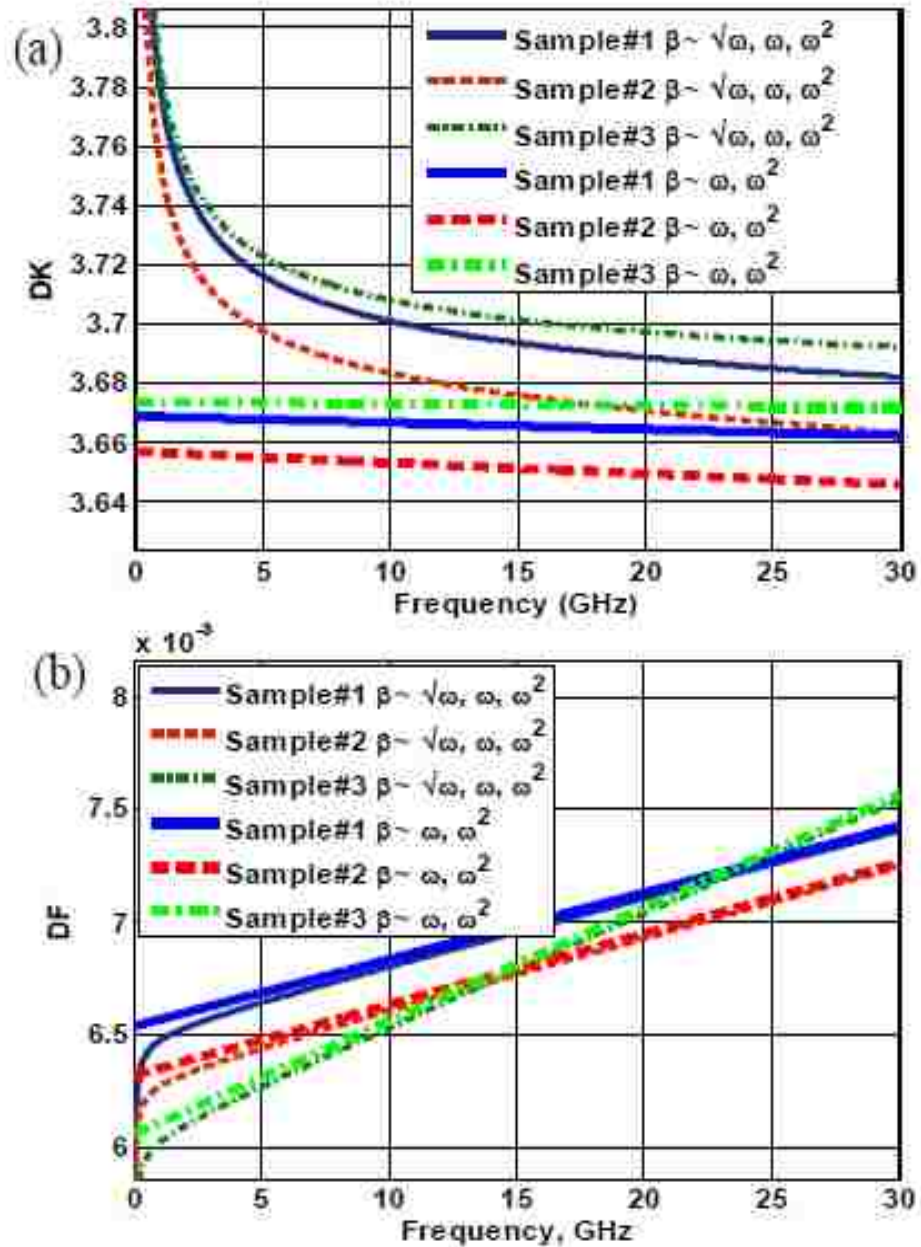


Figure 2.5 Effect of the removal of the  $\sqrt{\omega}$  component from  $\beta$  on the extracted DK (a) and DF (b) values for three samples

The difference between the phase constant  $\beta$  measured from the S-parameters [21] and the curve-fitted as (2.10) is presented in Figure 2.7 (a). This difference is

relatively low compared to the measured values of the total  $\beta$ . Figure 2.7 (b) shows two curves: the dashed blue line corresponds to the relative fitting error, when  $\beta$  is fitted as (11) with  $\sqrt{\omega}$  term, while the magenta solid line corresponds to the case, when the term  $\sqrt{\omega}$  is removed from  $\beta$ .

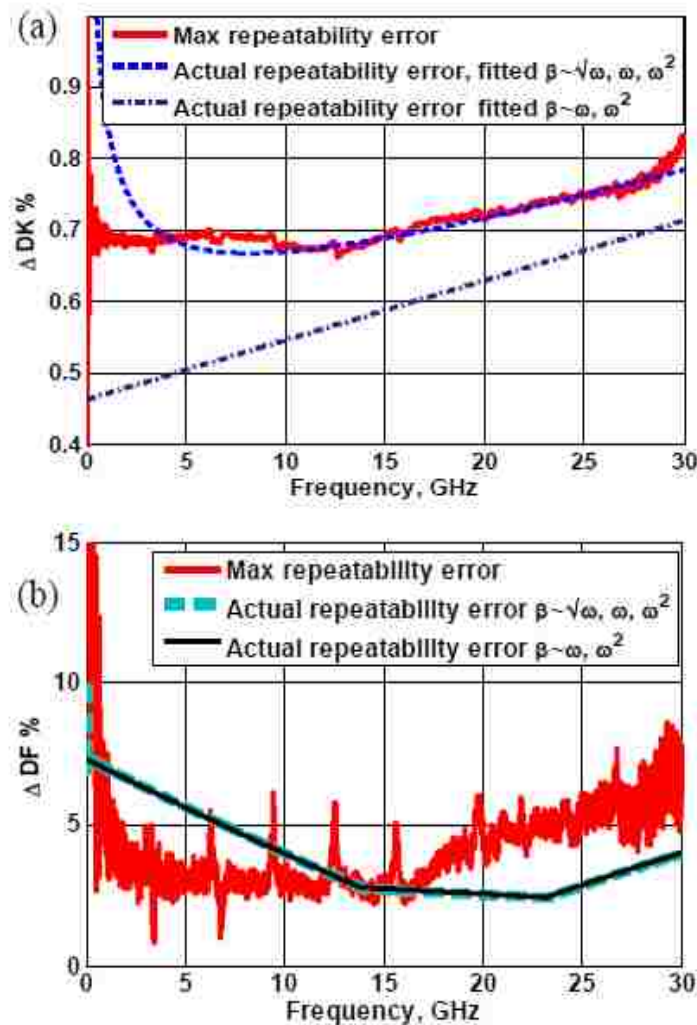


Figure 2.6 Effect of the removal of the  $\sqrt{\omega}$  component from  $\beta$  on the repeatability error in DK (a) and in DF (b)

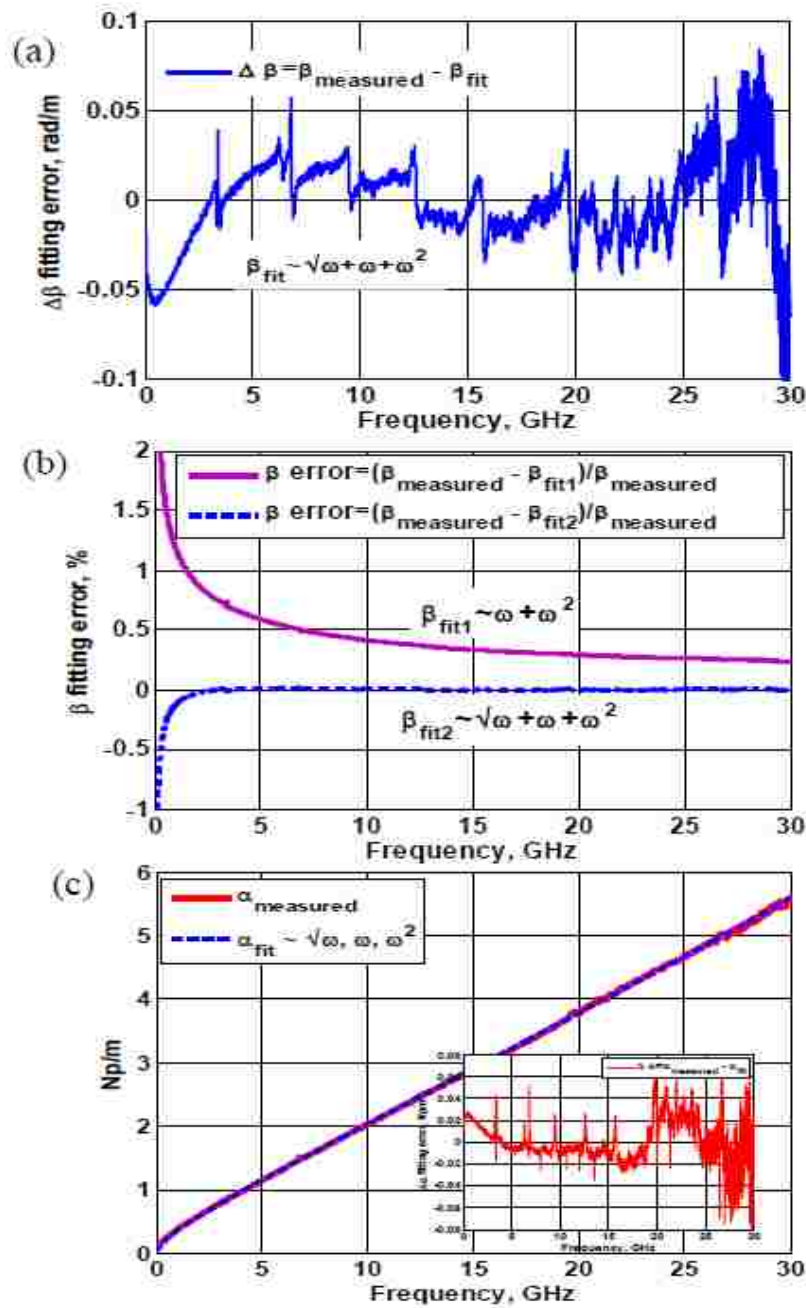


Figure 2.7 Difference between the measured and fitted  $\beta$  (a), relative errors between the measured and fitted  $\beta$  with and without the  $\sqrt{\omega}$  term (b), and the difference for  $\alpha$  (c)

The negligibly small difference between the measured and curve-fitted as  $\alpha = K_1\sqrt{\omega} + K_2\omega + K_3\omega^2$  attenuation constant on the line is shown in Figure 2.7 (c). In the

“root-omega” extraction procedure, the  $\sqrt{\omega}$  term in  $\alpha$  is associated with conductors, since skin-effect in metal behaves as  $\sqrt{\omega}$ , and the rest part, containing  $\omega$  and  $\omega^2$ , belongs to the dielectric. As is shown in [22], this is not quite correct, since conductor roughness couples to both “smooth” conductor and dielectric losses. However, for a single PCB with unknown geometry and conductor roughness, there is no other currently existing way to split conductor and dielectric loss. The development of such “design curves” to properly split unknown dielectric parameters from conductor effects is the future work, and it will be based on the detailed analysis of vast statistical data regarding possible types of foils and possible stripline geometries.

#### 2.4. DERIVATION OF SENSITIVITY FORMULAS

Herein, the mismatch on the line is taken into account in the uncertainty calculation for the DK and DF extraction. In the material parameter extraction procedure, as described in [21]. and [22], S-parameters are converted to ABCD matrix, and then the parameter A is used to calculate the complex propagation constant [45].

$$\gamma = \frac{\cosh^{-1}(A)}{l} = \alpha + j\beta, \quad (2.11)$$

where

$$A = [(1 + S_{11})(1 - S_{22}) - S_{12}S_{21}] / (2S_{21}). \quad (2.12)$$

If there is a mismatch, then  $A = A_0 + \delta A$ , where  $A_0$  corresponds to the matched case, and  $\delta A$  is a relatively small deviation  $|\delta A| \ll |A|$ .



If the network is reciprocal and symmetrical, then

$$A = \frac{1 - |S_{11}|^2 + |S_{21}|^2}{2|S_{21}|}, \quad (2.13)$$

which can be rewritten as

$$A = \left( \frac{1 + |S_{21}|^2}{2|S_{21}|} - \frac{|S_{11}|^2}{2|S_{21}|} \right) e^{-j|\phi_{21}|}. \quad (2.14)$$

Then

$$A_0 = \left( \frac{1 + |S_{21}|^2}{2|S_{21}|} \right) e^{-j|\phi_{21}|} \quad (2.15)$$

and

$$\delta A = \left( -\frac{|S_{11}|^2}{2|S_{21}|} \right) e^{-j|\phi_{21}|}. \quad (2.16)$$

If reflection loss  $|S_{11}| \rightarrow 0$ , then  $|\delta A| \rightarrow 0$ .

For

$$|\delta A| \ll |A_0|, \quad \gamma l = \cosh^{-1}(A_0 + \delta A) \approx \cosh^{-1}(A_0) + \frac{d(\cosh^{-1}(A))}{dA} \delta A. \quad (2.17)$$

Since

$$\frac{d(\cosh^{-1}(A))}{dA} \approx \frac{1}{\sqrt{A^2 - 1}} \text{ for } A \neq 1, \quad (2.18)$$

Then, since  $\delta A$  term in the total complex phase  $\gamma l$  (2.17) would mainly affect the loss part,

$$\gamma l \approx \cosh^{-1}(A_0) + \delta \alpha \cdot l, \quad (2.19)$$

while  $j \cdot \delta\beta \cdot l \rightarrow 0$  , then

$$\delta\alpha = \frac{\delta A}{\sqrt{A^2 - 1}} \Big|_{A=A_0} \approx \frac{|S_{11}|^2}{1 - |S_{21}|^2} \cdot \frac{1}{l}. \quad (2.20)$$

Since loss on the line is dominated by the dielectric loss  $\alpha_d$  everywhere, except for the frequencies below  $\sim 300$  MHz, where conductor loss may be dominating, then

$$\delta\alpha \approx \delta\alpha_D. \quad (2.21)$$

An approximate formula [45] relating  $\delta\alpha_D$  with the systematic error  $\delta DF$  is

$$DF = 2\alpha_D c / (\omega\sqrt{\epsilon'_r}), \quad (2.22)$$

where

$$\alpha_D \approx \alpha \approx |-S_{21}^{dB}| / (8.868 \cdot l). \quad (2.23)$$

The systematic error for the DF is obtained by variations with respect to  $\alpha_D$  and  $\epsilon'_r$  parameters,

$$\delta DF = \left( \frac{\partial DF}{\partial \alpha_D} \delta\alpha_D \right) + \left( \frac{\partial DF}{\partial \epsilon'_r} \delta\epsilon'_r \right). \quad (2.24)$$

Then from (2.20)-(2.22) one can get

$$\delta DF = \frac{c}{\omega\sqrt{\epsilon'_r}} \frac{|S_{11}|^2}{(1 - |S_{21}|^2)l} + \frac{c}{\omega\epsilon'_r\sqrt{\epsilon'_r}} \frac{|-S_{21}^{dB}|}{8.686 \cdot l} \delta\epsilon'_r. \quad (2.25)$$

## 2.5. SUMMARY

Formulas to quantify repeatability and systematic errors in DK and DF extraction using traveling-wave technique on PCB striplines have been derived and analyzed. The

necessity of removing the  $\sqrt{\omega}$  term associated with the conductor from the total phase constant  $\beta$  has been also demonstrated, and its effect on the repeatability errors of DK and DF has been shown. The results of measurements and computations in this work have been obtained using 30-GHz PCB test boards, but they are also important for future error analysis in extraction DK and DF using the new test vehicles specially designed for the DK and DF extraction up to 50 GHz.

### **3. CHARACTERIZATION OF COPPER FOIL SURFACE ROUGHNESS FROM MICROSECTION PHOTOGRAPHS**

Copper foil surface roughness affects accuracy of PCB dielectric characterization. There is an inhomogeneous interface between a laminate dielectric and copper foil, where copper particles and special treatment components penetrate into the dielectric. This penetration forms an inhomogeneous diffuse boundary layer with properties different from the parameters of the ambient dielectric, and this is not a conductor either. When using the travelling-wave technique S3 without taking into account this boundary layer, the extracted dielectric properties of laminate dielectrics may be corrupted, especially at higher frequencies. Hence, for accurate material parameter extraction, this boundary layer must be characterized, and its effects upon the extracted dielectric data must be de-embedded. To do this properly, it is important, to characterize geometrical parameters of roughness on any foil grown into a dielectric, as it takes place in an actual PCB stackup. It should be mentioned that initial “raw” untreated foil will not give useful information about roughness. The same is about a foil, which has been peeled off the dielectric, since peeling off may damage roughness profiles.

This section describes a new improved algorithm for semi-automatic characterization of copper foil profiles on microsection photographs of PCB striplines. This can be either optical or scanning electron microscopy (SEM) pictures. The collected statistics of numerous copper foil roughness profiles allows for introducing a new metric for roughness characterization of PCB interconnects. This is an important step to refining the measured DK and DF parameters from roughness contributions even at the very high frequencies up to 50 GHz and potentially higher.

### 3.1. PREVIOUS TOOL TO CHARACTERIZE SIGNAL TRACE GEOMETRY AND SURFACE ROUGHNESS

Surface roughness characterization means the definition of the special parameters and calculation their numerical values. Surface roughness profile can be treated as a statistical function of coordinates. The most commonly used surface roughness parameters in the PCB manufacturing industry are  $R_a$ ,  $R_q$  (or  $R_{rms}$ ),  $R_z$ , and  $R_t$ . There are some other parameters, which are used less commonly, e.g.,  $R_{mr}$ ,  $R_p$ ,  $R_s$ ,  $R_v$ , and  $R_{3z}$  to name a few. The definitions of these parameters can be found, e.g., in [46]. These parameters are typically extracted using various types of profilers (mechanical or laser), as is mentioned in [22] and presented in [47].

In this work, the two parameters, which can be extracted from microsection photographs, are used: an average peak-to-valley roughness amplitude  $A_r$  and roughness quasi-period  $\Lambda_r$ . As is mentioned in [22] and [48], the difference between  $R_z$  and  $A_r$  is that  $R_z$  is calculated based on the five highest peaks and the five lowest valleys on the total length of the roughness profile section, while  $A_r$  includes all peaks and all valleys, which exceed (for peaks) or below (for valleys) some threshold level along the entire profile.

$$A_r = \frac{\sum_{i=1}^m Y_{pi}}{m} + \frac{\sum_{j=1}^n Y_{vj}}{n}, \quad (3.1)$$

where  $Y_{pi}$  and  $Y_{vj}$  are the  $i$ -th peak and  $j$ -th valley respectively;  $m$  is the total number of peaks while  $n$  is the total number of valleys. In [47], the quasi-period  $\Lambda_r$  is defined simply as the average of quasiperiod for peaks and valleys on the sample length  $L$ ,

$$\Lambda_r = \frac{\Lambda^+ + \Lambda^-}{2}, \quad (3.2)$$

where  $\Lambda^+ = L/m$  and  $\Lambda^- = L/n$ .

Therefore, there is a direct analogy between random signals of time and random surface roughness function of a geometrical coordinate (or coordinates).

A methodology for semi-automatic copper foil surface roughness detection from PCB microsection images was described in [48]. The flowchart of this method is presented in Figure 3.1.

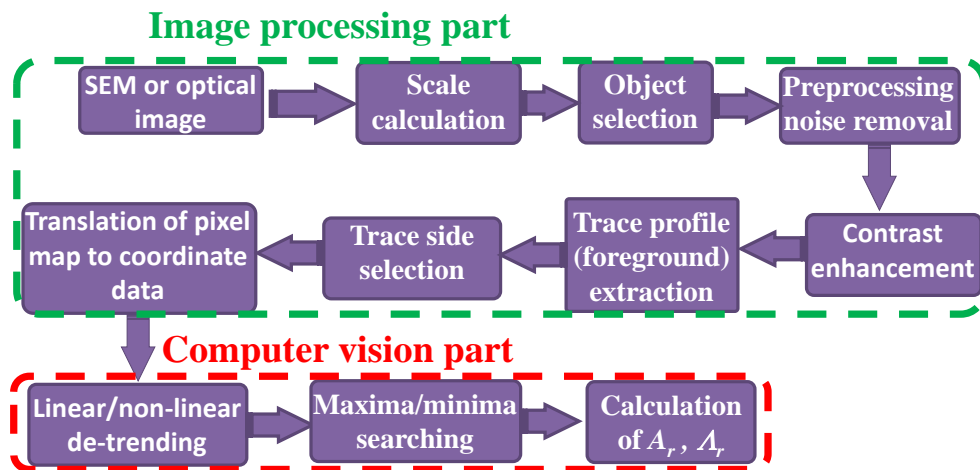


Figure 3.1 Flowchart for copper roughness extraction tool

A special Graphic User Interface (GUI) to implement this methodology was developed and used for getting roughness parameters and geometrical parameters of a signal trace. The input micro-photograph of SEM or optical images can be in the \*.tif or \*.jpg formats. For accurate calculations of feature dimensions, an embedded reference scale, as is shown in Figure 3.2, should be present on each image to be processed.

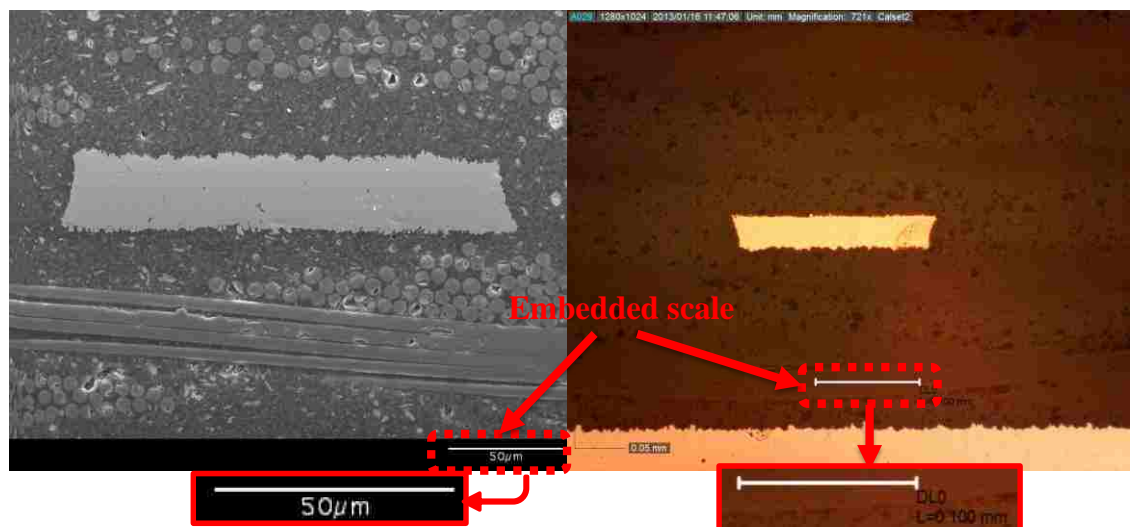


Figure 3.2 Input data for original GUI: SEM and optical microscope images

The GUI for PCB cross-sectional analysis operates with two tools: *Surface Roughness Profile Extraction Tool*, and *Trace Geometry Extraction Tool*.

The first one, *Surface Roughness Profile Extraction Tool*, is illustrated by Figure 3.3. The original image processing algorithm performs the following: pre-processing, noise removal, contrast enhancement, foreground extraction, surface roughness pixel map extraction, translation of pixel map to coordinate data, and calculation of the roughness

output parameters. The output data in this tool is the extracted surface roughness profile and automatically calculated parameters collected in the form a table. These parameters are the “standard”  $R_z$ ,  $R_a$ , and  $R_{rms}$  in addition to the abovementioned values of  $A_r$ ,  $\Lambda_r$ , and their ratio  $A_r / \Lambda_r$ .

The second one, *Trace Geometry Extraction Tool*, is illustrated by Figure 3.4. It automatically calculates the following parameters: the signal trace thickness (H); width of the oxide side (the narrower side of the trace,  $W_1$ ), width of the foil side (the wider side of the trace,  $W_2$ ), perimeter without roughness (“simple perimeter”), and perimeter with roughness (“true perimeter”), as well as the “user-defined perimeter”. The latter means that a user may introduce a correction of the signal trace borders.

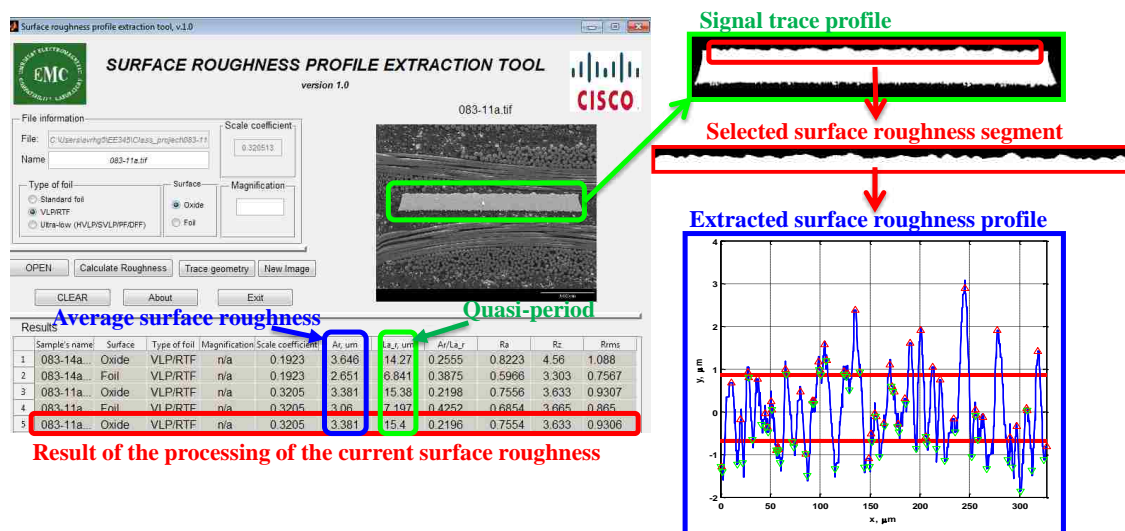


Figure 3.3 Copper roughness extraction tool and output data



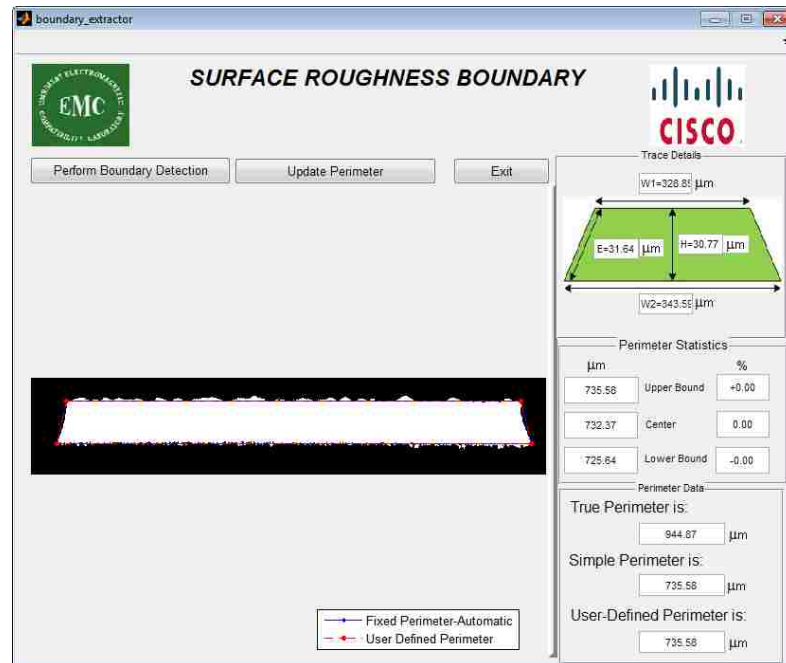


Figure 3.4 User interface of *Trace Geometry Extraction Tool*

The extracted using the abovementioned tools surface roughness profiles on signal traces and geometrical data on PCB stripline cross-sections were practically used to obtain the dielectric data on PCBs refined from smooth and rough conductor losses [22], [49], [50], [51], and [52].

However, to increase an accuracy of surface roughness profile extraction and characterization, the tools as described in [48], need further improvement of surface roughness detection algorithm. It is important to automatically get rid of various undesirable artifacts on photographs, *e.g.*, fuzzy images, weak contrast between copper foil and ambient dielectric or ceramic inclusions, “islands” of copper not connected to the trace itself, non-functional correspondence between  $x$  (coordinate along the tested sample length) and  $y$  (coordinate along roughness height), and other problems.

In addition, it is important to find a better metric to characterize surface roughness on a conductor rather than just  $A_r$ ,  $\Lambda_r$ , and their ratio  $A_r / \Lambda_r$ . In [22] and [52], only  $A_r$  on the foil side was used to build auxiliary curves in the DERM and DERM2 procedure. In [51],  $A_r$  values on both oxide and foil sides of the trace were used, and data of  $\Lambda_r$  was employed in finding effective roughness dielectric. In [49] and [50], an attempt was done to find a metric to characterize roughness on traces of different geometries and types of foils through the geometrical proportions for sets of test vehicles with the same dielectric. However, at that time the available data from pictures (SEM only) was insufficient to prove the validity of the proportions derived.

Currently, an optical microscope with high resolution (Inverted Metallurgical Microscope NIKON ECLIPSE MA100 and USB Digital Microscope Eye-Piece Camera DYNO-EYE) is available in the EMC Lab in addition to SEM facilities of Missouri S&T (Hitachi S-570). The maximum resolution for the optical microscope (Lens Nikon LU Plan Fluor 50x/0.80) is 23 pixels per micrometer, while for the SEM Hitachi S-570 the maximum resolution is 11 pixels per micrometer. This allows for making numerous test samples of boards under investigation and collecting statistical data on various roughness profiles. Obviously, this new collected data may significantly differ from the data obtained initially on a very limited number of samples.

Therefore two problems need to be solved: more accurate parameters extraction from microsection images, and identifying a new metric to better characterize surface roughness profiles. To solve these problems, a new surface roughness extraction and evaluation algorithm is needed.

### 3.2. GENERAL STRUCTURE AND PECULIARITIES OF THE NEW SURFACE ROUGHNESS EXTRACTION PROCEDURE

Surface roughness detection and quantification algorithm shown in Figure 3.1 consists of two parts: (1) image processing and (2) computer vision. Image processing part includes the general manipulations with a picture, *i.e.*, with pixel locations and their values. Computer vision part includes mathematical manipulations with the extracted profile vector and provides an output data – roughness parameters. A new proposed algorithm to characterize roughness of foils in PCBs also consists of these two parts.

The flowchart of the new surface roughness extraction procedure is shown in Figure 3.5.

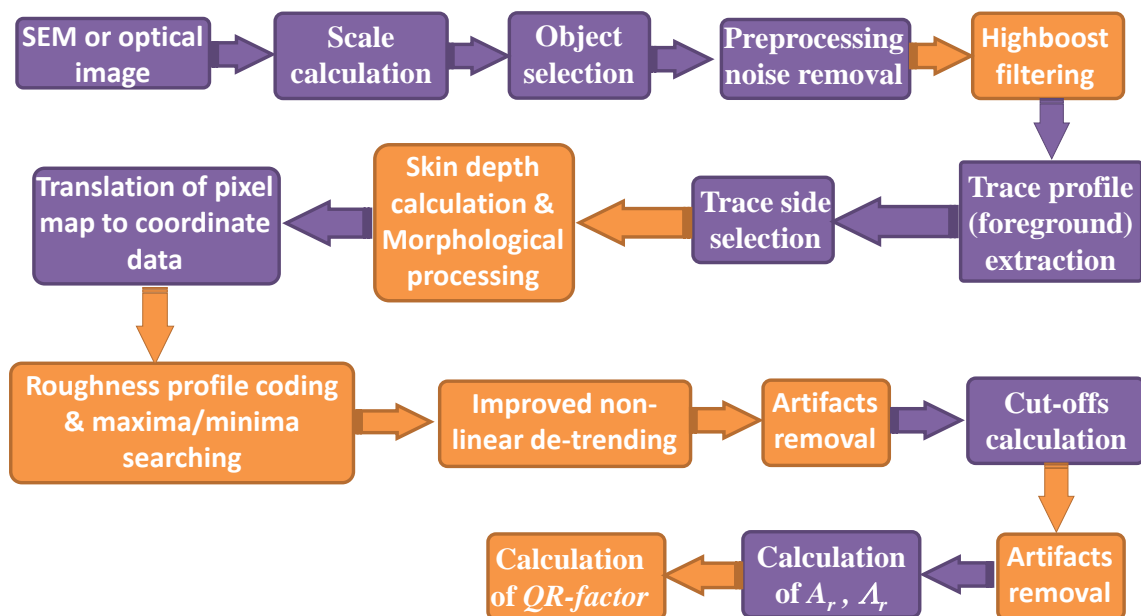


Figure 3.5 Flowchart of the new surface roughness extraction procedure

The purple blocks in Figure 3.5 are the blocks which are the same as in Figure 3.1, and the orange blocks correspond to the new functions specially designed and added in this present work. The distinctive functions in the new algorithm are

- High-boost filtering;
- Morphological filtering associated with taking into account skin depth;
- Roughness profile coding to locate extrema on roughness profiles;
- Modified non-linear de-trending to remove trace tilt and/or bend;
- Removal of artifacts, or a profile cleaning;
- Calculation of quantitative characteristics of surface roughness.

One can see that the procedure of artifacts removal is performed twice: at first, for the general cleaning of the profile extrema to provide the correct calculation of the cutoffs; and at the second time for detecting only significant peaks and valleys to provide correct calculation of the roughness parameters.

The new abovementioned functions will be further discussed in detail.

### **3.3. IMAGE PROCESSING PART IN THE NEW ALGORITHM**

Independently of whether an input image is gray or colored (RGB), in the new algorithm, the input data is converted to a grayscale image with double precision, and after that the image processing sequence is as shown in Figure 3.6.

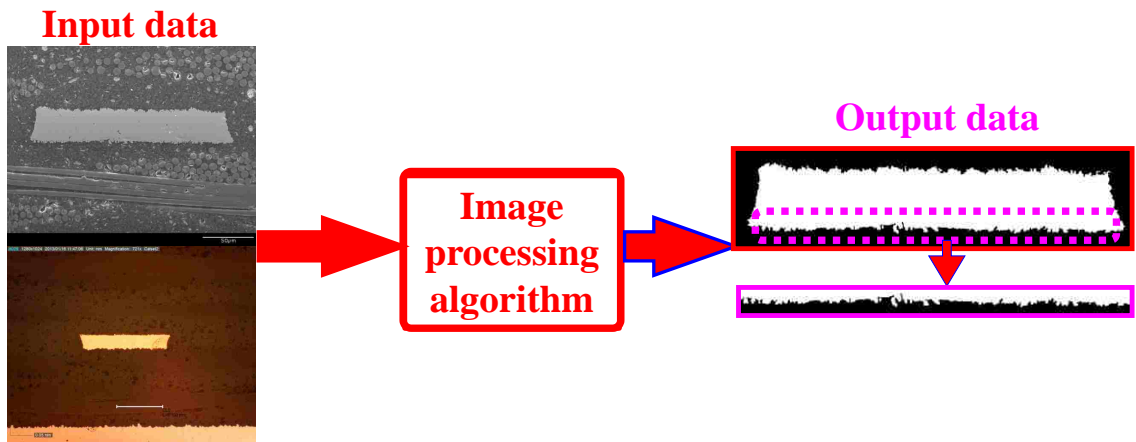


Figure 3.6 Flowchart of the image processing part

The image processing algorithm contains the following operations: scale coefficient calculation (using embedded scale), image rotation, logical operations of separation the background (dielectric and fibers), and foreground (signal trace), searching for the object boundaries. The output data in this part of the algorithm is the signal trace profile separated from the background details.

A segment of the output image which contains surface roughness on one of the sides of the trace, either foil or oxide side, is processed in the second, computer vision part.

*An objective of this work* is to improve the algorithm of the image processing part so that it would be robust with respect to image quality variations. Some artifacts in the input images, such as weak contrast and proximity of glass or ceramic inclusions to the copper foil profile, leading to errors, are illustrated in Figure 3.7. It is seen that the trace profile extraction, *i.e.*, an operation of separating the foreground from the background can be performed incorrectly due to various artifacts.

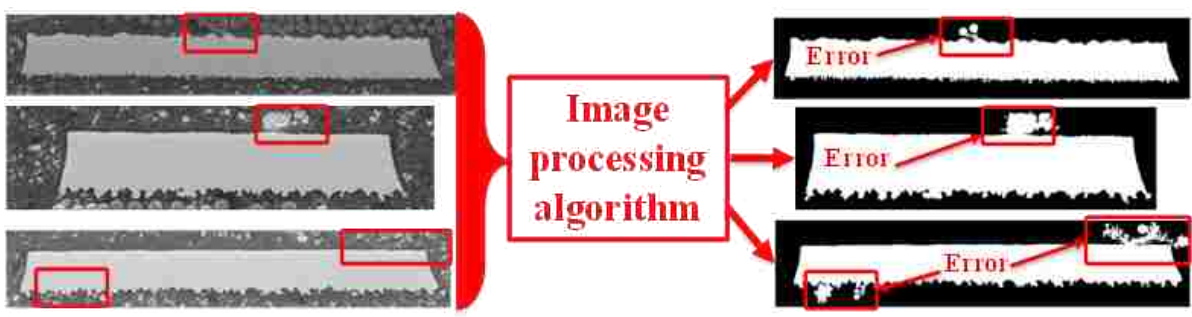


Figure 3.7 Artifacts in images and errors in image processing

The flowchart of manipulations according to the new image processing algorithm is shown in Figure 3.8. The peculiarity of the new image processing algorithm is using the so-called *high-boost filtering*. This procedure is detailed below.

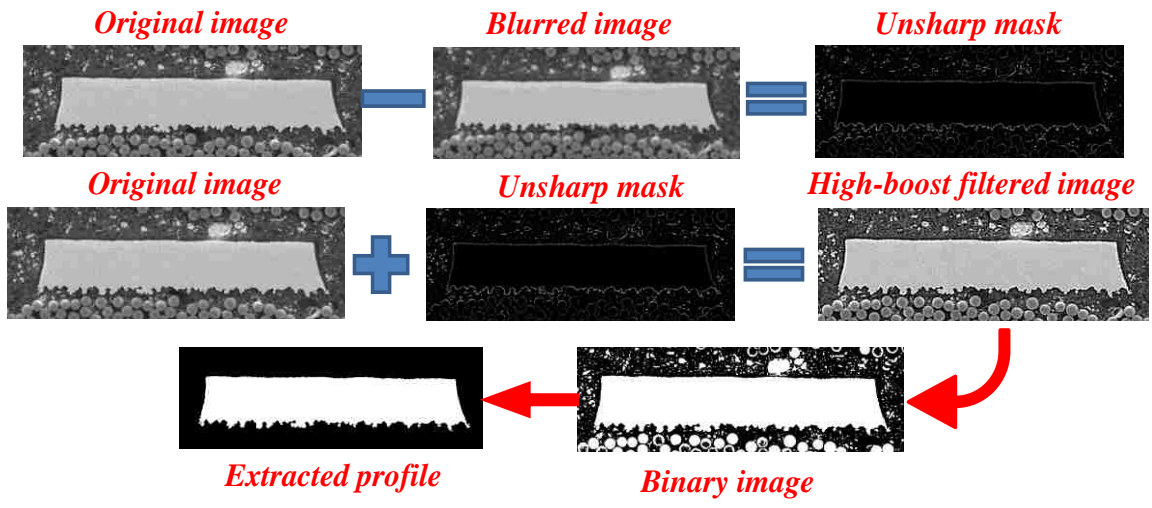


Figure 3.8 Image manipulations according to the new image processing algorithm

In the previous image processing algorithm, as described in [48], to extract a foil profile, two operations - contrast enhancement [53] and Otsu thresholding are done [54]. A grayscale image can be represented as a function  $g(x,y)$ , where  $x$ - and  $y$ -coordinates define the location of a pixel. The function value “ $g$ ” is the luminance of the pixel ranging from 0 (black) to 1 (white).

The image  $g(x,y)$  can be modeled as the product of the perfect image, denoted by  $f(x,y)$ , and the illumination function  $l(x,y)$ :

$$g(x, y) = f(x, y) * l(x, y). \quad (3.1)$$

The contrast enhancement operates with the illumination function to make  $g(x,y)$  closer to the perfect image, where any objects are easy distinguishable. Otsu thresholding automatically sets the level of brightness according to the gray-level histogram of the image. All the pixels with brightness higher than the threshold become white (value equals “1”). The pixels with brightness lower than the threshold become black (value equals “0”). Thus, the grayscale image converts to the binary image.

Distinct white objects on the binary image are compared to each other according to their area. An object with the largest area is automatically counted as the signal trace. All the other objects are removed from the picture.

The contrast enhancement operation in some cases may increase the illumination of the picture, whereas the highest brightness limit is 1. Then Otsu threshold level calculated from the enhanced picture may be not high enough. Therefore some pixels between fibers and profile become white on the binary image. Then fibers or any other white objects may connect to the profile by bridges of white pixels and thus may be

erroneously considered as a part of the extracted trace. The easiest intuitive solution of that trouble is usage of the *high-boost filtering* instead of the general contrast enhancement.

The high-boost filtering is the process of the image sharpening, and it can also be used if an image is darker than desired. The first step of the high-boost filtering is to calculate the *unsharp mask*  $g_{mask}(x,y)$  by subtracting the blurred image  $\bar{f}(x,y)$  from the original one  $f(x,y)$ ,

$$g_{mask}(x,y) = f(x,y) - \bar{f}(x,y). \quad (3.2)$$

To get the high-boost filtered image, the unsharp mask should be multiplied by the weighting coefficient  $k > 1$  and added to the original image:

$$g_{HB}(x,y) = f(x,y) + k \cdot g_{mask}(x,y). \quad (3.3)$$

The high-boost filtering highlights edges of objects in an image, and they become distinguishable. This operation obviously increases the level calculated by Otsu thresholding, but still keeps it low and far from the limits of the pixel brightness. Extra noise generated due to high-boost filtering can be easily removed by the median filtering [55].

### 3.4. COMPUTER VISION PART IN THE NEW ALGORITHM

Mathematical manipulations with an extracted profile are accomplished in the second, computer vision part of the entire algorithm. Computer vision part includes the following functions:

- removal of artifacts in the extracted profile;
- profile coding and extrema search;



- roughness quantification.

An input data for computer vision part is the black-and-white picture of the signal trace or its segment extracted as a result of the image processing part, as is shown in Figure 3.7. This segment of the signal trace profile, either on the oxide side or on the foil side, should contain surface roughness profile to be quantified. In any input picture, copper is white, and dielectric is black.

The first step of the computer vision algorithm is the conversion of the profile segment to the vector of numbers. The conversion is a simple columnwise summation of the corresponding pixel values. White color (copper) corresponds to the pixel value of “1”, while black color corresponds to the pixel value of “0”. Therefore, the simple columnwise summation yields the vertical size of the copper profile in each column of pixels, as is illustrated by Figure 3.9.

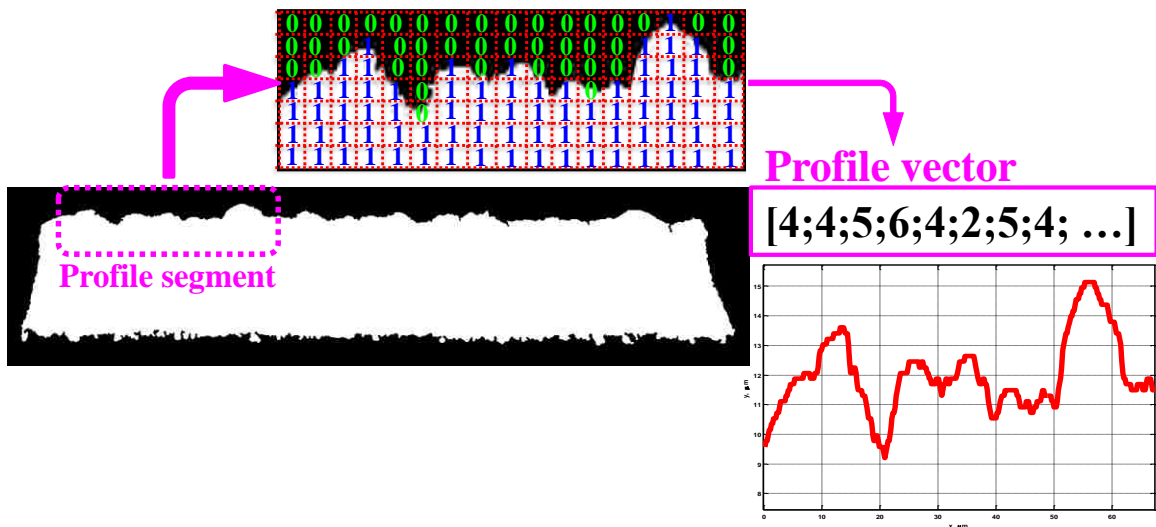


Figure 3.9 Image to vector conversion

As is mentioned above, a surface roughness profile may contain various artifacts, which may also be converted to the profile vector. Figure 3.10 illustrates three types of artifacts: false maxima, forks, and steps.

A “false maximum” artifact is just a notch on the side of the peak, which can be erroneously taken for a peak. A “fork” artifact is comprised of two closely located maxima separated by such a narrow valley, that they cannot be considered as two separate peaks.

An artifact “step” can be erroneously taken for a maximum in two different cases. The first case is when the step is located prior to the neighboring peak, and the de-trending operation yields the negative slope on the step. The second case is when the step is behind the neighboring peak, and the de-trending operation yields the positive slope on the step.

These three abovementioned artifacts are associated with peaks; however, the similar situation will be with valleys.

If the image processing algorithm is built as in Figure 3.1, *i.e.*, extrema are searched *after* the de-trending operation, the “steps” may be taken for maxima (or minima). This is illustrated by Figure 3.10.

If these image artifacts are not treated in a special way, the extracted quantitative characteristics of surface roughness profile, *e.g.*, peak-to-valley roughness amplitude  $A_r$  and quasi-period  $\Lambda_r$ , may be corrupted.

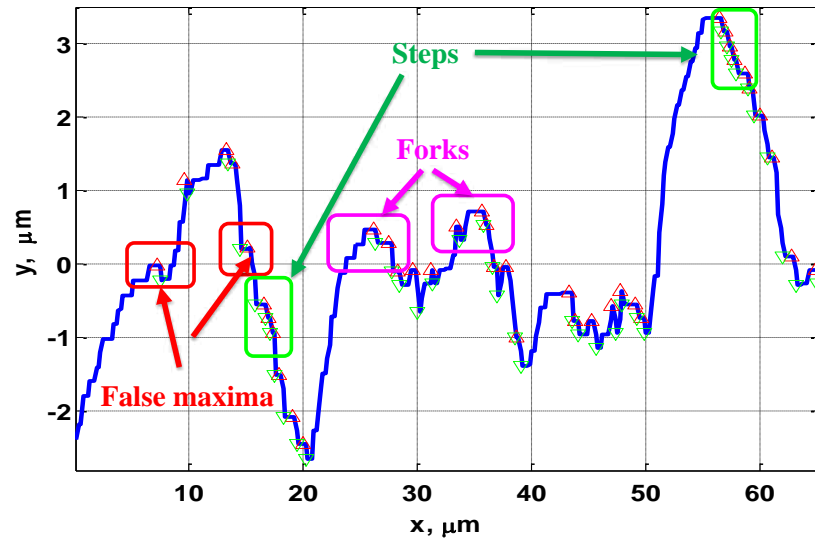


Figure 3.10 Image artifacts

The parameters  $A_r$  and  $\Lambda_r$  are calculated from the found coordinates of maxima and minima. Only comparatively distant (and distinct) peaks (or valleys) should be taken into account for roughness quantification. The previous version of computer vision algorithm as in [48] did not allow for a profile “cleaning” from artifacts, and it was not obvious whether the presence of artifacts corrupts the calculated results and how much. That is why in the present work the computer vision part has been totally rebuilt, and a new algorithm was constructed from scratch.

**3.4.1. Profile Coding and Extrema Search.** A new procedure for searching locations of maxima and minima was created. Maxima and minima locations are determined by indices of pixels on the image, where abovementioned features are located.

The first step is the calculation of the first derivative of the profile vector, from which one can easily find the positions of the profile rises (derivative  $>0$ ), profile falls (derivative  $<0$ ), and flat segments on the profile (derivative  $=0$ ). The numbers “1”, “4”, “2” can be assigned to the rise, fall, and flat segments of the profile, correspondingly, as is shown in Figure 3.11.

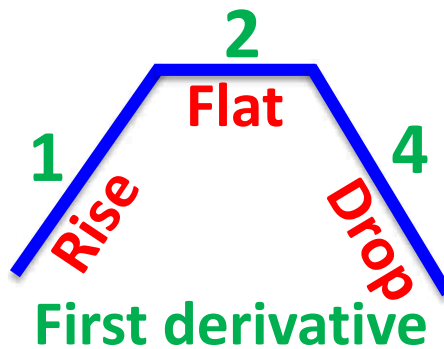


Figure 3.11 Profiles first derivative coding

The calculation of the derivative of the coded first-derivative profile vector results in the coded second-derivative profile vector. The choice of the numbers “1”, “2” and “4” is not arbitrary. The point is that the successive subtraction of any possible sequence of

these numbers always gives the numbers 0, or  $\pm 1$ , or  $\pm 2$ , or  $\pm 3$ . This is illustrated by Figure 3.12. The numbers  $\{0, \pm 1, \pm 2, \text{ and } \pm 3\}$  are then used to distinguish changes in the slope of the profile and to code this profile.

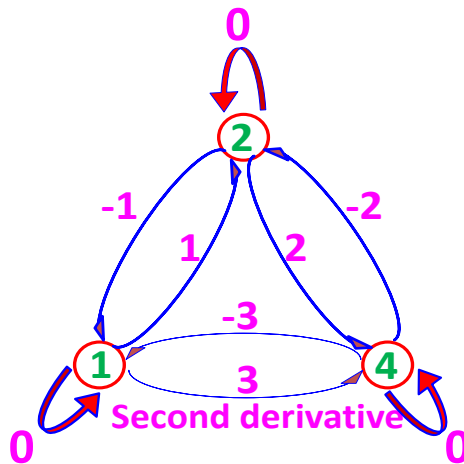


Figure 3.12 Profiles second derivative coding

These numbers correspond to the following scenarios:

- “0” means no changes;
- “+1” means profile rise changes to flat segment;
- “-1” means flat profile segment changes to the rise of the profile;
- “+2” means flat segment of the profile changes to fall;
- “-2” means fall changes to flat segment of the profile;
- “+3” means rise change to fall;

- “-3” means fall changes to rise.

The numbers “-3” and “+3” directly indicate the locations of sharp (of 1-pixel width) minima and maxima, respectively. In addition to sharp maxima and minima, a profile may contain flat regions on the top of peaks and bottoms of valleys. However, independently of the width of the flat region, any partial sum of the elements in the coded second-derivative vector between slope changes equals to “+3” for maxima and “-3” for minima. This is shown in Figure 3.13.

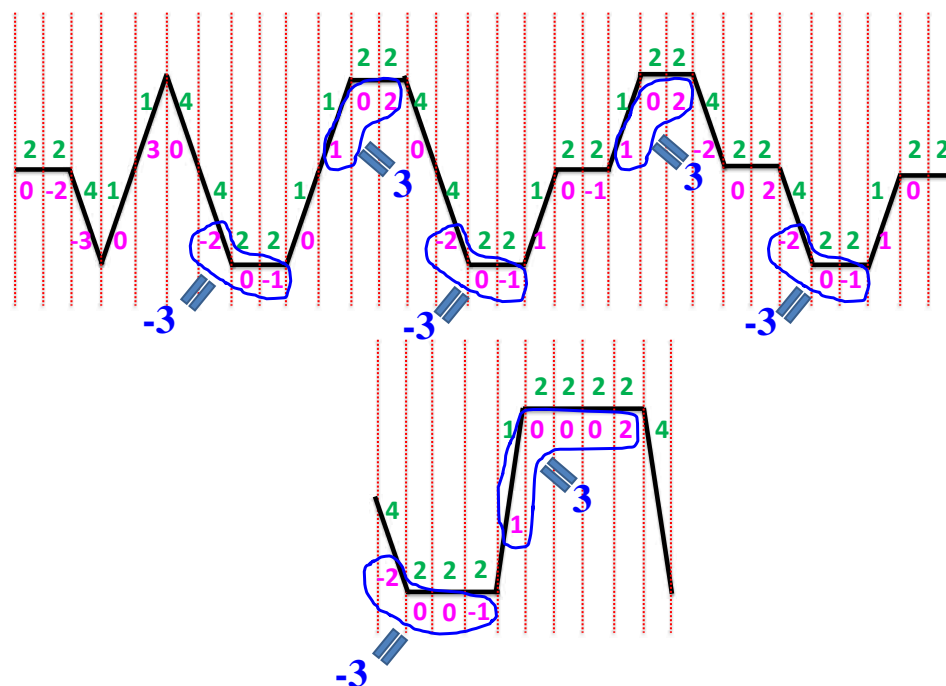


Figure 3.13 Profile coding example

Segments of the profile vector which contain  $[-2, 0 \dots (0), -1]$  and  $(2, 0 \dots (0), 1)$  can be recognized in the profile. Peak and valley locations are assigned to the center of the

corresponding segments, as is shown in Figure 3.14. When all extrema are found, it is important to decide which of these extrema should be taken into account for roughness parameters calculation. Some of the peaks and valleys are small and insignificant. To remove insignificant peaks and valleys from computations, all found maxima and minima should be compared by their amplitudes with some threshold levels.

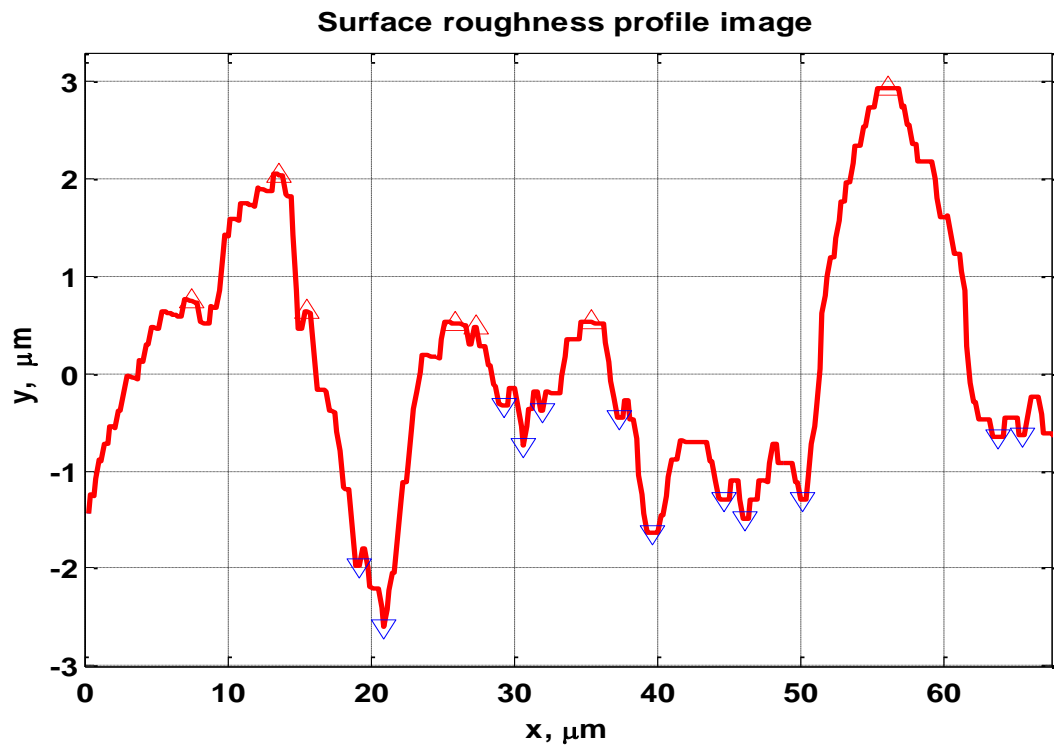


Figure 3.14 Extrema search example

**3.4.2. De-trending and Cutoffs.** Amplitudes of peaks and valleys in the new algorithm are calculated after a profile is centered about its mean level. A picture of surface roughness profile to be analyzed in many cases is tilted at some angle, and in this case this tilt should be eliminated for roughness quantification. Moreover, a signal trace may be bent to some extent, and then the curvature, which is not related to surface roughness, should be compensated. The operation, that performs all these corrections, is called de-trending.

The Matlab 2012 function *detrend(x)* was used in the previous version of the profile processing procedure [56] for linear de-trending in the case of the linear trend of the profile. However, this standard de-trending function *detrend(x)* does not remove a curvature of the trace. For this reason, a non-linear de-trending function based on Legendre polynomials was developed and implemented in the previous version of the algorithm [48]. In the limit of no curvature (just linear tilt), the non-linear de-trending function should converge to the linear de-trending case, which should give the same results as with the standard *detrend(x)* function. However, this was not the case in [48]. Therefore in the GUI based on the methodology [48] two separate algorithms, “linear de-trending” and “non-linear de-trending”, were used. Before doing de-trending, a user had to identify the curvature of the trace and manually switch de-trending procedure from linear to non-linear case. This is obviously is inconvenient. Moreover, application of the high-order Legendre polynomials may remove instead of the profile curvature its actual roughness profile, and the extracted results would be then corrupted.

In this work, an improved de-trending procedure is proposed and implemented. This new algorithm can automatically remove quadratic and cubic trends in the non-



linear case, and for the pure tilted case, the results are close to those obtained using the standard Matlab's linear de-trending function.

Similar to [48], the improved non-linear de-trending consists of fitting the profile under test by Legendre polynomials of some pre-defined order, and then the fitted curve is subtracted from the original profile. The main challenge is how to choose the proper order of polynomials to remove quadratic or cubic profile curvature while not corrupting wide peaks and valleys which may be present on the profile.

The solution is to perform the profile smoothing before the profile is fitted. This can be done by applying Matlab's *moving average* operation [57]. This filtering minimizes an impact of the fitted profile curvature on wide peaks and valleys. Example of improved non-linear de-trending is shown in Figure 3.15.

An example of the roughness profile processed with a new the improved non-linear de-trending is shown in Figure 3.16.

The non-linear de-trending operation makes the profile centered with respect to the zero level. Therefore the amplitude of the peaks and valleys can be calculated as absolute values of the  $y$ -coordinates of the corresponding maxima or minima.

Not all minima and maxima detected on the roughness profile should be taken into account. Obviously, there should be some *threshold levels* of peak and valley amplitudes below which maxima and minima are not taken into account. A level of the roughness magnitude, which is calculated as an *average of all the minima* that are located under the zero level (have negative  $y$ -coordinates), is called a *valley cutoff*. A level of roughness magnitude, which is calculated as an *average of all the maxima* that are locate above the zero level (have positive  $y$ -coordinates), is called a *peak cutoff*. Only

valleys that lie below the negative valley cutoff level are taken into account as significant. The other valleys are neglected. Similarly, only the peaks that are higher than the positive peak cutoff are considered as significant. All the rest peaks are neglected. Only *significant peaks* and *valleys* are used for calculating roughness parameters.

However, a roughness profile still may contain such artifacts as *forks*, which may corrupt calculation of roughness parameters, especially a roughness quasi-period. Such forks are indicated in Figure 3.16. How to remove undesirable forks is discussed in the next sub-section.

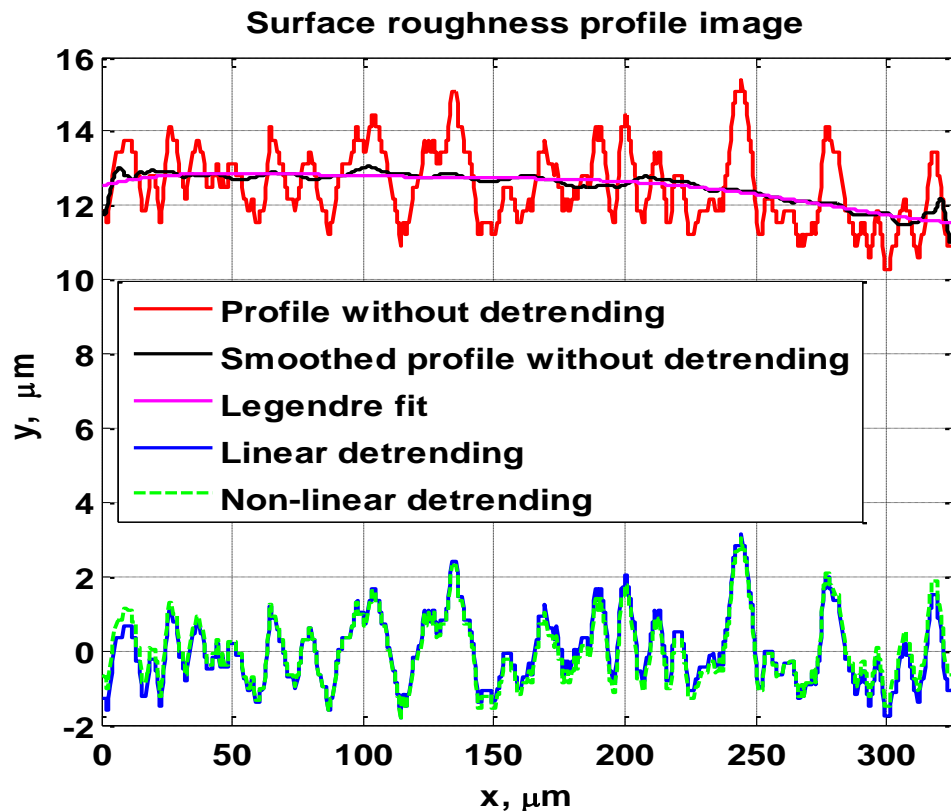


Figure 3.15 An example of a profile processing using the improved non-linear detrending

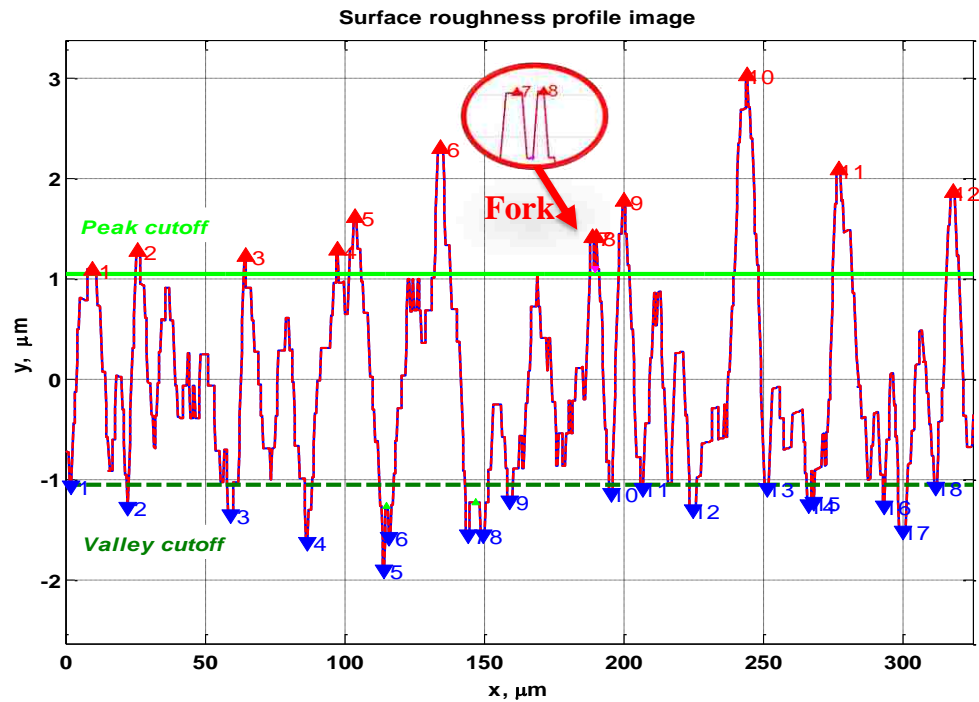


Figure 3.16 Surface roughness profile, peak and valley cutoffs, and selecting significant peaks and valleys

**3.4.3. Removal of False Maxima and Minima.** The most sensitive roughness parameter to the presence of such artifacts as forks and false maxima and minima is the quasi-period of a roughness function.

A special automatic procedure has been designed in this work to remove forks and false maxima/minima. The first-order approximation of the quasi-period can be calculated from the profile with detected peaks and valleys as those in Figure 3.16. This first-order quasi-period approximation can be used as the criterion for artifacts removal. The distance between neighboring peaks or valleys can be compared with one fifth of the approximate quasi-period. If neighboring peaks or valleys are located closer than this

distance, this would mean that they violate quasi-periodicity, and some of these peaks or valleys are false.

The indices of the neighboring peaks or valleys, which are closer to each other than one fifth of the approximate quasi-period, are saved in a special vector. If there are several indices in a row, this means that there is a region of the closely located peaks or valleys. Amplitudes of such kind of the peaks or valleys are compared separately within each region. Only the maximum peak or valley is taken in to account in each region, while all the others should be removed.

An artifact of the type “a fork of the peaks” usually has a minimum between the neighboring closely located peaks with the  $y$ -coordinate higher than the peak cutoff. The similar situation is typical for artifacts “fork of the valleys”: there is a maximum between the neighboring closely located valleys with the  $y$ -coordinate lower than the valley cutoff. Indices of such maxima or minima are added to the vector of valleys and to the vector of peaks, respectively. These split maxima and minima can help to identify the regions with violations of the quasi-periodicity and the presence of the artifacts. The procedure of removal of such artifacts as split extrema is illustrated by Figure 3.17.

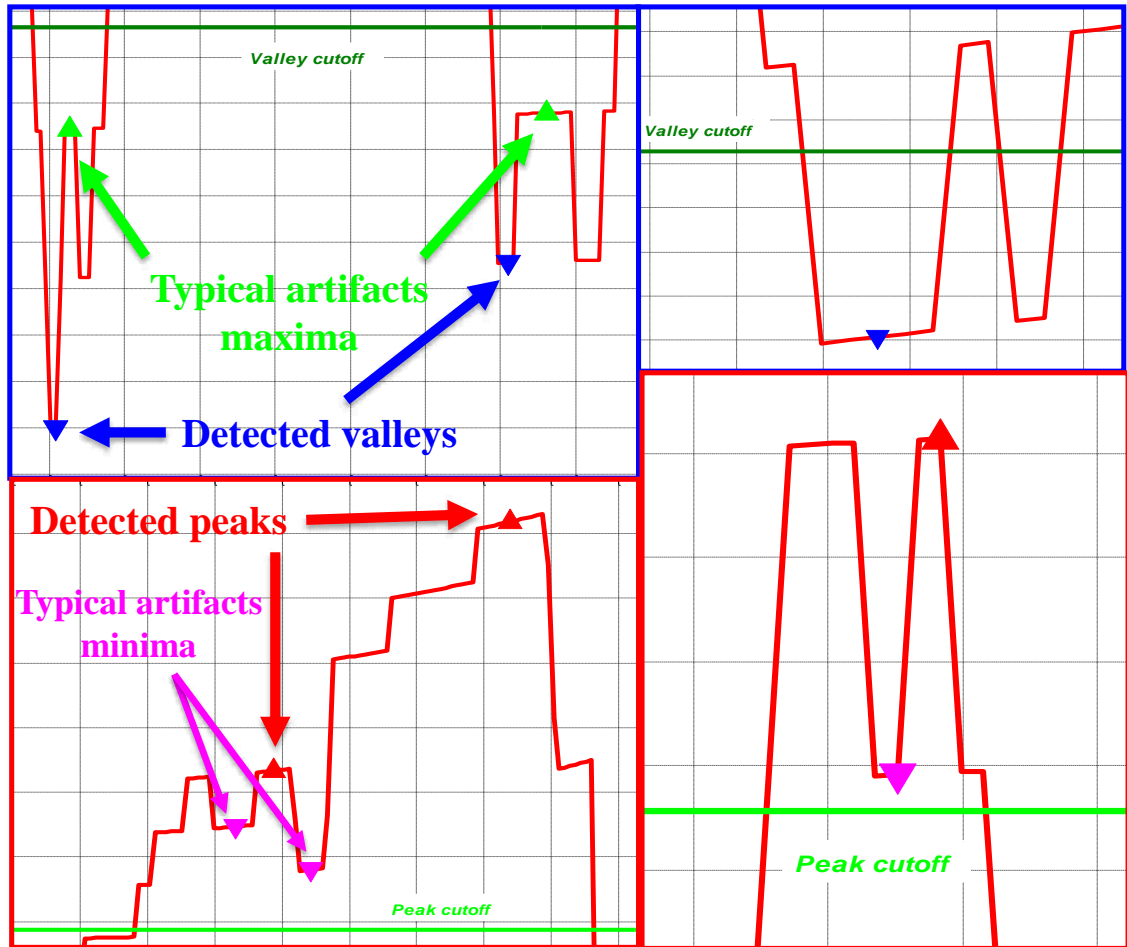


Figure 3.17 Examples of the artifacts removal

### 3.5. ROUGHNESS QUANTIFICATION

An accurate PCB dielectric characterization in S3 technique requires de-embedding conductor surface roughness effects on the measured insertion losses and phase. One of the ways to characterize surface roughness from the geometrical point of view is to use peak-to-valley amplitude  $A_r$  and roughness quasi-period  $\Lambda_r$ . Then it is

important to find a metric, which will be associated with effects of roughness upon loss and possible on phase constant (or delay time).

Herein, a roughness factor (or roughness parameter)  $QR$  is defined as a ratio of the peak-to-valley amplitude to the quasi-period on a profile under study,

$$QR = \frac{A_r}{\Lambda_r}. \quad (3.4)$$

Indeed, the higher the peak-to-valley amplitude, the greater the loss on the line. Therefore the roughness amplitude  $A_r$  stands in the numerator of (3.4). The greater the quasi-period, the slower the variation of the surface roughness along the coordinates, and the lower the loss on the line is. The higher quasi-period means that less copper peaks are there on the surface of the trace. Therefore the roughness quasi-period stands in the denominator of (3.4).

Surface roughness on both sides of the signal trace should be taken into account. For this reason, it is proposed that the roughness factor on the trace  $QR$  consists of two terms, corresponding to partial roughness factors on the oxide and on the foil sides of the trace,

$$QR = QR_{oxide} + QR_{foil}. \quad (3.5)$$

$QR$  quantifies the copper growth into a dielectric on the both sides of the trace. Volume fraction of the copper inclusions in the surface roughness layer should be proportional to the  $QR$ -factor. The contribution of the surface roughness to the insertion losses is proportional to the roughness amplitude, or, equivalently, to the “thickness” of the roughness layer determined by  $A_r$ .

According to the QR-factor formulation absolutely smooth foil with no roughness should have  $QR=0$ . A foil with the rougher profile will have the higher QR than a smoother foil one.

An example of insertion loss curves for three test vehicles with identical geometry and identical dielectric, but different surface roughness is presented in Figure 3.18. SEM pictures of traces made of HVLP, RTF, and STD foils are also shown in this figure.

According to the measured insertion losses shown on Figure 3.18,  $QR_{STD}$  should be bigger than  $QR_{RTF}$  and  $QR_{HVLP}$ ;  $QR_{RTF}$  should be bigger than  $QR_{HVLP}$ , but less than  $QR_{STD}$ ; and  $QR_{HVLP}$  should be less than  $QR_{RTF}$  and  $QR_{STD}$ .

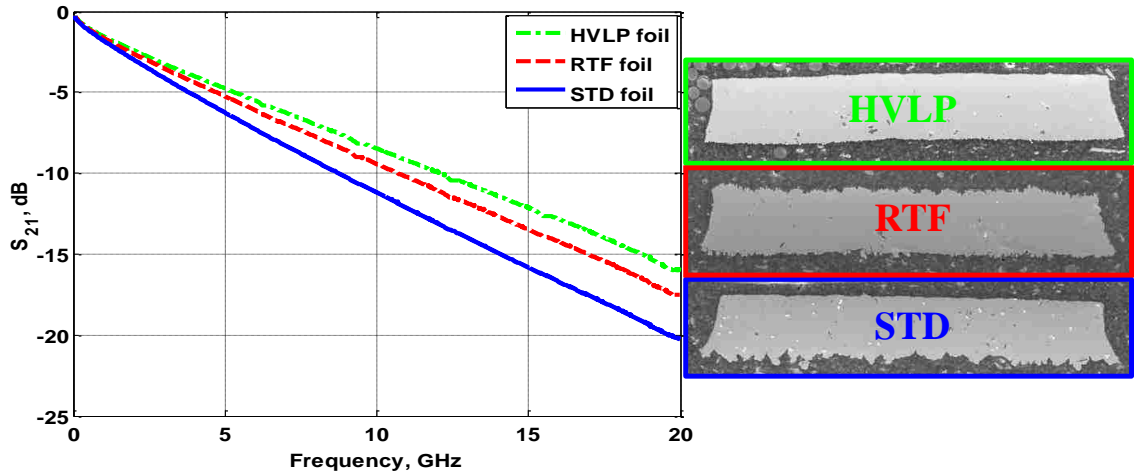


Figure 3.18 Surface roughness impact to insertion losses

The QR factors extracted from the cross-sectional SEM images using the new surface roughness extraction algorithm and GUI are the following:

$$QR_{STD} = \frac{A_r^{oxide}}{\Lambda_r^{oxide}} + \frac{A_r^{foil}}{\Lambda_r^{foil}} = 0.084 + 0.423 = 0.507 ;$$

$$QR_{RTF} = \frac{A_r^{oxide}}{\Lambda_r^{oxide}} + \frac{A_r^{foil}}{\Lambda_r^{foil}} = 0.309 + 0.270 = 0.579 ;$$

$$QR_{HVLP} = \frac{A_r^{oxide}}{\Lambda_r^{oxide}} + \frac{A_r^{foil}}{\Lambda_r^{foil}} = 0.061 + 0.109 = 0.170 .$$

It is seen from these calculations that there is a mismatch between calculated from SEM images QR-factors and the insertion losses. This means that the simple definition of the QR-factor in terms of the geometrical roughness parameters as (3.4) and (3.5) is *insufficient* for proper surface roughness characterization.

To overcome this problem, it is proposed in this work to compare conductor roughness feature sizes on a profile with skin depth, *i.e.*, take into account the high-frequency electromagnetic field penetration into a rough surface. Such penetration would cause additional loss due along the roughness contour due to the classical skin effect. If a characteristic size of a foil roughness feature, *e.g.*, the width of a sharp spike or a narrow valley, is too small compared to the skin depth at some frequency, the electromagnetic field will be not able to penetrate along the contour of this spike (or the valley). Quite the contrary, the electromagnetic field would be scattered, and this may lead to a partial compensation of loss in the foil.

In the next sub-section, it will be shown that a special image processing procedure called *morphological processing* may make the foil profile reasonably smoother so that it would correspond to the actual penetration of electromagnetic field into roughness due to skin-effect, and would be equivalent to the reduced loss in the case of electromagnetic field scattering on roughness inhomogeneities.



### 3.6. MORPHOLOGICAL PROCESSING OF THE ROUGHNESS PROFILE

Classical skin-effect and scattering of electromagnetic field on roughness profile features can be taken into account by using *morphological processing*. One of the morphological operations is called *erosion*. The erosion of set A (image) by set B (structuring element) has the notation  $A \bar{\oplus} B$ , and is defined as [58] and [59].

$$A \bar{\oplus} B = \{z | (B)_z \cap A^c = \emptyset\}. \quad (3.6)$$

This means that the erosion of A by B is the set of all the processed image points z such that B translated by z is contained in A. Erosion is illustrated by Figure 3.19.

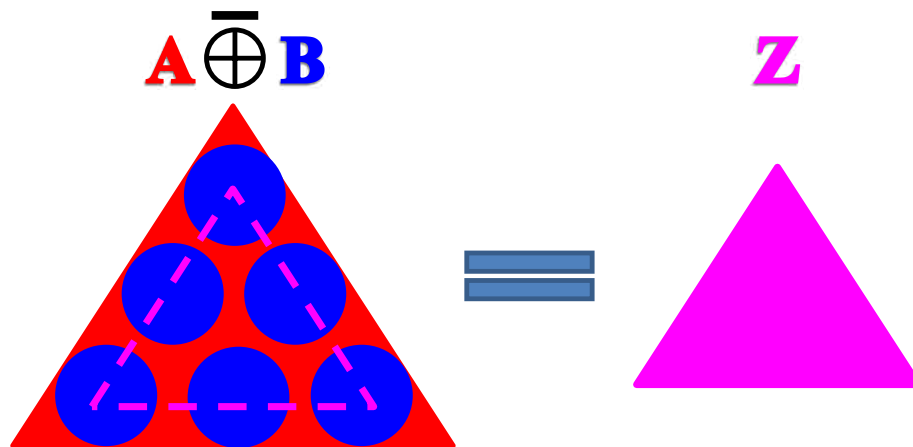


Figure 3.19 Morphological operation

In this work of optical or SEM image processing of foil roughness profiles, the set “A” is the black-and-white picture of the signal trace, which contains surface roughness profile to be quantified. The structure element “B” is the disk with a radius equal to the

skin-depth at the given frequency. The disk shape of the structure element has been chosen for simplicity, because this shape is isotropic with respect to any direction.

The peaks of the roughness profile, which are lower and/or narrower than the size of the structure element, fall out of the profile, as is shown in Figure 3.20, and excluded from the further operations with the profile.

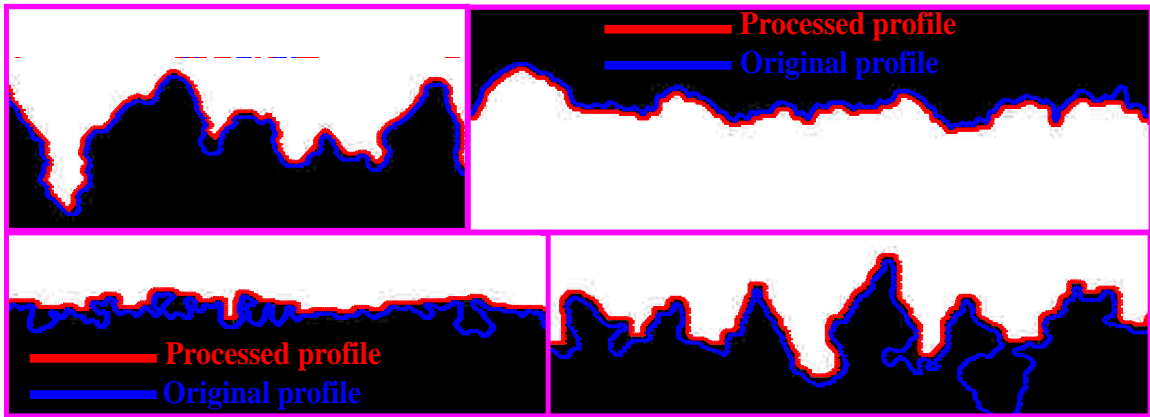


Figure 3.20 Examples of the morphological processing of the roughness profile image

The  $QR$  factors extracted from the roughness profiles processed with morphological operation are the following:

$$QR_{STD} = \frac{A_r^{oxide}}{\Lambda_r^{oxide}} + \frac{A_r^{foil}}{\Lambda_r^{foil}} = 0.084 + 0.423 = 0.49 ;$$

$$QR_{RTF} = \frac{A_r^{oxide}}{\Lambda_r^{oxide}} + \frac{A_r^{foil}}{\Lambda_r^{foil}} = 0.309 + 0.270 = 0.36 ;$$

$$QR_{HVLP} = \frac{A_r^{oxide}}{\Lambda_r^{oxide}} + \frac{A_r^{foil}}{\Lambda_r^{foil}} = 0.061 + 0.109 = 0.14 .$$

These calculations show the correct correspondence between the calculated from SEM images QR-factors and the insertion losses: the higher the QR, the greater insertion loss is.

The morphological processing of the profile image means some kind of “tuning” of the SEM or optical microscope images to the frequency of the electromagnetic field interacting with the foil roughness during S-parameter measurements on a test vehicle.

### **3.7. AUTOMATIC COLLECTION OF STATISTICS AND DATABASES**

The new designed surface roughness extraction procedure as in Figure 3.6 was built in the existing GUI. The new function for saving results of copper foil roughness characterization has been added to the existing GUI. The tables with results of the processing are automatically saved to the comma delimited \*.csv files. In addition to the existing GUI, a special subprogram for statistical analysis of the results has been created. The saved databases of the results in the form of tables can be uploaded to this subprogram. The subprogram calculates the mean value of the roughness or geometry parameters, as well as deviations from sample to sample in absolute values and percentages. Collecting the statistics for numerous copper foil roughness profile images was done by using the new algorithm and the GUI with the added function of saving databases.

In Table 3.1, the parameters are the following:  $w_1$  and  $w_2$  are the corresponding widths of the oxide and foil sides of a signal trace;  $H$  is the thickness of the trace;  $h_1$  and  $h_2$  are the distances between the oxide side or foil side of the trace to the corresponding ground plane;  $A_{r1}$  and  $A_{r2}$  are the peak-to-valley roughness amplitudes on the oxide and

foil sides, respectively;  $\Lambda_{r1}$  and  $\Lambda_{r2}$  are the quasi-periods of roughness function on the oxide and foil sides, respectively;  $QR_1$  and  $QR_2$  are the partial corresponding roughness parameters on each side of the trace.

**Table 3.1 Statistical Data for Various Types of Test Vehicles and Foils**

Foil/ trace	$w1,$ $\mu m$	$w2,$ $\mu m$	$H,$ $\mu m$	$P(user),$ $\mu m$	$h_1,$ $\mu m$	$h_2,$ $\mu m$	$A_{r1},$ $\mu m$	$A_{r2}, \mu m$	$\Lambda_{r1},$ $\mu m$	$\Lambda_{r2},$ $\mu m$	$QR_1$	$QR_2$
STD Wide	322.6 $\pm 9.7$ 3.0%	331.3 $\pm 21.4$ 6.5%	32.0 $\pm 1.3$ 4.0%	720.2 $\pm 23.97$ 3.3%	346.5 $\pm 6.7$ 2.0%	284.0 $\pm 7.5$ 2.7%	1.04 $\pm 0.42$ 40.0%	5.29 $\pm 0.83$ 15.8%	19.5 $\pm 5.4$ 27.8%	20.0 $\pm 3.5$ 17.7%	0.0584 $\pm 0.044$ 9 76.9%	0.2674 $\pm 0.0508$ 19.02%
STD Medium	182.0 $\pm 5.5$ 3.0%	186.7 $\pm 15.8$ 8.5%	31.78 $\pm 1.02$ 3.2%	433.5 $\pm 18.85$ 4.35%	218.6 $\pm 5.8$ 2.7%	201.3 $\pm 7.2$ 3.6%	1.01 $\pm 0.32$ 31.6%	5.28 $\pm 0.73$ 13.9%	18.14 $\pm 7.8$ 43%	19.3 $\pm 5.2$ 26.7%	0.061 $\pm 0.051$ 6 84.6	0.2802 $\pm 0.0835$ 29.8%
RTF Wide	321.4 $\pm 24.3$ 7.6%	332.9 $\pm 25.5$ 7.7%	31.3 $\pm 0.83$ 2.64 %	718.6 $\pm 50.7$ 7.01%	346.5 $\pm 7.4$ 2.1%	288.1 $\pm 5.9$ 2%	3.46 $\pm 0.5$ 14.5%	2.17 $\pm 0.33$ 15.4%	25.6 $\pm 1.96$ 7.7%	12.0 $\pm 1.7$ 14.3 %	0.1356 $\pm 0.019$ 1 14.12 %	0.1823 $\pm 0.0201$ 11.02%
RTF Medium	181.4 $\pm 4.7$ 2.6%	185.9 5 $\pm 14.7$ 7.9%	31.7 $\pm 1.03$ 3.23 %	431.93 $\pm 18.07$ 4.18%	236.9 $\pm 11.2$ 4.7%	199.0 $\pm 4.2$ 2.1%	2.75 $\pm 0.77$ 28.0%	1.97 $\pm 0.35$ 17.8%	21.2 $\pm 6.65$ 31.4%	16.3 $\pm 5.3$ 32.6 %	0.1319 $\pm 0.033$ 4 25.4%	0.1288 $\pm 0.0738$ 57.3%
STD Narrow	73.2 $\pm 3.7$ 5%	86.9 $\pm 5.7$ 6.5%	32.01 $\pm 2.34$ 7.3%	225.65 $\pm 13.1$ 5.8%	101.1 $\pm 7.0$ 6.9%	99.8 $\pm 2.3$ 2.3%	1.04 $\pm 0.33$ 31.4%	4.36 $\pm 2.4$ 55.0%	15.1 $\pm 7.66$ 50.6%	17.6 $\pm 7.7$ 43.5 %	0.0721 $\pm 0.023$ 8 33.01 %	0.2477 $\pm 0.0711$ 28.7%
RTF Narrow	74.25 $\pm 4.65$ 6.3%	87.18 $\pm 4.96$ 5.7%	32.03 $\pm 1.63$ 5.1%	226.87 $\pm 11.36$ 5.0%	94.3 $\pm 3.5$ 3.7%	100.1 $\pm 1.0$ 1%	2.52 $\pm 1.43$ 56.9%	1.75 $\pm 0.71$ 40.5%	19.2 $\pm 8.03$ 41.8%	16.08 $\pm 5.95$ 37.0 %	0.13 $\pm 0.030$ 5 23.47 %	0.1105 $\pm 0.0428$ 38.69%

The statistical data in Table 3.1 was collected from image processing of the ten different cross-sectional SEM and/or optical microscopy pictures taken from different slugs cut out along the signal trace in a number of different test vehicles. In particular, six different test vehicles with different geometry and foil profile were tested.

As is seen from Table 3.1, there is a significant deviation of geometrical roughness parameters from the mean values for all the tested slugs. This is a manifestation of the statistical nature of roughness.

A foil roughness is the same in any direction on the plane of the trace – along the width of the trace and along the signal trace length in the direction of electromagnetic wave propagation. Thus the roughness data extracted from the cross-sectional picture of the PCB stripline trace would be the same as along the trace. This is illustrated by Figure 3.21.

Collection of such statistics is important for developing surface roughness models, for correctly refining dielectric properties of laminate PCB dielectrics from foil roughness, and for the development of “design curves”. The latter will be discussed in Section 4. The collected statistical data is also important for an overall evaluation of quality of PCB materials fabrication.

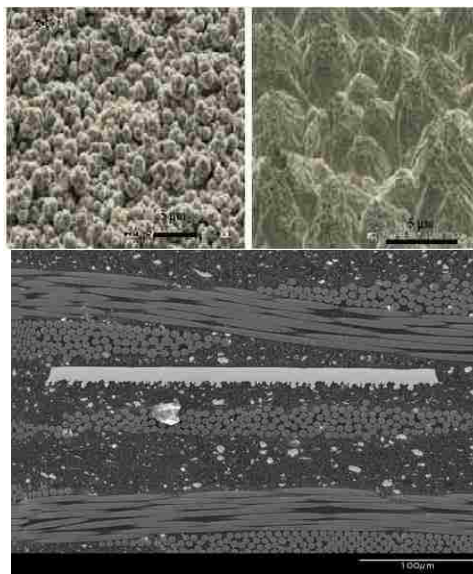


Figure 3.21 Roughness profile is the same along the trace width and along the trace length

### 3.8. FURTHER IMPROVEMENT OF ROUGHNESS CHARACTERIZATION

Over two hundred cross-sectional SEM or optical pictures have been processed using the new proposed algorithm. Based on the gained experience, some additional improvements of the new approach to processing of the surface roughness profiles can be formulated, tested, and built in the existing GUI.

SI engineers need models which describe conductor surface roughness on PCBs. A review of the existing surface roughness models is given in Section 4. No matter how different these models are, there is a common feature of all of them. In all these models, a surface roughness is considered as some geometrical structure (*e.g.*, a periodic structure, an impedance boundary condition, or a thin layer with some effective parameters) placed on a *smooth flat conducting basement*. The latter is either a signal trace surface, or a surface of a return plane.

However, the existing algorithm as described in Sections 3.2-3.7 does not provide a flat basis for roughness peaks, even though the roughness profile processing and quantification includes an operation of de-trending. When fitted trend is removed from the roughness profile, a part of the profile appears to be below the zero level, as is shown in Figure 3.16. The valleys under the zero level have different amplitudes. From Figure 3.22 is seen that the envelope around the valleys is not flat at all. This lack of flatness makes questionable the validity of using the extracted roughness profile in a model with a flat smooth conductor as a basis.

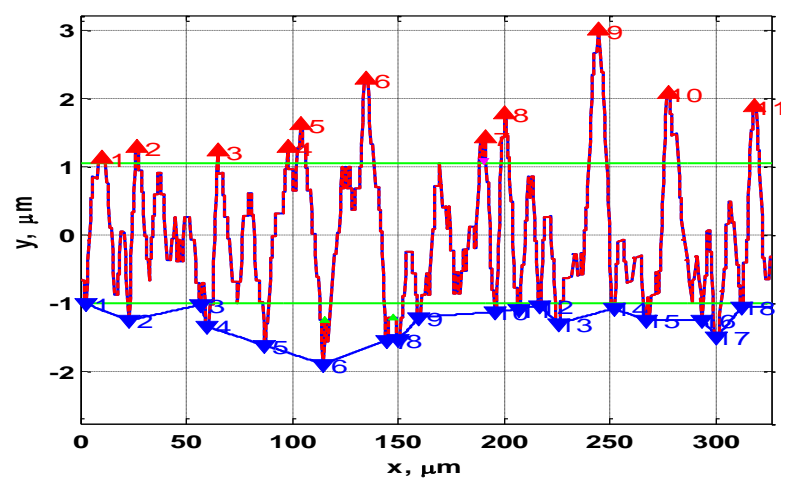


Figure 3.22 Extracted profile with non-flat envelope around valleys

Herein, it is proposed to apply the operation of subtraction of the valleys envelope from extracted profile instead of the de-trending operation. This means that the extracted roughness profile can be considered as the geometrical construction on the flat basement, as is shown in Figure 3.23.

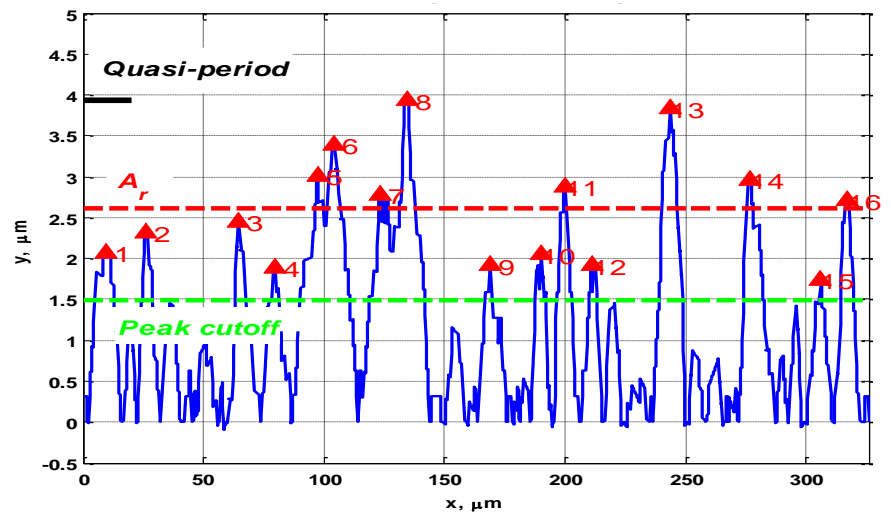


Figure 3.23 Enforcement of flat base for roughness profile

The data representation has been modified along with the “flattening” of the roughness profile basement. Figure 3.23 demonstrates the calculated roughness parameters. Thus a user has an opportunity of validating the calculated roughness parameters “manually”, *i.e.*, by a mere visual inspection and counting roughness “peaks”. All the “valleys” in this case will be on the zero level.

In addition, all the automatically detected roughness peaks can be superposed on the original cross-sectional microscope image for validation of the correct peaks search as it is shown in Figure 3.24.

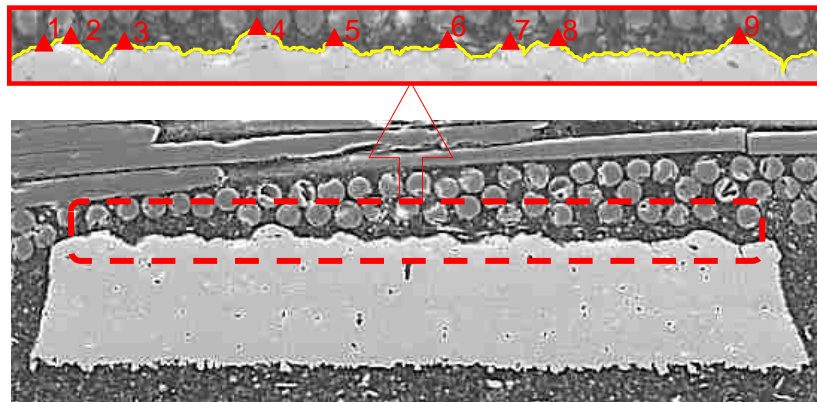


Figure 3.24 An example of the validation of automatically detected peaks

Peaks and valley then are processed separately. First, the detected minima of the extracted profile are processed. The envelope curve around valleys should be captured and subtracted from the extracted profile. Second, the detected maxima of the roughness profile should be processed, and only peaks are used to calculate roughness parameters.



As is mentioned above, there is an analogy between digital signal processing and surface roughness profile processing. A digital signal can be defined by its amplitude, period, pulse waveform, width of a pulse, and duty-cycle. So far, to describe roughness profile, only average peak-to-valley amplitude and quasi-period were used in our algorithm. Using an analogy with signals as functions of time, one can extend a set of the roughness parameters used for surface roughness description as a function of a spatial coordinate, *e.g.*,  $x$ .

An average shape of roughness profile peaks (“a waveform”) can be defined along the coordinate  $x$ . The average width of roughness peaks ( $\tau_r$ ) can be calculated from the average peak shape at some fixed level, *e.g.*, at the zero level of the base, or at  $\frac{1}{2}$  of the peak value. Then the ratio between the average width of the peaks ( $\tau_r$ ) and quasi-period ( $\Lambda_r$ ) can be calculated,

$$RSF = \frac{\tau_r}{\Lambda_r}. \quad (3.7)$$

This ratio is defined herein as a ***roughness shape factor*** (RSF). The parameter RSF is analogous to the duty-cycle for periodic or quasi-periodic signals of time. The calculations of the average shape for roughness profile and the RSF parameter are illustrated by Figure 3.25.

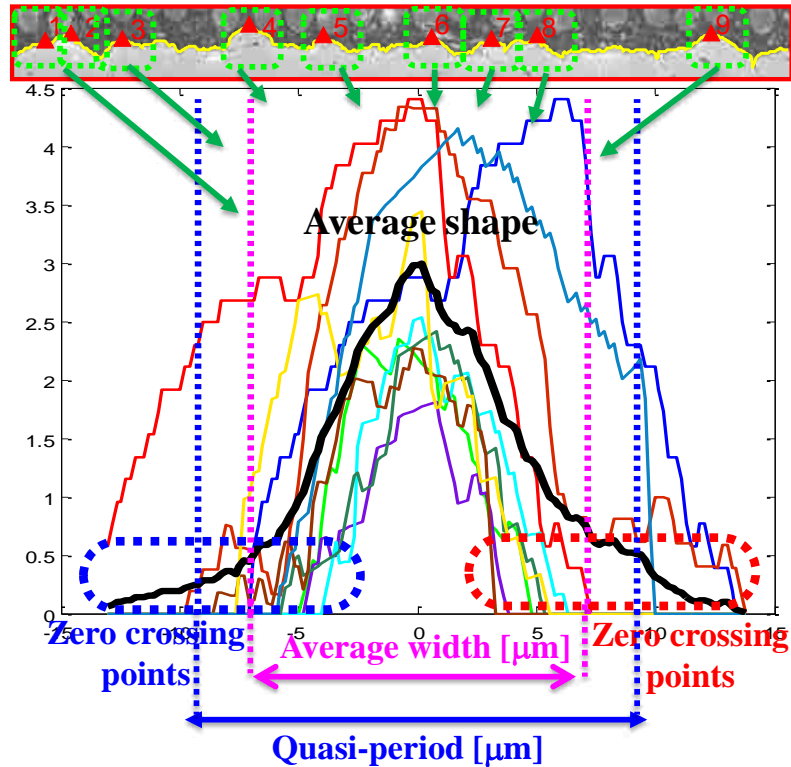


Figure 3.25 Average shape of the peaks along the roughness profile

To calculate an average width of the shape profile, one should first detect zero crossing points on both sides of each peak, as is shown in Figure 3.25. These zero crossing points are intersects of peak profiles with the zero amplitude level. Then average positions of all zero crossing points on each side of the average peak are calculated. The average width is the distance between the averages of these crossing points.

One of the future tasks is to determine how the shape of the peaks affects the insertion loss, and how roughness shape factor can be used for roughness quantification. The extraction algorithm which includes the calculation of a roughness shape factor is presented in Figure 3.26.

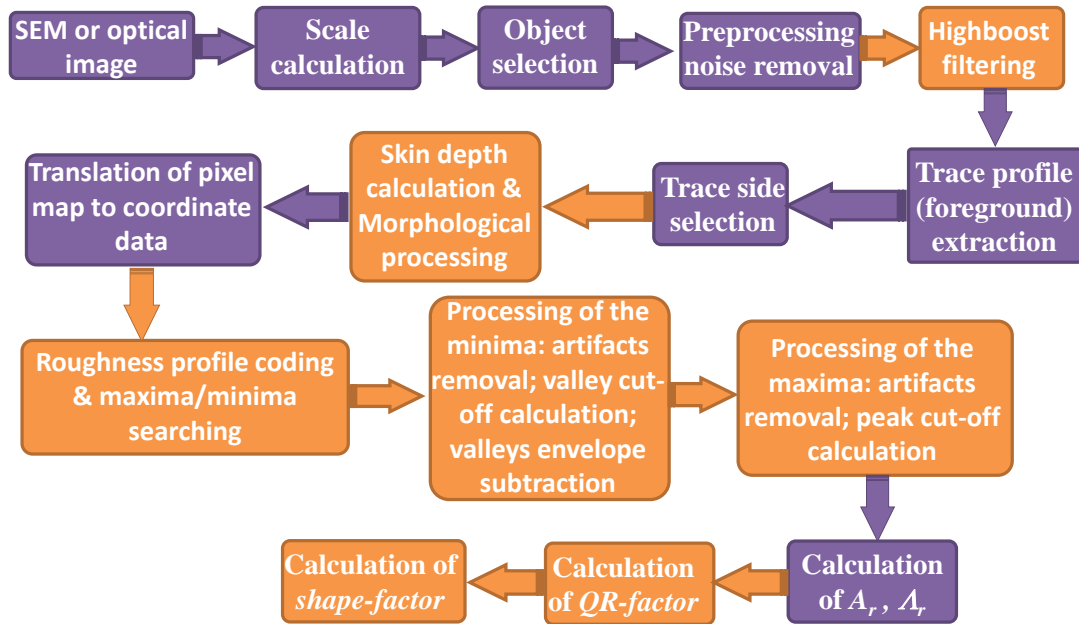


Figure 3.26 Flowchart of the new surface roughness extraction procedure based on the new approach

#### 4. DEVELOPMENT OF DESIGN CURVES

Designers of high-speed electronics to build adequate models of their designs based on PCB interconnects, need accurate data on both properties of dielectrics and conductors in PCBs. There is always an interface between a conductor and a dielectric, and this boundary layer has electromagnetic properties different from those of the base conductor (typically copper foil) and from the ambient dielectric (typically a fiber-glass-filled resin with possible ceramic inclusions). The material parameters of each layer (dielectric, roughness interface, or conductor) need to be known for both analytical and numerical modeling. On the one hand, DK and DF dielectric parameters refined from foil roughness contributions are needed for modeling. On the other hand, knowledge of morphology and conductivity of roughness inhomogeneities are needed to adequately model surface roughness effects.

However, any existing analytical and numerical models of conductor surface roughness are just approximations.

First, information on roughness profile is not always available, or only type of a foil is known (*e.g.*, STD, VLP, RTF, or HVLP), but ranges for roughness parameters could be comparatively wide. To properly model surface roughness, one needs to inspect and quantify this roughness, as is discussed in Section 3.

Second, any model applies some simplifications compared to the actual foil profile. Thus random in principle roughness profile is represented as a periodic or quasi-periodic function of coordinates as is done in [60], [61], [62], and [63].

The existing stochastic models of interconnects with roughness function along either one [61], or two spatial coordinates [64], [65], [66], use small perturbation

approach to represent roughness through  $R_{\text{rms}}$  amplitude, correlation length, and correlation function. Small perturbation theory agrees well with empirical Hammerstad-Bekkadal model [67], [68], and some of its modifications [69], but for extremely low-level roughness only ( $R_{\text{rms}} < 1 \mu\text{m}$ ). Such roughness is typical for microwave engineering devices, rather than for PCB interconnects. All the abovementioned papers introduce correction coefficients to effective conductivity of foil due to roughness. Two more models are worth mentioning here, where correction coefficients in electromagnetic power absorption due to roughness are introduced. In paper [70], roughness profile is represented as a 2D surface nested periodically by hemispheres with the same r.m.s. volume as the measured roughness profile. The most interesting is Huray's "snowball" model [3], [71]. This analytically derived model describes electromagnetic loss in a conglomerate of "snowballs" detected on atomic-force microscopy pictures of some groups of foil (Isola Group, Inc.). However, statistical distribution of sizes and conductivities of those "snowballs" are unknown and thus are fitting parameters. Another model, which uses periodic representation of roughness is described in [72]. The interface layer between a rough conductor and dielectric is substituted by impedance boundary conditions, as in [61]. However, these impedance boundary conditions are correlated with the effective constitutive parameters of magneto-dielectric composite appearing due to roughness in the shape of a rectangular periodic function.

Some researchers numerically model surface roughness by introducing pseudo-random patterns [73]. However, this "brute force" approach is unpractical, since it requires enormous computer resources, and still not able to reproduce the actual roughness. A technique based on a numerical finite-element method with Trefftz

elements and local impedance adjustment is described in [74]. However, this technique requires specialized numerical codes, and operates with r.m.s. amplitude  $R_{\text{rms}}$  and period of roughness function.

Study of roughness effects on both loss constant  $\alpha$  and phase constant  $\beta$  of TEM waves propagating in PCB test vehicles are important for accurate wideband measuring of dielectric constant DK and dissipation factor DF of dielectric substrates. Experiment-based differential and extrapolation techniques have been proposed earlier to get the refined of roughness contributions wideband DK and DF data: DERM technique described in [22], and DERM2 technique described in [52]. The DERM technique is based on curve-fitting of the total measured loss on the stripline as

$$\alpha_T = K_1\sqrt{\omega} + K_2\omega + K_3\omega^2, \quad (4.1)$$

and on building auxiliary curves of corresponding curve-fitting coefficients  $K_1, K_2,$  and  $K_3$  as functions of average peak-to-valley roughness amplitude  $A_r$  on the roughest (“foil”) side of copper conductors. Then the smooth conductor loss ( $\alpha_{c_0}$ ) and the refined dielectric loss  $\alpha_D$  are found by extrapolating these auxiliary curves to zero roughness. The loss due to roughness  $\alpha_r$  is found as the difference

$$\alpha_r = \alpha_T - (\alpha_{c_0} + \alpha_D). \quad (4.2)$$

In the DERM2 technique, the similar procedure is also done with respect to the total phase constant

$$\beta_T = B_1\sqrt{\omega} + B_2\omega + B_3\omega^2, \quad (4.3)$$

which assures for more accurate extraction of DK and DF of the fiber-glass filled resin laminate dielectric. This approach (DERM2) was tested on extracting dielectric properties of PCB dielectrics on two sets of test vehicles with the same dielectric, the same geometry, but different types of copper foils (three samples in each set), and has shown excellent agreement between the extracted results: the difference in DK curves does not exceed 0.02%, while the difference in DF curves is less than 0.08% over the entire frequency range of measurements (from 50 MHz to 20 GHz) [52].

The data extracted using DERM and DERM2 techniques were used for numerical modeling of PCB striplines and comparing modeled results with measurements. This is done in the papers [51] and [75].

In [51], the Effective Roughness Dielectric (ERD) approach was proposed to substitute an inhomogeneous roughness boundary layer by a layer with homogenized dielectric properties (a composite containing epoxy resin and copper inclusions with decreased conductivity). The presence of the ERD layer allowed for getting the proper loss in addition to smooth conductor loss and dielectric loss due to the refined DK.

In [75], the differential extrapolation roughness measurement technique (DERM) is first used to extract the dielectric properties of the substrate used for lamination, and then a periodic model of roughness based on Floquet theory [76] for a periodically distributed over the flat metal surface conducting hemispheres is used to calculate the equivalent roughened conductor surface impedance, which is then used to modify the transmission line per-unit-length parameters  $R$  and  $L$ . The parameters of roughness are taken for the same set of foils as in [22]: the height of hemispheres was equal to  $A_r$ , the period of the net is  $\Lambda_r$  in both directions, and the radius of the base of hemispheres was

chosen (0.25-0.4)  $\Lambda_r$ , depending on the foil profile as was seen in SEM pictures. This approach is validated using both a full-wave simulation tool (HFSS) and measurements, and is shown to provide robust results for the attenuation constant within 0.2 Np/m up to 20 GHz.

The works [22], [51], and [52] lay the basis to the development of the experiment-based *design curves*, which would allow for efficient modeling of transmission lines over wide frequency range at least till 30 GHz. The *objective* is to be able to easily incorporate these design curves into analytical and numerical models. To realize this objective, it is important to introduce a proper metric for surface roughness on each type of foil in a PCB transmission line, and correlate this metric with loss on the line.

#### 4.1. EXPERIMENTAL SAMPLES AND SETUP

Two sets of test vehicles have been tested – Set I and Set II, each containing striplines of identical (as close as technologically possible) cross-sectional geometry and length ( $L=15,410$  mils). Table 4.1 contains the cross-sectional geometry data for these two sets of test vehicles, and for the third one, which will be discussed later. Dielectric used in all these test vehicles was the same (Megtron 6), from the same manufacturer. Types of foils in these two groups were different: STD, RTF, and HVLP foils in Set I, and STDR (rougher than STD), RTF, and HVLP foils in Set II. The pictures of the cross-sections of the traces are shown in Figure 4.1.



**Table 4.1 Geometrical and Roughness Data for Two Sets of Test Vehicles**

		$w_1$ , $\mu m$	$w_2$ , $\mu m$	$H$ , $\mu m$	$P(user)$ , $\mu m$	$h_1$ , $\mu m$	$h_2$ , $\mu m$	$A_{r1}$ , $\mu m$	$A_{r2}$ , $\mu m$	$\Lambda_1$ , $\mu m$	$\Lambda_2$ , $\mu m$	$A_{r1}/\Lambda_1$	$A_{r2}/\Lambda_2$	QR
SET	STD	186.8	203.5	31.4	457.9	164.0	196.2	1.14	6.75	25.65	19.45	0.0443	0.3533	0.398
I	RTF	187.0	200.1	33.2	455.4	167.1	192.4	3.97	2.60	27.34	15.19	0.1462	0.1754	0.321
	HVLP	177.0	187.5	31.8	430.9	163.5	195.3	0.87	0.97	21.11	19.57	0.0421	0.0513	0.093
SET	STDR	181.1	199.2	33.2	457.5	168.0	197.3	1.47	7.52	12.28	25.37	0.1214	0.2964	0.418
II	RTF	185.7	200.1	33.5	452.1	163.1	196.0	3.40	2.39	18.88	15.92	0.1795	0.1501	0.330
	HVLP	181.4	191.7	32.2	438.5	165.4	193.9	1.77	1.20	13.70	18.40	0.1292	0.0665	0.196

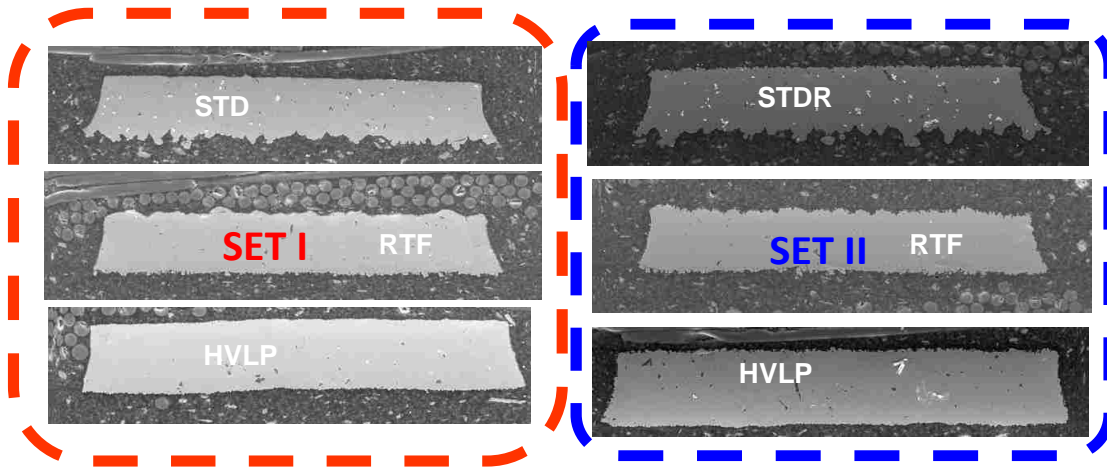


Figure 4.1 Two sets of test vehicles under study

## 4.2. IMPROVED DIFFERENTIAL EXTRAPOLATION MEASUREMENT TECHNIQUE (DERM2)

The extrapolation to zero roughness in DERM2 procedure is illustrated by Figure 4.2 and Figure 4.3. Herein, the roughness factor

$$QR = \frac{A_{r1}}{\Lambda_{r1}} \Big|_{oxide} + \frac{A_{r2}}{\Lambda_{r2}} \Big|_{foil} \quad (4.4)$$

has been chosen for the abscissa axis to build auxiliary curves in DERM2 procedure (after morphological processing as is done in Section 3). Roughness shape factor  $\tau_R$  is not taken into account.

The curve-fitting coefficients for losses and phase constants, as well as the extracted by applying DERM2 roughness parameters for all three sets of test vehicles, are collected in Table 4.2. The measurements of S-parameters, from which these curve-fitting coefficients were obtained, have been conducted over the frequency range from 10 MHz to 30 GHz in 6401 frequency points.

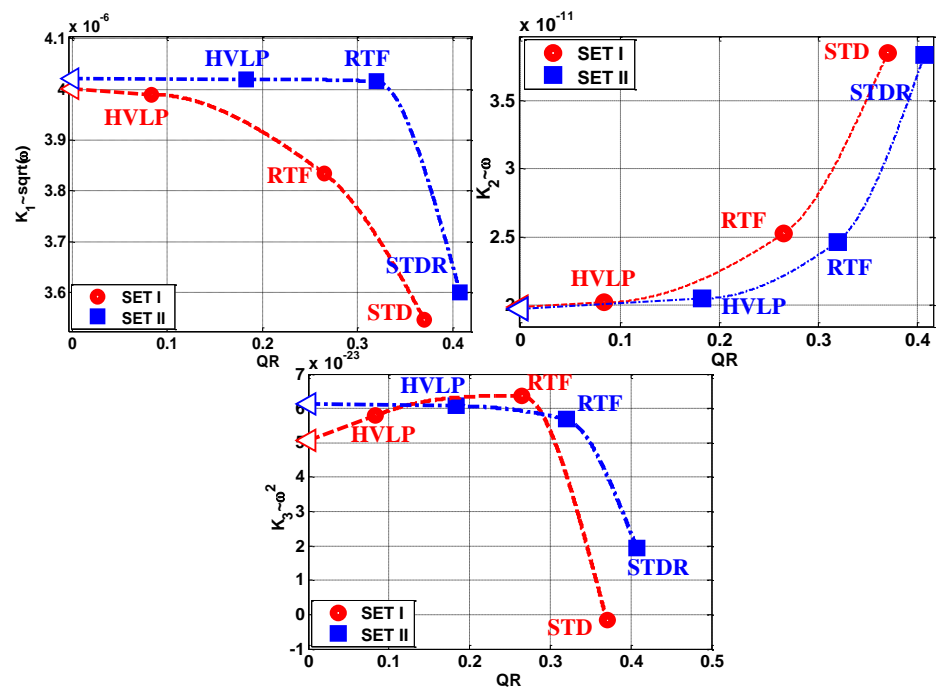


Figure 4.2 Extrapolation to zero roughness in DERM2 procedure applied to total loss on two sets of test vehicles with different foil roughness levels

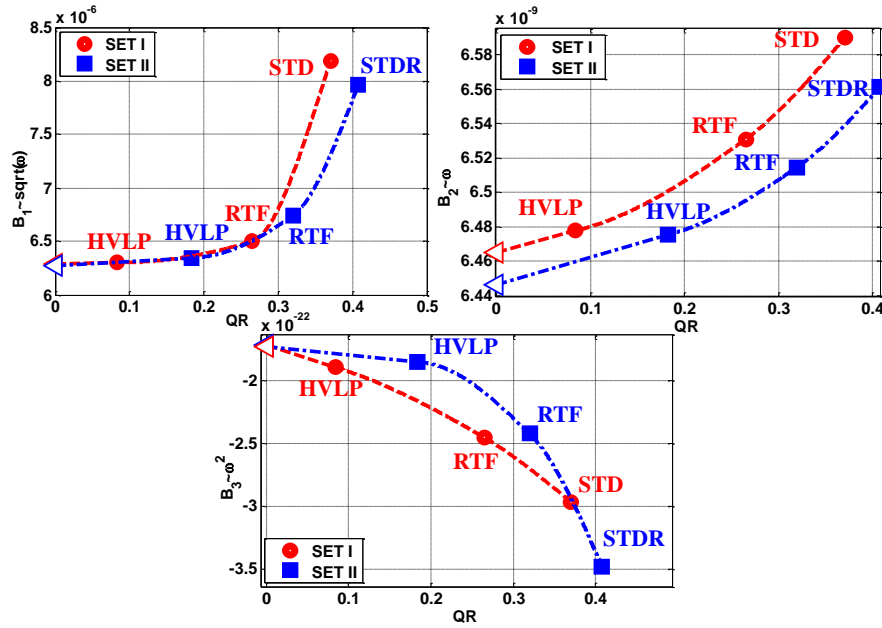


Figure 4.3 Extrapolation to zero roughness in DERM2 procedure applied to total phase constant on two sets of test vehicles with different foil roughness levels

Table 4.2 Curve-fitting Coefficients for Two Sets of Test Boards

	Foil Type	SET I "M6P-BO"			SET II "M6P-CB"		
		STD	RTF	HVLP	STDR	RTF	HVLP
$\alpha_r$ , Np/m	K1 ( $\sim\sqrt{\omega}$ )	$3.50 \times 10^{-6}$	$2.92 \times 10^{-6}$	$3.37 \times 10^{-6}$	$3.30 \times 10^{-6}$	$3.64 \times 10^{-6}$	$3.85 \times 10^{-6}$
	K2 ( $\sim\omega$ )	$3.92 \times 10^{-11}$	$3.23 \times 10^{-11}$	$2.49 \times 10^{-11}$	$4.11 \times 10^{-11}$	$2.82 \times 10^{-11}$	$2.24 \times 10^{-11}$
	K3 ( $\sim\omega^2$ )	$-1.29 \times 10^{-23}$	$9.54 \times 10^{-24}$	$2.34 \times 10^{-23}$	$-7.27 \times 10^{-24}$	$2.12 \times 10^{-23}$	$3.71 \times 10^{-23}$
$\beta_r$ , rad/m	B1 ( $\sim\sqrt{\omega}$ )	$1.13 \times 10^{-6}$	$9.70 \times 10^{-6}$	$8.77 \times 10^{-6}$	$1.04 \times 10^{-5}$	$8.63 \times 10^{-6}$	$7.70 \times 10^{-6}$
	B2 ( $\sim\omega$ )	$6.57 \times 10^{-9}$	$6.51 \times 10^{-9}$	$6.47 \times 10^{-9}$	$6.55 \times 10^{-9}$	$6.51 \times 10^{-9}$	$6.47 \times 10^{-9}$
	B3 ( $\sim\omega^2$ )	$-9.97 \times 10^{-23}$	$-7.03 \times 10^{-23}$	$-3.84 \times 10^{-23}$	$-1.60 \times 10^{-22}$	$-8.97 \times 10^{-23}$	$-7.48 \times 10^{-23}$
$\alpha_s$ , Np/m	R <sub>1</sub> ( $\sim\sqrt{\omega}$ )	$-1.72 \times 10^{-7}$	$-4.78 \times 10^{-7}$	$-2.75 \times 10^{-7}$	$-5.66 \times 10^{-7}$	$-3.97 \times 10^{-7}$	$-1.28 \times 10^{-7}$
	R <sub>2</sub> ( $\sim\omega$ )	$1.91 \times 10^{-11}$	$1.05 \times 10^{-11}$	$3.05 \times 10^{-12}$	$2.01 \times 10^{-11}$	$8.35 \times 10^{-12}$	$2.15 \times 10^{-12}$
	R <sub>3</sub> ( $\sim\omega^2$ )	$-5.46 \times 10^{-23}$	$-2.44 \times 10^{-23}$	$-1.04 \times 10^{-23}$	$-4.78 \times 10^{-23}$	$-2.56 \times 10^{-23}$	$-7.19 \times 10^{-24}$

The extracted smooth conductor loss for Set I and Set II is  $\alpha_{c_0} = 4.0 \times 10^{-6} \sqrt{\omega}$  Np/m, and the dielectric loss obtained by extrapolation to zero roughness for these sets is  $\alpha_D = 2.0 \times 10^{-11} \omega + 5.5 \times 10^{-23} \omega^2$  Np/m. The part of the phase constant associated with conductor and excluded from consideration is  $\beta_c = 6.3 \times 10^{-6} \sqrt{\omega}$  rad/m. The phase constant in the laminate dielectric is  $\beta_D = 6.46 \times 10^{-9} \omega - 1.75 \times 10^{-22} \omega^2$  rad/m. These extracted data are the same for all test vehicles in each set. Roughness contributions in total loss and in phase constant are different because of different roughness profiles on foils used.

The refined from surface roughness dielectric parameters of laminate dielectrics in two sets of test vehicles are presented in Figure 4.4. As this figure shows, there is an excellent agreement between the results of extraction (0.7% for DK and 2.5% for DF) over the frequency range is from 10 MHz to 30 GHz.

The frequency dependences of the pure dielectric loss, smooth conductor loss, and rough conductor loss for all the test vehicles are shown in Figure 4.5. There is a good agreement for the dielectric loss between Set I and Set II; for smooth conductor loss between Set I and Set II; and the rough conductor losses for all test vehicles are different, because foils are different.

The analysis of the insertion loss for the refined from roughness dielectric and smooth conductor loss, calculated as

$$|S_{21}|_{refined} = -8.686(\alpha_D + \alpha_{c_0})L \text{ (dB)}, \quad (4.5)$$

and the measured  $S_{21}(f)$  curves for both sets of boards shows that a foil roughness adds to the slope of the insertion loss as a function of frequency. The higher the roughness, the greater the slope is, as is shown in Figure 4.6.

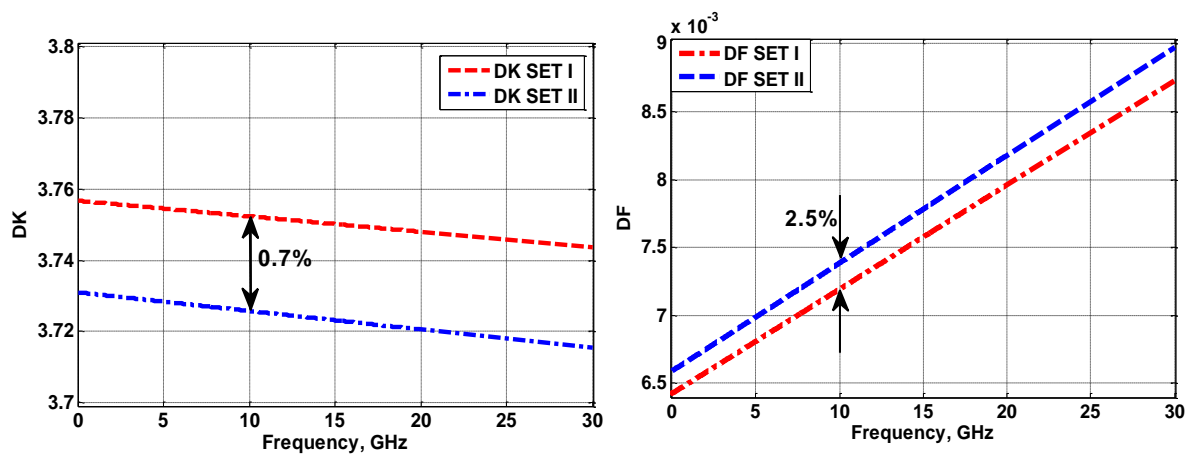


Figure 4.4 Refined from surface roughness dielectric parameters of laminate dielectrics in two sets of test vehicles

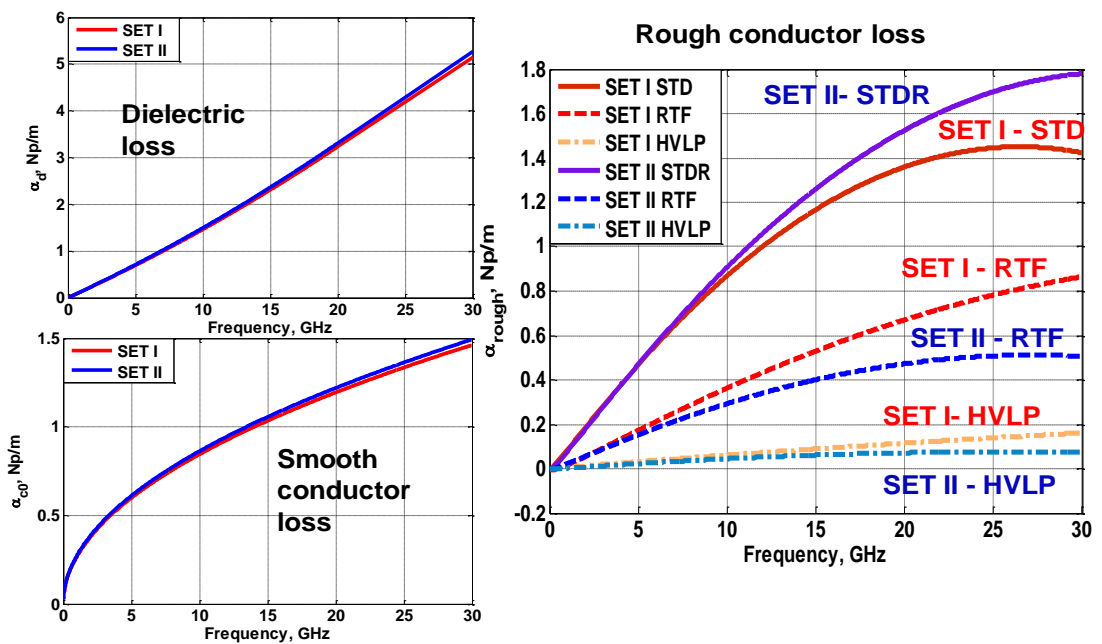


Figure 4.5 Dielectric loss, smooth conductor loss, and rough conductor loss as functions of frequency for both sets of test vehicles

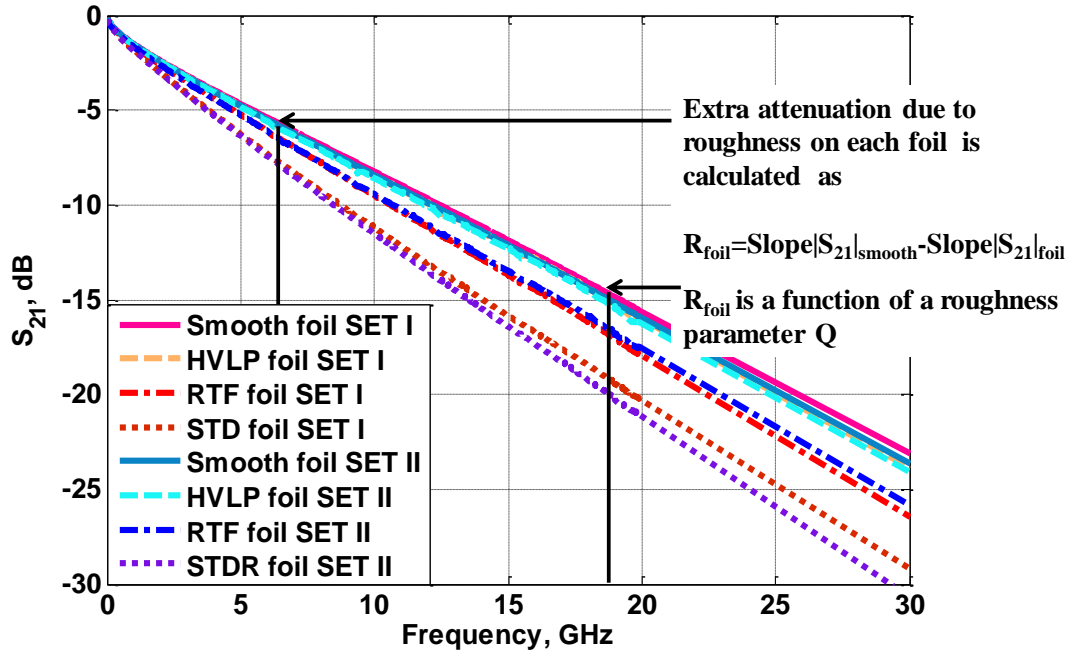


Figure 4.6 Slopes of insertion loss for all test vehicles

#### 4.3. ADDITIONAL SLOPE OF INSERTION LOSS AS A FUNCTION OF FREQUENCY DUE TO FOIL ROUGHNESS

Many roughness models, *e.g.*, Hammerstand-Bekkadal's [67], [68], Groiss's model [69], Huray's model [3], [71], and other, as is mentioned above, deal with the representation of the conductor loss through a roughness correction factor,

$$r = \frac{\Delta\alpha_r}{\alpha_{c0}}, \quad (4.6)$$

where  $\alpha_{c0}$  is the smooth conductor loss, and

$$\Delta\alpha_r = \alpha_c - \alpha_{c0} \quad (4.7)$$

is the loss increment due to roughness. Then the total conductor loss is represented as

$$\alpha_c = \alpha_{c0}(1+r). \quad (4.8)$$

Different roughness models have different forms for the roughness correction factor  $r$ . It is obvious that the presence of  $\Delta\alpha_r$  adds to the slope of the insertion loss.

Thus it is reasonable to calculate additional (extra) attenuation due to roughness  $\Delta\alpha_r$ , or, equivalently, as follows from (4.5), an additional slope due to roughness,

$$R = (\Delta S_{smooth} - \Delta S_{rough}) / \Delta f \quad [dB/GHz], \quad (4.9)$$

where

$$\Delta S_{smooth} = |S_{21}|_{smooth}(f_2) - |S_{21}|_{smooth}(f_1) \quad (4.10)$$

is the slope of  $|S_{21}|$  in the refined smooth case, and

$$\Delta S_{rough} = |S_{21}|_{rough}(f_2) - |S_{21}|_{rough}(f_1) \quad (4.11)$$

is the slope of  $|S_{21}|$  in the rough conductor case, and  $\Delta f = f_2 - f_1$  is the frequency increment.

The calculated additional slopes as a function of the roughness factor  $QR$  for two sets of test vehicles under study are presented in Figure 4.7. As is seen from this figure, even though  $QR$  factors for the analogous foils may differ, the projections on the ordinate axis are comparatively narrow:  $R = (0.01-0.02)$  dB/GHz for HVLP;  $R = (0.09-0.11)$  dB/GHz for RTF; and  $R = (0.030-0.032)$  dB/GHz for STD/STDR foils.

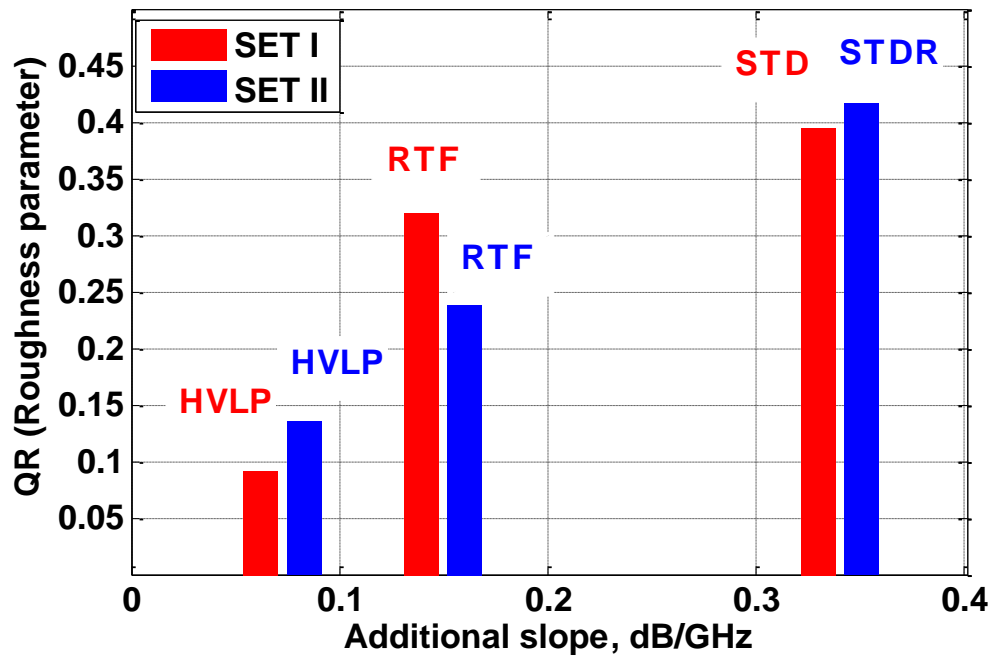


Figure 4.7 Additional slopes in insertion loss due to roughness of foils

Building the dependences  $R=f(QR)$  is a step to the development of the *design curves*. These dependences show how roughness of a certain group of foils affects the insertion loss on a stripline embedded in a PCB.

This information is necessary, but not sufficient to build a model of a high-speed electronics design. A designer needs to know *a priori* the following:

- the exact geometry to be modeled;
- pure dielectric properties (either given by a manufacturer, or predicted by mixing rules for a composite, or measured, *e.g.*, by applying DERM2 technique);
- properties of the smooth conductor (geometry; conductivity; in some cases – permeability); and



- properties of the roughness interface, or a layer (geometrical and/or electromagnetic representation of the roughness).

The latter means that one needs to know the *geometry of the roughness layer*, *e.g.*, its position within the PCB on the appropriate side of a signal trace or ground planes; its thickness (if roughness is modeled as a flat layer of homogeneous thickness); its periodic/quasi-periodic/random structure adopted in the model; and shape and size of roughness inhomogeneities, *e.g.*, “snowballs”, hemispheres, cones, pyramids, or random spikes. It is tempting to simply substitute roughness interface by a layer of fixed thickness and homogeneous effective constitutive electromagnetic properties. This will be discussed below.

#### 4.4. MODEL USING EFFECTIVE ROUGHNESS DIELECTRIC

The *Effective Roughness Dielectric* (ERD) approach was introduced recently in paper [51]. In this paper, the inhomogeneous boundary layer, comprised of “spikes” or “islands” (inclusions) and a surrounding dielectric matrix, is homogenized using a mixing rule for aligned prolate ellipsoids [77], as

$$\varepsilon_{eff,y} = \varepsilon_{matrix} \left( 1 + v_{incl} \frac{\varepsilon_{incl} - \varepsilon_{matrix}}{\varepsilon_{matrix} + (1 - v_{incl}) N_y (\varepsilon_{incl} - \varepsilon_{matrix})} \right), \quad (4.12)$$

where  $\varepsilon_{matrix}$  is the relative permittivity of the matrix material (herein – resin with possibly some ceramic particles). The ellipsoids with the depolarization factor  $N_y$  represent roughness inhomogeneities (“inclusions”) stretching in the  $y$  direction (the propagation direction is  $z$ ). The volume concentration of inclusions  $v_{incl}$  may be comparatively high,

but less than the percolation threshold, *i.e.*, the concentration where the material transforms from a dielectric to a conductor. The complex permittivity of conducting inclusions can be represented as

$$\varepsilon_{incl} = \varepsilon_i - \frac{j\sigma_i}{\omega\varepsilon_0}, \quad (4.13)$$

where  $\sigma_i$  is the intrinsic conductivity of inclusions (may be different from that of copper). This means that the inclusions in the mixture are conducting particles, with significant imaginary part of complex permittivity, while  $\varepsilon_i$  is on the order of 1. The matrix material is assumed to have a complex, non-dispersive over the entire frequency range of interest, permittivity,

$$\varepsilon_{matrix} = \varepsilon'_m - j\varepsilon''_m. \quad (4.14)$$

The laminate fiber-glass filled epoxy resin composite dielectric in the model in [51] is taken the same as the one experimentally tested in [22], and its refined from conductor effects dielectric properties have been extracted using the DERM technique. This data is then used to represent an ambient dielectric in the numerical Q2D model as it is shown in Figure 4.8. The model setups reproduce the cross-sections of the three test vehicles with STD, VLP, and HVLP foils – the geometry is described in [51].

The “roughness dielectric” is modeled as a lossy non-dispersive material for three types of foils with the following parameters [51]:

$$\text{STD: } \varepsilon_{STD} = 48.5 - j18.4 \quad (\tan\delta_{STD}=0.38);$$

$$\text{VLP: } \varepsilon_{VLP} = 33.1 - j4.97 \quad (\tan\delta_{VLP}=0.15);$$

$$\text{HVLP: } \varepsilon_{HVLP} = 28.9 - j1.73 \quad (\tan\delta_{HVLP}=0.06).$$

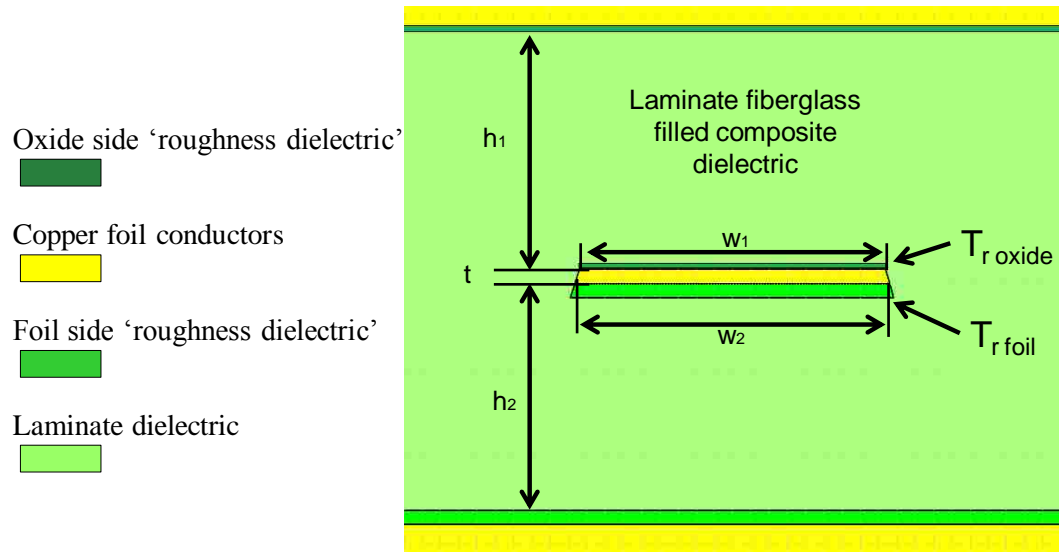


Figure 4.8 Cross-section of stripline in the numerical Q2D modeling setup

As is shown in [51], there is a good agreement between the measured and the 2D FEM modeled insertion loss as a function of frequency, if the abovementioned roughness dielectric data is considered. Thickness of each roughness dielectric layer is taken as the doubled  $A_r$  on the corresponding side of the copper foil.

Herein, the ERD approach is applied to another set of test vehicles, which have identical dielectric, as close as technologically possible geometries, but different types of foils (STD, VLP, and HVLP). The geometrical parameters of the cross-sections of these test vehicles are given in Table 4.3. The length of all test vehicles is the same as before – 15,410 mils (or 39.4 cm).

The dielectric parameters of laminate dielectric refined from roughness are obtained herein using the DERM2 procedure. This is different from applying just DERM

procedure as in paper [52]. The curve-fitting coefficients for frequency dependences of loss and phase constant needed to apply the DERM2 procedure are presented in Table 4.4.

**Table 4.3 Geometrical and Roughness Data for Set of Test Vehicles**

	$w_1, \mu m$	$w_2, \mu m$	$H, \mu m$	$P(user), \mu m$	$h_1, \mu m$	$h_2, \mu m$	$A_{r1}, \mu m$	$A_{r2}, \mu m$	$A_b, \mu m$	$A_2, \mu m$	$A_{r1}/A_1$	$A_{r2}/A_2$	QR
STD	337.9	343.2	16.44	712.8	308	286	0.85	6.2	25	14.2	0.034	0.44	0.474
RTF	364.3	368.5	16.8	769	308	286.4	0.87	2.38	24.7	13	0.035	0.18	0.215
HVLP	329.3	331.3	15.3	691.7	303	292	1.25	1.13	14.3	19.2	0.087	0.06	0.147

**Table 4.4 Curve-fitting Coefficients for Set of Test Vehicles**

Foil Type	$\alpha_r, Np/m$			$\beta_r, rad/m$			$\alpha_s, Np/m$		
	K1 ( $\sim\sqrt{\omega}$ )	K2 ( $\sim\omega$ )	K3 ( $\sim\omega^2$ )	B1 ( $\sim\sqrt{\omega}$ )	B2 ( $\sim\omega$ )	B3 ( $\sim\omega^2$ )	R1 ( $\sim\sqrt{\omega}$ )	R2 ( $\sim\omega$ )	R3 ( $\sim\omega^2$ )
STD	$1.50 \times 10^{-6}$	$3.46 \times 10^{-11}$	$-1.83 \times 10^{-24}$	$7.35 \times 10^{-6}$	$6.64 \times 10^{-9}$	$-1.39 \times 10^{-22}$	$-9.07 \times 10^{-7}$	$1.73 \times 10^{-11}$	$-4.06 \times 10^{-23}$
VLP	$2.28 \times 10^{-6}$	$2.13 \times 10^{-11}$	$2.43 \times 10^{-23}$	$5.63 \times 10^{-6}$	$6.57 \times 10^{-9}$	$-1.02 \times 10^{-22}$	$-1.34 \times 10^{-7}$	$3.98 \times 10^{-12}$	$-1.45 \times 10^{-23}$
HVLP	$2.37 \times 10^{-6}$	$1.85 \times 10^{-11}$	$3.20 \times 10^{-23}$	$5.23 \times 10^{-6}$	$6.56 \times 10^{-9}$	$-9.82 \times 10^{-23}$	$-3.72 \times 10^{-8}$	$1.17 \times 10^{-12}$	$-6.80 \times 10^{-24}$

The extracted DK and DF for the laminate dielectric used in all these test vehicles are shown in Figure 4.9. Figures 4.10 – 4.12 show the measured and modeled (in Q2D software) insertion loss and phase of  $S_{21}$  for the test vehicles with all types of foils – STD, VLP, and HVLP. The good agreement for all test vehicles is achieved with the roughness dielectric parameters summarized in Table 4.5.

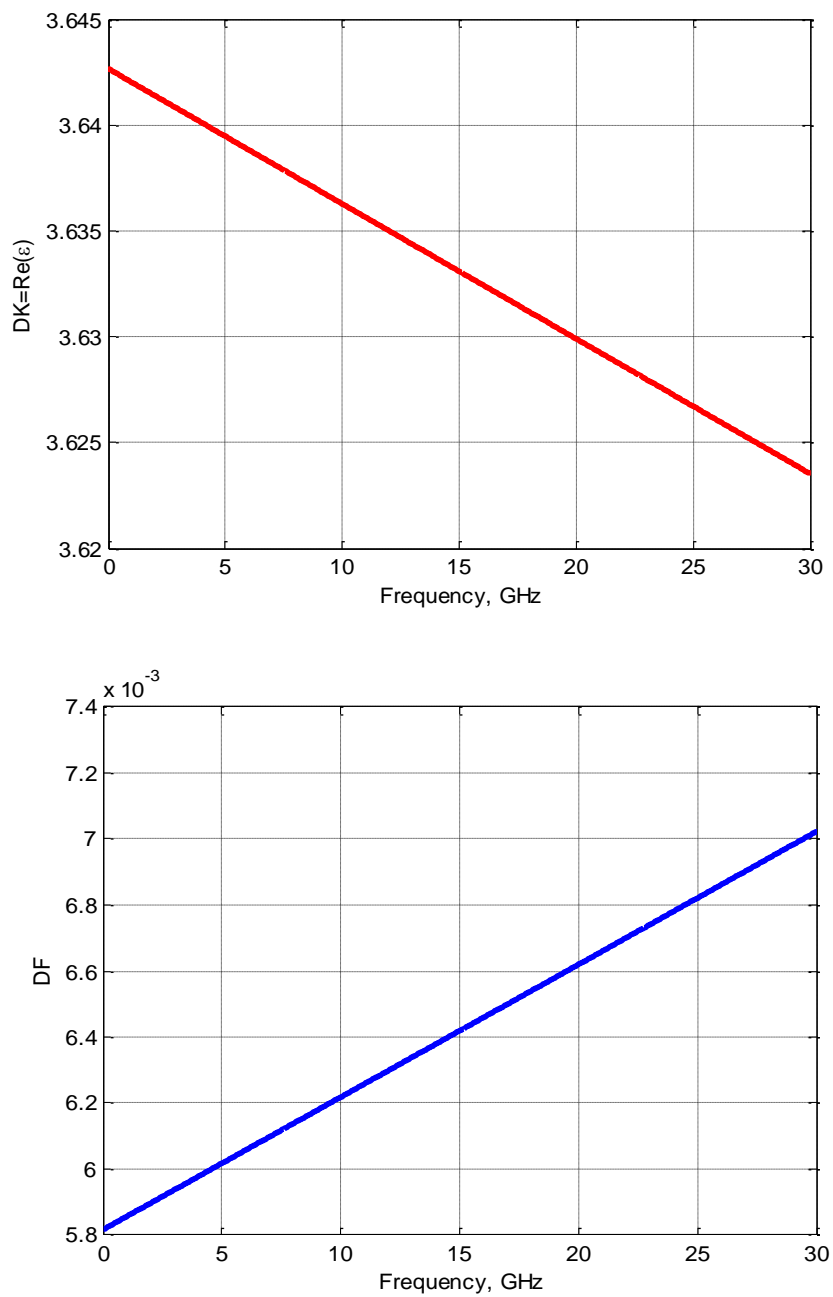


Figure 4.9 DK and DF for all three sets of test vehicles

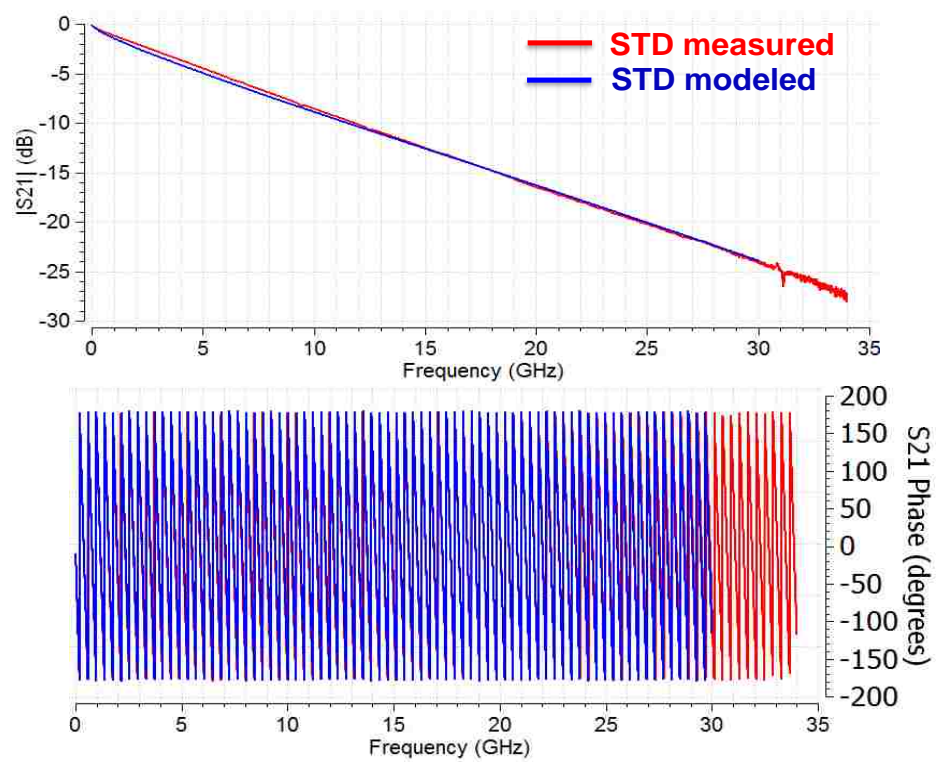


Figure 4.10 Measured and modeled insertion loss  $|S_{21}|$  in the STD test vehicle

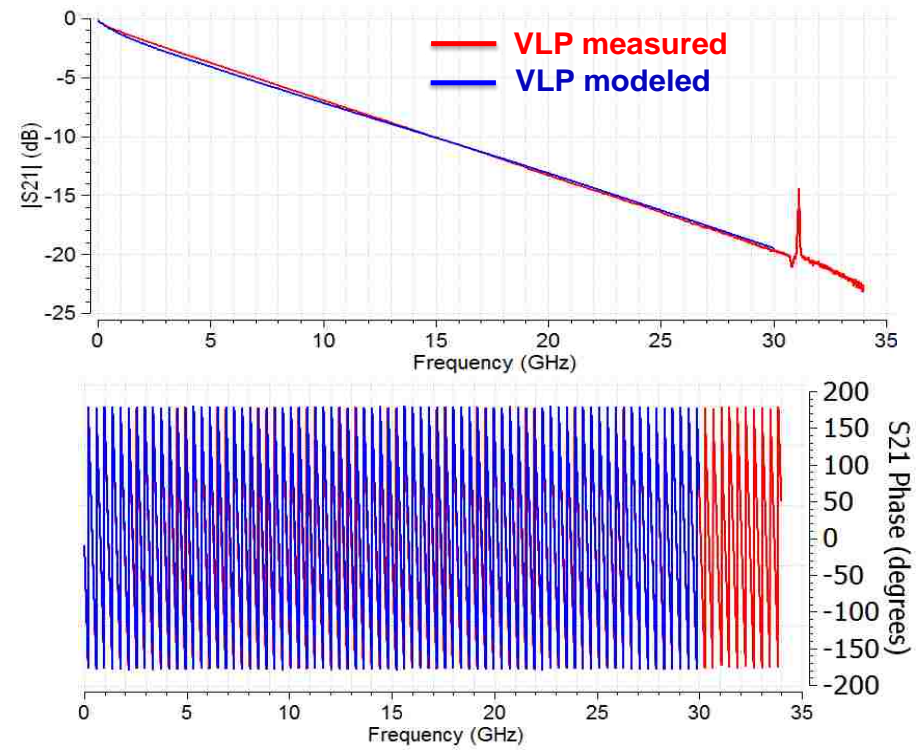


Figure 4.11 Measured and modeled insertion loss  $|S_{21}|$  in the VLP test vehicle

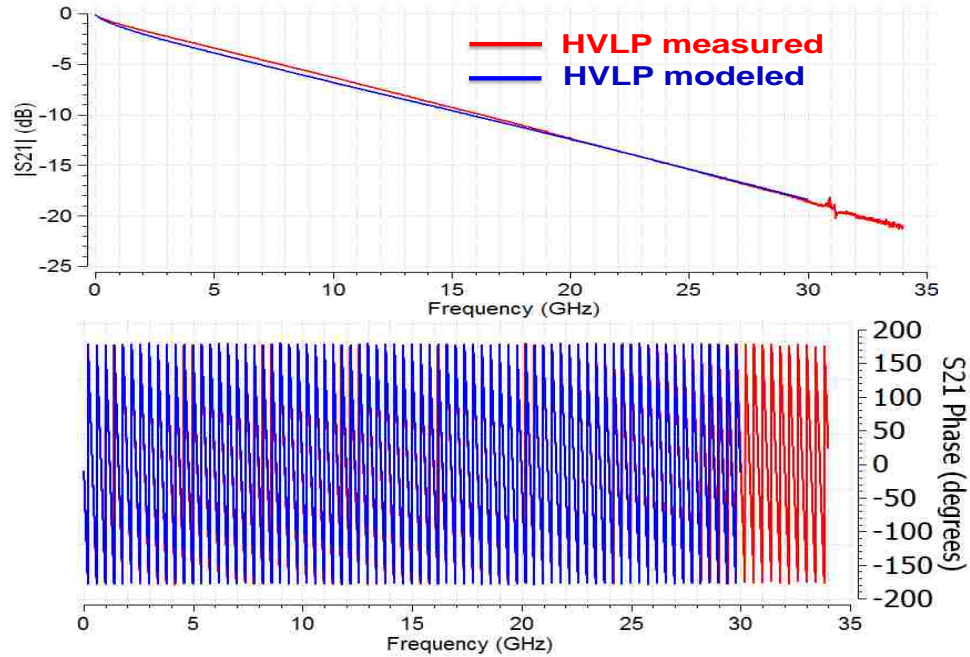


Figure 4.12 Measured and modeled insertion loss  $|S_{21}|$  in the HVLP test vehicle

**Table 4.5 Effective Roughness Dielectric**

	$T_{r1}$ (ox), $\mu\text{m}$	$T_{r2}$ (foil), $\mu\text{m}$	$\tan\delta_r$ (ox)	$\tan\delta_r$ (foil)	$\tan\delta_r$ (sum)	$\epsilon_r$ (ox)	$\epsilon_r$ (foil)	QR
STD	1.70	12.4	0.01	0.42	0.43	15	48	0.474
VLP	1.74	4.76	0.03	0.04	0.07	25	40	0.215
HVLP	2.50	2.26	0.01	0.02	0.03	20	32	0.147

The ERD approach has also been applied to the abovementioned Sets I and II of test vehicles. Their DK and DF were also refined using the DERM2 procedure, and they are shown in Figure 4.4. The modeled and measured data for both sets are shown in Figures 4.13 – 4.15. In these figures, the corresponding roughness loss tangents,  $\tan\delta_{r,o}$  (on the oxide side of the foil) and  $\tan\delta_{r,f}$  (on the foil side of the foil), are indicated. These values were used in modeling the corresponding insertion loss curves to get matching between the measured and modeled curves within  $\pm 0.5$  dB range up to 20 GHz.

Then the total roughness loss tangent for each foil has been calculated as the sum of roughness loss tangents on the oxide and foil sides,

$$\tan \delta_r \approx \tan \delta_{r0} + \tan \delta_{rf}. \quad (4.15)$$

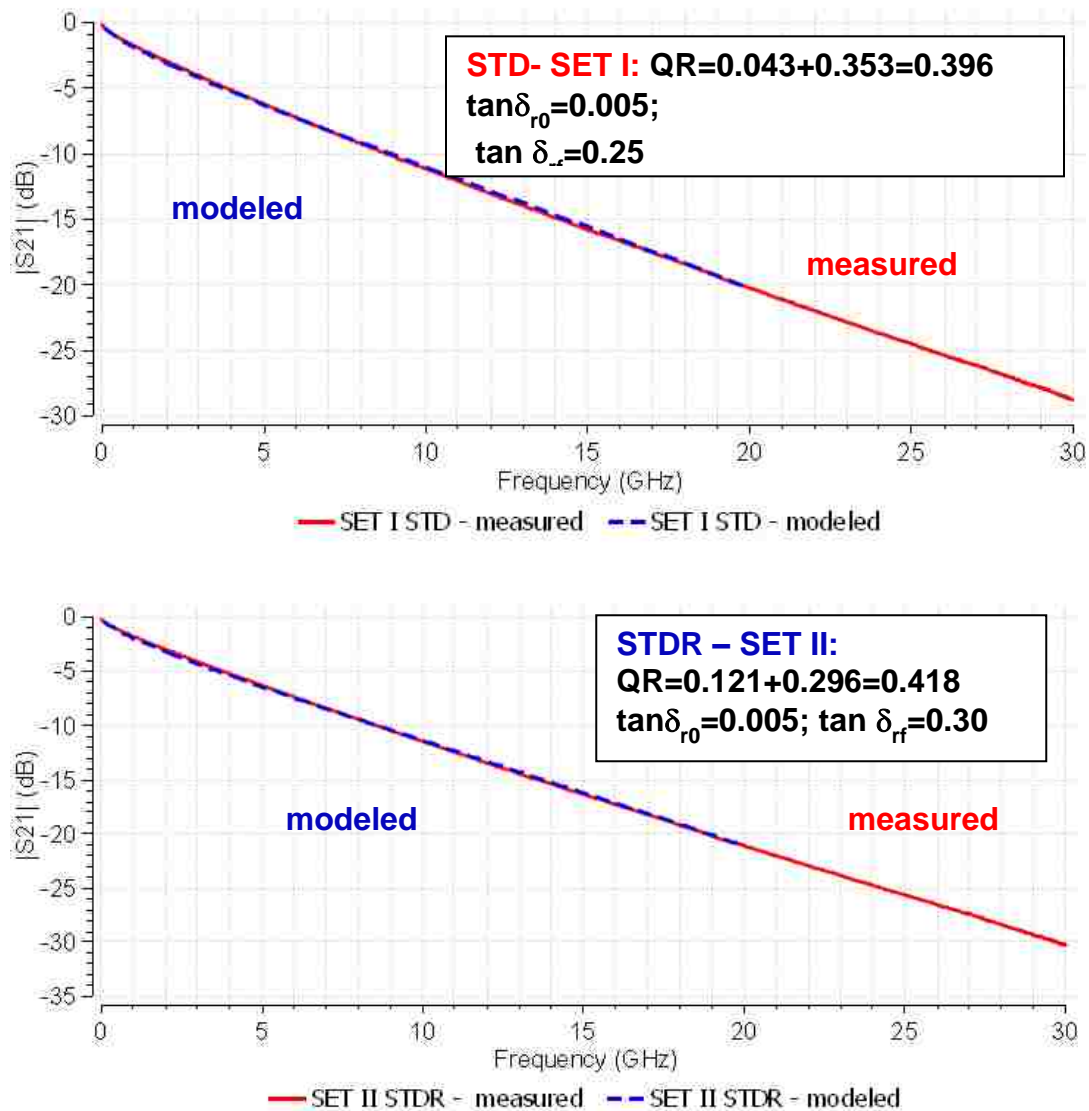


Figure 4.13 Measured and modeled insertion loss in Set I -STD foil and Set II - STDR foil



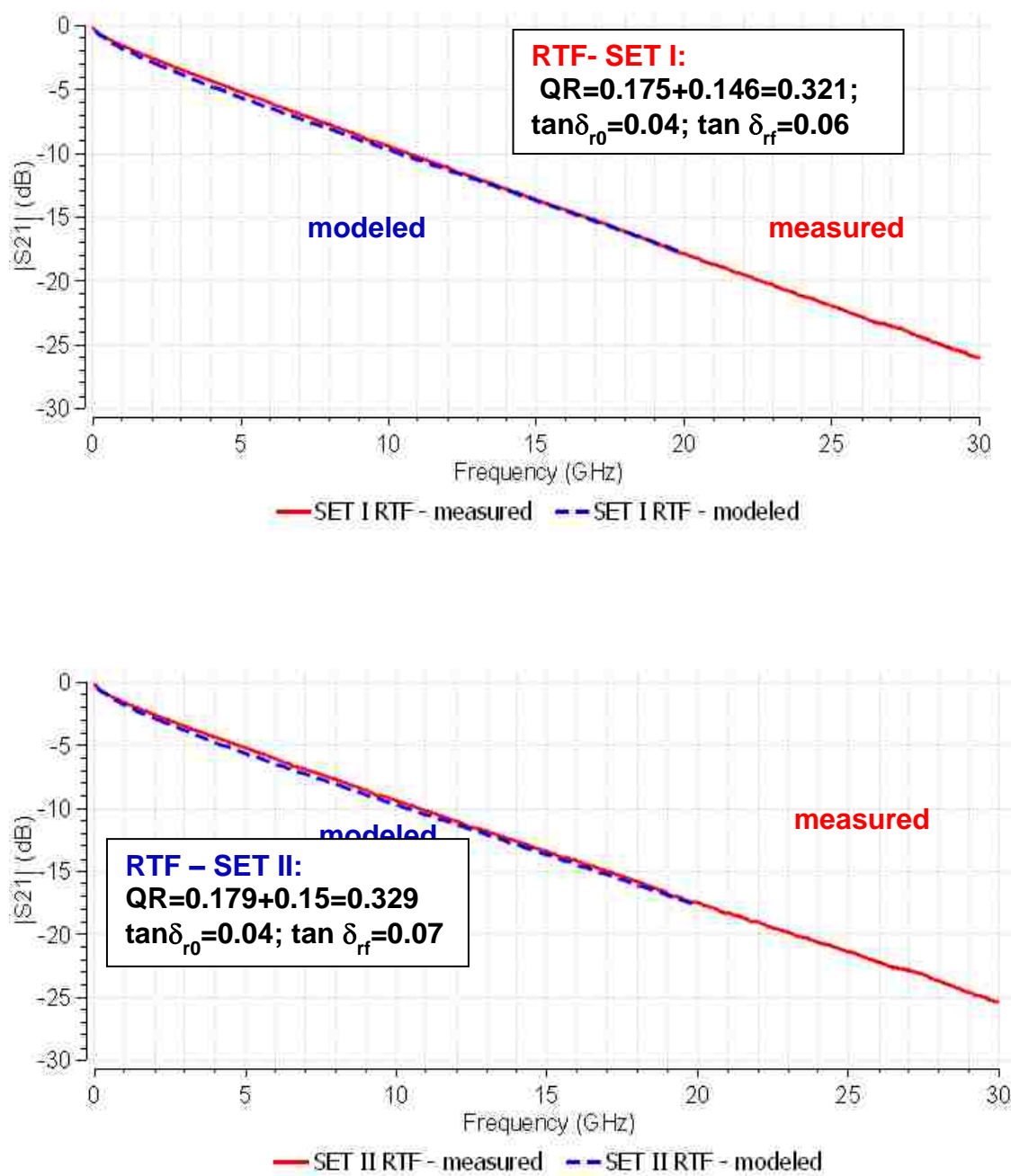


Figure 4.14 Measured and modeled insertion loss in Set I and Set II, both RTF foils

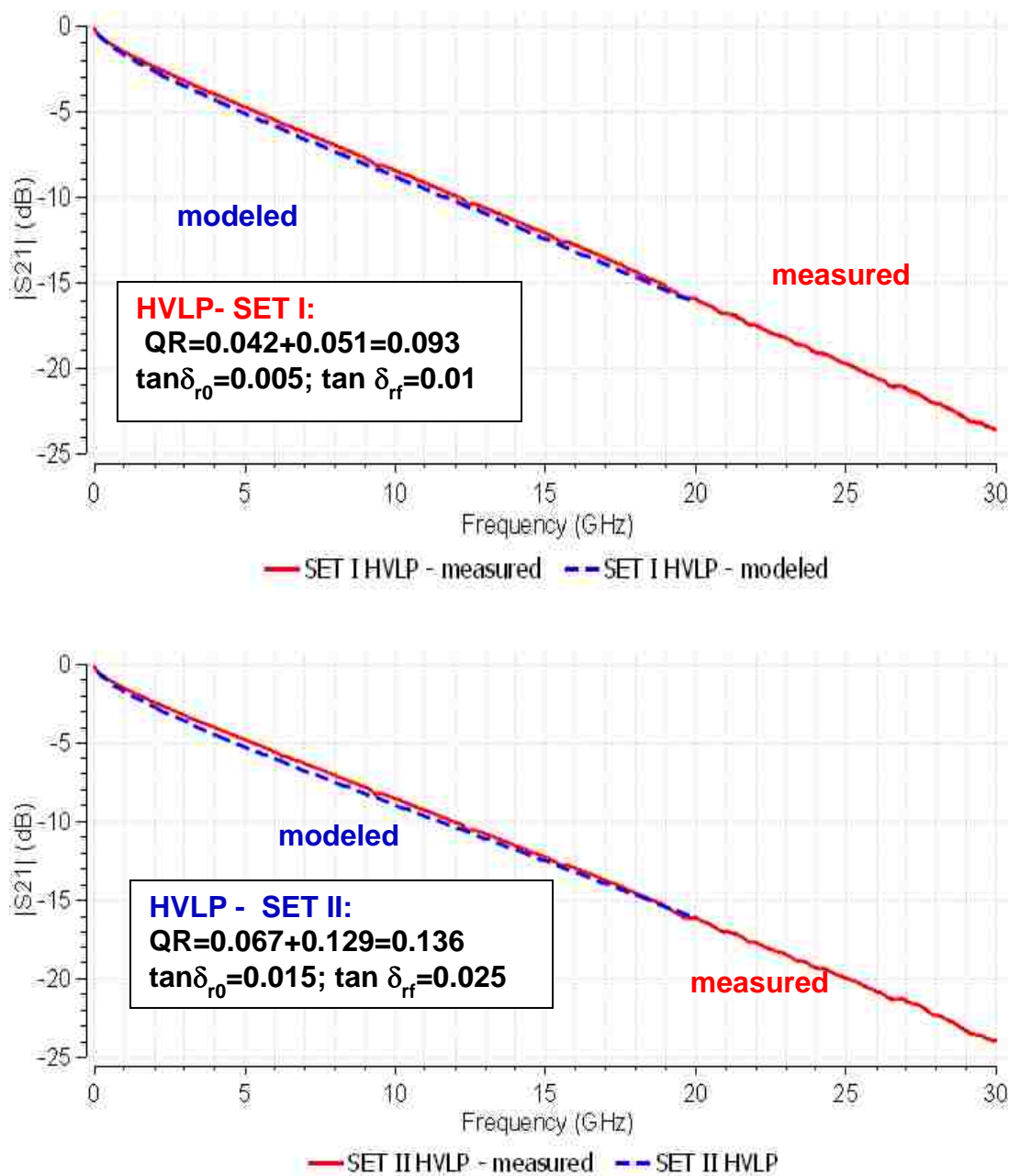


Figure 4.15 Measured and modeled insertion loss in Set I -HVLP foil (a) and Set II -HVLP foil (b)

Figure 4.16 shows the dependences of the total roughness loss tangent  $\tan\delta_r$  on the roughness factor QR for the two sets of test vehicles. Figure 4.17 contains almost

*linear dependences* of the additional slope  $R$  calculated as (4.9) on the total roughness loss tangent  $\tan \delta_r$ .

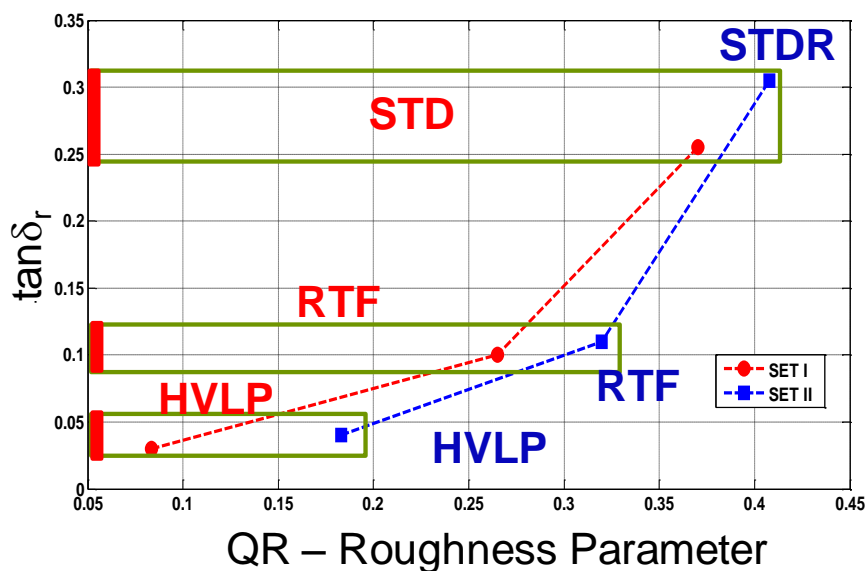


Figure 4.16 Total roughness loss tangent as a function of roughness parameter QR

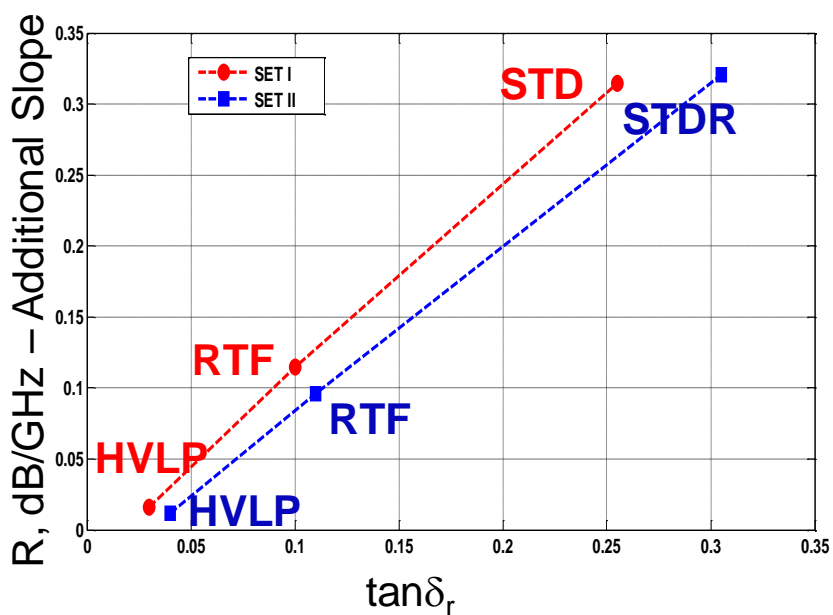


Figure 4.17 Additional slope in  $|S_{21}|$  as a function of the total roughness loss tangent

It is seen from Figure 4.16 that the total roughness loss tangent as a function of QR has a quadratic trend,  $R=kQ^2$ , where  $1<k<2$ . This is an interesting fact, which means that the roughness correction factor  $r$  as in (4.6) depends on the second power of the roughness amplitude  $A_r$ . The similar dependence was noticed in the Sundstroem-Sanderson's small perturbation model with a periodic roughness function of roughness [61], [62], and the correction factor in (4.8) for the conductor loss  $\alpha_{c0}$  is calculated as [78]

$$r = \frac{1}{\delta^2} \sum_{n=1}^{\infty} H_n^2 \left( 1 - \sqrt{\frac{1}{2} \left( \sqrt{n^4 s^4 \delta^4 + 4} - n^2 s^2 \delta^2 \right)} \right), \quad (4.16)$$

where  $H_n$  is the amplitude of the  $n$ -th Fourier harmonic roughness of roughness function, proportional to the roughness amplitude, in particular,  $A_r$ ;  $s=2\pi/\Lambda_r$  is the spatial “wave number”, associated with the roughness function quasi-period  $\Lambda_r$ ; and  $\delta$  is the skin-depth into the conductor.

#### 4.5. SUMMARY

“Design curves” for taking into account conductor surface roughness of different types of foils in PCBs have been defined. A “design curve” shows a variation of the total loss tangent of ERD as a function of the roughness factor QR. The QR parameter was introduced in the previous section as a “metric” of surface roughness of copper foil on a signal trace. A layer of an ERD will cause an additional slope in the  $|S_{21}|$  (f) dependence the same as the actual surface roughness. This additional slope can be associated with roughness correction factor for loss constant.

The “design curves” have been built for a number of sets of test vehicles. Loss tangents of effective roughness dielectrics, along with thickness of the ERD layer, can be directly used in high-speed design models.

## 5. A 50-GHZ TEST VEHICLE DESIGN OPTIMIZATION

Characterization of PCB laminate dielectric materials and copper foils is important for PCB manufacturers and high-speed digital electronics designers from SI point of view. The procedure of extraction dielectric material parameters and conductor losses in stripline structures inside PCBs is based on a traveling-wave method for TEM modes propagating along a stripline. This method includes measuring S-parameters of the specially designed single-ended test-stripline in the frequency domain using a vector network analyzer (VNA).

### 5.1. DESCRIPTION OF THE 30-GHZ TEST VEHICLE AS A PROTOTYPE

Single-ended test-stripline is manufactured inside the SI Test Vehicle. The SI Test Vehicle, which was used before, was designed to operate up to 30 GHz only, and was using “SMA 3.5 mm female” removable connectors. The previous SI Test Vehicle design, which is shown in Figure 5.1, is a 6-layer board, with signal layers on L2 and L5 and duplicate ground planes on L3 and L4.

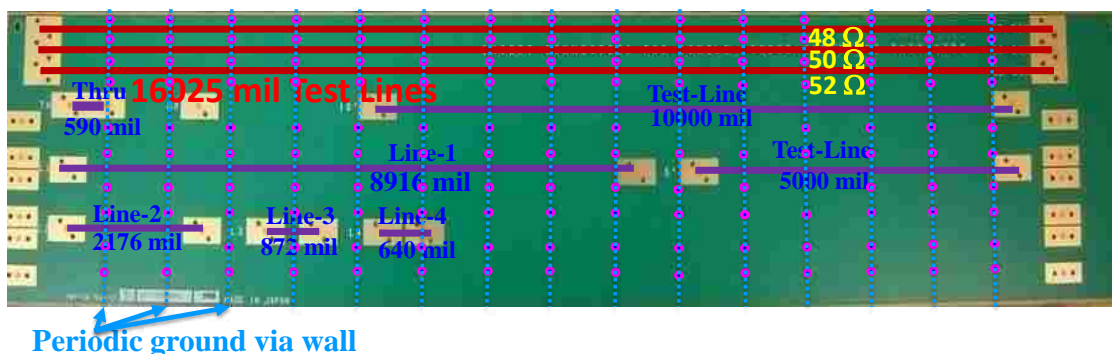


Figure 5.1 Layout of the 30-GHz SI Test Vehicle

All layers are 1-oz base copper. It includes calibration traces on Layer 2. Thru, open, and Line 1-4 calibration traces form the “through-reflect-line” (TRL) calibration pattern are employed to eliminate port effects at the connectors of the Test- lines. Differential traces located on Signal layer L5 are not used for the current material parameter extraction procedure. Stackup for 30-GHz SI Test Vehicle is shown in Figure 5.2.

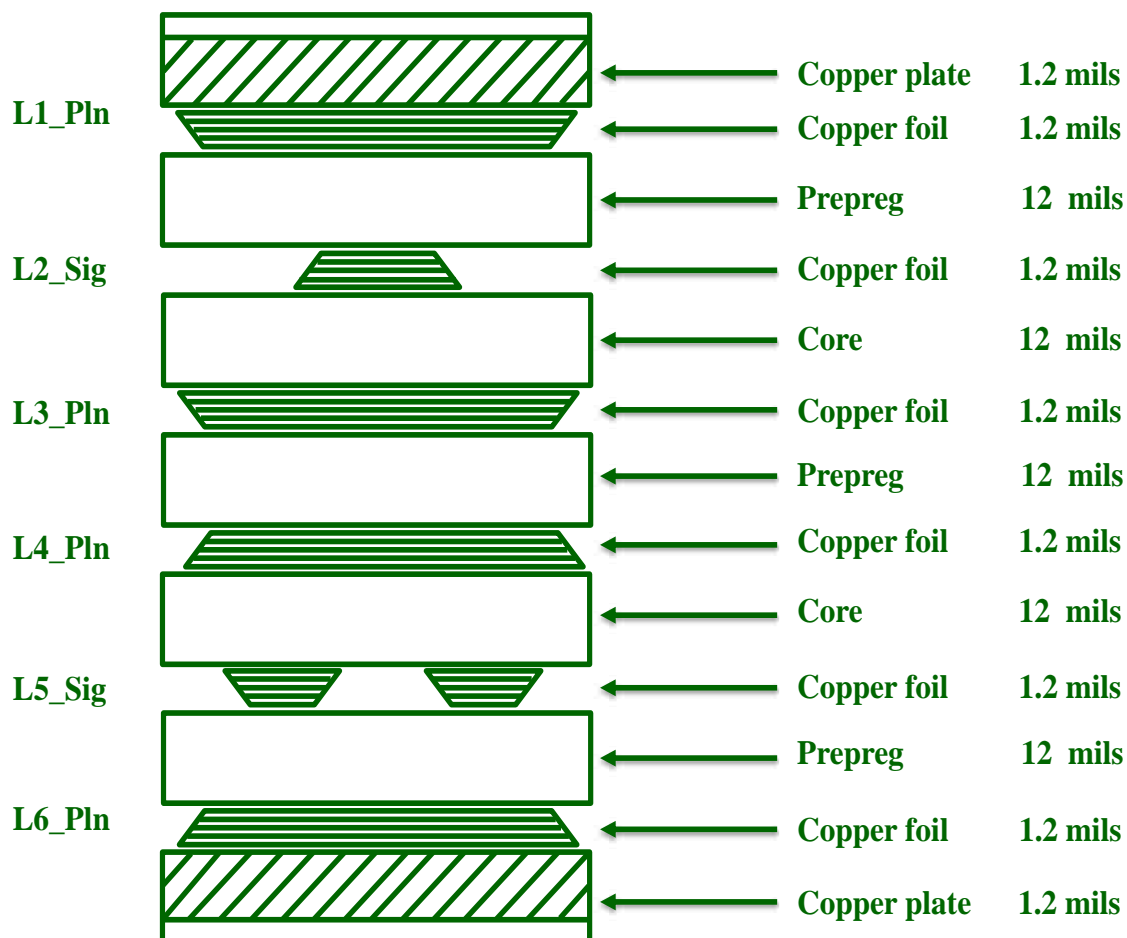


Figure 5.2 Stackup of the 30-GHz SI Test Vehicle

## 5.2. FIRST ATTEMPT TO DESIGN A 50-GHZ TEST VEHICLE

The data rates of high-speed digital designs using PCBs steadily increase with the progress in modern electronics, and hence there is a necessity for extending the frequency range of measuring material properties of PCBs up to 50 GHz. The wider frequency range, the more challenging EM problems arise, such as a high reflections and losses due to signal via-to-signal trace transitions, multiple resonances due to proximity of periodic via structure to the signal trace. These problems corrupt the measured S-parameters, and cause the artifacts, errors, and uncertainties in the material parameter extraction procedure.

The extension of the frequency range up to 50 GHz requires not only improvement of the material parameter extraction procedure, but also necessitates modifying a test vehicle design, or even developing substantially new designs of the test vehicles to satisfy required accuracy of operating at higher frequencies.

The first attempt to design the 50-GHz SI test vehicle was made in 2012 [23], [24]. This was mostly full-wave CST simulation work, based on which a new footprint for 2.4-mm SMA-female removable connectors and a modified signal via-to-signal trace structure were proposed. The CST model setup and S-parameter modeling results for the modified signal via-to-signal trace transition and footprint for of the 50-GHz SI test vehicle are shown in Figure 5.3 and Figure 5.4, respectively.

In addition, this test vehicle had some more modifications compared to the 30-GHz prototype. The new TRL pattern contained six lines. It was proposed to use an aperiodic ground via wall spacing, which was supposed to reduce the resonance effect of ground via wall structure on the propagation along the line. The original periodic ground



via wall structure in the proximity to the signal trace had one-inch spacing and contained 15 ground vias along the entire PCB. The aperiodic ground via wall structure proposed in [23], [24] has the mean spacing of 0.5 inch and totally 31 ground vias.

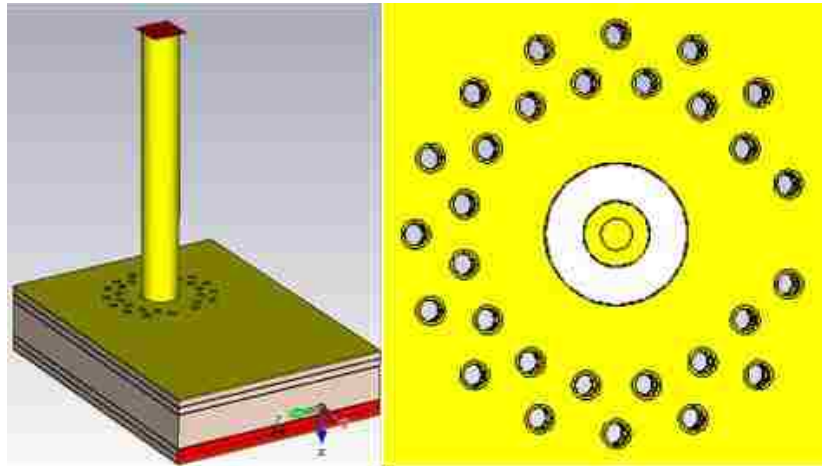


Figure 5.3 CST-model of the modified signal via-to-signal trace transition and footprint for the 50-GHz SI Test Vehicle

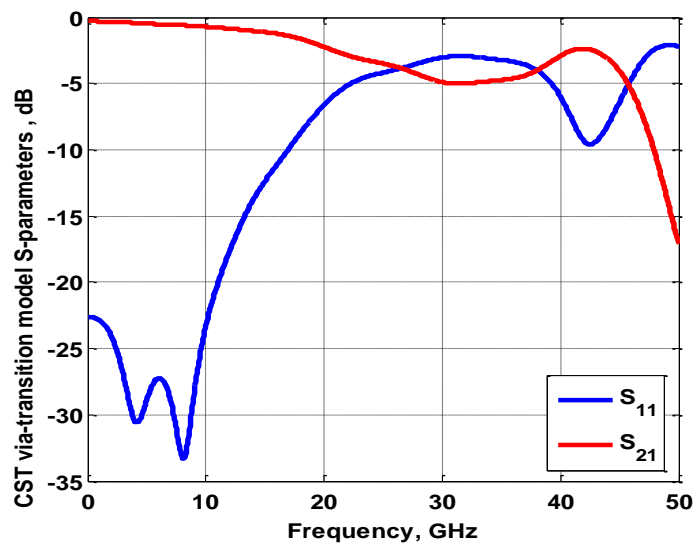


Figure 5.4 CST-modeled S-parameters for the modified signal via-to-signal trace transition

Subsequently, the proposed simulation structures as described in [23], [24] were converted to the artwork manufacture files and fabricated as the first version of the 50-GHz SI test vehicle. Unfortunately, S-parameters, measured on fabricated first version of the 50-GHz SI Test Vehicle, exhibit strong artifacts illustrated by Figure 5.5, which prevent from accurate extraction of material parameters on this test board. Therefore, further improvement of the 50-GHz test vehicle design is necessary. A design and fabrication of the second version of the 50-GHz SI test vehicle is a part of this present work, the objective of which is to extend material characterization procedure up to 50 GHz.

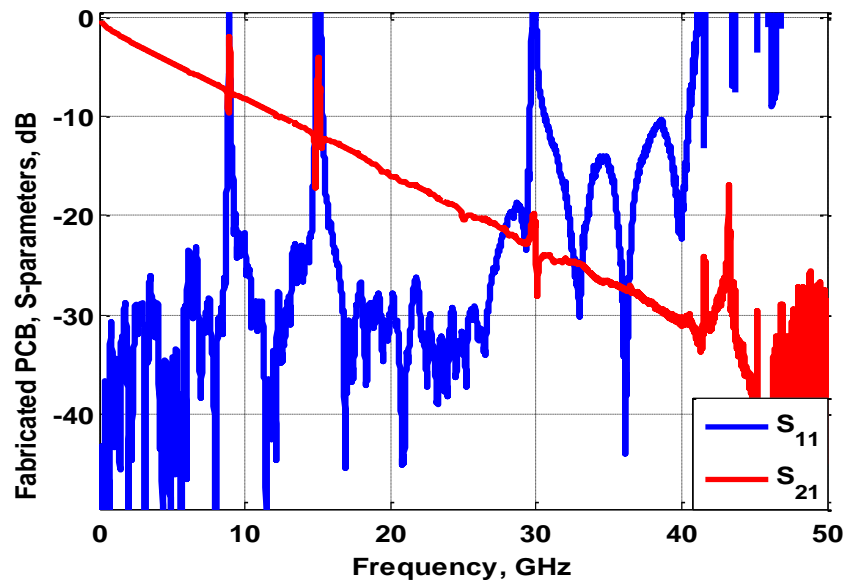


Figure 5.5 S-parameters of the fabricated PCB. The presence of strong resonances prevent from using this board for material parameter measurements.

### 5.3. MOLEX PROTOTYPE OF 50-GHZ VIA TRANSITION

The first step is to design a new via-transition structure. The prototype for this design is the 50-GHz via-transition HFSS model PCB kindly provided by Molex Simulation Design team. Molex's HFSS model has been developed for their complex 16-layer PCB structure. Molex's HFSS model is a connector-to-signal and via-to-signal trace geometrical structure. It contains two power levels, which are not needed in the 50-GHz test vehicle design. The stripline signal trace is 3.3 mils wide. This Molex's HFSS model geometry was converted to the CST model, as is illustrated by Figure 5.6.

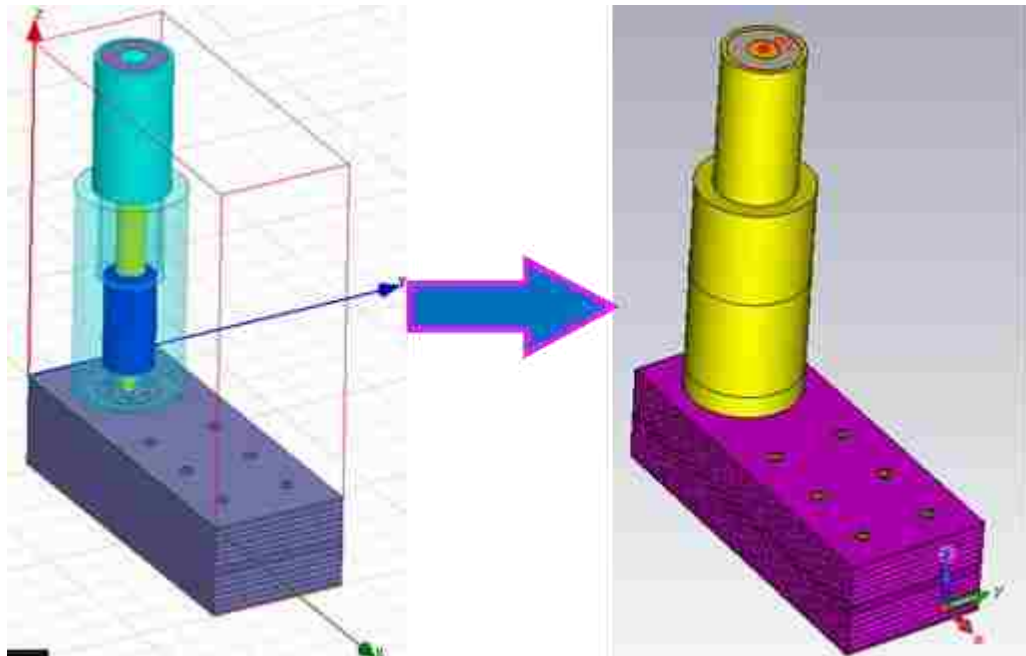


Figure 5.6 Conversion of HFSS Molex's signal via-to-signal trace transition model to CST model

The special properties of Molex via transition model are the rectangular diving boards (shields) on the reference planes below and above with the signal trace, and back drilling.

This is illustrated by Figure 5.7. S-parameters modeled using CST Microwave Studio. S-parameters of Molex structure up to 50 GHz are shown in Figure 5.8. [39].

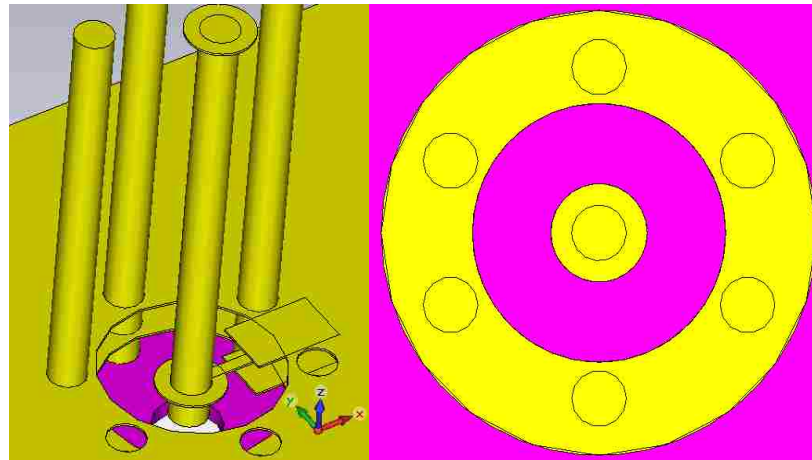


Figure 5.7 Via transition structure and footprint

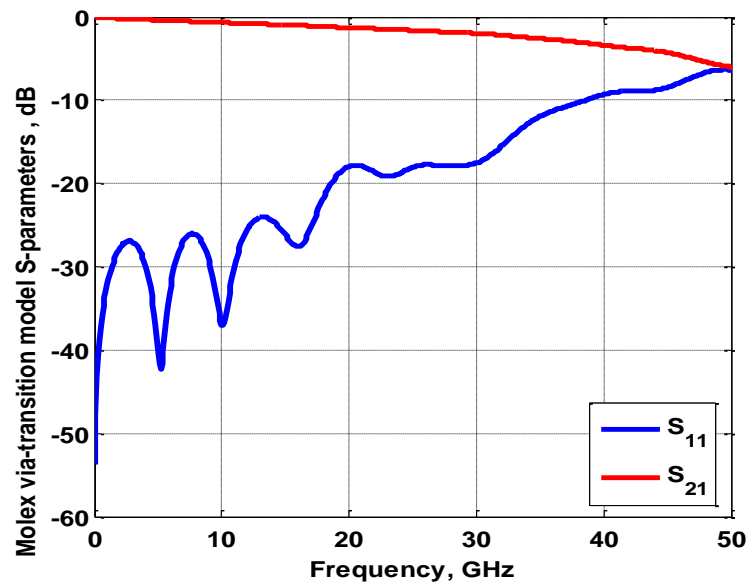


Figure 5.8 CST modeled S-parameters for Molex structure

All the design solutions from the first version of the 50-GHz SI Test vehicle and Molex design were revised and taken into account in the new optimized version.

#### 5.4. A NEW VIA TRANSITION DESIGN FOR 50-GHZ SI TEST VEHICLE

A new CST via transition model was constructed according to the following manufacture tolerances: footprint signal and ground via diameter equals to 12 mils, contact pad diameter is 20 mils, catching ring diameter is 22 mils, and back drill diameter equals 20 mils. The value of 9 mils was chosen for the signal trace width, since the medium width for a trace should be in the range from 8 to 11 mils. Taking into account these tolerances, via transition structure was constructed to have impedance as closer to 50 Ohm as possible in any cross-section. The new CST via transition model is shown in Figure 5.9.

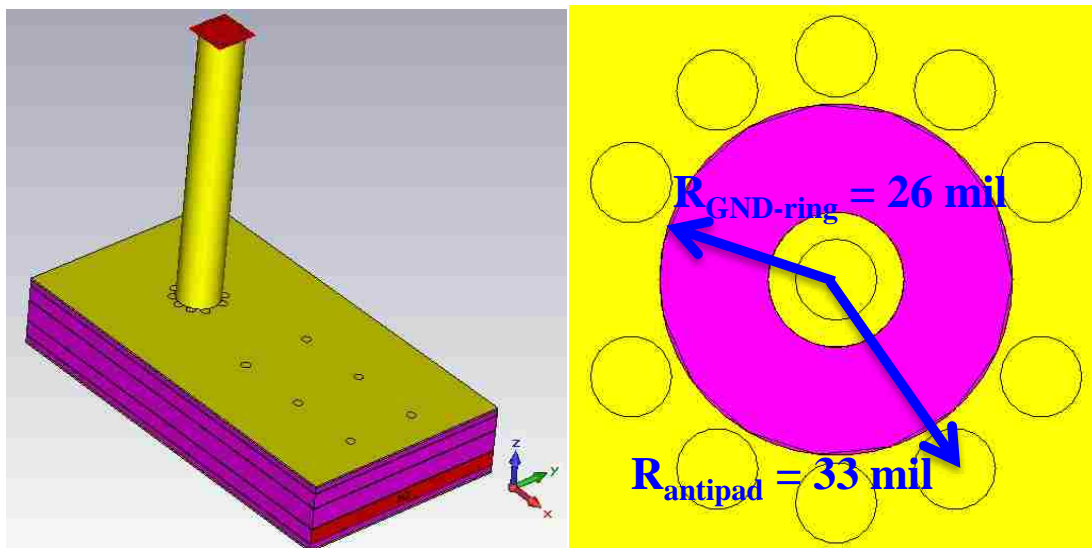


Figure 5.9 CST- via transition model and footprint for the new 50-GHz SI test vehicle design

Geometry optimization procedure was performed according to the following criteria:

- TDR response should show the impedance range around 47-51 Ohms along the signal via-to-signal trace segment.
- The insertion loss (the magnitude of  $S_{21}$  in dB) should be higher than -5 dB over the entire operating frequency range from 50 MHz up to 50 GHz.
- The return losses (the magnitude of  $S_{11}$  in dB) should be lower than -5 dB over the entire operating frequency range from 50 MHz up to 50 GHz.

After about 30 iterations of the optimization procedure, the compromise in the design to achieve the abovementioned criteria has been found. Herein, it was proposed to use smoothly shaped shields, back drilling, and tear drop shape of the transition from a contact catch ring to the signal trace. This significantly reduces impedance discontinuities and consequent reflections, and allows for achieving the claimed characteristics. In the new design, which is shown in Figure 5.10, the upper shield sticks out of the ground ring by 9.75 mils, and the lower shield sticks out of the lower ground ring by 16 mils.

The new footprint in the optimization procedure got extra via compared to the original Molex design, and now it contains ten stitching ground via. The stitching ground vias form an antipad. The radius of the antipad is 33 mils. The radius of the ground ring is 26 mils.

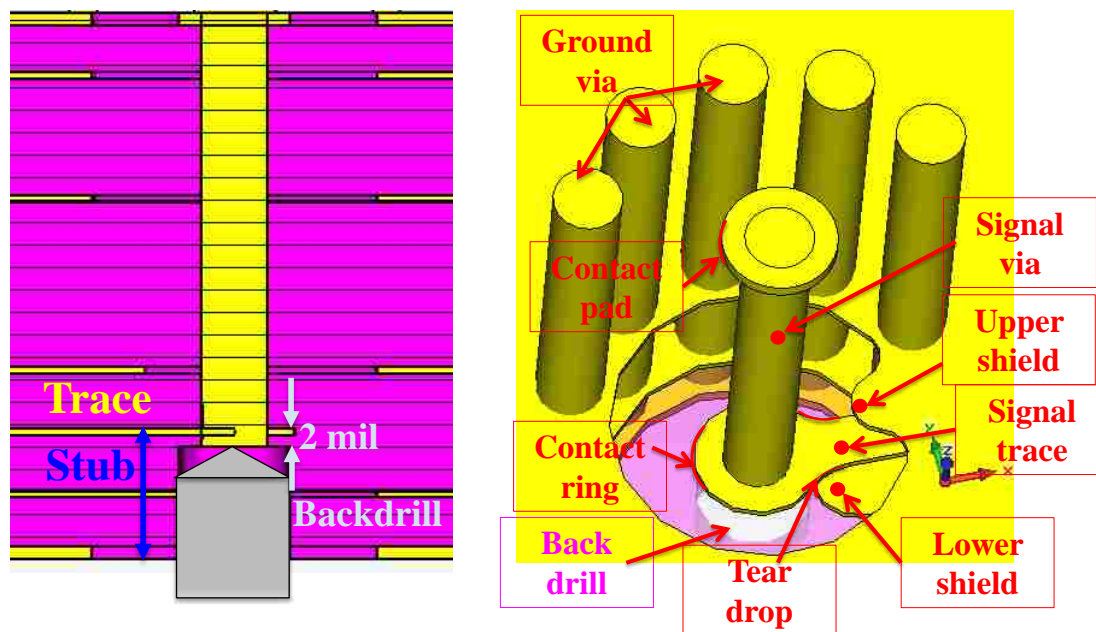


Figure 5.10 Backdrill and new optimized via transition structure

The modeled in CST Microwave Studio S-parameters and TDR response for the new via transition design are shown in Figure 5.11.

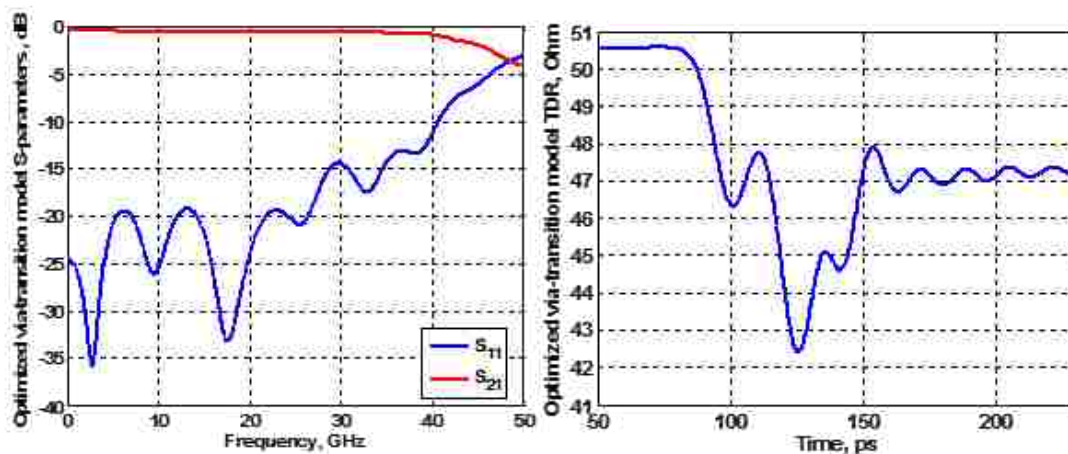


Figure 5.11 Simulated connector-via-trace S-parameters and TDR response for a new designed 50-GHz test vehicle

### 5.5. A NEW GROUND VIA WALL DESIGN

The new aperiodic ground via wall structure is implemented using normal distribution with standard deviation of 0.5 inch around the mean 1-inch value. It contains 15 ground vias.

The following manufacturing tolerances are taken into account. The ground via diameter equals to 63 mils, hence the smallest ground via- to- ground via spacing should be greater than 160 mils (ground via diameter itself plus 100 mils of additional spacing). The total length of the aperiodic ground via wall structure should be close to 15 inches. The positions of the ground vias generated automatically in the specially written Matlab script according to the abovementioned criteria are shown in Figure 5.12.

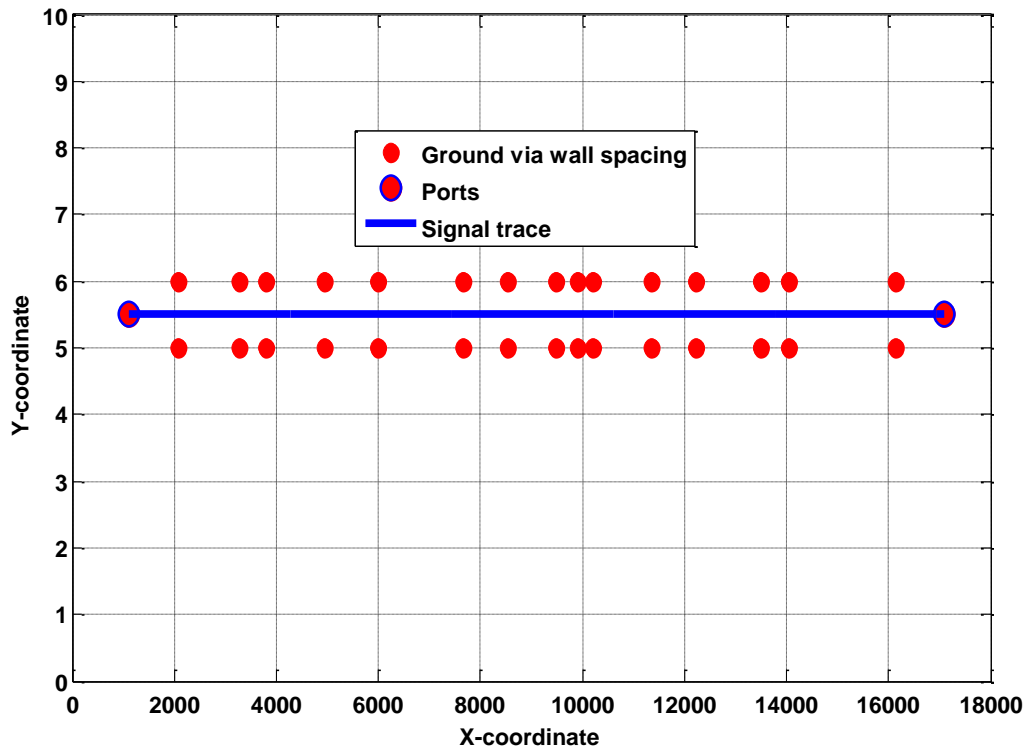


Figure 5.12 Normal distribution of the ground via generated along the test trace



## **5.6. TRL PATTERN**

The new 50 GHz SI test vehicle will keep the original TRL pattern, the same as in the very first 30-GHz test vehicle design, and contains one “reflect” (herein “open”) and five “thru” lines. This TRL pattern does not need any changes, since it was originally designed to cover the entire frequency range from 50 MHz to 50 GHz, even though the operation of the test vehicle was limited by 30 GHz.

## **5.7. NEW 50-GHZ SI TEST VEHICLE DESIGN AND ALLEGRO FILES FOR MANUFACTURING**

Fabrication of the 50-GHz SI Test Vehicle is the crucial and final point of the entire design process. It is very important to create detailed manufacture files and escort them with exhaustive comprehensive instructions.

Manufacture files implementation is performed in Cadence Allegro PCB Editor. A schematic net-list was created in OrCAD-Capture software. The schematic is very simple. It is just the set of two by two connected footprint symbols for single-ended and differential lines, as is shown in Figure 5.13. The PCB drawing, as is shown in Figure 5.14, contains footprints for single-ended and differential lines, net connections, screw holes, ground via walls and mechanic holes.

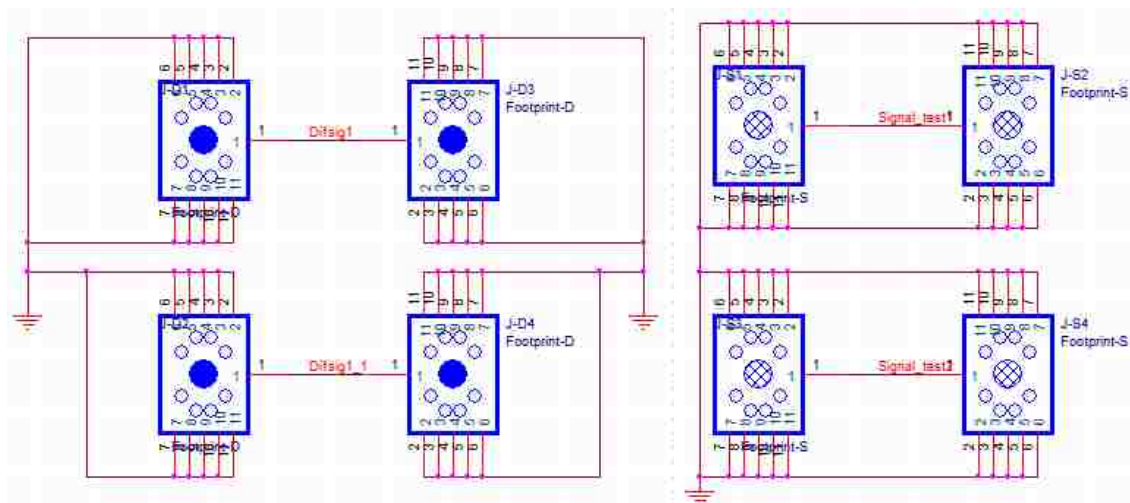


Figure 5.13 A segment of the schematic file for new 50-GHz SI Test Vehicle

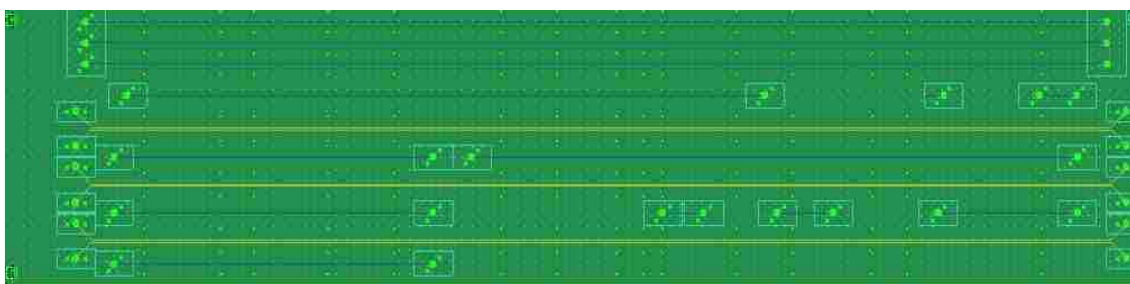


Figure 5.14 PCB drawing for new 50-GHz SI Test Vehicle

In addition to the main 16,025-mil long test lines and TRL calibration lines, the PCB also contains one 10-inch long line and three dummy test lines each five inches long. The dummy lines can be used for cross-sectional analysis after comprehensive testing of electromagnetic characteristics, while the main 16- and 10- inch lines remain intact. Removable 2.4-mm SMA female connectors should be attached to the bottom side for the single-ended lines, and to the top for the differential lines. Figure 5.15 shows the designed stackup with connectors for differential and single-ended lines.

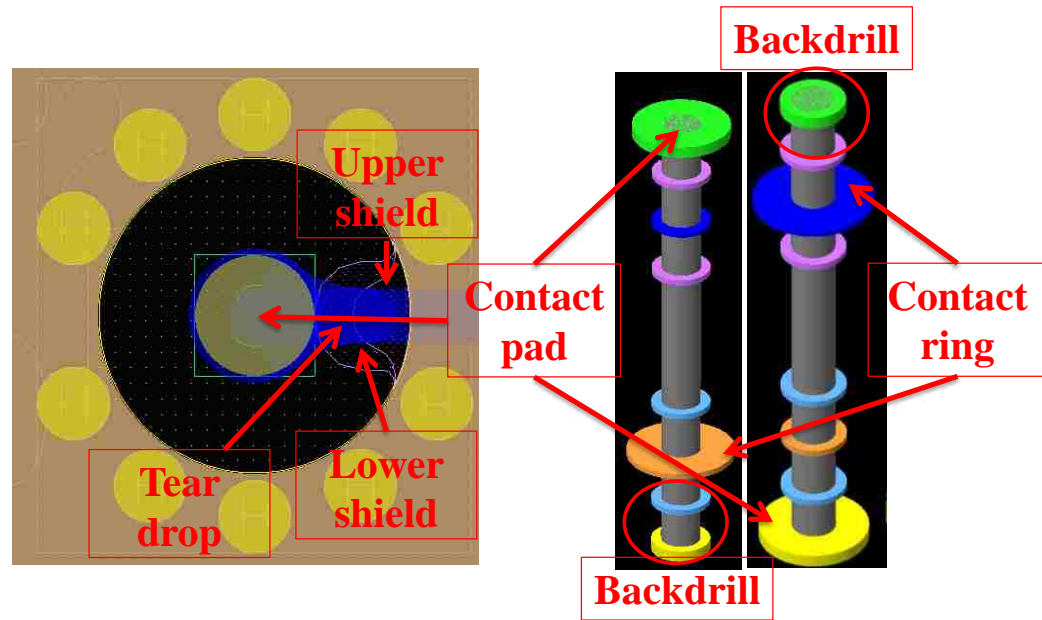


Figure 5.15 Connectors insertion in the new 50-GHz SI Test Vehicle

Differential and single ended lines are located on different signal layers. A side opposite to the corresponding connector should be back drilled. For this reason, two different signal via padstacks for a footprint are needed. The footprint and two types of padstacks, one for a differential line (on the left), and the other for a single-ended line (on the right), are shown in Figure 5.15. The upper and lower shields are created as the static solid copper shapes. Tear drops were added as a fillets. The gray cylinder in the padstack as is shown in Figure 5.15 has the diameter of 8 mils, which is the finished via diameter after plating. The small colored cylinders are the walls of the drill hole on the layers of padstack. Figure 5.16 shows implementation of footprint and padstacks in Allegro PCB editor.



Figure 5.16 Implementation of footprint and padstacks in Allegro PCB Editor

From the manufacturer's point of view, the new 50-GHz SI Test Vehicle is just an 8-layer board with signal layers L3 and L6 and duplicate ground planes on the layers L1 and L2, L4 and L5, and L7 and L8. All the signal and ground layers are made of 1-oz base copper. The TRL calibration traces are placed on the signal layer L3. In addition to the PCB drawing itself, the manufacture design file contains the stackup manufacture drawing, as is shown in Figure 5.17, and target impedance table presented in Table 5.1.

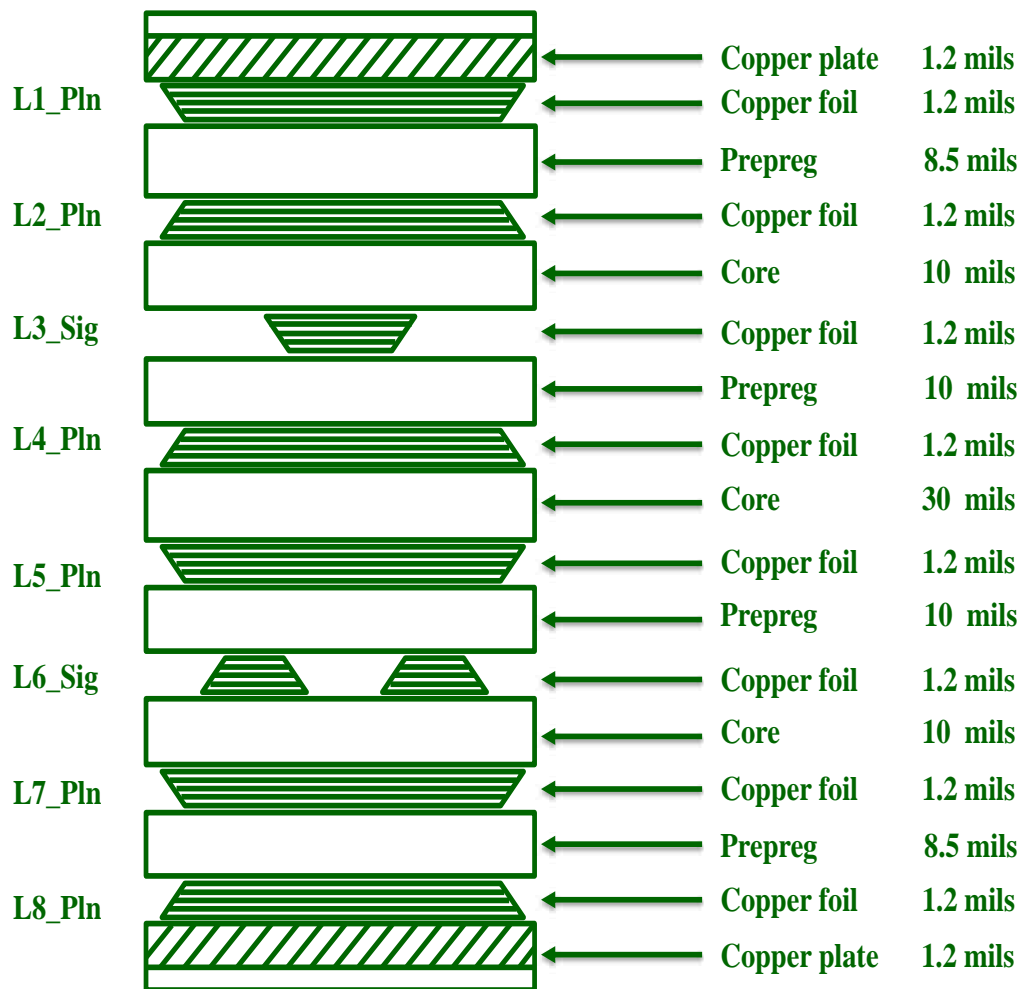


Figure 5.17 Stackup manufacture drawing for the new 50-GHz SI Test Vehicle

According to the data from Target Impedance Table, a manufacturer should adjust line widths of single-ended test traces for 48, 50, and 52 Ohms, respectively. Line widths of differential traces should be adjusted to get 96, 100, or 104 Ohms, respectively. The line width of the seven calibration traces on Layer 3 is chosen to match that of the 50-Ohm trace.

**Table 5.1 Target Impedance Table**

	TRACE	TRACE	TRACE	TRACE/PITCH	TRACE/PITCH	TRACE/PITCH
				/TRACE	/TRACE	/TRACE
	9.8 MIL	9.0 MIL	8.2 MIL	8.8/15/8.8	8.1/15/8.1	7.4/15/7.4
<b>TOP</b>	<b>PLANE + BACKDRILL</b>	<b>PLANE + BACKDRILL</b>	<b>PLANE + BACKDRILL</b>	<b>PLANE + CONNECTORS FOR DIFFERENTIAL LINE THIS SIDE</b>		
<b>GND2</b>	<b>PLANE+SPECIAL SHAPES/SHIELDS</b>			<b>PLANE</b>	<b>PLANE</b>	<b>PLANE</b>
<b>SIG2</b>	<b>48 OHM±10%</b>	<b>50OHM±10%</b>	<b>52 OHM±10%</b>	<b>N/A</b>	<b>N/A</b>	<b>N/A</b>
<b>GND3</b>	<b>PLANE+SPECIAL SHAPES/SHIELDS</b>			<b>PLANE</b>	<b>PLANE</b>	<b>PLANE</b>
<b>GND4</b>	<b>PLANE</b>	<b>PLANE</b>	<b>PLANE</b>	<b>PLANE+SPECIAL SHAPES/SHIELDS</b>		
<b>SIG5</b>	<b>N/A</b>	<b>N/A</b>	<b>N/A</b>	<b>96 OHM±10%</b>	<b>100 OHM±10%</b>	<b>104 OHM±10%</b>
<b>GND5</b>	<b>PLANE</b>	<b>PLANE</b>	<b>PLANE</b>	<b>PLANE+SPECIAL SHAPES/SHIELDS</b>		
<b>BOT</b>	<b>PLANE + CONNECTORS FOR SINGLE-ENDED LINE THIS SIDE</b>			<b>PLANE + BACKDRILL</b>	<b>PLANE + BACKDRILL</b>	<b>PLANE + BACKDRILL</b>

## 5.8. NEW FABRICATED 50-GHZ SI TEST VEHICLE

A new fabricated PCB SI test vehicle with mounted removable connectors is shown in Figure 5.18. The design of this test vehicle is described above. The measured S-parameters of this test vehicle are shown in Figure 5.19. It is seen that the ground via structure is aperiodic. The laminate fiber-glass filled dielectric of this PCB is the same as that of Sets I and II described in Section 4. The length of the main test line (between calibration planes) is also the same, 15,410 mils (39.14 cm).

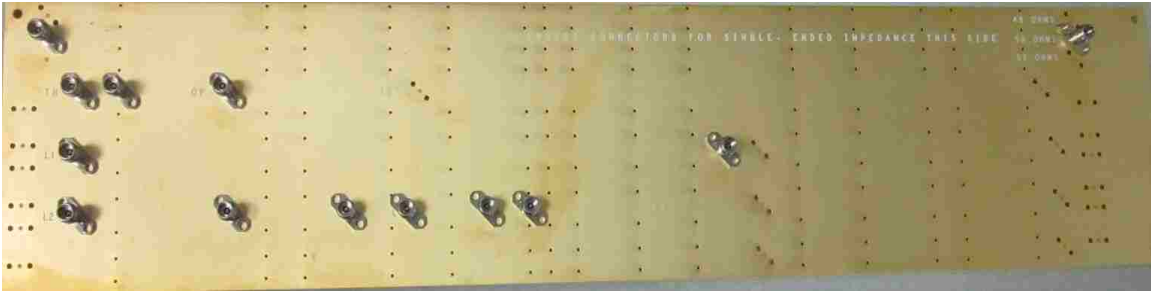


Figure 5.18 New fabricated 50-GHz PCB SI test vehicle with removable connectors

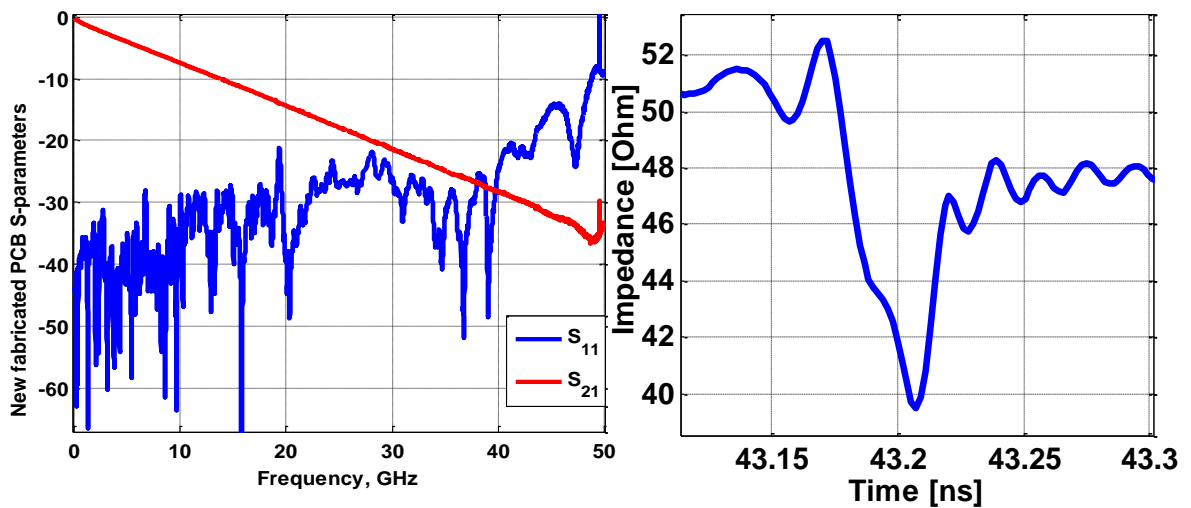


Figure 5.19 Measured S-parameters and TDR response of the new fabricated 50-GHz PCB SI test vehicle

As is seen from Figure 5.19, the reflection loss (blue curve) is below 20 dB over up to 44 GHz. The insertion loss is mainly linear till the same frequency of 44 GHz, and then some nonmonotone behavior is noticeable, which may lead to inaccurate extraction of DK and DF on the board due to curve-fitting to  $\sqrt{\omega}, \omega, \omega^2$ . Therefore, the frequency range of measurements is proposed to be cut at 44 GHz, and the extraction results would

be extrapolated to the higher frequencies based on the monotone behavior of DK and DF with frequency.

The DK and DF of the dielectric on the PCB extracted using the “root-omega” procedure (with the  $\sqrt{\omega}$  parts removed from both  $\beta$  and  $\alpha$ ) are shown in Figure 5.20. As is seen from this figure, the DK value slowly decreases, while DF linearly increases with frequency. The extracted data agrees well with the extracted DK and DF for Sets I and II as in Figure 4.4. Slight difference is explained by application of DERM2 procedure for Sets I and II, which removes conductor surface roughness effects, while herein the dielectric properties are not refined from roughness. However, the foil used to design this 50-GHz test vehicle is the smoothest HVLP, so indeed roughness effects are present, but minor.

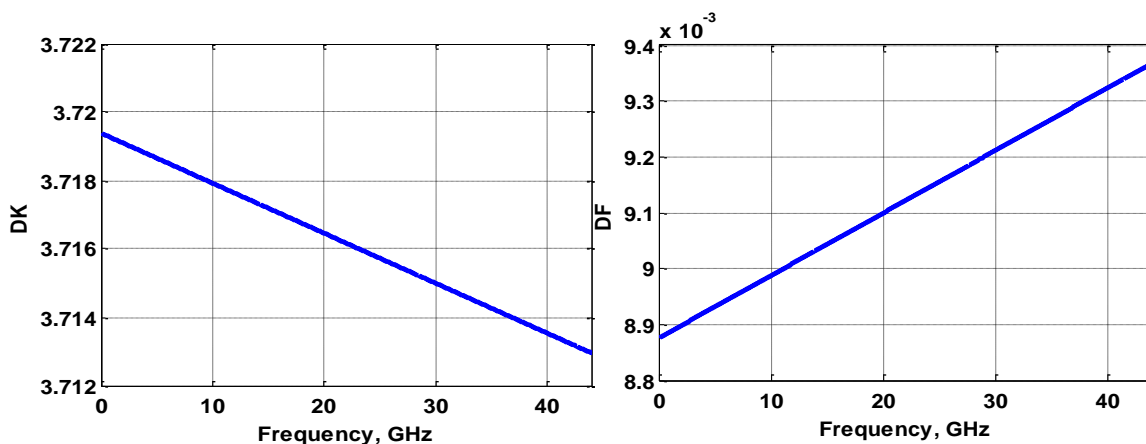


Figure 5.20 Extracted DK and DF

Systematic errors for this new 50-GHz test board have also been evaluated over the entire frequency range of measurements of S-parameters from 10 MHz to 50 GHz.



These errors are shown in Figure 5.21. The evaluation was done using the formulas described in Section 2. The systematic errors are comparatively high at the lower frequency end, since both  $\delta(\text{DK})$  and  $\delta(\text{DF})$  are inverse proportional to frequency, as is seen from formulas (2.7) and (2.8). However, at  $f=100$  MHz, the systematic error for DF does not exceed 15%, while for DK it is less than about 0.7%. As frequency increases, systematic errors for both DK and DF decrease, however, at  $f>49$  GHz there is a significant error in DF again.

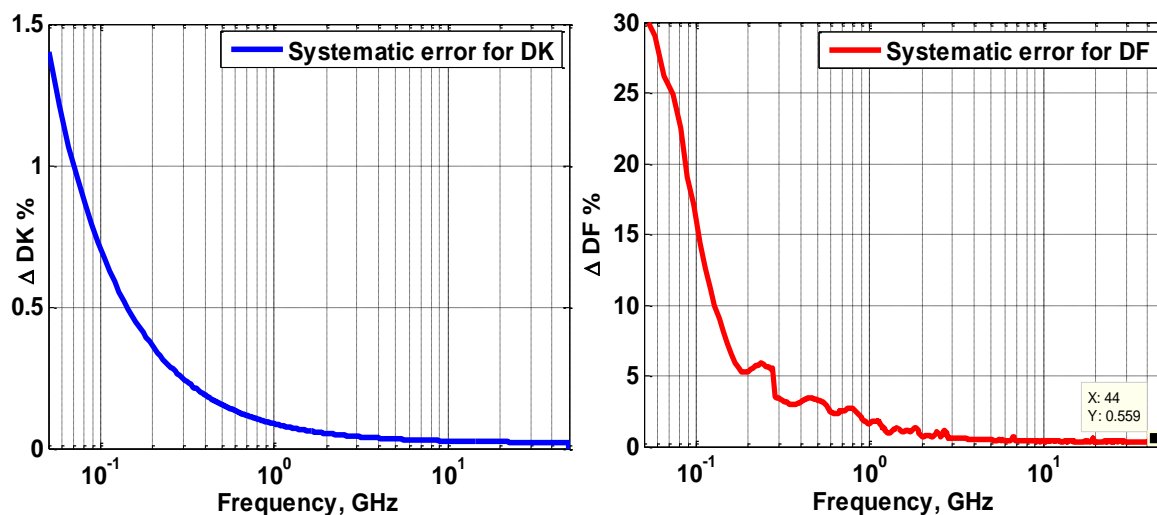


Figure 5.21 Evaluated systematic errors for DK and DF extracted on the 50-GHz test board

## 6. CONCLUSION AND FUTURE SCOPE

During the past few years (since 2009), the “in situ” wideband traveling-wave technique called S3 based on measuring S-parameters of the PCB test vehicles with ‘through-reflect-line’ (TRL) calibration pattern, has been developed and used for characterization of dielectric and copper foil properties of PCBs up to 30 GHz. In this work, a modified test vehicle (primarily, connector-via-trace design) to extend the frequency range for PCB material characterization up to 45-50 GHz has been proposed, designed, fabricated, and tested. The measured S-parameters and extracted DK and DF data using this test vehicle meet all the expectations.

An extension of frequency range up to 50 GHz leads to the increased requirements to the accuracy, sensitivity, and stability of measurements. The major error and sensitivity analysis is carried out in this work. Two groups of errors have been considered: manufacturing variability and systematic (reproducibility) errors. Formulas to quantify these types of errors have been derived in this work, and some examples of quantification are provided.

Frequency range extension up to 50 GHz requires paying special attention to a problem of the conductor surface roughness, since the latter increasingly contributes to the total loss on the line as frequency increases. To correctly refine dielectric parameters (DK and DF) from conductor roughness, one must correctly quantify conductor roughness. A new algorithm for semi-automatic characterization of copper foil profiles on optical or scanning electron microscopy (SEM) pictures of signal traces is proposed in this work. The algorithm to process microsection SEM or optical images has been significantly modified compared to the previous one of 2012. A number of new functions

in image processing and computer vision parts of the algorithm have been added. These new functions lead to the better reproducing of foil roughness profiles and higher accuracy of roughness characterization. A comprehensive roughness parameter QR to characterize foil roughness on a PCB signal trace has been introduced. This parameter includes amplitudes of roughness profiles on both “foil” and “oxide” sides of the trace, as well as quasi-periods of roughness profiles on each side. In addition, a shape roughness factor (SRF), analogous to the duty cycle for a time-domain signal sequence, has been introduced. In future, it can be included in the QR parameter for more accurate description of foil profiles.

Using the new proposed roughness characterization tool, statistical data of various cross-sectional slugs of PCB striplines have been tested. The collected statistics of numerous copper foil roughness values allows for refining the measured DK and DF parameters from roughness contributions and for developing “design curves”. The latter could be used by SI engineers and electronics developers in their designs. It was found that the slope of insertion loss as a function of frequency on a test vehicle is the sum of the slope due to the refined dielectric loss, loss in the smooth conductor, and an additional loss due to foil roughness.

A concept of an effective roughness dielectric (ERD) layer was applied in this work to describe an interface between a rough foil and ambient dielectric. The parameters of the ERD have been correlated with the roughness parameters, extracted from SEM or optical pictures of stripline cross-sections. The proposed “design curves” tie together effective dielectric parameters of an ERD with the corresponding geometrical roughness parameters extracted from cross-section or predicted from knowing a type of a foil used

on the line. Then a designer can employ full information on the PCB material. This would include (1) the known dielectric data, either given or refined from roughness in the material parameter extraction procedure; (2) loss on the smooth conductor of the given geometry; and (3) a thickness and effective dielectric parameters of ERD.

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