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MODELING OF VIAS AND VIA ARRAYS IN HIGH SPEED PRINTED CIRCUIT BOARDS

by

ARUN REDDY CHADA

A THESIS

Presented to the Faculty of the Graduate School of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

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Approved by

Dr. Jun Fan, Advisor Dr. James L. Drewniak Dr. Yaojiang Zhang

ABSTRACT

This thesis presents modeling approaches for fast calculation of signals in dense via arrays in high speed printed circuit boards (PCBs) and model to hardware correlation study of solid and perforated disk resonators. A 2D finite difference (FD) method to extract the via capacitance which includes the via pad capacitance obtained by solving the laplace equation in the via domain in multi-layer geometries is presented and validated with analytical formulation for via capacitance. Next, closed-form expression for the impedance of an infinitely large parallel plane pair is derived and validated by comparing with cavity model for several numerical examples. The infinitely large parallel plane pair model is applicable to practical printed circuit board (PCB) design problems where there are multiple shorting vias around the signal vias of interest. With the presence of multiple shorting vias, reflections from the plane pair edges can be neglected since the shorting vias prevent the electromagnetic energy from leaking away from the local cavity around the signal vias.

Next, improved multiple scattering method for fast calculation of signals in via arrays in plane pair is derived using analytical expressions. Parallel plate modes expressed as cylindrical waves are excited by the magnetic frill currents in via holes (antipads). Multiple scattering of these modes among vias as well as from the edge boundaries of the plate pair are rigorously considered with the addition theorem of the cylindrical waves.

In the final part of this thesis, different approaches mentioned here are applied to study solid and perforated disk resonator behaviors and to correlate the simulated and measured results.

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1. INTRODUCTION

Vias are widely used in multi-layer printed circuit boards (PCBs) and packages to connect traces or planes in different layers [1]. Although providing additional routing spaces for signal link path, vias cause serious concerns on signal integrity (SI), power integrity (PI) as well as electromagnetic interference (EMI). A via is an inevitable discontinuity causing mismatch in a signal trace. Furthermore, a high-speed vertical current flowing on a via excites propagating parallel plane modes of a power/ground pair. As a result, strong cross-talk or voltage fluctuation may occur in adjacent signal vias or power distribution network (PDN). In addition, the propagating modes may excite the resonant modes of the power/ground plane pair and cause strong radiation from the edges. Therefore, simulation and modeling of vias in a plane pair are crucial for practical designs of high-speed PCBs or packages.

In order to estimate the signal integrity (SI), power integrity (PI), and electromagnetic interference (EMI) effects caused by vias in printed circuit boards, there is a need for modeling tools which can handle via arrays in multi-layer printed circuit boards. At present, there are two kinds of approaches in dealing with via arrays in a plane pair. As vias are electrically small, a physics based circuit model was proposed to describe the via-plane interactions [2] - [3]. In this model, the via barrel is modeled as a short circuit and two via-plane capacitances are used for the displacement currents from the via to the top and bottom planes. The via plane capacitance values can be calculated using the analytical formulation in [3]. The impedance of the plane pair, namely Z_{pp} , is used to describe the return path of the via current. The physics based circuit model is flexible and suitable for any irregular plane pair because the Z_{pp} can be calculated easily

using cavity method or boundary element method (BEM). The power plane impedance Z_{pp} can also be computed using the infinite plane assumption when the planes are large or when a lot of ground vias form a local cavity around the signal vias. However, the via itself is not accurately modeled since the boundary condition on the via barrels is not rigorously enforced.

On the other hand, a different approach, called multiple scattering method, adopts magnetic frill currents as sources, and Green's function for an infinite, or a finite circular plane pair is used to calculate the fields in the plane pair [4] - [5]. The multiple scattering effects among vias are considered using the addition theorem of cylindrical waves. The method satisfies the boundary conditions on a via structure rigorously but a drawback is that the Green's function for an irregular plane pair is not available. This restricts the method for further applications in practical designs.

Full wave modeling tools, such as HFSS, CST Microwave Studio etc, can be used to simulate via arrays in typical PCB boards. The main advantage of full wave modeling tools is the high accuracy of the results. The two main disadvantages of full wave modeling tools are time consumption and dealing only limited model complexity due to available computer resources. Full wave tools can serve as a validation standard for canonical problems.

The remainder of this thesis is organized as follows. Section 2 presents an improved 2D finite difference (FD) method to extract the via barrel and via pad capacitance in a plane pair. Section 3 presents a closed-form expression for the impedance of an infinitely large parallel plane pair and its applications in design problems. Section 4 presents the derivation of improved multiple scattering method for

fast calculation of signals in via arrays in plane pair using analytical expressions. Section 5 presents model to hardware correlation study of solid and perforated disk resonators using physics based circuit model employing BEM, multiple scattering method and effective dielectric medium approach. Section 6 presents the concluding remarks as a part of this study and the future work that will done in due course.

2. THE 2D FINITE DIFFERENCE METHOD TO OBTAIN THE VIA CAPACITANCE

In order to simulate vias in a plane pair, circuit extraction of the plane pair which consists of via capacitances and Z_{pp} block is important. The Z_{pp} block is obtained using various approaches like cavity method, BEM method. The primary concern of this chapter is the extraction of the via barrel and via pad capacitance.

Via capacitance was computed previously using FEM method incorporated in commercial 3D full wave software Ansoft Q3D and finite difference method used in CST EM Studio. A 2D finite difference (FD) method to extract the via barrel and pad capacitances is discussed in Section 2.1. The laplace equation governing the via domain is discretized in to a set of linear simultaneous equations. These sets of linear simultaneous equations are solved iteratively. The advantage of iterative solution is that storing of large matrices is unnecessary. In this section, use of one such iterative procedure is demonstrated. The via capacitances are computed by solving the laplace equation for voltages at various locations in the via domain in every single plane pair of a multi-layer stackup using the 2D finite difference method by satisfying the boundary conditions at the boundaries of the entire domain. Large computation domain is chosen so as to account for all electric field lines from the via barrel and via pad on to the horizontal metal plane. The via capacitances are calculated from charge stored in the via domain obtained from electric field flux density by applying gauss's law. In Section 2.2 the computed via capacitance value is validated by comparing with the via capacitance calculated from analytical formulation developed in [3].

2.1. THE 2D FINITE DIFFERENCE METHOD ALGORITHM

Multi-layer geometries are analyzed on a block by block basis, where each block is a single plane pair as shown in Figure 2.1 where R_v is via radius, R_{ap} is antipad radius, R_p is pad radius, and L is dielectric thickness. A simplified structure for analysis is obtained by cutting along the midpoint between two planes which corresponds to a line where the normal component of electric field is zero. In this section, an improvement to the 2D finite difference method developed in [6] which takes in to account the via pad is derived.



Figure 2.1. Core geometry of a single plane pair which is a part of multi-layered stackup.

The 2D finite difference method is implemented by choosing the domain of interest, which in this case is the half geometry obtained by dividing the geometry of plane pair at its mid-point. The two dimensional domain of interest is then meshed as shown in Figure 2.2. Considering the radial symmetry of the geometry in the Φ direction as shown in Figure 2.3 and Figure 2.4 the laplace equation in polar coordinates ρ and z for the domain of interest can be derived.





Figure 2.2. The geometry of a via crossing a plane pair. (a) The geometry consisting of a single plane pair meshed in to 2D cells of size h by h. (b) The computational domain of the geometry is chosen as subset of the entire domain by using symmetry of the problem.

The laplace equation in the domain of interest in polar coordinates to obtain electric field potential is given by

$$\frac{1}{\rho}\frac{\partial}{\partial\rho}\left(\rho\frac{\partial v}{\partial\rho}\right) + \frac{\partial^2 v}{\partial z^2} = 0 \tag{1}$$



Figure 2.3. Geometry of a single plane pair showing direction of radial symmetry and boundary conditions.

Equation (1) can be further decomposed to

$$\frac{\partial^2 v}{\partial \rho^2} + \frac{\partial^2 v}{\partial z^2} + \frac{1}{\rho} \frac{\partial v}{\partial \rho} = 0$$
⁽²⁾

Equation (2) is discretized in to a set of linear simultaneous equations using the finite difference method. These equations are solved using iterative procedure at each and every grid point in the 2D FD cell. The 2D FD cell employed is h by h where h is the step size.





Figure 2.4. The computational domain of a via crossing a plane pair. (a) The computational domain obtained by drawing a line at the midpoint of the plane pair. (b) The computational domain of the via illustrating the boundary conditions.

Consider three points on the ρ axis separated by a distance h, as shown in Figure 2.5 (a). For convenience, the points have been labeled as (i-1, j), (i, j), and (i+1, j). The value of electric potential v(ρ ,z) at these three points are assigned as v(i-1,j), v(i,j), and v(i+1,j).

			• (i,j-1)
			• (i,j)
(i-1,j)	(i,j)	(i+1,j)	• (i,j+1)
	(a)		(b)

Figure 2.5. The grid lines along horizontal and vertical axes. (a) The grid line along horizontal axis. (b) The grid line along vertical axis.

Using the central difference scheme, the first and second differentials along the ρ direction can be obtained as

$$\frac{\partial^2 v}{\partial \rho^2} \Big|_{i,j} = \frac{v_{i+1,j} - 2v_{i,j} + v_{i-1,j}}{h^2}$$
(3)

$$\frac{\partial v}{\partial \rho}\Big|_{i,j} = \frac{v_{i+1,j} - v_{i-1,j}}{2h} \tag{4}$$

Consider three points on the z axis separated by a distance h, as shown in Figure 2.5 (b). For convenience, the points have been labeled as (i, j-1), (i, j), and (i, j+1). The value of electric potential $v(\rho,z)$ at these three points are assigned as v(i,j-1), v(i,j), and v(i,j+1).

Using the central difference scheme, the first and second differentials along the Z direction are obtained as

$$\frac{\partial^2 v}{\partial z^2}\Big|_{i,j} = \frac{v_{i,j+1} - 2v_{i,j} + v_{i,j-1}}{h^2}$$
(5)

$$\frac{\partial v}{\partial z}\Big|_{i,j} = \frac{v_{i,j+1} - v_{i,j-1}}{2h} \tag{6}$$

Figure 2.4 illustrates the boundary conditions that need to be satisfied together with the laplace equation. Boundary 1 is a neumann boundary condition satisfying $\frac{\partial v}{\partial z} = 0$, boundary 2 is a neumann boundary condition satisfying $\frac{\partial v}{\partial \rho} = 0$, and boundary 3

is a neumann boundary condition satisfying $\frac{\partial v}{\partial z} = 0$.

Boundaries 4 & 5 which denote the via barrel and via pad satisfy the dirichlet boundary condition $v = v_0$, and boundary 6 which denotes the top copper plane satisfies the dirichlet boundary condition $v = v_1$. The five point stencil in the mesh is illustrated in Figure 2.6.



Figure 2.6. Five point stencil applied at all interior points in the computational domain.

Discretizing equation (2) using the central difference equations for the derivatives at boundary 1 results in

$$\frac{v_{i+1,j} - 2v_{i,j} + v_{i-1,j}}{h^2} + \frac{v_{i,j+1} - 2v_{i,j} + v_{i,j-1}}{h^2} + \frac{1}{\rho_i} \left(\frac{v_{i+1,j} - v_{i-1,j}}{2h}\right) = 0$$
(7)

Rearranging the terms in the above equation

$$4v_{i,j} = \left(1 + \frac{h}{2\rho_i}\right)v_{i+1,j} + \left(1 - \frac{h}{2\rho_i}\right)v_{i-1,j} + v_{i,j+1} + v_{i,j-1}$$
(8)

$$v_{i,j} = \frac{\left(1 + \frac{h}{2\rho_i}\right)v_{i+1,j} + \left(1 - \frac{h}{2\rho_i}\right)v_{i-1,j} + v_{i,j+1} + v_{i,j-1}}{4}$$
(9)

where ρ_i is the radial distance to grid point (i, j).

All the points on boundary 1 satisfy the neumann boundary condition $\frac{\partial v}{\partial z} = 0$,

which is discretized in equation (10)

$$\frac{\partial v}{\partial z}\Big|_{i,j} = \frac{v_{i,j+1} - v_{i,j-1}}{2h} = 0 , \qquad (10)$$

which implies $v_{i,j+1} = v_{i,j-1}$. Since the point (i, j+1) is a fictitious point and is not located on the grid, the electric potential $v_{i,j+1}$ is replaced with $v_{i,j-1}$ by using the five point stencil shown in Figure 2.6.

Equation (9) can be further simplified using equation (10) to get the governing equation on boundary 1 as

$$v_{i,j} = \frac{\left(1 + \frac{h}{2\rho_i}\right)v_{i+1,j} + \left(1 - \frac{h}{2\rho_i}\right)v_{i-1,j} + 2v_{i,j-1}}{4}$$
(11)

Equation (9) applies at the boundary 2 as well. All the points on boundary 2 satisfy the neumann boundary condition $\frac{\partial v}{\partial \rho} = 0$, which is discretized in equation (12).

$$\frac{\partial v}{\partial \rho}\Big|_{i,j} = \frac{v_{i+1,j} - v_{i-1,j}}{2h} = 0$$
(12)

which implies $v_{i+1,j} = v_{i-1,j}$. Since the point (i+1, j) is a fictitious point and is not located on the grid, the electric potential $v_{i+1,j}$ is replaced with $v_{i-1,j}$ by using the five point stencil shown in Fig 2.6.

Equation (9) can be further simplified using equation (12) to get the governing equation on boundary 2 as

$$v_{i,j} = \frac{2v_{i-1,j} + v_{i,j+1} + v_{i,j-1}}{4}$$
(13)

Equation (9) also applies at the intersection point of boundaries 1 and 2. The intersection point satisfies the neumann boundary conditions $\frac{\partial v}{\partial z} = 0$ and $\frac{\partial v}{\partial \rho} = 0$.

Therefore, the governing equation at the intersection point of boundary 1 and boundary 2 can be obtained as

$$v_{i,j} = \frac{2v_{i-1,j} + 2v_{i,j-1}}{4} \tag{14}$$

Equation (9) is satisfied at boundary 3. All the points on boundary 3 satisfy the neumann boundary condition $\frac{\partial v}{\partial z} = 0$. The governing equation on boundary 3 is same as on boundary 1.

All other the points other than those on the boundaries have equation (9) as the governing equation. The voltage potential $v_0 = 1$ V on the boundaries 4 and 5 and voltage potential $v_1 = 0$ V on boundary 6 are set to satisfy the corresponding boundary conditions.

All the governing equations are solved iteratively in the entire domain for N runs where value of N is chosen such that the error between the previous and present voltage values on the grid is less than 1e-12.

After getting the electric field potentials at all the grid points, the electric field E from the via barrel and via pad to the horizontal copper plane set at the reference voltage of 0V is computed by

$$E = -\nabla V \tag{15}$$

Once the electric field is obtained the computation of the electric displacement field D in the computational region is done using the relation

$$D = \varepsilon E \tag{16}$$

where ε is the permittivity of the material in the region

The electric displacement field accounts for the bound charges within the material. Applying gauss's law in the computation domain of interest, charge stored in the region Q is computed.

The capacitance C between the via to the horizontal metal plane is given by

$$C = \frac{Q}{V} \tag{17}$$

where V is the potential difference between the via structure and the horizontal metal plane which is 1V.

The capacitance computed C is equal to $(C_b + C_p)$ where C_b is the via barrel capacitance, and C_p is the via pad capacitance.

A large computational domain is chosen to account for all the electric field lines from the via barrel and pad on to the horizontal metal plane to obtain an accurate capacitance value. Value R_{ext} is chosen so as to include all the electric field lines emerging from the via barrel and via pad to the top metal plane. Value h is chosen so as to generate a dense mesh and to minimize the error inherent in the 2D finite difference method. Moreover, the derivatives are approximated using the central difference scheme which is the best approximation since the truncation error is proportional to the square of the grid size h. The flowchart of the 2D finite difference method to compute the via barrel and via pad capacitance is shown in Figure 2.7.



Figure 2.7. Flow chart of the 2D finite difference method.

2.2. RESULTS AND DISCUSSIONS

The capacitance obtained from the proposed finite difference method and analytical formulations are compared to validate the finite difference method. The capacitance is computed for different via drill sizes and via pad sizes using the finite difference method and compared with analytical formulation as listed in Table 2.1 and Table 2.2. The value R_{ext} which is computational domain radius along the ρ direction is chosen as 50 mils. This value shall be large enough in order to capture all the electric field lines going from via barrel including its pad and terminating on the horizontal metal surface. The larger this value is, the larger the computational domain, and more accurate the solution. The 2D FD cell employed for the simulation is set at 0.05 by 0.05 mils which creates a dense mesh in the computational domain. The maximum percentage error between the capacitance values obtained from the finite difference method and the analytical formulation is 4 % which is acceptable in practical situations observed in Figures 2.8 and 2.9.

Via radius (mils)	Via pad radius (mils)	Via antipad Radius (mils)	R _{ext} (mils)	Dielectric thickness (mils)	Cvia (fF)	Cvia analytical (fF)
4	4	17	50	9	16.9	16.7
6	6	17	50	9	23.3	23.1
8	8	17	50	9	31.8	31.5
10	10	17	50	9	43.9	43.3

Table 2.1. Summary of the capacitance values obtained from the 2D finite difference method and the analytical formulation for various via drill radius values while fixing all other parameters.

Dielectric Viapad Anti Cvia Cpad Ctotal Cvia Rext Radius Analytical Pad (mils) thickness (\mathbf{fF}) (\mathbf{fF}) (fF)(mils) Radius (mils) (\mathbf{fF}) (mils) 9 4 50 16.9 0 16.9 17 16.7 17 9 14.9 4.2 50 0.4 15.3 15.2 17 50 9 0.8 14.4 4.4 13.6 14.3 17 9 4.6 50 12.6 1.2 13.8 13.6 12.3 17 9 8.0 4.3 6 50 12.1 7 7 17 9 50 6.1 13.1 12.7 9 17 9 50 3.6 13.2 16.8 16.4 10 17 50 9 2.8 16.9 19.7 19.3 11 17 9 50 2.2 21.3 23.5 22.9

Table 2.2. Summary of the capacitance values obtained from the 2D finite difference method and the analytical formulation for various pad radius values while fixing all other parameters.

 R_v denotes via radius that is fixed at 4 mils, R_p denotes via pad radius, and R_{ap} denotes via antipad radius. Number of runs employed in the 2D FD method is 50,000 and the step size of the mesh used is 0.05 mils.



Figure 2.8. The via capacitance curves obtained from the values listed in Table 2.1 for various via drill sizes while fixing all other parameters.



Figure 2.9. The via capacitance curves obtained from the values listed in Table 2.2 for various via pad sizes while fixing all other parameters.

From the values listed in Table 2.3 and Table 2.4, clearly the time taken by the finite difference method to get capacitance for any single geometry structure listed in Table 2.1 is large compared to the time taken by the analytical formulation. The simulation time difference is understandable as the time taken by the finite difference

method depends on the mesh density. However, the FD method is more flexible to deal with arbitrary geometries than the analytical formulation. The electric field potential values on the grid are computed for 50,000 runs, or when the past electric potential values and the current electric potential values have a relative error less than 1e-12. The simulation time can be improved by using an adaptive technique for computing the electric potential values on the grid for every run by setting an optimal learning rate. The convergence will be faster for adaptive technique compared to the non-adaptive technique used in this chapter. The technique presented in this chapter is an improvement over the method developed in [6] where via pad was not handled.

Table 2.3. Summary of the simulation times taken for getting the capacitance values of every geometry mentioned in Table 2.1.

Computational Method	Simulation time
Finite difference method	13 mins
Analytical formulation	0.5 secs

Table 2.4. Summary of the simulation times taken for getting the capacitance values of every geometry mentioned in Table 2.2.

Computational Method	Simulation time
Finite difference method	13 mins
Analytical formulation	0.5 secs

3. IMPEDANCE OF AN INFINITELY LARGE PARALLEL PLANE PAIR AND ITS APPLICATIONS IN ENGINEERING MODELING

Power and ground planes are extensively used in modern high-speed printed circuit board (PCB) designs. These planes are good transmission-line structures, and can support the propagation of the simultaneous switching noise (SSN) generated between the power and ground planes due to active device switching. The magnitude of the switching noise is proportional to the power/ground plane pair impedance, $Z_{\text{pp}},$ given in [2] and [7]. A lower impedance magnitude means a weaker voltage fluctuation in the power distribution network (PDN), and a better performance in terms of power integrity (PI). Recent investigations also reveal that parallel plane pair serves as a part of the return path for signal vias [2]. A lower Z_{pp} magnitude leads to a better transmission property in terms of signal integrity. Therefore, the impedance of parallel plane pair is an important property in high-speed circuit analysis. Parallel plane pair exhibits distributed resonances that are associated with its physical dimensions at high frequencies. These resonances could not only cause electromagnetic interference (EMI), but also affect ground bounce due to switching noise. Parallel plane resonances can be characterized by the Z_{pp} impedance matrix which is obtained using various approaches, including both analytical and numerical methods such as the cavity model [7]-[9], finite element method (FEM) [10], method of moments (MoM) [11], and finite difference method [12]- [13].

Placing shorting vias around signal vias provides some sort of shielding from other signal vias and significantly reduces the reflections of the electromagnetic waves generated by the signal vias from the edges of the parallel plane pair. Performance in terms of insertion loss, crosstalk, and electromagnetic interference (EMI) can be greatly improved. The transverse electromagnetic (TEM) wave travelling through the via antipad region (a very short coaxial structure [3]) excites the parallel plane modes in the cavity formed by the parallel planes. These parallel plane modes get reflected back and forth from the edges of the planes. When there are enough shorting vias closely surrounding the signal vias under the study, most of the electromagnetic waves excited between the planes due to the signal vias cannot reach the edges of the planes anymore, and are then confined in the local cavity formed by the shorting vias. In other words, the distributed plane pair resonances associated with the plane dimensions become negligible; thus the impedance of the parallel plane pair can be estimated using that of an infinitely large parallel plane pair at the frequencies of interest. The conventional cavity model to calculate the impedance of a rectangular parallel plane pair is briefly overviewed in Section 3.1. Then, the method to obtain the impedance of an infinitely large parallel plane pair is presented in Section 3.2, followed by some simulation examples that validate the effectiveness of the infinite plane pair approximation in Section 3.3.

3.1. CAVITY MODEL

The Z_{pp} plays an important role in the physics based circuit model for multi-layer printed circuit board (PCB) structures. To perform various signal and power integrity analyses containing parallel planes, the Z_{pp} needs to be calculated efficiently and accurately. In the cavity model, the Z_{pp} is computed based on the ratio of the induced voltage between the planes at the observation port to the impressed current at the source port when all other ports are left open. The cavity model approach in [2], and [7]-[9] has also been extended to handle irregularly shaped plane pair using the segmentation technique [14].

In the cavity model the transfer impedance is defined by the integration of the Green's function in a parallel plane cavity as

$$Z_{ij} = \frac{h}{S_i S_j} \iint_{S_i} \iint_{S_j} G(x, y; x', y') dx dy dx' dy'$$
(18)

where h is the separation between the two parallel planes; S_i and S_j are the area of the ports *i* and *j*, respectively; and G(x, y; x', y') is the electric field Green's function due to impressed electric current density inside a parallel-plane cavity, which is formed by two parallel planes and four perfect magnetic conductor (PMC) sidewalls. The observation and source points are located at $(x, y) \in S_i$ and $(x', y') \in S_j$ respectively, in equation (18).

The closed-form expression for the impedance matrix Z_{pp} of a rectangular plane pair with PMC boundaries as illustrated in Figure 3.1 is given as

$$Z_{ij} = \frac{j\omega\mu h}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{C_m^2 C_n^2 g f}{k_{xm}^2 + k_{yn}^2 - k^2}$$
(19)

where *a* and *b* are the dimensions of the rectangular plane pair; C_m and $C_n = 1$ for *m*, n = 0 and $\sqrt{2}$ otherwise;

$$\begin{split} k_{xm} &= \frac{m\pi}{a} \ , \ k_{ym} = \frac{n\pi}{b} \ ; \\ f &= \left(\frac{\sin\left(\frac{k_{xm}L_{xi}}{2}\right)}{\frac{k_{xm}L_{xi}}{2}}\right) \left(\frac{\sin\left(\frac{k_{xm}L_{xj}}{2}\right)}{\frac{k_{xm}L_{xj}}{2}}\right) \left(\frac{\sin\left(\frac{k_{ym}L_{yi}}{2}\right)}{\frac{k_{ym}L_{yi}}{2}}\right) \left(\frac{\sin\left(\frac{k_{ym}L_{yj}}{2}\right)}{\frac{k_{ym}L_{yj}}{2}}\right) (\frac{\sin\left(\frac{k_{ym}L_{yj}}{2}\right)}{\frac{k_{ym}L_{yj}}{2}}); \end{split}$$

$$g = \cos(k_{xm}x_i)\cos(k_{yn}y_i)\cos(k_{xm}x_j)\cos(k_{yn}y_j);$$

and k is the wavenumber in the dielectric medium between the two parallel planes.



Figure 3.1. Illustration of the parallel plane pair with PMC boundaries at its four sidewalls.

3.2. INFINITE PLANE ZPP MODEL

The definition of Z_{pp} of a plane pair using cylindrical wave's expansion applicable to multiple ports in an irregular plane pair is obtained by expanding electric and magnetic fields in terms of cylindrical waves near a plane port. Figure 3.2 shows the illustration of the observation and source ports i and j located in a parallel plane pair.

The analytical formula for computing the transfer impedance of a linear network is given by

$$Z_{ji} = \frac{V_j}{I_i} |_{I_k = 0, k \neq i}$$
(20)

where port *i* & *j* are the source and observation ports, respectively.



Figure 3.2. Illustration of the observation and source ports *i* and *j* located in a parallel plane pair.

When the spacing between the plane pair h is less than a half wavelength at the highest frequency of study, the only modes supported by the structure are the radial transmission-line modes with no variation in the z and ϕ directions.

Since E_z has no variation in z direction and H_{ϕ} has no variation in ϕ direction, it is possible to uniquely define the z direction voltage and the radial current as

$$V_j = -E_{zj}h, \qquad I_i = 2\pi r_i H_{\phi i}$$
⁽²¹⁾

Due to the completeness of cylindrical harmonics, the electric field distribution and the magnetic field distribution near source port i as illustrated in Figure 3.2 can be expressed as

$$E_{z}\left(\vec{r}^{i}\right) = \sum_{m=-\infty}^{\infty} \left[a_{i}^{(m)}H_{m}^{2}\left(kr^{i}\right) + b_{i}^{(m)}J_{m}\left(kr^{i}\right)\right]e^{jm\phi}$$
(22)

$$H_{\phi}\left(\vec{r}^{i}\right) = \frac{k}{j\omega\mu} \sum_{m=-\infty}^{\infty} \left[a_{i}^{(m)} \frac{\partial}{\partial r} H_{m}^{2}\left(kr^{i}\right) + b_{i}^{(m)} \frac{\partial}{\partial r} J_{m}\left(kr^{i}\right) \right] e^{jm\phi}$$
(23)
where $\vec{r}^i = r^i \angle \phi^i$ as illustrated in Figure 3.2, $H_m^{(2)}$ is Hankel function of the second kind, J_m is the bessel function, a_i and b_i are outward and inward wave expansion coefficients.

As mentioned earlier, when ports are small enough, which is usually true at the frequencies of interest, the ϕ directional variation in the electric and magnetic fields can be neglected. Therefore, considering only the m=0 mode, equations (22) and (23) can be simplified to

$$E_{z}(r^{i}) = \left[a_{i}^{(0)}H_{0}^{2}(kr^{i}) + b_{i}^{(0)}J_{0}(kr^{i})\right]$$
(24)

$$H_{\phi}\left(r^{i}\right) = \frac{k}{j\omega\mu} \left[a_{i}^{(0)}\frac{\partial}{\partial r}H_{0}^{2}\left(kr^{i}\right) + b_{i}^{(0)}\frac{\partial}{\partial r}J_{0}\left(kr^{i}\right)\right]$$
(25)

For an infinitely large plane pair, there are no reflected waves from the boundary of the plane pair. As a result, equations (24) and (25) are further simplified to

$$E_{z}\left(r^{i}\right) = \left[a_{i}^{\left(0\right)}H_{0}^{2}\left(kr^{i}\right)\right]$$
(26)

$$H_{\phi}\left(r^{i}\right) = \frac{k}{j\omega\mu} \left[a_{i}^{(0)}\frac{\partial}{\partial r}H_{0}^{2}\left(kr^{i}\right)\right]$$
(27)

Substituting (26) and (27) into (21), the voltage and current at Port i are derived as

$$V_i = -\left[a_i^{(0)}H_0^2\left(kr^i\right)\right]h\tag{28}$$

$$I_{i} = \frac{2\pi r^{i}k}{j\omega\mu} \left[a_{i}^{(0)} \frac{\partial}{\partial r} H_{0}^{2} \left(kr^{i} \right) \right]$$
(29)

In other words, the self (input) impedance at Port i is

$$Z_{ii} = \frac{V_i}{I_i} = \frac{j\omega\mu h}{2\pi k r^i} \cdot \frac{H_0^2\left(kr^i\right)}{H_1^2\left(kr^i\right)}$$
(30)

where $H_{0(1)}^2$ is the zero (first) order Hankel function of the second kind.

At an observation port j that is away from the source port (i.e $i \neq j$), the electric field at the center of Port *j* due to the excitation at the source port *i* is given as

$$E_{z}\left(r^{j}\right) = \left[a_{i}^{(0)}H_{0}^{2}\left(kr_{ji}\right)\right]$$

$$(31)$$

where $r_{ji} = |\vec{r}_{j0} - \vec{r}_{i0}|$ is the distance between the ports *i* and *j*. Here it is assumed that only Port i is excited and the rest of the ports are all open.

Then the electric field on the circumference of the observation port j can be approximated as

$$E_{z}\left(r^{j}\right) = \left[a_{i}^{(0)}H_{0}^{2}\left(kr_{ji}\right)J_{0}\left(kr^{j}\right)\right]$$

$$(32)$$

where r^{j} is the radius of Port j. The induced voltage at Port j is then obtained as

$$V_{j} = -\left[a_{i}^{(0)}H_{0}^{2}\left(kr_{ji}\right)J_{0}\left(kr^{j}\right)\right]h$$
(33)

Under the condition that only Port i is excited, the transfer impedance between Ports i and j of an infinitely large parallel plane pair can then be simply obtained as

$$Z_{ji} = \frac{V_j}{I_i} = \frac{j\omega\mu h}{2\pi kr^i} \cdot \frac{H_0^2(kr_{ji})J_0(kr^j)}{H_1^2(kr^i)}$$
(34)

Figure 3.3 shows a finite parallel plane pair with PMC boundaries at the four sidewalls. Shorting vias connecting the two planes as well as signal vias that are isolated from either plane are present in this geometry (only one signal via is illustrated in Figure 3.4). Ports are defined at the locations of these vias. Then port voltages and currents are related by the impedance matrix of the plane pair. This can be written in a submatrix form as



Figure 3.3. A signal via surrounded by four shorting vias in a finite parallel plane pair with PMC boundaries at the sidewalls.

$$\begin{bmatrix} V_s \\ V_g \end{bmatrix} = \begin{bmatrix} Z_{ss} & Z_{sg} \\ Z_{gs} & Z_{gg} \end{bmatrix} \begin{bmatrix} I_s \\ I_g \end{bmatrix}$$
(35)

Where V_s , I_s are the port voltage and current vectors at the locations of the signal vias; V_g , I_g are the port voltage and current vectors at the locations of the shorting vias.

For shorting vias, the port voltages are zero. In other words, V_g is a zero vector. Then, the parallel plane impedance sub-matrix among the signal via ports in the presence of the shorting vias can be obtained as

$$Z_{pp} = Z_{ss} - Z_{sg} Z_{gg}^{-1} Z_{gs}$$
(36)

3.3. NUMERICAL EXAMPLES

When shorting vias are placed around signal vias, whether the parallel plane pair impedance among the signal via ports in a finite plane pair can be approximately with that of an infinitely large plane pair depends on two parameters, the number of shorting vias around the signal vias; and the spacing between the shorting and signal vias.

Let's study an example case where the shorting vias are symmetrically placed around a signal via, forming an approximate square local cavity. As shown in Figure 3.4, the side length of the local cavity equals to 2S where S is the spacing between the signal via and a shorting via.



Figure 3.4. Top view of a finite rectangular plane pair with a local square cavity formed by shorting vias.

Recall that the via port shapes are different in the infinitely large plane pair Z_{pp} definition in equations (30) and (34) and the original cavity model Z_{pp} definition in equation (19). Square ports are used in the original cavity model while circular ports in the infinite plane pair Z_{pp} model. To make meaningful comparisons, the length of the

square ports is chosen such that the circumference of the square port is the same as the circumference of the circular port, whose radius r is usually equal to the via barrel radius.

The signal via is located at (300,600) mils from the lower left corner of the planes in Figure 3.4, with the via barrel radius equal to 12 mils. The dielectric material between the two planes has a tangent loss of 0.02 and a dielectric constant of 3.5. The spacing between the two planes is 11 mils. Simulations were performed in the frequency range from 100 MHz to 40 GHz.

Propagation constant k used in the simulations is given below

$$k = k' - k'' \tag{37}$$

where $k' = \omega * sqrt(\mu * \varepsilon_r * \varepsilon_0)$ and $k'' = 0.5 * k'*(\tan \delta)$; h is the dielectric thickness, μ is the permeability of the material, ε_0 is the permittivity of vacuum, ε_r is dielectric constant of the material, and $\tan \delta$ is the dielectric loss of the material. In the simulations, the conductor loss is ignored.

Figures 3.5-3.7 show the comparisons of the input impedance looking into the signal via with the presence of 8 surrounding shorting vias between using a finite rectangular plane pair model and using an infinite plane pair model. The spacing s between the signal via and a shorting via starts at 50 mils in Figure 3.5, and increases to 100 mils and 150 mils in Figures 3.6 and 3.7, respectively. From these three figures, it is obvious that the smaller the spacing s is, the better the agreement between the infinite and finite plane pair models. Even when s equals to 150 mils, the agreement is fairly decent. The resonances shown in the blue curves in Figures 3.6 and 3.7 are associated with the local square cavity formed by the shorting vias. The red curves in these two figures show some additional small wiggles that are due to the distributed resonances associated with

the finite plane sizes caused by a small portion of the electromagnetic waves escaped from the local cavity.



Figure 3.5. The $|Z_{pp}|$ comparisons between the infinite and finite models when the signal via is surrounded by 8 shorting vias located 50 mils away.



Figure 3.6. The $|Z_{pp}|$ comparisons between the infinite and finite models when the signal via is surrounded by 8 shorting vias located 100 mils away.



Figure 3.7. The $|Z_{pp}|$ comparisons between the infinite and finite models when the signal via is surrounded by 8 shorting vias located 150 mils away.

Figures 3.8 - 3.10 show the comparisons of the input impedance looking into the signal via with shorting vias located 50 mils away between the infinite and finite plane pair models. The numbers of the shorting vias are 3, 6, and 8, respectively. From these three figures, it can be concluded that, the more shorting vias are placed around the signal via, the better the agreement between the infinite and finite plane pair models. This can be clearly explained by the amount of the electromagnetic waves that could escape the local cavity formed by the shorting vias, and propagate back and forth between the plane pair edges, resulting in the resonances associated with the dimensions of the finite plane pair.

Using the infinite plane pair model in signal and power integrity simulations to replace the finite plane pair model is critical in terms of efficiency and speed. In practical PCB designs, there are hundreds or even thousands of vias present (fortunately many of

them are shorting vias), and further, the plane shapes are irregular. Using an infinite plane pair model works for many cases as a fast first-order estimation. The simulation speed of the infinite plane pair model is at least several orders faster than the finite plane pair model, depending on the complexity of the plane pair shapes.



Figure 3.8. The $|Z_{pp}|$ comparisons between the infinite and finite models when the signal via is surrounded by 3 shorting vias located 50 mils away.



Figure 3.9. The $|Z_{pp}|$ comparisons between the infinite and finite models when the signal via is surrounded by 6 shorting vias located 50 mils away.



Figure 3.10. The $|Z_{pp}|$ comparisons between the infinite and finite models when the signal via is surrounded by 8 shorting vias located 50 mils away.

4. MULTIPLE SCATTERING METHOD FOR ANALYZING VIA ARRAYS IN CIRCULAR/IRREGULAR PLANE PAIR AND ITS QUANTIFACTION WITH PHYSICS BASED CIRCUIT MODEL

This section introduces a improved multiple scattering method which uses the parallel plane modes to express the fields excited by the magnetic frill currents in via antipads. The parallel plane modes enables the extension of the multiple scattering method to any irregular plane pair, which overcomes the drawback of the conventional multiple scattering method. The formulation for the improved multiple scattering method has been derived by Dr. Yaojiang Zhang and myself in [15] and implemented in the Matlab environment. In Section 4.7, the improved multiple scattering method is validated for via arrays in circular and irregular multi-layer plane pair geometries using full wave solutions. In addition, the multiple scattering method is compared with physics based circuit model to check the limitations of physics based circuit model to handle dense via arrays in high speed printed circuit boards (PCB). An example via array is illustrated in Figure 4.1.



Figure 4.1. A via array in a circular plane pair with a radius of R.

4.1. COMPLETE PARALLEL PLANE MODES IN CYLINDRICAL COORDINATES

Consider a via array located in a finite circular plane pair as shown in Figure 4.1. Later it will be shown that an infinite plane pair is a special case of a finite one when there are no reflecting waves from the circular boundary. So, a concise multiple scattering method is proposed here to unify the methods proposed in [4] and [5].

In a parallel plane waveguide, the vertical electric field near the *i*th via can be expressed in its local cylindrical coordinates as

$$E_{z}^{i} = \sum_{m=-\infty}^{\infty} \sum_{n=0}^{\infty} \left\{ b_{mn}^{(i)} H_{mn}^{(i)} \left(\rho^{i}, \phi^{i}, z \right) + a_{mn}^{(i)} J_{mn}^{(i)} \left(\rho^{i}, \phi^{i}, z \right) \right\}$$
(38)

where $a_{mn}^{(i)}$ and $b_{mn}^{(i)}$ are the expansion coefficients for the inward and outward cylindrical waves; and the functions $H_{mn}^{(i)}(\rho^i, \phi^i, z)$ and $J_{mn}^{(i)}(\rho^i, \phi^i, z)$ are used to represent the field distribution of the parallel plane TM_{zmn} mode as

$$J_{mn}^{(i)}\left(\rho^{i},\phi^{i},z\right) = J_{m}\left(k_{n}\rho^{i}\right)e^{jm\phi^{i}}\cos\left(\frac{n\pi}{h}z\right)$$
(39)

$$H_{mn}^{(i)}\left(\rho^{i},\phi^{i},z\right) = H_{m}^{2}\left(k_{n}\rho^{i}\right)e^{jm\phi^{i}}\cos\left(\frac{n\pi}{h}z\right)$$

$$\tag{40}$$

where $J_m(.)$, $H_m^2(.)$ are mth order Bessel and second kind Hankel functions, respectively;

and (ρ^i, ϕ^i, z) is the cylindrical co-ordinate of the ith via. $k_n = \sqrt{k_0^2 \varepsilon_r - \left(\frac{n\pi}{h}\right)^2}$ is the

transverse wave number.

Propagation constant k_0 used in the simulations mentioned in equation (37) is

$$k_0 = k' - k'' \tag{41}$$

where $k' = \omega * sqrt(\mu * \varepsilon_r * \varepsilon_0)$ and $k'' = 0.5 * k' * (\tan \delta + \frac{\delta_s}{h})$; h is the dielectric thickness,

 μ is the permeability of the material, ε_0 is the permittivity of vacuum, ε_r is dielectric constant of the material, and $\tan \delta$ is the dielectric loss of the material. δ_s is the skin depth of the metal plates.

4.2. WAVEFORM TRANSFORMATION BETWEEN DIFFERENT VIAS

For a specific via, for example, the *i*th via, the inward and outward waves are related together by the reflection coefficient as

$$b_{mn}^{i} = \Gamma_{mn}^{i} a_{mn}^{i} \tag{42}$$

where

$$\Gamma_{mn}^{i} = -\frac{J_{m}(k_{n}r_{i})}{H_{m}^{2}(k_{n}r_{i})}$$
(43)

where r_i is the barrel radius of the *i*th via. On the other hand, the outward wave of *j*th via is related to the inward wave in *i*th via's coordinates as

$$H_{mn}^{j}(r^{j},z) = \sum_{p=-\infty}^{\infty} S_{jmn}^{ipn} J_{pn}^{(i)}(r^{i},z)$$
(44)

where S_{jmn}^{ipn} stands for the transform coefficient of the outward TM_{zmn} mode of the *j*th via to the inward TM_{zpn} mode of the *i*th via as

$$S_{jmn}^{ipn} = H_{p-m}^{2} \left(k_{n} r_{ji} \right) e^{-(p-m)\phi_{ji}} + \sum_{s=-\infty}^{\infty} \left[J_{s-m} \left(k_{n} r_{j} \right) e^{-j(s-m)\phi_{j}} \right] \cdot \Gamma_{R}^{(s)} \cdot \left[J_{p-s} \left(k_{n} r_{i} \right) e^{-j(p-s)(\phi_{i}+\pi)} \right]$$
(45)

where $r_{ji} = |r_j - r_i|$ and $\phi_{ji} = \arg\{r_j - r_i\}$; and $\Gamma_R^{(s)}$ denotes the reflection coefficient from the circular boundary of the plane pair as

$$\Gamma_{R}^{(s)} = \begin{cases} -\frac{H_{S}^{2}(k_{n}R)}{J_{S}(k_{n}R)} & \rho = R \quad PEC \\ -\frac{H_{S}^{2'}(k_{n}R)}{J_{S}^{'}(k_{n}R)} & \rho = R \quad PMC \\ 0 & \rho = R \quad PML \end{cases}$$
(46)

The first term of the right side of equation (45) represents the direct illumination from the *j*th via to the *i*th via, and the second summation term is the reflection waves from the edge of the circular plane. Obviously, for an infinite plane pair, the perfect matched layer (PML) boundary condition is selected at $\rho = R$ as a special case.

4.3. MULTIPLE SCATTERING EQUATIONS

From the above discussions, the outward mode coefficient vector $b^{(i)}$ of the *i*th via satisfies the following equation

$$b^{(i)} = b_0^{(i)} + \Gamma^{(i)} \left(a_0^{(i)} + \sum_{j=1, j \neq i}^P S^{(i,j)} b^{(j)} \right)$$
(47)

where $b_0^{(i)}$ and $a_0^{(i)}$ are the expansion coefficients of the TM_z modes originated from the magnetic frill currents in the antipads of the *i*th via and their evaluations will be given in the next section; the via reflection matrix $\Gamma^{(i)}$ and the wave transformation matrix $S^{(i,j)}$ are obtained from equations (43) and (45), respectively.

Equation (47) has a clear physical meaning for each via that, the illuminating waves come from two parts: the one that caused by the magnetic frill current $a_0^{(i)}$ and one that from all other vias' outward waves $b^{(j)}$. Assuming there are P vias in the circular plane, then

$$b = b_0 + \Gamma \left(a_0 + Sb \right) \tag{48}$$

where

$$b = \begin{bmatrix} b^{(1)} & b^{(2)} & \cdots & b^{(P)} \end{bmatrix}^T$$
(49)

$$a = \begin{bmatrix} a^{(1)} & a^{(2)} & \cdots & a^{(P)} \end{bmatrix}^T$$
(50)

$$b_0 = \begin{bmatrix} b_0^{(1)} & b_0^{(2)} & \cdots & b_0^{(P)} \end{bmatrix}^T$$
 (51)

$$a_0 = \begin{bmatrix} a_0^{(1)} & a_0^{(2)} & \cdots & a_0^{(P)} \end{bmatrix}^T$$
 (52)

and the wave transform matrix S and the via reflection matrix Γ are computed as

$$S = \begin{bmatrix} 0 & S^{(12)} & \cdots & S^{(1P)} \\ S^{(21)} & 0 & \cdots & S^{(2P)} \\ \vdots & \vdots & \ddots & \vdots \\ S^{(P1)} & S^{(P2)} & \cdots & 0 \end{bmatrix}$$
(53)

$$\Gamma = \begin{bmatrix} \Gamma^{(1)} & 0 & \cdots & 0 \\ 0 & \Gamma^{(2)} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \Gamma^{(P)} \end{bmatrix}$$
(54)

From equation (48), the outward wave expansion coefficient vector b is obtained as

$$b = (1 - \Gamma S)^{-1} (b_0 + \Gamma a_0)$$
(55)

and the inward wave expansion coefficient vector a is

$$a = a_0 + Sb \tag{56}$$

The vertical electrical field for each via can be obtained once the coefficient vectors b and a are known. The other field components of each via can be calculated by

$$E_t = \frac{1}{k_t^2} \partial_z \nabla_t E_z \tag{57}$$

$$H_t = -\frac{j\omega\varepsilon}{k_t^2} e_z \times \nabla_t E_z$$
(58)

Substituting equation (38) in equation (58) gives

$$H_{\phi}^{(i)} = \sum_{m=-\infty}^{\infty} \sum_{n=0}^{\infty} \frac{-j\omega\varepsilon}{k_n^2} \begin{bmatrix} b_{mn}^{(i)} \frac{\partial}{\partial\rho} H_{mn}^{(i)} \left(\rho^i, \phi^i, z\right) + \\ a_{mn}^{(i)} \frac{\partial}{\partial\rho} J_{mn}^{(i)} \left(\rho^i, \phi^i, z\right) \end{bmatrix}$$
(59)

Due to the assumption that there is only coaxial TEM mode that needs to be considered in the antipads in the planes, the current at the via pad is expressed as

$$I = 2\pi a \sum_{n=0}^{\infty} \frac{-j\omega\varepsilon}{k_n^2} \begin{bmatrix} b_{0n}^{(i)} \frac{\partial}{\partial\rho} H_{0n}^{(i)} \left(\rho^i, \phi^i, z\right) + \\ a_{0n}^{(i)} \frac{\partial}{\partial\rho} J_{0n}^{(i)} \left(\rho^i, \phi^i, z\right) \end{bmatrix}$$
(60)

Therefore,

$$I = 2\pi a \sum_{n=0}^{\infty} \frac{j\omega\varepsilon}{k_n} \begin{bmatrix} b_{0n}^{(i)} H_1^2(k_n a) + \\ a_{0n}^{(i)} J_1(k_n a) \end{bmatrix}$$
(61)

The original inward and outward wave coefficient vectors a_0 and b_0 due to the magnetic frill excitation in the antipad need to be calculated in order to find current *I*.

4.4. PARALLEL PLANE MODES EXCITED BY MAGNETIC FRILL CURRENT

The ith port current is given by Figure 4.2 shows a via structure with r, a and b as the radii of the barrel, pad and antipad, respectively; the separation of the plane pair or the via height is denoted as h; and the relative dielectric constant between plates is ε_R .



Figure 4.2. The via structure. (a) Top view of the via structure. (b) Side view of the via structure showing mode conversions.

A via can be viewed as a mode converter. The transverse electromagnetic (TEM) mode of a coaxial structure is assumed in the antipad apertures of the top and bottom planes. The TEM mode is converted into the parallel plane modes in the plane pair region. Due to the symmetry with regard to the azimuthal direction, there are only E_z , E_ρ and H_ϕ components (i.e., TMz modes) in the plane pair domain.

The TEM mode assumption in the via hole in the top or bottom plane results in a magnetic frill current distribution at z = z' and $\rho' \in [a, b]$.

$$M_{\phi} = -\frac{V_0}{\rho' \ln\left(\frac{b}{a}\right)} \delta(z - z')$$
(62)

The expression of the magnetic field H_{ϕ} is given in [3] and then, the vertical electric field can be derived as

$$E_{z} = \frac{1}{j\omega\varepsilon} \frac{1}{\rho} \frac{\partial \left(\rho H_{\phi}\right)}{\partial \rho}$$
(63)

Therefore, the inward and outward wave expansion coefficients can be expressed using $\Gamma_a^{(n)} = 0$ and $\Gamma_R^{(n)} = 0$ as

$$E_{z}(\rho,z) = \frac{j\pi V_{0}}{h\ln\left(\frac{b}{a}\right)} \sum_{n=0}^{\infty} \frac{\cos\frac{n\pi}{h}z'}{\left(1+\delta_{n0}\right)} \cdot \left[J_{0}(k_{n}b) - J_{0}(k_{n}a)\right] \cdot \left[H_{0}^{2}(k_{n}\rho)\cos\frac{n\pi}{h}z\right]$$
(64)

for $\rho \ge b$; and

$$E_{z}(\rho,z) = \frac{j\pi V_{0}}{h\ln\left(\frac{b}{a}\right)} \sum_{n=0}^{\infty} \frac{\cos\frac{n\pi}{h}z'}{\left(1+\delta_{n0}\right)} \cdot \left[H_{0}^{2}(k_{n}b) - H_{0}^{2}(k_{n}a)\right] \cdot \left[J_{0}(k_{n}\rho)\cos\frac{n\pi}{h}z\right]$$
(65)

for $\rho \le a$. Comparing equations (64) and (65) with (38), the elements for a_0 and b_0 can be obtained as for $\rho \ge b$.

$$b_{0mn}^{j}\left(V_{0},z'\right) = \frac{j\pi V_{0}\delta_{m0}}{h\ln\left(\frac{b_{j}}{a_{j}}\right)} \cdot \frac{\cos\frac{n\pi}{h}z'}{\left(1+\delta_{n0}\right)} \cdot \left[J_{0}\left(k_{n}b_{j}\right) - J_{0}\left(k_{n}a_{j}\right)\right]$$
(66)

and for $\rho \leq a$

$$a_{0mn}^{j}(V_{0},z') = \frac{j\pi V_{0}\delta_{m0}}{h\ln\left(\frac{b_{j}}{a_{j}}\right)} \cdot \frac{\cos\frac{n\pi}{h}z'}{(1+\delta_{n0})} \cdot \left[H_{0}^{2}(k_{n}b_{j}) - H_{0}^{2}(k_{n}a_{j})\right]$$
(67)

Obviously, the magnetic frill current can only excite the waves without azimuth variations. Equations (66) and (67) are used to fill the source vectors b_0 and a_0 in equation (55).

4.5. EXTENSION OF MULTIPLE SCATTERING METHOD TO VIA ARRAYS IN IRREGULAR SHAPED PLANE PAIR GEOMETRIES

The improved multiple scattering method uses the parallel plane modes to express the fields excited by the magnetic frill currents in via antipads instead of the plane pair Green's function. The parallel plane modes enable the extension of the multiple scattering method to any irregular plate pair. The wave transform matrix S for the entire via array in a plane pair can be also written in another form as illustrated in Figure 4.3.



Figure 4.3. Wave transform matrix S divided in sub matrix S_{nn} using addition theorem.

The S_{00} sub matrix which considers the zero-order mode and its reflection from the boundary of the irregular plane pair can be computed from the power plane impedance Z_{pp} of the via array using the transformation given in equation (68).

The entire transform matrix S is first obtained for a via array in a circular plane pair with PML boundary condition and then the S_{00} sub matrix is obtained using the transformation discussed above. The sub matrix S_{00} is replaced with S_{pp} and all other higher order sub-matrices are left unchanged.

The power plane impedance of an irregular plane pair geometry is computed using either cavity model, cavity model with segmentation method, or BEM method.

The transform function from Z_{pp} to S_{pp} is computed as in

$$S_{pp} = -\left[J_0 - Z_{pp}J_1\right]^{-1}\left[H_0 - Z_{pp}H_1\right]$$
(68)

where J_0 , J_1 , H_0 , and H_1 are all diagonal matrices of size P x P; P is no of vias in the array and are given as in equations (69) to (72).

$$H_0 = diag \left\{ H_0^2 \left(kr_i \right) h \right\}$$
(69)

$$J_0 = diag\left\{J_0\left(kr_i\right)h\right\}$$
(70)

$$H_{1} = diag \left\{ \frac{2\pi kr_{i}}{j\omega\mu} H_{1}^{2} (kr_{i})h \right\}$$
(71)

$$J_{1} = diag \left\{ \frac{2\pi kr_{i}}{j\omega\mu} J_{1}(kr_{i}) \right\}$$
(72)

where $H_{0(1)}^2$ is the zero(first) order Hankel function of second kind; $J_{0(1)}$ is zero(first) order Bessel function. r_i is the via port radius vector; k is the propagation constant.

4.6. MULTIPLE SCATTERING MECHANISMS AMONG VIA ARRAYS AND FLOWCHART OF MULTIPLE SCATTERING METHOD

The multiple scattering mechanisms possible in via arrays in practical printed circuit boards (PCB) are handled in the proposed multiple scattering method and is self explanatory in Figure 4.4.



Figure 4.4. The improved multiple scattering method mechanisms.

The flowchart of the improved multiple scattering method is shown in Figure 4.5. The flowchart illustrates the process flow of the multiple scattering method where the impressed magnetic frill currents in the via antipad region lead to the input and output vectors a and b on which pre-processing is done to obtain the admittance matrix. The post processing is done on the admittance matrix to obtain the overall scattering matrix of the via array.





Figure 4.5. The flowchart of the improved multiple scattering method.

The admittance matrix of the entire via array obtained at the end of the simulation is post-processed to extract S-parameters or Z-parameters. After obtaining the Sparameters of the via array in the plane pair, cross-talk between vias can be analyzed.

4.7. RESULTS AND DISCUSSIONS

The multiple scattering method is applied to three test cases for validations. The first two test cases deal with single cavity plane pair geometries. The third test case is a multi-layer rectangular geometry. Later, multiple scattering method is compared with a physics based circuit model to develop a understanding of the limitations of the physics based circuit model in engineering applications.

4.7.1. Validation of Multiple Scattering Method for Via Arrays in a Circular Plane Pair. Multiple scattering method is applied on a test geometry which is a circular plane pair geometry having two differential vias. The geometry of the via array in the circular plane pair is shown in Figure 4.6.



Figure 4.6. Circular cavity with two differential vias. (a) Top view of circular cavity with two differential vias. (b) Side view of circular cavity with two differential vias.

The input parameters used for simulation of the circular plane pair is listed in Table 4.1. Propagation constant k used in the simulations is mentioned in previous sections.

6.75 mils
20 mils
(-25,0) mils in X and Y direction
(25,0) mils in X and Y direction
5000 mils
60 mils
50 mils
Negligible
100 MHz to 10 GHz
1001 pts
3.5
0.004
PMC

Table 4.1. Input parameters of the simulation for two differential vias in a circular shaped plane pair.

In this example, differential and common modes in differential signaling are considered. Consider two signal vias 1, and 2 as shown in the Figure 4.6. This is a four port problem labeled as 1, 2, 3 and 4. B^i is the outward cylindrical wave from port i and A^i is the inward cylindrical wave into port i.

$$\begin{bmatrix} B^{1} \\ B^{2} \\ B^{3} \\ B^{4} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \begin{bmatrix} A^{1} \\ A^{2} \\ A^{3} \\ A^{4} \end{bmatrix}$$
(73)

As mentioned in [5], for differential mode, $A^1 = \frac{1}{2}$, $A^2 = -\frac{1}{2}$, $A^3 = 0$, $A^4 = 0$.

For this case, the reflection coefficient is $R = B^1 - B^2 = \frac{(S_{11} - S_{12} - S_{21} + S_{22})}{2}$ and

transmission coefficient is T = $B^3 - B^4 = \frac{(S_{31} - S_{32} - S_{41} + S_{42})}{2}$.

As mentioned in [5], for common-mode, $A^1 = 1$, $A^2 = 1$, $A^3 = 0$, $A^4 = 0$. For this case, the reflection coefficient is $R = B^1 = S_{11} + S_{12}$ and transmission coefficient is $T = B^3 = S_{31} + S_{32}$.

In numerical results, two signal vias are considered in either common mode or differential mode. The absolute value of $T = |S_{31} + S_{32}|$ can be used to describe the transmission of the common mode. The absolute value of $T = \left|\frac{(S_{31} - S_{32} - S_{41} + S_{42})}{2}\right|$

describes the transmission of the differential mode.

Magnitudes of the transmission coefficient for the common and differential modes are plotted as a function of frequency from 100 MHz to 10 GHz as shown in Figure 4.7. For a circular plane pair, oscillations are observed because of resonances and the resonant peaks are equally spaced as expected for circular waveguide geometries. The radius of the plane pair is 5 inches. The common mode exhibits resonances with a spacing equal to a few hundred MHz. At resonances, the common mode transmission coefficient amplitude decreases sharply. On the other hand, the differential mode transmission coefficient shows considerably less resonance effects. This is because, for the differential mode, only a very small portion of the return current passes through the plane pair impedance.



Figure 4.7. Transmission coefficient vs. frequency. (a) Common mode transmission coefficient vs. frequency. (b) Differential mode transmission coefficient vs. frequency.

The above test case has been simulated in [5]. The results from the reference paper and our improved multiple scattering method correlate very well with each other. Good correlation shown in FSV results listed in Table 4.2 and Table 4.3 verifies the correctness of the improved multiple scattering method and shows that it can handle circular shaped via array geometries.

Table 4.2. FSV results for comparison of common mode coefficient results from multiple scattering and reference paper for a circular shaped plane pair.

ADM	0.012349 (very good)
FDM	0.014713 (very good)
GDM	0.022671 (very good)

ADM	0.012578 (very good)
FDM	0.015822 (very good)
GDM	0.024541 (very good)

Table 4.3. FSV results for comparison of differential mode coefficient results from multiple scattering and reference paper for a circular shaped plane pair.

4.7.2. Validation of Multiple Scattering Method for Via Arrays in an Irregular Plane Pair. Multiple scattering method is applied on a test geometry which is an irregular plane pair geometry having 7 x 7 vias. The geometry of the via array in the irregular plane pair is shown in Figure 4.8. The result from the improved multiple scattering method for the test geometry is compared with full wave solutions for validation. The HFSS model of the 7 x 7 via array in irregular shaped cavity is shown in Figure 4.9.



Figure 4.8. A 7 x 7 via array in the irregular shaped cavity. (a) Port assignment of the 7 x 7 via array in the irregular shaped cavity. (b) Top view of the irregular shaped cavity with the 7 x 7 via array.



Figure 4.9. HFSS model of the 7 x 7 via array in the irregular shaped cavity.

The input parameters used for simulation of the 7 x 7 via array in the irregular plane pair is listed in Table 4.4.

Via drill radius	10 mils
Via antipad radius	15 mils
Signal via locations	(500,475), (500,425), (550,475), (550,525),
	(600,475), (600,525), and (1250,250)
	specified in X and Y direction in mils
Dimensions of the plane pair	1500 x 1000 mils specified in X and Y
	direction
Dielectric thickness	10 mils
Plate thickness	1 mil
Frequency range	100 MHz to 10 GHz
Frequency points	200 pts
Dielectric constant	4.2
Tangent loss	0.02
Boundary conditions	PMC

Table 4.4. Input parameters for the simulation of the 7 x 7 via array in the irregular shaped plane pair.

The simulation results from HFSS and the multiple scattering method are compared to validate the multiple scattering method. The results are shown in Fig 4.10.



Figure 4.10. Comparison of |S| results between HFSS and multiple scattering method for the irregular shaped plane pair. (a) – (f) S_{14} , S_{16} , S_{17} , S_{18} , S_{37} , and S_{67} results.

The FSV results for the magnitude comparisons are listed in Table 4.5.

	S ₁₄	S ₁₆	S ₁₇	S ₁₈	S ₃₇	S ₆₇
ADM	0.015944	0.034967	0.049039	0.040276	0.031733	0.022179
FDM	0.022235	0.05642	0.08278	0.046861	0.047115	0.023061
GDM	0.030637	0.0731	0.095483	0.067085	0.06219	0.035233

Table 4.5. FSV results for the magnitude comparison of S_{14} , S_{16} , S_{17} , S_{18} , S_{37} , and S_{67} from the multiple scattering method and HFSS.

The simulation time taken by the multiple scattering method is compared with HFSS as listed in Table 4.6.

Table 4.6. Summary of the simulation times taken by HFSS and the multiple scattering methods for the 7 x7 via array in the irregular shaped plane pair geometry.

Computational Method	Simulation time
HFSS	2.5 hrs
Multiple scattering method	$2 \text{ mins} + 1 \text{ min} (Z_{pp} \text{ computation})$

Good correlation shown in the FSV results proves that the improved multiple scattering method can handle via arrays in irregular shaped plane pair geometries. The comparison of the simulation times shows the improved multiple scattering method is much faster than full wave simulations. 4.7.3. Validation of Multiple Scattering Method for Via Arrays in a Multi – Layer Printed Circuit Board. Multiple scattering method is applied on a test geometry which is a multi-layer printed circuit board (PCB) built using rectangular plane pairs having a 6 x 6 via array. The test geometry has two signal vias and four ground vias. The geometry of the via array in the multi-layer printed circuit board (PCB) is shown in Figure 4.11. The result from multiple scattering method for this test geometry is compared with full wave and a physics based circuit model solutions for validation.



Figure 4.11. A multi-layer model of the 6 x 6 via array with 2 signal and 4 ground vias in the rectangular shaped cavity.

The multi-layer printed circuit board (PCB) is simulated by taking each single cavity at a time. The S-parameter block for each cavity is obtained using the multiple scattering method and all the blocks are cascaded together to get the final S-parameter block of the entire multi-layer printed circuit board (PCB). The multi-layer printed circuit board (PCB) geometry is also modeled using a physics based circuit model and HFSS to get the final response. The HFSS response is used as a benchmark to validate the multiple scattering method. The input parameters of the multi-layer geometry for each cavity are listed in Table 4.7. The cavity thicknesses of the individual cavities are listed in Table 4.8.

Table 4.7. Input parameters of the simulation for the 6 x 6 via array in the multi-layer printed circuit board geometry consisting of rectangular cavities.

Via drill radius	5 mile
v la ul III Laulus	5 11115
Via antipad radius	15 mils
Signal via locations	(475,750), and (525,750) specified
	in X and Y direction in mils
Ground via locations	(435,710), (565,710), (565,790),
	and (435,790) specified in X and Y
	direction in mils
Dimensions of the plane pair	1000 x 1500 mils specified in X
	and Y direction
Plate thickness	0.7 mil
Frequency range	200 MHz to 40 GHz
Frequency points	200 pts
Dielectric constant	4.0
Tangent loss	0.01
Boundary conditions	PMC

Table 4.8. Individual cavity thickness used in building the multi-layer PCB.

Cavity 1 thickness in mils	3.54
Cavity 2 thickness in mils	16.27
Cavity 3 thickness in mils	15.57
Cavity 4 thickness in mils	3.39
Cavity 5 thickness in mils	15.57
Cavity 6 thickness in mils	16.27
Cavity 7 thickness in mils	3.54

The results of the physics based circuit model, multiple scattering method, and HFSS are plotted in Figure 4.12 to validate the multiple scattering method for the multi-layer geometry.



Figure 4.12. Magnitude comparison between the physics based circuit model, the multiple scattering method, and HFSS of |S| parameters. (a) - (b) S₁₁ and S₁₂ results.

The comparison of the results demonstrates that the multiple scattering method is more accurate than the physics based circuit model for the test multi-layer geometry at high frequencies. Capacitive coupling between the via and planes is distributed along the via length, which is modeled as lumped capacitances in the physics based circuit model that might be a possible reason for the discrepancy between the physics based circuit model and the multiple scattering results. Neglecting multiple scattering of higher order modes among vias in the physics based circuit model is also a possible reason for the discrepancy. The simulation times listed in Table 4.9 show that the physics based circuit model and the multiple scattering method are very fast compared to HFSS.

Computational Method	Simulation time
HFSS	16 hrs
Multiple Scattering Method	12 mins + 5 mins (ADS)
Physics Based Circuit Model	5 mins + 5 mins (ADS)

Table 4.9. Summary of simulation time taken by HFSS, multiple scattering, and physics based circuit methods for the 6 x6 via array in multi-layer PCB consisting of rectangular cavities.

4.7.4. Quantifying Multiple Scattering Method and Physics Based Circuit Model for Via Arrays by Varying the Via Pitch Size and Dielectric Thickness. The multiple scattering method and the physics based circuit model results are compared in this section for a 9 x 9 via array in a rectangular plane pair with different via pitch and dielectric thickness values. The geometry of the 9 x 9 via array in a rectangular plane pair is shown in Figure 4.13.



Figure 4.13. A 9 x 9 via array in the rectangular cavity. (a) Port assignment of the 9 x 9 via array in the rectangular cavity. (b) Top view of the 9 x 9 via array in the rectangular cavity.

The input parameters of the 9 x 9 via array in the rectangularly shaped plane pair geometry is listed in Table 4.10. By varying the via pitch size 's' and dielectric thickness 'd' while keeping all other parameters fixed, a set of six simulation results are generated using the multiple scattering and the physics based circuit model methods. The physics based circuit model results are compared with multiple scattering method results to quantify when to use the multiple scattering method with via pitch and dielectric thickness as the deciding factors. Based on the comparison, a set of guidelines are framed for analyzing via arrays in printed circuit boards using either the physics based circuit model or the multiple scattering method. The comparison results are shown in Figures 4.14 - 4.19. The simulation time taken by each method as listed in Table 4.11 shows the efficiency of both methods for the present problem.

Table 4.10. Input parameters of the simulation for the 9 x 9 via array in the rectangular shaped geometry.

Via drill radius	6 mils
Via antipad radius	20 mils
Center signal via location	(3000,2000) mils in X and Y
	direction
Dimension of the plane pair	8000 x 6000 mils in X and Y
	direction
Dielectric thickness values (d)	5 mils, 10 mils, and 15 mils
Via pitch size values (s)	50 mils, and 200 mils
Plate thickness	1 mil
Frequency range	100 MHz to 40 GHz
Frequency points	799 pts
Dielectric constant	4.4
Tangent loss	0.02
Boundary conditions	PMC



Figure 4.14. Magnitude comparison between the physics based circuit model, and the multiple scattering method of S_{11} , and S_{1-15} results for the rectangular plane pair with via pitch = 50 mils and dielectric thickness = 5 mils. (a) - (b) S_{11} , and S_{1-15} results.



Figure 4.15. Magnitude comparison between the physics based circuit model, and the multiple scattering method of S_{11} , and S_{1-15} results for the rectangular plane pair with via pitch = 50 mils and dielectric thickness = 10 mils. (a) - (b) S_{11} , and S_{1-15} results.


Figure 4.16. Magnitude comparison between the physics based circuit model, and the multiple scattering method of S_{11} , and S_{1-15} results for the rectangular plane pair with via pitch = 50 mils and dielectric thickness = 15 mils. (a) - (b) S_{11} , and S_{1-15} results.



Figure 4.17. Magnitude comparison between the physics based circuit model, and the multiple scattering method of S_{11} , and S_{1-15} results for the rectangular plane pair with via pitch = 200 mils and dielectric thickness = 5 mils. (a) - (b) S_{11} , and S_{1-15} results.



Figure 4.18. Magnitude comparison between the physics based circuit model, and the multiple scattering method of S_{11} , and S_{1-15} results for the rectangular plane pair with via pitch = 200 mils and dielectric thickness = 10 mils. (a) - (b) S_{11} , and S_{1-15} results.



Figure 4.19. Magnitude comparison between the physics based circuit model, and the multiple scattering method of S_{11} , and S_{1-15} results for the rectangular plane pair with via pitch = 200 mils and dielectric thickness = 15 mils. (a) - (b) S_{11} , and S_{1-15} results.

Table 4.11. Summary of the simulation	time taken by	the multiple scatte	ering and the
physics based circuit methods for the	9 x 9 via array	in the rectangular	plane pair.

Computational Method	Simulation time
Multiple Scattering Method	$6 \text{ mins} + 8 \text{ mins} (Z_{pp} \text{ computation})$
Physics Based Circuit Model	15 mins

The physics based circuit model is described in Figures 4.20 and 4.21. The TEM mode wave excited in the via antipad holes excites the TM_z parallel plane modes between the plane pair. The power plane impedance Z_{pp} computed using the cavity or other numerical methods takes in to account the zero order TM_z modes. Via to plane capacitive coupling is described by the higher order TM_z modes and is modeled as lumped capacitances. The multiple scattering among vias is not considered in physics based circuit and the multiple scattering methods are plotted as functions of dielectric thickness and via pitch size shown in Figures 4.22 - 4.26.



Figure 4.20. The physics based circuit model for via arrays in the printed circuit board.

The via to plane connection in the physics based circuit model using the lumped capacitances and the power plane impedance Z_{pp} as illustrated in Figure 4.21.



Figure 4.21. Via to plane connection using the lumped capacitances and the Z_{pp} in the physics based circuit model.



Figure 4.22. Discrepancy comparison in S_{11} and S_{1-15} of the physics based circuit model and the multiple scattering method for different dielectric thickness keeping via pitch fixed at 50 mils. (a) Discrepancy in S_{11} result. (b) Discrepancy S_{1-15} result.



Figure 4.23. Discrepancy comparison in S_{11} and S_{1-15} of the physics based circuit model and the multiple scattering method for different dielectric thickness keeping via pitch fixed at 200 mils. (a) Discrepancy in S_{11} result. (b) Discrepancy S_{1-15} result.



Figure 4.24. Discrepancy comparison in S_{11} and S_{1-15} of the physics based circuit model and the multiple scattering method for different via pitch sizes keeping dielectric thickness fixed at 5 mils. (a) Discrepancy in S_{11} result. (b) Discrepancy S_{1-15} result.



Figure 4.25. Discrepancy comparison in S_{11} and S_{1-15} of the physics based circuit model and the multiple scattering method for different via pitch sizes keeping dielectric thickness fixed at 10 mils. (a) Discrepancy in S_{11} result. (b) Discrepancy S_{1-15} result.



Figure 4.26. Discrepancy comparison in S_{11} and S_{1-15} of the physics based circuit model and the multiple scattering method for different via pitch sizes keeping dielectric thickness fixed at 15 mils. (a) Discrepancy in S_{11} result. (b) Discrepancy S_{1-15} result.

From the comparison shown in Figures 4.14 - 4.19, differences between the results increase as the dielectric thickness increases when the via pitch size is either 50 mils or 200 mils. The physics based circuit model considers the coupling between via and

plane as lumped capacitances which may not be sufficient as dielectric thickness increases due to the onset of distributed behaviors. Other reasons might be that the coupling among the vias is modeled by the Z_{pp} (zero order modes) only in the physics based circuit model and multiple scattering of higher order modes among vias is not considered. As the via pitch size increases, differences are expected to be small as the effect of higher order mode coupling among vias has little effect.

In Figure 4.21 the connection between via and plane pair is shown with port numbering and lumped capacitances. The physics based circuit model considers the coupling between via and plane as lumped capacitances which may not be sufficient as dielectric thickness increases due to the onset of distributed behaviors. Other reasons might be that coupling among the vias is modeled by the Z_{pp} (zero order modes) only and multiple scattering of higher order modes among vias is not considered.

Looking at Figures 4.22 - 4.23, discrepancy increases with the increase in frequency. Looking at Figures 4.24 - 4.26, discrepancy increases with the increase in frequency. There is no clear relationship between the discrepancy observed and the via pitch size. The discrepancy in results does not decrease with the increase of via pitch size as expected. The reason for the trend exhibited by the discrepancy curves when dielectric thickness is fixed needs further investigations.

5. DISK RESONATOR STUDY USING BOUNDARY ELEMENT METHOD, MULTIPLE SCATTERING METHOD, AND EFFECTIVE DIELECTRIC MEDIUM APPROACH

The disk resonator is basically a circular shaped plane pair which consist a large number of vias or unplated holes. Disk resonator behaves more like a circular waveguide structure. Transverse electromagnetic (TEM) wave launched into a circular waveguide structure excites the parallel plane modes, which get reflected from the plane edges exhibiting resonant behaviors. The resonances observed are equally spaced in frequency as observed in a circular waveguide. Disk resonator behavior can be studied either by the physics based circuit model, the multiple scattering method, an effective dielectric medium approach, full wave modeling, or by measurements.

In the physics based circuit model, the disk resonator is modeled using lumped circuit elements. Boundary element method (BEM) in [16] is used to extract the power plane impedance Z_{pp} of a circular plane pair. Via barrel capacitance is computed using the analytical expressions developed in [3]. Using the physics based circuit model, a solid disk resonator as well as a perforated disk resonator can be modeled using BEM considering unplated holes as PMC boundaries. The overall Z_{pp} in a perforated case is further transformed to effective Z_{pp} which considers the unplated holes.

In the multiple scattering method presented in section 4, a disk resonator is modeled by taking multiple wave scattering among vias and also the reflections from edges of the disk resonator using the analytical expression in [11].

An effective dielectric medium approach can be used to model the perforated disk resonator case by modeling the unplated holes in the plane pair as air dielectric medium. The Maxwell Garnett formula [17] is applied to find the effective dielectric properties of the mixture containing air and dielectric materials. Once the effective dielectric medium is obtained, the physics based circuit model or the multiple scattering method can be applied.

5.1. SOLID DISK RESONATOR STUDY USING PHYSICS BASED CIRCUIT MODEL EMPLOYING BEM AND MULTIPLE SCATTERING METHOD

The Solid disk resonator studied here is a circular shaped plane pair with one via at the center shorted to the bottom plane as shown in Figure 5.1.



Figure 5.1. The cavity of the solid disk resonator including coax launch used in measurements. (a) Side view of the cavity of the solid disk resonator. (b) Side view of the solid disk resonator cavity including coax launch.

The actual setup used in measurements has a coax launch along with the disk resonator. The coax launch needs to be modeled first to include its effect in the final model simulations. The coax launch is modeled in HFSS using the inner conductor diameter and outer conductor diameter as shown in Figure 5.2.



Figure 5.2. The solid disk resonator stub used in measurements. (a) Side view of the solid disk resonator stub used in the measurements. (b) Actual measurement setup of the solid disk resonator stub. (c) Coax launch model for the solid disk resonator stub in HFFS.

The coax launch used in measurements is complex which takes considerable effort to model in HFSS, so a simple coax launch is modeled initially in HFSS and the coax length is optimized fixing all other parameters until the best phase match with actual coax used in measurements is achieved. The coax launch model is shown in Figure 5.2. The simulation for obtaining the equivalent coax launch length is done for two trials using lengths of 860 mils and 870 mils. The length of 860 mils is actually obtained from length listed in Figure 5.2 (a) specified in manufacturing sheet. The length is then varied until the best phase match with actual coax launch used in measurements is achieved. The input parameters of the coax launch trials modeled in HFSS are listed in Table 5.1.

	Trial 1	Trial 2
Inner conductor diameter	12	12
(mils)		
Outer conductor diameter	37	37
(mils)		
Dielectric constant	2.1	2.1
Tangent Loss	0.001	0.001
Length	860	870
(mils)		
Thickness of outer	10	10
conductor (mils)		
Frequency Range	100 MHz – 25 GHz	100 MHz – 25 GHz

Table 5.1. Input parameters used for designing the coax launch in HFSS for trials 1 and 2.

The S-parameter block obtained from HFSS simulation is assembled in ADS schematic shown in Figure 5.3 which models the equivalent measurement setup used to measure the reflection loss of a coax launch.



Figure 5.3. ADS schematic to simulate the reflection loss of the coax launch.

The simulation results obtained from ADS for the coax launch modeled in HFSS and measured results are compared to get the best match for the coax length. The phase S_{11} of the measured and simulated results are compared as shown in Figure 5.4.



Figure 5.4. Phase comparison between simulation and measurement results of the coax launch for two trials. (a) Phase comparison of S_{11} for trial 1. (b) Phase comparison of S_{11} for trial 2.

From the results in Figure 5.4, it can be said that trial 2 has the best phase match with the measured results. These simulations give an estimate of the equivalent coax length for the solid disk resonator to be used in later simulations. The trial 2 S-parameter block will be included in the overall model of the solid disk resonator.

5.1.1. Physics Based Circuit Model Employing BEM. Next intermediate step before the overall model is assembled is to extract the power plane impedance Z_{pp} of the solid disk resonator using the boundary element method (BEM).

The first order Debye model is used to model the FR-4 dielectric material, used in solid disk resonator as the exact dielectric constant and tangent loss term are not known for the FR-4 material. Skin effect loss is also considered in the simulations to account for the conductor loss in the metal plates.

The first order Debye equation used to model the dielectric material in the simulations is given as in equation (74).

$$\varepsilon = \varepsilon_{\infty} + \frac{(\varepsilon_s - \varepsilon_{\infty})}{(1 + j\omega\tau)}$$
(74)

where ε_{∞} is epsilon infinity, ε_s is epsilon static, τ is tau time constant, and ω is angular frequency.

From equation (74) dielectric constant and tangent loss term can be calculated using the equations (75) and (76).

$$\varepsilon_r = real(\varepsilon) \tag{75}$$

$$\tan \delta = -\frac{imag(\varepsilon)}{\varepsilon_r}$$
(76)

The propagation constant k used in the simulations is calculated as shown in equations (77) - (79).

$$k = k' - k'' \tag{77}$$

$$\vec{k} = \omega^* sqrt(\mu^* \mathcal{E}_r^* \mathcal{E}_0) \tag{78}$$

$$k'' = 0.5 * k' * (\tan \delta + \frac{\delta_s}{h}) \tag{79}$$

where h is the dielectric thickness, δ_s is the skin depth of the metal plates.

The dielectric constant and tangent loss terms are plotted versus frequency for the debye model used in simulations in Figure 5.5. The input parameters of the solid disk resonator to be used in extracting power plane impedance are listed in Table 5.2.



Figure 5.5. The debye model curves of the dielectric material used in simulations. (a) \mathcal{E}_r plot vs frequency for the debye model. (b) Tan δ plot vs frequency for the debye model.

After obtaining the power plane impedance Z_{pp} , the via to antipad capacitance needs to be computed for the geometry listed in Table 5.2 using the analytical formulation developed in [3]. The computed via to antipad capacitance is 113.7175 fF for the given geometry.

Via drill diameter	12 mils
Via antipad diameter	37 mils
Dielectric Material	FR-4
Diameter of Disk	3 inch
Dielectric thickness	57 mils
Frequency Range	100 MHz – 15 GHz
	(499 pts in linear scale)
Thickness of metal plates	1Oz
EpsInfinity	4.1068
EpsStatic	4.3021
Tautime	3.33e-11

Table 5.2. Input parameters used for extracting Z_{pp} of the solid disk resonator.

The final step is to assemble all the elements in ADS schematics to build the overall model of the solid disk resonator including the coax launch and run the simulation as in Figure 5.6.



Figure 5.6. ADS schematics of the entire model of the solid disk resonator including the coax launch using BEM.

The simulation results obtained from ADS for the entire solid disk resonator model using the BEM and the measured results are compared to check the effectiveness of the BEM to model the disk resonator. The magnitude and phase of the measured and simulated S_{11} results are compared as shown in Figure 5.7. The comparison is shown up to 15 GHz.



Figure 5.7. Comparison of S_{11} results from the BEM method and the measurements for the solid disk resonator. (a) Magnitude comparison of S_{11} results. (b) Phase comparison of S_{11} results.

The FSV results for the above comparisons are listed in Table 5.3. The FSV results show good correlations between the BEM and the measured results.

Table 5.3. FSV results for comparison of the results from the BEM and the measurements for the solid disk resonator.

ADM	0.18193 (very good)
FDM	0.24661 (good)
GDM	0.33486 (good)

5.1.2. Multiple Scattering Method. The next step after getting an equivalent coax launch model is to simulate the solid disk resonator shown in Figure 5.1 using the multiple scattering method. The input parameters of the solid disk resonator are listed in Table 5.2. The same first order Debye model for the dielectric and propagation constant k is used in simulations as in the previous section.

The computation of the via to antipad capacitance is not necessary in the multiple scattering method as it is already included in the formulation. The admittance matrix of the solid disk resonator obtained from the multiple scattering method includes the effect of the via to antipad capacitance as well as the power plane impedance Z_{pp} . The individual blocks of the entire solid disk resonator model including the coax launch is assembled in ADS schematic as shown in Figure 5.8.



Figure 5.8. ADS schematics of the entire model of the solid disk resonator including the coax launch using the multiple scattering method.

The simulation results obtained from ADS for the entire solid disk resonator model using the multiple scattering method and the measured results are compared to check the effectiveness of the multiple scattering method to model the disk resonator. The magnitude and phase of the measured and simulated S_{11} results are compared as shown in Figure 5.9. The comparison is shown only up to 15 GHz.

As expected from a circular waveguide the resonances due to the reflections of the parallel plane modes from plane edges exhibited in the solid disk resonator are equally spaced. This phenomenon is captured by both the BEM and the multiple scattering methods.



Figure 5.9. Comparison of S_{11} results from the multiple scattering method and the measurements for the solid disk resonator. (a) Magnitude comparison of S_{11} results. (b) Phase comparison of S_{11} results.

The FSV results for the above comparisons are listed in Table 5.4. The FSV results show good correlations between the multiple scattering method and the measured results. The simulation time taken by the BEM and the multiple scattering methods are compared in Table 5.5.

ADM	0.18193 (very good)
FDM	0.24661 (good)
GDM	0.33486 (good)

 Table 5.4. FSV results for comparison of the results from the multiple scattering method and the measurements for the solid disk resonator.

Table 5.5. Comparison of the simulation times of the BEM and the multiple scattering methods for the solid disk resonator study.

Approach	Simulation time
BEM with physics based circuit	8 hrs + 5 mins (ADS)
model	
Multiple Scattering	3 mins + 5 mins (ADS)

5.2. PERFORATED DISK RESONATOR STUDY USING PHYSICS BASED CIRCUIT MODEL EMPLOYING BEM AND EFFECTIVE DIELECTRIC MEDIUM APPROACH

The perforated disk resonator is a circular shaped plane pair with a via at the center shorted to the bottom plane and a number of unplated holes as shown in Figure 5.10.



Figure 5.10. Perforated disk resonator cavity used in measurements. (a) Side view of the cavity of the perforated disk resonator. (b) Side view of the cavity of the perforated disk resonator including coax launch.

The actual setup used in measurements has a coax launch along with the perforated disk resonator that is different to the coax launch in the solid disk resonator. The coax launch needs to be modeled first to include its effect in the final assembled model simulations. The coax launch is modeled in HFSS using the inner conductor diameter and outer conductor diameter as shown in Figure 5.11.



Figure 5.11. The perforated disk resonator stub used in measurements. (a) Side view of the perforated disk resonator stub. (b) Actual measurement setup of the perforated disk resonator stub (c) Coax launch model for the perforated disk resonator stub in HFFS.

The coax launch model built in HFSS is shown in Figure 5.11. The simulation for obtaining an equivalent coax launch length is done for three trials using lengths of 860 mils, 870 mils, and 890 mils. The ADS schematic to simulate the return loss of the coax launch is shown in Figure 5.3. The input parameters of the coax launch model for trial 3 is the same as the input parameters used in trial 1 and trial 2 except for the coax length.

The results obtained from ADS for the coax launch modeled in HFSS and from measurements are compared to get the best match for the coax length. The phase S_{11} of the measured and simulated results is compared as shown in Figure 5.12.



Figure 5.12. Phase comparison between simulation and measurement results of the coax launch for three trials. (a) S_{11} for trial 1. (b) S_{11} for trial 2. (c) S_{11} for trial 3.

From the results in Figure 5.12, it can be said that trial 3 has the best phase match with the measured results. These simulations give an estimate of the equivalent coax length of perforated disk resonator to be used in later simulations. The trial 3 S-parameter block will be included in the overall model of the perforated disk resonator.

5.2.1. Physics Based Circuit Model Employing BEM. Next intermediate step before the overall model is assembled is to extract the power plane impedance Z_{pp} of the perforated disk resonator using the boundary element method (BEM). The measurement setup of the perforated disk resonator is shown in Figure 5.13. The input parameters of the perforated disk resonator used in extracting power plane impedance are listed in Table 5.6.

The same first order debye model and the propagation constant k used in the solid disk resonator simulations are used for the perforated disk resonator simulations. Further, after obtaining the power plane impedance Z_{pp} the via to antipad capacitance needs to be computed for the geometry listed in Table 5.6 using analytical formulation developed in [3]. The computed via to antipad capacitance is 113.7175 fF for the given geometry.



Figure 5.13. Top view of the perforated disk resonator with holes in 1mm by 1mm grid.

Via drill diameter	12 mils
Via antipad diameter	37 mils
Dielectric Material	FR-4
Diameter of Disk	3 inch
Dielectric thickness	57 mils
Holes located on grid size	1mm x 1mm
Frequency Range	100 MHz – 15 GHz
	(150 pts in linear scale)
Thickness of metal plates	10z
EpsInfinity	4.1068
EpsStatic	4.3021
Tautime	3.33e-11

Table 5.6. Input parameters used for extracting Z_{pp} of the perforated disk resonator.

The final step is to assemble all the individual blocks in ADS as in Figure 5.14.



Figure 5.14. ADS schematics of entire model of the perforated disk resonator including the coax launch using the BEM.

The results obtained from ADS for the entire perforated disk resonator model using the BEM and from the measurements are compared to check the effectiveness of the BEM to model the perforated disk resonator. The magnitude and phase of the measured and simulated S_{11} results are compared as shown in Figure 5.15. The comparison is shown up to 15 GHz.



Figure 5.15. Comparison of S_{11} results from the BEM method and the measurements for the perforated disk resonator. (a) Magnitude comparison of S_{11} results. (b) Phase comparison of S_{11} results.

As expected from a circular waveguide, the resonances due to the reflections of the parallel plane modes from plane edges exhibited in the perforated disk resonator are equally spaced. The FSV results for the above comparisons are listed in Table 5.7. The FSV results show good correlations between the BEM and the measured results. The correlation is good for frequencies below 5 GHz. The higher order mode scattering among vias which are neglected in physics based circuit model employing BEM might be one of the reasons for the discrepancies observed at higher frequencies. Manufacturing tolerances are also one of the reasons for the discrepancy.

ADM	0.2883 (good)
FDM	0.29507 (good)
GDM	0.45831 (fair)

Table 5.7. FSV results for comparison of the results from the BEM and the measurements for the perforated disk resonator.

5.2.2. Effective Dielectric Medium Approach. In effective dielectric medium approach, the unplated holes on the circular disk resonator are considered as air dielectric medium. The extended Maxwell Garnett formula to find the effective dielectric material properties from the mixture of air and FR-4 dielectric media mentioned in [17] is applied to obtain the effective dielectric properties. The extended Maxwell Garnett formulation to obtain the effective dielectric properties of the mixture of dielectrics is given as

$$\varepsilon_{eff} = \varepsilon_b + v_i . \varepsilon_b . \frac{(\varepsilon_i - \varepsilon_b)}{\varepsilon_b + (1 - v_i) . (\varepsilon_i - \varepsilon_b) . F_z}$$
(80)

$$F_z = \left(\frac{1}{a}\right)^2 \ln a, a = \frac{l}{d}$$
(81)

$$F_x + F_y + F_z = 1 \tag{82}$$

$$F_x = F_y = \frac{1 - F_z}{2} \tag{83}$$

In equations (80) – (83), l = length of the inclusion, d = diameter of the inclusion, ε_b is the dielectric constant of the base material, ε_i is the dielectric constant of the inclusion material, v_i is the volume fraction of the inclusions, F_x is the polarization factor along the x direction, F_y is the polarization factor along the y direction, and F_z is the polarization factor along the z direction. As illustrated in Figure 5.16, all the perforations or air holes are aligned in the z direction. The effective dielectric property is actually a tensor, but dielectric property along the z direction which is the propagation direction is considered.



Figure 5.16. Air dielectrics due to the unplated holes on the disk aligned in the z propagation direction.

Once the effective dielectric material properties are extracted from the Maxwell Garnett formulation, the physics based approach employing BEM is used to simulate the perforated disk resonator. As the holes are modeled as air dielectrics, perforated disk resonator is modeled as a solid disk resonator with effective dielectric material properties.

The power plane impedance Zpp is extracted using the BEM for the solid disk resonator using the effective dielectric medium, and the via to antipad capacitance is computed as done in the previous simulations.

Then all the blocks are assembled in ADS schematics to build the entire model including the coax launch which is equivalent to the perforated disk resonator measurement setup used to take the measurements. The results obtained from ADS for the entire perforated disk resonator model using the effective dielectric medium approach and the measured results are compared to check the effectiveness of the approach to model the perforated disk resonator.

The FSV results for the above comparisons are listed in Table 5.8. The simulation time taken by the BEM and the effective dielectric medium approaches is compared in Table 5.9. The magnitude and phase of the measured and simulated S11 results are compared as shown in Figure 5.17. The comparison is shown up to 15 GHz.

Table 5.8. FSV results for comparison of the results from the effective dielectric medium approach and the measurements for the perforated disk resonator.

ADM	0.2463 (good)
FDM	0.26276 (good)
GDM	0.3467 (good)

Table 5.9. Comparison of the simulation times of the BEM and the effective dielectric medium approach for the perforated disk resonator study.

Approach	Simulation time
BEM with physics based circuit model	216 hrs + 5 mins (ADS)
Effective dielectric medium approach	2.4 hrs + 5 mins (ADS)



Figure 5.17. Comparison of S_{11} results from the effective dielectric medium approach and the measurements for the perforated disk resonator. (a) Magnitude comparison of S_{11} results. (b) Phase comparison of S_{11} results.

The correlation between the effective dielectric medium approach and the measured results is better than the BEM method possibly because the modeling of the dielectrics is more accurate in the effective dielectric medium approach.

6. CONCLUSION AND FUTURE SCOPE

In section 2, the capacitance values obtained from the finite difference method and the analytical formula are compared to validate the finite difference method. The simulation times of both the methods are compared to show the efficiency of the methods. Simulation time of the finite difference method can be improved by using adaptive technique to compute potential values on the grid by setting optimal learning rate. Future work involves the improvement of the finite difference method to compute the via capacitance when the pad is in a signal layer inside a parallel – plane cavity.

In section 3, the infinite plane pair model has been demonstrated to agree well with the conventional finite plane pair model when there are many shorting vias located around the signal vias. These shorting vias create a local resonant cavity that prevents the electromagnetic waves from escaping the local cavity, thus the distributed resonances associated with the plane pair dimensions are mostly eliminated. The more the shorting vias are located around the signal vias, and the smaller the spacing between the signal and shorting vias, the better the agreement between the infinite and finite plane pair models. The infinite plane pair Z_{pp} model can be used in practical PCB analyses to provide a fast first-order estimation, due to its efficiency and computational speed.

In section 4, the results shown validate the multiple scattering method for via arrays in circular shaped plane pair, irregular shaped plane pair, and multi-layer geometries. The FSV results show that the multiple scattering and HFSS have good correlations. The simulation time taken by the multiple scattering method for all the test cases demonstrate its ability in getting quick results compared to HFSS. The comparison of the multiple scattering, physics based circuit model, and full wave simulation results shows that the multiple scattering method may be more accurate at high frequencies than the physics based circuit model. Overall speaking, the discrepancies, as shown in the examples, are relatively small. In other words all three methods may be acceptable for engineering evaluations. When via pitch size is fixed, the discrepancy between the multiple scattering and physics based circuit model results increases with dielectric thickness which may be contributed by the inaccurate via-plane capacitance modeling in the physics based circuit model. When dielectric thickness is fixed, the discrepancy between the multiple scattering and physics based circuit model results does not have a clear relationship with the via pitch size and needs further investigations. Future work includes the addition of the phi-directional variation of fields for via arrays in irregularly shaped plane pairs and the addition of the boundary ports in the multiple scattering method so that it can be integrated with the physics based circuit model to handle via arrays in general PCB geometries.

In section 5, model to hardware correlation is demonstrated for solid and perforated disk resonators using the physics based circuit model employing BEM, multiple scattering method, and effective dielectric medium approach. Good correlation is observed between the simulated and measured results.

BIBLIOGRAPHY

- [1] S. H. Hall, G. W. Hall, and J. A. McCall, *High-speed digital system design-a* handbook of interconnect theory and design practices, John Wiley & Sons Inc., 2000.
- [2] C. Schuster, Y. Kwark, G. Selli, and P. Muthana, "Developing a 'Physical' Model for Vias," DesignCon 2006, Santa Clara, CA USA, Feb. 6 - 9, 2006.
- [3] Y. Zhang, J. Fan, G. Selli, M. Cocchini, F. D. Paulis, "Analytical evaluation of via-plate capacitance for multilayer printed circuit boards and packages," *IEEE Trans. Microwave Theory Tech.*, accepted, 2008.
- [4] H. Chen, Q. Lin, L. Tsang, C.-C. Huang, and V. Jandhyala, "Analysis of a large number of vias and differential signaling in multilayered structures," *IEEE Trans. Microwave Theory Tech.*, vol. 51, no. 3, pp. 818-829, Mar. 2003.
- [5] L. Tsang, and D. Miller, "Coupling of vias in electronic packaging and printed circuit board structures with finite ground plane," *IEEE Trans. Adv. Packag.*, vol. 26, no. 4, pp. 375-384, Nov. 2003.
- [6] Giuseppe Selli, "BGA Footprints modeling and physics based via models validation for power and signal integrity applications," PhD Dissertation, University of Missouri-Rolla, 2007.
- [7] G.-T. Lei, R. W. Techentin, P. R. Hayes, D. J. Schwab, and B. K. Gilbert, "Wave model solution to the ground/power plane noise problem," *IEEE Trans. Instrum. Meas.*, vol. 44, no. 2, pp. 300-303, April 1995.
- [8] Z. L. Wang, O. Wada, Y. Toyota, and R. Koga, "Convergence acceleration and accuracy improvement in power bus impedance calculation with a fast algorithm using cavity modes," *IEEE Trans. Electromag. Compat.*, vol. 47, no. 1, pp. 2-9, Feb. 2005.
- [9] M. Xu, T. H. Hubing, "The development of a closed-form expression for the input impedance of power-return plane structures," *IEEE Trans. Electromagn. Compat.*, vol. 45, pp. 478-485, 2003.
- [10] C. Guo, T. H. Hubing, "Circuit models of power bus structures on printed circuit boards using hybrid FEM-SPICE method," *IEEE Trans. Adv. Packaging.*, vol. 25, no 3, pp. 441-447, Aug 2006.
- [11] W. Shi, and J. Fang, "New efficient method of modeling electronics packages with layered power/ground planes," *IEEE Trans. Adv. Packag.*, vol. 25, no. 3, pp. 417-423, Aug. 2002.

- [12] T. -K. Wang, S.-T. Chen, C.-W. Tsai, S.-M. Wu, J. L. Drewniak, and T.-L. Wu, "Modeling noise coupling between package and PCB power/ground planes with an efficient 2-D FDTD/lumped element method," *IEEE Trans. Adv. Packag.*, vol. 30, no. 4, pp. 864-871, Nov.2007.
- [13] A.E. Engin, K. Bharath, and M. Swaminathan, "Multilayered finite -difference method (MFDM) for modeling of package and printed circuit board planes," *IEEE Trans. Electromagn. Compat.*, vol. 49, no. 2, pp. 441-447, May 2007.
- [14] C. Wang, J. Mao, G. Selli, S. Luan, L. Zhang, J. Fan, D. J. Pommerenke, R. E. DuBroff, and J. L. Drewniak, "An efficient approach for power delivery network design with closed-form expressions for parasitic interconnect inductances," *IEEE Transactions on Advanced Packaging*, Vol. 29, No. 2, pp. 320-334, May 2006.
- [15] Yaojiang Zhang, Arun Reddy Chada, Jun Fan, James L. Drewniak, "A concise Multiple Scattering method for Via Array Analysis in a circular plate pair," submitted to *IEEE EDAPS 2008 SYMPOSIUM*, December 2008.
- [16] Y. Zhang, G. Feng, J. Fan, "Radial Waveguide Interpretation of the Impedance of Power/Ground Planes and its Evaluation by Boundary Integral Method," *IEEE Trans. Microwave Theory Tech.*, submitted, 2008.
- [17] Marina Y. Koledintseva, "Part 2: Composite Materials for RF & Microwave Applications and Mixing Rules for Effective Constitutive Parameters," EE-474 Class Material, Missouri University of Science and Technology, 2009.

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