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Cable discharge events (CDE) -- A modeling and simulation perspective

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CABLE DISCHARGE EVENTS (CDE) - A MODELING AND SIMULATION PERSPECTIVE

by

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ABSTRACT

Cable discharge events (CDE) typically occur when a charged cable is connected to an electronic device. Several CDE damages in Ethernet LAN and USB communication interface equipment are reported by the IC manufacturers. CDE differs from other types of ESD such as human body model (HBM), charged device model (CDM) and IEC 61000-4-2 mainly due to faster rise times, longer pulse widths and higher peak currents. Various factors such as cable geometries, charging and discharging mechanisms, and load conditions influence CDE. Several researchers have developed some measurement techniques to understand CDE waveforms. However, there is little information regarding its modeling and simulation.

This study mainly focuses on developing simulation models for Cable Discharge Events (CDE) in general and specific to Ethernet LAN interfaces. An overview of some of the most relevant publications is provided at first, to understand the current state-of-the-art. Further, the factors that influence CDE are explained in detail. Next, various CDE modeling and simulation approaches are compared and two modeling techniques to simulate some of the most important aspects of CDE are proposed. The first method mainly deals with the estimation of voltages on conductors during charging and discharging. The second method, a hybrid modeling technique, aims at simulating the CDE of an unshielded twisted pair (UTP) with reasonable accuracy and simulation time. The details of a simple CDE tester that was developed to validate the simulation model are explained. Several factors that affect CDE such as cable length, cable's height above a ground plane, discharge sequencing, presence of a vertical discharge plane etc. are analyzed using the proposed simulation techniques. At the end, all major simulation results are discussed and the scope of future work is also mentioned.

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1. INTRODUCTION

It is well known that the electrostatic discharge (ESD) events are a major concern for the electronic systems. The protection strategies against ESD are mainly developed based on the type of ESD source, the discharge mechanism and the likelihood of its occurrence. An IC located internal to an electronics system is at a lesser risk to an ESD event when compared to an IC having an interface that is exposed to the external world. For example, Ethernet Physical Layer (PHY) transceivers may be subjected to a significantly different type of ESD called as a cable discharge event (CDE) when compared to the human body discharges that an IC that is connected to say, an LCD, may experience. Presently, the semiconductor industry has standard methodologies for testing the durability of a device or system to transient conditions. The standard tests for ESD are the human body model (HBM), machine model (MM), charged device model (CDM) and the system level IEC 61000-4-2. Over the past few years researchers have understood that CDE needs to be treated separately from other types of ESD tests due to vast differences between the effects caused by CDE. Some of the important differences are listed in Table 1.1.

However, no standard CDE tests for semiconductor devices or for equipment in the field exist and complying with the system level IEC 61000-4-2 standard may not ensure complete robustness of a device or a system against CDE. Several semiconductor manufacturers dealing with the communication interfaces have developed their own in-house CDE testers to qualify their ICs. Therefore, the need for standardizing the test procedure is ever growing.

One of the reasons why it is not trivial to develop a standard methodology is that there are many parameters that influence CDE such as the cable geometry, the charging and discharging mechanisms, the pin mating sequence, and the load conditions. Previous publications provide basic understanding of the cable discharges both from theoretical and measurement's point of view [3] to [5], [9] to [11]. However, there is a lot more to learn about the effects of CDE under different conditions. For example, CDE from a 1 m unshielded twisted pair (UTP) might be very different from that of a 100 m shielded

twisted pair (STP). Although all these parameter influences could be investigated experimentally the large number of combinations, and the desire to design ESD protection beforehand using simulation lead to the desire of having a simulation model. This study compares and contrasts several CDE modeling techniques and proposes a few methods to model some of the most important parameters that influence CDE. The first one is a simplified equivalent capacitive modeling approach which aims at estimating the voltages on the conductors during charging and discharging for different cable geometries. The details of the creation of an Ethernet LAN cable cross section in ANSYS Q2D, extracting the per unit length (p.u.l) capacitance matrix, incorporating the effect of cable twisting, generating a SPICE netlist file, simulating in ADS are presented in this section. The effect of ESD capacitor (1 nF 2kV) in the sequential discharges of short and long cables is analyzed using this method. Next, a new hybrid modeling technique combing the strengths of 2D transmission line theory, 3D modeling and SPICE solver is presented. A detailed description of the creation of the simulation models in CST cable studio, the extraction of s-parameter model and the SPICE simulation using ADS is provided. A detailed explanation of the creation of the simulation models, verification and analysis of the simulation results is presented. A simple CDE tester PCB has been developed to validate the simulation models.

Table 1.1. Comparison between different ESD types

Parameter	**HBM**	**CDM**	**IEC 61000-4-2**	**CDE**
Rise time	2 to 10 ns	100 to 500 ps	~ 0.8 ns	100 to 300ps
Pulse duration	150 ns	~ 2 ns	~ 80 ns	up to several milliseconds (depends on the cable length)
Peak current	0.7A/kV	1- 16A (depends on the size of IC)	3.75 A/kV	**Peak: ~5A/kV** **Plateau: ~3A/kV**

2. OVERVIEW OF EXISTING CDE KNOWLEDGE

Several researchers have already investigated different aspects of CDE. An overview of some of the most relevant literature is presented in this section. This helps in understanding the state of the art and also the motivation for this study.

In [1], several LAN CDE damages are reported. The need for distinguishing CDE from other ESD types is stressed. Cable charging up as a function of time and length is shown. Several CDE waveforms on the Ethernet PHY are measured and the threats posed by the high energy of CDE pulses are highlighted. Protection strategies from a board level designer's perspective such as the usage of magnetics with integrated TVS diodes, the usage of transformer circuits to suppress common-mode transients are discussed. Connecting an ESD capacitor (2 kV rating) from the line side center-tap to chassis ground is recommended. Since the time when [1] was published there have been several other publications that focused on understanding the CDE waveforms better. In [2], the origin of different parts of a CDE discharge current waveform such as the initial peak, plateau and pulse length is analyzed. The current peak and the plateau are quantified to be about 5A/ kV and 2 A/ kV respectively for simple cables placed 10cm above a ground plane. Since CDE highly depends on the cable type and geometry, the results presented in [2] can't be directly applied to the long twisted pair cables such as LAN CAT 5 UTP cables.

In [3] and [4], several CDE basics such as charging and discharging mechanisms are introduced. Surface charges due to the triboelectric effect, charge migration in dielectrics, net charge on the center conductor due to ESD are discussed. In [3], the effects of pin mating sequence on causing a common and/or a differential mode discharge are discussed. In [4], CDE is compared and contrasted with the IEC 61000-4-2. A simplified SPICE model to simulate CDE is shown where the cable is modeled using a transmission line whose parameters are obtained using measurements. However, the SPICE circuit models a single cable above ground plane and cannot be directly used to model the twisted pair cables.

In [5] and [6] CDE testers which help in making several repeatable measurements of CDE discharge current waveforms are developed. A CDE tester consists of a PCB that

has an incoming LAN cable attached on one end and an Ethernet device such as PHY chip is connected on the other end. The PCB has the ability to control the charging and discharging of each conductor of the connected LAN cable using high voltage relays. [5] Mainly deals with the impact of CDE on the magnetics of the Ethernet front end while. Several CDE waveforms are shown in this publication which emphasizes the threat posed by the differential discharge that may pass through the front end magnetics.

CDE stress on the interior lines of shielded cables is discussed in [7]. When the cable shield first contacts the ground of the device a spark occurs causing current to flow between the shield and the ground. The resultant W-shaped pulse on the interior cables due to magnetic coupling is analyzed. The coupling ratio between the shield current and the interior line current is estimated to be 1.3 % and therefore this scenario may not be very dangerous to the attached electronics.

A simple theoretical model to simulate CDE using a three body model represented using Maxwell's multi-body capacitance method is presented in [9]. The surface charges on the jacket of the cable are experimentally quantified. Several cable characteristics including length, surface charge density due to tribo-electrification and mode of termination are studied. Peak currents, discharge time constants and energies are theoretically calculated.

Although the CDE parameter influences could be investigated using some of the measurement techniques presented in previous publications, the large number of combinations, and the desire to design ESD protection beforehand using simulation requires the need for developing models to simulate CDE. However, very little information is available on modeling and simulating LAN CDE. In [10], a W-element model is obtained for a single UTP and it is used in SPICE to simulate the CDE voltages on the front end magnetics of a PHY circuit. Since this method models a single pair, it cannot simulate the effect of pair to pair coupling, the effect of discharge sequencing of different conductors. In [10], it is mentioned that more accurate models need to be developed to better simulate the CDE discharge waveforms. Also, the conventional 2D approach cannot model the initial peak of the discharge current waveform. Therefore, all these factors motivated the authors of this study to develop comprehensive simulation models to simulate many important parameters of CDE.

3. FACTORS THAT INFLUENCE CDE

There are several factors that influence the CDE discharges. It's convenient to group those factors based on the kind of influence they have on the CDE. One common parameter that is used to characterize CDE is its discharge current waveform which can be defined as

$$I_{CDE} = \frac{V_{charge}}{(Z_{cable}+Z_{load})} \quad (1)$$

Figure 3.1 shows a list of factors that affect one or more of the three parameters in the right hand side of equation (1).

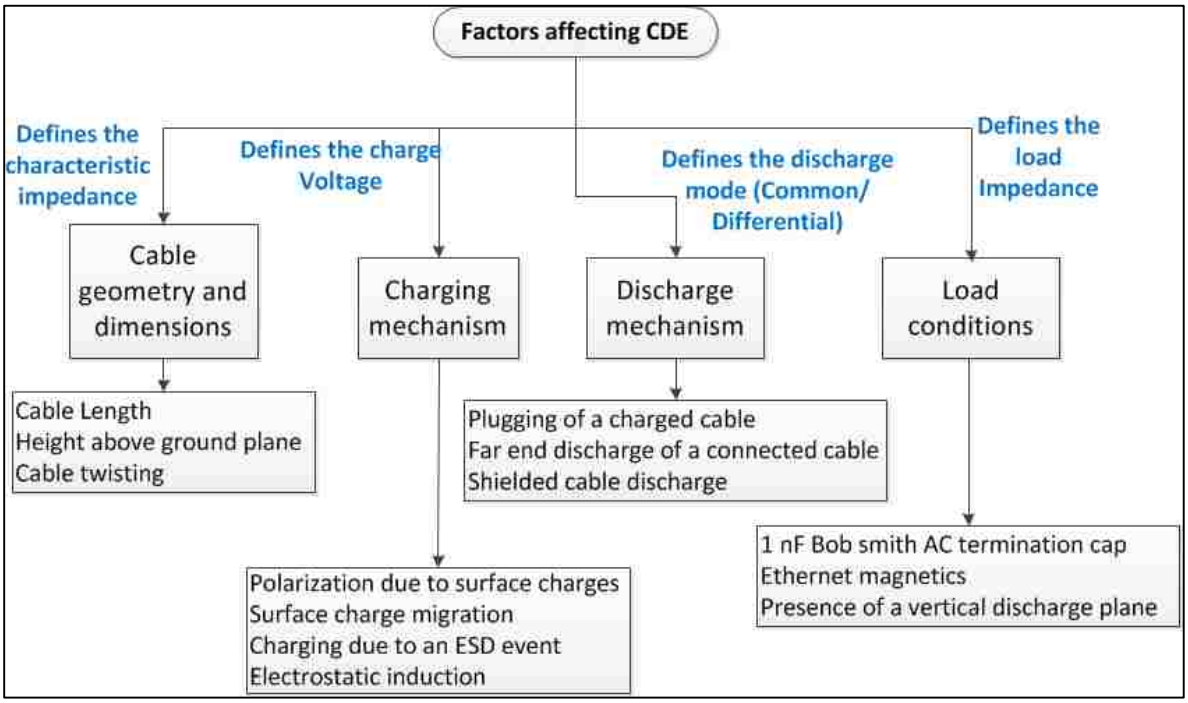

Figure 3.1. List of parameters that affect CDE

3.1. CABLE GEOMETRY AND DIMENSIONS

3.1.1. Height of the Cable Above Ground Plane. The capacitance of a wire above ground can be defined as

$$c = \frac{2\pi\varepsilon}{cosh^{-1}(\frac{h}{r})} * l_{wire} \quad \text{(F)} \quad (2)$$

For h>> r, $$c = \frac{2\pi\varepsilon}{log(\frac{2h}{r})} * l_{wire} \quad \text{(F)} \quad (3)$$

Where ‘h’ is the cable height above an infinite ground plane, ‘r’ is the wire radius and ‘l’ is wire length, all expressed in meters.

As per equations (2) and (3), the cable capacitance varies inversely with its height above ground plane. Therefore, a charged cable that is placed directly above ground plane may result in a higher discharge current when compared to that from a cable that is placed high above the ground.

3.1.2. Cable Length. A cable's capacitance to ground determines how much charge it will hold. Once the cable is charged, its capacitance to ground and the relative humidity typically determine how fast the charge will dissipate [16]. Cable capacitance is directly proportional to the length of the cable. Therefore, a longer cable can accumulate more charges and retain them for a longer time than a shorter cable. Also, the pulse length of the discharge current can be defined as

$$t_{pulse} = \frac{2*l_{wire}*\sqrt{\varepsilon_r}}{c} \quad (4)$$

Therefore, the longer the cable, the longer are the pulse length of the discharge current and the energy of the pulse.

3.1.3. Cable Twisting. Typically in Ethernet communication interfaces, the cable pairs are twisted to reduce signal crosstalk. Cable twisting may affect CDE in two ways.

- Capacitance of individual conductors:

  The cross section of a typical CAT 5 UTP cable is shown in the Figure 3.2. The capacitance of each conductor to ground and to other conductors is dependent on the height and the distance between each conductor. Cable twisting affects the capacitance and therefore it is important to analyze the effect of twisting on the discharge current waveform.

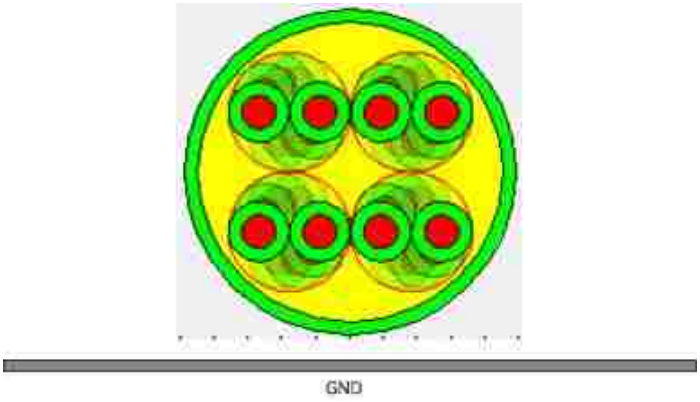

Figure 3.2. Cross section of a 4 pair twisted pair cable

- Inter pair coupling:

  When a charged cable is plugged into a LAN connector, not all pins mate at the same time. Therefore, a random pin mates first causing a current to flow through that conductor. This current may couple to the other pairs. The amount of coupling reduces if the cable pairs are twisted. Therefore, cable twisting needs to be considered for CDE investigations

3.2. CABLE CHARGING MECHANISMS

3.2.1. Polarization Due to Surface Charges. When a cable is dragged along the floor, the jacket of the cable may get charged due to tribo-electric effect. The surface charges polarize the conductors thus causing charge redistribution and therefore, positive charges are formed at the ends of the twisted pair as shown in the Figure 3.3. If the conductors were electrically neutral to begin with, they will remain neutral and hence will have no net charges. However, when the conductors come in contact with a directly or capacitive grounded connector there will be arcing which will charge the twisted pair and hence there is a current flowing between the cable and the connector. [4]

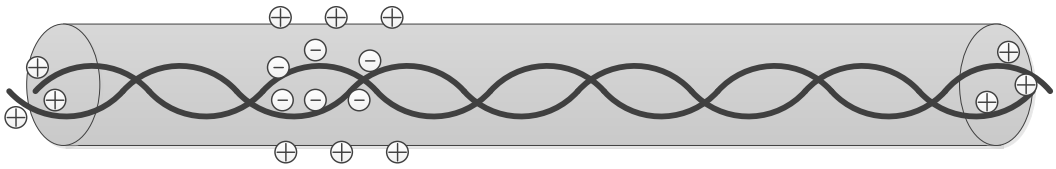

Figure 3.3. Charge separation on the twisted pair due to tribo charges on the jacket

In [9], the average surface charge density on a short cable was experimentally found out by pulling it through an inline triboelectrification charger consisting of a sleeve fabricated from PTFE and aluminum to provide a friction against the cable jacket. The surface charge was measured using an electrometer. Following are the average surface charge densities on the cable jacket for both the charging sleeve materials

For PTFE charging sleeve, $\sigma = 0.1 * 10^{-8}$ C.cm^{-2}

For aluminum charging sleeve, $\sigma = -0.15 * 10^{-8}$ C.cm^{-2}

[9] also establishes a relationship between the average surface charge density, cable length and the load impedance, discharge current peak($I_{CDE\text{-}peak}$) and the time constant (τ).

The major findings are as follows:

1. For conductors directly grounded, i.e. $Z_{load} = 0$,

- I_{CDE_peak} is directly proportional to the cable jacket surface charge density (σ)
- I_{CDE_peak} is inversely proportional to the cable length (for a constant σ)

- τ is proportional to the square of the cable length

2. For conductors grounded through a finite load impedance to ground ,i.e. Z_{load} is finite

- I_{CDE_peak} is proportional to the cable jacket surface charge density
- I_{CDE_peak} is inversely proportional to Z_{load}
- τ is proportional to the cable length

In another study a similar experiment has been performed where a spooled CAT 6 cable is unwounded over flooring materials like HPL and the voltage on the inner conductor is measured to be about 1.1 kV maximum as shown in Figure 3.4 and Figure **3.5**.

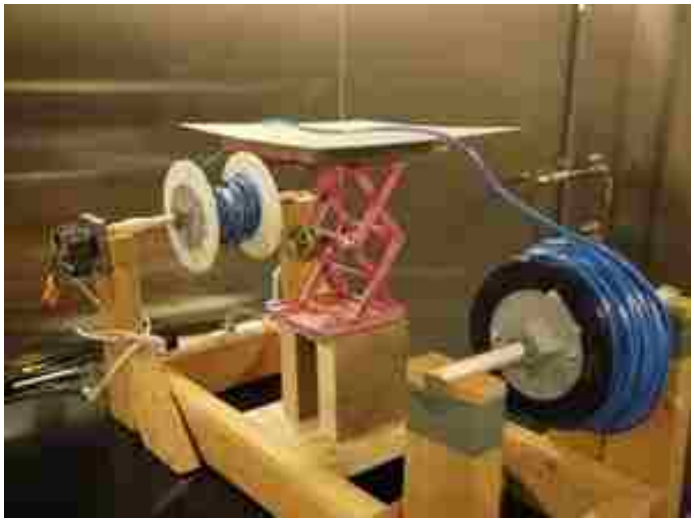

Figure 3.4. CAT 6 Cable Unwind Test Set up

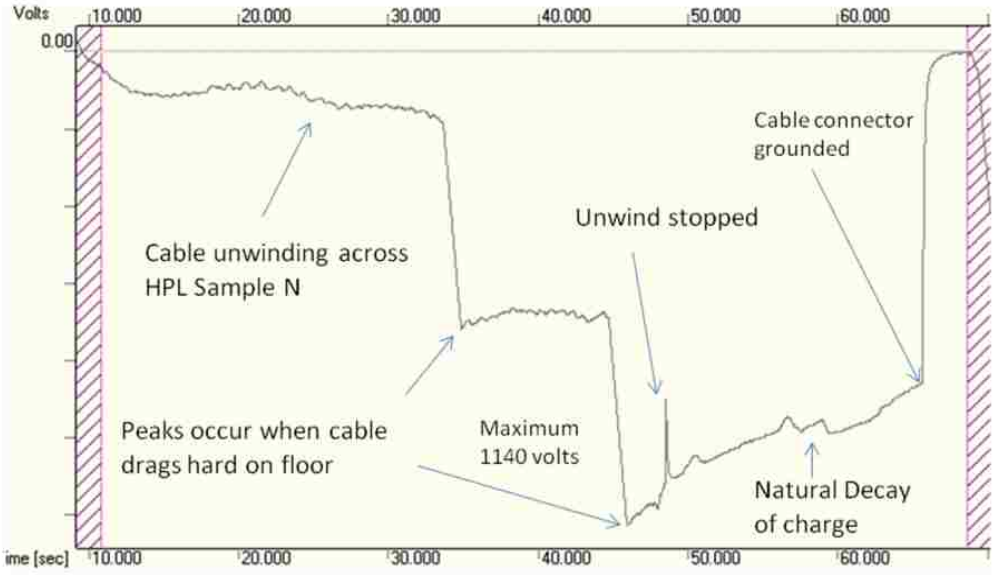

Figure 3.5. Voltage on the inner conductor of a CAT 6 cable during unwinding across HPL Sample

3.2.2. Surface Charge Migration. In this scenario again, a cable dielectric charged due to triboelectrification is considered. However, this mechanism considers the migration of the charges through the insulation layer. Therefore, a net charge is present on the inner conductors unlike in the previous case.

3.2.3. Charged Cable Due to An ESD Event. A charged worker handling a cable may leave the cable charged. In this scenario, the conductors have a net charge and will remain charged for several hours or until the cable is grounded. The charge retention depends on the cable capacitance and the humidity. An increase in humidity changes the air dielectric property between the cable and the ground so that the capacitance is reduced. From [5], the charge retention of an automotive wiring harness under laboratory conditions is shown in the Figure 3.6. Therefore, in low humidity conditions, a charged cable can pose significant threat even hours after it's charged.

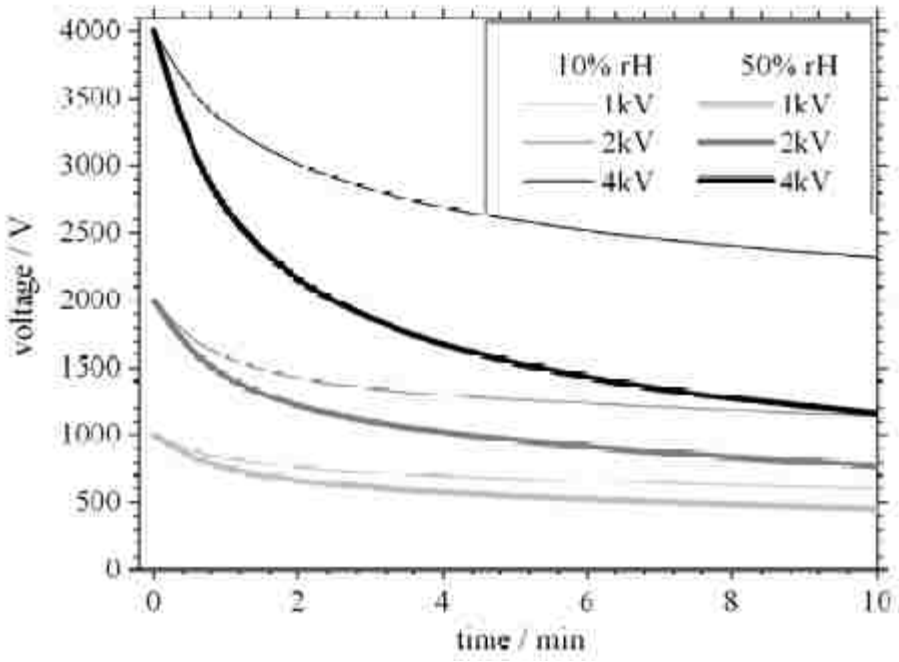

Figure 3.6. Discharge example of an isolated automotive wiring harness under laboratory conditions

3.2.4. Induction. If a cable is subjected to the electromagnetic field of a strong pulse (e.g., lighting ballast, strong switching transitions on a cable close by, ESD close to the cable) a momentary voltage will be introduced along the cable. This can be treated as the electromagnetic induction. Therefore, it may not be a problem as long as the cable is not connected to any network equipment. [4]

Another type of induction could be an electrostatic induction. For example, if a cable is placed under a strong electrostatic field, it will accumulate some charge carriers on its surface. While some of them may migrate, the other surface charge carriers polarize the conductors. When the external field is removed, the charge carriers which had partners will lose their partners thus causing the voltage to increase at the end of the cable. [4]

3.3. CABLE DISCHARGING MECHANISMS

3.3.1. A Charged UTP Cable inserted into a LAN Connector. In real world CDE events, when a charged CAT 5 UTP cable is plugged into a LAN connector, not all pins make contact at the same time. If the cable is charged in common mode, i.e., all 8 conductors have the same potential with respect to a reference plane, the first pin that contacts initiates a current flowing between that conductor and the LAN connector. This can be considered to be as a common mode discharge. At least two different modes can be initiated by the second pin that mates. The second pin can either be from the same twisted pair, or from another twisted pair. If it is from the same pair, a differential mode current will be initiated.

However, the sequencing may be less significant in the case of the CDE of very long cables (above 100 m) if the front ends magnetics has a high voltage 1 nF ESD capacitor as shown in the Figure 3.7. This is because the first discharge may charge up the capacitor hence limiting the current due to the subsequent discharges. For short cables, sequencing plays an important role.

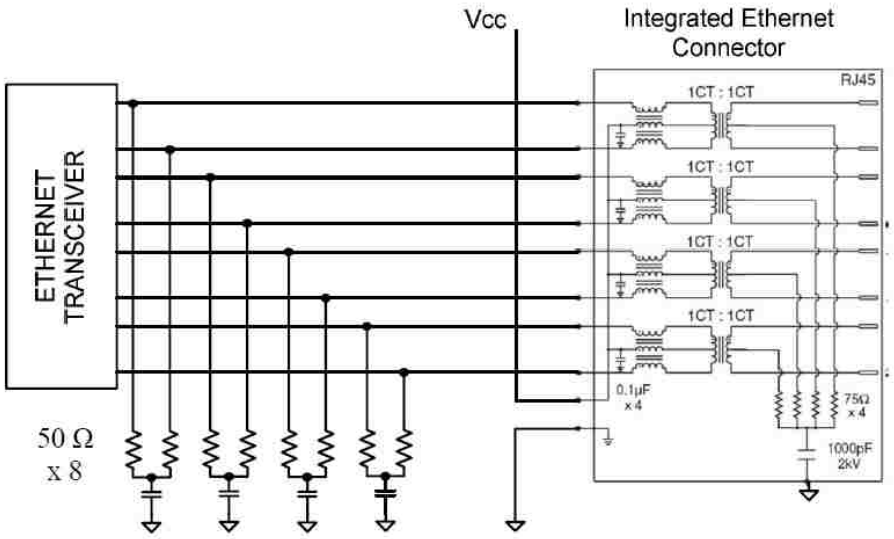

Figure 3.7 Simplified Ethernet port with a Bob Smith AC termination

3.3.2. Far End Discharge Event. In this case, the LAN cable is assumed to be attached to grounded network equipment on one end (a router for example). The near end

is connected to a non-grounded device such as a battery operated laptop as shown in the Figure 3.8. A human ESD event on the laptop may cause a pulse that may travel on the conductors of the LAN cable. Since the cable is connected between two Ethernet ports, either ends of the cable have the 1 nF Bob Smith termination that is shown in Figure 3.7. Therefore, the voltage that can develop across both 1 nF ESD protection capacitors can be roughly estimated using (5)

$$V_{load} = \left(\frac{C_{ESD}+C_{laptop}}{C_{load}}\right) * V_{ESD} \quad (5)$$

- Assume a human body ESD occurs and V_{ESD} ~ 10kV
- Capacitance of the human body, C_{ESD} ~ 150 pF
- Capacitance of the laptop and cable to ground C_{cable} ~ 50 pF
- Load side capacitance (ESD capacitor on the router front end) C_{load} ~ 2 nF.

So, for a 10 kV human ESD event, the two 1 nF capacitors in parallel on either ends of the cable may get charged to ~ 1 kV. The 1 nF ESD capacitor at the front end of the router is typically rated for up to 2 kV, therefore the voltage due to this CDE mechanism doesn't exceed the isolation voltage criteria.

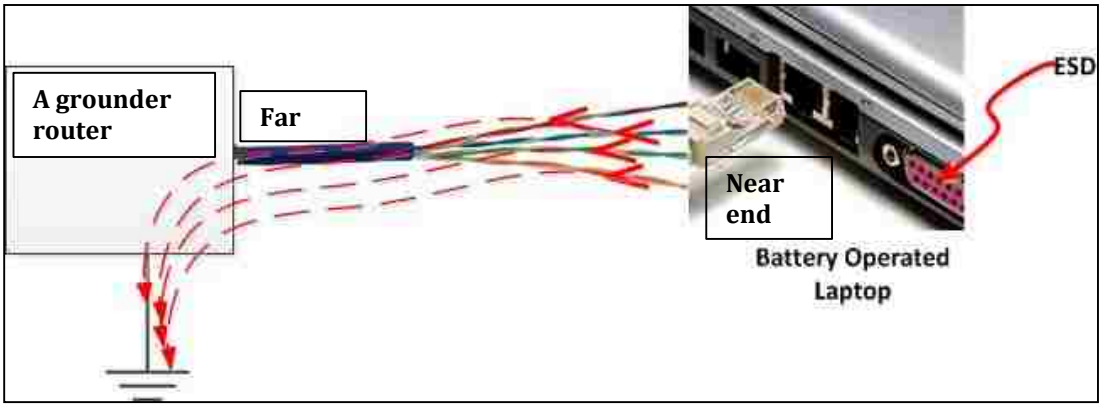

Figure 3.8. Far end discharge causing a common mode current on the LAN cable

Since the cable is already connected, the pulse may travel on all the conductors in a common mode. The front of Ethernet port contains an isolation transformer as shown in the Figure 3.7. So, the transformer doesn't allow the common mode to cause any induced

voltage on its secondary side. This is explained using a single pair of an Ethernet port in Figure 3.9

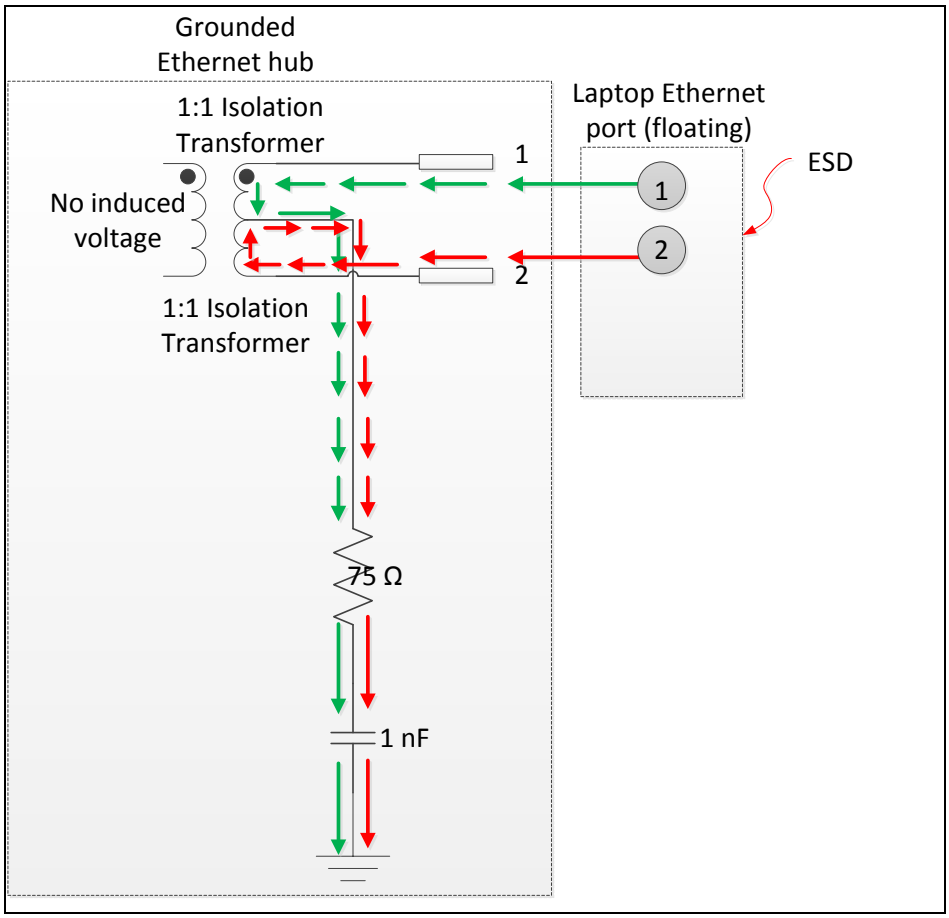

Figure 3.9. Single pair on an Ethernet pair showing common mode discharge current

3.3.3. Shielded Cable Discharge. In a shielded twisted pair (STP) cable, each twisted pair is shielded using an aluminum foil. The shields are internally connected to the shell of the connector as shown in the Figure 3.10.

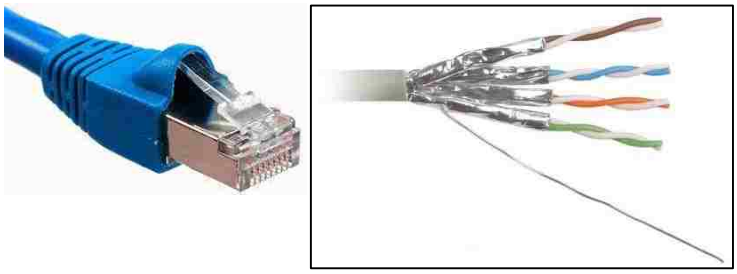

Figure 3.10. Images of a CAT 6 Shielded twisted pair cable (STP)

When a charged STP cable is plugged into a grounded Ethernet port, discharge current flows from the shield to the ground of the connector. However, this current flowing through the shield causes magnetic coupling to the inner conductors which may in turn cause some current flow between the conductors and the PHY electronics. In [8], shielded cable discharges are explained in detail. The major conclusion of [8] is that a shielded cable with a ground shell significantly reduces the impact of CDE. In cases where the cable has a foil shield, the magnetic coupling is extremely low and hence the induced voltages are very low. For cables with braided shields, the transfer impedance may be higher [17] and hence the impact of CDE may need to be evaluated in such cases.

3.3.4. Discussion. Several discharge mechanisms are presented in the above section 3.3.1, section 3.3.2, section 3.3.3. Based on the simplified Ethernet port's electronic circuit shown in the Figure 3.7, the discharge mechanism that may cause the most damage is when a charged UTP cable is plugged into a LAN connector (section 3.3.1). Therefore, this discharge mechanism is analyzed in detail in this study.

3.4. LOADING CONDITIONS

3.4.1. ESD Protection Capacitor. Load impedance to ground is one of the main factors that decide the discharge current's magnitude. The possibility of occurrence of a certain mode of discharge can also be determined based on the load termination structure. For example, Figure 3.7 shows the simplified Ethernet port connector's schematic. It can be seen that each pair has a 75 Ω termination resistance and all the pairs are grounded capacitively using a 1 nF, 2 kV ESD protection capacitor. The effect of this

capacitor on the CDE discharge current waveform for short and long cables is analyzed in detail in this study.

3.4.2. Presence of a Vertical Discharge Plane. The presence of a vertical plane at the discharge end of a CDE may cause an initial peak in the discharge current waveform [2]. For example consider a charged Ethernet cable is being plugged into a LAN port that has a metallic enclosure. Moments before the connection is made, a significant capacitance may be formed between the front portion of the cable and the metallic enclosure that may result in a fast rising initial peak. This effect is modeled and simulated in this study.

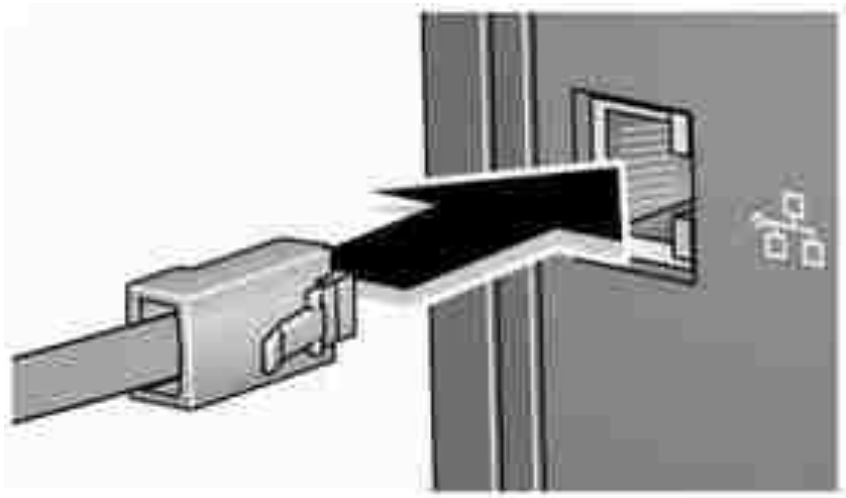

Figure 3.11. Image of an Ethernet cable being plugged into a LAN connector having a metallic enclosure

4. CDE MODELING TECHNIQUES

In this section several modeling techniques are compared first, and then, two modeling techniques that simulate many important CDE factors are explained in detail.

4.1. COMPARISON OF MODELING TECHNIQUES.

A list of CDE modeling techniques is shown in Figure 4.1. The advantages and disadvantages of each method are discussed in detail in this section. Table 4.1 shows a list of important CDE factors that need to be modeled based on section 3. The modeling capabilities of each simulation method are also indicated.

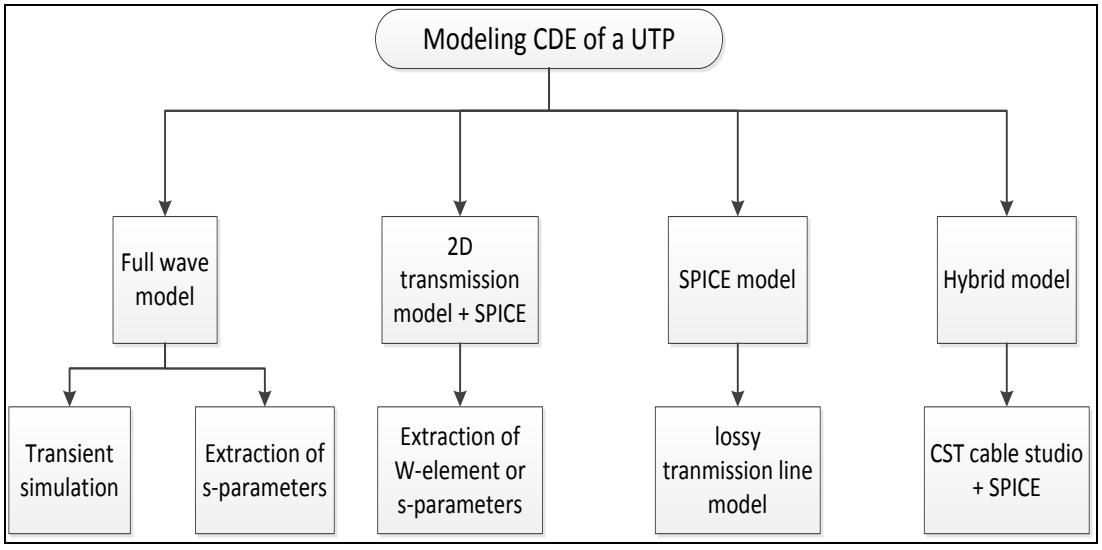

Figure 4.1. Comparison of CDE modeling techniques

Table 4.1. List of phenomena and the modeling capabilities of each simulation method

#	List of phenomena	Full wave transient analysis	Full wave + SPICE	2D transmission line + SPICE	SPICE	Hybrid model
1	Cable height variation	yes	yes	yes	yes	yes
2	Cable length variation	yes	yes	yes	yes	yes
3	Cable twisting	yes (complicated)	yes (complicated)	Possible(using averaging)	no	yes
4	Charging due to polarization	possible	possible	no	no	Possible but not implement ed
5	Surface charge migration	no	no	no	no	Possible but not implement ed
6	Charging due to an ESD event (modeled as the voltage on the inner conductors)	yes	yes	yes	yes	yes
7	Induction(model ed as the voltage on the inner conductors)	yes	yes	yes	yes	yes
8	Plugging of a charged cable (discharge sequence)	no	yes	yes	no	yes
9	Far end discharge	no	yes	no	no	Possible but implement ed
10	Shielded cable discharge	no	yes	yes	possible	Possible but implement ed
11	Ethernet magnetics with 1 nF capacitor	no	yes	yes	yes	Possible but but implement ed
12	Vertical discharge plane	yes	yes	yes	no	yes

4.1.1. Full Wave Modeling. Full wave modeling is the most fundamental way of simulated a twisted pair cable above ground plane geometry. List of phenomena that can be modeled using this method are shown in Table 4.1. In this section, the major problems associated with using the two possible simulation options for simulating CDE using a commercial 3D full wave solver like CST microwave studio are listed below.

4.1.1.1 Time domain solver and lumped ports.

- The smallest dimension of a UTP cable is the radius of conductors which is 0.25 mm and the largest is the cable length that could be in the range of several meters. Therefore, the number of mesh cells required to solve this geometry is very high and hence the simulation times are very long (several hours for each simulation).
- Any small change made to the geometry requires the entire full wave simulation to be run again.
- Charging a long cable (10 m long) using an excitation source takes about several milliseconds while its discharge is a transient phenomenon not lasting for more than several hundreds of nanoseconds. Therefore, simulating both charging and discharging will require very long simulation times.

4.1.1.2 Time / Frequency domain solver to obtain the s-parameters of the cable.

- Since an Ethernet cable has 8 conductors (referenced to a ground plane), the s-parameter model would have 16 ports to represent both ends of the cable. Therefore, this method may require very long simulation time too. However, one advantage of this method is that the s-parameter model can be used in SPICE to simulate both charging and discharging.
- Any change in the cable geometry requires re-calculation of all the s-parameters.

Therefore, using full wave solver is not a feasible method for modeling CDE.

4.1.2. 2D Transmission Line and SPICE. In this method, the UTP cable is simplified to be translationally invariant so that 2D transmission line theory can be applied and per unit length "RLGC" parameters are calculated.

The RLGC parameters can then be used to obtain W-element matrix or s-parameters to perform charging and discharging simulations in SPICE. Following are some of the advantages and disadvantages of using this method.

- The twisting of the cable can't be modeled by directly applying 2D transmission line theory.
- The presence of a vertical discharge plane is a 3D concept, so, it can be directly modeled using this approach. However, it can be approximately modeled by adding a lumped capacitance.
- One of the main advantages of this method is that the simulation time is very less. Calculating RLGC parameters of the cross section of a UTP requires less than minutes using any 2D cross sectional analysis too like FEMAS or ANSYS Q2D. The calculation of W-element matrix and importing it in SPICE and running transient simulations also doesn't take more than several minutes.

Even though this method has the least simulation time, due to the limited objectives it achieves, it may not be very useful. In section 4.2, a modified version of this approach to overcome a few shortcomings is explained in detail.

4.1.3. SPICE Modeling. In [5], a simple SPICE equivalent circuit of a cable above ground plane consisting of a lossy transmission line block is used. The parameters of the lossy transmission line block are entered based on the material properties and its characteristic impedance is experimentally found out. This approach is suitable only to get a basic understanding of a charged wire in general and it can't be extended for complicated cable geometry like a UTP above ground plane. Table 4.1 highlights the list of phenomena this approach can model.

4.1.4. Hybrid Modeling. A hybrid modeling technique that combines some of the strengths of all the simulation techniques discussed so far is proposed in this study. Following are the aspects that can be modeled in this technique:

- Charging mechanism: Charging the center conductors using voltage sources
- Discharging mechanism: Charged cable plugged into a LAN connector
- Cable geometry: Models the effects of varying the cable length, height above ground plane
- Discharge sequencing is analyzed
- Load impedance: Considers 1 Ω load resistance
- Vertical plane: Models the initial peak of the discharge current due to the vertical plane
- Twisted pairs are modeled accurately using CST Cable studio

4.1.5. Conclusions

- Due to excessively long simulation times, full wave method is not feasible to model CDE.
- SPICE modeling method is too simple to be applied to study cable geometries such as UTP above ground plane. It can be used to obtain a quick and basic understanding of the discharges of a charged wire.
- 2D transmission line + SPICE method may not be very useful if used directly since it can't model the effects of cable twisting. The importance of modeling the twisting is explained in section 3.1.3.

Considering the problems associated with some of the common modeling approaches, two new approaches that address some of the shortcomings are explained in the subsequent sections.

4.2. EQUIVALENT CAPACITANCE METHOD

4.2.1. Method. There are two main objectives of this approach

1. To estimate the voltages on the conductors of a UTP cable during charging and discharging as ratios of their self and mutual capacitances.
2. To estimate the voltage across the 1 nF ESD protection capacitor. See Figure 3.7

This method is a modified version of the approach presented in section 4.1.2.

From the p.u.l RLGC matrix that is obtained using a 2D cross sectional analysis tool, only p.u.l capacitance is used to estimate the voltages on the conductors.
It is important to note that this is not an equivalent representation of the cable. The simplification is done only to achieve a specific objective and this method cannot model the discharge currents, transmission line delays and transmission line losses.

Using the above mentioned simplifications, the capacitive equivalent circuit of a UTP cable is shown in Figure 4.2. In reality the orientation of the conductors inside the cable can be different due to the twisting of each pair and of the overall cable. The cross section shown in Figure 4.2 is taken from [13]

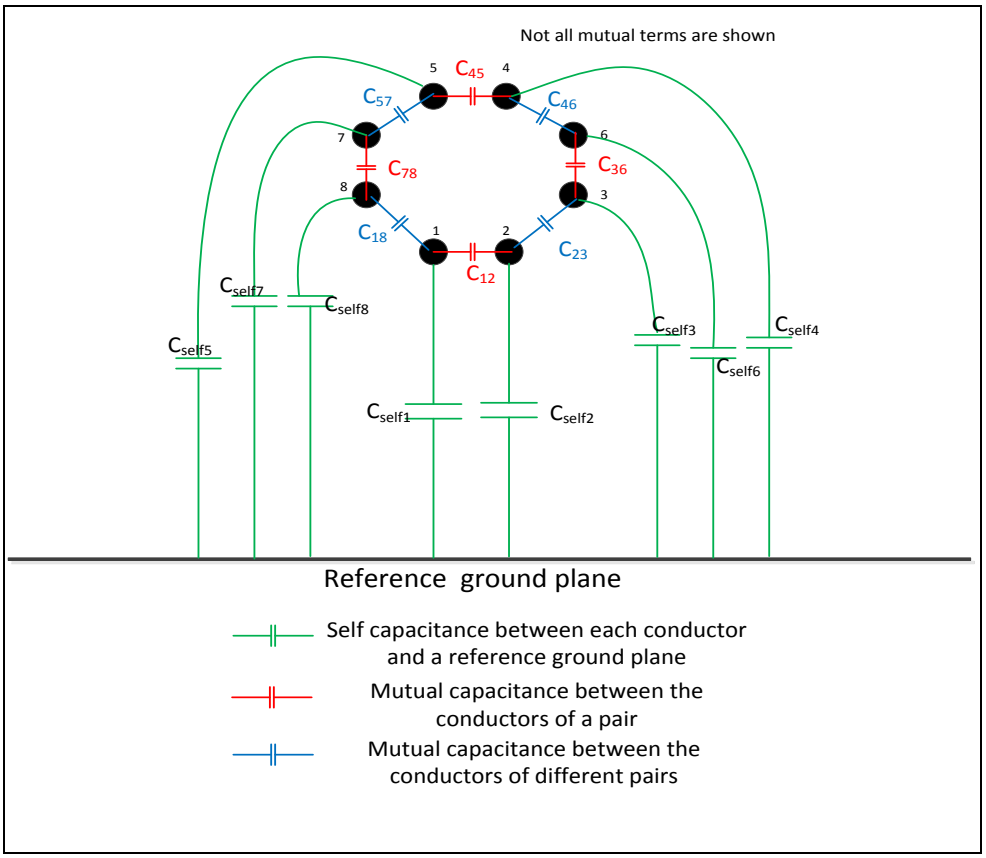

Figure 4.2. Simplified capacitive equivalent network model of a UTP cable above ground

4.2.2. Calculation of the Capacitance Matrix Using Q2D. Based on the cross section obtained from [13] a 2D cross section of a UTP cable is created in ANSYS Q2D [18] as shown in Figure 4.3.

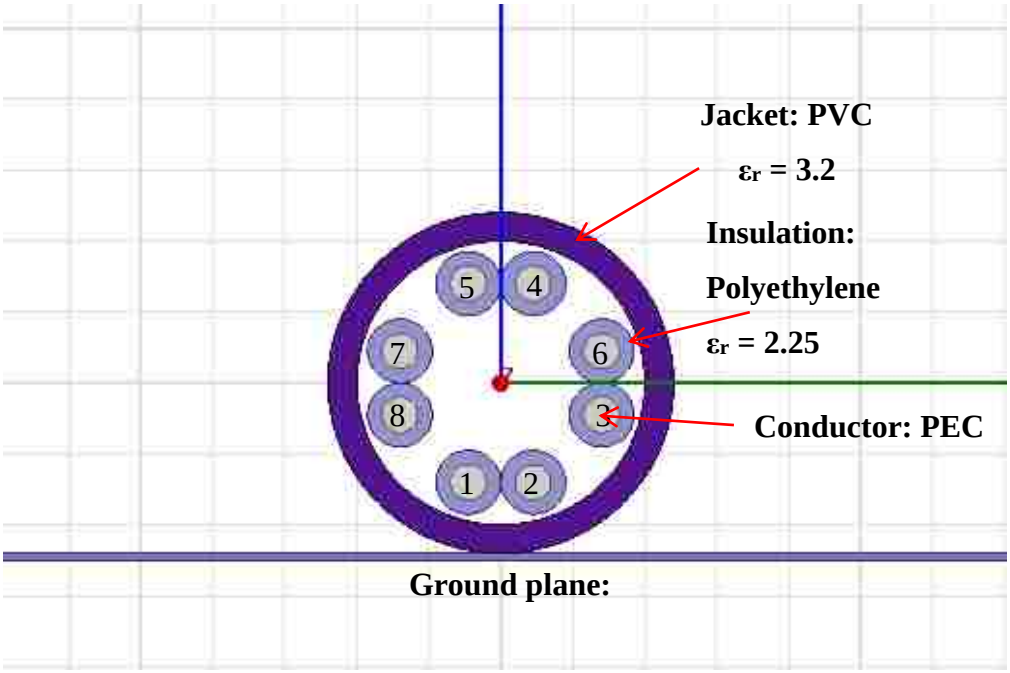

Figure 4.3. 2D cross section of a UTP cable created in ANSYS Q2D

4.2.3. Taking Wire and Cable Twisting Into Account. Section 3.1.3 explains the importance of modeling the cable twisting effects. In a typical CAT 5 UTP cable, the conductor pairs are twisted as shown in Table 4.2. In addition to the pair twisting, the whole cable bundle is also twisted, thought, at a much lesser twist rate when compared to the pair twisting. A simplified approach to model the effect of twisting is presented in the following sections.

Table 4.2. Cat 5 UTP details with twist rates

Pair	Pair color	[cm] per turn	Turns per [m]
1		Blue	64.8
2		Orange	56.2
3		Green	65.2
4		Brown	51.7

4.2.3.1 Twisting of cable pairs. The effect of twisting of individual wires can be approximately modeled as follows:

- Taking the average of the self-capacitance terms obtained from Q2D as shown in (6)

$$C_{11t} = C_{22t} = \frac{(C_{11} + C_{22})}{2} \quad (6)$$

- The mutual capacitance between the two conductors will not get affected since the distance between them remains the same. The mutual capacitance gives the characteristic impedance

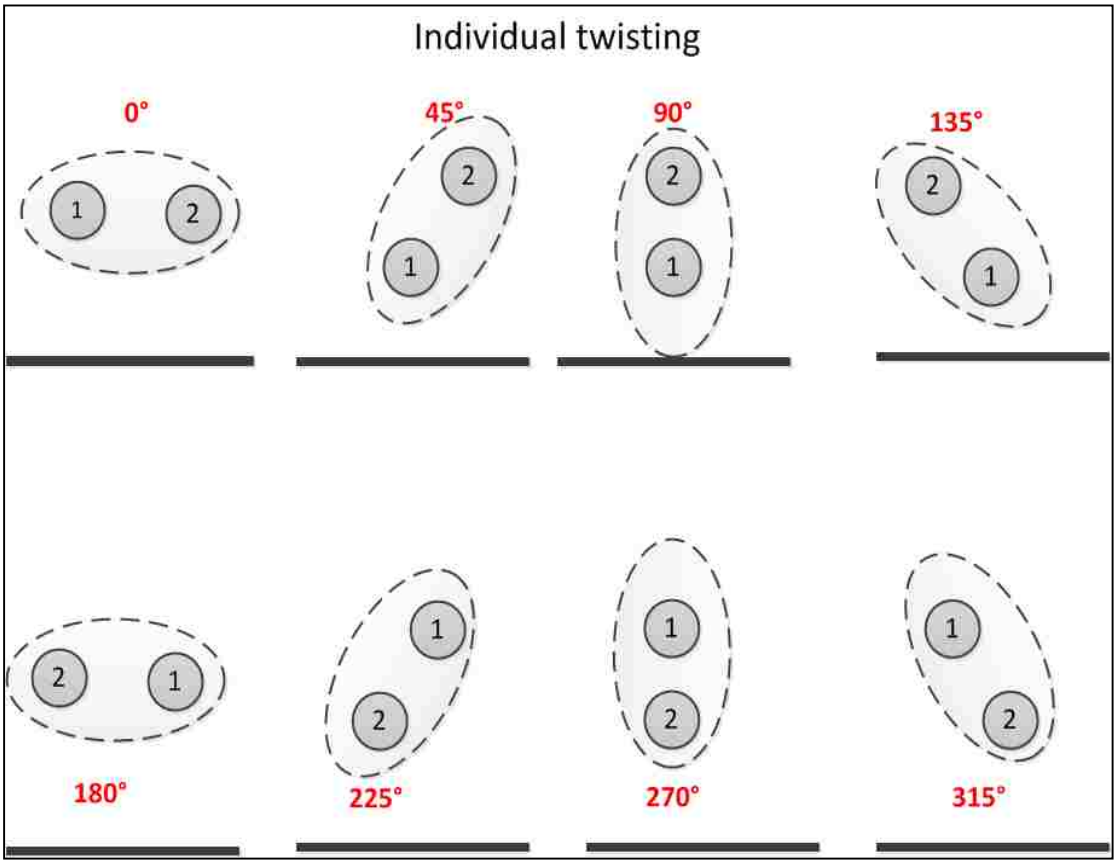

Figure 4.4. Several discretized cross sections of a twisted pair cable

4.2.3.2 Overall twisting. Overall twisting affects both self-capacitance terms and the mutual terms. The effect of twisting of individual wires can be approximately modeled as follows:

- The final self-capacitance terms are calculated using (7)

$$C_{xx\_final} = \sum_{x=1}^{8} \frac{C_{xxt}}{8} \quad (8)$$

Where C_{xxt} is the self-capacitance term with the individual twisting considered

- Similarly, the mutual terms are also averaged

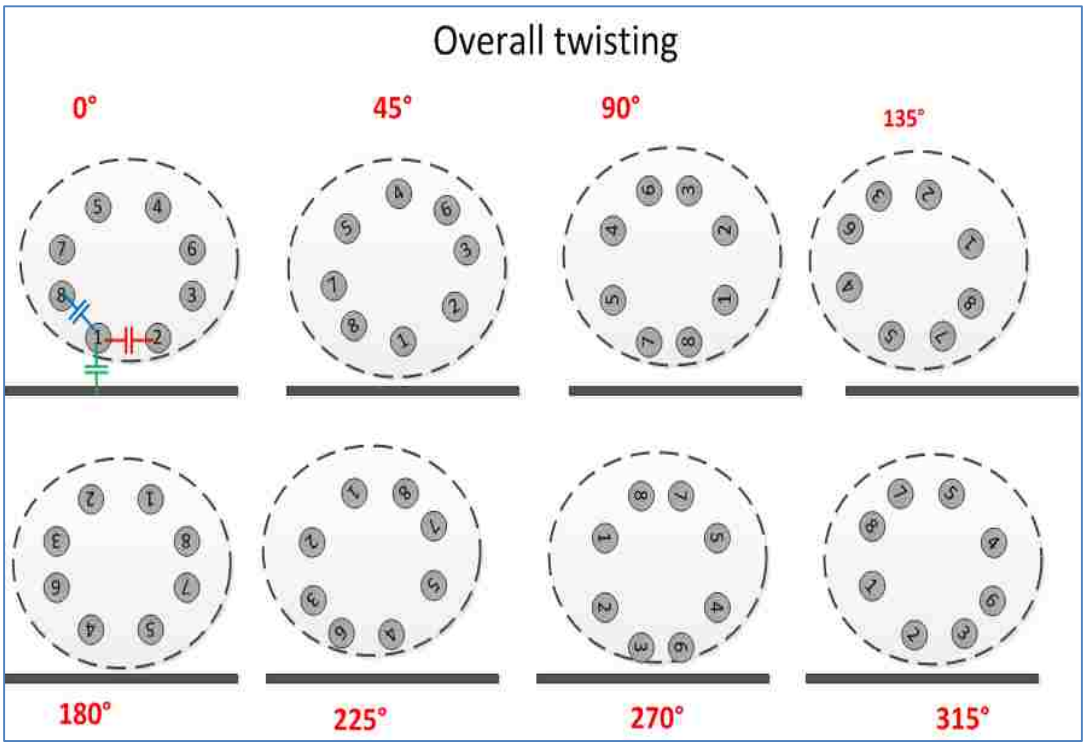

Figure 4.5. Several discretized cross sections of a UTP cable highlighting the overall twisting

4.2.3.3 UTP cable placed directly above ground plane. The capacitance matrix obtained from Q2D for a cable placed directly above ground plane is modified to incorporate twisting and the resultant capacitance matrix is shown in Figure 4.6

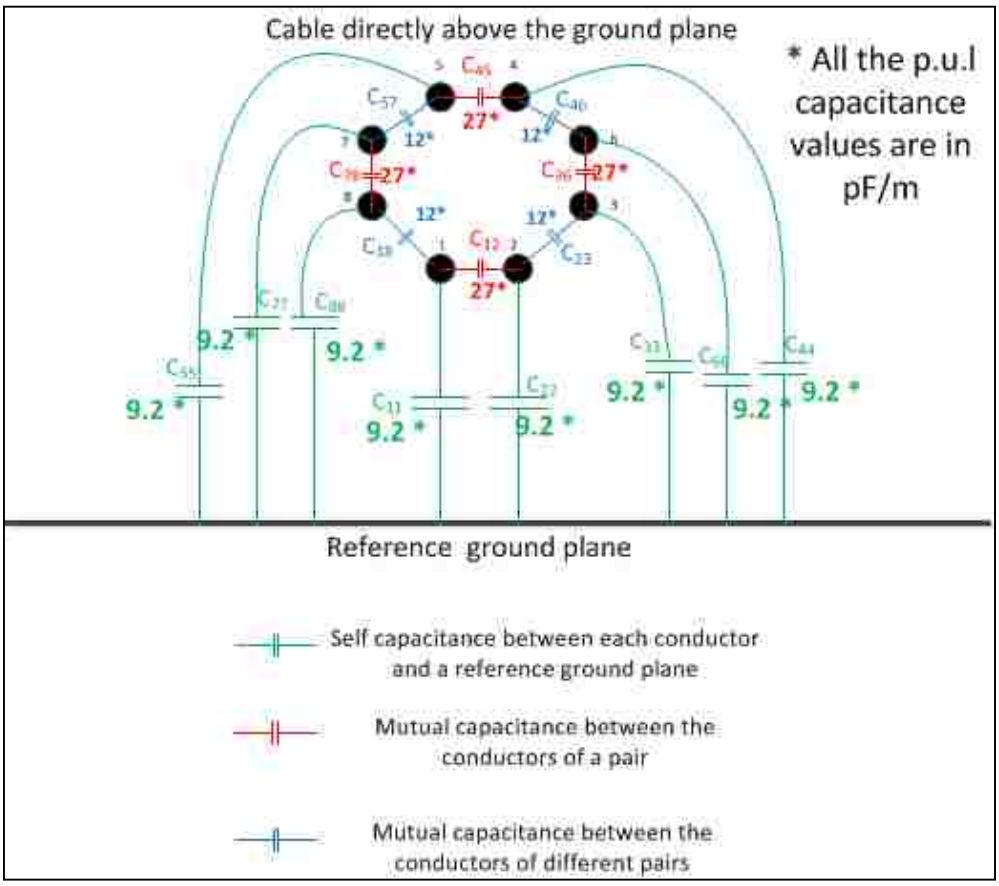

Figure 4.6. Equivalent capacitance model of a UTP cable placed directly above ground plane

- All the self-capacitance terms are equal due to overall twisting.
- Mutual capacitance between a pair is about 27 pF/m which is higher than the self-capacitance of 9 pF/m since the distance between a pair is lesser than the thickness of the insulator and the PVC jacket
- Not all the capacitances are shown in this figure such as C_{17}, C_{25} etc. however, they are used in the SPICE simulations

4.2.3.4 UTP cable placed 1m above ground plane. In this case the cable is placed directly above ground plane. Figure 4.6 shows the capacitance matrix that includes the effect of individual and overall twisting.

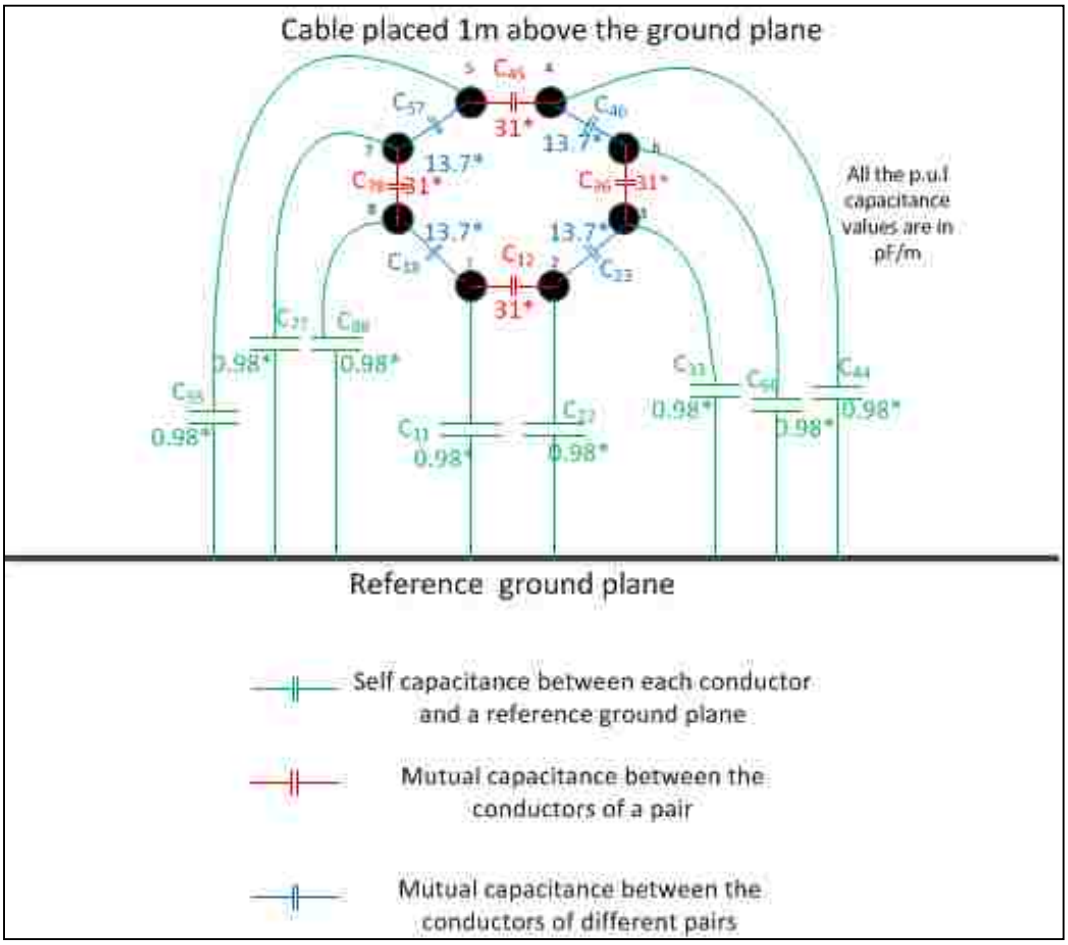

Figure 4.7. Equivalent capacitance model of a UTP cable placed 1 m above ground plane

- Since the cable is placed 1m above ground plane, the self-capacitance value is much lesser (1 pF/m) when compared to that of the cable placed directly above the ground plane (9 pF/m)
- Mutual capacitance between the conductors of a pair doesn't change much (31 pF/m). The increase in the height makes the mutual coupling slightly stronger.

- Not all the capacitances are shown in this figure such as C_{17}, C_{25} etc. however, they are used in the SPICE simulations

4.2.4. SPICE Simulation. Based on the capacitance matrix obtained from Q2D (after averaging to account for twisting) a SPICE simulation circuit is created in Agilent ADS to simulate charging and discharging as shown in Figure 4.8

- The circuit shown here can only model the voltages on the conductors during charging and discharge as a ratio of capacitances.
- It cannot model the transient phenomena, the discharge currents, the transmission line delays, the line losses etc.

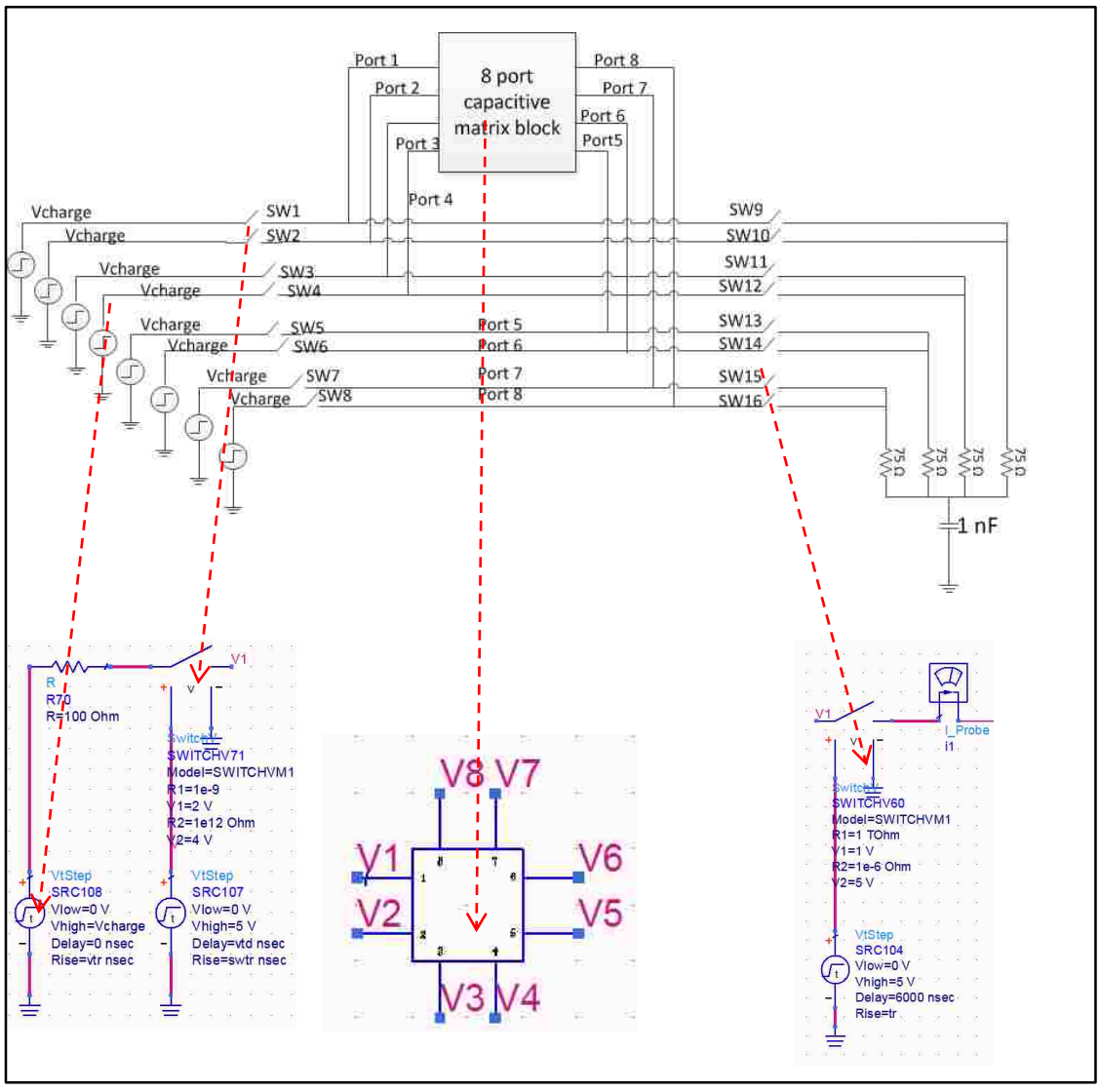

Figure 4.8. SPICE simulation scheme using the capacitive matrix obtained from Q2D

4.2.5. Simulation Results. Based on the cable geometry effects on CDE as discussed in section 3.1 two important simulation scenarios are shown in this section.

4.2.5.1 Simulating a 10 m cable discharge. The following steps are performed to simulate charging and discharging of a 10 m cable using the capacitive equivalent network model obtained from ANSYS Q2D.

- The cable length is set to 10 m.
- Firstly, all the conductors are charged to 1 kV using separate voltage sources.
- Once the voltage on the conductors reaches a steady state, the voltage sources are disconnected.
- At t = 6 μs, conductor 1 is discharged to ground via the termination shown in Figure 4.8
- Figure 4.9 shows the voltages on all the conductors of a 10 m UTP cable placed directly above ground.
- At t = 6 μs, conductor 1 is discharged, therefore, the voltage on this conductor drops significantly.
- Due to the capacitive coupling, the voltage on the conductors 2 to 8 also drops according to their proximity with conductor 1.

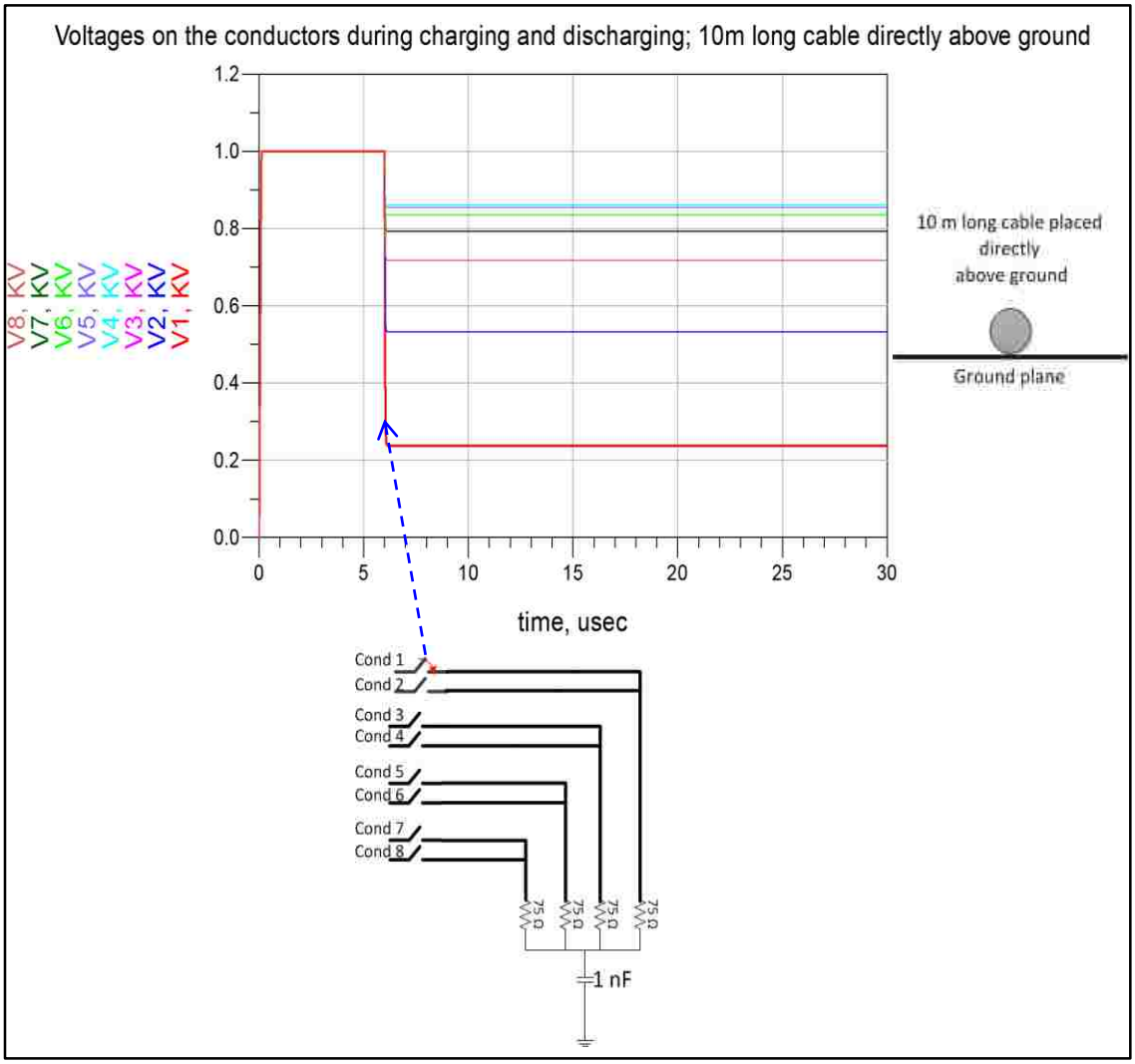

Figure 4.9. Voltage on the conductors of a 10 m long cable placed directly above ground

- Figure 4.10 shows the voltages on all the conductors of a 10m UTP cable placed directly above ground. While the behavior is similar to that seen in Figure 4.9, one major difference is that the drop in voltages at the time of discharge is significantly higher in the case when the cable is placed 1 m above ground plane.
- When conductor 1 is discharged, its pin to ground reduces significantly when compared to the impedance of all other conductors to ground via their self-

capacitances. Hence the all the conductors dump more charge out when conductor 1 is discharged.

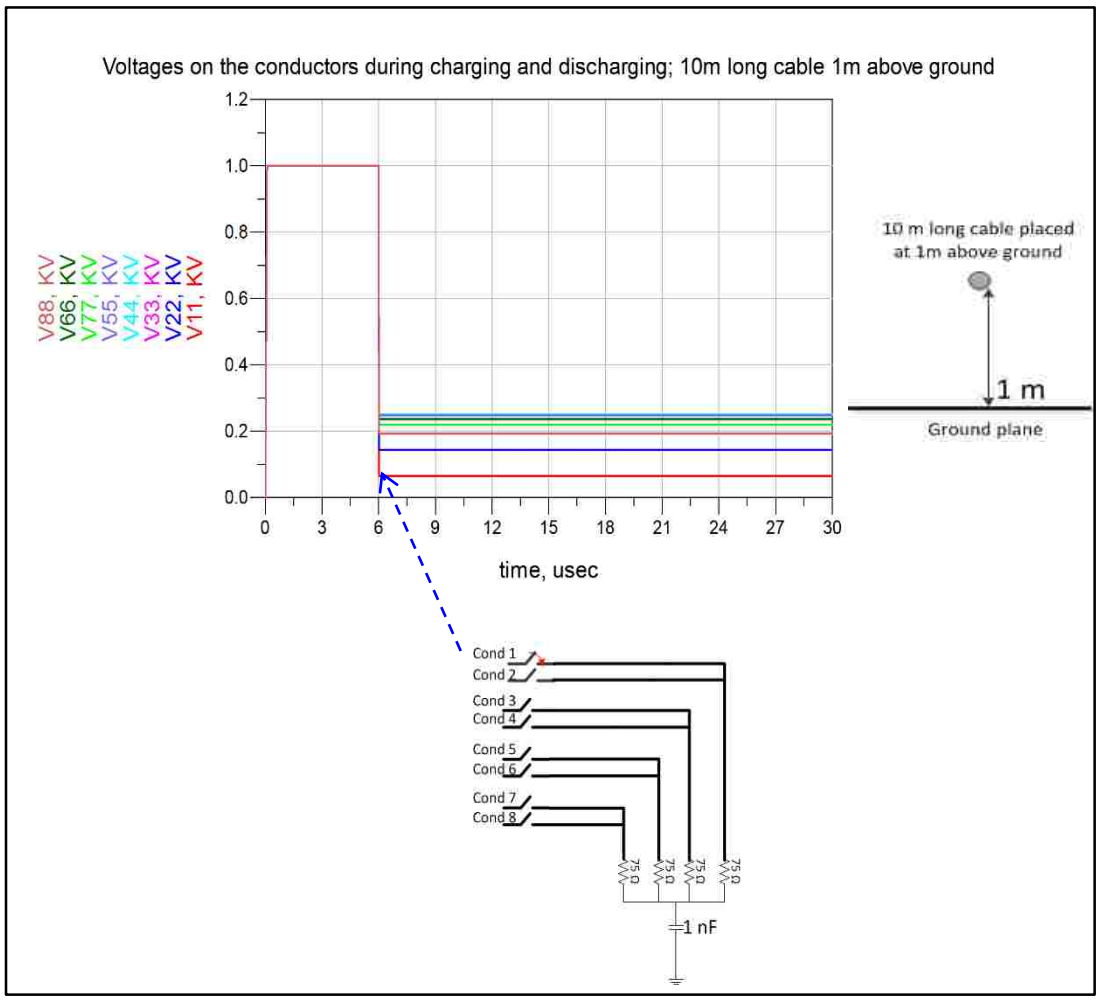

Figure 4.10. Voltage on the conductors of a 10 m long cable placed 1 m above ground

- Figure 4.11 shows the voltage on the 1 nF ESD capacitor during the first discharge. The self-capacitance value of a 10 m cable placed directly above the ground is ~ 0.1 nF. So, the 1 nF capacitor gets charged only to 240V after the first discharge.
- When the same cable is placed 1 m above the ground plane, it has a self-capacitance of ~ 0.09 nF. So, the 1nF capacitor gets charged only to 60V after the first discharge.
- However, in both cases, 1 nF doesn't get charged up to a value high enough to block significant current flowing through it during subsequent discharges. Therefore, for cable lengths up to 10 m, discharge sequencing may still be important.

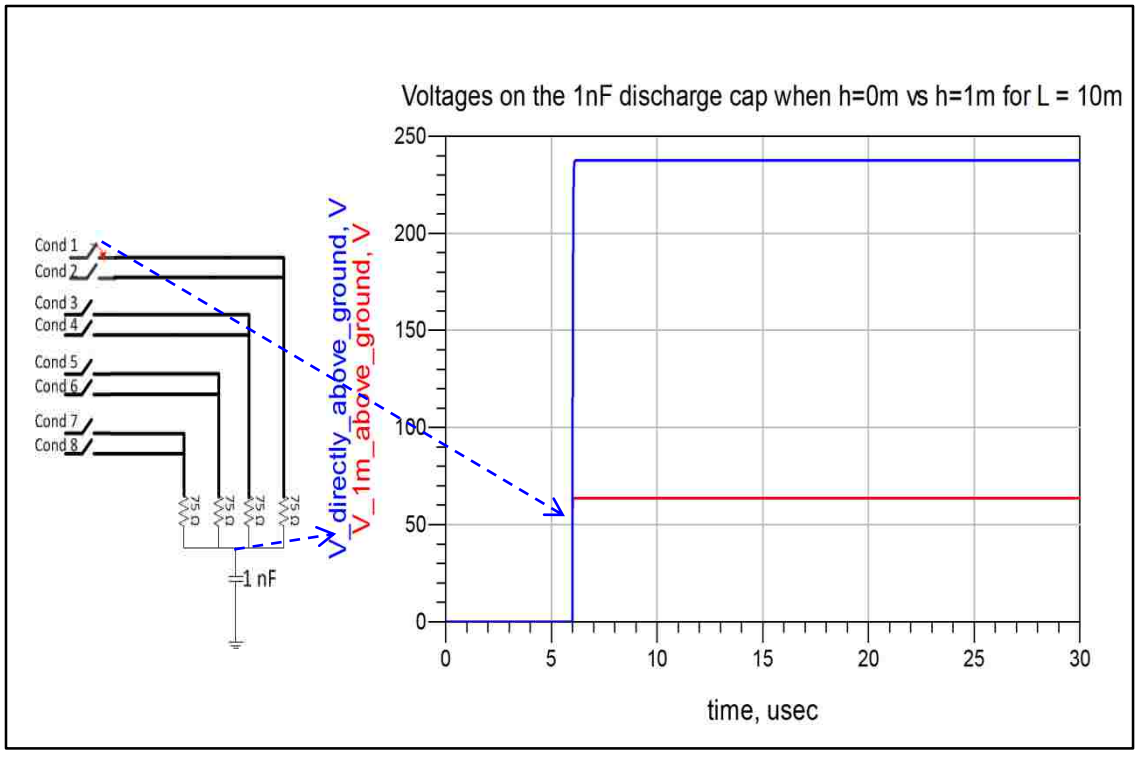

Figure 4.11. Voltage across the 1 nF ESD protection capacitor during the first discharge

4.2.5.2 Simulating a 200 m cable discharge. The cable length is set to 200 m and all other steps are the same that are used in section 4.2.5.1

- Figure 4.12 shows the voltages on all the conductors of a 200 m UTP cable placed directly above ground. An interesting observation is that the voltage on conductor 1 after the first discharge goes down to 820V while in the case of 10 m cable it went down to 220V (see Figure 4.1). The main reason is that the votlage on the conductor measured with respect to ground could only go down as much as the 1 nF capacitor gets charged to. See Figure 4.14
- Due to capacitive coupling, the voltage on the conductors 2 to 8 also drops according to their proximity with conductor 1.

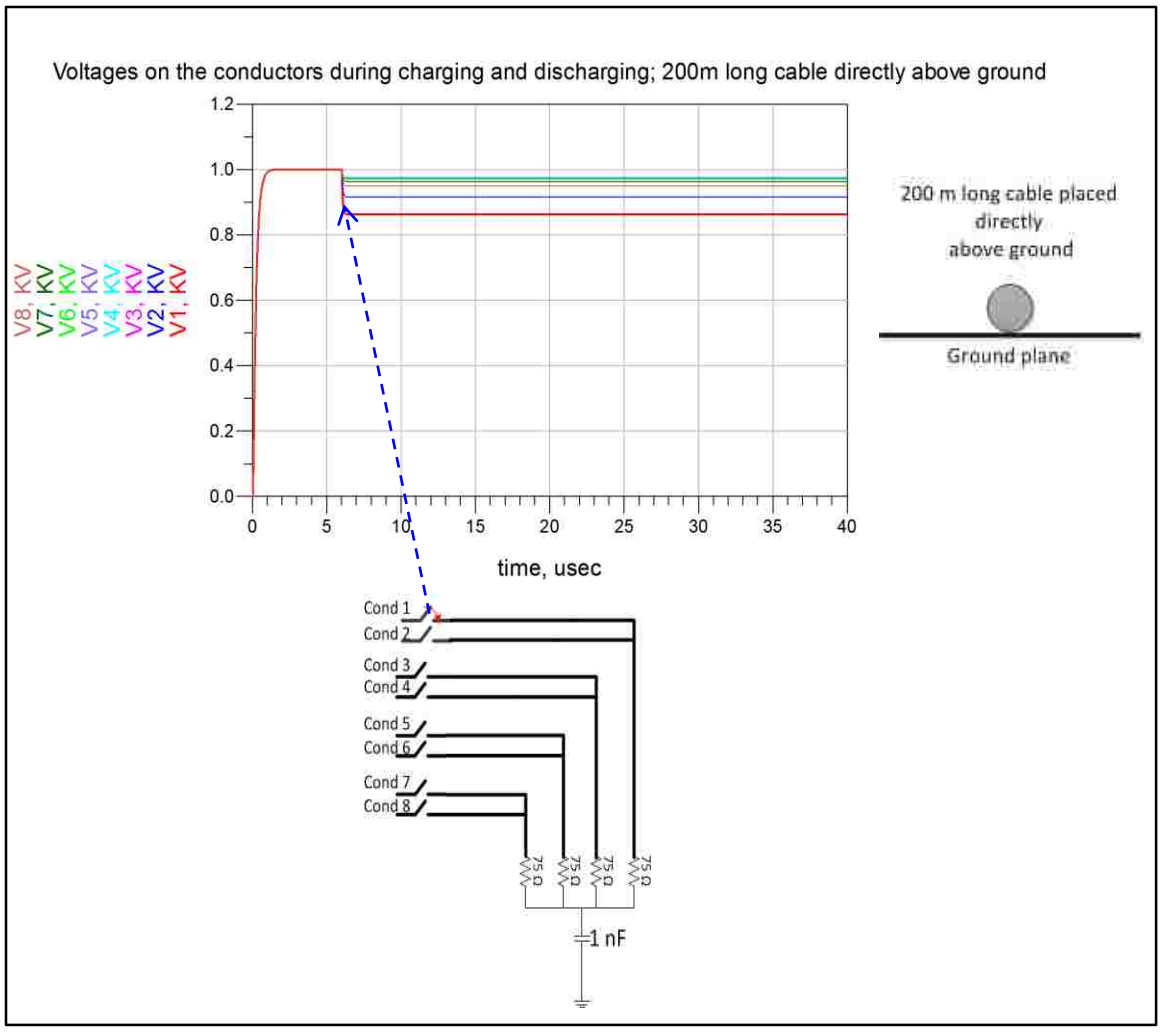

Figure 4.12. Voltage on the conductors of a 200 m long cable placed directly above ground

- Figure 4.13 shows the voltages on all the conductors of a 200 m UTP cable placed 1 m above ground.
- While the behavior is similar to that seen in Figure 4.12, following are the notable differences. The drop in the voltage on conductor 1 is more in this case because the 1 nF capacitor gets charged to a lesser value than that shown in Figure 4.12
- The reason why the voltages on all other conductors drop more than it did in the previous case is that the discharge of conductor 1 provides a lower impedance path to ground than that due to the self-capacitances of the other conductors.

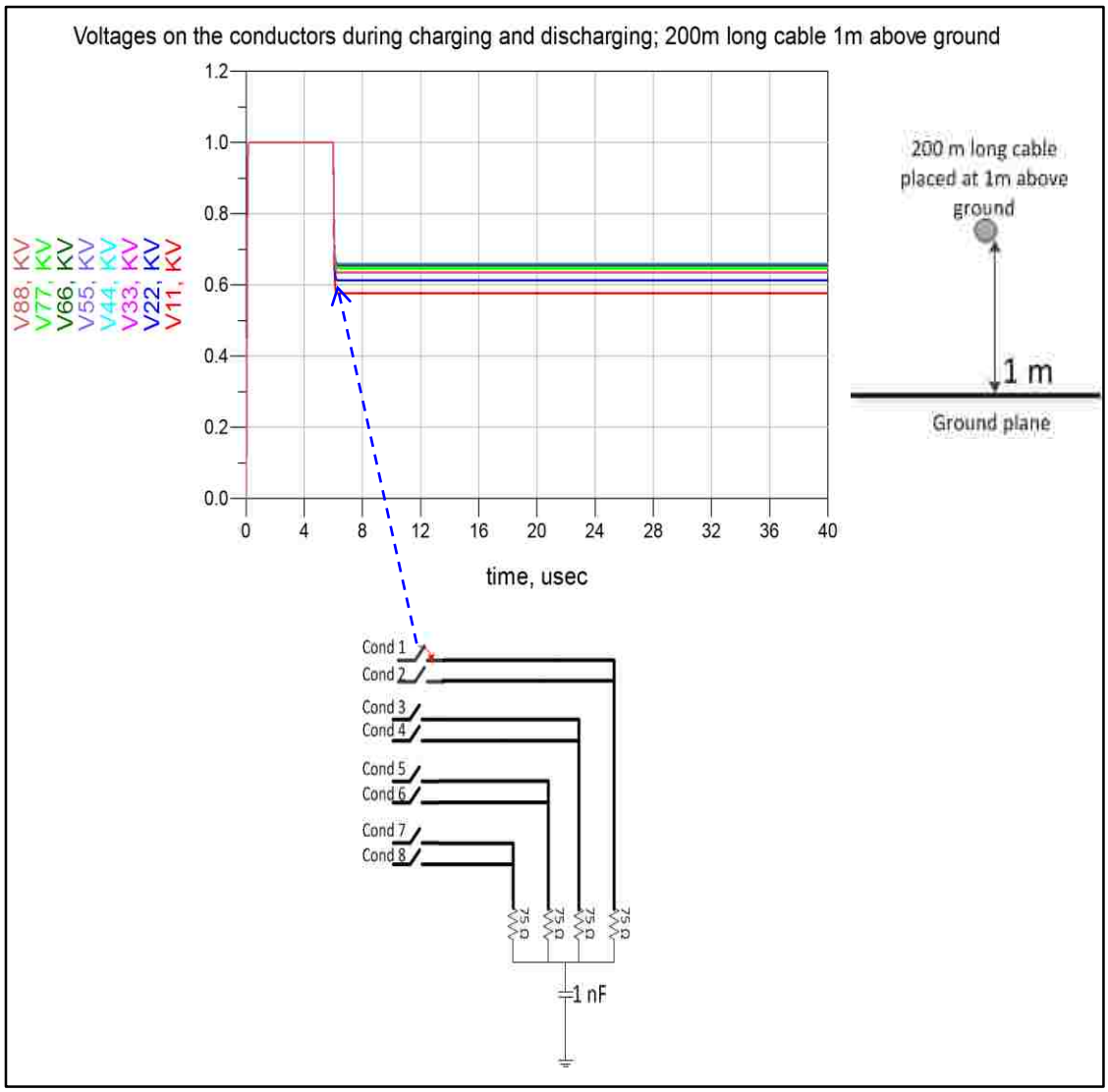

Figure 4.13. Voltage on the conductors of a 200 m long cable placed directly above ground

- In Figure 4.14, the voltage across the ESD protection capacitor when one conductor of a 200 m long cable placed directly above ground plane is discharged, the voltage on the 1nF capacitor rises to ~900V.
- Therefore, the subsequent discharges no longer have a low impedance path to ground through 1 nF.

- Therefore, for the cable lengths beyond 100 m, it may be sufficient to analyze the discharge waveforms of just one pair since the 1 nF capacitor doesn't allow other conductors to discharge any significant current through it.
- This was reported in [5] using measurement results. This study confirms it using simulation.

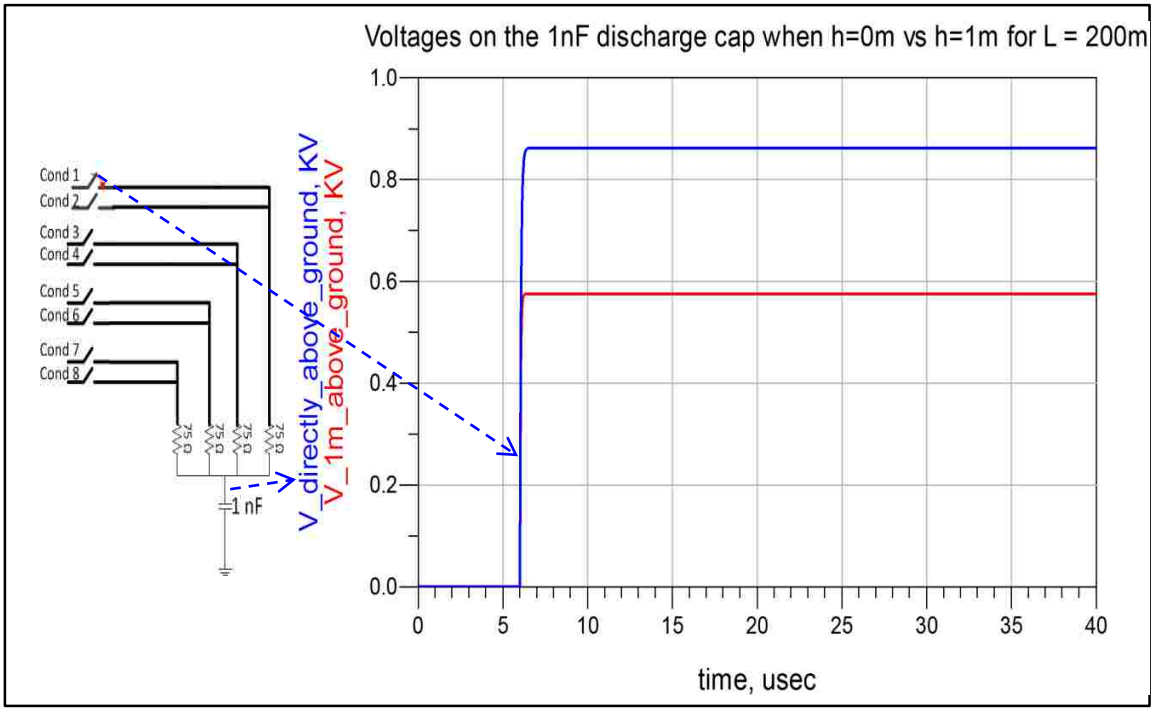

Figure 4.14. Voltage across the 1 nF ESD protection capacitor during the first discharge

4.2.6. Conclusions.

- Equivalent capacitance method is a simple and effective method to estimate the voltages on the conductors of a UTP cable relative to a ground plane during charging and discharging as the ratio of their self and mutual capacitance terms
- It is shown that for cables shorter than ~ 10 m, the 1 nF ESD capacitor doesn't get charged during the first discharge. Therefore, in this case the discharge sequence plays an important role.

- For cables in the range of several hundred meters, only the first discharge and the effects of its cross talk need to be analyzed since subsequent discharges cause negligible current

4.3. HYBRID MODELING TECHNIQUE

The main objective is to model the UTP cable geometry, charging and discharging scenarios as close as possible to the physical phenomena while not significantly increasing the simulation time. This method aims at combining the strengths of some of the modeling techniques mentioned in section Figure 4.1 and models the following aspects of CDE:

- **Charging mechanism:** Charging the center conductors using voltage sources.
- **Discharging mechanism:** Charged cable plugged into a LAN connector.
- **Cable geometry:** Models the effects of varying the cable length, height above ground plane.
- **Discharge sequencing:** Analyzes the effects of pin mating sequences on the discharge modes.
- **Load impedance:** Considers 1 Ω load resistance.
- **Vertical plane:** Models the initial peak of the discharge current due to the vertical plane.
- Twisted pairs are modeled accurately using CST Cable studio.

4.3.1. Method. This section explains the two major steps involved in simulating the CDE of a UTP cable. The first step describes the creation of cable geometry in CST Cable studio and the second step describes the SPICE simulation setup using the network model of the cable obtained from CST Cable studio.

4.3.1.1 Modeling twisted pair geometry in CST cable studio. Four twisted pair wires are created which are then bundled following the Cat 5 UTP specifications, see Table 4.2. Figure 4.15 shows an example of a twisted pair. Each copper conductor has a radius of 0.25 mm. Polyethylene ($\varepsilon_r = 2.25$) having a thickness of 0.2 mm forms the insulator. Four pairs are twisted using the rates given in Table 4.2.

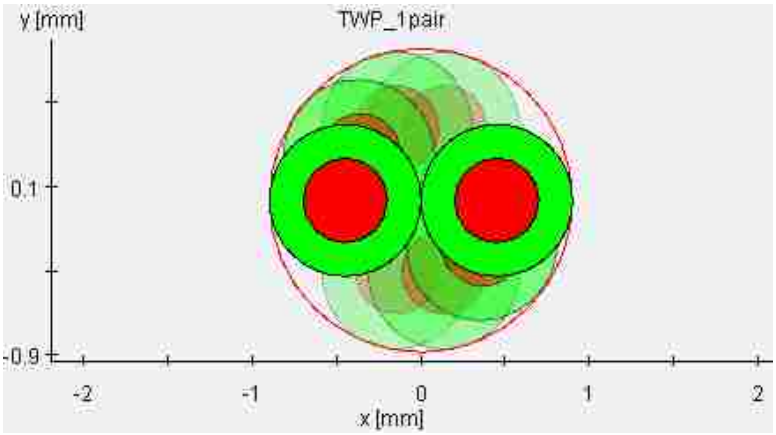

Figure 4.15. Cross section of a TWP created in CST Cable studio

Four twisted pairs are then bundled to form one CAT 5 UTP cable as shown in Figure 4.16. The dielectric between the twisted pairs is chosen to be air and the outer jacket is defined to have a thickness of 0.2 mm and the material used is Poly Vinyl Chloride (PVC) $\varepsilon_r = 3.18$.

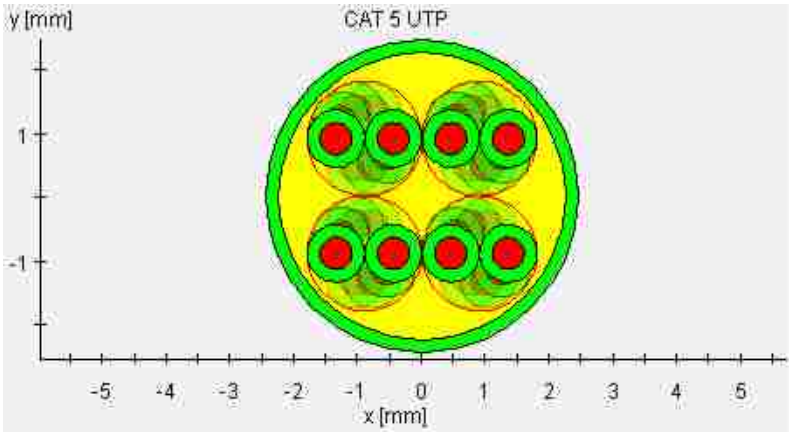

Figure 4.16. Cross section of a Cat 5 UTP cable created in CST cable studio

Next, the Cat 5 UTP cable bundle is placed at a height H above a ground plane as shown in the Figure 4.17.The length ‘L’ and the height ‘H’ are the simulation parameters.

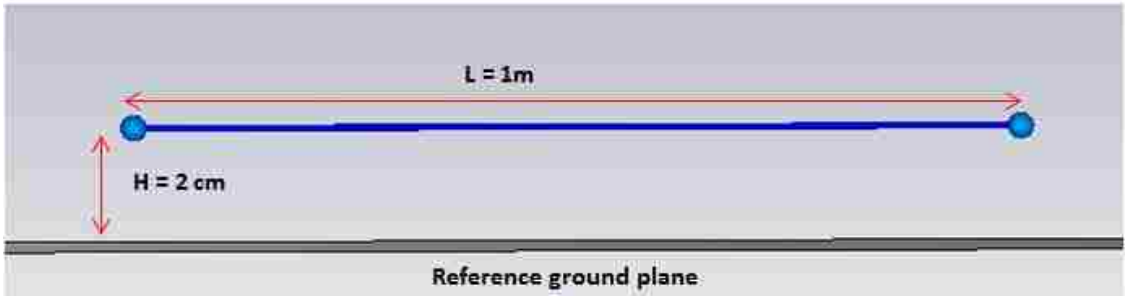

Figure 4.17. Cross section of the TWP cable (left); Side view of the TWP cable (left)

The TWP cable geometry is solved in CST cable studio to obtain a network equivalent model of the entire cable consisting of 8 conductors and a reference plane. The simulation result provides a 16-port scattering parameter (s-parameter) based network model as shown in Figure 4.18.

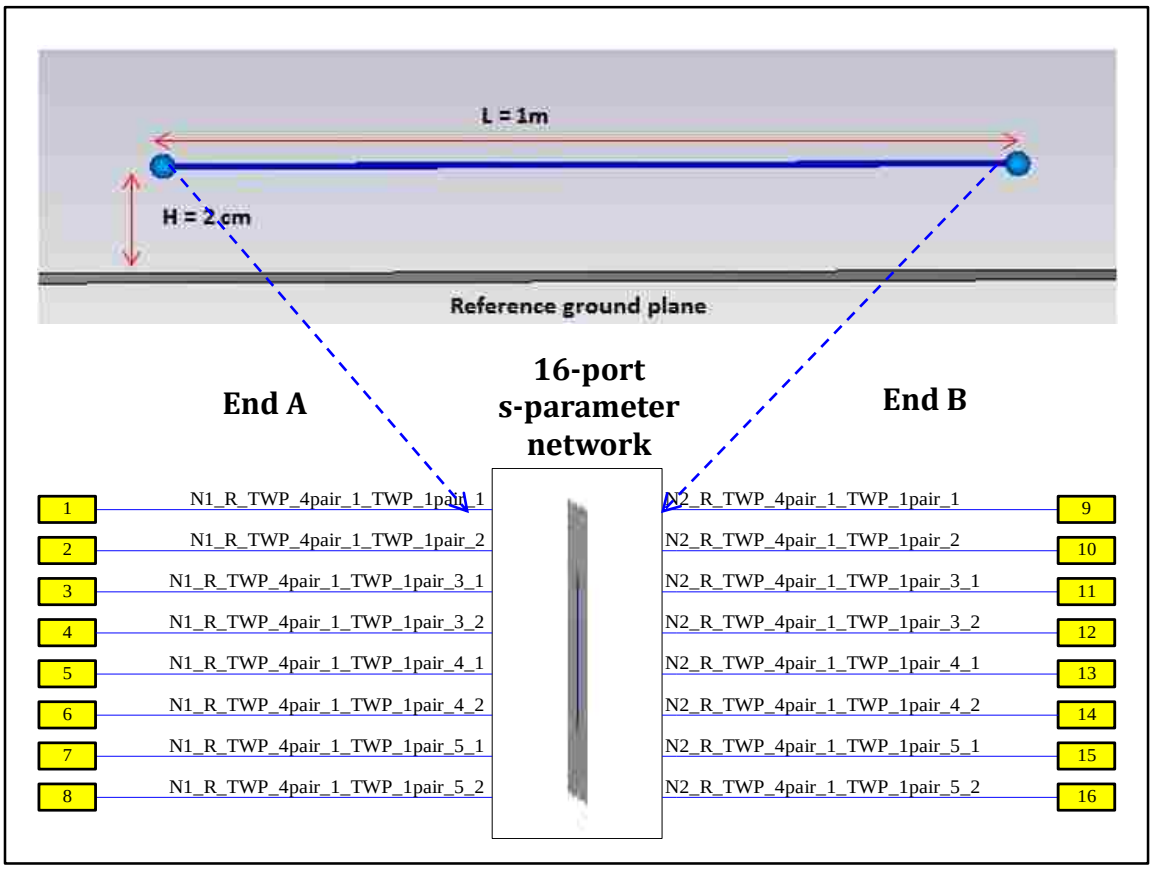

Figure 4.18. UTP cable network model obtained using CST cable studio

4.3.1.2 SPICE simulation in Agilent ADS. The 16-port s-parameter model obtained from CST cable studio can be directly imported into a SPICE solver since its transient solver is the most convenient way to simulate the charging and discharging scenarios. In this study, Agilent ADS is used to perform the transient simulations using the s-parameter model obtained from CST cable studio [18].

As shown in Figure 4.19, a 16 port s-parameter data block is used to import the s-parameters obtained from CST cable studio.

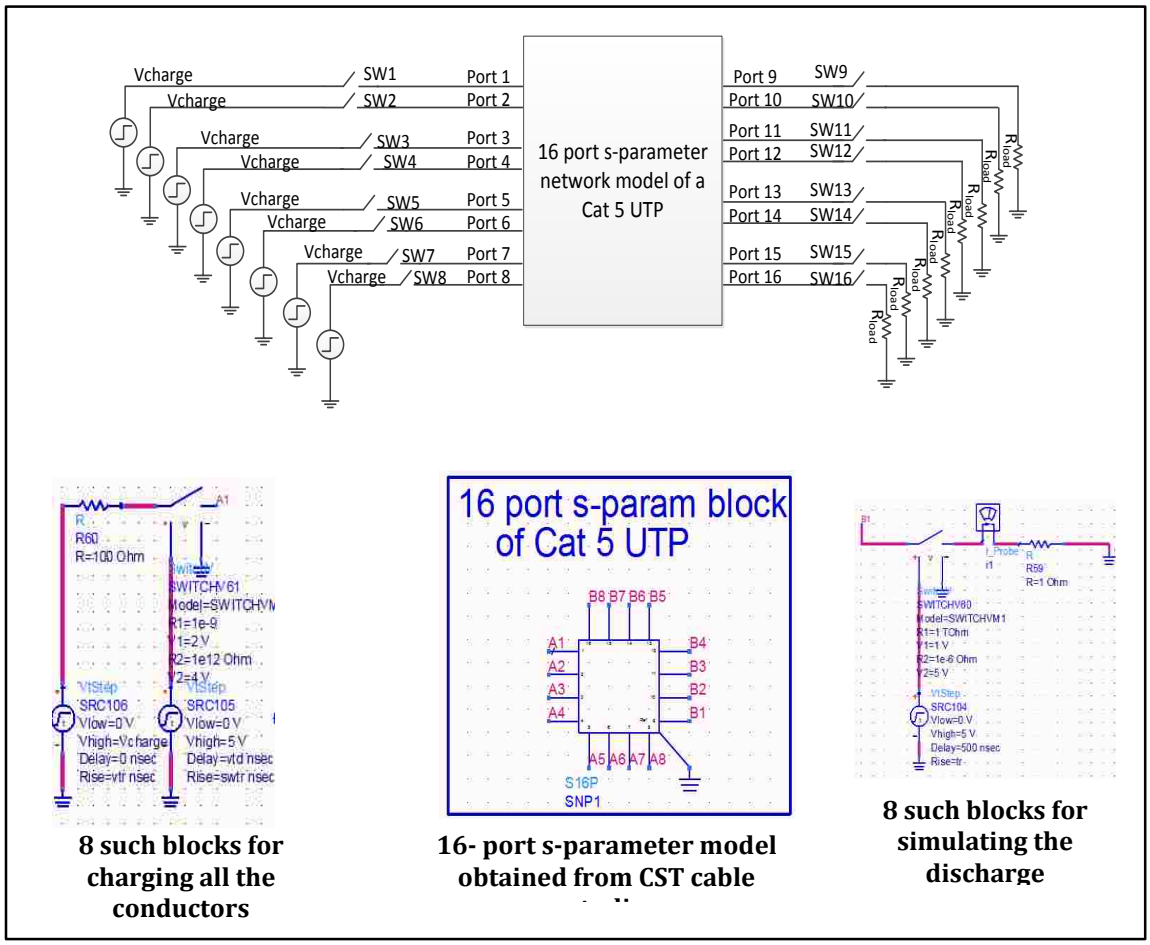

Figure 4.19. CDE SPICE simulation scheme using a network model obtained from CST Cable studio

Ports 1 to 8 represent one end of a TWP cable and ports 9 to 16 represent its other end. The charging of the cable can be simulated by applying voltages on the conductors of the cable with respect to the reference ground. For example, common mode charging

of the cable can be achieved by connecting ports 1 through 8 (or ports 9 to 16) to voltage sources with V_{charge} as the simulation parameter. The switches SW1 to SW8 are initially close to charge the conductors and once the voltage reaches a steady state, they are disconnected. At this moment, the discharge of the cable through a load resistance (R_{load}) can be simulated by closing any or all of the switches SW9 to SW16.

4.3.2. A Simple CDE Tester to Validate the Simulation Model. A CDE tester is developed to validate the simulation results by performing basic measurements. The tester consists of a PCB that has an RJ45 connector at its incoming end where a cable under test (CUT) is connected, as shown in Figure 4.20. Each pin can be separately charged to a high voltage via 500MΩ resistors. Eight mercury wetted reed relays are used to provide separately controlled discharge paths for all the conductors of the LAN cable into 1 Ω load resistors. Four 4 Ω resistors are placed radially to create the low inductance 1Ω current shunt. Since the main objective of this paper is to present the simulation results, the development of the CDE tester is not discussed in great detail and similar testers are discussed in [5] and [6].

Figure 4.21 depicts the test setup that can be used to measure the discharge current waveforms of a 1 m CAT 5 UTP cable. One end of the cable can be plugged into an RJ45 LAN connector on the CDE tester PCB while the other end is left open. Each pin can be charged to certain voltage using a high voltage power supply. All the conductors will be charged equally to the set voltage with respect to ground. Relays K1 to K8 can be used to simulate the discharge of any conductor in any sequence. Since the discharge load is a 1 Ω current shunt, the voltage across the load measured on an oscilloscope (50 Ω input impedance) directly indicates the discharge current value.

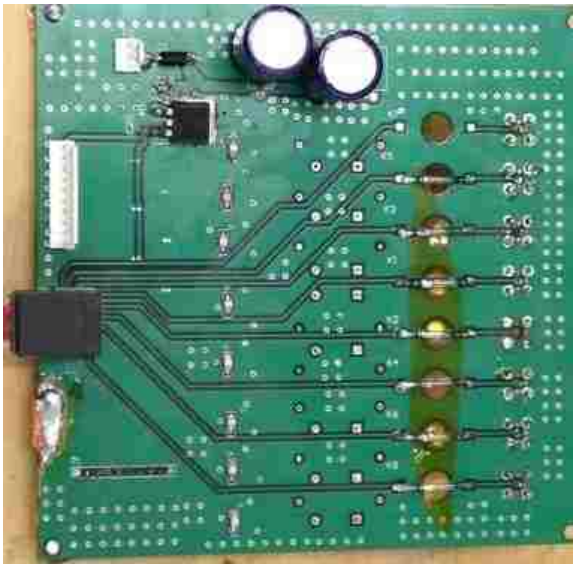

Figure 4.20. CDE tester PCB

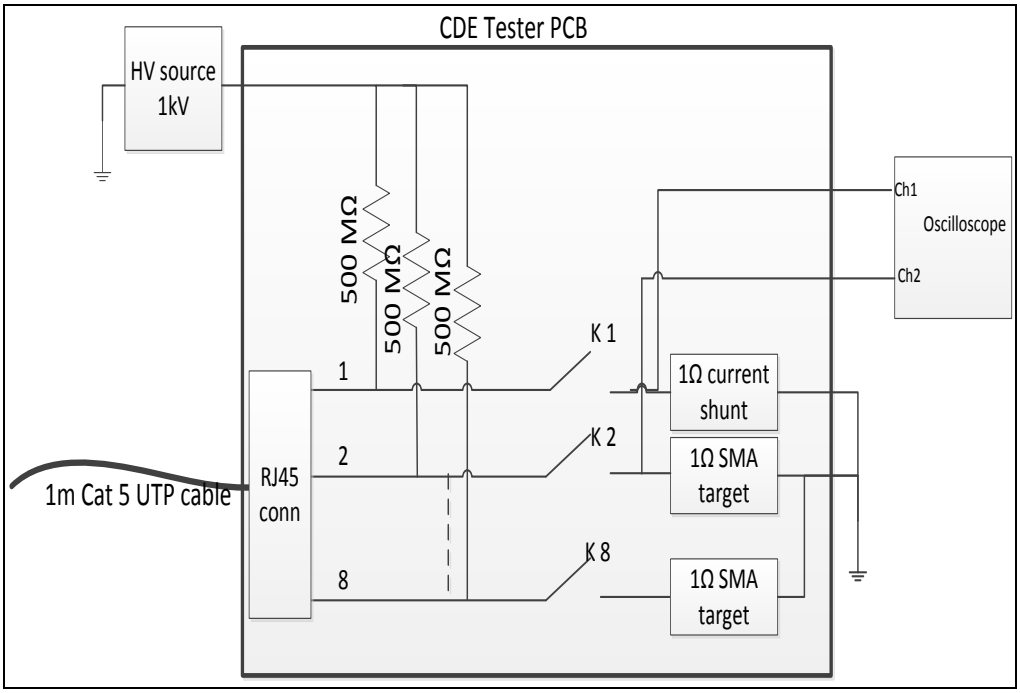

Figure 4.21. CDE test setup to measure discharged waveform

4.3.3. Validating the Simulation Model. Using the hybrid modeling technique, a 1 m long UTP cable placed 2 cm above the ground plane is simulated. All eight conductors of the cable are charged to a common mode voltage of 1 kV. The

charging voltage sources are disconnected after 1 μs which is sufficient to charge all the conductors to 1 kV, in the simulation. Conductor 1, at the far end of the cable, is then discharged into an R_{load} set as 1 Ω. See Figure 4.19

Using the CDE tester, the discharge current waveform of a 1 m CAT 5 UTP cable is obtained with the same charging and discharging conditions that were used in the simulation (V_{charge} = 1 kV)

The simulation result shown in Figure 4.22 reproduces the most important initial parts of the waveform well. Therefore the basic functionality of the simulation model is validated. The initial peak shown in the measurement is due to local capacitance formed between the front portion of the cable and the vertical discharge plane as discussed in section 3.4.2. Modeling the initial peak is discussed in detail in section 4.3.7

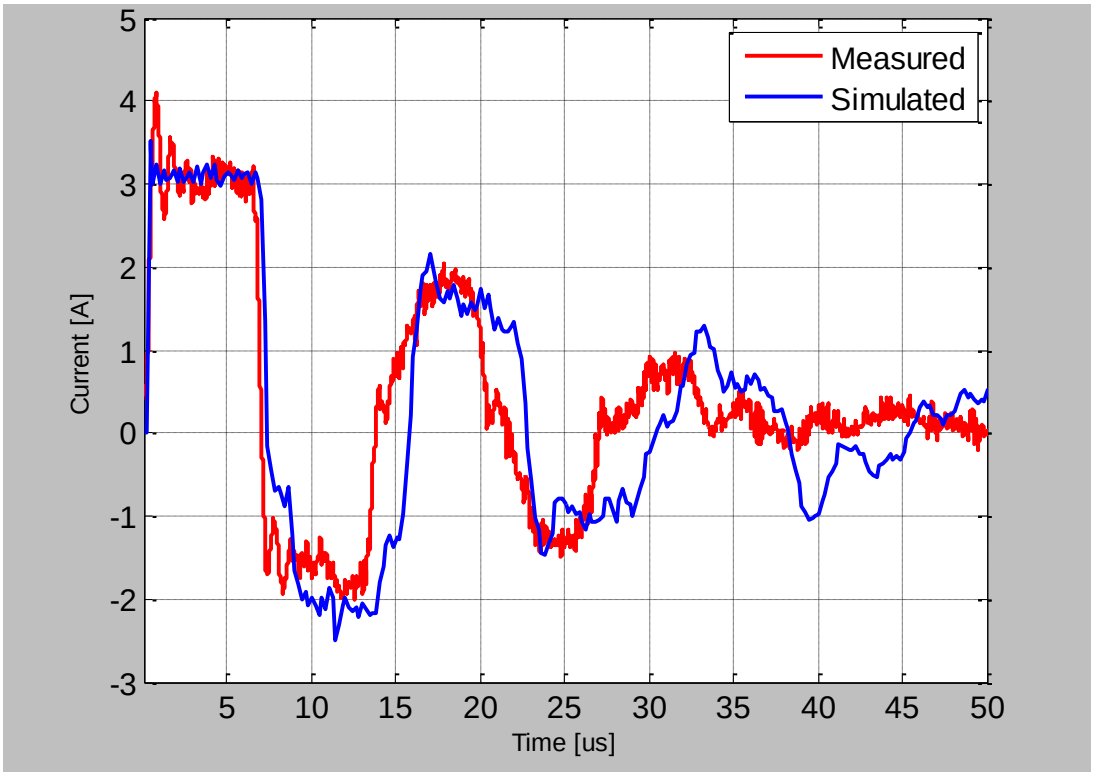

Figure 4.22. Measured vs simulated discharge current waveforms of a 1m Cat 5 UTP cable placed 2 cm above ground

4.3.4. Simulating the Effect of Discharge Sequencing (For Short Cables). In real world CDE events, when a charged Cat 5 UTP cable is plugged into a LAN connector, not all pins contact at the same time. If the cable is charged in common mode, i.e., all eight conductors have the same potential with respect to a reference plane, the first pin that contacts initiates a current between that conductor and the LAN connector. This can be considered as a common mode discharge. At least two different modes can be initiated by the second pin that mates. The second pin can either be from the same twisted pair, or from another twisted pair. If it is from the same pair, a differential mode current will be initiated. In section 4.2.6, it is concluded that the effect of discharge sequencing is important for short (less than 20 m or 30 m) LAN cables. Although the first discharge may cause the highest current, due to the presence of an isolation transformer in the front end of the LAN connector, it is quite important to analyze the differential discharge [5]. Two discharge sequences are simulated and analyzed in this study.

4.3.4.1 Sequence 1: conductor 1-> conductor 2 -> conductor 3. Conductors 1 and 2 belong to the same pair and conductor 3 belongs to a different pair. The time difference between the contact of each pin, in reality, could be several hundreds of micro seconds, whereas the discharge phenomenon doesn't last longer than several hundreds of nanoseconds. The transient solver's time step required to obtain the higher frequency content of the discharge current is about 0.5ns. Therefore, to reduce the simulation time, the time difference between each pin contact is simulated as 1us even though it is about several milliseconds in reality. So, the simulated time sequence is as follows

- Conductor 1 is discharged 500ns
- Conductor 2 is discharged at 1.5us
- Conductor 3 is discharge at 2.5us

Figure 4.23 shows the discharged current of all three conductors at 500ns. Since conductor 1 alone is discharged at this instant, the discharge mode is common mode.

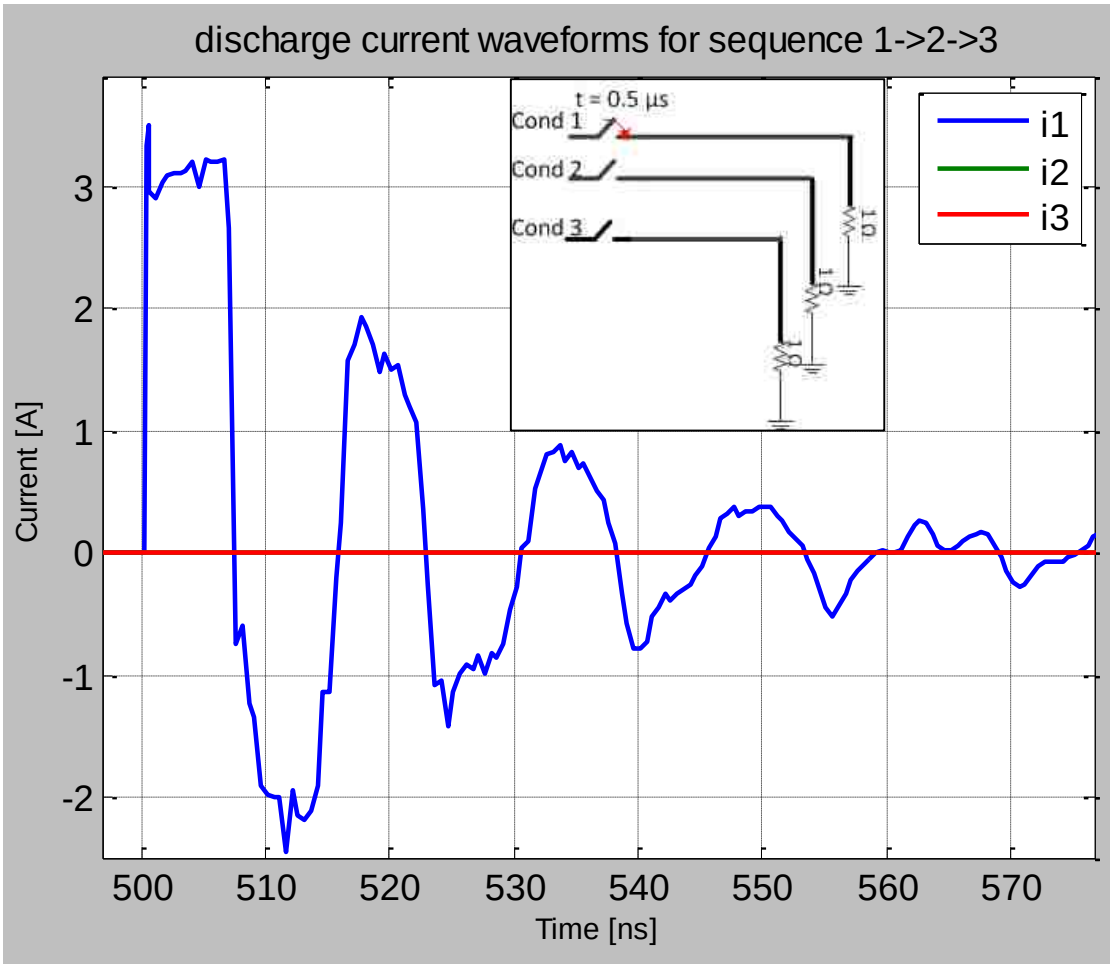

Figure 4.23. Discharge current on conductors 1 to 3 during the discharge of conductor 1 at 500ns.

At 1.5us, conductor 2 is discharged while conductor 1 is already connected. Therefore, currents can be observed in both the conductors as show in the Figure 4.24. It is important to note that the current in conductor 1 is due to cross talk from the discharge current of conductor 2. This is mainly a differential discharge mode with a peak value of ~ 1.7 A. Differential discharge is harmful for the Ethernet PHY layer's isolation transformer and subsequent electronics [5].

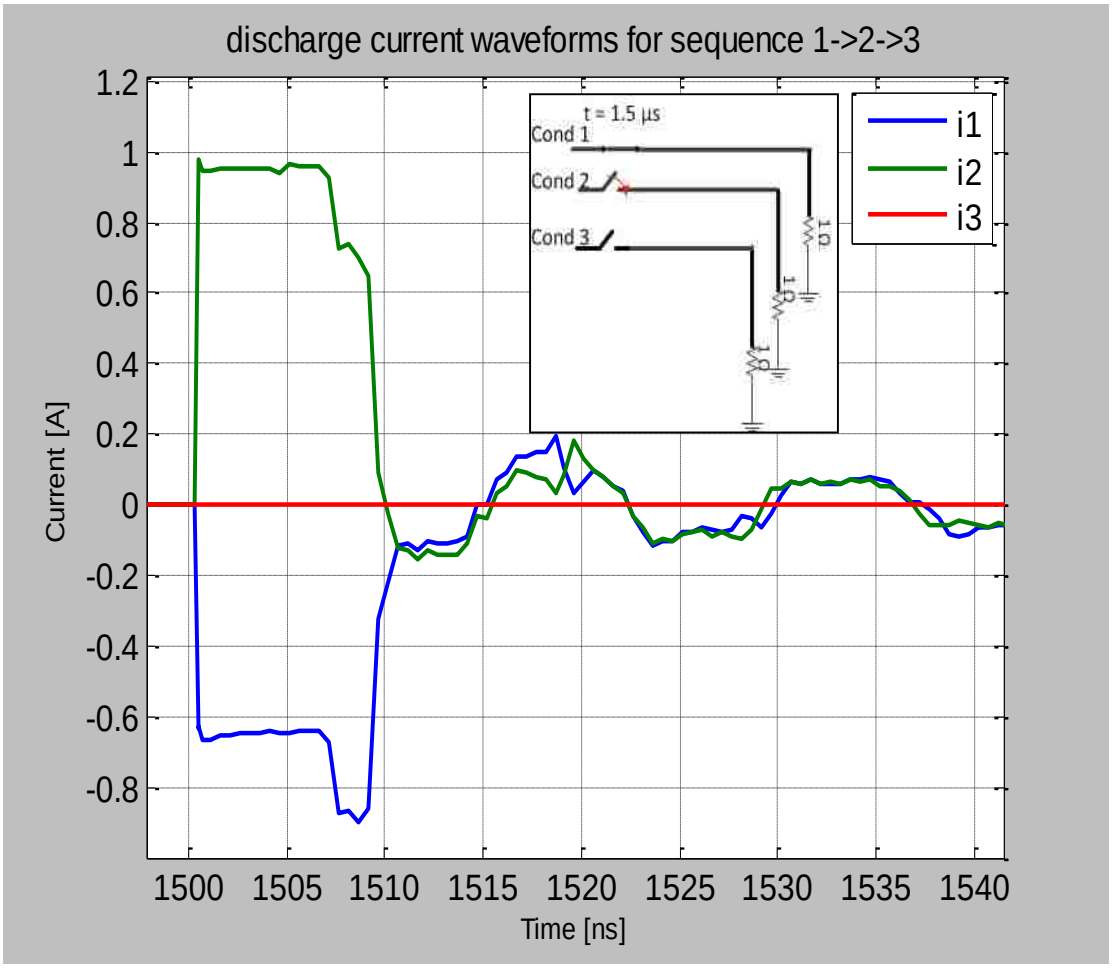

Figure 4.24. Discharge current on conductors 1 to 3 while conductor 2 is discharged at 1.5us.

At 2.5us, conductor 3 is discharged and this results in a common mode current in conductors 1 and 2 as shown in the Figure 4.25. Based on the simplified schematic shown in Figure 3.7, a common mode current on both the terminals on the primary side of an isolation transformer doesn't induce any voltage on its secondary side. Therefore, this discharge is not as harmful to the Ethernet PHY layer as the differential discharge at 2.5us.

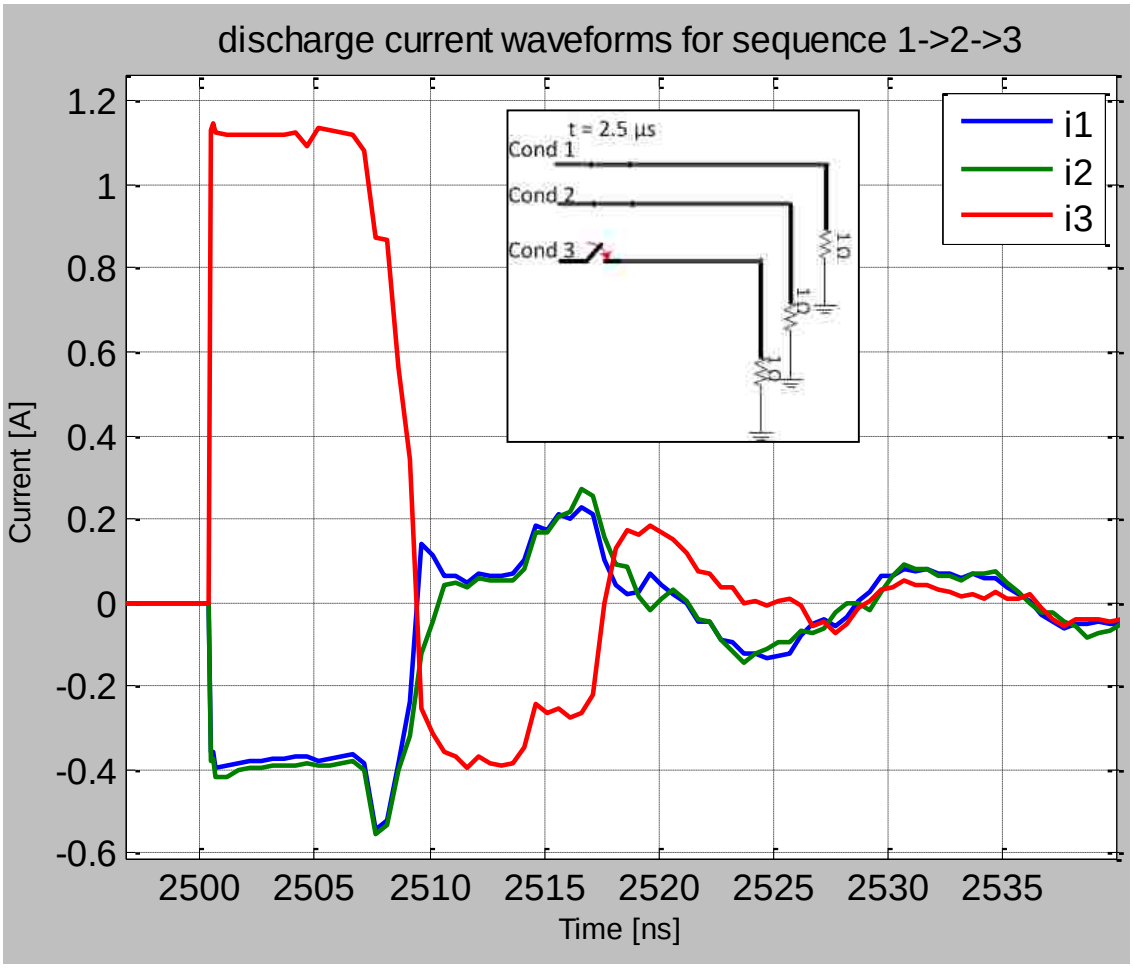

Figure 4.25. Discharge current on conductors 1 to 3 during the discharge of conductor 3 at 2.5us.

4.3.4.2 Sequence 2: conductor 1-> conductor 3 -> conductor 2. In this scenario, conductor 1 is again discharged first. The next discharge is performed on conductor 3 which belongs to a different twisted pair. Following is the sequence of discharges simulated in this scenario.

- Conductor 1 is discharged 500ns
- Conductor 3 is discharged at 1.5us
- Conductor 2 is discharge at 2.5us

The discharge currents of all three conductors at 500ns are the same as in section 4.3.4.1. See Figure 4.23.

Figure 4.26 shows the discharge current on all 3 conductors when conductor 3 is discharged at 1.5us. Magnetic coupling from current on conductor 3 results in a current in conductor 1 with an opposite polarity. However, since conductor 2 is still unconnected, the differential current between within the pair is equal to the current on conductor 1 which is 1 A.

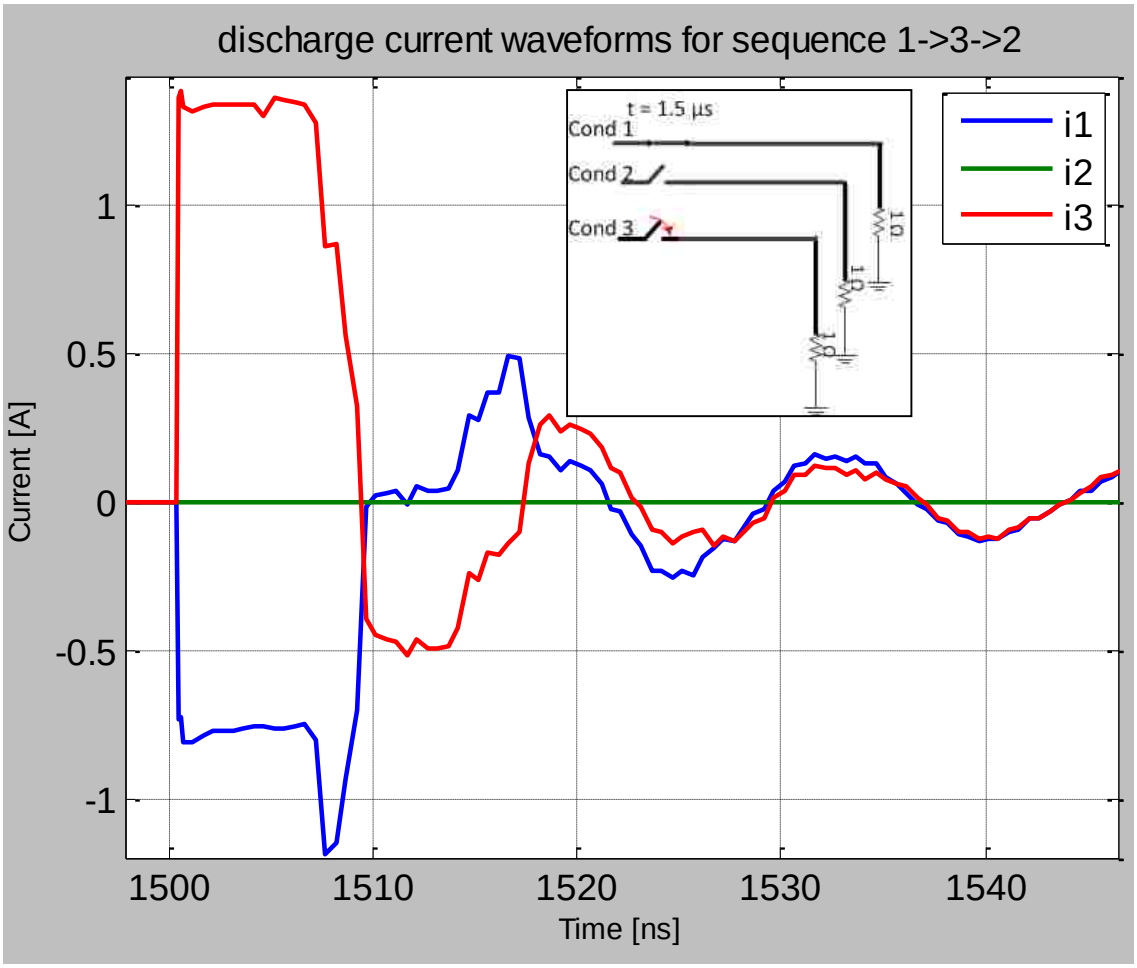

Figure 4.26. Discharge current on conductors 1 to 3 during the discharge of conductor 3 at 1.5us.

At 2.5 us, when conductor 2 is discharged, cross talk causes currents in the opposite direction in conductors 1 and 3 as shown in Figure 4.27. The differential current between conductors 1 and 2 is ~ 0.85A.

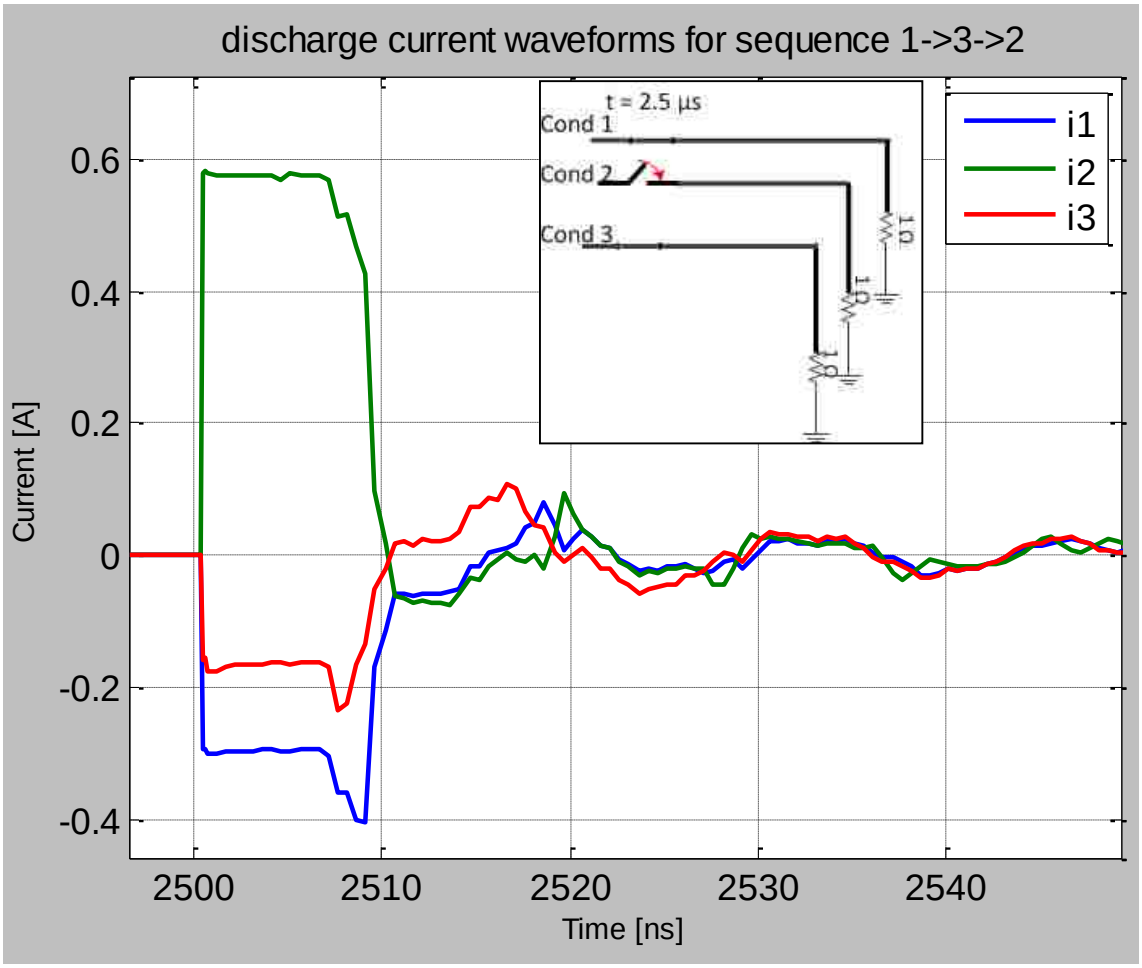

Figure 4.27. Discharge current on conductors 1 to 3 during the discharge of conductor 3 at 2.5us.

- A comparison of the magnitudes of differential currents within the conductor pair 1&2 for both the discharge sequences is shown in Figure 4.28. It is to be noted that the differential current between pair 1&2 during the sequence 2 (1->3->2) actually occurs at t = 2.5 µs. But, it is shifted to 1.5 µs to get a better figurative comparison.
- It can be observed that the differential current is almost double for sequence 1 than that for sequence 2. In other words, if the first two discharges belong to the

same twisted pair, the differential current between that twisted pair will be higher than that with any other combination.

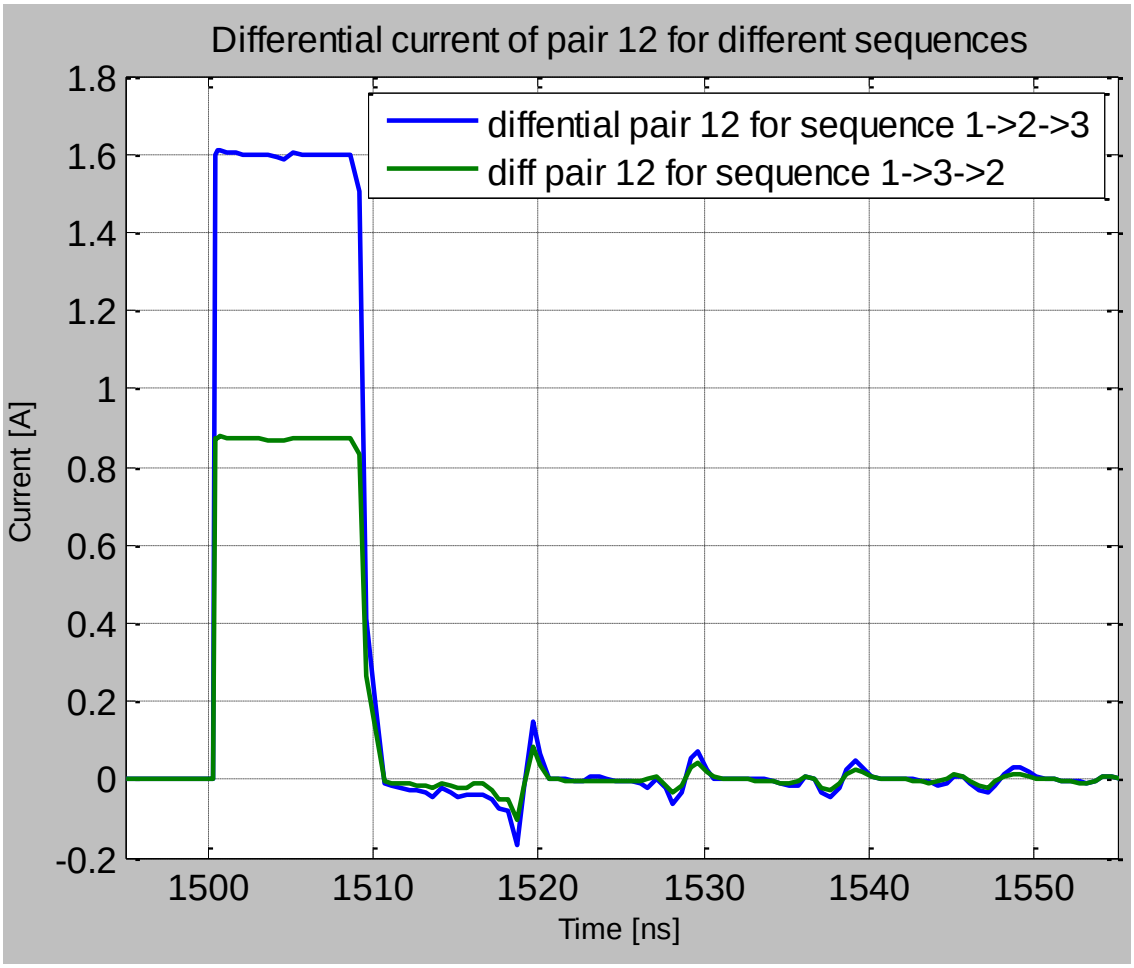

Figure 4.28. Comparing the magnitudes of differential currents of the pair12 for both the sequences. Time scale of the sequence 1,3,2 is shifted

4.3.5. Varying the Height of the Cable above the Ground Plane. In this case, the height of a 1m long CAT 5 UTP cable above the ground plane is varied from 0.5cm to 10cm. The plateau of the discharge current is a related to the capacitance of the cable above the ground plane and the load impedance into which it is being discharged into according to equation (2).

As the height of the cable is varied from the ground plane, the cable capacitance reduces and the plateau of the discharge current reduces gently following an inverse

hyperbolic function. The simulation results shown in the Figure 4.29 conform to the measurements done in [2].

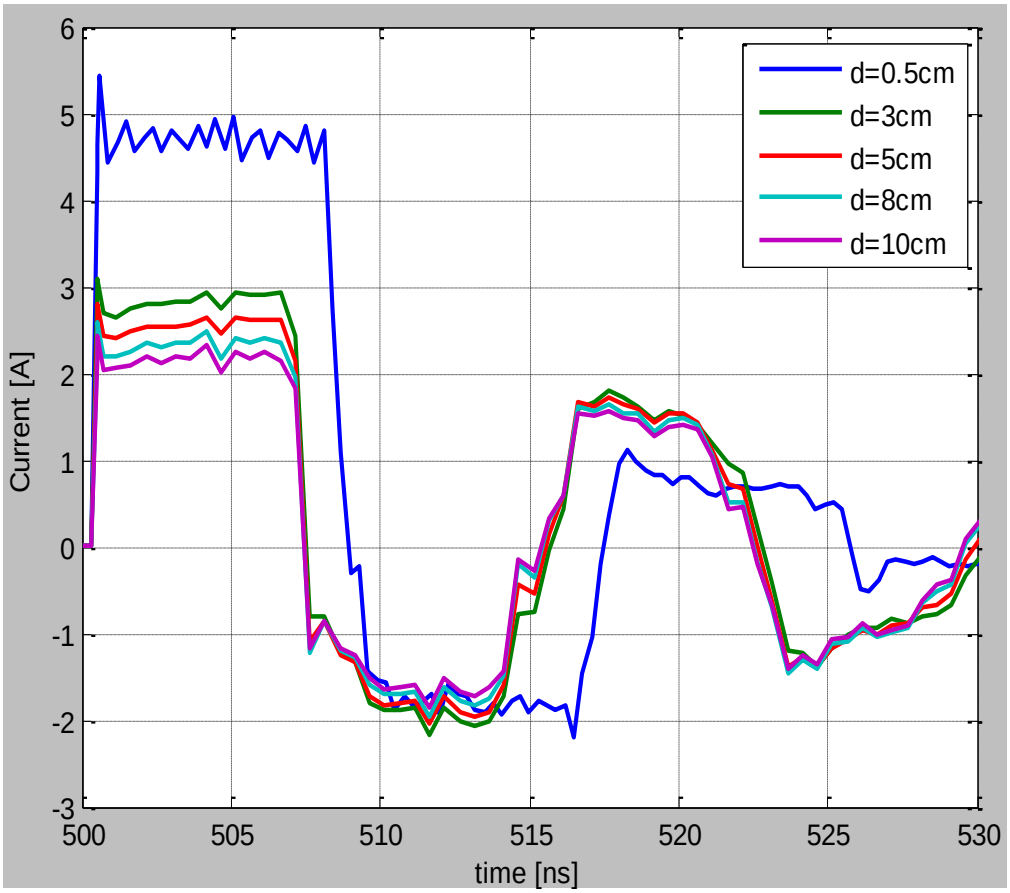

Figure 4.29. The effect of varying the height of the cable above the ground plane on the discharge current waveform

- It's interesting to note that when the height of the cable approaches the value of the jacket thickness (i.e. the cable is placed directly above ground), the electric permittivity of the jacket and the insulation dominates (ε_r ~ 1.5 or higher), thus increasing the pulse length. [3]
- For d>> conductor radius, the free electric permittivity dominates. So, the pulse length for all other heights doesn't change significantly
- Plateau value of the discharge current follows an inverse hyperbolic relationship as per equation (2)

4.3.6. Varying the Cable Length. In this case, the cable length is varied from 0.5m to 4m while all other cable parameters are unchanged. The length of the pulse can be calculated as per equation (4) [6]. This indicates that the pulse width increases with an increase in the cable length. The simulation result shown in Figure 4.30 conforms to the expected behavior.

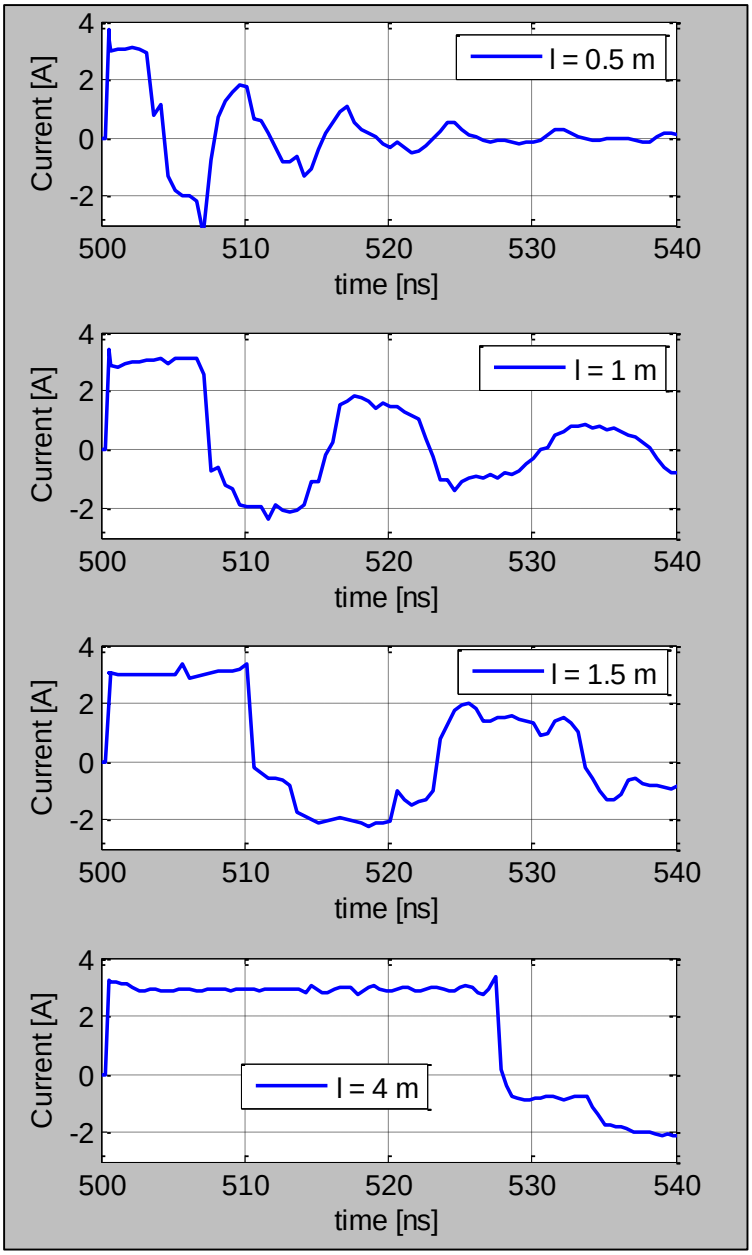

Figure 4.30. The effect of cable length on the pulse length of the discharge current waveform

However, it is found that the applicability of this modeling technique is limited to the cable lengths up to 20 m. There are two potential reasons for this limitation.

- Firstly, a 2D+ solver calculates an equivalent circuit (RLGC per unit length parameters) and then converts that information into s-parameters during post processing. This process involves solving inverse hyperbolic equations using their expansion series. The accuracy of this computation suffers with the increase in the cable length. The way around it is to use RLGC equivalent directly in SPICE.
- Another factor that my impact the accuracy of this method is that CDE is a transient phenomenon and hence the required simulation bandwidth is between DC and about 2 GHz to 3 GHz. Therefore, the application of 2D transmission line theory to model cable geometries beyond 20 m up to 3 GHz becomes questionable. A natural solution for this problem is to develop a full wave model of the cable but the major disadvantage its excessive simulation time. Hence, the proposed hybrid model strikes a balance between the accuracy and the simulation runt-time.

4.3.7. Modeling the Initial Current Peak. Section 3.4.2 explains the impact of having a vertical discharge plane on the discharge current. The fast rising initial peak is attributed to the capacitance formed between the front end of the cable and a vertical plane near the discharge point (for e.g. the metallic enclosure of a LAN port) [2], [8]. However, modeling the initial peak is not straightforward since it depends on several factors such as the ratio of the capacitances of the front end of the cable and the cable above ground, approach speed and arc formation. Two methods have been proposed to model the initial peak in this study.

4.3.7.1 Lumped capacitor method. As shown in section 4.2.1, in hybrid modeling technique, a UTP cable above a ground plane is modeled in CST cable studio and an equivalent network model (s-parameter) is used in SPICE to simulate charging and discharging. One way to incorporate the front end capacitance of the cable is to connect a lumped capacitance at the discharge end of the cable in the SPICE schematic. However, the value of this capacitance needs to be experimentally found out. Based on the measured discharge waveforms with an initial peak, the front end capacitance can be

estimated as follows. The initial peak current for 1 m cable when charged to 1 kV is measured to be 4.5 A and the rise time is less than 200 ps [2]. This results in a capacitance value of ~ 0.8 pF. Therefore, a 0.8 pF capacitance is connected at the discharge end of the cable as shown in Figure 4.31

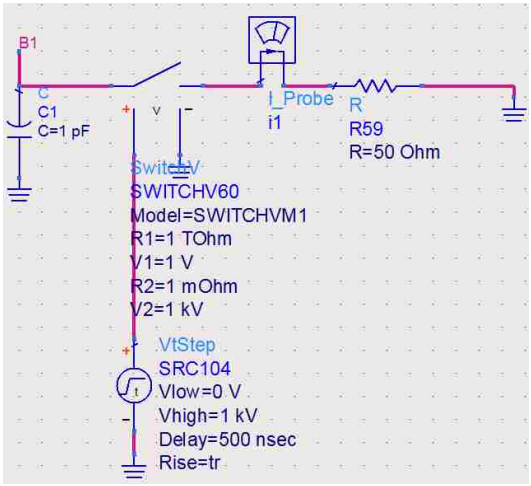

Figure 4.31. Adding a lumped capacitance at the discharge end of the cable to model the initial peak

Figure 4.32 shows the comparison between the measured discharge current with an initial peak and the discharge current obtained using a 0.8 pF lumped capacitor at the discharge end of the SPICE circuit. The simulated discharge current exceeds the measured discharge current peak by ~ 0.3 A. The accuracy of this method is limited by the accuracy of the estimated capacitance value and also due to not modeling the arcing rigorously.

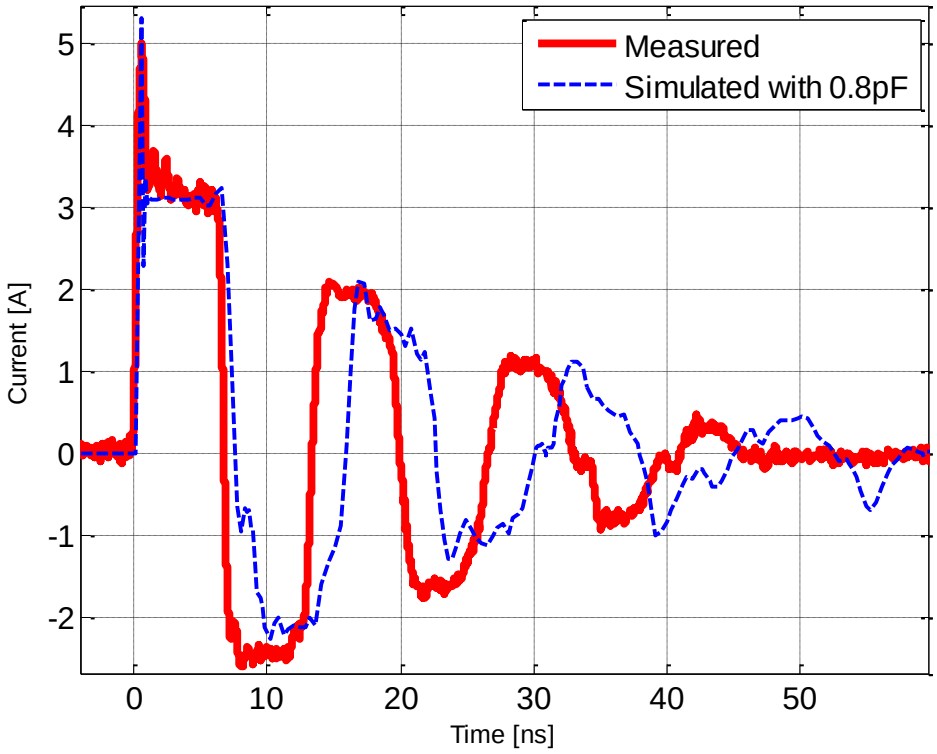

Figure 4.32. Measured discharge current vs simulated discharge current with the initial peak modeled using a lumped capacitor

4.3.7.2 Model the vertical discharge plane in CST cable studio. Another way to model the initial peak is to include the presence of a vertical discharge plane in the CST studio cable geometry. In this approach, the16-port network model obtained from CST cable studio should implicitly model the effect of the front end capacitance of the cable. However, it is important to note that to obtain a significant initial peak, the capacitance between the front end of the cable and the VCP should be higher than that between the cable and the HCP. In other words, the front end of the cable has to be much closer to the VCP than to HCP as shown in Figure 4.33

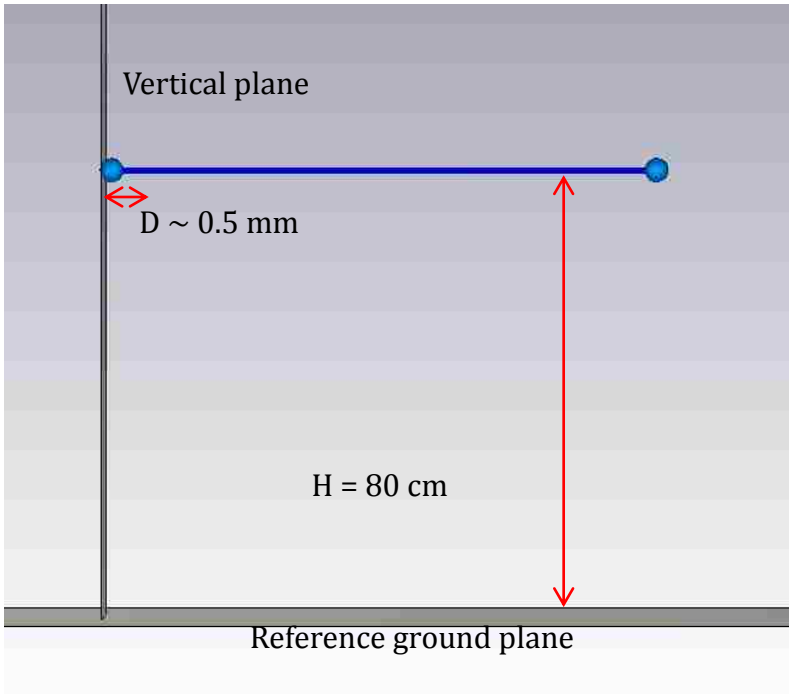

Figure 4.33. Modeling a vertical discharge plane with the cable placed 80 cm above ground

Figure 4.34 shows the comparison between the two modeling methods and the measured discharge current waveforms. It can be observed that method 2 underestimates the initial peak by 0.2A. One reason is that the front end capacitance is directly proportional to the distance between the cable and the VCP; therefore, in real world CDE, this capacitance increases as the cable approaches the VCP and reaches a maximum value before arcing occurs. The exact distance at which arcing occurs depends on several parameters such as the approach speed and relative humidity [19]. Since these factors are not considered in the simulation model, the accuracy is limited.In comparison with method 1, the advantage of method 2 is that the value of the capacitance need not be experimentally found out.

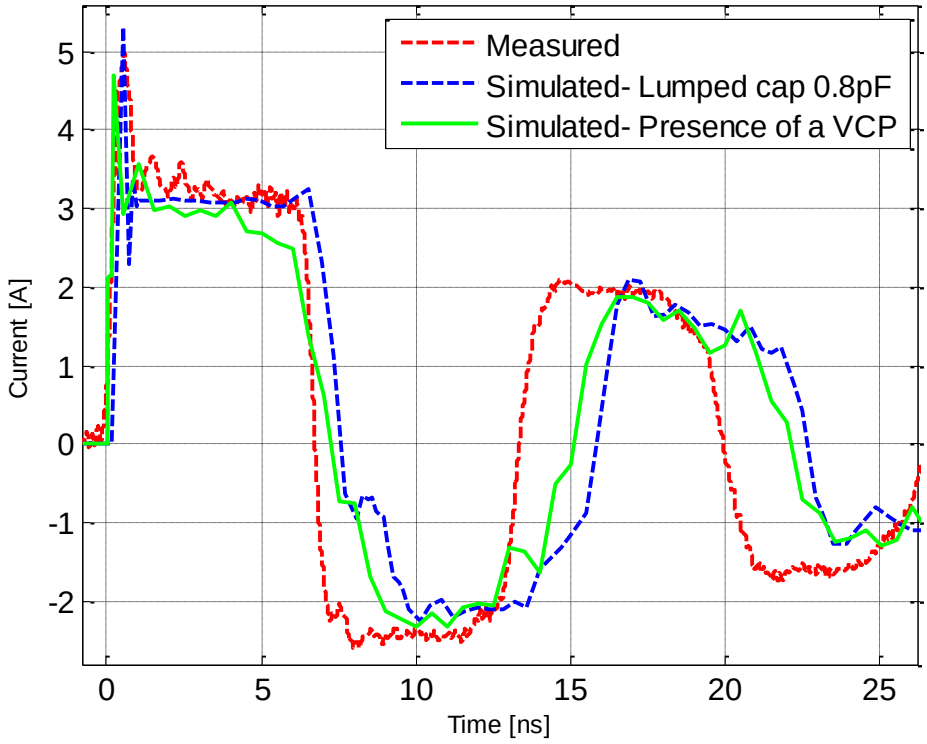

Figure 4.34. Comparing the measured and the simulated discharge current waveforms with initial peak using methods 1 and 2

5. CONCLUSIONS AND FUTURE WORK

5.1. CONCLUSIONS

- Protection against LAN CDE requires special attention due to the faster rise times (~200 ps), longer pulse widths (lasting for milliseconds in some cases), electrical over-stress due to differential discharges and high initial peaks.
- The impact of ESD induced CDE on a cable that is connected between a grounded system and a floating device is minimal due to the following reasons.
    - Based on the source and load capacitance ratios, a 10 kV human ESD which in turn causes CDE results in a voltage of 2 kV across the 1 nF capacitor on the grounded Ethernet device which is within the isolation criterion.
    - Since the cable is already connected, the discharge mode is significantly a common mode. Therefore, there is little voltage induced on the secondary of the isolation transformers of the PHY chip.
- An STP cable with a ground shell connected to a grounded Ethernet port significantly reduces the threat posed by CDE on the inner wiring and the PHY connector. The magnetic coupling due to shielding imperfections is too small to cause any damage. Cables with braided shielding will have higher magnetic coupling than that in the cables with a foil shield.
- Full wave simulation is not feasible to model CDE due to excessively long simulation times
- This simplified modeling technique works well for estimating the voltages on conductors during charging and discharging
- For any given length, the worst case discharge scenario could occur when the cable is placed directly above ground than that at any other height.
- First conductor discharge of cables longer than 100m charges the Bob Smith AC termination 1 nF cap significantly, therefore, subsequent discharges are harmless.

- For cables shorter than ~ 50 m, the discharge sequencing needs to be investigated since the 1 nF capacitance is not effective in reducing the impact of subsequent discharges.
- CST cable studio allows accurate modeling of twisted pair cables and also provides the ability to model the 3D effects. Since the cable geometry is solved using several cascaded uniform cross sections, simulation times are less than several minutes.
- For short cables, the worst case discharge sequence is that when the first two discharges happen from the pins belonging to the same twisted pair. Significant differential discharge current is produced in this sequence. The differential current due to the second discharge might be more dangerous than the first discharge since it current flows through both windings of the transformer. Therefore, protecting the PHY electronics against the first discharge alone is not sufficient for short cables.
- For a Cat 5 UTP cable of 1m placed 2cm above a ground plane, the discharge current plateau is simulated to be about 3A/kV of charge voltage and the pulse length is about 7 ns per meter. This conforms to the findings of [1]
- The accuracy of this method is limited to cable lengths up to 20 m. This can be overcome by using a tool that allows exporting RLGC or W-element of a twisted pair cable.
- Lumped capacitance method to model the initial peak works well with reasonable accuracy. However, the drawback of this method is that the value of the capacitance needs to be experimentally found out.
- Another method is to model the presence of the vertical coupling plane in CST cable studio so that the s-parameters implicitly include this effect. While this method is closer to the actual discharge phenomenon, its accuracy suffers from the fact that effects of approach speed, arc formation and humidity are not modeled.

5.2. FUTURE WORK

The framework laid by the current study can be extended by adding the following aspects

- Develop SPICE models of Ethernet magnetics to estimate the voltages induced on the PHY electronics. These models can be connected to the cable models developed using the hybrid modeling technique presented in this study, to simulate CDE.
- System efficient ESD design (SEED) modeling of the Ethernet magnetics and PHY electronics with the IV curves of the ESD protection diodes and the saturation of magnetics included.
- Analyze the CDE of power over Ethernet (PoE) type Ethernet connector interface.
- Hybrid modeling technique as a concept should work for any cable length. The limitation of the existing model can be overcome by finding a simulation tool that can accurately model twisted pair geometry and export "RLGC" models. RLGC parameters can be used to generate a W-element matrix which can be imported in SPICE to perform charging and discharging simulations.

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