Fall 2013

Trough-silicon-via inductor: Is it real or just a fantasy?

Rongbo Yang

Department:

TROUGH-SILICON-VIA INDUCTOR:

IS IT REAL OR JUST A FANTASY?

by

RONGBO YANG

A DISSERTATION

Presented to the Faculty of the Graduate School of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

MASTER Of SCIENCE

in

COMPUTER ENGINEERING

2013

Approved by

Dr. Yiyu Shi, Advisor
Dr. Jun Fan
Dr. Minsu Choi

ABSTRACT

Through-silicon-vias (TSVs) can potentially be used to implement inductors in three-dimensional (3D) integrated system for minimal footprint and large inductance. However, different from conventional 2D spiral inductor, TSV inductors are buried in lossy substrate, thus suffering from low quality factors. This thesis presents how various process and design parameters affect their performance. A few interesting phenomena that are unique to TSV inductors are observed. We then proposed a novel shield mechanism utilizing the micro-channel, a technique conventionally used for heat removal, to reduce the substrate loss. The technique increases the quality factor and inductance of the TSV inductor by up to 21x and 17x respectively. It enables us to implement TSV inductors of up to 38x smaller area and 33% higher quality factor, compared with spiral inductors of the same inductance. To the best of the authors' knowledge, this is the very first in-depth study on TSV inductors. We hope our study shall point out a new and exciting research direction for 3D IC designers.

ACKNOWLEDGMENTS

I would like to thank Dr. Shi for his guidance and direction during the pursuit of a Master of Science degree in Missouri University of Science and Technology. Without his support my work would have not been possible. I would also express my sincere gratitude to Dr. Jun Fan and Dr. Minsu Choi for being my committee members.

I would like to express heartfelt appreciation to my parents, who have supported me through my entire life, for their emotional and financial help during my master's work.

TABLE OF CONTENTS

Page

LIST OF ILLUSTRATIONS

Page

LIST OF TABLES

Page

1. INTRODUCTION

1.1. BACKGROUND

Three-dimensional integrated circuits (3D ICs) are generally considered to be most promising alternative that offers a path beyond Moore's Law. Instead of making transistors smaller, it makes use of the vertical dimension for higher integration density, shorter wire length, smaller footprint, higher speed and lower power consumption, and is fully compatible with current technology [1].

The through-silicon-vias (TSV) is a critical enabling technique for 3D ICs, which forms vertical signal, power and thermal paths. While many challenges still exist in 3D ICs, a big one is related to TSVs: they are large in size, typically 5-10x larger than the standard cells in 32nm process [8]. Yet their diameters do not scale with the devices due to imposed limitations of wafer handling and aspect ratios. International Technology Roadmap for Semiconductors (ITRS) suggests that the TSV diameter will remain almost constant in 2012-2015 [2]. On the other hand, a large number of TSVs are needed to deliver signal and power, to dissipate heat and to provide redundancy. Moreover, to guarantee high yield rate, foundries typically impose a *minimum TSV density rule*. For example, Tezzaron requires that at least one TSV must exist in every 250 um x 250 um area [3]. To satisfy this rule, lots of dummy TSVs need to be inserted, which further increase the area overhead.

To alleviate the problem, there have been efforts in the literature to make use of those dummy TSVs for alternative purposes. In this thesis, we are particularly interested in the application of TSVs towards on-chip inductors, which are the critical component in

various microelectronic applications, e.g. on-chip voltage regulators, voltage control oscillators, power amplifiers and radio frequency (RF) circuits.

Conventional implementation of on-chip inductors uses multi-turn planar spiral structure. This structure occupies a significant area and requires special RF process for higher quality factor. For example, [19] reported an inductor which occupies 78,400 um^2 routing area, equivalent to the area of 62K gates in 45 nm technology. In 3D ICs, however, it is possible to utilize through-silicon-vias (TSVs) to build vertical inductors [4-7]. One example of a toroidal TSV inductor in a two-tier 3D IC is shown in Figure 1.1 An apparent advantage of such TSV inductors is the minimal footprint on routing layers and accordingly high inductance density. However, since it is completely buried in the lossy substrate, its quality factor is inferior compared with that of the 2D spiral inductor. Accordingly, as pointed out in [7], TSV inductor can be used when area is the only concern. This essentially declares that such a TSV inductor is only a “fantasy”, useless in practice.

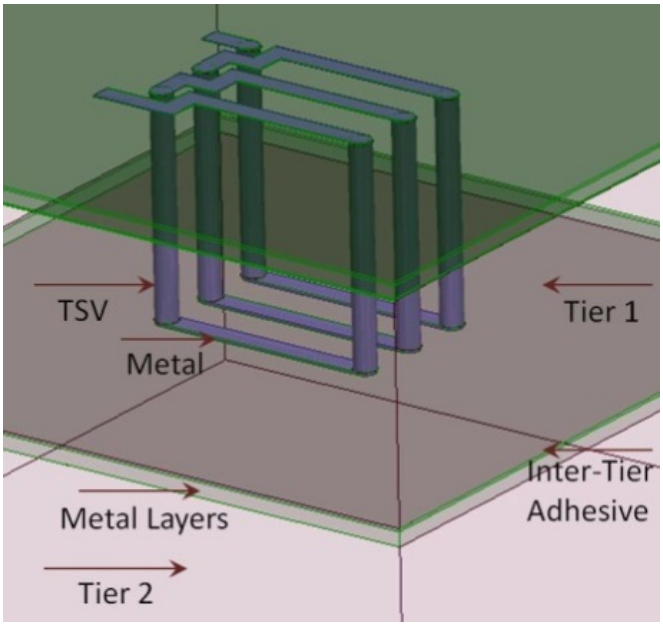


Figure 1.1 3D TSV inductor

1.2. MOTIVATION

Due to the limited space on an integrated circuit chip and highly competitive chip market, on-chip inductors must fit within a limited space and be inexpensive to fabricate. In that regard, it is desirable for an on-chip inductor to have a high inductance L per unit area. The spiral structure in a square shape can typically achieve lower than 100 nH/mm^2 density[1] [10, 11].

Another important inductor metric is the quality factor Q, which is the ratio of its inductive reactance to its resistance and is used to measure energy efficiency [10]. To achieve high quality factor, on-chip inductors are typically implemented using thick metal on top metal layers in RF process. To reduce the EM coupling between the inductor and any metal wires beneath it, Patterned Ground Shield (PGS) technique is typically used, further occupying valuable routing resources. The general structure of existing 3D TSV inductors [4-7] is shown in Fig. 1, which is composed of front/back metals and TSVs in a toroidal structure. The most attractive advantage of such a TSV inductor is its minimal footprint on the silicon surface. In addition, no PGS is necessary as the majority of the magnetic flux run in parallel with metal wires (in the horizontal plane).

However, all existing works [4-7] simply conduct case studies on a few selected geometries, and no systematic conclusions have been drawn on how various parameters would affect the performance of the TSV inductor. It is not clear yet whether the new TSV inductor structure will result in different behaviors with respect to these parameters. In addition, there are a few parameters that are unique to TSV inductors such as the TSV

[1] Inductance density up to 1700 nH/mm^2 can be achieved by magnetic cores [18], but would require nonconventional processes.

liner thickness. We argue that these issues need to be fully explored to help circuit designers understand the behavior of the TSV inductor and make better use of it.

Moreover, according to the literature, the quality factor of the TSV inductor is significantly less than its 2D spiral counterpart, mainly due to the loss from the substrate. Unlike the 2D spiral inductor, the entire TSV inductor is buried in the silicon substrate, which is lossy at high frequencies. As a result, Bontzios et al [7] suggested that for 50 um substrate thickness and below, TSV inductor should be used when area is the only concern, which means it is of little practical value. One question that rises here is: *Is there any way that we can reduce substrate losses for TSV inductors, so that their quality factor can be at par or even better compared with spiral inductors for practical use?*

1.3. LITERATURE REVIEW

1.3.1. On-chip planar inductors. Inductors are considered vital components in analog, RF, and microwave circuits. The on-chip 2D inductors have become widely used due to its relatively simple integration with existing CMOS capabilities and processing steps. There have been numerous publications on inductor design. The most widely used type is the spiral inductor; Figure 1.2 illustrates the layout for square, hexagonal, octagonal and circular spirals, which are common in modern IC devices [21]. The shape of inductor is often limited to the availability of fabrication processes, although a circular shaped inductor may be more efficient and yield better performance [22]. Design parameters such as number of turns, the separation between adjacent turns (or loop pitch), outer dimension and substrate conductivity are all important factors in determining the performance of on-chip inductors.

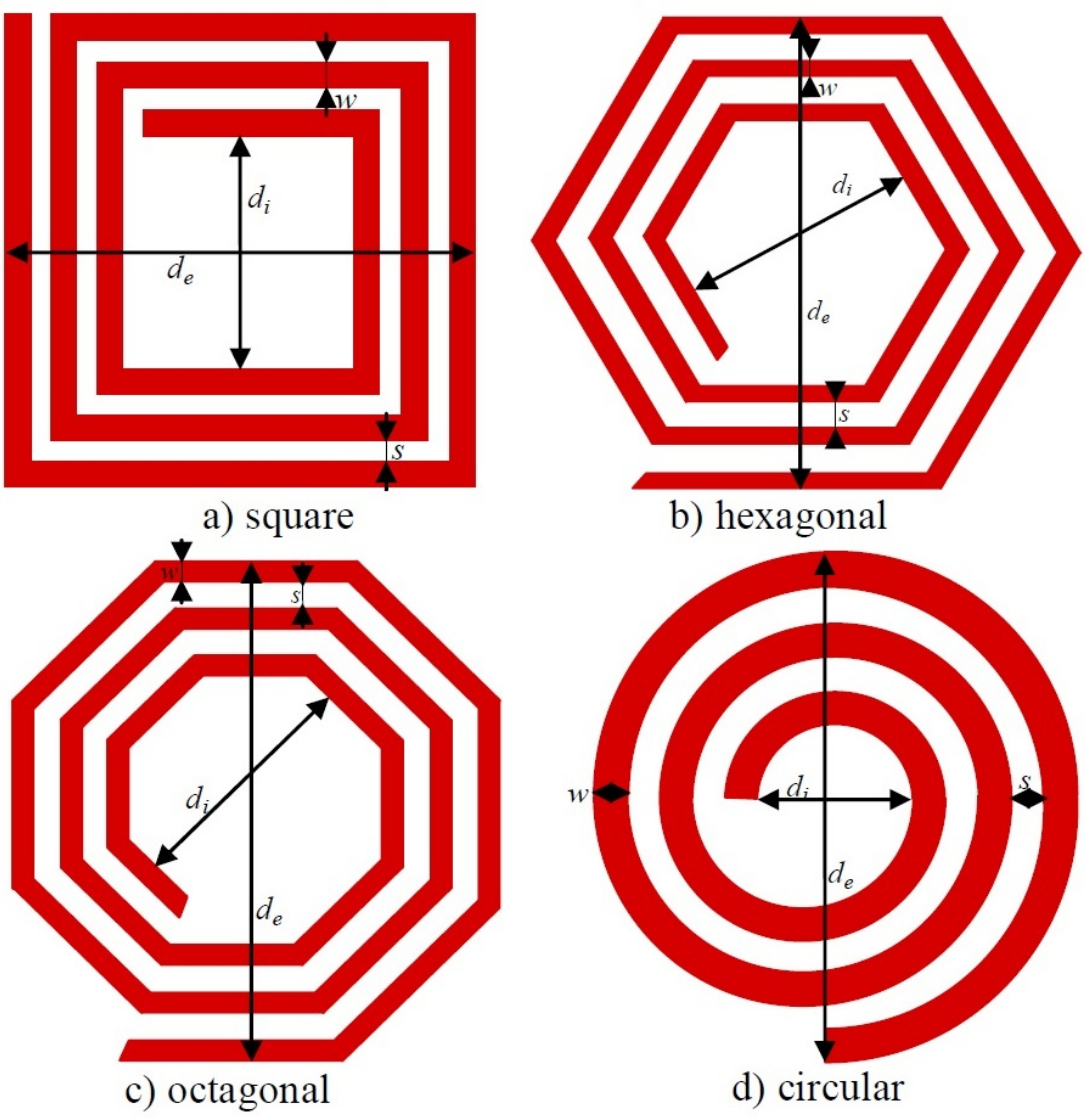


Figure 1.2 4 layout shapes of spiral inductors

1.3.2. Patterned Ground Shield. In the literature, it is shown that energy loss can be reduced by shielding the electric field of the inductor from the silicon substrate. The ground shield is patterned with slots orthogonal to the spiral. Those slots act as an open circuit to cut off the path of the induced loop current. As a typically used technique, PGS can improve the quality factor and isolation of an inductor. However, the skin effect will

result in reduction of the inductance [20], because of a decrease in magnetic intensity in the space of PGS layer. In addition, to achieve the integrity of the ground connection, which is the fundamental of this technique, it will further occupy valuable routing resources.

1.4. THESIS ORGANIZATIONS

To make TSV inductors “real”, two fundamental questions need to be understood: First, what are the parameters that can effectively improve the TSV inductor performance? Second, is there any shield mechanism that can be used to reduce substrate loss? This thesis provides answers to both questions. Specifically, the main contributions of our work are as follows.

First, we use ANSYS full-wave simulation to systematically study how the inductance and the quality factor of the TSV inductor are affected by various process parameters and design parameters. A few interesting phenomena that are unique to TSV inductors can be observed. The conclusions drawn can provide guidance to inductor designers as well as information for dedicated process development towards better TSV inductors.

Second, we put forward a novel shield technique using the micro-channel, which has been used in 3D IC industry including IBM and Nanonexus as a low-cost cooling technique [16], to reduce the substrate loss. Experimental results indicate that it can boost the quality factor and the inductance of the TSV inductor by up to 21x and 17x respectively. It changes the TSV inductor concept from just a fantasy to something practical - with the technique, TSV inductors can achieve up to 38x smaller area and 33% higher quality factor, compared with spiral inductors of the same inductance. This

suggests that TSV inductors with micro-channel shields are a much better option than spiral inductors in 3D ICs.

To the best of the authors' knowledge, this is the very first in-depth study on TSV inductors, along with a way to make them practical in 3D ICs.

The remainder of the thesis is organized as follows. Section 1 reviews the existing efforts on the TSV inductor and the motivation of our work. Section 2 systematically studies how various process and design parameters affect their performance. Section 3 proposes a novel micro-channel shield mechanism to increase the inductance and the quality factor of the TSV inductor. The concluding remarks are given in Section 4.

2. IMPACT OF PROCESS AND DESIGN PARAMETERS

2.1. INTRODUCTION

In this chapter, we will study how various process and design parameters affect the inductance, the quality factor, as well as the self-resonance frequency (SRF)[2] of the TSV inductor. All the simulations in this thesis are done using ANSYS full-wave simulator HFSS [9] with mixed order basis function. Our machine is a 64-bit Dell T7500 Windows server with 2.4 GHz duo-core Xeon CPU and 96 GB memory. For clarity purposes, we outline the parameters of study in Table 2.1. The practical range of interest for each parameter is also listed.

Table 2.1 List of parameters, the respective default unit and ranges of interest

Type	Notation	Meaning	Range
Process	H (um)	Substrate height	30-120
	σ (S/m)	Substrate conductivity	0-10,000
	D (um)	TSV diameter	2-15
	d (um)	Liner thickness	0.2-0.7
Design	N	Number of turns	1-6
	T	Number of tiers	2-4
	P(um)	Loop pitch[3]	13-23
	W(um)	Width of metal strip	3-12
	f(GHz)	Operating frequency	0.15, 1, 5, 10

[2] The Self-resonant frequency (SRF) of an inductor is defined as the critical frequency when it ceases to behave like an inductor.

[3] Loop pitch is defined as the separation between adjacent turns.

There are four things worthwhile to note here: 1) While existing works only use two tiers (T=2) to implement the inductor, in this thesis we extend the study to designs of up to four tiers (according to [17], 3D ICs of up to five tiers have already been fabricated). Since the bottom tier does not need any TSV, the actual inductor is formed in the top T-1 tiers. 2) To achieve maximum quality factor, the cross-sectional area should be square. In other words, once we fix the number of tiers T, the TSV pitch should be (T-1)H, where H is the height of a single tier. 3) The substrate height and the TSV diameter are chosen such that the TSV aspect ratio (AR) is between 5:1 and 20:1, in accordance with ITRS [2]. 4) The 150 MHz operating frequency represents applications such as on-chip voltage regulator applications, while 1/5/10 GHz represent resonant clocking or RF applications.

To study the impact of various parameters, we use the control variable method to change one parameter at a time. The nominal settings are illustrated in Fig. 2:

Process parameters: H = 60 um, σ = 10 S/m, D = 6 um, d = 0.2 um.

Design parameters: N = 1, T = 2, P = 18 um (not shown), W = 6 um.

In addition to these parameters of study, for each tier we assume a normal process with 8 metal layers. The metal layers have a total thickness (including field dioxide) of 4 um. The metal strips connecting TSVs are implemented using M1 (0.3 um thick) and backside metal (0.8 um thick)[4].

The corresponding inductance and quality factor vs. frequency plot for the above nominal settings are shown in Figure 2.1 and Figure 2.2.

---

[4] These values are extracted and modified slightly from the datasheet of a real process in order to protect the confidential information while making the studies practical.

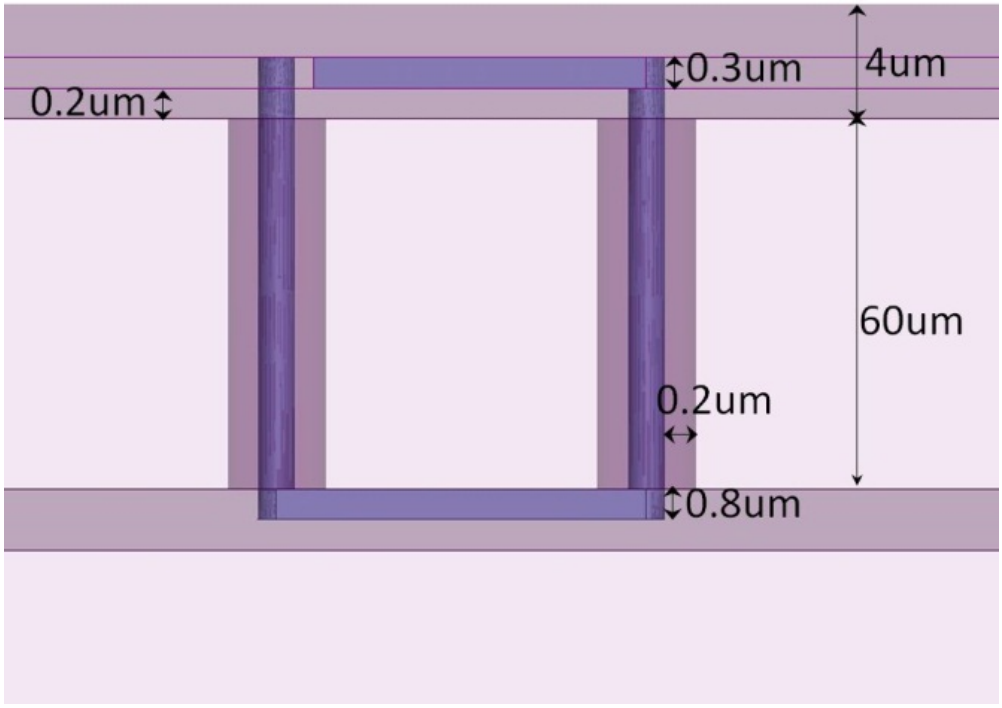


Figure 2.1 Nominal settings (not to scale)

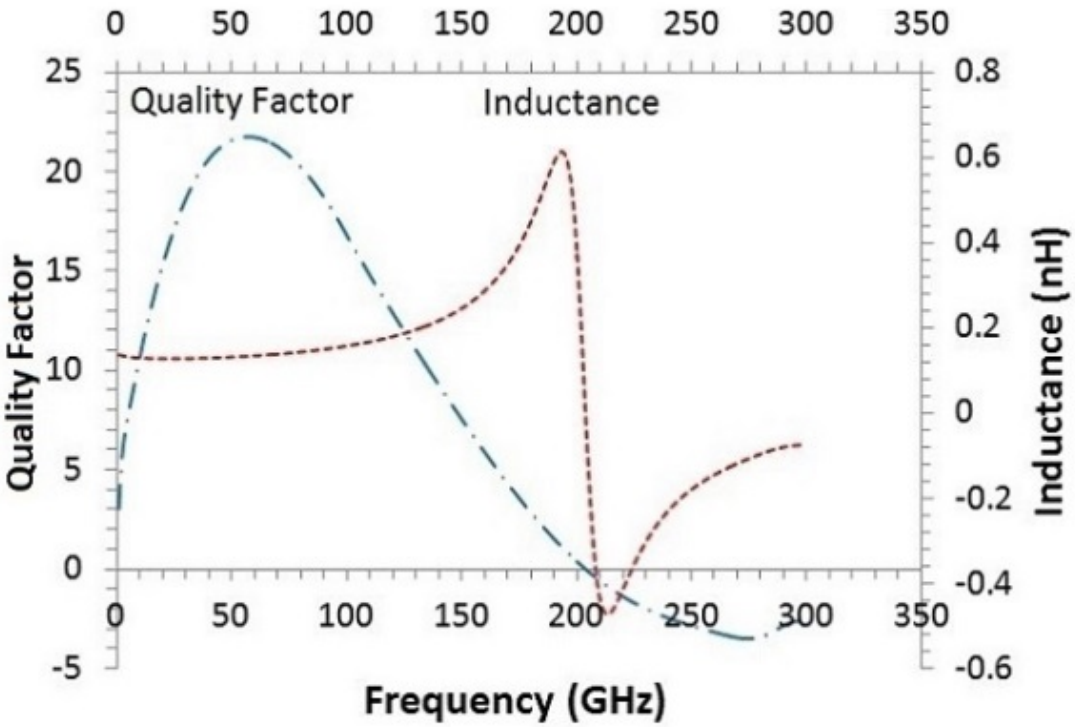


Figure 2.2 Quality factor and inductance vs. frequency for the TSV inductor with nominal settings

2.2. PROCESS PARAMETERS

In this section, we study the impact of process parameters on the inductance, quality factor and self-resonant frequency of the TSV inductor, hoping to suggest directions for dedicated 3D TSV inductor process development in the near future.

2.2.1. Substrate Height (H). The quality factor and the inductance for different substrate heights and operating frequencies are shown in Figure 2.3. Based on the analogy to the spiral inductors, the inductance should be proportional to Hln(H). This can be clearly verified by curve fitting, where L = 0.0006Hln(H)-0.0115 according to the fitting result. In this equation and all the remaining equations throughout the thesis, L takes the unit nH. All the parameters take the unit listed in Table 2.1.

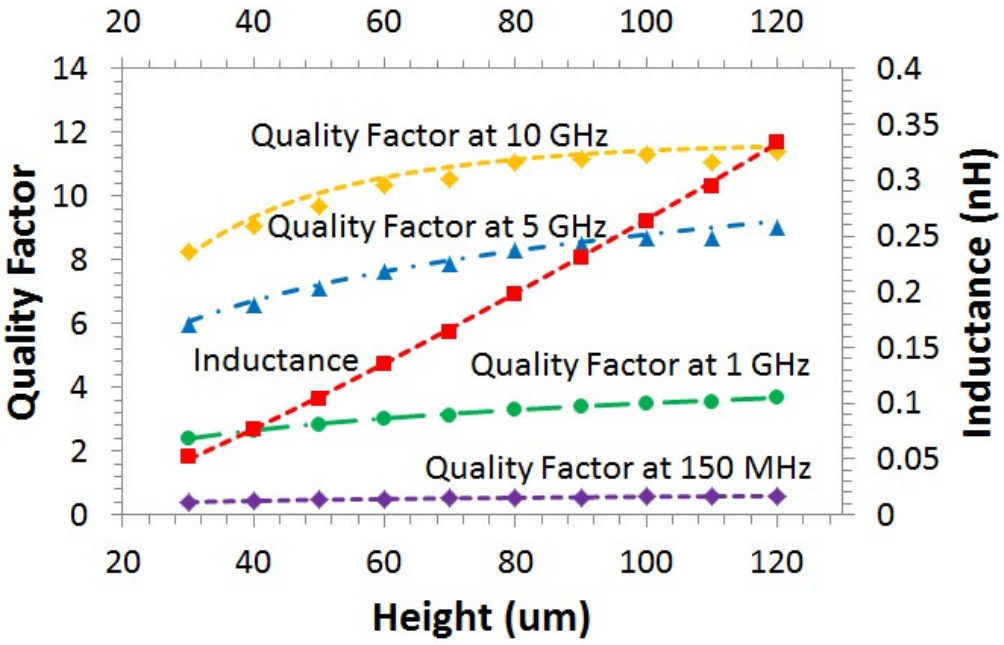


Figure 2.3 Quality factor and inductance vs. substrate height

In terms of quality factor, it increases with H, but at different rates for different frequencies. At higher frequency, the quality factor is larger and the slope w.r.t. H is higher. According to fitting, Q should be proportional to ln(H). At 150 MHz, Q = 0.14ln(H) – 0.07. At 1 GHz, Q = 0.93ln(H) – 0.76. At 5 GHz, Q = 2.27ln(H) – 1.66. At 10 GHz, Q = 30.00ln(H) – 43.58.

Finally, although not shown in the figure, we note that self-resonant frequency decreases from over 250 GHz to 100 GHz when H increases from 30 um to 120 um.

Observation 1: For the range of interest, increasing substrate height increases both the inductance and the quality factor, but reduces the self-resonant frequency.

2.2.2. Substrate Conductivity (σ). The quality factor and the inductance for different substrate conductivities and operating frequencies are shown in Figure 2.4. From the figure, we can see that the inductance is not directly impacted by σ (L = 0.13 nH).

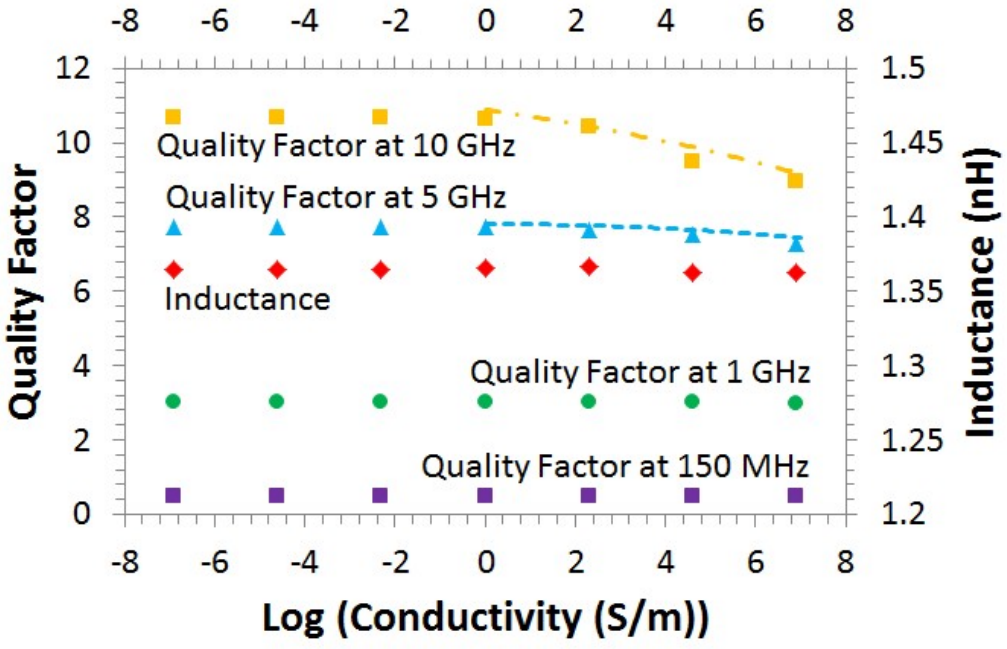


Figure 2.4 Q and L vs. substrate conductivity σ (note that log-scale is used for the x-axis)

On the other hand, when σ is low (corresponding to the lightly doped substrate) or when the frequency is low (150 MHz or 1 GHz), the quality factor almost remains constant, because in this region the quality factor loss is mainly due to the ohmic loss in the inductor. When both σ and the frequency are high, the quality factor decreases with, at higher rate for higher frequencies. This is due to the fact that in this region, the loss mainly occurs in the substrate. For 5 GHz and 10 GHz, we choose the last four points with highest σ to fit the trend. Fitting results suggest that at 5 GHz, Q = -0.008(lnσ)2 + 0.005(lnσ) + 7.802. At 10 GHz, Q = -0.012(lnσ)2 - 0.163(lnσ) + 10.880. The log functions indicate the changes w.r.t. are gradual.

Finally, although not shown in the figure, we note that self-resonant frequency decreases from over 200 GHz to 60 GHz when increases from 0 S/m to 10,000 S/m.

Observation 2: For low substrate doping density (σ < 10 S/m) or low frequency (<1GHz), the ohmic loss of the inductor dominates. When the doping density is high and the frequency is high, the substrate loss dominates.

Observation 3: For the range of interest, increasing substrate conductivity does not change the inductance, and has little impact on the quality factor at low frequency or low substrate conductivity. It reduces the quality factor gradually at high frequency for high substrate conductivity. The self-resonance frequency drops with the increase of substrate conductivity.

2.2.3. TSV Diameter (D). The quality factor and the inductance for different TSV diameters and operating frequencies are shown in Figure 2.5. Based on the analogy to the spiral inductors (metal width), the inductance should be proportional to ln(H/D). This can

be clearly verified by curve fitting, where L = 0.018ln(60/D)+ 0.093 according to the fitting result.

In terms of quality factor, the quality factor should increase with D as the resistance of the inductor becomes smaller. Fitting results suggest that at 150 MHz, Q = -1.399D0.28 ln(H/D) +5.906. At 1 GHz, Q = 1.583D0.66 ln(H/D) -8.593. At 5 GHz, Q = 0.233D1.23 ln(H/D) + 2.760. At 10 GHz, Q = 0.133D1.54 ln(H/D) +6.230. Apparently, at higher frequency, the quality factor is larger and the slope w.r.t. D is higher. The larger slope is due to the effect of further AC resistance reduction from substrate coupling at higher frequencies.

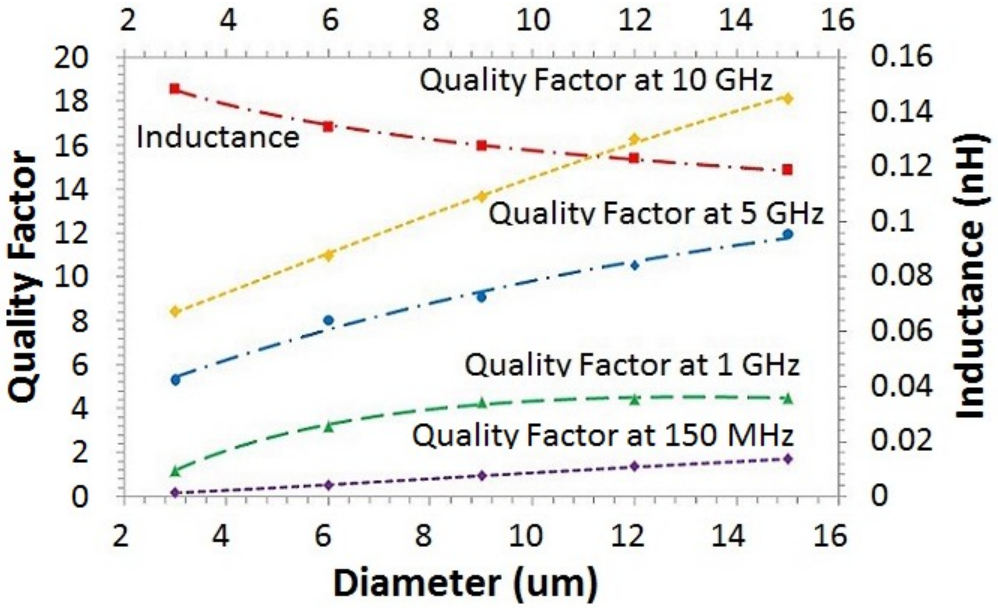


Figure 2.5 Q and L vs. diameter D

Finally, although not shown in the figure, we note that self-resonant frequency is almost constant (~200 GHz) for our diameter range (3um-15um).

Observation 4: For the range of interest, increasing TSV diameter reduces the inductance, increases the quality factor, and does not change the self-resonant frequency significantly.

2.2.4. Liner Thickness (d). The quality factor and the inductance for different liner thickness and operating frequencies are shown in Figure 2.6. This parameter is unique to the TSV inductor and based on the plot, it can be seen that d has little impact on the inductance and the quality factor. It also has subtle impact on the self-resonant frequency.

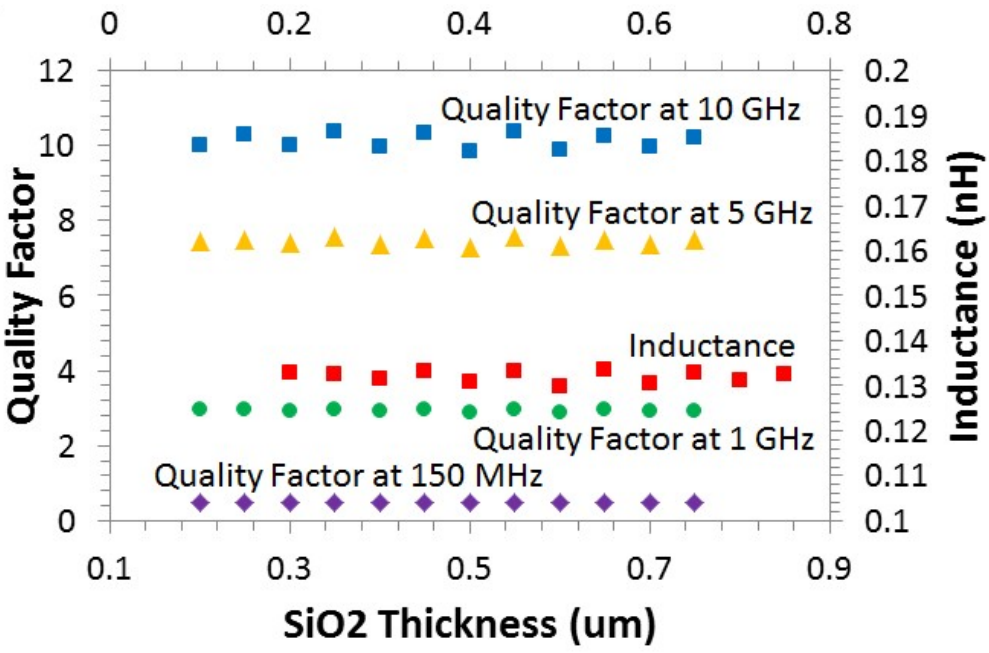


Figure 2.6 Q and L vs. linear thickness d

Observation 5: For the range of interest, TSV liner thickness has subtle impact on the TSV inductor behavior.

2.3. DESIGH PARAMETERS

2.3.1. Number of Turns (N). The quality factor and the inductance for different number of turns and operating frequencies are shown in Figure 2.7. Based on the analogy to the 2D spiral inductors, inductance should be proportional to N2. However, fitting results suggest that L = 0.14N1.3, which is due to other non-ideal factors such as capacitive coupling and the loop pitch P (separation between the TSV turns).

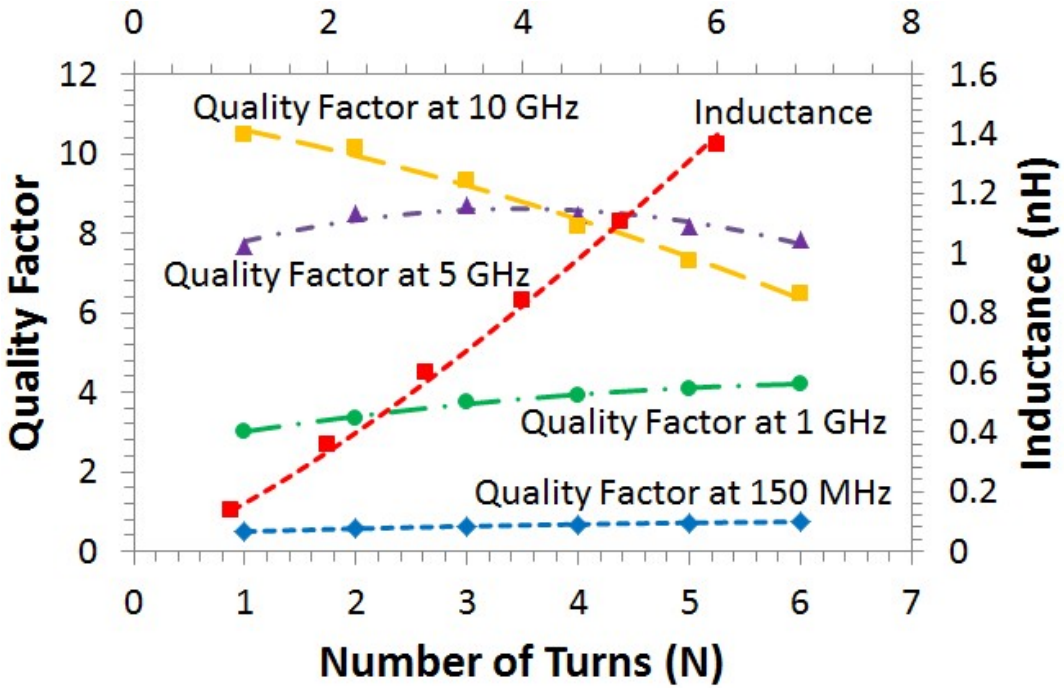


Figure 2.7 Q and L vs. number of turns N

In terms of quality factor, a few interesting phenomena can be observed. First, there exists a particular N_c that gives maximum quality factor. Second, such N_c decreases with the frequency. At 150 MHz and 1 GHz, it is over 6 (beyond the scope of the plot) and as a result, the quality factor increases monotonically with N within our range of

interest. At 5 GHz, the peak quality factor is reached at N_c = 3. At 10 GHz, it drops to 1, and thus the quality factor monotonically decreases with N. Third, for higher frequency, the quality factor changes (either increases or decreases) faster with N. We find that the trend can be best fitted with quadratic functions, where at 150 MHz Q = -0.006N2 + 0.093N + 0.409. At 1 GHz, Q = -0.036N2 + 0.489N + 2.560. At 5 GHz, Q = -0.136N2 + 0.939N + 6.996. At 10GHz, Q = -0.051N2 - 0.496N + 11.140.

Finally, although not shown in the figure, we note that self-resonant frequency is decreasing from over 200 GHz to 40 GHz when N increases from 1 to 6.

Observation 6: For the range of interest, increasing the number of turns N increases the inductance. There might exist a critical number of turns N_c that gives maximum quality factor, and such N_c decreases with the frequency. The self-resonance frequency drops rapidly with the increase of N.

2.3.2. Number of Tiers (T). The quality factor and the inductance for different number of tiers and operating frequencies are shown in Figure 2.8. The parameter T looks similar to the TSV substrate height H, but it is the non-conducting inter-layer adhesive that makes it different. We can expect that the adhesive layer should have little impact on the inductance, but big impact on the quality factor. Fitting results suggest that L = 0.105TlnT -0.006.

In terms of the quality factor, first, there exists a particular T_c that gives maximum quality factor. Second, such T_c decreases with the frequency. At 1 GHz, it is over 6 and as a result, the quality factor increases monotonically with T. At 5 GHz, the peak quality factor is reached at T_c = 4. At 10 GHz, it drops to 3. Third, for higher frequency, the quality factor changes (either increase or decrease) faster with T. We find that the trend

can be best fitted with cubic functions, where at 150 MHz, Q= 0.002T3 -0.038T2 + 0.259T + 0.116. At 1 GHz, Q = 0.015T3 -0.270T2 + 1.758T + 0.475 . At 5 GHz, Q = -0.055T3 + 0.102T2 + 1.810T + 4.131. At 10 GHz, Q = 0.260T3 -3.417T2 + 13.200T - 4.358.

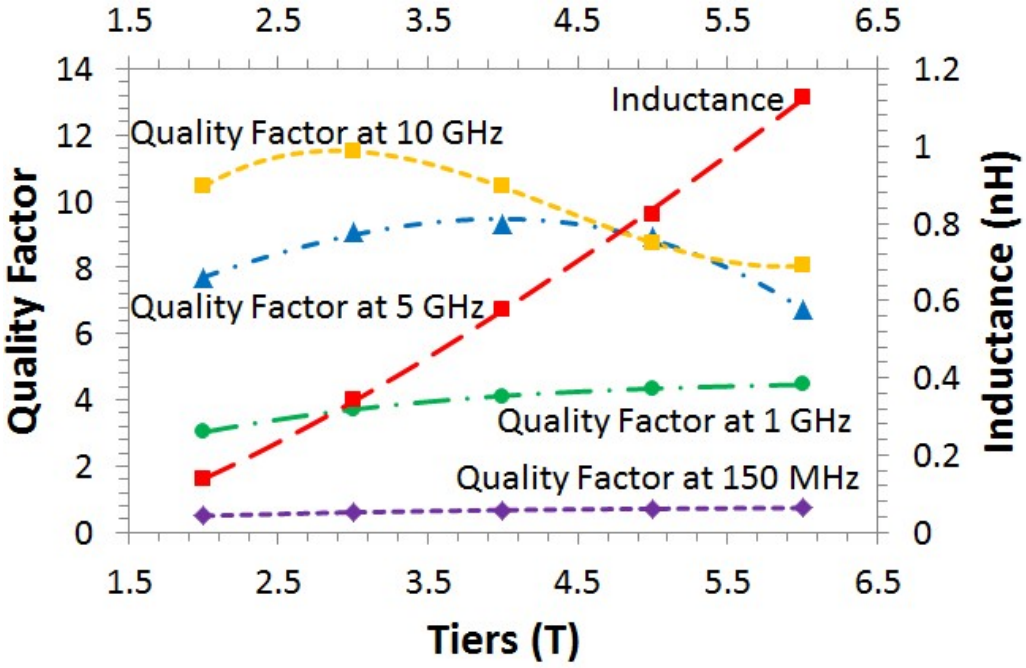


Figure 2.8 Q and L vs. number of tiers T

Finally, although not shown in the figure, we note that self-resonant frequency decreases from over 250 GHz to 38 GHz when T increases from 2 to 6.

Observation 7: For the range of interest, increasing the number of tiers T increases the inductance. There might exist a critical number of tiers T_c that gives maximum quality factor, and such T_c decreases with the frequency. The self-resonance frequency drops rapidly with the increase of T.

Before we continue, one more thing we would like to study is how T_c changes with different N, and how N_c changes with different T, at the same frequency. We again vary N and T based on nominal setting to perform simulation, and the results at 5 GHz are reported in Table 2.2 and Table 2.3, respectively. We also include the corresponding Qmax at T_c (or N_c). From Table 2.2, it can be seen that with more turns, the number of tiers that gives maximum quality factor decreases. Similarly, from Table 2.3, with more tiers, the number of turns that gives maximum quality factor decreases.

Table 2.2 t_c and q v.s. n (measured at 5 GHz)

N	1	2	3	4	5
T_c	4	2	2	2	2
Q_{max}	9.32	8.50	8.77	8.60	8.23

Table 2.3 N_c and q v.s. t (measured at 5 GHz)

T	2	3	4	5
N_c	3	1	1	1
Q_{max}	8.77	9.11	9.32	8.95

2.3.3. Loop Pitch (P). The quality factor and the inductance for different loop pitches and operating frequencies are shown in Figure 2.9. This is a unique parameter for the TSV inductor. If the loop pitch increases, the inductance decreases slightly, mainly due to the reduced magnetic flux. Fitting results suggest that the inductance follows the quadratic trend L= 0.0003P2 -0.0122P + 0.5019.

On the other hand, the quality factor decreases with the increase of P at lower frequencies and remains almost constant at higher frequencies. This is because at lower

frequencies the loss is mainly due to the metal resistance which increases with P. At higher frequencies, the substrate loss starts to dominate, which decreases with the magnetic flux (with the increase of P). It conforms to our observation 2. Fitting results suggest that at 150MHz, Q = -3.3x10-5P3+ 0.002P2- 0.053P + 1.000. At 1 GHz, Q = -0.0001P3 + 0.0060P2 - 0.1740P + 4.9130. At 5 GHz and 10 GHz, it is almost constant.

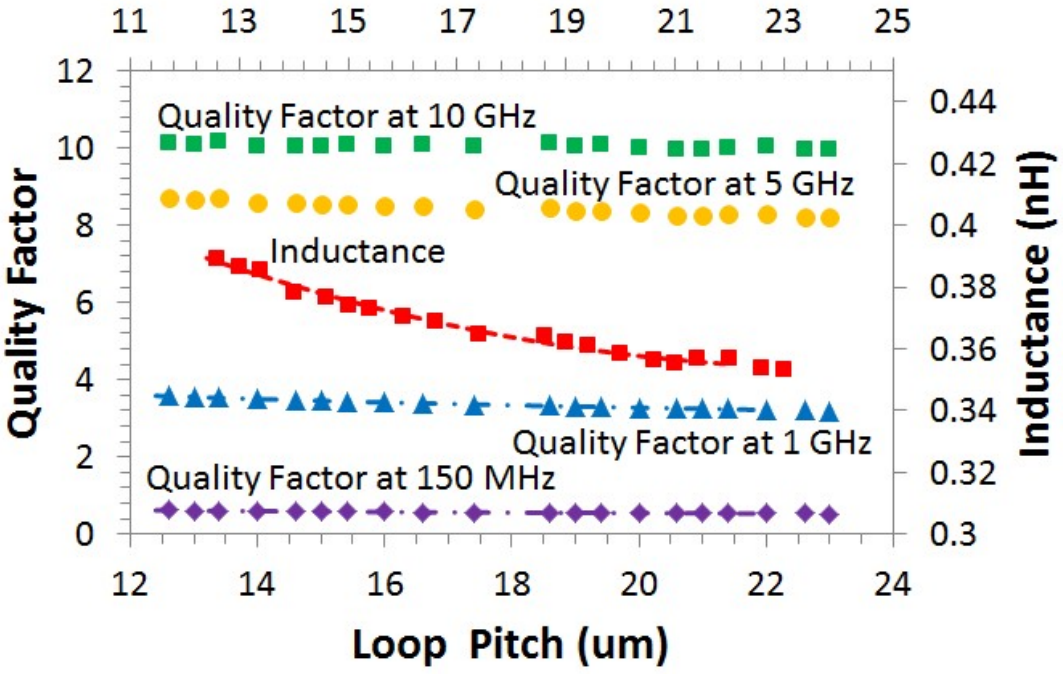


Figure 2.9 Q and L vs. loop pitch P

Finally, we note that the self-resonant frequency remains almost constant (~250 GHz).

Observation 8: For the range of interest, increasing the loop pitch P slightly decreases the inductance. The quality factor also slightly decreases with P at low

frequency, and remains almost constant at high frequency. The self-resonance frequency does not change significantly with P.

2.3.4. Metal Width (W). The quality factor and the inductance for different metal widths and operating frequencies are shown in Figure 2.10. The inductance should decrease as W increases due to the increased capacitive coupling. According to the fitting results, the value of inductance follows the quadratic trend where L = 0.0005W2 - 0.0117W + 0.1907.

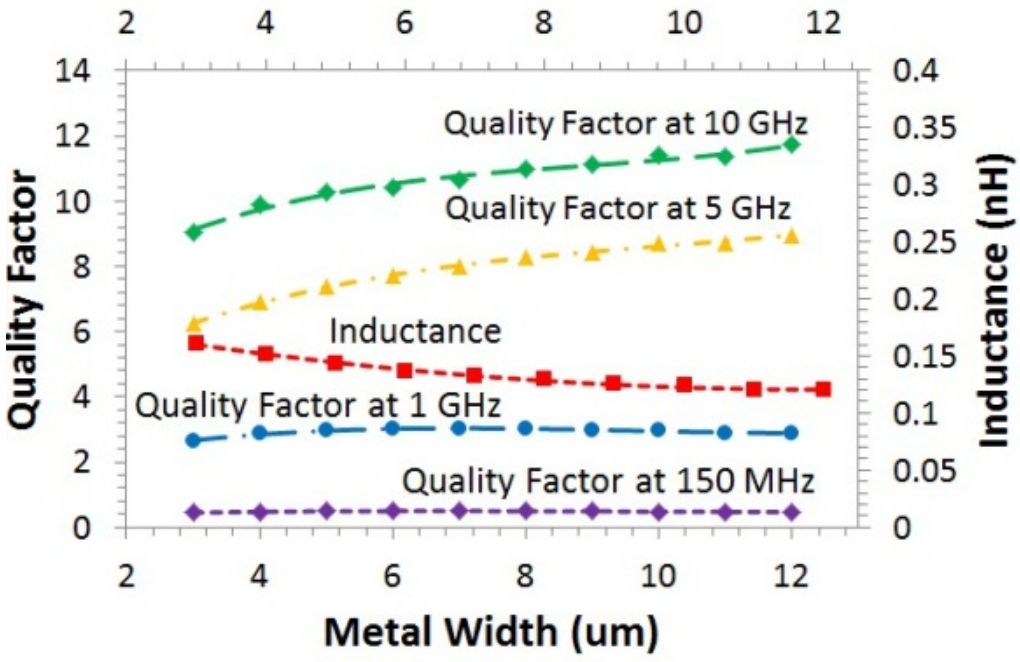


Figure 2.10 Q and L vs. metal width (W)

In terms of quality factor, it should increase with W as the ohmic loss becomes smaller. The impact of W on Q also becomes more profound at higher frequency. Fitting results suggest that the quality factor almost remains constant at 150 MHz. At high

frequency, the quality factor increases with cubic trend, which is due to the effect of further AC resistance reduction from substrate coupling. At 1 GHz, Q = 0.002W3 - 0.056W2 + 0.499W + 1.619. At 5 GHz, Q = 0.003W3 - 0.104W2 + 1.200W + 3.471. At 10 GHz Q = 0.006W3 -0.146W2 + 1.435W + 5.977.

Observation 8: For the range of interest, increasing the metal width W decreases the inductance, and has little impact on the quality factor at low frequency. It increases the quality factor at high frequency. The self-resonant frequency does not change with W significantly.

3. LOSS REDUCTION VIA MICRO-CHANNEL SHIELD

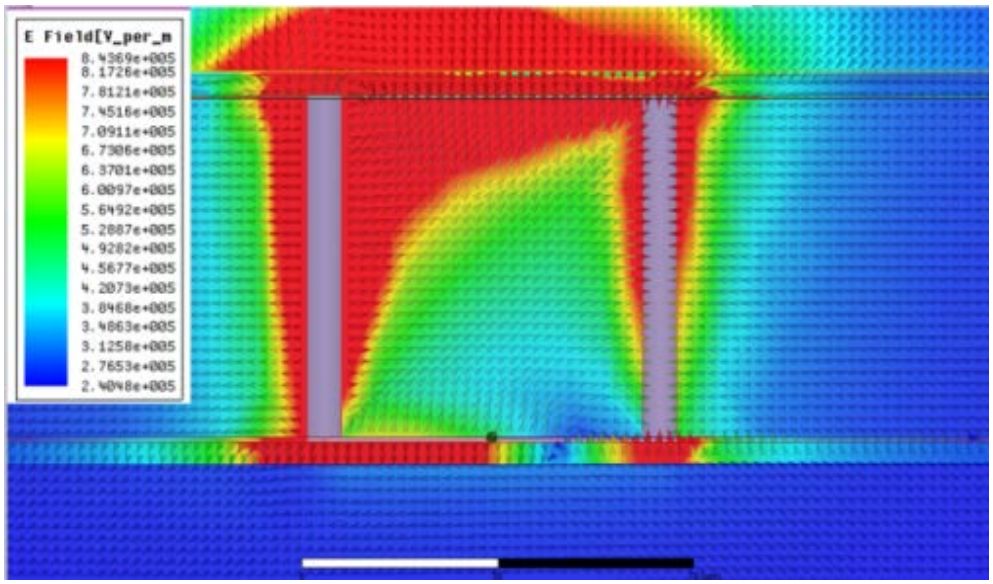
3.1. INTRODUCTION

From Observation 2 in Section 3, the substrate loss dominates when the frequency is over 1 GHz and when the substrate conductivity is over 10 S/m (which is normal for digital applications). In other words, the TSV inductor is subject to severe efficiency loss over 1 GHz. To tackle the issue, we are interested in devising effective shield mechanism to reduce substrate loss.

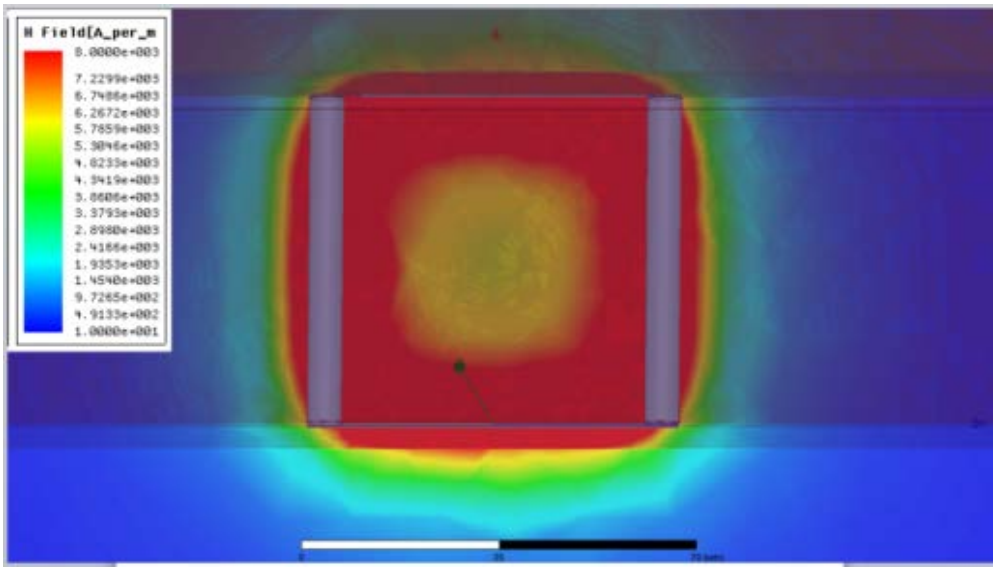
3.2. PRINCIPLES AND METHODOLOGY

To help understand the distribution of eddy current in the TSV inductor, we simulate it with the nominal setting shown in Section 3. The resulting E and H fields are plotted in Figure 3.1(a) and (b), respectively. From the figure, we can see clearly that the E field decreases as we get farther from the TSVs, while the H field completely penetrates through the area between the TSVs. As such, we can expect that most of the eddy current loss comes from the silicon substrate near the TSVs, which inspires us to think: Why not remove the silicon substrate in that area?

This reminds us about a seemingly irrelevant technique, micro-channel, which has been widely used as a low-cost heat-removal technique in 3D ICs (e.g.[12, 13]). Simply speaking, the technique etches a channel from the bottom surface of the substrate for liquid cooling and only requires extra two lithography steps, which are relatively cheap to implement. The fabrication process of micro-channel is already mature–an example of such process from IBM and Nanonexus is shown in Figure 3.2[16].



(a)



(b)

Figure 3.1 E field (a) and H field (b) distributions

In our situation, we can place such channels adjacent to the TSVs to remove part of the substrate. Specifically, we etch four identical channels, one on each side of the two TSVs. An illustration of such a structure is shown in Figure 3.3 for a two-tier design. For

multiple tiers, we need to place four channels at each tier, adjacent to the TSVs. The micro-channels can either be filled with coolant like conventional micro-channels, or just open with air. Note that these channels are etched on the backside of the silicon substrate, and will not affect any devices.

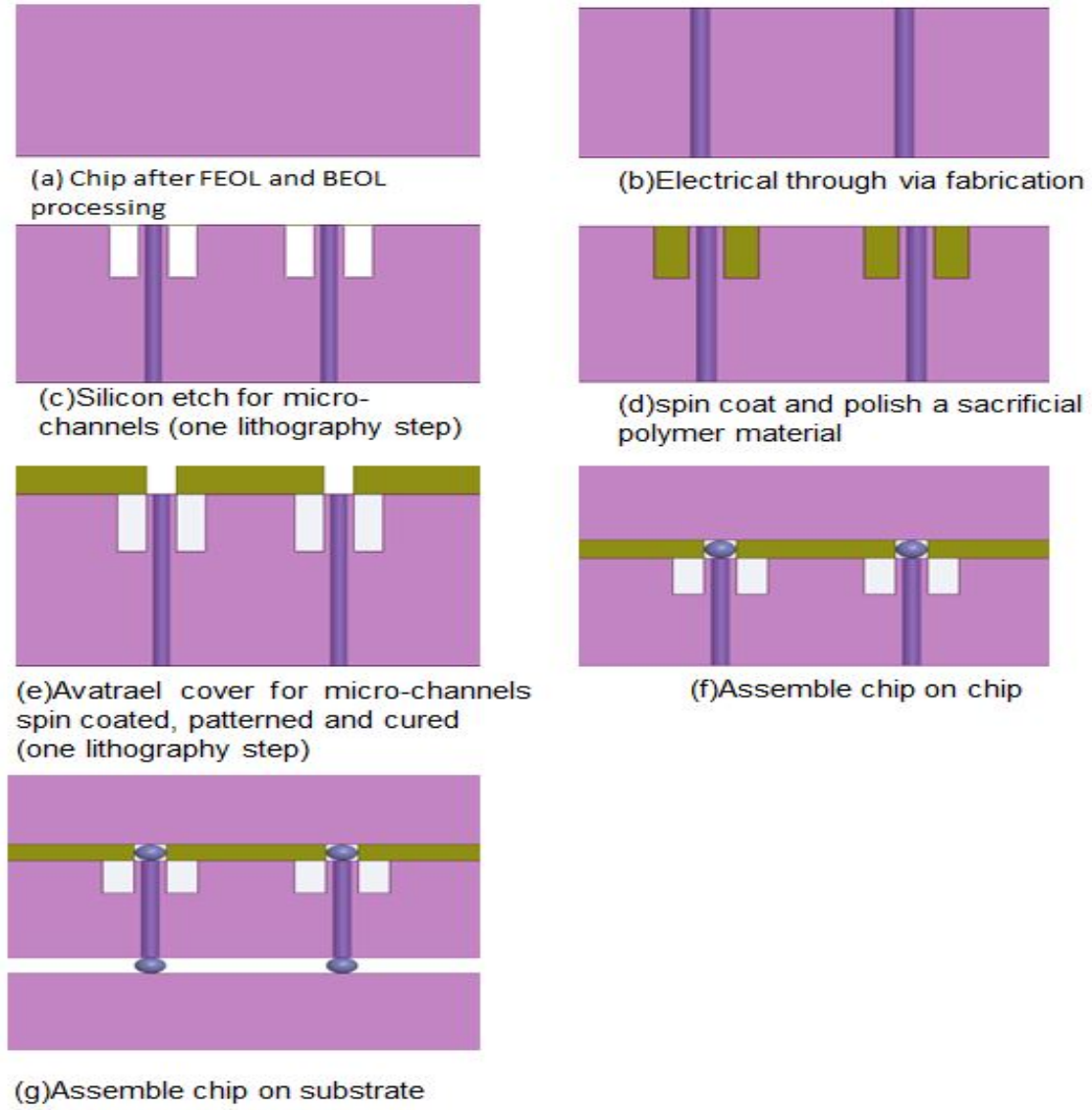


Figure 3.2 Micro-channel fabrication steps (only two extra lithography steps (c) and (e) are required) [16]

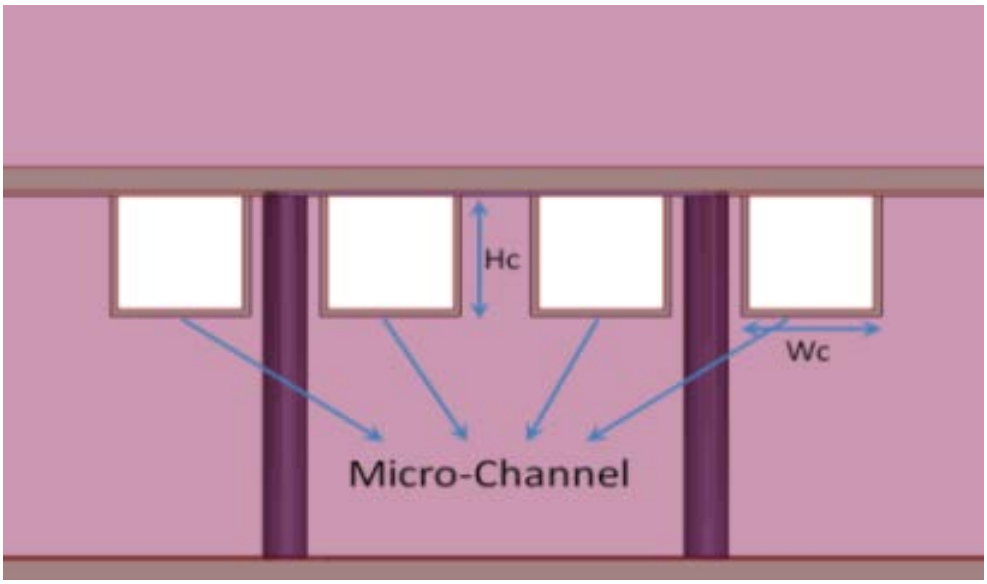


Figure 3.3 Micro-channel shields for substrate loss reduction

An extra benefit of such technique is the reduced temperature at the inductor. When inductors are used to form antennas, they typically bear high temperature [14]. Accordingly, with the micro-channels the heat will be able to dissipate faster.

3.3. SIMULATION RESULTS AND DISCUSSION

To verify the effectiveness of this approach, we simulate the eddy current in TSV inductors with micro-channels with the nominal settings in Section 3. The resulting E and H fields are plotted in Figure 3.4 and Figure 3.5, respectively. From the figures we can see that the E filed decreases much as we introduce the micro-channel while the H field still completely penetrates through the area between the TSVs. The comparison shows the improvement over the one without micro-channel.

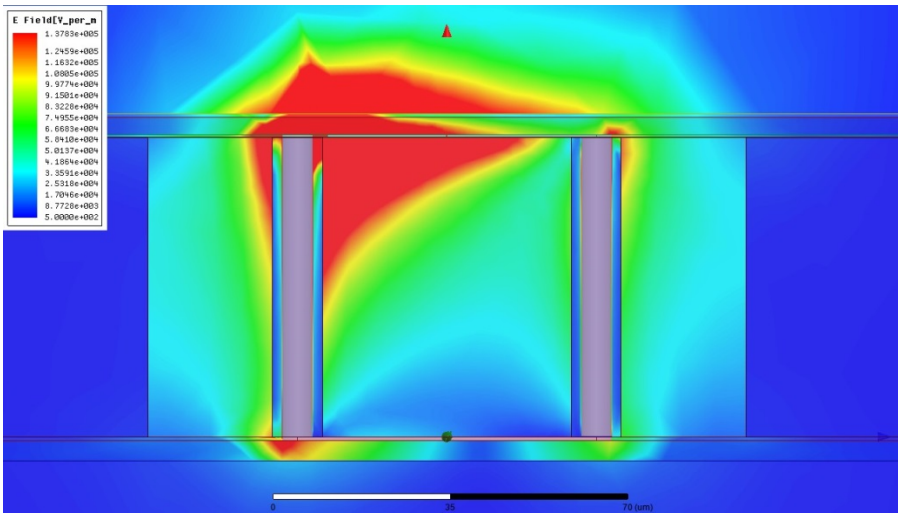


Figure 3.4 E field distributions of TSV inductors with micro-channel

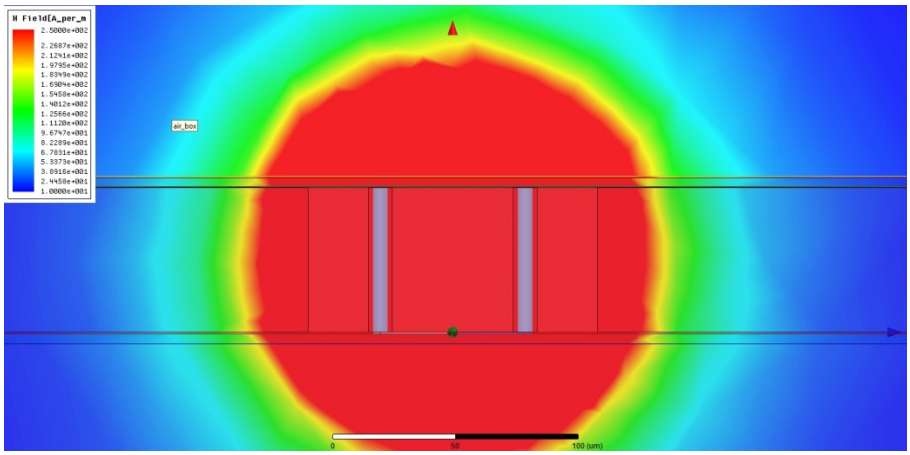


Figure 3.5 H field distributions of TSV inductors with micro-channel

Furthermore, we vary the height (H_c) and the width (W_c) of the four micro-channels and compare the improvement of Q and L at 10 GHz based on a structure with two tiers (T=2) and six turns (N = 6). All the other parameters conform to the nominal settings discussed in Section 3. The micro-channels are placed 5um from TSV center to the nearer edge of the channel. The resulting Q and L are reported in Table 3.1. The

improvements over the case without micro-channel shields are also reported in parentheses. From the table, we can easily see that both channel height and width have profound impact on Q. For the maximum height of 60 um and width of 25 um, a 71.0% improvement of Q over the TSV inductor without micro-channel can be observed. Considering reliability and manufacturability, the aspect ratio of the channel is limited [15]. Accordingly, designers should carefully consider the tradeoff between the micro-channel dimension and Q. On the other hand, L remains almost constant with various W_c and H_c.

Table 3.1 Q and L vs. micro-channel dimension (10 GHz, N = 6, T = 2).The relative improvement over the case without micro-channel shields is reported in parentheses.

		W_c (um)					
		Quality Factor			Inductance (nH)		
		10	20	25	10	20	25
H_c (um)	10	6.71 (4.5%)	6.92 (8.1%)	7.03 (9.6%)	1.396 0.0%	1.395 0.0%	1.394 0.0%
	20	7.02 (9.6%)	7.29 (13.8%)	7.46 (16.3%)	1.393 0.0%	1.390 0.0%	1.390 0.0%
	30	7.34 (14.6%)	7.76 (21.1%)	7.94 (23.9%)	1.391 0.0%	1.386 0.0%	1.384 0.0%
	40	7.73 (20.5%)	8.28 (29.2%)	8.59 (34%)	1.388 0.0%	1.386 0.0%	1.382 0.0%
	50	8.25 (28.8%)	8.98 (40.1%)	9.41 (46.1%)	1.388 0.0%	1.380 0.0%	1.376 0.0%
	60	9.12 (42.2%)	10.34 (61.4%)	10.96 (71.0%)	1.386 0.0%	1.374 0.0%	1.377 0.0%

We further study how Q and L change when using maximum micro-channel dimensions for different number of turns N, number of tiers T and frequency f. The results on Q and L at 10 GHz are reported in Tables 3.2 and Table 3.3, respectively. To show the effect at different frequencies, the results on Q at 1 GHz are reported in Table

VII. Note that we omit the table for L at 1 GHz as it remains constant with or without the micro-channel. In all the tables, improvement over the case of the same N and T but without the micro-channel is also reported in parentheses.

From the tables we can draw the conclusion that micro-channel technique is more important at larger N and T, and at higher frequencies – both Q and L improves significantly. This is in accordance with the intuition that substrate losses become larger with larger N, T, or higher f. At 10 GHz, up to 21x increase in Q and 17x increase in L are observed (Tables 3.2 and Table 3.3, N=3, T=5), while at 1 GHz only Q is improved by up to 3x (Table 3.4, N=6, T=5).

One more thing worth mentioning here is that the increased self-resonant frequency brought by the micro-channel. For example, in Table 3.3, when N = 5 and T = 4, the TSV inductor without micro-channels ceases to work as an inductor (Q<0), while the TSV inductor with micro-channels still provides positive quality factor. For that reason, no improvement is reported.

Table 3.2 Q vs. Number of turns(N) and number of tiers(t) for maximum micro-channel dimensions (measured at 10 GHz). The relative improvement over the case without micro-channel shields is reported in parentheses.

Q		T			
		2	3	4	5
N	1	10.96 (5.88%)	13.12 (14.5%)	14.53 (38.9%)	14.90 (70.3%)
	2	11.36 (11.7%)	11.31 (78.52%)	7.59 (168%)	6.14 (359%)
	3	11.89 (26.3%)	9.15 (167%)	4.65 (406%)	2.00 (2034%)
	4	11.89 (42.4%)	7.46 (269%)	2.93 (1007%)	1.03 N/A
	5	11.37 (55.3%)	5.97 (371%)	1.87 N/A	0.19 N/A
	6	10.98 (71%)	4.74 (483%)	1.01 N/A	-2.08 N/A

Table 3.3 L vs. Number of turns (N) and number of tiers (t) for maximum micro- channel dimensions (measured at 10 GHz). The relative improvement over the case without micro-channel shields is reported in parentheses.

L (nH)		T			
		2	3	4	5
N	1	0.135 (0.0%)	0.344 (0.0%)	0.577 (0.0%)	0.828 (1.2%)
	2	0.344 (0.0%)	0.958 (0.0%)	1.729 (0.0%)	2.708 (11.9%)
	3	0.594 (0.0%)	1.700 (0.0%)	3.523 (39.9%)	5.882 (1615%)
	4	0.843 (0.0%)	2.741 (1.0%)	5.959 (424%)	8.855 N/A
	5	1.093 (0.0%)	3.390 (2.2%)	8.577 N/A	3.055 N/A
	6	1.376 (0.0%)	5.206 (58.5%)	10.634 N/A	-3.518 N/A

Table 3.4 Q vs. Number of turns (N) and number of tiers (t) for maximum micro- channel dimensions (measured at 1 GHz). The relative improvement over the case without micro-channel shields is reported in parentheses.

Q		T			
		2	3	4	5
N	1	4.29 (30.6%)	3.74 (0.5%)	4.15 (1.0%)	4.44 (2.0%)
	2	3.36 (0.0%)	4.72 (3.2%)	5.37 (4.8%)	5.90 (9.9%)
	3	3.76 (0.2%)	5.28 (1.7%)	6.39 (15.8%)	6.83 (36.4%)
	4	4.02 (0.8%)	6.04 (11.1%)	7.11 (37.4%)	7.57 (88.3%)
	5	4.13 (0.1%)	6.49 (17.8%)	7.65 (67.0%)	7.78 (153.0%)
	6	4.29 (2.7%)	6.81 (26.5%)	7.92 (98.5%)	8.01 (235.1%)

Table 3.5 quality factor (q) and area (a) comparison between 2d spiral inductors (w/ pgs) and 3d TSV inductors (both w/o and w/ micro-channel shields) under same design specs (L and F**).**

Design Specs			Spiral Inductor						TSV Inductor						
#	f (GHz)	L (nH)	Geometry				Q	A (um^2)	Geometry				Q		A (um^2)
			T (um)	D (um)	d (um)	W (um)			N	T	W (um)	P (um)	w/o shield	w/ Shield	
1	1	6.5	2	560	535	10	5.7	313,600(1)	6	2	7	20	4.6	7.6	8,255(1/37.9x)
2	5	2.50	2	400	355	20	6.9	160,000(1)	4	3	6	18	4.3	10.3	9,358(1/17.1x)
3	10	0.95	1	330	320	10	10.0	108,900 (1)	2	3	6	18	5.8	10.1	4,679(1/23.3x)

Finally, we set up three different sets of target inductance and operating frequency, and compare the resulting 2D spiral inductor, conventional TSV inductor without micro-channel shields, and our TSV inductor with micro-channel shields in terms of quality factor and area. The results are reported in Table 3.5. The 2D spiral inductors are implemented through a special RF process, which includes a total of 9 metal layers of 8 um thick in total. The spiral inductor is implemented on M9 of 4 um thick (to improve Q). The PGS as shown in [10] is also embedded. T, D, d and W denote the number of turns, outer diameter, loop pitch, and metal width for the spiral inductor respectively. For the TSV inductors with and without micro-channel shields under the same design spec, we use the same geometries for comparison. Their notations are shown in Table 2.1 and other process details are listed in Section 3. The area for all inductors is measured by the total routing resource occupied. For TSV inductors, the area also includes the substrate occupied by the TSVs.

From the table, we can easily see that the TSV inductors without micro-channel shields has much inferior quality factor compared with the spiral inductor of the same inductance, while the TSV inductors with the micro-channel shields can achieve higher quality factor compared with the spiral inductor. For example, at 1 GHz, while 6.5 nH is achieved by all the three inductors, our TSV inductor with micro-channel shields can achieve a 38x area reduction with 33% quality factor improvement compared with the spiral inductor. In other words, circuits implemented using our TSV inductor with micro-channel shields can improve energy efficiency by up to 33% and reduce the area by 38x compared with its counterpart implemented using conventional spiral inductor. The results suggest that the micro-channel shields make TSV inductors a much better option over spiral inductors in 3D ICs.

4. CONCLUSIONS AND FUTURE WORK

In this thesis, we have systematically examined how various parameters affect their performance. In addition, we have proposed a novel shield mechanism utilizing the micro-channel technique to drastically improve the quality factor and the inductance. To the best of the authors' knowledge, this is the very first in-depth study on TSV inductors along with a technique to make them practical.

In the future, we will try to implement benchmark applications such as on-chip transceivers and transceivers using the proposed TSV inductors.

BIBLIOGRAPHY

[1] Franzon, P.D.; Davis, W.R.; Thorolffson, T.; , "Creating 3D specific systems: Architecture, design and CAD," in Proc.Design, Automation & Test in Europe Conference & Exhibition (DATE), pp.1684-1688, 8-12 March 2010.

[2] 2011 ITRS roadmap, http://www.itrs.net/Links/2011ITRS /2011Chapters/2011Metrology.pdf

[3] Dae Hyun Kim et al; , "*3D-MAPS: 3D massively parallel processor with stacked memory*," Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International , vol., no., pp.188-190, 19-23 Feb. 2012.

[4] Gary VanAckern, "*Design Guide for CMOS Process On-Chip 3D Inductor Using Thru-Wafer Vias*," Master Thesis, 2011

[5] Zhang Bo et al., "*3D TSV Transformer Design for DC-DC/ACDC Converter*", 60th Electronic Components and Technology Conference (ECTC), pp. 1653 - 1656, Jun 2010.

[6] Huang et al, "*Interleaved Three-Dimensional On-Chip Differential Inductors and Transformers*," US Patent 2008/0272875, Nov. 2008.

[7] Bontzios, Y.I.; Dimopoulos, M.G.; Hatzopoulos, A.A.; , "*Prospects of 3D inductors on through silicon vias processes for 3D ICs*," VLSI and System-on-Chip (VLSI-SoC), 2011, IEEE/IFIP 19th International Conference on , vol., no., pp.90-93, 3-5 Oct. 2011

[8] Loi, I.; Angiolini, F.; Fujita, S.; Mitra, S.; Benini, L.; , "*Characterization and Implementation of Fault-Tolerant Vertical Links for 3-D Networks-on-Chip*," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , vol.30, no.1, pp.124-134, Jan. 2011

[9] HFSS websit:"http://www.ansys.com/

[10] C. Pattrick Yue and S. Simon Wong, "*On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's*," IEEE Journal of Solid-State Circuits, vol. 33, no. 5, pp. 743-752, May 1998.

[11] J. Zhang, "*Indcutor with Patterned Ground Plane*," US Patent 2009/0250262, 2008

[12] Yoon Jo Kim et al, "*Thermal Characterization of Interlayer Microfluidic Cooling of Three-Dimensional Integrated Circuits With Nonuniform Heat Flux*," Journal of Heat Transfer-transactions of The Asme - J HEAT TRANSFER , vol. 132, no. 4, 2010

[13] Bing Shi and Ankur Srivastava, "*TSV-constrained micro-channel infrastructure design for cooling stacked 3D-ICs*," ACM International Symposium on Physical Design, pp. 113-118, 2012

[14] http://gradient-da.com

[15] K. Gantz and M. Agah, "Predictable three-dimensional microfluidic channel fabrication in a single-mask process," Technical Digest of the 14th International Conference on Solid-State Sensors, Actuators, and Microsystems (Transducers07), pp. 755-758, June 10-14, 2007

[16] D. Sekar et al, "A 3D IC Technology with Integrated Micro-channel Cooling," Interconnect Technology Conference, IITC 2008.

[17] Z. Tao, W. Kui, F. Yi, C. Yan, L. Qun, S. Bing, X. Jing, S. Xiaodi, D. Lian, X. Yuan, C. Xu and L. Youn-Long," A 3D SoC design for H.264 application with on-chip DRAM stacking," 3D Systems Integration Conference (3DIC), 2010 IEEE International, 2010.

[18] D. S. Gardner, G. Schrom, F. Paillet, T. Karnik and S. Borkar, "Review of on-chip inductor structures with magnetic films," IEEE Trans. Magnetics, 45 pp. 4760-4766, 2009

[19] Xinhai Bian et al," Simulation and modeling of wafer level silicon-base spiral inductor," Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 13th International Conference, 13-16 Aug, 2012.

[20] H. A. Wheeler, "Formulas for the skin effect," Proc. IRE, vol.30, pp. 412-424, Sept. 1942.

[21] Sunderarajan S. Mohan, "The Design, Modeling and Optimization of On-Chip Inductor and Transformer Circuits," PhD Thesis, 1999.

[22] Ji Chen and Juin J. Liou, "On-Chip Spiral Inductors for RF Applications: An Overview," Journal of semiconductor technology and science, vol.4, no.3, September, 2004

VITA

Rongbo was born on May 1st, 1989 in Yichang, People's Republic of China. In 2011, he obtained a Bachelor's degree in Department of Computer Science and Technology from Huazhong University of Science and Technology, Wuhan.

In August 2011, he enrolled at the Missouri University of Science and Technology to a master's degree in the Department of Electrical and Computer Engineering. He worked under the guidance of Dr. Yiyu Shi. He received his Master of Science Degree in Computer Engineering in December, 2013.