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Characterization of noise on PDN and electromagnetic shielding

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Department:

- 16 global clock trees and 32 regional clock trees.
- High speed DSP blocks with dedicated multipliers (upto 450 MHz), multi-accumulators, and FIR filters.
- Support of numerous single-ended and differential I/O standards.
- High-speed, source-synchronous differential I/O up to 71 channels.
- The FPGA used in the experiments has 15 I/O banks with 1152 FBGA encapsulation.
- The FPGA supports SSTL, LVTTL, and other I/O standards. Its core power level is 1.2V.

1.1.2. Quartus. Quartus is Altera's integrated VHDL design system. It supports VHDL, Verilog HDL, AHDL, and schematic design. Quartus also provides its own built-in Intellectual Property (IP) library with many built functionalities. The Quartus interface is shown in Figure 1.1.

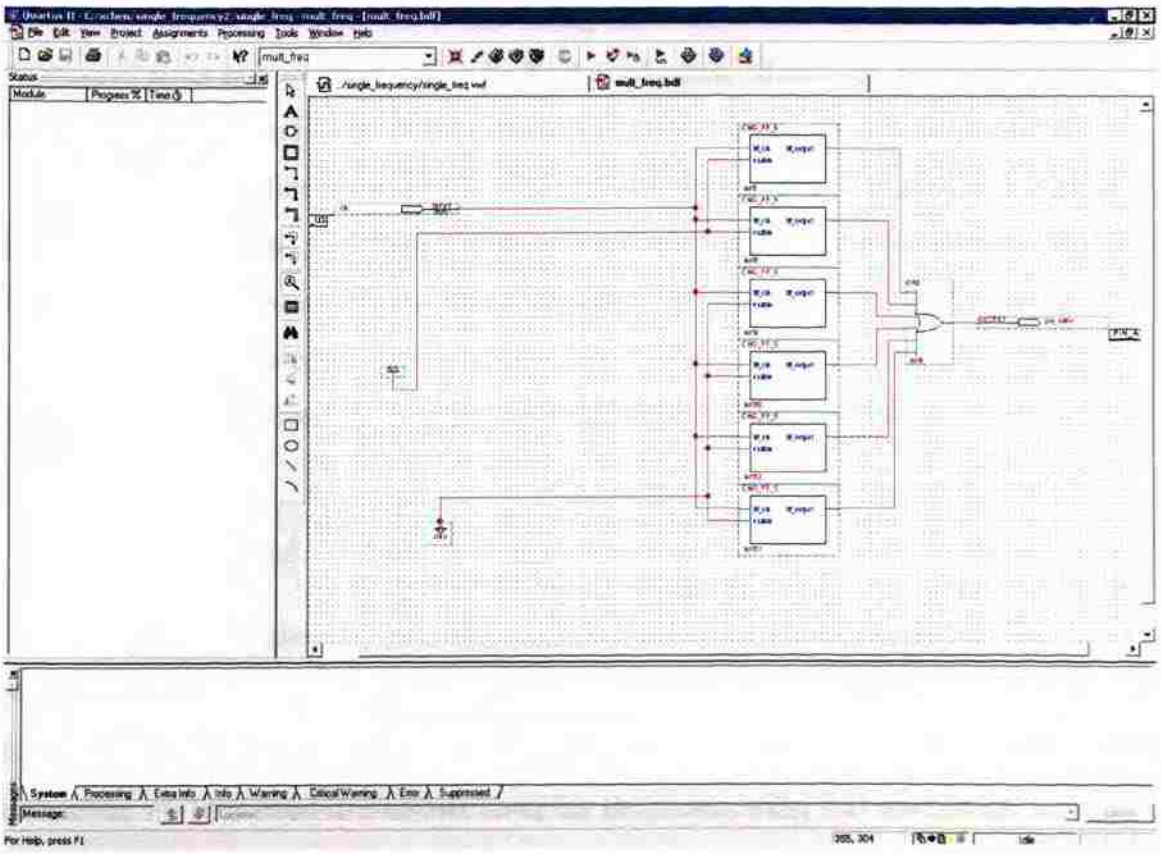

Figure 1.1. Quartus Interface

Special patterns are developed in Quartus to analyze the current drawn in a known way. For example, a T-Flip Flop (TFF) will switch once every two clock cycles and hence has half the frequency as a clock. Thousands of TFF's can be made to switch together to draw a huge amount of current at a single time. Such patterns have predictive behavior and are implemented at the initial stages to help predict the current drawn. Measurements and simulations are then performed using these patterns and then compared to each other.

1.2. ELECTROMAGNETIC SHEILDING

In today's world there is a need to reduce unwanted electromagnetic radiation, emitted by electronic devices, and also there is a need to protect sensitive circuits from the outside electromagnetic radiation. Sometimes, electromagnetic radiation can be intentionally generated to disrupt the electronic devices. Shielding material can be used to shield sensitive equipment to reduce the emissions and improve the immunity of electronic equipment. Usually a highly conductive material (metal) is used to form a shielding enclosure. The effectiveness of such shielding enclosure is mainly determined by the presence of slots and aperture arrays for heat dissipation. Moreover, metal enclosures are massive, large size, and difficult to move around and manipulate. Materials designed from the conductive fibers and carbon-rich foam materials tend to absorb and reflect electromagnetic waves, and, hence, can be used to design shielding enclosures. Shields made of these kinds of materials tend to be lighter and easy to shape, move, and manipulate. These materials can be stacked up together to provide better shielding. Shielding is characterized by the parameter called Shielding Effectiveness (S.E). It can be calculated as

$$(SE)_{dB} = 10\log\left(P_{incident}/P_{transmitted}\right) \tag{1.1}$$

Composite materials, including carbon-filled ones, are measured for their shielding effectiveness. The Debye dielectric parameters are obtained by approximating frequency dependencies of S-parameters taken from measurements. The Debye parameters are then used to simulate complex structures using 3-D simulation tools to evaluate shielding effectiveness [7].

1.3. MODELING AND VALIDATION

Full-wave modeling is an important method to solve complex electromagnetic models. There are many commercially available tools out in the market, and each is designed to solve a specific set of problems. Common methods that are employed in commercial tools to solve the Maxwell equations are Finite Difference Time Domain method (FDTD), Finite Element Method (FEM), Integral Equation Solution or Method of Moments (MOM). Each method has its own advantages and disadvantages. A method to be employed should be chosen depending on a type o f a problem to be solved and accuracy required. However, solution offered by new 3-D simulation software cannot be considered correct, until it is validated by different method. Validating the solution can be done either by using the other software with a different solution method, or by making real measurements, or by analytically solving the problem. Measurements of an adequate prototype are not always possible, and analytically solving a problem can be too complicated. Thus, using two different software solutions to the same problem is a good validation approach. An antenna over different ground planes is studied herein, using the EZ-FDTD tool and the WireMoM. These two types of software use different numerical methods – Finite Difference Time Domain (FDTD) technique and Method of Moments (MoM).

2. CHARACTERIZATION OF NOISE ON PDN

Special patterns are developed in Quartus to understand and estimate the current drawn from the PDN in a known way.

2.1. PATTERN

In this experiment, the FPGA logic (pattern) is called the single frequency parallel toggling flip-flop (TFF) pattern with one single clock input and one testing output pin terminated using LVTTL standard [2].

To implement different percentages of the FPGA utilization using this pattern, simply connect the enabled bits from different blocks to the GND or VCC, as shown in Figure 2.1. Parallel TFF Pattern the top 2 blocks are connected to the VCC and the rest are connected to the ground, thus implementing a 10% parallel TFF pattern.

The clock input pin (PIN_U31) directly drives six parallel TFF modules, each of which includes around 2.7K TFFs or about 5% of the total FPGA logic utilization as shown in Figure 2.2. A total of 30% of the FPGA utilization can be implemented using this pattern.

The advantage of using all 6 blocks for percentages between 0% and 30% is to maintain certain amounts of routing and clock tree structures so that it will be easy to quantize the resulting core noise.

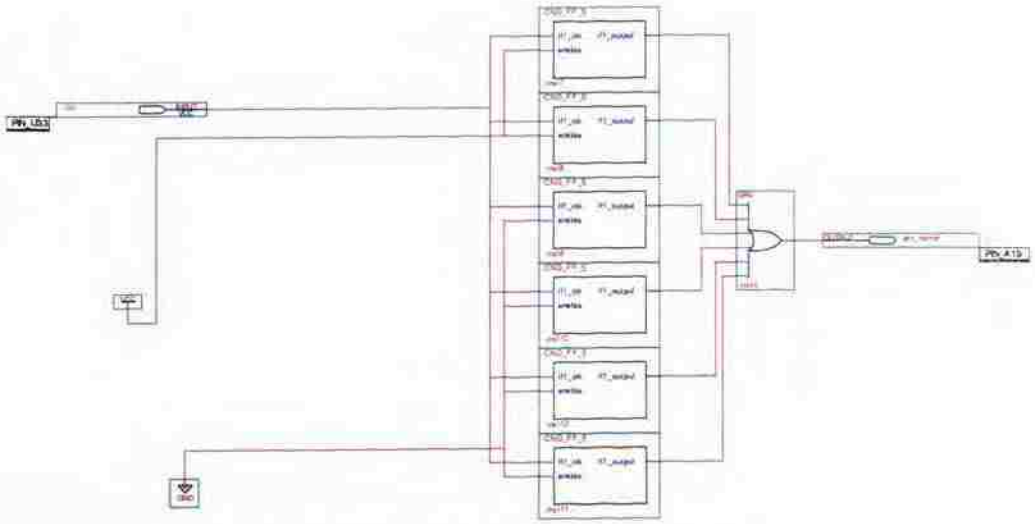

Figure 2.1. Parallel TFF Pattern

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All TFFs are then connected with the OR gate to the output pin (A19) to use the oscilloscope to check if the signal is correctly passed through the FPGA. The output pin will create a certain amount of I/O noise despite the core noise created by the parallel toggling logic inside the chip. The I/O noise is a constant compared to the core noise.

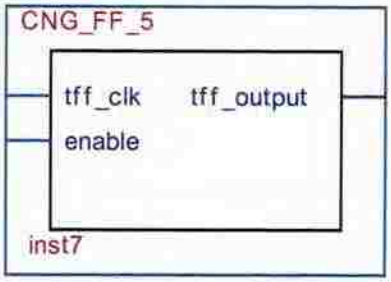

Figure 2.2. Parallel TFF Block Containing 5% of Logic

It is not possible to eliminate the output pin because the Quartus will then optimize and remove any logic that does not have a direct output associated with it.

2.2. CORE NOISE TEST VEHICLE

In order to characterize and correctly depict the noise from the FPGA core it is important to have a good test vehicle. A special board shown in Figure 2.3 was designed and manufactured to achieve the following goals:

- Isolate core power plane from rest of the power planes.
- Avoid any loss of resonances associated FPGA placement.
- Provide good measurements points to measure noise directly on the power plane.
- Provide enough decoupling capacitor pads.
- Provide enough signal measurement pins from all banks of the FPGA.

In order to achieve the goals listed above, several steps were taken during the board design stages. Stack up as shown in Figure 2.4 was chosen carefully to provide enough isolation and backdrilling was used to ensure that there was no coupling from the via. Capacitor pads for Vcc were all placed at the top layer. Capacitor pads were mainly concentrated around FPGA. FPGA was placed asymmetrically to avoid missing any

resonance. Many differential signal lines were brought out of FPGA for the purpose of measuring jitter.

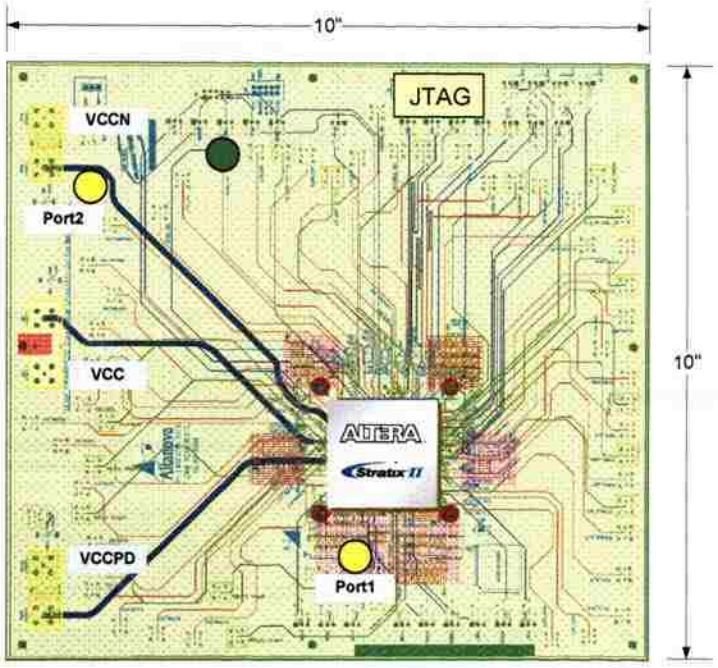

Figure 2.3. Test PCB Board

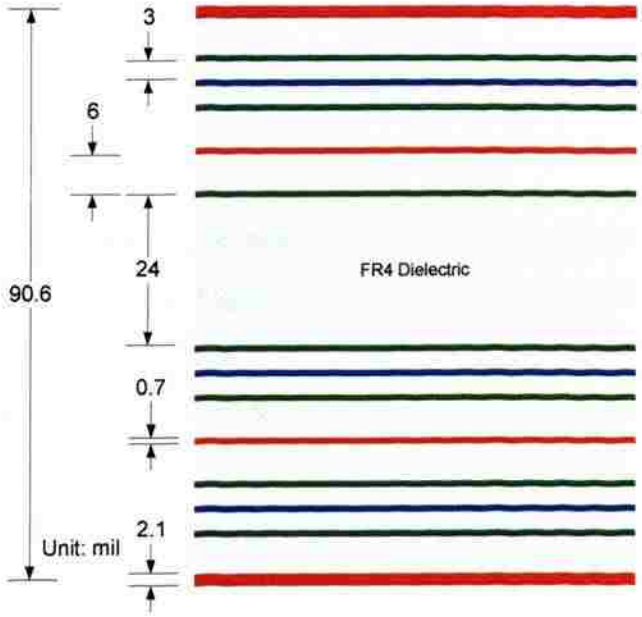

Figure 2.4. Board Stack Up

The first phase during the development of the test vehicle is to choose the stack up of the board. The Altera Stratix II-GX FPGA required three power levels VCC, VCC-I/O, and VDD- pre driver for I/O. Research interest is in the core power layer VCC. The main concern during stack up design was to make sure that any noise observed in the VCC layer is due to switching activity in the VCC layer only, not to coupling between VCC-I/O or VCC-PD. In order to achieve this isolation, the VCC layer was placed at the top of the stack and rest of the power layers were placed below as shown in Figure 2.5.

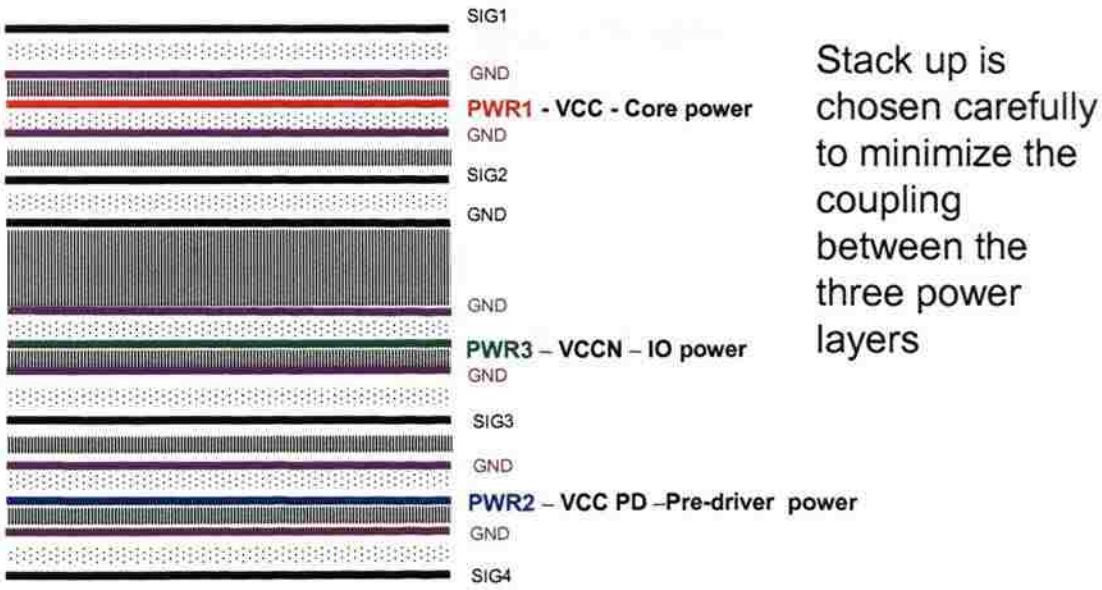

Figure 2.5. Stack Up

In order to present coupling between the power planes due to via-coupling, all the vias were back drilled as shown in Figure 2.6. Back drilling was performed on following pins:

- All SMA connectors connected to power planes and signal traces.
- All capacitor pads.
- From the bottom of the board for VCC layer and from top of the board for other two layers.

The pins from FPGA were not back drilled in order to provide signal probing underneath the FPGA. Also, all ground was stitched together.

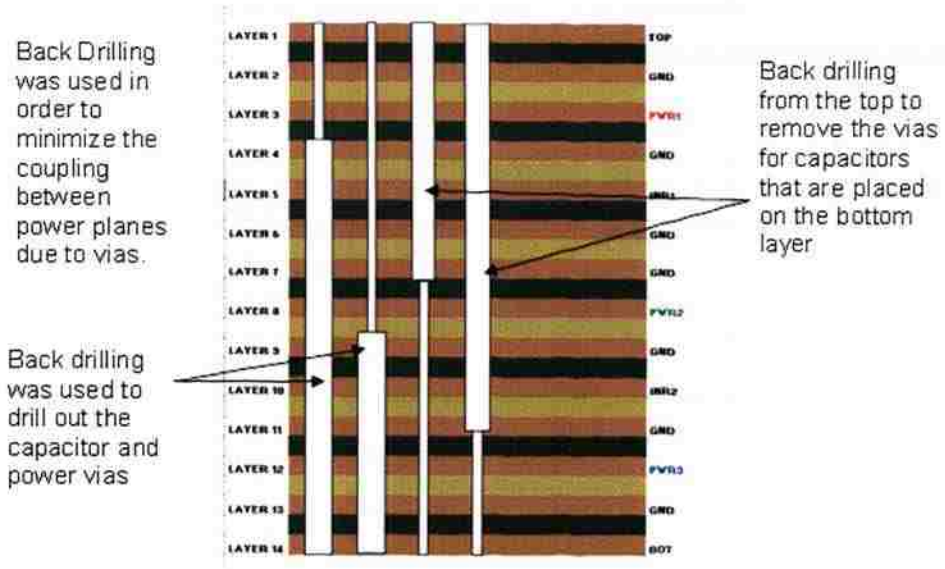

Figure 2.6. Backdrilling of Vias

Another important consideration during board design was the FPGA placement as shown in Figure 2.7. FPGA is the noise source that has to be characterized. If the noise source is exactly at the center, then the noise produced at some of the resonant modes will not be picked up by the observation points. This will be demonstrated with an example using simulations.

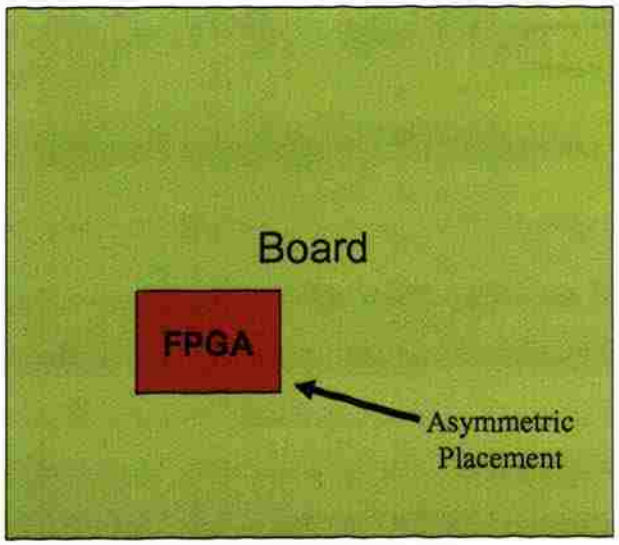

Figure 2.7. FPGA Placement

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The importance of FPGA placement is shown by an example using simulations as shown in Figure 2.8. Three ports were placed on a board. Port 1, assumed to be the location of the FPGA, was placed at the center in one simulation and asymmetrically in another. $|Z_{12}|$ was compared between two simulations. The simulation clearly shows that when the Port 1 is at the center not all the resonances can be observed at port 2 and 3. So, any noise produced at these frequencies cannot be observed at any observation point and, hence, cannot be characterized correctly. These are only simulations, to prove the point that placing an FPGA at the center will result in improper observation of noise at the measurement points.

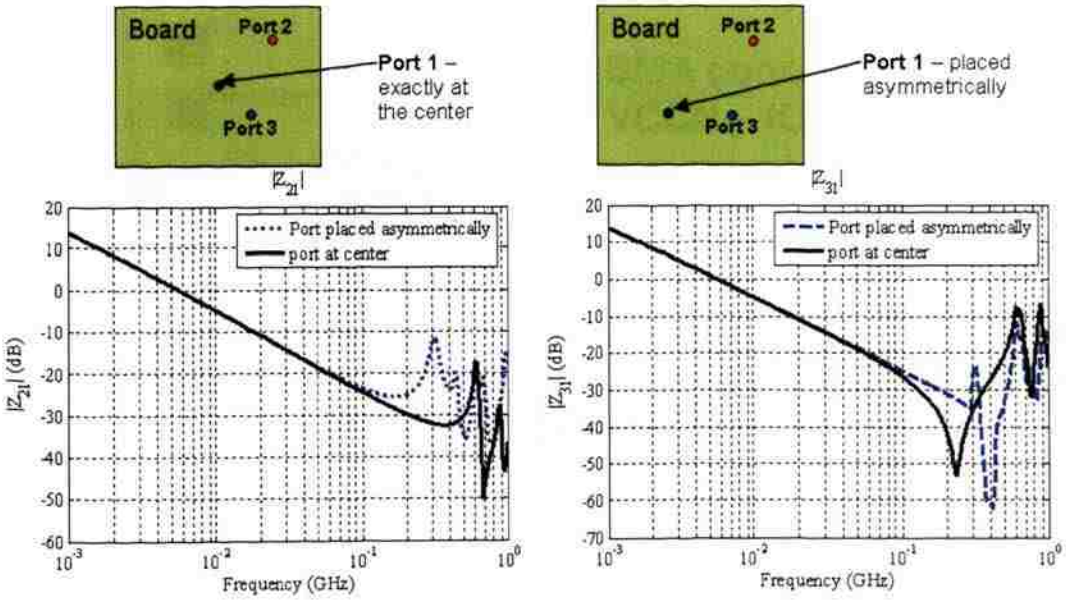

Figure 2.8. Importance of FPGA Placement

In order to directly measure noise on the power plane, the SMA connector is attached directly to the power layer. Two such SMAs are attached to one power layer with a total of 6 SMA for three power layers as shown in Figure 2.9. The purpose of this SMA is to measure noise voltage on the power plane. Placing one SMA closer to the FPGA and the other far from FPGA provides two different measurement points for noise observation. Ideally, a measurement point would have been placed directly underneath

the FPGA, but due to routing issues the SMA must be placed at least1.5 inches away from the FPGA. To avoid the stub effect, the probing point was also placed at least 1 inch away from the FPGA instead of directly underneath it.

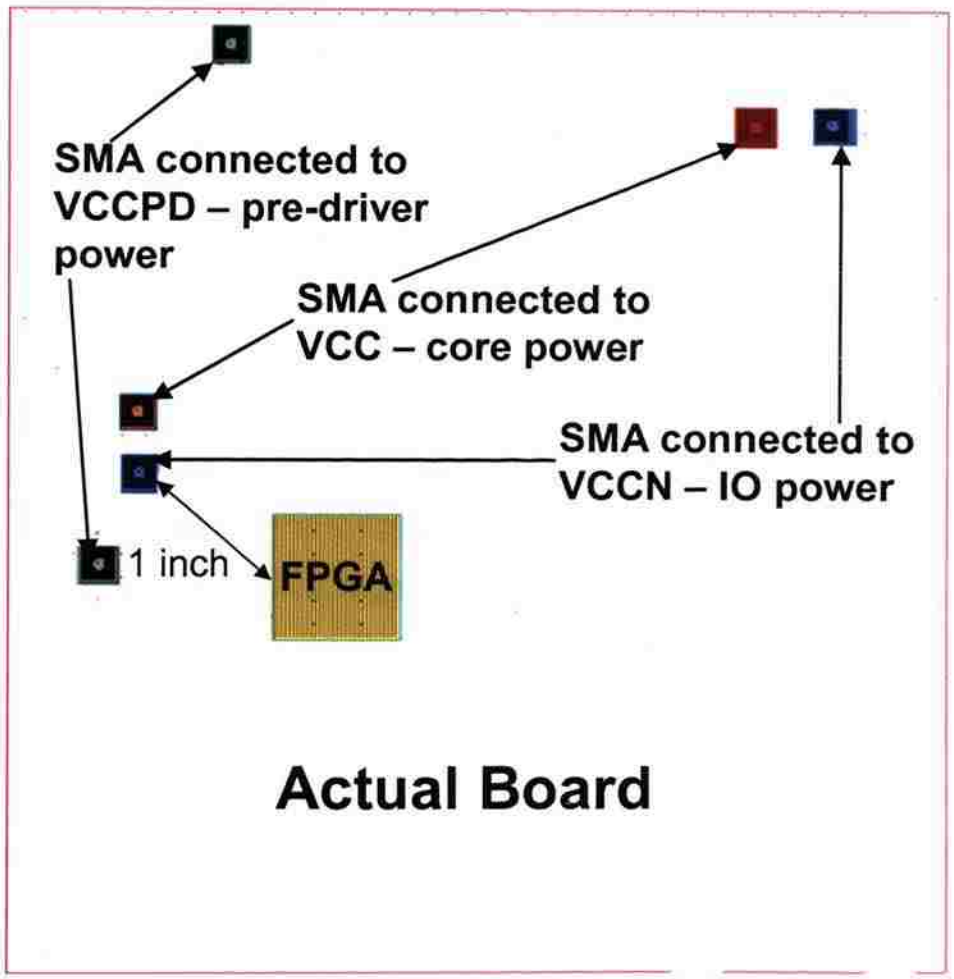

Figure 2.9. SMA Connectors on Board

Placement of capacitor pads was also carefully considered during the broad design [3]. All the capacitors for the VCC power plane were placed on the top side of the board and all the capacitors for the VCCN and the VCC PD were placed on the bottom side of the board as shown in Figure 2.10. This ensured minimal inductance associated with capacitor vias especially for VCC power plane and also eliminates coupling between

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capacitor vias of different power planes. The capacitor vias were also back drilled in order to ensure that there was no coupling due to vias.

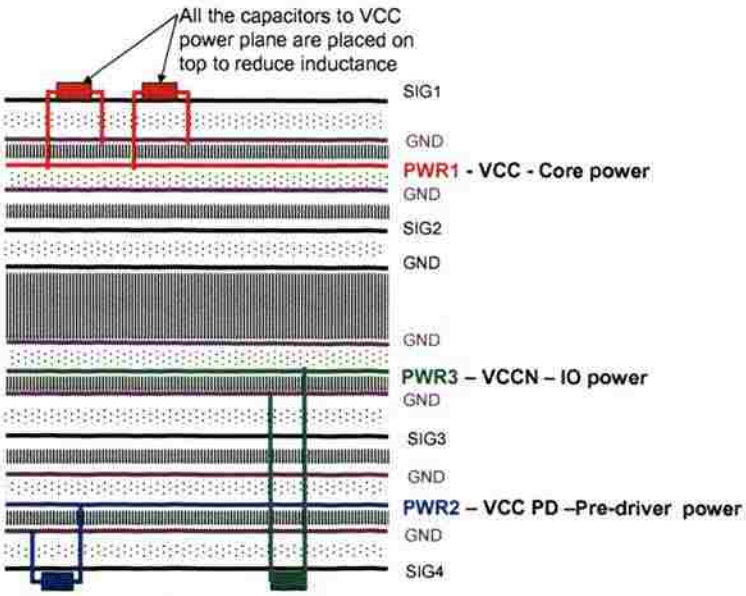

Figure 2.10. Capacitor Placement for Power Planes

All the capacitor pads for the VCC power layer were placed around FPGA as shown in Figure 2.11. Considering the routing issues, some of them were placed a fairly far from FPGA. Placing the capacitors as close as possible to the FPGA provided an opportunity to develop a better decoupling strategy.

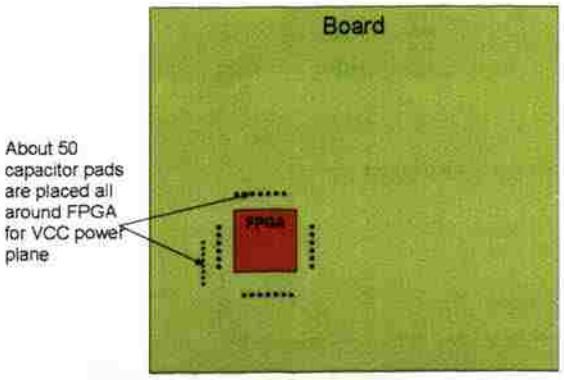

Figure 2.11. Capacitor Placement Around FPGA

2.3. IMPEDANCE MODELING

One of the main requirements for the project's success is correct modeling of the broad's impedance profile. The self impedance and transfer impedance between any ports on the board should be estimated accurately both with and without capacitors. A Maxwell equation solver tool- EZ-Power Plane [6] developed by UMR was used for estimation. Also, commercially available HSPICE was used to include the effects of package and port inductances.

Simulations using these tools were then compared to measurements in order to verify modeling accuracy. Simulations were also used during the design of the board to roughly estimate the number of capacitor pads required for the VCC power plane as shown in Figure 2.12.

During the broad design the approximate number of capacitor pads required to be placed on board was determined. Simulations indicated that the target impedance of 0.1 ohm was easily achievable with around 50 capacitor pads placed closed to FPGA, assuming the use of different capacitor values and sizes as shown in Figure 2.13. The effects of package/FPGA were not considered during these simulations.

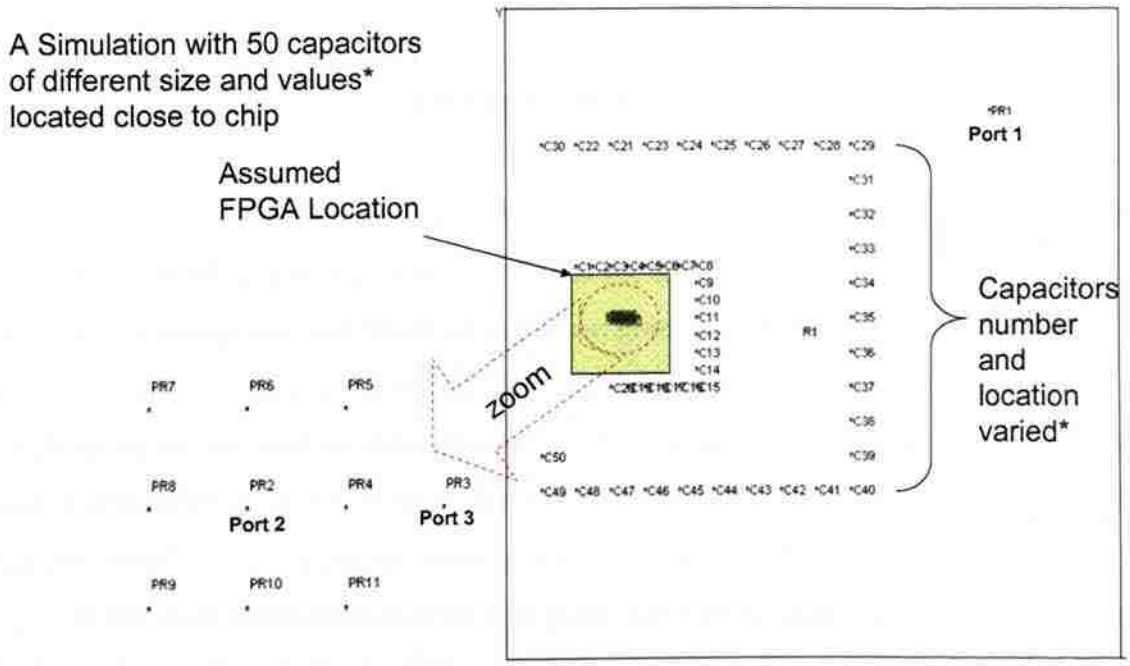

Figure 2.12. Simulation Setup

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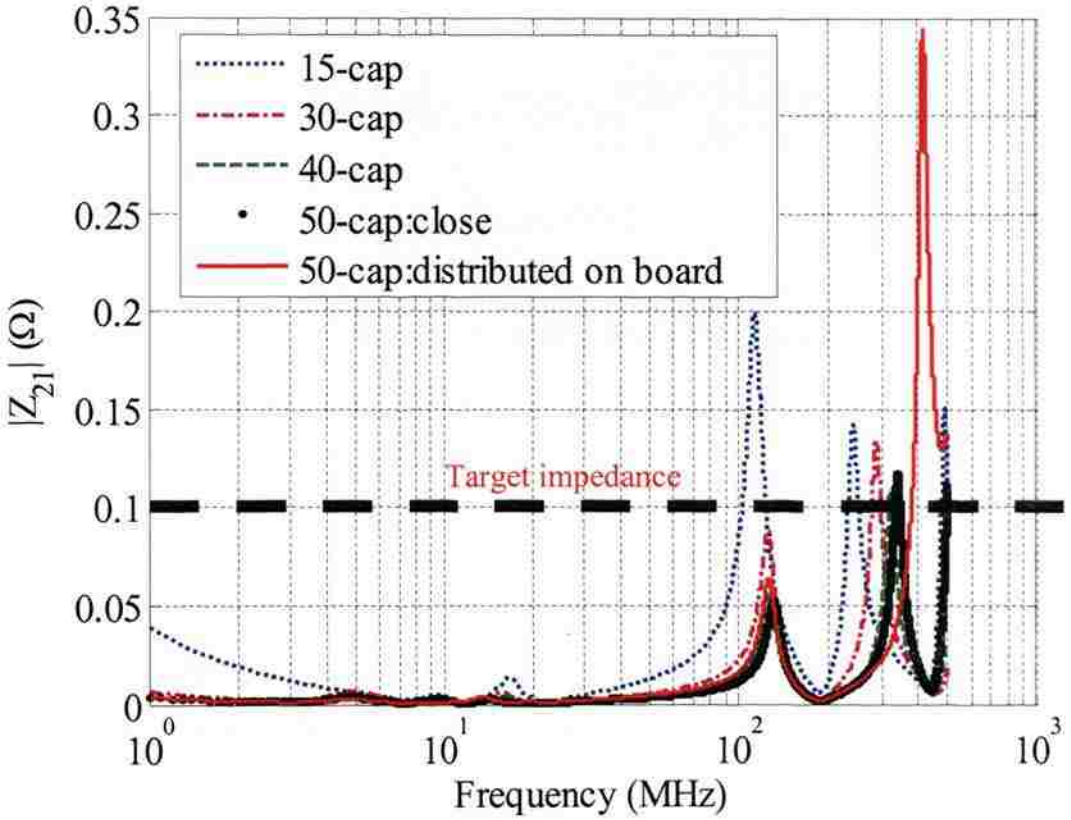

Figure 2.13. Target Impedance Check

The target impedance was met up to 500 MHz with 50 capacitor pads close to FPGA.

2.3.1. Transfer Impedance – Measurements vs. Simulations. Once the board was manufactured, it was important to validate the impedance simulations. A full S-parameter measurement was made between two points on the board. The two points shown in Figure 2.14 the far point (far from FPGA location) and the near point (near FPGA location), are used as measurement points. In order to validate the simulations, a board without FPGA on it was taken for measurements. The S-parameters measured were then converted into Z-parameters and compared to the simulated impedance profile.

It has to be noted here that the near point SMA mounting point was damaged at the time of mounting. A decoupling capacitor mounting pad was used to mount a coaxial cable at the near point.

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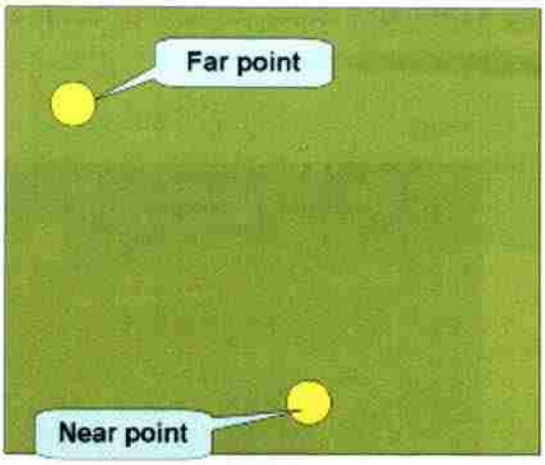

Figure 2.14. Port Locations and Port Names

The simulations matched the measurements taken on the board between the ports near point and far points on the board as shown in Figure 2.15, please note here that the board does not have FPGA on it and it is completely bare without any capacitors. The board was not powered up and did not have any type of DC connection.

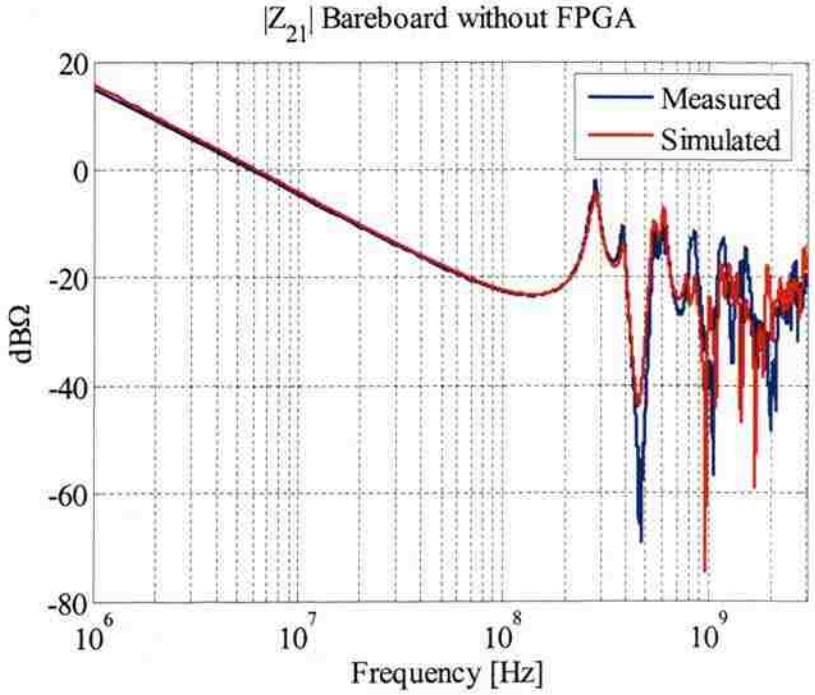

Figure 2.15. Transfer Impedance Between Far Point (Port 1) and Near Point (Port 2)

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Figure 2.16 illustrates the board simulation points with FPGA on it.

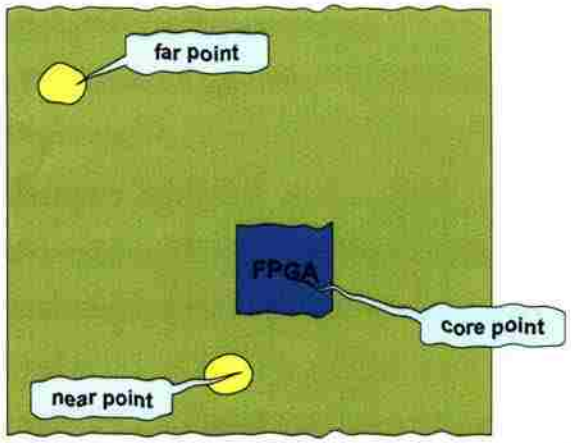

Figure 2.16. Port Location and Port Name for FPGA

Once the FPGA was placed on the board, the same measurements as above were repeated and compared to simulations. Simulations in this case still did not consider the effects of FPGA on the board as shown in Figure 2.17. The board again did not contain any capacitors, was not powered up and did not have any type of DC connection.

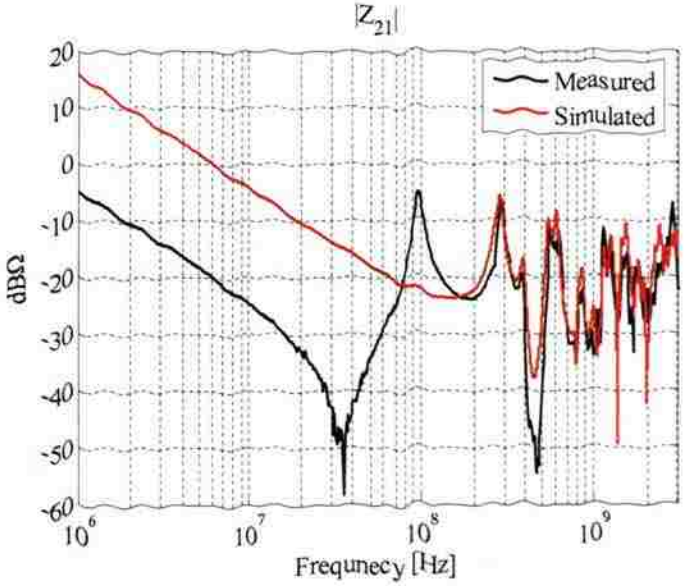

Figure 2.17. Simulation Without Considering Effect of FPGA vs. Measurements

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Figure 2.17 illustrate that the FPGA is contributing a great deal of, more like a big capacitor. Simulations, on the other hand, are just two ports between two power planes and did not take anything else into account. So, the simulations which did not take this effect into account did not match the measurements.

2.3.2. Modeling FPGA as a Capacitor – Low Frequency Model. Taking into account the effects of FPGA requires accurately modeling. If FPGA is thought of as one big capacitor sitting on the top of the board, then it can be modeled as a simple capacitor with some capacitance and series inductance. In order to obtain the capacitance of FPGA, two transfer or self impedance measurements were made, one on the board with out FPGA and one on the board with FPGA. By calculating the difference in capacitive slope at low frequencies, the value of capacitance contributed by FPGA alone was obtained. The series inductance can be obtained by carefully studying the resonant peaks from the measurements. The calculated values for capacitance of FPGA and inductance of FPGA from these measurements for a powered down board were 238.3nF and 10pH, respectively.

Remember that these values are for the powered down board. Powering up the board changes the capacitance contributed by FPGA. The calculated values for capacitance of FPGA and inductance of FPGA from these measurements for powered up board were 440nF and 10pH respectively. Low frequency model of FPGA as a capacitor is shown in Figure 2.18. Low Frequency FPGA Model is only valid for low frequency.

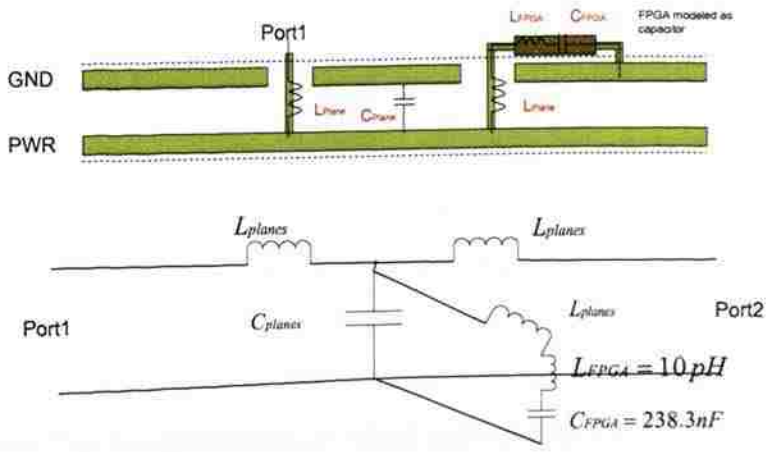

Figure 2.18. Low Frequency FPGA Model

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With the capacitance and inductance values extracted from calculations, it is possible to model the FPGA as a capacitor in the simulations. A capacitor was placed between power and ground planes with values extracted and simulation is done using EZ-powerplane. It can be seen from the above Figure 2.19 that the simulation, in which considering the FPGA is modeled as a capacitor, matches up with the measurements.

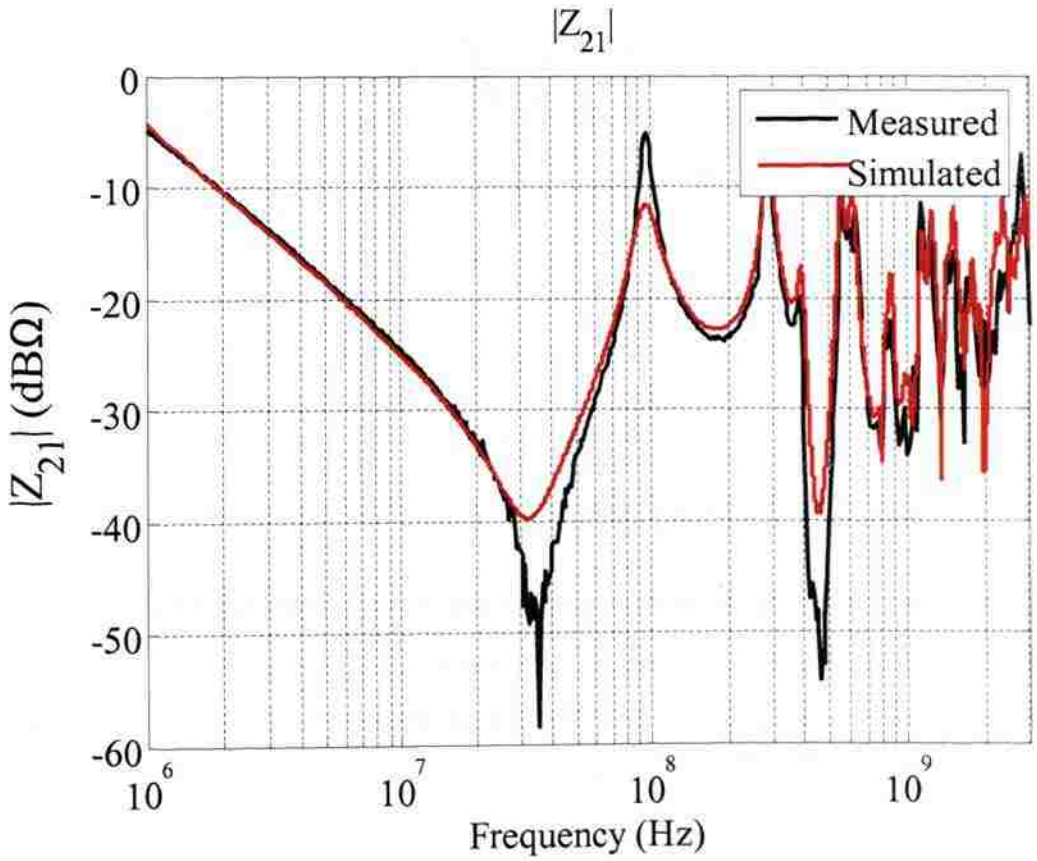

Figure 2.19. Simulation vs Measurements of Transfer Impedance

The measurements and simulations are between the near point and far point. The board here again does not contain any capacitors. The board is powered down and does not have any type of DC connection to it. The simulated model is also with board powered down. The capacitance of FPGA is 238.3 nF with a series inductance of 10 pH. Figure 2.20 show that the simulation, in which considering the FPGA is modeled as a capacitor, matched the measurements.

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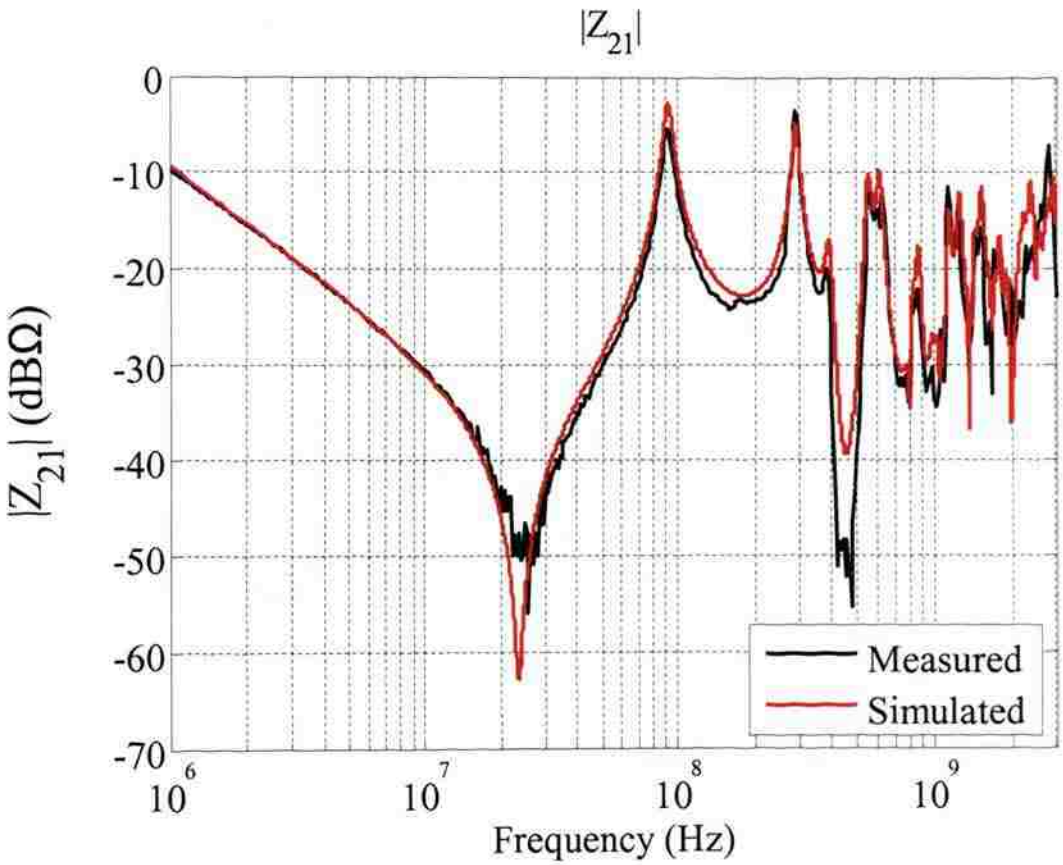

Figure 2.20. Simulated vs. Measured Transfer Impedance with Board Powered On

The measurements and simulations were between the near point and far point. Again board did not contain any capacitors. The board is powered up with a power supply of 1.3 V to VCC. The simulated model was also done with board powered up. The capacitance of FPGA is 440 nF with a series inductance of 10 pH.

The next step was to correctly estimate the transfer impedance with capacitors on board. Measurements were again made between far point and near points, but this time the board contained 15 capacitors in one case and 37 capacitors in the other case [4]. Their respective simulations were compared as shown in Figure 2.21 and Figure 2.22. Capacitors were carefully mounted on the board, so that no extra inductance is added due to solder. The effective inductance contributed by the via depth and solder was added as ESL in the simulations.

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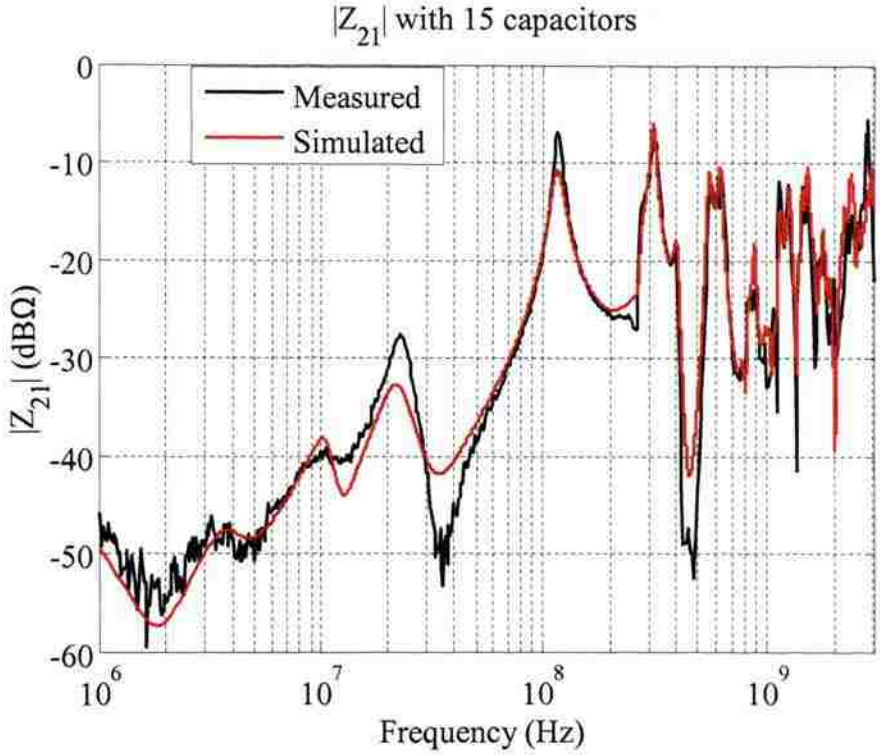

Figure 2.21. Simulated vs. Measured Transfer Impedance with 15 Decoupling Capacitors

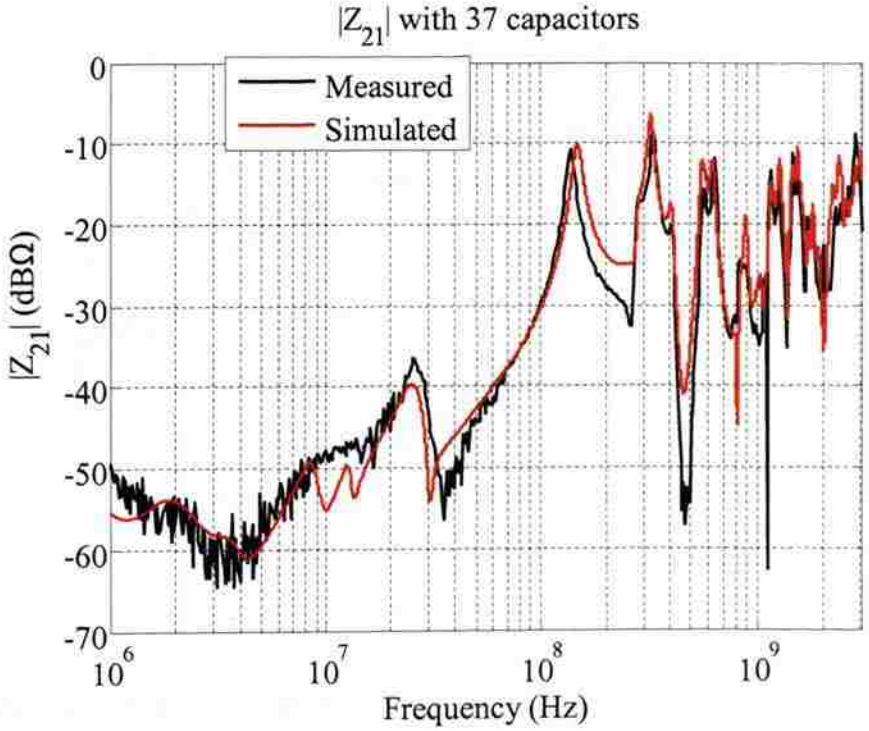

Figure 2.22. Simulated vs. Measured Transfer Impedance with 37 Decoupling Capacitors

The difference in low frequency capacitive slope and a slight shift in resonances could be a result of actual capacitor value on board and capacitor value taken for simulation. There may be a slight difference between each capacitor value specified in the data sheet and the actual value on board.

2.3.3. Modeling Transfer Impedance from Core to Measurement Points. In order to estimate the noise produced by switching current in the core and then make a comparison at a known measurement point, it is important to estimate transfer impedance from the switching core to the measurement point. Both EZPP and HSPICE were used to simulate the model. First, the board alone with out any capacitors was simulated with EZPP and with three ports. EZPP produces a HSPICE model for the complete board, which is then imported into HSPICE. For the port at core point the inductance, capacitance and resistance are added as shown in the Figure 2.23. Then the complete HSPICE model is simulated to get full S-Parameters between all three ports. Then the S-Parameters are converted into Z-Parameters to get the transfer and self impedances of the model as shown in Figure 2.24.

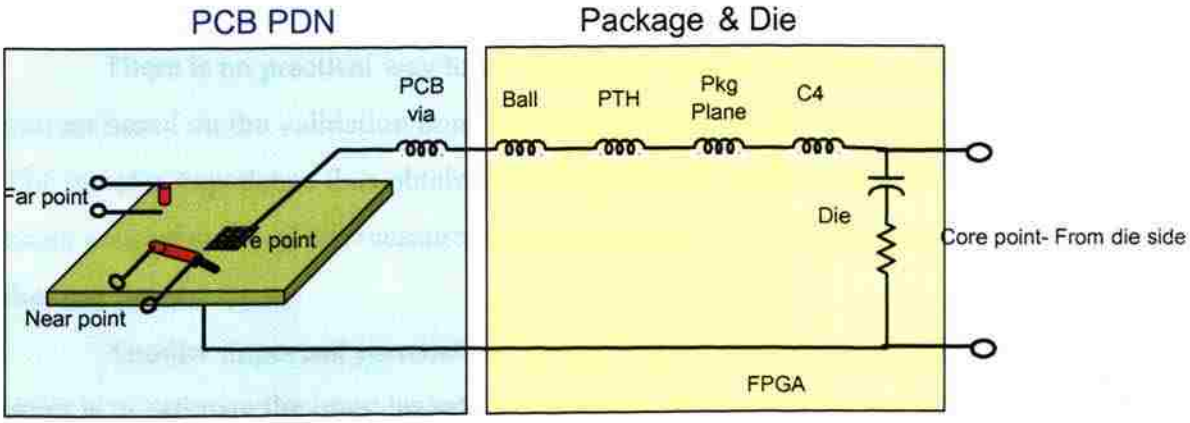

Figure 2.23. Spice Model of Package and PCB

Figure 2.24 show the transfer from the die side of the core to the far point and input impedance observed at far point.

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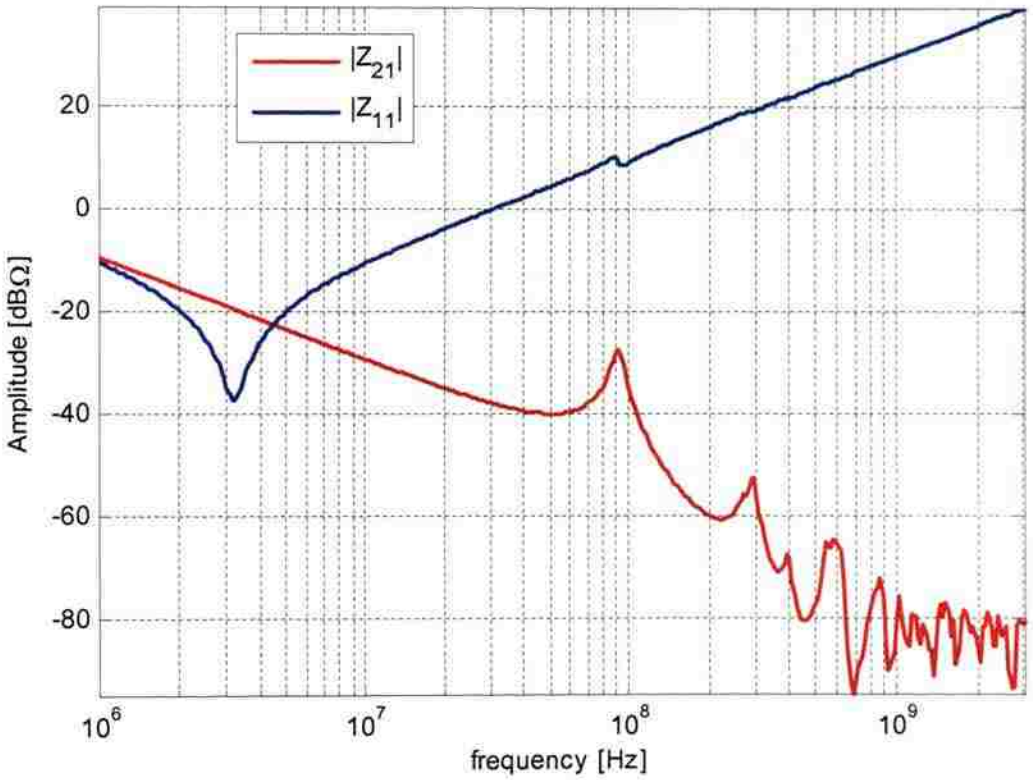

Figure 2.24. Transfer and Self Impedance from Die (Port 2) to Far Point (Port 1)

There is no practical way to validate these results, but they are assumed to be correct based on the validation done between far and near point as previously explained. The transfer impedance thus obtained from the SPICE model was used to estimate the noise voltage at any given measurement port. In this case, it is either at the far point or at the near point.

Another important parameter in estimating the noise power at the measurement point is to estimate the input impedance looking into the board at the measurement point. The EZPP model does not take the inductance associated with ports into account as seen in Figure 2.25. Input impedance of the near point can not be simulated accurately because of a poor SMA connection which causes extra capacitance and inductance.

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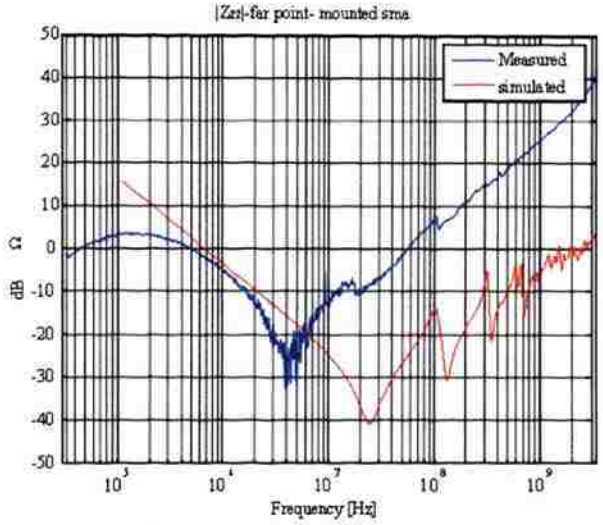

Figure 2.25. Simulated vs. Measured Input Impedance at Far Point

Once again HSPICE is used to include the port inductance and to obtain the input impedance of the measurement points. An inductance of 5nH was added at the far port measurement point. In the Figure 2.26 comparison is made between the measured and simulated self impedance.

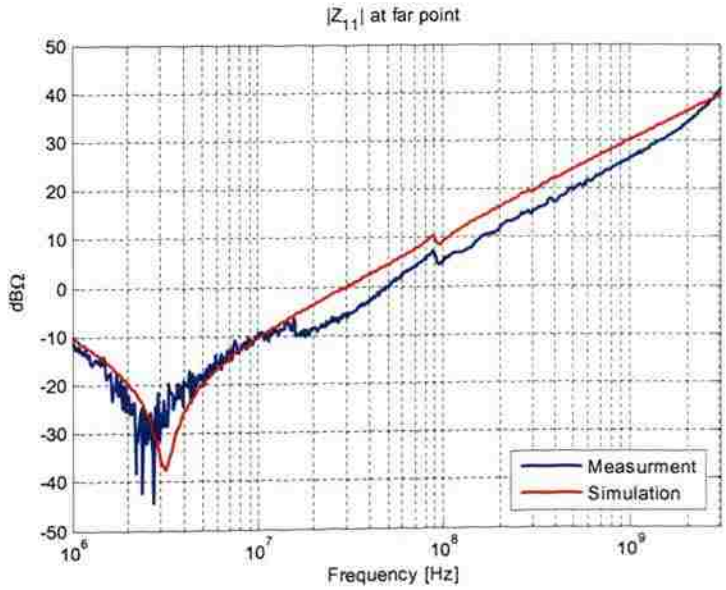

Figure 2.26. Simulated vs. Measured Input Impedance at Far Point with Series Inductance

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2.4. CURRENT SOURCE MODELING

Apart from impedance modeling, another most important parameter required to estimate noise is to model the current drawn. Current drawn can be estimated using two methods: TCO distribution method and PPPA analysis method which are described as follows.

2.4.1. Modeling Using TCO Distribution. The core noise is due the internal activity of the FPGA. To model the noise current, a triangular current source based on one register's activity can be constructed as shown in Figure 2.27. The pulse width of the triangular wave is determined by the speed of the transistor or how fast could the Flip-flop toggles. The other parameter, per unit pulse width, is determined by the correlation between the transistors and power plane. This parameter is shared to measure.

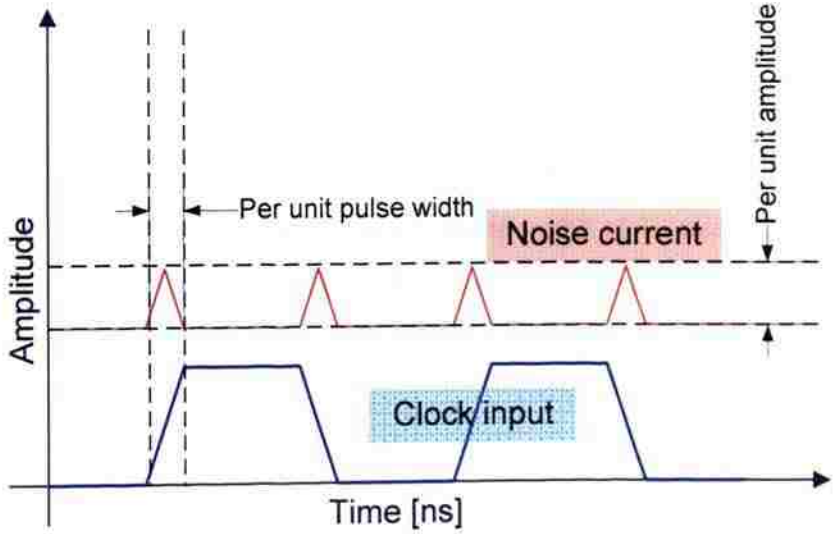

Figure 2.27. Current Source Model

From the per unit noise current can derive the total current based on the Quartus™ statistics. Quartus provides electrical path statistics (clock to output delay) in its timing analysis functionality. As shown in Figure 2.28, the actual clock to output delay is provided in the timing analysis report.

25

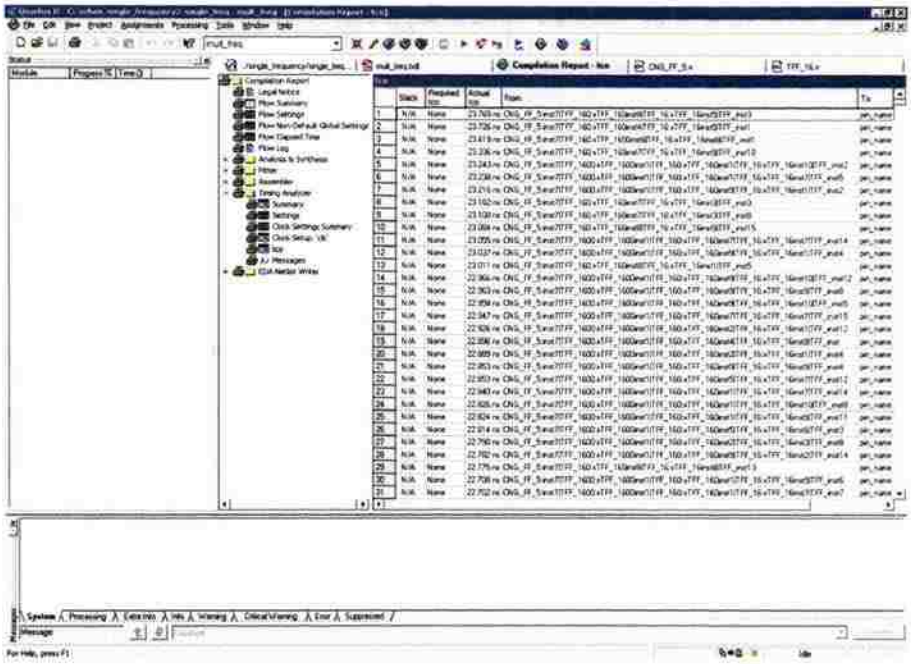

Figure 2.28. Clock to Output Delay Report Shown in Quartus Timing Analysis Report

The information is then extracted from the Quartus and processed by Matlab to create an electrical length distribution. Despite the phase information, Figure 2.29 shows the electrical length distribution had an approximate width of 10 ns using 30% of the toggling flip-flops utilization or 16,300 TFFs. The distribution had a standard deviation of 1.32 ns.

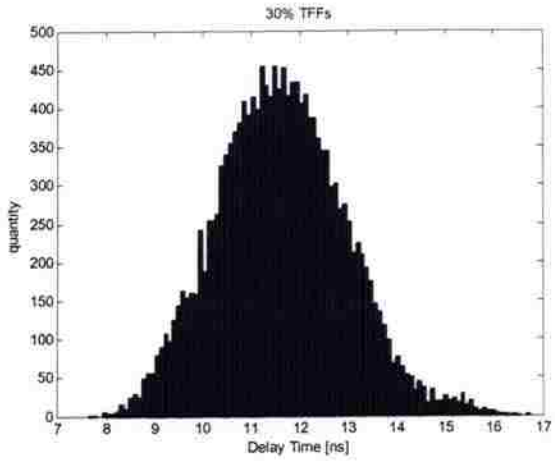

Figure 2.29. TFF Switching Delays

Using the integral equation below, the total current by the overall utilization of the FPGA could be derived,

$$I_{TFF} = F(t - t_{tco}), \tag{2.1}$$

$$I_{total} = \frac{1}{T}\int_{t=0}^{T} I_{TFF}\, dt \quad , \tag{2.2}$$

where t_{tco} is the time delay obtained from Quartus. $F(t - t_{tco})$ gives the total current associated with all the TFF switching at a particular instance of time. Integrating over the time period sums up all the current.

Figure 2.30 shows the shape of the total current pulse.

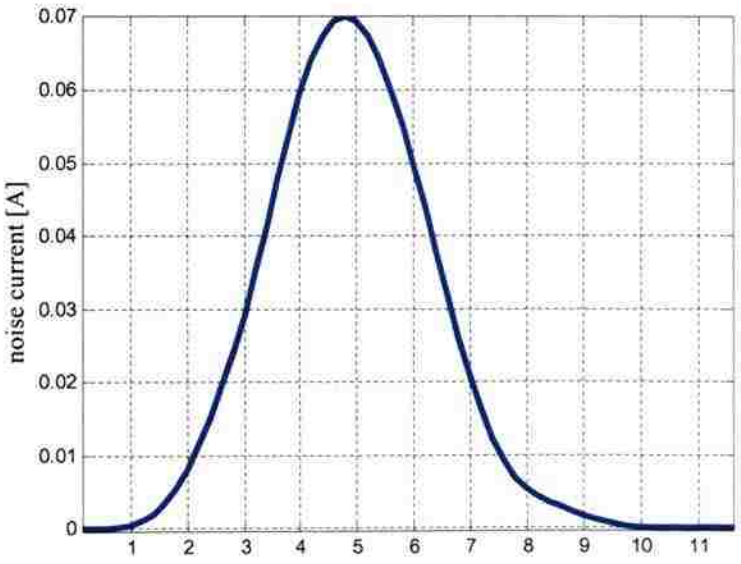

Figure 2.30. Total Current Estimated (One Pulse)

For the pattern used in the experiment, the electrical paths were split into two parts. One is the path from the input pin spell out a number of buffers to the clock input of the TFF, the other part is from the TFF to the output pin. As shown in Figure 2.31, the logic is a frequency splitter. The input path has a frequency of *2f* and output path has a freuency of *f*.

27

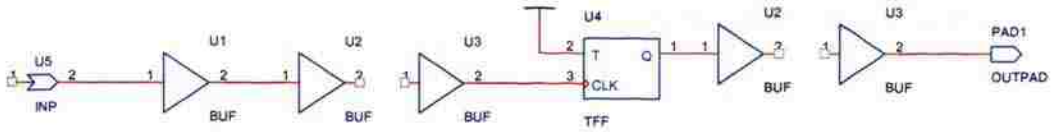

Figure 2.31. FPGA Logic of a Single Electrical Path

There are two electrical paths of noise current, as shown above. One was caused by clock transition, with a frequency the same as the clock frequency. The other was caused by the TFF toggling, the frequency is toggling frequency, half of the clock frequency. When both of noise current path were considered, the current amplitude at 0 ns, 200 ns, 400 ns was higher than 100 ns, 300 ns, and on 500 ns.

To more accurately model the noise current, an the following equation to include both electrical paths was developed :

$$I_{total} = \frac{1}{T}\int_{t=0}^{T} I_{TFF}\,dt + \frac{1}{2T}\int_{t=0}^{2T} I_{clock}\,dt \,. \qquad (2.3)$$

I_{clock} and I_{TFF} is the total current drawn by clock tree and TFF, respectively. A sum of the total current is shown in Figure 2.32.

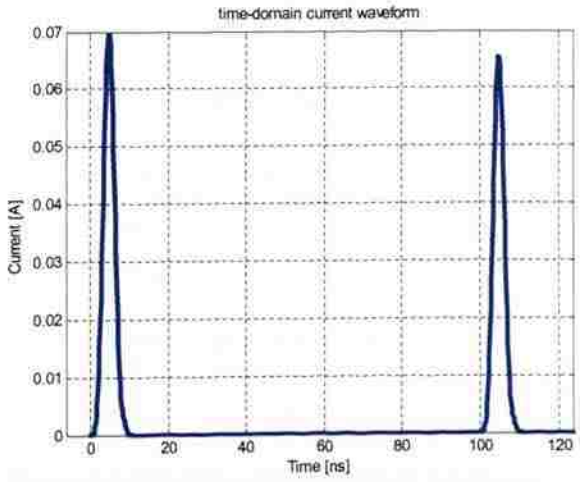

Figure 2.32. Total Current Using Two Frequencies Model

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Frequency patterns of the estimated current are shown in Figure 2.33. The frequency between two harmonics is a half of the input frequency. Based on the parameters chosen, the odd and even harmonics showed different amplitude.

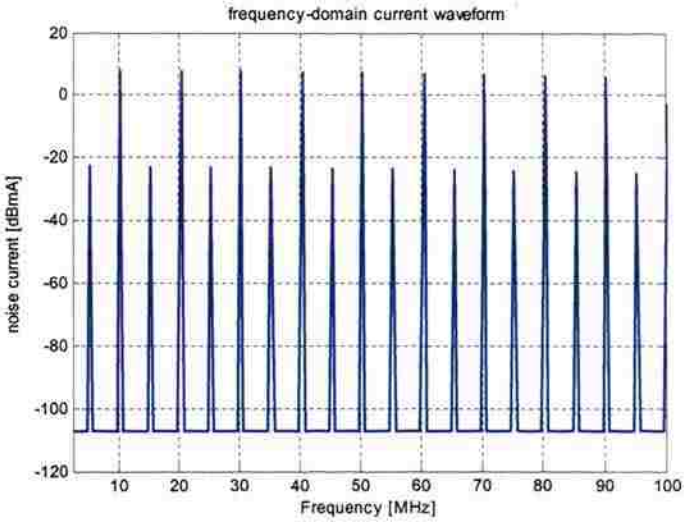

Figure 2.33. Total Current Spectrum Using Two Frequencies Model

2.4.2. Modeling Using PowerPlay Power Analyzer Tool. Another way of predicting the current consumption in the core is by using the PowerPlay Power Analyzer Tool built by Quartus shown in Figure 2.34.

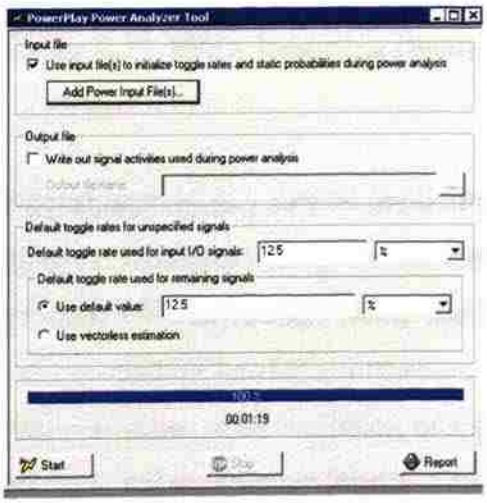

Figure 2.34. PowerPlay Power Analyzer Tool

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This tool basically estimates the power consumed by the FPGA for a particular pattern and a particular clock signal simulated.

The Quartus II software includes the PowerPlay power analyzer feature [5]. This feature improves the accuracy of power consumption estimations given by the early power estimator spreadsheets by:

- accounting for device resource usage and place-and-route results;
- accounting for functional and timing simulation input/output stimuli;
- performing statistical analysis of expected design-node activity rates when simulation vector inputs are not available;
- Producing detailed reports that can pinpoint which device structures, and even which design hierarchy blocks, are dissipating the most thermal power;

Figure 2.35 shows the available PowerPlay power analyzer reports.

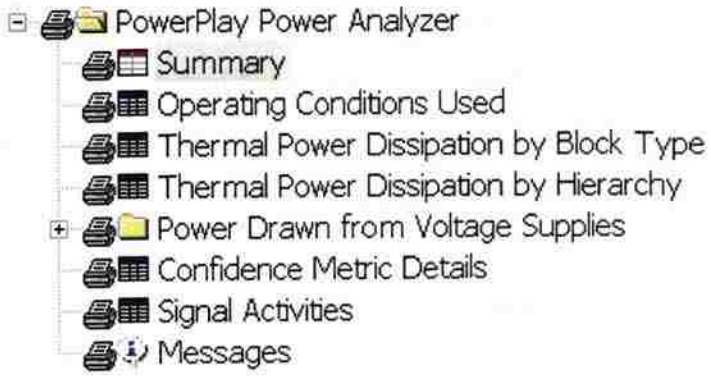

Figure 2.35. PPPA Reporting Details

In order to use the PowerPlay tool as a current predicting tool, the pattern should be first simulated with a frequency of interest using the Simulator tool in Quartus. A successful simulation will produce a Value Change Dump file VCD file. A Value Change Dump file is an ASCII file which contains header information, variable definitions, and the value changes for specified variables, or all variables, of a given design. The value changes for a variable are given in scalar or vector format, based on the nature of the variable. The PowerPlay tool can be used to import this VCD file. The resulting power

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analysis uses all the signal activities information from the generated VCD file to estimate the dynamic current drawn by any given pattern as shown in Figure 2.36. Since the pattern uses only core logic elements and does not include I/O, all the current is drawn from VCC.

Current Drawn from Voltage Supplies Summary

	Voltage Supply	Total Current Drawn (1)	Dynamic Current Drawn (1)	Static Current Drawn (1)	Minimum Power Supply Current (2)
1	VCCINT	796.96 mA	0.00 mA	796.96 mA	796.96 mA
2	VCCIO	4.00 mA	0.00 mA	4.00 mA	4.00 mA
3	VCCPD	4.32 mA	0.00 mA	4.32 mA	4.32 mA
4	VCCT	14.67 mA	0.00 mA	14.67 mA	14.67 mA
5	VCCH (1.2V)	0.00 mA	0.00 mA	0.00 mA	0.00 mA
6	VCCH (1.5V)	0.00 mA	0.00 mA	0.00 mA	0.00 mA
7	VCCR	45.45 mA	0.00 mA	45.45 mA	45.45 mA
8	VCCA	8.79 mA	0.00 mA	8.79 mA	8.79 mA
9	VCCP	44.26 mA	0.00 mA	44.26 mA	44.26 mA
10	VCCL	18.66 mA	0.00 mA	18.66 mA	18.66 mA

Figure 2.36. PPPA Current Estimation

One way of efficiently and correctly predicting the switching current is by conducting restricted time analysis of the VCD file [5]. The PowerPlay Tool provides the option to simulate the current or power estimation for a limited period of time, as shown in Figure 2.37. This option provides an opportunity to obtain the current value over a small period of time steps. Then by taking all the readings over at least one period of time it is possible to construct a current waveform in time domain.

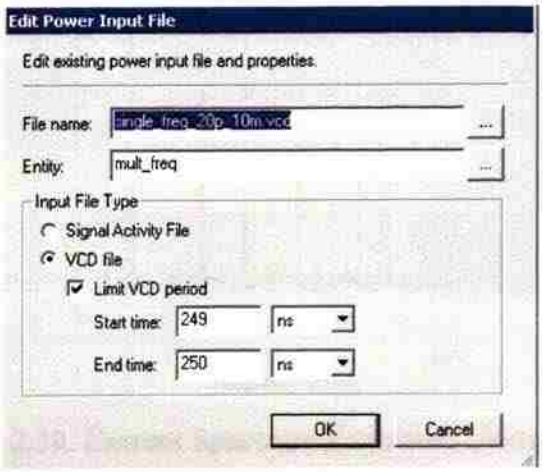

Figure 2.37. PPPA Restricted Time Analysis

A unique current signature is obtained for any given pattern simulated. Hence, this method can also be generalized to more complex patterns such as counters. A current waveform obtained from restricted time analysis is shown in Figure 2.38 in time domain and Figure 2.39 in frequency domain.

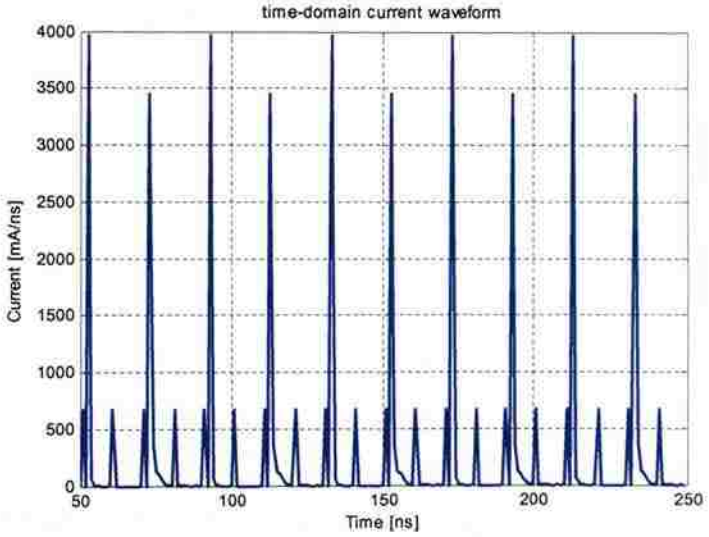

Figure 2.38. Current Estimated Using PPPA

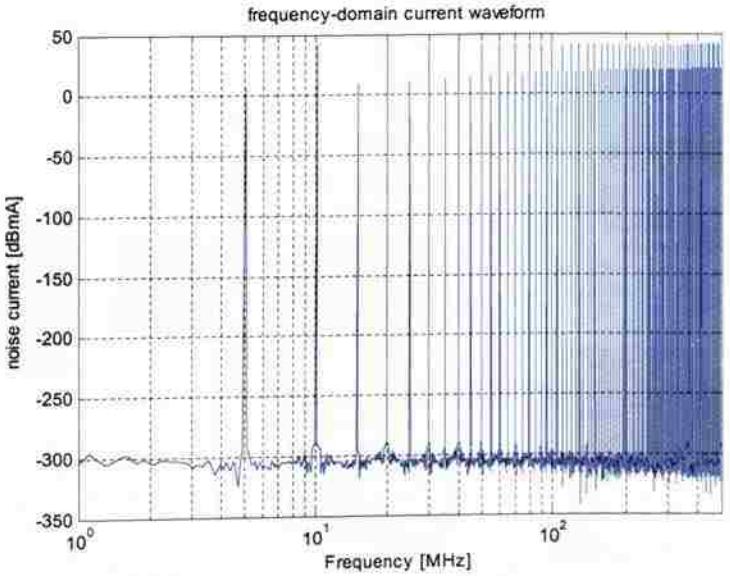

Figure 2.39. Current Spectrum Estimated Using PPPA

2.5. MEASUREMENTS

In order to validate simulations, good and accurate measurements are very important. One part of the measurement consists of measuring full two port S-parameters using a network analyzer at any given two ports on the board. Another part consists of spectrum measurements using a spectrum analyzer at any given observation point. These measurements, an actual test board, three power supplies, a signal generator, a computer, a network analyzer and a spectrum analyzer are needed.

The setup with all the required components is shown in the Figure 2.40. The power supply used for VCC was a special power supply with a sense line. This special line senses the voltage variations on the power plane and adjusts the voltage accordingly to maintain a constant voltage level. The board was setup as shown in the Figure 2.40 with all the three voltage supplies turned on. In order to measure S-parameter measurements, the board was turned on with all the three power supplies. The network analyzer is then connected to any two given observation ports to make full two-port measurements. For spectrum analyzer measurements, the board was first turned on with all three power supplies, and the clock signal was then applied using Stanford Research CG635 signal generator. Then the FPGA was programmed using Quartus. Once the program was loaded and running, spectrum analyzer was connected to the observation point to take spectrum readings.

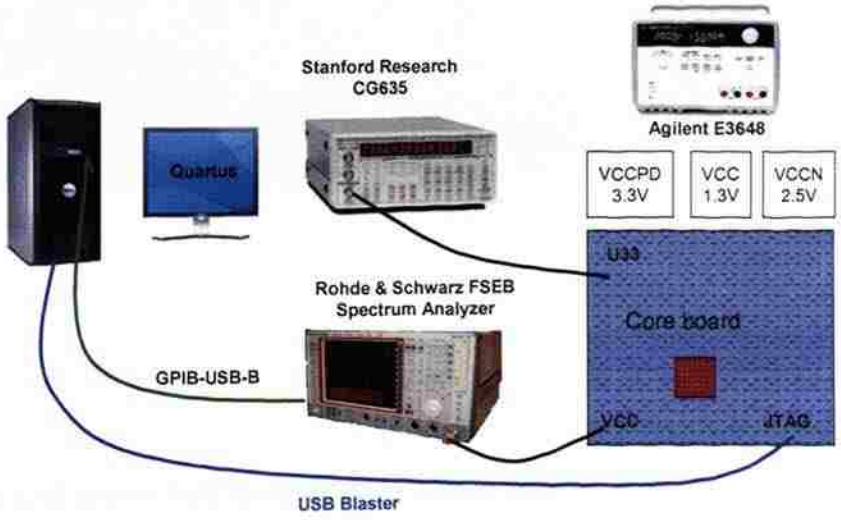

Figure 2.40. Measurement Setup

There were two main observation points, one which was close to FPGA and the other of which was far from the FPGA. They are named near point and far point respectively. The far point is a well connected SMA, while the near port was constructed by a coaxial cable probe mounted on the pads of decoupling capacitor pads as shown in the Figure 2.41. These two points were the main observation points for all the measurements concerned. S-parameter measurements were made between the far points and the near point with the board turned on, with and with out decoupling capacitors. Spectrum analyzer measurements are made either at the near point or at the far point with different clock frequencies, different percentage of TFFs, and with and without decoupling capacitors.

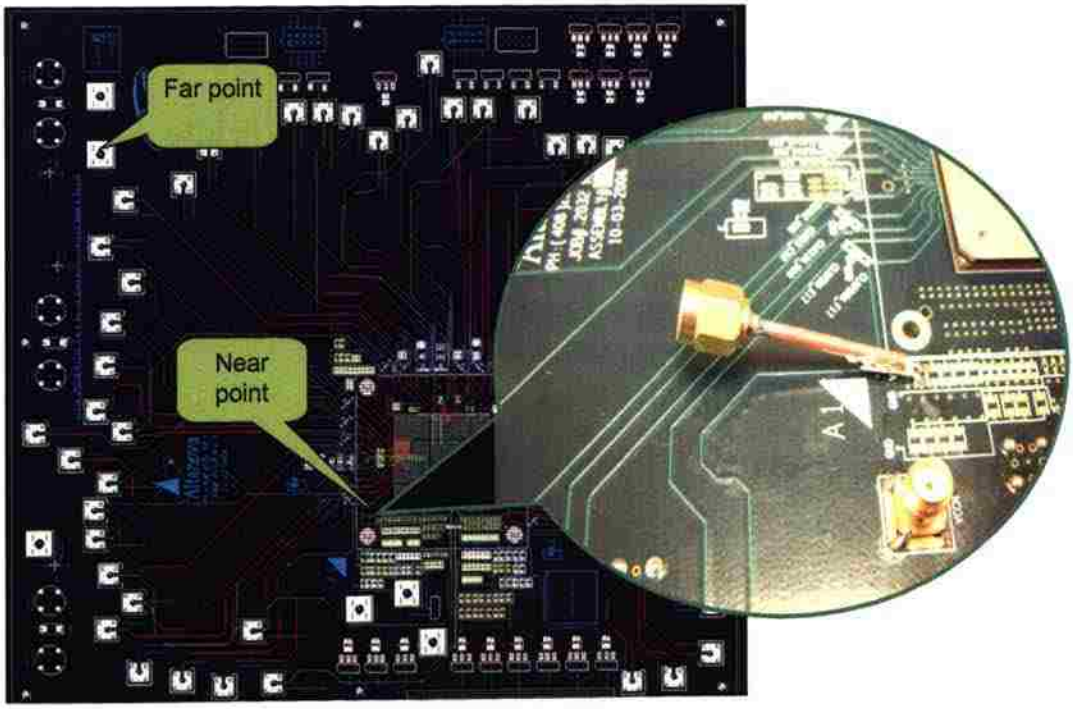

Figure 2.41. Near Point SMA Connection

All the spectrum analyzer measurements were made in a completely closed chamber in order to ensure that the noise measured was not affected by outside world noise. Figure 2.42 shows that the noise spectrum measured at the far point with clock frequency was 25 MHz, 10% of TFFs used. Because the toggling frequency is half of the

clock frequency, the frequency interval between peaks was 12.5 MHz. The resolution bandwidth was 5 KHz, to make the noise floor low (about -105 dBm).

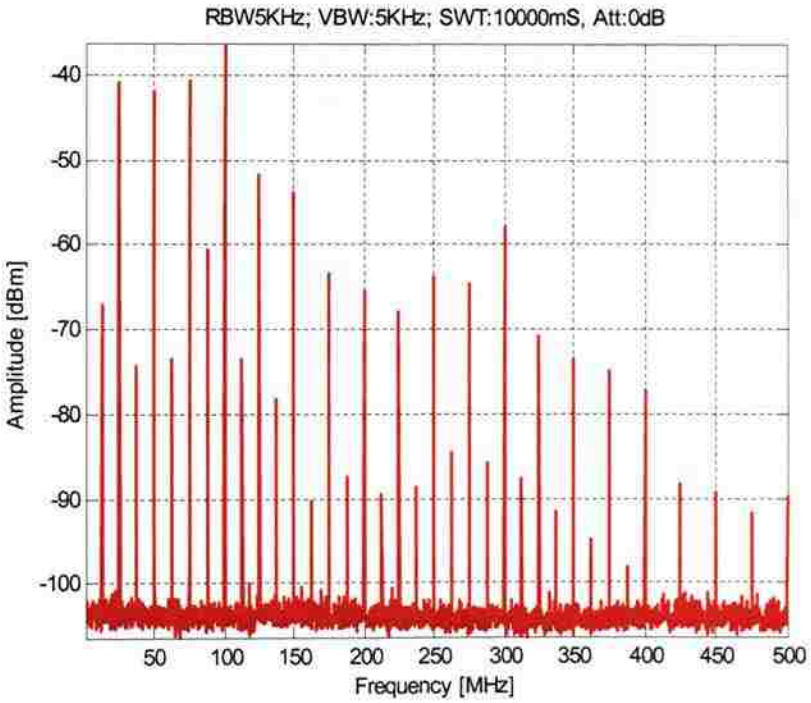

Figure 2.42. Spectrum Measurement at Far Point

Noise spectrum at 0%, 10%, 20%, and 30% of TFFs is compared. The value of each spectral component was then studied according to the percentage of TFF used. As shown in Figure 2.43, noise power was proportional to the amount of TFFs used. Noise spectrum at 0% is nothing but buffers toggling in the clock tree. Clock is routed significantly to all places of inside the FPGA. The routing requires buffers which consist of registers toggling at the frequency of the clock. This toggling of clock tree alone will contribute to noise generated. Figure 2.43 is a graphical representation of individual spectral component.

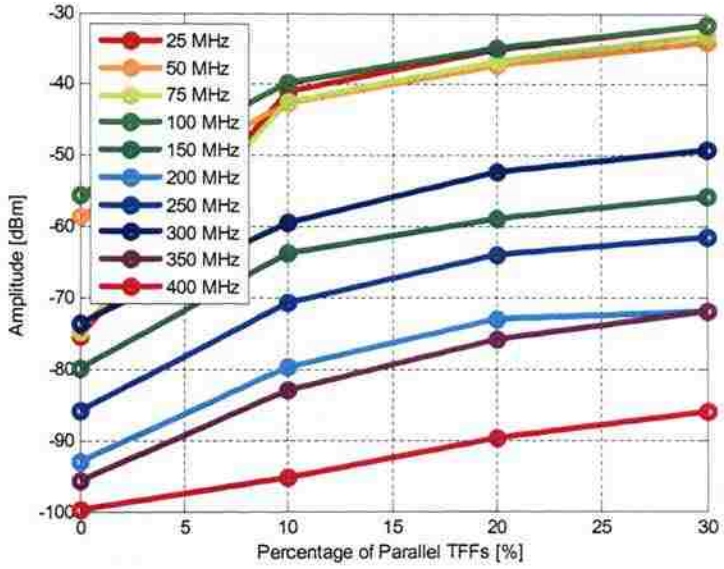

Figure 2.43. Spectral Component Comparison at Far Point

Similarly, the spectrum analyzer measurements were made at the near point with 25 MHz clock and 10% TFF used, as shown in Figure 2.44.

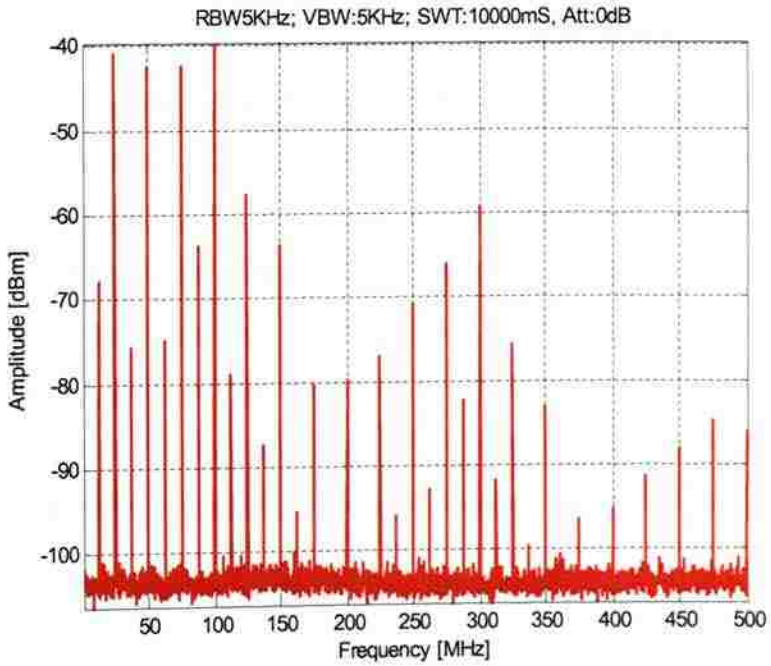

Figure 2.44. Spectrum Measurement at Near Point

36

Noise spectrum at 0%, 10%, 20%, 30% of TFFs is compared. Value of each spectral component is then studied according to the percentage of TFF used. As shown in Figure 2.45 noise power is proportional to the amount of TFFs used even for the near point.

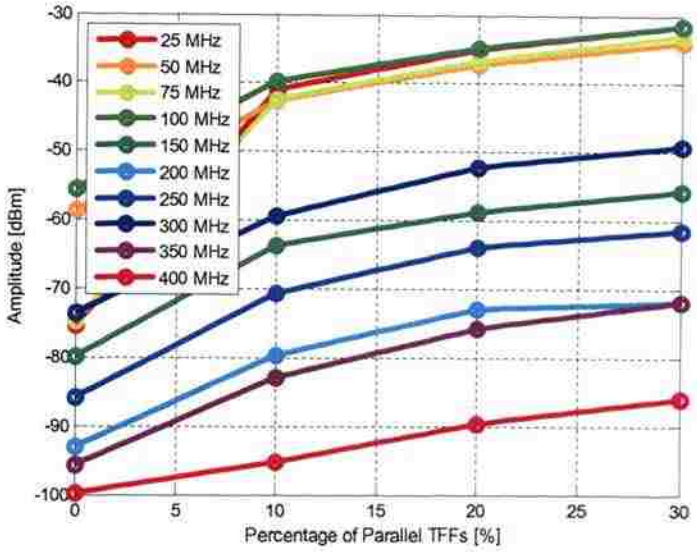

Figure 2.45. Spectral Component Comparison at Near Point

All the measurements with 0%, 10%, 20%, and 30% TFF used are taken along with different clock input of 10MHz, 25MHz, 50MHz , 70MHz, and 100MHz are taken both with and without decoupling capacitors at both far point and near points.

2.6. NOISE SPECTRUM ESTIMATION AND RESULTS

Once the current waveform is obtained and the estimated, either by using a TCO distribution or by using Power Play Analyzer, it is possible to obtain noise power at any given observation point. As shown in Figure 2.46 by using the transfer and self impedance associated for that point, noise is estimated as given by the following equations:

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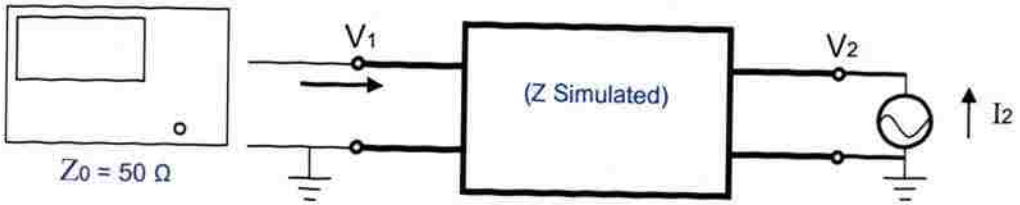

Figure 2.46. Noise Power Estimation Circuit

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \times \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, \tag{2.4}$$

Where $V_1 = I_1 \times 50\Omega$, (2.5)

$$V_1 = Z_{11} \times I_1 + Z_{12} \times I_2 = Z_{11} \times \frac{V_1}{50} + Z_{12} \times I_2 , \tag{2.6}$$

$$V_1 = Z_{21} I_2 / (1 - Z_{11}/50) , \tag{2.7}$$

$$\left| P_{spec} \right| = \left| |V_1|^2 / Z_0 \right| = \left| Z_{21} I_2 / (1 - Z_{11}/50) \right|^2 / 50 . \tag{2.8}$$

While estimating the noise power spectrum using a TCO distribution, the initial value of per unit current pulse width and amplitude were curve fitted. The initial value of per unit pulse width and amplitude were determined using one measured result at 25MHz, 10% of TFF implementation in the FPGA. The estimated power spectrum was then calculated using the equation above. To determine whether the fitted parameters can be applied to the measurements for the other frequencies, the same parameters were applied to calculate the estimated spectrum at different frequencies and different locations. The measurements were done on the bare board and do not include any capacitors.

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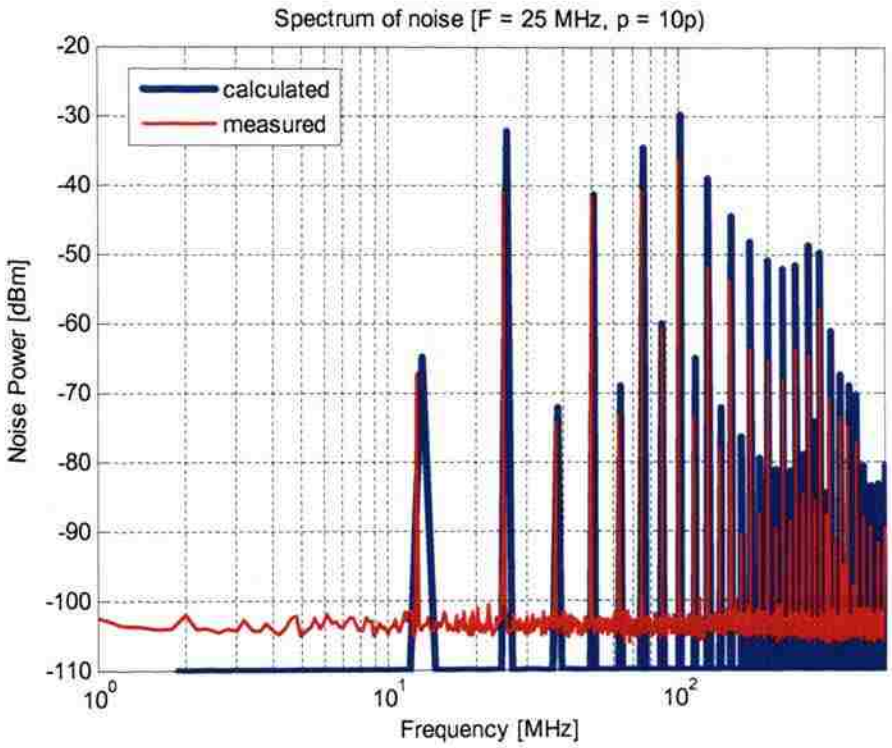

Figure 2.47. Noise Spectrum Calculated at 25 MHz, 10% TFF Using TCO Current Distribution

The fitted parameters are the following:

- single TFF current pulse amplitude = 5.5e-6 A;
- single TFF current pulse width = 1e-9 s;
- clock pulse amplitude = 45e-6 A;
- clock pulse width = 1e-9 s;

Once these parameters were determined by curve fitting any one of the spectral component, then the same parameters were used to calculate for other frequencies and other percentage of logic used, as shown in Figure 2.48, Figure 2.49, Figure 2.50 and 2.51. In Figure 2.48, 25 MHz clock and 30% TFF logic was used. In Figure 2.49 15 MHz clock and 10% TFF logic was used. In Figure 2.50 15 MHz clock and 30% TFF logic was used. Same parameters were used for simulations and measurements. Curve fitting was used only on one of the measurement data. Use of curve fitting will be very difficult when using complex patterns. Low frequency components are curve fitted, however high frequency components do not match with the measurements.

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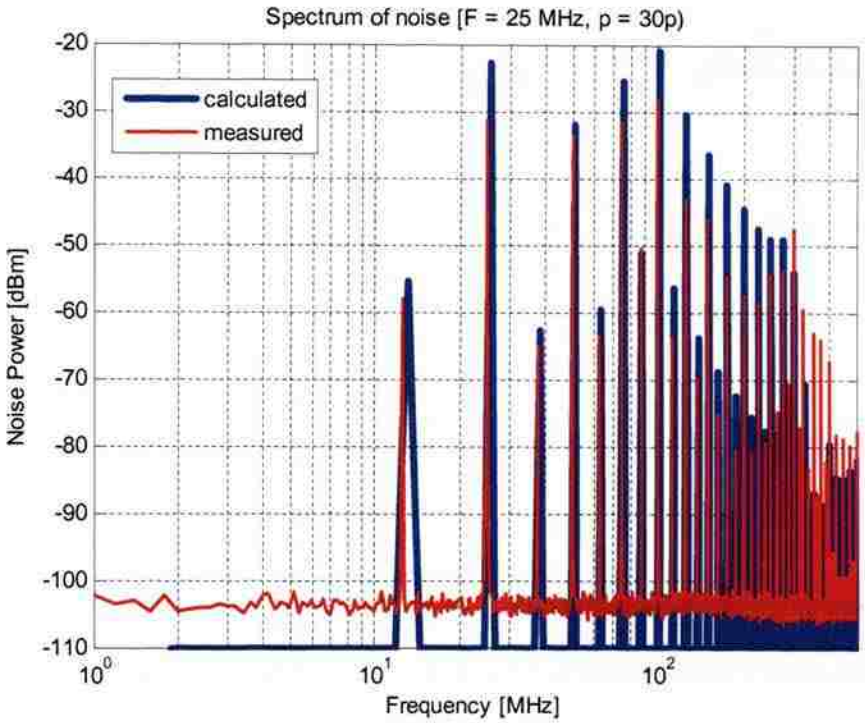

Figure 2.48. Noise Spectrum Calculated at 25 MHz, 30% TFF Using TCO Current Distribution

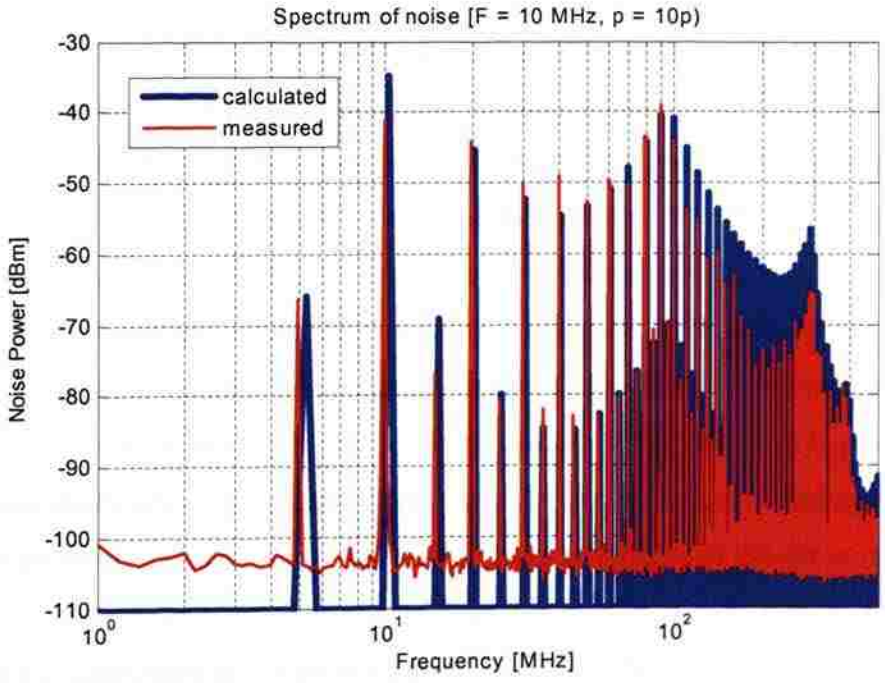

Figure 2.49. Noise Spectrum Calculated at 10 MHz, 10% TFF Using TCO Current Distribution

40

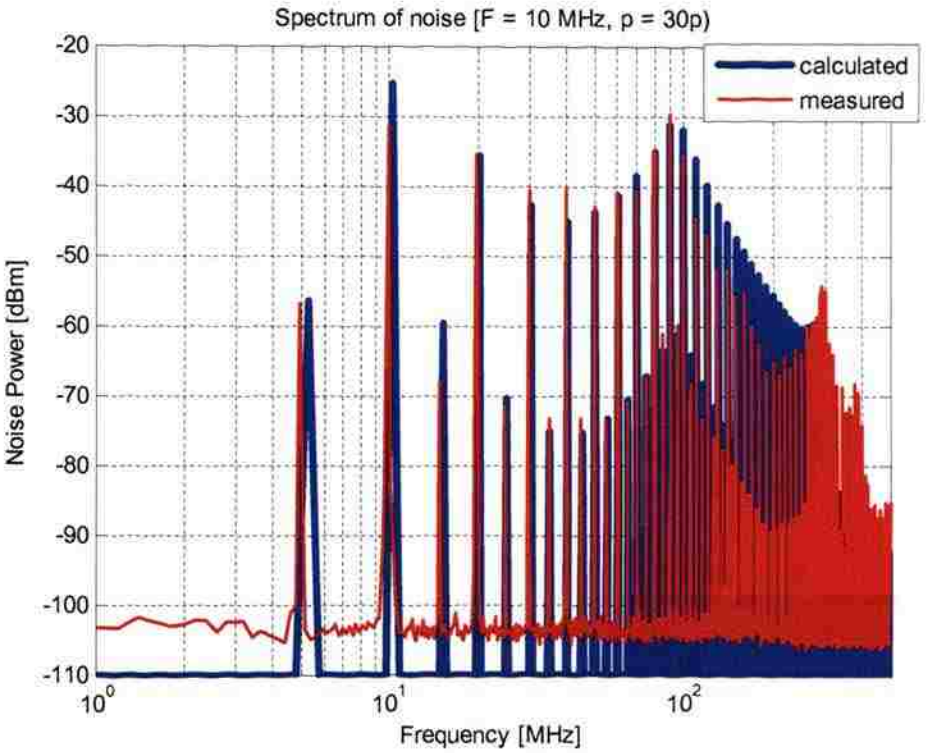

Figure 2.50. Noise Spectrum Calculated at 10 MHz, 30% TFF Using TCO Current Distribution

The above figures show that the high frequency components do not match with the measurements. This mismatch is mainly caused by way the current waveform is estimated. The TCO estimation does not take into account any fast switching current transitions, so all the high frequency components are lost. Curve fitting is very particular to a given pattern and may not work for more complex patterns.

On the other hand, estimating the current using the PPA, determines the exact amount of current at a particular switching instant. Calculating the noise spectrum using the current estimated from the PPA from the equations given above, it is possible to estimate the spectrum very accurately and easily with-out any curve fitting. Figure 2.51 compares the measured spectrum of 30% TFF used at 10MHz at the far point, which is relatively far from FPGA. The board here does not contain any capacitors. The comparison is also made at the point near to FPGA. The board does not contain any capacitors here. Figure 2.52 compares the measured spectrum of 30% TFF used at 10MHz at the far point.

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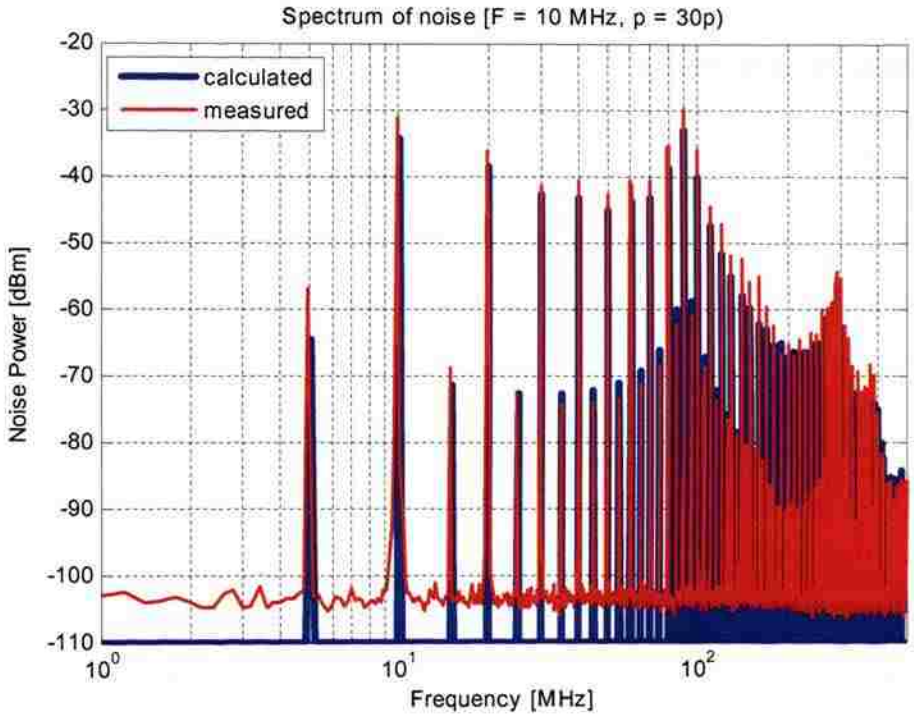

Figure 2.51. Noise Spectrum Calculated at 10 MHz, 30% TFF Using PPPA Current Distribution

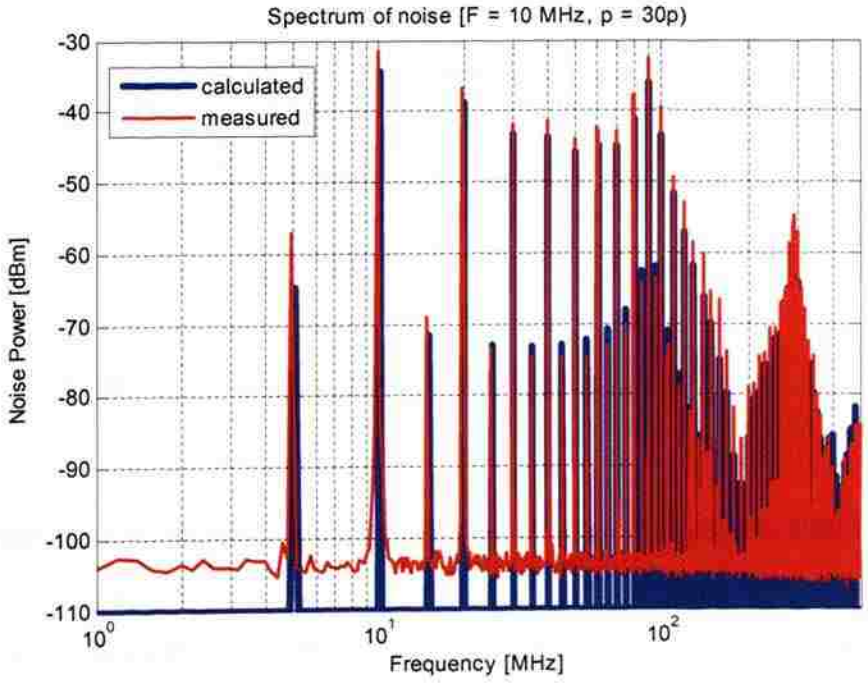

Figure 2.52. Noise Spectrum Calculated at 10 MHz, 30% TFF Using PPPA Current Distribution at Far Point

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This method can be used for any complex pattern apart from parallel switching TFF. The noise power is mainly modulated by transfer function from the source to observation point. Based on the noise predicted on the bare board, the decoupling strategy can be developed accordingly.

The noise measured at the observation points can also be analyzed in time domain. Measurements are made with an oscilloscope and the estimated current spectrum noise is converted back to time domain.

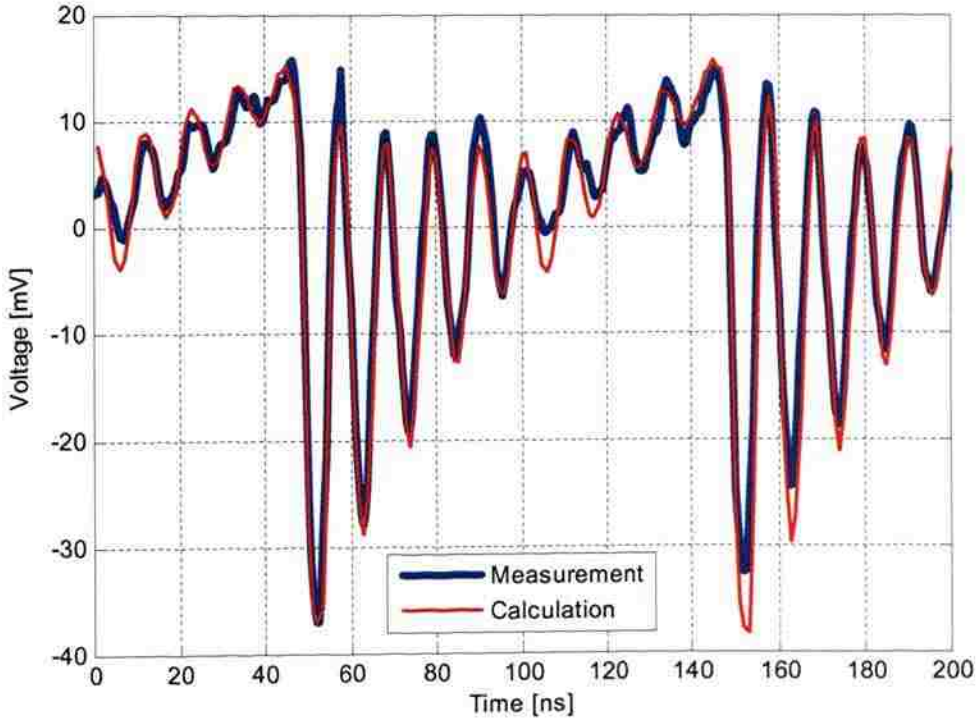

Figure 2.53. Time Domain Noise Voltage at Far Point

The measurement shown in Figure 2.53 was taken at the far point with no capacitors on board and with 30% of TFF logic used at 10MHz clock input. The DC offset was removed and then compared with the estimated noise voltage in time domain. This comparison was exactly the same as in Figure 2.51, but in time domain.

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3. ELECTROMAGNETIC SHIELDING

3.1. MATERIALS FOR SHIELDING

Two types of materials are studied for their shielding effectiveness and simulations are done to support the theory.

3.1.1. Composite Materials. Previous work done by the student [8], shows that composite materials can provide effective shielding [9] when manufactured accordingly. The program developed in [8], can estimate the shielding effectiveness of a composite material with any given properties. An example of the screen view for this program is shown in Figure 3.1.

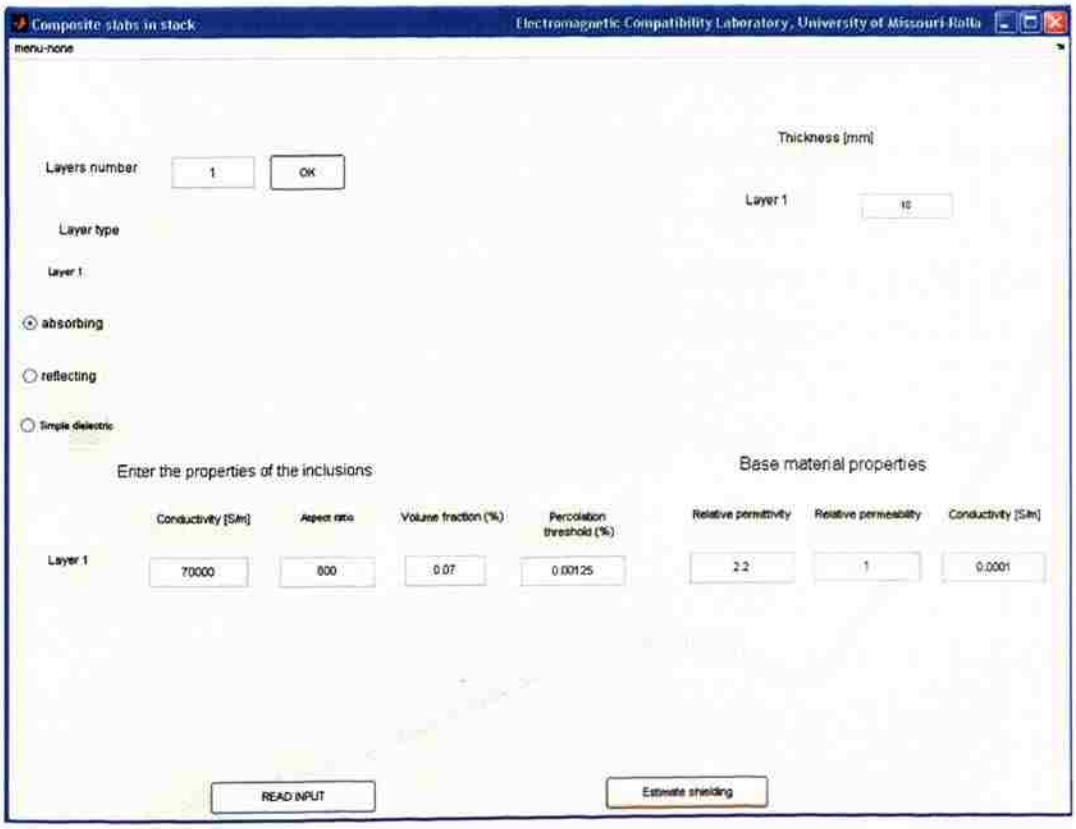

Figure 3.1. Composite Stack Shielding Estimator

Using the composite material properties from Table 3.1, shielding effectiveness is estimated is as shown in Figure 3.2.

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Table 3.1. Composite Material Properties

Carbon fiber composite material properties	
Fiber conductivity	70000 S/m
Fiber shape	cylindrical
Concentration	0.0007 vol. fraction
Aspect ratio (length/diameter)	800
Percolation threshold (equation 3.32)	0.00125 vol. fraction
Diameter of the fiber	$< 10\ \mu m$
Base material	Teflon ($\varepsilon = 2.2$)

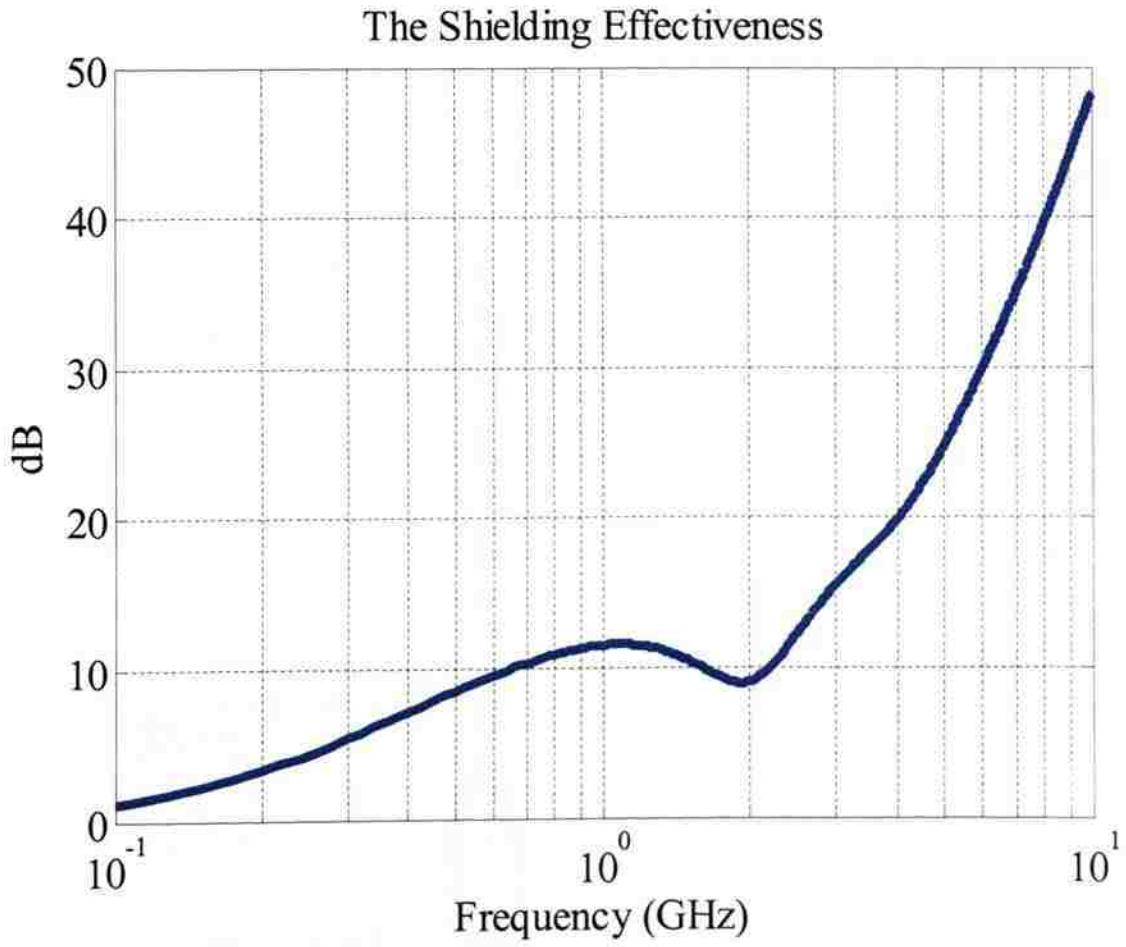

Figure 3.2. Analytical Shielding Effectiveness of Composite Slab of 10 mm thick

A 10 mm thick composite slab made of the materials in Table 3.1 has a promising shielding effectiveness, when the parameters of the material are controlled and uniform. Maxwell Garnett formalism has been successfully applied for engineering microwave absorbing materials containing carbon particles [10],

$$\varepsilon_{ef} = \varepsilon_b + \frac{\frac{1}{3}\sum_{i=1}^{n} f_i(\varepsilon_i - \varepsilon_b)\sum_{j=1}^{3}\frac{\varepsilon_b}{\varepsilon_b + N_{ij}(\varepsilon_i - \varepsilon_b)}}{1 - \frac{1}{3}\sum_{i=1}^{n} f_i(\varepsilon_i - \varepsilon_b)\sum_{j=1}^{3}\frac{N_{ij}}{\varepsilon_b + N_{ij}(\varepsilon_i - \varepsilon_b)}}. \tag{3.1}$$

where, f_i is the volume fraction occupied by the inclusions, N_{ij} are the depolarization factors of the i-th kind of inclusions , ε_b is the relative permittivity of a base dielectric, ε_i is the relative permittivity of i-th kind of inclusions. Index j=1, 2, 3 corresponds to x, y and z coordinates. Two depolarization factors are close to $N_{i1,2} \approx 1/2$ for cylindrical inclusions. The third depolarization factor is calculated as $N_{i3} \approx (1/a)^2 \ln(a)$, where $a = l/d$, or a ratio (length/diameter), is an aspect ratio of an inclusion.

The analytical formulation assumes that the inclusion aspect ratio is constant, and the length of each inclusion is much longer than its diameter, i.e. l / d >> 1. However, practically manufacturing such a material with a constant and high aspect ratio is difficult given today's technology. As shown in Figure 3.3, the particles look broken and do not maintain uniform aspect ratio.

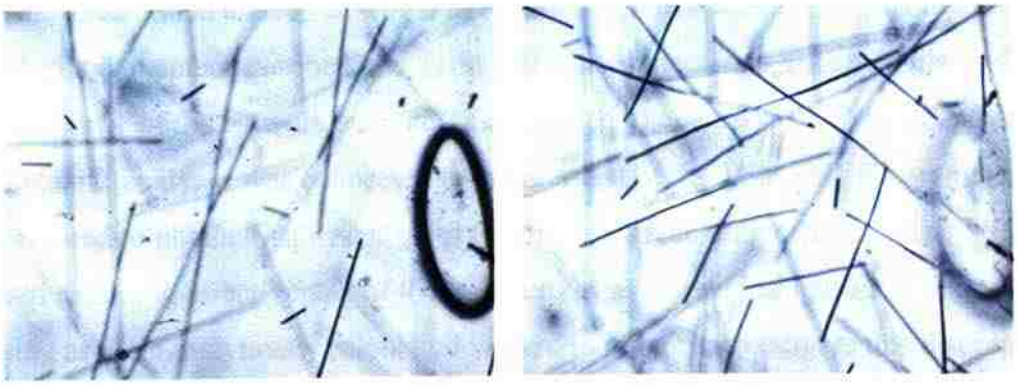

Figure 3.3. Microscopic View of Composite Materials

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shielding effectiveness was analyzed for the sensitivity of volume fraction. Figure 3.6 shows the variations of shielding effectiveness as the volume fraction of inclusions vary.

Figure 3.4. Composite Material Setup in TEM Cell

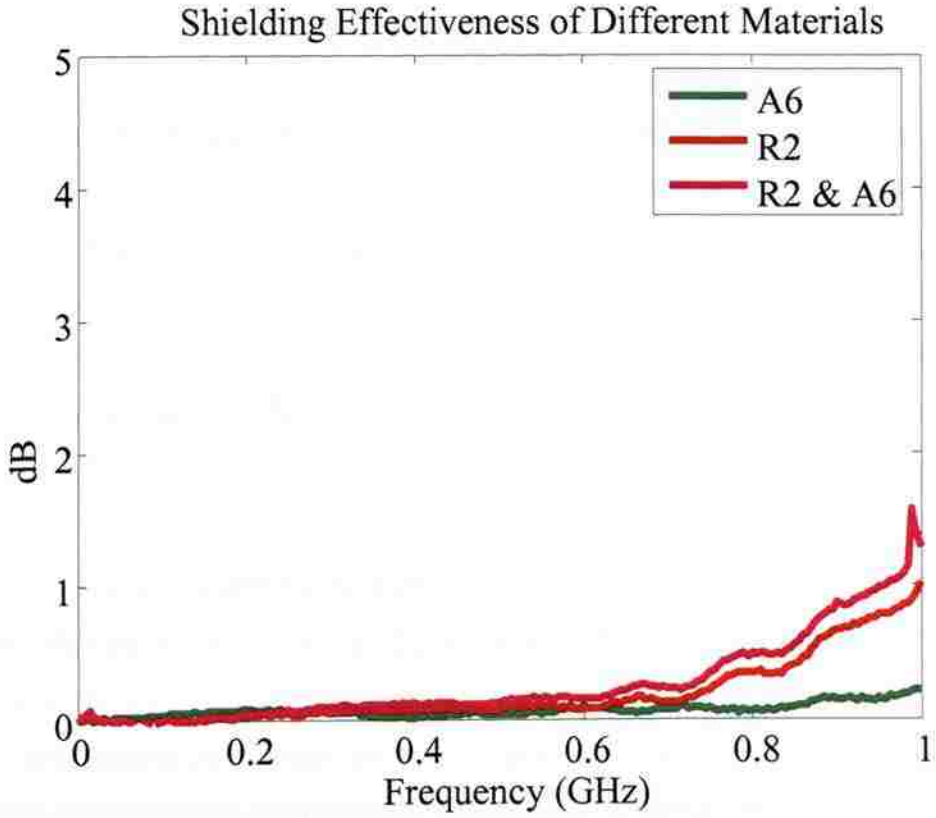

Figure 3.5. Composite Materials Measured Shielding Effectiveness

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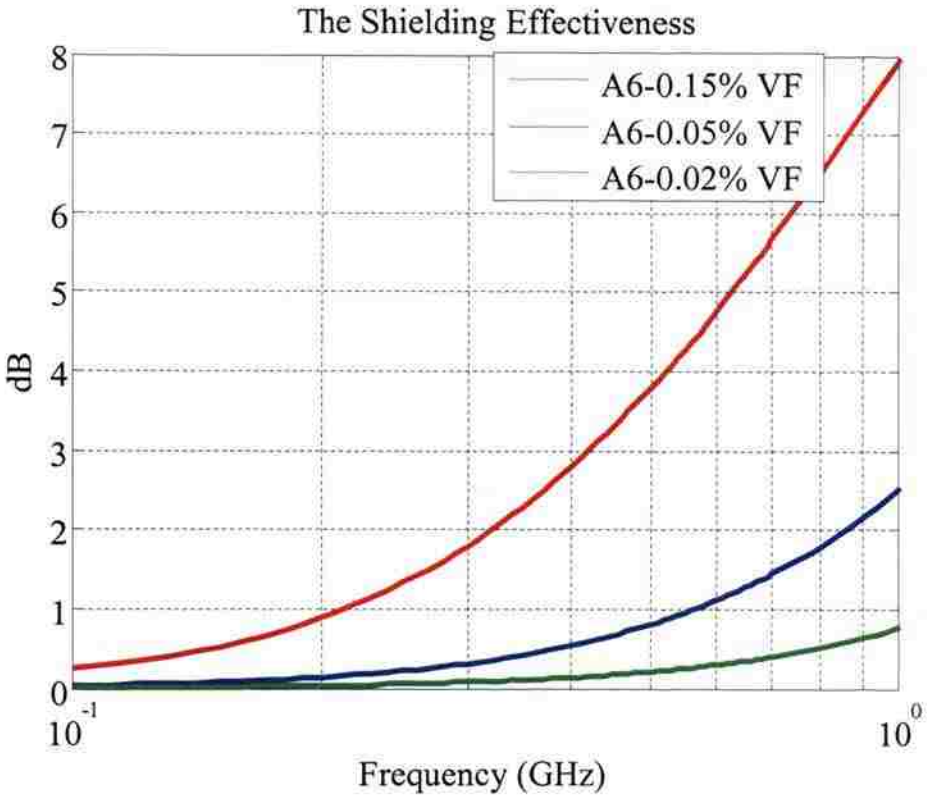

Figure 3.6. Sensitivity of Shielding Effectiveness to Volume Fraction of Inclusions

The volume fraction of A6 material is varied from 0.15% to 0.02%. It is seen from Figure 3.6 that the shielding effectiveness is highly sensitive to the volume fraction of inclusions. A small change in the volume fraction causes considerable variation of shielding effectiveness. Because the technology is not so advanced to control the volume fraction, the volume fractions in Table 3.2 cannot be trusted. So, a comparatively low shielding effectiveness is obtained, as shown in Figure 3.5. Composite materials are promising in terms of shielding, but not until technology can control the manufacturing variables.

3.1.2. Carbon-filled Foam Materials. On the other hand, carbon filled foam materials offer promising shielding effectiveness. These materials absorb and reflect electromagnetic radiation that passes through them. The foam is very light and soft. It can be easily manipulated and moved around. A stack up of these foam materials can be used to provide better shielding performance. The amount of carbon percentage inside these

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optimization technique based on specifically written genetic algorithm is used to curve fit the S-parameter data in such a way, that it yields the Debye curve parameters.

Figure 3.7. TEM Cell Measurement Setup

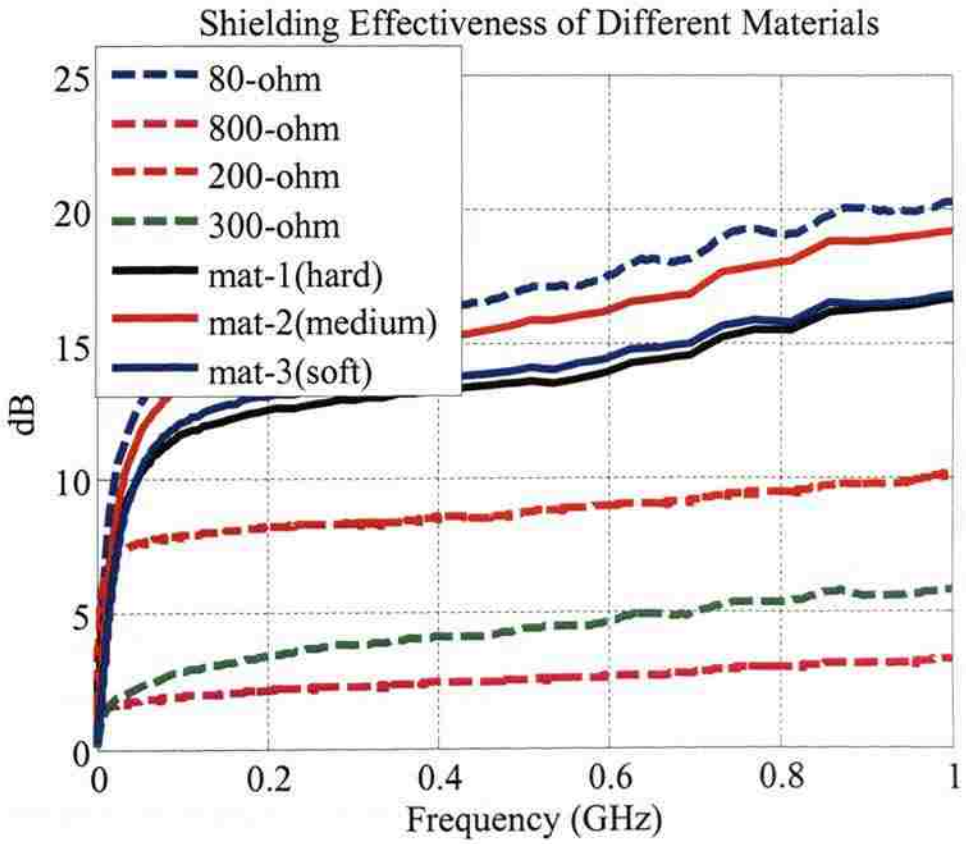

Figure 3.8. Shielding Effectiveness of Carbon Filled Foam Material

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Figure 3.9 illustrates the graphical user interface of the Debye parameter extractor tool.

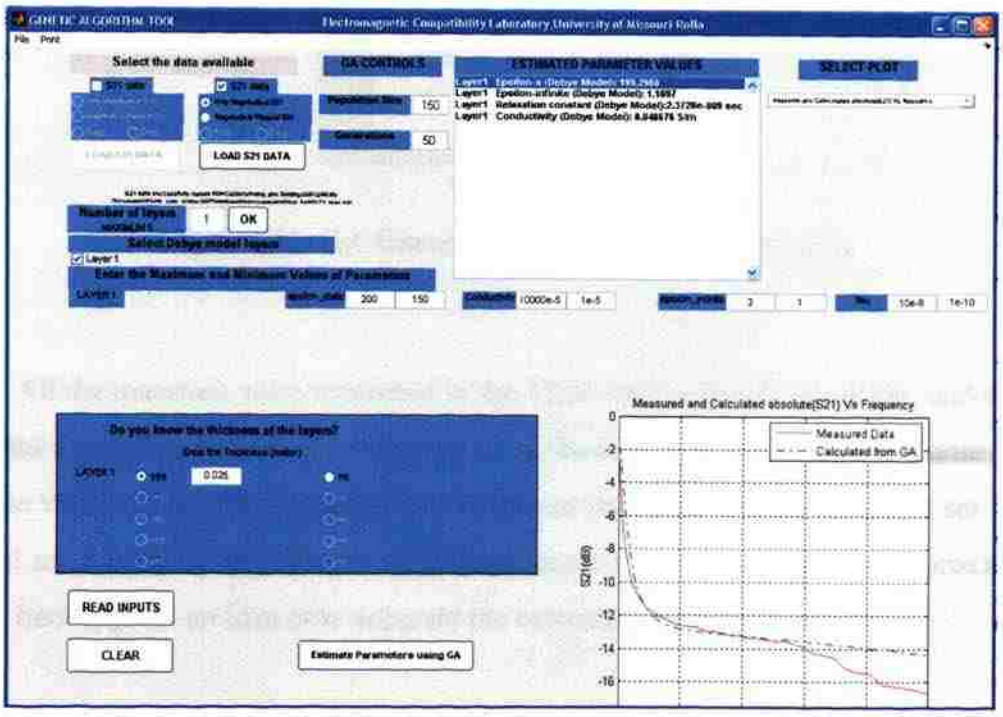

Figure 3.9. Debye Parameter Extraction Tool

The tool accepts the S-parameter data in magnitude alone or with both magnitude and phase as input. The user has to select how many layers are to be used, and how many of them are of the Debye type. Then an initial range of the Debye parameters is entered. Range of thickness, or even the exact thickness of the material, should be entered as well. Finally, the genetic algorithm variables of population size and generations number should be specified. Once all the parameters are entered into the tool, the tool can be run for curve fitting of the S-parameter data to obtain the Debye parameters. The results can be analyzed to see which set of parameter ranges must be changed to obtain a good curve fitting. The genetic algorithm varies and optimizes all the given variables simultaneously until the error with measured data is minimized. The solution given is one of many similar solutions. An example of such curve-fitted comparison between the measured data and the data obtained from the GA optimization is shown in Figure 3.10. Once the data has been curve-fitted, Debye parameters can be extracted.

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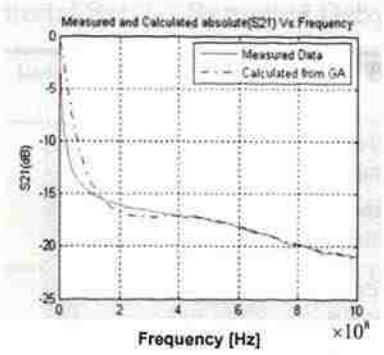


Figure 3.10. GA Curve Fitted Data vs. Measurements

All the materials were measured in the TEM cell as described earlier, and then the properties of each material were extracted using the GA tool. Table 3.4 and Table 3.5 show the values of the Debye parameters extracted using this tool for material set 1 and material set 2, respectively. The curve fitting column shows how good the approximation is, and, hence, gives an idea how accurate the extracted parameters can be.

Table 3.4. Material Set 1 – Extracted Debye Parameters

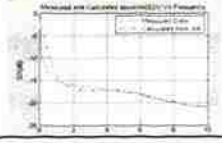
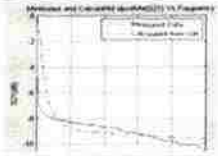
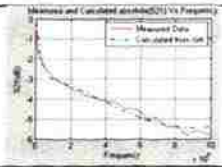
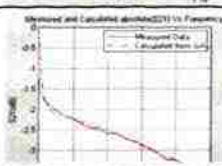
Material	Curve fitting using GA (up to 1GHz)	Estimated Debye parameters
80 ohm (0.025m thick)		**Epsilon Static : 192.3** **Epsilon Infinite : 39.2** **Relaxation constant : 5.1e-10 s** **Conductivity : 0.012 S/m**
200 ohm (0.025m thick)		**Epsilon Static : 99.47** **Epsilon Infinite : 1.0565** **Relaxation constant : 2.1e-9s** **Conductivity : 0.005011 S/m**
300 ohm (0.025m thick)		**Epsilon Static : 61.38** **Epsilon Infinite : 9.65** **Relaxation constant : 5.5e-9** **Conductivity : 0.00331 S/m**
800 ohm (0.025m thick)		**Epsilon Static : 57.61** **Epsilon Infinite : 5.38** **Relaxation constant : 8.1e-9 s** **Conductivity : 0.0011075 S/m**

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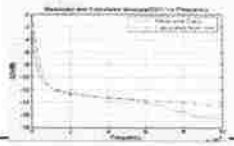
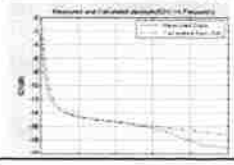
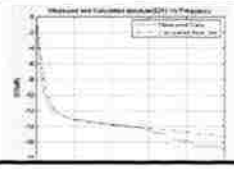
Table 3.5. Material Set 2 – Extracted Debye Parameters

Material	Curve fitting using GA (up to 1GHz)	Estimated Debye parameters
Mat – 1 hard kind (0.025m thick)		**Epsilon Static : 199.56** **Epsilon Infinite : 1.55** **Relaxation constant : 2.2e-9s** **Conductivity : 0.000535 S/m**
Mat – 2 medium hard kind (0.025m thick)		**Epsilon Static : 249.67** **Epsilon Infinite : 1.3326** **Relaxation constant : 2.1e-9s** **Conductivity : 0.0077 S/m**
Mat -3 soft kind (0.025m thick)		**Epsilon Static : 199.825** **Epsilon Infinite : 1.17** **Relaxation constant : 2.05e-9** **Conductivity : 0.00092 S/m**

3.2. MODELING

After extracting the Debye parameters from the materials, it is possible to use them for further analytical modeling or 3-D full wave numerical modeling of structures containing such materials. Full wave modeling helps in predicting the behavior of materials in complex geometry and at higher frequencies. Analytical modeling can be used to validate the full-wave model in the known environment.

3.2.1. Analytical Modeling. Analytical modeling using a plane-wave formulation is basically calculating the transmission and reflection coefficients for the material of the given thickness. Plane wave propagation is assumed through the air and through the material. The effective complex permittivity of the material is calculated, which is then used to calculate the complex propagation constant across the material. ABCD parameters are obtained using this propagation constant. The ABCD are converted to S-parameters to obtain the shielding effectiveness of an infinitely long sheet for a plane wave excitation. Once the ABCD parameters are known, they can be cascaded for any number of layers, giving an opportunity to calculate the total parameters of interest for any stack of layers. The ABCD parameters are then converted into S-parameters to get the shielding effectiveness of interest [11].

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The complex effective permittivity for the Debye dielectric is calculated as

$$\varepsilon_a = \varepsilon_o \varepsilon_r = \varepsilon_o \left(\varepsilon_\infty + \frac{\varepsilon_s - \varepsilon_\infty}{1 + j\omega\tau} \right) - \frac{\sigma_e}{j\omega} \quad , \tag{3.2}$$

$$\gamma = j\omega\sqrt{\mu\varepsilon_a} \quad , \tag{3.3}$$

Where, ε_s is the static permittivity, ε_∞ is the optic limit permittivity, σ_e is the effective conductivity, τ is the relaxation constant and γ is the propagation constant. Then, the ABCD parameters are calculated using propagation constant as follows,

$$A = \cosh(\gamma \times d); \tag{3.4}$$

$$B = Z_o \times \sinh(\gamma \times d); \tag{3.5}$$

$$C = \frac{1}{Z_o} \times \sinh(\gamma \times d); \tag{3.6}$$

$$D = \cosh(\gamma \times d), \tag{3.7}$$

where d is the thickness of the material. Using the data from Table 3.4, the shielding effectiveness of each material is analytically calculated and compared with the measurements. Figure 3.11 shows the comparison of the calculated S.E. to the measurements.

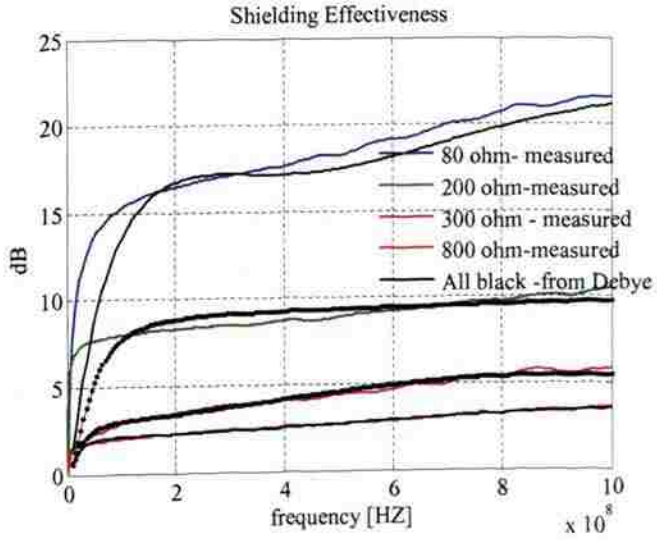

Figure 3.11. Analytical Calculation of Shielding Effectiveness

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Similarly, a stack of different materials is measured and then compared to the analytically calculated shielding effectiveness, as shown in Figure 3.12. Measurements here are done using the TEM cell, as described earlier. Each material is cut into a 1.25 cm thick block and stacked together inside the TEM cell.

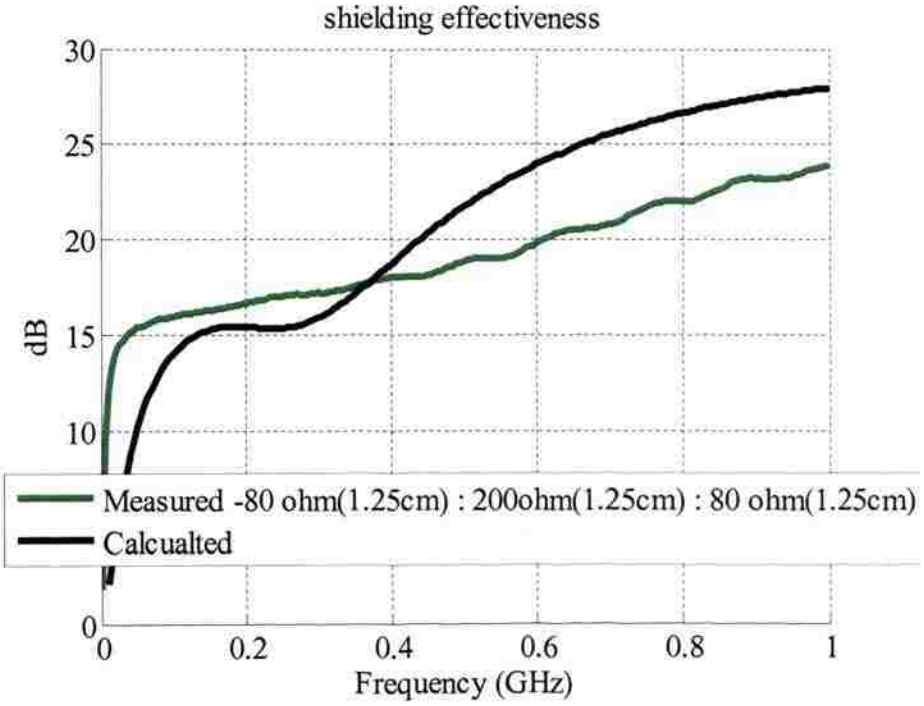

Figure 3.12. Analytical S.E. of Stack of Materials

3.2.2. Full Wave 3-D Modeling. Analytical modeling has the ability to model infinitely long sheets with only plane wave excitation. It is not possible to analyze how the fields inside complex structures behave in different conditions. Thus, for analyzing complex structures a model that employs a full wave 3D Maxwell equation solver is needed. EZ-FDTD is used in this case to model complex box structures made of the material with the given Debye characteristics.

Before analyzing complex structures, it is important to validate 3-D modeling with the known analytical solution. The Debye dielectric material is placed in between the PEC plates, and these PEC plates are extended into the boundaries to make it infinite. The setup is shown in the Figure 3.13, where FD1 is the Debye dielectric material, P1

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and P2 are the PEC plates, S1 is the pseudo wire source and MP1 is the monitor point for E and H fields. The figure depicts a top view of the geometry. Table 3.6 shows the simulation parameters used.

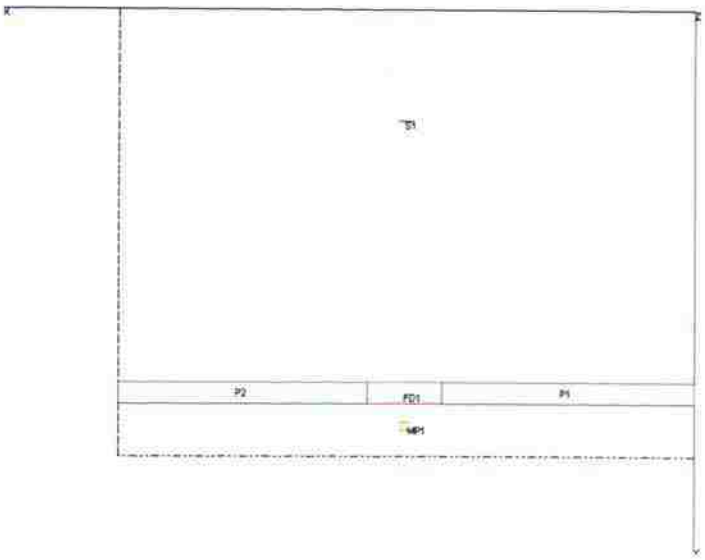

Figure 3.13. Modeling Debye Dielectric Slab for Estimating Shielding Effectiveness

Table 3.6. FDTD Model Details Debye Dielectric Slab Simulation

Computational Domain Size	78, 60, 160 cells in x, y and z directions respectively
Cell size	0.005, 0.001, 0.001 meters in x, y and z directions respectively
Source	Pseudo Wire
Boundary Scheme	PML
Debye Material Dimensions	10, 3, 160 cells in x, y and z directions respectively
Frequency Range	100MHz – 10GHz

The source is placed at the center of the (ZX) plane. The field monitor point is also placed at the center of (ZX) plane, and three cells away from the material. The

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material simulated was the "80-ohm" material with the properties detailed in Table 3.4. In order to obtain shielding effectiveness, it also important to simulate an empty computational domain with out the Debye material. The model has the exact properties shown in Figure 3.13 and Table 3.6, but with out the Debye material. Once the E and H fields are obtained from both of simulations, the ratio of E or H field with empty space to E or H field with the material gives the shielding effectiveness of the simulated material. Figure 3.14 shows the comparison of the simulation result to the analytically calculated result.

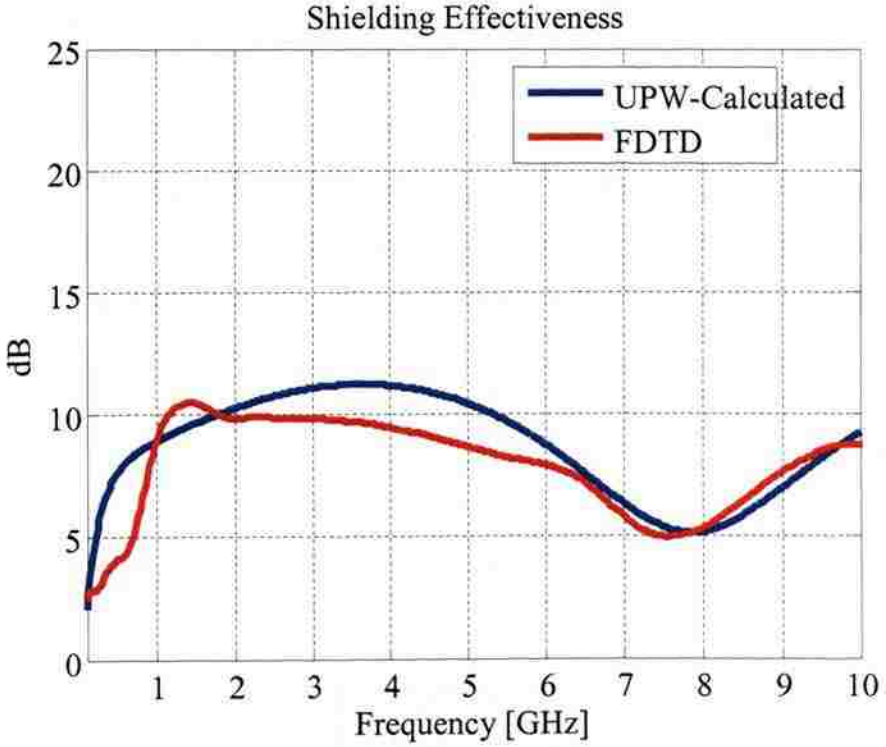

Figure 3.14. FDTD Infinite Debye Sheet Shielding Effectiveness

The difference between the analytical and simulated result is mainly because due to the observation point. The analytical solution, as in equations (3.1) – (3.7), assumes far field, while the full-wave simulation includes the near-field region. Once it has been ensured that the 3-D simulation works as expected, more complex geometries made of this material can be simulated.

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A useful simulation to conduct is to simulate a box made of these materials. This box is that it intended to provide the maximum possible shielding effectiveness, even if there are some presence of some gaps along the walls and vent holes for air circulation. In order to estimate how the box made of these materials can perform with the given set of materials, it is necessary to simulate the entire box.

The structure of the box is chosen in such a way that it can provide the maximum shielding for the given thickness of walls. Figure 3.8 illustrates that the "80-ohm" material has the highest shielding for the given thickness (2.5 cm). The material was cut into two equal 1.25-cm thick blocks, and a PEC plate was placed in between them to increase the shielding. However, the PEC plates were placed 1cm away from the edges in order to avoid any edge currents that can effectively radiate and reduce the shielding effectiveness. The box was simulated with a plane wave propagating across the box. The field monitor points were placed inside the box to measure E and H fields. First, a box with no gap between the materials was simulated to observe the overall shielding in the best case. Figure 3.15 shows the geometry simulated. Figure 3.15 shows that the PEC plates (blue thin blocks) were not close to each other; they were sandwiched between the Debye dielectric materials (thick orange blocks).

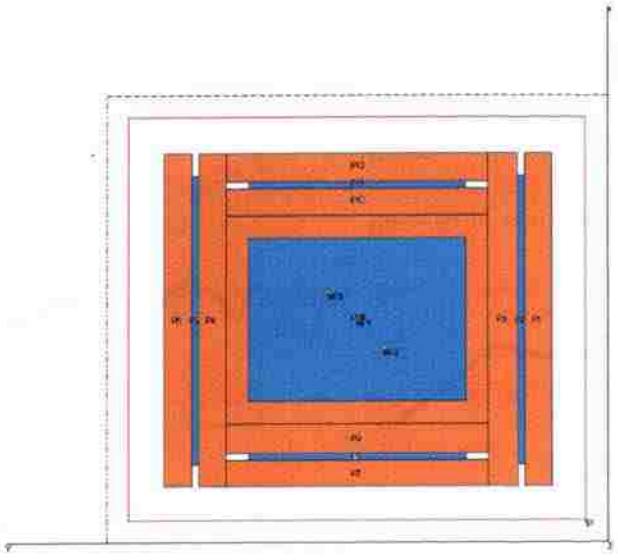

Figure 3.15. Debye Material Box - No Gap

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Figure 3.16 shows that the S.E for both E and H fields was on the order of 40 dB average. With a combined effect of the PEC added to the Debye material, it was possible to achieve 40 dB of shielding in the best case.

However, it is not always possible to build a box with completely closed edges. The walls of the box can have a gap between them, through which fields can penetrate. In order to study a more practical case, gaps of 2-mm wide were left all around the walls of the box, as shown in Figure 3.17. The (XZ) plane plot also looks the same, since the box is almost a square. Table 3.8 shows the simulation parameters used in this simulation.

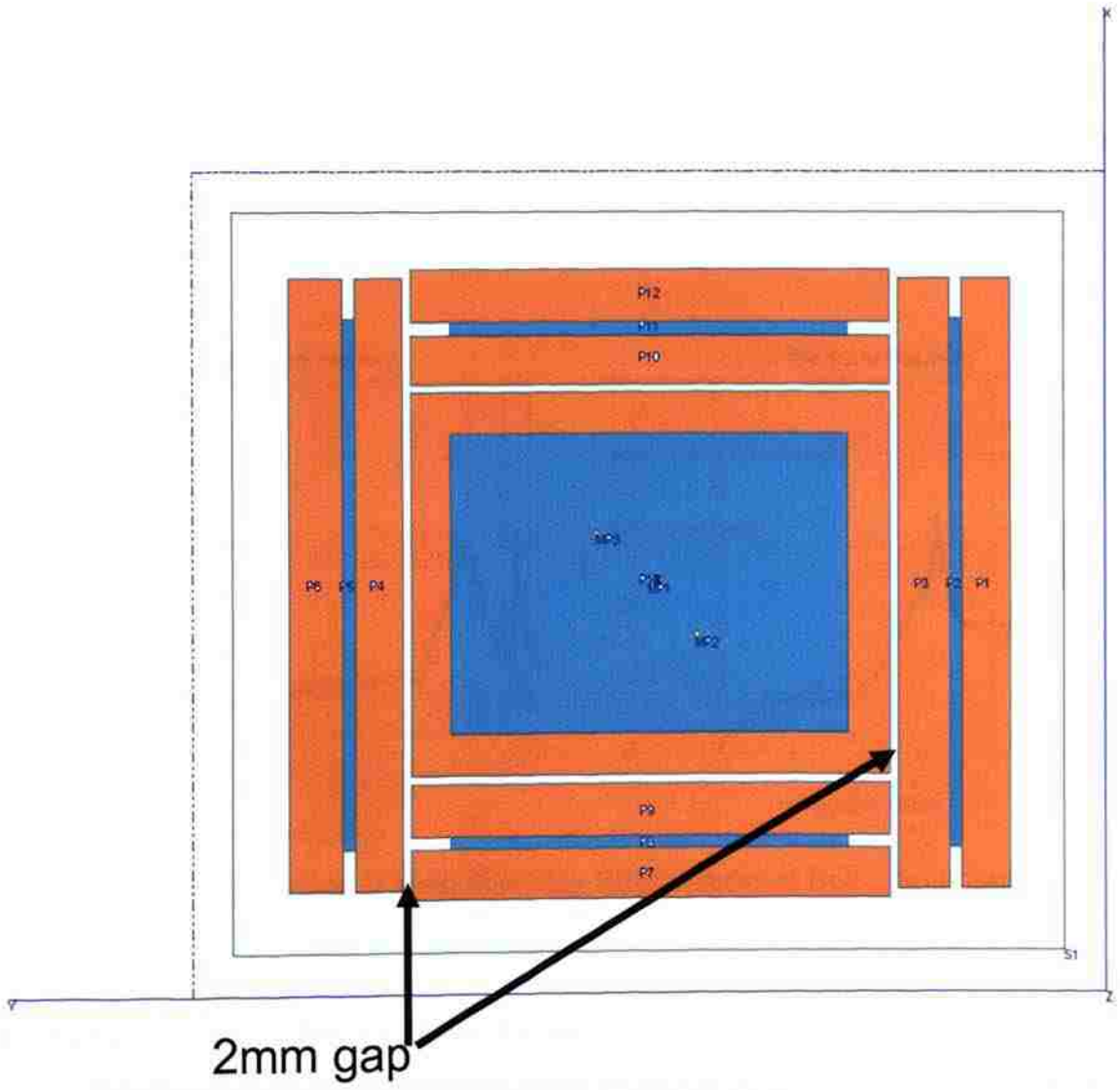

Figure 3.17. Debye Material Box - With Gap

were not compromised. Computational domain can be bigger than the one used in this simulation, it will yield more accurate results, but will take longer time to compute.

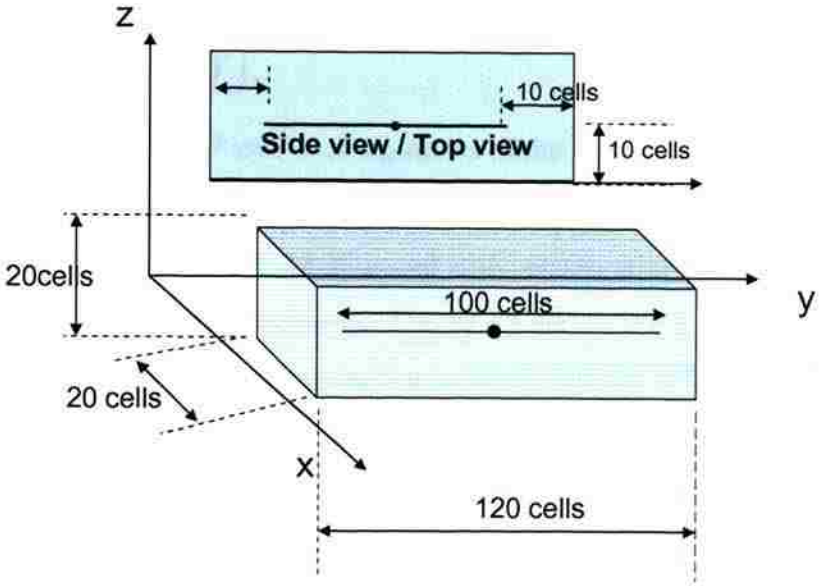

Figure 4.2. FDTD Model – No Ground

Table 4.1. FDTD Model Details – No Ground

Computational Domain	20 x 120 x 20 cells
Cell Size	0.0025 m
Wire Radius	20% of cell size
Source	Voltage resist – 1v, 50 ohm
Monitor Points	Far field monitor points

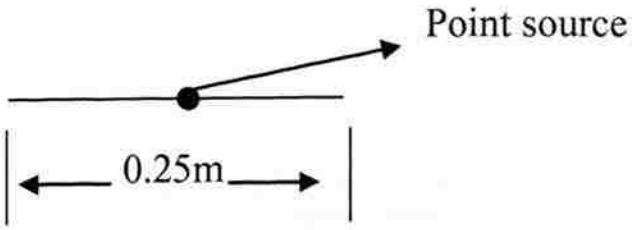

Figure 4.3. WireMoM Model – No Ground

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Observation points here were far field points. Neglecting the higher order terms c $1/r^n$ for the far filed, E field has only θ and ϕ components [12]:

$$E_\theta = -j\omega A_\theta ; \quad (4.1$$

$$E_\phi = -j\omega A_\phi ; \quad (4.2$$

$$\text{and } E_{total} = \sqrt{\left((E\theta)^2 + (E\phi)^2\right)}, \quad (4.3$$

where $A\theta$ and $A\phi$ are the θ and ϕ components of the vector magnetic potential and ar obtained from the simulations.

Figure 4.4 shows the E-field observed at the observation point which is 0.5 m above the transmitting antenna reference. Figure 4.5 shows the E-field observed at the observation point which is 1m above the transmitting antenna reference. Figure 4.6 shows E-field observed at the observation point which is 1.5m above the transmitting antenna reference. Figure 4.7 shows E-field observed at the observation point which is 2.0m above the transmitting antenna reference. Figure 4.8 shows E-field observed at the observation point which is 2.5m above the transmitting antenna reference. Figure 4.9 shows E-field observed at the observation point which is 3m above the transmitting antenna reference. Figure 4.10 shows E-field observed at the observation point which is 3.5m above the transmitting antenna reference.

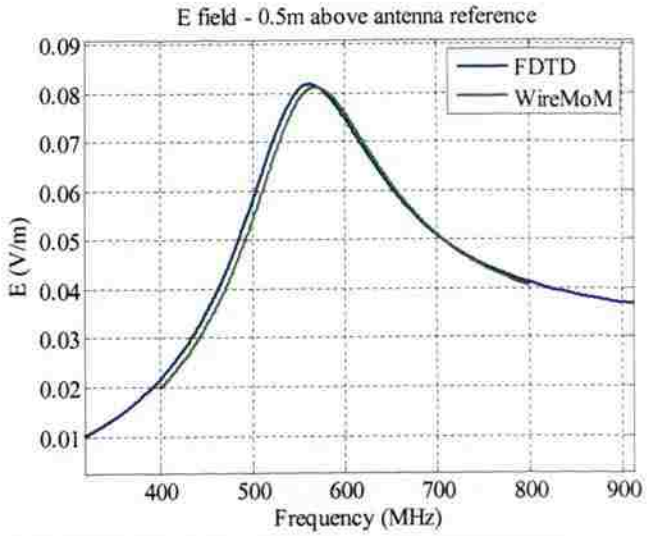

Figure 4.4. E-Field -0.5m Above Antenna Reference – No Ground

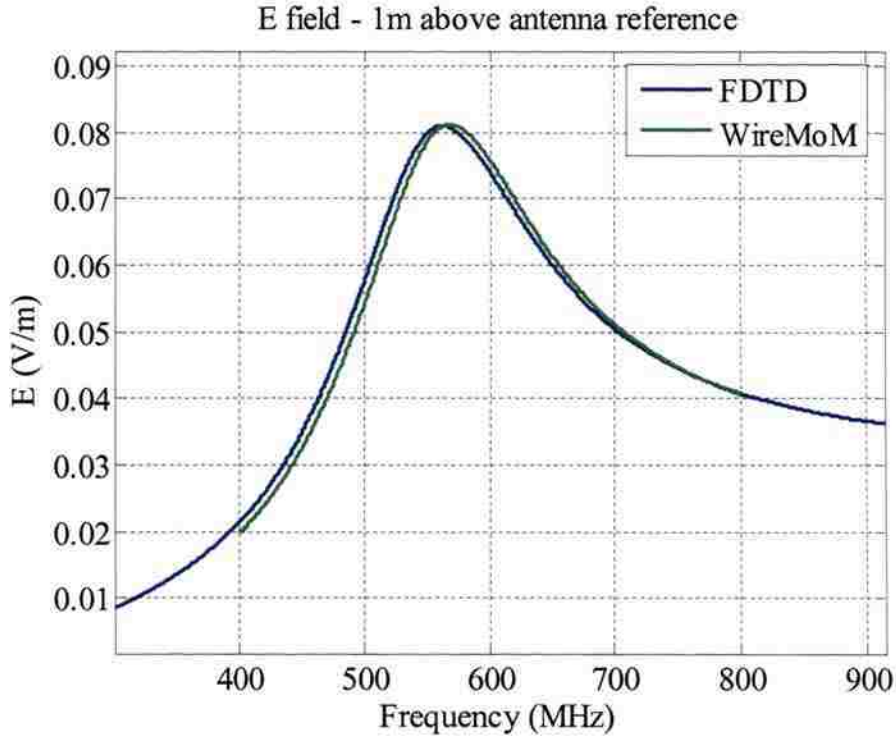

Figure 4.5. E-Field -1m Above Antenna Reference – No Ground

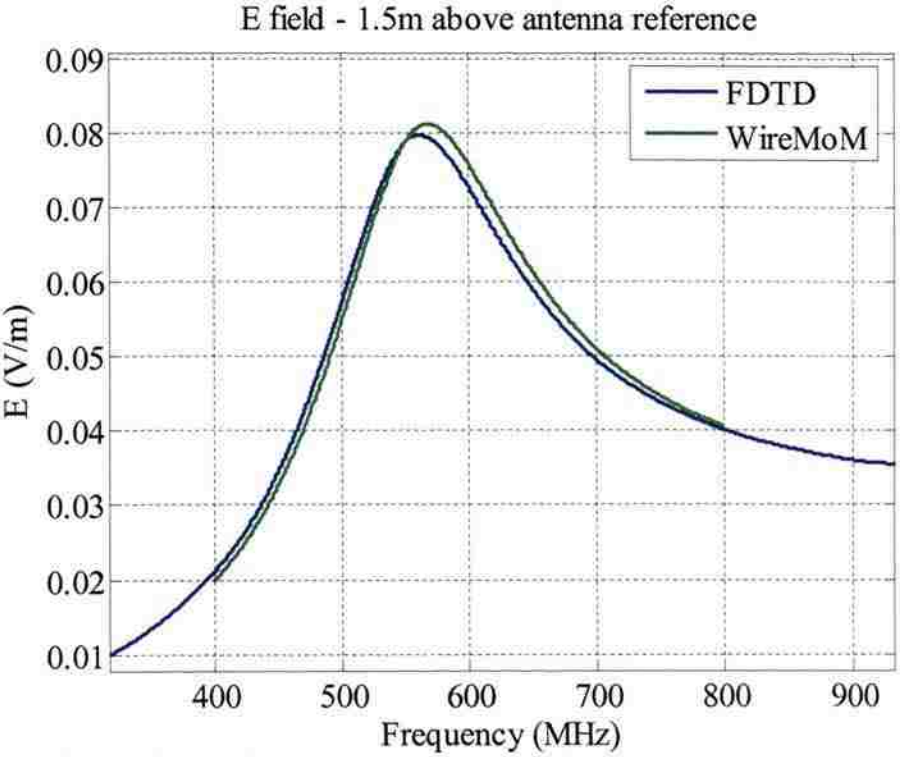

Figure 4.6. E-Field -1.5m Above Antenna Reference – No Ground

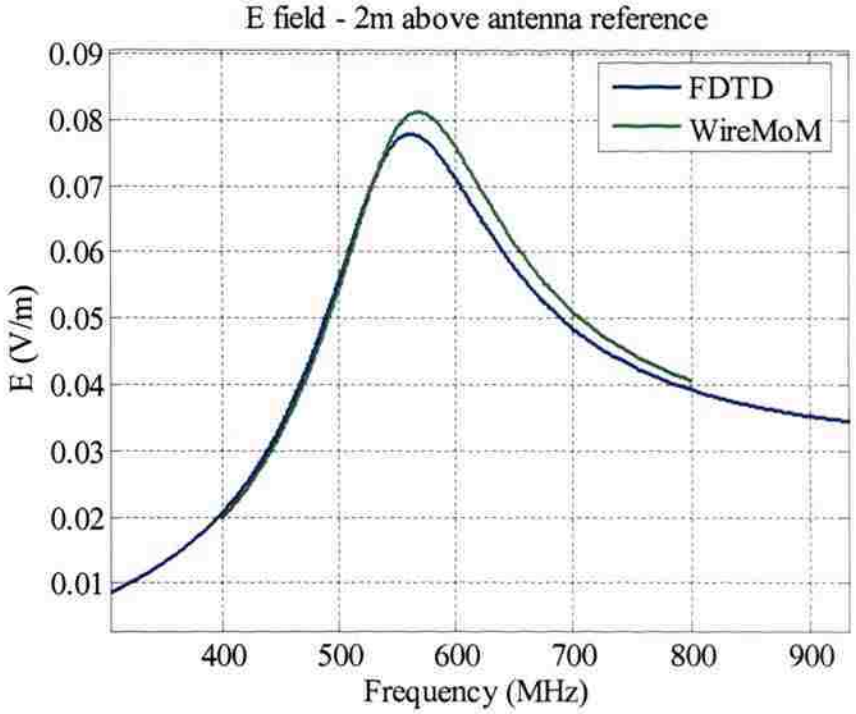

Figure 4.7. E-Field -2m Above Antenna Reference – No Ground

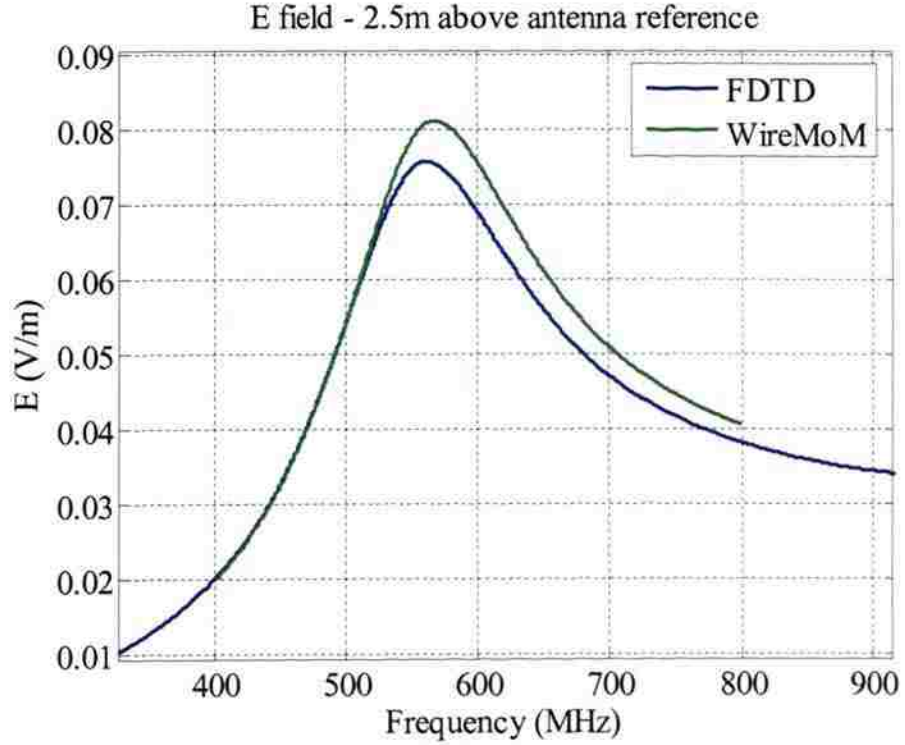

Figure 4.8. E-Field -2.5m Above Antenna Reference – No Ground

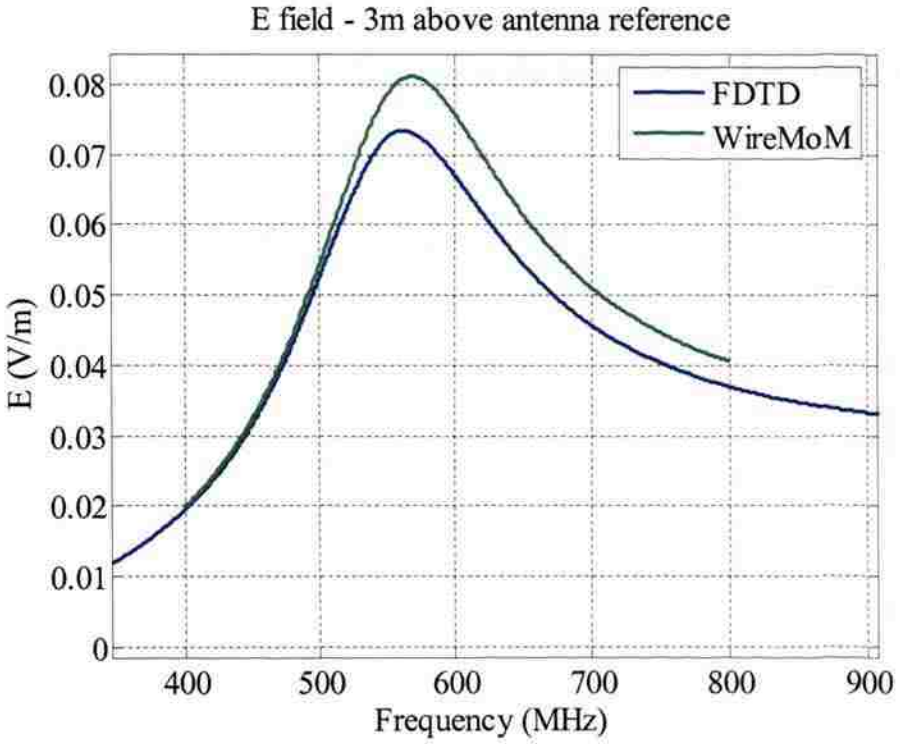

Figure 4.9. E-Field -3m Above Antenna Reference – No Ground

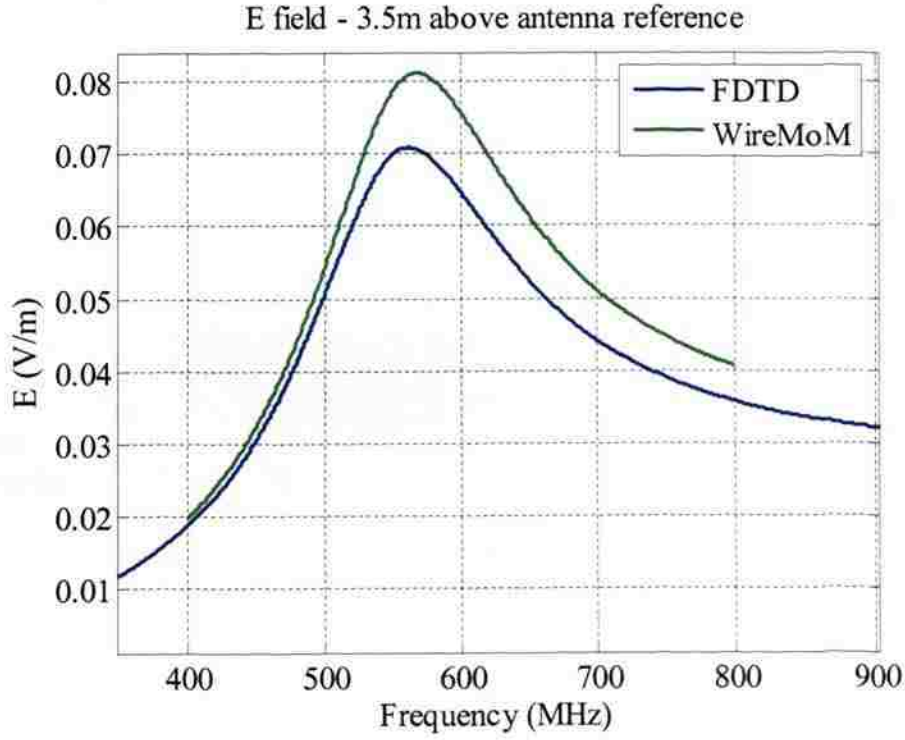

Figure 4.10. E-Field -3.5m Above Antenna Reference – No Ground

The above figures show that the agreement between FDTD and WireMoM is agreeable over a frequency range. However, as the height of the observation point increases, the error also increases. The reason for this disagreement is unknown and requires further investigation.

4.2.2. With Infinite Ground Plane. The geometry was modeled in the EZ-FDT with a PEC plane touching the computational domain. The transmitting antenna was placed at the center of the ground plane, so that the plane was touching the boundary to simulate the effect of an infinite ground plane. Far-field monitor points were used to calculate the fields at 6 m away from the transmitting antenna.

Figure 4.11 and Figure 4.12 describe this geometry. Table 4.2 shows the FDTD model specifications. The WireMoM model was similar to that specified in Figure 4.3 but with an infinite ground plane. Simulations with both software tools were compared for different observation point heights.

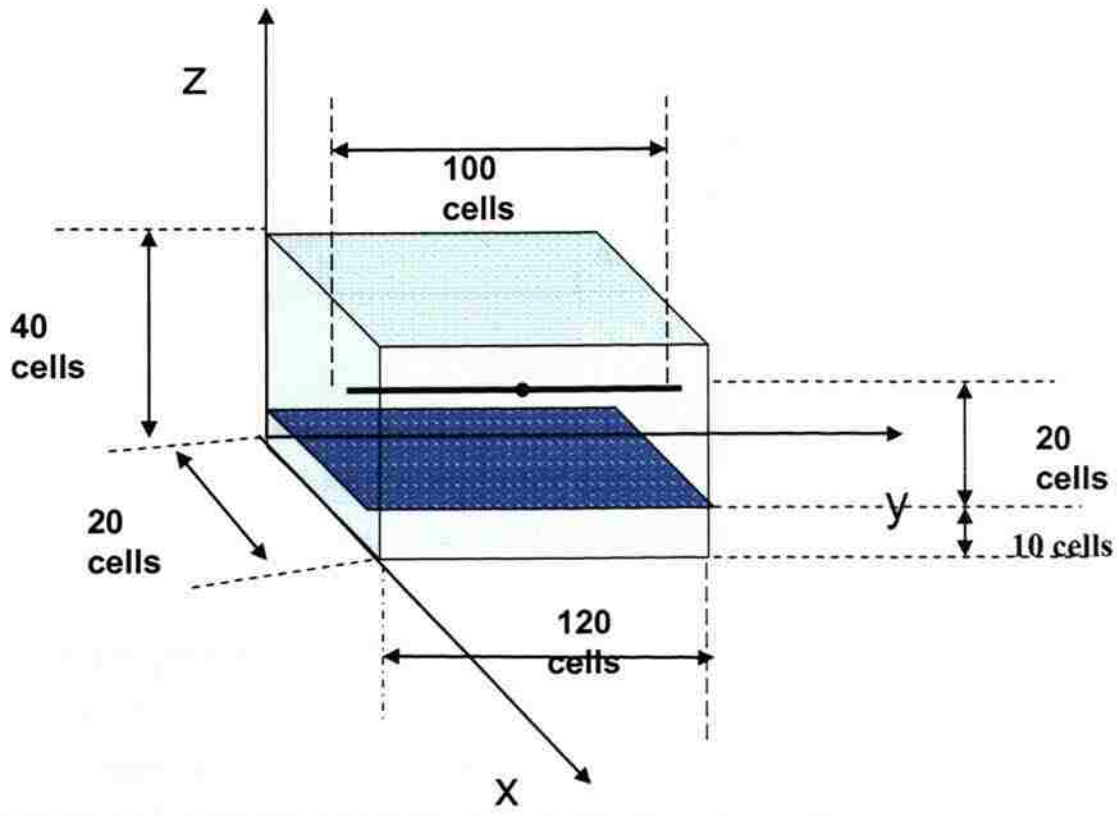

Figure 4.11. FDTD Model – Infinite Ground

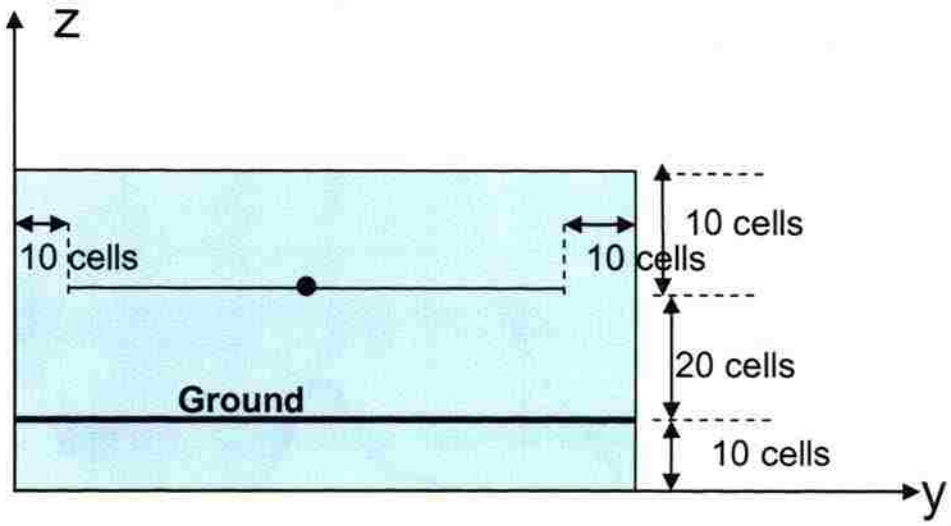

Figure 4.12. FDTD Model Side View – Infinite Ground

Table 4.2. FDTD Model Specifications – Infinite Ground

Computational Domain	20 x 120 x 20 cells
Cell Size	0.0025 m
Wire Radius	20% of cell size
Source	Voltage resist – 1v, 50 ohm
Monitor Points	Far field monitor points
PEC Plate	At x= 0 cell, y = 0 cell and z = 10 cells

Figure 4.13 show the E-field observed at the observation point which is 1m abov the ground plane. Figure 4.14 shows E-field observed at the observation point which is 1.5m above the ground plane. Figure 4.15 shows E-field observed at the observation point which is 2m above the ground plane. Figure 4.16 shows E-field observed at the observation point which is 2.5m above the ground plane. Figure 4.17 shows E-field observed at the observation point which is 3m above the ground plane. Figure 4.18show E-field observed at the observation point which is 3.5m above the ground plane. Figure 4.19 shows E-field observed at the observation point which is 4m above the ground plane.

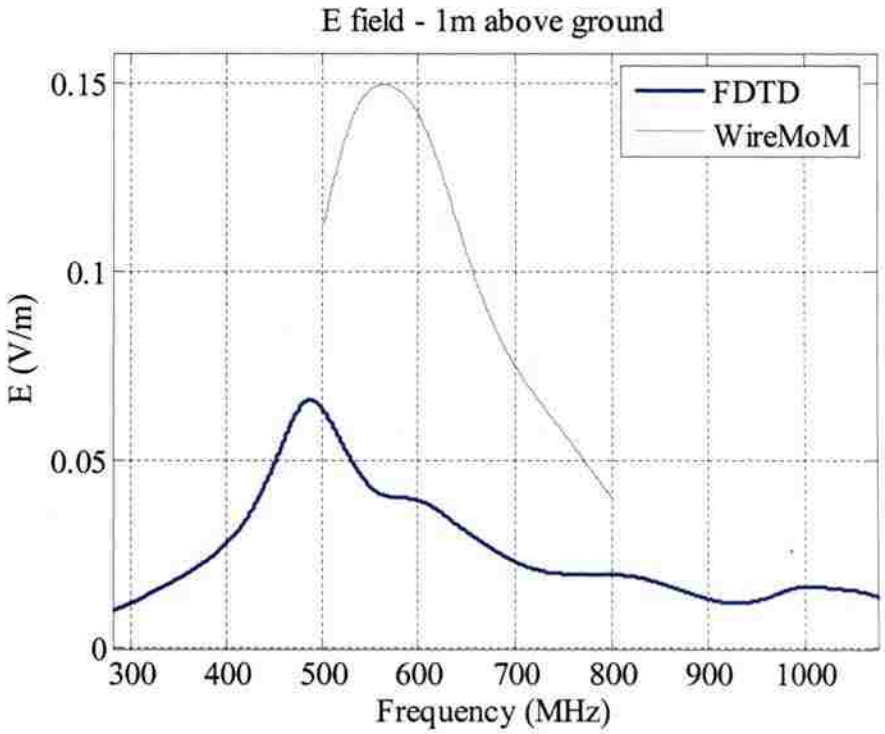

Figure 4.13. E-Field -1m Above Antenna Reference – Infinite Ground

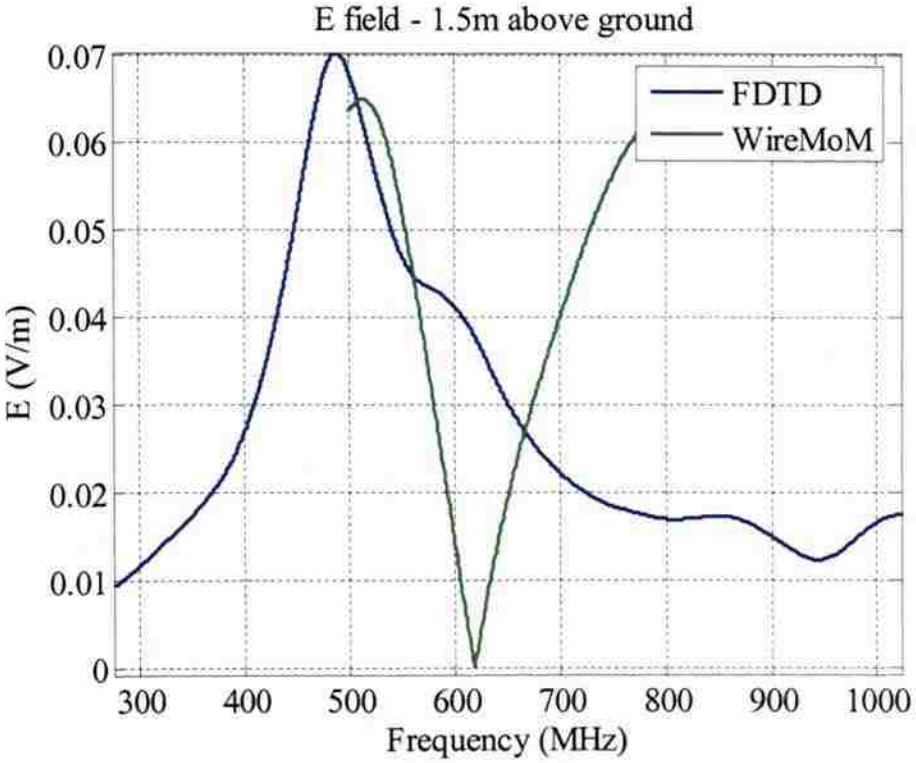

Figure 4.14. E-Field -1.5m Above Antenna Reference – Infinite Ground

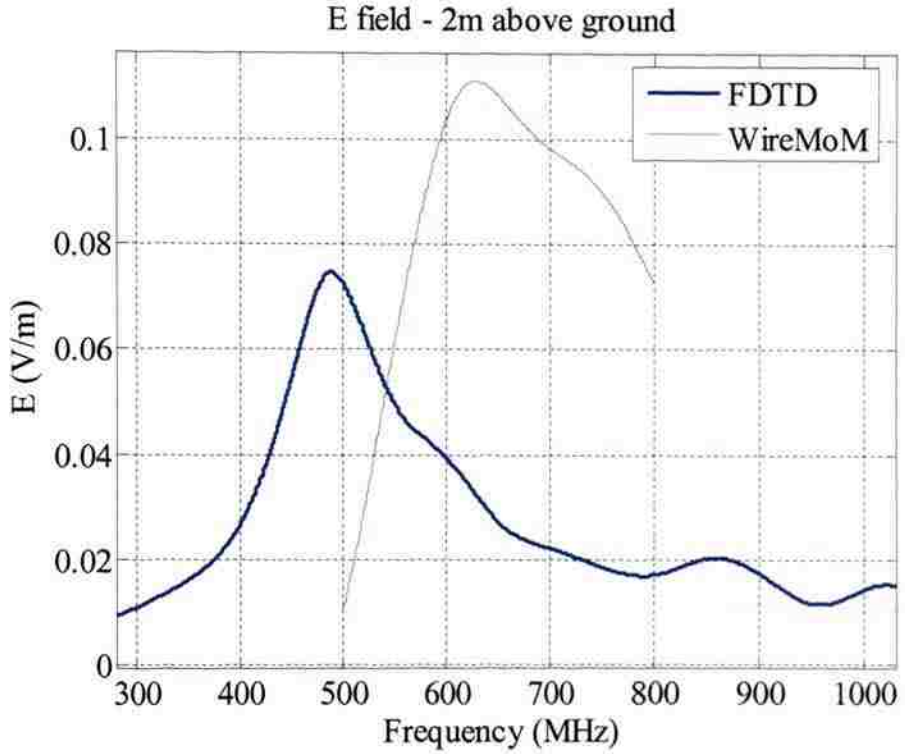

Figure 4.15. E-Field -2m Above Antenna Reference – Infinite Ground

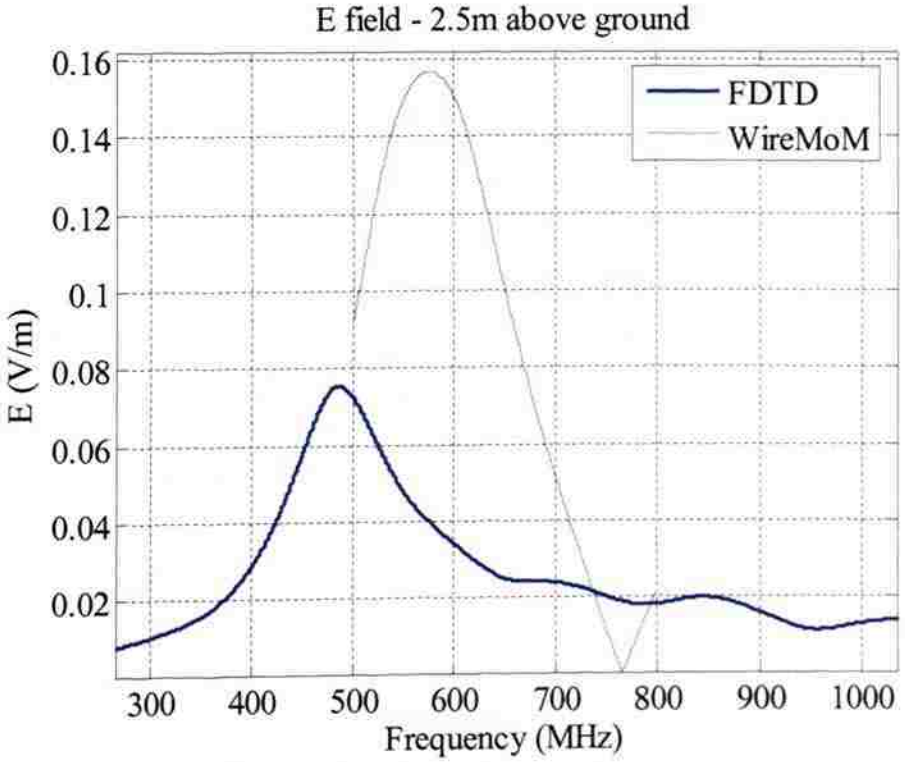

Figure 4.16. E-Field -2.5m Above Antenna Reference – Infinite Ground

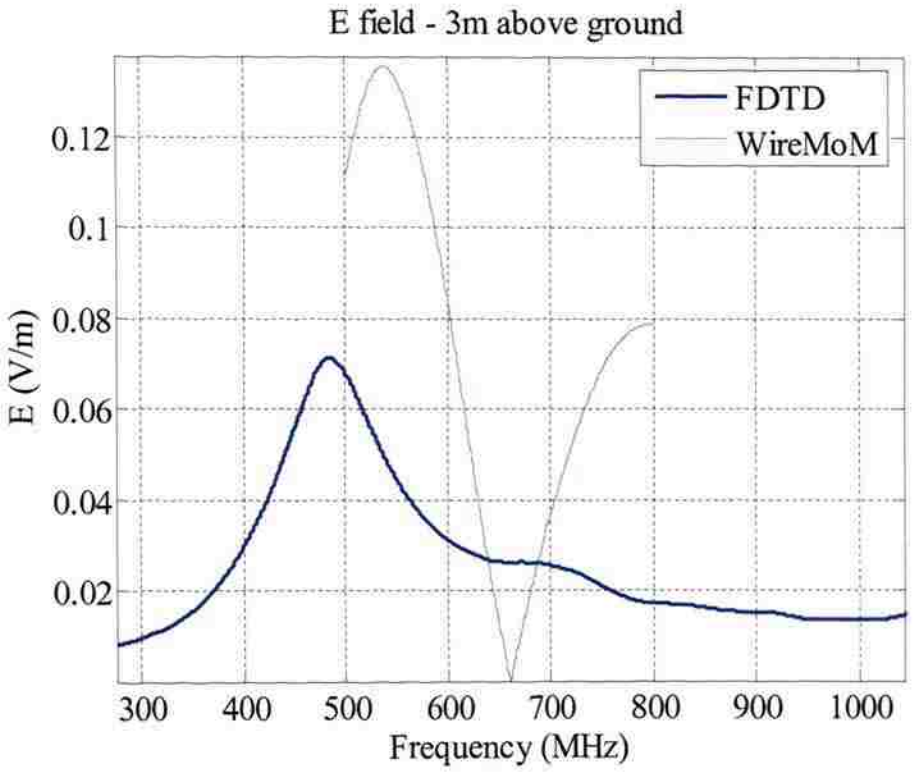

Figure 4.17. E-Field -3m Above Antenna Reference – Infinite Ground

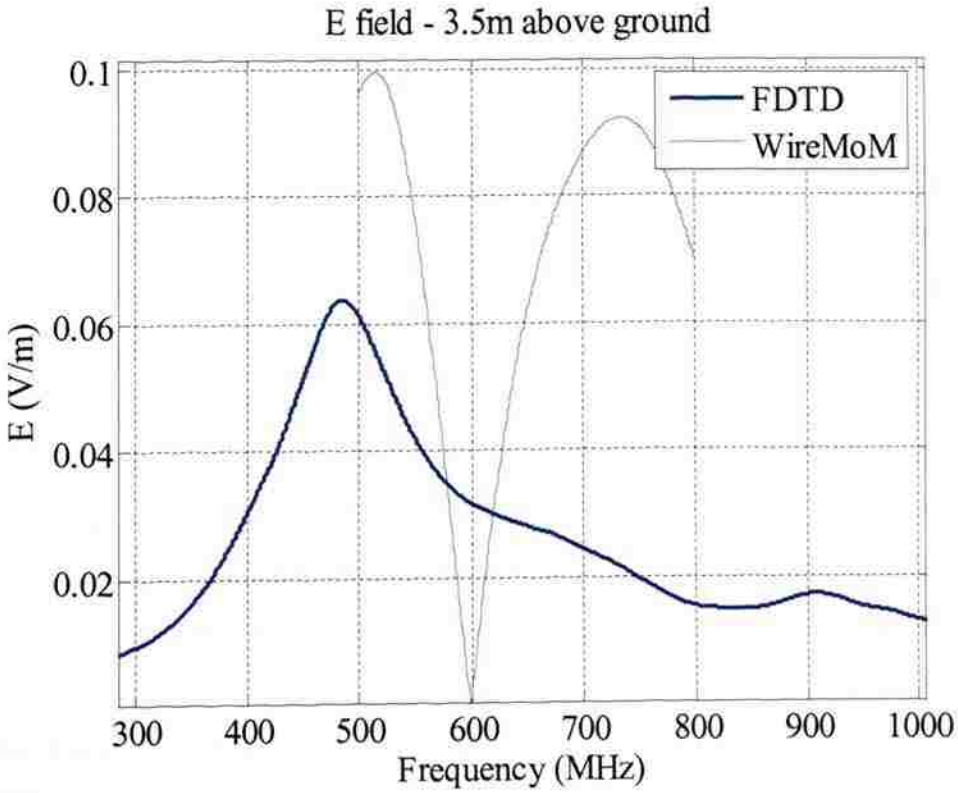

Figure 4.18. E-Field -3.5m Above Antenna Reference – Infinite Ground

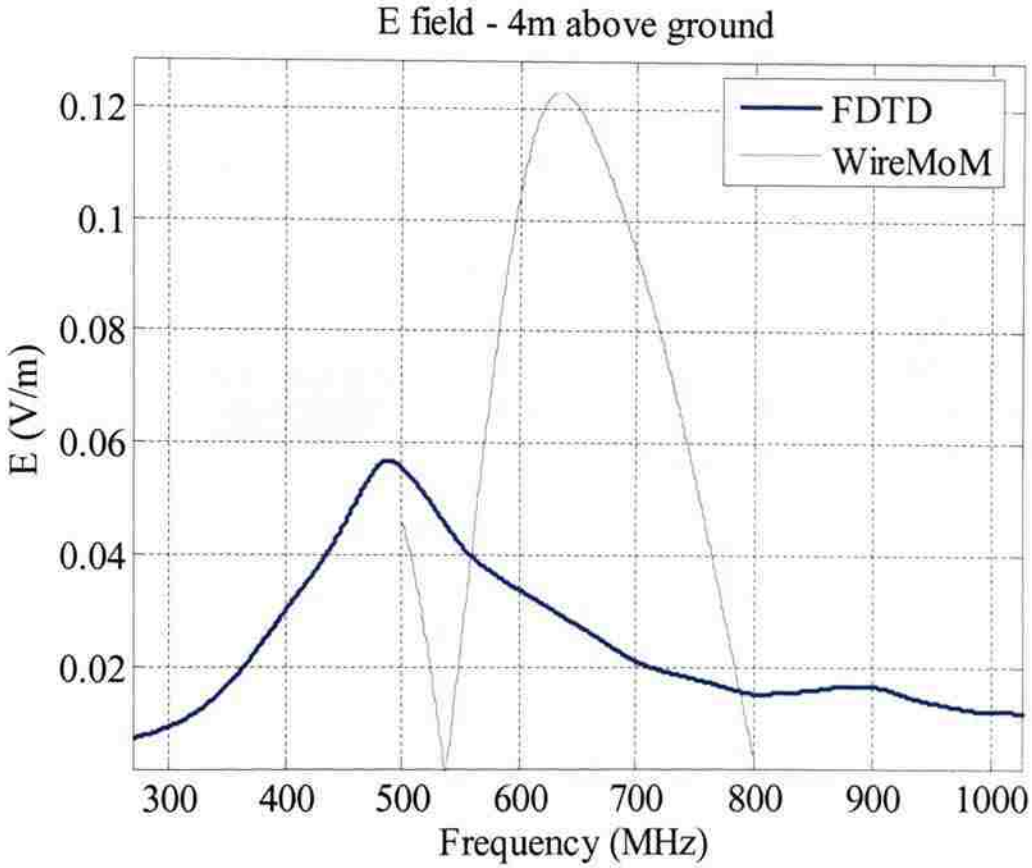

Figure 4.19. E-Field -4m Above Antenna Reference – Infinite Ground

The above figures illustrate that there is no match between the E Field simulated by FDTD and WireMoM. The reason for this mismatch has not been known yet. It could be due to the way this software considers the infinite ground settings. Moreover, there is a shift on transmitting antenna, between the current on the wire simulated with FDTD and the one simulated with WireMoM, which can also be the reason for the difference in E-field at the distant points. This shift increases with the increase of the transmitting antenna height with respect to the ground plane. This problem needs more investigation.

4.2.3. Finite Ground - Perfectly Conducting. The geometry was modeled in the EZ –FDTD and WireMoM by placing a finite PEC plane at z=0. The transmitting antenna was placed at x= 0m, and fields were measured using a far-field monitor placed at x=6m. Figure 4.20 and Table 4.3 describe the model and specifications, used to model in FDTD.

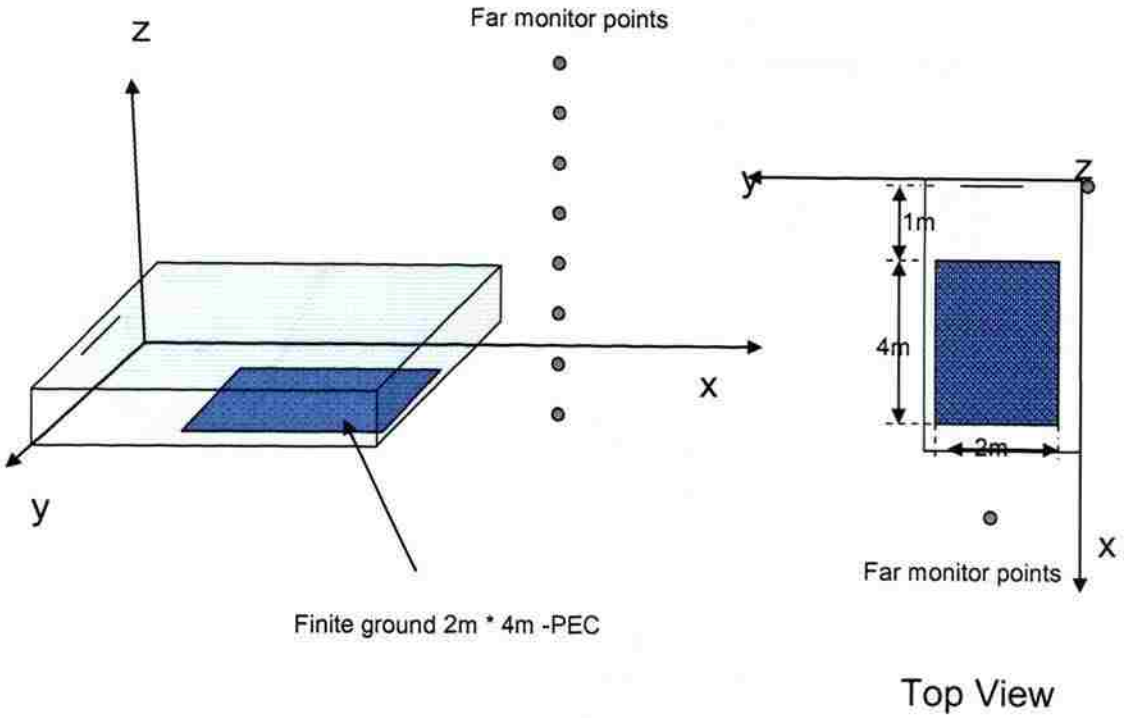

Figure 4.20. FDTD Model - Finite Ground

Table 4.3. FDTD Model Specifications – Finite Ground

Computational Domain	20 x 820 x 40 cells
Cell Size	0.05m x 0.0025 m x 0.05m
Wire Radius	20% of cell size
Source	Voltage resist – 1v, 50 ohm
Monitor Points	Far field monitor points

Simulations with both types of software were run and then compared for different observation point heights. Figure 4.21 to Figure 4.26 show that the E-field for both programs followed the shape, but did not quite agree. The reason for this mismatch is unknown, and requires further investigation.

The other ground cases are not simulated because it is impossible to simulate them using the WireMoM tool, although they can be simulated using the EZ-FDTD.

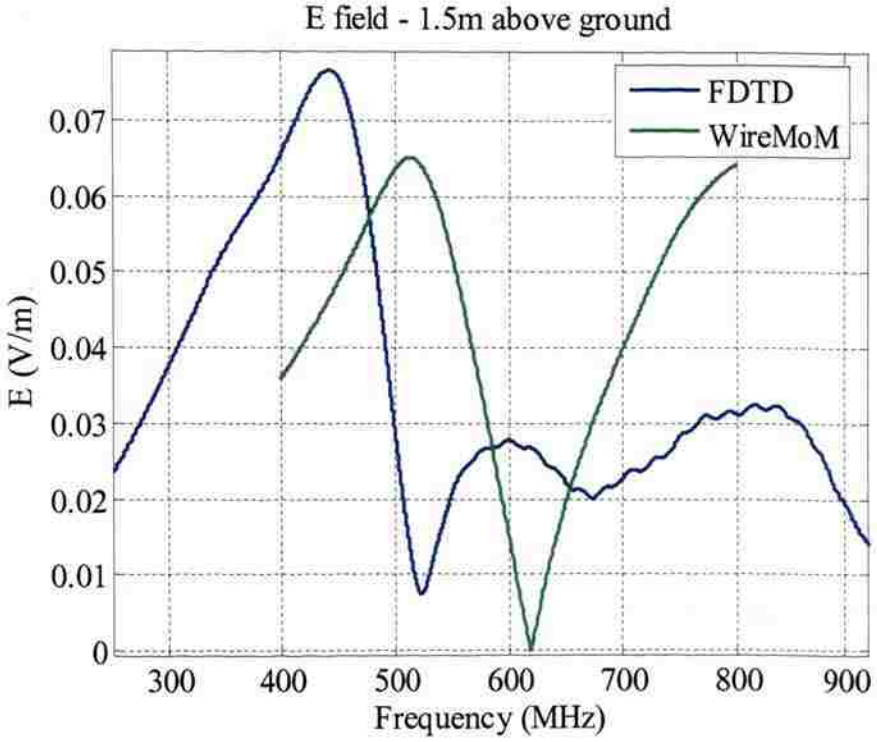

Figure 4.21. E-Field -1.5m Above Antenna Reference – Finite Ground

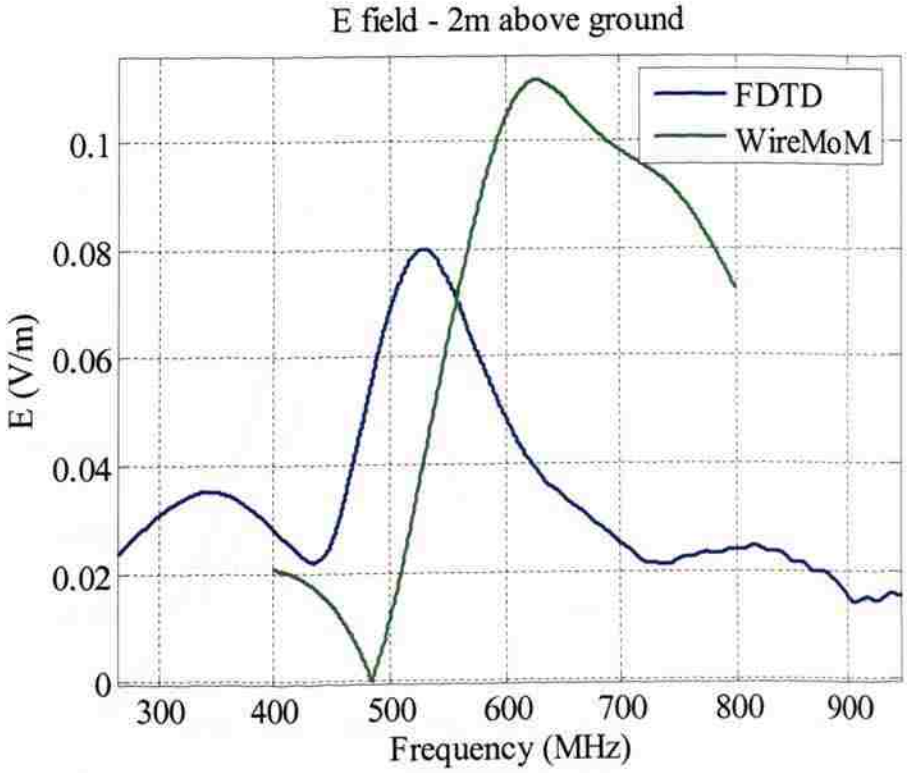

Figure 4.22. E-Field -2m Above Antenna Reference – Finite Ground

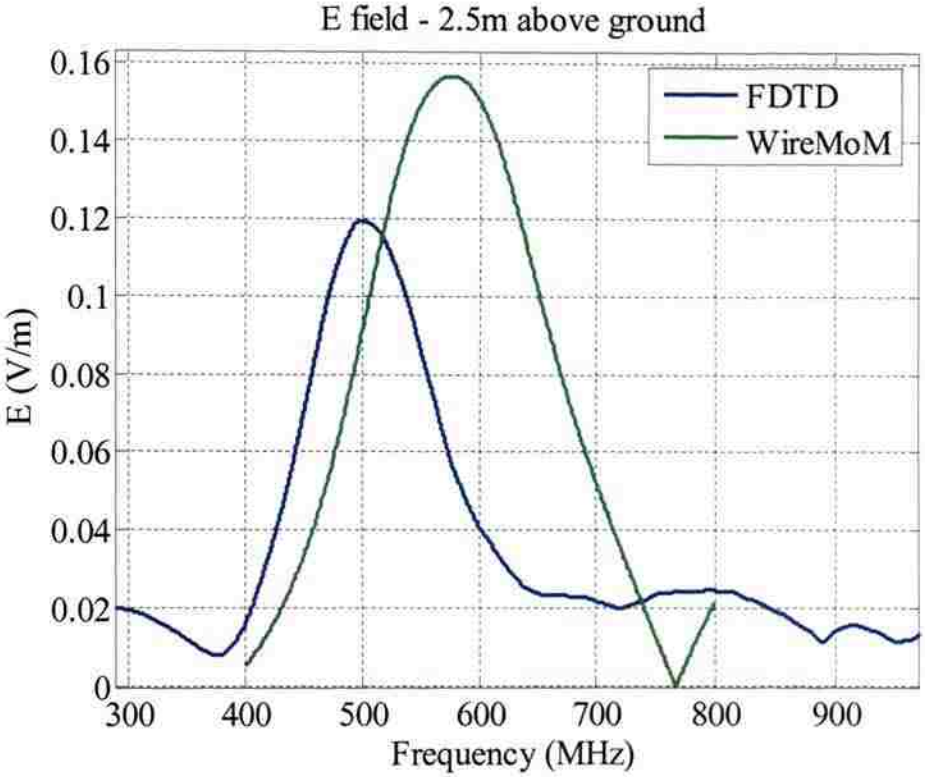

Figure 4.23. E-Field -2.5m Above Antenna Reference – Finite Ground

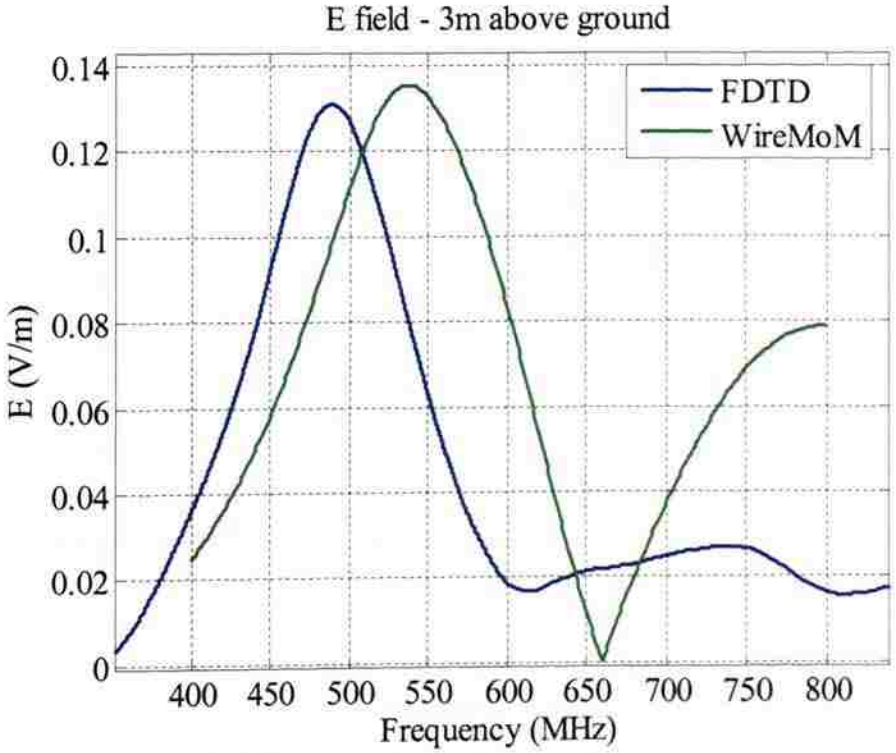

Figure 4.24. E-Field -3m Above Antenna Reference – Finite Ground

80

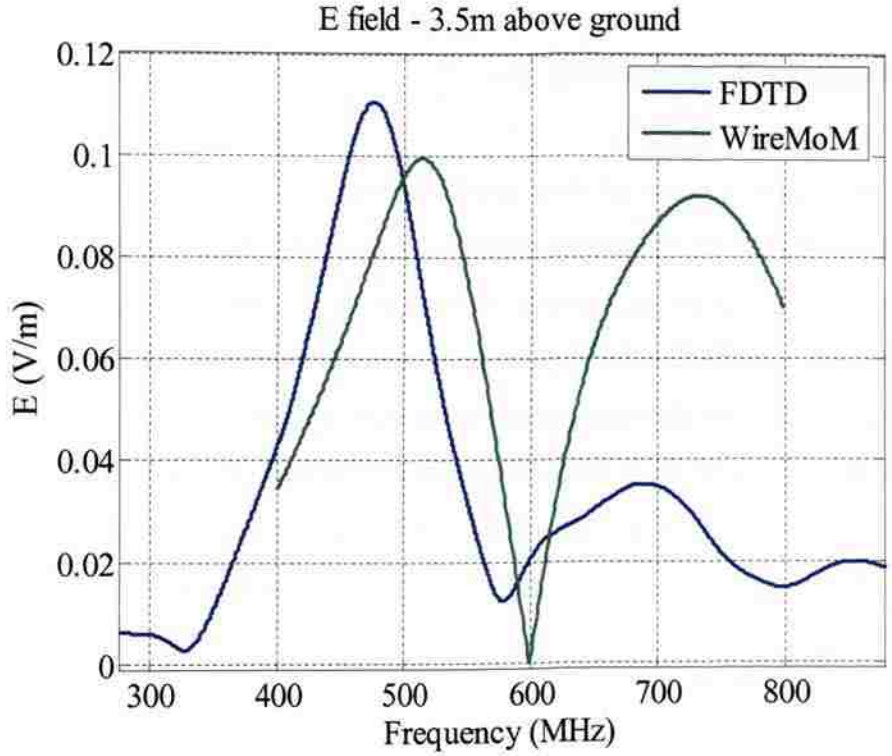

Figure 4.25. E-Field -3.5m Above Antenna Reference – Finite Ground

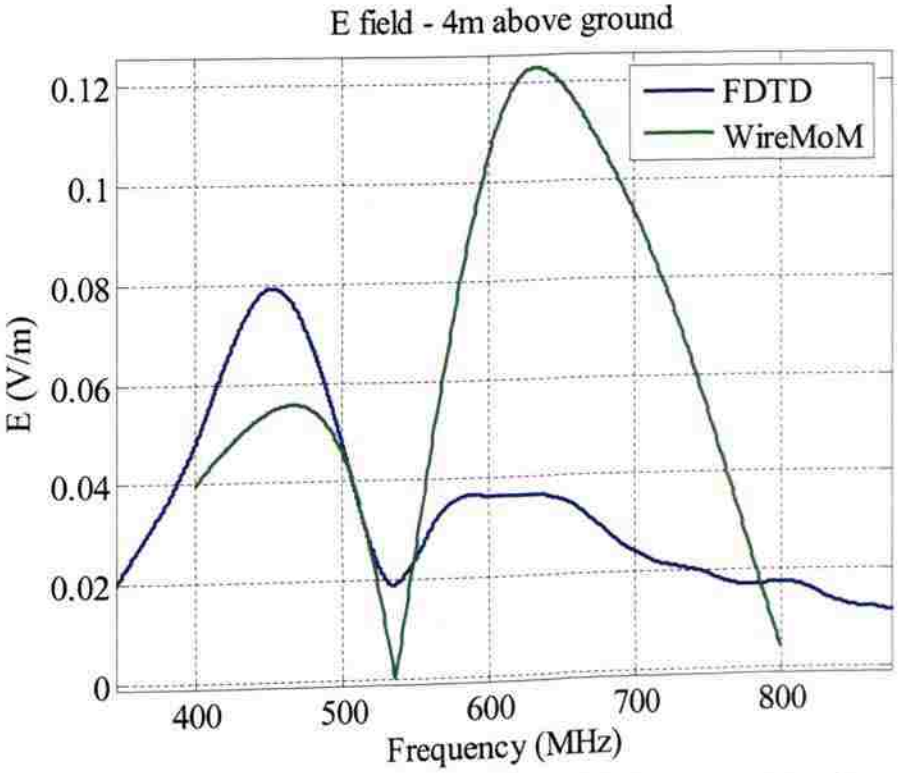

Figure 4.26. E-Field -4m Above Antenna Reference – Finite Ground