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"Green" on-chip inductors in three-dimensional integrated circuits

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“GREEN” ON-CHIP INDUCTORS IN THREE-DIMENSIONAL INTEGRATED CIRCUITS

by

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ABSTRACT

This thesis focuses on the technique for the improvement of quality factor and inductance of the TSV inductors and then on the utilization of TSV inductors in various on-chip applications such as DC-DC converter and resonant clocking. Through-silicon-vias (TSVs) are the enabling technique for three-dimensional integrated circuits (3D ICs). However, their large area significantly reduces the benefits that can be obtained by 3D ICs. On the other hand, a major limiting factor for the implementation of many on-chip circuits such as DC-DC converters and resonant clocking is the large area overhead induced by spiral inductors. Several works have been proposed in the literature to make inductors out of idle TSVs. In this thesis, the technique to improve the quality factor and inductance is proposed and then discusses about two applications utilizing TSV inductors i.e., inductive DC-DC converters and LC resonant clocking. The TSV inductor performs inferior to spiral inductors due to its increases losses. Hence to improve the performance of the TSV inductor, the losses should be reduced. Inductive DC-DC converters become prominent for on-chip voltage conversion because of their high efficiency compared with other types of converters (e.g. linear and capacitive converters). On the other hand, to reduce on-chip power, LC resonant clocking has become an attractive option due to its same amplitude and phases compared to other resonant clocking methods such as standing wave and rotary wave. A major challenge for both applications is associated with the required inductor area. In this thesis, the effectiveness of such TSV inductors in addressing both challenges are demonstrated.

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

PAPER II

PAPER III

LIST OF TABLES

1. INTRODUCTION

Three-dimensional integrated circuits (3D ICs) are generally considered to be the most promising alternative that offers a path beyond Moore's Law. Instead of making transistors smaller, it makes use of the vertical dimension for higher integration density, shorter wire length, smaller footprint, higher speed and lower power consumption [1].

Through-silicon-vias (TSVs) are a critical enabling technique for 3D ICs, which form vertical signal, power and thermal paths. The TSVs are bulky and are typically 5-10x larger than the 32 nm standard cells [2]. Moreover, many thermal TSVs need to be inserted to reduce the chip temperature. To guarantee high yield rate, foundries typically impose a minimum TSV density rule. For example, Tezzaron requires that at least one TSV must exist in every 250 μm x 250 μm area [1]. To satisfy this rule, lots of dummy TSVs need to be inserted. The thermal TSV and the dummy TSV are both idle yet further increase the area overhead.

On the other hand, the large area overhead induced by the conventional spiral inductor is a limiting factor to implement many important circuit constructs on chip, including inductive DC-DC converters and LC resonant clocks. For example, [3] reported an inductor which occupies 78,400 μm2 routing area, equivalent to the area of 62K gates in 45 nm technology.

To alleviate both problems, there have been efforts in the literature to make use of these idle TSVs for TSV inductors [4-8]. However, these inductors suffer from losses at high frequencies. In this thesis, a method of micro-channel shielding is proposed to reduce the losses and then two applications utilizing TSV inductors i.e., inductive DC-DC converters and LC resonant clocking are used as vehicles to demostrate the effectiveness. Inductive DC-DC converters become prominent for on-chip voltage conversion because of their high efficiency compared with other types of converters (e.g. linear and capacitive converters). On the other hand, to reduce on-chip power, LC resonant clocking has become an attracting option due to its same amplitude and phases compared to other resonant clocking methods such as standing wave [9] and rotary wave

[10]. A major challenge for both applications is associated with the inductor area required.

In this thesis, the behavior of TSV inductors is systematically studied and the impact of the parameters on its quality factor and inductance. The micro-channel shielding technique to increase the quality factor and inductors is then presented. Two applications i.e., inductive DC-DC Converter and Resonant clocking are studied to observe the effectiveness of TSV inductors.

The remainder of the thesis is organized as follows: Paper I discusses about on the efficacy of through-silicon-via inductors. Paper II discuss about the implementation of DC-DC converters and paper III is about resonant clocking using TSV inductors respectively. Concluding remarks are given in Section 2.

I. ON THE EFFICACY OF THROUGH-SILICON-VIA INDUCTORS

Abstract

Through-silicon-vias (TSVs) can potentially be used to implement inductors in three-dimensional (3D) integrated systems for minimal footprint and large inductance. However, different from conventional 2D spiral inductors, TSV inductors are fully buried in the lossy substrate, thus suffering from low quality factors. In this thesis, how various process and design parameters affect their performance is examined. A few interesting phenomena that are unique to TSV inductors are observed. A novel shield mechanism utilizing the micro-channel, a technique conventionally used for heat removal, to reduce the substrate loss is then proposed. The technique increases the quality factor and the inductance of the TSV inductor by up to 21x and 17x respectively.

1. TSV INDUCTORS

Due to the limited space on an integrated circuit chip and highly competitive chip market, on-chip inductors must fit within a limited space and be inexpensive to fabricate. In that regard, it is desirable for an on-chip inductor to have a high inductance L per unit area. The spiral structure in a square shape can typically achieve lower than 100 nH/mm^2 density [24].

Another important inductor metric is the quality factor Q, which is the ratio of its inductive reactance to its resistance and is used to measure energy efficiency [24]. To achieve high quality factor, on-chip inductors are typically implemented using thick metal on top metal layers in RF process. To reduce the EM coupling between the inductor and any metal wires beneath it, Patterned Ground Shield (PGS) technique is typically used, further occupying valuable routing resources.

The general structure of existing toroidal TSV inductors [4-8] is shown in Figure 1.1, which is composed of front/back metals and TSVs in a toroidal structure for face-to-back bonding. The most attractive advantage of such a TSV inductor is its minimal footprint on the silicon surface. In addition, no patterned ground shield is necessary as the majority of the magnetic flux run in parallel with metal wires (in the horizontal plane).

Several works in literature exist on TSV inductors. [4,5] discussed the implementation of toroidal and vertical spiral TSV inductors. [6,7] proposed a micro-channel based shielding mechanism to enhance the quality factor of TSV inductors for RF applications. On the other hand, [8] demonstrated that TSV inductors can replace conventional spiral inductors for AC to DC converters at extremely low frequencies (50 Hz).

However, all existing works simply conduct case studies on a few selected geometries, and no systematic conclusions have been drawn on how various parameters would affect the performance of the TSV inductor. It is not clear yet whether the new TSV inductor structure will result in different behaviors with respect to these parameters. In addition, there are a few parameters that are unique to TSV inductors such as the TSV liner thickness.

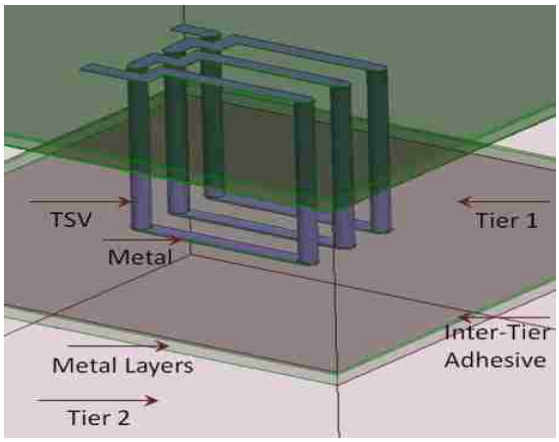


Figure 1.1 Illustration of a toroidal TSV Inductor

Moreover, according to the literature, the quality factor of the TSV inductor is significantly less than its 2D spiral counterpart, mainly due to the loss from the substrate. Unlike the 2D spiral inductor, the entire TSV inductors are buried in the silicon substrate, which is lossy at high frequencies. As a result, [4] suggested that for 50 um substrate thickness and below, TSV inductor should be used when area is the only concern, which means it is of little practical value. *One question that rises here is: Is there any way that the substrate losses can be reduced for TSV inductors, so that their quality factor can be at par or even better compared with spiral inductors for practical use?*

2. IMPACT OF PROCESS AND DESIGN PARAMETERS

In this section, how various process and design parameters affect the inductance, the quality factor, as well as the self-resonance frequency (SRF) of the TSV inductor is studied. All the simulations in this thesis are done using commercial full-wave simulator with mixed order basis function. Machine used is a 64-bit Dell T7500 Windows server with 2.4 GHz duo-core Xeon CPU and 96 GB memory. For clarity purposes, the parameters of study are outlined in Table 2.1. The practical range of interest for each parameter is also listed.

Table 2.1 List of parameters, the respective default unit and ranges of interest

Type	Notation	Meaning	Range
Process	H (μm)	Substrate height	30-120
	σ (S/m)	Substrate conductivity	0-10,000
	D(μm)	TSV diameter	2-15
	d(μm)	Liner thickness	0.2-0.7
	h(μm)	Metal height	0.2-3
Design	N	Number of turns	1-6
	T	Number of tiers	2-4
	P(μm)	Loop pitch	13-23
	W(μm)	Width of metal strip	3-12
	F(GHz)	Operating frequency	0.15, 1 , 5, 10

There are four things worthwhile to note here: 1) While existing works only use two tiers (T=2) to implement the inductor, in this thesis the study to designs is of up to four tiers (according to [28], 3D ICs of up to five tiers have already been fabricated).

Since the bottom tier does not need any TSV, the actual inductor is formed in the top T-1 tiers. 2) To achieve maximum quality factor, the cross-sectional area should be square. In other words, once the number of tiers T is fixed, the TSV pitch should be (T-1)H, where H is the height of a single tier. 3) The substrate height and the TSV diameter are chosen such that the TSV aspect ratio (AR) is between 5:1 and 20:1, in accordance with ITRS. 4) The 150 MHz operating frequency represents applications such as on-chip voltage regulator applications, while 1/5/10 GHz represents resonant clocking or RF applications.

To study the impact of various parameters, the control variable method is used to change one parameter at a time. The nominal settings are illustrated in Figure 2.1:

Process parameters: H = 60 μm, σ = 10 S/m, D = 6 μm, d = 0.2 μm.

Design parameters: N = 1, T = 2, P = 18 μm (not shown), W = 6 μm.

In addition to these parameters of study, for each tier a normal process with 8 metal layers is assumed. The metal layers have a total thickness (including field dioxide) of 4 μm. The metal strips connecting TSVs are implemented using M1 (0.3 μm thick) and backside metal (0.8 μm thick). The corresponding inductance and quality factor vs. frequency plot for the above nominal settings are shown in Figure 2.2.

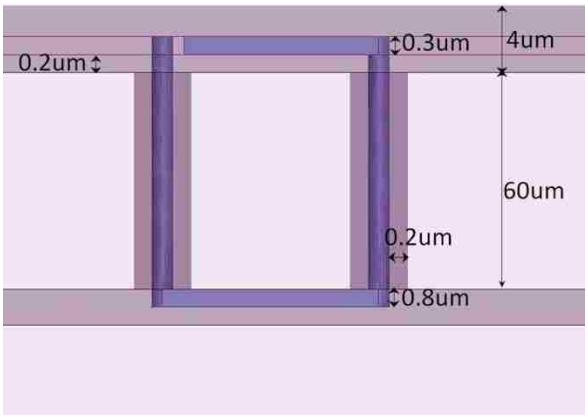


Figure 2.1 Nominal settings of TSV Inductor (not to scale)

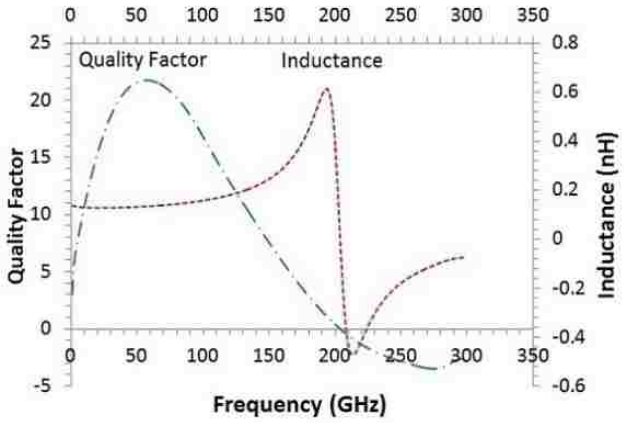


Figure 2.2 Q and L vs. frequency for the TSV inductor with nominal settings

2.1 SUBSTRATE HEIGHT (H)

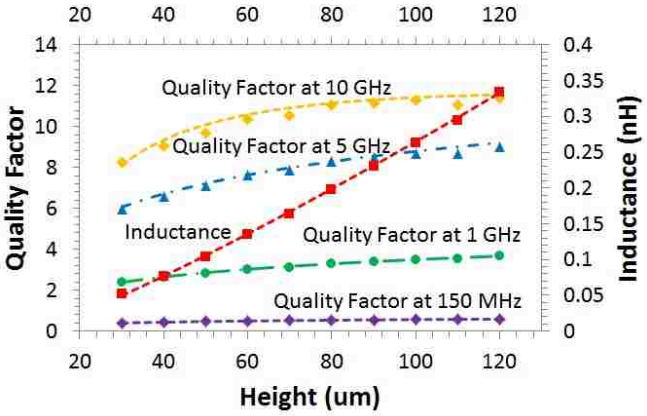


Figure 2.3 Q and L vs. substrate height H

The quality factor and the inductance for different substrate heights and operating frequencies are shown in Figure 2.3. Based on the analogy to the spiral inductors, the inductance should be proportional to Hln(H). This can be clearly verified by curve fitting. In terms of quality factor, it increases with H, but at different rates for different

frequencies. Finally, although not shown in the figure, self-resonant frequency decreases from over 250 GHz to 100 GHz when H increases from 30 μm to 120 μm.

Observation 1: For the range of interest, increasing substrate height increases both the inductance and the quality factor, but reduces the self-resonant frequency.

2.2 SUBSTRATE CONDUCTIVITY (σ)

The quality factor and the inductance for different substrate conductivities and operating frequencies are shown in Figure 2.4. From the figure, the inductance is not directly impacted by σ (L = 0.13 nH). On the other hand, when σ is low (corresponding to the lightly doped substrate) or when the frequency is low (150 MHz or 1 GHz), the quality factor almost remains constant, because in this region the quality factor loss is mainly due to the ohmic loss in the inductor. When both σ and the frequency are high, the quality factor decreases with σ, at higher rate for higher frequencies. This is due to the fact that in this region, the loss mainly occurs in the substrate. Finally, although not shown in the figure, self-resonant frequency decreases from over 200 GHz to 60 GHz when σ increases from 0 S/m to 10,000 S/m.

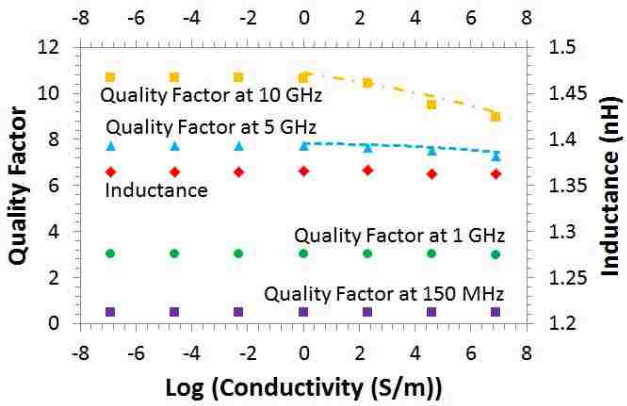


Figure 2.4 Q and L vs. substrate conductivity σ

Observation 2: For low substrate doping density ($\sigma < 10$ S/m) or low frequency (<1GHz), the ohmic loss of the inductor dominates. When the doping density is high and the frequency is high, the substrate loss dominates.

Observation 3: For the range of interest, increasing substrate conductivity does not change the inductance, and has little impact on the quality factor at low frequency or low substrate conductivity. It reduces the quality factor gradually at high frequency for high substrate conductivity. The self-resonance frequency drops with the increase of substrate conductivity.

2.3 TSV DIAMETER (D)

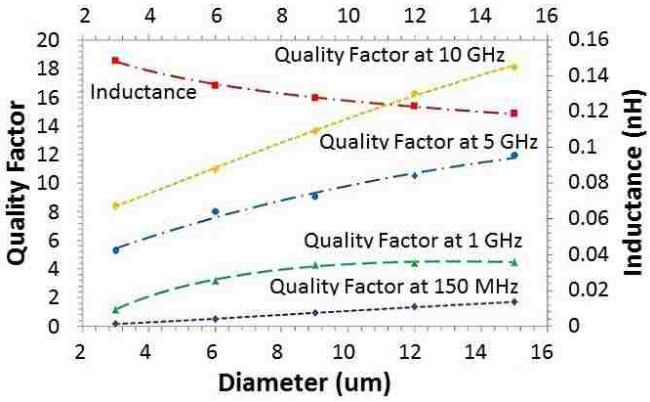


Figure 2.5 Q and L vs. diameter D

The quality factor and the inductance for different TSV diameters and operating frequencies are shown in Figure 2.5. Based on the analogy to the spiral inductors (metal width), the inductance should be proportional to ln(H/D). In terms of quality factor, the quality factor should increase with D as the resistance of the inductor becomes smaller. Apparently, at higher frequency, the quality factor is larger and the slope w.r.t. D is higher. The larger slope is due to the effect of further AC resistance reduction from

substrate coupling at higher frequencies. Finally, although not shown in the figure, self-resonant frequency is almost constant (~200 GHz) for the diameter range (3 µm -15 µm).

Observation 4: For the range of interest, increasing TSV diameter reduces the inductance, increases the quality factor, and does not change the self-resonant frequency significantly.

2.4 LINER THICKNESS (d)

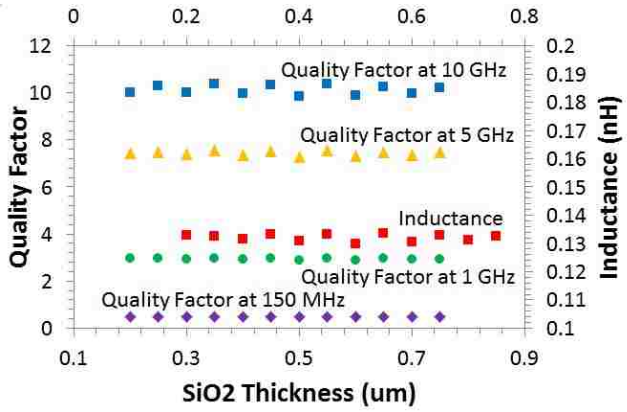


Figure 2.6 Q and L vs. linear thickness d

The quality factor and the inductance for different liner thickness and operating frequencies are shown in Figure 2.6. This parameter is unique to the TSV inductor and based on the plot, it can be seen that d has little impact on the inductance and the quality factor. It also has subtle impact on the self-resonant frequency.

Observation 5: For the range of interest, TSV liner thickness has subtle impact on the TSV inductor behavior.

2.5 METAL HEIGHT (h)

The quality factor and the inductance for different metal heights and operating frequencies are shown in Figure 2.7. The inductance decreases as h increases due to the increased capacitive coupling. In terms of quality factor, it increases with h, as the ohmic loss becomes smaller. The impact of h on Q also becomes more profound at higher frequency. Finally, the self-resonant frequency remains almost constant (~250 GHz).

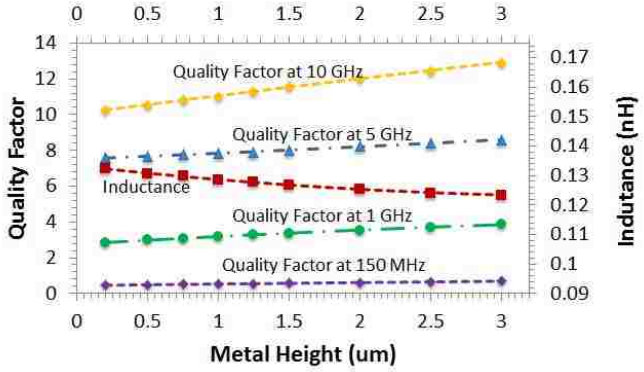


Figure 2.7 Q and L vs. Metal height h

Observation 6: For the range of interest, increasing the metal height h decreases the inductance, and has little impact on the quality factor at low frequency. It increases the quality factor at high frequency. The self-resonant frequency does not change with h significantly.

2.6 NUMBER OF TURNS (N)

The quality factor and the inductance for different number of turns and operating frequencies are shown in Figure 2.8. Based on the analogy to the 2D spiral inductors, inductance should be proportional to N_k. In terms of quality factor, a few interesting

phenomena can be observed. First, there exists a particular N_c that gives maximum quality factor. Second, such N_c decreases with the frequency. At 150 MHz and 1 GHz, it is over 6 (beyond the scope of the plot) and as a result, the quality factor increases monotonically with N within the range of interest. At 5 GHz, the peak quality factor is reached at $N_c = 3$. At 10 GHz, it drops to 1, and thus the quality factor monotonically decreases with N. Third, for higher frequency, the quality factor changes (either increases or decreases) faster with N.

Finally, although not shown in the figure, self-resonant frequency is decreasing from over 200 GHz to 40 GHz when N increases from 1 to 6.

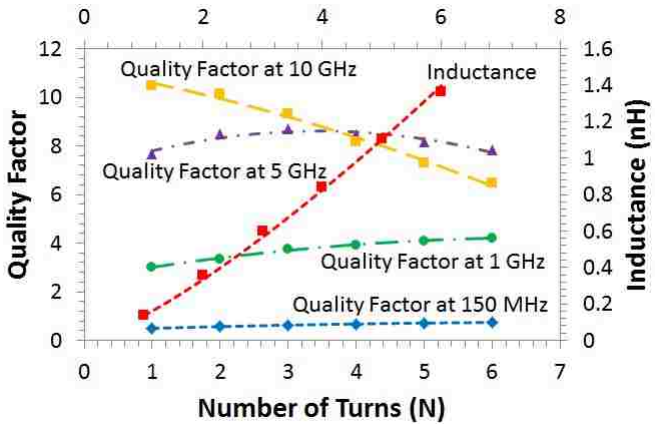


Figure 2.8 Q and L vs. number of turns N

Observation 7: For the range of interest, increasing the number of turns N increases the inductance. There might exist a critical number of turns N_c that gives maximum quality factor, and such N_c decreases with the frequency. The self-resonance frequency drops rapidly with the increase of N.

2.7 NUMBER OF TIERS (T)

The quality factor and the inductance for different number of tiers and operating frequencies are shown in Figure 2.9. The parameter T looks similar to the TSV substrate height H, but it is the non-conducting inter-layer adhesive that makes it different. The adhesive layer should have little impact on the inductance, but big impact on the quality factor. In terms of the quality factor, first, there exists a particular T_c that gives maximum quality factor. Second, such T_c decreases with the frequency. At 1 GHz, it is over 6 and as a result, the quality factor increases monotonically with T. At 5 GHz, the peak quality factor is reached at $T_c = 4$. At 10 GHz, it drops to 3. Third, for higher frequency, the quality factor changes (either increase or decrease) faster with T.

Finally, although not shown in the figure, the self-resonant frequency decreases from over 250 GHz to 38 GHz when T increases from 2 to 6.

Observation 8: For the range of interest, increasing the number of tiers T increases the inductance. There might exist a critical number of tiers T_c that gives maximum quality factor, and such T_c decreases with the frequency. The self-resonance frequency drops rapidly with the increase of T.

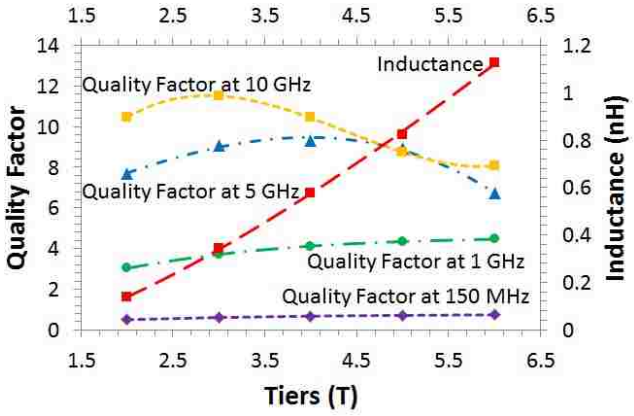


Figure 2.9 Q and L vs. number of tiers T

How T_c changes with different N, and how N_c changes with different T, at the same frequency need to be studied. N and T are varied based on nominal setting to perform simulation, and the results at 5 GHz are reported in Table 2.2 and Table 2.3, respectively. The corresponding Q_{max} at T_c (or N_c) are included. From Table 2.2, it can be seen that with more turns, the number of tiers that gives maximum quality factor decreases. Similarly, from Table 2.3, with more tiers, the number of turns that gives maximum quality factor decreases.

Table 2.2 T_c and Q vs. N (measured at 5 GHz)

N	1	2	3	4	5
T_c	4	2	2	2	2
Q_{max}	9.32	8.50	8.77	8.60	8.23

Table 2.3 N_c and Q vs. T (measured at 5 GHz)

T	2	3	4	5
N_c	3	1	1	1
Q_{max}	8.77	9.11	9.32	8.95

2.8 LOOP PITCH (P)

The quality factor and the inductance for different loop pitches and operating frequencies are shown in Figure 2.10. This is a unique parameter for the TSV inductor. If the loop pitch increases, the inductance decreases slightly, mainly due to the reduced magnetic flux. On the other hand, the quality factor decreases with the increase of P at lower frequencies and remains almost constant at higher frequencies. This is because at lower frequencies the loss is mainly due to the metal resistance, which increases with P. At higher frequencies, the substrate loss starts to dominate, which decreases with the

magnetic flux (with the increase of P). It conforms to the observation 2. Finally, the self-resonant frequency remains almost constant (~250 GHz).

Observation 9: For the range of interest, increasing the loop pitch P slightly decreases the inductance. The quality factor also slightly decreases with P at low frequency, and remains almost constant at high frequency. The self-resonance frequency does not change significantly with P.

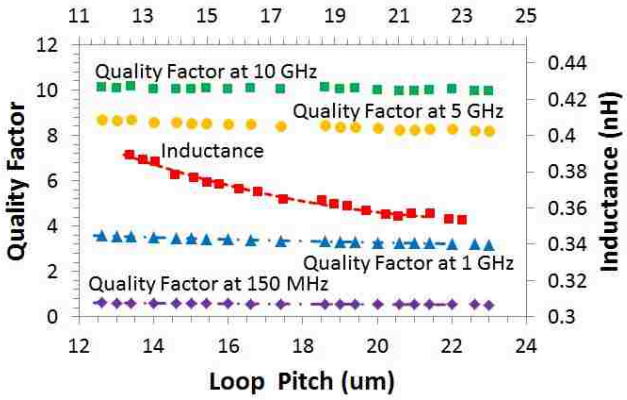


Figure 2.10 Q and L vs. loop pitch P

2.9 METAL WIDTH (W)

The quality factor and the inductance for different metal widths and operating frequencies are shown in Figure 2.11. The inductance decreases as W increases due to the increased capacitive coupling. In terms of quality factor, it increases with W, as the ohmic loss becomes smaller. The impact of W on Q also becomes more profound at higher frequency. Fitting results suggest that the quality factor almost remains constant at 150 MHz. At high frequency, the quality factor increases with cubic trend, which is due to the effect of further AC resistance reduction from substrate coupling.

Finally, the self-resonant frequency remains almost constant (~250 GHz).

Observation 10: For the range of interest, increasing the metal width W decreases the inductance, and has little impact on the quality factor at low frequency. It increases

the quality factor at high frequency. The self-resonant frequency does not change with W significantly.

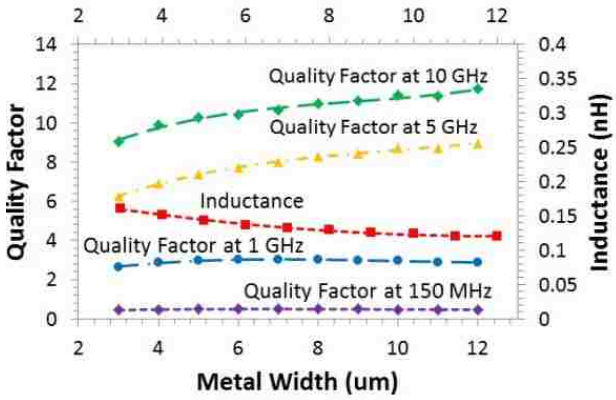
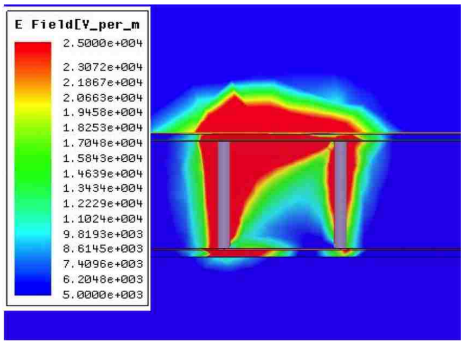


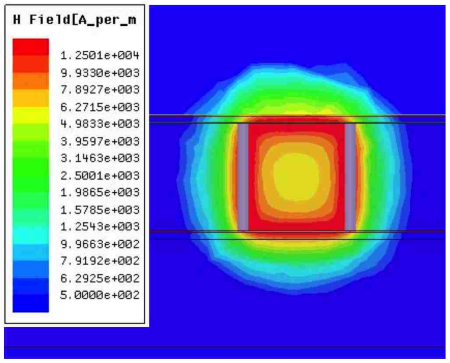
Figure 2.11 Q and L vs. metal width W

3. MICRO-CHANNEL SHIELDING

From Observation 2 in Section 2, the substrate loss dominates when the frequency is over 1 GHz and when the substrate conductivity is over 10 S/m (which is normal for digital applications). In other words, the TSV inductor is subject to severe efficiency loss over 1 GHz due to the eddy current in the substrate. To tackle the issue, effective shield mechanisms to reduce such loss needs to be devised.



(a)



(b)

Figure 3.1 (a) E field and (b) H field without micro-channel distributions

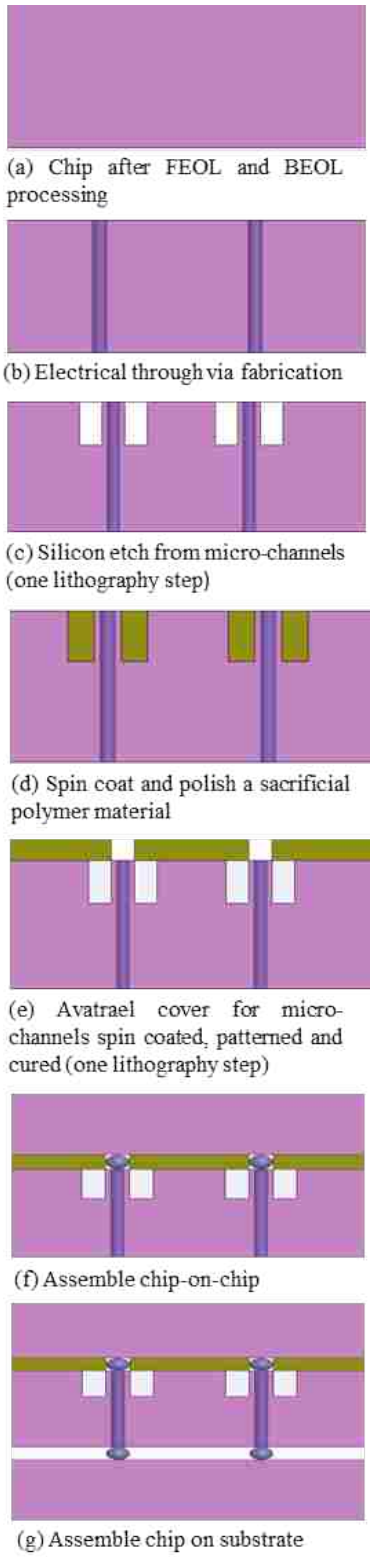


Figure 3.2 Micro-channel fabrication steps

To help understand the distribution of eddy current in the TSV inductor, the nominal setting shown in Section 2.2 is simulated. The resulting E and H fields are plotted in Figure 3.1 (a) and (b), respectively. From the figure, the E field decreases as moving farther from the TSVs, while the H field completely penetrates through the area between the TSVs. As such, most of the eddy current loss comes from the silicon substrate near the TSVs, which inspires to think: *Why not remove the silicon substrate in that area?*

This reminds about a seemingly irrelevant technique, micro-channel, which has been widely used as a low-cost heat-removal technique in 3D ICs (e.g.[29, 30]). Simply speaking, the technique etches a channel from the bottom surface of the substrate for liquid cooling and only requires extra two lithography steps, which are relatively cheap to implement. The fabrication process of micro-channel is already mature – an example of such a process from IBM and Nanonexus is shown in Figure 3.2 [16].

In this situation, such channels adjacent to the TSVs to remove part of the substrate can be placed. Specifically, four identical channels are etched, one on each side of the two TSVs. An illustration of such a structure is shown in Figure 3.3 for a two-tier design. For multiple tiers, four channels at each tier are placed, adjacent to the TSVs. The micro-channels can either be filled with coolant like conventional micro-channels, or just open with air. Note that these channels are etched on the backside of the silicon substrate, and will not affect any devices.

The E and H fields for the TSV inductor structure with micro-channels are plotted in Figure 3.4 (a) and (b), respectively. From the figure, the E field is almost same in the silicon and the E field in the micro-channel doesn't contribute to losses. Hence the quality factor increases. The H field doesn't have any impact and hence the inductance doesn't vary much for the design with micro-channels compared without the micro-channels case.

An extra benefit of such technique is the reduced temperature at the inductor. When inductors are used to form antennas, they typically bear high temperature [29]. Accordingly, with the micro-channels the heat will be able to dissipate faster.

Table 3.1 Q vs. micro-channel dimension (10 GHz, N = 6, T = 2)

		W_c (μm)		
		10	20	25
H_c (μm)	10	6.71 (4.5%)	6.92 (8.1%)	7.03 (9.6%)
	20	7.02 (9.6%)	7.29 (13.8%)	7.46 (16.3%)
	30	7.34 (14.6%)	7.76 (21.1%)	7.94 (23.9%)
	40	7.73 (20.5%)	8.28 (29.2%)	8.59 (34.0%)
	50	8.25 (28.8%)	8.98 (40.1%)	9.41 (46.1%)
	60	9.12 (42.2%)	10.34(61.4%)	10.96 (71.0%)

To verify the effectiveness of this approach, the height (H_c) and the width (W_c) of the four micro-channels are varied and the improvement of Q at 10 GHz based on a structure with two tiers (T=2) and six turns (N = 6) are compared. All the other parameters conform to the nominal settings discussed in Section 2. The micro-channels are placed 5 μm from TSV center to the nearer edge of the channel. The resulting Q is reported in Table 3.1. The improvements over the case without micro-channel shields are also reported in parentheses.

From the table, the channel height and width have profound impact on Q. For the maximum height of 60 μm and width of 25 μm, a 71.0% improvement of Q over the TSV inductor without micro-channel can be observed. Considering reliability and manufacturability, the aspect ratio of the channel is limited [31] and it depends on the dimensions of the channel and the separation between them. Accordingly, designers should carefully consider the tradeoff between the micro-channel dimension and Q.

How Q and L change when using maximum micro-channel dimensions for different number of turns N, number of tiers T and frequency f are studied. The results on Q and L at 10 GHz are reported in Tables 3.2 and 3.3, respectively. To show the effect at different frequencies, the results on Q at 1 GHz are reported in Table 3.4. Note that the table for L at 1 GHz is omitted as it remains constant with or without the micro-channel. In all the tables, improvement over the case of the same N and T but without the micro-channel is also reported in parentheses.

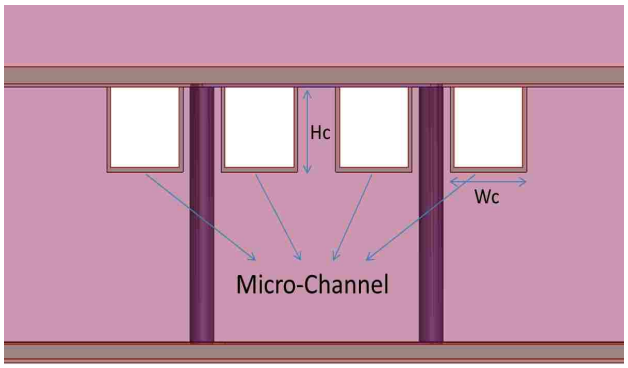
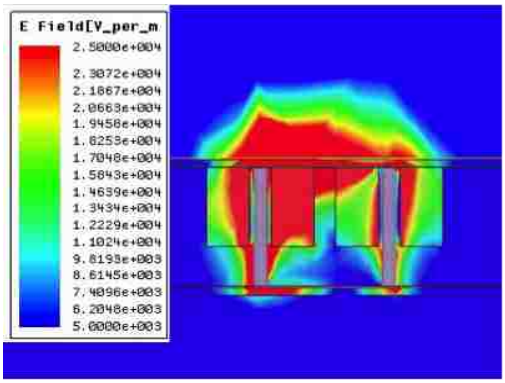


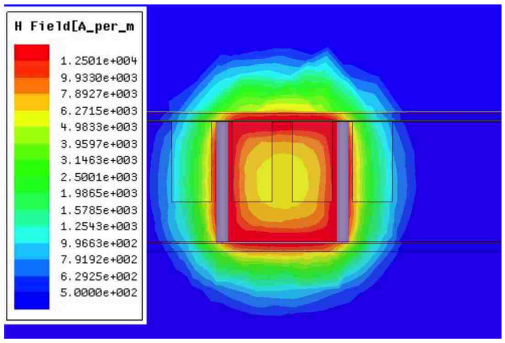
Figure 3.3 Micro-channel shields for substrate loss reduction

From the tables the micro-channel technique is more important at larger N and T, and at higher frequencies – both Q and L improves significantly. This is in accordance with the intuition that substrate losses become larger with larger N, T, or higher f. At 10 GHz, up to 21x increase in Q and 17x increase in L are observed in Tables 3.2 and 3.3 for N=3 and T=5 case, while at 1 GHz only Q is improved by up to 3x is observed when N= 5 and T=5 as shown in Table 3.4.

One more thing worth mentioning here is that the increased self-resonant frequency brought by the micro-channel shield. For example, in Table 3.2, when N = 5 and T = 4, the TSV inductor without micro-channels ceases to work as an inductor ($Q<0$), while the TSV inductor with micro-channels still provides positive quality factor due to the reduced capacitive coupling. For that reason, no improvement is reported for these cases. However, for some cases in Table 3.3 and Table 3.4 the reduction of capacitive coupling is not sufficient to make the structure work as an inductor as observed for the N=6 and T=5 case.



(a)



(b)

Figure 3.4 (a) E field and (b) H field with micro-channel distributions

Table 3.2 Q vs. N and T for maximum micro-channel dimensions (at 10 GHz)

Q		T			
		2	3	4	5
N	1	10.96 (5.88%)	13.12 (14.5%)	14.53 (38.9%)	14.90 (70.3%)
	2	11.36 (11.7%)	11.31 (78.52%)	7.59 (168%)	6.14 (359%)
	3	11.89 (26.3%)	9.15 (167%)	4.65 (406%)	2.00 (2034%)
	4	11.89 (42.4%)	7.46 (269%)	2.93 (1007%)	1.03 N/A
	5	11.37 (55.3%)	5.97 (371%)	1.87 N/A	0.19 N/A
	6	10.98 (71%)	4.74 (483%)	1.01 N/A	-2.08 N/A

Table 3.3 L vs. N and T for maximum micro-channel dimensions (at 10 GHz)

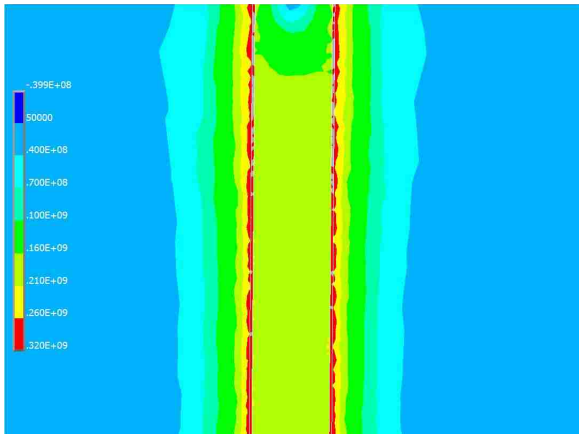
L (nH)		T			
		2	3	4	5
N	1	0.135 (0.0%)	0.344 (0.0%)	0.577 (0.0%)	0.828 (1.2%)
	2	0.344 (0.0%)	0.958 (0.0%)	1.729 (0.0%)	2.708 (11.9%)
	3	0.594 (0.0%)	1.700 (0.0%)	3.523 (39.9%)	5.882 (1615%)
	4	0.843 (0.0%)	2.741 (1.0%)	5.959 (424%)	8.855 N/A
	5	1.093 (0.0%)	3.390 (2.2%)	8.577 N/A	3.055 N/A
	6	1.396 (0.0%)	5.206 (58.5%)	10.634 N/A	-3.518 N/A

Table 3.4 Q vs. N and T for maximum micro-channel dimensions (at 1 GHz)

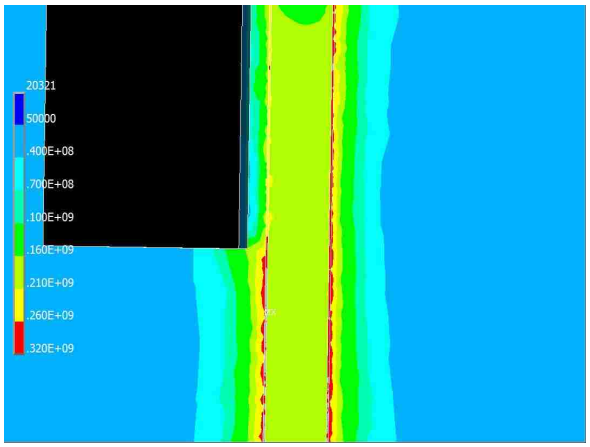
Q		T			
		2	3	4	5
N	1	3.03 (0.0%)	3.74 (0.5%)	4.15 (1.0%)	4.44 (2.0%)
	2	3.36 (0.0%)	4.72 (3.2%)	5.37 (4.8%)	5.90 (9.9%)
	3	3.76 (0.2%)	5.28 (1.7%)	6.39 (15.8%)	6.83 (36.4%)
	4	4.02 (0.8%)	6.04 (11.1%)	7.11 (37.4%)	7.57 (88.3%)
	5	4.13 (0.1%)	6.49 (17.8%)	7.65 (67.0%)	7.78 (153.0%)
	6	4.29 (2.7%)	6.81 (26.5%)	7.92 (98.5%)	8.01 (235.1%)

Table 3.5 Parameters and their respected values used in the stress simulation

Parameter	Copper	Silicon dioxide	Silicon
Elastic modulus (GPa)	110	71	160
Coefficient of thermal expansion (μK^{-1})	17.0	5.0	2.3
Poisson ratio	0.35	0.16	0.28



(a)



(b)

Figure 3.5 Stress distribution (a) without micro-channel and (b) with micro-channel

Finally, how the micro-channel affects the stress distribution are studied. In order to observe the stress distribution with and without micro-channel, ANSYS Mechanical software to simulate the stress are used; the micro-channel are placed as close as to the TSV as possible to observe the maximum impact. The parameters of the materials used are summarized in Table 3.5. The substrate height is 60 μm and the micro-channel width (height) is 20 μm (30 μm). The Von Moises stress distributions of the inductor structure with and without the micro-channel are shown in Figure 3.5 (a) and (b), respectively. From the figure, the stress is actually decreased, which is mainly due to the expansion allowed along the channel surface. Therefore, the micro-channel has the extra benefit of stress reduction.

4. CONCLUSION

In this paper, how various parameters affect their performance is examined. In addition, a novel shield mechanism utilizing the micro-channel technique to drastically improve the quality factor and the inductance is proposed. The technique increases the quality factor and the inductance of the TSV inductor by up to 21x and 17x respectively. To the best of the authors' knowledge, this is the very first in-depth study on TSV inductors to make them practical for high frequency applications. In the future, the metal-filling optimization for inductor formation will be studied.

II. NOVEL THROUGH-SILICON-VIA INDUCTOR BASED ON-CHIP DC-DC CONVERTER DESIGNS IN 3D ICS

Abstract

There has been a tremendous research effort in recent years to move DC-DC converters on chip for enhanced performance. However, a major limiting factor to implement on-chip inductive DC-DC converters is the large area overhead induced by spiral inductors. Towards this, through-silicon-vias (TSVs), a critical enabling technique in three-dimensional (3D) integrated systems, to implement on-chip inductors for DC-DC converters is proposed. While existing literature show that TSV inductors are inferior compared with conventional spiral inductors due to substrate loss for RF applications. In this paper, DC-DC converters are used to demonstrate that the TSV inductors performs better, which operate at relatively low frequencies. Experimental results show that by replacing conventional spiral inductors with TSV inductors, with almost the same efficiency and output voltage, up to 4.3x and 3.2x inductor area reduction can be achieved for the single-phase buck converter and the interleaved buck converter with magnetic coupling, respectively.

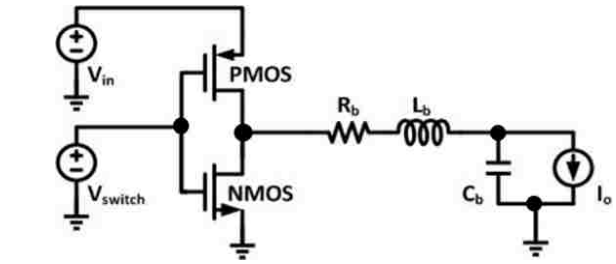
1. INTRODUCTION

There are different types of DC-DC converters such as linear converters, capacitive converters and inductive converters. Linear converters have low area overhead but their efficiency drops rapidly with the increased load or input/output voltage difference. Capacitive converters can work for large input/output voltage difference but their efficiency is still limited to relatively low current loads.

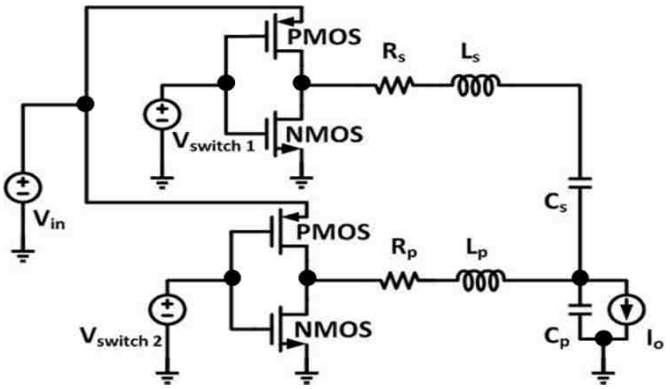
Different from linear and capacitive converters, the efficiency of the inductive converters solely depends on the parasitics of the components. There are various ways to implement inductive converters such as single-phase buck converters, interleaved buck converters and interleaved buck converters with magnetic coupling [11]. They span the tradeoffs between design complexity and performance, which can be evaluated by the voltage ripple, power efficiency and output droop [11, 12]. In this paper, two types of converters, single-phase buck converter and interleaved buck converter with magnetic coupling are used as the vehicles to demonstrate the efficacy of the TSV inductors for DC-DC converter designs.

The circuit diagram for the single-phase buck converter and the interleaved buck converter with magnetic coupling is shown in Figure 1.1. The singe-phase buck converter is the simplest inductive converter. The output voltage ripple occurs due to the charging and discharging of the capacitor and decreases with increase of inductance and capacitance. Despite its simplicity, the output ripple is usually high.

In order to reduce the output ripple, the interleaved buck converter with magnetic coupling has been proposed. The magnetic coupling between two vertically stacked inductors (L_s and L_p) helps to increase the inductance within the same area. The primary phase (L_p and C_p) is connected to the load and operates with the duty cycle D, while the secondary phase (L_s and C_s) is unloaded and operates with the duty cycle of 1-D. The only remarkable difference in its operation compared with the single-phase buck converter is that the two phases generate different voltages and are coupled with a capacitor C_s which blocks DC current between the primary and secondary phases. The AC current is out of phase to the load current and hence the ripple is reduced.



(a)



(b)

Figure 1.1 (a) Single-phase buck converter and (b) Interleaved buck converter with magnetic coupling schematics

The biggest challenge to implement both converters on chip is the large area required by the inductors, either the single inductor in the single-phase buck converter or the coupled inductor pairs in the interleaved buck converter with magnetic coupling.

2. TSV INDUCTOR DESIGNS

TSV allows implementing inductors in a three-dimensional space to save area. In this section, various interesting structures for a single TSV inductor and a coupled TSV inductor pair are proposed, and their metrics such as the inductance L, quality factor Q, series DC resistance (R_{dc}) and AC resistance (R_{ac}) are compared. For all the simulations in this section, an industrial 3D full-wave electromagnetic (EM) simulation tool is used. All the process parameters in this section are modified slightly from real foundry data.

For the TSV inductors, a three-tier 3D process with 20 μm TSV diameter and 0.5 μm liner thickness is assumed. The inductor can be constructed in the top two tiers, the substrate height of which are thinned to 60 um and have the conductivity of 10 S/m. For each tier a total of 9 metal layers (M1-M9) are available of 30 μm thick in total. M8 and M9 metal layers are 7 μm thick each and the oxide layer between them is 5 μm thick. The M7 metal layer is of 1 μm thick and the oxide layer between M7 and M8 is 2 μm thick. The inter-adhesive layer (used to connect two tiers) between tiers is 2 μm thick. All the metal strips to connect TSVs are 30 μm wide.

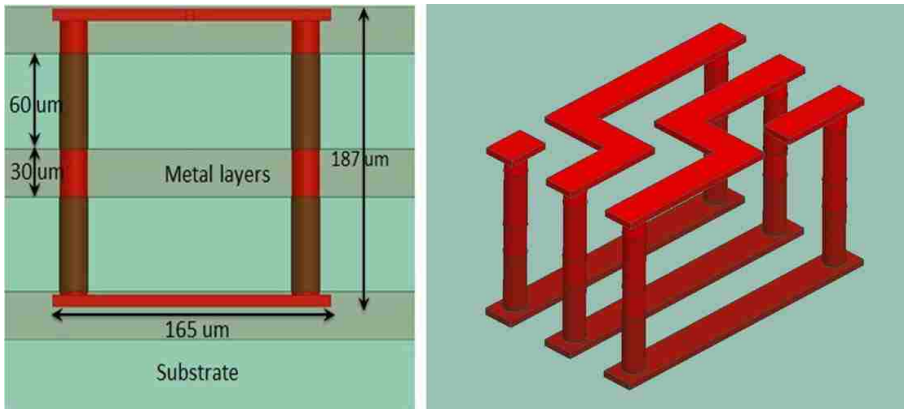
For comparison purposes, a single spiral inductor and a coupled spiral inductor pair following the description in [24,25] are also implemented. For both designs, a process of 9 metal layers (M1-M9) with 30 μm thickness in total is assumed. The top two metal layers M8 and M9 are of 7 μm thick each. The substrate height is 300 μm. The patterned ground shield (PGS) is constructed 5 μm below the spiral inductor(s). The PGS use 10 μm metal width with 1 μm pitch.

The single inductor is implemented in a 2-turn spiral structure, using only the top metal layer M9. The diameter of the spiral inductor is 336 μm. The metal width is 30 μm and the pitch is 5 μm. The simulated inductance is 1.72 nH and R_{dc} is 178 mΩ.

The coupled inductor pair is stacked using M8 and M9 (one on each layer). Each inductor has 2 turns, and the diameter is 350 μm. The metal width is 30 μm and the pitch is 5 μm. The simulated inductance of each inductor is 1.85 nH. The R_{dc} of each inductor is 178 mΩ and the mutual coupling factor k=0.81.

2.1 SINGLE TSV INDUCTOR DESIGN

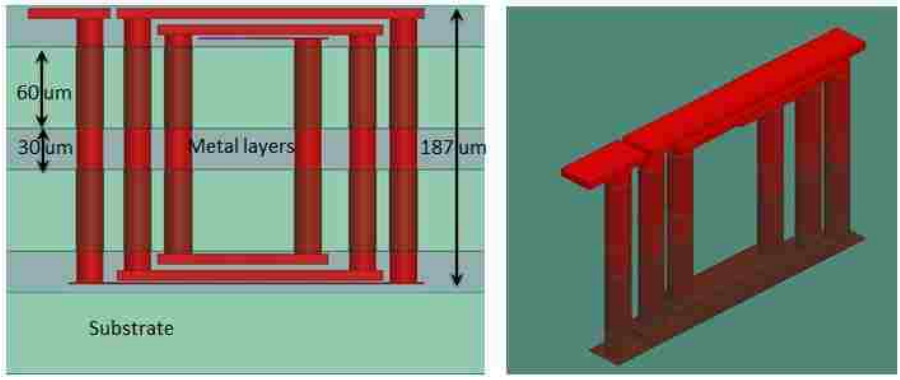
Two TSV inductor structures are designed in order to implement the single-phase buck converter. The first structure (toroidal) is shown in Figure 2.1. To reduce resistance of the inductor, the horizontal metal strips to connect TSVs use M9 of the top tier and the bottom tier. It is easy to find out based on the process parameters discussed previously that the total height of the TSV inductor is 187 µm. As such, in order to maximize the quality factor, the TSV pitch is also set of 165 µm (square cross-sectional area). Furthermore, in order to match the inductance of the conventional spiral inductor discussed above, a total of 3 turns are used, with a loop pitch (defined as the separation between adjacent turns measured from the edges) of 5 µm. The simulated R_{dc} is 170 mΩ and the inductance is 1.72 nH.



(a) (b)

Figure 2.1 Toroidal TSV inductor (a) cross-sectional and (b) rotated view (not to scale)

The second structure (vertical spiral) is inspired by the conventional spiral inductor, as shown in Figure 2.2. A 3-turn structure is implemented. The outermost loop uses M9 of the top tier and M7 of the bottom tier; the middle loop uses M8 of both tiers; and the innermost loop uses M7 of the top tier and M9 of the bottom tier. The simulated R_{dc} is 230 mΩ and the inductance is 1.73 nH.



(a) (b)

Figure 2.2 Vertical TSV inductor (a) cross-sectional and (b) rotated view (not to scale)

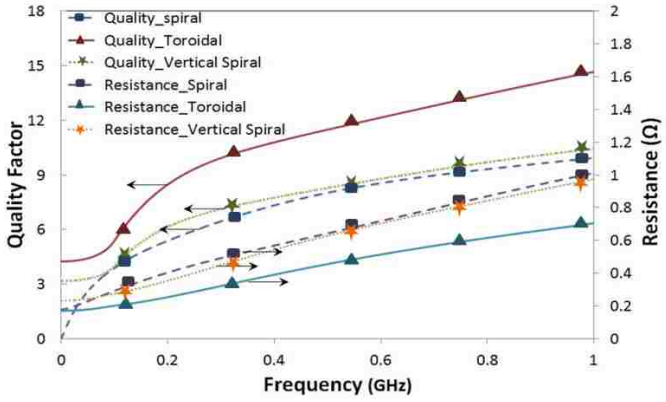


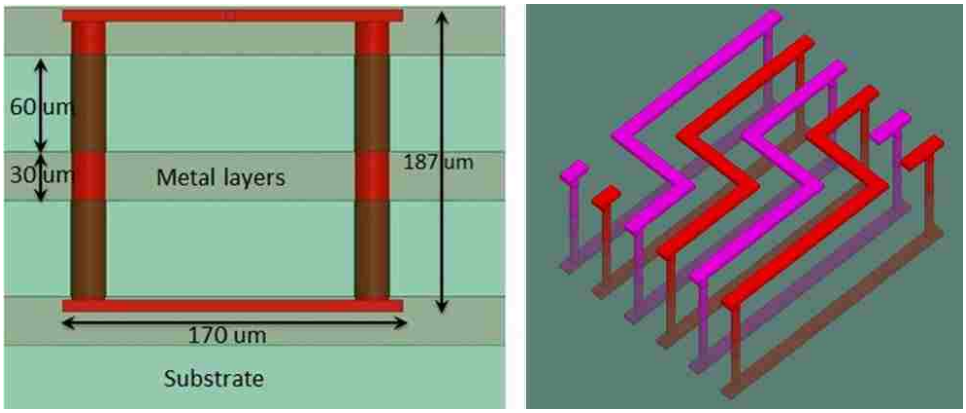
Figure 2.3 AC resistance and Q vs. frequency for different types of inductors

Finally, the quality factor Q of both TSV inductors as well as the conventional spiral inductor with respect to frequency is simulated. The results with respect to frequency are shown in the Figure 2.3. The frequency range is limited to 1 GHz considering the target application of DC-DC converters. From the figure, the toroidal TSV inductor has the smallest Rac and the highest Q compared with the other two inductors, due to its larger cross-sectional area.

2.2 COUPLED TSV INDUCTOR DESIGN

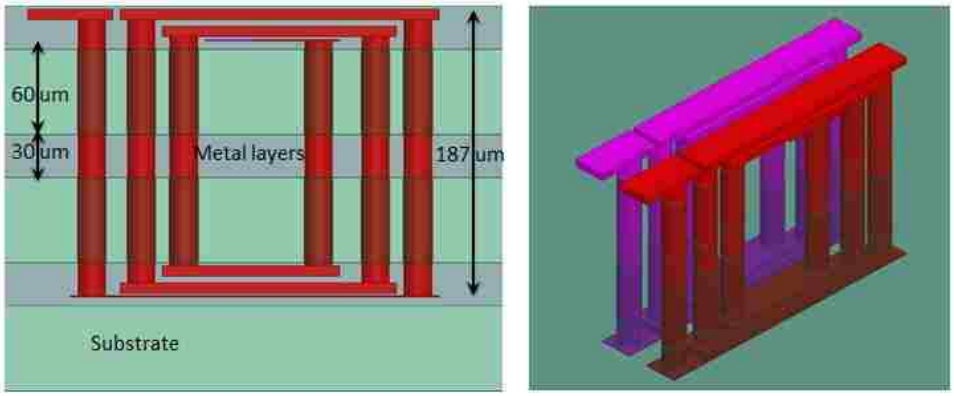
For interleaved buck converters with magnetic coupling, a coupled TSV inductor pair is needed. In addition to enhance performance, high mutual coupling factor k is desired. The question now is how to design best structures with maximal k.

For toroidal TSV inductors, an interleaved coupling structure as shown in Figure 2.4 is proposed. Such structure allows maximum interaction between the magnetic flux from each inductor. All the geometric parameters remain the same as for the single torodial TSV inductor case described in Section 2, except that the loop pitch is now measured between the adjacent turns of different inductors and the TSV pitch is 170 μm. The mutual coupling factor is simulated to be k=0.71. The smaller k compared with that of the spiral inductor (0.81) is due to the lossy substrate. The R_{dc} of each inductor is 246 mΩ and the inductance of each inductor is 1.86 nH.



(a) (b)

Figure 2.4 Coupled toroidal TSV inductor pair (a) cross-sectional view and (b) rotated view (not to scale)



(a) (b)

Figure 2.5 Coupled vertical spiral TSV inductor pair (a) cross-sectional view and (b) rotated view (not to scale)

The coupling structure for vertical spiral TSV inductors is relatively straightforward, as shown in Figure 2.5. All geometric parameters follow those of the single vertical spiral inductor in Section 2.1. The pitch between the two vertical spiral TSV inductors is 5 μm. The mutual coupling factor is simulated to be k=0.57. The R_{dc} of each inductor is 312 mΩ and the inductance of each inductor is 1.84 nH.

3. COMPARISON WITH SPIRAL INDUCTORS

To compare the performance of TSV inductors and conventional spiral inductors in DC-DC converters, a total of six designs are implemented, i.e., single-phase buck converters with conventional spiral inductor, toroidal TSV inductor and vertical spiral TSV inductor, as well as interleaved buck converters with magnetic coupling using these three inductors. For all designs, the target design specs are listed in Table 3.1. The designs are implemented in an industrial custom IC design environment with a 45nm process design kit. The inductors are embedded in the designs using S-parameter models, which are extracted from an industrial 3D full-wave EM simulation tool in the frequency range of DC to 20 GHz.

Table 3.1 Target design specs for all DC-DC converters

Vin	Vout	Max output droop	Frequency	Rise/Fall times
1.5 V	1.2V	15%	200 MHz	50 ps

3.1 SINGLE-PHASE BUCK CONVERTER

Based on the simulation results in Section 2.1, the metrics for the spiral inductor as well as the two single TSV inductors as described in Section 3 at 200 MHz are listed in Table 3.2. The transistor sizes and the capacitors are tuned for the single-phase buck converter as shown in Figure 1.1(a) to achieve the design specs listed in Table 3.1. The resulting circuit parameters are shown in Table 3.3 (same for all the three inductors).

The peak efficiency, ripple and area comparison for the single-phase buck converter using different types of inductors are shown in Table 3.4. As from Table 3.4, the three designs exhibit almost the same efficiency, although the peak efficiency is slightly higher for the toroidal TSV inductor and lower for the vertical spiral TSV inductor. It is mainly due to the lower R_{dc} for the toroidal TSV inductor and higher R_{dc} for the vertical spiral TSV inductor, as can be seen from Table 3.2. The output voltage ripple for all the cases are also almost the same as it depends on the inductance and the

capacitance values, which are the same in all the cases. The area for all inductors is measured by the total routing resource occupied. For TSV inductors, the area also includes the substrate occupied by the TSVs. Compared with the spiral inductor, the toroidal TSV inductor and the vertical spiral TSV inductor can reduce the area by 3.5x and 4.3x respectively.

The efficiencies of the three designs change with the load current are studied. As shown in Figure 3.1, all three designs achieve almost the same efficiency in the range from 0 to 600 mA, which is the maximum load under the output voltage droop limit. The optimal load for all designs is 400 mA - 600 mA. Note that according to the discussion in [26], the maximum current density a TSV can handle is around 8 mA/μm^2. Therefore, the optimal load can be achieved since the TSV diameter is 20 μm.

Table 3.2 Parameters for different inductor types (200 MHz)

Type	Spiral	Toroidal	Vertical spiral
L(nH)	1.73	1.72	1.73
R_{dc}(mΩ)	178	170	232
R_{ac}(mΩ)	404	254	354
Q	5.4	8.5	6.1

Table 3.3 Circuit specifications

D (%)	80
C_s	10 nF
ESR of C_s	1 mΩ
PMOS size (W/L)	9.6 mm/ 50 nm
NMOS size (W/L)	1.92 m/ 50 nm

Table 3.4 Peak efficiency, ripple and area comparison for single-phase buck converters with different inductor types

Type	Spiral	Toroidal	Vertical spiral
Peak efficiency (%)	76.6	77.1	74.0
Ripple (mV)	45	45	46
Inductor area (μm^2)	225,792(1)	64,999(1/3.5x)	53,120(1/4.3x)

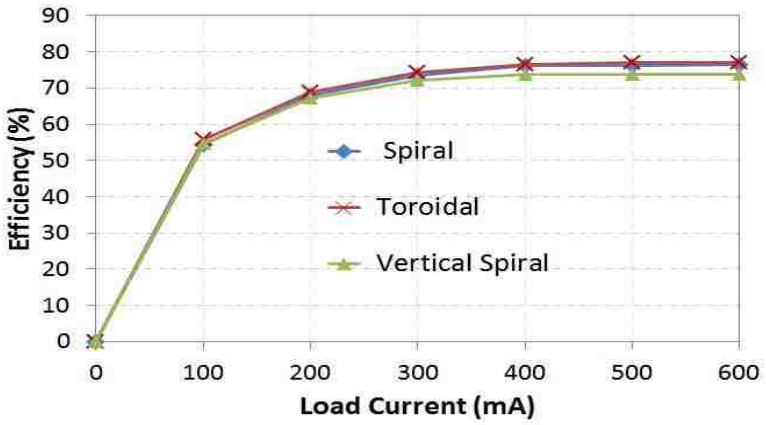


Figure 3.1 Efficiency vs. load current for single-phase buck converters

From all these results, it is clear that TSV inductor based single-phase buck converters can achieve the same efficiency and ripple compared with conventional spiral inductor based ones, but with significantly reduced inductor area.

3.2 INTERLEAVED BUCK CONVERTER WITH MAGNETIC COUPLING

Based on the simulation results in Section 3.1, the metrics for the coupled spiral inductor pair as well as the two TSV inductor pairs as described in Section 2.2 at 200 MHz is listed in Table 3.5.

The transistor sizes and capacitors of the interleaved buck converter with magnetic coupling are tuned as shown in Figure 1.1(b) to achieve the design specs listed in Table 1. The resulting circuit parameters are shown in Table 3.6 (same for all the three inductors).

Table 3.5 Parameters for different inductor types (200 MHz)

Type	Spiral	Toroidal	Vertical spiral
k	0.81	0.71	0.57
L_p (nH)	1.85	1.86	1.84
L_s (nH)	1.85	1.86	1.84
R_{p_dc}(mΩ)	178	246	312
R_{s_dc}(mΩ)	177	246	312
R_{p_ac}(mΩ)	630	358	494
R_{s_ac}(mΩ)	808	356	489
Q_p	3.7	6.5	4.7
Q_s	2.9	6.5	4.6

The peak efficiency, ripple and area comparison using different types of inductors are shown in Table 3.7. The three designs exhibit almost the same efficiency, although the peak efficiency is slightly higher for the coupled spiral inductor pair and lower for the coupled vertical spiral TSV inductor pair. It is due to the lower R_{dc} for the spiral inductor pair and higher R_{dc} for the vertical spiral TSV inductor pair, as can be seen from Table 3.5. Compared with the spiral inductor pair, the toroidal TSV inductor pair and the vertical spiral TSV inductor pair can reduce the area by 2.5x and 3.2x respectively.

Table 3.6 Circuit specifications

D (%)	80
C_s (ESR)	10 nF (1 mΩ)
C_p (ESR)	3 nF (1 mΩ)
PMOS size (W/L)	9.6 mm/ 50 nm
NMOS size (W/L)	1.92 mm/ 50 nm

Table 3.7 Peak efficiency, ripple and area comparison for interleaved buck converters with different inductor types

Type	Spiral	Toroidal	Vertical spiral
Peak efficiency(%)	71.7	69.4	66.0
Ripple (mV)	9	10	10
Inductor area (μm^2)	367,500(1)	147,208(1/2.5x)	115,438(1/3.2x)

The efficiencies of the three designs are studied with the change in load current. As shown in Figure 3.2, all three designs achieve similar efficiency in the range from 0 to 600 mA, which is the maximum load under the maximum output droop constraint. The design with the spiral inductor has the highest efficiency due to its lowest Rdc. The optimal load for all designs is around 600 mA.

From all these results, it is clear that the TSV inductor based interleaved buck converters with magnetic coupling can achieve the same efficiency compared with conventional spiral inductor based ones, but with significantly reduced inductor area.

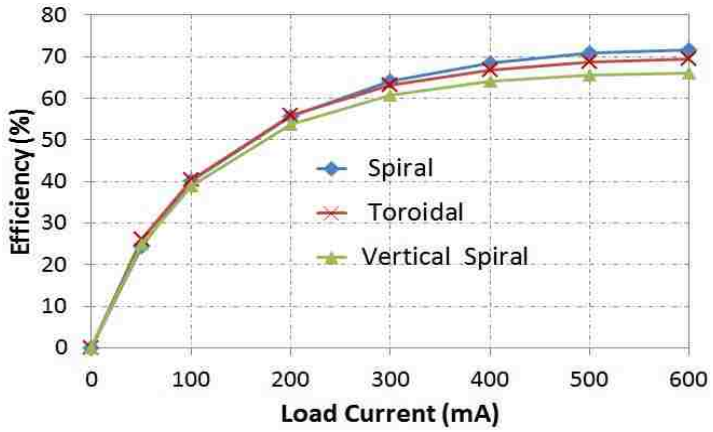


Figure 3.2 Efficiency vs. load current for the interleaved buck converters with magnetic coupling

4. IMPACT OF 3D PROCESS PARAMETERS

In this section, various process parameters of 3D ICs affect the efficiency of inductive converters are studied. Four designs from the previous section are used, i.e., the single-phase buck converters with toroidal TSV inductor and with vertical spiral TSV inductor, as well as the interleaved buck converters with magnetic coupling using these two types of inductors. The practical range of interest for each parameter is listed in Table 4.1. All the other settings conform to those listed in Section 2.

4.1 DIAMETER (D)

The efficiency of the single-phase converter using the two types of inductors at 600 mA load vs. TSV diameter is shown in Figure 4.1. From the figure, the efficiency increases as the TSV diameter increases, due to the reduced Ohmic loss. The converter efficiency is 65.9% at 10 μm and 73.0% at 24 μm. The same observation can be made for the single-phase converter with vertical spiral inductor. The converter efficiency is 59.8% at 10 μm and 70.4% at 24 μm.

Table 4.1 List of parameters, the respective default unit and the ranges of interest

Notation	Meaning	Range
D (μm)	TSV diameter	10 - 24
σ (S/m)	Substrate conductivity	0.1 - 1,000
d (um)	Liner thickness	0.1 - 0.9

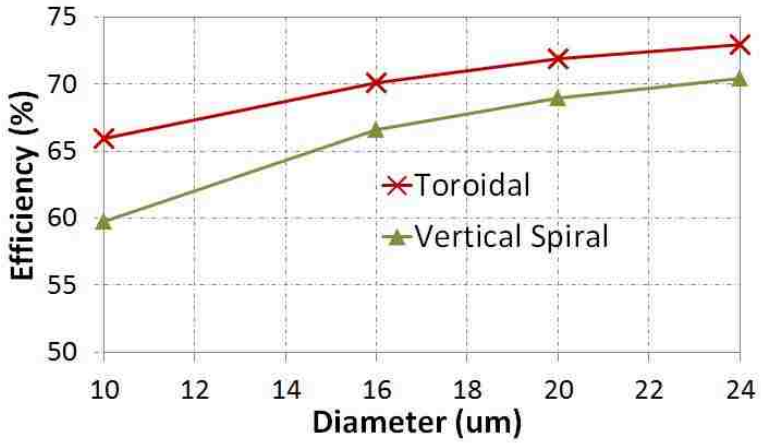


Figure 4.1 Efficiency vs. TSV diameter for single-phase buck converters (600 mA load)

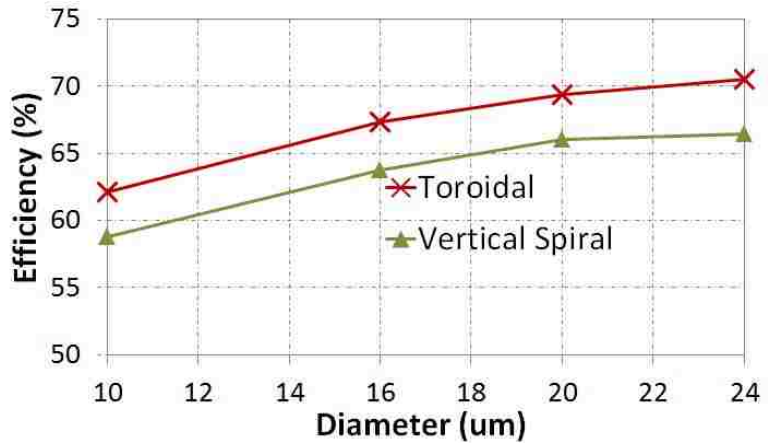


Figure 4.2 Efficiency vs. TSV diameter for interleaved buck converters with magnetic coupling (600 mA load)

The effect of TSV diameter on the efficiency of interleaved buck converters with magnetic coupling is similar, as shown in Figure 4.2.

4.2 SUBSTRATE CONDUCTIVITY (σ)

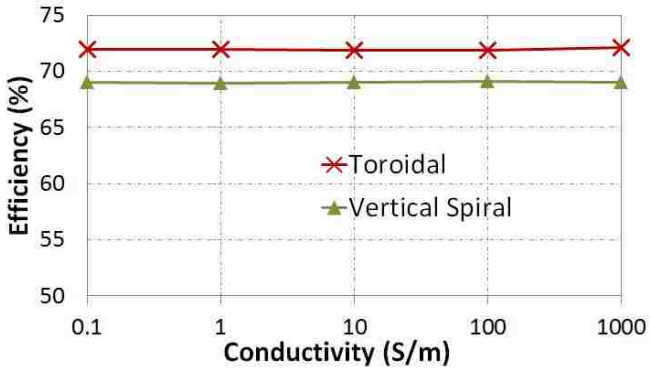


Figure 4.3 Efficiency vs. substrate conductivity for single-phase buck converters (600 mA load). Note that log scale is used for x-axis

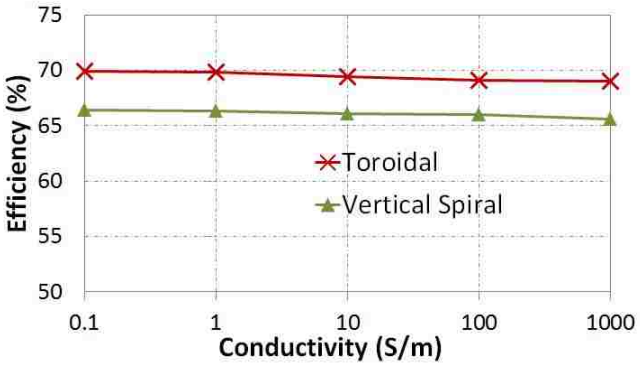


Figure 4.4 Efficiency vs. substrate conductivity for interleaved buck converters with magnetic coupling (600 mA load). Note that log scale is used for x-axis

The efficiency of the single-phase converter using the two types of inductors with 600 mA load vs. substrate conductivity is shown in Figure 4.3. From the figure, the efficiency does not change much with the substrate conductivity. This is because at 200 MHz the eddy current loss in the substrate is minimum [8].

The effect of substrate conductivity on the efficiency of interleaved buck converters with magnetic coupling is shown in Figure 4.4. As can be seen from the figure, the efficiency decreases slightly as the substrate conductivity increases, mainly due to the slightly increased loss in the substrate for the coupled structure.

4.3 LINER THICKNESS (d)

The efficiency of the single-phase converter using the two types of inductors with 600 mA load vs. liner thickness is shown in Figure 4.5. From the figure, the efficiency does not change much with the liner thickness. This is expected, as the liner thickness within the range of interest does not affect the inductor behavior much [8]. Similar observation can be made for interleaved buck converters with magnetic coupling, as shown in Figure 4.6.

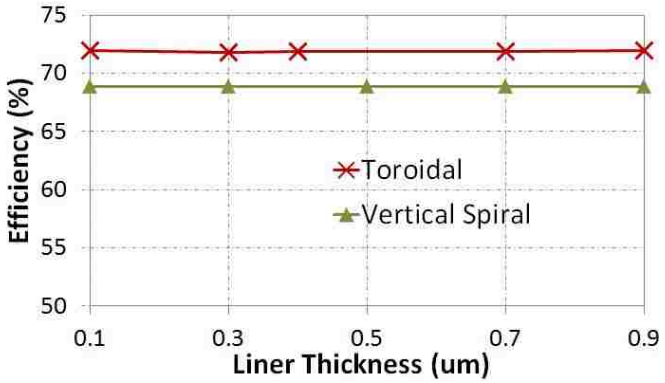


Figure 4.5 Efficiency vs. liner thickness for single-phase buck converters (600 mA load).

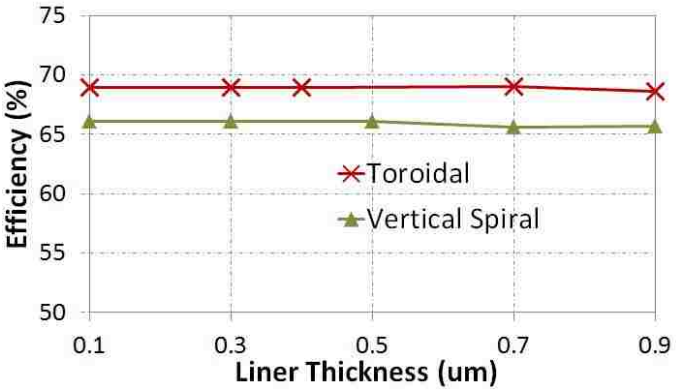


Figure 4.6 Efficiency vs. liner thickness for interleaved buck converters with magnetic coupling (600 mA load).

5. CONCLUSION

On-chip DC-DC converters implementation with significantly reduced area using TSV inductors in 3D ICs is demonstrated. Experimental results show that by replacing conventional spiral inductors with TSV inductors, with almost the same efficiency and output voltage, up to 4.3x and 3.2x inductor area reduction can be achieved for the single-phase buck converter and the interleaved buck converter with magnetic coupling, respectively. Various 3D IC process parameters affect the converter efficiency are observed.

III. OPPORTUNISTIC THROUGH-SILICON-VIA INDUCTOR UTILIZATION IN LC RESONANT CLOCKS: CONCEPTS AND ALGORITHMS

Abstract

LC resonant clock is an attracting option for low power on-chip clock distribution designs. However, a major limiting factor to its implementation is the large area overhead due to the conventional spiral inductors. On the other hand, idle through-silicon-vias (TSVs) in three-dimensional integrated circuits (3D ICs) can form vertical inductors with minimal footprint and little noise coupling with horizontal traces, particularly suitable for the application of LC resonant clock. However, due to the strict constraints on the location of idle TSVs, the use of the TSV inductor is limited by the constrained choices of its location, inductance and quality factor. Moreover, these TSV inductors can be in any orientation with any distance apart, thereby causing complicated coupling effects. In this paper, a novel scheme to opportunistically use idle TSVs to form inductors in LC resonant clock of 3D ICs for maximum power reduction is presented. The problem is formulated and a greedy algorithm to efficiently solve it is devised. Experimental results on a few industrial designs show that compared with the conventional resonant clock designs using spiral inductors, the scheme with TSV inductors can reduce the inductor footprint by up to 6.30x with the same power consumption. Especially these TSV inductors are formed by existing idle TSVs so they essentially come for free.

1. INTRODUCTION

Power consumption has become a major limiting factor to many high performance designs today. Despite the development of various low power design techniques, the clock distribution network (CDN) consumes a significant portion (i.e., 30%-70%) of the total on-chip power, mainly due to the constant switching and large capacitance loads from the registers.

To reduce CDN power, many prior works have examined techniques such as logic reordering [13], clock and power gating [14], and dynamic voltage and frequency scaling [15]. However, these techniques either require modification of the circuit logic, or are not effective at peak data rate. In this respect, resonant clocking has become an attracting option and widely investigated in low power designs, which utilize some resonant mechanisms for power reduction [16-23].

Resonant clocks can be implemented in different ways such as standing wave [16], rotary wave [17] and LC tank [18]. Standing wave has the limitation of amplitude variation while rotary wave has the limitation of phase variation. Thus, the original CDN needs to be modified accordingly in order to reduce the distortion. On the other hand, LC tank resonant clocks have the same phase and amplitudes, and hence require minimum modification to the CDN. An illustration of LC resonant CDN is shown in Figure 1.1, which contains a top-level buffer tree connecting to a resonant grid and then the registers. A few inductors are attached to selected nodes in the grid to form LC tanks with the capacitances from adjacent registers. Capacitors can be inserted between the inductors and the ground for DC decoupling and voltage level shifting.

Although the LC resonant CDN is easy to implement, a major bottleneck is the demanded large area overhead (1) to form the inductors with the desired inductance and quality factor; and (2) to insert shields ensuring signal integrity and preventing coupling. In order to resolve this issue, various inductor placement strategies have been proposed in literature for efficient utilization and footprint reduction [19-23].

With the overall structure shown in Figure 1.1, the main idea of LC resonant CDN is to store energy in the distributed LC oscillators and hence reducing the energy dissipation. This concept can be simply explained using Figure 1.1. Consider the circuit

shown in Figure 1.2(a). There is no energy stored in the circuit and the capacitor draws energy from the source every time it needs to charge. Now consider the circuit shown in Figure 1.2(b) where an inductor is attached parallel to the capacitor, forming a parallel LC tank. At resonance, the LC tank oscillates and energy is exchanged between inductor and capacitor. Whenever the capacitor needs to charge, some energy is transferred from the inductor, and vice versa. As such, the capacitor draws less power from the source. This exchange of energy between inductor and capacitor occurs at a specific frequency called resonant frequency and is given by

$$f_r = \frac{1}{2\pi\sqrt{L_1 C_1}} \tag{1}$$

Ideally, f_r needs to be perfectly aligned with the fundamental frequency f_0 of the clock, i.e.,

$$f_r = f_0 = 1/T_0 \tag{2}$$

where T_0 is the period of the clock.

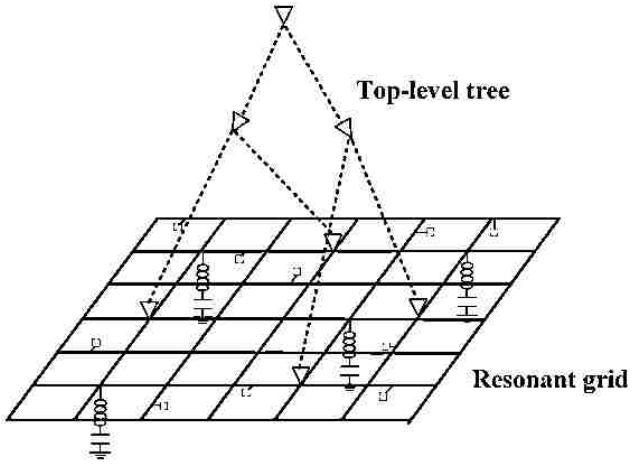


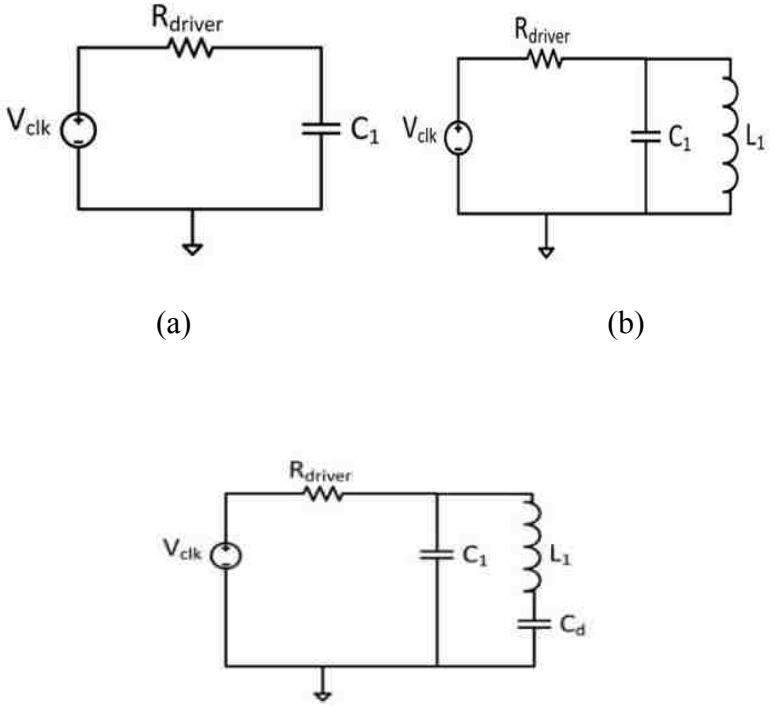
Figure 1.1 Resonant CDN using distributed LC tanks

The LC tank configuration in Figure 1.2(b) will oscillate between positive and negative amplitudes. For the circuit to operate from 0 to V_{dd} as required by CMOS logic,

a positive bias is added using a decoupling capacitor (decap) in series with the inductor, as shown in Figure 1.2(c). To ensure proper functioning of the circuit, the resonant frequencies of the series LC and the parallel LC should be distinct. Accordingly, careful sizing of the decap is needed [20]

$$\frac{1}{2\pi\sqrt{L_1 C_d}} \ll \frac{1}{2\pi\sqrt{L_1 C_1}} \tag{3}$$

In practice $C_d \approx 10C_1$ according to [21]



(a) (b)

(c)

Figure 1.2 (a) RC circuit (b) LC tank (c) LC tank with decoupling capacitor (decap)

2. PROBLEM FORMULATION

In this section, the problem of opportunistic TSV inductor utilization in LC resonant CDNs is formulated. The assumptions are listed below.

1) Due to the quality factor constraint, the wires to form TSV inductors are very short (close to the substrate height, typically 30-140 um). Accordingly, it is always possible to form TSV inductors using any desired routing pattern is assumed, i.e., there is no routing congestion with other nets. In practice, if an inductor cannot be formed due to congestion that can be skipped.

2) While there are many different ways to form TSV inductors depending on the number of tiers available in a 3D IC, in this thesis a two-tier design is assumed and the inductance will be formed in the top tier. With the typical clock frequency (2-3 GHz) and the capacitance that needs to be resonant by an inductor (~20-40 pF) [11], a single-turn TSV inductor is sufficient (~0.1-0.2 nH). Accordingly, all TSV inductors are single turn.

3) Multiple single-turn TSV inductors to share a common TSV as long as in these inductors the current through the common TSV is always following in the same direction (in phase) are allowed. An example is given in Figure 2.1, in which TSV A and TSV B to form an inductor can be used, and then TSV B and TSV C to form another. Any such inductors are positively coupled, which increases the effective inductance and the quality factor.

4) All the process parameters including TSV height, diameter, liner thickness and substrate doping density is assumed to be provided. In the experiments, these parameters are extracted from a real 3D process from industry.

5) All idle TSVs, including thermal TSVs and dummy TSVs for density filling are assumed to be available to form inductors. The scheme will not change their locations and thus there is no perturbation to the existing placement.

6) The insertion of TSV inductors will impact the skew, but not significantly. A local tuning of the buffer size can be performed if necessary, after the TSV inductors are placed.

7) The TSV inductors are vertical and accordingly have little magnetic coupling with the horizontal traces. The Keep-Out-Zone (KOZ) of TSVs further reduces the noise coupling. Accordingly, the noise issue is not considered in this work.

8) The decap C_d can always be formed at desired locations using MIM technology [29], so it will not limit the formation of TSV inductors.

A straightforward formulation of the TSV utilization problem is as follows.

Formulation 1: Given an LC CDN with the extracted parasitic capacitance and resistance, the clock frequency f0, the locations of the idle TSVs and the process parameters, identify the best way to pair these idle TSVs to form single-turn inductors and to connect them to the CDN, so that the maximum dynamic power reduction can be achieved.

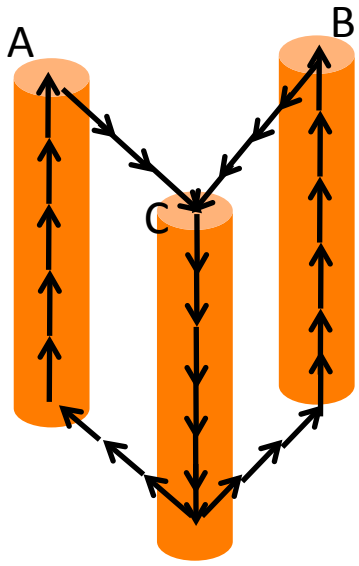


Figure 2.1 TSV inductors sharing one common TSV

The above formulation is very complicated to solve: the locations of the idle TSVs are fixed, and accordingly, the inductance, the quality factor and the location of the TSV inductors are strictly constrained. As such, they may not be optimal or even available as what is desired. In addition, these TSV inductors can be in any orientation

with any distance apart, and thus the coupling situation is complicated. These are different from the placement of conventional spiral inductors, and accordingly none of the existing works can be applied. A Naïve solution is to enumerate all the possible scenarios and simulate each using SPICE to find the best solution, which gives exponential complexity. In later sections, provide a greedy heuristic to solve it efficiently is presented.

3. ALGORITHM OVERVIEW

3.1 ALGORITHM OVERVIEW

Considering the complexity of the problem, it is mapped into a graph and resort to a greedy heuristic, which iteratively forms the "best available" TSV inductor. The overall flow of the algorithm is illustrated in Figure 3.1. The three major steps in the algorithm are (1) inductor characterization, (2) grid annotation, and (3) greedy inductor selection.

In inductor characterization, the parameters of the 3D process and decide which of the idle TSVs can be paired to form an inductor are taken. One vertex is used to represent each TSV, and an edge to connect any two TSVs that can form an inductor. The resulted graph is denoted as connectivity graph. The detailed rules to form this graph are discussed in Section 3.2.

Once this graph is formed, for each edge (TSV inductor) a list of candidate nodes in the CDN it can possibly connect to are identified, and the capacitors adjacent to each candidate node. This is detailed in Section 3.3.

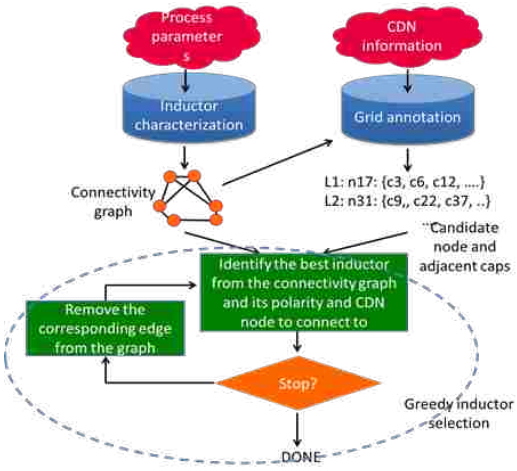


Figure 3.1 Algorithm overview

When the above information is ready, select the best TSV inductor among the ones left iteratively, along with its polarity (i.e., which terminal to connect to the decap, which will affect the coupling with other inductors and accordingly the power reduction) and the best candidate node it should connect to. The corresponding edge from the graph is removed after the TSV inductor is selected. Two tricky questions here are: 1) How to identify the best TSV inductor, its polarity and the node to connect to? And 2) when shall the algorithm stop? These questions will be answered in Section 4.5.

3.2 INDUCTOR CHARACTERIZATION

In order for an inductor to be used in a resonant CDN, it needs to satisfy two properties: 1) its value must be within the proper range so that the frequency at which the inductor resonates with adjacent capacitors aligns with the target clock frequency, and 2) its quality factor needs to be high enough to maintain the resonance. Reference [23] suggests that the quality factor must be at least 3.

As mentioned earlier, the TSV inductors are physically constrained, and thus their inductances and quality factors may deviate from the optimal value. Also, the mutual coupling between TSV inductors will change their inductance and quality factor. To see how these issues affect the power reduction, the inductance and quality factor of the inductor in Figure 1.2(c) are changed and simulate the corresponding power reduction. C_d=560 pF and C_s = 56 pF are used for a clock frequency of 2 GHz. The SPICE simulation result is shown in Figure 3.2. From the figure the power reduction in general increases with the quality factor, and the optimal inductance is 0.11 nH. On the other hand, any inductor with inductance in the range of 0.08-0.12 nH and quality factor over 3 still provides reasonable power reduction. For different capacitance or clock frequency, a similar procedure to get the range is followed. A more theoretical explanation about the trend is provided in Section 4.5.

The parameters of the 3D process including TSV diameter, liner thickness, TSV height and substrate doping density are taken, and use a commercial full-wave simulator

to obtain the relationships between the quality factor/inductance and the distance of the two TSVs that form the inductor. This will allow translating the range of inductance and quality factor to the range of TSV distances.

Finally, the connectivity graph can be constructed by using one vertex to represent each TSV, and then connecting the vertices (TSVs) within the distance range with an edge. The commercial full-wave simulator to characterize the inductance and quality factor of each inductor is used.

3.3 GRID ANNOTATION

Before selecting the TSV inductors for resonant CDN, one more issue need to be addressed that is the possible nodes in the CDN to connect them.

Since these TSV inductors have fixed locations, if a node far away is connected, the extra metal wire will introduce excessive resistance and significantly reduce the quality factor. As such, a constraint for the candidate nodes a TSV inductor can connect to is set: The resistance of the bridge wire (the wire used to connect the inductor to the CDN node) cannot exceed 5% of the total inductor resistance, which translates to no more than 5% loss in the quality factor approximately. If the width of the bridge wire is fixed, the area for the candidate node forms a shape as shown in Figure 3.3, where d=RL/r assuming TSV inductor resistance R_L and bridge wire per-unit-length resistance r. These nodes form a candidate node list for a TSV inductor.

Then for each candidate node, a list of capacitors that are adjacent to it are connected, denoted as adjacent capacitor list. A capacitor is considered adjacent to a node and will appear on the list if and only if 1) There is a resistive path between that node and the capacitor and 2) the total resistance of the path is smaller than a threshold. The first condition guarantees the connection between the inductance and the capacitance. For example, if a candidate node is connected through a wire to the input of a buffer, then the input capacitance of that buffer satisfies this condition while the output capacitance does not. The second condition guarantees that the wire resistance does not significantly shield the capacitor. The following condition is used:

$$R_i \leq \frac{1}{20\pi f_0 C_i} \quad (4)$$

where R_i is the resistance of the path between the candidate node and the capacitor C_i, and f_0 is the clock frequency. This condition guarantees that the capacitor is shielded by no more than 10%. Note that the R_i of each C_i are stored for later use.

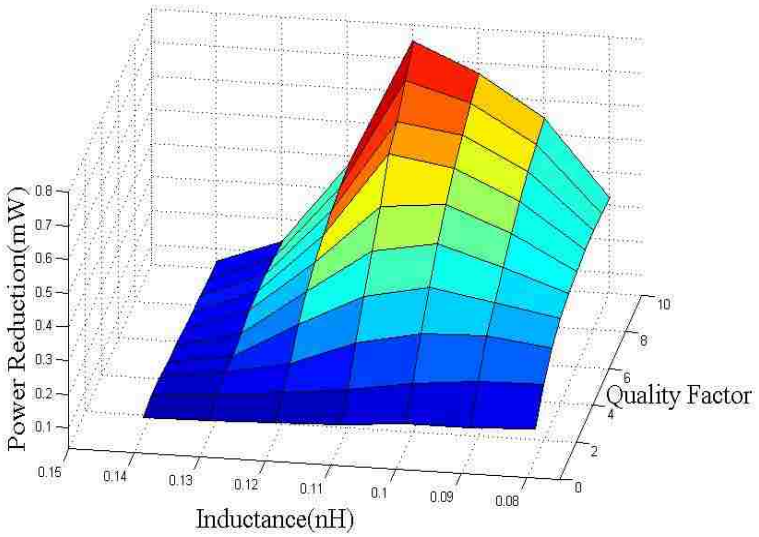


Figure 3.2 Power reduction vs. inductance and quality factor

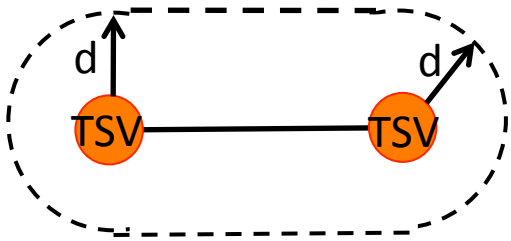


Figure 3.3 Illustration of the area for the candidate node

3.4 GREEDY INDUCTOR SELECTION

With the output from the two steps above, the inductors for resonate CDN construction using a greedy approach are selected. As shown in Figure 3.1, two critical criteria need to be established: the one to identify the best inductor to select, its polarity and the CDN node to connect to, and the one to stop the iterations. In this section, some interesting properties in forming the TSV inductors are first explored, and then establish the two criteria based on theoretical analysis.

3.4.1 Interpretation Using Bipartite Subgraph. The polarities of TSV inductors impose restriction during the selection process. For example, in Figure 3.1, TSVs A and B cannot form an inductor as the currents in both TSVs are always flowing in the same direction. In general, there should be no odd cycles formed by TSV inductors. This has very interesting implication on the distributions of the final TSV inductors selected, as indicated by the theorem below.

Theorem 1. The edges corresponding to the selected TSV inductors in a connectivity graph G form a bipartite graph.

Proof: It is fair to consider the connectivity graph G as being connected. Otherwise each component may be considered separately.

Suppose G has no odd cycles. Choose any vertex $v \in G$. Divide G into two sets of vertices: Let A be the set of vertices such that the shortest path from each element of A to v is of odd length; Let B be the set of vertices such that the shortest path from each element of B to v is of even length. Then $v \in B$ and $A \cap B = \emptyset$.

Suppose $a1, a2 \in A$ are adjacent. Then there would be a closed walk of odd length (v,…,a1, a2 ,…,v). But a graph containing closed walk of odd length also contains odd cycle, which contradicts the fact that G contains no odd cycles. So no two vertices in A can be adjacent.

By the same argument, neither can any two vertices in B be adjacent. Thus A and B satisfy the conditions to be bipartite. ■

Based on Theorem 1, if fixed weight to each edge in the connectivity graph is assigned and if the optimal solution of Formulation 1 would correspond to those edges with maximum weights, then the problem would become a max-weight bipartite subgraph problem, which can be shown to be equivalent to the classical max-cut problem. Unfortunately, due to the mutual coupling between TSV inductors, such a scenario could not happen, and some simple greedy heuristic needs to be used. Fortunately, experimental results suggest that this method is still quite effective.

3.4.2 Selection and Termination Criteria. Intuitively speaking, the selection criterion is to select a best combination of the TSV inductor, its polarity and the corresponding candidate node in the CDN to connect, so that the power reduction can be maximized. Thus, the question is equivalent to identifying the best way to estimate the power reduction for each such combination. Detailed SPICE simulation is not an option here, due to the extremely large number of combinations. An efficient yet accurate estimation is needed.

Towards this, it is important to first establish the following lemma and theorem.

Lemma 1: Assuming the clock period is long enough to allow full swing on all capacitors, the dynamic power consumed in any RC clock network can be expressed as

$$P = \sum_{i=1}^{n} C_i V^2 f_0 \qquad (5)$$

where C_i $(1 \leq i \leq n)$ is the ith capacitance in the network. V is the supply voltage and f0 is the clock frequency.

The strict proof of Lemma 1 involves lengthy manipulations and is omitted here in the interest of space. a brief yet more intuitive justification of its correctness is provided.

Lemma 1 is equivalent to the statement that within a clock cycle, the total dynamic energy dissipated in an RC network is $\sum_{i=1}^{n} C_i V^2$. Apparently, the network only consumes dynamic energy from the power supply during the charging phase (when the clock is high). The energy consumption in this phase can be divided into two portions: that stored on the capacitors (which is subsequently dissipated by the resistors in the network during the discharging phase when the clock is low), and that dissipated on the

resistors. The former is readily expressed as $\frac{1}{2}\sum_{i=1}^{n} C_i V^2$. In order to obtain the latter, consider the fact that during discharging, the current flowing through any resistor is identical to that during charging, except for the direction. Accordingly, the total energy dissipated on the resistors during discharging, which is equal to the total energy stored on the capacitors, is the same as that dissipated on the resistors during charging. As such, the total dynamic energy consumed in a clock cycle is $\sum_{i=1}^{n} C_i V^2$.

Lemma 1 suggests that the dynamic power consumption in an RC clock network only depends on the capacitance, and is independent of the wire resistance or the network topology. Note that other power such as leakage or short-circuit power does not follow this conclusion. With Lemma 1, the following theorem can be proved.

Theorem 2: Under first order approximation and ignoring the impact of wire and TSV resistance, the total dynamic power consumption that can be reduced by inserting an inductor with inductance L_i is

$$\Delta P = \begin{cases} \frac{V^2}{4\pi^2 f_0^2 L_i} & (\text{if } L_i \geq \frac{1}{4\pi^2 f_0^2 C_i^{adj}}) \\ C_i^{adj} V^2 - \mu(L_i - \frac{1}{4\pi^2 f_0^2 C_i^{adj}}) & (\text{otherwise}) \end{cases} \quad (6)$$

where C_i^{adj} is the total adjacent capacitance available to resonate with L_i, V the supply voltage, f_0 the clock frequency and μ some constant.

Proof: If $L_i \geq \frac{1}{4\pi^2 f_0^2 C_i^{adj}}$ or equivalently $C_i^{adj} \geq \frac{1}{4\pi^2 f_0^2 L_i}$, C_i^{adj} can be viewed as two capacitance in parallel, $\frac{1}{4\pi^2 f_0^2 L_i}$ and $C_i^{adj} - \frac{1}{4\pi^2 f_0^2 L_i}$. At the fundamental frequency, if the wire resistance is ignored, the former resonates with L_i at f_0 and the LC tank becomes open. Ignoring the higher order harmonics which decay quadratically in amplitude, from Lemma 1, the total power that can be reduced is $\frac{V^2}{4\pi^2 f_0^2 L_i}$. Apparently, this reduction decreases as L_i increases.

If $C_i^{adj} \leq \frac{1}{4\pi^2 f_0^2 L_i}$, the LC tank behaves as an inductor at the fundamental frequency. It will consume energy through the resistive wires during charging process, and store energy to be dissipated during the discharging process. It is well established that such power is proportional to its inductance. Also consider the fact that when

$L_i = \frac{1}{4\pi^2 f_0^2 C_i^{adj}}$, the maximum reduction is achieved as $C_i^{adj} V^2$. The constant μ can be obtained by fitting with simulation results. ■

Note that the above analysis also explains the trend in Figure 3.4. For fixed quality factor, when the inductance is larger than the optimal value, the power reduction decreases almost linearly. On the other hand, when the inductance is smaller than the optimal value, the power reduction decreases following an inverse function.

When a new inductor is added in each iteration, it can reduce the power consumption by resonating with the capacitors in its adjacent region. However, it will also introduce mutual coupling effects with some or all of the inductors that have already been selected in previous iterations, thereby impacting their power reductions. The procedure in Algorithm 1 is used to estimate the total power reduction when a new inductor (with given polarity and candidate node) is added to the ones already selected,. Note that in the algorithm M((L_i, L_j) is used to denote the mutual inductance between the two inductors with inductance L_i and L_j when p_i=p_j=1.

INPUT: For each inductor that has already been selected, the inductance L_j^*, polarity p_j^* (-1 or 1, indicating which terminal to connect to the decap), the CDN node n_j^* it connects to, and the adjacent capacitor list of n_j^* $(1 \le j \le k)$; one of the remaining inductors L_i, its polarity p_i, a node n_i in its candidate node list, and the adjacent capacitor list of n_i

OUTPUT: Total power reduction ΔP_{total} achieved by (L_i, p_i and n_i) when combined with the selected ones;

IF Li forms an odd cycle with some inductors in L_j^* $(1 \le j \le k)$ THEN

    Continue;

END IF;

FOR (j=1; $j \le k$; j + +)

    $L_{j,new}^* = L_j^* + p_j^* p_i M(L_j^*, L_i)$; (7)

END FOR;

$L_{k+1,new} = L_i + \sum_{j=1}^{k} p_j^* p_i M(L_j^*, L_i)$; (8)

FOR (j=1; $j \leq k+1$; $j++$)

cap_cover_listj = ∅;

IF $j \leq k$ THEN

adj_cap_listj = adjacent capacitor list of n_j^*;

ELSE

adj_cap_listj = adjacent capacitor list of n_i;

END IF;

N = size(adj_cap_listj); q=0;

Sort adj_cap_listj according to ascending order of the path resistance;

WHILE sum(cap_cover_listj) $\leq \frac{1}{4\pi^2 f_0^2 L_{j,new}}$ and q≤N

Cq = q-th capacitor in adj_cap_listj;

IF Cq ∉ cap_cover_listd ($1 \leq d \leq j-1$);

cap_cover_listj = cap_cover_listj ∪ Cq;

END IF;

q++;

END WHILE;

Use (6) to get ΔP_j based on $L_{j,new}^*(L_{i,new})$ and C_j^{adj} =sum(cap_cover_listj);

END FOR;

RETURN $\Delta P_{total} = \sum_{j=1}^{k+1} \Delta P_j$;

Figure 3.4 Power reduction estimation when adding (L_i, p_i and n_i)

There are three points that are worth noting in the algorithm. First, in (7)-(8) that the current flowing through each TSV inductor has approximately the same amplitude is assumed so that the mutual inductance can be simply superposed among multiple

inductors. Second, a capacitor coverage list for each inductor is used to track the capacitors it covers. This is to address the potential problem that two inductors are resonating with the same capacitor: if (6) is used to obtain the power reduction for each inductor without considering this issue, the total power reduction can be overestimated. Finally, the sorting of adjacent capacitor list is based on the path resistance discussed at the end of Section 3.3.

As for the termination criterion of the whole flow, it will be one of the two cases: 1) No more edge is left in the graph, which means all the TSV inductors are examined, or 2) the TSV inductor corresponding to any remaining edges will not provide further power reduction.

4. EXPERIMENTAL RESULTS

The algorithm is implemented in C. Experiments are performed on a workstation with dual six-core, 2.4 GHz, Intel Xeon E5645 CPU and 96 GB memory. A set of four CDNs extracted from real industrial designs is used, and the detailed information is reported in Table 4.1. All the CDNs are designed to work at 3 GHz. A commercial circuit simulator is used for CDN simulation, and a commercial full-wave simulator to model the inductors. After the inductors are inserted, the buffer size is fine tuned so that the max skew is below 100 ps for all cases.

The 3D process parameters is extracted from in-house flow, with 12 um TSV diameter, 2 um KOZ and 0.5 um liner thickness. The inductors are constructed in the top tier, the substrate height of which is thinned to 60 um and has the conductivity of 10 S/m. For each tier a total of 9 metal layers (M1-M9) are available of 30 μm thick in total. The metal strips to connect TSVs are in M9, which are 7 μm thick and 8 μm wide. The oxide layer between M9 and M8 is 5 μm thick. The inter-adhesive layer between the tiers is 2 μm thick. For each design, the dummy TSVs and thermal TSVs are inserted such that the maximum chip temperature is below 80^{o}C and that there is at least one TSV in every 250 um x 250 um window.

The inductor footprint and skew between the TSV inductor based resonant designs synthesized from the method and the conventional inductor based ones synthesized from the method described in [3] are compared. The power from both methods is matched for fair comparison, and the results are reported in Table 4.2. In the table the number of inductors used by [3] are also reported, as well as the total number of idle TSVs. For the power, the reduction percentage over the regular design without inductors is also included. The footprint of all inductors is measured by the total routing resource occupied. For spiral inductors, the footprint also includes the PGS area, while for TSV inductors it also includes the substrate occupied by the TSVs (including KOZ). From the table TSV inductors usage can reduce the inductance area by up to 8.18x compared with using the conventional spiral inductors, with the same power reduction. In addition, keep in mind that the TSV inductors actually come for free as the existing idle

TSVs are used. Also, it is interesting to see that only a small number of idle TSVs can be utilized to form TSV inductors. The max skew for all cases is below 100 ps.

Table 4.1 Benchmark information

Design	Sink cap (pF)	Total buffer size (mm)	Power (W)
D1	4.2	172.7	11.4
D2	4.1	103.5	7.1
D3	3.6	192.6	11.6
D4	3.4	73.8	5.0

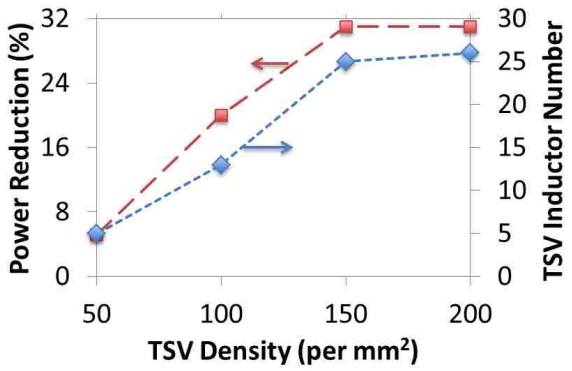


Figure 4.1 Power reduction and TSV inductor number vs. TSV density for design D1

Table 4.2 Footprint/power comparison between TSV inductor based and conventional spiral inductor based resonant CDNs.

	Total buffer size (mm)	# of inductors	Conventional spiral inductor based CDN		TSV inductor based CDN		
			Footprint (μm^2)	Power (W)	# of idle TSVs	Footprint (μm^2)	Power (W)
D1	126.9	26	988000 (1)	8.0 (-29.8%)	24319	166841 (1/5.92)	7.9 (-30.7%)
D2	62.1	23	897000 (1)	3.8 (-46.5%)	21607	147591 (1/6.06)	3.7 (-47.9%)
D3	120.6	40	1620000 (1)	6.7 (-42.2%)	32591	256680 (1/6.30)	6.6 (-43.1%)
D4	52.2	12	456000 (1)	3.4 (-32.0%)	15925	77004 (1/5.92)	3.2 (-36.0%)

The impact of TSV density on the power reduction that can be achieved and the number of TSV inductors that can be formed are studied. The result for Design D1 is depicted in Figure 4.1. As expected, with the increase of TSV density, both the power reduction and the number of TSV inductors increases.

Finally, the impact of the clock frequency using the same design is studied when the TSV density is 200/mm^2, and the result is shown in Figure 4.2. From the figure the decrease of clock frequency, both the power reduction and the number of TSV inductors drops. This is because as the clock frequency decreases, larger inductance is needed to resonate the same capacitor, and accordingly fewer TSV inductors can be formed with the same TSV density.

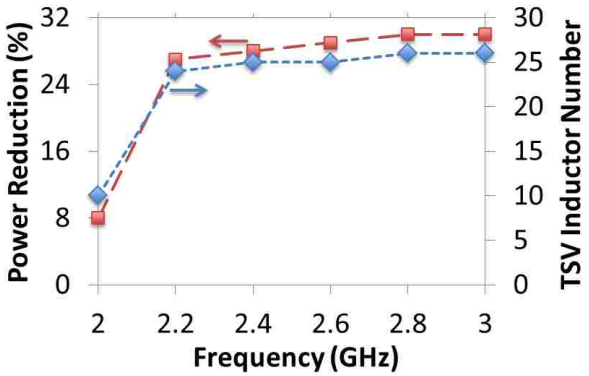


Figure 4.2 Power reduction and TSV inductor number vs. clock frequency for design D1 (TSV density = 200/mm^2)

5. CONCLUSION

The opportunistic application of TSV inductors, formed by idle TSVs in 3D ICs, to reduce the large inductor area in resonant clocks is explored. A novel scheme to handle the unique challenges of constrained inductance and quality factor of TSV inductors is proposed. Experimental results on a few industrial designs show that compared with the conventional resonant clock designs using spiral inductors, the scheme with TSV inductors can reduce the inductor footprint by up to 6.30x with the same power consumption.

SECTION

2. CONCLUSIONS

In this thesis, two applications i.e., DC-DC converters and Resonant clocking method using TSV inductors are studied systematically. For inductive DC-DC converters, experimental results show that by replacing conventional spiral inductors with TSV inductors, with almost the same efficiency and output voltage, up to 4.3x and 3.2x inductor area reduction can be achieved for the single-phase buck converter and the interleaved buck converter with magnetic coupling, respectively. Various 3D IC process parameters affect the converter efficiency is also discussed. For LC resonant clocking, experimental results on a few industrial designs show that compared with the conventional resonant clock designs using spiral inductors, the scheme with TSV inductors can reduce the inductor footprint by up to 6.30x with the same power consumption.

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