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Photo-effects on Current Transport in Back-gate Graphene Field-effect Transistor

Xinlu Chen
Louisiana State University and Agricultural and Mechanical College, xchen67@lsu.edu

PHOTO-EFFECTS ON CURRENT TRANSPORT IN BACK-GATE GRAPHENE FIELD-EFFECT TRANSISTOR

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Xinlu Chen
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ABSTRACT

Graphene, which has attracted wide attention because of its two-dimensional structure and high carrier mobility, is a promising candidate for potential application in optics and electronics. In this dissertation, the photonic effects on current transport in back-gate graphene field-effect transistor is investigated.

Chemical vapor deposition (CVD) on metal provides a promising way for large area, controllability and high quality graphene film. The transfer and back-gate transistor fabrication processes are proposed in this dissertation.

The theoretical analysis of photodetector based on back-gate graphene field-effect transistor has been done. It is shown that the photo-electronic current consists of current contributions from photovoltaic, photo-thermoelectric and photo-bolometric effects. A maximum external responsivity close to 0.0009A/W is achieved at 30µW laser power source and 633nm wavelength. The photodiode based on graphene/silicon Schottky barrier is also. A computed 238.8 W^{-1} photocurrent to dark current ratio normalized by the power source (633nm wavelength and 10mW laser) is obtained. An equivalent circuit model of the graphene/silicon Schottky barrier diode compatible with SPICE simulation is developed and simulated photo-response characteristics are presented using analog behavior modeling which are in close agreement with the theoretical analysis. Besides the optical applications, graphene based-transistors can also be used in applications related to space electronics. The irradiation effects including oxide trap charge and graphene layer traps charges are investigated. A semi-empirical model of graphene back-gate transistors before and after irradiation is predicted.

CHAPTER 1. INTRODUCTION

1.1   Background

Integrated circuit based on silicon technology following the Moore's law has been developing for more than fifty years. The feature size has been scaled from 125 micrometers to 16 nanometers. However, with the technology down to the sub-nanometer scale, the quantum effects appear and increase the difficulty of fabrication, which blocks the Moore's law. How to model and fabricate high speed and low power consumption devices which are related to the high mobility of materials become the key factor to further development of integrated circuits in post silicon era. Emerging nanomaterials based on carbon have attracted much attention and are being studied since carbon nanotube (CNT) was discovered in 1991 [1]. The discovery of two-dimensional carbon material graphene makes this attention of carbon reach a new height in 2004 [2]. Graphene formed by a hexagonal arrangement of carbon atoms has already appeared in theoretical calculation in 1947 [3]. However, due to the Mermin-Wagner theory, it was just considered as a theoretical lattice structure until Geim and Novoselov prepared graphene by mechanical exfoliation [2]. It can be treated as a single layer of graphite or a cut-off carbon nanotube. Since this discovery, graphene has become the most promising material as a result of its unique properties: extremely high mechanical strength [4], high carrier mobility in which the velocity of electrons in graphene is 1/300 times faster than that of light in vacuum, and large spectrum range of absorbing light.

Graphene has a wide range of applications after silicon age. In electronics area, graphene can replace silicon in high speed and low power RF transistors. Besides, it has superior thermal conductivity that can be used as interconnection. Furthermore, the optical applications of graphene have attracted much attention. Various optoelectronic devices have been investigated for integration such as photovoltaic modules, plasmatic devices and solar cells [5, 6].

1.2 Electronic Properties of Graphene

1.2.1 Band Structure

Graphene consists of a hexagonal monolayer σ bond network of sp^2 hybridized carbon atoms which are formed from electrons in the 2s, 2p$_x$ and 2p$_y$ orbitals. The residual 2p$_z$ orbital makes up the π bond which hybridizes together to form the π (occupied) and π* (unoccupied) bands. Figure 1.1 shows the hexagonal structure of carbon atoms in graphene and corresponding hexagonal Brillouin zone. In Figure 1.1, the lattice vectors a$_1$ and a$_2$ are given by:

$$\vec{a}_1 = \frac{3a}{2}\hat{x} + \frac{\sqrt{3}a}{2}\hat{y}, \quad \vec{a}_2 = \frac{3a}{2}\hat{x} - \frac{\sqrt{3}a}{2}\hat{y} \tag{1.1}$$

The lattice constant a=$\sqrt{3}$ a$_{c-c}$, where a$_{c-c}$=0.142 nm is distance to the nearest neighbor atom. The reciprocal lattice vectors b$_1$ and b$_2$ are given by:

$$\vec{b}_1 = \frac{2\pi}{3a}\hat{k}_x + \frac{2\sqrt{3}\pi}{3a}\hat{k}_y, \quad \vec{b}_2 = \frac{2\pi}{3a}\hat{k}_x - \frac{2\sqrt{3}\pi}{3a}\hat{k}_y \tag{1.2}$$

To calculate the band structure of graphene, we frequently use the nearest neighbor tight binding approximation, in which the resultant dispersion relation can be expressed:

$$E_{\pm}(k_x, k_y) = \pm t_0 [1 + 4\cos(\frac{\sqrt{3}}{2}ak_y)\cos(\frac{3}{2}ak_x) + 4\cos^2(\frac{\sqrt{3}}{2}ak_y)]^{1/2} \tag{1.3}$$

(a)   (b)
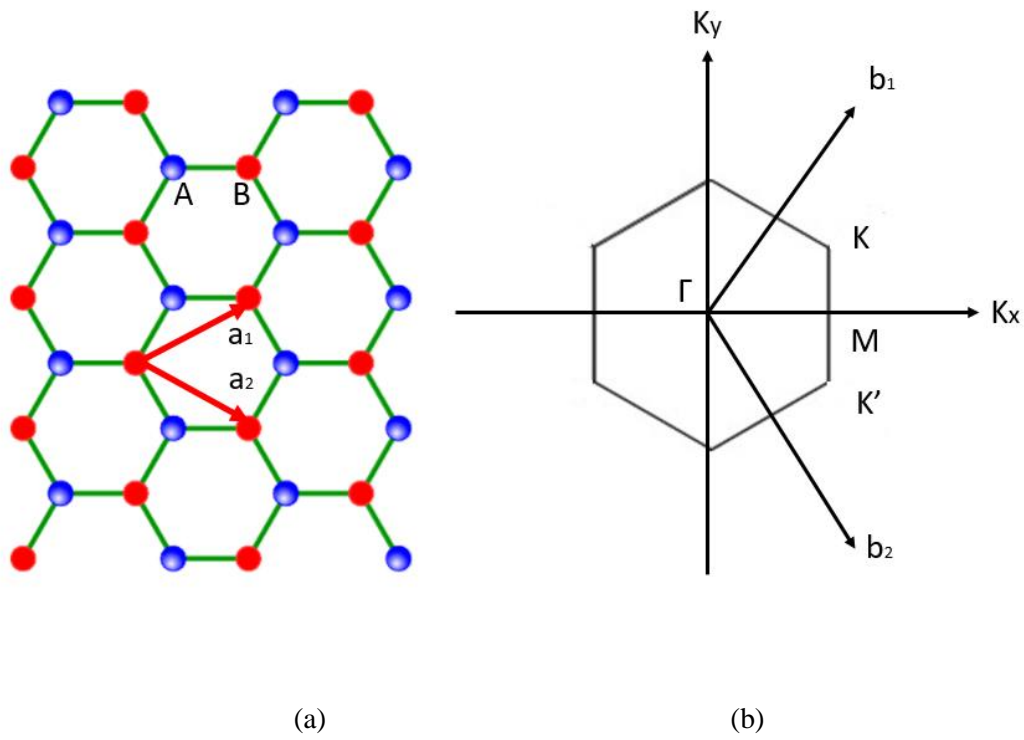
Figure 1.1 (a) Sub-lattice schematic of graphene. An A sub-lattice is surrounding by three B sub-lattice atoms. (b) The Brillouin zone of graphene.

where the ± corresponds to the valence and conduction bands, t_0 is the nearest neighbor hopping energy. In the Brillouin zone, the valence and conduction bands meet at symmetry $K = (\dfrac{2\pi}{3a}, \dfrac{2\pi}{3\sqrt{3}a})$ and $K^{'} = (\dfrac{2\pi}{3a}, \dfrac{2\pi}{3\sqrt{3}a})$ points which are called Dirac points. Figure 1.2 shows the band structure of graphene. From this figure, we can see that graphene is a zero bandgap semiconductor or semi-metal, the upper band forms the conduction band, while the lower band forms the valence band. They meet at Dirac points and near every Dirac point forms a valley. Near to the Dirac point, the liner relationship between energy and momentum can be expressed as follows:

$$E = \hbar v_F k = \hbar v_F \sqrt{k_x^2 + k_y^2} \tag{1.4}$$

where v_F is the Fermi velocity, and unique band structure of graphene gives a constant $v_F = 10^6$ m/s. The zero bandgap allows graphene easily changing from electron to hole through external voltage. The high mobility and ability to adjust the carrier density make the rapid growth in graphene investigations.

1.2.2 Quantum Hall Effect

Because the Dirac carriers move in circular cyclotron orbitals, graphene has uniform magnetic properties. Considering an x-y plane in which a uniform magnetic field in the z direction is applied, the Eigen energies are given by [7]:

$$E_l = \hbar \omega_c (l + \dfrac{1}{2}) \tag{1.5}$$
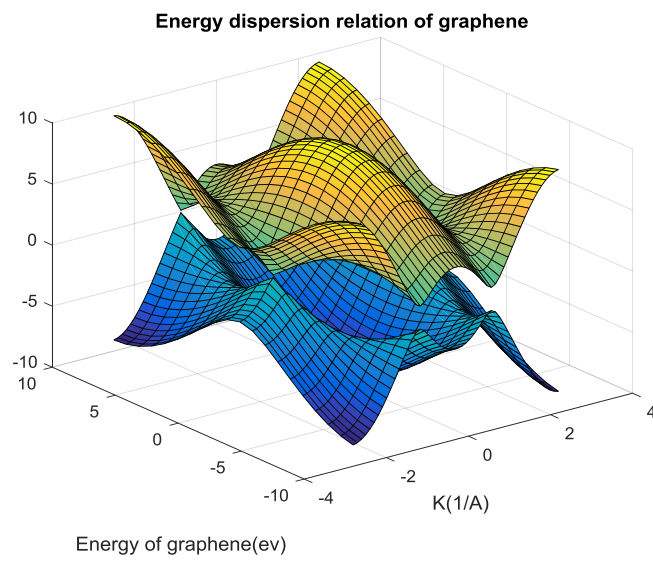
Figure 1.2 Graphene band structure calculated by using Matlab.

where ω_c is the cyclotron frequency. The major difference between graphene and conventional 2D systems is the existence of a Landau levels at zero energy (l=0) due to the massless Dirac fermions. When l=0, the degeneracy is half of that for any other l.

1.3   Optical Properties of Graphene

The optical image contrast of graphene can be identifies on top of SiO_2/Si substrate. The transmittance of single layer graphene is a constant which can be derived by the Fresnel equations with a fixed universal optical conductance $G_0 = e^2/4\hbar$. It can be expressed as [9]:

$$T = (1 + 0.5\pi\alpha)^{-2} \approx 1 - \pi\alpha \approx 97.7\% \tag{1.6}$$

where $\alpha = e^2/(4\pi\varepsilon_0\hbar c)$ is the fine structure constant. The thickness of a single graphene layer is 0.334 nm which obtains an absorption coefficient around $7*10^5$ cm^{-1}. This is 50 times higher than the absorption of gallium arsenide at 1.55 μm [10]. However, according to the Pauli principle, the interband transitions block the photon energies which are twice less than of the graphene Fermi level. This property gives a way for tuning the absorbance of graphene. The absorption of doped graphene can be extended into the terahertz ranges. Using heavy chemical doping in single layer graphene, the absorption can increase up to 40% in far-IR [11].

The optical excited charge carriers in graphene involve interaction between carrier-carrier and carrier-phonon scattering including intraband and interband transitions. The intraband transitions dominate at low photon energy, while the interband transition becomes important at high photon energy. The carrier-carrier interaction leads to an ultrafast thermalization of multiple carriers [12].

1.4   Application of Graphene Device

High carrier mobility and ballistic propagation properties in submicron scale are the most outstanding advantages as electronic devices for graphene. Furthermore, it differs from traditional materials. Graphene has stable electrical properties when reducing to few hexagon lattices. Finally, graphene is a two-dimensional lattice which is compatible with any substrate without lattice mismatch problem. These excellent physical properties allow graphene to have wide application in devices and circuits. In spite of electrical applications, graphene also can be used in optical application due to its unique optical properties. Because graphene has zero bandgap, it can absorb a wide energy spectrum from ultraviolet to infrared. The high carrier mobility and very short life time make graphene to be very useful in upper THz frequencies.

1.4.1   Graphene Electronics Application

Semiconductor electronics can be divided into two main areas: digital logic and radio frequency. The development and improvement of graphene and its devices are moving towards those two directions. Because the FET structure is a universal device structure, graphene devices always use this structure to prepare electronic devices.

Digital logic circuits need very high on/off current ratio (normally from 10^4~10^7), however, graphene has zero bandgap which results in low on/off current ratio and results in large leakage current. This is a major problem impeding graphene to be integrated in digital circuits. Currently, there are two main methods to open the bandgap: graphene nanoribbon [13], and double layer graphene with longitudinal electric field [14]. Graphene nanoribbon is one of the most popular structure, and the theoretical calculation shows that the bandgap is inversely proportional to the width of graphene nanoribbon. When the width of nanoribbon is less than 20nm, the bandgap can be more than 20 meV. However, in practical fabrication, it is difficult to get smooth edge, which

will reduce the bandgap. Furthermore, the relationship between energy and momentum near Dirac point will follow a parabola instead of linear, which increases the effective mass and reduces the carrier mobility of graphene. At present, the width of nanoribbon can be less than 5nm and the on/off ratio is larger than 10^8, but the carrier mobility is less than 200 cm^2/Vs [13, 15]. Such device characteristics are clearly inferior compared to the traditional Si based device, which limit the use of graphene nanoribbon. Double layer graphene doesn't have bandgap, but when applying longitudinal electric field, the k point in Brillouin zone will open a small bandgap. The size of bandgap depends on the strength of applied electric field, the bandgap can be larger than 200 meV under high electric field ($(1{\sim}3)*10^7$ V/cm) in theoretical analysis. IBM already uses this method to open the bandgap up to 130 meV, and the on/off ratio is 1000 under room temperature [16]. However, this on/off current ratio is still too small to implement robust digital logic. Although, to some extent, we have methods to open the bandgap of graphene, those methods not only destroy the original band structure reducing the carrier mobility but also can only obtain a small band gap. Instead of FET structure, a new graphene based device, graphene barristor, has been reported recently [17, 18]. It uses Schottky barrier formed by the graphene layer and the silicon substrate layer. The experiment result shows the possibility of using in logic device by achieving a high on/off ratio more than 10^7.

Meanwhile, radio frequency circuits do not need devices with high on/off current ratio. The most important indexes to evaluate the performance of the RF devices are cut-off frequency and maximum oscillation frequency, both of which are related to the carrier mobility. Besides, the two-dimensional structure of graphene lattice can inhibit the short channel effect to improve the performance of circuits. Currently, IBM demonstrates a graphene top-gated FET that has cut-off frequency of 280 GHz and maximum oscillation frequency of 35 GHz [19]. Based on the

development of RF devices, researchers also fabricate graphene RF circuits. The graphene common source amplifier exhibits 5 dB low frequency gain with the 3 dB bandwidth greater than 6 GHz [20]. However, this performance is still not as good as the traditional radio frequency devices based on HEMT (high electron mobility transistor). Due to the bipolar conductive properties of graphene, it doesn't have saturation characteristic which is hard to lift up the maximum oscillation frequency.

1.4.2   Graphene Optical Application

The conversion of electrical signals from light is very important for applications in opto-electronics. Photodetectors and photo-biosensors, have been developed based on the emerging materials and novel structures. However, there is a need for high performance over the broad range of wavelengths. The carrier mobility of graphene is larger than that of silicon since the carriers in graphene follow the linear relationship between the energy and momentum, which causes no bandgap [2]. On one hand, the property of zero bandgap is a major problem impeding graphene to be used in digital circuits because of the low on/off current ratio. On the other hand, this property has advantage in applications related to opto-electronics. Zero bandgap enables charge carriers to be generated by the light absorption over a wide energy spectrum from ultraviolet to infrared. Furthermore, graphene has ultrafast carrier dynamics, the high carrier mobility can make it to be used in microwave range [21]. These characteristics make graphene to be a competitive candidate for optoelectronic integrated circuits.

Various optoelectronic devices based on graphene have been investigated for integration such as plasmonic devices, photovoltaic modules and photodetector [22, 23]. In previous studies, the challenge of graphene-based photodetectors has been; how to separate electron-hole pairs effectively. Usually, the photodetectors using different Fermi levels of graphene interface have

been explored through experiments. In previous studies, the photocurrent response at graphene-metal contacting interface is explored by experiments [24, 25]. This phenomenon is based on the electronics transfer between graphene and metal electrode that shifts the Fermi level of graphene and forms build-in potential. The carriers excited by light can be separated by this electrical field thereby generating the photocurrent. Another mechanism which can be accomplished in graphene is photo-thermoelectric effect. This phenomenon is first identified in the interface between single and bilayer graphene interface [26]. The Seebeck coefficient difference between monolayer and bilayer graphene results in thermal current due to the temperature gradient. However, those experiments have limitations that the photocurrent can be only detected by using scanning electron microscopy since the photonic current only exists in limited area.

The photodetectors that were discussed before are all used in visible light range. However, owing to the high carrier mobility, graphene is a promising material for the development of Terahertz photodetectors. The THz photodetector based on traditional back gated bilayer graphene FET has been proposed [27]. Besides the photodetector, graphene can be also used in optical modulators which is used for manipulating the property of light. The Fermi level of graphene can be adjusted by gate voltage which results in its application as fast electro-absorption modulator. Although graphene has strong interaction with light, the absorption of light is still insufficient, the graphene couple with the silicon waveguide is used to improve the absorption with modulation of 0.1 dBμm^{-1} at wavelength of 1.35 μm [28]. A different structure of electro-optic modulation using photonic crystal nanocavity is proposed [29]. By tuning the Fermi level of the graphene layer, the modulation of cavity reflection can be up to 10 dB.

1.5   Research Accomplishments

The following three aspects of photonic effects in back-gate graphene field-effect transistor are examined in detail in this thesis.

1. The photodetector is based on back-gate graphene transistor.

2. The barristor and photodiode are based on graphene/silicon Schottky barrier and compatible model in SPICE.

3. Irradiation effect on back-gate graphene field-effect transistor.

The organization of this thesis is as follows: the first chapter introduces the background, structure and properties of graphene. It also discusses the applications of graphene, and proposes the purpose of this thesis. The second chapter discusses the preparation and characterization methods of graphene. It also analyzes the advantage and disadvantage of different methods preparing graphene sheet, and introduces the common methods of characterizing graphene properties. Using the NanoCVD in our laboratory, we fabricated the graphene sheet on a copper foil. Based on the graphene sheet, the back-gate graphene transistor is prepared and its current-voltage characteristics are measured. In the third chapter, photo-electronic current transport in a back-gated graphene field-effect transistor is studied. Under the light illumination, band bending at the metal/graphene interface develops a built-in potential which generates photonic current at varying back-gate biases. It is shown that the photo-electronic current consists of current contributions from photoelectric, photo-thermoelectric and photo-bolometric effects. In the fourth chapter, photodiode and barristor based on two-dimensional graphene, when a Schottky barrier formed between graphene layer and silicon substrate layer can be adjusted by the bias voltage, are proposed. Moreover, using analog behavior modeling method, the SPICE compatible models of graphene photodiode and barristor are developed which can be used in photonics integrated circuits

design. In the fifth chapter, the irradiation mechanisms is investigated, which is based on graphene back-gate transistor and quantitatively analyzes the irradiation influences on electrical properties of the device. The sixth chapter summarizes the main research results.

Part of the work is reported in following publications:

Ashok Srivastava, Xinlu Chen and Ashwani K. Pradhan, "Photo-electronic current transport in back-gated graphene transistor," in SPIE/NDE – SSN06: Nano-, Bio-, Info-Tech Sensors and 3D systems and 3D Systems, 25-29 March 2017, Portland, Oregon.

Ashok Srivastava, Xinlu Chen and Ashwani K. Pradhan, "A SPICE compatible model of graphene/silicon Schottky barrier photodiode," in 231st ECS Meeting, May 28 to June 1, 2017, New Orleans.

Xinlu Chen, Ashok Srivastava, Ashwani K. sharma and Clay Mayberry, "Irradiation effect on back-gate graphene field-Effect transistor," in SPIE/Defense+ Security: Sensors and systems for Space Applications X, 9-13 April 2017, Anaheim, California.

CHAPTER 2. FABRICATION OF GRAPHENE AND GRAPHENE BACK-GATE DEVICE

Geim and Novoselov first prepared graphene using mechanical exfoliation from graphite in 2004 [2]. Until now, there are three major methods to prepare a graphene sheet: mechanical exfoliation, chemical vapor deposition (CVD), and epitaxial growth on SiC. In this chapter, the advantages and disadvantages of these three methods and the illustration of the characteristic of graphene sheet are introduced. Based on the NanoCVD in our laboratory, we prepare the graphene sheet on a cooper foil, develop the transfer process to silicon oxide/silicon and fabricate back-gate field effect transistor.

2.1   Methods for Preparing Graphene

2.1.1   Mechanical Exfoliation

Mechanical exfoliation separates graphene layers from bulk graphite using mechanical force. This method uses the weak bonding between the layers in graphite and strong bonding in the hexagonal lattice to exfoliate the graphene sheets. It is very simple: stick graphite with a piece of scotch tape and cover with another piece of tape. Repeating this process, get thinner and thinner graphite layer. Finally, contact with the target substrate, and the sample of graphene can be obtained after removing the tape [2].

Unlike other methods which need expensive equipment, mechanical exfoliation only requires graphite, scotch tape, and silicon oxide/silicon substrate. The advantage of this method is easy to obtain high quality graphene sheet which has complete lattice and less defects. This kind of graphene has high mobility and is suitable to be used in laboratory research instead of preparing large area of graphene which can be used for large scale of semiconductor technology.

2.1.2   Chemical Vapor Deposition

Chemical vapor deposition (CVD) is the method in which gases are introduced into the deposition chamber that reacts and forms the desired film on the surface of the substrate. This technology is always used to produce high quality thin films with large area. This is the most widely used method in depositing graphene over transition metal (Ni and Cu) substrates, which is based on the hydrocarbon gas decomposing into carbon atoms at high temperature with transition metal as catalyst. The solubility of carbon in substrate decreases when temperature goes down, and the thin film of carbon is precipitated on the surface. Various kinds of hydrocarbons such as methane and ethylene can be used to decompose on different transition metal substrates, such as Cu, Ru, Ni and Pd [30].

We use Nano CVD-8G to prepare graphene on Cu substrate. The biggest area in this system is $2*4$ cm^2 which is enough for the research purpose. Figure 2.1 shows the graphene on Cu substrate prepared in our laboratory. The disadvantage of CVD is that graphene growth on Cu foil needs to transfer into silicon oxide/silicon substrate. During this process, defects and wrinkle can be introduced and reduce the quality of graphene film. Figure 2.2 shows the process of transfer graphene sheet from copper foil into silicon oxide substrate.

The transfer process can be described as follows: CVD grows double sides of the graphene on copper foil. In order to remove the copper substrate, firstly, we use nitric acid solution to wipe one side of graphene.

Figure 2.1 Graphene on copper foil prepared by NanoCVD in our laboratory.
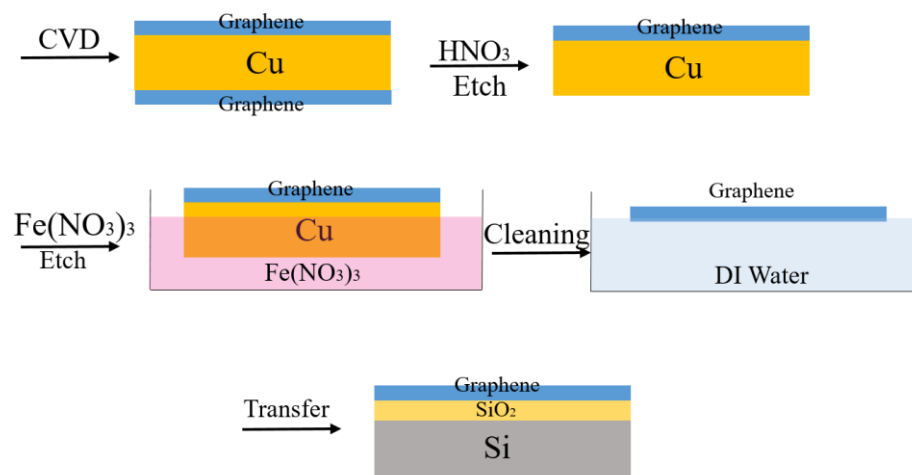
(a)

Figure 2.2 Process of transfer graphene from copper to silicon oxide/silicon substrate.

Secondly, prepare $Fe(NO_3)_3$ solution which can react with copper foil. After etching, the copper foil will be removed and graphene sheet will float on the solution. Using deionized water replaces the $Cu(NO_3)_3$ solution and cleans the graphene sheet. Finally, using silicon oxide/silicon substrate to get the graphene sheet out.

2.1.3 Epitaxial Growth of Graphene on SiC

Same as CVD, this method is also an efficient way to prepare large area and high quality graphene sheet. It heats the 6H-SiC substrate at Ar gas atmosphere until around 1000°C to remove the Si. The thickness of graphene depends on temperature [31]. The advantages of epitaxial graphene on SiC are that we don't need to transfer graphene sheet into isolated substrate and the size of graphene is as large as the substrate. However, SiC has two inequivalent terminations: Si face and C face [32]. Graphene growth on Si face has poor electronic properties, while on C face has good electric conductivity. Thus, the temperature and vapor pressure should follow strict requirements to guarantee that graphene is grown on C face. Besides, the SiC substrate is expensive and hard to compatible with CMOS technology.

2.2 Characterization of Graphene

Characterization of graphene is a significant part of graphene research. It includes determination of the number of graphene layers, the purity of samples and quality of graphene sheet. In this section, we introduce different methods to show the characterization of graphene.

2.2.1 Optical Microscopy

Optical microscopy is the easiest way to verify the number of graphene layers. In fact, we always use it for a quick thickness check before using more accurate methods like Raman spectroscopy. Using optical contrast between graphene and silicon oxide substrate, optical microscopy can illustrate different numbers of layers with different colors. However, the color

difference between single, double and a few layers of graphene is not very clear which need other characterization methods to distinguish. However, the visibility of graphene not only depends on the thickness of silicon oxide/silicon substrate, but also determines on the light wavelength. Under white light, we can only observe graphene sheet when the thickness of silicon oxide is 90-100nm and 270-330nm [33]. Optical microscopy method is easy but not accurate, and only can roughly determine the number of layers. Other characterization of graphene like defects should use other methods to illustrate.

2.2.2   Raman Spectroscopy

Raman spectroscopy is a spectroscopic method using a laser source which interacts with graphene. The light transmits to the graphene sheet, and the scattered light is collected with a system of lenses. Through the spectrophotometer we can get the Raman spectrum. In this process, graphene absorbs the photons from laser source and re-emits them with same and different frequencies. When the photons from a laser beam interact with material atoms which can be treated as the center of scattering, only a very small number of photon's frequency will change. This process is called Raman scattering, while the most of the photons only change the direction and the frequency remain the same, which is called Rayleigh scattering.

In graphene's Raman spectrum, the most common modes we can observed are G peak at 1580 cm^{-1}, 2D peak at 2700 cm^{-1}, D peak at 1350 cm^{-1}, and G* peak at 2450 cm^{-1}. According to the vibrational character, the G peak is correspond to the in plane vibration of sp^2 carbon atoms. The resonant processes of G peak is described as follows: the electrons at Γ point are excited by the incident photon from valence band to conduct band. These photonic excited electrons will be further scattered by phonon and back to valence band by emitting scattered light. The strength of G peak is dependent on the layer of graphene. According to the experiment results, when less than

10 layers, the strength of G peak increases linearly as the number of layers. With more than 10 layers, the strength decreases with the increase of layers' number [32]. This phenomenon results in the multiple scattering between graphene and SiO_2 substrate. D peak is related to the defects of graphene. For perfect graphene lattice, D peak does not exist. Thus, the defects dimension can be expressed by the ratio of intensity of D peak and intensity of G peak (I_D/I_G) [33]. In Raman spectra of graphene, the strongest peak is near 2500~3000 cm^{-1}, which is called 2D peak. The 2D peak is a double resonance Raman scattering and corresponds to the overtone of the D band. The intensity of 2D peak is highly influenced by the number of layers of graphene, which decrease with the increase of the number of layers [32]. Figure 2.3 shows the Raman spectrum on one fabricated film and transformed to the SiO_2/Si substrate.

2.3 Graphene Back-Gate Transistor

In this sub section, we introduce the basic principle of graphene back-gate transistor and explain the unique electrical mechanisms of graphene device. Figure 2.4 shows the cross section of graphene back-gate device. Heavily doped Si is the back gate and SiO_2 as back gate dielectric. The gate voltage controls the conduction type of graphene channel.

2.3.1 Carrier Density of Graphene

Because graphene has zero bandgap, near the Dirac point, it follows the linear relationship between energy and momentum. The low field transport calculation is given by:

$$E(\vec{k}) = \hbar v_F \left| \vec{k} \right| \tag{2.1}$$

where $\hbar$ is the reduced Planck constant, $v_F = 10^6$ m/s is the Fermi velocity of graphene. In this kind of band structure, the density of state can be expressed by [34]:
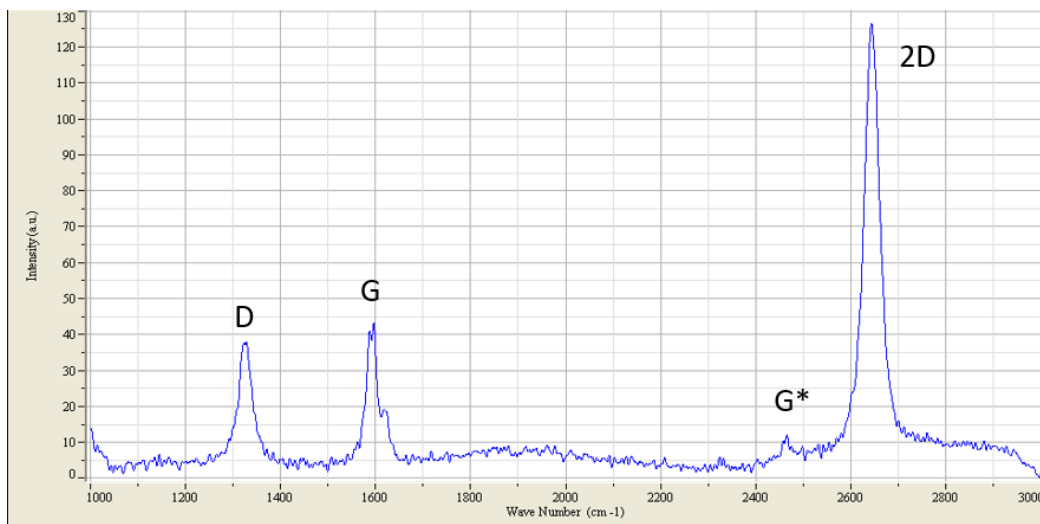
Figure 2.3 Intensity of Raman spectrum of graphene fabricated by our laboratory.
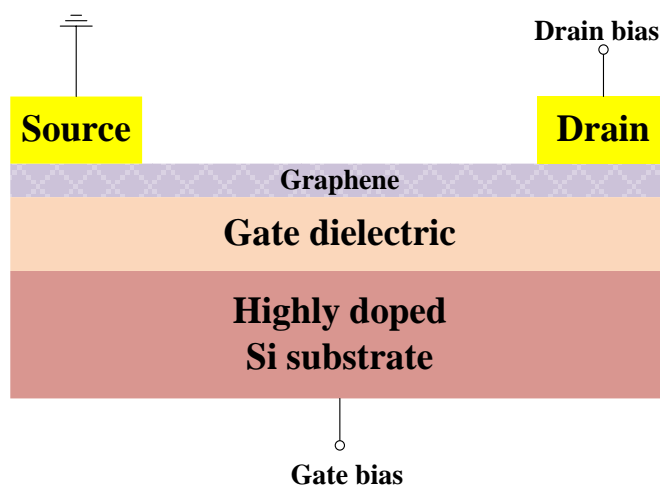
Figure 2.4 Cross view of graphene back-gate field-effect transistor.

$$D(E) = \frac{g_s g_D}{2\pi} \frac{|E|}{(\hbar v_F)^2} \tag{2.2}$$

where a 2 is for the spin and 2 for valley degeneracy. Combining with the Fermi-Dirac distribution function f(E), the density of electrons and holes are given by:

$$n = \int_E^\infty D_C(E) f(E) dE = \frac{2}{\pi(\hbar v_F)^2} \int_0^\infty \frac{E}{\exp(\frac{E - E_F}{k_B T}) + 1} dE \tag{2.3}$$

$$p = \int_{\infty}^E D_C(E)[1 - f(E)] dE = \frac{2}{\pi(\hbar v_F)^2} \int_0^\infty \frac{E}{\exp(\frac{E + E_F}{k_B T}) + 1} dE \tag{2.4}$$

where E_F is the Fermi level of graphene sheet and k_B is Boltzmann constant. At zero temperature, the calculation of carrier density leads to the following:

$$n - p = \frac{2}{\pi(\hbar v_F)^2} (\int_0^\infty dEE(1 - step(E - E_F)) - \int_0^\infty dEE(1 - step(E + E_F))) \tag{2.5}$$

Finally, we can get

$$|n - p| = \frac{E_F^2}{\pi(\hbar v_F)^2} \tag{2.6}$$

2.4   Fabrication of Graphene Back-gate Transistor

We deposit graphene and transfer to SiO_2/Si substrate, the thickness of silicon oxide is 300nm. Depositing metal electrodes on graphene requires microelectronic photolithography. During the photolithography process, the residual photoresist remains on graphene sheet. Due to the strong adsorption of graphene, the residue of photoresist is even more serious.
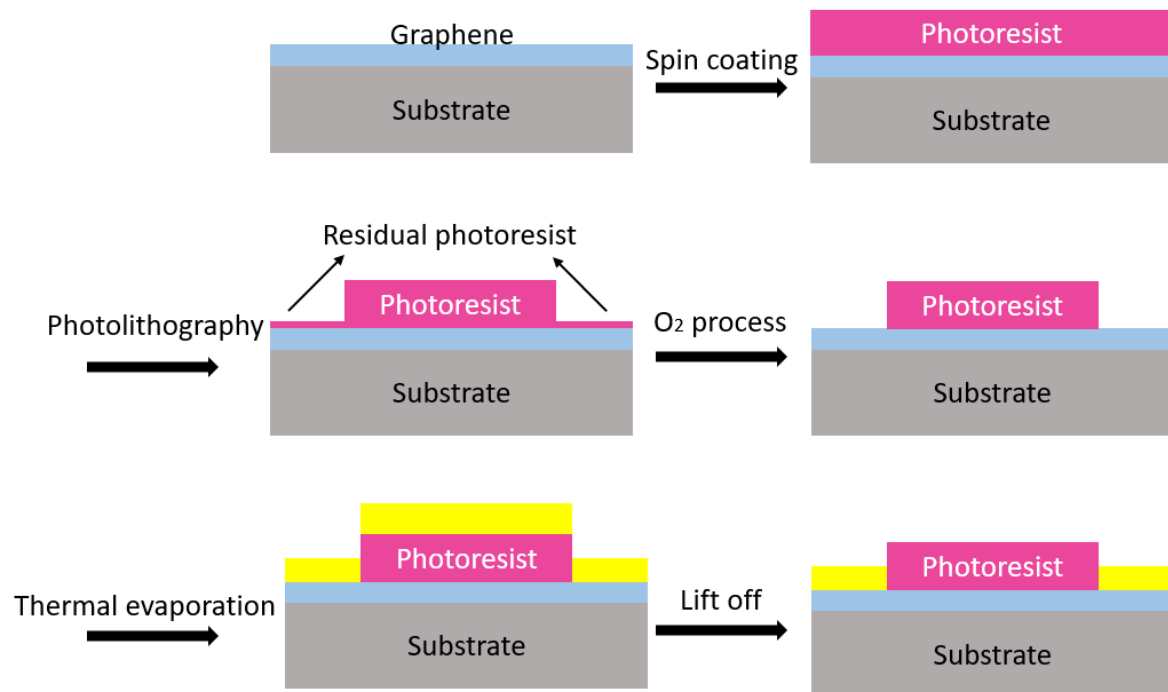
Figure 2.5 Process of using O_2 removing the residual photoresist.
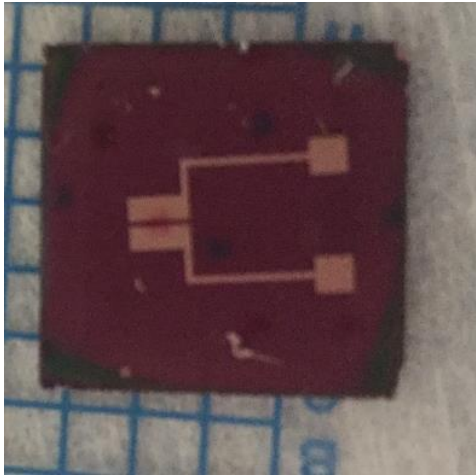
Figure 2.6 Back-gate transistor based on graphene.

The presence of residual photoresist inhibits the contact between metal and graphene, which increases the scattering of carriers during the process of interface transport. Usually, we use O_2 bombardment method to remove the photoresist which can decrease the contact resistance. Figure 2.5 shows the process of using O_2 removing the residual photoresist. To deposit the metal, we use the thermal evaporation method. Thermal evaporation is a common method of depositing thin films which allows vapor particles to travel directly to the target. In our laboratory, aluminum is deposited on the top of graphene as shown in Figure 2.5. See Appendix-A for the summary of fabrication process.

The electrical testing of the device is carried out in the air at room temperature. Figure 2.7 shows the transfer characteristics of graphene back-gate transistor. This curve illustrates obvious ambipolar conduction characteristics. When V_d=2V, the Dirac voltage (V_{Dirac}) is 2V. As the drain voltage increase, the Dirac voltage shifts to the right. This phenomenon is easy to understand: for intrinsic graphene, the number of holes injected into graphene increases through drain electrodes, which decrease the Fermi level. To restore the intrinsic state, it needs apply corresponding gate voltage, which results in the movement of Dirac voltage. Using Dirac points as differentiated points, the left branch is hole conduction, while the right branch is electron conduction. Figure 2.8 shows the output characteristic of graphene back-gate transistor. It differs from the traditional silicon FET. Our device doesn't have obvious saturation trend. Current and drain voltage follow the linear relationship. This is because graphene has zero bandgap.
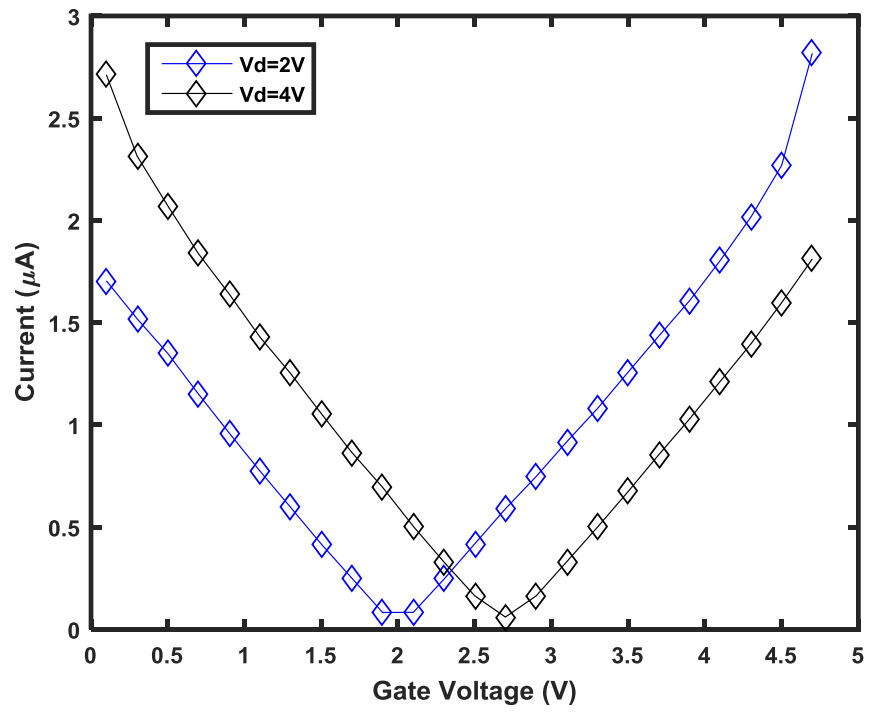
Figure 2.7 Transfer characteristics graphene back-gate field-effect transistor.
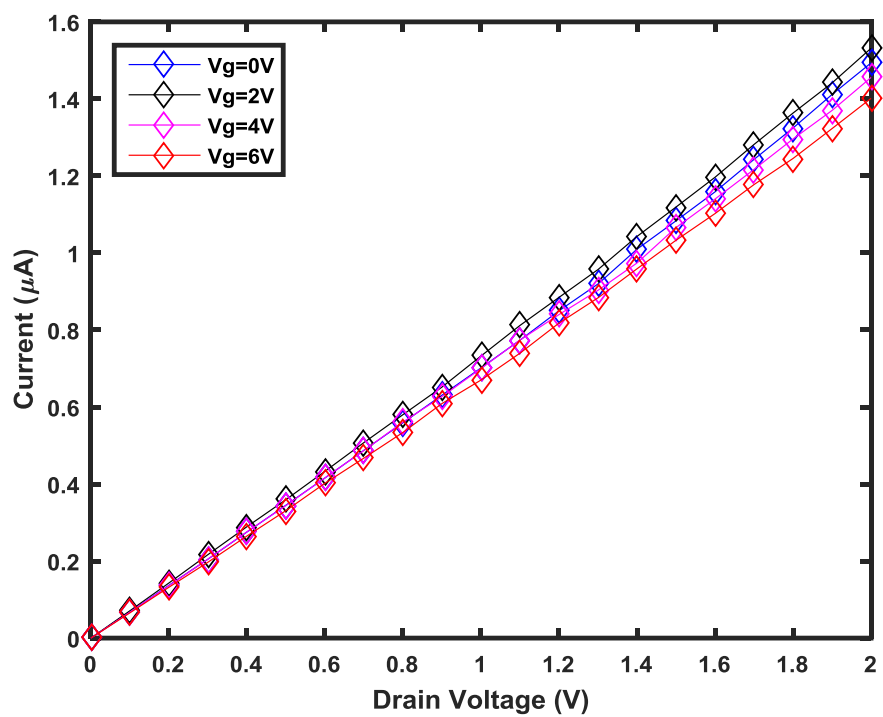
Figure 2.8 Output characteristics graphene back-gate field-effect transistor.

CHAPTER 3. PHOTO-ELECTRONIC CURRENT TRANSPORT IN BACK-GATE GRAPHENE TRANSISTOR

Although the property of zero bandgap is a major problem impeding graphene to be used in digital circuits because of the low on/off current ratio, this property has advantage in applications related to optoelectronics. In this chapter, we present theoretical analysis and computed photo-electronic current in a back-gated graphene field-effect transistor. It is shown that the photo-electronic current consists of current contributions from photovoltaic, photo-thermoelectric and photo-bolometric effects. For the photo-electronic transport, we use the quantum model based on Landauer approach [35] to study the transportation property of the transistor and computed the photocurrent for different laser wavelengths and powers.

3.1   Structure of Graphene Photodetector

The cross section view of a graphene photodetector is shown is Figure 3.1. It can be seen that a typical MOSFET type back-gated transistor structure uses a monolayer graphene as a channel over the silicon dioxide/silicon substrate and Ti/Pd forms source and drain electrodes. The adjustable gate voltage is applied on the silicon substrate, while the source is connected to ground and drain bias is varied. The thickness of silicon dioxide is 300 nm and the graphene channel in this device is 0.6 μm wide and 1.45 μm long. The incident excitation laser power is about 30μW and the wavelength is 633 nm which focuses on the source. The device can be separated into three regions. The region I is the metal controlled.
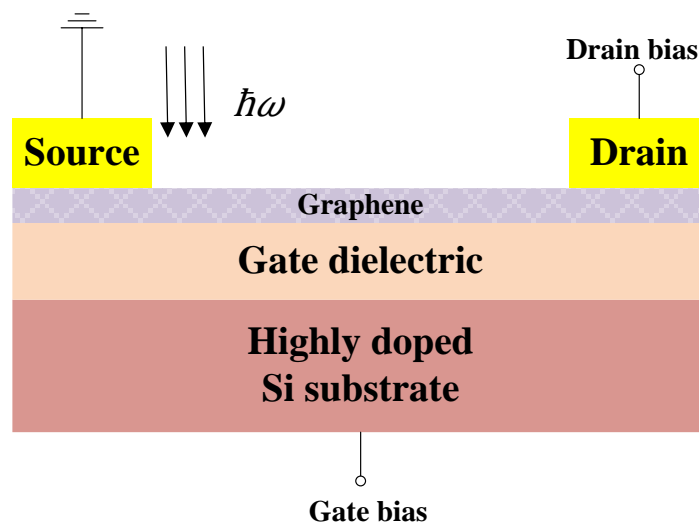
Figure 3.1 Cross section view of a graphene photodetector.
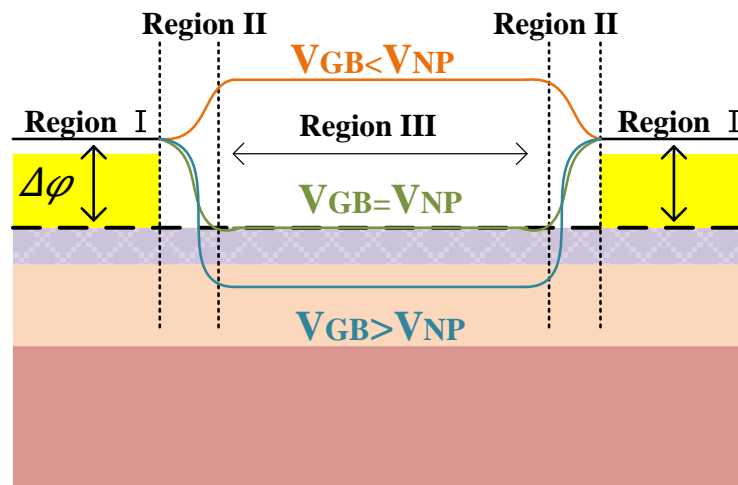
Figure 3.2 Energy band diagram under different gate bias voltages.

When metal contacts with graphene, the Fermi level of graphene is shifted due to the electrons transfer between the graphene and metal forming a built-in potential at the interface [36]. In this region, we can ignore the effect of gate voltage. Region II is the transition region forming the built-in potential. Region III is the graphene channel controlled by the gate voltage. In this region, the gate voltage controls the shift in Fermi level and it can be calculated using the capacitor model [37]. The energy band diagram under the gate voltage variation is shown in Figure 3.2. In this figure, $\Delta\varphi$ is the change in Fermi level after graphene is contacted by the metal which forms a Schottky contact characterized by its barrier height at the metal semiconductor contact. V_{GB} is the back-gate bias, V_{NP} is the neutrality point of the device and $\hbar\omega$ is the photon energy of the laser source. Figure 1 (b) illustrates that when $V_{GB}>V_{NP}$, it forms a p-n junction and when $V_{GB}<V_{NP}$, it forms a p-p$^+$ junction. For ease in calculation, we define $V_G=V_{GB}-V_{NP}$ since different technologies and fabrication methods cause different device neutrality points and this effect should be minimized in theoretical analysis.

3.2 Photo-electronic Current Transport in Photodetector

3.2.1 Photovoltaic Effect

Photovoltaic effect is based on the separating photo generated electron-hole pairs using the built-in potential at differently doped graphene junction interface. In previous studies [38], the photovoltaic effect was observed in graphene p-n junction doped by chemical and electrostatic methods. In this work, we have used band bending at the metal/graphene interface forming the built-in electrical field. When photons are absorbed by graphene and excite electron-hole pairs, these are separated and propelled by the built-in electric field in Region II shown in Figure 3.2 which is determined by the difference in Fermi levels in Region I and Region III. In our device, $\Delta\varphi$ is fixed around 0.1eV because we have used Titanium/Palladium as the source and drain

electrodes. However, the Fermi level of graphene can be changed in Region III due to varying back-gate bias. The capacitor model can be used to calculate the variation of Fermi level, $\Delta E = \hbar v_F \sqrt{\pi C_g V_g / q}$, where ħ is the reduced Planck constant, v_F is the Fermi velocity of graphene, C_g is the gate capacitance which is related to the thickness of oxide silicon. $V_G = V_{GB} - V_{NP}$ is the difference between actual back gate bias and device neutrality point voltage and q is the electron charge. Thus, this mechanism can switch from p-n to p-p$^+$ junction.

In this phenomenon, photons create electron-hole pairs, providing additional conductance in the device channel. When graphene absorbs photons, the electrons are excited into a high energy level which create additional carriers for the electric current. The photo-generated carriers driven by the gate induced electric field can be calculated by the optical conductance of monolayer graphene as follows:

$$I_{ph} = \gamma A q \mu \Delta n E = \gamma A \Delta \sigma E \tag{3.1}$$

where γ is the internal quantum efficiency and A is the cross section area of active layer. The change in conductance is Δσ=Δnqμ where Δn is the photo-excited charge density determined by the incident laser and E is the electrical field discussed above. Optical conductivity can be used in describing Δσ. Previous study on the optical conductivity of pure graphene sheet uses the model of interband optical conductivity [39]. However, in our device where graphene channel has the gate bias, the quantum conductance cannot be used correctly. Thus, the change of conductivity resulted from the photon is shown to follow [40]:

$$\Delta\sigma(\omega) = \sigma\left(\frac{1}{72}\frac{(\hbar\omega)^2}{(t)^2}\right)*\left(\tanh\frac{\hbar\omega+2E_F}{4kT} + \tanh\frac{\hbar\omega-2E_F}{4kT}\right) \tag{3.2}$$

where σ is the conductivity of graphene device, ꞷ is the angular frequency of laser, t is the hopping parameter connecting first-nearest neighbor and E_F is the Fermi level of graphene under the gate bias. To calculate the conductivity of graphene at different gate biases, there are many methods. The first one is from the semiconductor physics view that is usually used in experiment-based analysis. This method has many fixed parameters and can be used in fitting with real device current curve. However, this work is a pure theoretical analysis. We can use the second method which is from quantum considerations of the graphene device. Compared to semiconductor physics method, quantum method is based on the number of modes and transmission coefficient for the channel to conduct charge carriers and drain current. The number of modes in a channel defined by Landauer expression over k space is as follows [35]:

$$M(E) = \sum_{k} \delta(E - E(k)) \frac{\pi \hbar}{L} |v_x(k)| \tag{3.3}$$

where L is the length of graphene, E(k) is the graphene dispersion relation, v_x (k) is the group velocity in transport direction and E is the energy range of calculating transverse modes. This energy range is used as the back-gate voltage which controls the energy window and number of modes can be calculated. The number of conducting channels at a fixed energy range is determined by the width of device. Besides, the band structure of conductor also affects the number of modes. Thus, in this work, the number of modes can be expressed as $M(E) = \frac{W}{\pi} \frac{|E|}{\hbar v_F}$, where W is the width of graphene channel. Another effect determining the current is the transmission coefficient. The channel length of our device is 1.4 μm so that we should take scattering into consideration.
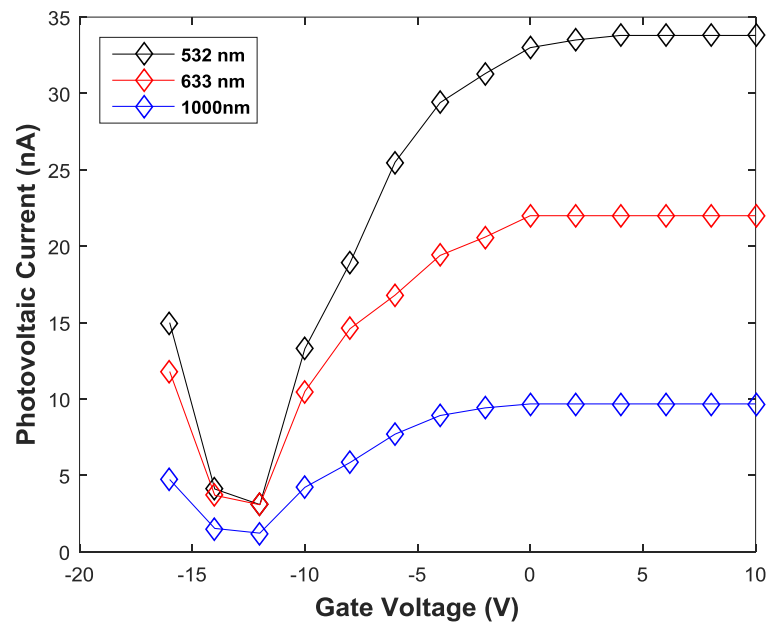
Figure 3.3 Photovoltaic current under different frequency.

Thus, the transmission coefficient is expressed as: $T = \dfrac{\lambda}{\lambda + L}$, where λ is the mean free path.

Considering source and drain Fermi-Dirac statistics in Landauer formalism, the conductivity can be calculated as follows:

$$\sigma = \frac{L}{W}\frac{2q^2}{h}\int dE M(E)T(E)(-\frac{\partial f_0}{\partial E}) \tag{3.4}$$

Where $-\dfrac{\partial f_0}{\partial E} = \dfrac{e^{(E-E_F)/kT}}{(1+e^{(E-E_F)/kT})^2}$, written in equation (3.4) as derivative of the Fermi function with

opposite signs for E_F and using integration by parts, we can obtain,

$$\sigma = \frac{L}{W}\frac{2q^2}{h}\frac{2W}{\pi \hbar v_F}T(\int_0^\infty dE \frac{1}{1+e^{(E+E_F)/kT}} + \int_0^\infty dE \frac{1}{1+e^{(E-E_F)/kT}}) \tag{3.5}$$

According to equations (3.1) and (3.2), the photovoltaic current depends on the frequency of laser source. The generated photocurrent decrease with the increase of wavelength. In Fig. 3.3, we calculated the photovoltaic current at three different wavelength: 532nm, 633nm, and 1000nm. In Fig. 3.2, when $V_G > 12V$, the direction of photocurrent is from drain to source while for $V_G < 12V$ the direction is from source to drain. Besides, another important phenomenon should be taken into account is the saturation. This is motivated by the fact that when the built-in electrical field is large enough, the mobility of all the carriers will reach to the saturation.

3.2.3 Photo-thermoelectric Effect

In spite of photovoltaic effect, another significant phenomenon in contributing to the photocurrent is photo-thermoelectric effect which is introduced by the light illumination. This phenomenon has been first described in monolayer/bilayer graphene junction due to hot carriers [7]. In our device, graphene absorbs photons, exciting electron-hole pairs in Region II near the source terminal. Due to strong electron-electron interaction, excited electron-hole pairs by the

photon heat the carriers which is also called as hot carriers in graphene channel. Because the optical phonon energy is large, hot carriers created by the laser source radiation keep the temperature higher than that of the lattice [41]. Thus, in this thermoelectric effect, laser radiation source creates a temperature gradient ΔT in graphene junction interface. This thermal generated current can be expressed as follows:

$$I_{PTE} = \frac{(S_2 - S_1)\Delta T}{R}$$
(3.6)

where R is the resistance, S_1 and S_2 are the thermoelectric power (Seebeck Coefficient) in Region I and Region II, respectively, which are varied by different gate biases. This parameter can be expressed as follows [26]:

$$S = \frac{\pi^2 k^2 T}{3q} \frac{1}{G} \frac{\partial G}{\partial V_G} \frac{\partial V_G}{\partial E}\bigg|_{E=E_F}$$
(3.7)

where k is the Boltzmann constant and G is conductance which can be calculated using equation (3.5). The Seebeck Coefficient, S at various gate voltages is shown in Figure 3.4. The temperature gradient can be calculated by treating laser source as a radiation wave that delivers the heat flow in the Region II. The difference of temperature with laser and without laser radiation is expressed as $k_T 2\pi d\Delta T = P\alpha$, where k_T is the thermal conductivity of monolayer graphene which has been reported as 5×10^3 W/m*K at room temperature, d is the thickness of graphene that is 3Å, P is the power of incident laser source and α is the absorption coefficient of monolayer graphene [26].

The temperature gradient can be calculated by treating laser source as a radiation wave that delivers the heat flow in the Region II.
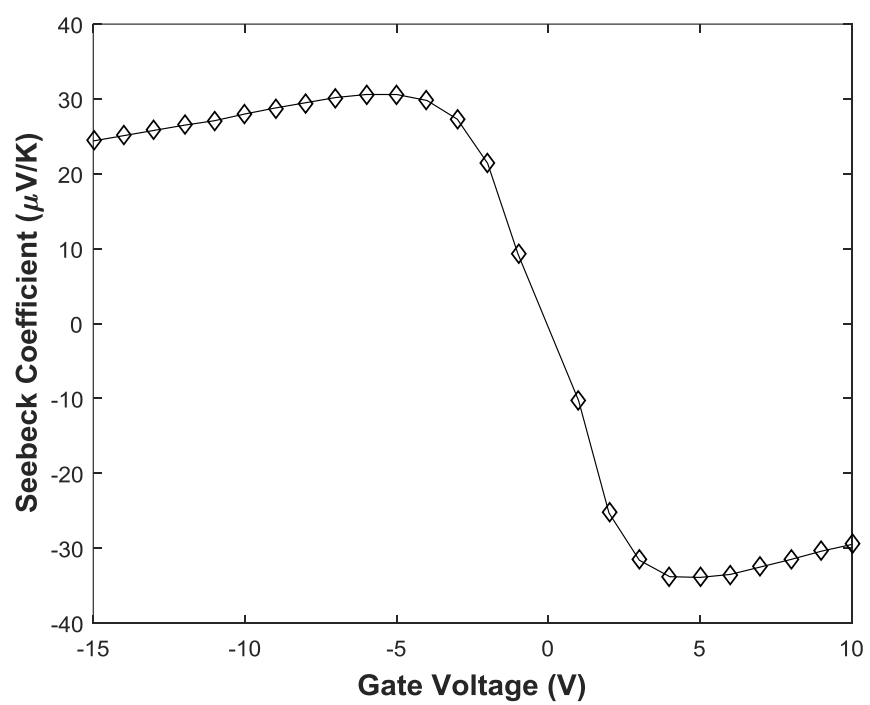
Figure 3.4 Seebeck Coefficient (S) at various gate voltages.
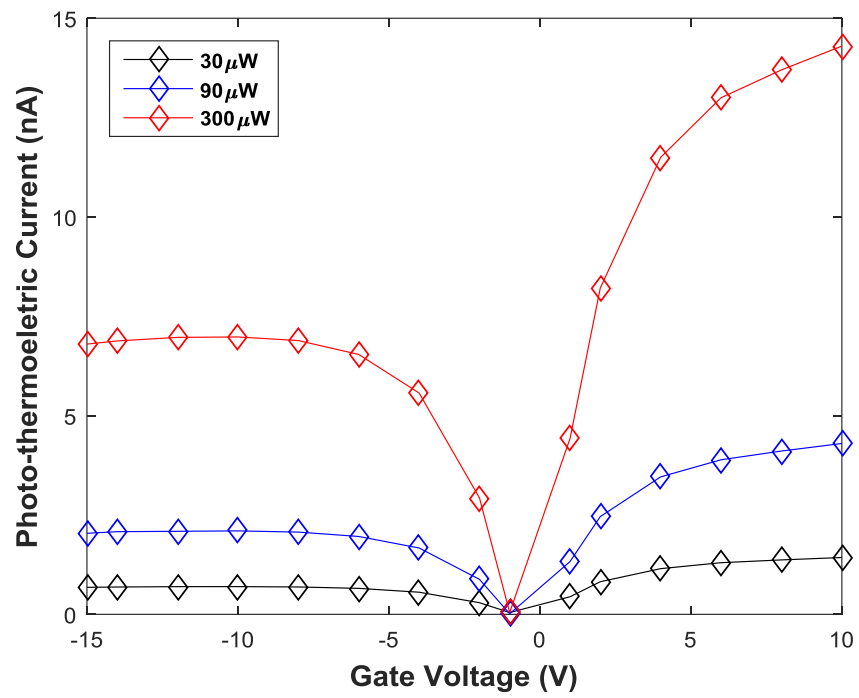
Figure 3.5 Photo-thermoelectric current at different powers of laser: 30µW, 90 µW and 300 µW.

The difference of temperature with laser and without laser radiation is expressed as $k_T2\pi d\Delta T=P\alpha$, where k_T is the thermal conductivity of monolayer graphene which has been reported as 5×10^3 W/m*K at room temperature, d is the thickness of graphene that is 3Å, P is the power of incident laser source and α is the absorption coefficient of monolayer graphene [26].

Figure 3.5 shows the amplitude of photo-thermoelectric current at different powers of the laser source. According to the computed results, under low laser power source, this effect is small, while in high laser power source, it becomes noticeable. The direction of thermoelectric current is determined by the built-in electric field in Region II. When the junction is p-n, the sign of this current is the same as that of the photovoltaic effect, while in some unipolar junction, like p-p$^+$ and n-n$^-$ junction, the sign is reversed.

3.2.3   Photo-bolometric Effect

Photo-bolometric effect is another mechanism responsible for the photocurrent of graphene photodetectors. This phenomenon is related to the change in the transport conductance when exposed to a laser source. Bolometers are used to measure the change in temperature due to the change of power after absorbing incident radiation. The traditional bolometers are mainly made by the superconductor and semiconductor which can be utilized in THz wavelength range [42]. Considering the bolometric effect in graphene, which has unique thermal properties, such as the hot carrier effect, electron-photons-decay bottleneck and small electronic specific heat cause this mechanism [10]. The photo-bolometric effect is determined by measurement of the temperature change. This change can be calculated by the change in transport mechanism. Thus, the photo-bolometric response of graphene photodetector should only be observed in biased transistors, which can be ignored in other unbiased photodetectors. The current and temperature depending on photo-bolometric effect, voltage can be expressed by the equation [43]:

$$\Delta V_{phb} = I_{ds} \frac{\partial R}{\partial T} \Delta T \qquad (3.8)$$

where I_{ds} is the biased current, ΔT is the change of electron temperature due to photon absorption which can be also calculated by treating laser source of radiation wave, and $\frac{\partial R}{\partial T}$ is the temperature derivative of the resistance. The reason of resistance change in this effect is that scattering increases due to temperature rise. According to the experiment proposed by Shao et al. [44], the linear temperature-dependent correlation of the resistivity is shown by, $R_T = R_0[1 + \alpha(T - T_0)]$, where α is the temperature coefficient of resistance. At low temperature, the Coulomb scattering is dominant, while at room temperature, the Coulomb scattering mechanism does not contribute to this change. In graphene, such a change in resistance is due to electron-phonon scattering due to increase in temperature. For our device modeling, we calculated the biased current at different temperatures and calculated the change in resistance. The bias current I_{ds} can also be calculated by Landauer formalism as follows:

$$I_{ds} = \int dE G(E)(f_S(E) - f_D(E)) \qquad (3.9)$$

where $f_S = \dfrac{1}{1 + e^{(E - E_f^S)/kT}}$ and $f_D = \dfrac{1}{1 + e^{(E - E_f^D)/kT}}$ are the Fermi levels corresponding to source and drain.

Figure 3.6 shows the current-voltage characteristics of graphene transistor and Fig. 3.7 shows the normalized resistance of our device as a function of temperature comparing with the experiment data in [44]. According to the results, the temperature derivative of the resistance is $\frac{\partial R}{\partial T} = 11.73$.
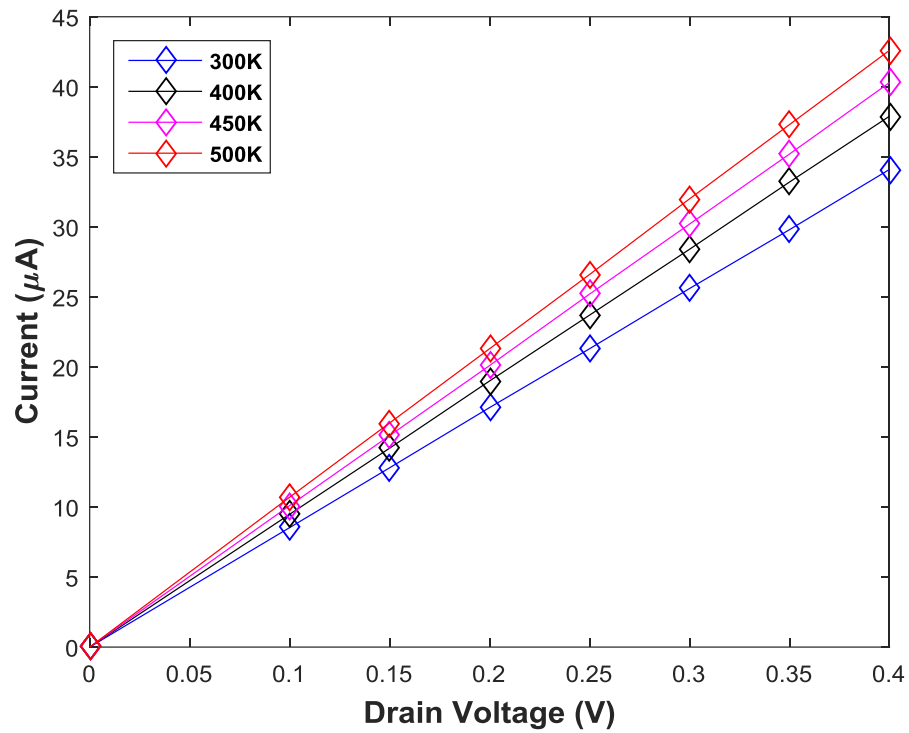
Figure 3.6 Current-voltage characteristics of graphene transistor at different temperature.
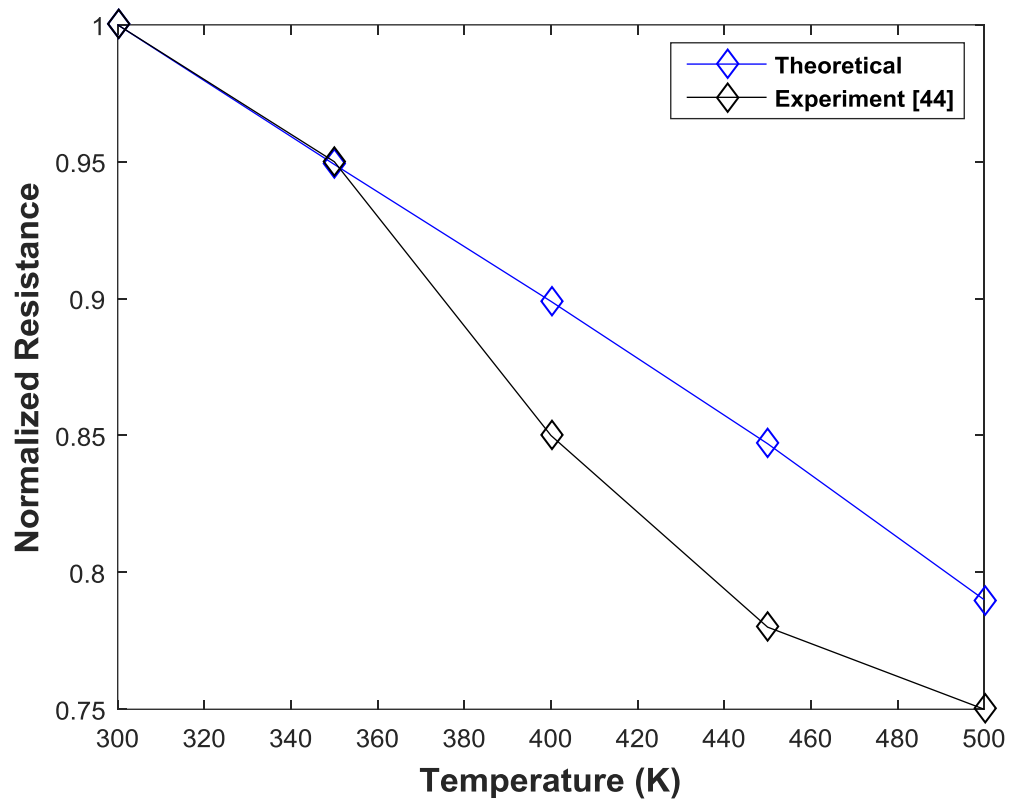
Figure 3.7 Normalized resistance of our device as a function of temperature.
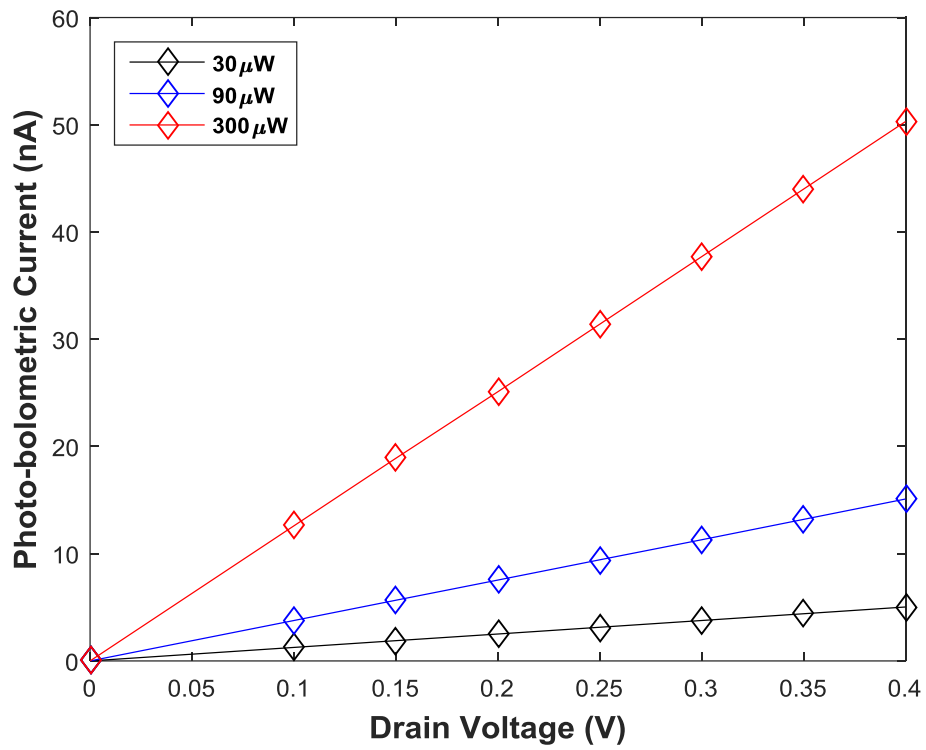
Figure 3.8 Photo-bolometric current at different laser power: 30μW, 90 μW, and 300 μW.
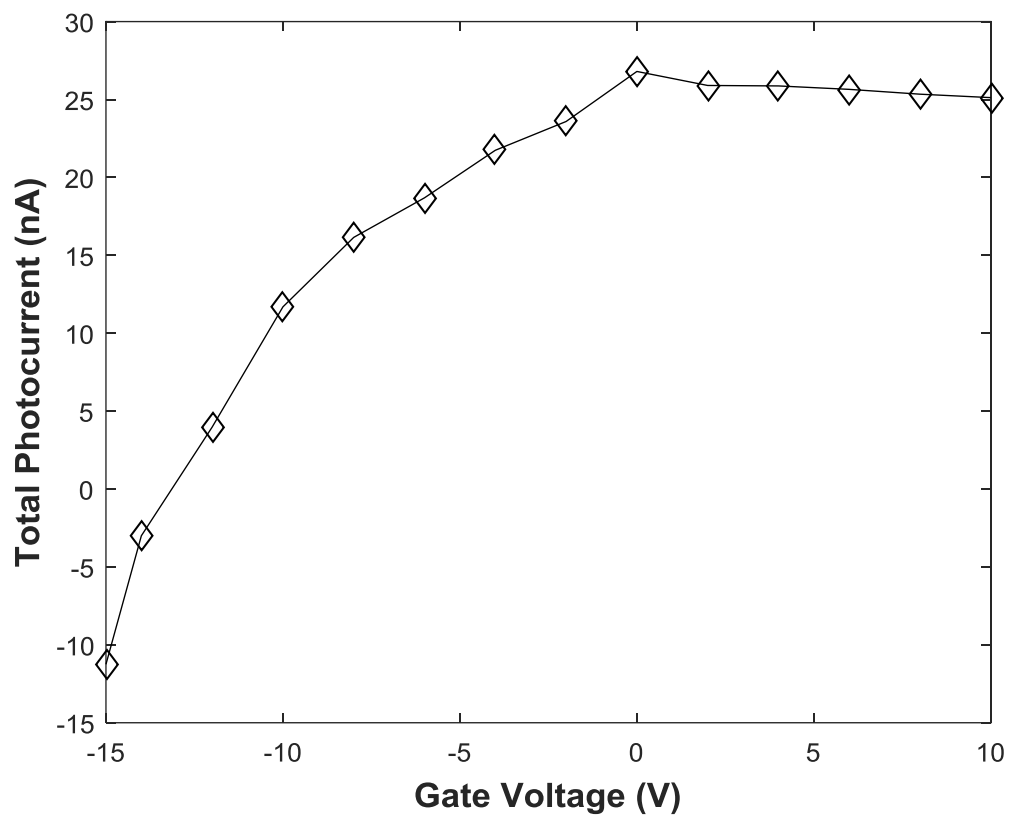
Figure 3.9 Total photocurrent of device for V_{DS}=0.4V for 633nm wavelength and 30µW laser power.

Combining those parameters together, the photocurrent generated by the bolometric effect can be express as, $I_{phb} = \dfrac{V_{phb}}{R}$. Figure 3.8 shows the photo-bolometric current for the fixed gate bias, $V_G=0V$ and sweep drain bias from 0.1 to 0.4 V for different powers of the laser source. Corresponding wavelength is 633nm and power is 30μW, 90 μW, and 300 μW, respectively.

Combining all three effects discussed above together, we computed total photo generated current for the 633nm wavelength and 30μW power of laser source. Figure 3.9 shows the total photocurrent as a function of gate bias. In Fig. 3.9, the negative photocurrent means the direction is from source to drain. Calculating the external responsivity (I_{photo}/P_{laser}), the maximum is 0.0009A/W.

3.3   Conclusion

In summary, we have developed a photocurrent model based on back-gated monolayer graphene field-effect transistor on silicon dioxide/silicon substrate. The results are consistent with the models of photovoltaic effect and contributing currents generated using the built-in electrical field at the graphene junction interface, photo-thermoelectric effect, where thermoelectric current is formed because of the elevated temperature at the junction by the absorbing laser power, and the photo-bolometric effect, where bolometric current is due to applied drain bias. We also discussed the influence of those effects for different powers of the laser source corresponding to 633nm wavelength. We concluded that the photovoltaic current decreases with the increase of wavelength. At low laser power, the photo-thermoelectric and photo-bolometric effects become negligible. However, at high laser power and applied large drain bias, these two effects play a significant role and cannot be ignored.

CHAPTER 4. MODELING OF BARRISTOR AND PHOTODIODE BASED ON GRAPHENE/SILICON SCHOTTKY

In this chapter, we propose new kind of graphene devices: barristor and photodiode, which are based on Schottky barrier between graphene and silicon substrate. This barrier height can largely widen the bandgap so that the device can be used for digital logic. We have used analog behavior modeling in SPICE to model the graphene barristor and photodiode. The analog behavior modeling method can adjust dynamically each current in the device according to the variation of voltage.

4.1   Graphene/Silicon Schottky Photodiode

There are reported experiment work on the graphene/silicon junctions and its photo response [45, 46] which is based on the light excited carriers separated by the electrostatically adjustable Schottky barrier junction. In this work, we present an analysis of the carrier transport model of graphene/silicon Schottky barrier photodiode under a variable bias voltages. We have discussed the change of Schottky barrier height between graphene and silicon due to the bias voltage and analyzed its performance for the dark current and photocurrent at room temperature. An equivalent circuit model compatible with SPICE is proposed for generating photo response characteristics. We have used the analog behavior modeling in PSPICE to describe the behavior of graphene Schottky photodiode from its equivalent circuit.
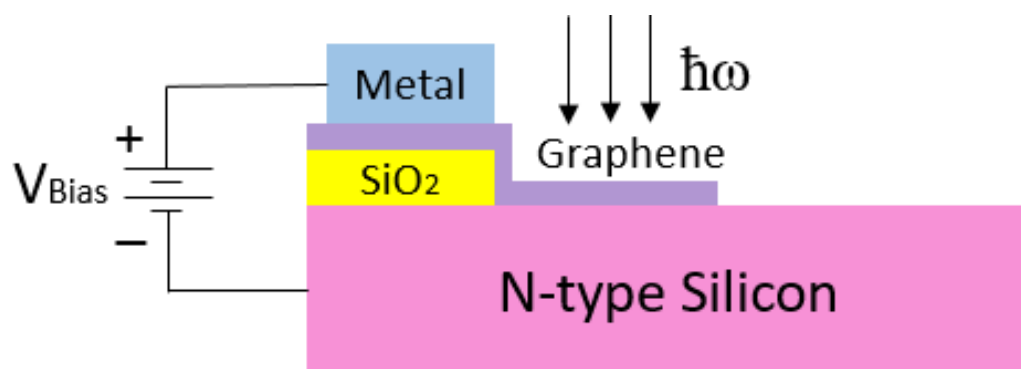
Figure 4.1 Schematic diagram of Schottky photodiode based on graphene/n-type silicon.
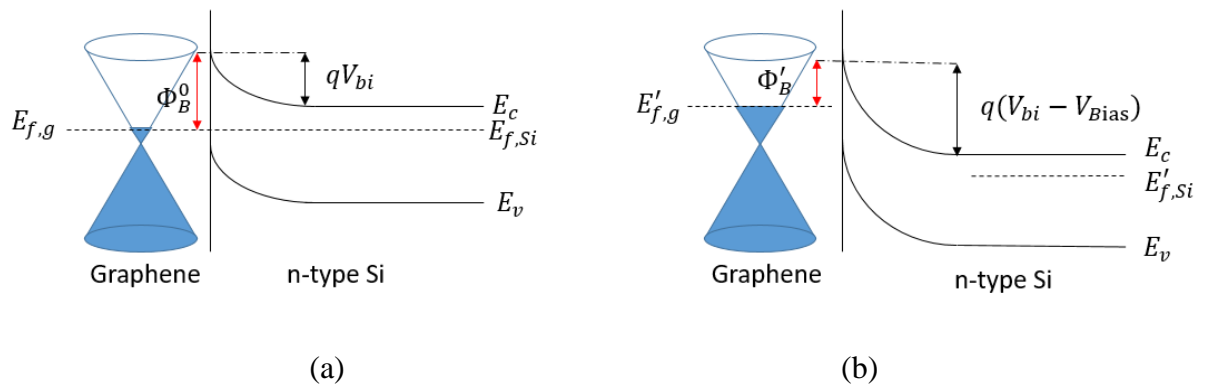
Figure 4.2 Energy band diagram of graphene/n-type silicon at (a) zero bias and (b) reverse bias.

4.1.1 Structure of Schottky Photodiode

A schematic diagram of the Schottky photodiode is shown in Figure 4.1. Monolayer graphene contacts with the metal electrode and n-type silicon substrate forming the graphene/silicon Schottky junction. The thickness of silicon dioxide is 300nm. A bias voltage V_{Bias} is applied between metal and silicon substrate. Figure 4.2 also shows the energy band diagram of graphene/n-type silicon Schottky junction under zero bias (figure 4.2 (a)) and reverse bias (figure 4.2 (b)) conditions. The Fermi level of graphene, which relates to the residual carrier density, n_0 is higher than that in silicon before the contact. When graphene layer contacts the silicon substrate, the thermal equilibrium makes the Fermi level continuous. Thus, electrons transfer from silicon to graphene which change the Fermi level of graphene, while the holes remain in semiconductor and form a depletion region, which introduces a built-in potential.

Unlike a typical metal/silicon Schottky junction, which has a fixed Schottky barrier, the change of Schottky barrier height between graphene and n-type silicon substrate follows the bias voltage. The Fermi level of graphene, which is determined by the transfer charges can be described by [46]:

$$E_F(V_{Bias}) = \hbar v_F \sqrt{\pi(n_0 + \sqrt{2\varepsilon_s N_v (V_{bi} - V_{Bias})/q})} \qquad (4.1)$$

$$\Phi_B(V_{Bias}) = \Phi_B^0 + E_F(V_{Bias} = 0) - E_F(V_{Bias}) \qquad (4.2)$$

where $\hbar$ is the reduced Planck constant, V_{bi} is the built-in voltage when bias voltage is zero. v_F is the Fermi velocity of graphene, n_0 is the residual carrier density due to thermal excitation, ε_s is the permittivity constant of silicon, $N_v = 3.5*10^{16}$ cm^{-3} is donor density in silicon substrate. V_{Bias} is the bias voltage on the Schottky diode and Φ_B^0 is the Schottky barrier height at zero bias voltage.
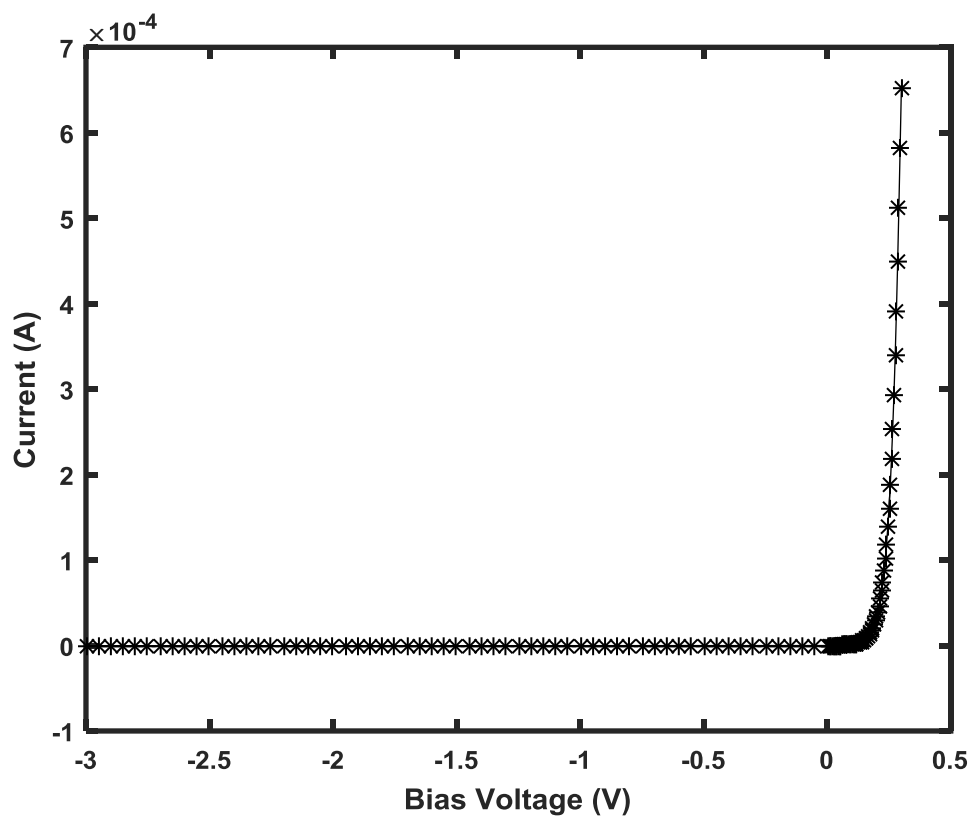
Figure 4.3 I-V characteristics of graphene Schottky diode.
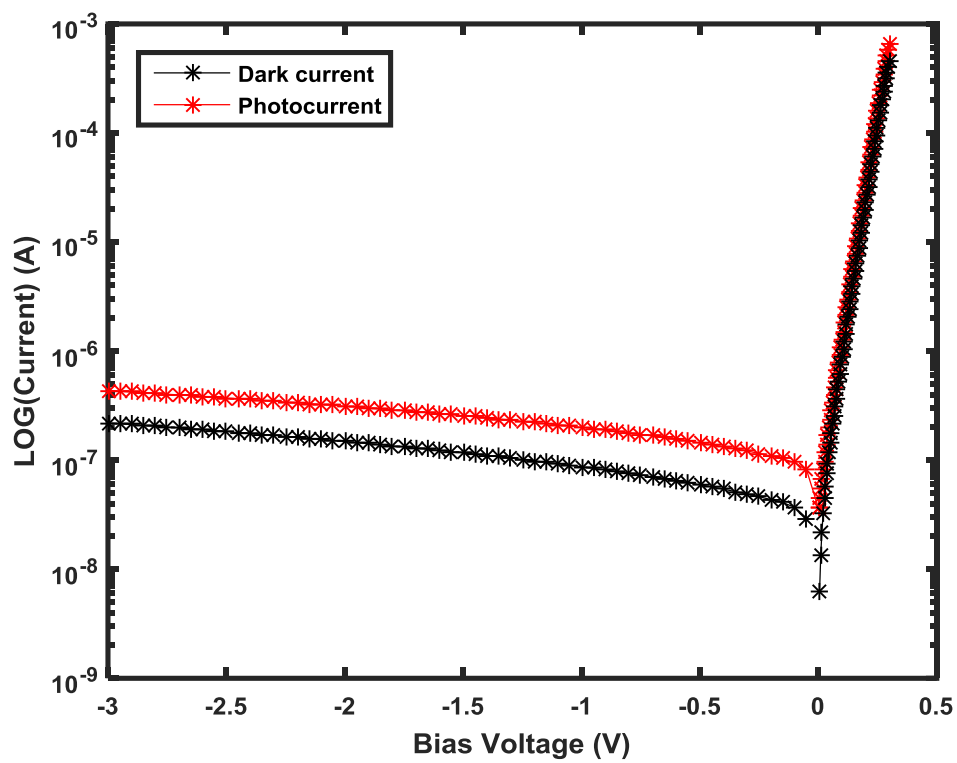
Figure 4.4 Current on a log scale under laser on and off conditions.

The current due to the electrons flowing from silicon to the graphene can be obtained by multiplying the density of charge at the interface by the area A of the junction. Taking the effect of carrier tunneling through the thin interfacial oxide layer into account, the current density of this graphene/silicon Schottky diode can be expressed as [47]:

$$J = A^* T^2 \exp(-\chi^{0.5}\delta_t) \exp(\frac{-q\Phi_B}{k_B T})[\exp(\frac{qV_B}{n_{id}k_B T})-1]$$ (4.3)

where A* is the effective Richardson constant, χ is the effective tunneling barrier height of the oxide, δ_t is the thickness of the thin oxide layer, T is the temperature, k_B is the Boltzmann constant, and n_{id} is the ideality factor. Figure 4.3 shows the current-voltage characteristics of a graphene/n-Si Schottky diode. When bias voltage less than around 0.15V, the Schottky diode turns off, which is smaller than in typical Schottky diodes.

The Schottky diode is a majority carrier device and switches faster than the p-n junction diode, which makes it suitable for photodiodes and photodetectors. In order to increase the sensitivity of a Schottky photodetector, it is important to use a semitransparent layer structure to reduce the reflected light loss from the metal. For our photodiode, graphene is transparent, which provides a rectifying junction to separate light generated electron-hole pairs and reduces reflection of light. The photocurrent density of a Schottky photodiode is expressed by:

$$J_{ph} = eWG_L$$ (4.4)

where G_L is the generation rate of excess carriers and $W = 0.5\sqrt{\frac{2\varepsilon_{si}(V_{bi}-V_{Bias})}{qN_v}}$ is the space charge region width. Figure 4.4 shows the current density under laser- on and off conditions. We used 633nm wavelength and 10mW power laser at room temperature.

(a)   (b)
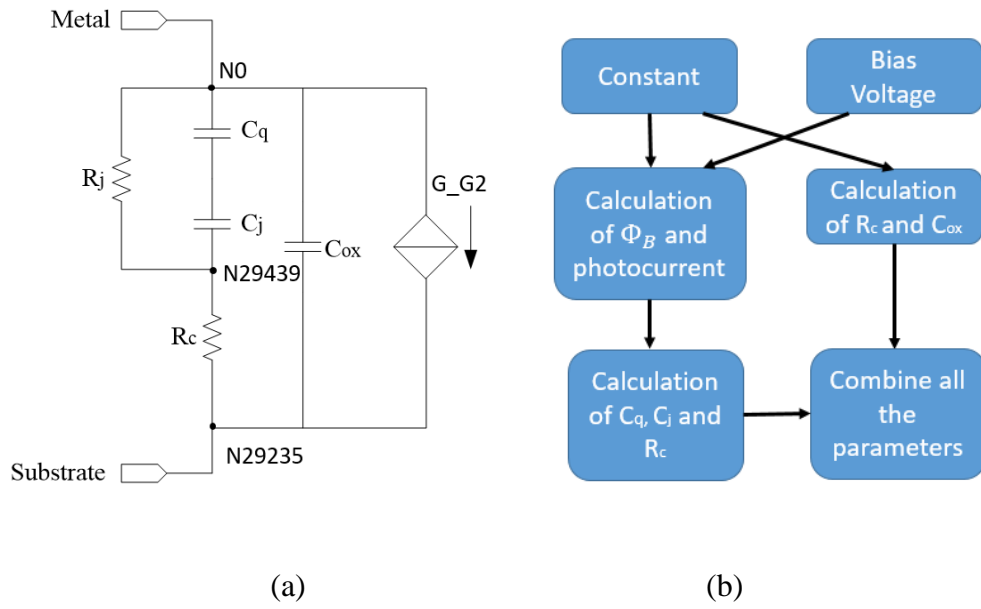
Figure 4.5. (a) Equivalent circuit of Schottky photodiode. The parasitic parrametes are shown on equivalent circuit: quantum capacitance (C_q), junction capacitance (C_j), oxide capacitance (C_{ox}), series resistance (R_c) and junction resistance (R_j). The node numbers shown in the circuit are from PSPICE simulation. (b) Modeling process using analog behavioral modeling in PSPICE.

To illustrate the performance of the photodiode, we used photocurrent-to-dark current ratio as the figure of merit, which is defined as NPDR (normalized photocurrent-to-dark current ratio) = $(I_{photo}/I_{dark})/P_{inc}$, where P_{inc} is the laser power. The computed maximum NPDR is 238.8 W^{-1}.

4.1.2 Modeling of Graphene Photodiode

Above analysis is based on the theoretical equation and Matlab computation but it cannot be used in circuit simulation. In this work, we use analog behavioral modeling which is a module in SPICE to build the model of a photodiode. The method can develop a model for a device and system representing the behavior rather than from a microscopic description. The device modeling in SPICE can be divided into a controlled source and parameters. Controlled source only describe the current-voltage behavior, therefore, parasitic parameters should also be taken into account. We propose an equivalent circuit model for graphene/silicon Schottky photodiode for use in SPICE is shown in Figure 4.5.

The quantum capacitance of graphene is the unique parameter of two-dimensional material which is due to the Pauli Exclusion Principle. Assuming that device is in quasi- equilibrium, derived quantum capacitance based on free electron gas model can be described by [48]:

$C_q = \dfrac{\partial Q}{\partial V} = \dfrac{2q^2}{\hbar v_F \sqrt{\pi}} \sqrt{n}$, where n is the carrier concentration, which depends on the bias voltage.

This theory provides a quantitative description of graphene quantum capacitance in terms of Fermi velocity. The junction capacitance, C_j of Schottky diode can be expressed as one-sided abrupt junction for the analysis and is voltage dependent. This junction capacitance, C_j is given by following relation:

$$C_j = A\sqrt{\frac{q\varepsilon_{si}N_v}{2(V_{bi} - V_{Bias})}} \qquad (4.5)$$

```
 ****      CIRCUIT DESCRIPTION


******************************************************************************

** Creating circuit file "PHOTO_GRAPHENE.cir"
** WARNING: THIS AUTOMATICALLY GENERATED FILE MAY BE OVERWRITTEN BY SUBSEQUENT SIMULATIONS

*Libraries:
* Profile Libraries :
* Local Libraries :
.LIB "../../../photo_graphene-pspicefiles/photo_graphene.lib"
* From [PSPICE NETLIST] section of C:\Users\xchen67\cdssetup\OrCAD_PSpice/16.6.0/PSpice.ini file:
.lib "nom.lib"

*Analysis directives: |
.DC LIN V_V1 -3 0.3 0.01
.OPTIONS ADVCONV
.PROBE64 V(alias(*)) I(alias(*)) W(alias(*)) D(alias(*)) NOISE(alias(*))
.INC "..\PHOTO_DIODE.net"



**** INCLUDING PHOTO_DIODE.net ****
* source PHOTO_GRAPHENE
V_V1          VIN 0 0
G_G2          0 N29235 VALUE {
+  a*ABS((-2.88E6)*(EXP((v(ef1)-0.56)/(0.0259)))*(EXP(v(vin)/0.0285)-1))+4.5E-09
+  }
R_R4          0 N29235  0.00001 TC=0,0
C_C7          EF1 0  1.7E-8  TC=0,0
E_E3          EF1 0 VALUE {
+  (hb*vf/q)*(SQRT(pi*(no+(SQRT((2*es*nv*(vbi-v(vin)))/(q)))))) }
C_C8          EF1 N29439  {a*SQRT((q*es*nv)/(2*(vbi-v(vin))))}  TC=0,0
R_R6          EF1 N29439  {(0.0259*EXP((vbi-v(vin))/0.0259))/(2.88E6)} TC=0,0
R_R5          N29439 0  {(2*w)/(q*ue*nv*a)} TC=0,0
.PARAM  w=1e-4 vf=1.1e8 no=3.5e11 ue=1350 vbi=0.307 nv=3e16 hb=1.054e-34
+  q=1.6e-19 a=64.2e-8 g1=3.1e22 es=1.03e-12

**** RESUMING PHOTO_GRAPHENE.cir ****
.END
```

Figure 4.6 Simulation SPICE input file of graphene/silicon Schottkty photodiode.

(A) PHOTO_GRAPHENE (active)

□ I(G2)   ◇ I(G1)

V_V1

Date: May 10, 2017   Page 1   Time: 15:29:00
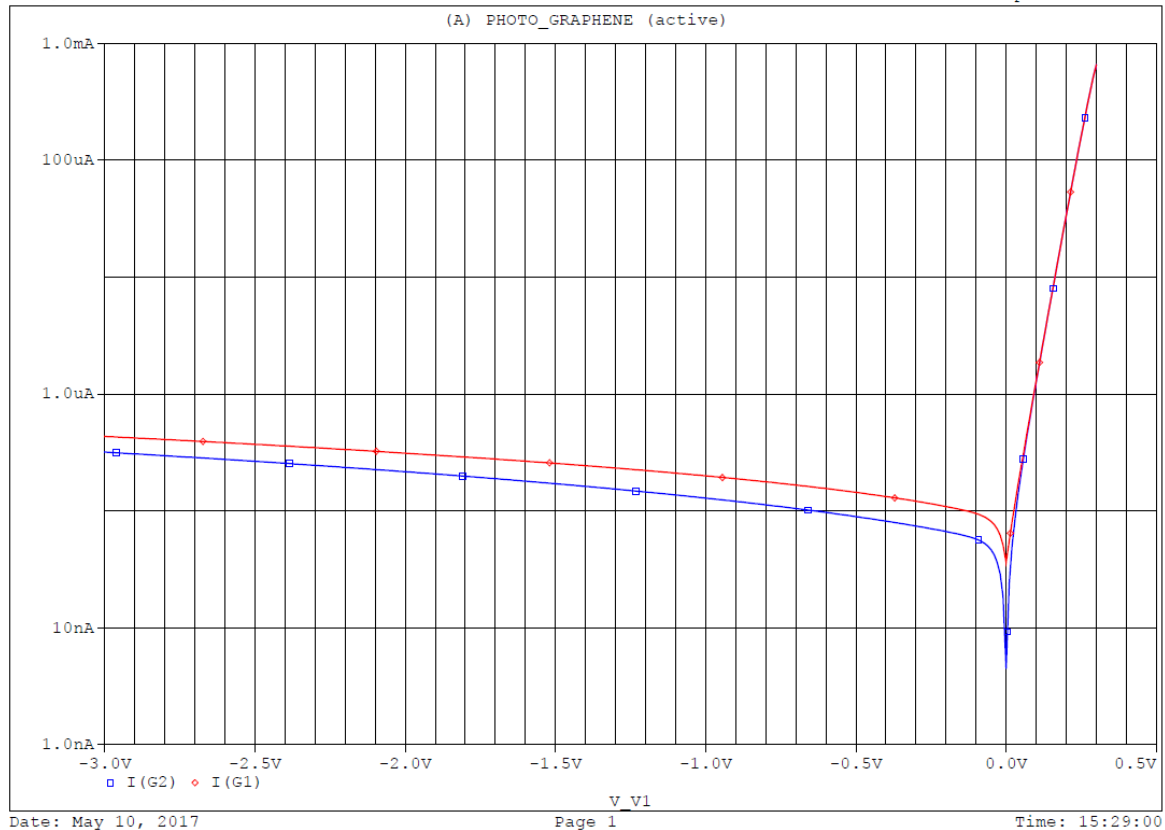
(b)

Figure 4.7 Photocurrent response of graphene/silicon Schottky photodiode under variable bias voltage. Note: The lower curve (I(G2)) is the current in dark and the upper curve (I(G1)) is the photocurrent.

Besides these capacitances, the capacitance due to the metal contact, C_{ox} overlapping the dielectric layer should also be taken into account. The oxide capacitance is expressed by $C_{ox}=\varepsilon_{si}/t_{ox}$, where t_{ox} is the thickness of dielectric layer.

The series resistance, R_c describes the resistance of the silicon substrate and depends on the junction geometry and doping concentration of the substrate. The series resistance can be expressed by, $R_c = \dfrac{2d}{A(q\mu_e N_v)}$, where d is the thickness of substrate, μ_e is the electron mobility in the substrate and N_v is the donor density of the substrate. Besides the series resistance, the junction resistance of graphene and silicon, R_j should also be included into this model. When the graphene contacts with silicon forming a rectifying contact, the thermionic emission current plays important role and is modeled by [49]:

$$R_j = (\frac{\partial J}{\partial V})^{-1} = \frac{(\frac{kT}{q})\exp(-\chi^{0.5}\delta_t)\exp(\frac{q\Phi_B}{kT})}{A^* T^2} \tag{4.6}$$

Figure 4.6 shows the PSPICE input file for the photoresponse simulation from the equivalent circuit of graphene/silicon Schottky photodiode shown in Fig. 4.5(a). Figure 4.7 shows the simulated photocurrent characteristics at 633nm wavelength and 10mW laser source. The X-axis is the bias voltage while the Y-axis is the curent of photodiode. Results are similar to as computed in Fig. 4.4. It illustrates that the analog behavior modeling in PSPICE can be used for photoresponse study of graphene/silicon Schottky barrier diodes.

4.2 Graphene Barristor

Graphene barristor, in which a Schottky barrier formed between graphene layer and silicon layer can widen the bandgap with the control of gate voltage, is a promising method to enhance on/off current ratio for a digital transistor for circuit.
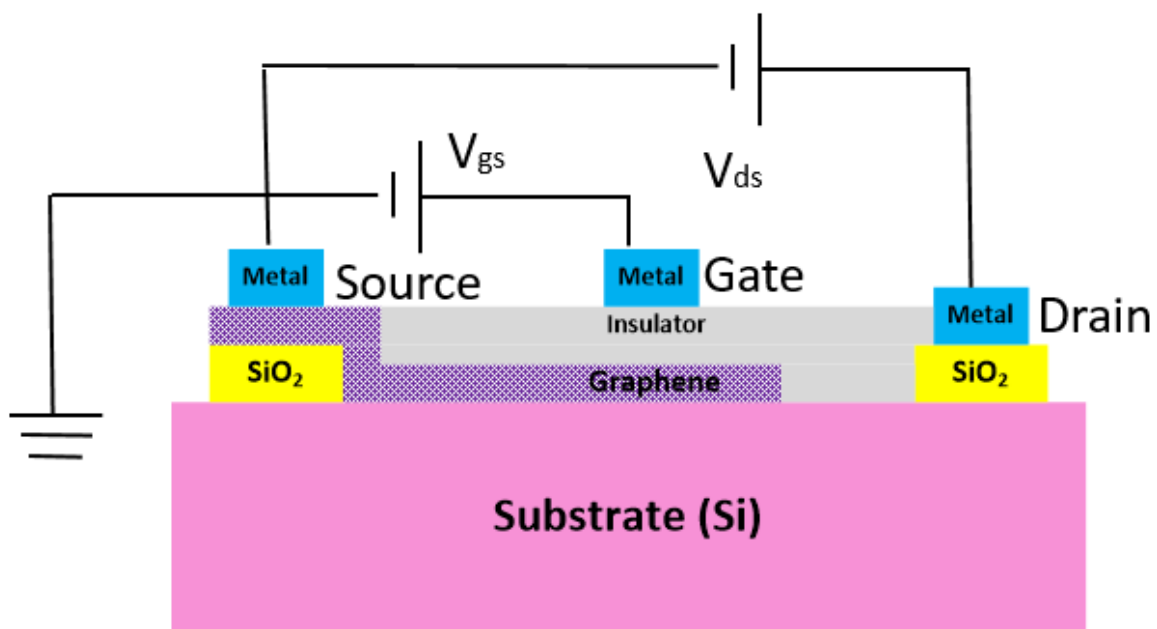
Figure 4.8 Cross section view of graphene barristor.

A theoretical study is presented based on device modeling. Furthermore, using a analog behavior modeling in SPICE, we have developed a compact device model to evaluate the performance of graphene barristor.

4.2.1   Structure of Graphene Barristor

The cross section view of a graphene barristor is shown in Figure 4.8. It can be seen that there is a graphene-silicon Schottky barrier formed around the source node and the gate node. The study regarding the graphene-silicon junction has been reported in [45]. For analysis, it is defined that forward bias and reverse bias are positive voltage applied in graphene layer and silicon layer, respectively. The essence of the graphene/silicon junction is formation of a diode with two nodes. To achieve three-node device working for digital logic, a drain node is added to extend the diode to FET-like structure. The potential of the drain can control the whole current going through the device. When the potential of the drain is the same as of source, from the view of the device, the net current will be zero since there is no voltage difference between the source and the drain. Thus, with the gate control and drain-source control the graphene barristor can perform like a typical FET with three nodes that can be used in digital circuit design.

4.2.2   Analyasis of Graphene Barristor

The equivalent circuit of graphene barristor is shown as Figure 4.9. For the calculation of capacitor existed in graphene barristor, first start with charge balance considering metal, silicon, and oxide silicon [50] expressed by Eq. (4.7) as follows:

Figure 4.9 Equivalent circuit of graphene barristor.

$$
\begin{cases}
Q_m + Q_{gr} + Q_{si} = 0 \\[2mm]
Q_m = \dfrac{\varepsilon_m\left(V_g - V_{gr}\right)}{t_{ox}} \\[3mm]
Q_{gr} = \dfrac{2q}{\pi}\left(\dfrac{kT}{\hbar v_f}\right)^2\left[\zeta_1\left(-\dfrac{qV_{gr}}{kT}\right) - \zeta_1\left(\dfrac{qV_{gr}}{kT}\right)\right] \\[3mm]
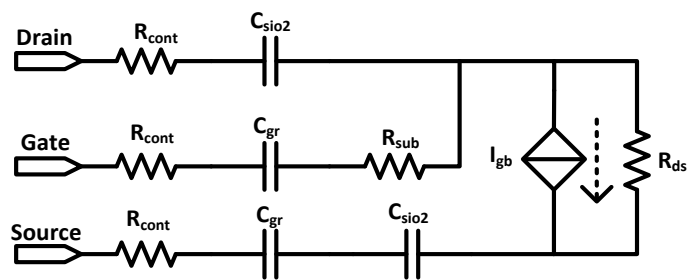Q_{si} = \dfrac{\Phi_d}{|\Phi_d|}\sqrt{2\varepsilon_{si}kTN_d}\sqrt{\left[\exp\left(-\dfrac{q\Phi_d}{kT}\right) + \dfrac{q\Phi_d}{kT} - 1\right] + \dfrac{n_i^2}{N_d^2}\left[\exp\left(\dfrac{q\Phi_d}{kT}\right) - \dfrac{q\Phi_d}{kT} - 1\right]}
\end{cases}
\tag{4.7}
$$

where ε_m and ε_{si} are the permittivity constants of metal contact and silicon, respectively. $t_{ox} = 1\text{nm}$ is the thickness of oxide silicon layer, V_g is the external gate voltage, V_{gr} is the potential of graphene surface, q is the unit electron charge, k is the Boltzmann constant, T is the temperature (default temperature is 300K for the following analysis), $\hbar$ is the reduced plank constant, Φ_d is the potential of silicon surface, v_f is the Fermi velocity in graphene, n_i is the intrinsic carrier concentration in silicon, $N_d = 10^{22}\text{m}^{-3}$ is the doping concentration in silicon. ζ_1 is the Fermi-Dirac integral with order of 1.

For getting the value of capacitor, it is obvious that in above equations both Φ_d and V_{gr} need to be obtained. The function Φ_d with these two parameters can be expressed as follows:

$$
\Phi_d = \Phi_{bo} - V_{gr} + V_{ds} + \frac{kT}{q}\zeta_{1/2}^{-1}\left[\frac{N_d h^3}{2\left(2.16\pi m_o kT\right)^{3/2}}\right]
\tag{4.8}
$$

Where Φ_{bo} is the barrier height for the device under zero bias, and is set to 0.5V in the case of graphene/silicon junction. h is the Planck's Constant, and m_o is the unit electron mass. And $\zeta_{1/2}^{-1}$ is the inverse Fermi-Dirac integral with order of 0.5.

In the analysis regarding capacitance, we can get the potentials of the graphene surface and the silicon layer, which are needed to the calculation of device current. For Φ_b, the barrier height, it can be expressed as: $\Phi_b = \Phi_{bo} - V_{gr}$. The original current density function can be expressed as follows [50]:
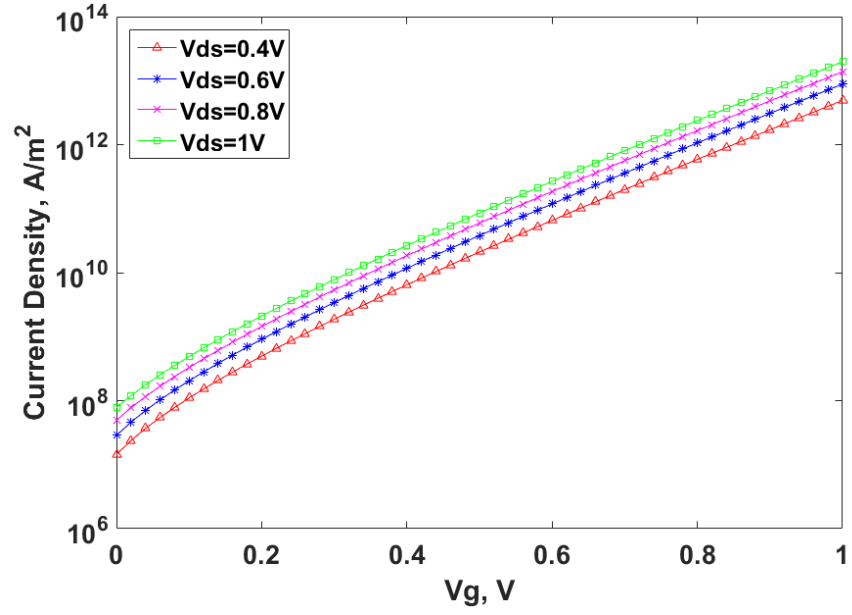
(a)
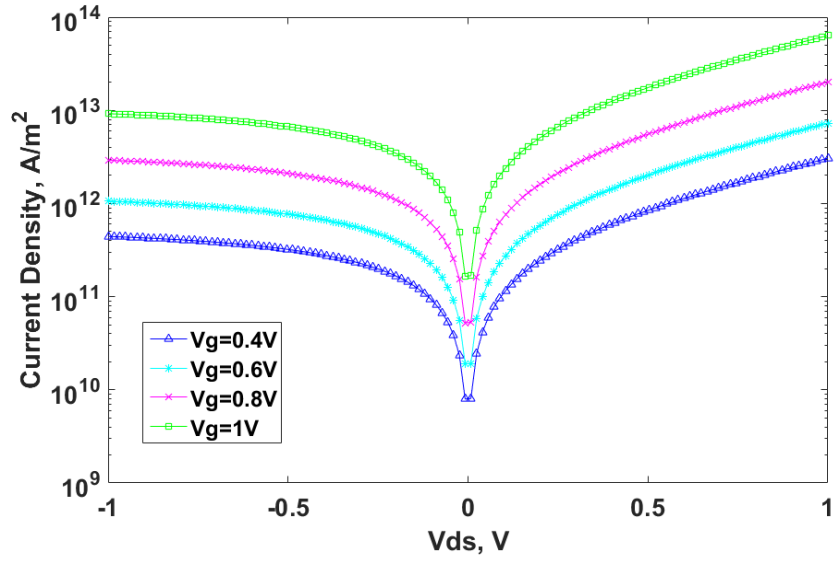
(b)

Figure 4.10 Simulated current: (a) gate voltage as variable; (b) drain-source voltage as variable.

$$J = A^{*}T^{2} \exp\left(\frac{q(V_{gr} - \Phi_{bo})}{kt}\right)\left[1 - \exp\left(-\frac{qV_{ds}}{kt}\right)\right] \quad (4.9)$$

To verify the current analysis, first we use the gate voltage as the variable under fixed drain-source voltage to calculate current density. Then take the drain-source voltage as a variable under the fixed gate voltage to simulate the current density. The both results are shown in Figure 4.10, which are in agreement to the reported results in [51]. It can be seen that the ratio of switch-on current to switch-off current is closed to 10^{5}, which is a practical value to use graphene barristor in digital logic.

For the output resistor between the drain and the source, it can be obtained by taking a derivative of current function with respect to drain-source voltage. The simulated result is shown in Figure 4.10. From the result, we can find that the output resistance of graphene barristor is not sensitive to the drain-source voltage. This fact is due to the modulation by the potential of the silicon layer and the potential of the graphene layer. For the resistance of the substrate, it can be calculated by [52] :

$$R_{sub} = \frac{2t_{sub}}{q\mu_{e}N_{d}A_{cont}} \quad (4.10)$$

where t_{sub} is the thickness of substrate, μ_{e} is the electron mobility in silicon substrate, and A_{cont} is the effective contact area between silicon substrate and graphene layer contributing current channel. The contact resistance is set to 800Ω for our modeling.

Now we have finished the entire analysis of all parameters including device current, graphene capacitor, silicon oxide capacitor, substrate resistance, and metal/graphene contact resistance, all of which are necessary to our device modeling needs. The following section will introduce the modeling of graphene barristor in SPICE using analog behavior modeling.
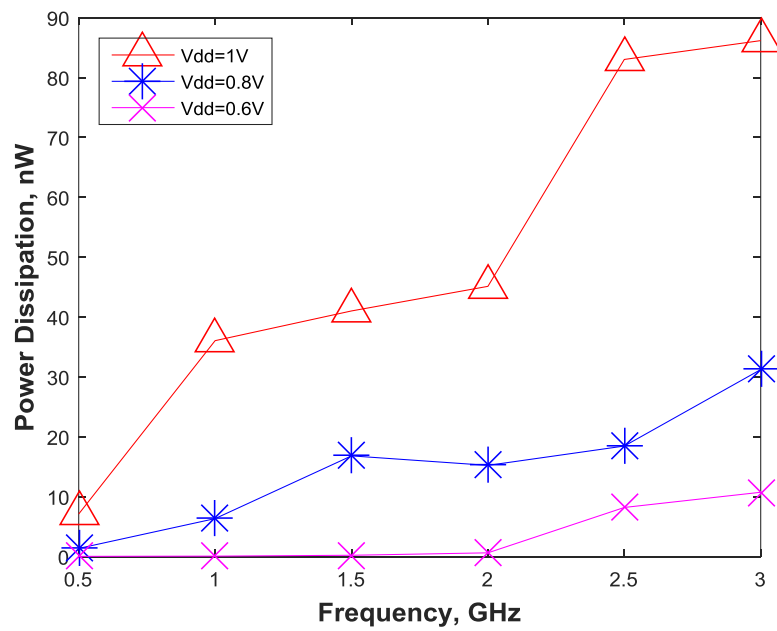
Figure 4.11 Graphene barristor based inverter performance: power dissipation dependence of frequency.

4.2.3   Graphene Barristor Modeling

For the modeling of graphene barristor with our previous analysis, we can find both potentials of the graphene surface and the silicon surface, two important variables which are related to graphene capacitance, silicon oxide capacitance, output resistance, and device current. When these two parameters are solved, with the definition of other constants and the input voltage such as gate voltage and drain-source voltage, required graphene capacitance, silicon oxide capacitance, output resistance, and device current can be solved smoothly. For other parameters serving for modeling, substrate resistance and graphene/metal resistance, these can be easily calculated by constants without variables.

The analysis of the current means that both forward bias and reverse bias conditions have current to achieve digital logic action. We notice that the current under reverse bias is smaller than under forward bias. And the on/off ratio under forward bias is larger than under reverse bias, which means using graphene barristor under forward bias is more suitable to digital current design. We use both forward bias and reverse bias principles to design circuit finding that even though the power dissipated in reverse bias condition is smaller than in forward bias condition, the signal integrity in reverse bias condition is much worse than in forward bias condition. Thus, we choose the way of forward biasing to build circuitry. With this method, the logic design using graphene barristor is same as in traditional CMOS and FinFET, which has both pull-down n-type tree and pull-up p-type tree combined to obtain a complementary tropology.

For low power design, in the simulation, we set 1V, 0.8V, and 0.6V as three supply voltages cases to study. To evaluate the performance of digital circuit using the proposed model of graphene barristor, we designed a complimentary inverter for power dissipation versus frequency dependence. Figure 4.11 shows the simulation results. From the simulation results, we can see that

in most of the cases gate logic under 1V supply dissipates more power than under the reduce supply voltages. The barristor uses relatively large channel length and on/off current ratio is within the acceptable range; and from the view of power dissipation, graphene barristor is a competitive candidate which can be used for the digital circuit design.

4.3   Conculsion

In this work, we presented an analysis of the modeling of barristor and photodiode based on graphene/silicon Schottky barrier diode. Using analog behavior modeling, the accurate SPICE models are proposed for both devices. The proposed model can be adjusted dynamically by the voltage variation for accurate simulations.

CHAPTER 5. IRRADIATION EFFECT ON BACK-GATE GRAPHENE FIELD-EFFECT TRANSISTOR

Besides the optical applications, the graphene-based transistor can also be used in applications related to space electronics. Thus, it becomes important to develop a better understanding of mechanisms related to interactions of high energy radiation with the graphene and graphene-based device structures. In this chapter, we investigate irradiation mechanism based on a semi-empirical model for the graphene back-gate transistor and quantitatively analyze the irradiation influences on electrical properties of the device structure. The irradiation shifts the current which changes the region of device operation, degrades the mobility and increases the channel resistance which can increase the power dissipation.

5.1 Current Transport Model of Graphene Back-Gate Transistor

There are several works investigating the irradiation effects on graphene transistors based on experiments under different radiation sources. As described in the work of Han et.al [53], the different layers of graphene sheet exposed under Cobalt-60 (Co-60) γ-rays, Raman spectra illustrates the irradiation effects on a graphene sheet. The irradiation effect on the graphene sheets is reflected in the ratio of D mode and G mode of Raman spectra. The irradiation effects on graphene transistors with the back gate bias are also studied experimentally [54, 55]. Radiation effect properties are studied by measuring the current-voltage characteristics before and after exposer to x-rays. As observed in this experimental study, the mobility is degraded, the conductance is decreased and the Dirac point is shifted. Although the details of irradiation mechanisms in graphene devices are still unclear, the effects of irradiation on MOSFET and bipolar junction transistors are already well known which can provide some insight [56, 57]. The traps between graphene and silicon oxide interface are expected to have significant effects on graphene-based device structures and should be taken into consideration. The cross section view

of graphene transistor is shown in Figure 5.1. It can be seen that the structure is similar to a typical MOSFET type back-gate transistor which uses a monolayer graphene as a channel over silicon dioxide/silicon substrate and Ti/Pd source and drain electrodes. The adjustable gate voltage is applied on the silicon substrate, while the source is connected to a ground and drain connected to a drain bias. The thickness of silicon dioxide is 300nm and the pure graphene channel in this device is 1.2 μm wide and 0.3μm long.

The semi-empirical model of graphene can be derived following the short-channel MOSFET current transport mechanism. Unlike MOSFETs where nMOS transistor has electrons as carriers while the pMOS transistor has holes, graphene transistor has two types of carriers in the channel due to zero band gap. The kind of carriers is depending on the device bias: if $V_{gs}>0$ and $V_{gd}>0$, the carriers are electrons; if $V_{gs}<0$ and $V_{gd}<0$, the carriers are holes; otherwise the channel has both types of carriers present. The source-drain current can be expressed as follows [58]:

$$I_{ds} = \frac{W}{L} \int_0^L qn(x)v_d(x)dx \qquad (5.1)$$

where W/L is the ratio of channel width and length, n(x) is the carrier concentration along the channel, $v_d(x)$ is the carrier drift velocity. Due to the charge impurities located at the substrate, carries in graphene layer have Coulomb scattering which makes the carrier concentration near the Dirac point no longer to be zero.
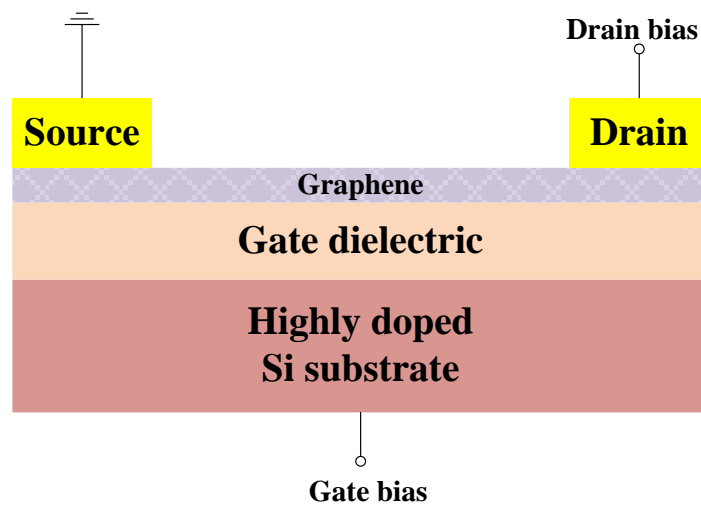
Figure 5.1. Cross section view of a back-gate graphene transistor.

Taking this into consideration, n(x) can be expressed as follows:

$$n(x) = \sqrt{n_0^2 + \left(\frac{C(V_g - V_{g,Dirac} - V(x))}{q}\right)^2} \tag{5.2}$$

where n_0 is the minimum carrier concentration at Dirac point, C is the back-gate capacitance per area, $C = C_{ox} = \varepsilon_{ox}/t_{ox}$, t_{ox} is the thickness of oxide layer. In top-gate device structure, the total gate capacitance is the graphene quantum capacitance C_q in series with the oxide capacitance. However, in the back-gate device, the thickness of the oxide is large, thus the oxide capacitance is much smaller than C_q, so the effect of quantum capacitance can be ignored.

When a high electric field is applied between source and drain, the carrier saturation velocity should be also taken into account. The drift velocity can be described as follows:

$$v_d(x) = \frac{\mu\varepsilon(x)}{\sqrt[a]{1 + \left(\frac{\mu|\varepsilon(x)|}{v_{sat}}\right)^a}} \tag{5.3}$$

where μ is the carrier mobility, $\varepsilon(x)$ is the electric field at position x, a is constant from 1 to 2. In this model, a is assumed to be 1. The carrier saturation velocity, v_{sat} is determined as follows [59]:

$$v_{sat}(n) = \frac{v_F\beta}{\sqrt{n}} \tag{5.4}$$

where v_F is the Fermi velocity, β is a constant related to scattering and is equal to $4\times10^5 cm^{-1}$. For simplicity, the carrier saturation velocity is expressed as follows:

$$v_{sat} = \frac{v_F\beta}{\sqrt[4]{n_0^2 + \left(\frac{C}{2q}(V_{gs} - V_{gs,Dirac} + V_{gd} - V_{gd,Dirac})\right)^2}} \tag{5.5}$$
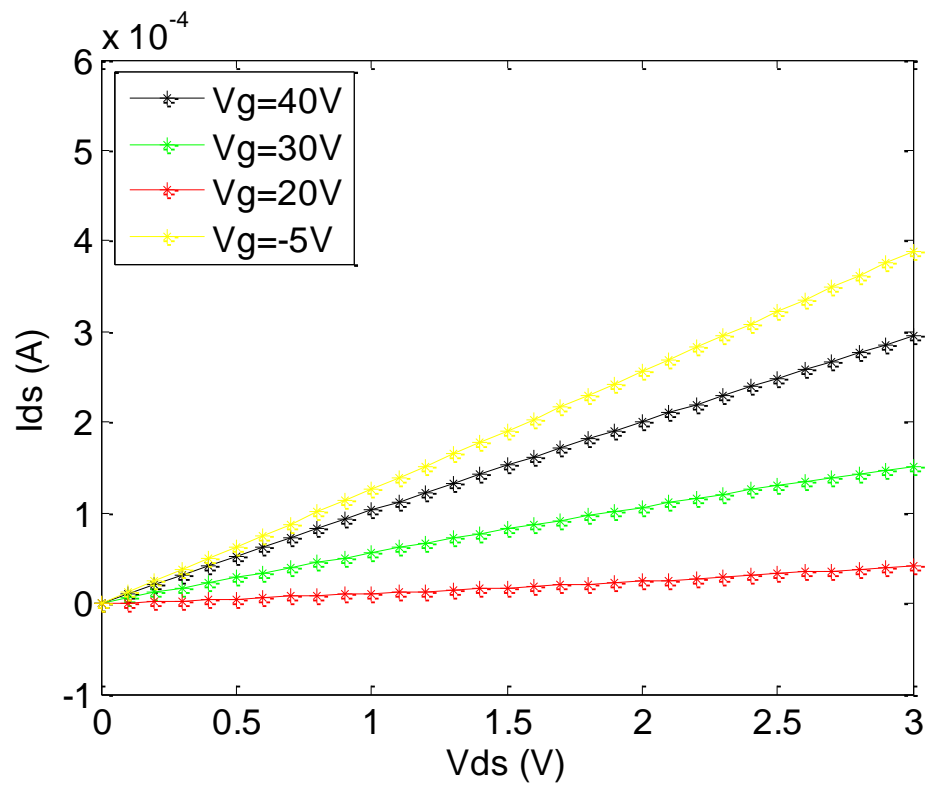
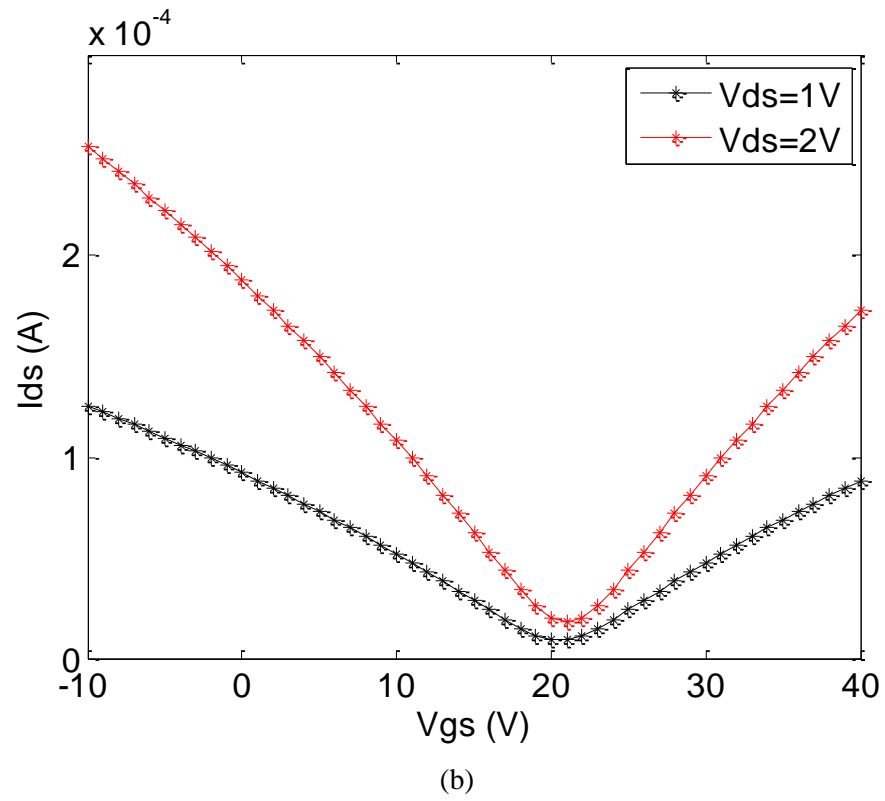Figure 5.2 Drain curren, I_{ds} versus V_{ds} at different Vgs.

(b)

Figure 5.3 Drain curren, I_{ds} versus V_{gs} at V_{ds}=1V and 2V.

Thus, the drain current depending on the voltage along the channel can be described by,

$$I_{ds} = \frac{q\mu W}{L} \int_{V_s}^{V_d} \frac{n(V)}{1 + \frac{\mu|\varepsilon(V)|}{v_{sat}(V)}} dV$$

(5.6)

Considering the effect of charge transfer between metal contact and graphene, the p-n junction formed contributes to an extra resistance. Thus, the contact resistance, R_c should be also included in this current model. In Eq. (5.5), V_d and V_s can be replaced with $V_{ds}-I_{ds}R_c$ and $I_{ds}R_c$, respectively. The intrinsic transconductance of the transistor is defined as $gm = \frac{dI_{ds}}{dV_{gs}}\Big|_{V_{ds}=const}$.

According to a classical transistor model, the field-effect mobility for a given device can be obtained from its output characteristics as follows: $\mu_{FE} = g_m L/(WCV_{ds})$. Figure 5.2 and 5.3 show a plot of drain-source current of a back-gate graphene transistor versus drain-source voltage and also versus gate-source voltage, respectively for W/L=4, $n_0 = 2.2 \times 10^{11} cm^{-2}$ and $V_{g,Dirac}=20V$.

5.2 Irradiation Effect on Graphene Transistor

The irradiation damage is caused by the interaction of high energy charged particles like heavy ions and electrons. Silicon oxide layer is very sensitive to the radiation. The known irradiation theory on MOSFET and bipolar transistors can effectively help us to analyze the irradiation mechanisms of graphene transistor devices. The charged defects in SiO_2 layer nearby the graphene channel create interface traps that cause the decrease of mean free path and carrier mobility because of the Coulomb scattering effects [60]. Interface trapped charge is formed due to capture of holes in the oxide layer. After radiation exposure, electron-hole pairs are generated in SiO_2 layer by the deposited energy. Electrons in the oxide layer are swept out by the electric field since the mobility in SiO_2 layers of electrons is higher than that of holes, while the holes remain in the oxide layer and will be captured by neutral oxygen vacancies [55]. The trapped charge build-up in gate oxide can shift the Dirac point of graphene transistor. When the shift is large, it will

affect the electronic properties of graphene transistor. The continuity equation can calculate the behavior of holes generated by irradiation in silicon dioxide layer and captured by traps [61]. The equation is shown as follows:

$$\frac{\partial p}{\partial t} = -\frac{\partial f_p}{\partial x} + gk_g f_y \qquad (5.7)$$

$$\frac{\partial p_t}{\partial t} = (N_t - p_t)\sigma_{pt} f_p \qquad (5.8)$$

where p is the concentration of holes, f_p is the hole flux, k_g is the generation rate of electron-hole pairs per unit dose in SiO_2, g is the irradiation dose rate, f_y is the electron-hole pair yield. N_t is the density of hole traps, σ_{pt} is the hole capture cross section in the interface. These two equations describe the formation of oxide trapped charge N_{ot} [61] and can be obtained as follows:

$$N_{ot} = K_1 D t_{ox} \qquad (5.9)$$

where $K_1 = N_t \sigma_{py} k_g f_y$, D=gt is the total irradiation dose, and t_{ox} is the thickness of silicon dioxide layer. The main influence of interface traps after radiation is to shift the Dirac point which relates to the radiation dose. The voltage shift can be calculated using following equation:

$$\Delta V_g = -\frac{qt_{ox}}{\varepsilon_{ox}} N_{ot} \qquad (5.10)$$

Besides the effects on oxide layer, irradiation also destroys the sp^2 bond in graphene layer. Graphene sheets have strong in plane σ bonds and an out of plane π bonds which provide the weak bond electrons. In experiments, Raman spectroscopy is widely used to determine the layers and quality of graphene sheets. In Raman spectrum, G peak is the first order in plane vibrational mode, 2D peak is the second order overtone of a different in plane vibration and D peak is related to the inter-valley electron scattering [62]. The ratio of D peak and G peak can illustrate the disorder and

74

defects in graphene sheets. Irradiation can cause vacancies type defects in carbon atomic lattices because the high-energy particles destroy the σ bonds. The vacancies in graphene causes inter-valley electron scatterings and affects the electrical properties of graphene transistor. The irradiation can significant increase the Raman D band which is shown in the work of Han et.al [53]. However, unlike charged impurities, the vacancies creating defects will not change the residual charge density, n_0 of graphene which we can ignore when modeling the irradiation effects. Those defects change the electrical properties of graphene itself especially the short range scatterings which will decrease the mobility. The density of defects can be calculated by the Raman Spectroscopy which can be expressed as follows [62]:

$$N_{defect} = (7.3 \pm 2.2) * 10^9 E_L^4 (\frac{I_D}{I_G})$$

(5.11)

where (I_D/I_G) is the ratio of D peak and G peak in graphene's Raman Spectroscopy and E_L is the energy of laser beam (1.96eV).

Figure 5.4 shows the dc source-drain current and mobility change under 100krad (SiO_2) γ-ray exposure. Besides shifting the dc current, irradiation can also degrade field effect mobility, μ_{FE} and increase the channel resistance, r_{ds} because of the Coulomb scattering from extra charges. According to Matthiessen's rule, the mobility after irradiation can be expressed as follows [63]:

$$\mu = \frac{\mu_0}{1 + \alpha_{ot} N_{ot} + \alpha_{trap} N_{defect}}$$

(5.12)

(a)

(b)

76
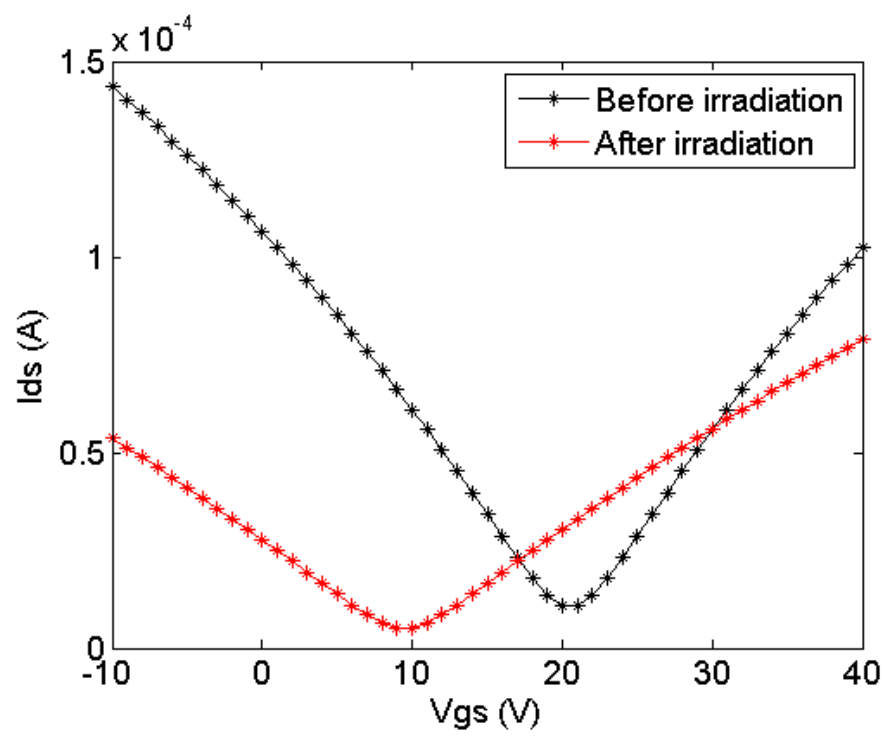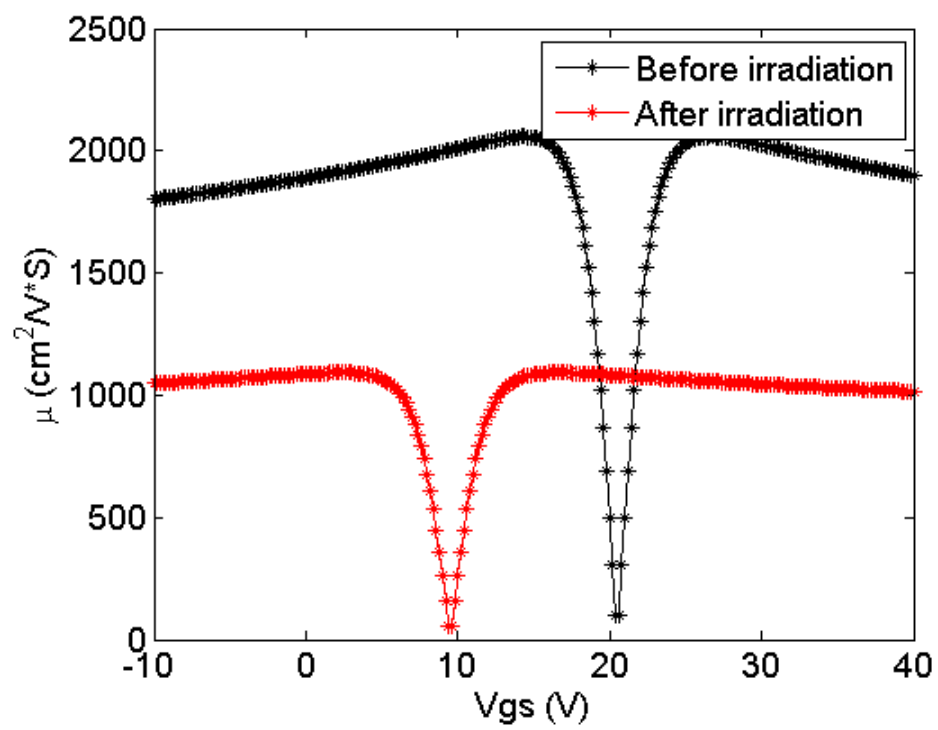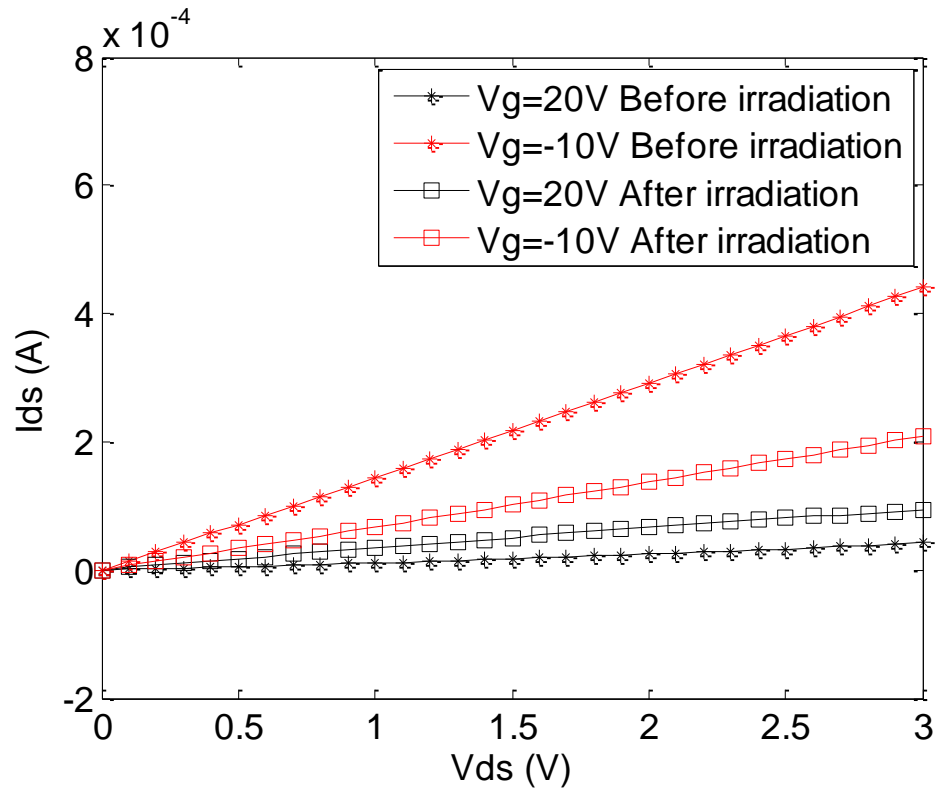
(c)

Figure 5.4 DC source-drain current and mobility changes before and after irradiation (a) Current as a function of V_{gs} at $V_{ds}=1.0V$, (b) Mobility as a function of voltage V_{gs} at $V_{ds}=1.0V$ and (c) Drain current, I_{ds} as a function of V_{ds}.

An attempt is also made to study irradiations effects on the graphene back gate transistor from quantum considerations using atomic level simulation tools such as the Quantum Espresso for simulations at the nanoscale. The simulations also demonstrate degradation in I-V characteristics of the graphene back gate transistor similar to change in I-V characteristics as obtained from the semi-classical modeling approach. The results are shown in Appendix.

5.3 Atomic Level Simulation

Another method to analyze the irradiation effects in a graphene sheet is to use atomic level simulation tools. This is at a quantum level and calculates the transmission coefficient through the Quantum Espresso. Quantum Espresso is an open source software for modeling of electronic properties of materials at the nanoscale. It is based on the density functional theory (DFT) using plane wave's basis set and pseudopotentials. Radiation effects create defects in an atomic layer thick graphene which can change the transmission coefficient values. Figure 5.5 shows the lattice structures of a graphene sheet before and after radiation. In this method, we use Landauer expression to express the conductance of graphene at absolute zero temperature which is given by,

$$I = \frac{q}{h} \int dE T(E)(f_S(E) - f_D(E)) \tag{5.13}$$

where $f_S = \dfrac{1}{1 + e^{(E - \mu_S)/kT}}$ and $f_D = \dfrac{1}{1 + e^{(E - \mu_D)/kT}}$. T(E) is the transmission coefficient which can be calculated through Quantum Espresso. Figure 5.6 shows the drain to source current before and after irradiation.

(a)   (b)
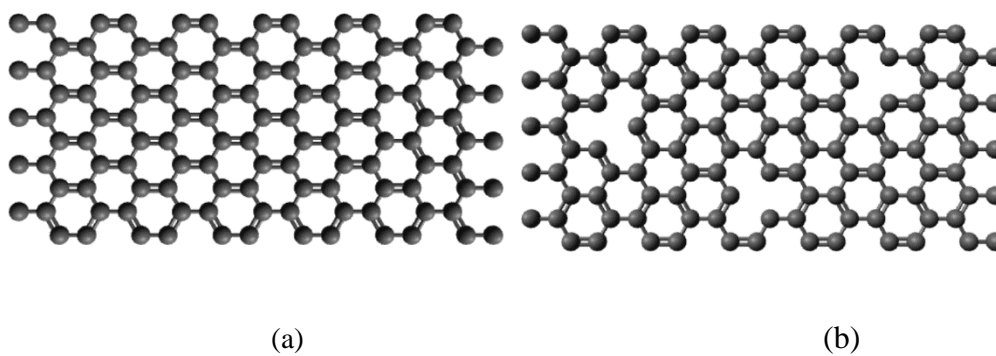
Figure 5.5 (a) Graphene sheet before radiation and (b) Graphene sheet after radiation.
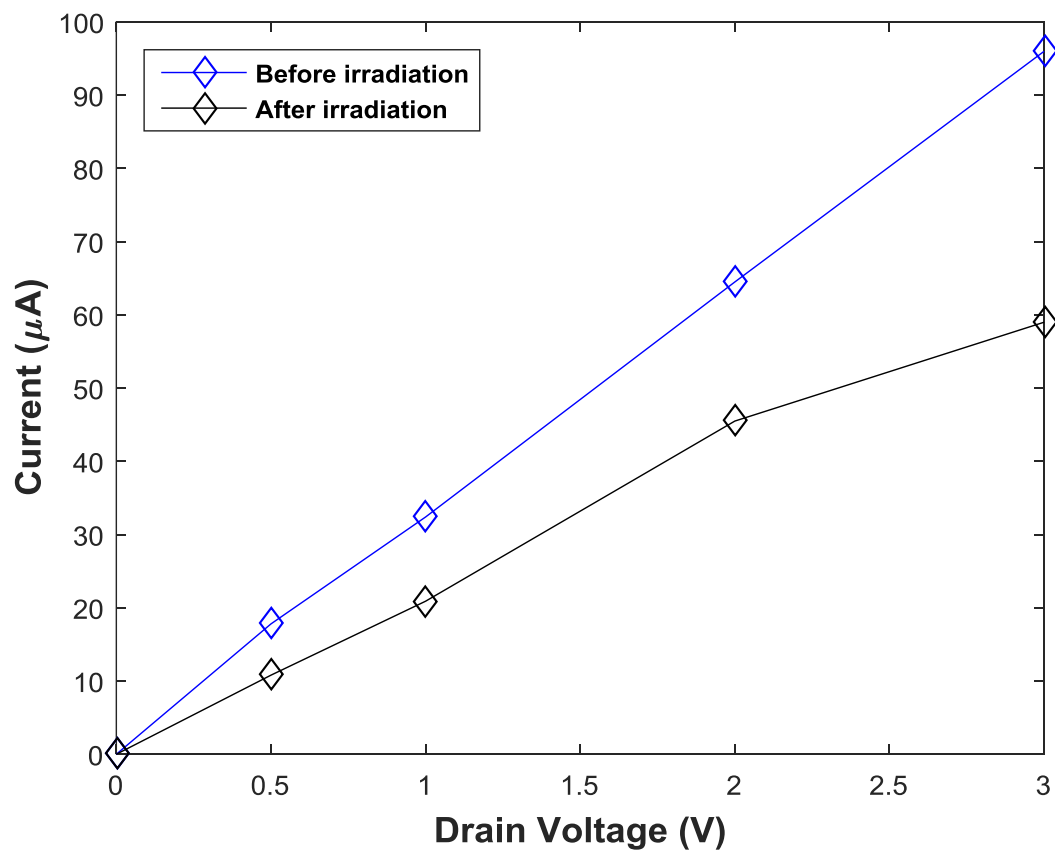
Figure 5.6 Drain-source current before and after irradiation.

5.4   Conclusion

In this work, we have developed a semi-empirical model of graphene-based back-gate transistors which includes irradiation effects and predicts dc characteristics. The irradiation shifts the current which changes the region of device operation, degrades the mobility due to the SiO_2/graphene interface and graphene layer traps charges. Simulations using Quantum Espresso also demonstrate degradation in I-V characteristics of graphene back gate transistor.

CHAPTER 6. CONCLUSION

In this thesis, graphene and graphene back-gate device fabricating process are described in Chapter 2. Using the Nano CVD and Raman spectroscopy in our laboratory, we formed graphene sheet over copper foil and transferred to the silicon oxide/silicon substrate. We also fabricated graphene back-gate transistor using thermal evaporation and deposited aluminum as drain and source electrodes. The I-V characters are tested by Cascade Microtech, Probe Station and HP B1500A Semiconductor Parameter Analyzes.

In Chapter 3, we developed a photocurrent model for photodetector based on back-gated monolayer graphene field-effect transistor on silicon/dioxide substrate. The phenomena including photovoltaic effect, using the built-in electrical field at the graphene junction interface, photo-thermoelectric effect, where thermoelectric current is formed because of the elevated temperature at the junction by the absorbing laser power, and the photo-bolometric effect, where bolometric current is due to applied drain bias, is taken into consideration. The maximum external responsivity is 0.0009A/W at 633nm wavelength and 30 μW laser power. In Chapter 4, we presented an analysis of the modeling of barristor and photodiode based on graphene/silicon Schottky barrier which can be adjusted by the bias voltage. A simple SPICE model is proposed which includes current control and passive parameters. Besides, the optical applications, graphene can be also used for RF applications which requires full understanding of mechanisms related to interaction of high energy radiation with the graphene and graphene devices. In Chapter 5, we have developed a semi-empirical model of graphene back-gate transistor under irradiation effects. Simulation using Quantum Espresso is studied and observed degradation in I-V characteristics.

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APPENDIX: EXPERIMENT

We present a summary of processes of fabricating graphene and graphene based field-effect transistor. To prepare a graphene sheet, we used NanoCVD-8G from Moorefield Nanotechnology in EMDL. (1) We turned on gas tanks and vent the system. (2) After that, we used IPA, DI water and acetone to clean the copper foil. Then, we opened the chamber door and put the cooper foil into the chamber. (3) We purged the system. (4) We chose Program 1 to anneal the copper foil at 700 °C for 120s. Then, we chose Program 5 to grow graphene for 120s at 1000 °C in ambient pressure. (5) Finally, we vent the system again and pull out the door. After the CVD growth, both sides of the graphene are deposited on copper foil. In order to remove the copper foil, we used nitric acid solution to wipe one side of graphene. Then, prepared $Fe(NO_3)_3 \cdot 9H_2O$ solution which can react with copper foil. This reacting process lasted around 2 hours at room temperature. After etching, the copper foil removed and graphene sheet floated in the solution. The residual solution was replaced by deionized water and used to clean the graphene sheet. Finally, we used tweezer to scoop the graphene sheet and put over SiO_2/Si substrate.

To fabricate the graphene based back-gate transistor, we need to deposit metal electrodes on the top of graphene by using photolithography process. First, we used HMDS and positive photoresist (AZ 1512) spinning them for 5 seconds at 3000 RPM and 40 seconds at 4000RPM, respectively. Then, we baked the wafer for 15s. After baking, we exposed the sample alloying with mask for 15 seconds under UV light at room temperature. Finally, we used developer (AZ 425M) to obtain the pattern. After photolithography, in order to deposit the aluminum as electrodes, we used the thermal evaporation method for 2 min and the thickness of aluminum was around 50 μm. After deposition, we used acetone to remove the photoresist.

VITA

Xinlu Chen was born in 1990 in Guizhou, China. She completed her B.S. in electrical and electronic engineering from the Shandong University, Shandong, China in June 2012. Since August 2014, she stated her Ph.D under Dr. Ashok Srivastava at the Louisiana State University, Baton Rouge, LA. She transferred to the MS in spring 2017. Xinlu Chen's research interest includes theory, modeling and design of optical devices and integrated circuits based on graphene. She is expected to graduate in August 2017.