2017

Modeling Of Two Dimensional Graphene And Non-graphene Material Based Tunnel Field Effect Transistors For Integrated Circuit Design

Md Shamiul Fahad
Louisiana State University and Agricultural and Mechanical College, shamiul.fahad@gmail.com

MODELING OF TWO DIMENSIONAL GRAPHENE AND NON-GRAPHENE MATERIAL BASED TUNNEL FIELD EFFECT TRANSISTORS FOR INTEGRATED CIRCUIT DESIGN

A Dissertation

Submitted to the Graduate Faculty of the
Louisiana State University and
Agricultural and Mechanical College
in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

in

The Division of Electrical and Computer Engineering

by
Md Shamiul Fahad
M.S., Louisiana State University, Baton Rouge, LA, 2016
B.S., Islamic University of Technology, Bangladesh, 2009
August 2017

To my late father Nurul Islam and my mother Fatema Khatun for her strong encouragement and relentless effort towards make me coming all the way

To my loving wife Muna and daughter Juwayriyya for their constant patience, caring and support throughout this great journey

ACKNOWLEDGMENTS

I would like to thank first the Almighty Allah for giving me the strength, endurance, capability, mental and physical fitness to undertake the great challenge of pursuing this degree.

I am very much grateful and most privileged to have Dr. Ashok Srivastava as my dissertation supervisor and would like to thank him exceptionally for his relentless support, excellent guidance, constant patience and outstanding mentorship throughout my research carried out in this dissertation and having an understanding of never giving up hope on me.

I most respectfully thank Dr. Pratul Ajmera, Dr. Jonathan Dowling, Dr. Jorge Pullin and Dr. Yuri Antipov for serving as the dissertation committee member and for their outstanding suggestions towards establishing this dissertation.

I am thankful to Dr. Ashwani K. Sharma and Mr. Clay Mayberry of US Air Force Research Laboratory, Kirtland Air Force Base, New Mexico, for their support and encouragement for the research carried out in this dissertation. Special thanks to the director of IT in the department of continuing education at LSU, Mr. Scott Delaney, for offering me the opportunity to work as a graduate assistant.

I would also like to thank K. M. Mohsin for being a great friend and co-worker.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

The Moore's law of scaling of metal oxide semiconductor field effect transistor (MOSFET) had been a driving force toward the unprecedented advancement in development of integrated circuit over the last five decades. As the technology scales down to 7 nm node and below following the Moore's law, conventional MOSFETs are becoming more vulnerable to extremely high off-state leakage current exhibiting a tremendous amount of standby power dissipation. Moreover, the fundamental physical limit of MOSFET of 60 mV/decade subthreshold slope exacerbates the situation further requiring current transport mechanism other than drift and diffusion for the operation of transistors.

One way to limit such unrestrained amount of power dissipation is to explore novel materials with superior thermal and electrical properties compared to traditional bulk materials. On the other hand, energy efficient steep subthreshold slope devices are the other possible alternatives to conventional MOSFET based on emerging novel materials. This dissertation addresses the potential of both advanced materials and devices for development of next generation energy efficient integrated circuits.

Among the different steep subthreshold slope devices, tunnel field effect transistor (TFET) has been considered as a promising candidate after MOSFET. A superior gate control on source-channel band-to-band tunneling providing subthreshold slopes well below than 60 mV/decade. With the emergence of atomically thin two-dimensional (2D) materials, interest in the design of TFET based on such novel 2D materials has also grown significantly.

Graphene being the first and the most studied among 2D materials with exotic electronic and thermal properties. This dissertation primarily considers current transport modeling of graphene based tunnel devices from transport phenomena to energy efficient integrated circuit

design. Three current transport models: semi-classical, semi-quantum and numerical simulations are described for the modeling of graphene nanoribbon tunnel field effect transistor (GNR TFET) where the semi-classical model is in close agreement with the quantum transport simulation. Moreover, the models produced are also extended for integrated circuit design using Verilog-A hardware description language for logic design.

In order to overcome the challenges associated with the band gap engineering for making graphene transistor for logic operation, the promise of graphene based interlayer tunneling transistors are discussed along with their existing fundamental physical limitation of subthreshold slope. It has been found that such interlayer tunnel transistor has very poor electrostatic gate control on drain current. It gives subthreshold slope greater than the thermionic limit of 60 mV/decade at room temperature. In order to resolve such limitation of interlayer tunneling transistors, a new type of transistor named "junctionless tunnel effect transistor (JTET)" has been invented and modeled for the first time considering graphene-boron nitride (BN)-graphene and molybdenum disulfide (MoS_2)-boron nitride (BN) heterostructures, where the interlayer tunneling mechanism controls the source-drain ballistic transport instead of depleting carriers in the channel. Steep subthreshold slope, low power and high frequency THz operation are few of the promising features studied for such graphene and MoS_2 JTETs. From current transport modeling to energy efficient integrated circuit design using Verilog-A has been carried out for these new devices as well. Thus, findings in this dissertation would suggest the exciting opportunity of a new class of next generation energy efficient material based transistors as switches.

CHAPTER 1

INTRODUCTION

1.1 Challenges and Limitations of CMOS Technology

Scaling of metal oxide semiconductor field effect transistor (MOSFET) has largely been governed by the Moore's law over the last five decades providing an unprecedented advancement in the present day technology comprising internet of things (IoT), big data, high performance computing (HPC), artificial intelligence, autonomous vehicle system, augmented or virtual reality and low power energy efficient computer microprocessor.

The idea goes back to 1965, when Gordon Moore from Intel proposed the projection of scaling of MOSFETs, commonly known as 'Moore's Law'. The law states that the number of transistors in an integrated circuit (IC) would double every 18 months [1]. Following the Moore's law, continuous improvement in IC performance had been achieved over the last five decades. Numerous technological advancements have been proposed and implemented for the continuation of the Moore's law as well [2-4].

Recently, a 7 nm technology roadmap has been reported using extreme ultra violet (EUV) lithography technique and dual strained channel with an enhanced mobility for high performance application, demonstrating further a continuation of Moore's law [5]. Compared to tri-gate FinFET, recently a superior electrostatic gate control in Si nanowire CMOS GAA has been demonstrated at a channel length of 24 nm with double metal gate [6].

As the technology node scales down to sub-10 nm channel length operation, significant short channel and quantum mechanical effects prevail which further limit channel length and supply voltage scaling. Direct source-drain tunneling, drain induced barrier lowering (DIBL), gate induced drain leakage (GIDL), and vertical gate tunneling leakage current are some of these

non-ideal effects. Along with high power dissipation, such effects also degrade transistor logic levels and overall computations which restrict technology advancement beyond the Moore's law.

In addition to non-ideal effects resulting from channel length scaling of MOSFET, performance had always remained suppressed by MOSFET's fundamental physical limit in terms of its supply voltage scaling. At room temperature, a MOSFET requires a minimum of ~60 mV/decade subthreshold slope (SS) which is also referred as the thermionic limit of MOSFET. Subthreshold slope is a measure of required gate to source voltage (V_{GS}) needed per decade for a change in drain current (I_D) in the subthreshold region. Since MOSFETs is a digital switch, there is a required minimum difference of current level between it's off and on states, measured in logarithmic scale which is close to 10^4. Therefore, minimum supply voltage required for the MOSFET to go from off to on state is approximately or 0.24 V. Current 14 nm technology node based second generation FinFETs operate at 65 mV/decade considering different non-ideal effects [7].

In order to resolve the issue of thermionic limit of a MOSFET, alternative device architectures have been proposed. Nathanael et al. [8] proposed a novel four terminal nanoelectromechanical system (NEMS), however, such devices are slow due to the moving parts required in switching. Gopalakrishnan et al. [9] proposed impact ionization MOSFET to obtain steep SS operation. Transistor with negative capacitances through ferroelectric gate has also been proposed by Salahuddin and Datta [10]. Other routes involving internal transduction of the voltage into other state variables such as strain, spin, or electron localization have also been proposed [11].

Compared to different alternatives, field effect transistors utilizing band-to-band tunneling, known as the tunnel field effect transistor (TFET), has widely been acknowledged to

overcome the thermal limit of 60 mV/decade at room temperature which eliminates the challenges associated with the supply voltage scaling [12]. Significant progresses have been achieved and competitive performances are obtained compared to MOSFET in TFET. Recently, Memisevic et al. [13] have demonstrated an on current of 10 μA/μm, off current of 1 nA/μm and a subthreshold slope of 48 mV/decade at a supply voltage of only 0.3 V in a Si nanowire TFET of 20 nm diameter. Moreover, with suitable choice of channel material, TFETs are found to be independent of channel length scaling which also provides a lifeline for Moore's law [14].

Performance of TFETs largely depends on the choice of a suitable material. Conventional bulk three dimensional material (e.g. Si, Ge, GaAs, InGaAs) based TFETs have already shown promise compared to MOSFETs [14]. Since the discovery of two dimensional (2D) atomically thin graphene in 2004 by Novoselov et al. [15], the possibilities of a wide class of graphene and non-graphene materials are now explored for design of TFETs. The electronic properties of two dimensional materials are different than their three dimensional counterparts. Therefore, such 2D materials provide a unique compelling potential not only for novel device exploration like TFETs but also for further iteration of Moore's law. In order to obtain high higher transistor density, new type of transistors based on vertical interlayer tunneling have been proposed by Britnell et al. [16]. These new type of vertical transistors are generally referred as interlayer tunnel field effect transistor (iTFET) and studied considering stacking of atomically thin two dimensional layered materials. The concepts of tunneling in a TFET and iTFET are enumerated in the following sections for appropriate understanding of energy efficient TFETs.

1.2 Introduction to Tunneling Field Effect Transistor (TFET)

The 'concept' of band-to-band tunneling through a forbidden potential barrier was first introduced in 1934 by Zener [17] to explain the dielectric breakdown due to sharp increase in

current as the field strength increases. Precisely, in a heavily doped semiconductor p - n junction, under a reverse bias, electrons in the p^+ valence band can tunnel into the n^+ conduction band. The effect is called Zener tunneling which is the principle of operation of band-to-band tunnel field effect transistors.

Historically, Stuetzer in 1952 [18] demonstrated a field controlled 'fieldistor' in a three terminal configuration with ambipolar behavior in current-voltage characteristics based on tunneling of carriers between a p-n germanium junction. Esaki [19] in 1958 first demonstrated the seminal work on band-to-band tunneling in narrower germanium p - n junction diode and explained in detail of I-V characteristics along with negative differential resistance (NDR) behavior. In later years, attempts were made by Srivastava and colleagues [20-22], to study the switching behavior of bipolar silicon n - p - n transistors with GaAs tunnel diodes in hybrid integration across emitter-base and collector-base of transistors for ultra-high speed electronics. These tunnel diode transistors were first of its kind to incorporate circuit level transient analysis. The gated three terminal p-i-n structure comprising a p- and n- doped regions across an intrinsic region was proposed by Quinn et al. in [23] 1978 which was a TFET type structure. Banerjee et al. [24] studied Si TFET in 1987 followed by the study of band-to-band tunneling in MOSFET in 1988 by Takeda et al. [25]. Using III-V materials, Baba in 1994 fabricated TFETs [26] and called it surface tunnel transistor (STT) which was followed by Si STT by Reddick and Amaratunga [27] in 1995. Koga and Toruimi [28] proposed in 1996 a three terminal silicon forward biased tunnel device as a post CMOS switch candidate. Hansch et al. [29] in 2000 fabricated reversed biased vertical Si TFET using molecular beam epitaxy. The lateral TFET on silicon on insulator (SOI) was reported by Aydin et al. [30] in 2004 which was in principle a TFET without an intrinsic region.

The focus on TFET as an energy efficient steep subthreshold slope device started from 2004 when Appenzeller et al. [31] experimentally demonstrated 40 mV/decade subthreshold slope in a carbon nanotube field effect transistor. Since then, extensive research and development in TFETs has been accelerated to mitigate the problem of power consumption in existing CMOS technology. So far the studies comprised of not only conventional Si, Ge and III-V material based TFETs but also non-classical emerging materials such as graphene, two dimensional transition metal dichalcogenides (TMD), topological insulators and non-graphene Dirac-cone based materials such as silicene and germanene [32]. While a lot of such materials based TFETs have been studied theoretically by numerical quantum transport simulation, major achievements in reliability analysis have also been obtained in experimental studies [33]. Analytical current transport modeling of TFETs has also come under investigation to pave the route for circuit and system level simulation for VLSI design. Moreover, TFETs have also shown promise for both digital and analog low power electronics [34].

1.3 Theory of Zener Tunneling

The concept of Zener tunneling is understood in a two terminal diode like framework. For this reason the theory of Zener tunneling in a reverse bias p-n junction is discussed first which is then extended to a gated three terminal FET structure to understand the operating principles of a TFET.

In a reverse bias degenerate p^+ - n^+ junction shown in Fig. 1.1(a), the valence band of p^+ type material E_P^V remains in equilibrium with the conduction band of n^+ type material E_N^C. Due to degenerate doping, the Fermi level of p^+- type material E_P^F lies below E_P^V and the Fermi level of n^+- type material E_N^F lies above E_N^C. The forbidden gap at the tunnel junction works as the potential barrier which limits any zero bias tunneling of carriers between these two bands. As a

reverse bias V_R is applied between this degenerate p^+ - n^+ junction, as shown in Fig. 1.1(b), the electrons at the valence band of the p^+ side can tunnel through this forbidden bandgap into the conduction band of the n^+ side. The process is similar to an electron penetrating through a triangular potential barrier, the barrier height of which is higher than the energy of the electron and varies in spatial direction. The slope of this potential barrier is given by the electron charge times the junction electric field, $q\xi$ as shown in Fig. 1.1(c). Considering a material having parabolic band structure, the energy dispersion relation can be expressed as follows:

$$E = \frac{\hbar^2 k^2}{2m^*} \tag{1.1}$$

where m^* is the effective mass of an electron, $\hbar$ is the reduced Planck constant, E is the particle's energy and k is the wave vector along the transport direction and in one dimensional transport the vector reduces to k_x. For a potential barrier U greater than the particle's energy *(> E)*, the wave vector $k_x(x)$ can be written as follows:

$$k_x(x) = \sqrt{\frac{2m^*\{E - U(x)\}}{\hbar^2}} \tag{1.2}$$

For the junction electric field ξ varying along the tunneling distance d, potential barrier $U(x)$ can be described as follows:

$$U(x) = E + q\xi x \;\; (0 < \mathrm{x} < \mathrm{d}), \tag{1.3}$$

where $d=(E_G/q)\xi$ and is shown in Fig. 1.1(c). Since $U(x) > E$, the wave vector $k_x(x)$ is an imaginary number. Now applying the WKB (Wentzel-Kramers-Brillouin) approximation to the triangular potential barrier at the p^+-n^+ tunnel junction, tunneling probability can be calculated as follows [35]:

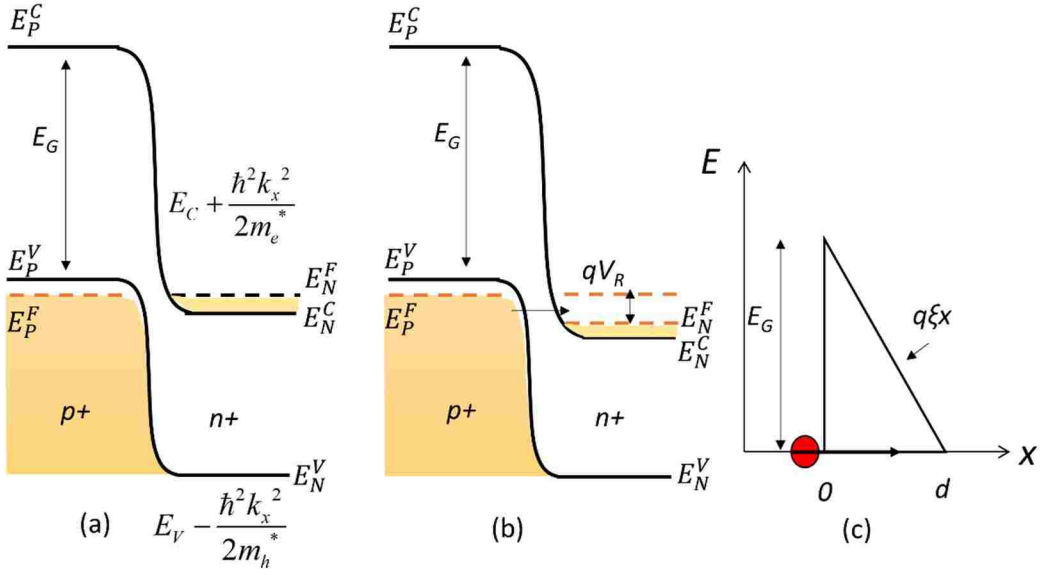


Figure 1.1: Operating principles of Zener tunneling in a reverse biased p^+ - n^+ junction of a parabolic band structure material (a) energy band diagram in off state (b) energy band diagram in on-state as a reverse bias V_R is applied at the tunnel junction and (c) energy barrier seen by an electron for a tunneling distance of d and energy band gap of E_G. Note, ξ is junction electric field and red marker represents position of an electron from which point it starts tunneling.

$$U(x) = E + q\xi x \quad (0 < x < d), \tag{1.3}$$

where $d=(E_G/q)\xi$ and is shown in Fig. 1.1(c). Since $U(x) > E$, the wave vector $k_x(x)$ is an imaginary number. Now applying the WKB (Wentzel-Kramers-Brillouin) approximation to the triangular potential barrier at the p^+-n^+ tunnel junction, tunneling probability can be calculated as follows [35]:

$$T_{WKB} \approx e^{-2\int_0^d k_x(x)dx} \tag{1.4}$$

Substituting the expression of $k_x(x)$ from Eq. (1.2) into Eq. (1.4) yields the expression of tunneling probability as follows:

$$T_{WKB} = \mathrm{e}^{-\frac{4\sqrt{2m_r^*}E_G^{3/2}}{3q\hbar\xi}} \tag{1.5}$$

where m^* is replaced by the reduced effective mass $m_r^* = (1/m_e^* + 1/m_h^*)^{-1}$ for a 1D- direct band gap semiconductor p^+ - n^+ junction with m_e^* and m_h^* electron and hole effective masses, respectively. ξ is the maximum electric field at the tunnel junction [36]. Now integrating the product of the charge flux and the tunneling probability, the 1D Zener tunneling current can be described as follows [35]:

$$I^{1D} = \int qV_g(k_x)\rho(k_x)(f_V - f_C)T_{WKB}dk \tag{1.6}$$

$$I^{1D} = \frac{q^2}{\pi\hbar}T_{WKB}V_T \ln\{1+\cosh(\frac{V_R}{V_T})\} \tag{1.7}$$

where $V_g(k_x) = \frac{1}{\hbar}\left(\frac{dE}{dk_x}\right)$ is the group velocity and $\rho(k_x) = 1/\pi$ is the 1D density of states. f_V and f_C are the Quasi-Fermi-Dirac distributions at the valence band of the p^+ side and conduction band of the n^+ side, respectively, which are expressed as follows:

$$f_V(E) = \frac{1}{1+\exp((E - qV_R)/qV_T)} \tag{1.8}$$

$$f_C(E) = \frac{1}{1+\exp(E/qV_T)} \tag{1.9}$$

Here V_R is the reverse bias and V_T is the thermal voltage defined as k_BT/q (k_B is Boltzmann's constant) and E is energy of electron. Equation (1.7) is the generalized expression for estimating tunneling current in a reverse bias p^+ - n^+ tunnel junction. Since transistor is a three terminal device with a gate electrode between the source and drain, the theory enumerated in this section will be extended further for describing the operation of TFET.

1.4 Operating Principle of a TFET

Compared to a conventional MOSFET where the carriers from source flow based on diffusion and drift mechanisms, to the drain, the primary transport mechanism in a TFET is interband tunneling or Zener tunneling which has been discussed in the previous section. In a TFET, the interband tunneling is responsible for the switching 'on' and 'off' the transistor by controlling the band bending in the channel region effectively by means of a gate bias. The operation has been explained in Fig. 1.2 for a p^+ - i - n^+ n- type TFET for positive gate bias. Figure 1.2(a) shows the schematic of the considered TFET. The positive gate bias makes the source-channel p^+ - i junction reverse biased which is a required criteria for a TFET to operate. It has been assumed that the source Fermi level (E_F^S) aligns with the channel Fermi level (E_F^C) which lies at the midgap (at $E_G/2$). However, source Fermi level (E_F^S) differs from drain Fermi level (E_F^D) by an amount of qV_{DS}, as shown in Fig. 1.2(b).

In the off-state shown in Fig. 1.2(b), the source valence band (E_V^S) and drain conduction band (E_C^D) differs with an amount of qV_{DS}. The channel conduction band (E_C^C) lies above the source valence band (E_V^S) which works as a barrier for the electrons to traverse from source to drain.

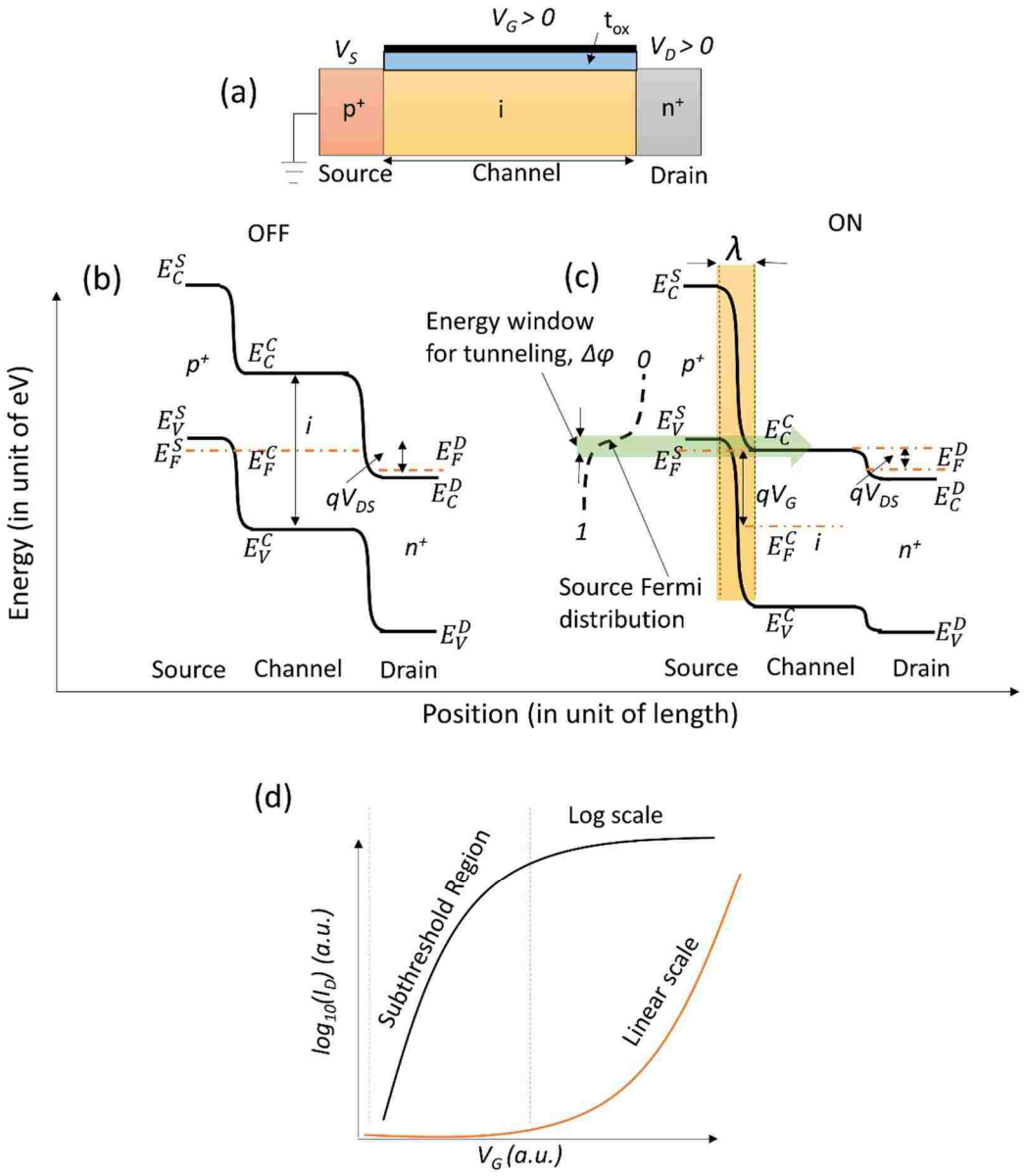


Figure 1.2: Operating principles of a p^+ - i - n^+ n-type tunnel field effect transistor. (a) Schematic of the transistor, (b) off-state diagram, (c) on-state diagram with both V_{GS} and V_{DS} applied and (d) subthreshold conduction during band-to-band tunneling corresponding to the tunnel window shown in (c). Note: (a.u.) refers for arbitrary unit.

This is referred as the 'off' state of the TFET with a very small off-state leakage current. Now as a positive gate bias is applied (negative in p-type TFET), the channel conduction band moves down and comes opposite to the source valence band as shown in Fig. 1.2 (c). A conductive channel referred as tunneling window is now opened through which electrons in the source valence band can tunnel to the empty states of the channel conduction band. At this state the TFET is 'on'. Since the carriers in the tunneling window $\Delta\varphi$ can tunnel into the channel, the energy distribution of carriers from the source is limited. Only the low energy portion of the Fermi-Dirac distribution function contributes towards this tunneling and the high energy part of the source Fermi distribution is effectively cut-off. This is shown by the green arrow in Fig. 1.2(c). Thus, the electronic system is effectively 'cooled down'. From Fig. 1.2(d) we see that the subthreshold region of the transfer characteristics of TFET is a direct reflection of the tunneling current originating from the small energy window. The TFET behaves like a band-pass type filter eliminating the transport from highly energy tails. The length scale for potential variation of this tunneling window between source and channel is defined as λ which is expressed as follows [37]:

$$\lambda = \sqrt{(\varepsilon_C / \varepsilon_{ox}) t_C t_{ox}} \tag{1.10}$$

where ε_c and ε_{ox} are the channel and oxide dielectric permittivity. t_c and t_{ox} are channel and oxide thicknesses, respectively. Following the reverse biased p^+-n^+ tunnel junction, drain current in TFET also depends on the tunneling probability, which can be estimated in terms of λ as follows [38]:

$$T_{WKB} = \exp\left(-\frac{4\lambda\sqrt{2m_r^*}E_G^{3/2}}{3q\hbar(E_G + \Delta\varphi)}\right) \tag{1.11}$$

Here, $\Delta\varphi$ is the energy window for tunneling. Comparing Eq. (1.11) with Eq. (1.5), the electric field at the tunnel junction can be estimated as follows:

$$\xi = \frac{E_G + \Delta\varphi}{\lambda} \tag{1.12}$$

$$\xi = \frac{E_G + \Delta\varphi}{\sqrt{(\varepsilon_C / \varepsilon_{ox}) t_C t_{ox}}} \tag{1.13}$$

For a three terminal gated TFET, the drain current is estimated using the modified current equation of Eq. (1.6) as follows:

$$I_T = \int_0^{\Delta\varphi} q V_g(k_x) \rho(k_x) (f_S - f_D) T_{WKB} dk\,, \tag{1.14}$$

where f_S and f_D are the source and drain quasi Fermi-Dirac distributions, respectively with following expressions:

$$f_S(E) = \frac{1}{1 + \exp\left(\left(E - E_F{}^S\right) / qV_T\right)} \tag{1.15}$$

$$f_D(E) = \frac{1}{1 + \exp\left(\left(E - E_F{}^D\right) / qV_T\right)} \tag{1.16}$$

Note that, $E_F{}^S$ and $E_F{}^D$ are the position of the Fermi levels in source and drain sides, respectively. Both Eqs. (1.11) and (1.14) depend on specific device geometry and properties of the channel material, modeling of which are the objectives of this proposal.

1.5 Subthreshold Behavior of TFET and Comparison with MOSFET

In this section, the subthreshold behavior of TFET is explained and compared with that of a MOSFET. For this, we first discuss the physical insight into the subthreshold slope of a MOSFET and the reasoning of the intrinsic physical limit of conventional MOSFET of

thermionic Boltzmann's limit of 60 mV/decade. Following this discussion, the subthreshold slope in TFET is described.

1.5.1 Subthreshold Slope (SS) of a MOSFET

An important figure of merits of MOSFET is the subthreshold slope or inverse subthreshold swing (SS). It is a measure of the input parameter (gate voltage) to the output current (drain current) and is defined as the gate voltage required to change the drain current by an order of magnitude when the transistor is operated in the subthreshold region. In a MOSFET, expression of SS is defined as follows [39]:

$$SS = \frac{dV_{GS}}{d\left(\log_{10} I_D\right)} = \underbrace{\frac{dV_{GS}}{d\psi_S}}_{m} \underbrace{\frac{d\psi_S}{d\left(\log_{10} I_D\right)}}_{n} = \left(1+\frac{C_d}{C_{ox}}\right)\left(\frac{k_B T}{q}\right)\ln 10 \tag{1.17}$$

In Eq. (1.17), V_G is the gate voltage and I_D is the drain current, k_BT/q is the thermal voltage, ψ_S is surface potential, 'm' is the body factor and 'n' is the factor which characterizes the change in drain current I_D with surface potential ψ_S.

The depletion and gate capacitances are described in terms of C_d and C_{ox}, respectively. Oxide capacitance, C_{ox} is determined from $C_{ox}=\varepsilon_{ox}/t_{ox}$. We can see C_{ox} can vary from a minimum to a maximum value depending on oxide thickness, t_{ox} and the body factor 'm' become as low as 1. Hence the net expression of SS in Eq. (1.17) reduces to (k_BT/q) ln10. Now for a room temperature of T = 300 K, SS becomes,

$$\rightarrow \frac{kT}{q}\ln 10 \cong 60 mV decade^{-1}\Big|_{T=300K}$$

Therefore, irrespective of the channel length scaling, the operation of MOSFET cannot go down below 60 mV/decade. This puts a fundamental limit on the power supply scaling. For a MOSFET as a digital switch, ITRS required on/off current ratio to be ~10^4 which means,

between the off to the on state of the transistor there should be a difference of 4 orders of magnitude of drain current. Now in the subthreshold region, SS can be least as 60 mV/decade which reflects the required supply voltage to obtain this on/off current ratio as follows: *60 mV/decade x 4 decade = 240 mV = 0.24 V.*

1.5.2 Subthreshold Slope of a TFET

For deriving the subthreshold slope of a band-to-band tunneling device, we start from the expression of tunneling current in a reverse bias p-n junction as follows [38]:

$$I_D = aV_{eff}\xi \exp(-b/\xi) \tag{1.18}$$

where

$$a = \frac{q^3\sqrt{2m^*/E_G}}{4\pi^2\hbar^2} \tag{1.19}$$

$$b = \frac{4\sqrt{m^*}E_G^{3/2}}{3q\hbar} \tag{1.20}$$

V_{eff} is the effective bias at the tunnel junction and ξ is the electric field at the tunnel junction which can be estimated from Eq. (1.13). Replacing the value of I_D from Eq. (1.18) in the generalized form of subthreshold slope, SS for TFET in Eq. (1.17) yields [40]:

$$SS = \ln 10\left[\frac{1}{V_{eff}}\frac{dV_{eff}}{dV_{GS}} + \frac{\xi + b}{\xi^2}\frac{d\xi}{dV_{GS}}\right]^{-1} \tag{1.21}$$

From Eq. (1.21) it is evident that SS is independent of the thermionic limit of kT/q as in SS of MOSFET SS. Moreover, SS of TFET is more dependent on gate-source bias, V_{GS} which means that SS in TFET is not constant [40].

There are two terms in the denominator in Eq. (1.21) which needs to be maximized in order to achieve a low SS. According to the first term in Eq. (1.21), TFET needs to be engineered

for V_{GS} to fully control over V_{eff}. To obtain that, the transistor geometry along with thin or high-κ dielectric and ultrathin body is highly desirable. Hence, a low SS will occur at low V_{GS}. Second way to achieve low SS is to maximize the derivative of junction electric field with respect to V_{GS}. Using this technique Bhuwalka et al. [41] obtained high electric field at low tunneling width for an increasing V_{GS}. However, in practice both V_{eff} and ξ are coupled together and cannot be engineered independently.

1.6 Interlayer Tunneling in Vertical Heterostructure

The tunneling phenomena discussed so far considers the band-to-band tunneling in a field effect tunneling in a planar direction between the conduction and valence bands of a single material or planar heterostructure. However, compared to in-plane tunneling, out-of-plane tunneling in a van-der Waals heterostructure of stacked two dimensional layered material has attracted interest like never before [16]. Though the interlayer tunneling through thin insulating barrier exists in metal-insulator-metal (MIM) and metal-insulator-semiconductor (MIS) tunnel structures, its applicability for three or four terminal transistor level operations is not much explored. Field effect transistors based on such tunneling mechanism is generally referred as interlayer TFET (iTFET), which will also to be the acronym used in this work. In this section, recent advancements in iTFETs are enumerated followed by principles of operation of such interlayer tunneling.

1.6.1 Tunneling Through Thin Insulating Barrier

Sommerfield and Bethe [42] in 1933 were first to theoretically study and predict electron tunneling between two similar metal electrodes separated by thin insulating tunneling barrier for both low and high voltage, which was extended by Holm [43] in 1951 to incorporate the intermediate biasing effects. Fischer and Giaever [44] in 1960 experimentally studied the

electron tunneling though thin Al_2O_3 film of width of few nanometers and also proved the theoretical prediction of Holm [43] with an effective mass correction inside the tunneling barrier of Holm's model. Both works observed the exponential decay of the tunneling current as the tunneling barrier increases. Simmons [45] in 1963 proposed a theory of electron tunneling though thin insulating films separated by similar electrodes using image potential. The interest of interlayer tunneling in recent years emerged with the discovery and extensive exploratory research on two dimensional materials such as graphene and hex-boron nitride. Being isolable at its atomic scale monolayer form, vertical stack of such layered materials provides the best combination to study interlayer tunneling phenomena [46].

Sciambi et al. [47] in 2011 demonstrated interlayer tunneling transistor based on GaAs/AlGaAs vertical heterostructure where the wave function from one GaAs layer extend towards the other GaAs layer penetrating through AlGaAs. In a transistor form, such quantum device was first of its kind [47]. Although the experiment was carried out at 4.2 K (temperature of liquid He), Sciambi et al. [47] predicted similar room temperature operation for graphene heterostructures. Being a zero band gap semiconductor, graphene based field effect transistor has been providing very poor on/off current ratio which made graphene transistors questionable for digital applications. Therefore, it has been necessary to find an alternative way to design graphene transistor suitable for digital applications. Britnell et al. [16] demonstrated the first room temperature operation of interlayer field effect tunneling transistor in 2012. The transistor provided an on/off current ratio of 50 for graphene-boron nitride-graphene and 10^4 for graphene-molybdenum disulfide (MoS_2)-graphene vertical heterostructure. Feenstra et al. [48] simultaneously reported a theoretical study of single particle tunneling characteristic of doped graphene-boron nitride (BN)-graphene showing the need to incorporate momentum conservation

in estimating tunnel current density. However, the experimental study of Britnell et al. [16] doesn't provide any momentum conservation for which the current obtained by Britnell et al. [16] had no resonant peak. This was further corrected in [49] for similar device structure and the results matched with that of [48].

Georgiou et al. [50] in 2013 studied similar graphene-tungsten disulfide (WS_2) - graphene iTFET providing an on/off current ratio of 10^6. Along with the reported MOSFET type interlayer field effect tunneling transistors based on both graphene and non-graphene materials, bipolar junction transistor (BJT) type interlayer tunneling transistor architectures have been studied extensively [51, 52].

1.6.2 Principles of Operation of Interlayer Tunneling

In order to study the interlayer tunneling phenomena between two electrodes separated by a thin tunneling barrier, three necessary theories are required to be discussed, i.e. a) estimation of tunneling charge density, b) estimation of tunneling probability and c) estimation of tunneling current. Compared to a MIM tunnel diode where the electrode materials at both sides of the insulator are metal, iTFET considers either semi-metal or semiconductor at both sides of the insulating barrier. We refer the such electrode-1 as source and electrode-2 as drain. Figure 1.3(a) shows schematic of an iTFET where source and drain are separated by a thin tunneling barrier. The heavily doped Si under SiO_2 works as the back gate which controls the tunneling between source and drain shown by the green arrow. Note that the green arrow also shows the direction of drain current flow between source and drain. To avoid lattice mismatch between SiO_2 and electrode-2, additional substrates can be used on top of SiO_2. The vertical line AA′ directs the cross section of the transistor for which the energy band diagrams of Fig. 1.3(b) and (c) are drawn. In the off state, the drain-source bias, $V_{DS} = 0\ V$ for which both the Fermi levels of the top

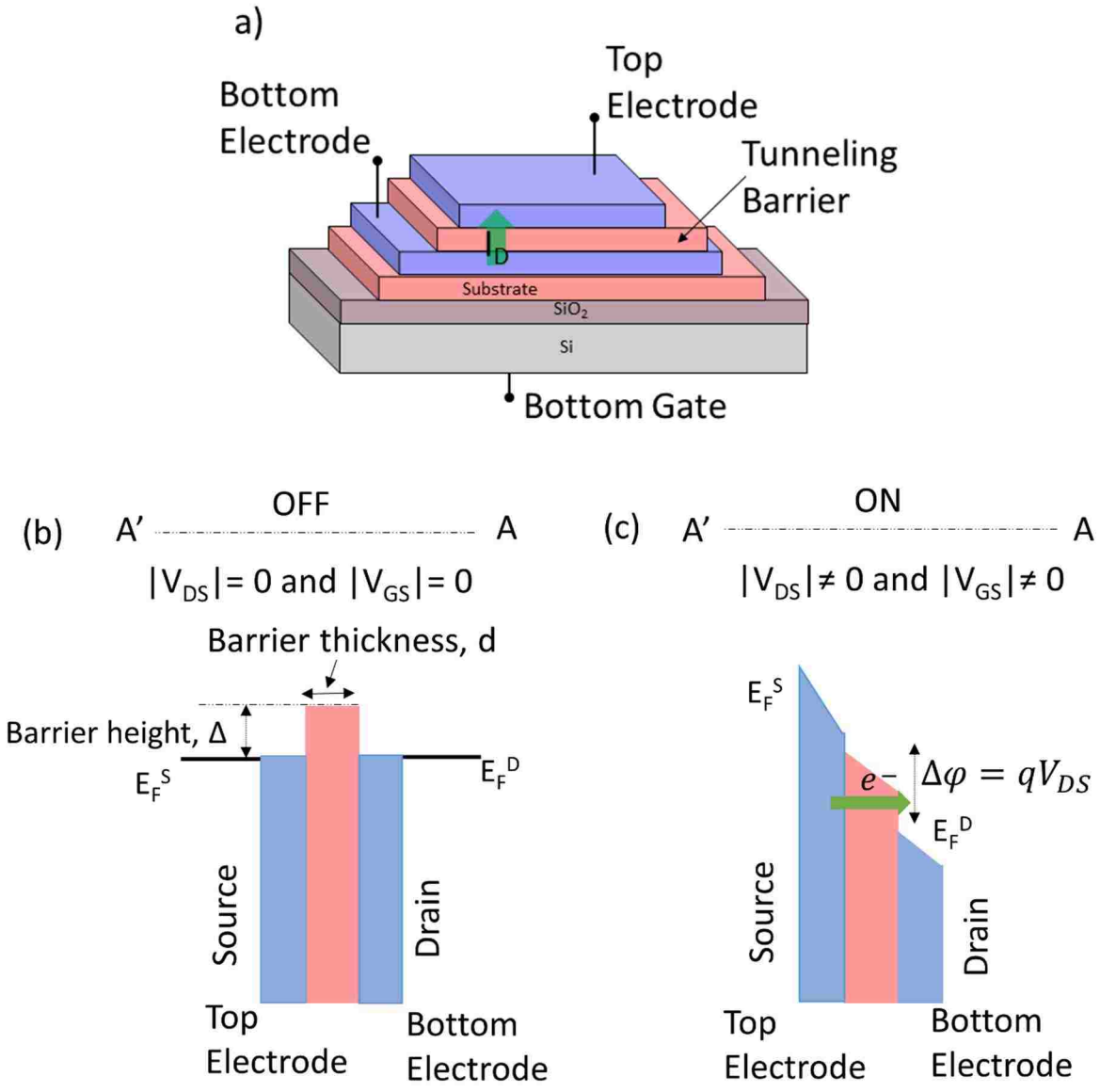


Figure 1.3: (a) Schematic of an interlayer tunnel field effect transistor (iTFET), (b) cross-sectional energy band diagram along AA′ in off state and (c) on-state energy band diagram where the green arrow shows direction of tunneling from source (electrode-1) to drain (electrode-2) due to a bias V_{DS}. Tunneling window is $\Delta\varphi$.

and bottom electrodes are in equilibrium and hence no electrons can tunnel thorough the barrier. This is referred as the 'off' state of the transistor. Compared to the source, the height of the energy barrier Δ is estimated in electron volt (eV). The thickness of the tunnel barrier is d, which is few nanometer (nm). As the bias is applied between source and drain (for $|V_{DS}| \neq 0\ V$), the Fermi level of drain (E_F^D) goes below the source Fermi level (E_F^S) by an amount of qV_{DS} which initiates an interlayer tunneling between source and drain. However, the net tunneling current is controlled by the gate terminal using a gate bias. This is referred as the 'on' state of the transistor. The schematic shown in Fig. 1.3(b) represents for off state and Fig. 1.3(c) for on state of iTFET.

1.6.3 Estimation of Tunneling Probability

Unlike planar TFET where the tunnel junction electric field and device geometry provides key control of the tunneling probability, in iTFET, tunneling is dependent on the barrier height and the thickness of the barrier. If the tunneling conductance of the channel is smaller than the quantum conductivity ($q^2/\hbar$) then the tunneling probability, T_{WKB} exponentially depends on the energy of the tunneling electrons as follows [16]:

$$T_{WKB}(E) = A\exp[-W_z(E)], \tag{1.22}$$

where, A is a function who's value depends on the details of the wave function matching at the interface. For simplicity we assume A = 1 [16]. For an isotropic barrier, the following dispersion relation needs to be solved for each of the barrier material:

$$E = E_n(k_x, k_y, k_z), \tag{1.23}$$

where E is the energy of the electron tunneling along vertical A′A direction and described using the three dimensional energy dispersion relation $E_n(k_z, k_y, k_z)$ for n-number of bands [16]. Inside the energy gap no real solution for k_z is possible since the barrier height is higher than the energy

of an electron. Hence, the function $W_Z(E)$ is expressed with the minimal imaginary k_z (Imk_z) for a given energy E and arbitrary k_x and k_y as follows:

$$W_Z(E) = 2d \operatorname{Im} k_z \tag{1.24}$$

For a parabolic band structure, Imk_z is defined as follows [16]:

$$\operatorname{Im} k_z = \frac{\sqrt{2m^* \Delta}}{\hbar} \tag{1.25}$$

Where Δ is the barrier height and m^* is the effective mass of the electron inside the barrier. Δ is a measure of energy gap from the source Fermi level to the valence band of the tunneling barrier for hole transport or to the conduction band for electron transport. Combining Eqs. (1.22), (1.24) and (1.25), expression of interlayer tunneling probability becomes [16, 50]:

$$T_{WKB}(E) = \exp(-2\,\mathrm{d}\frac{\sqrt{2m^* \Delta}}{\hbar}) \tag{1.26}$$

It is to be noted that, tunneling probability through layered crystal depends on E weakly (logarithmically) compared to an isotropic crystals which exhibits standard square-root energy dependence. For small changes in Δ, such difference is insignificant. Since majority of the layered or bulk materials used as tunneling barrier are non-Dirac cone material, using parabolic dispersion relation for describing their band structure, makes Eq. (1.26) acceptable. Nevertheless for describing tunneling through Dirac materials (i.e. graphene, silicene, germanene, stanene) would require a correction to Eq. (1.26) with a linear dispersion relation for these materials. Since the method of estimating drain current is similar to the one discussed previously for planar band-to-band TFET, hence it is not repeated here.

1.7 Scope of Research

In this dissertation, modeling of two dimensional graphene and non-graphene material based planar and vertical tunnel transistors are studied from the current transport phenomena to energy efficient integrated circuit design.

Graphene is the first of the isolated atomically thin two dimensional materials and so far the most extensively studied promising material. Since a significant portion of this dissertation considers graphene as a channel material in different types of transistors, Chapter 2 discusses the history, synthesis, electronic structure, band gap engineering and doping of graphene.

In Chapter 3, a physics based compact analytical current transport model has been deduced for a graphene nanoribbon (GNR) TFET. Two types of modeling approaches are considered and both of them are compared with quantum transport simulation for validation. The effect of width dependent GNR band gap is also studied on the performance of GNR TFET.

In order to overcome challenges associated with band gap engineering of graphene, a novel device architecture is proposed in Chapter 4 considering interlayer tunneling between two graphene layers separated by an insulating hex boron nitride tunneling barrier. This new type of transistor is called junctionless tunnel effect transistor (JTET). A compact physics based current transport model has been derived for the complete understanding of the operation of JTET and its potential for logic applications.

Graphene is a zero band gap semiconductor. Therefore, in order to study the suitability of JTET for large band gap semiconductors, Chapter 5 enumerates the device structure, operation and current transport model of a JTET considering molybdenum disulfide (MoS_2) and boron nitride (BN) vertical heterostructure. The promise of MoS_2 JTET for THz operation is also discussed in Chapter 5.

With an interest to study the suitability of traditional iTFET for energy efficient logic applications, physics based subthreshold slope model of a graphene and boron nitride (BN) based iTFET has been derived in Chapter 6.

In Chapter 7, the applications of GNR TFET and graphene JTET are studied for digital integrated circuit design using the Verilog-A hardware description language and SPICE environment. The compact physics based analytical models derived in Chapter 3 and 4 are incorporated in commercial Mentor Graphics® Tanner Tool through Verilog-A.

The conclusion and scope of future work are described in Chapter 8. The list of model parameters are provided in Appendix A. Appendix B and Appendix C enlist the complete Verilog-A codes for discrete n- type and p- type GNR TFET and graphene JTET, respectively. The list of published work is provided in Appendix D. The dissertation concludes with the short vita of the author.

1.8 References

[1] G. E. Moore, "Cramming more components onto integrated circuits," *IEEE Solid-State Circuits Society Newsletter,* vol. 11, pp. 33-35, 2006 Reprinted from *Electronics*, vol. 38, no. 8, pp. 114, 1965.

[2] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, "A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors," *Tech. Digest IEEE Int. Elect. Dev. Meetings*, pp. 11.6.1-11.6.3, 2003.

[3] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C. H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, "A 45nm logic technology with high-*k* metal gate transistors, strained silicon, 9 Cu interconnect

layers, 193nm dry patterning, and 100% Pb-free packaging," *Tech. Digest IEEE Int. Elect. Dev. Meetings*, pp. 247-250, 2007.

[4] C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. McFadden, B. McIntyre, J. Neirynck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki, and K. Mistry, "A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," *Symposium on VLSI Technology (VLSIT)*, pp. 131-132, 2012.

[5] R. Xie, P. Montanini, K. Akarvardar, N. Tripathi, B. Haran, S. Johnson, T. Hook, B. Hamieh, D. Corliss, J. Wang, X. Miao, J. Sporre, J. Fronheiser, N. Loubet, M. Sung, S. Sieg, S. Mochizuki, C. Prindle, S. Seo, A. Greene, J. Shearer, A. Labonte, S. Fan, L. Liebmann, R. Chao, A. Arceo, K. Chung, K. Cheon, P. Adusumilli, H. P. Amanapu, Z. Bi, J. Cha, H. C. Chen, R. Conti, R. Galatage, O. Gluschenkov, V. Kamineni, K. Kim, C. Lee, F. Lie, Z. Liu, S. Mehta, E. Miller, H. Niimi, C. Niu, C. Park, D. Park, M. Raymond, B. Sahu, M. Sankarapandian, S. Siddiqui, R. Southwick, L. Sun, C. Surisetty, S. Tsai, S. Whang, P. Xu, Y. Xu, C. Yeh, P. Zeitzoff, J. Zhang, J. Li, J. Demarest, J. Arnold, D. Canaperi, D. Dunn, N. Felix, D. Gupta, H. Jagannathan, S. Kanakasabapathy, W. Kleemeier, C. Labelle, M. Mottura, P. Oldiges, S. Skordas, T. Standaert, T. Yamashita, M. Colburn, M. Na, V. Paruchuri, S. Lian, R. Divakaruni, T. Gow, S. Lee, A. Knorr, H. Bu, and M. Khare, "A 7nm FinFET technology featuring EUV patterning and dual strained high mobility channels," *Tech. Digest IEEE Int. Elect. Dev. Meetings*, pp. 2.7.1-2.7.4, 2016

[6] H. Mertens, R. Ritzenthaler, A. Chasin, T. Schram, E. Kunnen, A. Hikavyy, L. Å. Ragnarsson, H. Dekkers, T. Hopf, K. Wostyn, K. Devriendt, S. A. Chew, M. S. Kim, Y. Kikuchi, E. Rosseel, G. Mannaert, S. Kubicek, S. Demuynck, A. Dangol, N. Bosman, J. Geypen, P. Carolan, H. Bender, K. Barla, N. Horiguchi, and D. Mocuta, "Vertically stacked gate-all-around Si nanowire CMOS transistors with dual work function metal gates," *Tech. Digest IEEE Int. Elect. Dev. Meetings*, pp. 19.7.1-19.7.4, 2016

[7] S. Natarajan, M. Agostinelli, S. Akbar, M. Bost, A. Bowonder, V. Chikarmane, S. Chouksey, A. Dasgupta, K. Fischer, Q. Fu, T. Ghani, M. Giles, S. Govindaraju, R. Grover, W. Han, D. Hanken, E. Haralson, M. Haran, M. Heckscher, R. Heussner, P. Jain, R. James, R. Jhaveri, I. Jin, H. Kam, E. Karl, C. Kenyon, M. Liu, Y. Luo, R. Mehandru, S. Morarka, L. Neiberg, P. Packan, A. Paliwal, C. Parker, P. Patel, R. Patel, C. Pelto, L. Pipes, P. Plekhanov, M. Prince, S. Rajamani, J. Sandford, B. Sell, S. Sivakumar, P. Smith, B. Song, K. Tone, T. Troeger, J. Wiedemer, M. Yang, and K. Zhang, "A 14nm logic technology featuring 2nd generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm^2 SRAM cell size," *Tech. Digest IEEE Int. Elect. Dev. Meetings,* pp. 3.7.1-3.7.3, 2014.

[8] R. Nathanael, V. Pott, H. Kam, J. Jeon, and T. J. K. Liu, "4-terminal relay technology for complementary logic," *Tech. Digest IEEE Int. Elect. Dev. Meetings,* pp. 1-4, 2009.

[9] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, "I-MOS: a novel semiconductor device with a subthreshold slope lower than kT/q," in *Tech. Digest IEEE Int. Elect. Dev. Meetings*, pp. 289-292, 2002.

[10] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Letters,* vol. 8, pp. 405-410, 2008.

[11] D. Newns, B. Elmegreen, X. Hu Liu, and G. Martyna, "A low-voltage high-speed electronic switch based on piezoelectric transduction," *J of App. Phys.,* vol. 111, p. 084509, 2012.

[12] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature,* vol. 479, pp. 329-337, 2011.

[13] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L. E. Wernersson, "Vertical InAs/GaAsSb/ GaSb tunneling field-effect transistor on Si with S = 48 mV/decade and Ion = 10 μA/μm for Ioff = 1 nA/μm at Vds = 0.3 V," *Tech. Digest IEEE Int. Elect. Dev. Meetings,* pp. 19.1.1-19.1.4, 2016

[14] C. Sandow, J. Knoch, C. Urban, Q. T. Zhao, and S. Mantl, "Impact of electrostatics and doping concentration on the performance of silicon tunnel field-effect transistors," *Solid State Elect.,* vol. 53, pp. 1126-1129, 2009.

[15] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science,* vol. 306, pp. 666-669, 2004.

[16] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, A. K. Geim, K. S. Novoselov, and L. A. Ponomarenko, "Field-effect tunneling transistor based on vertical graphene heterostructures," *Science,* vol. 335, pp. 947-950, 2012.

[17] C. Zener, "A theory of the electrical breakdown of solid dielectrics," *Proc. of the Royal Society of London A: Mathematical, Physical and Engineering Sciences,* vol. 145, pp. 523-529, 1934.

[18] O. M. Stuetzer, "Junction Fieldistors," *Proc. of the IRE,* vol. 40, pp. 1377-1381, 1952.

[19] L. Esaki, "New phenomenon in narrow germanium p-n junctions," *Phys. Rev.,* vol. 109, pp. 603-604, 1958.

[20] A. Srivastava and M. L. Gupta, "Transient behavior of a transistor-tunnel diode circuit," *Proc. of the IEEE,* vol. 64, pp. 1114-1116, 1976.

[21] A. B. Bhattacharyya and A. Srivastava, "Transient response of a transistor-tunnel diode hybrid combination with resistive feedback," *Proc. of the IEEE,* vol. 61, pp. 790-792, 1973.

[22] S. L. Sarnot, M. L. Gupta, A. Srivastava, and A. B. Bhattacharyya, "Tunnel-diode-transistor binary counter," *Proc. of the IEEE,* vol. 60, pp. 461-462, 1972.

[23] J. J. Quinn, G. Kawamoto, and B. D. McCombe, "Subband spectroscopy by surface channel tunneling," *Surface Science,* vol. 73, pp. 190-196, 1978.

[24] S. Banerjee, W. Richardson, J. Coleman, and A. Chatterjee, "A new three-terminal tunnel device," *IEEE Elect. Dev. Lett.,* vol. 8, pp. 347-349, 1987.

[25] E. Takeda, H. Matsuoka, Y. Igura, and S. Asai, "A band to band tunneling MOS device (B2BT-MOSFET) - A kind of 'Si quantum device'," *Tech. Digest IEEE Int. Elect. Dev. Meetings*, , pp. 402-405, 1988.

[26] T. Baba, "Proposal for surface tunnel transistors," *Japanese J. of Appl. Phys.,* vol. 31, pp. L455, 1992.

[27] W. M. Reddick and G. A. J. Amaratunga, "Silicon surface tunnel transistor," *Appl. Phys. Lett.,* vol. 67, pp. 494-496, 1995.

[28] J. Koga and A. Toriumi, "Negative differential conductance in three-terminal silicon tunneling device," *Appl. Phys. Lett.,* vol. 69, pp. 1435-1437, 1996.

[29] W. Hansch, C. Fink, J. Schulze, and I. Eisele, "A vertical MOS-gated Esaki tunneling transistor in silicon," *Thin Solid Films,* vol. 369, pp. 387-389, 2000.

[30] C. Aydin, A. Zaslavsky, S. Luryi, S. Cristoloveanu, D. Mariolle, D. Fraboulet, and S. Deleonibus, "Lateral interband tunneling transistor in silicon-on-insulator," *Appl. Phys. Lett.,* vol. 84, pp. 1780-1782, 2004.

[31] J. Appenzeller, Y. M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Phys. Rev. Lett.,* vol. 93, pp. 196805, 2004.

[32] D. Jena, "Tunneling transistors based on graphene and 2-D crystals," *Proc. of the IEEE,* vol. 101, pp. 1585-1602, 2013.

[33] S. Datta, H. Liu, and V. Narayanan, "Tunnel FET technology: A reliability perspective," *Microelectronics Reliability,* vol. 54, pp. 861-874, 2014.

[34] P. F. Wang, K. Hilsenbeck, T. Nirschl, M. Oswald, C. Stepper, M. Weis, D. Schmitt-Landsiedel, and W. Hansch, "Complementary tunneling transistor for low power application," *Solid State Elect.,* vol. 48, pp. 2281-2286, 2004.

[35] L. D. L. a. E. M. Lifshitz, *Quantum Mechanics*. Reading, Mass: Addison-Wesley, 1958.

[36] G. A. M. Hurkx, "On the modelling of tunnelling currents in reverse-biased p-n junctions," *Solid State Elect.,* vol. 32, pp. 665-668, 1989.

[37] J. Appenzeller, J. Knoch, M. T. Bjork, H. Riel, H. Schmid, and W. Riess, "Toward nanowire electronics," *IEEE Trans. on Elect. Dev.,* vol. 55, pp. 2827-2845, 2008.

[38] S. M. Sze and K. K. Ng, "Tunnel Devices," in *Physics of Semiconductor Devices*, ed: John Wiley & Sons, Inc., 2006, pp. 415-465.

[39] M. S. Lundstrom, "The MOSFET revisited: device physics and modeling at the nanoscale," *Proc. of IEEE International SOI Conference,* pp. 1-3, 2006.

[40] Q. Zhang, W. Zhao, and A. Seabaugh, "Low-subthreshold-swing tunnel transistors," *IEEE Elect. Dev. Lett.,* vol. 27, pp. 297-300, 2006.

[41] K. K. Bhuwalka, J. Schulze, and I. Eisele, "Performance enhancement of vertical tunnel field-effect transistor with SiGe in the δp + layer," *Japanese J. of Appl. Phys,* vol. 43, p. 4073, 2004.

[42] A. Sommerfeld and H. Bethe, "Handbuch der Physik von Geiger und Scheel," *Julius Springer- Verlag,* vol. 2, 1933.

[43] R. Holm, "The electric tunnel effect across thin insulator films in contacts," *J of App. Phys.,* vol. 22, pp.569-574, 1951.

[44] J. C. Fisher and I. Giaever, "Tunneling through thin insulating layers," *J of App. Phys.,* vol. 32, pp. 172-177, 1961.

[45] J. G. Simmons, "Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film," *J of App. Phys.,* vol. 34, pp. 1793-1803, 1963.

[46] A. K. Geim and I. V. Grigorieva, "Van der Waals heterostructures," *Nature,* vol. 499, pp. 419-425, 2013.

[47] A. Sciambi, M. Pelliccione, M. P. Lilly, S. R. Bank, A. C. Gossard, L. N. Pfeiffer, K. W. West, and D. Goldhaber-Gordon, "Vertical field-effect transistor based on wave-function extension," *Phys. Rev. B,* vol. 84, pp. 085301, 2011.

[48] R. M. Feenstra, D. Jena, and G. Gu, "Single-particle tunneling in doped graphene-insulator-graphene junctions," *J. of App. Phys.,* vol. 111, pp. 043711, 2012.

[49] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, M. I. Katsnelson, L. Eaves, S. V. Morozov, A. S. Mayorov, N. M. R. Peres, A. H. Castro Neto, J. Leist, A. K. Geim, L. A. Ponomarenko, and K. S. Novoselov, "Electron tunneling through ultrathin boron nitride crystalline barriers," *Nano Letters,* vol. 12, pp. 1707-1710, 2012.

[50] T. Georgiou, R. Jalil, B. D. Belle, L. Britnell, R. V. Gorbachev, S. V. Morozov, Y.-J. Kim, A. Gholinia, S. J. Haigh, O. Makarovsky, L. Eaves, L. A. Ponomarenko, A. K. Geim, K. S. Novoselov, and A. Mishchenko, "Vertical field-effect transistor based on graphene-WS_2 heterostructures for flexible and transparent electronics," *Nat Nano,* vol. 8, pp. 100-103, 2013.

[51] C. Zeng, E. B. Song, M. Wang, S. Lee, C. M. Torres, J. Tang, B. H. Weiller, and K. L. Wang, "Vertical graphene-base hot-electron transistor," *Nano Letters,* vol. 13, pp. 2370-2375, 2013.

[52] F. Driussi, P. Palestri, and L. Selmi, "Modeling, simulation and design of the vertical Graphene Base Transistor," *Microelectronic Engineering,* vol. 109, pp. 338-341, 2013.

CHAPTER 2

2D GRAPHENE AND 1D GRAPHENE NANORIBBON

2.1 Introduction

The physics of TFET requires a tunneling probability as high as unity ($T_{WKB} \approx 1$) for high performance. The expression of T_{WKB}, Eq. (1.11) in Chapter 1 suggests that, the band gap (E_G), effective mass (m^*) and the screening tunneling length (λ) need to be minimized for a high tunneling drive current and a steep subthreshold slope [1]. While the band gap (E_G) and the effective mass (m^*) are material properties, the screening tunneling length (λ) depends on device geometry, dimensions, doping profile and gate capacitances [2]. Moreover, Knoch et al. [3] reported that one dimensional tunneling is preferable compared to bulk three dimensional transport in TFET which can be observed in 2D materials. Hence, atomically thin graphene becomes suitable for TFET study.

Since graphene is a two dimensional atomically thin material, the synthesis and growth are significantly different from traditional bulk three dimensional materials. While the current process technology for CMOS integrated circuit is mature, graphene process technology is still under development and extensive research have been carried out in this direction. Moreover, the challenges associated in obtaining large area single crystal graphene and bi-layer graphene are also present. In this Chapter, graphene's synthesis and growth mechanism have been studied followed by electronic structure, properties and design criteria for TFET applications.

2.2 Introduction to Graphene

Graphene is a monolayer of carbon atoms packed into a dense hexagonal honeycomb crystal structure (Fig. 2.1(a)), which can be separated and viewed as an individual atomic plane extracted from graphite (Fig. 2.1(b)) or as an unrolled single wall carbon nanotube (Fig. 2.1(c))

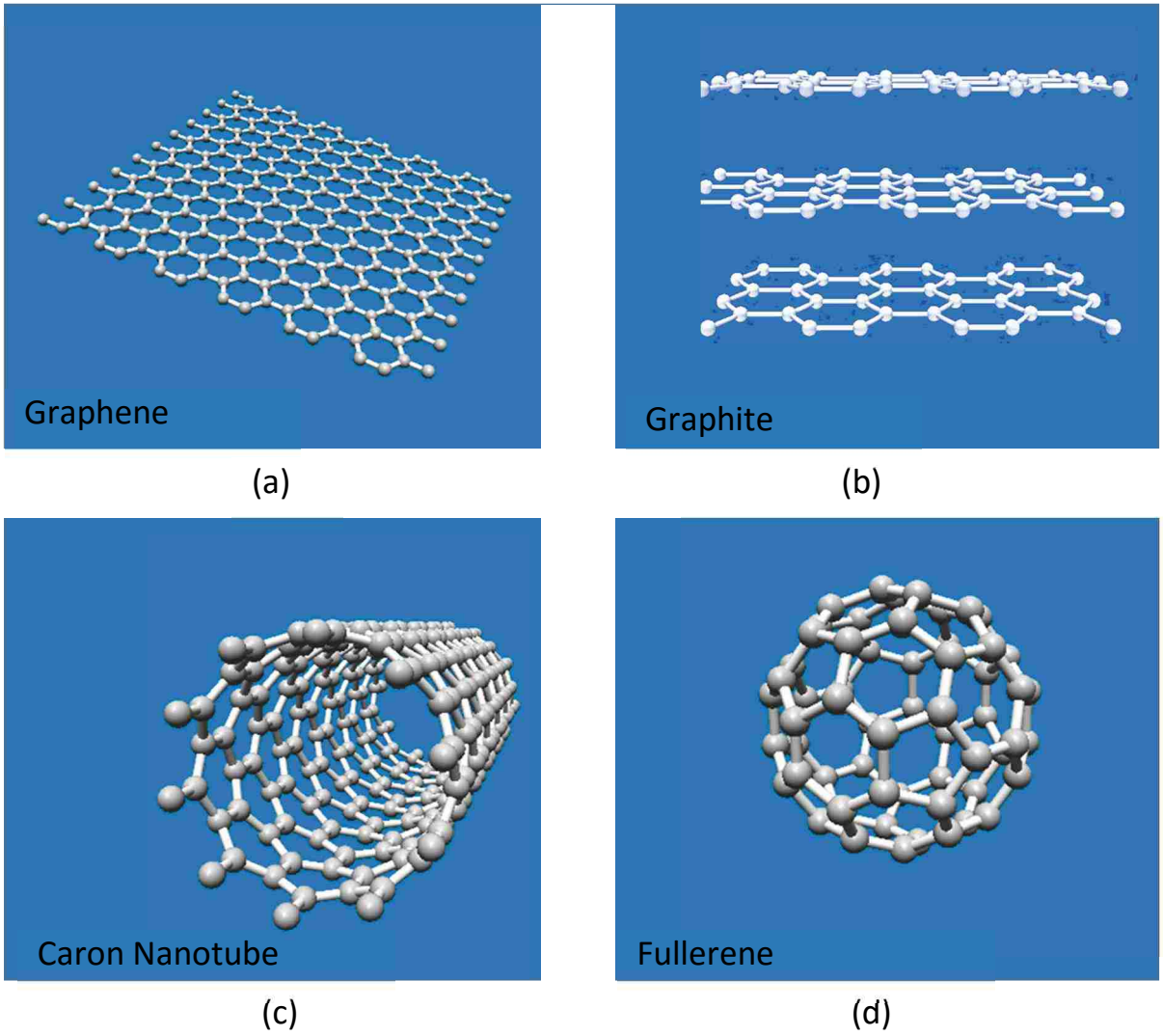


Figure 2.1: Different allotropes of carbon in different dimensions (a) two dimensional (2D) atomically thick graphene, (b) three dimensional (3D) graphite, (c) one dimensional (1D) carbon nanotube and(d) zero dimensional (0D) fullerene.

or as a giant flat fullerene molecule (Fig. 2.1(d)) [4]. Single layer of graphite or graphene was presumed not to exist in free stable form until 2004 when Novoselov et al. [5] experimentally first isolated single layer graphene by micromechanical cleavage technique (peeling off repeatedly from graphite crystal using adhesive scotch tape) and reported their seminal work on the field effect study of such atomically thin carbon film. However, the historical background of graphene goes back to Brodie [6] in 1859 who discovered the lamellar structure of thermally reduced graphene oxide, a multilayer carbon oxide material often used as an analogy to graphene. Kohlschutter and Haenni [7] in 1918 studied the properties of graphene oxide papers, a composite material with graphene skeleton. Three decades later, Reuss and Vogt [8] in 1948 reported the first transmission emission microscopy of few layers graphite dry residue which is structurally a multi-layer graphene. This remained the best observation of graphene for several decades. The theoretical groundwork of graphene also goes back to Wallace [9] who in 1947 first described the zone structure, number of free electrons and conductivity of a single hexagonal layer of graphite.

Between late 1970s to early 1990s, major attention was focused to fullerenes (buckyballs) and carbon nanotubes which were discovered in 1985 [10] and 1991 [11], respectively. However, some key features of currently known formal graphene were reported during that period. Semenoff [12] found in 1984 that the wave functions of graphene are similar to the solutions of relativistic Dirac equation. Finally in 1987, Mouras et al. [13] coined the term “graphene” for single crystalline 2D carbon allotrope, before which graphene was commonly termed as “thin graphite lamellae.” Surprisingly, even before the experimental observation of two different types of edge states (zigzag and armchair) in graphene nanoribbon (a nanometer dimensional form of

infinite graphene sheet), Nakada et al. [14] in 1996 extensively and accurately predicted their edge states with corresponding energy band structure.

From 2004 to 2008, research on graphene spurred tremendously considering graphene as an exciting condensed matter physics problem. Novoselov et al. [15] found that the electron transport in graphene is governed by relativistic Dirac equation where the charge carriers resembles Dirac fermions, relativistic particles with zero rest mass (massless particle) with an effective speed in the range of light. Moreover, Katsnelson et al. [16] reported that, by using electrostatic barriers in single and bi-layer graphene, the massless Dirac fermions in graphene demonstrates Klein tunneling which is the unhindered penetration of relavistic particles through a wide potential barrier [16]. The quantized quantum Hall conductance, which is generally observed at low temperature and strong magnetic field, was also observed in graphene at room temperature [17]. Bolotin et al. [18] found that the low temperature carrier mobility is three times that of the best semiconductor. Thermal conductivity of graphene is also reported to be at least twice as large as that of copper for similar geometry [19]. The electron mobility in suspended graphene is found as 200,000 cm^2/V-s which is 143 times greater than that of Si (1400 cm^2/V-s at 300 K) [20, 21].

2.3 Synthesis of Graphene

Different methods are used for the synthesis and deposition of graphene. Figure 2.2 summarizes some of the methods used for graphene synthesis. One of the popular methods is the mechanical exfoliation from highly oriented pyrolytic graphite (HOPG) crystal. The other is through high temperature thermal chemical vapor deposition (CVD). Compared to non-scalable mechanical exfoliation, CVD method provides high quality scalable production of atomically

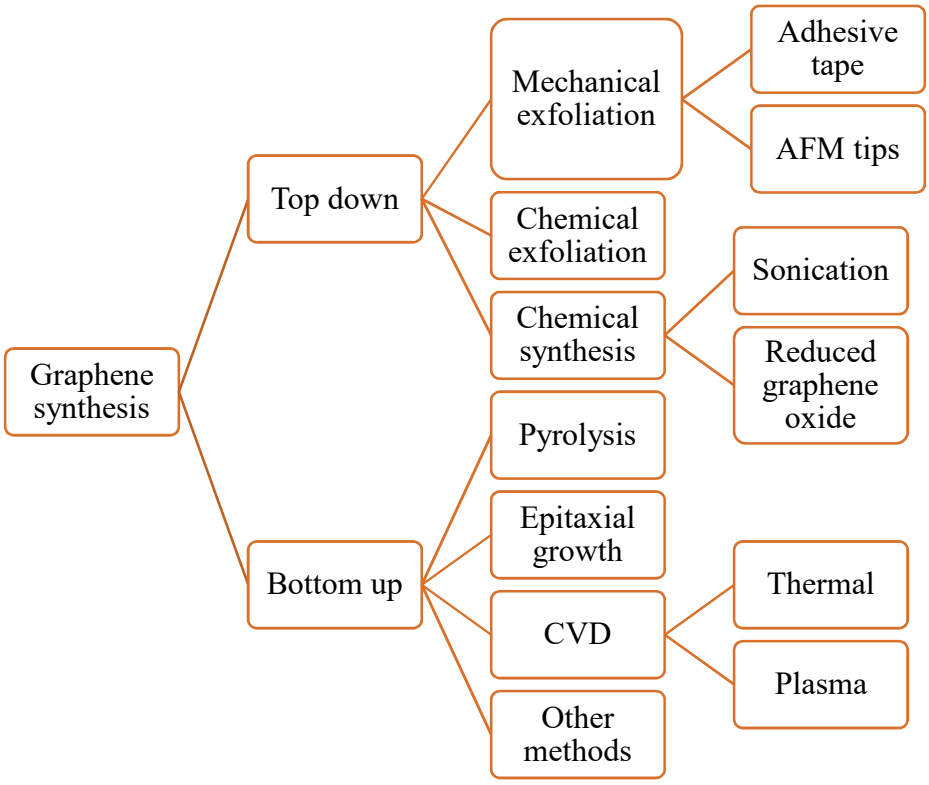


Figure 2.2: Synthesis methods for graphene.

thin graphene. Using an adhesive scotch tape to repeatedly peel off layer by layer is the first technique adopted by Novoselov et al. [5]. However, large-area graphene fabrication using mechanical cleaving is a serious challenge which limits the feasibility of this process for industrialization. Hernandez et al. [22] reported the exfoliation of pure graphite in N-methyl-pyrrolidone by a simple sonication process. The reported exfoliated graphene films showed high-quality synthesis at yields of ~1%. Hazra et al. [23] in 2011 demonstrated plasma-assisted etching of graphite to form multilayered graphene and monolayer graphene in 2011. Direct graphene synthesis using electrochemical methods was reported by Liu et al. [24]. The method is environment friendly and leads to the production of a colloidal suspension of imidazolium ion–functionalized graphene sheets by direct electrochemical treatment of graphite. In 2006, Somani et al. [25] first attempted for CVD grown graphene on Ni using camphor (terpinoid, a white transparent solid of chemical formula $C_{10}H_{16}O$) as the precursor material. However, using TEM, they found that the planar few-layer graphene consists of ~35 layers of stacked single graphene sheets with an interlayer distance of 0.34 nm. Using methane (CH_4), Li et al. [26, 27] studied growth of large scale ($1cm^2$) single layer graphene on Ni and Cu substrates which is so far the most widely used method employed for obtaining CVD graphene. Further, they developed a graphene transfer method by solution etching of Cu and then transferring of the floated graphene onto any substrate. Bae et al. [28] in 2010 produced a 30-inch scaled graphene sheet using roll to roll production on a Cu substrate and transferred by wet chemical etching of Cu.

A typical CVD process for deposition of graphene consists of four steps: a) adsorption and catalytic decomposition of precursor gas, b) diffusion and dissolution of decomposed carbon species on the surface and metal bulk, c) dissolved carbon atoms segregation onto metal surface and d) surface nucleation and growth of graphene [29]. However, in case of metals having poor

carbon affinity such as copper, the decomposition of carbon precursor is followed by direct formation of graphene on copper where dissolution and subsequent segregation of carbon atoms are prohibited. The low solubility of the carbon in copper also makes the growth process predominantly self-limiting to single layer graphene [26]. The most common carbon precursor for graphene growth is methane (CH_4) which has a strong C-H bond (440 $kJmol^{-1}$). For this strong C-H bond in methane, its thermal decomposition occurs at very high temperature (> 1200^o C). However, such a high temperature is not easily obtained in typical thermal CVD set-up. In order to reduce the decomposition temperature of methane, different transition metal catalysts (e.g. Fe, Co, Ni, Cu) are widely used and the growth of graphene on such metals can be obtained at low temperatures (< 900^o C).

During the annealing step, the catalyst surface is covered with molecular hydrogen which can be referred as dissociative chemisorption of H_2 on the metal surface [29]. Compared to Ni, Cu shows higher hydrogen solubility. This process is followed by the catalytic decomposition of the carbon precursors on the metal surface. At this stage, the competitive process between the dissociative chemisorption of H_2 and physical adsorption and dehydrogenization of CH_4 on catalyst surface occurs. With suitable choice of thermodynamic parameters, the chemical potential of surface carbon atoms are maintained lower than the carbon in gas phases which further helps to form stable graphitic rings and grow into large graphitic structures up to graphene formation [29]. Once such nucleation of graphene structure is stable on the metal surface, the growth mechanism is followed by attachment of carbon species onto graphene edges. The quality, uniformity and surface coverage on metal substrate depends on suitable choice of high temperature, pressure and exposure time. As the growth time increases, the individual graphene domains progressively increase in size and coalesce into a continuous layer.

Nevertheless, after the growth and formation of a continuous layer, further exposure to carbon precursor does not lead to deposition of multi-layered graphene due to the self-limiting process as described earlier in case of copper substrate. It is important to note that the graphene growth on copper is surface related and does not occur due to out-diffusion from bulk. Using the isotope labeling, Li et.al [27] demonstrated that the Raman modes of ^{12}C and ^{13}C isotopes differ in energy which provided a substantial understanding of the gradual increment of the graphene layer growth laterally on copper surface providing critical structural information of graphene growth.

Figure 2.3(a) shows floating graphene film on Cu etchant $Fe(NO_3)_3$ after Cu has been fully etched. Prior to that, CVD graphene was grown on Cu foil of 25 μm thick. Fig. 2.3(b) shows the floating graphene transferred on SiO_2 substrate. The optical contrast confirms single layer graphene compared to SiO_2. Fig. 2.3(c) shows Raman spectroscopy of graphene transferred on SiO_2 substrate. A 632 nm laser is used for Raman spectroscopy. The graphene on Cu has been deposited using the NanoCVD reactor (at EMDL in the Electrical and Computer Engineering division at LSU). A small D peak and a dominant 2D peak compared to the G peak confirm the growth of single layer graphene on Cu foil.

The CVD rector for the growth and synthesis of graphene on metal substrate is cold wall resistive heater type system as shown in Fig. 2.4(a) and 2.4(b). The gas flow process and standard recipe following the work of Bointon et al. [30] are depicted in Fig. 2.4(c) and 2.4(d), respectively. Graphene grown through CVD system is typically polycrystalline in nature where a lot of graphene seeds nucleates and coalesce. Hence, the growth of graphene film on metallic substrate is twofold, a) the nucleation and b) growth [29].

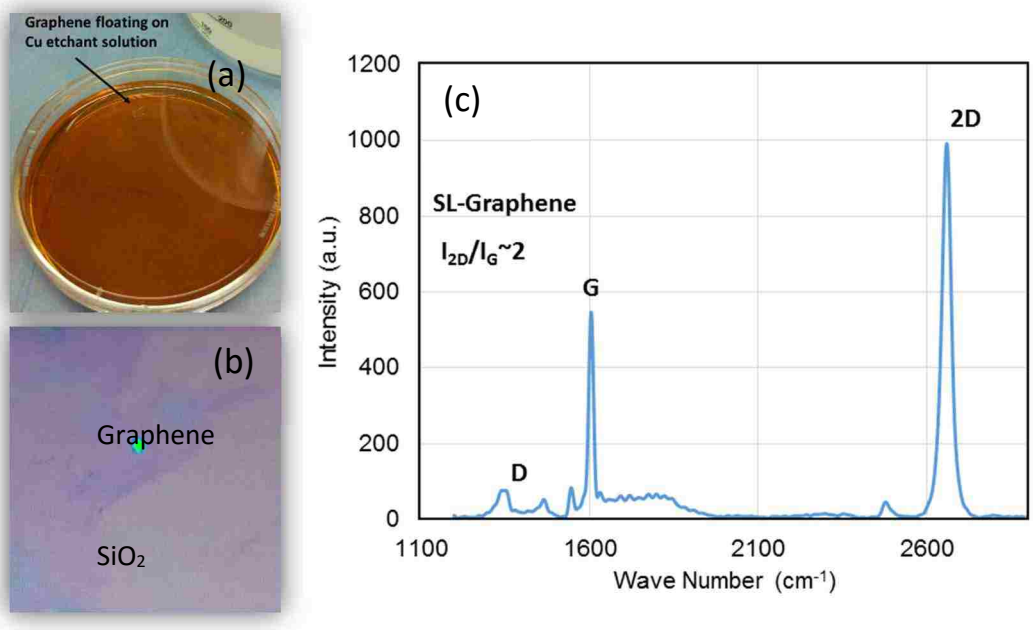


Figure 2.3: (a) CVD grown graphene floating on Cu etchant after Cu has been fully etched, (b) transferred on SiO_2 and (c) Raman spectroscopy of single layer graphene after transferred on SiO_2.

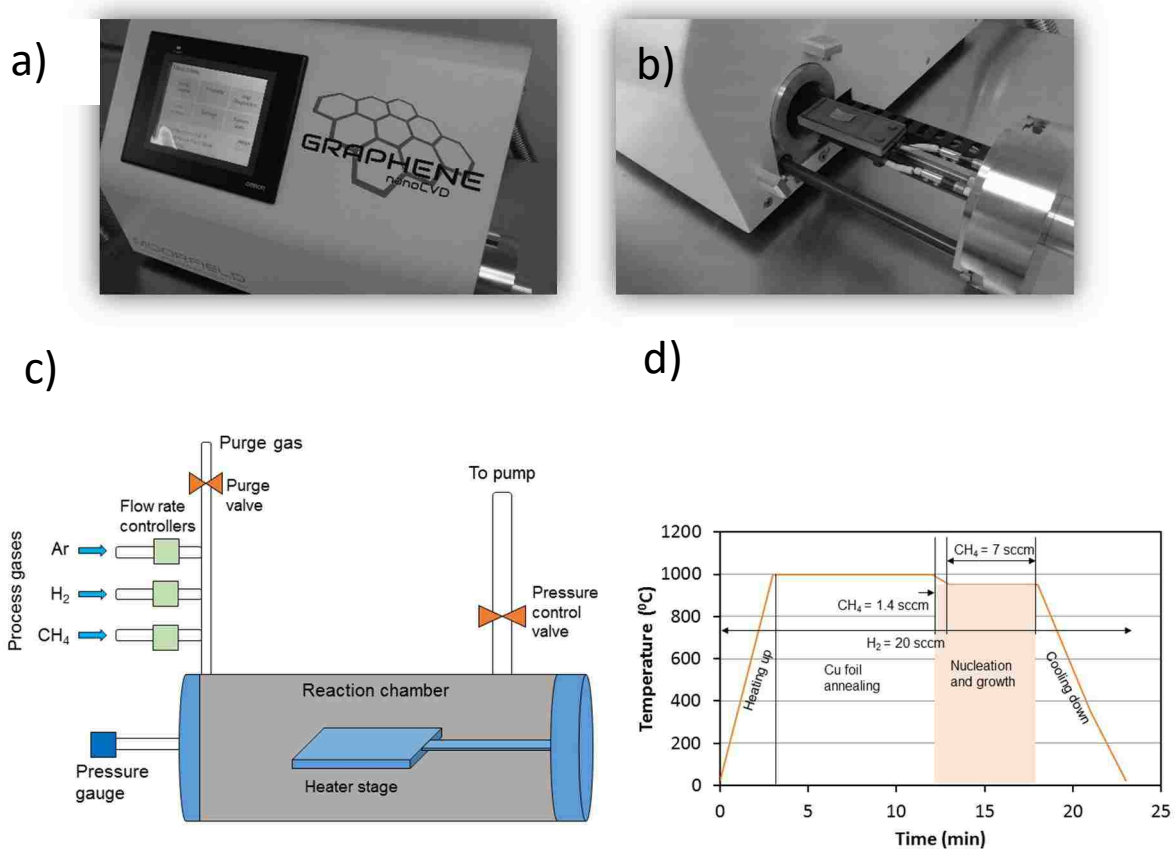


Figure 2.4: Cold wall resistive heater type chemical vapor deposition system by Moorefield Nanotechnology® at EMDL. a) CVD assembly, b) heater and chamber assembly, c) schematic of gas flow process and d) standard growth condition for single layer graphene [30].

Moreover, due to self-limiting catalytic decomposition of carbon molecules in metal substrates through diffusion and adsorption, controlled growth of bilayer graphene is challenging. Therefore, as the process technology for graphene continues, the growth of large area single crystal as opposed to polycrystalline graphene and controlled synthesis single/poly crystalline bilayer graphene is necessary.

Recently, Hao et al. [31] have demonstrated that, by controlling the oxygen on copper substrate centimeter scale graphene single crystal can be obtained repeatedly. Traditionally the size of single crystals in a polycrystalline graphene sheet is few micro-meter only. Using cold wall CVD system, Misekis et al. [32] have grown millimeter scale graphene sheet on copper foil at a time of 30-60 minutes compared to traditional hot wall CVD system which requires 3-7 hours of growth time. Nevertheless, the growth of more than centimeter scale graphene single crystal is still challenging. Many attempts to grow bilayer graphene on copper have been carried out, however, majority of these studies have resulted small domain of bilayer graphene with a large variation in the domain size [33]. Since, an electric field tunable band gap can be obtained in a bilayer graphene, it is essential to produce uniform and large domain single crystal bilayer graphene sheet. Hao et al. [33] recently have shown that an oxygen activated CVD process can produce as large as half-milimeter size bernal A-B stacked bilayer graphene singe crystal on copper. Mu et al. [34] have shown that, by controlling the partial pressure of hydrogen during the nucleation stage, bilayer graphene can be grown on copper foil.

As part of growth studies of single layer and bilayer graphene in this dissertation, control of chamber pressure during growth period has been modified for obtaining bilayer graphene on copper foil. Detail of the process variability effect is provided in the following section.

2.4 Growth of Multi-layer Graphene Film on Copper

Chen et al. [35] proposed that by switching hydrogen pressure between high and low would result growth of bilayer graphene. Similar results were produced by Lu et al. [36] where by simply controlling the hydrogen pressure bilayer graphene has been grown. Following the work of [35] and [36], the chamber pressure has been modified for obtaining multi-layer graphene using the cold wall resistive heater CVD at EMDL. However, compared to the earlier reported growth time, the process adopted here not only requires less time but also becomes economic. Figure 2.5(a) shows the optical image of a copper foil processed under the similar growth as described in the work of Bointon et al. [30] for a chamber pressure of 20 Torr during the growth period. With the carbon precursor CH_4 = 10%, H_2 = 5% and Ar = 85% for 120 seconds and a chamber pressure of 20 Torr at 1000^{o}C, both the bilayer and multi-layer graphene have been observed along with single layer. The Raman spectroscopy performed at different areas as observed in Fig. 2.5(a), confirms the observation of bilayer and multi-layer graphene on copper foil which are shown in Fig. 2.5(b) and 2.5(c). Note, that with a growth time of only 120 seconds, the total processing time for such graphene sheet on copper foil was only 20 minutes which is shorter than the earlier reported growth time of Bointon et al. [30]. From the optically contrast image of Fig. 2.5(a), difference in numbers of layers of graphene can be easily understood as well. Compared to the lighter area, the darker area represents more number of graphene layers. The Raman peaks studied in the comparatively less dark area and shown in Fig. 2.5(b) reveals that graphene is bilayer with an extensive level of defects or hydrogenated edges. A strong D peak compared to both G and 2D peak is a characteristic feature of a graphene film with defects or halogen terminated edges. A I_{2D}/I_G ratio near 1 also reveals that the area is bilayer [37].

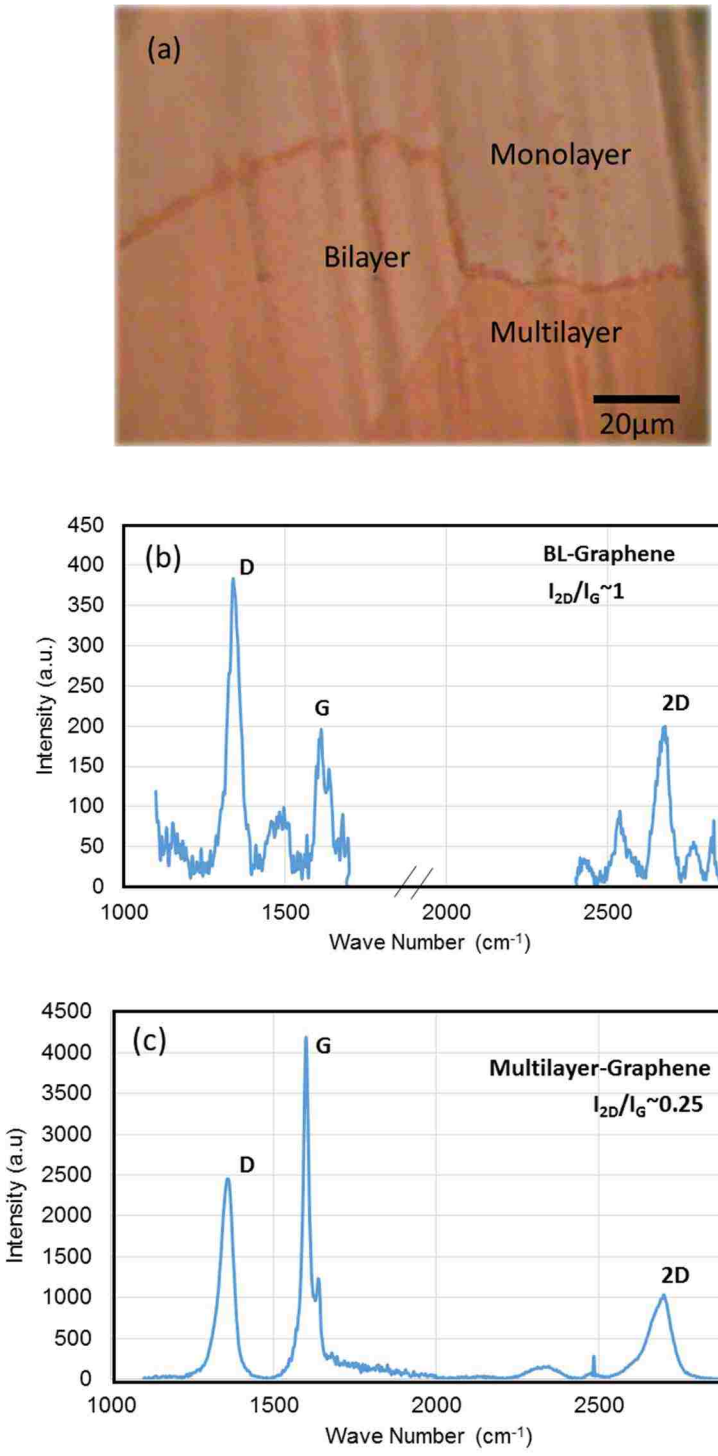


Figure 2.5: Raman spectroscopy of graphene grown on copper foil at 20 Torr pressure, a) optical image showing three different regions, b) Raman peaks for bilayer graphene area and c) Raman peaks for multilayer graphene area.

Further, the Raman analysis of the most darker region confirms that the graphene is multilayer as shown in Fig. 2.5(c). With a I_{2D}/I_G ratio of near 0.25 confirms that the graphene in the region is more than 10 layers and similar to graphitic carbon [37]. The D peak for this region is low which informs comparatively less defects or hydrogen terminated edges compared to the Raman spectra of Fig. 2.5(b).

In order to analyze the effect of growth or exposure time on the number of graphene layers in similar growth condition, the copper foil was exposed for 300s instead of only 120s. Figure 2.6(a) shows a sample area of the grown graphene for such growth condition. It has been found that, compared to uniform planar graphene sheet, graphene growth for such long period of time results not only multi-layer graphene, but also a graphitic carbon with extensive level of hydrogen terminated edges. For this reason, the Raman peaks obtained for such region of hydrogenated graphitic carbon reveals a strong D peak, and poor I_{2D}/I_G ratio which is shown in Fig. 2.6(b). Note, compared to the 0.25 ratio of $I_{2D}/I_{G,}$ the sample exposed for 300s provides only a I_{2D}/I_G ratio of 0.19. Therefore, based on the results obtained through Fig. 2.5 and Fig. 2.6, an optimized growth period is required for large area bilayer graphene synthesis. Nevertheless, further process variation of CH_4 and H_2 concentration, growth temperature and chamber pressure would provide difference in graphene quality which are left as a scope of future work.

2.5 Electronic Structure of Graphene

In this section, a brief description of graphene electronic structure has been discussed. The carbon atoms in graphene plane forms strong σ-covalent bonds with three neighboring carbon atoms by in-plane sp^2 hybridization. The fourth bond is in the form of a π-bond in z-direction [4]. Electrons from this bond can move freely in the delocalized π-electronic system referred as the π-band and π*-band. The hexagonal lattice can be drawn as shown in Fig. 2.7(a)

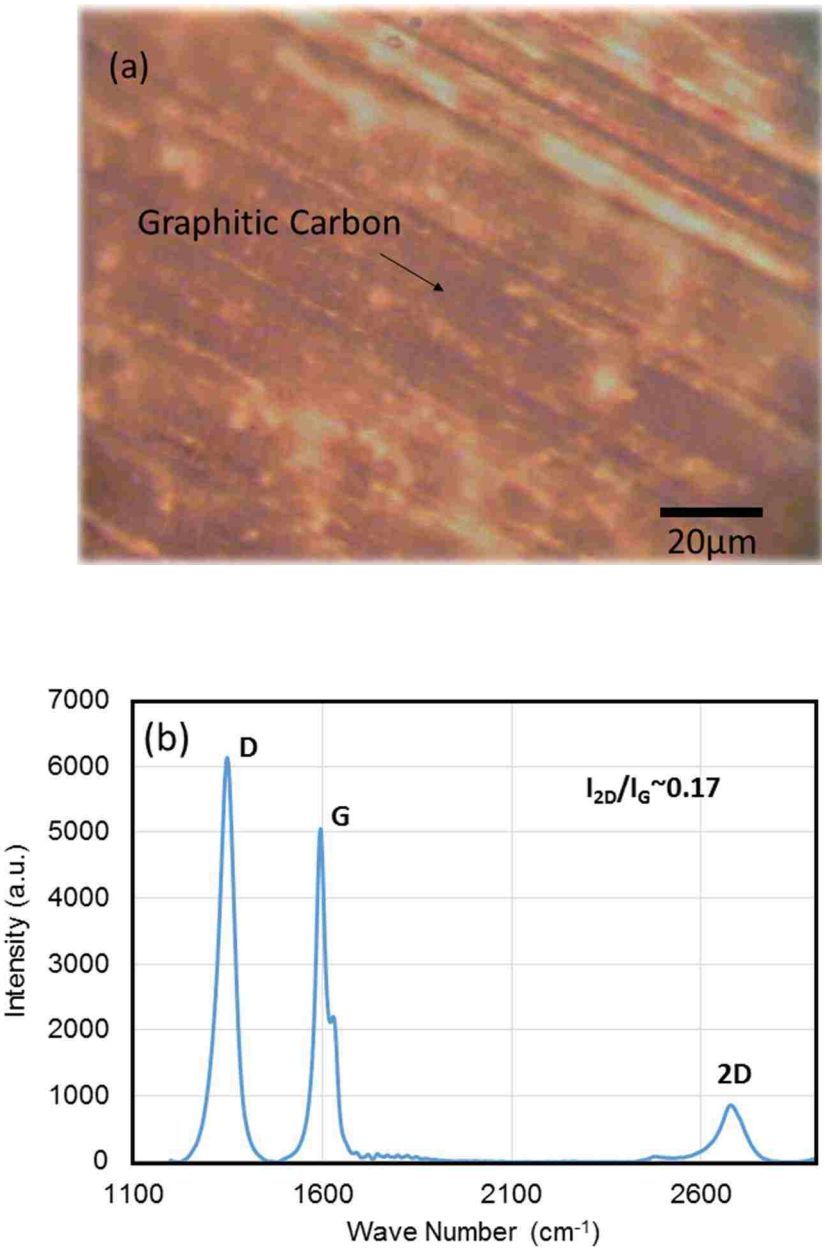


Figure 2.6: a) Optical image of graphitic carbon grown on copper after an exposure time of 300s at a chamber pressure of 20 Torr and b) Raman spectroscopy of the dark area marked with arrow.

and can be seen similar to a parallelogram lattice with a basis of two atoms per unit cell. The lattice constants can be written as follows [4]:

$$\mathbf{a}_1 = \frac{a}{2}\left(3, \sqrt{3}\right), \quad \mathbf{a}_2 = \frac{a}{2}\left(3, -\sqrt{3}\right) \tag{2.27}$$

where a ≈ 1.42 A^0 is the carbon-carbon distance. The reciprocal-lattice vectors are given by,

$$\mathbf{b}_1 = \frac{2\pi}{3a}\left(1, \sqrt{3}\right), \quad \mathbf{b}_2 = \frac{2\pi}{3a}\left(1, -\sqrt{3}\right) \tag{2.28}$$

The two points K and K′ are at the corners of the Brillouin zone (BZ). They are referred as Dirac points. The positions of these two points in a momentum space are defined as follows:

$$K = \left(\frac{2\pi}{3a}, \frac{2\pi}{3\sqrt{3}a}\right), \quad K' = \left(\frac{2\pi}{3a}, -\frac{2\pi}{3\sqrt{3}a}\right) \tag{2.28}$$

The three nearest-neighbor vectors in real space are given by,

$$\boldsymbol{\delta}_1 = \frac{a}{2}(1, \sqrt{3}), \ \boldsymbol{\delta}_2 = \frac{a}{2}(1, -\sqrt{3}), \ \boldsymbol{\delta}_3 = -a(1, 0) \tag{2.29}$$

Using the expressions of lattice vector and reciprocal lattice constants, the nearest neighbor tight binding Hamiltonian of graphene results in the following linear dispersion [4],

$$E(\vec{k}) = \pm t\sqrt{1 + 4\cos\frac{\sqrt{3}k_x a}{2}\cos\frac{k_y a}{2} + 4\cos^2\frac{k_y a}{2}} \tag{2.30}$$

Here, t is nearest-neighbor hopping energy (hopping between different sublattices). The plus sign applies to the upper (π^*) and the minus sign the lower (π) band corresponding to the conduction and valence bands, respectively. It is clear from Eq. (2.30) that the spectrum is symmetric around zero energy where both the conduction and valence bands touch each other. Figure 2.8 shows the full band structure of graphene first Brillouin zone [4]. It can be seen that the energy dispersion around the band edges of graphene is linear. Plots are shown for the electron energy dispersion

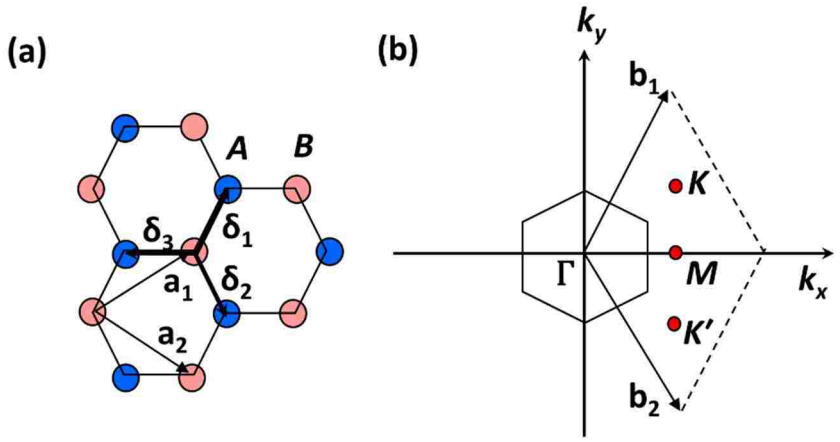


Figure 2.7: (a) Hexagonal lattice structure of graphene consisting of two atoms A and B in a unit cell. $\mathbf{a_1}$ and $\mathbf{a_2}$ shows direction of the lattice vectors in the unit cell and (b) reciprocal lattice vectors $\mathbf{b_1}$ and $\mathbf{b_2}$ in the first Brillouin zone.

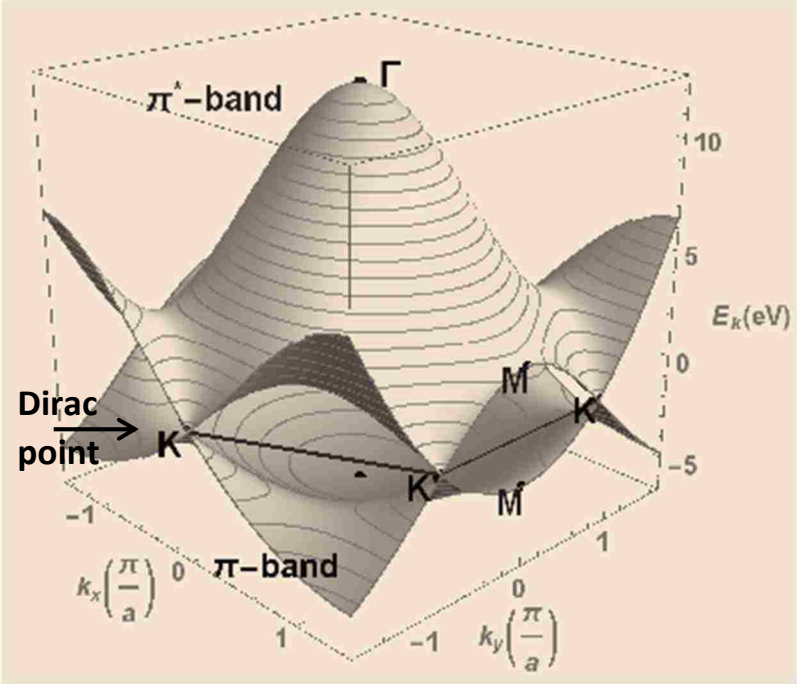


Figure 2.8: Dispersion relation of graphene first Brillouin zone shown in reciprocal lattice space (k-space) with both x and y axis normalized with π/a. **K** and **K´** are the symmetric points.

for π and π*-bands in the first Brillouin zones as contour plots at equidistant energies and as pseudo-3D representations for the 2D structures. The demonstrated linear dispersion shows that the conduction and the valence bands touches each other at the charge neutrality point or more commonly known as the Dirac point shown by the arrow in Fig. 2.8 at the symmetric K and K′ points which has been plotted in Wolfram computational dynamic player tool. This shows that the band gap in graphene to be zero or specifically graphene is referred as a zero bandgap semiconductor or a semimetal.

2.6 Band Gap Engineering of Graphene

Graphene is a zero band gap semiconductor or a semi-metal. This results in transistors made from graphene difficult to turn off. In order to obtain appropriate switching behavior using graphene based transistors, a significant band gap is required which leads to the study of band gap engineering of graphene. In this section, some methods for obtaining a band gap in graphene are discussed. Figure 2.9 shows a summary of different ways of obtaining band gap in graphene.

Castro et al. [38] reported that if electric field is applied to a bilayer graphene vertically, then this opens a band gap, making graphene as a field tunable semiconductor. Both the theoretical and experimental considerations have shown that for a field of few 10^4 kV/cm could open a band gap of 250 meV. Recently, two unconventional methods have been reported namely: 1) graphene growth on MgO [39] and 2) by irradiation of graphene with an ion beam [40]. Being atomically thin, interaction of graphene with underneath substrate plays critical role on graphene electronic properties. Giovannetti et al. [41] reported in 2007 the ab-initio density functional theory (DFT) based electronic structure calculation of graphene on hex-boron nitride substrate, results in a band gap 53 meV. Recently, Nevius et al. [42] reported growth of semiconducting graphene on highly ordered SiC substrate along the [0001] direction of the SiC hexagonal crystal

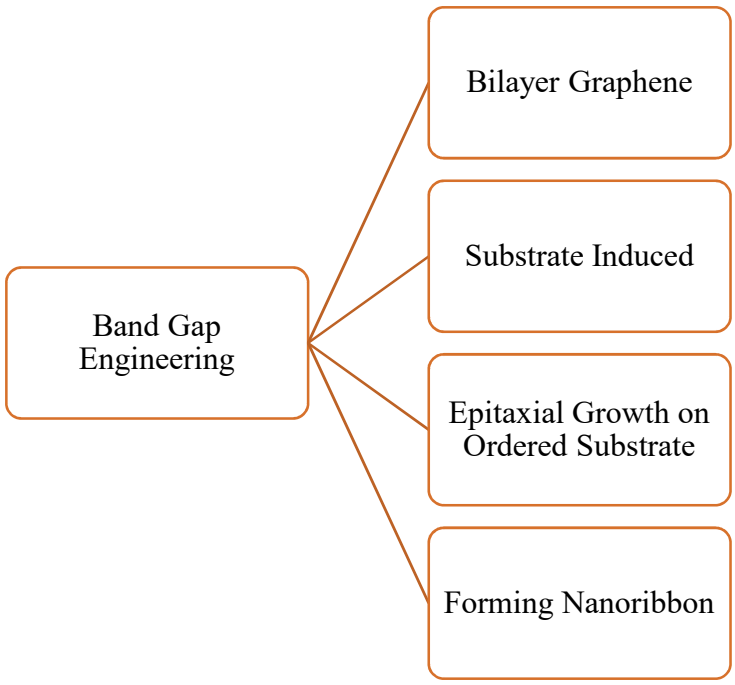


Figure 2.9: Energy band gap engineering methods used for graphene.

pack (HCP). Their measured band gap of single layer graphene of 0.55 eV using ARPES was the highest recorded so far. The most common method for opening a band gap in graphene is to confine the infinite graphene sheet into narrow ribbons where the ribbon length is much greater than itswidth. Due to the quantum confinement of the electrons in nanoribbon, a measureable finite band gap opens up [43, 44]. For using graphene in transistor level operation, it is necessary to have a finite band gap of the material and graphene nanoribbon (GNR) helps in this regards significantly.

2.7 Energy Band Gaps of GNR

In GNR, the band gap is directly proportional to the inverse of the width [43]. It has been predicted that, GNR with width scaled down to 2nm should provide a gap in excess of 1eV [43]. It is important to note that, the origin of band gap is still under debate. Apart from considering the lateral confinement as the origin of band gap, it has been suggested that other notable effect such as Coulomb blockade is responsible for the formation of such band gap [45]. Han et al. [44] experimentally demonstrated lithographically patterned GNR with width dependent band gap. One of the most effective method for obtaining GNR is to unzip a single wall carbon nanotube with bottom-up chemical approach [46]. Compared to lithographically patterned GNR, this method provides smooth defect free GNR [47].

Energy band gaps in GNR is also dependent on the edge types along which the transport occurs. Figure 2.10 shows a top view of a GNR with two types of edges, i.e. armchair and zigzag edges. Localized edge states at the Fermi level are observed in zigzag edge nanoribbon whereas such edge states are absent in armchair edge nanoribbons. These localized states are important as these infer to localized wave functions at the GNR edges and contribute to antibonding properties of GNR and electronic structure [14]. For the GNR shown in Figure 2.10, the nano-

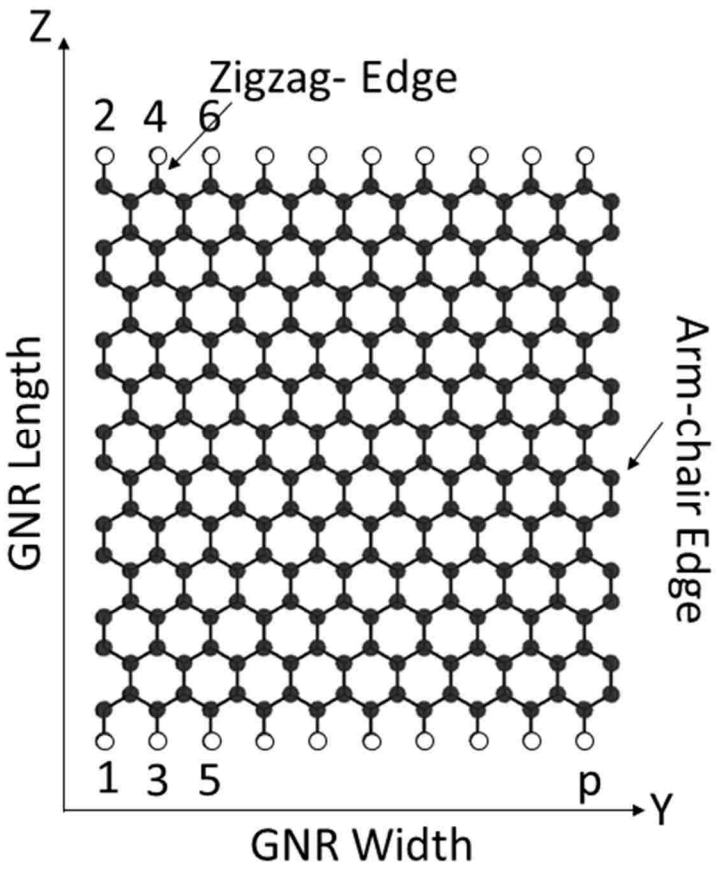


Figure 2.10: Graphene nanoribbon (GNR) were p is an integer denoting the p^{th} atom along the width.

ribbon width varies along the Y direction and length along Z direction. The variable p is an integer. The numbering of atoms (1, 2, 3… *p*) along the GNR width are also shown in Fig. 2.10.

The notation of chirality used for GNR is expressed as (*p, 0*) where '*p'* is the number of carbon atoms on each ring of unrolled nanotube in armchair or zigzag direction and *'0'* refers to zero atoms deviating from the direction of '*p*.' Generally '*p*' is defined in terms of any of the configurations from 3*N*, 3*N*+1 or 3*N*+2 along the GNR width. Note, *p* is the total number of atoms considering both sides of the nanoribbons whereas *N* is an integer. Therefore, in a (*4,0*) armchair GNR, $p = 4$ with 3*N*+1 configuration considering $N = 1$. Whereas in a (*5,0*) armchair GNR, $p = 5$ with a 3*N*+2 configuration considering $N = 1$. For (*6,0*) armchair GNR, $p = 6$ with 3N configuration considering $N = 2$.

Energy band gap of GNR, both armchair and zigzag, differs depending on the method of calculation. Electronic structure of GNR is modeled traditionally by the simple tight binding (TB) approximation based on π-bonded p_z -orbital electrons or usually studied by Dirac equation of massless particle considering effective speed of light (~10^6 m/s). Such assumptions lead to conclude armchair GNR to be either metallic or semiconducting. Results obtained by TB approximation considering nearest neighbor hopping integral of 2.7 eV show that armchair GNR is metallic for $p = 3N+2$ and semiconducting for both $p = 3N$ and $p = 3N+1$ configurations [48]. Basically the hierarchy of energy band gap is maintained as $\Delta_{3N+1} > \Delta_{3N} > \Delta_{3N+2}$ (**= 0 eV**), Δ being the energy gap where *N* is an integer. Figure 2.11 shows the width dependent band gap, calculated using nearest neighbor tight binding Hamiltonian considering p_z orbital encoded in "CNTbands", available in the open source simulation framework Nanohub [49]. In Fig. 2.11, both (*4,0*) and (*6,0*) are semiconducting. Zero band gap is observed for (*5,0*) GNR which is a 3*N*+2 configuration for $N = 1$.

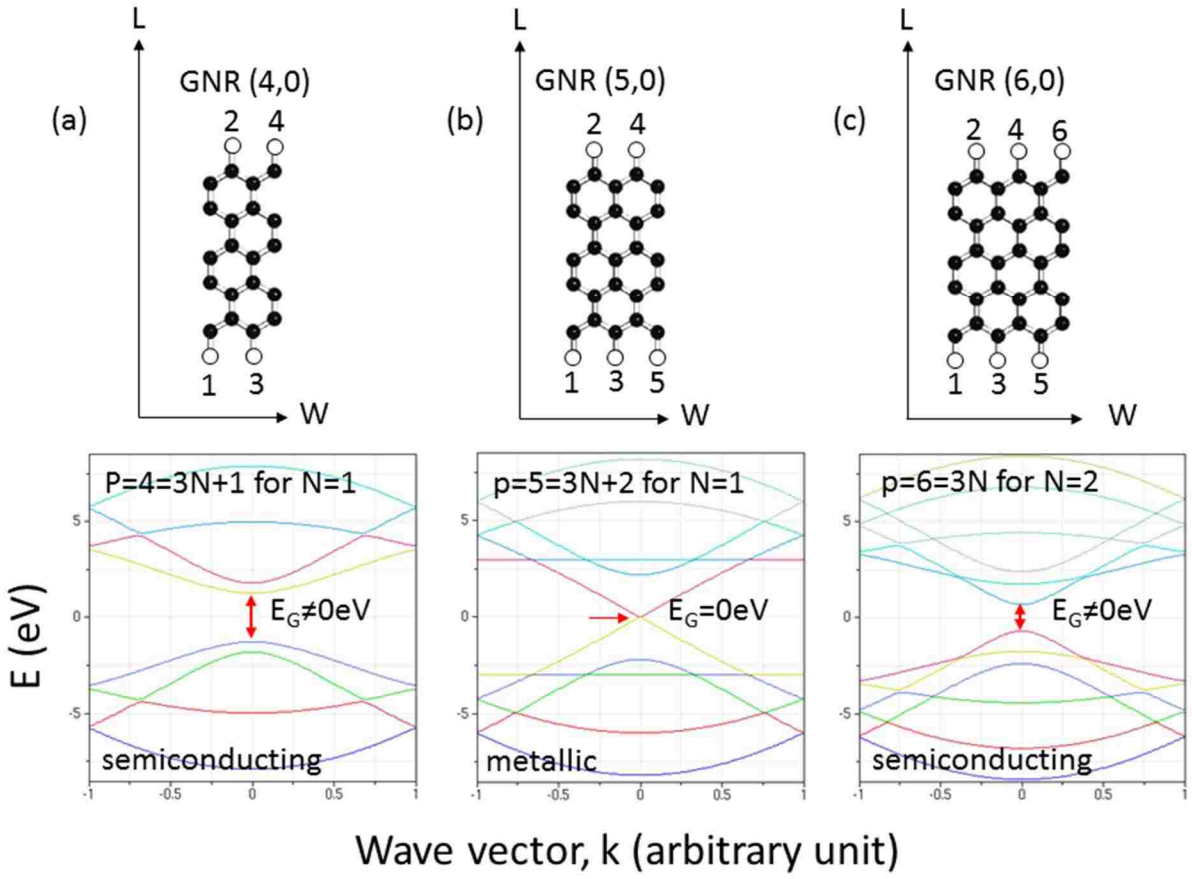


Figure 2.11: Width dependent band gap of graphene nanoribbon with increase in number of atoms. (a) Energy band diagram for (*4,0*) GNR which is a 3*N*+1 configuration for *N* = 1 and semiconducting, (b) energy band diagram for (*5,0*) GNR which is a 3*N*+2 configuration for *N* = 1 and metallic, (c) energy band diagram for (*6,0*) GNR which is a 3N configuration for N=2 and semiconducting. *L* denotes length and *W* denotes width of GNR. The numbers shown for chirality of GNR are depicted along the width of GNR.

However, first principle calculation using self-consistent pseudopotential method by Local (spin) Density Approximation (L(S)DA) shows that there are no metallic GNR [48]. The energy gap as a function of width is now grouped in a family of energy gaps and maintains the hierarchy of $\Delta_{3N+1} > \Delta_{3N} > \Delta_{3N+2}$ (**≠0 eV**). Such energy gap originates from the quantum confinement and crucial role of edge states and changes with GNR width. Moreover, first principle many electrons Green's function approach within the GW approximation provides quasi-particle energy gap with additional self-energy correction for both armchair and zigzag GNRs. Note, GW refers for the single particle Green's function 'G' and the screened coulomb interaction 'W'. Recently, Kim et al. [50] have shown that proper consideration of higher energy levels in addition to p_z -orbitals in TB scheme gives more accurate description of the GNR band structure. It is shown that within the TB method 3*N*+2 GNRs are not really metallic if higher energy levels such as '*d*' orbitals are included. This is in agreement with the electronic structure obtained from rigorous first principle based calculations.

The nearest neighbor tight binding Hamiltonian based calculation predicts that irrespective of nanoribbon width zigzag edge type GNRs are metallic which is contrary to the band gap obtained from first principle calculation using self-consistent pseudopotential method by local (spin) density approximation (L(S)DA) [48]. Based on the calculation of Son et al. [48], zigzag GNRs show gaps because of a staggered sublattice potential on the hexagonal lattice due to edge magnetization. Recently, the experimental work of Ruffieux et al. [51] has also reported that there are finite energy band gaps in zigzag GNRs which matches with the first principle based calculation of zigzag GNRs. Therefore, the predictions based on tight binding approximation are no more valid.

2.8 Doping of Graphene

Graphene can be doped either by chemical doping or by electrostatic doping [52]. In electrostatic doping, a positive and negative gate voltage generates n- and p- type graphene, respectively [53]. Moreover, ion doping in graphene sheets can reach electron and hole density around $10^{14}/cm^2$ [54]. Traditionally boron (B) and nitrogen (N) are treated as natural candidates for doping graphene due to same atomic size as in carbon. Wang *et al.* [54] observed experimentally n-type doping of GNR through electrochemical reaction with NH_3. Such doping forms C-N bonds at GNR edges. Though the method provides high ON/OFF current ratio of $\sim 10^5$, mobility degrades in n-type GNR FET compared to in pristine GNR FET. One problem associated with it is that N (nitrogen)-doped graphene (NG) can be both n- and p-type based on bonding nature of N atoms [55-57]. Recently, it has been studied experimentally that chemically functionalized array of GNR with 4-nitrobenzenediazonium (4-NBD) and diethylene triamine (DETA) molecules can provide doping of GNR arrays to p- and n-type, respectively [58]. In both cases, due to presence of a large quantity of edges, higher doping effect is observed in GNRs than that in pristine graphene sheets.

2.9 Conclusion

Graphene with its unique electronic properties is highly suitable for numerous electronic applications. Among different growth techniques, chemical vapor deposition (CVD) is most promising due to its low cost and large area. However, growth of large area single crystal graphene is still challenging. Owing to its zero band gap property, graphene is not yet suitable for digital applications. However, finite band gap can be obtained in the form of graphene nanoribbon (GNR) which demonstrates width and edge type dependent energy band gap. GNR TFET can be a viable option for low power high performance integrated circuit design which is

discussed in Chapter 3. By utilizing the zero band properties of graphene, the promise of graphene interlayer tunnel transistor can also be explored which is discussed in Chapter 4.

2.10 References

[1] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature,* vol. 479, pp. 329-337, 2011.

[2] A. M. Ionescu, *Small Swing Switches*. Cambridge: Cambridge University Press, 2011.

[3] J. Knoch, S. Mantl, and J. Appenzeller, "Impact of the dimensionality on the performance of tunneling FETs: bulk versus one-dimensional devices," *Solid State Elect.,* vol. 51, pp. 572-578, 2007.

[4] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Rev. of Modern Phys.,* vol. 81, pp. 109-162, 2009.

[5] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science,* vol. 306, pp. 666-669, 2004.

[6] B. C. Brodie, "On the atomic weight of graphite," *Philosophical Trans. of the Royal Society of London,* vol. 149, pp. 249-259, 1859.

[7] V. Kohlschütter and P. Haenni, "Zur kenntnis des graphitischen kohlenstoffs und der graphitsäure," *Zeitschrift für anorganische und allgemeine Chemie,* vol. 105, pp. 121-144, 1919.

[8] G. Ruess and F. Vogt, "Höchstlamellarer kohlenstoff aus graphitoxyhydroxyd," *Monatshefte für Chemie und verwandte Teile anderer Wissenschaften,* vol. 78, pp. 222-242, 1948.

[9] P. R. Wallace, "The band theory of graphite," *Phys. Rev.,* vol. 71, pp. 622-634, 1947.

[10] H. W. Kroto, J. R. Heath, S. C. O'Brien, R. F. Curl, and R. E. Smalley, "C60: Buckminsterfullerene," *Nature,* vol. 318, pp. 162-163, 1985.

[11] S. Iijima, "Helical microtubules of graphitic carbon," *Nature,* vol. 354, pp. 56-58, 1991.

[12] G. W. Semenoff, "Condensed-matter simulation of a three-dimensional anomaly," *Phys. Rev. Lett.,* vol. 53, pp. 2449-2452, 1984.

[13] S. Mouras, A. Hamm, D. Djurado, and J. C. Cousseins, "Synthesis of first stage graphite intercalation compounds with fluorides," *Revue de chimie minérale,* vol. 25, pp. 572-582, 1987.

[14] K. Nakada, M. Fujita, G. Dresselhaus, and M. S. Dresselhaus, "Edge state in graphene ribbons: Nanometer size effect and edge shape dependence," *Phys. Rev. B,* vol. 54, pp. 17954-17961, 1996.

[15] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, M. I. Katsnelson, I. V. Grigorieva, S. V. Dubonos, and A. A. Firsov, "Two-dimensional gas of massless Dirac fermions in graphene," *Nature,* vol. 438, pp. 197-200, 2005.

[16] M. I. Katsnelson, K. S. Novoselov, and A. K. Geim, "Chiral tunnelling and the Klein paradox in graphene," *Nat Phys,* vol. 2, pp. 620-625, 2006.

[17] K. S. Novoselov, Z. Jiang, Y. Zhang, S. V. Morozov, H. L. Stormer, U. Zeitler, J. C. Maan, G. S. Boebinger, P. Kim, and A. K. Geim, "Room-temperature quantum hall effect in graphene," *Science,* vol. 315, pp. 1379-1379, 2007.

[18] K. I. Bolotin, K. J. Sikes, J. Hone, H. L. Stormer, and P. Kim, "Temperature-dependent transport in suspended graphene," *Phys. Rev. Lett.,* vol. 101, pp. 096802, 2008.

[19] R. Prasher, "Graphene Spreads the Heat," *Science,* vol. 328, pp. 185-186, 2010.

[20] J. C. Meyer, A. K. Geim, M. I. Katsnelson, K. S. Novoselov, T. J. Booth, and S. Roth, "The structure of suspended graphene sheets," *Nature,* vol. 446, pp. 60-63, 2007.

[21] K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H. L. Stormer, "Ultrahigh electron mobility in suspended graphene," *Solid State Comm.,* vol. 146, pp. 351-355, 2008.

[22] Y. Hernandez, V. Nicolosi, M. Lotya, F. M. Blighe, Z. Sun, S. De, I. T. McGovern, B. Holland, M. Byrne, Y. K. Gun'Ko, J. J. Boland, P. Niraj, G. Duesberg, S. Krishnamurthy, R. Goodhue, J. Hutchison, V. Scardaci, A. C. Ferrari, and J. N. Coleman, "High-yield production of graphene by liquid-phase exfoliation of graphite," *Nat Nano,* vol. 3, pp. 563-568, 2008.

[23] K. S. Hazra, J. Rafiee, M. A. Rafiee, A. Mathur, S. S. Roy, J. McLauhglin, N. Koratkar, and D. S. Misra, "Thinning of multilayer graphene to monolayer graphene in a plasma environment," *Nanotechnology,* vol. 22, pp. 025704, 2011.

[24] N. Liu, F. Luo, H. Wu, Y. Liu, C. Zhang, and J. Chen, "One-step ionic-liquid-assisted electrochemical synthesis of ionic-liquid-functionalized graphene sheets directly from graphite," *Advanced Func. Mat.,* vol. 18, pp. 1518-1525, 2008.

[25] P. R. Somani, S. P. Somani, and M. Umeno, "Planer nano-graphenes from camphor by CVD," *Chemical Phys. Lett.,* vol. 430, pp. 56-59, 2006.

[26] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, "Large-area synthesis of high-

quality and uniform graphene films on copper foils," *Science,* vol. 324, pp. 1312-1314, 2009.

[27] X. Li, W. Cai, L. Colombo, and R. S. Ruoff, "Evolution of graphene growth on Ni and Cu by carbon isotope labeling," *Nano Letters,* vol. 9, pp. 4268-4272, 2009.

[28] S. Bae, H. Kim, Y. Lee, X. Xu, J.-S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. Ri Kim, Y. I. Song, Y.-J. Kim, K. S. Kim, B. Ozyilmaz, J.-H. Ahn, B. H. Hong, and S. Iijima, "Roll-to-roll production of 30-inch graphene films for transparent electrodes," *Nat Nano,* vol. 5, pp. 574-578, 2010.

[29] K. Yan, L. Fu, H. Peng, and Z. Liu, "Designed CVD growth of graphene via process engineering," *Accounts of Chemical Research,* vol. 46, pp. 2263-2274, 2013.

[30] T. H. Bointon, M. D. Barnes, S. Russo, and M. F. Craciun, "High quality monolayer graphene synthesized by resistive heating cold wall chemical vapor deposition," *Advanced Materials,* vol. 27, pp. 4200-4206, 2015.

[31] Y. Hao, M. S. Bharathi, L. Wang, Y. Liu, H. Chen, S. Nie, X. Wang, H. Chou, C. Tan, B. Fallahazad, H. Ramanarayan, C. W. Magnuson, E. Tutuc, B. I. Yakobson, K. F. McCarty, Y.-W. Zhang, P. Kim, J. Hone, L. Colombo, and R. S. Ruoff, "The role of surface oxygen in the growth of large single-crystal graphene on copper," *Science,* vol. 342, pp. 720, 2013.

[32] V. Miseikis, D. Convertino, N. Mishra, M. Gemmi, T. Mashoff, S. Heun, N. Haghighian, F. Bisio, M. Canepa, V. Piazza, and C. Coletti, "Rapid CVD growth of millimetre-sized single crystal graphene using a cold-wall reactor," *2D Materials,* vol. 2, pp. 014006, 2015.

[33] Y. Hao, L. Wang, Y. Liu, H. Chen, X. Wang, C. Tan, S. Nie, J. W. Suk, T. Jiang, T. Liang, J. Xiao, W. Ye, C. R. Dean, B. I. Yakobson, K. F. McCarty, P. Kim, J. Hone, L. Colombo, and R. S. Ruoff, "Oxygen-activated growth and bandgap tunability of large single-crystal bilayer graphene," *Nat Nano,* vol. 11, pp. 426-431, 2016.

[34] W. Mu, Y. Fu, S. Sun, M. Edwards, L. Ye, K. Jeppson, and J. Liu, "Controllable and fast synthesis of bilayer graphene by chemical vapor deposition on copper foil using a cold wall reactor," *Chemical Engineering Journal,* vol. 304, pp. 106-114, 2016.

[35] W. Chen, P. Cui, W. Zhu, E. Kaxiras, Y. Gao, and Z. Zhang, "Atomistic mechanisms for bilayer growth of graphene on metal substrates," *Phys. Rev. B,* vol. 91, pp. 045408, 2015.

[36] Q. Liu, Y. Gong, J. S. Wilt, R. Sakidja, and J. Wu, "Synchronous growth of AB-stacked bilayer graphene on Cu by simply controlling hydrogen pressure in CVD process," *Carbon,* vol. 93, pp. 199-206, 11// 2015.

[37] A. C. Ferrari, J. C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K. S. Novoselov, S. Roth, and A. K. Geim, "Raman spectrum of graphene and graphene layers," *Physical Review Letters,* vol. 97, pp. 187401, 2006.

[38] E. V. Castro, K. S. Novoselov, S. V. Morozov, N. M. R. Peres, J. M. B. L. dos Santos, J. Nilsson, F. Guinea, A. K. Geim, and A. H. C. Neto, "Biased bilayer graphene: semiconductor with a gap tunable by the electric field effect," *Phys. Rev. Lett.,* vol. 99, pp. 216802, 2007.

[39] J. A. Kelber, M. Zhou, S. Gaddam, F. L. Pasquale, L. M. Kong, and P. A. Dowben, "Direct graphene growth on oxides: interfacial interactions and band gap formation," *ECS Trans.,* vol. 45, pp. 49-61, 2012.

[40] S. Nakaharai, T. Iijima, S. Ogawa, S. Suzuki, K. Tsukagoshi, S. Sato, and N. Yokoyama, "Electrostatically-reversible polarity of dual-gated graphene transistors with He ion irradiated channel: toward reconfigurable CMOS applications," in *Tech. Digest IEEE Int. Elect. Dev. Meetings*, pp. 4.2.1-4.2.4, 2012.

[41] G. Giovannetti, P. A. Khomyakov, G. Brocks, P. J. Kelly, and J. van den Brink, "Substrate-induced band gap in graphene on hexagonal boron nitride: Ab initio density functional calculations," *Phys. Rev. B,* vol. 76, pp. 073103, 2007.

[42] M. S. Nevius, M. Conrad, F. Wang, A. Celis, M. N. Nair, A. Taleb-Ibrahimi, A. Tejeda, and E. H. Conrad, "Semiconducting graphene from highly ordered substrate interactions," *Phys. Rev. Lett.,* vol. 115, pp. 136802, 2015.

[43] L. Yang, C.-H. Park, Y. W. Son, M. L. Cohen, and S. G. Louie, "Quasiparticle energies and band gaps in graphene nanoribbons," *Phys. Rev. Lett.,* vol. 99, pp. 186801, 2007.

[44] M. Y. Han, B. Özyilmaz, Y. Zhang, and P. Kim, "Energy band-gap engineering of graphene nanoribbons," *Phys. Rev. Lett.,* vol. 98, pp. 206805, 2007.

[45] F. Sols, F. Guinea, and A. H. C. Neto, "Coulomb blockade in graphene nanoribbons," *Phys. Rev. Lett.,* vol. 99, pp. 166803, 2007.

[46] L. Xie, H. Wang, C. Jin, X. Wang, L. Jiao, K. Suenaga, and H. Dai, "Graphene nanoribbons from unzipped carbon nanotubes: atomic structures, raman Spectroscopy, and electrical properties," *J. of the American Chemical Society,* vol. 133, pp. 10394-10397, 2011.

[47] D. V. Kosynkin, A. L. Higginbotham, A. Sinitskii, J. R. Lomeda, A. Dimiev, B. K. Price, and J. M. Tour, "Longitudinal unzipping of carbon nanotubes to form graphene nanoribbons," *Nature,* vol. 458, pp. 872-876, 2009.

[48] Y. W. Son, M. L. Cohen, and S. G. Louie, "Energy gaps in graphene nanoribbons," *Phys. Rev. Lett.,* vol. 97, pp. 216803, 2006.

[49] www.nanohub.org/cntbands, (L. Yang, M. P. Anantram, J. Han, and J. P. Lu, "Band-gap change of carbon nanotubes: Effect of small uniaxial and torsional strain," *Phys. Rev. B,* vol. 60, pp. 13874-13878, 1999).

[50] S. Kim, M. Luisier, T. B. Boykin, and G. Klimeck, "Computational study of heterojunction graphene nanoribbon tunneling transistors with p-d orbital tight-binding method," *Appl. Phys. Lett.,* vol. 104, pp. 243113, 2014.

[51] P. Ruffieux, S. Wang, B. Yang, C. Sánchez-Sánchez, J. Liu, T. Dienel, L. Talirz, P. Shinde, C. A. Pignedoli, D. Passerone, T. Dumslaff, X. Feng, K. Müllen, and R. Fasel, "On-surface synthesis of graphene nanoribbons with zigzag edge topology," *Nature,* vol. 531, pp. 489-492, 2016.

[52] R. Lv and M. Terrones, "Towards new graphene materials: doped graphene sheets and nanoribbons," *Materials Letters,* vol. 78, pp. 209-218, 2012.

[53] H. Y. Chiu, V. Perebeinos, Y.-M. Lin, and P. Avouris, "Controllable p-n Junction formation in monolayer graphene using electrostatic substrate engineering," *Nano Letters,* vol. 10, pp. 4634-4639, 2010.

[54] X. Wang, X. Li, L. Zhang, Y. Yoon, P. K. Weber, H. Wang, J. Guo, and H. Dai, "N-Doping of graphene through electrothermal reactions with ammonia," *Science,* vol. 324, pp. 768-771, 2009.

[55] Y. Fujimoto and S. Saito, "Formation, stabilities, and electronic properties of nitrogen defects in graphene," *Phys. Rev. B,* vol. 84, pp. 245446, 2011.

[56] T. Schiros, D. Nordlund, L. Pálová, D. Prezzi, L. Zhao, K. S. Kim, U. Wurstbauer, C. Gutiérrez, D. Delongchamp, C. Jaye, D. Fischer, H. Ogasawara, L. G. M. Pettersson, D. R. Reichman, P. Kim, M. S. Hybertsen, and A. N. Pasupathy, "Connecting dopant bond type with electronic structure in N-doped graphene," *Nano Letters,* vol. 12, pp. 4025-4031, 2012.

[57] Z. Hou, X. Wang, T. Ikeda, K. Terakura, M. Oshima, and M. Kakimoto, "Electronic structure of N-doped graphene with native point defects," *Phys. Rev. B,* vol. 87, pp. 165401, 2013.

[58] P. Solis-Fernandez, M. A. Bissett, M. Tsuji, and H. Ago, "Tunable doping of graphene nanoribbon arrays by chemical functionalization," *Nanoscale,* 2015.

CHAPTER 3*

MODELING OF GRAPHENE NANORIBBON TUNNEL FIELD EFFECT TRANSISTOR

3.1 Introduction

Graphene nanoribbon field effect transistors (GNR-FETs) have been fabricated and characterized which demonstrated promising performance. Wang et al. [1] first observed an on/off current ratio of 10^6 in a GNR FET operating at 2000 μA/μm on-state drain current for a channel width of ~2 nm. However, the channel length is 236 nm and the subthreshold slope is 210 mV/decade which clearly makes such GNR FET un-suitable for current high performance CMOS based IC design. Therefore, the constant demand for GNR transistors operation at low supply voltage at CMOS compatible channel length still exists.

Based on the earlier discussion provided for TFET, graphene nanoribbon (GNR) is promising for tunneling FETs due to its symmetric band structure, low band gap, light effective mass, and monolayer-thin body. Zhang et al. [2] in 2008 first reported the conceptual theoretical study of a graphene nanoribbon tunnel field effect transistor. The idealistic theoretical model predicted a GNR TFET performance of 800 μA/μm drain current at 0.1 V supply voltage for a GNR width of 5 nm and a channel length of 20 nm. The computed subthreshold slope was 0.19

---

*Part of this work is reported in the following publications:

1. Md S Fahad, A. Srivastava, A. K. Sharma and C. Mayberry, "Analytical current transport modeling of graphene nanoribbon tunnel field effect transistor for digital circuit design," *IEEE Transactions on Nanotechnology*, vol. 15, Issue. 1, pp. 39-50, Jan 2016.
2. Md S Fahad, A. Srivastava, A.K. Sharma and C. Mayberry, "Current transport in grapheme tunnel field effect transistor under constant electric field," SPIE 2013 Nanoscience+Engineering: Carbon Nanotubes, Graphene, and Associated Devices VI (OP109), *Proc. of SPIE*, vol. 8814, 8 pages (25-29 August 2013, San Diego, CA).
3. Md S Fahad, A. Srivastava and A.K. Sharma, C. Mayberry, "Current transport in graphene tunnel field effect transistor for RF integrated circuits," *Proc. IEEE MTT-S International Wireless Symposium*, 4 pages (13-18 April 2013, Beijing, China).

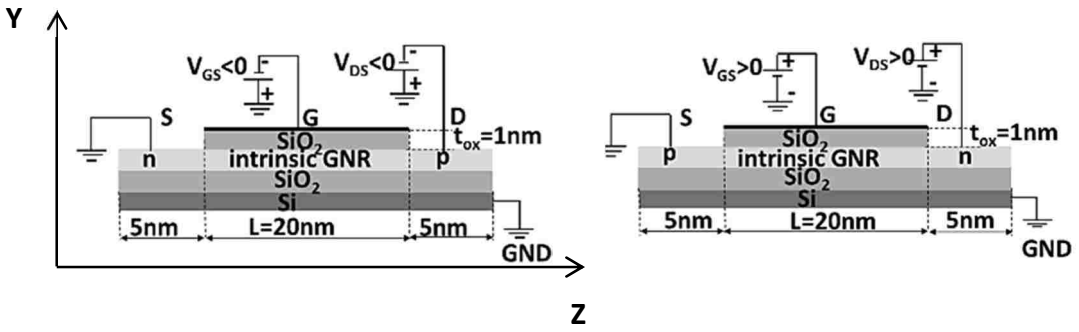
mV/decade which was neither validated from numerical simulations nor experiments.

Further, band-to-band tunneling in GNR tunnel FET has been studied by numerical simulations for graphene homo-junctions [3], hetero-junctions [4], single and bilayers [5, 6] and dissipative transport through rough edges for the understanding of current transport [7]. Majority of these numerical simulations are obtained by solving 3D Poisson's equation coupled with Schrodinger's equation for a nearest neighbor tight binding (NNTB) Hamiltonian for a finite width and specific edge type GNR. Compared to numerical simulations, physics based compact analytical models of such novel emerging devices not only allows a better understanding of the transistor operation but also enables their potential for circuit level synthesis.

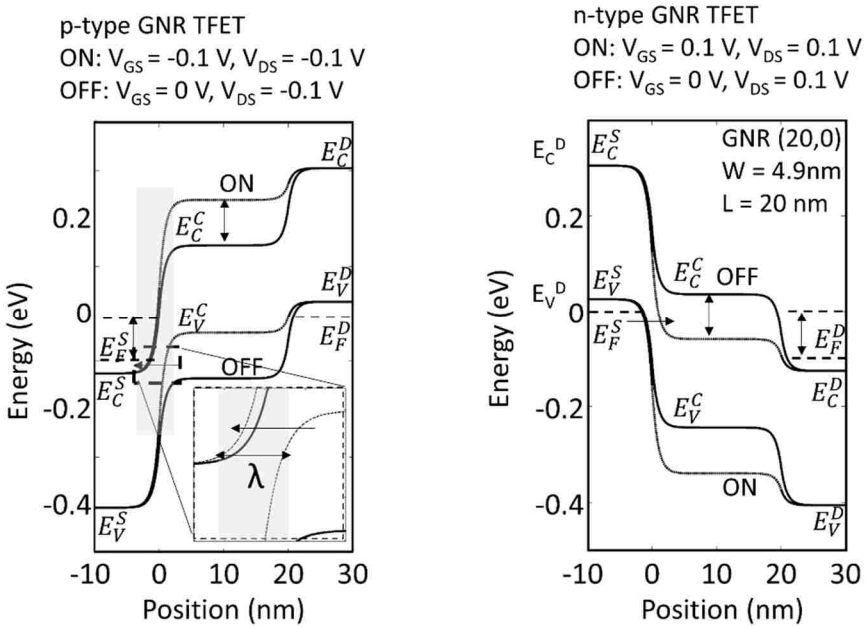
In this chapter, an analytical current transport model of a p-i-n n-type armchair GNR TFET is developed which is compared with numerical simulation. Two separate current transport models are derived analytically from semi-classical and semi-quantum modeling approaches. Non-equilibrium Green Function (NEGF) based numerical simulation study is also carried out. Results obtained from these two methods are compared with the numerical simulation to establish analytical models. The analytical model in the work of Zhang el al. [2] is revisited and results are also compared with the analytical and numerically simulated results in this work. Furthermore, GNR TFET's performance is studied for varying GNR width using semi-classical, semi-quantum and NEGF simulation based current transport models. Finally, complementary GNR TFET inverter for digital circuit design is demonstrated through the computation of voltage transfer characteristic from all three modeling approaches.

3.2 Device Structure and Operation of GNR TFET

Schematic of a GNR TFET is shown in Figs. 3.1(a) and 3.1(b) where GNR is placed on top of SiO_2 substrate. Silicon dioxide of 1 nm is considered as a top gate oxide. Length of gate



a) b)



c) d)

Figure 3.1: Schematic of GNR TFET. (a) Vertical cross section of p-type GNR TFET with 1 nm SiO_2 top gate dielectric. Channel length is 20 nm with 10 nm of source and drain extension making the total length of GNR 40 nm, (b) n - type GNR TFET, (c) energy band diagram of n- i - p GNR TFET (p-type GNR TFET where both V_{GS} and V_{DS} are '-' ve) and (d) energy band diagram of p - i - n GNR TFET (n - type GNR TFET where both V_{GS} and V_{DS} are '+' ve). Note: In both (c) and (d), solid line is for off state whereas dashed line is for on state. off state is defined as $|V_{DS}|$ = 0.1 V and $|V_{GS}|$ = 0 V and on state is defined as $|V_{DS}|$ = 0.1 V and $|V_{GS}|$ = 0.1 V. Semiconducting GNR (20,0) has a band gap of 0.28 eV for its corresponding 4.9 nm width. Inset: Enlarged view of potential variation.

dielectric is 20 nm as shown in both Figs. 3.1(a) and 3.1(b) for a GNR channel width of 4.9 nm and 0.28 eV energy band gap. Cr/Au or Ti/Cu contacts are typically used.

By solving 3D Poisson's equation coupled with 1D Schrodinger's equation within the NEGF formalism, three-dimensional potential is obtained for GNR TFET in all three (X, Y and Z) spatial directions. Corresponding energy band diagrams along the channel in Z- direction are plotted from the Z-component of this potential. Figures 3.1(c) and (d) show the energy band diagram during an off/on condition for n - i - p (p - type) and p - i - n (n - type) TFET, respectively. E_C^S, E_C^C and E_C^D are source, channel and drain conduction bands, respectively, whereas E_V^S, E_V^C and E_V^D are the source, channel and drain valence bands, respectively. The solid and dash lines show off and on states of TFET, respectively. Note for both types of transistors, off state is defined for $|V_{DS}|$ = 0.1 V and $|V_{GS}|$ = 0 V and on state is defined for $|V_{DS}|$ = 0.1 V and $|V_{GS}|$ = 0.1 V. Throughout this chapter positive bias of V_{GS} and V_{DS} is considered assuming n-type GNR TFET operation. Junction electric field of 3.85×10^6 V/cm is taken into account which is identical with the estimated electric field in [2]. For the p - i - n n - type GNR TFET, source and drain are assumed to be p - and n - type where Fermi levels are assumed to coincide with the valence band and conduction bands, respectively.

In thermal equilibrium, Fermi levels in source, channel and drain regions are aligned together. During off state, there is a difference of $|V_{DS}|$ between $E_C^S$and E_V^D in p-type TFET and E_V^S and E_C^D in n-type TFET. However, source and channel Fermi levels remain aligned together. Therefore, no tunneling of carriers occurs through source-channel tunnel junction. Further, for $V_{GS} > 0$ (in n-type TFET) and $V_{GS} < 0$ (in p-type TFET), a tunneling window opens and initiates band-to-band tunneling. Direction of arrows shows flow of carriers due to tunneling between source and channel. GNR TFET is less sensitive to channel mobility since band-to-band

tunneling dominates over the scattering in channel. Both source and channel are of same material assuming momentum conservation in both conduction and valence bands. The inset and the shaded area in Fig. 3.1(c) show the relevant length scale for potential variation (λ) which is usually dependent on the device geometry. For 1D geometry of GNR, λ is determined from $\lambda = \sqrt{(\varepsilon_{GNR} / \varepsilon_{ox}) t_{GNR} t_{ox}}$ where ε_{GNR} and ε_{ox} are the GNR and oxide dielectric constants, respectively, and t_{GNR} = 0.35 nm is the thickness of the GNR. In this work, we consider λ to be significantly lower than the channel length L. For $L >> \lambda$, it has been found that the drain induced barrier lowering (DIBL) is significantly suppressed thereby yielding an ideal turn-off characteristic [8].

3.3 Current Transport Model

In following subsections, three types of current transport models are presented and compared.

3.3.1 Semi-classical Analytical Model

In conventional inversion mode MOSFETs, threshold voltage is well defined. However, definition of threshold voltage in TFET is not so well defined rather varies depending upon the geometry and the channel material. The definition of threshold voltage proposed by Boucart and Ionescu for Si p-i-n TFET [9] considers threshold voltage as the voltage where the I_D-V_{GS} characteristic makes a transition between quasi-exponential and linear dependence of the drain current. It is termed as either gate threshold voltage or the drain threshold voltage depending on its reference point and depends strongly on the tunnel junction design and gate geometry. Recently, Ortiz-Conde et al. [10] proposed an extrapolated threshold extraction method for the bulk semiconductor and compared with experimental fin type TFETs. The method, however

considers strong conduction modeling scheme and does not explain transition type threshold voltage for the weak conduction region.

For TFETs having GNR as the channel material, contact materials play a crucial role. The graphene is doped by adsorption on metal substrates based on studies from the Density Functional Theory (DFT). Graphene establishes a weak bond with metal atoms while preserving its electronic structure. A significant shift of the Fermi level with respect to the conical point by ~0.5 eV is observed [11]. In contrast to graphene, GNR has inherent non-zero and direct band gap. Nevertheless, there is still a high probability of GNR to get doped by adsorption on metal. Hence, for GNR TEFT to operate in its actual bias condition, such inherent contact potential needs to be overcome. Hence, their contribution towards calculating GNR TFET threshold voltage comes into existence.

Here we consider a simple expression of threshold voltage (V_{TH}) for a-GNR TFET similar to a MOSFET threshold voltage. However, unlike in MOSFET, this expression is assumed to be dominated by contact potentials. In absence of dangling bonds, mobile charges and fixed ions, V_{TH} can be expressed as follows:

$$V_{TH} = \varphi_{BI} + \varphi_S + \varphi_G + \varphi_{ox} \tag{3.1}$$

where φ_G and φ_S are contact potentials due to gate and source contacts. The built in potential φ_{BI} is defined as follows [12]:

$$\varphi_{BI} = \frac{E_G}{2} - V_T \ln\left(\frac{N}{n_i}\right) \tag{3.2}$$

where E_G is GNR band gap (0.289 eV), V_T is thermal voltage (0.0259 V at 300 K), N is doping density (~ $5\text{x}10^{11}/\text{cm}^2$) and n_i is intrinsic carrier density ($9\text{x}10^{10}/\text{cm}^2$) [13]. φ_{OX} is the potential

drop due to gate oxide over the channel. Corresponding change in GNR band gap due to additional intermediate energy states from edge roughness can be considered through Eq. (3.2). Potential drop through the gate oxide is defined as follows:

$$\varphi_{ox} = \frac{Q_o}{C_{ox}} \tag{3.3}$$

In Eq. (3.3), $Q_0 = n_s q$ is the total charge, where n_s is induced surface charge density through gate oxide and is calculated as follows [14]:

$$n_s = \frac{\varepsilon_o \varepsilon_{ox} (V_{GS} - V_{TH})}{q\, t_{ox}} \tag{3.4}$$

Here, V_{GS} is input gate-source voltage. For 1 nm SiO_2 gate oxide (relative permittivity 3.9) and 0.1 V gate-source input voltage, calculated n_s is 2.16×10^{12} cm^{-2} [15]. Oxide capacitance is defined as, $C_{ox} = \varepsilon_o \varepsilon_{ox} / t_{ox}$. Substituting values of C_{ox} in Eq. (3.3) and replacing φ_{ox} in Eq. (3.4), V_{TH} can be calculated as a function of both dielectric permittivity and oxide thickness.

Integrating product of charge flux and tunneling probability from 0 to energy window of $\Delta\varphi$, 1D Zener tunneling current is calculated as follows [12]:

$$I_T = \int_0^{\Delta\varphi} qV_g \rho_{GNR}(k) \left[f_S(E) - f_D(E) \right] T_{WKB}\, dk \tag{3.5}$$

In Eq. (3.5), I_D is tunneling drain current, V_g is group velocity ($1/\hbar\ (dE/dk)$); $\rho_{GNR}\ (k)$ is the 1D density of states of graphene in k-plane ($1/\pi$) [2] and $f_D(E)$ is the Fermi level position at drain (qV_{DS}) and $f_S(E)$ is the Fermi level position at source (0). T_{WKB} is tunneling probability in a semiconducting p-n junction GNR and is expressed as follows [16]:

$$T_{WKB} = \exp\left(-\frac{\pi E_G^2}{4q\hbar v_F \xi}\right) \tag{3.6}$$

Here, $v_F \sim 10^8$ cm/s is Fermi velocity, E_G is GNR band gap, $\hbar$ is reduced Plank's constant and ξ is the electric field at the source-channel tunnel junction. Based on the universal analytic model for TFET proposed by Lu et al. [17], electric field at the tunnel junction is linearly dependent on the junction built-in electric field, V_{GS} and V_{DS}. This is expressed as follows:

$$\xi = \xi_0(1 + \gamma_1 V_{GS} + \gamma_2 V_{DS}) \tag{3.7}$$

where ξ_0 is the built-in electric field at the source-channel tunnel junction when V_{GS}=V_{DS}=0V. Parameters γ_1 and γ_2 are the linear coefficients in unit of inverse of volt (V^{-1}). An increase in gate bias enhances the electric field at the tunnel junction by narrowing the tunneling barrier whereas an increase in drain bias also does the same with a lesser degree as the drain field is screened by the gate electrode. The limit considered in this work for γ_1 ranges from 1 to 5 whereas for γ_2 from 5 to 10 which are higher than those proposed in [17]. The model derived in [17] describes the parameters with respect to bulk three-dimensional heterojunction material. It is to be noted that the electrical properties and energy band structure of GNR is significantly different from such materials. Built-in electric field is dependent on both the built-in potential and the length of potential screening at the source- channel tunnel junction as follows:

$$\xi_0 = \varphi_{BI} / \lambda \tag{3.8}$$

The Fermi level at drain and source are expressed as follows:

$$f_D(E) = \frac{1}{1 + e^{\left(E - E_f^D\right)/kT}} \tag{3.9}$$

$$f_S(E) = \frac{1}{1 + e^{\left(E - E_f^S\right)/kT}} \tag{3.10}$$

Here, E is the energy of electron with an unit in electron-volt (eV) during the operation of band-to-band tunneling occurs. During off state, source Fermi level is at 0V and drain Fermi level is at V_{DS} with reference to source. Considering proper limits of integration from 0 to $\Delta\varphi=V_{GS}-V_{TH}$, Eq. (3.5) can be expressed as follows:

$$I_T = \int_0^{\Delta\varphi} q\frac{1}{\hbar}\frac{dE}{dk}\frac{1}{\pi}\left[\frac{1}{1+e^{\left(E-E_f^D\right)/kT}} - \frac{1}{1+e^{\left(E-E_f^S\right)/kT}}\right] T_{WKB}\, dk \tag{3.11}$$

$$I_T = q\frac{1}{\hbar}\frac{1}{\pi} T_{WKB} \int_0^{\Delta\varphi}\left[\left(1-\frac{e^{(E-qV_{DS})/qV_T}}{1+e^{(E-qV_{DS})/qV_T}}\right) - \left(1-\frac{e^{(E)/qV_T}}{1+e^{(E)/qV_T}}\right)\right] dE \tag{3.12}$$

We obtain,

$$I_T = \frac{1}{2}\frac{4q^2}{\hbar\pi} V_T T_{WKB}\left[\begin{array}{l} -\ln\left(1+\exp\left(\frac{V_{GS}-V_{TH}-V_{DS}}{V_T}\right)\right) + \ln\left(1+\exp\left(\frac{V_{GS}-V_{TH}}{V_T}\right)\right) + \\ \ln\left(1+\exp\left(-\frac{V_{DS}}{V_T}\right)\right) - \ln(2) \end{array}\right] \tag{3.13}$$

The term $4q^2/2\pi\hbar$ in Eq. (3.13) can be termed as the minimum conductivity of graphene (σ). Following Drude model, minimum conductivity in graphene can be expressed in terms of mobility and charge density as follows:

$$\sigma = 4q^2/2\pi\hbar = \mu_n(n_S)q \tag{3.14}$$

where μ_n is carrier mobility. Combining Eqs. (3.4), (3.13) and (3.14), tunneling current equation for GNR TFET is expressed as follows:

$$\begin{aligned} I_T = {} & \frac{\mu_n\varepsilon_0\varepsilon_{ox}(V_{GS}-V_{TH})}{t_{ox}} V_T T_{WKB}\left[-\ln\left(1+\exp\left(\frac{V_{GS}-V_{TH}-V_{DS}}{V_T}\right)\right)\right. \\ & \left. +\ln\left(1+\exp\left(\frac{V_{GS}-V_{TH}}{V_T}\right)\right) + \ln\left(1+\exp\left(-\frac{V_{DS}}{V_T}\right)\right) - \ln(2)\right] \end{aligned} \tag{3.15}$$

Considering built-in potential and thermal voltage, leakage current for GNR TFET can be defined as follows [2]:

$$I_L = \frac{q^2}{\pi\hbar} V_T \exp(-\frac{\varphi_{BI}}{V_T}) \tag{3.16}$$

Combining Eqs. (3.15) and (3.16) drain current for GNR TFET can be expressed as follows:

$$I_D = I_T + I_L \tag{3.17}$$

$$\begin{aligned} I_D = {} & \frac{\mu_n \varepsilon_0 \varepsilon_{ox} (V_{GS} - V_{TH})}{t_{ox}} V_T T_{WKB} \left[-\ln\left(1+\exp\left(\frac{V_{GS} - V_{TH} - V_{DS}}{V_T}\right)\right)\right. \\ & \left. +\ln\left(1+\exp\left(\frac{V_{GS} - V_{TH}}{V_T}\right)\right) + \ln\left(1+\exp\left(-\frac{V_{DS}}{V_T}\right)\right) - \ln(2)\right] + \frac{q^2}{\pi\hbar} V_T \exp(-\frac{\varphi_{BI}}{V_T}) \end{aligned} \tag{3.18}$$

Equation (3.18) has been derived for semi-classical current transport model for the n-type GNR TFET. Since the minimum conductivity of graphene of $4q^2/2\pi\hbar$ is maintained at a charge density corresponding to Eq. (3.3), mobility in Eq. (3.18) is estimated as 223.6 cm^2/V-s. Such a small value of mobility has little or no effect on tunneling phenomena as tunneling dominates over the scattering in TFETs [8]. The current transport model as described in [2] does not account for any leakage current effect on drain current which may lead to an erroneous result.

3.3.2 Semi-quantum Analytical Model

Compared to semi-classical analytical model, a semi-quantum 'mode' based analytical model is developed for GNR TFET and performance is compared with both semi-classical analytical model and numerical simulations. Considering transverse 'mode' of current transport and transmission coefficient for the channel to conduct charge carriers from source to drain, conductance of the channel defined according to Landauer expression is as follows [18]:

$$G(E) = \frac{2q^2}{\hbar} M(E) T_{WKB}(E) \tag{3.19}$$

Where

$$M(E) = W \frac{2|E_{TM}|}{\pi(\hbar v_F)} \tag{3.20}$$

W is width of GNR and $|E_{TM}|$ is the energy of electron in transverse mode. In this work, E_{TM} is described in terms of gate-source voltage and is applied to control energy window through which number of modes are calculated. The number of conducting channels at energy E_{TM} is proportional to the width of the conductor in two-dimensional and to the cross-sectional area in three-dimensional geometry. Band structure of the conducting channel also affects total number of modes. Expression of *M(E)* in Eq. (3.20) is specific to graphene which is different from the expression of mode usually adopted for a parabolic band structure [19]. In ballistic transport, transmission coefficient, $T_{WKB}(E)$ is assumed as 1. However, in order to apply the similar concept for a tunneling transistor, transmission coefficient is assumed to be equal to tunneling probability as described by Eq. (3.6) in [20]. Considering source and drain Fermi-Dirac statistics and channel conductance expressed in Landauer formalism, current can be calculated as follows:

$$I = \int dE G(E)(f_S(E) - f_D(E)) \tag{3.21}$$

where drain Fermi function $f_D(E)$ and source Fermi function $f_S(E)$ are described in Eq. (3.9) and (3.10), respectively and can be rewritten for $|E_{TM}|$ instead of E. Combining Eqs. (3.9), (3.10), (3.19) and (3.21), drain current is expressed as follows:

$$I_D = \int dE \frac{2q^2}{\hbar} M(E) T_{WKB}(E) \left(f_S(E) - f_D(E) \right) \tag{3.22}$$

Substituting expression of $T_{WKB}(E)$ from Eq. (3.6) and *M(E)* from Eq. (3.20), Eq. (3.22) becomes,

$$I_D = \int dE \frac{2q^2}{\hbar} W \frac{2|E_{TM}|}{\pi(\hbar v_F)} \exp(-\frac{\pi E_G^2}{4q\hbar v_F \xi}) \left(\frac{1}{1+e^{\left(E_{TM}-E_F^S\right)/kT}} - \frac{1}{1+e^{\left(E_{TM}-E_F^D\right)/kT}} \right) \tag{3.23}$$

$$I_D = \frac{2q^2}{\hbar} \exp(-\frac{\pi E_G^2}{4q\hbar v_F \xi}) \frac{2W}{\pi(\hbar v_F)} \int \left(\frac{|E_{TM}|}{1+e^{\left(E_{TM}-E_F^S\right)/kT}} - \frac{|E_{TM}|}{1+e^{\left(E_{TM}-E_F^D\right)/kT}} \right) dE \tag{3.24}$$

$$I_D = \frac{4q^3 W}{\pi(\hbar^2 v_F)} \exp(-\frac{\pi E_G^2}{4q\hbar v_F \xi})$$
$$\left[-V_T (V_{GS} - V_{TH}) \{ \ln(1+\exp(\frac{V_{GS}-V_{TH}}{V_T})) - \ln(1+\exp(\frac{V_{GS}-V_{TH}-V_{DS}}{V_T})) \} - \frac{(\pi V_T)^2}{12} \right] \tag{3.25}$$

In Eq. (3.25), in order to obtain a closed form of solution, complex polylog expression is avoided. For $V_{GS} >> k_B T/q$ polylog terms becomes insignificant compared to other terms. Only the non-vanishing term remains after the integration in Eq. (3.25).

3.3.3 NEGF-based Numerical Model: Simulation Method and Approach

In this section, we model the GNR TFET with numerical simulation. Device schematic shown in Fig. 3.1(b) for n-type TFET is studied through self-consistent solution of the Poisson and Schrödinger equations using NEGF formalism incorporated in open source device simulation tool NanoTCAD ViDES [20]. The object of this study is to compare and verify the validity of the previously derived semi-classical and semi-quantum analytical models.

The band structure of armchair graphene nanoribbon of (*20,0*) chirality is modeled using first principles pseudo-potential method by Local (spin) Density Approximation (L(S)DA) in which energy relaxation at the GNR edges is assumed. The Hamiltonian for this calculation is obtained from [21].

The associated three-dimensional potential is obtained by solving self consistently 3D Poisson's equation coupled with Schrodinger equation which is solved for the real space. The carbon to carbon hopping parameter is 2.7 eV. The simulations are performed at the room

temperature, 300 K which is also the considered temperature in other two models. The default parameters for (*20,0*) GNR simulations are described as follows: the channel is intrinsic and the doped contacts are considered for better comparison with the analytical TFET models.

The p-type source and n-type drain are doped with a molecular fraction of 2.19×10^{-4} which is 0.026/nm compared to carbon atom density of 122/nm and is consistent with the considered doping concentration of $5x10^{11}/cm^2$ used in semi-classical analytical model in Eq. (3.2). The SiO_2 layer of thickness 1 nm is used as the gate dielectric at the top of the channel. The length of the nanoribbon is 30 nm with channel length of 20 nm and source drain extension of 5 nm on each side of the channel. With chirality of (*20,0*) GNR width becomes 4.9 nm and calculated semiconducting band gap is 0.289 eV. Since low energy band gap is preferred for TFET design, GNR (*20,0*) is considered instead of GNR (11,0) which was shown earlier in Fig. 3.1. The same GNR band gap and width considered for the numerical simulations are also used for all three current transport models discussed in this Chapter.

3.4 Transfer Characteristics of GNR TFET

Performance of GNR TFET obtained from all these three current transport models are discussed in this section. Using analytical current transport models developed in Eqs. (3.18) and (3.25), transfer characteristics are plotted in Fig. 3.2(a) for the n-type GNR TFET for an idealistic GNR with zero threshold voltage and no defects or edge roughness. The obtained results from the analytical model are compared with the numerical simulation. Results obtained from the model of Zhang et al. [2] is also shown in Fig. 3.2(a). It is found that semi-classical analytical current transport model gives fairly good agreement with the results obtained from rigorous NEGF simulation. However, the derived semi-quantum analytical model deviates from the NEGF simulated results to a larger extent.

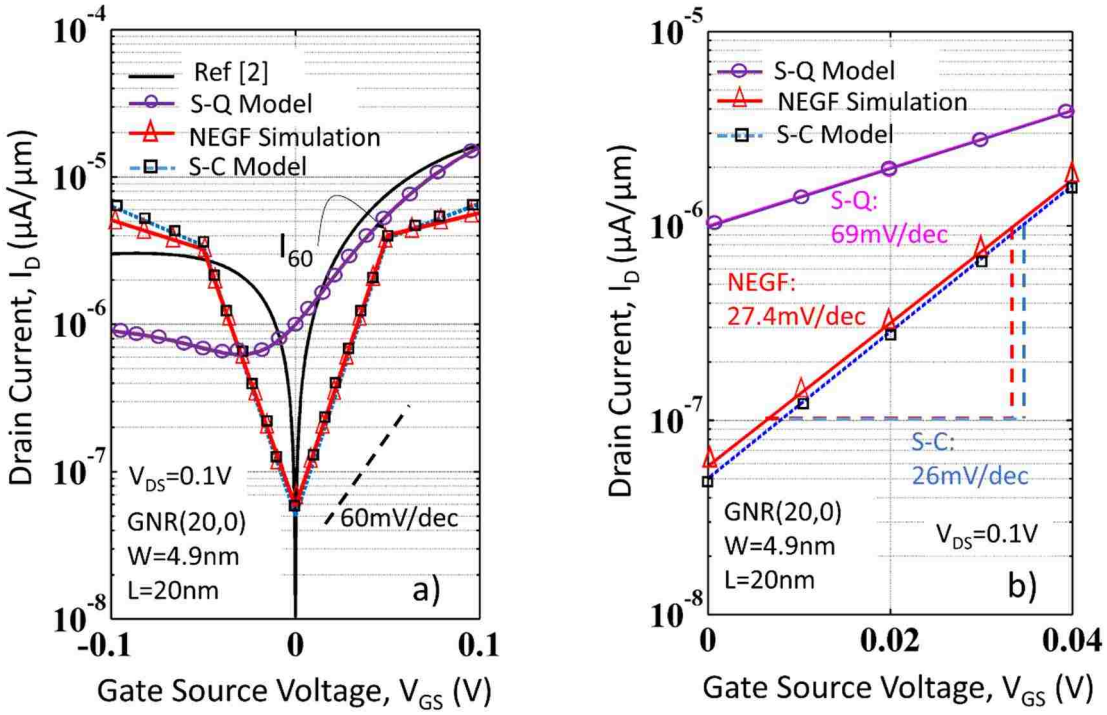


Figure 3.2: (a) Comparison of transfer characteristics of n-type GNR-TFET obtained from three current transport models along with that of [2]. (b) Method of obtaining subthreshold swing for three current transport models. Note: S-Q stands for semi-quantum and S-C for semi-classical. Values written in Figure 3.2(b) are obtained using Eq. (3.27).

A supply voltage V_{DS} (= V_{DD}) of 0.1 V maintains minimum power consumption. This also ensures the condition $V_{BI} + V_{DS} < 2E_G$ to shut down any ambipolar tunneling characteristics at off-state of the TFET where V_{BI} is the built-in voltage of the p-i-n structure [22]. The on/off current ratio for both semi-classical model and NEGF simulation are calculated as 122 and 116 at $V_{GS} = V_{DS} = 0.1$ V, respectively which are fairly close within an accepted margin. Drive current for semi-classical model is 6.2×10^{-6} μA/μm which is also in close agreement with the calculated drive current of 5.95×10^{-6} μA/μm from NEGF simulation. Table 3.1 summarizes performance comparison among these three current transport models. Note that the drain current has been normalized along the GNR width. Though the semi-classical analytical model and numerical simulation for the current transport matches closely, the semi-quantum analytical model differs from both. Before further studies into GNR TFET transfer characteristics; it is to be mentioned that the tunneling probability used in calculating drain current in semi-quantum model is taken from the semi-classical model which is semi-classical in nature. The transmission coefficient (T_{WKB}) of the Landauer's conductance expression has been considered as the equivalent tunneling probability (T_{WKB}) from semi-classical model following Eq. (3.6). A more rigorous calculation considering source and drain contacts and their corresponding self-energy, and Fermi-Dirac distribution between the source and drain and effect from the gate is required to describe 'T_{WKB}' properly. Moreover, a self-consistent calculation of the number of 'modes' is essential to describe the semi-quantum analytical model completely since the number of modes in on- and off- states differs based on the bias conditions. For these reasons, the semi-quantum analytical model differs in describing current transport in GNR TFET when compared with semi-classical analytical model and NEGF simulation.

Table 3.1

Comparison of n-type GNR TFET performance from different current transport models

Model	V_{DD} (V)	V_{GS} (V)	Channel (nm)	t_{ox} (nm)	Drive Current, I_D (μA/μm)	OFF State Leakage Current, I_{OFF} (μA/μm)	Leakage Power, $V_{DD}I_{OFF}$ (μW/μm)	Dynamic Power ½ I_DV_{DD} (μW/μm)	I_{ON}/I_{OFF}	Subthreshold Slope (mV/dec)	I_{60} (μA/μm)
Analytical Model [2]	0.1	0.1	L=20 W=5	1	1.51×10^{-5}	1.2×10^{-11}	1.2×10^{-12}	7.55×10^{-7}	1.25×10^{6}	14.15	3.8×10^{-6}
Semi-classical Analytical Model	0.1	0.1	L=20 W=4.9	1	6.2×10^{-6}	5.05×10^{-8}	5.05×10^{-9}	3.1×10^{-7}	122	26	4.2×10^{-6}
Semi-quantum Analytical Model	0.1	0.1	L=20 W=4.9	1	1.6×10^{-5}	9.8×10^{-7}	9.8×10^{-8}	8×10^{-7}	16.3	69	Does not provide
NEGF-based Simulation	0.1	0.1	L=20 W=4.9	1	5.95×10^{-6}	5.145×10^{-8}	5.15×10^{-9}	2.9×10^{-7}	116	27.4	4.4×10^{-6}

3.5 Subthreshold Slope of GNR TFET

For energy efficient switching technique, subthreshold swing (SS) of TFETs is required to be below the thermionic limit of 60 mV/decade of conventional MOSFETs. In order to verify the suitability of the studied current transport model for digital circuit design, SS of all three models are compared. Figure 3.2(b) shows a decade change of drain current (I_D) from which SS is calculated. This method expresses the conventional SS as, $SS = \ln(10)[I_D / (dI_D / dV_{GS})]$. Using this method, the semi-classical model and NEGF simulation give a SS of 26 mV/decade and 27 mV/decade, respectively. SS for semi-quantum model is 71 mV/decade in this case. Moreover, following the method of Seabaugh and Zhang in [23], effective swing is determined as follows:

$$SS_{eff} = (V_{DD} / 2) / \log_{10}(I_{TH} / I_{OFF}) \tag{3.26}$$

where I_{TH} is the current at threshold voltage (V_{TH}) and I_{OFF} is the off current determined at V_{GS} = 0V. In [23] V_{TH} is considered as the half of the supply voltage ($V_{TH} = V_{DD}/2$) which returns I_{TH} as I_D at $V_{DD}/2$. Following this notation and after extracting the corresponding value of $V_{DD}/2$ as 0.05 V, SS for all three models is also evaluated from Fig. 3.2(b) using Eq. (3.26). Here, calculated SS is 28 mV/decade for the semi-classical model and 27 mV/decade for the NEGF simulation. Both of these values closely match with previously mentioned values of SS. SS of 68 mV/decade is obtained from this method for semi-quantum model.

Here we propose a method of estimating average subthreshold swing using point slope method which depends on the bias voltage at the gate and corresponding TFET current ratio at that point. This can be written as follows:

$$SS_{avg} \approx (V_{GS}) / \log_{10}(I_{D,V_{GS}} / I_{OFF}) \tag{3.27}$$

Note, the above expression is similar to Eq. (3.26) with minor changes that make it independent of threshold voltage and applicable to any order magnitude of drain current. Using Eq. (3.27), SS for all three models is calculated as specified in Fig. 3.2(b). Using V_{GS} of 0.04 V and corresponding I_D at V_{GS} = 0.04 V and V_{GS} = 0 V from Fig. 3.2(b), calculated values of SS from semi-classical, semi-quantum and NEGF simulation are 26 mV/decade, 69 mV/decade and 27.4 mV/decade, respectively. The values of SS mentioned in Fig. 3.2(b) and Table 3.1 are obtained using Eq. (3.27). Based on the rigorous calculation and comparison of SS for all three models, it is evident that semi-classical analytical model can predict the current transport in GNR TFET very similar to the numerical simulation using NEGF formalism. However, the semi-quantum analytical model lags such proximity due to inherent weakness in calculating SS as discussed earlier. For circuit simulation, the semi-classical analytical model can be fairly adopted for large scale integration.

3.6 Estimation of Subthreshold Swing Point, I_{60}

One of the most important figure of merits for TFET is the highest current where subthreshold slope of 60 mV/decade is obtained [24]. This parameter is written as 'I_{60}' and has the unit of μA/μm. For a TFET to be competitive with MOSFET, I_{60} should be 1-10 μA/μm. However, existing theoretical, experimental and simulated results have shown that I_{60} is still lagging behind this range. Note, current has been normalized along the channel width.

Figure 3.2(a) shows the point for I_{60} estimation where the drain current makes a transition from sub-60 to super-60 with respect to gate bias. Both the semi-classical analytical model and NEGF simulation approximates I_{60} around $4x10^{-6}$ μA/μm, however, I_{60} remains undeterminable for semi-quantum analytical model. As calculated earlier, average SS for semi-quantum model is 69 mV/decade for which the point slope does not converge to a specific point where SS makes a

transition from sub-60 and super-60 region. Compared to the earlier reported I_{60} of $2x10^{-6}$ μA/μm in [25], 10^{-5} μA/μm in [26] and $3x10^{-5}$ μA/μm in [27], estimated value of I_{60} falls within an acceptable range.

3.7 Output Characteristic of GNR TFET

Figure 3.3 shows output characteristic (I_D - V_{DS}) of n-type a-GNR TFET using the three current transport models studied in this work for different V_{GS}. The semi-classical analytical model shows good agreement with the results obtained from the numerical simulation, however, the semi-quantum model differs largely.

For a fixed V_{GS}, a constant amount of carriers tunnel through the source-channel tunnel junction. For V_{DS} = 0 V and V_{GS} > 0 V, a small tunneling window is opened at the source-channel tunnel junction which works as the origin of leakage current. From Eq. (3.7), maximum electric field at the source-channel tunnel junction has linear dependence on V_{DS} which is used to determine T_{WKB}. It is obvious from Eq. (3.7), for a fixed V_{GS}, junction maximum electric field will solely depend on $V_{DS.}$ As a result, tunneling probability depends exponentially on V_{DS}. For a fixed V_{GS} with varying $V_{DS,}$ semi-quantum model is now strongly governed by the difference in source-drain Fermi level. Therefore, any change in drain current calculated by semi-quantum model is also strongly controlled by V_{DS} as opposed to V_{GS} dependence of semi-classical and NEGF simulated current transport models. For this reason a large deviation of semi-quantum model is observed in Fig. 3.3 compared to semi-classical analytical model and numerical simulation. Compared to output characteristics of conventional MOSFETs where V_{DS} governs channel electric field and affects pinch-off and velocity saturation, output characteristics in TFET not only depends on V_{GS} but also on V_{DS}. Especially in reduced dimensional materials as in graphene such behavior is often observed. Current transport equations of Eq. (3.18) and (3.25)

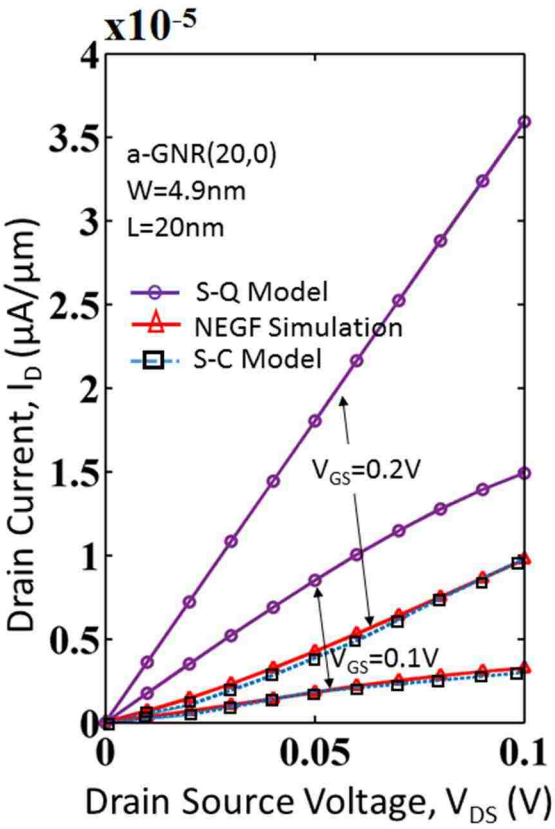


Figure 3.3: I_D - V_{DS} characteristic of n-type GNR TFET for semi-classical analytical model, semi-quantum analytical model and NEGF simulation for V_{GS} = 0.1 V and V_{GS} = 0.2 V.

derived from semi-classical and semi-quantum considerations, respectively, can be used also for p-type GNR TFET n-i-p structure shown in Fig. 3.1(a) with opposite voltage polarities.

3.8 Width Dependent Performance Analysis of GNR TFET

In this section, performance of GNR TFET is examined for different number of atoms along the GNR width. As the number of atoms varies along the width, electronic properties of armchair nanoribbon change, based on any one of $3N$, $3N$+1 and $3N$+2 configurations along with the associated band gap of nanoribbon [21]. As a result, GNR TFET performance also changes. To get suitable performance from GNR TFET, appropriate chirality of GNR needs to be selected.

Since the band gap of GNR is determined using first principles L(S)DA approximation, band gaps of GNR are nonzero and direct irrespective of width. This can be observed in Table 3.2 for GNR with different width. The major difference between tight binding and first principles based energy gaps calculation is observed for $3N$+2 configuration. The method used for estimating GNR energy band gap in NanoTCAD ViDES can be understood as follows: a GNR (7,0) has 14 atoms considering both sides of an unrolled carbon nanotube. Hence, these 14 atoms represents $3N$+2 configuration (for N = 4) instead of $3N$+1 representing 7 (for N=2). Similarly, a GNR (10,0) has 20 atoms considering both sides of an unrolled carbon nanotube atoms and represents $3N$+2 configuration (for N=6) instead of $3N$+1 representing 10 (for N=3). The energy band gaps in Table 3.2 are calculated using this method. Among the considered chiral armchair nanoribbons, GNR TFET with (*20,0*) and (*11,0*) chiral nanoribbon represents $3N$+2 configuration. In conventional tight binding method based calculation of GNR band gap, 3N+2 configuration provides metallic GNR whereas first principles method considers 3N+2 as semiconducting as well. For this reason a band gap is observed for (*20,0*) and (*11,0*) chiral nanoribbons. A higher on/off current ratio are seen in Table 3.2 for semi-classical and NEGF

Table 3.2

Performance comparison of n-type GNR TFET for different GNR width and band gap

GNR	V_{DS} (V)	V_{GS} (V)	Band Gap (eV)	GNR Width (nm)	NEGF Simulation			Semi-classical Model			Semi-quantum Model		
					OFF Current (μA/μm)	ON Current (μA/μm)	I_{ON}/I_{OFF}	OFF Current (μA/μm)	ON Current (μA/μm)	I_{ON}/I_{OFF}	OFF Current (μA/μm)	ON Current (μA/μm)	I_{ON}/I_{OFF}
(7,0)	0.1	0.1	0.13	1.62	9.3×10^{-7}	7.5×10^{-6}	8	1×10^{-6}	7.3×10^{-6}	7.3	4.9×10^{-7}	6.4×10^{-6}	13
(10,0)	0.1	0.1	0.092	2.37	3.8×10^{-6}	7.7×10^{-6}	2	1.9×10^{-6}	3.7×10^{-6}	1.9	5.8×10^{-7}	9.6×10^{-6}	16.6
(11,0)	0.1	0.1	0.52	2.61	3.5×10^{-9}	4.6×10^{-7}	46	2.9×10^{-10}	5×10^{-7}	1724	2.94×10^{-7}	4.7×10^{-6}	15.98
(12,0)	0.1	0.1	0.313	2.86	1.9×10^{-7}	6.5×10^{-6}	34	2.2×10^{-7}	6.3×10^{-6}	29	5.4×10^{-7}	8.7×10^{-6}	16.1
(15,0)	0.1	0.1	0.252	3.62	9.3×10^{-8}	6.6×10^{-6}	71	8.6×10^{-8}	6.8×10^{-6}	79	7.7×10^{-7}	1.3×10^{-5}	16.9
(20,0)	0.1	0.1	0.289	4.9	5.1×10^{-8}	5.9×10^{-6}	116	5×10^{-8}	6.2×10^{-6}	122	9.8×10^{-7}	1.6×10^{-5}	16.3

simulations. However, on/off current ratio obtained for (*11,0*) GNR in semi-classical model differs largely compared to other two current transport models. For (*11,0*) chiral GNR, the on-state drive current in semi-classical model ($5x10^{-7}$ μA/μm) matches closely with the that obtained from NEGF simulation ($4.6x10^{-7}$ μA/μm), however, off- state leakage current differs by a decade of magnitude. It is important to note that method of calculating off- state leakage current in these two models are different. Following Eqs. (3.2) and (3.16), off- state leakage current in semi-classical analytical model has built-in potential (φ_{BI}) and band gap (E_G) dependence. A GNR with large band gap provides a significantly large built-in potential as read from Eq. (3.2). This limits additional thermionic transport over the barrier at off- state and results in low leakage current. Moreover, condition of $V_{BI} + V_{DS} < 2E_G$ to limit additional ambipolar tunneling at the off- state becomes $V_{BI}+V_{DS} << 2E_G$ for $V_{DS} << 2E_G$. Both of these conditions lower the off- state leakage current for larger GNR band gap in semi-classical analytical model for which a high on/off current ratio is observed for (*11,0*) GNR. In contrast to compact semi-classical analytical model, NEGF simulation adopts rigorous Newton-Raphson method with a predictor corrector scheme to calculate the charge density and channel electrostatic potential. The simulation thereby takes into account the deeper detail of current transport mechanism in estimating even the leakage current. This could be one of the limitations of the semi-classical analytical current transport model to differ from NEGF simulation.

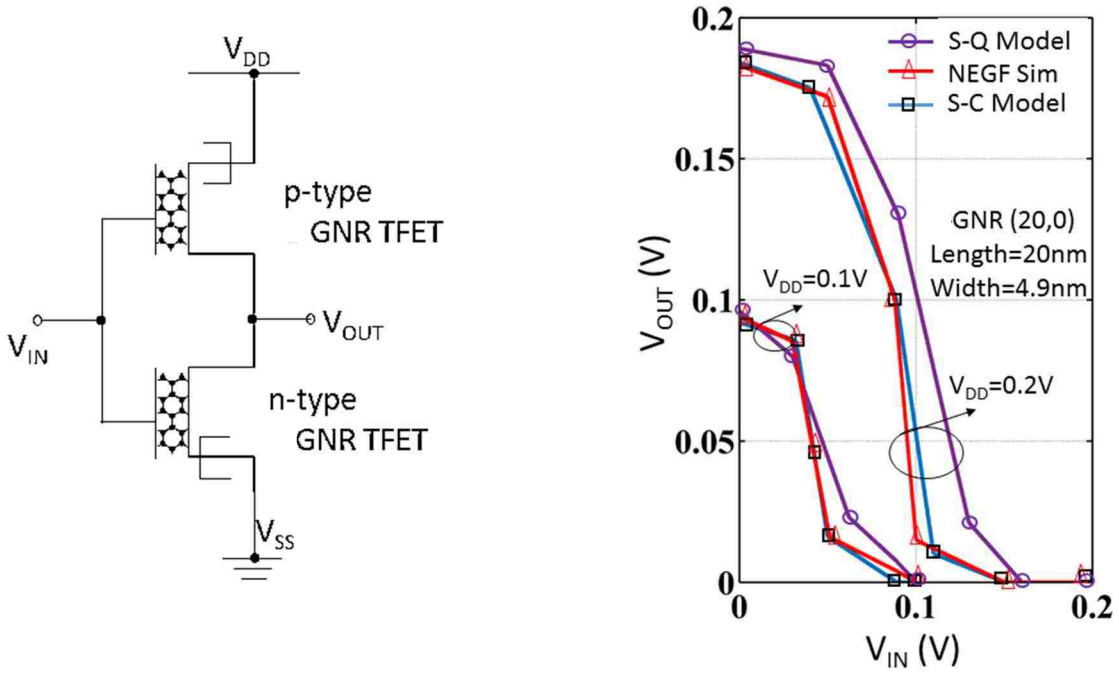
However, a better description of off- state leakage current considering quantum confinement and energy states from GNR edges can solve this problem and substantiate the semi-classical analytical model as a reliable tool for circuit simulation.

3.9 Voltage Transfer Characteristics of GNR TFET Complementary Inverter

Figure 3.4(a) shows schematic of a complementary GNR TFET inverter for operation at different supply voltages and is similar to CMOS inverter in design and operation. Characteristics of GNR TFET inverter is plotted from all three current transport models. At input logic level "1" (either 0.1 V or 0.2 V), n-type GNR TFET turns ON, p-type GNR TFET is OFF and output gives logic "0". Similarly when input is at logic "0" (0 V), p-type GNR TFET turns ON and n-type GNR TFET is OFF, output is at logic "1" (either 0.1 V or 0.2 V for the case in Fig. 3.4(b)). Figure 3.4(b) shows plot of voltage transfer characteristics (VTC) of the complementary GNR TFET based inverter of Fig. 3.4(a) for GNR for (*20,0*) chirality and V_{DD}=0.1 V and 0.2 V supply voltages. Following the transfer characteristics obtained for all three current transport models, VTC of GNR TFET inverter also shows good agreement between semi-classical analytical model and NEGF simulation. However, semi-quantum analytical model differs from both of these models in this case as well. A decrease in the logic "1" is observed due to inherent leakage current at off state for both transistors. However, sharp transition between on to off state is observed at reduced supply voltage. The VTC shown in Fig. 3.4(b) confirms the reliable use of semi-classical analytical model for digital circuit simulation with a good agreement with numerical simulation.

3.10 Conclusion

The semi-classical analytical model closely agrees with numerical simulation whereas significant difference between semi-quantum model and NEGF simulation is observed. Performance of n - type GNR TFET is also studied for GNR width variation. The semi-classical analytical current transport model of n - type GNR TFET can be applied to p-type GNR TFETs (n-i-p structure) with opposite voltage polarities. Promise of GNR TFET for digital logic



(a) (b)

Figure 3.4: (a) A complementary GNR TFET inverter circuit and (b) voltage transfer characteristic of GNR TFET inverter for different supply voltages.

application as a TFET inverter is studied by three current transport models. Characteristics sharp transition from ‘on’ to ‘off’ condition is observed for lower supply voltage. By comparing the semi-classical analytical model with the numerical simulation it is evident that the semi-classical analytical model derived can predict near similar performance of GNR TFET for different figure of merits. However, semi-quantum analytical model differs from simulation due to inherent limitation in calculation and hence it is not yet reliable in its current form. Therefore we conclude the semi-classical analytical current transport model as a powerful tool for circuit simulation for digital integrated circuit design.

3.11 References

[1] X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai, "Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors," *Phys. Rev. Lett.,* vol. 100, pp. 206803, 2008.

[2] Q. Zhang, T. Fang, H. Xing, A. Seabaugh, and D. Jena, "Graphene nanoribbon tunnel transistors," *IEEE Elect. Dev. Lett.,* vol. 29, pp. 1344-1346, 2008.

[3] P. Zhao, J. Chauhan, and J. Guo, "Computational study of tunneling transistor based on graphene nanoribbon," *Nano Letters,* vol. 9, pp. 684-688, 2009.

[4] G. Fiori, A. Betti, S. Bruzzone, and G. Iannaccone, "Lateral graphene–hBCN heterostructures as a platform for fully two-dimensional transistors," *ACS Nano,* vol. 6, pp. 2642-2648, 2012.

[5] R. K. Ghosh and S. Mahapatra, "Proposal for graphene boron nitride heterobilayer-based tunnel FET," *IEEE Trans. Nanotech.,* vol. 12, pp. 665-667, 2013.

[6] G. Fiori and G. Iannaccone, "Ultralow-voltage bilayer graphene tunnel FET," *IEEE Elect. Dev. Lett.,* vol. 30, pp. 1096-1098, 2009.

[7] Y. Yoon and S. Salahuddin, "Dissipative transport in rough edge graphene nanoribbon tunnel transistors," *Appl. Phys. Lett.,* vol. 101, pp. 263501, 2012.

[8] J. Knoch and J. Appenzeller, "Tunneling phenomena in carbon nanotube field-effect transistors," *physica status solidi (a),* vol. 205, pp. 679-694, 2008.

[9] K. Boucart and A. M. Ionescu, "A new definition of threshold voltage in Tunnel FETs," *Solid State Elect.,* vol. 52, pp. 1318-1323, 2008.

[10] A. Ortiz-Conde, F. J. García-Sánchez, J. Muci, A. Sucre-González, J. A. Martino, P. G. D. Agopian, and C. Claeys, "Threshold voltage extraction in Tunnel FETs," *Solid State Elect.,* vol. 93, pp. 49-55, 2014.

[11] G. Giovannetti, P. A. Khomyakov, G. Brocks, V. M. Karpan, J. van den Brink, and P. J. Kelly, "Doping graphene with metal contacts," *Phys. Rev. Lett.,* vol. 101, pp. 026803, 2008.

[12] S. M. Sze and K. K. Ng, "Tunnel Devices," in *Physics of Semiconductor Devices*, ed: John Wiley & Sons, Inc., 2006, pp. 415-465.

[13] T. Fang, A. Konar, H. Xing, and D. Jena, "Carrier statistics and quantum capacitance of graphene sheets and ribbons," *Appl. Phys. Lett.,* vol. 91, pp. 092109, 2007.

[14] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science,* vol. 306, pp. 666-669, 2004.

[15] M. S. Fahad, A. Srivastava, A. K. Sharma, and C. Mayberry, "Current transport in graphene tunnel field effect transistor for RF integrated circuits," in *IEEE International Wireless Symposium (IWS)*, pp. 1-4, 2013.

[16] D. Jena, T. Fang, Q. Zhang, and H. Xing, "Zener tunneling in semiconducting nanotube and graphene nanoribbon p-n junctions," *Appl. Phys. Lett.,* vol. 93, pp. 112106, 2008.

[17] H. Lu, D. Esseni, and A. Seabaugh, "Universal analytic model for tunnel FET circuit simulation," *Solid State Elect.,* vol. 108, pp. 110-117, 2015.

[18] S. Datta, *Quantum Transport: Atom to Transistor*: Cambridge University Press, 2005.

[19] M. Lundstrom and C. Jeong, *Lessons from Nanoscience: A Lecture Note Series Near-Equilibrium Transport*: World Scientific, 2012.

[20] G. Fiori and G. Iannaccone. (2013). *NanoTCAD ViDES*. Available: www.nanotcad.com/vides

[21] Y. W. Son, M. L. Cohen, and S. G. Louie, "Energy gaps in graphene nanoribbons," *Phys. Rev. Lett.,* vol. 97, pp. 216803, 2006.

[22] M. Luisier and G. Klimeck, "Performance analysis of statistical samples of graphene nanoribbon tunneling transistors with line edge roughness," *Appl. Phys. Lett.,* vol. 94, pp. 223505, 2009.

[23] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. of the IEEE,* vol. 98, pp. 2095-2110, 2010.

[24] W. G. Vandenberghe, A. S. Verhulst, B. Sorée, W. Magnus, G. Groeseneken, Q. Smets, M. Heyns, and M. V. Fischetti, "Figure of merit for and identification of sub-60 mV/decade devices," *Appl. Phys. Lett.,* vol. 102, pp. 013510, 2013.

[25] R. Gandhi, C. Zhixian, N. Singh, K. Banarjee, and L. Sungjoo, "Vertical Si-Nanowire n-type tunneling FETs with low subthreshold swing (<50mV/decade) at room temperature," *IEEE Elect. Dev. Lett.,* vol. 32, pp. 437-439, 2011.

[26] B. Ganjipour, A. W. Dey, B. M. Borg, M. Ek, M.-E. Pistol, K. A. Dick, L.-E. Wernersson, and C. Thelander, "High current density Esaki tunnel diodes based on GaSb-InAsSb heterostructure nanowires," *Nano Letters,* vol. 11, pp. 4222-4226, 2011.

[27] K. Sung Hwan, H. Kam, C. Hu, and T. J. K. Liu, "Germanium-source tunnel field effect transistors with record high I_{ON}/I_{OFF}," in *Symposium on VLSI Technology,* pp. 178-179, 2009.

CHAPTER 4*

GRAPHENE AND BORON NITRIDE JUNCTIONLESS TUNNEL EFFECT TRANSISTOR

4.1 Introduction

Atomically thin two dimensional graphene has emerged as a potential candidate for next generation electronics due to its unique electronic properties. However, single layer graphene is a zero bandgap semiconductor. As discussed in the previous chapters, band gap engineering is required for obtaining a band gap in graphene. Undoubtedly, this makes the fabrication process complicated. In absence of a bandgap, graphene field effect transistor suffers from poor on/off current ratio with high off-state leakage current. Following the ITRS requirement [1] of energy efficient circuit design, a minimum on/off current ratio of 10^4 is required for a supply voltage below 0.7 V for digital applications. Performance of existing graphene-based MOS-type transistors are still lagging behind unless graphene is lithographically patterned to GNR or chemically synthesized.

In order to resolve the issue of on/off current ratio, vertical heterostructure consisting of multilayer stacks of graphene and other atomically thin two dimensional materials such as boron nitride and the transition metal dichalcogenides have been proposed for different transistor structures [2-11]. Basically interlayer tunneling technique discussed in Chapter 1 is employed in these type of transistors. Majority of these transistors contain two graphene conducting layers

*Part of this work is reported in the following publications:

1. A. Srivastava and M. Fahad, "Vertical Interlayer Tunnel Field Effect Transistor Using Hexagonal Boron Nitride," LSU Application No. LSU-2016-049, filed provisional patent, Dec 2016.
2. Md S Fahad and Ashok Srivastava, "A graphene switching transistor for vertical circuit design," *ECS Journal of Solid State Science and Technology*, Vol. 5, Issue. 3, M13-M21, 2016.

separated by a thin tunneling barrier. These transistors are commonly known as interlayer tunnel field effect transistor (iTFET). Schematic of a conventional n-channel MOSFET, a p-i-n band-to-band tunnel field effect transistor (TFET) and an iTFET are shown in Figs. 4.1(a), (b) and (c), respectively for distinction. High on/off current ratio, sharp resonant tunneling characteristic and suitability for flexible and transparent electronics are some of the reported key features of this graphene iTFET. However, these transistors lag the potential for digital integrated circuit design considering the requirements of steep subthreshold slope and high drive current. Due to fundamental physical limit, subthreshold slope of such iTFET cannot go below the thermionic limit of 60 mV/decade detail of which is will be discussed in Chapter 5. Moreover, high supply voltage (> 2 V) is also required for operation in some of the reported iTFETs. Studies of some of these devices have been carried out at cryogenic temperatures with poor performance at the room temperature. Therefore, an improved current transport mechanism in a novel device structure is essential for making such iTFETs competitive for next generation more than Moore's era.

In iTFET, source and drain contacts are placed at the two opposite conducting layers as seen in Fig. 4.1(c) contrary to contacts in conventional four terminal MOSFET shown in Fig. 4.1(a) and TFET shown in Fig. 4.1(b), In this way, a bias between drain and source (V_{DS}) controls the vertical interlayer tunneling of carriers between the two conducting materials separated by a tunneling barrier. However, V_{DS} overshadows the actual control of channel electrostatic potential by the gate voltage [7]. For this reason, linear resistive behavior is obtained as opposed to current saturation at different gate biases of output characteristics [8]. This impedes iTFETs' prospect in digital logic circuits. Apart from this, observed negative differential resistance (NDR) also undermines the scope of iTFETs. Therefore, a graphene switching transistor meeting the ITRS requirement with high on/off current ratio, steep subthreshold slope,

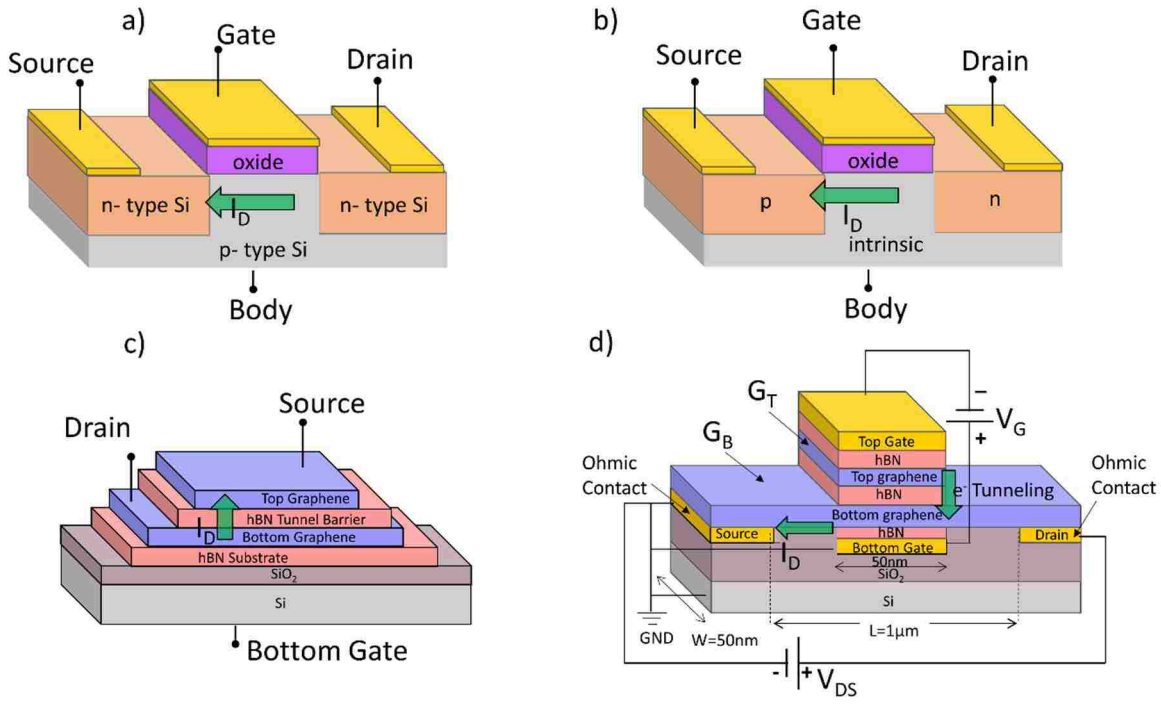


Figure 4.1: (a) Schematic of a conventional n - channel depletion type MOSFET, (b) schematic of conventional p - i - n n - type band-to-band tunnel field effect transistor (TFET), (c) schematic of n - type interlayer tunnel field effect transistor (iTFET) and (d) schematic of a n - type graphene junctionless tunnel effect transistor (JTET). Note, G_B refers the bottom graphene layer and G_T refers the top graphene layer. The arrow in each of the device structures shows the direction of current flow except the vertical arrow in Fig. 4.1(d), which shows vertical interlayer tunneling of electrons from top to bottom graphene layer.

non-resonant high drain current and drain current saturation at sub-0.5V operation is necessary for graphene to be suitable for digital integrated circuit design.

In this chapter, modeling of a graphene switching transistor is discussed considering graphene-hBN-graphene vertical heterostructure and named as junctionless tunnel effect transistor (JTET). JTET is one types of iTFET as referred in Chapter 1 earlier. Schematic of graphene JTET is shown in Fig. 4.1(d) which is significantly different from the generic iTFET as shown in Fig. 4.1(c). However, graphene JTET ensembles similarity with a MOSFET shown in Fig. 4.1(a) in terms of the location of source and drain. Compared to MOSFET, TFET and iTFET, graphene JTET adopts a different method for controlling the channel barrier height. JTET utilizes vertical tunneling of electrons between top and bottom graphene layers through hBN to control the channel barrier height between source and drain that eventually regulates the ballistic transport between source and drain at the bottom graphene layer.

Compared to planar MOSFET where a gate bias fully depletes the channel by "field effect" and inverts the channel's majority carrier type, JTET operates based on gate induced "tunneling effect". In addition to that, JTET doesn't require any doping in source, channel or drain regions and inherently remains junctionless for which it is termed as 'junctionless tunnel effect transistor (JTET)'. Compared to planar TFET, JTET is also free from any depletion region originating from high doping concentration and thus becomes suitable for both channel length scaling and vertical integration. For transport mechanism in JTET, analytical compact current transport model has been derived in this chapter for understanding of the device physics of JTET. Further, performance of graphene JTET is compared with ITRS projected 2020 nMOSFET as well. Similar to a CMOS inverter, a complementary graphene JTET (p-type JTET and n-type JTET) inverter is designed and voltage transfer characteristics studied.

4.2 Device Structure and Operation

Figure 4.1(d) shows schematic of the graphene JTET based on graphene-hBN-graphene. Over the Si/SiO_2 substrate a bottom gate contact is placed followed by the multilayer boron nitride deposition as the gate dielectric. Thermal evaporation or sputtering technique can be employed for the formation of contacts. First principle density functional theory (DFT) has shown that graphene doped by adsorption on metal substrates still preserves its unique electronic properties. A small shift in Fermi level at the graphene Dirac point by ~0.5 eV is observed [12]. For simplicity, in our current transport model, we have assumed zero shift in graphene Fermi level due to the metal contact. Multilayer hBN can be deposited by micromechanical cleavage technique from boron nitride crystal. The buried layers of hBN work as the bottom gate dielectric for the gate contact and a substrate for the bottom graphene layer.

Boron nitride substrate preserves graphene's electronic properties compared to SiO_2 substrate for which hBN is considered as both top and bottom gate dielectrics [13]. Moreover, hBN graphene lattice mismatch is 1.7% for which hBN is suitable as an interlayer tunneling barrier [14]. We have assumed ohmic contacts in source and drain. For top and bottom gates, a metal-insulator-graphene tunneling junction is formed through metal-hBN-graphene heterostructure. This provides a low differential contact resistance because of hBN-graphene very low lattice mismatch. Deposition of graphene layer can be carried out using any of the techniques as discussed in Chapter 2. The graphene layer on top of the buried hBN is referred to as bottom graphene layer (G_B). Source and drain contacts are placed at the two ends of G_B as seen in Fig. 4.1(d). Atomically thin multilayer hBN are then deposited on the top of G_B followed by a second layer deposition of graphene. This layer is defined as the top graphene layer (G_T). Finally, multiple layers of hBN are further deposited on G_T as the top gate dielectric followed by

the metal contact deposition. The top metal contact is termed as the top gate contact. The graphene JTET discussed in this chapter considers an effective channel area of 0.05 μm^2 with a channel length of 1 μm and a width of 50 nm. It has been observed experimentally that electrons can propagate without scattering, a distance in micrometer range in graphene [15] for which we have assumed an idealistic scattering free graphene channel of 1μm. Moreover, such a channel length simplifies the current transport model from the complexity arising from short channel effects and reduces the probability of direct source-drain tunneling effect. The drain current is also less affected by the drain induced barrier lowering (DIBL) for the considered channel length in graphene JTET.

It is found that quantum confined graphene in its nanoribbon shape (length >> width) demonstrates an observable band gap depending on its edge type [15]. The bandgap of graphene nanoribbon increases as the width of nanoribbon reduces for armchair graphene nanoribbon. Therefore, a graphene channel of 50 nm width ensures a zero bandgap semiconductor. It is to be noted that the channel width << 50 nm (1-10 nm) will open up a band gap which will change the current transport mechanism in graphene JTET whereas channel width > 50nm will have potentially no additional effect on the current transport. Therefore, the assumption of 50 nm channel width in this section provides a good approximation between graphene and graphene nanoribbon. Following the work of Britnell et al. [2], graphene JTET considers top and bottom hBN gate dielectrics of 20 nm thickness each. The thickness of the interlayer tunneling barrier is 1.02 nm for three hBN layers. Sciambi et al. [16] have studied that two graphene layers separated by a nanometer scale tunneling barrier, preserves not only the coherent length of tunneling but also conserves the out of plane momentum of carriers. The coherent length of tunneling drastically degrades as the tunneling barrier thickness increases [16]. Therefore, we have

considered 1.02 nm of hBN as the thickness of tunneling barrier of three layers of hBN. It is to be noted that a single layer of hBN is 0.34 nm thick [17]. Nevertheless, single or bilayer of hBN can also be adopted which are more susceptible to etching in such vertical heterostructures.

In the off-state, the Fermi levels of top and bottom graphene layers remain in equilibrium. We assume at equilibrium the Fermi level coincides with the channel Dirac point and no intermediate energy states exist due to roughness or defects. Gate voltage (V_G) is defined as the difference between the bottom (V_{GB}) and top gate voltages (V_{GT}). To turn-on the transistor, V_G ($V_G = V_{GT} - V_{GB}$) is applied between G_T and G_B. V_{DS} is applied between source and drain. Device off-state is defined for $|V_G| = 0$ V, $|V_{DS}| = 0.1$ V and on-state for $|V_G| \neq 0$ V, $|V_{DS}| = 0.1$ V.

For low power dissipation, supply voltage of any switching transistor needs to be compliable with one of the ITRS requirements. Existing silicon and III-V material-based TFETs operate at sub-0.5 V supply voltage for which it is essential for the switching transistor to operate at equal or low supply voltage. Moreover, it is found that the graphene-based transistors can be operated at low supply voltages for which the assumption of 0.1 V operation of graphene JTET is in accordance with the existing TFET performance and ITRS requirement.

Figure 4.2(a) shows off-state of graphene JTET. E_F^S, E_F^C and E_F^D are source, channel and drain Fermi levels, respectively. As V_G is applied, interlayer tunneling of carrier occurs between top and bottom graphene layers. The carrier concentration (N) due to tunneling, shifts E_F^C from the Dirac point of the channel graphene layer by an amount of ΔE_F as seen in Fig. 4.2(b) [18]. Considering both the vertical tunneling between graphene layers and corresponding lateral planar transport in the bottom graphene channel, the off and on states are shown in Fig. 4.2(c) and 4.2(d), respectively.

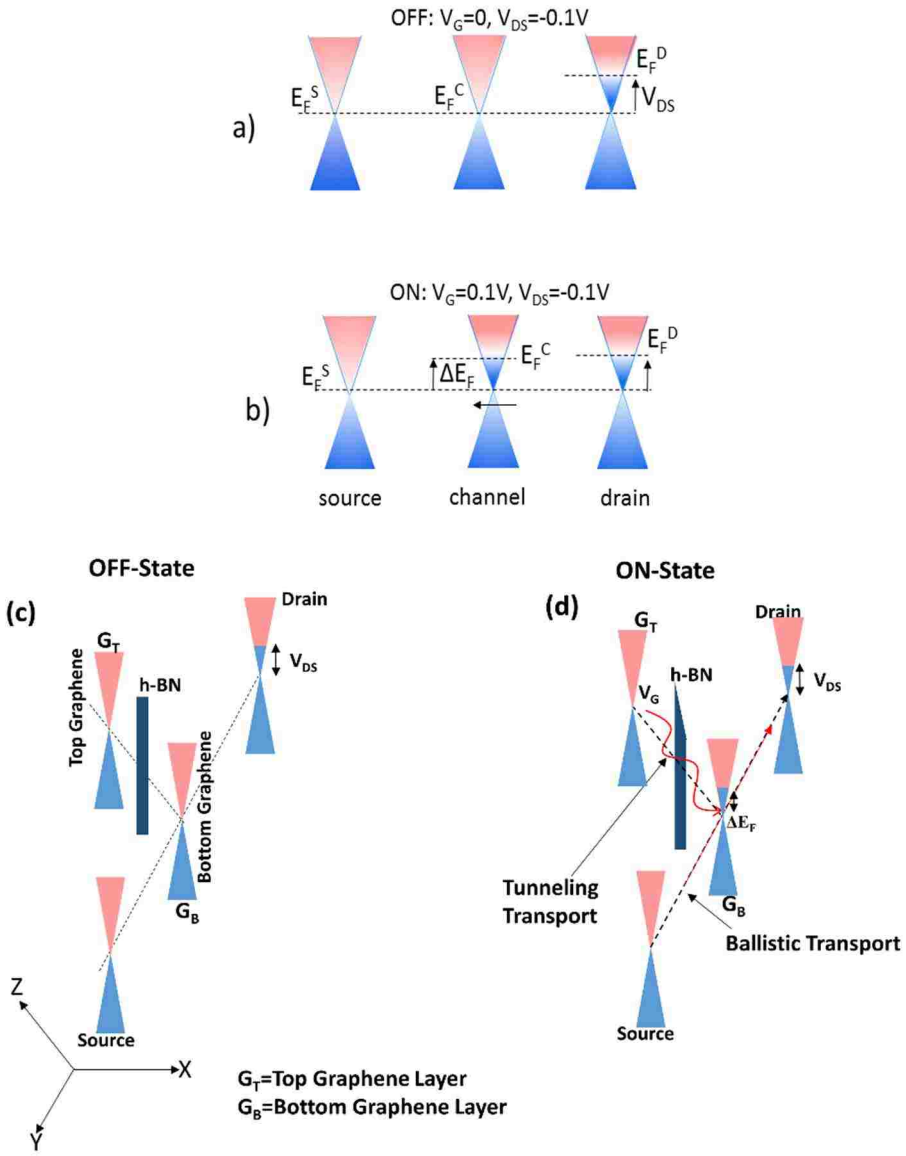


Figure 4.2: (a) Energy band diagram of graphene JTET in off- state for V_G = 0V and V_{DS} = - 0.1 V, (b) on-state for V_G = 0.1 V and V_{DS} = - 0.1 V, (c) schematic of energy band diagram drawn (not to scale) in both vertical (Z) direction and lateral (X-Y) direction in off state and (d) schematic of energy band diagram drawn (not to scale) in both vertical (Z) direction and lateral (X-Y) direction in on state. Note: Parabolas represent the E-k diagram of graphene and rectangular bar represents energy barrier of hBN.

This shift in Fermi level results in change of barrier height between E_F^S and E_F^D which controls the current transport between source and drain due to V_{DS}. In this way, drain current becomes a function of vertical tunneling of carriers between the top and bottom graphene layers. It should be noted that, the bottom graphene layer is also the channel graphene layer.

Based on the experimental study in [4], it is found that a positive gate bias shifts the Fermi level above the Dirac point whereas a negative gate bias shifts the Fermi level below the Dirac point. Therefore, $V_G > 0$ provides $\Delta E_F < 0$ and $V_G < 0$ provides $\Delta E_F > 0$. The channel barrier height is controlled by the vertical interlayer tunneling between two graphene layers. It is important to note that in conventional iTFET, the interlayer tunneling bias results the tunnel drain current whereas in graphene JTET, the interlayer tunneling bias changes the channel barrier height which regulates the source-drain ballistic transport. Conventional iTFET does not discuss any source-drain ballistic transport mechanism.

As the Dirac point at the top and bottom graphene layers are misaligned, an interlayer tunneling carriers cross the tunneling barrier. Electrons having the energy half way between the Dirac points contribute toward this flow [4]. A change in such tunneling of carriers due to gate voltage is also confirmed by the phenomena of wave function extension of one graphene layer to the other and a corresponding overlap at the bottom graphene layer. For both positive and negative gate voltages, the wave function extension is observed [16]. In this way, the out of plane momentum is conserved for a longer coherent length for tunneling, preferably in a nanometer range [8]. We assume that the source and drain wave functions do not result in any interference with the wave function extended from the top graphene layer to the bottom graphene layer. The net vertical interlayer tunneling between top and bottom graphene layers, therefore, only contributes toward the barrier control of the channel electrostatic potential.

4.3 Current Transport Model

4.3.1 Estimation of Tunneling Probability

The change of the effective barrier height via the shift in Fermi level of graphene is dominated by the height and shape of the barrier [4]. It has been observed that using wide bandgap monolayer of two dimensional semiconductor, the changes in Fermi level of the graphene due to external bias are near to or more than the height of the tunneling barrier. However, in the case of wide bandgap insulator, such changes in the Fermi level of graphene are insignificant. Wide bandgap insulator like hBN (bandgap > 5 eV) helps in this regard.

In this Section, tunneling probability for a specific tunneling energy barrier height (Δ) and thickness (d) are considered in determining the tunneling probability of carriers from the top graphene layer to the bottom graphene layer and vice-versa. Tunneling probability (T_{WKB}) is calculated from the well-known WKB approximation which has been discussed in detail in Chapter 1 and is written as follows [4]:

$$T_{WKB}(E) = \exp(-2d\frac{\sqrt{2m^*\Delta}}{\hbar}) \tag{4.1}$$

In Eq. (4.1), d is the thickness of the tunneling barrier material, Δ is the energy gap between either graphene valence band to hBN valence band for holes or graphene conduction band to hBN conduction band for electrons and m^* is the effective mass of electron in the tunneling barrier material.

The separation between the graphene Dirac point and the top of the valence band of hBN (Δ) is 1.5 eV whereas this value is > 4 eV in case of hBN conduction band [18]. Following the work of Britnell et al. [2] we have chosen Δ as 1.5 eV. This yields an effective tunneling mass of holes, $m^*=0.5m_o$ (m_o is the free electron mass) which is also the effective mass for holes in hBN.

It has been observed that a barrier separating two graphene layers where Fermi surface in one side is electron like and is hole like on the other side demonstrates that electrons incident normally at one side continue to propagate as holes with 100% efficiency at the other side [19]. For this reason, the choice of Δ as 1.5 eV for hole conduction remains consistent. For relativistic carriers, a perfect tunneling probability of 1 can be obtained. However, for nonrelativistic electrons, this is not the case for which the tunneling probability is always less than 1. With a negligible inter-valley scatterings and very low lattice mismatch, a potential barrier shows no reflections for the electrons incident normal to the potential barrier [20]. In graphene JTET, it is assumed that electrons incident normal to the hBN barrier where graphene and hBN has a lattice mismatch of only 1.7%.

4.3.2 Estimation of Charge Density

When a bias is applied between top and bottom graphene layers, a corresponding potential difference between the two Fermi levels is observed. Considering the potential difference between top and bottom graphene layers as $\Delta\varphi$, carriers tunneling from top to bottom graphene layers are described as follows [21]:

$$N_1 = \int_0^{\Delta\varphi} D(E)T_{WKB}(E)f_T(E)dE\,, \tag{4.2}$$

Similarly the carriers tunneling from bottom to top graphene layers can also be expressed as follows:

$$N_2 = \int_0^{\Delta\varphi} D(E)T_{WKB}(E)f_B(E)dE\,, \tag{4.3}$$

Net carriers tunneling from top to bottom graphene layers can be written as follows:

$$N = N_1 - N_2 = \int_0^{\Delta\varphi} D(E)T_{WKB}(E)f_T(E)dE - \int_0^{\Delta\varphi} D(E)T_{WKB}(E)f_B(E)dE \tag{4.4}$$

$$N = \int_0^{\Delta\varphi} D(E)T_{WKB}(E)(f_T(E) - f_B(E)dE \tag{4.5}$$

Here $D(E)$ is the density of states of graphene, $f_T(E)$ is Fermi function for the top graphene layer, $f_B(E)$ is Fermi function for the bottom graphene layer, $T_{WKB}(E)$ is tunneling probability obtained from Eq. (4.1). $\Delta\varphi$ is the limit of integration. In this case, it is the total energy window between top and bottom graphene layers through which the tunneling occurs. Density of states in graphene layer is defined as follows [20]:

$$D(E) = \frac{g_s g_v E}{2\pi(\hbar v_F)^2}, \tag{4.6}$$

where E is the energy of electron tunneling. For the proposed current transport model of graphene JTET, energy range E is limited between 0 to $\Delta\varphi$. g_s and g_v are spin and valley degeneracy, respectively. For graphene, $g_s = 2$ and $g_v = 2$ [20]. Fermi function in top and bottom graphene layers are defined as follows:

$$f_T(E) = \frac{1}{1 + e^{\left(E - E_f^T\right)/k_B T}} \tag{4.7}$$

$$f_B(E) = \frac{1}{1 + e^{\left(E - E_f^B\right)/k_B T}} \tag{4.8}$$

In Eqs. (4.7) and (4.8), E_f^T and E_f^B are the positions of the Fermi levels at the top and bottom graphene layers, respectively. E is the energy of the electron during tunneling. Fermi level in top graphene layer is at $E_f^T = qV_G$ and the Fermi level in bottom graphene layer is at $E_f^B = 0$. Combining Eqs. (4.5) to (4.8),

$$N = \int_0^{\Delta\varphi} \frac{g_s g_v E}{2\pi(\hbar v_F)^2} T_{WKB}(E)\left(\frac{1}{1+e^{\left(E-E_f^T\right)/k_BT}} - \frac{1}{1+e^{\left(E-E_f^B\right)/k_BT}}\right)dE \tag{4.9}$$

Replacing the values of E_f^T and E_f^B by qV_G *and 0*, Eq. (4.9) can be expressed as follows:

$$N = \int_0^{\Delta\varphi} \frac{2E}{\pi(\hbar v_F)^2} T_{WKB}(E)\left(\frac{1}{1+e^{(E-V_G)/kT}} - \frac{1}{1+e^{(E)/kT}}\right)dE \tag{4.10}$$

The energy window for tunneling ($\Delta\varphi$) from top to bottom graphene layers is assumed as $\Delta\varphi = E_f^T - E_f^B = qV_G - 0 = qV_G$. Now integrating Eq. (4.10) from $E = 0$ to $E = \Delta\varphi = qV_G$, closed form of Fermi-Dirac integration becomes,

$$N = \frac{g_s g_v}{2\pi(\hbar v_F)^2} T_{WKB}(E)\left(\frac{V_G^{\,2}}{12} - (V_G)k_BT\ln[1+\exp(V_G/k_BT)] - \frac{(\pi k_BT)^2}{12} - (k_BT)^2\, Poly\log(2,-\exp(V_G/k_BT))\right) \tag{4.11}$$

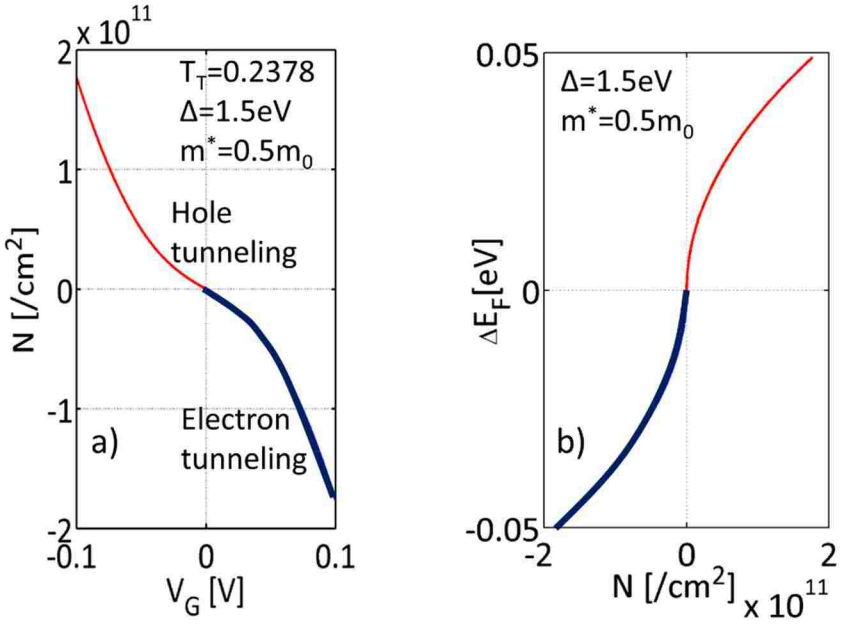
Now for any $qV_G >> k_BT$, it is found that the first few terms dominate over the later parts of Eq. (4.11) for which the higher energy terms in Eq. (4.11) can be simplified as follows:

$$\frac{V_G^{\,2}}{2} - (V_G)k_BT\ln[1+\exp(V_G/k_BT)] >> \frac{(\pi k_BT)^2}{12} - (k_BT)^2\, Poly\log(2,-\exp(V_G/k_BT))$$

Therefore, the closed form solution of Eq. (4.11) can be expressed as follows:

$$N = \frac{2}{\pi(\hbar v_F)^2} T_{WKB}(E)\left(\frac{V_G^{\,2}}{12} - (V_G)k_BT\ln[1+\exp(V_G/k_BT)]\right) \tag{4.12}$$

Equation (4.12) expresses the doping density which is the net amount of carriers tunneling from top to bottom graphene layers due to applied voltage, V_G as shown in Fig. 4.3(a). Following the work of Georgiou et al. [4], a positive bias generates electron tunneling whereas the negative bias generates hole tunneling. The electron tunneling is shown in blue curve and hole tunneling is shown in red curve in Fig. 4.3(a) for positive and negative biases, respectively. The induced doping density through interlayer tunneling (N) calculated using Eq. (4.12), has a square root dependence on Fermi level of the bottom graphene layer which is expressed as follows [4]:



c)

Step 1:
V_G Applied Between Top and Bottom Graphene Layer

Step 2:
Induced Charge Density Estimation:

$$N=\frac{2}{\pi(\hbar v_F)^2}\int T_T(E)\left(\frac{V_G^2}{12}-(V_G)kT(\ln[1+\exp(V_G/kT)])\right)$$

Step 3:
Change in Channel Fermi Level Estimation:

$$\Delta E_F=\pm\hbar v_F\sqrt{(\pi|N|)}$$

Step 4:
Drain Current Estimation:

$$I=\frac{2q^2V_T}{\hbar}\left[W\frac{2\Delta E_F}{\pi(\hbar v_F)}(-\ln(1+\exp(\Delta E_F/V_T))+\ln(1+\exp((\Delta E_F-V_{DS})/V_T))+\ln 2-\ln(1+\exp(-V_{DS}/V_T))\right.$$

Figure 4.3: (a) Carrier concentration (N) versus V_G, (b) change of Fermi level (ΔE_F) with N and (c) flow chart showing operation of graphene JTET.

$$\Delta E_F = \pm \hbar \upsilon_F \sqrt{\pi \mid N \mid} \tag{4.13}$$

The sign of the Fermi level shift (positive or negative) is determined from the polarity of the gate voltage [19]. A positive bias shifts the Fermi level upward which is shown in Fig. 4.2(b). Figure 4.3(b) shows change in the amount of shift in Fermi level (ΔE_F) due to induced carrier concentration (N) at the bottom graphene layer. The red and blue lines in Fig. 4.3(b) represent the change of Fermi level based on the polarity of V_G.

4.3.3 Estimation of Drain Current

Based on 'mode' (M) based modeling approach of nanoscale transistor, drain current in graphene JTET can be calculated considering channel conductivity and transmission coefficients. Considering the change of Fermi level at the bottom graphene layer due to vertical tunneling of carriers between top and bottom graphene layers due to V_G and the source-drain lateral transport due to V_{DS}, drain current in graphene JTET can be expressed using Landauer's expression as follows [22]:

$$I = \int dE[(G(E)(f_S(E) - f_D(E)))] \tag{4.14}$$

Here, $G(E)$ is channel conductance. $f_S(E)$ and $f_D(E)$ are source and drain Fermi functions, respectively, which can be expressed similar to Eqs. (4.7) and (4.8). Based on Landauer expression, conductance ($G(E)$) can be expressed as follows [22]:

$$G(E) = (2q^2 / \hbar) M(E) T_B(E) \tag{4.15}$$

Here $T_B(E)$ is transmission coefficient in ballistic transport and $M(E)$ is number of modes in graphene. Number of modes (M) in graphene is expressed as follows [23]:

$$M(E) = 2W \mid E_{TM} \mid / \pi(\hbar \upsilon_F) \tag{4.16}$$

In Eq. (4.16), W is the width of channel and $|E_{TM}|$ is the energy range for calculating transverse mode. In this work, E_{TM} is considered as the amount of shift in Fermi level in the channel (ΔE_F) which controls the number of modes in the channel between source and drain. The number of conducting channels at energy E_{TM} is proportional to the width of the conductor in two dimensional and to the cross-sectional area in three-dimensional geometry. Total number of modes are also affected by the band structure of the channel material [23]. Expression of *M(E)* in Eq. (4.16) is specific to the graphene which differs from the expression of mode usually used for a parabolic band structure. v_F is the Fermi velocity. Combining from Eq (4.14) to Eq. (4.16), drain current can be written as follows:

$$I = \frac{2q^2}{\hbar}\int dE[(M(E)T_B(E)(f_S(E) - f_D(E)))] \tag{4.17}$$

Considering a scattering free source-drain ballistic transport in the channel, we have assumed the transmission coefficient, $T_B(E)$ as 1 in Eq. (4.17). Now, combining the energy window for ballistic transport from 0 to qV_{DS} and the change in channel barrier height from 0 to ΔE_F, Eq. (4.17) can be written as follows:

$$I = \frac{2q^2}{\hbar}[\int_0^{\Delta E_F} W\frac{2|E_{TM}|}{\pi(\hbar v_F)}(\frac{1}{1+e^{\left(E_{TM}-E_F{}^S\right)/kT}} - \frac{1}{1+e^{\left(E_{TM}-E_F{}^D\right)/kT}})dE] \tag{4.18}$$

The closed form analytical solution of Eq. (4.18) is as follows:

$$I = \frac{2q^2V_T}{\hbar}\left[W\frac{2\Delta E_F}{\pi(\hbar v_F)}(-\ln(1+\exp(\Delta E_F/V_T)) + \ln(1+\exp((\Delta E_F - V_{DS})/V_T)) + \ln(2) - \ln(1+\exp(-V_{DS}/V_T)))\right] \tag{4.19}$$

In Eq. (4.19), k_BT is replaced by the thermal voltage qV_T, value of which is defined as 0.0259 eV at 300 K. We consider this as the equation of drain current in graphene JTET which is applicable for both the electronic conduction (n- type behavior) and hole conduction (p- type behavior), provided appropriate bias is considered. Figure 4.3(c) provides the flow chart of the operation of graphene JTET with necessary current transport equations. Mobility is an important

parameter in graphene JTET. Considering Drude model for conductivity ($\sigma = \mu_n Nq$, where σ is conductivity, μ_n is carrier mobility and q is charge on electron) and graphene minimum conductivity ($\sigma = 4q^2/h$ where h is Planck's constant), we have calculated the mobility of the graphene JTET as 5468 cm^2/V-s. The doping density through tunneling (N) of $1.76x10^{11}/cm^2$ at 0.1 V gate bias is considered for the mobility extraction. Graphene band structure is symmetric around the Dirac point for which nearly identical value applies for both electron and hole mobility [20].

4.4 Performance Analysis of Interlayer Tunneling Based Graphene JTET

Using Eq. (4.19), drain current is calculated which has both T_{WKB} and N dependence. The plotted transfer characteristic in Fig. 4.4(a) considers a fixed tunneling probability (T_{WKB} = 0.2378) for different V_{DS}. For V_{GS} = 0.1V and V_{DS} = 0.1V, on-current density of 88 μA/μm^2 is obtained for the effective channel area of 0.05 μm^2. With three hBN layers, graphene JTET operating at 0.1 V supply voltage turns-on at an average subthreshold slope of 25 mV/decade with $2.45x10^4$ on/off current ratio. The off-state leakage current of 3.5 nA/μm^2 gives an off-state static power of 0.35 nW/μm^2. Calculated dynamic power for graphene JTET is 4.4 μW/μm^2 for the drive current of 88 μA/μm^2 at 0.1 V supply voltage. A comparison of the transfer characteristic of graphene JTET with some of the earlier reported iTFETs is presented in Fig. 4.4(b) for 0.1 V gate bias. Figure 4.4(b) shows that the earlier reported iTFETs provide low on-current density and high subthreshold slope. Table 4.1 summarizes the comparison obtained from Fig. 4.4(b). For the focus on digital circuit, we have avoided the inclusion of similar graphene-insulator-graphene devices showing NDR effects in Table 4.1 and Fig. 4.4(b); thus limited the comparison with non-NDR devices only.

It is observed from both Fig. 4.4(b) and Table 4.1 that graphene JTET performs better

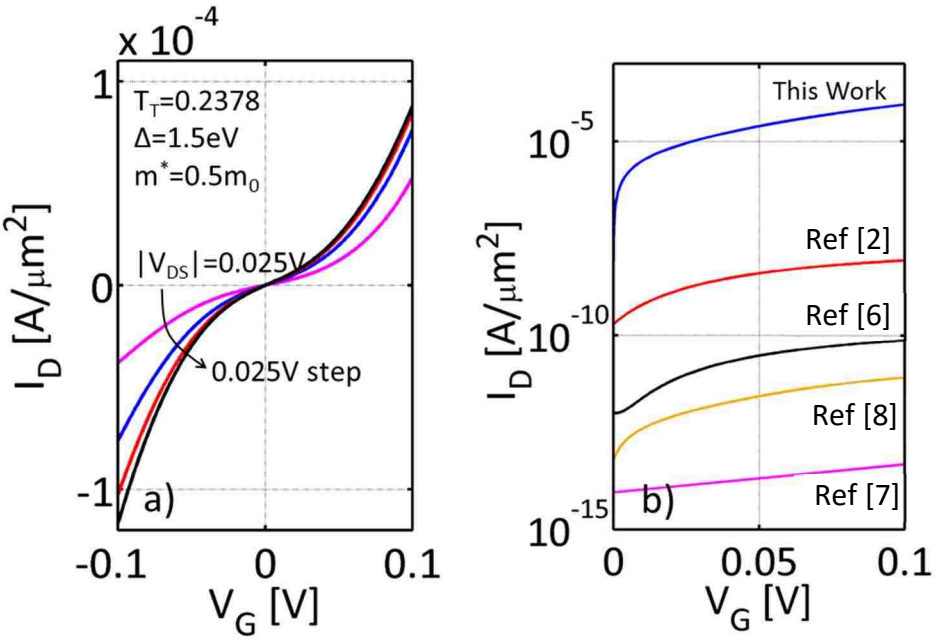


Figure 4.4: Transfer characteristics for the graphene JTET. (a) I_D - V_G curve for different V_{DS} in linear scale with 0.025 V step and (b) comparison of the transfer characteristics of graphene JTET with earlier similar type of iTFETs. Note: Fig. 4.4(a) is drawn in linear scale and Fig. 4.4(b) in log scale.

Table 4.1

Comparison of graphene JTET performance with similar iTFET

Model	$\lvert V_{DD}\rvert$ or V_{DS}**	$\lvert V_G\rvert$	Tunneling Barrier	I_{ON}/I_{OFF}	Subthreshold Slope (mV/decade)
This Work	0.1	0.1	hBN, 3 layers	$2.45\text{x}10^4$	25
Ref [2]	25	0.1	hBN, 4 layers	10 to 10^4	16
Ref [4]	2	0.1	WS_2, 4 layers	10^6	20
Ref [7]	0.5	10	hBN, 5 layers	30	300
Ref [6]	0.8	0	TiO_x/TiO_2, 5nm*	Unspecified	70

* x=0.68-0.75

** Literature considers both form of expression for drain bias

than other similar iTFETs. Few explanations are required at this stage for describing the high performance of graphene JTET. We have considered three layers of hBN equivalent to 1.02 nm in thickness as the tunneling barrier. Whereas the other listed iTFETs in Fig. 4.4(b) and Table 4.1 consider a thicker tunneling barrier. Such a small barrier thickness not only induces a higher charge density at the bottom graphene layer but also energy momentum in vertical direction remains conserved. This is consistent with having a relatively smaller coherence length of tunneling which suppresses the NDR effect [6]. ITRS requires a minimum value of on/off current ratio (I_{ON}/I_{OFF}) as 10^4 at $V_{DD} < 0.7$ V for next generation devices for digital applications [7]. From Table 4.1, graphene JTET provides the I_{ON}/I_{OFF} of 2.45×10^4 at $V_{DD} = 0.1$ V which meets the ITRS requirement. Although graphene JTET provides low I_{ON}/I_{OFF} compared to some other iTFET, it is still suitable for digital circuit design. It is to be mentioned that Georgiou et al. [4] obtained a current ratio of 10^6 at $V_{DD} = 2$ V ($> V_{DD}$ of graphene JTET) range for graphene-WS_2-graphene iTFET, however, subthreshold slope is larger than that obtained for graphene JTET at 0.1 V supply voltage. Moreover, WS_2 is a wide bandgap semiconductor compare to hBN which is a wide bandgap insulator. The electronic properties of graphene-WS_2 super lattice is different from the graphene-hBN super lattice for which I_{ON}/I_{OFF} of graphene JTET differs from the I_{ON}/I_{OFF} in [4]. Using the method of average subthreshold slope, SS can be determined as follows [24, 25]:

$$SS = \frac{dV_{GS}}{d(\log_{10} I_D)} \tag{4.20}$$

where I_D is the drain current and V_G is the gate bias. For a decade change in drain current in the subthreshold region, required gate bias is calculated which gives the subthreshold slope. Figure 4.5 shows the extraction of subthreshold slope. It is to be mentioned that Fig. 4.5 is plotted in log scale compared to linear scale in Fig. 4.4(a). The values of SS mentioned in Table 4.1 is also

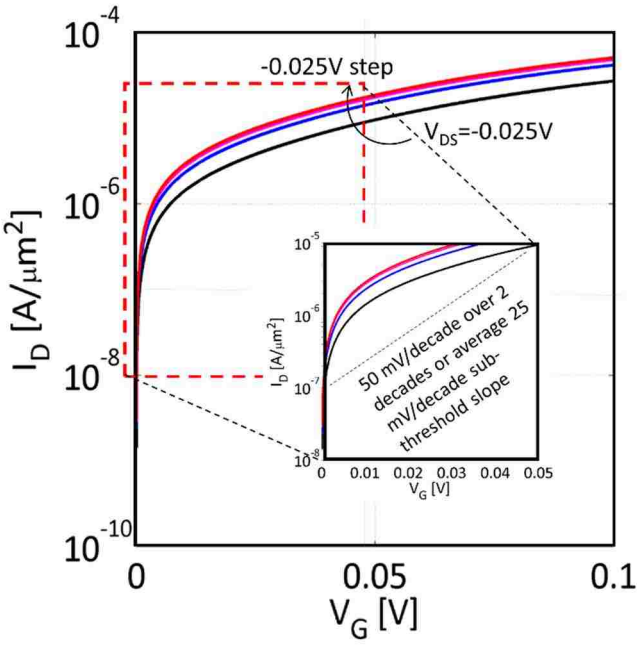


Figure 4.5: Subthreshold slope extraction from I_D - V_G curve of graphene JTET. Inset shows change in V_G for estimating average subthreshold slope over three decades of drain current [25]. Note: Drain current is plotted in log scale compared to linear scale as in Fig. 4.4(a).

calculated using Fig. 4.5 following the method described in the work of Appenzeller et al. [25].

For energy efficient switching technology, it is necessary that a transistor provides subthreshold slope (SS) less than the conventional thermionic limit of 60 mV/decade. Since most iTFETs provide either NDR behavior or linear resistive characteristic, SS of such devices is not always discussed explicitly. The iTFET proposed by Roy et al. [6] obtained a SS of 70 mV/decade for the TiO_x/TiO_2 stack for a tunneling barrier (x = 0.68 - 0.75) which is also found to be limited by the gate capacitance. Using first principles density functional theory combined with non-equilibrium Green function (NEGF), Fiori et al. [7] studied a very large on-current modulation in graphene-hBN-graphene vertical heterobilayer. For a drain-source voltage of 0.5 V, a corresponding SS ~ 300 mV/decade has been obtained. Such performance is observed due to the poor electrostatic control of channel potential by the gate voltage. Ghobadi and Pourfath [8] obtained > 1000 mV/decade SS for similar iTFETs with three hBN layers. The fundamental physical limitation of such iTFETs in terms of subthreshold slope, which will be derived in Chapter 6, is also consistent with the high subthreshold slope obtained for similar iTFETs discussed in this chapter. Compared to iTFETs, graphene JTET adopts a mixed-mode mechanism of vertical interlayer tunneling of carriers between two graphene layers and lateral ballistic transport between source and drain for which gate capacitance has little or no effect. Moreover, the shift in Fermi level controlling source-drain ballistic transport provides superior channel electrostatic control. For these reasons, a very steep subthreshold has been obtained for graphene JTET compared to previously reported iTFETs. Table 4.2 enlists performance comparison of graphene JTET with ITRS projected 2020 nMOSFETs. Compared to the on-state drain current of 1942 μA/μm at V_{DD} = 0.68 V for 2020 nMOSFET, graphene JTET on-state drain current is calculated as 880 μA/μm at V_{DD} = 0.1 V. Calculated off-state leakage current is 3.5 nA/μm

compared to 100 nA/μm of 2020 nMOSFET. Therefore, graphene JTET provides 194 times less off-state leakage power and dissipates ~15 times less dynamic power than the 2020 nMOSFET. Note that the current values mentioned in Table 4.2 for graphene JTET has been normalized with the channel length which provides the drain current unit in μA/μm. Transfer characteristics of graphene JTET is highly dependent on the thickness of the tunneling barrier. Therefore, it is necessary to study the performance of graphene JTET at different tunneling barrier thicknesses. Since graphene JTET is designed as a vertical heterostructure, its tunneling barrier thickness is determined by the number of hBN layers used between top and bottom graphene layers. Figure 4.6(a) shows transfer characteristics of graphene JTET for different number of hBN layers. From Eq. (4.1) we found that the tunneling probability is exponentially dependent on the thickness of the barrier. Therefore, on-current density of 96.03 μA/μm^2 is observed for the monolayer hBN (0.34 nm thick) as the tunneling barrier, value of which decreases to 0.282 μA/μm^2 for six layers of hBN used. The ratio between the on-current to the off-current (I_{ON}/I_{OFF}) also changes with the total number of the hBN layers along with subthreshold slopes of graphene JTET. Figure 4.6(b) shows I_{ON}/I_{OFF} and SS for different number of hBN layers. As the tunneling barrier thickness increases with the number of hBN layers, I_{ON}/I_{OFF} decreases. The subthreshold slope of graphene JTET increases with the increase in number of hBN layers due to reduced tunneling probability. For the monolayer hBN, only 0.9 mV/decade of SS over single decade is estimated which increases to 20.31 mV/decade for six hBN layers. With smaller barrier thickness, precise gate control over the channel is obtained. Moreover, the wave function of the top graphene layer easily extends toward the bottom graphene layer [16]. This provides not only high on-current density but also a reduced off-state leakage current along with the steep subthreshold slope. Therefore, a high I_{ON}/I_{OFF} and low SS are observed for less number of hBN layers.

Table 4.2

Comparison of graphene JTET performance with 2020 n-MOSFET projected in 2012 edition of ITRS

Parameter	2020 nMOSFET	Graphene JTET	Unit
Supply voltage, V_{DD}	0.68	0.1	V
Drive current, I_D	1942	880	µA/µm
Off-state leakage current, I_{OFF}	100	3.5	nA/µm
Off- lekage power, ~ $I_{OFF}V_{DD}$	68	0.35	µW/µm
Dynamic power, ~1/2 I_DV_{DD}	660.28	44	µW/µm

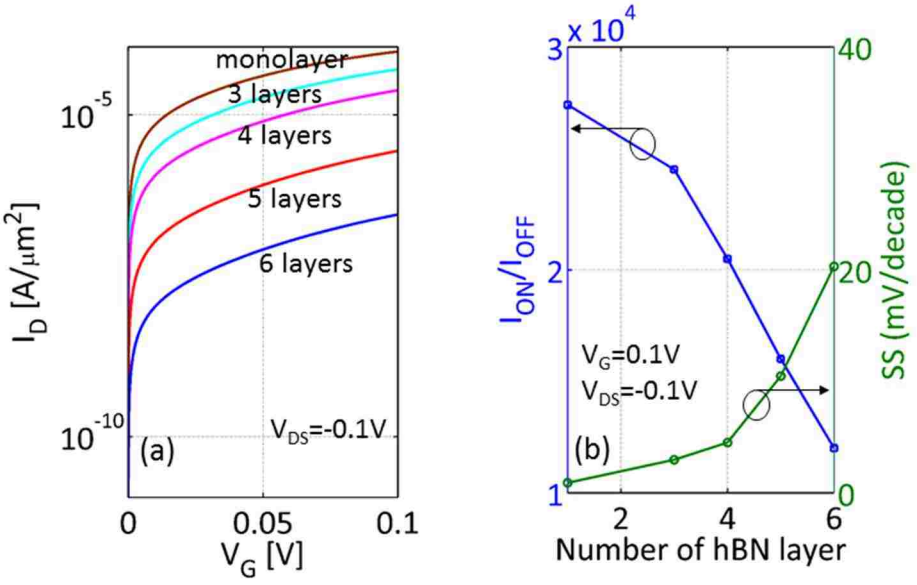


Figure 4.6: (a) Change in transfer characteristics of graphene JTET for multiple hBN layers as tunneling barrier and (b) change in on/off current ratio (I_{ON}/I_{OFF}) and subthreshold slope (SS) with the number of hBN layers.

I_D-V_{DS} characteristics in conventional iTFET suffers large NDR effect. Therefore, their scope in digital circuit design becomes limited. However, the proposed graphene JTET overcomes such limitations and provides NDR free output characteristics with separate n- and p-type behavior. Figures 4.7(a) and (b) depict the output characteristics (I_D -V_{DS}) of graphene JTET for p-type and n-type graphene JTET for different V_G, respectively. Compared to conventional MOSFETs, n-type electronic transport is obtained for $V_{DS} > 0$ and $V_G < 0$ whereas p- type hole transport is obtained for $V_{DS} < 0$ and $V_G > 0$. Since a positive gate bias induces a negative shift in Fermi level and a negative gate bias induces a positive shift in Fermi level [26], the sign of notation used in Fig. 4.7 is consistent with the overall current transport. Figure 4.7 considers equal tunneling probability (T_{WKB}) in both the p- and n- type transistors. With independently applied bias at the top and bottom graphene layers, a strong coulomb drag is generated due to interlayer electron- hole interaction [27]. By applying a positive bias at the gate ($V_G > 0$), electron like Fermi surface is formed at the top graphene layer. Further when a negative bias at drain ($V_{DS} < 0$) is applied, hole like Fermi surface is formed at the bottom graphene layer. Both of these opposite types of Fermi surfaces are necessary for: 1) scattering free elastic tunneling normal to the barrier and 2) positive Coulomb drag for interlayer electron- hole interaction. Similarly, a negative Coulomb drag with elastic scattering free tunneling is observed when $V_G < 0$ is applied at the top graphene layer and $V_{DS} > 0$ at the bottom graphene layer. Thus, the need of such opposite polarity of biasing for obtaining the output characteristic is understood. Figures 4.8(a) and (b) show the plot of output characteristics of p-type and n-type graphene JTET at high V_{DS}, respectively. Note that at higher V_{DS}, drain current saturation is observed. For all three conditions of $V_{DS} < V_G$, $V_{DS} = V_G$ and $V_{DS} > V_G$, graphene JTET provides drain current saturation.

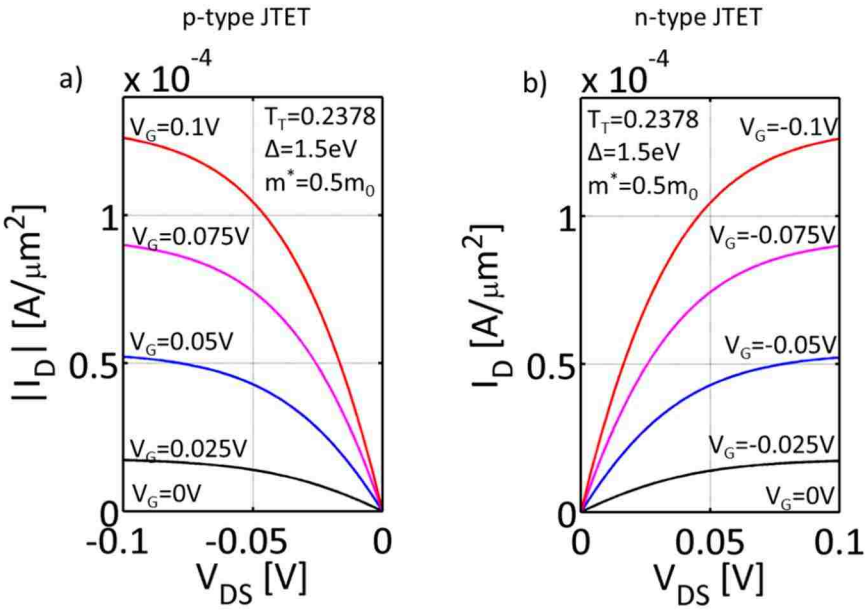


Figure 4.7: Output characteristics for graphene JTET. a) p-type behavior obtained for $V_G > 0$, $V_{DS} < 0$ and b) n-type behavior obtained for $V_G < 0$, $V_{DS} > 0$.

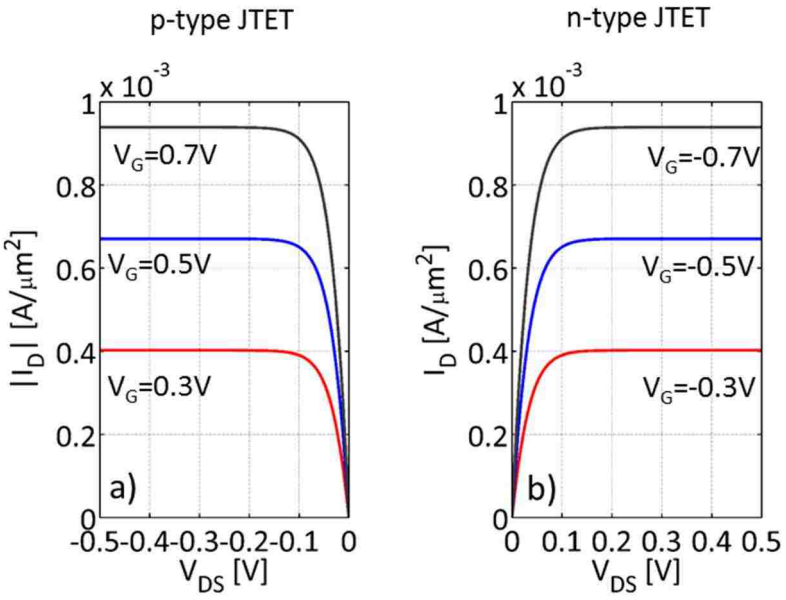


Figure 4.8: Output characteristics of graphene JTET with increasing V_{DS} for varying V_G. (a) p - type graphene JTET and (b) n - type graphene JTET.

This implies that the magnitude of the Coulomb drag originating at higher drain and gate bias provides not only a precise interlayer tunneling but also preserves superior gate control over the channel. For this reason, smooth output characteristics are obtained.

4.5 Voltage Transfer Characteristics of Graphene JTET Inverter

The inverter is the basic building block of a digital integrated circuit and its performance reflects the type of transistors used as switches. Complementary inverter using vertical heterostructure transistors as switches can be used similar to a CMOS inverter. Figures 4.9(a) shows the schematic of a graphene JTET logic inverter with the logic operation from 1 to 0 and 0 to 1 in Fig. 4.9(b) and 4.9(c), respectively. Since graphene JTET has similarity with a ballistic nanoscale MOSFET with respect to source-drain ballistic transport, such symbols are partially designed based on the conventional depletion type MOSFET symbols. However, since the channel barrier control is carried out through the vertical interlayer tunneling, we have adopted conventional sign of tunneling between top and bottom gate electrodes. Therefore, the symbols drawn in Figs. 4.9 combine both the concept of vertical interlayer tunneling between gates at the top and bottom graphene layers and source-drain ballistic transport.

The gate bias (V_G) is defined as the difference between the top and bottom gate bias of the transistor. The bottom gate of bottom graphene JTET is connected with the top gate of top graphene JTET for which it is termed as common gate contact. Compared to opposite type of MOSFETs needed in CMOS operation, only single type of graphene JTET (n-type in this case) can perform the inverter operation. An input voltage (V_{IN}) applied at the common gate contact will generate two opposite type of shifts in Fermi levels in each of these transistors independently. Source of the top graphene JTET is connected to the source of bottom graphene JTET. Drain of top graphene JTET is connected to the supply voltage (V_{DD}) and drain of the

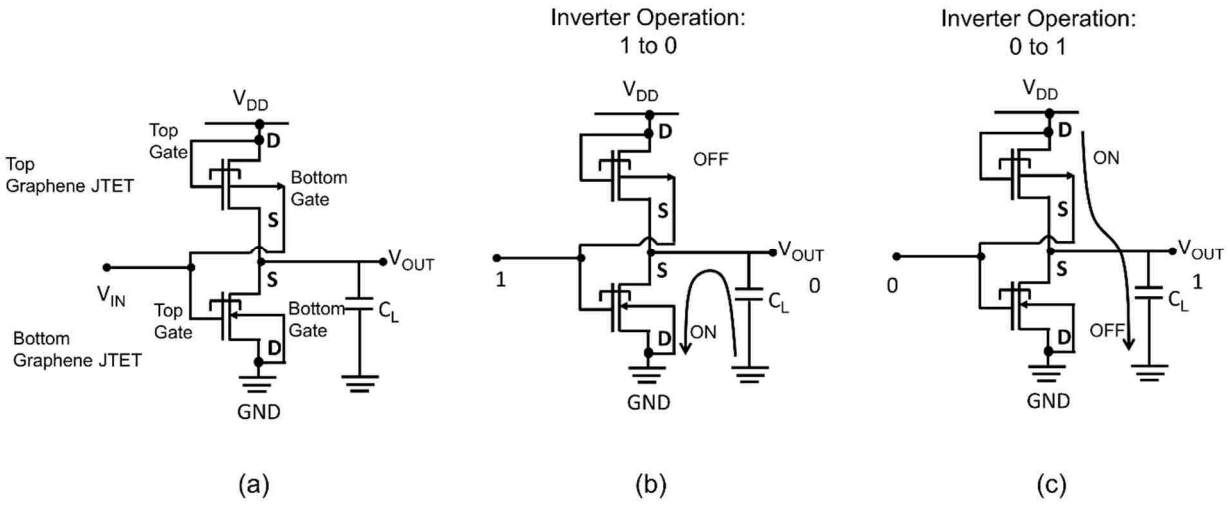


Figure 4.9: (a) Schematic of complementary graphene JTET based vertical logic inverter, (b) inverter operation for logic input 1 and (c) inverter operation for logic input 0.

bottom graphene JTET is grounded (0 V). Being vertically connected, a single gate contact is necessary for graphene JTET vertical inverter. In this way, no additional interconnect is required to connect the two gates of the two complementary transistors.

In the inverter operation shown in Fig. 4.9(b), a logic high '1' at the inverter input (V_{IN}) turns 'on' the bottom JTET since the bottom gate of this JTET is at ground potential resulting a positive V_G, whereas turns off the top JTET since the top gate of this JTET is connected to V_{DD}, resulting in 0V gate bias (V_G). Hence, the output load capacitor gets discharged through this bottom JTET and the output logic becomes '0.' Similarly a logic low '0' at the inverter input (V_{IN}) turns 'on' the top JTET since the top gate of this JTET is at V_{DD} resulting a positive V_G, whereas turns 'off' the bottom JTET since the bottom gate of this JTET is connected to ground, resulting in 0V gate bias (V_G). Hence, the output load capacitor gets charged through top JTET and the output logic becomes '1.'

Figure 4.10(a) shows voltage transfer characteristics (VTC) of the complementary graphene JTET inverter operating at different supply voltages. The inverter gain (A_V) of 4.35 is obtained for V_{DD} = 0.5 V whereas the gain in 3.15 for V_{DD} = 0.1 V. This reflects the capability of graphene JTET inverter to operate at reduced supply voltage with higher gain.

Compared to a conventional CMOS inverter where gain plummets as supply voltage goes below 0.5 V, graphene JTET vertical inverter can retain its gain at low supply voltages. It is also noted from the transfer characteristics that sharp transition between off to on state is obtained at all supple voltages. Figure 4.10(b) shows the extraction of noise margin for V_{DD} = 0.1 V for the graphene JTET inverter. We have calculated the low noise margin, N_{ML} as 0.021 V and high noise margin, N_{MH} as 0.022 V. Both of these values are more than 20% of the original signal which substantiates strong noise immunity.

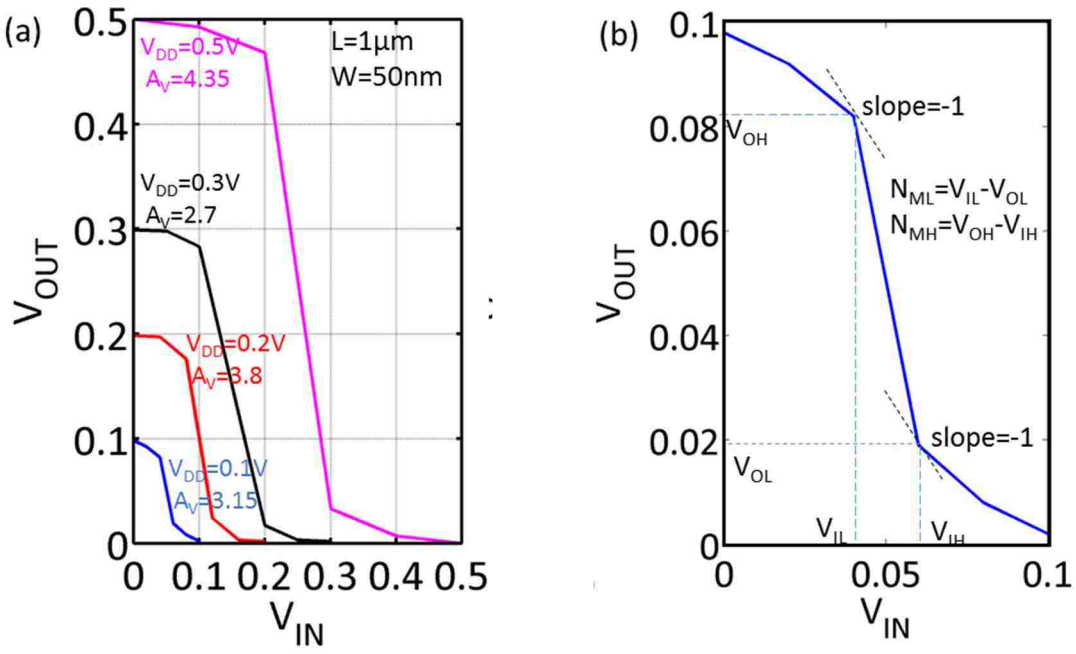


Figure 4.10: (a) Voltage transfer characteristics of a complementary graphene JTET vertical inverter for different supply voltages with corresponding inverter gain and (b) noise margin for the supply voltage of 0.1 V.

4.6 Conclusion

A new type of graphene switching transistor termed as 'junctionless tunnel effect transistor (JTET)' based on graphene-hBN-graphene vertical heterostructure is proposed and an analytical current transport model has been developed. The drain current in graphene JTET flows between source and drain of bottom graphene layer. The current in the channel is regulated by the shift in channel Fermi level which depends on the net vertical tunneling of carriers from top graphene to bottom graphene layers through hBN. Performance of graphene JTET is evaluated for different numbers of hBN layers. A comparison between graphene JTET and ITRS projected 2020 nMOSFET is also provided apart from graphene JTET performance comparison with similar iTFETs. Current saturation is observed in graphene JTET output characteristic for both p- and n- type operations, which makes graphene JTET suitable for digital circuit design. Graphene JTET is also capable of suppressing negative difference resistance (NDR) effect, shows steep subthreshold slope with high on/off current ratio and normal operation at the room temperature. A complementary vertical inverter is presented similar to a CMOS inverter and analyzed for its performance. Graphene JTET vertical inverter gives inverter gain higher than unity at the low supply voltage and both low and high noise margins. It is concluded that with an average 25 mV/decade subthreshold slope at 0.1 V supply voltage and a current ratio of ~10^4, graphene JTET meets ITRS requirement of device scaling for energy efficient circuit design.

4.7 References

[1] *International Technology Roadmap for Semiconductor*. Available: www.itrs.net, 2013.

[2] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, A. K. Geim, K. S. Novoselov, and L. A. Ponomarenko, "Field-effect tunneling transistor based on vertical graphene heterostructures," *Science,* vol. 335, pp. 947-950, 2012.

[3] A. K. Geim and I. V. Grigorieva, "Van der Waals heterostructures," *Nature,* vol. 499, pp. 419-425, 2013.

[4] T. Georgiou, R. Jalil, B. D. Belle, L. Britnell, R. V. Gorbachev, S. V. Morozov, Y.-J. Kim, A. Gholinia, S. J. Haigh, O. Makarovsky, L. Eaves, L. A. Ponomarenko, A. K. Geim, K. S. Novoselov, and A. Mishchenko, "Vertical field-effect transistor based on graphene-WS_2 heterostructures for flexible and transparent electronics," *Nat Nano,* vol. 8, pp. 100-103, 2013.

[5] P. Zhao, R. M. Feenstra, G. Gong, and D. Jena, "SymFET: a proposed symmetric graphene tunneling field-effect transistor," *IEEE Trans. Elect. Dev.,* vol. 60, pp. 951-957, 2013.

[6] T. Roy, Z. R. Hesabi, C. A. Joiner, A. Fujimoto, and E. M. Vogel, "Barrier engineering for double layer CVD graphene tunnel FETs," *Microelectronic Engineering,* vol. 109, pp. 117-119, 2013.

[7] G. Fiori, S. Bruzzone, and G. Iannaccone, "Very large current modulation in vertical heterostructure graphene/hBN transistors," *IEEE Trans. Elect. Dev.,* vol. 60, pp. 268-273, 2013.

[8] N. Ghobadi and M. Pourfath, "A comparative study of tunneling FETs based on graphene and GNR heterostructures," *IEEE Trans. Elect. Dev.,* vol. 61, pp. 186-192, 2014.

[9] A. Mishchenko, J. S. Tu, Y. Cao, R. V. Gorbachev, J. R. Wallbank, M. T. Greenaway, V. E. Morozov, S. V. Morozov, M. J. Zhu, S. L. Wong, F. Withers, C. R. Woods, Y. J. Kim, K. Watanabe, T. Taniguchi, E. E. Vdovin, O. Makarovsky, T. M. Fromhold, V. I. Fal'ko, A. K. Geim, L. Eaves, and K. S. Novoselov, "Twist-controlled resonant tunnelling in graphene/boron nitride/graphene heterostructures," *Nat Nano,* vol. 9, pp. 808-813, 2014.

[10] B. Fallahazad, K. Lee, S. Kang, J. Xue, S. Larentis, C. Corbet, K. Kim, H. C. P. Movva, T. Taniguchi, K. Watanabe, L. F. Register, S. K. Banerjee, and E. Tutuc, "Gate-tunable resonant tunneling in double bilayer graphene heterostructures," *Nano Letters,* vol. 15, pp. 428-433, 2015.

[11] S. Kang, B. Fallahazad, L. Kayoung, H. Movva, K. Kyounghwan, C. M. Corbet, T. Taniguchi, K. Watanabe, L. Colombo, L. F. Register, E. Tutuc, and S. K. Banerjee, "Bilayer graphene-hexagonal boron nitride heterostructure negative differential resistance interlayer tunnel FET," *IEEE Elect. Dev. Lett.,* vol. 36, pp. 405-407, 2015.

[12] G. Giovannetti, P. A. Khomyakov, G. Brocks, V. M. Karpan, J. van den Brink, and P. J. Kelly, "Doping graphene with metal contacts," *Phys. Rev. Lett.,* vol. 101, pp. 026803, 2008.

[13] C. R. Dean, A. F. Young, I. Meric, C. LeeC, L. Wang, S. Sorgenfrei, K. Watanabe, T. Taniguchi, P. KimP, K. L. Shepard, and J. Hone, "Boron nitride substrates for high-quality graphene electronics," *Nat Nano,* vol. 5, pp. 722-726, 2010.

[14] G. Giovannetti, P. A. Khomyakov, G. Brocks, P. J. Kelly, and J. van den Brink, "Substrate-induced band gap in graphene on hexagonal boron nitride: Ab initio density functional calculations," *Phys. Rev. B,* vol. 76, pp. 073103, 2007.

[15] Y. W. Son, M. L. Cohen, and S. G. Louie, "Energy gaps in graphene nanoribbons," *Phys. Rev. Lett.,* vol. 97, pp. 216803, 2006.

[16] A. Sciambi, M. Pelliccione, M. P. Lilly, S. R. Bank, A. C. Gossard, L. N. Pfeiffer, K. W. West, and D. Goldhaber-Gordon, "Vertical field-effect transistor based on wave-function extension," *Phys. Rev. B,* vol. 84, pp. 085301, 2011.

[17] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, M. I. Katsnelson, L. Eaves, S. V. Morozov, A. S. Mayorov, N. M. R. Peres, A. H. Castro Neto, J. Leist, A. K. Geim, L. A. Ponomarenko, and K. S. Novoselov, "Electron tunneling through ultrathin boron nitride crystalline barriers," *Nano Letters,* vol. 12, pp. 1707-1710, 2012.

[18] N. Kharche and S. K. Nayak, "Quasiparticle band gap engineering of graphene and graphone on hexagonal boron nitride substrate," *Nano Letters,* vol. 11, pp. 5274-5278, 2011.

[19] M. I. Katsnelson, K. S. Novoselov, and A. K. Geim, "Chiral tunnelling and the Klein paradox in graphene," *Nat Phys,* vol. 2, pp. 620-625, 2006.

[20] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Rev. of Modern Phys.,* vol. 81, pp. 109-162, 2009.

[21] J. G. Simmons, "Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film," *J of App. Phys.,* vol. 34, pp. 1793-1803, 1963.

[22] S. Datta, *Quantum Transport: Atom to Transistor*: Cambridge University Press, 2005.

[23] M. Lundstrom and C. Jeong, *Lessons from Nanoscience: A Lecture Note Series Near-Equilibrium Transport*: World Scientific, 2012.

[24] M. Fahad and A. Srivastava, "Subthreshold slope of vertical graphene interlayer tunnel transistor," *Nano,* vol. 6, pp. 1750069, 2017.

[25] J. Appenzeller, Y. M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Physical Review Letters,* vol. 93, pp. 196805, 2004.

[26] D. Newns, B. Elmegreen, X. Hu Liu, and G. Martyna, "A low-voltage high-speed electronic switch based on piezoelectric transduction," *J of App. Phys.,* vol. 111, p. 084509, 2012.

[27] S. Kim, I. Jo, J. Nah, Z. Yao, S. K. Banerjee, and E. Tutuc, "Coulomb drag of massless fermions in graphene," *Phys. Rev. B,* vol. 83, pp. 161401, 2011.

CHAPTER 5*

MOLYBDENUM DISULFIDE / BORON NITRDE JUNCTIONLESS TUNNEL EFFECT TRANSISTOR

5.1 Introduction

Scaling of planar metal oxide semiconductor field effect transistor (MOSFET) is predicted to face its formal end as the Moore's continues down to the technology node of 7nm and below [1]. In addition to shrinking MOSFET channel length to sub-10nm for high transistor density, vertical integration of MOSFETs based on stacking of two dimensional layered materials have recently been explored [2-16]. Novel two dimensional material systems such as graphene and non-graphene have largely made this feasible [17]. These transistors hold the promise for vertical integration, providing an alternative approach for maintaining the lifeline of Moore's law and beyond. Compared to conventional inversion mode of operation, field effect tunneling based current transport has been studied in these vertical FETs. Majority of these vertical FETs consider two graphene layers separated by a thin tunnel barrier, mostly hex boron nitride (*h*BN).

Considering Bose condensation of Fermions (electron-hole pairs) between two graphene layers, BiSFET proposed by Banerjee *et al.* [5] was one of the theoretical graphene based interlayer FETs. The theoretical model of an interlayer tunneling transistor, SymFET, proposed by Zhao *et al.* [7] was another graphene/*h*BN heterostructure. With an on/off current ratio of

---

*Part of this work is reported in the following publications:

1. A. Srivastava and M. Fahad, "Vertical Interlayer Tunnel Field Effect Transistor Using Hexagonal Boron Nitride," LSU Application No. LSU-2016-049, filed provisional patent, Dec 2016.
2. A. Srivastava and M. Fahad, "Vertical MoS_2/hBN/MoS_2 interlayer tunneling field effect transistor," *Solid State Elect.*, vol. 126, pp. 96-103, 2016.

~100, SymFET provides a large resonant current peak. However, the model in [7] does not provide any insight of SymFET subthreshold slope. Operating frequency of SymFET was also not reported in [7]. Recently, Fiori *et al.* [9] have studied very large current modulation in graphene/*h*BN vertical heterostructure from the multi-scale simulation approach. A large subthreshold slope of 385 mV/decade with an on/off current ratio of ~15 is reported. The intrinsic cut-off frequency also falls below 1 GHz.

Ghobadi and Pourfath [10] studied a vertical heterostructure similar to [9] considering both graphene and quantum confined graphene nanoribbon (GNR) separated by *h*BN with a focus on high frequency operation. However, low on/off current ratio (~3 - 10) and high subthreshold slope (> 1000 mV/decade) were obtained for ~100 GHz cut-off frequency. Compared to graphene, atomically thin molybdenum disulfide (MoS_2) based planer FET has already shown promise [18-21]. However, unlike graphene, study of vertical FET based on interlayer tunneling between two MoS_2 layers separated by a thin tunnel barrier has remained largely unexplored. Moreover, the current transport mechanism proposed for graphene JTET requires additional understanding for the case of JTET with large band gap material. Graphene is a zero band semiconductor. Therefore, performance of JTET other than graphene as top and bottom electrode separated by tunneling barrier structure needs further description.

In this Chapter, the operating principle of JTET discussed in Chapter 4 has been extended for the study of MoS_2 JTET considering MoS_2/*h*BN/MoS_2 for reduced subthreshold slope operation and sustainable leakage. The interlayer tunneling based barrier control mechanism as proposed for graphene JTET in Chapter 4 and [16] is used for the current transport study of MoS_2 JTET through self-consistent simulation method. Similar to graphene JTET, multilayer

*h*BN is considered as the gate dielectric for MoS_2 JTET. The performances of MoS2 JTET are compared with the earlier reported graphene based iTFET reported in [9] and [10].

5.2 Device Structure and Operation

Figure 5.1 shows schematic of MoS_2 JTET where the channel is a monolayer MoS_2 of 10 nm length and 5 nm width. Compared to the graphene JTET device structure discussed in Chapter 4, MoS_2 JTET considers as single layer MoS_2 as both top and bottom electrodes. Following the work in [3] and [16], gate dielectric comprises of 20 layers of *h*BN (~7 nm). Monolayer *h*BN is considered as the vertical tunneling barrier between two MoS_2 layers. Compared to conventional interlayer tunneling field effect transistor (iTFET), MoS_2 JTET considers source and drain ohmic contacts on bottom MoS_2 layer.

Recently, it has been experimentally observed that chemical vapor deposition based direct growth of monolayer MoS_2 on *h*BN provides smaller lattice strain, low doping level and clean and sharp interface [22]. Moreover, monolayer MoS_2 is stable over monolayer hexagonal BN (*h*BN) substrate for an inter-planer distance of 4.89 A^0 [23]. Based on density functional theory (DFT), an energy bandgap of 1.83 eV is observed between the MoS_2 and *h*BN [23]. This is little more than the energy bandgap (1.5 eV) between graphene and *h*BN valence bands. A hybridization between d_{x-y} orbital of MoS_2 and the p_z orbital of *h*BN originates such band gap [23]. Recently, it is demonstrated that monolayer MoS_2 retains high carrier mobility free of surface scattering on *h*BN substrate. The substrate layer of *h*BN protects MoS_2 layer from Coulomb scattering from charge impurities in SiO_2 [24].

In a fully planar two dimensional FET based on layered semiconductors, *h*BN has also been used as the top gate dielectric layer providing superior gate control over the channel [25]. Therefore, *h*BN is considered as both top and bottom gate dielectric in MoS_2 JTET.

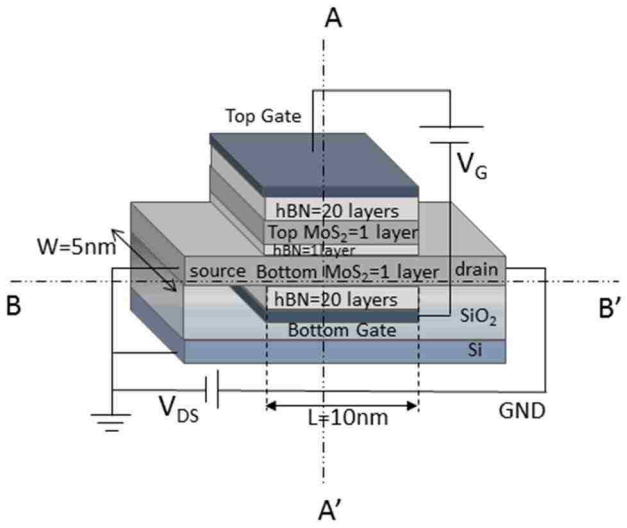


Figure 5.1. Schematic of MoS_2 JTET considering MoS_2/*h*BN/MoS_2. The dash line A-A′ refers to vertical direction of interlayer tunneling and B-B′ refers to lateral direction of source-drain ballistic transport.

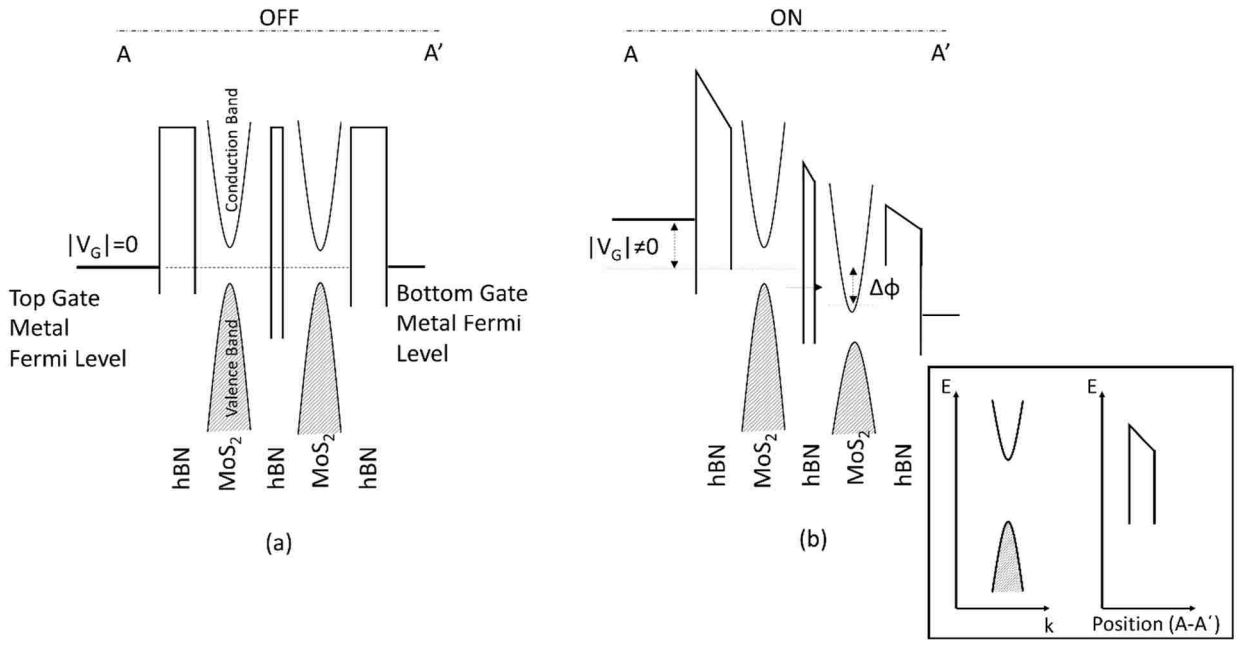


Figure 5.2: a) Energy band diagram along vertical AA′ direction in off state in MoS_2 JTET and b) in on state. $\Delta\phi$ denotes change in Fermi level at bottom (channel) Fermi level. Note: Inset box shows parabola representing E-k diagram of MoS_2 and rectangular bar represents energy barrier with position along A-A′ of hBN. All figures are schematic only and not drawn to the scale.

Experimentally it is found that single layer *h*BN is a potential candidate for interlayer tunneling extension between two semiconducting layers but also preserves the coherent length of tunneling [4].

Operation of MoS_2 JTET is twofold [16], i.e. a) gate bias (V_G) between top and bottom MoS_2 layers initiate the vertical interlayer tunneling of carriers which changes the channel Fermi level and b) the corresponding shift in channel Fermi level controls the height of the barrier between source and drain. In Fig. 5.1, dashed line A - A′ refers to the band diagram in vertical direction of interlayer tunneling and B-B′ refers to the lateral direction of source-drain ballistic transport.

Figures 5.2(a) and 5.2(b) show the MoS_2/*h*BN vertical energy band diagram for $V_G = 0$ V and $|V_G| \neq 0$ V, respectively. For $V_G = 0$ V, Fermi levels of both top and bottom MOS_2 layers are assumed to be in equilibrium as shown in Fig. 5.2(a). As bias is applied between these two layers, the tunnel barrier *h*BN screens out some electric field, however, a shift in Fermi level at the bottom (channel) MoS_2 layer is still observed. This is shown in Fig. 5.2(b).

As the gate bias is applied, a finite amount of carrier tunnels from top MoS_2 layer to bottom MoS_2 which is estimated as follows [28]:

$$N_1 = \int_0^{\Delta\phi} \rho_{MoS_2} T_{WKB}(E) f_T(E) dE \tag{5.1}$$

Similarly tunneling of carriers from bottom MoS_2 to top MoS_2 layer is estimated from,

$$N_2 = \int_0^{\Delta\phi} \rho_{MoS_2} T_{WKB}(E) f_B(E) dE \tag{5.2}$$

The net amount of tunnel carrier concentration at the bottom MoS_2 channel is described as follows:

$$N = \int_0^{\Delta\phi} \rho_{MoS_2} T_{WKB}(E)(f_T(E) - f_B(E)) dE \tag{5.3}$$

where $\rho_{MoS_2} = g_s g_v m^*_{MoS_2}/(2\pi\hbar^2)$ is density of states (DOS) in MoS_2, g_s(=2) and g_v(=2) are spin and valley degeneracy, respectively, $m^*_{MoS_2}$ is effective mass in MoS_2 ($0.57m_o$) and $\hbar$ is reduced Planck's constant [29]. $T_{WKB}(E)$ is tunneling probability between two MoS_2 layers through *h*BN barrier and $f_T(E)$ and $f_B(E)$ are Fermi functions at the top and bottom MoS_2 layers (with the generic expression of $(1/(1+\exp((E-E_F)/k_BT)))$ and k_B is Boltzmann's constant), respectively. Interlayer tunneling probability is determined as in [6],

$$T_{WKB}(E) = exp\left(-2d\sqrt{2m^*\Delta}/\hbar\right) \tag{5.4}$$

where d is the thickness of the tunnel barrier (1.3 nm in this work), m^* is carrier effective mass inside the barrier ($=0.5m_o$ inside *h*BN) [3] and Δ is height of the tunneling barrier (1.83eV between MoS_2 and *h*BN) [23]. Effective change in Fermi level of the bottom MoS_2 layer (which is also the channel MoS_2 layer) is expressed as $\Delta\phi$. Using proper limits of integration, net doping density (N) from Eq. (5.3) is integrated as follows:

$$N = \frac{2qV_T m^*_{MoS_2}}{\pi(\hbar)^2} T_{WKB}(E)\left[ln\left(1+exp\left(-\frac{\Delta\phi}{V_T}\right)\right)+ln\left(4/\left(1+exp\left(\frac{\Delta\phi}{V_T}\right)\right)\right)\right] \tag{5.5}$$

where V_T ($= k_BT/q$) is the thermal voltage. Compared to a doped MoS_2 layer, we have estimated the position of Fermi level for a biased and non-doped MoS_2 channel. The objective is to study the gate induced channel degeneracy due to an applied bias in an intrinsic MoS_2 layer. For a positive bias, an n-type degeneracy in channel Fermi level is observed whereas for a negative bias, p-type degeneracy in channel Fermi level is observed. Change in Fermi level in n-type channel is determined as follows [29]:

$$E_{Fn} = E_C + qV_T ln\left[exp\left(N/\left(\rho_{MoS_2}k_BT\right)\right)\right] \tag{5.6}$$

and in p-type, the expression is given as follows:

$$E_{Fp} = E_V - qV_T ln\left[exp\left(N / \left(\rho_{MoS_2} k_B T \right) \right) \right] \quad (5.7)$$

In both types of interlayer tunneling transistors and vertical band-to-band tunneling transistors, tunneling phenomena is dependent on temperature [6, 19]. Using Eqs. (5.4) to (5.7), Fig. 5.3(a) is plotted which shows the change in Fermi level with temperature at different interlayer gate biases. Figure 5.3(b) shows the induced carrier concentration from interlayer tunneling. It is found that Fermi level curve for an intrinsic MoS_2 channel biased at 0.74 V matches with the that of an unbiased MoS_2 channel doped at $10^{17}/cm^2$. Considering the band gap of 1.8 eV of single layer MoS_2, the conduction or valence band lies at $\pm E_G/2$. However, using interlayer tunneling technique, the Fermi level of an intrinsic MoS_2 can shift above the conduction band or below the valence band for positive or negative gate bias, respectively.

Temperature effect on carrier concentration is also studied in Fig. 5.3(b). The zero gate bias carrier concentration increases as the temperature increases and gets saturated at higher gate bias. At high temperature, more carriers gain higher energy resulting in interlayer tunneling between the two MoS_2 layers which raises the zero bias carrier concentration. Furthermore, impurity scattering and electron-hole interaction at higher gate bias cause the carrier concentration to saturate.

5.3 Estimation of Drain Current

The effective change in channel Fermi level not only depends on gate bias but also on associated voltage drops between the two gate contacts [29]. In order to model and calculate drain current of iTFET, these voltage drops are necessary to calculate as follows in this section.

The voltage drop in the channel (V_{ch}) due to interlayer tunneling based doping density (N), is determined as follows [29]:

$$V_{ch} = V_o \pm V_T ln\left[exp\left(\left(N / \left(\rho_{MoS_2} k_B T \right) \right) - 1 \right) \right] \quad (5.8)$$

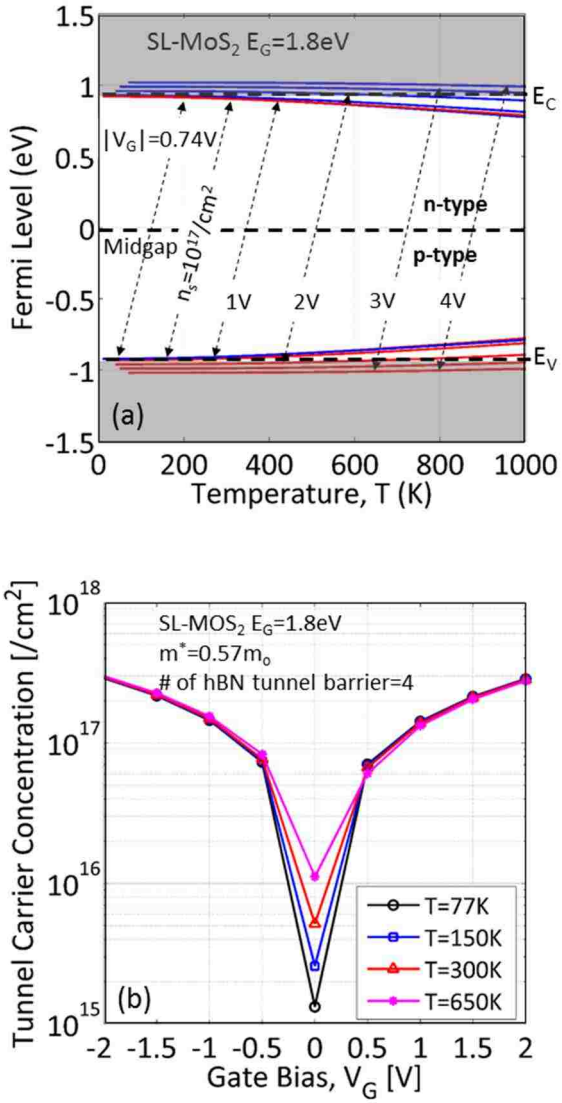


Figure 5.3: a) Change in Fermi level in n - type (above 0 eV) and p-type (below 0 eV) for a single layer (SL) MoS_2 channel with change in temperature (T) for different gate bias (V_G). The Fermi level for a doped SL-MoS_2 of n_s = 1x10^{17}/cm^2 at zero gate bias matches with non-doped SL MoS_2 JTET operating at $|V_G|$ = 0.74 V. b) Induced interlayer tunnel carrier concentration (N) with change in gate bias (V_G) for different temperatures (T).

where $V_0 = E_0/q$ and $E_0 = E_G/2$ [27]. Note, V_0 is termed as intrinsic mid-gap bias [29]. We refer the channel charge induced voltage drop along A-A′ as in [29] as follows:

$$V_V = qN / C_V \tag{5.9}$$

where C_V is net vertical capacitance between top and bottom gate electrodes. Having similarity with MOSFET, iTFET is also assumed to suffer the effect of drain induced barrier lowering (DIBL). We consider DIBL as,

$$\lambda_{DIBL} = \alpha V_{DS} \tag{5.10}$$

where α is the frational coefficient of DIBL and lies between 0 to 1 where 0 stands for no drain bias effect and 1 stands for full drain bias effect [30]. Now the effective change in channel Fermi level $\Delta\phi$ becomes,

$$\Delta\phi = V_G - V_{ch} - V_V - \lambda_{DIBL} \tag{5.11}$$

Equation (5.11) is dependent on Eq. (5.5) and is a transcendental equation which needs to be solved both numerically and self-consistently. Considering transverse mode along the channel for an energy window between 0 to $\Delta\phi$, using Landauer's expression, lateral drain current between source and drain of MoS_2 JTET can be written as follows [30]:

$$I = \int dE[(G(E)(f_S(E) - f_D(E)))] \tag{5.12}$$

Here G(E) is channel conductance and expressed as,

$$G(E) = (2q^2/\hbar) T_B(E) M(E) \tag{5.13}$$

where $f_S(E)$ and $f_D(E)$ are source and drain Fermi levels, respectively. $T_B(E)$ is the ballistic transmission coefficient in the channel and is taken 1 for the ballistic transport. $M(E)$ is the number of modes in the channel and written as follows [31]:

$$M(E) = g_v W \sqrt{2m^*_{MoS_2}(E - E_C)} \Big/ \pi\hbar \tag{5.14}$$

where W is the width of the channel and E_C is position of the channel conduction band. Combining Eq. (5.12) to Eq. (5.14), drain current becomes,

$$I_D = \int dE \left(\frac{2q^2}{\pi\hbar^2} g_v W \sqrt{2m^*_{MoS_2}(E - E_C)} \left(f_S(E) - f_D(E) \right) \right) \tag{5.15}$$

The Fermi functions in the source and drain are described as follows:

$$f_S(E) = \frac{1}{1 + e^{\left(E - E_F^S\right)/k_B T}} \tag{5.16}$$

and $$f_D(E) = \frac{1}{1 + e^{\left(E - E_F^D\right)/k_B T}} \tag{5.17}$$

Equation (5.15) becomes,

$$I_D = \frac{2q^2}{\pi\hbar^2} g_v W \sqrt{2m^*_{MoS_2}} \int \left(\frac{\sqrt{(E - E_C)}}{1 + e^{\left(E - E_F^S\right)/k_B T}} - \frac{\sqrt{(E - E_C)}}{1 + e^{\left(E - E_F^D\right)/k_B T}} \right) dE \tag{5.18}$$

Now considering,

$$\xi = (E - E_C)/k_B T \tag{5.19}$$

$$\eta_{FS} = (E_F^S - E_C)/k_B T \tag{5.20}$$

$$\eta_{FD} = (E_F^D - E_C)/k_B T \tag{5.21}$$

Drain current in Eq. (5.18) can be written as follows:,

$$I_D = \frac{q^2}{\sqrt{\pi}\hbar^2} g_v W \sqrt{2m^*_{MoS_2} q V_T} \left[\Im_{1/2}(\eta_{FS}) - \Im_{1/2}(\eta_{FD}) \right] \tag{5.22}$$

where $$\Im_{1/2}(\eta_{FS}) = \frac{2}{\sqrt{\pi}} \int_0^{\Delta\phi} \frac{\xi^{1/2}}{1 + e^{(\xi - \eta_{FS})}} d\xi \tag{5.23}$$

and $$\Im_{1/2}(\eta_{FD}) = \frac{2}{\sqrt{\pi}} \int_0^{\Delta\phi} \frac{\xi^{1/2}}{1 + e^{(\xi - \eta_{FD})}} d\xi \tag{5.24}$$

Both Eq. (5.20) and Eq. (5.21) are the expressions of Fermi-Dirac integral of order ½ which needs to be solved numerically. Solving Eq. (5.19) for ξ from 0 to $\Delta\phi$, drain current can be written as follows:

$$I = \frac{2q^2}{\sqrt{\pi}\hbar^2} W \sqrt{2m^*_{MoS_2} q V_T}\,[\sqrt{\chi_1} - \sqrt{\chi_2}\,] \tag{5.25}$$

$$\chi_1 = (\Delta\phi - E_C)[ln(1+exp(\Delta\phi - E_F^D)) - ln(1+exp(\Delta\phi - E_F^S))] \tag{5.26}$$

$$\chi_2 = (-E_C)[ln(1+exp(-E_F^D)) - ln(1+exp(-E_F^S))] \tag{5.27}$$

From Eq. (5.25), the drain current depends on both Eqs. (5.5) and (5.11) for which it needs to be solved self-consistently in order to account for both interlayer tunneling induced charge density and source-drain ballistic transport.

5.4 Results and Discussion

Using Eqs. (5.5), (5.11) and (5.25), transfer characteristics of iTFET are plotted in Fig. 5.4. A small negative differential resistance (NDR) region is observed at different drain bias at room temperature as shown in Fig. 5.4(a). For V_{DS} = 1.2V, an on/off current ratio of 17 with a subthreshold slope of 57 mV/decade is obtained for $V_G > 0$ which is 70 mV/decade for $V_G < 0$ with an on/off current ratio of 18. The off-state leakage current of MoS_2 JTET is calculated as 25.2 μA for V_{DS} = 1.2 V. Subthreshold slope is calculated from SS=ln(10)[I_D/(dI_D/dV_G)], where I_D is the drain current and V_G is the gate bias. Compared to a conventional MOSFET, a reduced subthreshold slope at low on/off current ratio in MoS_2 JTET is observed and explained through Figs. 5.5(a)-(c).

The intrinsic MoS_2 channel in Fig. 5.5(a) considers the source (E_{FS}), channel (E_{FC}) and drain (E_{FD}) Fermi levels in equilibrium. As the negative gate bias ($V_G < 0$ giving $qV_G > 0$) is applied, the degenerately doped (from interlayer tunneling) n-type channel Fermi level (E_{FC})

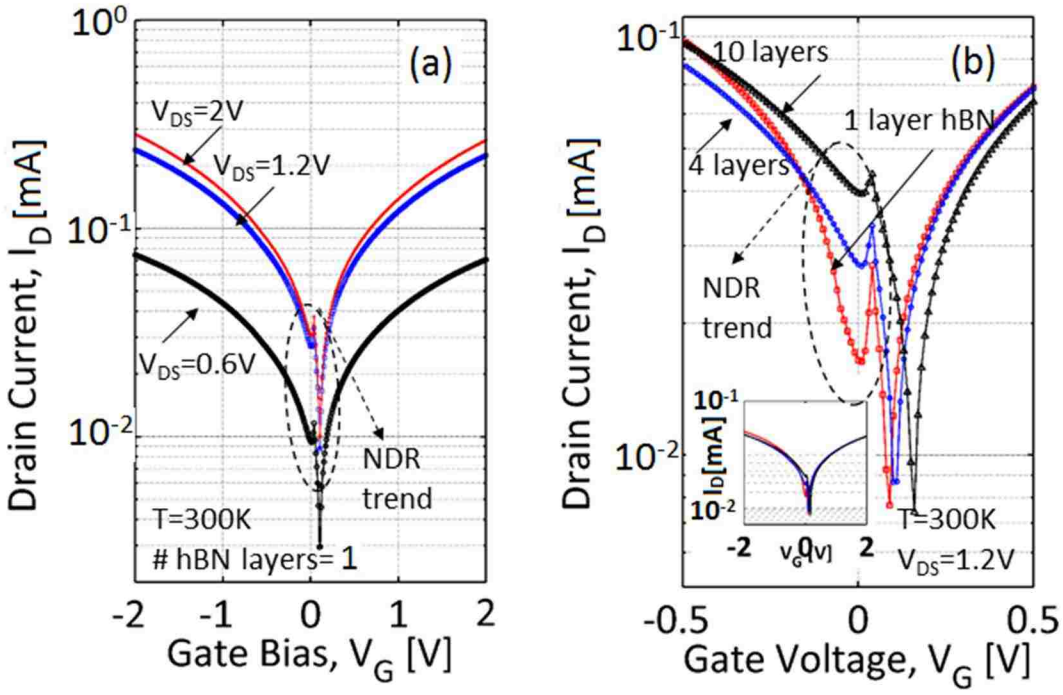


Figure 5.4: Transfer characteristics of MoS_2 JTET. a) I_D - V_G curve for different drain biases (V_{DS}) and b) I_D - V_G curve for different number of *h*BN layers as tunnel barrier between top and bottom MoS_2 n drain culayers. Inset in (b) shows drain current for complete bias operation where effect of number of *h*BN layers orrent are non-differentiable.

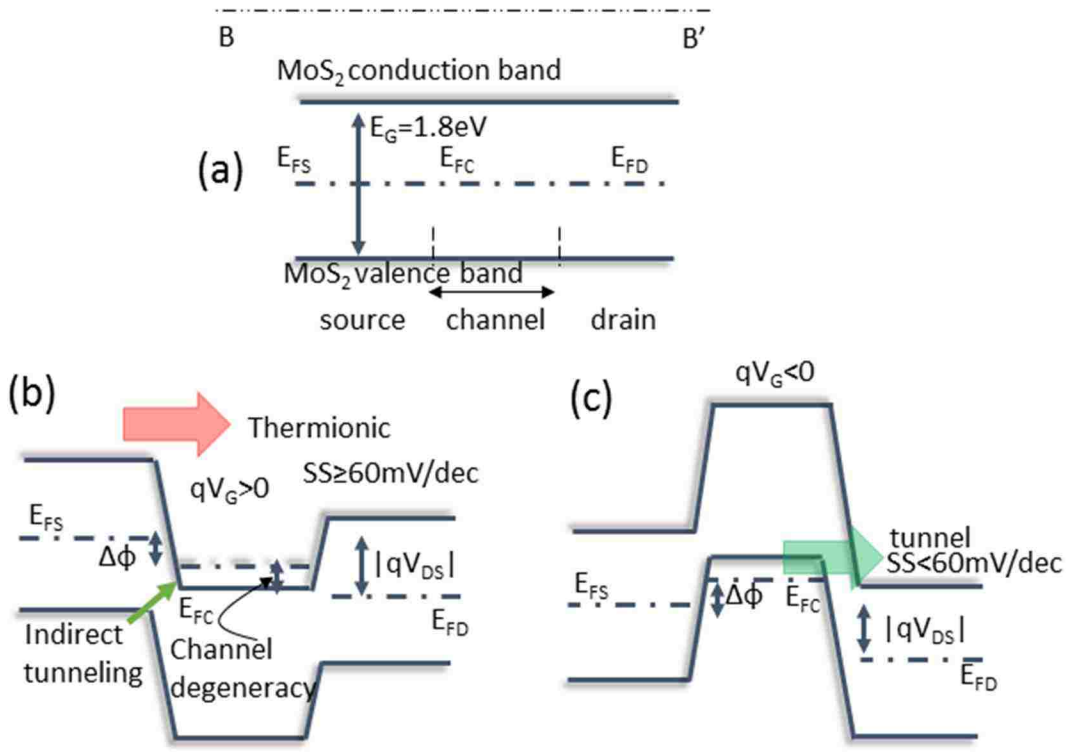


Figure 5.5: (a) Energy band diagram of bottom (channel) MoS_2 layer in equilibrium at off-state of MoS_2 JTET, (b) energy band diagram at on-state for $qV_G > 0$ and (c) energy band diagram at on-state for $qV_G < 0$. Red arrow points for thermionic transport and green arrow for band-to-band tunneling transport. BB′ refers to lateral direction of ballistic transport between source and drain.

moves down which is shown in Fig. 5.5(b). The $|qV_{DS}|$ is the amount of shift between E_{FS} and E_{FD} due to drain-source bias. Similar to a MOSFET, thermionic transport (red arrow) dominates the source-drain ballistic transport. For this reason, a subthreshold slope more than the thermionic limit of 60 mV/decade is observed. A small amount of phonon assisted indirect band-to-band tunneling (BTBT) is assumed which occurs between source and channel and is shown by a single green arrow in Fig. 5.5(b). Note that similar BTBT contributes toward the NDR trend which is also found in ATLAS TFET for a p+ Ge source and n- MoS_2 channel [19]. As the positive gate bias ($V_G > 0$ giving $qV_G < 0$) is applied, the degenerately doped (from interlayer tunneling) p-type Fermi level (E_{FC}) of the channel moves below the channel valence band. Hence, the channel valence band comes opposite to the drain conduction band and channel-drain BTBT is occurred. A subthreshold slope of 57 mV/decade is observed due to this BTBT dominated drain current which is shown by green arrow in Fig. 5.5(c).

Number of hBN layers as tunnel barriers also affects MoS_2 JTET transfer characteristics which is studied in Fig. 5.4(b). As the number of *h*BN layers as tunnel barrier increases, the tunneling probability exponentially decreases which results in less charge density. Therefore, with a shallow degeneracy, less NDR is observed at higher number of *h*BN layers. The output characteristics of MoS_2 JTET are plotted in Figs. 5.6(a) and 5.6(b) considering change of gate bias and change in number of *h*BN layers, respectively. Since operation of MoS_2 JTET is more controlled by the gate bias than drain bias, insignificant effect is observed in output characteristics as the number of *h*BN layers varies in Fig. 5.6(b).

Compared to benchmarked performance of monolayer MoS_2 transistor [20, 21], MoS_2 JTET provides low on/off current ratio. This can be understood from the field effect mobility (μ_{FE}) diagram in Fig. 5.7. Field effect mobility is estimated from $\mu_{FE}=dI_D/dV_G(L/W)(1/C_G)$,

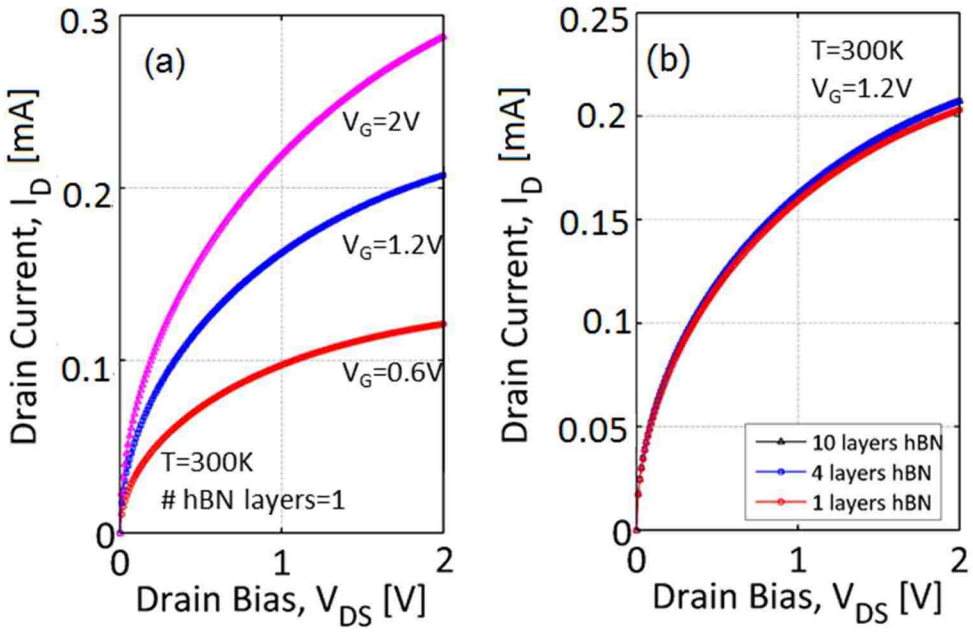


Figure 5.6: Output characteristics of MoS_2 JTET. a) I_D - V_{DS} curve for different gate biases (V_G) and b) I_D - V_{DS} curve for different number of *h*BN layers as tunnel barrier between top and bottom MoS_2 layers.

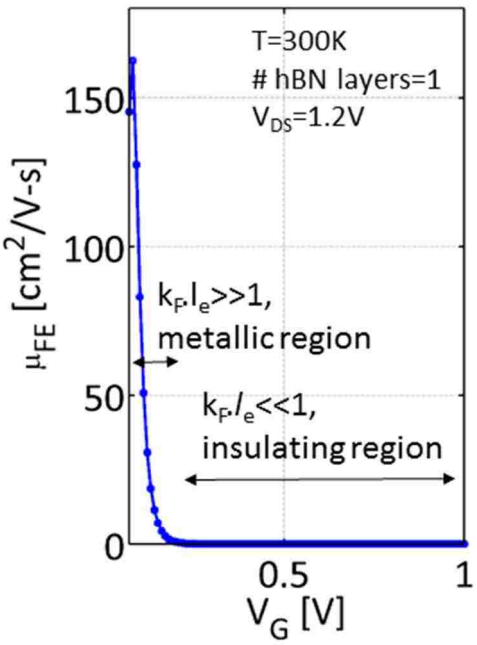


Figure 5.7: Gate bias dependent field effect mobility in MoS_2 JTET.

considering both quantum and geometric capacitances [29]. As V_G increases, μ_{FE} drops. Based on semi-classical Drude formula, conductivity $\sigma(=\mu_{FE}Nq)$ is linearly dependent on μ_{FE}. Therefore, as the channel MoS_2 becomes degenerately doped, conductivity drops as μ_{FE} decreases.

Moreover, a further study of metal-insulator transition in the channel MoS_2 layer of MoS_2 JTET can be understood by Ioffe-Regel criterion [32, 33]. According to this criterion, MoS_2 is metallic for $k_F l_e >> 1$ and is insulating for $k_F l_e << 1$. Here $k_F = \sqrt{(2\pi N)}$ is Fermi wave vector and $l_e = \hbar k_F \sigma / Nq^2$ is the mean free path [32]. Two points are selected to check this criteria ($V_G = 0.2$ V and 0.5 V) between which the mobility drops. Using Fig. 5.7, $V_G = 0.2$ V, $k_F l_e \sim 294$ (>> 1); and at $V_G = 0.5$ V, $k_F l_e \sim 5.16 \times 10^{-4}$ (<< 1) are found, providing a metal-insulator transition in the channel MoS_2 layer at high gate bias. Therefore, a low on-state drive current is obtained resulting in low on/off current ratio in MoS_2 JTET. The low subthreshold slope of MoS_2 JTET is comparable with the standard MOSFET subthreshold slope of 60 mV/decade. However, metal insulator transition and mixed mode of thermionic and BTBT current transport limits achieving high on/off current ratio in MoS_2 JTET.

The capacitance network for the MoS_2 JTET is shown in Fig. 5.8. The total gate capacitance is estimated as follows: $1/C_G = 1/C_V + 1/Cq_{ch}$ where $1/C_V = 1/(C_1+C_2) + 1/(C_3+C_4) + 1/(C_5+C_6) + 1/(C_8+C_9)$ considering series-parallel network of all the vertical capacitances. The geometric and quantum capacitances of top and bottom gate *h*BN layers and top MoS_2 layer are expressed as $C_1 = C_8 = \varepsilon_0 \varepsilon_{hBN}/(Z_g t_{hBN})$, $C_2 = C_9 = C_{q,hBN}/Z_g$, $C_3 = \varepsilon_0 \varepsilon_{MoS2}/t_{MoS2}$ and $C_4 = C_{q,MoS2} = q^2 \rho_{MoS2}$, respectively. $C_{q,hBN} = q^2 \rho_{hBN}$ (where $\rho_{hBN} = g_s g_v m^*_{hBN}/(2\pi\hbar^2)$) is the quantum capacitance of single layer *h*BN [34]. Z_g is the number of *h*BN layers ($Z_g = 20$) in gate dielectric in AA′ direction. Similarly, the geometric and quantum capacitances of the single layer *h*BN as tunnel barrier are expressed as $C_5 = \varepsilon_0 \varepsilon_{hBN}/(Z_t t_{hBN})$ and $C_6 = C_{q,hBN}/Z_t$ (where Z_t is the number of *h*BN layers ($Z_t = 1$) in

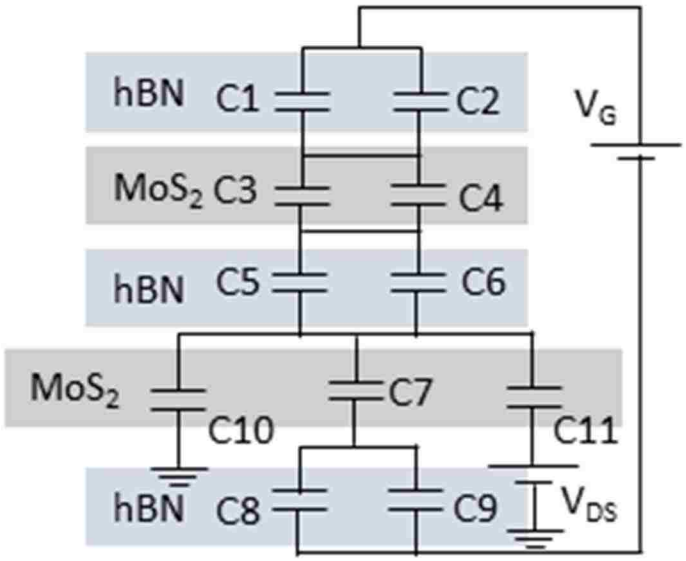


Figure 5.8. Capacitive network of MoS_2 JTET.

tunnel barrier), respectively. C_{10} and C_{11} are source and drain quantum capacitance of MoS_2. Note that t_{MoS2} (=0.65 nm) and ε_{MoS2} (=2.8) [35], t_{hBN} (= 0.325 nm) and ε_{hBN} (= 4) are the thickness and dielectric permittivity of MoS_2 and hBN, respectively. Based on the work of Ma and Jena [29], the gate dependent channel quantum capacitance (Cq_{ch}) is estimated as follows:

$$Cq_{ch} = C_7 = q^2 \rho_{MoS_2} \left[1 + \frac{exp(E_G / 2k_B T)}{2\, cosh(q\, \Delta\phi / k_B T)} \right]^{-1} \tag{5.28}$$

Using Eqs. (5.5) and (5.11), Eq. (5.28) is solved and is plotted in Fig. 5.9. For V_G = 1.2 V, C_G is estimated to be 0.0952 F/m^2. Intrinsic cut-off frequency (f_T=g_m/2πC_G) dependence on gate bias is shown in Fig. 5.10 for transconductance, $g_m = dI_D/dV_G$. For a supply voltage of 1.2 V, f_T = 19.73 THz has been calculated which increases as V_G reduces. This value is higher than the reported f_T in [9] and [10]. Intrinsic frequency of MoS_2 transistors is independent of on/off current ratio [36, 37] and is related to gate capacitance. From Fig. 5.9, the gate capacitance (C_G) is nearly two orders less than the channel quantum capacitance (Cq_{ch}) for which MoS_2 JTET achieves very low gate capacitance providing high intrinsic cut-off frequency. Using $\tau = C_G V_{DD}/I_{ON}$, intrinsic gate delay is plotted in Fig. 5.11(a) from which the power delay product ($PDP = \tau V_{DD} I_{ON}$) is plotted in Fig. 5.11(b). From Figs. 5.9 and 5.10, beyond THz operation of MoS_2 JTET can be observed.

Performance of MoS_2 JTET is compared in Table 5.1 with the results reported in [9] and [10] for an equal number of *h*BN layers as tunnel barrier and gate bias. In terms of subthreshold slope, MoS_2 JTET provides ~7 and ~27 times less than that of the reported in [9] and [10], respectively, for graphene vertical FETs. Due to a small band gap at 5nm width, subthreshold slope of MoS_2 JTET is 23 times less than that of the vertical GNR iTFET reported in [10]. Compared to both [9] and [10], MoS_2 JTET provides THz operation due to very low gate capacitance. The on/off current ratio is nearly the same as reported in [9] and [10]. Furthermore,

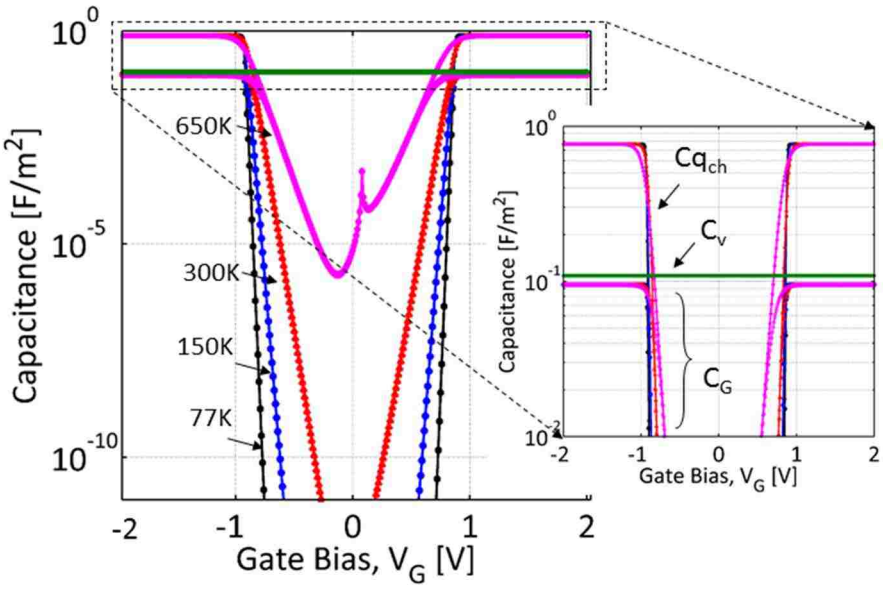


Figure 5.9: Change in channel quantum capacitance (Cq_{ch}) and total gate capacitance (C_G) with gate bias (V_G) for different temperature of MoS_2 JTET. Note: Non-channel fixed vertical capacitance (C_V) is shown in green line.

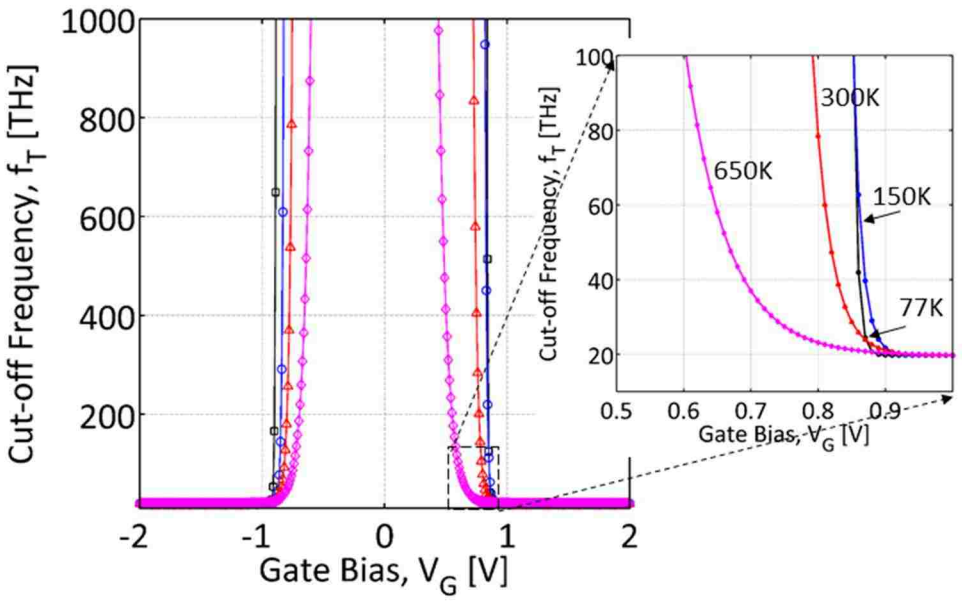


Figure 5.10: Intrinsic cut-off frequency (f_T) variation of MoS_2 JTET with change in gate bias (V_G).

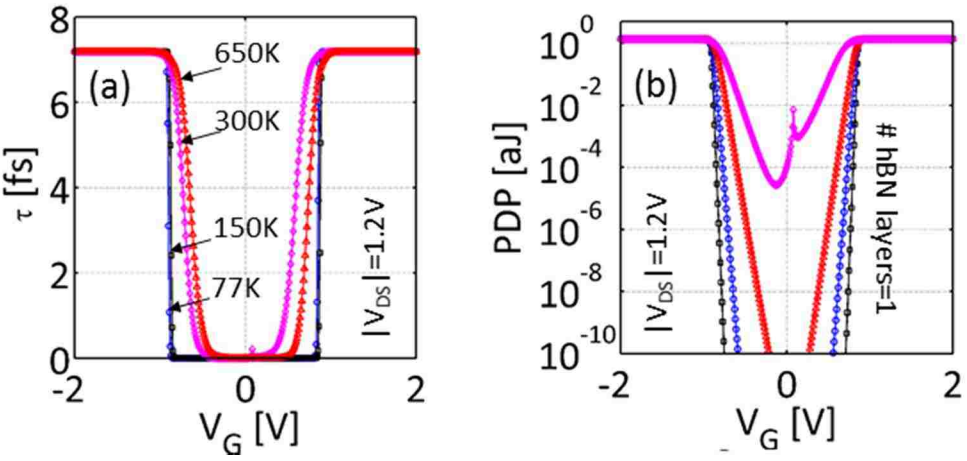


Figure 5.11: (a) Intrinsic gate delay (τ) versus the gate bias (V_G) and (b) corresponding power delay product (PDP) for different temperatures of MoS_2 JTET.

Table 5.1

Comparison of MoS2 JTET Performance with Earlier Similar Models

Parameters	Fiori et al. Ref [9]	VTGFET Ref [10]	VTGNRFET Ref [10]	MoS_2 JTET
Gate Voltage	1.2 V	1.2 V	1.2 V	1.2 V
#hBN Layers	3	3	3	3
Subthreshold Slope	386 mV/dec	1535 mV/dec	1297 mV/dec	57 mV/dec
I_{on}/I_{off}	~15	3	4	17
Cut-off Frequency	0.5 GHz	58 GHz	97 GHz	19.73 THz

Table 5.2

Comparison of MoS2 JTET with Existing Two Dimensional High Frequency Devices

Ref. [Year]	Device Transport Type	Material System/Channel	Channel Length/Tunneling Barrier Thickness	Bias Voltage	I_{On}/I_{Off}	f_T
9 [2013]	iTFET	Graphene-*h*BN-Graphene	1.03 nm (tunneling barrier thickness)	1.2V	15	0.5 GHz
10 [2014]	iTFET	GNR-*h*BN-GNR	1.03 nm (tunneling barrier thickness)	1.2V	4	97 GHz
36 [2016]	FET	CVD MoS_2 on flexible substrate	1 μm (channel)	2V	10^5	5.6 GHz
38 [2009]	FET	Graphene	500 nm (channel)	1.6V	~2	4 GHz
39 [2014]	FET	MoS_2	240 nm (channel)	2V	~300	8.2 GHz
40 [2012]	FET	Bilayer Graphene	40 nm (channel)	1V	~800	1.5 THz
41 [2010]	FET	Graphene	140 nm (channel)	1V	~3	300 GHz
42 [2011]	FET	Graphene	40 nm (channel)	1.5V	~800	155 GHz
43 [2013]	FET	Epitaxial Graphene from SiC	100 nm (channel)	0.8V	~2	110 GHz
44 [2013]	BJT type	Graphene base heterojunction	2-5 nm (SiO_2 tunneling barrier thickness)	1V	10^4	1 THz
45 [2013]	Hot electron transistor	Graphene base	2 nm (Al_2O_3 tunneling barrier thickness)	1.5V	$>10^5$	unspecified
46 [2015]	TFET	Graphene Nanoribbon (GNR)	20 nm (channel)	0.1V	122	~1 THz

(Table 5.2 continued)

Ref. [Year]	Device Transport Type	Material System/Channel	Channel Length/Tunneling Barrier Thickness	Bias Voltage	I_{On}/I_{Off}	f_T
47 [2012]	TFET	Graphene-*h*BCN	7 nm (channel)	0.6V	10^4	~2 THz
48 [2016]	Interlayer excitonic generation	MoS_2-*h*BN-MoS_2	5 nm (tunneling barrier thickness)	-	-	-
49 [2014]	FET	Black phosphorus	300 nm (channel)	2V	$2x10^3$	12 GHz
50 [2012]	iTFET-plasma resonance based	Graphene-barrier-Graphene	10 nm (tunneling barrier thickness) 500 nm (channel)	0.5V	unspecified	1.42 THz
51 [2014]	FET	Bilayer Graphene	2.5 μm (channel)	0.001	unspecified	0.29-0.38THz
52 [2014]	FET	Exfoliated MoS_2 on SiO_2	68 nm (channel)	5V	10^4	42 GHz
53 [2015]	FET	CVD MoS_2 on SiO_2	250 nm (channel)	3.5V	200	6.7 GHz
This work	iTFET-interlayer tunneling based barrier control	MoS_2-*h*BN-MoS_2	10 nm (channel) 1.03 nm (tunneling barrier thickness)	1.2V	17	19.73THz

high frequency performance of this MoS_2 JTET is also compared with the existing two dimensional materials (both graphene and non-graphene) based high frequency devices and is summarized in Table 5.2.

Based on the data in Table 5.2, MoS_2 JTET outperforms other devices at a comparable supply voltage, on/off current ratio and channel length. The only similar device structure like MoS_2 JTET is found in the work of Calman et al. [48] which studies controlled excitonic generation in similar van da Waals heterostructure. However, the work in [48] does not account for any high frequency performance estimation and transistor type electronic behavior and hence become unsuitable for comparison. The high frequency performance of MoS_2 JTET originates from interlayer tunneling based barrier control mechanism and use of two dimensional layered materials (in this work *h*BN) as the gate dielectric providing low gate-capacitance.

5.5 Conclusion

Current transport MoS_2 JTET is studied in this chapter which is controlled by the gate induced interlayer tunneling dependent charge density unlike inversion mode operation in MOSFETs. The current transport between source and drain is ballistic. Compared to recently reported device structures in [9] and [10], the present device structure gives subthreshold slope close to 60 mV/decade and demonstrates upper GHz operation with relatively comparable on/off current ratio. Low bandgap insulator or wide bandgap layered semiconductor materials can be used as interlayer tunneling barrier to improve the on/off current ratio and making MoS_2 JTET suitable for digital applications. A comparison of performance of MoS_2 JTET with other types of device structures exhibits superior performance and high frequency THz operation.

5.6 References

[1] M. Waldrop, The chips are down for Moore's law. *Nature*, vol. 530, pp. 144–147, 2016.

[2] A. B. Sachid, M. Tosun, S. B. Desai, C.-Y. Hsu, D.-H. Lien, S. R. Madhvapathy, Y.-Z. Chen, M. Hettick, J. S. Kang, Y. Zeng, J.-H. He, E. Y. Chang, Y.-L. Chueh, A. Javey, and C. Hu, "Monolithic 3D CMOS using layered semiconductors," *Advanced Materials,* vol. 28, pp. 2547-54, 2016.

[3] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, A. K. Geim, K. S. Novoselov, and L. A. Ponomarenko, "Field-effect tunneling transistor based on vertical graphene heterostructures," *Science,* vol. 335, pp. 947-950, 2012.

[4] A. Sciambi, M. Pelliccione, M. P. Lilly, S. R. Bank, A. C. Gossard, L. N. Pfeiffer, K. W. West, and D. Goldhaber-Gordon, "Vertical field-effect transistor based on wave-function extension," *Physical Review B,* vol. 84, p. 085301, 2011.

[5] S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy, and A. H. MacDonald, "Bilayer pseudoSpin field-effect transistor (BiSFET): a proposed new logic device," *IEEE Elect. Dev. Lett.,* vol. 30, pp. 158-160, 2009.

[6] T. Georgiou, R. Jalil, B. D. Belle, L. Britnell, R. V. Gorbachev, S. V. Morozov, Y.-J. Kim, A. Gholinia, S. J. Haigh, O. Makarovsky, L. Eaves, L. A. Ponomarenko, A. K. Geim, K. S. Novoselov, and A. Mishchenko, "Vertical field-effect transistor based on graphene-WS2 heterostructures for flexible and transparent electronics," *Nat Nano,* vol. 8, pp. 100-103, 2013.

[7] P. Zhao, R. M. Feenstra, G. Gong, and D. Jena, "SymFET: a proposed symmetric graphene tunneling field-effect transistor," *IEEE Transactions on Electron Devices,* vol. 60, pp. 951-957, 2013.

[8] S. C. de la Barrera, Q. Gao, and R. M. Feenstra, "Theory of graphene–insulator–graphene tunnel junctions," *J. of Vac. Sci. & Tech. B,* vol. 32, p. 04E101, 2014.

[9] G. Fiori, S. Bruzzone, and G. Iannaccone, "Very large current modulation in vertical heterostructure graphene/hbn transistors," *IEEE Trans. on Elect. Dev.,* vol. 60, pp. 268-273, 2013.

[10] N. Ghobadi and M. Pourfath, "A comparative study of tunneling fets based on graphene and gnr heterostructures," *IEEE Trans. on Elect. Dev.,* vol. 61, pp. 186-192, 2014.

[11] A. Mishchenko, J. S. Tu, Y. Cao, R. V. Gorbachev, J. R. Wallbank, M. T. Greenaway, V. E. Morozov, S. V. Morozov, M. J. Zhu, S. L. Wong, F. Withers, C. R. Woods, Y. J. Kim, K. Watanabe, T. Taniguchi, E. E. Vdovin, O. Makarovsky, T. M. Fromhold, V. I. Fal'ko, A. K. Geim, L. Eaves, and K. S. Novoselov, "Twist-controlled resonant tunnelling in graphene/boron nitride/graphene heterostructures," *Nat Nano,* vol. 9, pp. 808-813, 2014.

[12] B. Fallahazad, K. Lee, S. Kang, J. Xue, S. Larentis, C. Corbet, K. Kim, H. C. P. Movva, T. Taniguchi, K. Watanabe, L. F. Register, S. K. Banerjee, and E. Tutuc, "Gate-tunable

resonant tunneling in double bilayer graphene heterostructures," *Nano Letters,* vol. 15, pp. 428-433, 2015.

[13] K. Sangwoo, B. Fallahazad, L. Kayoung, H. Movva, K. Kyounghwan, C. M. Corbet, T. Taniguchi, K. Watanabe, L. Colombo, L. F. Register, E. Tutuc, and S. K. Banerjee, "Bilayer graphene-hexagonal boron nitride heterostructure negative differential resistance interlayer tunnel FET," *IEEE Elect. Dev. Lett.,* vol. 36, pp. 405-407, 2015.

[14] G. Iannaccone, Q. Zhang, S. Bruzzone, and G. Fiori, "Insights on the physics and application of off-plane quantum transport through graphene and 2D materials," *Solid-State Electronics,* vol. 115, Part B, pp. 213-218, 2016.

[15] S. Bruzzone, D. Logoteta, G. Fiori, and G. Iannaccone, "Vertical transport in graphene-hexagonal boron nitride heterostructure devices," *Scientific Reports,* vol. 5, p. 14519, 2015.

[16] M. Fahad and A. Srivastava, "A Graphene Switching Transistor for Vertical Circuit Design," *ECS Journal of Solid State Science and Technology,* vol. 5, pp. M13-M21, 2016.

[17] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S. K. Banerjee, and L. Colombo, "Electronics based on two-dimensional materials," *Nat Nano,* vol. 9, pp. 768-779, 2014.

[18] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS2 transistors," *Nat Nano,* vol. 6, pp. 147-150, 2011.

[19] D. Sarkar, X. Xie, W. Liu, W. Cao, J. Kang, Y. Gong, S. Kraemer, P. M. Ajayan, and K. Banerjee, "A subthermionic tunnel field-effect transistor with an atomically thin channel," *Nature,* vol. 526, pp. 91-95, 2015.

[20] K. Alam and R. K. Lake, "Monolayer MoS_2 transistors beyond the technology road map," *IEEE Trans. on Elect. Dev.,* vol. 59, pp. 3250-3254, 2012.

[21] Y. Yoon, K. Ganapathi, and S. Salahuddin, "How good can monolayer MoS_2 transistors be?," *Nano Letters,* vol. 11, pp. 3768-3773, 2011.

[22] S. Wang, X. Wang, and J. H. Warner, "All chemical vapor deposition growth of MoS_2:h-BN vertical van der Waals heterostructures," *ACS Nano,* vol. 9, pp. 5246-5254, 2015.

[23] J. Jaarsma, "Monolayer MoS_2 on a substrate of hexagonal boron nitride", B.S. Thesis. Comp. Mat. Sci. Univ of Twente, 2014.

[24] G.-H. Lee, Y.-J. Yu, X. Cui, N. Petrone, C.-H. Lee, M. S. Choi, D.-Y. Lee, C. Lee, W. J. Yoo, K. Watanabe, T. Taniguchi, C. Nuckolls, P. Kim, and J. Hone, "Flexible and transparent MoS_2 field-effect transistors on hexagonal boron nitride-graphene heterostructures," *ACS Nano,* vol. 7, pp. 7931-7936, 2013.

[25] T. Roy, M. Tosun, J. S. Kang, A. B. Sachid, S. B. Desai, M. Hettick, C. C. Hu, and A. Javey, "Field-effect transistors built from all two-dimensional material components," *ACS Nano,* vol. 8, pp. 6259-6264, 2014.

[26] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, M. I. Katsnelson, L. Eaves, S. V. Morozov, A. S. Mayorov, N. M. R. Peres, A. H. Castro Neto, J. Leist, A. K. Geim, L. A. Ponomarenko, and K. S. Novoselov, "Electron tunneling through ultrathin boron nitride crystalline barriers," *Nano Letters,* vol. 12, pp. 1707-1710, 2012.

[27] C. M. Orofeo, S. Suzuki, and H. Hibino, "Ultrathin chemical vapor deposition (CVD)-grown hexagonal boron nitride as a high-quality dielectric for tunneling devices on rigid and flexible substrates," *The Journal of Physical Chemistry C,* vol. 118, pp. 3340-3346, 2014.

[28] J. G. Simmons, "Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film," *Journal of Applied Physics,* vol. 34, pp. 1793-1803, 1963.

[29] N. Ma and D. Jena, "Carrier statistics and quantum capacitance effects on mobility extraction in two-dimensional crystal semiconductor field-effect transistors," *2D Materials,* vol. 2, p. 015003, 2015.

[30] S. Datta, Quantum transport: Atom to transistor. Cambridge University Press. 2005

[31] M. Lundstrom and C. Jeong, Lessons from nanoscience: a lecture note series near-equilibrium transport, World Scientific. 2012: 20-31.

[32] B. Radisavljevic and A. Kis, "Mobility engineering and a metal–insulator transition in monolayer MoS_2," *Nat Mater,* vol. 12, pp. 815-820, 2013.

[33] M. Gurvitch, "Ioffe-Regel criterion and resistivity of metals," *Physical Review B,* vol. 24, pp. 7404-7407, 1981.

[34] S. Luryi, "Quantum capacitance devices," *Applied Physics Letters,* vol. 52, pp. 501-503, 1988.

[35] F. A. Rasmussen and K. S. Thygesen, "Computational 2D materials database: electronic structure of transition-metal dichalcogenides and oxides," *The Journal of Physical Chemistry C,* vol. 119, pp. 13169-13183, 2015.

[36] H. Y. Chang, M. N. Yogeesh, R. Ghosh, A. Rai, A. Sanne, S. Yang, N. Lu, S. K. Banerjee, and D. Akinwande, "Large-area monolayer MoS_2 for flexible low-power RF nanoelectronics in the GHz regime," *Advanced Materials,* vol. 28, pp. 1818-1823, 2016.

[37] L. Jongho, C. Hsiao-Yu, H. Tae-Jun, L. Huifeng, R. S. Ruoff, A. Dodabalapur, and D. Akinwande, "High-performance flexible nanoelectronics: 2D atomic channel materials for

low-power digital and high-frequency analog devices," *IEDM Tech. Digest*, pp. 19.2.1-19.2.4, 2013.

[38] Y.-M. Lin, K. A. Jenkins, A. Valdes-Garcia, J. P. Small, D. B. Farmer, and P. Avouris, "Operation of graphene transistors at gigahertz frequencies," *Nano Letters,* vol. 9, pp. 422-426, 2009.

[39] D. Krasnozhon, D. Lembke, C. Nyffeler, Y. Leblebici, and A. Kis, "MoS_2 transistors operating at gigahertz frequencies," *Nano Letters,* vol. 14, pp. 5905-5911, 2014.

[40] G. Fiori and G. Iannaccone, Insights on radio frequency bilayer graphene FETs. *IEDM Tech. Digest*, pp. 17.3.1-7.3.4, 2012.

[41] L. Liao, Y.-C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K. L. Wang, Y. Huang, and X. Duan, "High-speed graphene transistors with a self-aligned nanowire gate," *Nature,* vol. 467, pp. 305-308, 2010.

[42] Y. Wu, Y. M. Lin, A. A. Bol, K. A. Jenkins, F. Xia, D. B. Farmer, Y. Zhu, and P. Avouris, "High-frequency scaled graphene transistors on diamond-like carbon," *Nature,* vol. 472, pp. 74-78, 2011.

[43] Z. Guo, R. Dong, P. S. Chakraborty, N. Lourenco, J. Palmer, Y. Hu, M. Ruan, J. Hankinson, J. Kunc, J. D. Cressler, C. Berger, and W. A. de Heer, "Record maximum oscillation frequency in c-face epitaxial graphene transistors," *Nano Letters,* vol. 13, pp. 942-947, 2013.

[44] V. D. Lecce, R. Grassi, A. Gnudi, E. Gnani, S. Reggiani, and G. Baccarani, "Graphene-base heterojunction transistor: an attractive device for terahertz operation," *IEEE Elect. Dev. Lett.,* vol. 60, pp. 4263-4268, 2013.

[45] C. Zeng, E. B. Song, M. Wang, S. Lee, C. M. Torres, J. Tang, B. H. Weiller, and K. L. Wang, "Vertical graphene-base hot-electron transistor," *Nano Letters,* vol. 13, pp. 2370-2375, 2013.

[46] M. S. Fahad, A. Srivastava, A. K. Sharma, C. Mayberry, Analytical current transport modeling of graphene nanoribbon tunnel field-effect transistors for digital circuit design. *IEEE Trans. Nanotech*., vol. 15, pp. 39-50, 2016.

[47] G. Fiori, A. Betti, S. Bruzzone, and G. Iannaccone, "Lateral graphene–hbcn heterostructures as a platform for fully two-dimensional transistors," *ACS Nano,* vol. 6, pp. 2642-2648, 2012.

[48] E. V. Calman, C. J. Dorow, M. M. Fogler, L. V. Butov, S. Hu, A. Mishchenko, and A. K. Geim, "Control of excitons in multi-layer van der Waals heterostructures," *Applied Physics Letters,* vol. 108, p. 101901, 2016.

[49] H. Wang, X. Wang, F. Xia, L. Wang, H. Jiang, Q. Xia, M. L. Chin, M. Dubey, and S. J. Han, "Black phosphorus radio-frequency transistors," *Nano Letters,* vol. 14, pp. 6424-6429, 2014.

[50] V. Ryzhii, T. Otsuji, M. Ryzhii, and M. S. Shur, "Double graphene-layer plasma resonances terahertz detector," *Journal of Physics D: Applied Physics,* vol. 45, p. 302001, 2012.

[51] D. Spirito, D. Coquillat, S. L. De Bonis, A. Lombardo, M. Bruna, A. C. Ferrari, V. Pellegrini, A. Tredicucci, W. Knap, and M. S. Vitiello, "High performance bilayer-graphene terahertz detectors," *Applied Physics Letters,* vol. 104, p. 061111, 2014.

[52] R. Cheng, S. Jiang, Y. Chen, Y. Liu, N. Weiss, H.-C. Cheng, H. Wu, Y. Huang, and X. Duan, "Few-layer molybdenum disulfide transistors and circuits for high-speed flexible electronics," *Nat Comm.,* vol. 5, 2014.

[53] A. Sanne, R. Ghosh, A. Rai, M. N. Yogeesh, S. H. Shin, A. Sharma, K. Jarvis, L. Mathew, R. Rao, D. Akinwande, and S. Banerjee, "Radio frequency transistors and circuits based on CVD MoS_2," *Nano Letters,* vol. 15, pp. 5039-5045, 2015.

CHAPTER 6*

FUNDAMENTAL PHYSICAL LIMITATION OF INTERLAYER TUNNEL TRANSISTOR

6.1 Introduction

In absence of an energy band gap, field effect transistor (FET) based on graphene channel suffers high off-state leakage current and a very poor on/off current ratio [1]. Subthreshold slope of such a graphene transistor is also very high making these questionable for the digital integrated circuit design. With the advancement of band gap engineering, graphene nanoribbon (GNR) based FET becomes suitable for logic applications. Nevertheless, complicated band gap engineering makes such GNR devices complicated for further process integration compared to mature CMOS technology. For this reason, use of infinite graphene sheet free of band gap engineering becomes an idealistic approach for exploration of graphene based transistor technology. However, conventional planar transport in graphene FET suffers the inherent high off-state leakage current requiring alternative current transport mechanism. With this regard, transistor based on interlayer tunneling between two graphene layers separated by a few layers of two dimensional materials (both semiconductor and insulators) have been studied and promising results are obtained [2-12]. High on/off current ratios (~10^4 - 10^6) at low supply voltages have been observed in these interlayer tunnel transistors. Some of these tunnel transistors have demonstrated resonant tunneling behavior as well. Interlayer tunneling based barrier control mechanism in novel vertical two dimensional MOSFETs has been studied recently and promising performances are obtained at low supply voltages [13, 14]. However, subthreshold slope for such a type of interlayer tunnel transistors remains unreported or poorly discussed.

---

*Part of this work is reported in the following publication:
M. Fahad and A. Srivastava, "Subthreshold slope of vertical graphene interlayer tunnel transistor," *Nano,* vol. 12, no. 6, p. 1750069, 2017

Moreover, the material or device parameters determining the subthreshold slope are not often understood properly, which is a key figure of merit in determining their suitability beyond the Moore's law. Since the subthreshold slope in a MOSFET is limited to 60 mV/decade or higher at room temperature, it is necessary to study the subthreshold slope of such graphene-hBN-graphene heterostructure interlayer tunnel transistors for their suitability of sub-60 mV/decade operation. Compared to a MOSFET, planar tunnel field effect transistors (TFETs) have shown the promise of sub-60 mV/decade subthreshold slopes [15, 16].

Compared to a conventional MOSFET and TFET, subthreshold slope in a Schottky barrier FET cannot go down below 60 mV/decade which was shown in the work of Vandenberghe et al. [17]. Considering a dielectric tunnel barrier along the channel laterally in a tunnel transistor consisting graphene, Svintsov et al. [18] estimated that the subthreshold slope of such a Schottky barrier FET is also limited to 60 mV/decade. However, compared to the theory developed in [17] and [18] for the Schottky barrier FET, graphene interlayer tunnel transistors are not only different structurally but also in terms of operating principles. For this reason, it is necessary to formulate an accurate subthreshold slope model of graphene interlayer tunnel field effect transistor type structures compared to conventional TFET, MOSFET and Schottky barrier FET. Although an analytical subthreshold slope model for a planer TFET can be found for the bulk material or graphene nanoribbon TFET in [19] and [20], and for Schottky barrier FET in [17] and [18], respectively, similar model for vertical interlayer tunnel transistors is still an active field of research. Hence, a physics based subthreshold slope model validated by either numerical computation or experimental data retains high importance for the progress of interlayer tunnel transistor research beyond the Moore's law. Moreover, such model will help to study suitability for logic, analog and THz frequency operations of this interlayer tunnel transistor.

In this Chapter, it has been derived that the subthreshold slope of interlayer tunnel transistors is limited by (ln10)(k_BT/q) or 60 mV/decade. The drain Current equations, with and without energy dependence, are plotted, which demonstrate higher subthreshold slope compared to the thermionic limit of 60 mV/decade. Furthermore, we have developed a physics based analytical model for estimating the subthreshold slope of an interlayer tunnel transistor considering graphene-hBN-graphene vertical heterostructure. The results obtained from analytical calculations are compared with the subthreshold slope obtained from numerical calculations.

6.2 Device Structure of Interlayer Tunnel Transistor

Schematic of a graphene/hBN/graphene vertical interlayer tunnel transistor is shown in Fig. 6.1. Considering tunneling through a few layers of hBN, the considered device structure is shown in Fig. 6.1 which ensembles similar to devices reported in [2, 3, 8, 9, 11] for graphene/hBN/graphene interlayer tunneling transistor. The tunneling direction between source and drain is in the vertical direction (Y-axis). The energy band diagrams for the schematic of Fig. 6.1 are shown in Figs. 6.2(a) and 6.2(b) for the off- and on- state, respectively. In the off-state shown in Fig. 6.2(a), the Fermi levels in both the top (E_F^T) and bottom (E_F^B) graphene layers are in equilibrium resulting in no net tunneling between these two layers. As the gate-source bias, V_{GS} is applied in addition to the drain-source tunneling bias, V_{DS}, the hBN tunneling barrier screens out some electric field. However, still some band bending occurs in the bottom graphene layer which results in a finite energy difference due to ΔV_{GS} between E_F^T and E_F^B. This results in tunneling current to flow between the top and bottom graphene layers through hBN. As the device turns on, following three components contribute to current transport in the interlayer

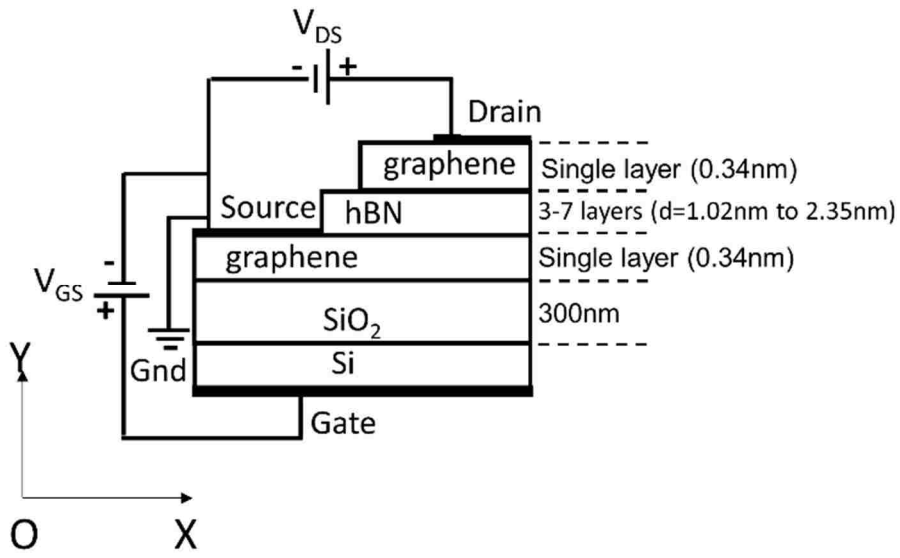


Figure 6.1: Schematic of a graphene/hBN/graphene vertical interlayer tunnel transistor. Drain current flows in vertical O-Y direction between source and drain controlled by the gate.

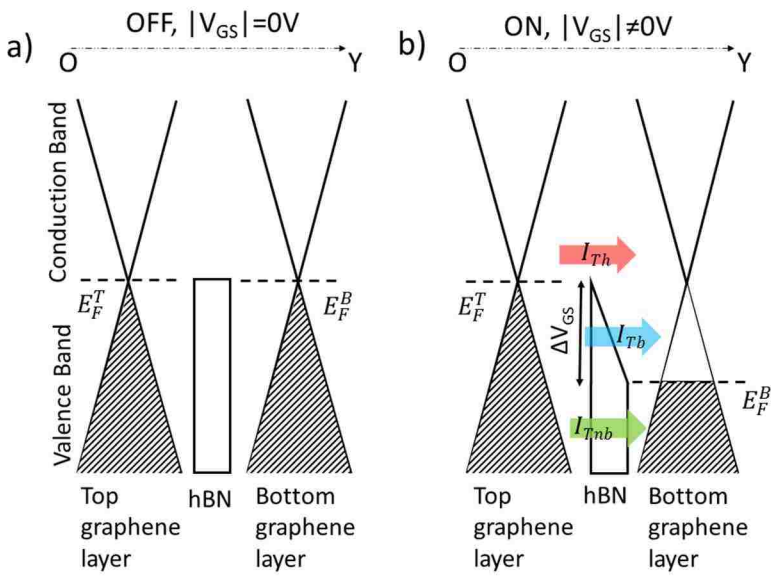


Figure 6.2: Schematic of interlayer tunneling between two graphene layers separated by a tunneling barrier hBN. a) Off state when the bias, $|V_{GS}| = 0$ V and b) on state when bias $|V_{GS}| \neq 0$ V. Note: Tunneling in vertical O-Y direction is shown following the schematic of Fig. 6.1.

tunnel transistor: a) thermionic current component over the barrier, I_{Th}, b) tunneling bias current, I_{Tb} and c) tunneling non-bias current, I_{Tnb}. We define the initial current, I_{In} at the moment bias is applied and the final current, I_{Fi} when the tunneling bias, V_{GS} is applied. The initial and final currents are expressed as follows:

$$I_{In} = I_{Th} + I_{Tb} + I_{Tnb} \tag{6.1}$$

$$I_{Fi} = I_{Th} e^{\left(\Delta q V_{GS} / k_B T\right)} + I_{Tb} \tag{6.2}$$

We have assumed that the net change between two graphene Fermi levels occurs due to the V_{GS}. Since the standard expression of subthreshold slope is dependent on gate-source bias (V_{GS}) rather on drain-source bias (V_{DS}) [19], the assumptions in this chapter do not consider the effect of drain bias for ease of calculation while estimating the subthreshold slope of this type of interlayer tunnel transistor.

Now considering gate bias, $V_{GS,}$ initial current I_{In} and final current, I_{Fi}, the subthreshold slope can be expressed as follows [16]:

$$SS = \frac{\Delta V_{GS}}{\log_{10}\left(\frac{I_{Fi}}{I_{In}}\right)} = \frac{\ln 10(\Delta V_{GS})}{\ln\left(\frac{I_{Fi}}{I_{In}}\right)} \tag{6.3}$$

$$SS = \frac{\ln 10(\Delta V_{GS})}{\ln\left(\frac{I_{Th} e^{\left(\Delta q V_{GS} / k_B T\right)} + I_{Tb}}{I_{Th} + I_{Tb} + I_{Tnb}}\right)} \tag{6.4}$$

$$\text{In (4), } \frac{I_{Th} e^{\left(\Delta q V_{GS} / k_B T\right)} + I_{Tb}}{I_{Th} + I_{Tb} + I_{Tnb}} < \frac{I_{Th} e^{\left(\Delta q V_{GS} / k_B T\right)}}{I_{Th}} \tag{6.5}$$

Therefore, the expression of subthreshold slope can be reduced to as follows:

$$\frac{\ln 10(\Delta V_{GS})}{\ln\left(\frac{I_{Th}e^{\left(\Delta qV_{GS}/k_BT\right)}+I_{Tb}}{I_{Th}+I_{Tb}+I_{Tnb}}\right)} > \frac{\ln 10(\Delta V_{GS})}{\ln\left(\frac{I_{Th}e^{\left(\Delta qV_{GS}/k_BT\right)}}{I_{Th}}\right)} = \ln 10\frac{k_BT}{q} \tag{6.6}$$

Hence, it is obtained that subthreshold slope (SS) > 60 mV/decade from Eq. (6.6). This implies that the subthreshold slopes of such interlayer tunnel transistor structures are limited by the thermionic limit of 60 mV/decade.

6.3 Estimation of Subthreshold Slope in Vertical Interlayer Tunnel Transistor

The tunneling drain current flowing between source and drain and controlled by the gate in a vertical tunnel transistor is generally expressed in terms of the density of states integrated over all the allowed energy states for tunneling to occur from source to drain. With a finite tunneling probability and Fermi-Dirac distribution, this tunneling drain current depends on the type of the tunneling barrier material and the adjacent two conductive materials. For the graphene/hBN/graphene vertical heterostructure, the tunneling drain current can be written as follows [2]:

$$I = \int dE DoS_B(E) DoS_T(E - qV_{GS}) T_{WKB}(f_T - f_B) \tag{6.7}$$

where $DoS_B(E)$ and $DoS_T(E\text{-}qV_{GS})$ are the density of states of the bottom and top graphene layers, respectively. T_{WKB} is the finite tunneling probability estimated within the Wentzel–Kramers–Brillouin (WKB) approximation and E is the energy of electron at which tunneling occurs. The f_T and f_B are the Fermi-Dirac distributions of carriers at the top and bottom graphene layers, respectively.

Equation (6.7) assumes that there is no in-plane momentum or parallel wave vector conservation for a realistic case of graphene and hBN interface [2]. For a square tunneling barrier, both the perpendicular and parallel wave vectors are required to be considered for estimating the tunneling probability. However, at high electric field, tunneling probability can be

determined using the WKB approximation for a triangular tunneling barrier considering only perpendicular wave vectors and excluding the effect of parallel wave vectors. Thus, the in-plane or parallel momentums are not conserved. Tunneling probability can still be calculated for a graphene-hBN interface for a triangular potential barrier as found in both the works of Britnell et al. [2] and Britnell et al. [5]. Following the work of Britnell et al. [2], we have also considered the expression of tunneling probability for a triangular barrier independent of in-plane momentum, also known as parallel wave vector conservation.

For an isotopic heterostructure where a tunneling barrier separating top and bottom conductive layers are from the same type of materials, T_{WKB} can be expressed as follows [3]:

$$T_{WKB} = \exp\left(-\frac{2\sqrt{2m^*}}{\hbar} \int_0^d dx \sqrt{\Delta - \frac{xqV_{GS}}{d}} \right) \tag{6.8}$$

where m^* is the carrier (either hole or electron) effective mass inside the tunneling barrier, $\hbar$ is the reduced Planck's constant, Δ is the finite energy gap between the tunneling barrier and the conductive layers (unit in eV), d is the thickness of the tunneling barrier (unit in nm), q is the charge of an electron (magnitude) and V_{GS} is the applied gate bias with reference to source. Considering specific energy window from 0 to $\Delta - qV_{GS}$, from $\Delta - qV_{GS}$ to Δ and Δ to ∞, the tunneling probability and associated drain current with and without top and bottom density of states can be expressed as follows:

$$T_{WKB} = T_{WKB1} + T_{WKB2} \tag{6.9}$$

$$T_{WKB1} = \exp\left(-\frac{4\sqrt{2m^*}q^{3/2}}{3\hbar q V_{GS}/d} \left((\Delta - E)^{3/2} - (\Delta - E - V_{GS})^{3/2} \right) \right) \tag{6.10}$$

$$T_{WKB2} = \exp\left(-\frac{4\sqrt{2m^*}q^{3/2}}{3\hbar q V_{GS}/d} \left((\Delta - E)^{3/2} \right) \right) \tag{6.11}$$

$$f\left(E,\varepsilon_F\right)=\frac{1}{1+exp\left(\frac{E-\varepsilon_F}{V_T}\right)} \tag{6.12}$$

E is the energy of electron during tunneling and ε_F is the position of Fermi level. Excluding the effect of top and bottom graphene layer's density of states, drain current in Eq. (6.7) can be written as follows:

$$I=\int_0^{\Delta-qV_G}\left(f\left(E,\varepsilon_F\right)-f\left(E,\varepsilon_F-V_D\right)\right)T_{WKB1}dE+ \int_{\Delta-qV_G}^{\Delta}\left(f\left(E,\varepsilon_F\right)-f\left(E,\varepsilon_F-V_D\right)\right)T_{WKB2}dE+\int_{\Delta}^{\infty}\left(f\left(E,\varepsilon_F\right)-f\left(E,\varepsilon_F-V_D\right)\right)dE \tag{6.13}$$

In addition to Eq. (6.13), considering the effect of top and bottom graphene layer's density of states, drain current in Eq. (6.7) can be written as follows:

$$I_{DoS}=\int_0^{\Delta-qV_G}\left(f\left(E,\varepsilon_F\right)-f\left(E,\varepsilon_F-V_D\right)\right)|E||E-V_G|T_{WKB1}dE+ \int_{\Delta-qV_G}^{\Delta}\left(f\left(E,\varepsilon_F\right)-f\left(E,\varepsilon_F-V_D\right)\right)|E||E-V_G|T_{WKB2}dE+\int_{\Delta}^{\infty}\left(f\left(E,\varepsilon_F\right)-f\left(E,\varepsilon_F-V_D\right)\right)|E||E-V_G|dE \tag{6.14}$$

Compared to the schematic of interlayer tunnel transistor shown in Fig. 6.1, the top conductive layer material represents the drain whereas the bottom conductive layer material represents the source. The total tunneling probability is integrated over the distance, x along the thickness of the tunneling barrier, d. This can be translated along the Y-axis (O-Y direction) as shown in Fig. 6.1. For the graphene/hBN/graphene heterostructure system, Δ is 1.5eV between the graphene valence band and hBN valence band and m^* is $0.5m_o$ inside the hBN [2]. The magnitude of 'd' depends on the number of the hBN layers considered between the top and bottom graphene layers [5].

For a fixed Δ and m^*, the number of hBN layers control the tunneling current. Hence, the corresponding subthreshold slope also changes as the number of hBN layer changes. The generic model developed for graphene/hBN/graphene in this chapter has been studied for different dielectric thicknesses. Using the expressions of energy dependent tunneling probability through Eq. (6.10) to Eq. (6.12), numerically computed tunneling drain current with and without density of states prefactors are shown in Fig. 6.3 for d = 15 nm. Based on the I_d - V_{GS} curve obtained in Fig. 6.3, both the energy dependent and energy independent current shows poor subthreshold slopes compared to the thermionic limit. From this calculation, it becomes evident again that irrespective of the energy dependent calculation, the subthreshold slope of interlayer tunnel transistors will remain higher than the thermionic limit of 60 mV/decade. Hence, the assumption obtained in the previous section through Eq. (6) agrees with the I_d - V_{GS} curves in Fig. 6.3. It should be observed from Fig. 6.3 significantly low drain current for d = 15 nm. The standard expression of subthreshold slope, with detail derivation in Appendix - 6.1, for an interlayer tunnel transistor with drain current, I_D and V_{GS} can be written as follows [15]:

$$SS = (\ln 10)\left| I_D \left(\frac{dI_D}{dV_{GS}} \right)^{-1} \right| \tag{6.15}$$

From Eq. (6.7), we obtain,

$$\frac{I_D}{\frac{dI_D}{dV_{GS}}} = \frac{\int dE DoS_B(E) DoS_T(E - qV_{GS}) T_{WKB}(f_T - f_B)}{\frac{d}{dV_{GS}} \int dE DoS_B(E) DoS_T(E - qV_{GS}) T_{WKB}(f_T - f_B)} \tag{6.16}$$

which can be further simplified to the following form,

$$\frac{I_D}{\frac{dI_D}{dV_{GS}}} = \frac{T_{WKB}}{\frac{dT_{WKB}}{dV_{GS}}} \tag{6.17}$$

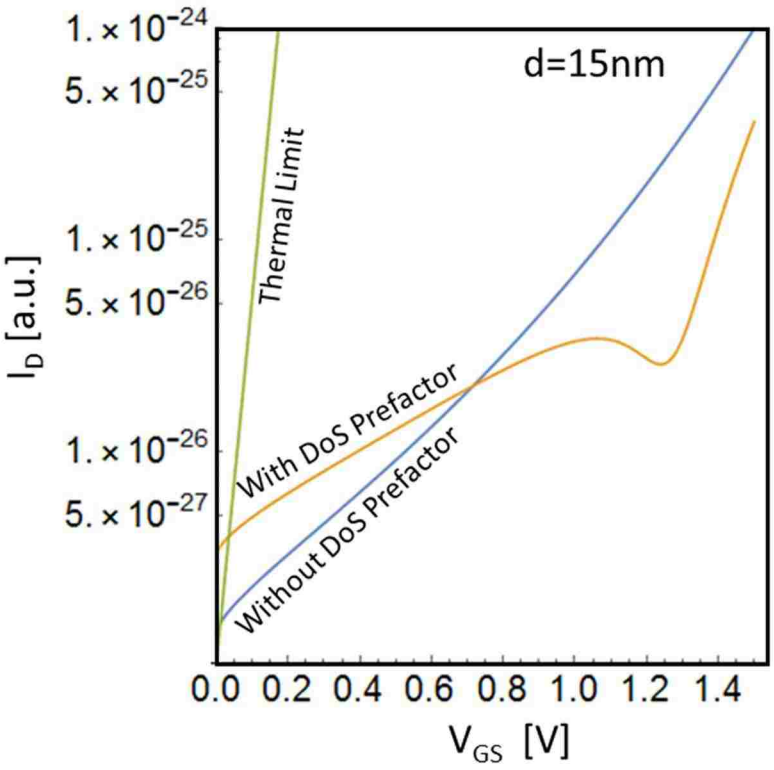


Figure 6.3: I_D - V_{GS} characteristics considering with and without density of states prefactors for d =15 nm tunneling barrier thickness. Note, a.u. refers to arbitrary unit.

From Eq. (6.15) and Eq. (6.17), it is evident that the estimation of subthreshold slope is mostly dependent on the derivative of T_{WKB}. The expression of Eq. (6.8) for T_{WKB} is energy independent with the integration limit ranging in terms of tunneling barrier thickness. However, for appropriate estimation of tunneling probability, drain current and subthreshold slope, energy dependent expression of tunneling probability is necessary. For this reason, the barrier thickness dependent expression of T_{WKB} requires to be modified by incorporating energy dependence. In order to include energy dependence, we consider the following method.

$$\text{Let } \frac{xqV_{GS}}{d} = E \tag{6.18}$$

$$\text{Therefore, } dE = \frac{qV_{GS}dx}{d} \tag{6.19}$$

$$\text{and } dx = \frac{d}{qV_{GS}}dE \tag{6.20}$$

Considering the total tunneling barrier height Δ for the total tunneling barrier thickness d, the relation between Δ and d can be obtained using Eq. (6.18). At $x=0$, $E=0$ and at $x=d$, $E=\Delta$. Then, the expression of T_{WKB} in Eq. (6.8) can be written as follows:

$$T_{WKB} = \exp\left(-\frac{2\sqrt{2m^*}}{\hbar}\int_0^{qV_{GS}}\frac{d}{qV_{GS}}dE\sqrt{\Delta - E}\right) \tag{6.21}$$

$$T_{WKB} = \exp\left(-\frac{2d\sqrt{2m^*}}{\hbar qV_{GS}}\int_0^{qV_{GS}}dE\sqrt{\Delta - E}\right) \tag{6.22}$$

$$T_{WKB} = \exp\left(-\frac{2d\sqrt{2m^*}}{\hbar qV_{GS}}\left(-\frac{2}{3}\left(-\Delta^{3/2} + \Delta\sqrt{\Delta - qV_{GS}} - qV_{GS}\sqrt{\Delta - qV_{GS}}\right)\right)\right) \tag{6.23}$$

$$T_{WKB} = \exp\left(-\frac{4d\sqrt{2m^*}}{3\hbar qV_{GS}}\left(\Delta^{3/2} - \Delta\sqrt{\Delta - qV_{GS}} + qV_{GS}\sqrt{\Delta - qV_{GS}}\right)\right) \tag{6.24}$$

$$T_{WKB} = \exp\left(-\frac{4d\sqrt{2m^*}}{3\hbar qV_{GS}}\left(\Delta^{3/2} - \left(\Delta - qV_{GS}\right)\left(\sqrt{\Delta - qV_{GS}}\right)\right)\right) \tag{6.25}$$

$$T_{WKB} = \exp\left(-\frac{4d\sqrt{2m^*}}{3\hbar q V_{GS}} \left(\Delta^{3/2} - \left(\Delta - qV_{GS} \right)^{3/2} \right) \right) \tag{6.26}$$

$$T_{WKB} = \exp\left(-\frac{4d\sqrt{2m^*}}{3\hbar} \left(\frac{\Delta^{3/2} - \left(\Delta - qV_{GS} \right)^{3/2}}{qV_{GS}} \right) \right) \tag{6.27}$$

Considering the expression of T_{WKB} as shown in Eq. (27), Eq. (17) can be expressed as follows:

$$\frac{T_{WKB}}{\frac{dT_{WKB}}{dV_{GS}}} = \frac{T_{WKB}}{\frac{d}{dV_{GS}} \exp\left(-\frac{4d\sqrt{2m^*}}{3\hbar} \left(\frac{\Delta^{3/2} - \left(\Delta - qV_{GS} \right)^{3/2}}{qV_{GS}} \right) \right)} \tag{6.28}$$

$$\frac{T_{WKB}}{\frac{dT_{WKB}}{dV_{GS}}} = \frac{1}{-\frac{4d\sqrt{2m^*}}{3\hbar} \frac{d}{dV_{GS}} \left(\frac{\Delta^{3/2} - \left(\Delta - qV_{GS} \right)^{3/2}}{qV_{GS}} \right)} \tag{6.29}$$

$$\frac{T_{WKB}}{\frac{dT_{WKB}}{dV_{GS}}} = \frac{-3\hbar}{4d\sqrt{2m^*} \left(\frac{\frac{3}{2} q^2 V_{GS} \sqrt{\left(\Delta - qV_{GS} \right)} - q\left(\Delta^{3/2} - \left(\Delta - qV_{GS} \right)^{3/2} \right)}{\left(qV_{GS} \right)^2} \right)} \tag{6.30}$$

$$\frac{T_{WKB}}{\frac{dT_{WKB}}{dV_{GS}}} = \frac{-3\hbar q V_{GS}^2}{4d\sqrt{2m^*} \left(\sqrt{\left(\Delta - qV_{GS} \right)} \left(\Delta + \frac{1}{2} qV_{GS} \right) - \Delta^{3/2} \right)} \tag{6.31}$$

$$\frac{T_{WKB}}{\frac{dT_{WKB}}{dV_{GS}}} = \frac{-3\hbar V_{GS}^2}{4d\sqrt{2m^* q} \left(\sqrt{\left(\frac{\Delta}{q} - V_{GS} \right)} \left(\frac{\Delta}{q} - \frac{V_{GS}}{2} \right) - \left(\frac{\Delta}{q} \right)^{3/2} \right)} \tag{6.32}$$

Expression (6.17) can be now expressed as follows:

$$\frac{I_D}{\frac{dI_D}{dV_{GS}}} = \frac{3\hbar V_{GS}^2}{4d\sqrt{2m^* q} \left(\sqrt{\left(\frac{\Delta}{q} - V_{GS} \right)} \left(\frac{\Delta}{q} - \frac{V_{GS}}{2} \right) - \left(\frac{\Delta}{q} \right)^{3/2} \right)} \tag{6.33}$$

Combining Eq. (6.33) with Eq. (6.15), the expression of subthreshold slope of the vertical interlayer tunnel transistor can be written as follows:

$$SS = \left(\ln 10\right)\left|\frac{3\hbar V_{GS}^{2}}{4d\sqrt{2m^{*}q}\left(\sqrt{\left(\frac{\Delta}{q}-V_{GS}\right)}\left(\frac{\Delta}{q}-\frac{V_{GS}}{2}\right)-\left(\frac{\Delta}{q}\right)^{3/2}\right)}\right| \tag{6.34}$$

6.4 Results Comparison and Discussion

Using Eq. (6.34), the subthreshold slope of graphene/hBN/graphene vertical interlayer tunnel transistor is plotted in Fig. 6.4 for $m^{*}= 0.5m_o$, Δ = 1.5 eV and different tunneling barrier thicknesses. For a very thin tunneling barrier (three layers, d = 1.02 nm), the wave function from one graphene layer easily penetrates through the thin barrier to the other graphene layer due to negligible coherent length of tunneling [21]. A strong Coulomb drag also becomes dominant in such multilayer heterostructures [22]. Combining both the effects of wave function extension and Coulomb drag, an off-state leakage current flows between the two graphene layers resulting in a high subthreshold slope at the reduced number of hBN layers or thin tunnel barrier. However, the combined effects are screened out as the thickness of the tunneling barrier increases and as well as the coherent length of tunneling increases with an increased number of hBN layers. Thus, a reduced subthreshold slope is observed at a higher number of hBN layers or thick tunneling barrier. In Fig. 6.4(a), for V_{GS} = 1.5 V, the subthreshold slope remains greater than 500 mV/decade which gets improved as the tunneling barrier thickness (d) is further increased. For d = 2.38 nm or 7 layers of hBN, the subthreshold slope decreases to 250 mV/decade, which is still far greater than the thermionic limit of 60 mV/decade.

As the tunneling barrier thickness is further increased to 5 nm, 10 nm and 15 nm as shown in Fig. 6.4(b), the subthreshold slope also decreases. However, none of the plotted curves of the calculated subthreshold slopes go below 60 mV/decade except for the tunneling barrier at

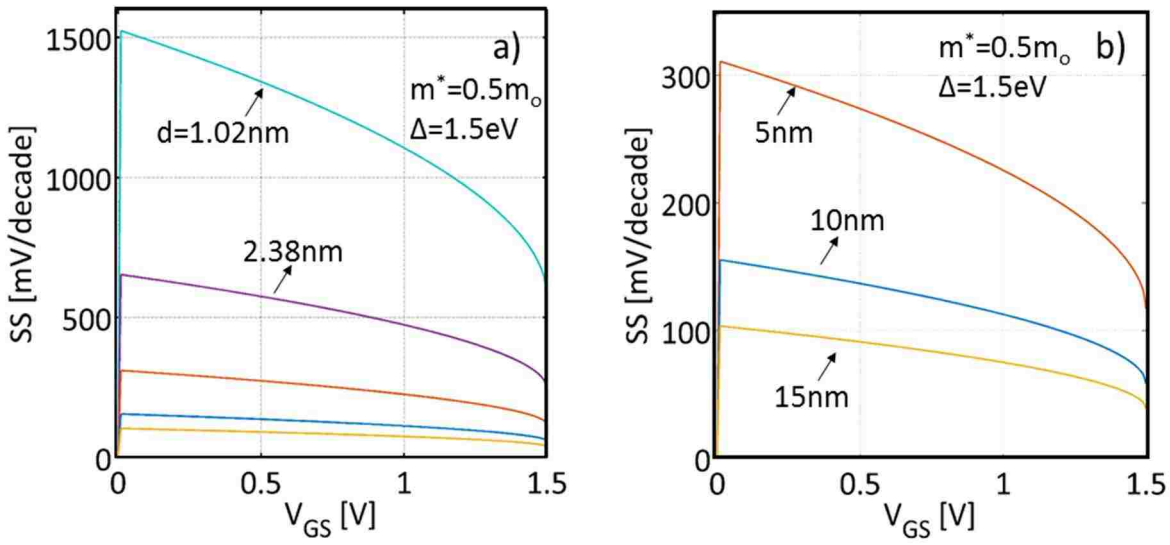


Figure 6.4: a) Estimation of subthreshold slope (SS) in an interlayer tunnel transistor for different tunneling barrier thicknesses, d with V_{GS} dependence and b) for 5 nm, 10 nm and 15 nm tunneling barrier thicknesses.

unrealistically large thickness (e.g. d = 15 nm) at V_{GS} = 1.5 V. Although, it seems promising that the theoretical assumption of subthreshold slope of interlayer tunnel transistor can go below 60 mV/decade at a higher tunneling barrier thickness, the earlier estimated current from the numerical calculations prove that at such a thick tunneling barrier (d = 15 nm), the drain current is extremely low even at a higher gate bias (V_{GS} = 1.5 V) as shown in Fig. 6.3. Such unrealistically small drain current shows no practical use of interlayer tunnel transistors for digital, analog or high speed applications and the subthreshold slopes of interlayer tunnel transistors cannot go down below the thermionic limit of 60 mV/decade in a working transistor. Table 6.1 shows a comparison of computed subthreshold slope in this work with the earlier reported work in [8, 9]. Fiori et al. [8] studied computationally graphene/hBN/graphene heterostructure with a 4 nm HfO_2 as gate dielectric for seven layers of hBN and a tunneling bias of 0.5 V, and calculated a subthreshold slope of 350 mV/decade. The computed value of the subthreshold slope in [8] is lower than the computed value of 456 mV/decade obtained through this work due to superior electrostatic gate control over the channel. Moreover, Fiori et al. [8] predicted that a thin HfO_2 gate dielectric could reduce the subthreshold slope. Nevertheless, the assumption of higher subthreshold slope than the thermionic limit of 60 mV/decade for interlayer tunnel transistor in [8] matches with the computation performed in this work.

Considering 300 nm SiO_2 top gate oxide, Ghobadi and Pourfath [9] also computed a subthreshold slope of 1534 mV/decade for three layers of hBN for a similar graphene/hBN/graphene heterostructure. Computed subthreshold slope for 5 and 7 layers of hBN are on higher side in comparison to their subthreshold data which differs from the model in this chapter due to electrostatic gate control with low-κ dielectric and high oxide thickness. The trend in decrease of subthreshold slope at higher tunneling barrier thickness can also be observed in

Table 6.1

Comparison of subthreshold slope in this work with the earlier reported interlayer tunnel transistors

Reference	#hBN layers	V_{GS} (V)	*SS* (mV/decade)	*SS* in this work (mV/decade)
Ref [8]	7	0.5	350	456
Ref [9]	3	0.5	1534	1342
Ref [9]	5	0.5	558	805
Ref [9]	7	0.5	198	575

the subthreshold slope model derived in this work, which supports the computational model of this chapter.

Compared to the work of Fiori et al. [8] and Ghobadi and Pourfath [9], Roy et al. [10] demonstrated improved performance in similar graphene/ hBN/graphene heterostructure for the CVD grown graphene. However, the work in [10] not only considers few layers hBN but also includes a 2 nm of TiO_x seeding layer along with the few layers of hBN and 10 nm HfO_2 as the gate dielectric (x = 0.6-0.75) [10]. Since the tunneling barrier is not fully hBN based, the model here does not consider any comparison with the work of Roy et al. [10].

Equation (6.15) of the subthreshold slope is different than Eq. (6.3). The derived subthreshold slope model in Eq. (6.15) has '*ln*' in the numerator instead of a '$\log_{10}$' in the denominator as in Eq. (6.3). Based on the assumption from Eq. (6.17), that the subthreshold slope depends on the derivative of T_{WKB}, the subthreshold slope from Eq. (6.3) can be modified as follows:

$$SS = \left[\frac{d \log_{10}\left(T_{WKB}\right)}{dV_{GS}} \right]^{-1} \tag{6.35}$$

Figure 6.5 shows the plot of subthreshold slope computed from Eq. (6.35). Based on the subthreshold slope curves obtained in Fig. 6.5 through the numerical calculations, the calculations obtained here through modified subthreshold slope model matches very well. Both Fig. 6.4(b) and Fig. 6.5 show similar results which implies that irrespective of the difference in subthreshold slope models, interlayer tunnel transistor cannot provide sub-thermionic current transport. Nevertheless, the promise of such interlayer tunnel transistors can be found for high frequency applications [24, 25].

Compared to MoS_2 (E_G = 1.8 eV) and WS_2 (E_G = 1.4 eV) which are wide band gap semiconductors, hBN (E_G = 6 eV) is a wide band gap insulator. The hBN provides a large

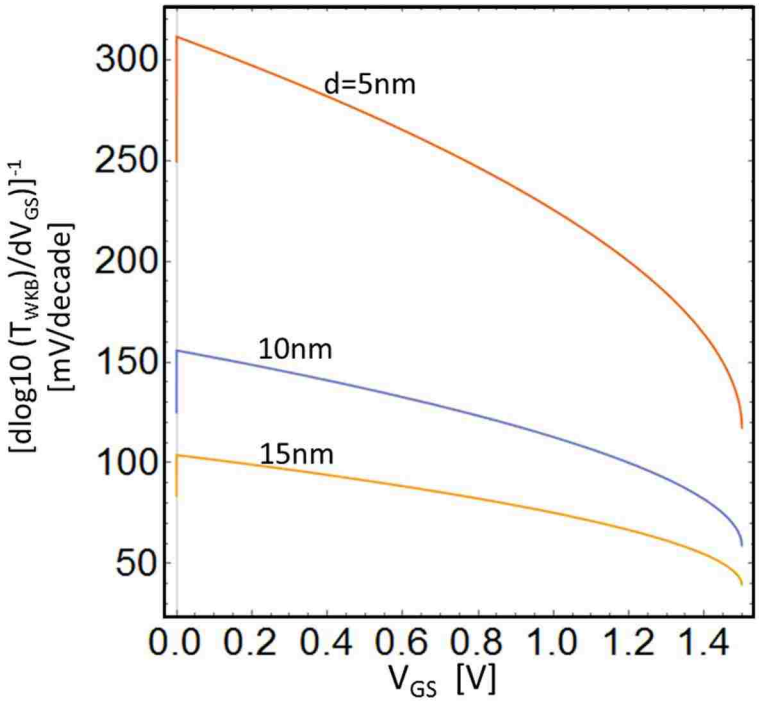


Figure 6.5: Subthreshold slope computed from Eq. (6.35) for different V_{GS} and different tunneling barrier thicknesses.

screening effect due to a large tunneling barrier height and controls the source-drain interlayer tunneling transport. For this reason a large subthreshold slope is obtained for graphene/hBN/graphene heterostructure. Compared to hBN, the energy band gap of MoS_2 and WS_2 is less, thus providing a small tunneling barrier height. Hence, subthreshold slopes obtained by using MoS_2 and WS_2 as a tunneling barrier are lower than the one obtained with hBN. The lattice mismatch of hBN to graphene is 1.7% which provides an improved interlayer tunneling transport [23]. Due to low lattice mismatch of hBN with graphene, the work in this chapter primarily considers hBN as the tunneling barrier as compared to MoS_2 and WS_2 materials.

Georgiou et al. [3] proposed that the subthreshold slope of the interlayer tunnel transistor is not limited by the thermionic limit of 60 mV/decade. However, the assumption was neither validated experimentally nor by any theoretical or numerical computation. Based on the analytical subthreshold slope model, which matches with the numerical computation carried in this chapter, the subthreshold slope of interlayer tunnel transistor is limited by the thermionic limit and cannot go down below 60 mV/decade for the ultra-thin tunneling barrier. Theoretically, a lower subthreshold slope can be obtained at unrealistically large (~15 nm) tunneling barrier, that possibility becomes unacceptable due to impractically low drain current thereby making interlayer tunnel transistor to be non-operational. Following the experimental work in [11], earlier similar reports of twisted graphene interlayer tunnel transistors [7, 26-27] have also predicted similar resonant tunneling currents at the compromise of high subthreshold slope which is also observed in the computation enumerated in this section.

6.5 Conclusion

A physics based analytical model has been derived for calculating the subthreshold slope of the graphene vertical interlayer tunnel transistor. Similar to a Schottky barrier FET and lateral

barrier graphene tunnel FET, the subthreshold slope of interlayer tunnel transistor cannot go below the thermionic limit of 60 mV/decade. The compact subthreshold slope model which matches with the numerical computation can accurately predict subthreshold slope of the interlayer tunnel transistor. With suitable choice of tunneling barrier height, carrier effective mass and tunneling bias, the subthreshold slope can reach the limit of 60mV/decade with superior electrostatic gate control and free of defects, impurities and scattering. Such novel interlayer tunnel transistors show a great promise for THz and plasmonic applications. Nevertheless, in order to make graphene based transistors suitable for logic applications, novel current transport in a novel device structure is required.

Appendix-6.1

Standard expression of subthreshold slope can be written as follows [18]:

$$SS = \frac{dV_{GS}}{d(\log_{10} I_D)} \tag{A6.1}$$

$$SS = \left(\frac{d(\log_{10} I_D)}{dV_{GS}} \right)^{-1} \tag{A6.2}$$

Using standard differential rule for logarithm,

$$SS = \left(\frac{1}{I_D \ln 10} . \frac{dI_D}{dV_{GS}} \right)^{-1} \tag{A6.3}$$

Which can be written for the absolute values as follows:

$$SS = (\ln 10) \left| I_D \left(\frac{dI_D}{dV_{GS}} \right)^{-1} \right| \tag{A6.4}$$

6.6 References

[1] F. Schwierz, "Graphene transistors," *Nat Nano,* vol. 5, pp. 487-496, 2010.

[2] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, A. K. Geim, K. S. Novoselov, and L. A. Ponomarenko, "Field-effect tunneling transistor based on vertical graphene heterostructures," *Science,* vol. 335, pp. 947-950, 2012

[3] T. Georgiou, R. Jalil, B. D. Belle, L. Britnell, R. V. Gorbachev, S. V. Morozov, Y.-J. Kim, A. Gholinia, S. J. Haigh, O. Makarovsky, L. Eaves, L. A. Ponomarenko, A. K. Geim, K. S. Novoselov, and A. Mishchenko, "Vertical field-effect transistor based on graphene-WS_2 heterostructures for flexible and transparent electronics," *Nat. Nano,* vol. 8, pp. 100-103, 2013.

[4] R. M. Feenstra, D. Jena, and G. Gu, "Single-particle tunneling in doped graphene-insulator-graphene junctions," *J. of App. Phys.,* vol. 111, pp. 043711, 2012.

[5] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, M. I. Katsnelson, L. Eaves, S. V. Morozov, A. S. Mayorov, N. M. R. Peres, A. H. Castro Neto, J. Leist, A. K. Geim, L. A. Ponomarenko, and K. S. Novoselov, "Electron tunneling through ultrathin boron nitride crystalline barriers," *Nano Lett.,* vol. 12, pp. 1707-1710, 2012.

[6] S. Kang, B. Fallahazad, L. Kayoung, H. Movva, K. Kyounghwan, C. M. Corbet, T. Taniguchi, K. Watanabe, L. Colombo, L. F. Register, E. Tutuc, and S. K. Banerjee, "Bilayer graphene-hexagonal boron nitride heterostructure negative differential resistance interlayer tunnel FET," *IEEE Elect. Dev. Lett.,* vol. 36, pp. 405-407, 2015.

[7] P. Zhao, R. M. Feenstra, G. Gong, and D. Jena, "SymFET: a proposed symmetric graphene tunneling field-effect transistor," *IEEE Trans. Elect. Dev.,* vol. 60, pp. 951-957, 2013.

[8] G. Fiori, S. Bruzzone, and G. Iannaccone, "Very large current modulation in vertical heterostructure graphene/hBN transistors," *IEEE Trans. Elect. Dev.,* vol. 60, pp. 268-273, 2013.

[9] N. Ghobadi and M. Pourfath, "A comparative study of tunneling FETs based on graphene and GNR heterostructures," *IEEE Trans. Elect. Dev.,* vol. 61, pp. 186-192, 2014.

[10] T. Roy, L. Liu, S. de la Barrera, B. Chakrabarti, Z. R. Hesabi, C. A. Joiner, R. M. Feenstra, G. Gu, and E. M. Vogel, "Tunneling characteristics in chemical vapor deposited graphene–hexagonal boron nitride–graphene junctions," *App. Phys. Lett.,* vol. 104, p. 123506, 2014.

[11] A. Mishchenko, J. S. Tu, Y. Cao, R. V. Gorbachev, J. R. Wallbank, M. T. Greenaway, V. E. Morozov, S. V. Morozov, M. J. Zhu, S. L. Wong, F. Withers, C. R. Woods, Y. J. Kim, K. Watanabe, T. Taniguchi, E. E. Vdovin, O. Makarovsky, T. M. Fromhold, V. I. Fal'ko, A. K. Geim, L. Eaves, and K. S. Novoselov, "Twist-controlled resonant tunneling in graphene/boron nitride/graphene heterostructures," *Nat. Nano,* vol. 9, pp. 808-813, 2014.

[12] B. Fallahazad, K. Lee, S. Kang, J. Xue, S. Larentis, C. Corbet, K. Kim, H. C. P. Movva, T. Taniguchi, K. Watanabe, L. F. Register, S. K. Banerjee, and E. Tutuc, "Gate-tunable

resonant tunneling in double bilayer graphene heterostructures," *Nano Lett.,* vol. 15, pp. 428-433, 2015.

[13] M. Fahad and A. Srivastava, "A graphene switching transistor for vertical circuit design," *ECS J. of Solid State Sci. and Tech.,* vol. 5, pp. M13-M21, 2016.

[14] A. Srivastava and M. S. Fahad, "Vertical MoS2/hBN/MoS2 interlayer tunneling field effect transistor," *Solid-State Elect*, vol. 126, pp. 96-103, 2016.

[15] J. Appenzeller, Y. M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Phys. Rev. Lett.,* vol. 93, p. 196805, 2004.

[16] D. Sarkar, X. Xie, W. Liu, W. Cao, J. Kang, Y. Gong, S. Kraemer, P. Ajayan and K. Banerjee "A subthermionic tunnel field-effect transistor with an atomically thin channel," *Nature*, vol. 526, pp. 91-95, 2015.

[17] W. G. Vandenberghe, A. S. Verhulst, B. Sorée, W. Magnus, G. Groeseneken, Q. Smets, M. Heyns and M. V. Fischetti, "Figure of merit for and identification of sub-60 mV/decade devices," *Appl Phys Lett*. vol. 102, pp. 013510, 2013.

[18] D. A. Svintsov, V. V. Vyurkov, V. F. Lukichev, A. A. Orlikovsky, A. Burenkov, and R. Oechsner, "Tunnel field-effect transistors with graphene channels," *Semiconductors*, vol. 47, pp. 279-284, 2013.

[19] Q. Zhang, W. Zhao, and A. Seabaugh, "Low-subthreshold-swing tunnel transistors," *IEEE Elect. Dev. Lett.,* vol. 27, pp. 297-300, 2006.

[20] M. S. Fahad, A. Srivastava, A. K. Sharma, and C. Mayberry, "Analytical current transport modeling of graphene nanoribbon tunnel field-effect transistors for digital circuit design," *IEEE Trans. on Nanotech.,* vol. 15, pp. 39-50, Jan 2016.

[21] A. Sciambi, M. Pelliccione, M. P. Lilly, S. R. Bank, A. C. Gossard, L. N. Pfeiffer, K. W. West, and D. Goldhaber-Gordon, "Vertical field-effect transistor based on wave-function extension," *Phys. Rev. B,* vol. 84, p. 085301, 2011.

[22] R. V. Gorbachev, A. K. Geim, M. I. Katsnelson, K. S. Novoselov, T. Tudorovskiy, I. V. Grigorieva, A. H. MacDonald, S. V. Morozov, K. Watanabe, T. Taniguchi, and L. A. Ponomarenko, "Strong coulomb drag and broken symmetry in double-layer graphene," *Nat. Phys,* vol. 8, pp. 896-901, 2012.

[23] G. Giovannetti, P. A. Khomyakov, G. Brocks, P. J. Kelly, and J. van den Brink, "Substrate-induced band gap in graphene on hexagonal boron nitride: Ab initio density functional calculations," *Physical Review B*. vol. *76*, pp. 073103. 2007.

[24] D. Svintsov, T. Otsuji, V. Mitin, M. S. Shur, and V. Ryzhii, "Negative terahertz conductivity in disordered graphene bilayers with population inversion," *Applied Physics Letters,* vol. 106, pp. 113501. 2015.

[25] D. Svintsov, V. G. Leiman, V. Ryzhii, T. Otsuji, and M. S. Shur, "Graphene nanoelectromechanical resonators for the detection of modulated terahertz radiation," *Journal of Physics D: Applied Physics,* vol. 47, pp. 505105, 2014.

[26] L. Brey, "Coherent tunneling and negative differential conductivity in a graphene/hBN/graphene heterostructure," *Phys. Rev. Appl*. Vol. 2, pp. 014003, 2014.

[27] S. C. de la Barrera, Q. Gao, and R. M. Feenstra, "Theory of graphene–insulator–graphene tunnel junctions," *Jour. of Vac. Sci. & Tech. B*. vol. 32, pp. 04E101, 2014.

CHAPTER 7*

GRAPHENE TUNNEL TRANSISTOR BASED INTEGRATED CIRCUIT DESIGN

7.1 Introduction

With the compelling thrust for energy efficient memory design for next generation internet of things and big data platform, field effect transistors based on planar band-to-band tunneling have attracted great interest recently due to its potential to operate at sub-60 mV/decade subthreshold swing at very low voltage [1]. Compared to conventional bulk three dimensional material systems (Si, Ge, GaAs, InAs), atomically thin two dimensional materials have also been studied for the design of such emerging tunnel field-effect transistors (TFETs) [2], promise of which has already been discussed in the previous chapters. Graphene nanoribbon, the quantum confined one dimensional form of graphene, is one of the extensively studied materials for TFETs. Numerical simulations and analytical models have shown the promise of GNR TFET for low power circuit design [3, 4]. Moreover, the modeling of graphene junctionless tunnel effect transistor (JTET) has also shown promise for energy efficient integrated circuit design for next generation more than Moore's applications.

However, in order to study the GNR TFET and graphene JTET circuit level applicability, SPICE compatible model is required. Since majority of the commercially available SPICE simulators depend on library models such as BSIM or EKV3, GNR TFETs cannot be simulated with these conventional SPICE simulators. In this regard, high level hardware description

---

*Part of this work is reported in the following publication:
M. S. Fahad, Z. Zhao, A. Srivastava and L. Peng., "Modeling of GNR TFET in Verilog-A for digital circuit design," Proc. of 2nd IEEE Computer Society Int. Sym. on Nanoelectronics and Information Science (iNIS), Gwalior, India, 2016, pp. 1-5.

language such as Verilog-A provides an efficient and accurate way of simulating emerging devices which do not have SPICE level models. Verilog-A is a simple and straightforward way which facilitates the encoding of mathematical expressions describing the device physics of the emerging devices like TFETs and JTETs [5]. Since research of compact modeling of tunnel transistor is still under progress, Verilog-A is the tool which can be used very effectively for studying the circuit level performance of tunnel transistors prior to synthesis of very large scale integration (VLSI) design. Numerous approaches have been undertaken to study the circuit level performance of GNR TFETs for both digital and analog circuit design and competitive performances are obtained. Being novel in terms of device structure and operation, Verilog-A also helps efficiently for JTET based logic and memory integrated circuit design, which is also discussed in detail along with GNR TFET in this chapter.

A universal analytic model of InGaSb/InAs TFET from Lu et al. [6] have been studied using Verilog-A, however, the simulation considers a look-up table based approach which does not meet the criteria of standard electronic design automation (EDA). Yang et al. [2] reported a GNR TFET circuit design which depends largely on the quantum transport based device simulation and look-up table based Verilog-A approach. Compared to look-up table based simulation approach, physics based analytical current transport models are also required to be validated by numerical quantum transport simulation prior to their Verilog-A implementation.

In this chapter, modeling of GNR TFET and graphene JTET based digital logic inverter in Verilog-A are discussed through Mentor Graphics® Tanner EDA S-Edit and T-Spice circuit simulation. Details of the compact models of GNR TFET and graphene JTET are provided in Chapter 3 and 4, respectively, and not repeated here.

7.2 Modeling in Verilog-A

Since conventional CMOS SPICE simulators are unable to provide simulation of emerging devices such as GNR TFET or JTET, and require additional compact models, Verilog-A provides advantage in this regard. The anaytical current transport models discussed in chapter 3 and 4 are written in Verilog-A and compiled in T-Spice. A flow diagram showing different steps to simulate such new devices in Verilog-A is shown in Fig. 7.1. For comparison, the transfer characteristics and output characteristics obtained through the Verilog-A simulations are plotted along with the same obtained from analytical models for both GNR TFET and graphene JTET are shown in Fig. 7.2 and 7.3, respectively. For a 22 nm channel length, GNR TFET of 4.9 nm width and 0.289 eV band gap and graphene JTET having a hBN tunneling barrier thickness of 1.02 nm, transfer and output characteristics are obtaned using Verilog-A simulations which match closely with analytical models. Note, the simulation reported by Yang et al. [3] and analog model reported by Barboni et al. [4] consider look-up table based approach. Compared to both [3] and [4], the Verilog-A simulated GNR TFET and graphene JTET can directly capture the transistor device physics controlling the circuit level performance and thus become more suitable for EDA based design.

7.3 Performance Evaluation of Graphene Tunnel Transistor Inverter

Considering the Verilog-A model of both p- and n- type GNR TFETs, complementary GNR TFET inverter is simulated in Mentor Graphics® Tanner EDA T-Spice. The schematic of the GNR TFET and graphene JTET inverter are shown in Figs. 7.4(a) and Fig. 7.4(b). Corresponding voltage transfer charactertics are shown in Figs. 7.4(c) and 7.4(d), respectively for a supply voltage of 0.3 V. The input, output and delay waveforms are extracted directly from Mentor Graphics® Tanner for 1V supply voltage.

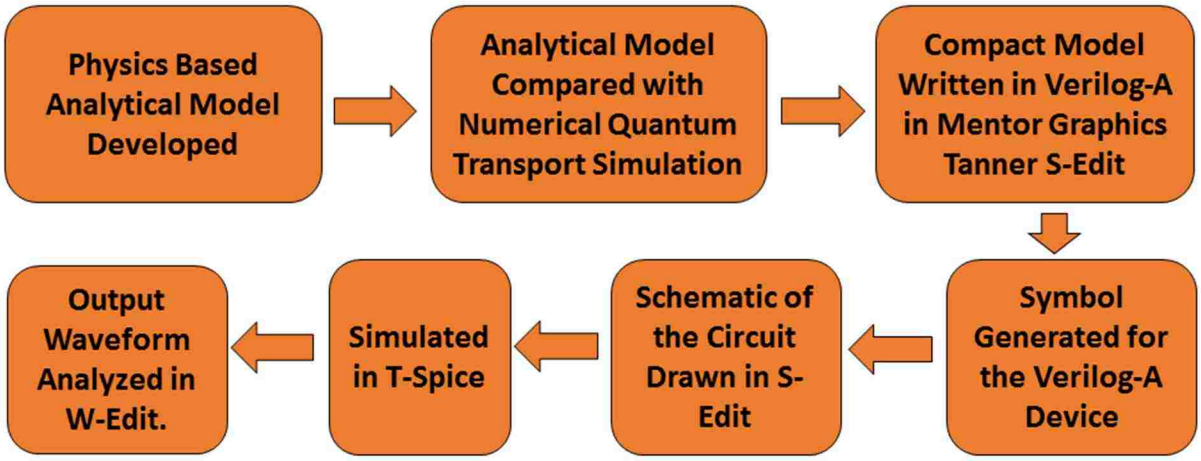


Figure 7.1: Flow chart of simulating emerging new devices using compact analytical current transport models in Verilog-A code through Mentor Graphics® Tanner EDA S-Edit and T-Spice.

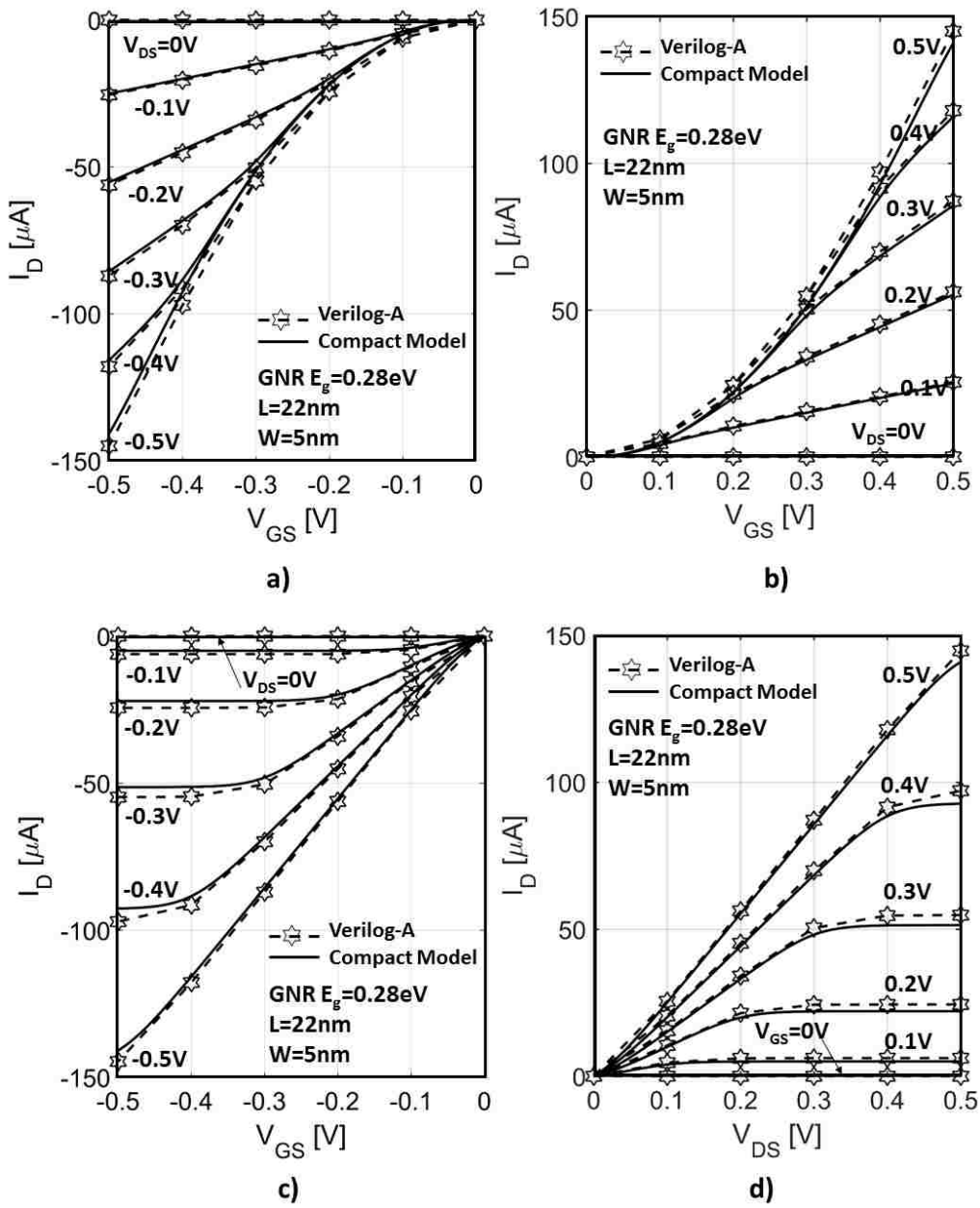


Figure 7.2: Comparison of GNR TFET characteristics obtained from Verilog-A simulation with the analytical current transport model. a) I_D - V_{GS} transfer characteristics for different V_{DS} for p - type GNR TFET, b) I_D - V_{GS} transfer characteristics for different V_{DS} for n - type GNR TFET, c) I_D - V_{DS} output characteristics for different V_{GS} p - type GNR TFET and d) I_D - V_{DS} output characteristics for different V_{GS} n - type GNR TFET.

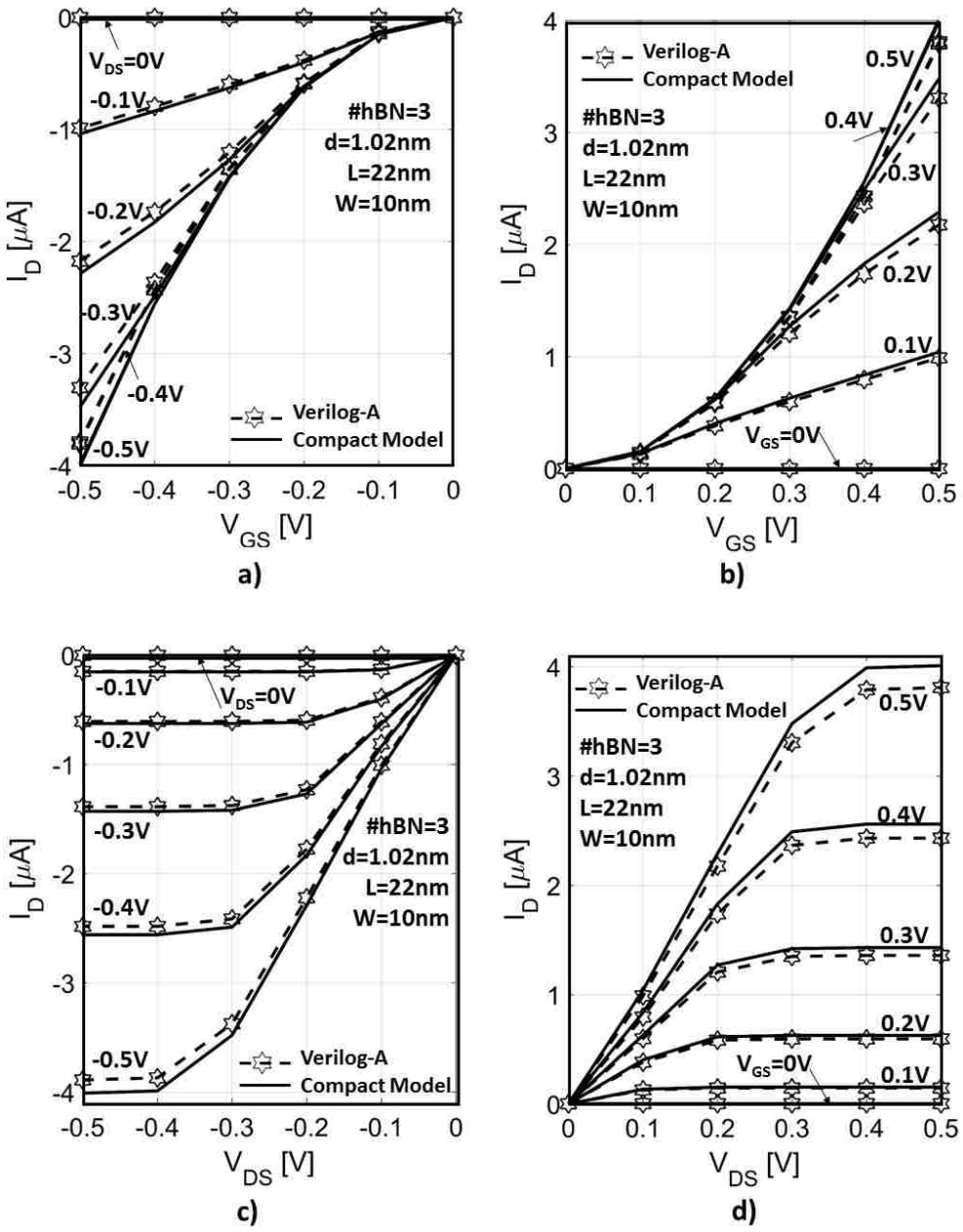


Figure 7.3: Comparison of graphene JTET characteristics obtained from Verilog-A simulation with the analytical current transport model. a) I_D - V_{GS} transfer characteristics for different V_{DS} for p - type graphene JTET, b) I_D - V_{GS} transfer characteristics for different V_{DS} for n - type graphene JTET, c) I_D - V_{DS} output characteristics for different V_{GS} p - type graphene JTET and d) I_D - V_{DS} output characteristics for different V_{GS} n - type graphene JTET.

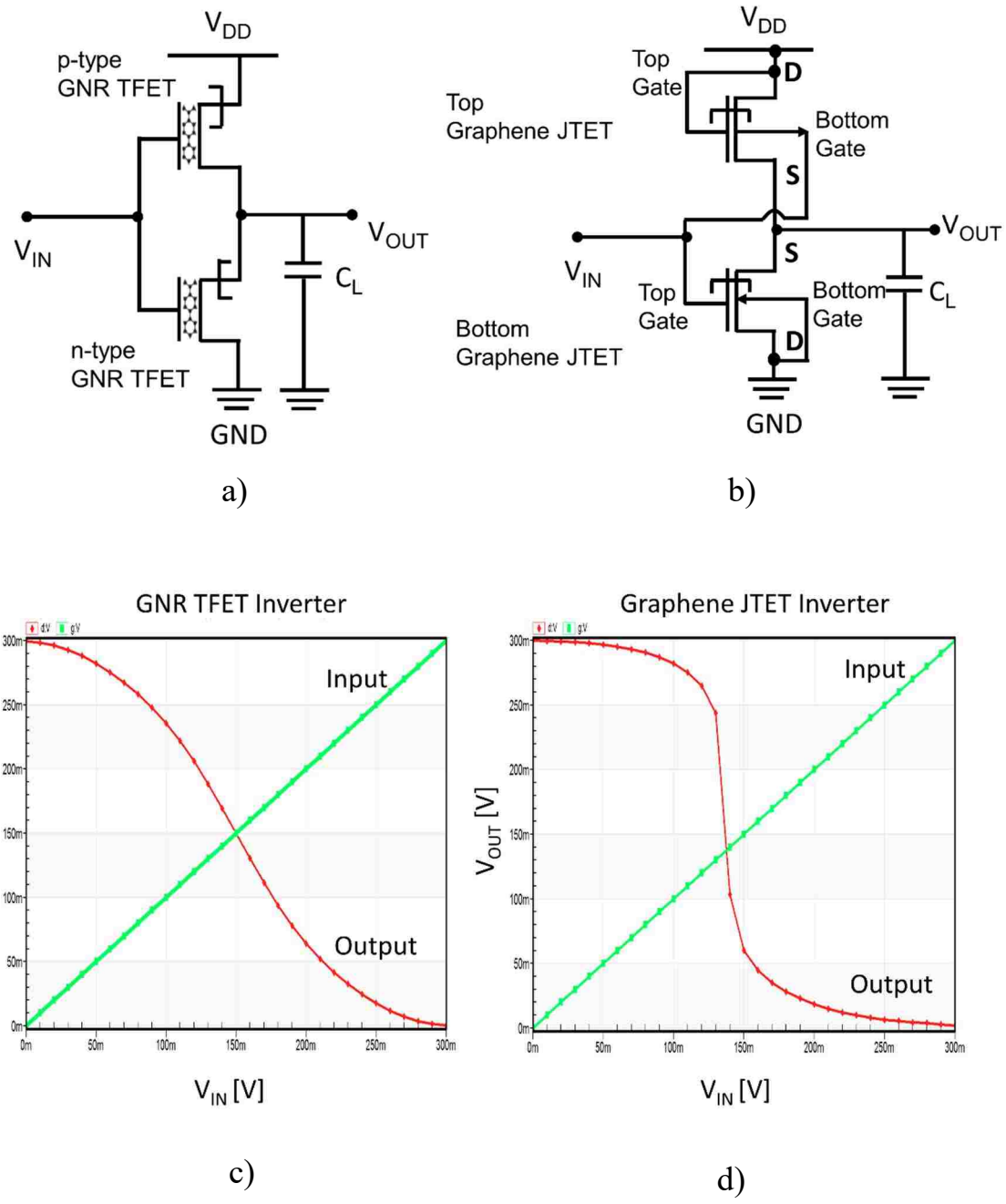


Figure 7.4: a) Schematic of GNR TFET inverter, b) schematic of graphene JTET inverter, c) DC voltage transfer characteristics (VTC) of GNR TFET inverter at a supply voltage of 0.3 V, and d) DC voltage transfer characteristics (VTC) of graphene JTET inverter at a supply voltage of 0.3 V. C_L refers to load capacitance.

EDA W-Edit which are shown in Fig. 7.5(a), 7.5(b) and 7.5(c), respectively. For an input signal of 0.2 GHz with 1ps rise and fall times, the estimated delay of the GNR TFET inverter is ~ 60 ps. Compared to earlier reported GNR TFET inverter delay of 14 ns of Yan et al., [3] for similar GNR width and supply voltage, GNR TFET inverter shows much small delay.

The inverter schematic shown in Fig. 7.4(a) is similar to CMOS technology which has been extensively studied for extraction of different figure of merits of the GNR TFET inverter. The supply voltage and operating frequency variations on the performance of GNR TFET inverter are considered and are shown in Fig. 7.6. Figure 7.6(a) shows the variation of power dissipation with the supply voltage. Under 1.8 V operation, the power dissipation is 47.16 μW and is 2.09 μW for 0.1 V. The trend is approximately linear. In Fig. 7.6(b), the delay is estimated for change in supply voltage. For low supply voltages, maximum delay is observed. This shows that how the supply voltage influences the transmission delay of an inverter. It can be seen that above 0.5 V, the delay is smaller than 10 ps. Even in extremely scaled supply voltage of 0.1 V, the delay is still less than 100 ps. The estimated power dissipation at 1.8 V supply voltage is 47.16 μW, however, the smallest delay as low as 1 ps has been observed in this case. Therefore, a trade-off between delay and power dissipation is required while choosing the supply voltages in GNR TFET inverter. The power dissipation in VLSI circuits is very sensitive to frequency. Figure 7.6(c) shows the relationship between frequency and power dissipation. It shows that the power dissipation of GNR TFET is not very sensitive to frequency. Thus, this study proves that the modeled GNR TFET has extremely fast data transmission, acceptable power dissipation and signal integrity. Hence, it becomes a good candidate for future digital circuit design. For the GNR TFET inverter, it is important to study the effect of frequency with both delay and power dissipation.

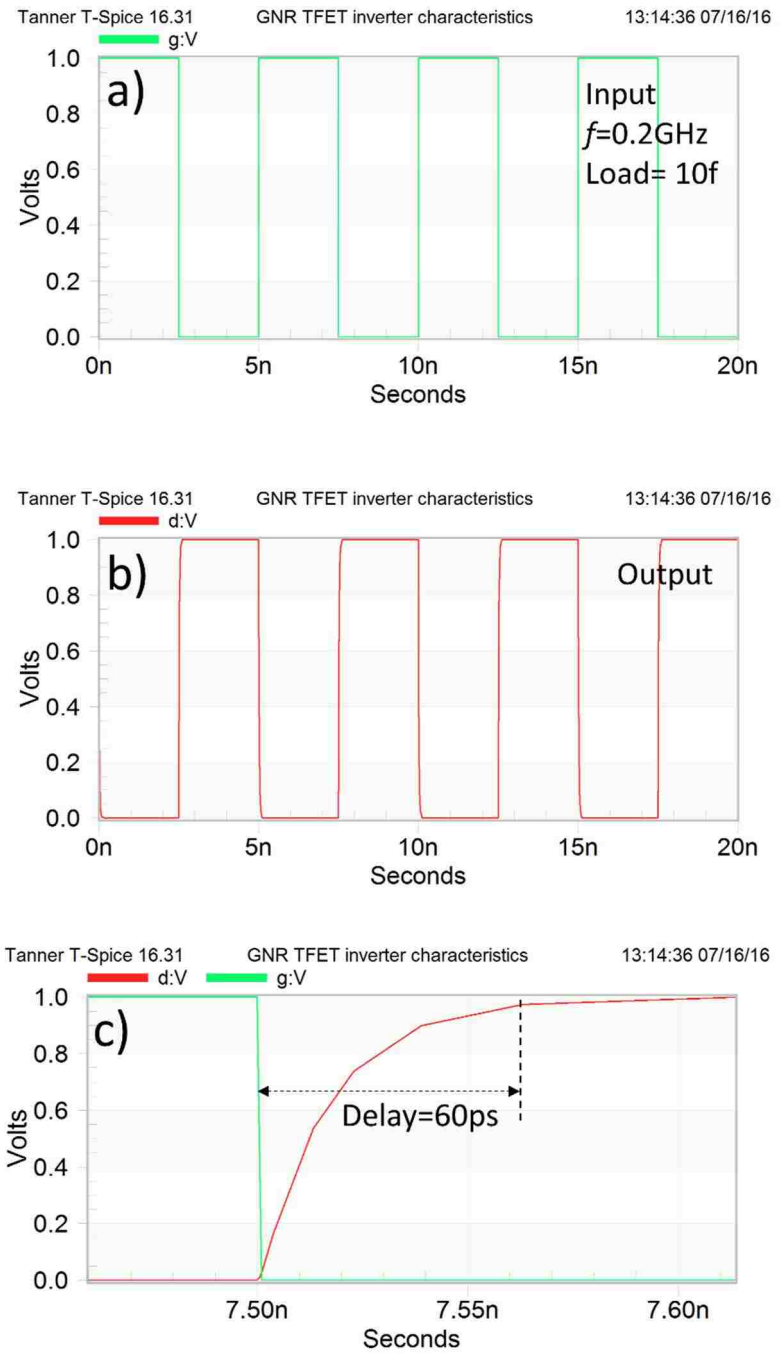


Figure 7.5: GNR TFET transient performance analysis, a) Input square-wave signal at 0.2 GHz, b) obtained output from GNR TFET inverter at 10 fF load capacitance, and c) inverter delay calculation.

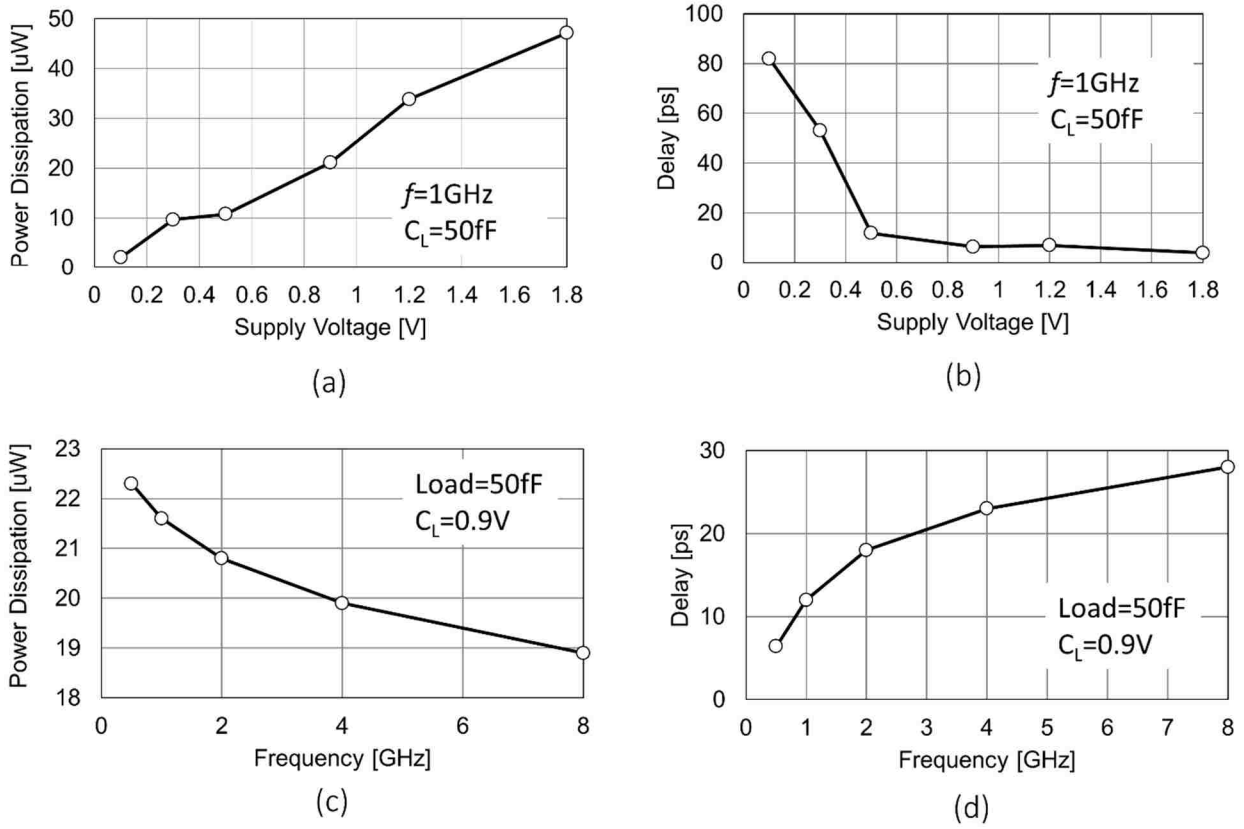


Figure 7.6: a) Relationship between supply voltage and power dissipation for GNR TFET inverter for load capacitance of 50 fF and test frequency of 1 GHz, b) relationship between supply voltage and delay at load capacitance of 50 fF and the test frequency at 1 GHz, c) relationship between operating frequency and GNR TFET inverter power dissipation for load capacitance of 50 fF and the supply voltage of 0.9 V and d) relationship between frequency and delay for 50 fF load capacitance and 0.9 V supply voltage.

Figure 7.6(d) shows the trend of inverter delay with the frequency. The largest delay is 45 ps when the frequency is 4 GHz. Up to 8 GHz, the delay is only around 28 ps which is also within an acceptable range.

The transient analysis of graphene JTET inverter is also investigated and has been provided in Figs. 7.7 (a), 7.7(b), and 7.7(c) for graphene JTET inverter input signal, output signal and delay at a supply voltage of 0.9 V and a load capacitance of 0.001 fF. With a significantly low delay of only 10 ps, graphene JTET inverter provides very fast operation. Note the small load capacitance required for graphene JTET inverter operation due to the dominant quantum capacitance originating from two graphene layers and the hBN tunneling barrier. Similar to GNR TFET inverter performance analysis, graphene JTET inverter has been studied for supply voltage and operating frequency variations and corresponding power dissipation and signal delays are enumerated which are shown in Fig. 7.8. For a fixed load capacitance of 0.001 fF and an operating frequency of 1 GHz, graphene JTET inverter demonstrates very low power dissipation in the nW range as shown in Fig. 7.8(a). With the ITRS recommended roadmap of 1 nW power dissipation for sub-10 nm MOSFET, graphene JTET inverter power dissipation with an increasing supply voltage fulfils ITRS requirement. Note a competitive power dissipation of 48 nW has been obtained even at a supply voltage of 1.2 V. With the increasing supply voltage, a decreasing trend for graphene JTET inverter delay is also observed as shown in Fig. 7.8(b). It is assumed with low supply voltage poor charging and discharging of load capacitance contributes to such high delay which can be resolved at higher supply voltage. Nevertheless, a trade-off between delay and power dissipation at higher supply voltage is required for best graphene JTET inverter operation. Similarly, with the increase in operating frequency at a fixed supply voltage,

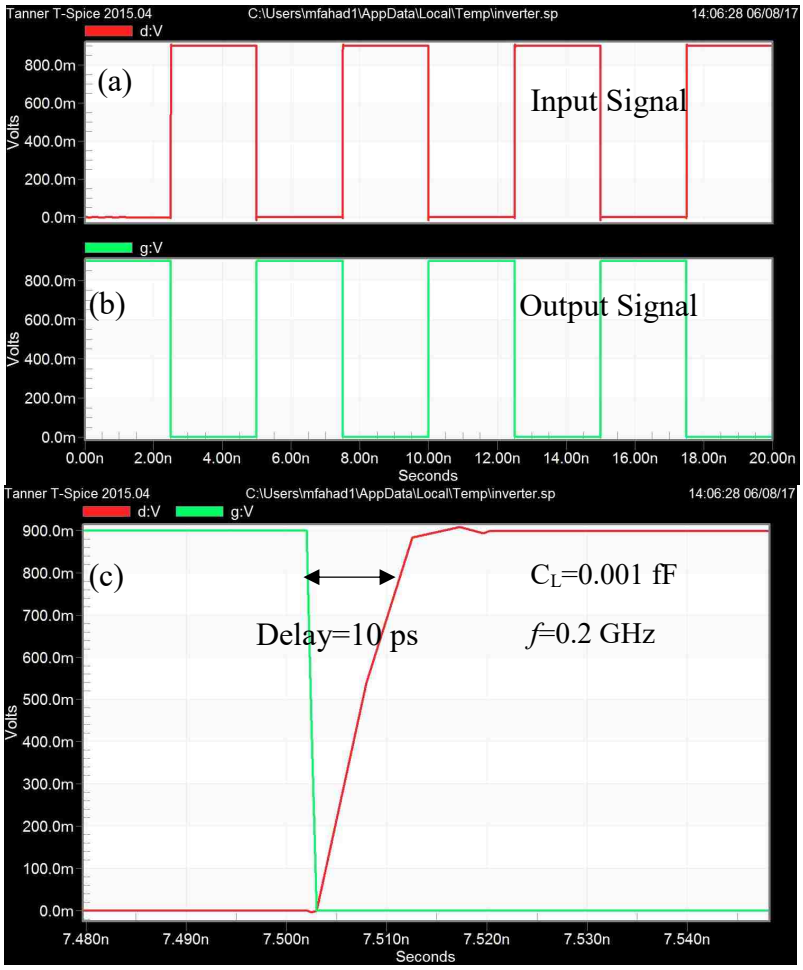


Figure 7.7: Graphene JTET transient performance analysis, a) Input square-wave signal at 0.2 GHz, b) obtained output from Graphene JTET inverter at 0.001 fF load capacitance, and c) inverter delay calculation.

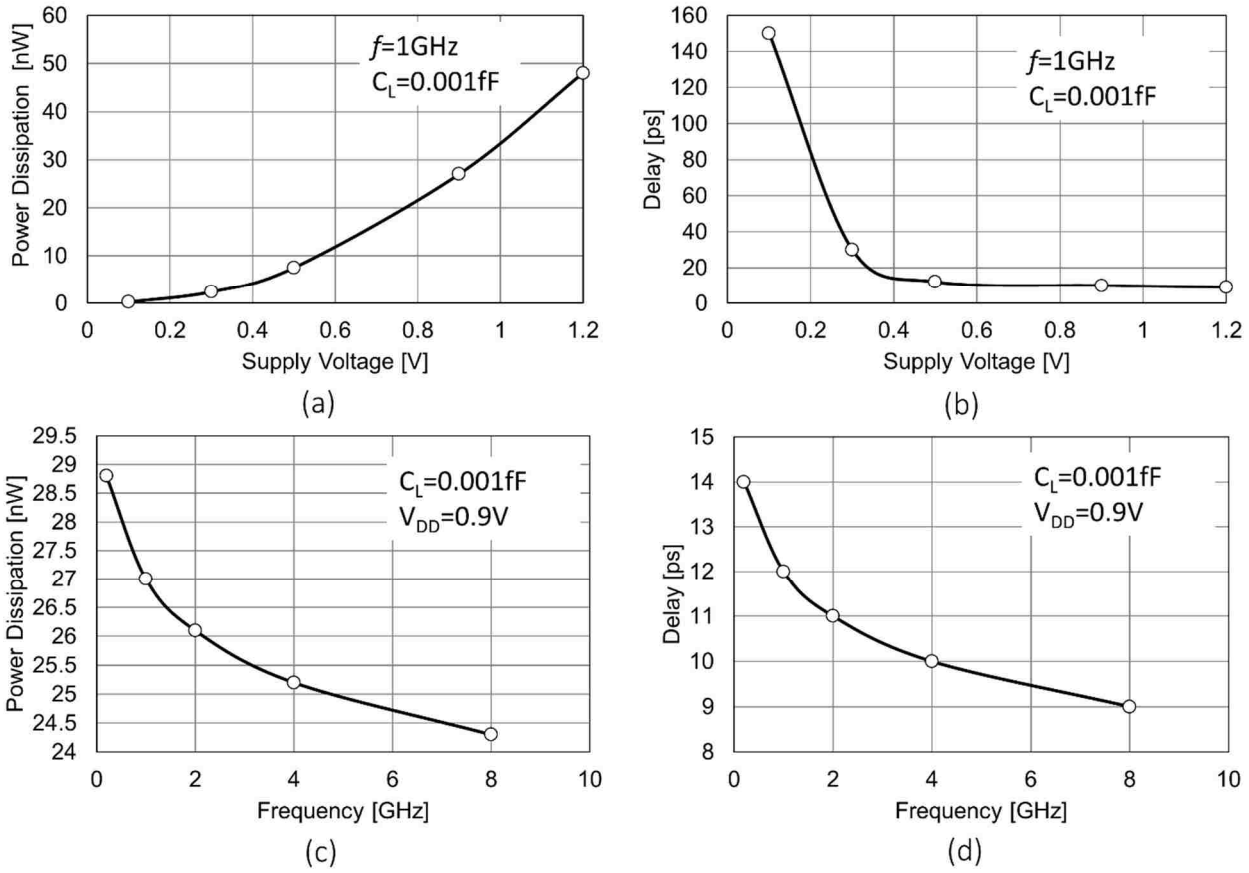


Figure 7.8: (a) Relationship between supply voltage and power dissipation for graphene JTET inverter for load capacitance of 0.001 fF and test frequency of 1 GHz, (b) relationship between supply voltage and delay at load capacitance of 0.001 fF and the test frequency at 1 GHz, (c) relationship between operating frequency and graphene JTET inverter power dissipation for load capacitance of 0.001 fF and the supply voltage of 0.9 V and (d) relationship between frequency and delay for 0.001 fF load capacitance and 0.9 V supply voltage.

both graphene JTET inverter power dissipation and delay decreases insignificantly which are shown in Fig. 7.8(c) and 7.8(d), respectively. With a very fast tunneling of carriers between top and bottom graphene layers in both p- and n- type graphene JTET, inverter power dissipation and delay changes very little for which graphene JTET inverter becomes suitable for high frequency logic operation. Compared to GNR TFET inverter performance shown Fig. 7.6(a) and 7.6(b) for a fixed supply voltage, graphene JTET shows similar trend in power dissipation and delay as the supply voltage increases. However, opposite behavior is observed in graphene JTET inverter for a fixed supply voltage and varying frequency for the estimation of power dissipation and delay as shown in Fig. 7.8(c) and 7.8(d), respectively. Power dissipation at 0.2 GHz is 28.8 nW for the graphene JTET inverter, which reduces to 24.25 nW at 8 GHz. Similarly, the delay estimated as 14ps at 0.2 GHz reduces to 9ps at 8 GHz. It can be explained as follows.

The performance of graphene JTET inverter shown in Fig. 7.8 is assumed to be dominated by long relaxation time of carriers in both the top and bottom graphene layers and existing population inversion in the channel. Both these effects are considered responsible for graphene's THz sensitivity [11]. In the case of graphene JTET, the tunneling electrons in the channel coming from top graphene layer remains at higher energy states compared to the existing electrons in the channel, which can result in population inversion. Hence, at a high frequency operation, significant number of electrons with their long relaxation time contribute to fast charge transfer between the top and bottom graphene layers resulting near constant delay at high frequency operation. Although the performance is studied up to 8 GHz, it is anticipated that similar high performance can be obtained above 8GHz.

Furthermore, compared to a large load capacitance, e.g. 50fF, a load capacitance of 0.001 fF is considered for graphene JTET inverter. It has been found that, a minimum of 0.05 fF of

load capacitance is required for appropriate charging and discharging of the load capacitance for retaining the logic values (either '0' or '1'). The computation shows that the higher values of load capacitances result in distorted logic levels.

7.4 Conclusion

GNR TFET and graphene JTET based digital integrated circuit design have been modeled and simulated in high level hardware description language Verilog-A in this chapter. Compared to conventionally reported look-up table based simulation approach of emerging nanoscale devices, direct compact model based Verilog-A simulations become suitable for EDA platforms. The performance obtained from GNR TFET inverter and graphene JTET inverter shows promising for low power energy efficient ultra-fast digital circuit design. Therefore, it is projected that the graphene based tunnel transistors hold the promise for energy efficient high performance integrated circuit design.

7.5 References

[1] M. Ionescu and H. Riel H., "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature,* vol. 479, pp. 329-337, Dec 2011.

[2] D. Jena, "Tunneling transistors based on graphene and 2-D crystals," *Proceedings of the IEEE*, vol. 101, pp. 1585-1602, 2013.

[3] X. Yang, J. Chauhan, J. Guo, and K. Mohanram, "Graphene tunneling FET and its applications in low-power circuit design," Proc. of *20th Great Lakes Symposium on VLSI*, Providence, Rhode Island, USA, 2010.

[4] L. Barboni, M. Siniscalchi, and B. Sensale-Rodriguez, "TFET-based circuit design using the transconductance generation efficiency g_m/I_d method," *IEEE Journal of the Electron Devices Society*, vol. 3, pp. 208-216, 2015.

[5] M.-A. Chalkiadaki, C. Valla, F. Poullet, and M. Bucher, "Why- and how- to integrate Verilog-A compact models in SPICE simulators, "*International Journal of Circuit Theory and Applications*," vol. 41, pp. 1203-1211, 2013.

[6] H. Lu, D. Esseni, and A. Seabaugh, "Universal analytic model for tunnel FET circuit simulation," *Solid-State Electronics*, vol. 108, pp. 110-117, Jun 2015.

[7] M. S. Fahad, A. Srivastava, A. K. Sharma, and C. Mayberry, "Analytical current transport modeling of graphene nanoribbon tunnel field-effect transistors for digital circuit design," *IEEE Transactions on Nanotechnology,* vol. 15, pp. 39-50, Jan 2016.

[8] G. Fiori and G. Iannaccone, (2013). *NanoTCAD ViDES* [Online].Available: http://vides.nanotcad.com/vides/

[9] A. Srivastava, Y. Xu, and R. Soundararajan, "Energy Recovery Techniques for CNT-FET Circuits," Proc. of *International Symposium on Electronic System Design (ISED)*, India, pp. 81-84, 2010.

[10] A. Raychowdhury, C. Augustine, Y. Gao, M. Lundstrom, K. Roy, "PETE: Purdue Emerging Technology Evaluator," https://nanohub.org/resources/pete, 2016.

[11] V. Ryzhii, T. Otsuji, M. Ryzhii, and M. S. Shur, "Double graphene-layer plasma resonances terahertz detector," *Journal of Physics D: Applied Physics,* vol. 45, p. 302001, 2012.

CHAPTER 8

CONCLUSION

Current transport modeling of two dimensional material based tunnel transistor is studied in this dissertation. Compared to traditional MOSFET, TFET holds the promise of steep subthreshold slope operation through band-to-band tunneling mechanism contrary to thermionic transport in MOSFET. For this reason, a comparatively low energy is required. Since the low energy Fermi-Dirac distribution contributes to such band-to-band tunneling, the subthreshold slope of TFET is independent of the thermionic limit of 60 mV/decade at room temperature and can go well below this value. Atomically thin two dimensional low energy band gap and low effective mass materials also provide significant improvement for TFET performance. Graphene with its superior electronic properties remains an attractive alternative channel material for the design of TFET compared to the bulk material based TFET.

A physics based compact analytical current transport model of a graphene based planar band-to-band tunnel transistor is derived and validated through quantum transport numerical simulations. The model is compatible Mentor Graphics® Tanner Tool EDA/Verilog-A for the analysis and design of integrated circuits.

Since the band gap engineering is very challenging for the realization of graphene based devices, research for alternative device structure exploiting new current transport mechanism has become critical. With this regard, iTFET plays a critical role. However, a physics based subthreshold slope model derived has shown that the supply voltage scaling of such iTFET is restrained by the thermionic limit of 60 mV/decade. With a reasonably thin tunneling barrier, iTFET will always result a subthreshold slope far greater than that of a standard MOSFET. Therefore, novel current transport process other than in MOSFET, TFET and iTFET becomes

necessary. Considering such challenges, the concept of junctionless tunnel effect transistor (JTET) is proposed. JTET is independent of the thermionic limit of MOSFET and becomes suitable for aggressive supply voltage scaling. Considering two dimensional vertical heterostructure of graphene and boron nitride, and molybdenum disulfide and boron nitride, the interlayer tunneling based current transport model is derived.

Based on the findings for such a graphene JTET and MoS_2 JTET, the concept of interlayer tunneling based barrier control mechanism can be extended for other material systems. Since JTET is free of inherent doping, large depletion regions are also absent in JTET. Hence, the JTETs become suitable for extreme channel length scaling. Moreover, being vertically oriented for the current transport, JTET is suitable for vertical integration and would require a significantly reduced interconnects at the back end of line (BEOL) process. Therefore, for a technology node similar to FinFET or TFET, JTET would provide relatively double transistor density. The promising performances of GNR TFET and graphene JTET integrated circuits are obtained through the simulation of inverters using Verilog-A. Nevertheless, further experiments and characterizations are required to validate the proof of concept of JTET. This is beyond the scope of present work and is suggested for the future work.

With the aggressive downscaling of technology node and continuous demand of energy efficient integrated circuits, exploratory research of emerging materials and devices are highly required. By adopting a complete integration from material growth to integrated circuit simulation, design, fabrication and characterization, such a technological challenge can be overcome successfully. While the present work contributes to the theory, design and simulation of emerging materials such as graphene, BN and MoS_2, and devices such as MOSFET, TFET, iTFET and JTET; the experimental procedures are left as the scope of future work.

APPENDIX-A

LIST OF MODEL PARAMETERS

Symbol	Definition
$p+$	Degenerately doped p-type semiconductor
$n+$	Degenerately doped n-type semiconductor
E_P^V	Valence band energy level in p-type material
E_N^C	Conduction band energy level in n-type material
E_P^F	Fermi level in p-type material
E_N^F	Fermi level in n-type material
q	Charge of electron
ξ	Electric field at the tunnel junction
m^*	Carrier effective mass
m_e^*	Electron effective mass
m_h^*	Hole effective mass
$\hbar$	Reduced Planck constant
E	Energy of particle
k	Wave vector
k_x	One dimensional Wave vector in x direction
U	Potential barrier
d	Thickness of the tunneling barrier
T_{WKB}	Tunneling probability in WKB (Wentzel-Kramers-Brillouin) approximation
E_G, E_g	Energy band gap
m_r^*	Reduced effective mass
I^{1D}	1D Zener tunneling current
V_g	Group velocity
$\rho(k_x)$	1D density of states
f_V	Fermi-Dirac distributions at the valence band
f_C	Fermi-Dirac distributions at the conduction band
V_R	Reverse bias voltage
V_T	Thermal voltage
k_B	Boltzmann's constant
T	Temperature
NDR	Negative temperature resistance
E_F^S	Source Fermi level
E_C^S	Source conduction band
E_V^S	Source valence band
E_F^C	Channel Fermi level
E_C^C	Channel conduction band
E_V^C	Channel conduction band
E_F^D	Drain Fermi level
E_C^D	Drain conduction level
E_V^D	Drain valence level

E_F^T	Fermi level at the top electrode
E_F^B	Fermi level at the bottom electrode
λ	The length scale for potential variation
ε_c	Channel dielectric permittivity
ε_{ox}	Oxide dielectric permittivity
t_c	Channel thicknesses
t_{ox}	Oxide thicknesses
$\Delta\varphi$	The energy window for tunneling
f_S	Source Fermi-Dirac distributions
f_D	Drain Fermi-Dirac distributions
I_D	Drain current
V_G	Gate voltage
C_d	Depletion capacitances
C_{ox}	Gate capacitances
V_{eff}	Effective bias at the tunnel junction
V_{GS}	Gate-source bias
V_{DS}	Drain-source bias
A	Constant in Eq. (1.22) and is equal to 1
$E_n(k_z, k_y, k_z)$	Three dimensional energy dispersion relation for n-number of bands
k_y	Wave vector in y direction
k_z	Wave vector in z direction
$W_z(E)$	Function expressed with the minimal imaginary k_z (Imk_z)
Δ	Barrier height
$\boldsymbol{a_1, a_2}$	Lattice vectors in real space
$\boldsymbol{b_1, b_2}$	Lattice vectors in reciprocal lattice space
$\boldsymbol{K, K'}$	Two points at the corners of the Brillouin zone (BZ) in momentum space
$\boldsymbol{\delta_1, \delta_2, \delta_3}$	The three nearest-neighbor vectors in real space of graphene
$(p,0)$	Chirality of carbon nanotube specific for GNR
p	Number of carbon atoms on each ring of unrolled carbon nanotube
t_{GNR}	Thickness of the GNR
V_{TH}	Threshold voltage
φ_G	Contact potentials due to gate contact
φ_S	Contact potentials due to source contact
φ_{BI}	Built in potential
N	Doping density
n_i	Intrinsic carrier density
φ_{OX}	Potential drop due to gate oxide over the channel
n_s	Induced surface charge density through gate oxide
Q_0	Total charge due to n_s
v_F	Fermi velocity
ξ_0	Built-in electric field at the source-channel tunnel junction
γ_1, γ_2	The linear coefficients in unit of inverse of volt (V^{-1})
σ	Conductivity
μ_n	Carrier mobility

I_T	Tunneling current
I_L	Leakage current
W	Channel width
$\|E_{TM}\|$	Energy of electron in transverse mode
$M(E)$	Transverse mode of current transport
$G(E)$	Conductance
I_{TH}	Current at threshold voltage
I_{OFF}	Off current determined at V_{GS}=0V.
I_{Th}	Thermionic current component over the barrier
I_{Tb}	Tunneling bias current
I_{Tnb}	Tunneling non-bias current
I_{In}	Initial current
I_{Fi}	Final current
DoS_B	Density of states of the bottom graphene layers
DoS_T	Density of states of the top graphene layers
f_T	Fermi-Dirac distributions at the top electrode
f_B	Fermi-Dirac distributions at the bottom electrode
ΔE_F	Shift in Fermi level
$D(E)$	Density of states of graphene
g_s	Spin degeneracy
g_v	Valley degeneracy
$T_B(E)$	Transmission coefficient in ballistic transport
V_{GT}	Top gate bias
V_{GB}	Bottom gate bias
ρ_{MoS_2}	Density of states (DOS) in MoS_2
$m^*_{MoS_2}$	Effective mass in mos_2
$\Delta\phi$	Effective change in channel Fermi level
E_{FN}	Fermi level in n-type material
E_{FP}	Fermi level in p-type material
E_C	Conduction band energy level
E_V	Valence band energy level
V_{ch}	Voltage drop in the channel
V_0	Intrinsic mid-gap bias
V_V	Channel charge induced voltage drop
C_V	Net vertical capacitance between top and bottom gate electrodes
λ_{DIBL}	Drain induced barrier lowering (DIBL) parameter
α	Fractional coefficient of DIBL
μ_{FE}	Field effect mobility
k_F	Fermi wave vector
l_e	Mean free path
C_G	Total gate capacitance
C_V	Net vertical capacitances
hBN	Hex boron nitride
ε_{hBN}	Dielectric permittivity of hBN
ε_{MoS2}	Dielectric permittivity of MoS_2
t_{MoS2}	Thickness of MoS_2

t_{hBN}	Thickness of hBN
Z_g	Number of hBN layers as gate dielectric
Z_t	The number of hBN layers as tunnel barrier
$C_{q,hBN}$	Quantum capacitance of single layer hBN
ρ_{hBN}	Density of states of hBN
$C_{q,MoS2}$	Quantum capacitance of single layer MoS_2
ρ_{MoS2}	Density of states of MoS_2
C_1	Geometric capacitances of top gate dielectric hBN
C_8	Geometric capacitances of bottom gate dielectric hBN
C_2	Quantum capacitances of top gate dielectric hBN
C_9	Quantum capacitances of bottom gate dielectric hBN
C_3	Geometric capacitance of top MoS_2
C_4	Quantum capacitance top MoS_2
C_5	Geometric capacitances of tunneling barrier hBN
C_6	Quantum capacitances of tunneling barrier hBN
C_{10}	Source quantum capacitance of MoS_2
C_{11}	Drain quantum capacitance of MoS_2
C_7, Cq_{ch}	Gate dependent channel quantum capacitance
f_T	Intrinsic cut-off frequency
g_m	Transconductance
τ	Intrinsic gate delay
PDP	Power delay product
V_{DD}	Supply voltage
I_{ON}	ON current
L	Channel length
V_{high_real}	Central point of real logic high
$V_{high\_perfect}$	Central point of perfect logic high
N_A	Total number of atoms along GNR width
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
TFET	Tunnel Field Effect Transistor
iTFET	Interlayer Tunnel Field Effect Transistor
JTET	Junctionless Tunnel Effect Transistor

APPENDIX-B

VERILOG-A CODE FOR GNR TFET

```
// Verilog-A for GNRTFET, nTFET, veriloga

`include "constants.vams"
`include "disciplines.vams"


// Physical Constants
`define pi 3.1416
`define hb 1.05e-34                 // modified plank constant
`define q 1.602e-19                 // Charge
`define epo 8.86e-14                // Permittivity of free space
`define mu 223.6                    // Mobility
`define vf 1e8                      // Fermi velocity
`define Eg 0.15                             // Energy band gap
`define F 3.85e6                    // Electric field at the tunnel junction
`define KT 0.0259


module nTFET(d, s, g);
inout d;
electrical d;
inout s;
electrical s;
input g;
electrical g;

//Instance Parameters

parameter real Tox = 1e-9;          // oxide layer thickness in meter
parameter real T = 300;                     // temperature in K
parameter real L = 20e-9;           // length of GNR in meter
parameter real er = 3.9;                    // permitivity of top oxide layer


// Variables

real Vgs,Vds,Vth;                   // External voltages
real Cgs,Cgd,Cds;                   // Capacitance
real Ids;
real Twkb;                          // Tunneling probability
real e1;                            // Argument before arg2
real e2;                            // Argument with log
```

```
analog begin

Vgs=V(g)-V(s);
Vds=V(d)-V(s);
Vth=0.1;
Vgs=Vgs+0.01;


Cgs=5e-18;
Cgd=5e-18;
//Cds=5e-10;

if ((Vgs-Vth) >= 0) begin
Twkb=exp(-`pi*((`Eg*`q)*(`Eg*`q))/(4*`q*`hb*`vf*`F));
e1=(`mu*`epo*er*Vgs)/Tox;
e2=(-ln(1+exp((Vgs-Vth-Vds)/`KT))+ln(1+exp((Vgs-Vth)/`KT))+ln(1+exp(-Vds/`KT))-ln(2));

Ids=e1*`KT*Twkb*e2;

end

// Current
I(d,s)<+ Ids*1;

//Cap
I(g,s) <+ ddt(Cgs*V(g,s));
//I(s,g) <+ ddt(Cgs*V(g,s));
I(g,d) <+ ddt(Cgd*V(g,d));

end //analog
endmodule

// Verilog-A for GNRTFET, pTFET, veriloga

`include "constants.vams"
`include "disciplines.vams"


// Physical Constants
`define pi 3.1416
`define hb 1.05e-34                 // modified plank constant
`define q 1.602e-19                 // Charge
`define epo 8.86e-14                // Permittivity of free space
`define mu 223.6                    // Mobility
`define vf 1e8                      // Fermi velocity
```

```
`define Eg 0.28                         // Energy band gap
`define F 3.85e6                        // Electric field at the tunnel junction
`define KT 0.0259


module pTFET(d, s, g);
inout d;
electrical d;
inout s;
electrical s;
input g;
electrical g;

//Instance Parameters

parameter real Tox = 1e-9;              // oxide layer thickness in meter
parameter real T = 300;                 // temperature in K
parameter real L = 20e-9;               // length of GNR in meter
parameter real er = 3.9;                // permitivity of top oxide layer

// Variables

real Vgs,Vds,Vth;                       // External voltages
real Cgs,Cgd,Cds;                       // Capacitance
real Ids;
real Twkb;                              // Tunneling probability
real e1;                                // Argument before arg2
real e2;                                // Argument with log

analog begin

Vgs=V(g)-V(s);
Vds=V(d)-V(s);
Vth=-0.1;
Vgs=Vgs-0.01;

Cgs=5e-18;
Cgd=5e-18;
//Cds=5e-10;

if ((Vgs-Vth) <= 0) begin
Twkb=exp(-`pi*((`Eg*`q)*(`Eg*`q))/(4*`q*`hb*`vf*`F));
e1=(`mu*`epo*er*Vgs)/Tox;
e2=(-ln(1+exp((Vgs-Vth-Vds)/`KT))+ln(1+exp((Vgs-Vth)/`KT))+ln(1+exp(-Vds/`KT))-ln(2));

Ids=e1*`KT*Twkb*e2;
```

```
end

// Current
I(d,s)<+ Ids*1;

//Cap
I(g,s) <+ ddt(Cgs*V(g,s));
//I(s,g) <+ ddt(Cgs*V(g,s));
I(g,d) <+ ddt(Cgd*V(g,d));
end //analog
endmodule
```

APPENDIX-C

VERILOG-A CODE FOR GRAPHENE JTET

```
// VerilogA for JTET, nJTET, veriloga

`include "constants.vams"
`include "disciplines.vams"


// Physical Constants
`define pi 3.1416
`define hb 6.58e-16                    // modified plank constant
`define h 6.63e-34                     // plank's constant
`define T 0.005                        // interlayer tunneling probability
`define q 1.602e-19                    // charge
`define vf 1e8                         // Fermi velocity
`define KT 0.0259                      // thermal voltage
`define W 50e-9                        // graphene channel width


module JTET(dn1, sn1, g1);
inout dn1;
electrical dn1;
inout sn1;
electrical sn1;
input g1;
electrical g1;


//Instance Parameters

parameter real L1 = 1e-6;              // tunneling area's length in micormeter
parameter real W1 = 0.05e-6;           // tunneling area's width in micormeter


// Variables

real Vg,Vds;                           // External voltages
real Cgs,Cgd;                          // Capacitance
real a1;                               // partial argument
real b1;                                       // partial argument
real arg1;                             // argument
real N;                                // tunneling charge density
real Ef;                               // change in Fermi level
real VG1;                              // translating fermi level into bias
```

```
real A;                                  // tunneling area
real a2;                                 //partial argument
real b2;                                         // partial argument
real J;                                          // current density
real Ids;                                // drain current

analog begin
Vg=V(g1)-V(sn1);
Vds=V(dn1)-V(sn1);

Vg=Vg+0.01;

Cgs=0.0952e-18;
Cgd=0.0952e-18;

if (Vg >= 0) begin
   a1=Vg*Vg/12;
   b1=Vg*`KT*ln(1+exp(Vg/`KT));
   arg1=a1-b1;
   N=arg1*`T*(2/(`pi*(`hb*`vf)* (`hb*`vf)));
   Ef=`hb*`vf*sqrt(`pi*(-N));
   VG1=Ef;
   A=L1*W1;
   a2=`W*2*VG1/(`pi*`hb*`vf);
   b2=-ln(1+exp(VG1/`KT))+ln(1+exp((VG1-Vds)/`KT))+ln(2)-ln(1+exp(-Vds/`KT));
   Ids=-((2*`q*`q*`KT/`h)*a2*b2);
   J=Ids/A;

end

// Current
I(dn1,sn1)<+ Ids*1;

//Cap
I(g1,sn1) <+ ddt(Cgs*V(g1,sn1));
//I(g2,s) <+ ddt(Cgs*V(g2,s));
I(g1,dn1) <+ ddt(Cgd*V(g1,dn1));
//I(g1,d) <+ ddt(Cgd*V(g1,d));
//I(g2,d) <+ ddt(Cgd*V(g2,d));

end //analog
endmodule

// VerilogA for JTET, pJTET, veriloga

`include "constants.vams"
```

```
`include "disciplines.vams"


// Physical Constants
`define pi 3.1416
`define hb 6.58e-16                    // modified plank constant
`define h 6.63e-34                      // plank's constant
`define T 0.04                          // interlayer tunneling probability
`define q 1.602e-19                    // Charge
`define vf 1e8                         // Fermi velocity
`define KT 0.0259                       // thermal voltage
`define W 50e-9                                 // graphene channel width

module JTET(dp1, sp1, g1);
inout dp1;
electrical dp1;
inout sp1;
electrical sp1;
input g1;
electrical g1;

//Instance Parameters

parameter real L1 = 1e-6;              // tunneling area's length in micormeter
parameter real W1 = 0.05e-6;           // tunneling area's width in micormeter

// Variables

real Vg,Vds;                           // External voltages
real Cgs,Cgd;                          // Capacitance
real a1;                               // partial argument
real b1;                                        // partial argument
real arg1;                             // argument
real N;                                // tunneling charge density
real Ef;                                // change in Fermi level
real VG1;                                // translating fermi level into bias
real A;                                // tunneling area
real a2;                               //partial argument
real b2;                                        // partial argument
real J;                                // current density
real Ids;                                       // drain current

analog begin

Vg=V(g1)-V(sp1);
Vds=V(dp1)-V(sp1);
```

```
Vg=Vg-0.01;

Cgs=0.0952e-18;
Cgd=0.0952e-18;

if (Vg <= 0) begin
   a1=Vg*Vg/12;
   b1=Vg*`KT*ln(1+exp(Vg/`KT));
   arg1=a1-b1;
   N=arg1*`T*(2/(`pi*(`hb*`vf)* (`hb*`vf)));
   Ef=`hb*`vf*sqrt(`pi*(N));
   VG1=Ef;
   A=L1*W1;
   a2=`W*2*VG1/(`pi*`hb*`vf);
   b2=-ln(1+exp(VG1/`KT))+ln(1+exp((VG1-Vds)/`KT))+ln(2)-ln(1+exp(-Vds/`KT));
   Ids=-((2*`q*`q*`KT/`h)*a2*b2);
   J=Ids/A;

end

// Current
I(dp1,sp1)<+ Ids*1;

//Cap
I(g1,sp1) <+ ddt(Cgs*V(g1,sp1));
//I(g,sp) <+ ddt(Cgs*V(g,sp));
I(g1,dp1) <+ ddt(Cgd*V(g1,dp1));
//I(gp1,o) <+ ddt(Cgd*V(gp1,o));
//I(g,o) <+ ddt(Cgd*V(g,o));

end //analog
endmodule
```

APPENDIX-D

LIST OF PUBLICATIONS

Patent

A. Srivastava and M. Fahad, "Vertical Interlayer Tunnel Field Effect Transistor Using Hexagonal Boron Nitride," LSU Application No. LSU-2016-049, filed provisional patent, Dec 2016.

Journals

1. M. Fahad and A. Srivastava, "Subthreshold slope of vertical graphene interlayer tunnel transistor," *Nano,* vol. 12, no. 6, p. 1750069, Jul 2017.

2. A. Srivastava and M. Fahad, "Vertical MoS_2/hBN/MoS_2 interlayer tunneling field effect transistor", *Solid State Electronics*, vol. 126, pp. 96-103, Dec 2016.

3. M. Fahad, A. Srivastava, A. K. Sharma, and C. Mayberry, "Analytical current transport model of graphene nanoribbon tunnel field effect transistor for digital circuit design," *IEEE Trans. Nanotech.*, vol. 15, no. 1, pp. 37-48, Jan 2016.

4. M. Fahad and A. Srivastava, "A graphene switching transistor for vertical circuit design," *ECS J. of Solid State Sci. and Tech.*, vol. 5, no. 3, M13-M21, Dec 2016.

5. K. Mohsin, A. Srivastava, A. K. Sharma, C. Mayberry and Md Fahad, "Temperature sensitivity of resistivity of graphene/copper hybrid nanoribbon interconnect: a first principle study," *ECS J. of Solid State Sci. and Tech*, vol. 6, no. 4, pp. P119-P124, Feb 2017.

Conference Proceedings

1. M. Fahad, A. Srivastava, A. K. Sharma and C. Mayberry, "Silicene nanoribbon tunnel field effect transistor," *ECS Trans.*, vol. 75, no.5, pp. 1-4, 2016.

2. K. Mohsin, A. Srivastava, A. K. Sharma, C. Mayberry and M. Fahad, "Current transport in graphene/copper hybrid nano ribbon interconnect: a first principle study," *ECS Trans.*, vol. 75, no.13, pp. 1-4, 2016.

3. A. Srivastava, Y. Banadaki and M. Fahad, "Dielectrics for graphene transistors for emerging integrated circuits," *ECS Trans.*, vol. 61, no.2, pp. 1-11, 2014.

4. M. Fahad, Z. Zhao, A. Srivastava and L. Peng., "Modeling of GNR TFET in Verilog-A for digital circuit design," Proc. 2nd IEEE Computer Society Int. Sym. on Nanoelectronics and Information Science (iNIS), Gwalior, India, pp. 1-5, 2016.

5. M. Fahad, A. Srivastava, A. K. Sharma and C. Mayberry, “Current transport in graphene tunnel field effect transistor under constant electric field,” *Proc. of SPIE*, vol. 8814, pp. 1-8, 2013.

6. M. Fahad, A. Srivastava, A. K. Sharma and C. Mayberry, “Current transport in graphene tunnel field effect transistor for RF integrated circuits,” *Proc. IEEE MTT-S Int. Wireless Sym.*, pp. 1-4, 2013.

VITA

Md Shamiul Fahad was born in 1988 in Dhaka, Bangladesh. He completed his B.S. in electrical and electronic engineering with first class with honors and a CGPA of 3.96 from the Islamic University of Technology (IUT), Gazipur, Bangladesh in November 2009. Since January 2012, he started his Ph.D. under Dr. Ashok Srivastava in the division of electrical and computer engineering at the Louisiana State University, Baton Rouge, LA. He obtained his M.S. from the same university in December 2016. Md Fahad's research interest includes theory, design, modeling, simulation and fabrication of energy efficient two dimensional materials and devices for integrated circuit design. He is also a visionary futuristic, technocrat and has an active interest on technology trend combining the concept of engineering, philosophy and entrepreneurship of nanotechnology. He is expected to graduate in August 2017. Md Shamiul Fahad will join technology and manufacturing group in Intel Corporation at Hillsboro, OR as an interconnect integration development engineer after his graduation.