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# Carbon Nanotube Interconnect Modeling for Very Large Scale Integrated Circuits

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# CARBON NANOTUBE INTERCONNECT MODELING FOR VERY LARGE SCALE INTERGRATED CIRCUITS

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*To my loving and supportive wife, Xiuli*

*&*

*To my wonderful sons, Evan & Kevin*

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# ABSTRACT

In this research, we have studied and analyzed the physical and electrical properties of carbon nanotubes. Based on the reported models for current transport behavior in non-ballistic CNT-FETs, we have built a dynamic model for non-ballistic CNT-FETs. We have also extended the surface potential model of a non-ballistic CNT-FET to a ballistic CNT-FET and developed a current transport model for ballistic CNT-FETs.

We have studied the current transport in metallic carbon nanotubes. By considering the electron-electron interactions, we have modified two-dimensional fluid model for electron transport to build a semi-classical one-dimensional fluid model to describe the electron transport in carbon nanotubes, which is regarded as one-dimensional system. Besides its accuracy compared with two-dimensional fluid model and Lüttinger liquid theory, one-dimensional fluid model is simple in mathematical modeling and easier to extend for electronic transport modeling of multi-walled carbon nanotubes and single-walled carbon nanotube bundles as interconnections.

Based on our reported one-dimensional fluid model, we have calculated the parameters of the transmission line model for the interconnection wires made of single-walled carbon nanotube, multi-walled carbon nanotube and single-walled carbon nanotube bundle. The parameters calculated from these models show close agreements with experiments and other proposed models. We have also implemented these models to study carbon nanotube for on-chip wire inductors and it application in design of LC voltage-controlled oscillators.

By using these CNT-FET models and CNT interconnects models, we have studied the behavior of CNT based integrated circuits, such as the inverter, ring oscillator, energy recovery logic; and faults in CNT based circuits.

# CHAPTER 1

# INTRODUCTION

## 1.1 Challenges of Silicon Integrated Circuits

Semiconductor Research Corporation (SRC) in its International Technology Roadmap of Semiconductors report (ITRS 2003) has refereed to several non-classical devices, which could be the candidates of future technology to replace the existing silicon MOSFETs as the end of Moore's law approaches year 2020 [1]. Double gate MOSFET and FinFET are recognized as two of the most promising candidates for future very large scale integrated (VLSI) circuits [2-5]. The carbon nanotube field-effect transistor (CNT-FET) is regarded as an important contending device to replace silicon transistors [6, 7] since many of the problems that silicon technology is facing are not present in CNTs. For example, carrier transport is 1-D in carbon nanotubes; the strong covalent bonding gives the CNTs high mechanical and thermal stability and resistance to electromigration; and diameter is controlled by its chemistry and not by the standard conventional fabrication process [2].

For interconnects, as CMOS processes scale into the nanometer regime, lithography limitations, electromigration, and the increasing resistivity and delay of copper interconnects have driven the need to find alternative interconnect solutions [8]. Carbon nanotubes have emerged as a potential candidate to supplement copper interconnects because of their ballistic transport and ability to carry large current densities in the absence of electromigration [9]. Previous studies that assess the potential use of CNTs as interconnects [10-13] primarily focus on the relative interconnect delay of CNTs to copper for sub-nm CMOS technology nodes. Carbon nanotubes are being explored extensively as the material for making future complementary devices, integrated circuits [14-16], interconnects [17] and hybrid CMOS/Nanoelectronic circuits [18].

## 1.2 Introduction to Carbon Nanotubes

In 1991, electron microscopist Sumio Iijima [19], of the NEC laboratories in Japan discovered the carbon nanotubes that are a tubular shape in the form of coaxial tubes of graphitic sheets, ranging from two shells to approximately fifty. These structures

were categorized as the multi-walled carbon nanotubes (MWCNTs). Subsequently growth of single-walled carbon nanotubes (SWCNTs) were reported by Bethune et al. [20] and Iijima and Ichihashi [21].

Most SWCNTs have a diameter close to 1 nanometer, with a tube length that can be many thousands of times longer. The structure of a SWCNT can be conceptualized by wrapping an atomic thick layer of graphite called graphene into a seamless cylinder. Multi-walled carbon nanotubes consist of multiple layers of graphite rolled in to form a tubular shape. Since CNTs are planar graphite sheets wrapped into tubes, electrical characteristics vary with the tube diameter and the wrapping angle of graphene [22]. One of the interesting features of the carbon nanotube is that it can be metallic or semiconducting with bandgap depending on its chirality [23-25]. In the following, we discuss structure and electronic behavior of carbon nanotubes.

## 1.3 Structure of Carbon Nanotubes

There are four types of natural occurring carbon, diamond, graphite, ceraphite, and fullerenes. Fullerenes are molecules formed entirely of carbon and take the shape of a hollow sphere, ellipsoid, or a tube. Fullerenes that take the shape of a tube are called buckytubes or nanotubes.

Carbon nanotubes can be pictured as a result of folding graphene layers into a tubular structure as seen in Fig. 1.1 [26]. These cylindrical form of carbon nanotubes can be single-walled or multi-walled depending on the number of shells that form the tubular structure [25]. Single-walled carbon nanotubes are composed of one shell of carbon atoms. Multi-walled carbon nanotubes have multiple nested shells of carbon atoms, as shown in Fig. 1.2. Single-walled carbon nanotubes tend to adhere strongly to each other forming ropes or bundles of nanotubes as shown in Fig. 1.3 [26] exhibiting physical properties of both metallic and semiconducting materials [22].

Carbon nanotubes exhibit promising mechanical and electrical properties. Tables 1.1 and 1.2 summarize mechanical and electrical properties of carbon nanotubes [27-29]. It also compares properties with that of silicon, currently used material in CMOS technologies.

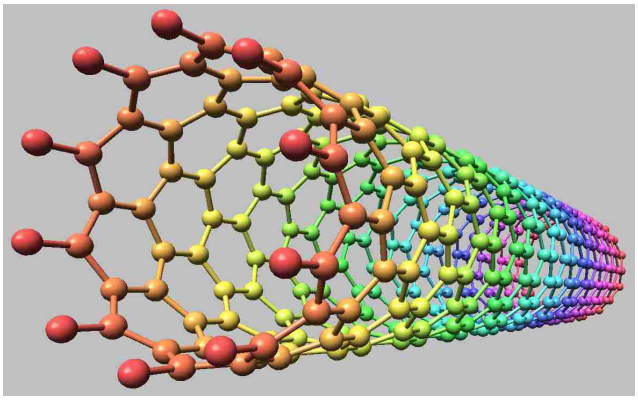


Figure 1.1: Single-walled carbon nanotube (Nanotube Modeler Software) [26].

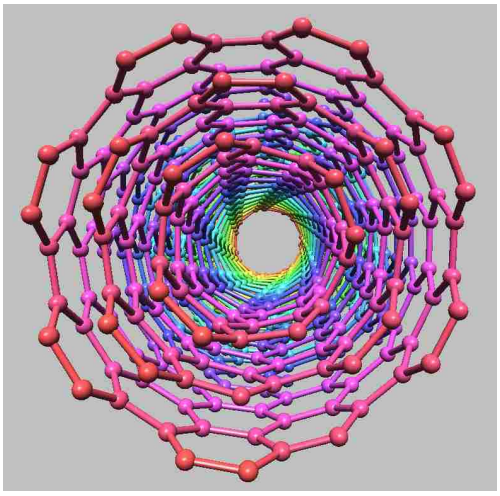


Figure 1.2: Multi-walled carbon nanotubes (Nanotube Modeler Software) [26].

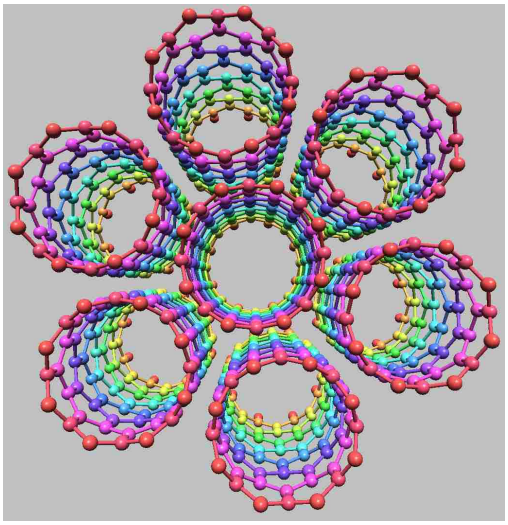


Figure 1.3: Single-walled carbon nanotubes bundle (Nanotube Modeler Software) [26].

Table 1.1: Mechanical properties of carbon nanotubes and comparison with other materials [27]

| Material | Young's Modulus (TPa) | Tensile Strength (GPa) | Elongation at Break (%) | Thermal Conductivity (W/mK) |
|---|---|---|---|---|
| **SWCNT** | 1-5 | 13-53 | 16 | 3,500-6,600 |
| **MWCNT** | 0.27-0.95 | 11-150 | 8.04-10.46 | 3000 |
| **Stainless steel** | 0.186-0.214 | 0.38–1.55 | 15-50 | 16 |
| **Kevlar** | 0.06–0.18 | 3.6–3.8 | ~2 | ~1 |
| **Copper** | 0.11–0.128 | 0.22 | | 385 |
| **Silicon** | 0.185 | 7 | | 149 |

Table 1.2: Electrical properties of carbon nanotubes and comparison with other materials [28, 29]

| **Semiconductor** | | | | | **Metal** | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Semiconducting SWCNT** | **Silicon** | **GaAs** | **Ge** | **Parameter** | **Metallic SWCNT** | **Copper** |
| **Bandgap (eV)** | 0.9/diameter | 1.12 | 1.424 | 0.66 | **Mean Free Path (nm)** | 1,000 | 40 |
| **Electron Mobility ($cm^2/Vs$)** | 20,000 | 1,500 | 8,500 | 3,900 | **Current density ($A/cm^2$)** | $10^{10}$ | $10^6$ |
| **Electron Phonon Mean Free Path (Å)** | ~700 | 76 | 58 | 105 | **Resistivity (Ω·m)** | $\sim 10^{-5}$ | $1.68 \times 10^{-8}$ |

Metallic carbon nanotubes conduct extremely large amount of current densities. This property is what allows the application of metallic CNTs in interconnection substituting to metal wires, such as Cu, for the next generation of integrated circuits. On the other hand, semiconducting CNTs can be switched on and off by using a gate electrode. This property is what allows the application of CNTs in implementing field-effect transistors.

Single-walled carbon nanotubes have risen as one of the most likely candidates for miniaturizing electronics beyond current technology. The most fundamental application of metallic SWCNTs is in interconnection. Since it is difficult to prepare metallic CNT, fabrication and process integration of MWCNTs and CNT bundles interconnects have been reported [30, 31]. This work will focus on carbon nanotube field-effect transistors (CNT-FETs) and CNT interconnects made using semiconducting and metallic single-walled carbon nanotubes (SWCNTs), respectively, and on some basic circuits, such as the inverter and ring oscillator which are composed of complementary CNT-FETs and CNT interconnects.

## 1.4 Properties of Single-Walled Carbon Nanotubes

Single-walled carbon nanotubes can be characterized by its chirality or chiral vector. The chirality is an adapted concept uniquely of each type of nanotube that determines its properties and diameter [25]. The chirality is represented with a pair of indices (n,m) called the chiral vector, which is shown in Fig 1.4. The chiral vector traces the CNT around its circumference from one carbon atom (called the reference point) back to itself. It is expressed as,

$$\vec{C}_h = n\vec{a}_1 + m\vec{a}_2 , \tag{1.1}$$

where $\vec{a}_1$ and $\vec{a}_2$ are the unit vectors for the graphene hexagonal structure and (n,m) are integers that represent the number of hexagons away from the reference point to the point, which will overlap to the reference point after rolled over, in the $a_1$ and $a_2$ directions, respectively.

Using n, m indices CNTs can be classified in three groups: armchair nanotubes for n = m, zigzag nanotubes for m = 0 or n = 0, and chiral nanotubes for any other combination. Furthermore, integers n, m also determine whether a CNT is metallic or semiconducting, when n – m = 3*l* (*l* is an integer), the nanotube is metallic, and when n – m ≠ 3*l*, the nanotube is semiconducting. The energy gap of the semiconducting CNT depends on its diameter and is described as follows [25],

$$E_{gap} = 2V_{pp\pi}a_{c-c} / d\,, \tag{1.2}$$

where $V_{pp\pi}$ is Slater–Koster π tight-binding matrix element which is one of the Slater–Koster parameters for $sp^3$ tight-binding, $a_{c\text{-}c}$ is the nearest neighbor distance between C-C bonds (0.142 nm) and d is the diameter of the CNT, which can be calculated using the following equation [25, 32, 33],

$$d = \sqrt{3}\, a_{c-c} \sqrt{n^2 + mn + m^2} \,/ \pi \tag{1.3}$$

### 1.4.1 Electronic Band Structure

#### A. Crystal Lattice and Reciprocal Lattice

Lattice is used to describe arrangement of atoms or molecules in a crystalline liquid or solid. The primitive cell of a carbon nanotube lattice can be described from the unit vectors [22]:

$$\vec{a}_1 = \frac{a}{2}\left(\sqrt{3}\hat{x} + \hat{y}\right) \text{ and } \vec{a}_2 = \frac{a}{2}\left(\sqrt{3}\hat{x} - \hat{y}\right), \tag{1.4}$$

where $\vec{a}_1$ and $\vec{a}_2$ are the unit cell vectors and a is the lattice constant, a = $\sqrt{3}\, a_{c\text{-}c}$.

The reciprocal lattice is a lattice in the Fourier space associated with the crystal lattice. The reciprocal lattice vectors, $\vec{b}_1$ and $\vec{b}_2$ are given as follows [22, 34]:

$$\vec{b}_1 = \frac{2\pi}{a}\left(\frac{1}{\sqrt{3}}\hat{k}_x + \hat{k}_y\right) \text{ and } \vec{b}_2 = \frac{2\pi}{a}\left(\frac{1}{\sqrt{3}}\hat{k}_x - \hat{k}_y\right) \tag{1.5}$$

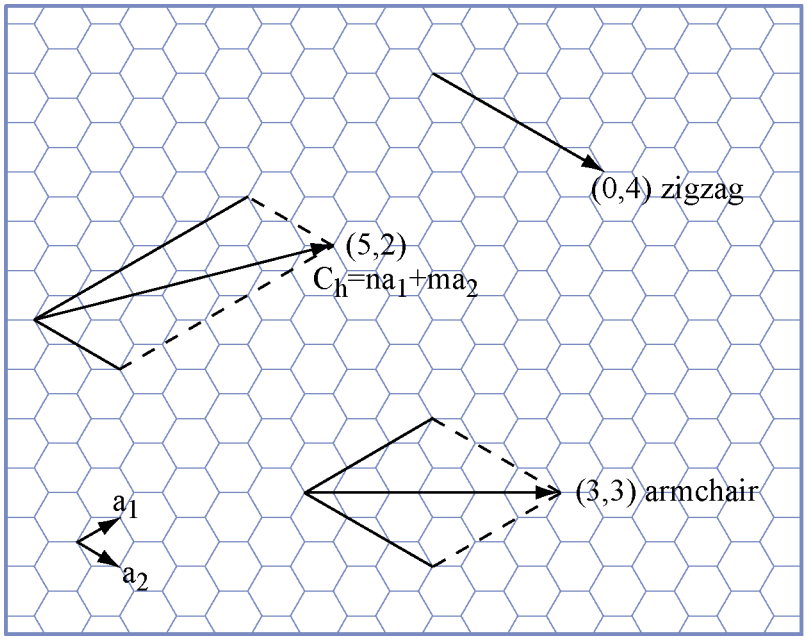



Figure 1.4: Schematic representation of a chiral vector in the crystal lattice of a carbon nanotube.

Figure 1.5 shows plots of the crystal lattice structure and reciprocal lattice structure for a carbon nanotube with a chiral vector (4,3) generated using MATLAB from the chiral vector and the unit vectors from Eqs. (1.4) and (1.5).

### B. Energy dispersion relation

The energy dispersion relation defines relationship between the energy, E and wave vector, k. The energy dispersion relation for carbon nanotubes can be calculated from the electronic structure of graphene. The energy dispersion relation of a two-dimensional graphene is given by [35-37],

$$E_{2D}(\vec{k}) = \pm V_{pp\pi}\left\{3 + 2\cos(\vec{k}\cdot\vec{a}_1) + 2\cos(\vec{k}\cdot\vec{a}_2) + 2\cos\left[\vec{k}\cdot(\vec{a}_1 - \vec{a}_2)\right]\right\}^{1/2}, \tag{1.6}$$

where $\vec{k}$ is the wave vector.

One-dimensional (1D) energy band can be derived from Eq. (1.6) for single-walled carbon nanotubes (SWCNTs) as follows [22, 25, 34],

$$E_{1D}(k) = \pm V_{pp\pi}\left\{1 + 4\cos(\frac{\sqrt{3}k_x}{2}a)\cos(\frac{k_y}{2}a) + 4\cos^2\left(\frac{k_y}{2}a\right)\right\}^{1/2}, \tag{1.7}$$

where the wave vectors $k_x$ and $k_y$ are obtained using the following relation,

$$\vec{k}(k_x, k_y) = \left(k\frac{\vec{K}_2}{|K_2|} + q\vec{K}_1\right) \qquad \text{for } -\frac{\pi}{|T|} < k < \frac{\pi}{|T|} \text{ and } q = 1, \ldots, N, \tag{1.8}$$

where k is the magnitude of the wave vector along the nanotube axis, |T| is the magnitude of the translational vector and N is the number of hexagons within a unit cell. |T| and N are given by [22, 25],

$$|T| = \frac{\sqrt{3}\pi d_t}{d_R}, \qquad N = \frac{2\left(n^2 + nm + m^2\right)}{d_R} \tag{1.9}$$

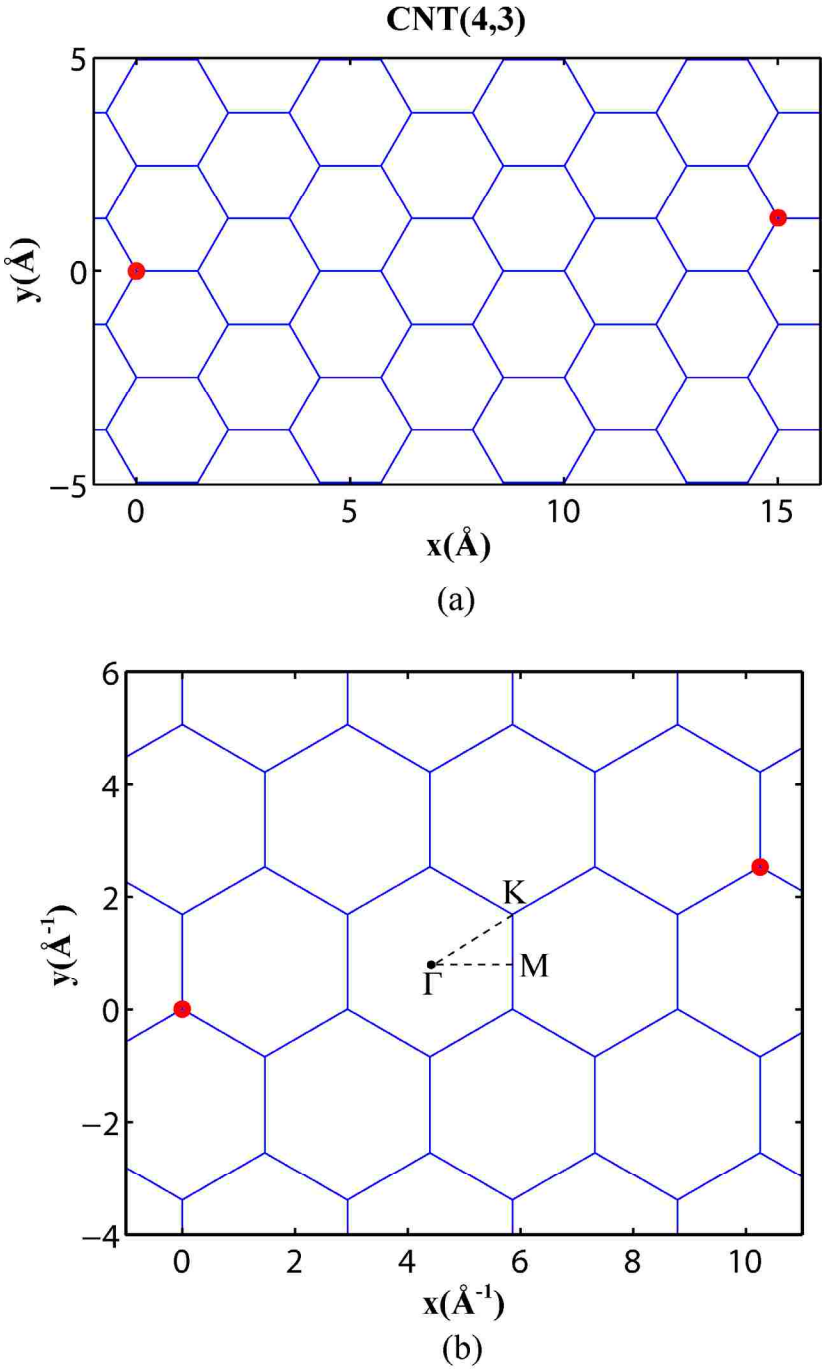



Figure 1.5: Schematic representation of (a) crystal lattice and (b) reciprocal lattice of a carbon nanotube with chiral vector (4,3).

where $d_R$ is the greatest common divisor of (2n+m) and (2m+n) and $d_t$ is the diameter of the CNT. $\vec{K}_1$ and $\vec{K}_2$ denote the allowed reciprocal wave vectors along the tube and circumference axis given by [22, 34],

$$\vec{K}_1 = \frac{(2n+m)\vec{b}_1 + (n+2m)\vec{b}_2}{Nd_R}, \qquad \vec{K}_2 = \frac{m\vec{b}_1 - n\vec{b}_2}{N} \tag{1.10}$$

Figure 1.6 shows the plot of wave vector in k-space (momentum space) for a CNT with chiral vectors (a) (4,2) and (b) (8,2). The reciprocal Bravais lattices are lines, which mean that carbon nanotube is a 1D material. Unlike CNT (4,2), the wave vector of CNT (8,2) passes through K point in the 2D Brillouin zone of graphene. Figure 1.7 shows the plot of the energy band diagram in k-space for a CNT with chiral vectors (a) (4,2) and (b) (8,2).

### 1.4.2 Density of States

The k-vectors in momentum (k) space depend on vectors $K_1$ and $K_2$ as shown in Fig. 1.6. It also represents the area in the momentum space for each state (each single line), which is $A_p^{1\text{-state}} = \hbar^2|K_1||K_2|/2$ and a differential area as $dA_p = \hbar^2|K_1|dk$, where dk is in the direction of $K_2$ and ħ is the Planck Constant (h) divided by 2π. The density of states per unit energy is obtained as follows [38-40],

$$D(E)dE = 2\frac{dA_p}{A_p^{1-state}} = \frac{4}{\hbar^2|K_1||K_2|}\hbar^2|K_1|\frac{dk}{dE}dE = \frac{2|T|}{\pi}\left(\frac{dE}{dk}\right)^{-1}dE \tag{1.11}$$

A combination of Eq. (1.7) for 1D energy dispersion and Eq. (1.11) for density of states can be used to plot the density of states for any chiral vector of carbon nanotube. Figure 1.8 shows density of states plots for a CNT (4,2) and CNT (8,2) abtained from MATLAB. Each peak in Fig. 1.8 is called a Van Hove Singularity and its respective energy represents a conduction energy-band minimum value. The total number of Van Hove Singularities is the number of bands a CNT has. There is a band gap in Fig. 1.8 (a), which means the CNT (4,2) is semiconducting and there is a finite value of the density of states at the Fermi level in Fig. 1.8 (b) which means the CNT (8,2) is metallic.

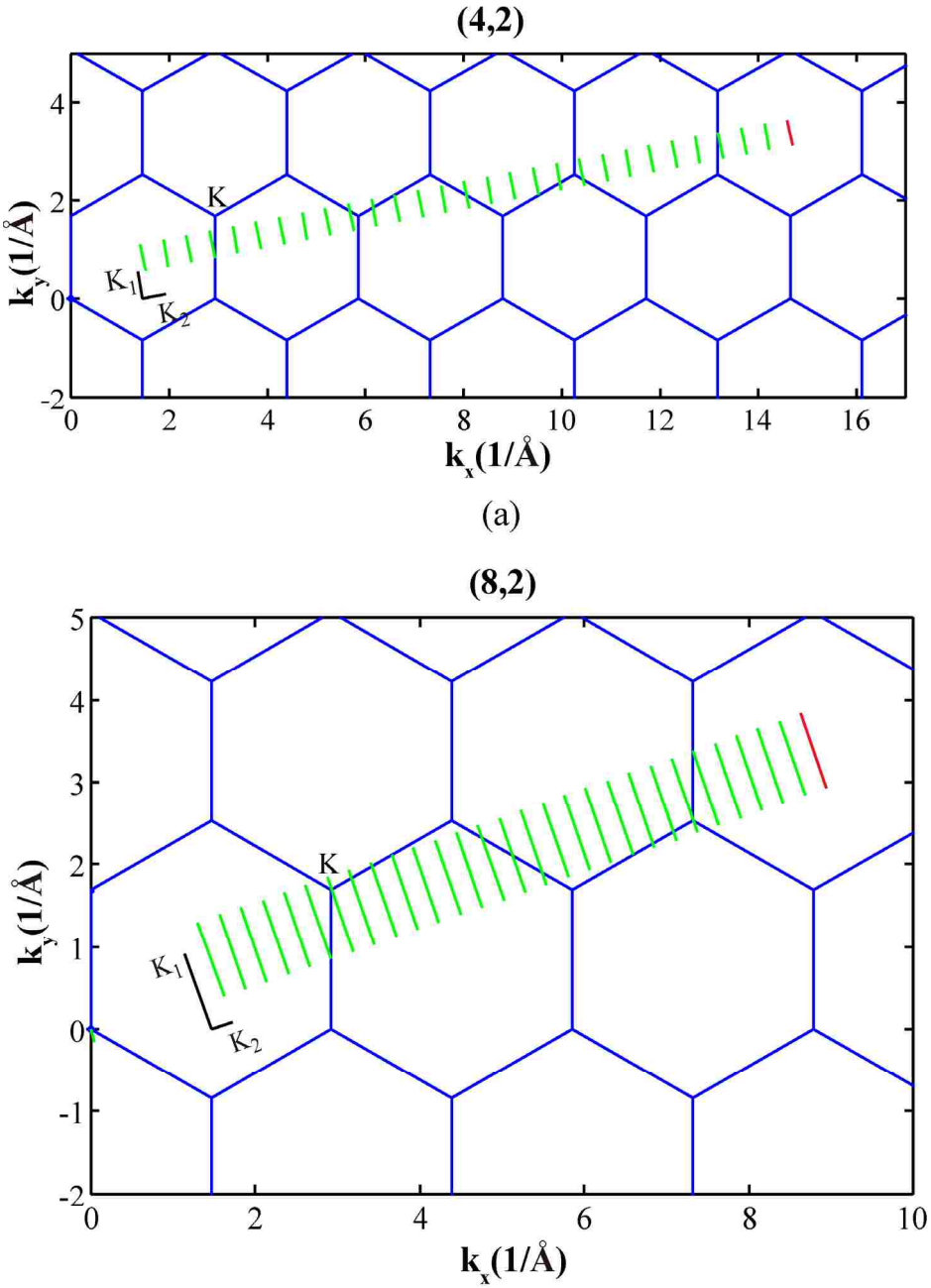



Figure 1.6: Plot of the allowed wave vectors in k-space for a CNT with (a) chiral vector (4,2) and (b) chiral vector (8,2).

Figure 1.7: Plot of the energy band diagram in k-space for a CNT with (a) chiral vector (4,2) and (b) chiral vector (8,2). **Note**: Bang gap is the distance between the top of the valence band and the bottom of the conduction band marked by 1 in (a).

Figure 1.8: Plot of the density of states for a CNT with (a) chiral vector (4,2) and (b) chiral vector (8,2).

It is shown from Figs. 1.6, 1.7 and 1.8 that the wave vectors of CNT (4,2) do not pass through K point in the 2D Brillouin zone of graphene, there is a band gap and thereis no state in the band gap. Therefore, CNT (4,2) is a semiconductor. Some of the wave vectors of CNT (8,2) pass through K point in the 2D Brillouin zone of graphene, there is no band gap and there is a finite state in the band gap. Therefore, CNT (4,2) is metallic.

## 1.5 Applications of CNTs in Integrated Circuits

Whereas semiconducting CNTs found applications in making CNT-FETs, metallic CNTs have distinct advantages compared with metal wires for interconnection in integrated circuits.

### 1.5.1 Applications of Semiconducting Carbon Nanotubes

Studies have demonstrated that semiconducting CNTs have excellent electrical properties, including long mean free path (~0.7μm) and high electron mobility [28, 41, 42]. Experiments with CNT-FETs [7, 15, 43] have further demonstrated that transistors based on semiconducting CNTs have large transconductance, which indicates a great potential for sub-nm integrated circuits as demonstrated through the fabrication of five-stage ring oscillator circuit by Chen et. al. [44].

It has been suggested that high-κ dielectrics are essential for future transistors due to low leakage currents and reduced power dissipation [45-47]. However, a fundamental problem for conventional semiconductors is the degradation of electrical properties due to carrier scattering mechanisms introduced at the high-κ film semiconductor interface [48]. Recently, Javey et al. [49-52] have shown that CNT-FETs can be operated in ballistic range with high-κ dielectrics, thereby opening the door to ultrafast devices since both the ballistic transport of electrons and high-κ dielectrics facilitate high on-current that is directly proportional to the speed of a transistor.

Early CNT-FETs were fabricated on oxidized Si substrates [7, 53]. The poor gate coupling due to the thick SiO2 layer and back gate geometry limited their applications. However, in 2002, the implementation of top-gate geometry [15, 16] made the CNT-FET a more promising candidate for next generation field-effect transistors. Both n-type CNT-

FETs and p-type CNT-FETs were made [52] and demonstrated for performance similar to current MOSFETs. Additional improvements in the metal-CNT contact resistance at the source and drain ends have led improved CNT-FET performances [51, 54]. Now with improved processing techniques, CNT-FETs with very high ON/OFF switching ratio and high carrier mobility have been fabricated [55-59]. In addition, fabrication of inverters which are composed of n-type and p-type CNT-FETs were also reported in [60, 61]. Recently, Zhang et al. [62] proposed a doping-free fabrication of CNT-based ballistic complementary metal-oxide semiconductor (CMOS) devices and circuits, which are compatible with current CMOS fabrication processes. This work may lead to the fabrication of complex CNT-based integrated circuits.

### 1.5.2 Applications of Metallic Carbon Nanotubes

Metallic CNTs have attracted significant attention because their current carrying ability is remarkable. Ballistic transport of electrons has been observed and values for the conductance that approaches the theoretical limit ($4e^2/h$)* [28] have been measured at small biases [63]. Metallic CNTs hold promise as interconnects in sub-nm CMOS circuits because of their low resistance and strong mechanical properties. An emerging problem with interconnects in sub-nm CMOS technology is the breakdown of copper wires due to electromigration when current densities exceed $10^6$ A/cm$^2$ [64]. Preliminary work [65, 66] have shown that an array of nanotubes can be integrated with silicon technology and holds promise as vertical vias to carry more than an order of magnitude larger current densities than conventional vias. Wei et al. [9] have demonstrated that MWCNTs can carry current densities approaching $10^{10}$ A/cm$^2$. Metallic CNTs are excellent wires, with near-perfect experimentally measured conductance. This is because surface scattering, disorder, defects and phonon scattering, which lead to a decrease in conductance, have negligible effects in metallic CNTs, especially when the size of the conductor is shrinking. The reasons for this are the following.

The acoustic phonon mean free paths in CNTs are longer than a micron [67]. The

* $4e^2/h = 155uS$

dominant scattering mechanisms are due to zone boundary and optical phonons with energies of approximately 160 and 200 meV; but scattering with these phonons at room temperature is ineffective at small biases [68].

In a silicon field effect transistor, there is significant scattering of electrons due to the disordered nature of the Si–SiO2 interface. However, the CNT has a crystalline surface without disordered boundaries [68].

Any potential that is long-ranged compared with the CNT lattice constant will not effectively couple the two crossing sub-bands because of lack of wave vector components in the reciprocal space [69].

The electrons in the crossing sub-bands of carbon nanotubes have a large velocity of 8×105 m/s at the Fermi energy. There are only two sub-bands at the Fermi energy. These two facts make the electron reflection probability due to disorder and defects small [36, 69].

## 1.6 Synthesis of Carbon Nanotubes

At present carbon nanotubes are being synthesized using the following techniques: arc discharge, laser ablation, high-pressure carbon monoxide (HiPCO) and chemical vapor deposition (CVD) methods.

Arc discharge [70], laser ablation [71] and chemical vapor deposition (CVD) [72] are popular methods to produce CNTs. Arc discharge method creates CNTs through arc vaporization of two carbon rods placed end to end, separated by a small gap (~mm), in an enclosure that is usually filled with inert gas at low pressure. In this method, carbon nanotubes are produced at the cathode crater [70]. Laser ablation can be carried out in a horizontal flow tube under a flow of inert gas at controlled pressure. In this set-up, the flow tube is heated to ~1200°C by a tube furnace. Laser pulses enter the tube and strike a target consisting of a mixture of graphite and a metal catalyst such as Co, Pt, Ni, Cu, etc. Carbon nanotubes condense from the laser vaporization plume and are deposited on a collector sitting outside of the furnace [71]. Arc discharge and laser ablation are modified physical vapor deposition (PVD) techniques and are high temperature and low production

processes, which are more suitable for laboratory research. Chemical vapor deposition (CVD) has become the most important commercial approach for synthesis of CNTs. It is also suitable to produce on-chip nanotubes directly, which provides a convenient way for further device fabrication [73]. First, the gaseous carbon molecules, such as methane, carbon monoxide are heated in a furnace and break into atomic carbons [74]. Then the atomic carbons diffuse toward the substrate coated with catalyst particles forming carbon nanotubes. Carbon nanotube synthesis by CVD is essentially a two-step process. The first step is a preparation of patterned catalyst, such as clusters of Ni, Fe and Co. The next step is a synthesis of the nanotube by heating up the substrate in a carbon rich gaseous environment. In all of these methods, the generation of free carbon atoms and the precipitation of dissolved carbon from catalyst particles are involved [25]. The growth terminates when the catalyst particle gets poisoned by the impurities or the stable metal carbide is formed.

Besides these three popular methods, there are other proposed methods to synthesize CNTs, such as flame synthesis, CoMoCat method and high pressure carbon monoxide (HiPCO). Recent work has shown that flame synthesis is an inexpensive large-scale method to produce single-walled carbon nanotubes [75, 76]. In a flame synthesis process, the hydrocarbon fuel combusts to generate enough heat to trigger the process, and to form small aerosol metal catalyst islands. Single-walled carbon nanotubes grow in these catalyst islands in the same way as in the arc discharge and laser ablation processes [77, 78].

CoMoCat method produces SWCNTs of high quality at very high selectivity and with a remarkably narrow distribution of tube diameters. The technique is based on a unique Co-Mo catalyst formulation that inhibits the formation of undesired forms of carbon. During the reaction, cobalt (Co) is progressively reduced from the oxidic state to the metallic form. The strategy used in the CoMoCAT method is to keep the active cobalt stabilized in a non-metallic state by interaction with molybdenum oxide ($MoO_3$). When exposed to carbon monoxide, the Co-Mo dual oxide is carburized, producing molybdenum carbide ($Mo_2C$) and small metallic Co clusters, which remain in a high state of dispersion and result in high selectivity towards SWCNT of very small diameter [79].

This catalytic synthesis of SWCNTs uses a continuous-flow gas phase using CO as the carbon source and $Fe(CO)_5$ as the iron-containing catalyst precursor. Single-walled carbon nanotubes are synthesized when the two gases flow through a heated reactor. Diameter of the nanotubes can be roughly selected by controlling the pressure of carbon monoxide (CO). Single-walled carbon nanotubes with 0.7 nm in diameter, which are expected to be the smallest SWCNTs, have been produced by this method [80].

## 1.7 CNT Based Circuit Modeling

As discussed in Section 1.5, CNT-FETs and metallic CNT wires show performance metrics significantly above those of Si MOSFETs and metal interconnect wires, respectively. Liang et al. [81] fabricated SWCNT CNT-FETs in which MWCNTs are used as local interconnects, making a successful first step towards CMOS circuits fabricated entirely from carbon nanotubes. However, studies of individual CNT-FET and CNT wire are not comprehensive enough to enable conclusions about development of large-scale CNT based integrated circuits. The viability of CNT-FET circuits depends on the behavior of logic gates that are composed of multiple CNT-FETs and used in larger scale circuits. Therefore, circuit models including device models and interconnects model are necessary to predict the behavior of CNT based circuits. Furthermore, like the great help by the CMOS models in optimization of CMOS circuits design, it will be helpful to optimize the CNT based circuits design by utilizing the CNT-FET and CNT interconnect models. As a result, CNT-FET modeling and CNT interconnects modeling are the current focus of most active research in CNT based integrated circuits design.

### 1.7.1 CNT-FET Modeling

A good amount of work on modeling carbon nanotube field-effect transistors (CNT-FETs) has been reported [10, 15, 51, 53, 82-90]. However, these models are still numerical-based and require a mathematical/software realization. Recently, Srivastava et al. [91] have obtained an analytical solution of current transport model for the CNT-FET for analysis and design of CNT-FET based integrated circuits.

### 1.7.2 CNT Interconnect Modeling

A model describing the electromagnetic field propagation along a CNT is indispensable in order to study the interconnection performance of CNT while comparing with traditional metal interconnects. Three theories are used to build different models. Lüttinger liquid theory [92] describes interacting electrons (or other fermions) in one-dimensional conductor and is necessary since the commonly used Fermi liquid model breaks down in one-dimension. Burke [93, 94] regards that electrons are strongly correlated when they transport along the CNT and proposed a transmission line model based on the Lüttinger liquid theory. Another transmission line model was built based on Boltzmann Transport Equation (BTE) [95]. Two-dimensional electron gas, where the charged particles are confined to a plane and neutralized by an inert uniform rigid positive plane background was studied by Fetter [96, 97]. Based on the work of Fetter [96, 97], Maffucci et al. [98] investigated electron transport along the CNT and proposed a third model, fluid model. The first model is based on quantum dynamics concepts; the second model requires solving the Boltzmann Transport Equation; the third model has been developed within the framework of the classical electrodynamics and is simple on concepts and mathematical modeling.

## 1.8 Scope of Research

In this dissertation, we first introduced a channel length modulation parameter, $\lambda$ in current transport equation for saturation region, which was recently derived by Srivastava et al. [91]. By introducing this parameter, the calculated I-V curve fits the experiments results better. We then derive and analyze the dynamic behavior of CNT-FET based on the current transport equations. We plotted the calculated capacitances for linear and saturation regions of operation of CNT-FET. Thus, we have the models to describe both static and dynamic behaviors of a CNT-FET, which will be discussed in Chapter 2. . In this chapter, we also use Verilog-AMS language to describe the developed non-ballistic CNT-FET models for simulations in Cadence/Spectre and study the CNT based circuits, such as inverter pair, ring oscillator. Furthermore, we have attempted to develop a current transport equation for the ballistic CNT-FETs and shown that computed I-V characteristics are fairly close to experimental I-V characteristics.

In Chapter 3, we make modification in two-dimensional fluid model of electron transport in carbon nanotubes to include electron-electron repulsive interaction and built a semi-classical one-dimensional fluid model. By using this model, we calculate the transmission line parameters for the metallic SWCNT. We also applied the one-dimensional fluid model to study the MWCNT and SWCNT bundle interconnect wires and analyzed their performances in Chapter 4.

The utilization of CNT wires in on-chip inductors is studied in Chapter 5. In Chapters 6 and 7, we introduced some CMOS concepts in CNT based circuits, such as the energy recovery techniques and fault modeling, respectively to study the performances of CNT based circuits.

Conclusion, limitations and future scope for further advancement of research conducted are summarized in Chapter 8.

# CHAPTER 2*

# CARBON NANOTUBE FIELD-EFFECT TRANSISTOR

The field-effect transistor is a type of transistor that relies on an electric field to control the conductivity of a "channel" of one type of charge carrier in a semiconductor material. Devices such as the MOSFET achieve full conduction under the influence of gate voltage when the channel is inverted and current flows between drain and source terminals. The carbon nanotube field-effect transistor (CNT-FET) works under the same principle as the MOSFET. It achieves this operation by using a semiconducting SWCNT as the conducting channel between the source and the drain. The conductivity of the channel depends on the applied gate voltage. For a given gate voltage above a threshold voltage, drain current is obtained by varying the drain to source potential.

## 2.1 Background of CNT-FETs

Rapid development of carbon nanotube field-effect transistor has occurred especially after the first transistors were reported in 1998 by Dekker's group [7] and others [53]. Such devices used semiconducting silicon substrate (covered by a layer of $SiO_2$) as a back gate and platinum (Pt) electrodes for the drain and source terminals. Carbon nanotubes were produced by laser ablation synthesis [99] and dispersed randomly in the oxidized Si-substrate with contacts for predefined electrodes, resulting in an undefined number of contacts being bridged with CNTs. Consequently, the use of chemical vapor deposition of methane on patterned substrate allowed then the implementation of carbon nanotube growth only in specific catalyst islands. As a result, some of these catalyst metal islands are bridged with CNTs [73].

As mentioned above, early CNT-FETs devices were fabricated on oxidized Si

* Part of the work is reported in the following publications:

1. A. Srivastava, J. M. Marulanda, Y. Xu and A. K. Sharma, "Current transport modeling of carbon nanotube field effect transistors," *physica status solidi (a),* vol. 206, no. 7, pp. 1569-1578, 2009.
2. Y. Xu and A. Srivastava, "Dynamic response of carbon nanotube field effect transistor circuits," in *Proc. 2009 NSTI Nanotechnology Conference and Expo*, Houston, TX, May 3-7, 2009, vol. 1, pp. 625-628.
3. Y. Xu and A. Srivastava, "Transient behavior of integrated carbon nanotube field effect transistor circuits and bio-sensing applications," in *Proc. of SPIE: Nano-, Bio, and Info-Tech Sensors and Systems*, San Diego, CA, USA, March 9-13, 2009, vol. 7291, pp. 72910I-72910I-11.

substrate, the gate coupling and control of the drain current was very poor due to the thick $SiO_2$ layer and back gate geometry [7, 53]. In 2002, major improvement was observed after the implementation of CNT-FETs using the top-gate geometry [100]. Transconductance of 3.25 μS and subthreshold slope of 130 mV/decade were found, which were much higher than the values in alternate devices [101] with transconductance of only 0.3 μS. Further enhancement in performance was obtained by using high-κ dielectric [52] and electrolyte gating [102, 103]. Javey et al. [52] reported the integration of top gated p-type CNT-FETs using the high-κ dielectric material $ZrO_2$ (k = 25) as the gate oxide, achieving a transconductance and subthreshold slope of 12 μS and 70 mV/decade, respectively. Electrolyte gating, first introduced by Krüger et al. [104], involves applying a voltage at the electrolyte gate which creates an electrochemical potential between the electrolyte and the device. The leakage current between the electrolyte and the electrodes is negligible and the electrolyte behaves as an insulating liquid gate [102]. Subthreshold slopes of 80 mV/decade and hole mobility of 1500 $cm^2$/Vsec were reported by Rosenblatt et al. [102]. Later on, hole mobility of 2600 cm2/Vsec and subthreshold slopes of 62 mV/decade [103], corresponding to a gate efficiency parameter, $\alpha = 0.97$ (the shift in Fermi level for a change in the gate voltage of $\Delta V_{gb} = 1V$), which is approaching the ideal efficiency value of 1, were also reported. Recently, Javey et al. [49-52] have shown that CNT-FETs can be operated in ballistic range with high-κ dielectrics, thereby opening the door to ultrafast devices since both the ballistic transport and high-κ dielectrics facilitate high on-current that is directly proportional to the speed of a transistor.

Figure 2.1 shows the typical vertical cross-section of a CNT-FET. According to the types of contact between source/drain metals and the semiconducting CNT, the CNT-FETs can be categorized as: (a) Schottky Barrier CNT-FETs (SB-CNT-FETs), with a Schottky contact between metal and semiconducting CNT at source and drain regions, and (b) Repress Barrier CNT-FETs (RB-CNT-FETs), with either decreased Schottky barrier in the contact between metal and semiconducting CNT at source and drain regions (by using certain techniques which reduce the work function at room temperature [51] such as by the exposure of palladium (Pd) to molecular hydrogen) or with Ohmic contact

between metal and semiconducting CNT at source and drain regions. Schottky Barrier CNT-FETs [16, 53] show large barriers at the electrode-nanotube interfaces with strong dependence on the height of these barriers. Repress Barrier CNT-FETs [51, 105] show small, negative, or no barrier at the electrode-nanotube interfaces. The second type of transistors allows a device modeling approach similar to current MOSFETs models, so-called MOSFET-like CNT-FETs. This type of CNT-FETs were achieved by either using heavily doped CNT sections as source and drain [105, 106] or using metals with proper work functions to contact the semiconducting SWCNT, for example, scandium (Sc) for n-type CNT-FETs [62] and palladium (Pd) for p-type CNT-FETs [51, 107].

Both of the two CNT-FETs can also be categorized as non-ballistic and ballistic CNT-FETs [7, 15, 28, 41-43, 49-52, 108]. One of the promising properties of CNT-FET is its absence of scattering in the channel, which is ballistic transport. Studies have demonstrated that semiconducting CNTs have excellent electrical properties, including long mean free path (~0.7μm) and high electron mobility [28, 41, 42]. Experiments with CNT-FETs [7, 15, 43] have further demonstrated that transistors based on semiconducting CNTs have large transconductance, which indicates a great potential for sub-nm integrated circuits.

With the advancement in fabrication technology of CNT-FETs, efforts have also been made in modeling of the current transport behavior and models have been developed for the design of CNT-FET based logic circuits [10, 85, 89]. An analytical model has been built by Srivastava et al. [91] to characterize the current transport in CNT-FETs for the analysis and design of integrated circuits. We have used these current transport equations to generate I-V characteristics for CNT-FETs using different chiral vectors (n,m) of carbon nanotubes. In this work, based on the static model of Srivastava et al. [91], we have built a dynamic model to describe the transition behavior of CNT-FETs and using these models we have studied performances of some basic CNT-FETs circuits, such as the inverter and ring oscillator. In addition, the current equation of ballistic CNT-FET is also studied.

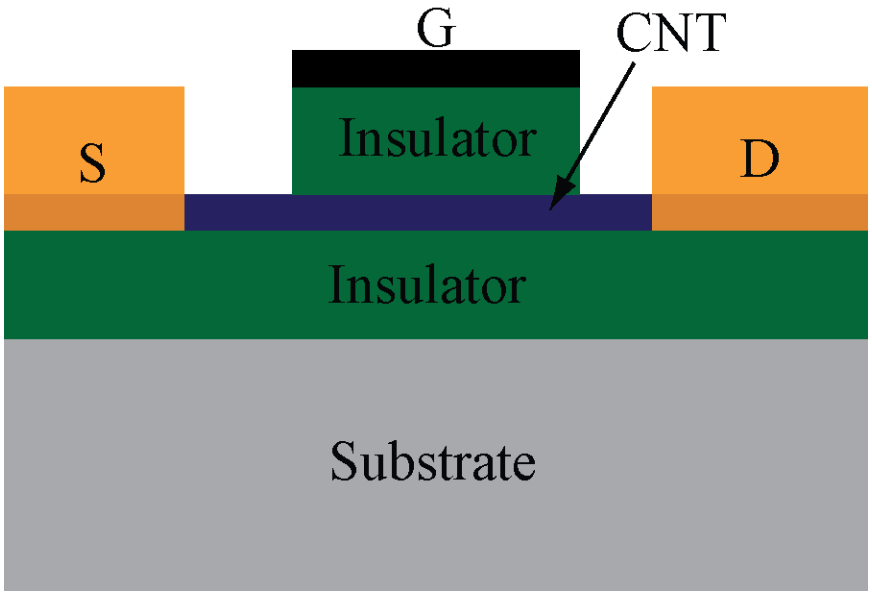



Figure 2.1: Typical vertical cross-section of a CNT-FET. **Note**: Insulators in the figure are $SiO_2$ or high-κ dielectric.

## 2.2 Surface Potential of CNT-FETs

Figure 2.2 (a) and (b) show the basic cross section of a Schottky Barrier CNT-FET and MOSFET-like CNT-FET, respectively, including the charge distributions. Gate oxide and $SiO_2$ are corresponding to the insulators in Fig. 2.1. Both of these two structure can be utilized in realizing non-ballistic and ballistic CNT-FETs [7, 15, 28, 41-43, 49-52, 108] since the necessary and sufficient condition that the carrier transport in a CNT-FET is ballistic is that the length of channel (length of CNT between source and drain) is shorter than the mean free path of carrier in it. Figure 2.2 (c) shows the corresponding potential distributions between the gate and the substrate. In Fig. 2.2 (a) and (b), charge distributions are explained as follows: the charge on the gate is $Q_g$, the charges in the oxide layers are $Q_{01}$ and $Q_{02}$, the charge inside the CNT is $Q_{cnt}$ and the charge in the substrate is $Q_{subs}$. In Fig. 2.2 (c), six different potential distributions are shown, which are also described as follows: the voltage between the gate and the substrate (back gate) is $V_{gb}$, the potential drop across the oxides are $\psi_{ox1}$ and $\psi_{ox2}$, the surface potential in the substrate with respect to the back gate, $\psi_{subs}$, the potential across the CNT, $\psi_{cnt}$ and the work function difference between the gate and the substrate materials is $\Phi_{ms}$.

Using Kirchoff's voltage law, the potential balance and charge neutrality condition, we can write for the Fig. 2.2,

$$V_{gb} = \phi_{ms} + \psi_{subs} + \psi_{ox2} + \psi_{cnt} + \psi_{ox1} \tag{2.1}$$

$$Q'_g + Q'_{01} + Q'_{cnt} + Q'_{02} + Q'_{subs} = 0 \tag{2.2}$$

The prime in Eq. (2.2) denotes the charge per unit area. $\phi_{ms}$ is divided in two parts and expressed as follows,

$$\phi_{ms} = \phi_{mc} + \phi_{cs} \tag{2.3}$$

where $\phi_{mc}$ and $\phi_{cs}$ are the work function differences between the metal gate and carbon nanotube materials and the carbon nanotube and substrate materials, respectively.

Combining potentials $\psi_{cnt}$, $\psi_{ox2}$, $\phi_{cs}$ and $\psi_{subs}$ into a single potential, $\psi_{cnt,s}$, Eq.(2.1)

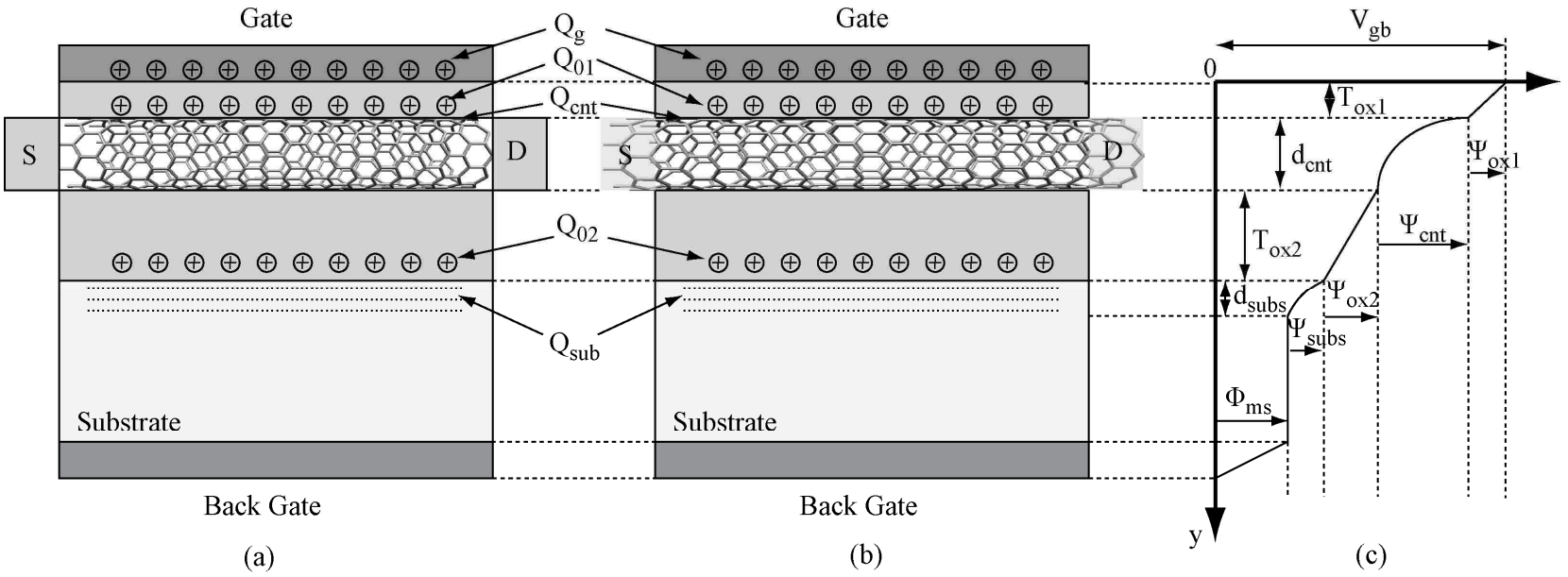



Figure 2.2: (a) Plot of the charges from the gate to the substrate for Schottky Barrier CNT-FET, (b) Plot of the charges from the gate to the substrate for MOSFET-like CNT-FET and (c) plot of the potential distribution from the gate to the substrate in a CNT-FET [91].

can be re-written as follows,

$$V_{gb} = \phi_{mc} + \psi_{ox1} + \psi_{cnt,s} \tag{2.4}$$

where $\psi_{cnt,s}$ describes the surface potential at the interface of the gate oxide and the carbon nanotube with respect to the back gate.

The electric field in terms of the charge distribution can be written from the Maxwell's third equation [109] and is given by,

$$\nabla(\varepsilon E) = \rho_v \tag{2.5}$$

where ε is the permittivity of the material, E is the electric field and $\rho_v$ is the charge per unit volume. Assuming that the electric field in Fig. 2.2 (a) is constant through the gate oxide region and at the bottom edge of the carbon nanotube, Eq. (2.5) can be integrated between the gate and the bottom edge of the carbon nanotube, that is in Fig. 2.2 (a) from $y = 0$ to $y = T_{ox1} + d_{cnt}$, to obtain the following Eq. (2.6), where $d_{cnt}$ is the diameter of the carbon nanotube. In this derivation, we have assumed that the carbon nanotube has a relative permittivity, $\varepsilon_{cnt}$. We can write Eq. (2.6) as follows,

$$\varepsilon_{cnt} E_{cnt} - \varepsilon_{ox1} E_{ox1} = Q'_{01} + Q'_{cnt} \tag{2.6}$$

where $E_{cnt}$ and $E_{ox1}$ are the electric fields along the y-axis across the carbon nanotube and gate oxide, respectively.

We assume that any charge applied at the gate is compensated only by an induced charge in the carbon nanotube as follows:

$$\Delta Q'_g = -\Delta Q'_{cnt} \tag{2.7}$$

Furthermore, there is a specific gate voltage, called the flat band voltage, $V_{fb}$ [110], when applied at the gate with respect to the back gate; it compensates for the band bending at the gate oxide and carbon nanotube interface. Under this flat band condition, the electric field at the bottom edge of the carbon nanotube, $E_{cnt}$ in Eq. (2.6) can be

neglected. Under this assumption and replacing $E_{ox1}$ with the potential gradient $-\frac{d\psi_{ox1}(y)}{dy}$ in Eq. (2.6) we obtain,

$$\varepsilon_{ox1}\frac{d\psi_{ox1}(y)}{dy} = Q'_{01} + Q'_{cnt} \tag{2.8}$$

By integrating Eq. (2.8) through the gate oxide region, that is in Fig. 2.2(a) from y = 0 to y = $T_{ox1}$, we can write an expression for the gate oxide potential as:

$$\psi_{ox1} = -\frac{Q'_{01} + Q'_{cnt}}{C'_{ox1}} \tag{2.9}$$

In Eq. (2.9), $C'_{ox1}$ is the gate oxide capacitance per unit area. Substituting Eq. (2.9) in Eq. (2.4), we obtain an expression for the gate voltage given by,

$$V_{gb} = \psi_{cnt,s} - \frac{Q_{cnt}}{C_{ox1}} + \phi_{mc} - \frac{Q_{01}}{C_{ox1}} \tag{2.10}$$

In Eq. (2.10), $Q_{cnt}$, $Q_{01}$ and $C_{ox1}$ are the total charges and capacitance, respectively, which are obtained by multiplying $Q'_{01}$, $Q'_{cnt}$, and $Q'_{02}$ with their respective areas. $C_{ox1}$, the capacitance between the gate and the carbon nanotube, can be redefined by considering the carbon nanotube to be a line of charge and the gate to be a planar conducting plate. Therefore, the gate oxide capacitance of thickness $T_{ox1}$ of a carbon nanotube of length L and radius r can be defined as follows [111],

$$C_{ox1} = \frac{2\pi\varepsilon_{ox1}L}{\ln\left(\frac{T_{ox1} + r + \sqrt{T_{ox1}^2 + 2T_{ox1}r}}{r}\right)} \tag{2.11}$$

In Eq. (2.10), the flat band voltage, $V_{fb}$ is:

$$V_{fb} = \phi_{mc} - \frac{Q_{01}}{C_{ox1}} \tag{2.12}$$

The gate voltage, $V_{gb}$ in Eq. (2.10) after combining with the Eq. (2.12) can be expressed as follows,

$$V_{gb} = \psi_{cnt,s} - \frac{Q_{cnt}}{C_{ox1}} + V_{fb} \tag{2.13}$$

In Eq. (2.13), $\psi_{cnt,s}$ can be explained as a control potential in the carbon nanotube in charge of shifting the energy band at the interface of the gate oxide and carbon nanotube.

In Eq. (2.13), the charge inside the carbon nanotube can be calculated using the relation $|Q_{cnt}| = qn_{cnt}L$, where $n_{cnt}$ is the carrier concentration per unit length inside the carbon nanotube, which was derived in [112] and is given by,

$$n_{cnt}(\eta) = \frac{8\sqrt{kT}}{\pi\sqrt{3}V_{pp\pi}a}\int_0^{\infty}\frac{kTx + E_c}{\sqrt{x(kTx + 2E_c)}}\left(1 + e^{x-\eta}\right)^{-1} dx \tag{2.14}$$

where a is the lattice constant, $V_{pp\pi}$ is Slater–Koster π tight-binding matrix element which is one of the Slater–Koster parameters for $sp^3$ tight-binding, k is Boltzmann's constant and T is the temperature. The parameter, η is given by:

$$\eta = \frac{E_F - E_c}{kT} \tag{2.15}$$

where $E_c$ is the conduction band minima.

Under two limiting cases, the charge inside the carbon nanotube can be described as in [112],

Limit 1, $\eta << -1$:

$$|Q_{cnt}| = qLN_c\, I e^{\frac{E_F - E_c}{kT}}, \tag{2.16}$$

Limit 2, $\eta >> 1$:

$$|Q_{cnt}| = qLN_c \frac{\sqrt{E_F^2 - E_c^2}}{kT}, \tag{2.17}$$

where

$$I = \sum_{A=0}^{\mathrm{int}\left(6\frac{E_c}{kT}\right)} \left\{ e^{-A}\sqrt{x\left(x+2\frac{E_c}{kT}\right)}\left[1 - \tfrac{1}{2}x + A + \tfrac{1}{2}\frac{E_c}{kT} + \tfrac{1}{6}x^2 - \tfrac{1}{6}\frac{E_c}{kT}x - \tfrac{1}{2}Ax + \tfrac{1}{2}\left(\frac{E_c}{kT}\right)^2 + \tfrac{1}{2}A\frac{E_c}{kT} + \tfrac{1}{2}A^2 - \tfrac{1}{4}A^2x + \right.\right.$$
$$+ \tfrac{5}{16}\left(\frac{E_c}{kT}\right)^3 + \tfrac{1}{6}A^3 - \tfrac{1}{24}x^3 + \tfrac{1}{24}\frac{Ec}{kT}x^2 - \tfrac{5}{48}\left(\frac{Ec}{kT}\right)^2 x + \tfrac{1}{2}A\left(\frac{Ec}{kT}\right)^2 + \tfrac{1}{2}A^2\frac{E_c}{kT} + \tfrac{1}{6}Ax^2 - \tfrac{1}{6}A\frac{E_c}{kT}x\Big]$$
$$\left. + \tfrac{1}{2}\left(\frac{E_c}{kT}\right)^2\left[1 + A + \frac{E_c}{kT} + \tfrac{1}{2}A^2 - A\frac{Ec}{kT} - \tfrac{5}{8}\left(\frac{Ec}{kT}\right)^2\right]\ln\left[\frac{E_c}{kT} + \sqrt{kT} + \sqrt{kTx^2 + 2xE_c}\right]\right\}_{x=A}^{x=A+1}$$

and

$$N_c = \frac{8kT}{\pi\sqrt{3}V_{pp\pi}a}.$$

In order to effectively describe the potential inside the carbon nanotube, we need to determine the energy separation between the Fermi level and the conduction band at the interface of the gate oxide and carbon nanotube. Assuming a flat band energy level in the carbon nanotube, we can say that the Fermi level and the conduction band at the interface of the gate oxide and carbon nanotube will be shifted by an amount determined by $qV_{cb}$ and $q\psi_{cnt,s}$, respectively; where $V_{cb}$ is the induced potential between the carbon nanotube and the substrate due to the drain and source terminal voltages. The potential, $V_{cb}$ varies from $V_{sb}$ (source to back gate potential) to $V_{db}$ (drain to back gate potential). Figure 2.3 shows the energy band diagram from gate to substrate of a CNT-FET when (a) $V_{gb} = |V_{fb}|$ and (b) $V_{gb} > 0$ [91]. In Fig. 2.3(a), we have used hafnium dioxide ($HfO_2$) as the gate oxide, which is a high-κ dielectric insulator material. Furthermore, $\phi_0$ in Fig. 2.3(a) is the carbon nanotube surface potential, $\psi_{cnt,s}$ when $V_{gb} = V_{fb}$ and $\psi_{cnt} = 0$. $\phi_0$ is then given by,

$$\phi_0 = \psi_{ox2} + \psi_{subs} + \phi_{cs} \tag{2.18}$$

As it was previously done, by integrating Eq. (2.5) from y = $T_{ox1}+d_{cnt}$ to y = $T_{ox1}+d_{cnt}+T_{ox2}+d_{subs}$, where $d_{subs}$ is the thickness of $Q_{subs}$ in the substrate as shown in Fig. 2.2(a), we can write,

$$\varepsilon_s E_s - \varepsilon_{ox2} E_{ox2} = Q'_{02} + Q'_{subs} \tag{2.19}$$

where $\varepsilon_s$ is the permittivity of the substrate material. Assuming the electric field, $E_s$ is to be negligible deep inside the substrate and replacing $E_{ox2}$ with the potential gradient $-\frac{d\psi_{ox2}(y)}{dy}$ in Eq. (2.19), we obtain,

$$\varepsilon_{ox2} \frac{d\psi_{ox2}(y)}{dy} = Q'_{02} + Q'_{subs} \tag{2.20}$$

By integrating Eq. (2.20) from y = $T_{ox1}+d_{cnt}$ to y = $T_{ox1}+d_{cnt}+T_{ox2}$ in Fig. 2.2(a) we can obtain an expression for the second oxide potential as:

$$\psi_{ox2} = -\frac{Q'_{02} + Q'_{subs}}{C'_{ox2}} \tag{2.21}$$

The total capacitance $C_{ox2}$, which is the capacitance between the carbon nanotube and the substrate and can be obtained as follows [111]:

$$C_{ox2} = \frac{2\pi\varepsilon_{ox2} L}{\ln\left(\frac{T_{ox2} + r + \sqrt{T_{ox2}^2 + 2T_{ox2} r}}{r}\right)} \tag{2.22}$$

Assuming $Q_{subs}$ and $\psi_{subs}$ to be small compared to $Q_{02}$ and $\phi_{cs} + \psi_{ox2}$, we can rewrite Eq. (2.18) for $\phi_0$ as follows:

$$\phi_0 = \phi_{cs} - \frac{Q_{02}}{C_{ox2}} \tag{2.23}$$

We are interested in the separation between the Fermi level and conduction band at the interface of the gate oxide and carbon nanotube. Following the Fig. 2.3(a) we can

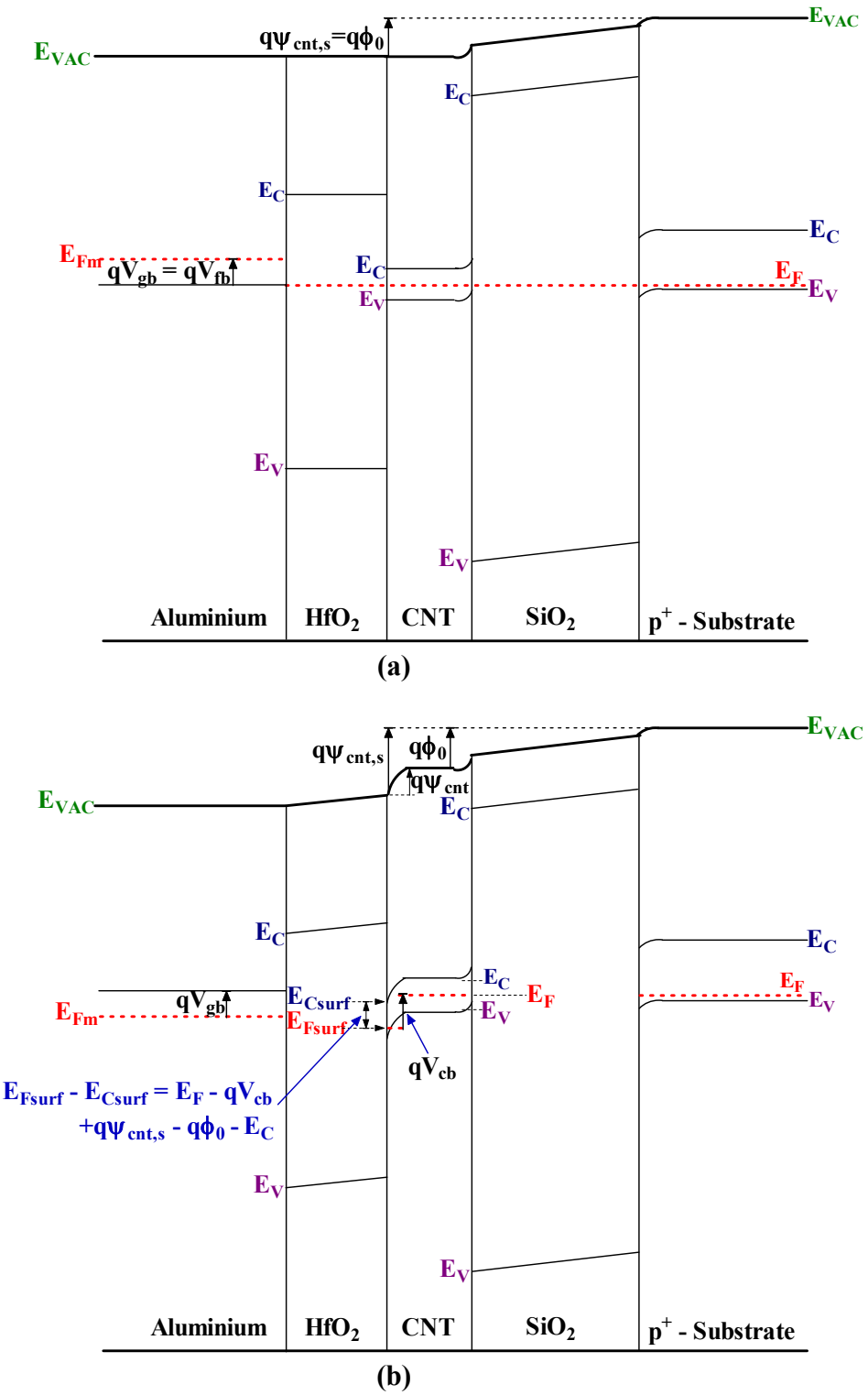



Figure 2.3: Energy band diagram of a two terminal CNT-FET for (a) $V_{gb} = V_{fb}$ and (b) $V_{gb} > 0$. Note: $HfO_2$ is the high-κ dielectric hafnium oxide [91].

observe that the conduction band of the carbon nanotube is shifted by an amount of $\psi_{cnt,s} - \phi_0$ which can be expressed through the following relation [110, 113],

$$E_{Csurf} = E_c - q\left(\psi_{cnt,s} - \phi_0\right) \tag{2.24}$$

where $E_{Csurf}$ is the conduction band energy at the interface of the gate oxide and carbon nanotube. The Fermi level at the interface, $E_{Fsurf}$ is shifted by an amount of $V_{cb}$ and is expressed as follows [110, 113],

$$E_{Fsurf} = E_F - qV_{cb} \tag{2.25}$$

From Eqs. (2.24) and (2.25) we can write following equation for intrinsic CNT:

$$E_{Fsurf} - E_{Csurf} = E_F + q\left(\psi_{cnt,s} - V_{cb} - \phi_0\right) - E_c \tag{2.26}$$

The shift in the Fermi level of the carbon nanotube due to impurity doping can be obtained as follows. The carrier concentration in a doped carbon nanotube is given by [91],

$$n_{cnt} = N_c I e^{\frac{E_F - E_c}{kT}} \tag{2.27}$$

The intrinsic carrier concentration, $n_{cnt,i}$ can be obtained by setting $E_F = 0$ in Eq. (2.27),

$$n_{cnt,i} = N_c I e^{\frac{-E_c}{kT}} \tag{2.28}$$

Using Eq. (2.28), we can rewrite Eq. (2.27) as follows:

$$E_F = kT \ln\left(\frac{n_{cnt}}{n_{cnt,i}}\right) \tag{2.29}$$

The carrier concentration in a doped carbon nanotube can also be obtained by adding an ionized impurity doping concentration, N in Eq. (2.28) as follows:

$$n_{cnt} = n_{cnt,i} + N \tag{2.30}$$

The ionized impurity concentration, N in Eq. (2.30) can be either donor atoms, $N_D$ or acceptor atoms, $N_A$.

In an intrinsic carbon nanotube, the Fermi level lies in the middle of the band gap; we can use Eq. (2.29) to express the shift in the Fermi level depending upon the doping. Furthermore, using Eq. (2.30) we can define a parameter $\Delta E_F$ given by,

$$\Delta E_F = \pm kT \ln\left(1 + \frac{N}{n_{cnt,i}}\right) \tag{2.31}$$

where $\Delta E_F$ is positive for an n-type carbon nanotube (donors impurity concentration, N = $N_D$) and negative for a p-type carbon nanotube (acceptors impurity concentration, N = $N_A$). Equation (2.31) is valid for $N \leq n_{cnt,i}(e^{Eg/2kT}-1)$ and the impurity concentration, N is limited by the maximum value of $|\Delta E_F|$ which can be determined from energy gap of the carbon nanotube as $\Delta E_F \leq E_g/2$. Thus, using Eq. (2.31) for the shift in the Fermi level, we can rewrite Eq. (2.26) for the n-type CNT-FET as follows:

$$E_{Fsurf} - E_{Csurf} = \Delta E_F + q\left(\psi_{cnt,s} - V_{cb} - \phi_0\right) - E_c \tag{2.32}$$

Using Eq. (2.32) in the analytical expressions for the charge inside the carbon nanotube given by Eqs. (2.16) and (2.17), the gate substrate voltage, $V_{gb}$, in Eq. (2.10) can be rewritten as:

$$V_{gb} = \psi_{cnt,s} - \delta f\left(\psi_{cnt,s}, V_{cb}\right) + V_{fb} \tag{2.33}$$

where

$$f\left(\psi_{cnt,s}, V_{cb}\right) = \begin{cases} Ie^{\frac{\Delta E_F + q\left(\psi_{cnt,s} - V_{cb} - \phi_0\right) - E_c}{kT}}; & for \quad \psi_{cnt,s} \leq V_{cb} + \varphi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{KT}{q} \\ \frac{\sqrt{\left(\Delta E_F + q\psi_{cnt,s} - qV_{cb} - q\phi_0\right)^2 - E_c^2}}{kT}; & \\ & for \quad \psi_{cnt,s} \geq V_{cb} + \phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{KT}{q} \end{cases}$$

and

$$\delta = \frac{qLN_c}{C_{ox1}}$$

By partitioning the Eq. (2.33) in three regions, an explicit solution in terms of the terminal voltages can be obtained: Region 1 (linear region), in which the carbon nanotube potential has a linear and exponential dependence on the gate to substrate voltage, Region 3 (saturation region), in which the carbon nanotube potential does not change significantly with the gate to substrate voltage, and Region 2 (inter-median region), in which no real dependence of the carbon nanotube potential on gate to substrate voltage can be established and an approximate curve fitting can be obtained. The carbon nanotube potential can be found using the following equations:

Saturation and inter-median regions: $V_{ds} \geq V_{gs} - \left( V_{fb} + \phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q} - \frac{Ie^{-1}}{\Delta} \right)$

$$\begin{aligned} \psi_{cnt,s}(0) &= \frac{V_{gs} + V_{sb} - \delta Ie^{-1} - V_{fb} + \delta\Delta\left(V_{sb} + \phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q}\right)}{1 + \delta\Delta} \\ \psi_{cnt,s}(L) &= V_{gs} + V_{sb} - V_{fb} \end{aligned} \tag{2.34}$$

Linear region: $V_{ds} \leq V_{gs} - \left( V_{fb} + \phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q} - \frac{Ie^{-1}}{\Delta} \right)$

$$\begin{aligned} \psi_{cnt,s}(0) &= \frac{V_{gs} + V_{sb} - \delta Ie^{-1} - V_{fb} + \delta\Delta\left(V_{sb} + \phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q}\right)}{1 + \delta\Delta} \\ \psi_{cnt,s}(L) &= \frac{V_{gs} + V_{sb} - \delta Ie^{-1} - V_{fb} + \delta\Delta\left(V_{db} + \phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q}\right)}{1 + \delta\Delta} \end{aligned}, \tag{2.35}$$

where $\Delta = \frac{q}{2kT}\left[\sqrt{\frac{2E_c}{kT} + 1} - Ie^{-1}\right]$ is the slope of linear region and $\delta = qLN_c / C_{ox1}$ . $\Phi_0$ is the carbon nanotube surface potential, $\psi_{cnt,s}$ when $V_{gb} = V_{fb}$ and $\psi_{cnt} = 0$. $\Delta E_F$ is the shift in the Fermi level from the middle of the band gap due to the doping. $N_c$ is the density of states given by $N_c = 8kT / \pi\sqrt{3}V_{pp\pi}a$.

Equations for surface potentials described above can now be used in current transport modeling of non-ballistic and ballistic CNT-FETs for the structures shown in Figs. 2.1 or 2.2 (a) and (b).

## 2.3 Non-Ballistic CNT-FET Modeling

### 2.3.1 Current Transport Modeling

Current equations are given in [91] as follows, which includes drift current and diffusion current.

$$\begin{aligned} I_{ds} &= I_{drift} + I_{diff} \\ &= \beta\left[f_{drift}\left(\Psi_{cnt,s}(L), V_{gs}\right) - f_{drift}\left(\Psi_{cnt,s}(0), V_{gs}\right)\right] + \\ &+ \beta\left[f_{diff}\left(\Psi_{cnt,s}(L), V_{gs}\right) - f_{diff}\left(\Psi_{cnt,s}(0), V_{gs}\right)\right] \end{aligned} \tag{2.36}$$

where

$$f_{drift}\left(\psi_{cnt,s}(x), V_{gs}\right) = \left(V_{gs} + V_{sb} - V_{fb}\right)\psi_{cnt,s}(x) - \frac{1}{2}\psi_{cnt,s}^2(x)$$

$$f_{diff}\left(\psi_{cnt,s}(x), V_{gs}\right) = \frac{kT}{q}\psi_{cnt,s}(x)$$

$$\beta = \gamma \frac{\mu C_{ox1}}{L^2}$$

In Eq. (2.36), various parameters are defined as follows: L: gate length, μ: carrier mobility in graphite, k: Boltzmann constant, T: temperature, $^{o}$K, $V_{fb}$: flat-band voltage, $V_{gs}$: gate-source voltage, $V_{sb}$: source-substrate voltage, $\psi_{cnt,s}$: potential at the interface of the gate oxide and the carbon nanotube with respect to the back gate, which can be expressed as, $\psi_{cnt,s} = \phi_{cs} + \psi_{cnt} + \psi_{ox2} + \psi_{subs}$, γ: a conversion factor for CNT from graphite with a value varying from 0 to 1 and $C_{ox1}$: gate-oxide capacitance per unit area. The threshold voltage is given by,

$$V_{gb} \geq V_{sb} + V_{fb} + \phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{KT}{q} - \frac{(I)e^{-1}}{\Delta} \tag{2.37}$$

As considered in MOSFET, a channel length modulation parameter, λ is also introduced in our CNT-FET model. In the saturation region, Eq. (2.36) is modified as follows,

$$I_{ds} = \beta \left[ f\{\psi_{cnt,s}(L), V_{gs}\} - f\{\psi_{cnt,s}(0), V_{gs}\} \right](1 + \lambda V_{ds}) \tag{2.38}$$

Figure 2.4 shows the I-V characteristics for a CNT-FET with chiral vector (11,9) for different overdrive gate voltages. In Fig. 2.4, experimentally measured data taken from the work of Wind et al. [15] are plotted for the comparison. The model equation follows closely the experimentally measured data. Figure 2.5 shows a plot of $I_{ds}$ versus the gate to source voltage, $V_{gs}$ of a CNT-FET with chiral vector (11,9) for varying V ds values. The curves show that for a given $V_{gs}$ the current $I_{ds}$ increases with increasing $V_{ds}$, in saturation region as in Fig. 2.4.

### 2.3.2 Logic Gates Modeling

CNT-FETs can be made both n- and p-types as in CMOS [14], making possible the implementation of CNT-FETs as fully complementary logic, such as the inverters, NOR and NAND gates as shown in Fig. 2.6. The model equations characterizing the current voltage transport described in Section 2.3.1 are for n-type CNT-FETs, can also be used for p-type CNT-FETs by changing the polarities of the voltages as in a standard p-MOSFET. In generating voltage transfer characteristics of logic gates, we have used Eqs. (2.36) and (2.38) and two complementary CNT-FETs.

Inverter, NAND and NOR constitute basic building blocks in designing of digital integrated circuits. Understanding of their voltage transfer characteristics gives information about high and low logic levels, transition region and noise margins. Using the current transport model we have modeled voltage transfer characteristics of basic gates using complementary CNT-FETs. Figure 2.7 shows the voltage transfer characteristic of an inverter for a chiral vector (11,9). The dotted line in Fig. 2.7 is the experimental curve plotted from the work of Derycke et al. [60] and Martel et al. [61] for comparison. The two solid lines in Fig. 2.7 correspond to λ = 0.1 and 0 $V^{-1}$ with and without channel length modulation, respectively. It should be noted in Fig. 2.7 that $V_{IN}$

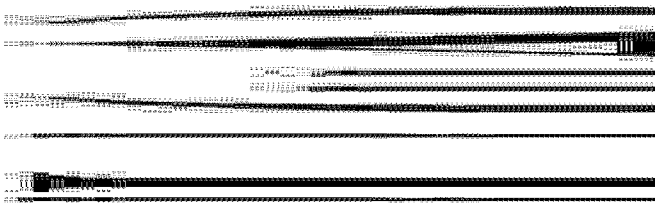


Figure 2.4: I-V characteristics of CNT-FET (11,9) with $V_{fb}$ = -0.79 V and $\phi_0 = 0$. The device dimensions are $T_{ox1}$ = 15 nm, $T_{ox2}$ = 120 nm and L = 250 nm. In modeled curve, $Q_{01} = Q_{02} = 0$ and $\lambda = 0.1\ V^{-1}$.

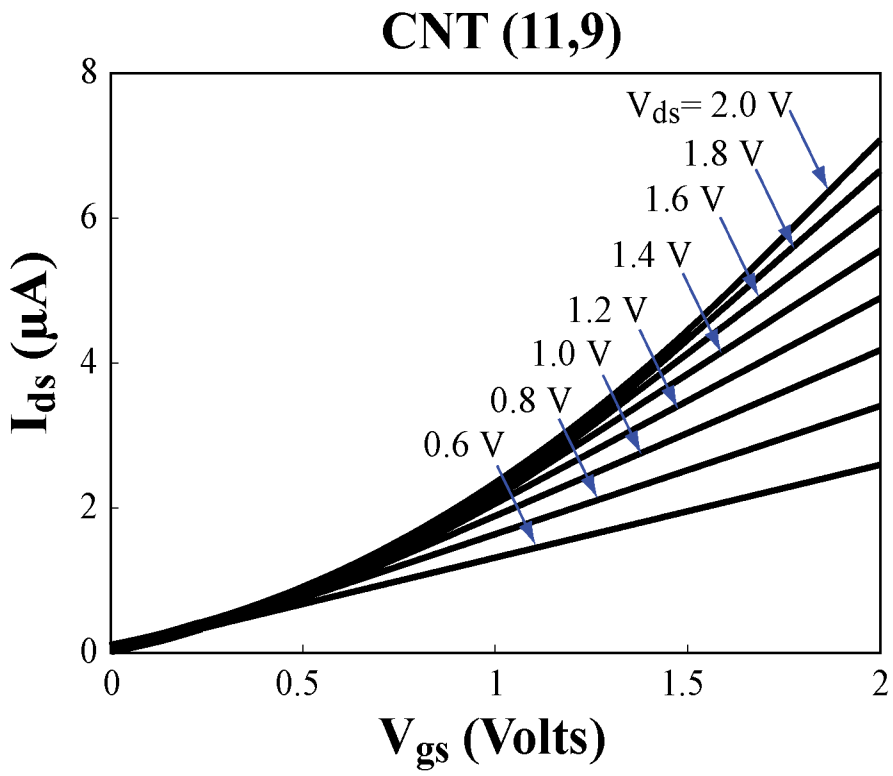



Figure 2.5: Current, $I_{ds}$ versus gate to source voltage, $V_{gs}$ using $V_{fb}$ = -0.79 and $\phi_0$ =0 for CNT-FET (11,9). The device dimensions are: $T_{ox1}$ = 15 nm, $T_{ox2}$ = 120 nm and L = 250 nm. In modeled curve, $Q_{01} = Q_{02} = 0$ and $\lambda = 0.1\ V^{-1}$.

Figure 2.6: CNT-FET logic: (a) Inverter, (b) two input NAND gate and (c) two input NOR gate.

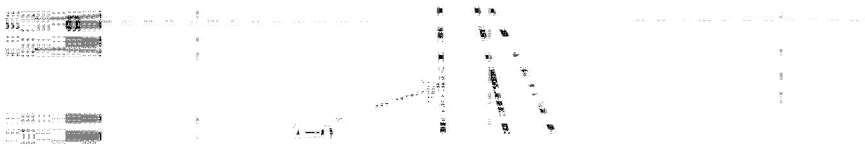


Figure 2.7: Voltage transfer characteristics of an inverter using CNT-FETs (11,9) with $V_{fb}$ = 0 V, $\lambda$ = 0, 0.1 $V^{-1}$ and $\phi_0$ = 0. The dimensions of both the n-type CNT-FET and p-type CNT-FET are: $T_{ox1}$ = 15 nm, $T_{ox2}$ = 120 nm and L = 250 nm.

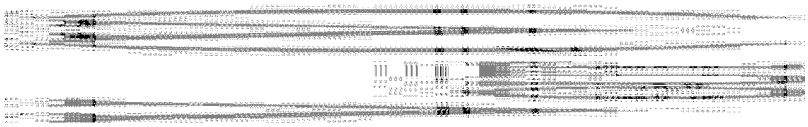
varies from -2 V to 2 V and $V_{OUT}$ varies from -2 V to 1.5 V, which correspond to conditions of the experiment. Therefore, modeled curves have been obtained for conditions of the experiment for comparison. It is seen from the Fig. 2.7 that the experimental voltage transfer characteristics closely follow the modeled voltage transfer characteristic corresponding to channel length modulation, $\lambda = 0.1\ V^{-1}$. Experimental transfer characteristic shows some deviation from the modeled behavior which may be attributed to influence of process variation on device parameters.

Figure 2.8 (a) shows the voltage transfer characteristics of an inverter and two input NAND gate for a chiral vector (11,9). Figure 2.8 (b) shows the voltage transfer characteristics of an inverter and a NOR gate for a chiral vector (11,9). The voltage transfer characteristic of the inverter is included to show its full output voltage. The power supply voltage is 2 V. The input voltage is varied from 0 to 2 V and corresponding output voltage is obtained. In NAND and NOR gates, voltage transfer characteristics have been obtained for the following input conditions: setting one of the inputs to high ($V_{DD}$) or low ($V_{SS}$) and varying the other input or varying both of the inputs simultaneously, as shown in Figs. 2.8 (a) and (b). It is seen that the inverter, NOR and NAND gates give full logic swing similar to inverter and gates designed in CMOS. The inverter switching threshold voltage is 1V. In NAND and NOR gates, the switching threshold voltage is dependent on input voltage conditions. The voltage transfer characteristics in these gates also exhibit sharp transition at switching thresholds and are similar to characteristics observed in corresponding gates implemental in CMOS.

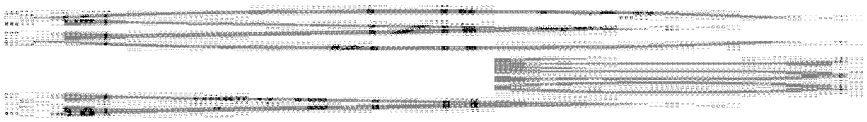
### 2.3.3 Dynamic Modeling

To model the dynamic response of CNT-FETs, we use a Meyer capacitance model [114] shown in Fig. 2.9. Following two assumptions are made: 1) The capacitances in a CNT-FET are reciprocal, that is, $C_{gb} = C_{bg}$, $C_{gd} = C_{dg}$, $C_{gs} = C_{sg}$; 2) In strong inversion, the rate of change of gate charge $Q_g$ and $Q_{cnt}$ are equal and the rate of change of $Q_{subs}$ is neglected.

We can rewrite Eq. (2.2) as,



(a)



(b)

Figure 2.8: Voltage transfer characteristics of (a) an inverter and a NAND gate (b) an inverter and a NOR gate using CNT-FETs (11,9) with $V_{fb} = 0$ V and $\phi_0 = 0$. The dimensions of both the n-type CNT-FET and p-type CNT-FET are: $T_{ox1} = 15$ nm, $T_{ox2} = 120$ nm and L = 250 nm.

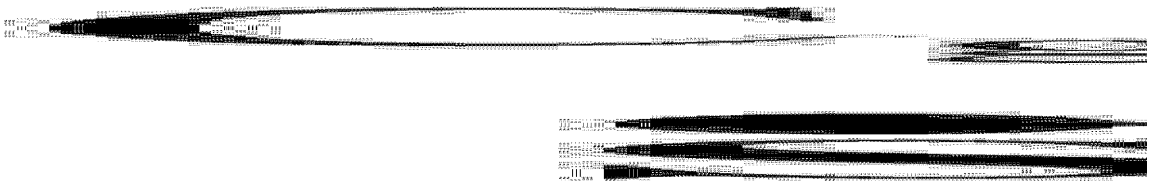


Figure 2.9: Meyer capacitance model for CNT-FETs [114].

$$Q'_g = -Q'_{cnt} - Q'_{subs} - Q'_{01} - Q'_{02} \tag{2.39}$$

The prime in Eq. (2.39) denotes the charge per unit area. Using the potential balance and charge neutrality conditions, we obtain $Q'_{cnt}$,

$$Q'_{cnt} = -C'_{ox1}\left(V_{gb} - \psi_{cnt,s}(x) - V_{fb}\right) \tag{2.40}$$

In our recent work [91], we regarded $Q_{cnt} = ½|C_h|LQ'_{cnt}$, where $C_h$ is the chiral vector and its magnitude equals to the circumference of the CNT. We have used the charge per unit area, but only to show that we have considered a surface area, $|C_h|L/2$ for the carbon nanotube. Therefore, we can regard the CNT-FET channel width is to be half of the CNT circumference. The drift current can be described as follows,

$$I_{drift} = \frac{|C_h|}{2}\gamma\mu Q'_{cnt}\frac{\mathrm{d}\psi_{cnt,s}}{\mathrm{d}x} \Rightarrow \mathrm{d}x = \frac{|C_h|\gamma\mu Q'_{cnt}}{2I_{drift}}\mathrm{d}\psi_{cnt,s}, \tag{2.41}$$

Thus, the total charge in the gate is,

$$\begin{aligned} Q_g &= -W\int_0^l Q'_{cnt}\mathrm{d}x - Q_{subs} - Q_{01} - Q_{02} \\ &= -\frac{\gamma\mu W|C_h|C'^2_{ox1}}{I_{drift}}\int_{V_0}^{V_1}\left(V_{gb} - \psi_{cnt,s} - V_{fb}\right)^2\mathrm{d}\psi_{cnt,s} - Q_{subs} - Q_{01} - Q_{02}, \\ &= -\frac{\gamma\mu|C_h|^2 C'^2_{ox1}}{2I_{drift}}\int_{V_0}^{V_1}\left(V_{gb} - \psi_{cnt,s} - V_{fb}\right)^2\mathrm{d}\psi_{cnt,s} - Q_{subs} - Q_{01} - Q_{02} \end{aligned} \tag{2.42}$$

where W is the width of the gate for carbon nanotube and it is half of the circumference. The charge per unit area in the substrate is given by,

$$Q'_{subs} = -\sqrt{2q\varepsilon N_A}\sqrt{\psi_{subs}} \tag{2.43}$$

We obtain the capacitance $C_{gs}$, $C_{gd}$ and $C_{gb}$ from the following definitions,

$$C_{gb} \equiv \left.\frac{\partial Q_g}{\partial V_{gb}}\right|_{V_{gs},V_{gd}} \tag{2.44a}$$

$$C_{gs} \equiv \left.\frac{\partial Q_g}{\partial V_{gs}}\right|_{V_{gb},V_{gd}} \tag{2.44b}$$

$$C_{gd} \equiv \left.\frac{\partial Q_g}{\partial V_{gd}}\right|_{V_{gs},V_{gb}} \tag{2.44c}$$

In Eq. (2.1), $\psi_{subs}$ can be neglected [91], therefore, $Q_{subs}$ in Eq. (2.42) can be neglected. In addition, we assume that $Q_{01}$ and $Q_{02}$ are fixed. Substitute Eqs. (2.34) and (2.35) in Eq. (2.36) to compute $I_{drift}$ part of $I_{ds}$ and then substitute $I_{drift}$ and Eq. (2.43) for $Q'_{subs}$ in Eq. (2.42). Thus, we obtain $Q_g$ for computing $C_{gs}$, $C_{gd}$ and $C_{gb}$ from Eq. (2.44).

In linear region:

$$C_{gb} = 0 \tag{2.45a}$$

$$C_{gs} = -\frac{\gamma\mu|C_h|^2 C'^2_{ox1}}{4\beta} \cdot \frac{\left[Ie^{-1} - \Delta(\phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - V_{gs})\right]\left[Ie^{-1} - \Delta(\phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - \frac{2}{3}V_{gd} - \frac{1}{3}V_{gs})\right]}{\left[Ie^{-1} - \Delta(\phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - \frac{1}{2}V_{gd} - \frac{1}{2}V_{gs})\right]^2} \tag{2.45b}$$

$$C_{gd} = -\frac{\gamma\mu|C_h|^2 C'^2_{ox1}}{4\beta} \cdot \frac{\left[\delta Ie^{-1} - \delta\Delta(\phi_0 - \frac{\Delta E_c}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - V_{gd})\right]\left[\delta Ie^{-1} - \delta\Delta(\phi_0 - \frac{\Delta E_c}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - \frac{1}{3}V_{gd} - \frac{2}{3}V_{gs})\right]}{\left[\delta Ie^{-1} - \delta\Delta(\phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - \frac{1}{2}V_{gd} - \frac{1}{2}V_{gs})\right]^2} \tag{2.45c}$$

In saturation region:

$$C_{gb} = 0 \tag{2.46a}$$

$$C_{gs} = \frac{1}{3}\frac{\gamma\mu\left|C_h\right|^2 C_{ox1}'^2}{\beta} \times \left\{ 3 - \frac{2\left[Ie^{-1} - \Delta(\phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - V_{gs})\right]^3 - \left[Ie^{-1} - \Delta(\phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - V_{th})\right]^3}{\left[Ie^{-1} - \Delta(\phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - V_{gs})\right]^3} \right\} \quad (2.46b)$$

$$C_{gd} = 0 \quad (2.46c)$$

In linear and saturation regions, $C_{gb}$ equals to zero because $Q_{subs}$ is neglected. Physically, $C_{gb}$ is negligible since $Q_{cnt}$ shields the gate from the bulk and prevent any response of the gate charge to a change in the substrate bias. If we consider the small change of $Q_{subs}$, $C_{gb}$ will be a small value compared with $C_{gs}$ and $C_{gd}$ as shown in the work of Deng and Wong [33].

In the saturation region, the channel is pinched-off at the drain end of the CNT. This electrically isolates the CNT from the drain so that the charge on the gate is not influenced by a change in the drain voltage and $C_{gd}$ vanishes.

$C_{sb}$ and $C_{db}$ are equal to one half the insulator capacitance, $C_{ox2}/2$ in series with the depletion-layer capacitance, $C_{subs}/2$. $C_{ox2}$ is calculated using Eq. (2.22) and $C_{sub}$ is calculated as follows [115].

$$C_{subs} = \frac{\varepsilon_s}{W_s} = \sqrt{\frac{\varepsilon_s q N_A}{2\psi_{subs}}}, \quad (2.47)$$

where $\varepsilon_s$ is the permittivity of the semiconductor, $W_s$ is the depletion region width and $N_A$ is the doping concentration.

From the definition of $\psi_{cnt,s}$, we can get $\psi_{subs}$ as follows,

$$\psi_{subs} = \psi_{cnt,s} - \psi_{cnt} - \psi_{ox2} - \phi_{cs} \quad (2.48)$$

and,

$$\frac{\psi_{subs}}{\psi_{ox2}} = \frac{C_{ox2}}{C_{subs}} \tag{2.49}$$

Combing Eqs. (2.47) - (2.49), the expression for $C_{subs}$ is obtained,

$$C_{subs} = \frac{N_A q\varepsilon_s + \sqrt{N_A q\varepsilon_s}\sqrt{8C_{ox2}^2\left(\psi_{cnt,s} - \psi_{cnt} - \phi_{cs}\right) + N_A q\varepsilon_s}}{4C_{ox2}\left(\psi_{cnt,s} - \psi_{cnt} - \phi_{cs}\right)} \tag{2.50}$$

Figure 2.10 shows the capacitances of CNT-FET (11,9) with $V_{fb}$ = -0.79 V and $\Phi_0$ = 0. The device dimensions are $T_{ox1}$ = 15 nm, $T_{ox2}$ = 120 nm and L = 250 nm. The capacitances behaviors are similar to that of MOSFET. $C_{gs}$ and $C_{gd}$ are almost the same at $V_{ds}$ = 0V since the transistor is symmetric in terms of drain and source. $C_{gd}$ becomes negligible in saturation region because the drain voltage has no significant effect on the channel charge at drain end. The results are in same order with calculated results by Deng and Wong [33].

## 2.4 Ballistic CNT-FET Modeling

Ballistic CNT-FETs with CNTs shorter than the mean free path (mfp) of acoustic phonons (~ 0.5 μm) are currently the most attractive semiconducting nano device [49, 87, 116] for high performances VLSI circuits. Models for Ballistic CNT-FETs are required in order to design circuits intuitively by examining key physical parameters that determine performance. Some of the models are either numerical, requiring a self-consistent quantum mechanical formalism that is usually time consuming [49], or semi-analytical, requiring an iterative numerical method to solve for the surface potential [33, 87, 117, 118]. We have developed a fully analytical ballistic transport model of CNT-FETs enabled by an analytical surface potential.

Besides inducing charge in the CNT-FET channel, the gate voltage also modulates the top of the energy band between the source and the drain. Current will flow between the source and the drain when the barrier at source and drain is lowered. For ballistic transport, all scattering mechanisms can be neglected. An important aspect of ballistic transport is at the top of the source and drain barriers, electrons coming from the source fill up the +k states and electrons coming from the drain fill up the –k states.

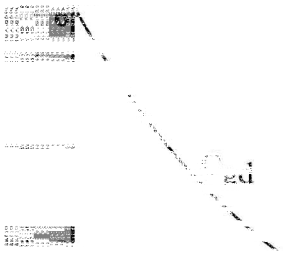


Figure 2.10: The capacitances of CNT-FET (11,9) with $V_{fb}$ = -0.79 V and $\phi_0 = 0$. The device dimensions are $T_{ox1}$ = 15 nm, $T_{ox2}$ = 120 nm and L = 250 nm. In modeled curve, $Q_{01} = Q_{02} = 0$.

As described in Section 2.2, Eqs. (2.34) and (2.35) for surface potential can be used for ballistic CNT-FETs shown in Fig. 2.1 (b).

The total drain current including each sub-band is obtained as follows [16, 88, 119, 120]:

$$I_D = \frac{4qkT}{h}\sum_{p=1}^{\infty}\left[\ln(1+\exp\xi_S) - \ln(1+\exp\xi_D)\right], \tag{2.51}$$

where q is electron charge, k is the Boltzmann constant, T is the absolute temperature, h is the Plank constant, p is the number of sub-band and ξS = (qψcnt,s-Ecp)/kT and ξD = (qψcnt,s-Ecp-qVDS)/kT. Here, Ecp is the sub-band conduction minima. VDS is the drain to source voltage.

Figure 2.11 shows the modeled I-V characteristics for a self-aligned p-type CNFET with Ohmic metallic contacts (dielectric constant, κ = 15, tox = 8 nm and d = 1.7nm) and comparison with the experimental work of Javey et al. [49]. Figure 2.11 also shows the results from the analytical work of Akinwande et al. [116] for comparison. Although both of the analytical models show close agreement with the experimental data, the computed I-V characteristics using the model developed by Akinwande et al. [116] are closer at lower gate voltages. This parameter is decided by the experiments

The sub-band spacing in a small diameter tube (~l.7nm) is larger [121]. Equation (2.51) shows that the current depends exponentially on the barrier height; therefore, the current of the higher sub-band is small compared to that of the lower sub-band. As a result, the first sub-band conduction dominates for the ballistic CNT-FET. Figure 2.12 shows the I-V curves at $V_{gs}$ = 0.4V considering one, two and three or more sub-bands. The sub-band conduction minima are 0.2098, 0.4047, 0.8587 and 0.9645 eV for the first, second, third and fourth sub-bands. It shows that three sub-bands are sufficient to describe the current of CNT-FET with sufficient accuracy and in agreement with the theoretical prediction [122] and experimental measurements [121].

## 2.5 Verilog-AMS Simulations

New CNT-FETs do not behave the same way as the traditional CMOS-FETs.

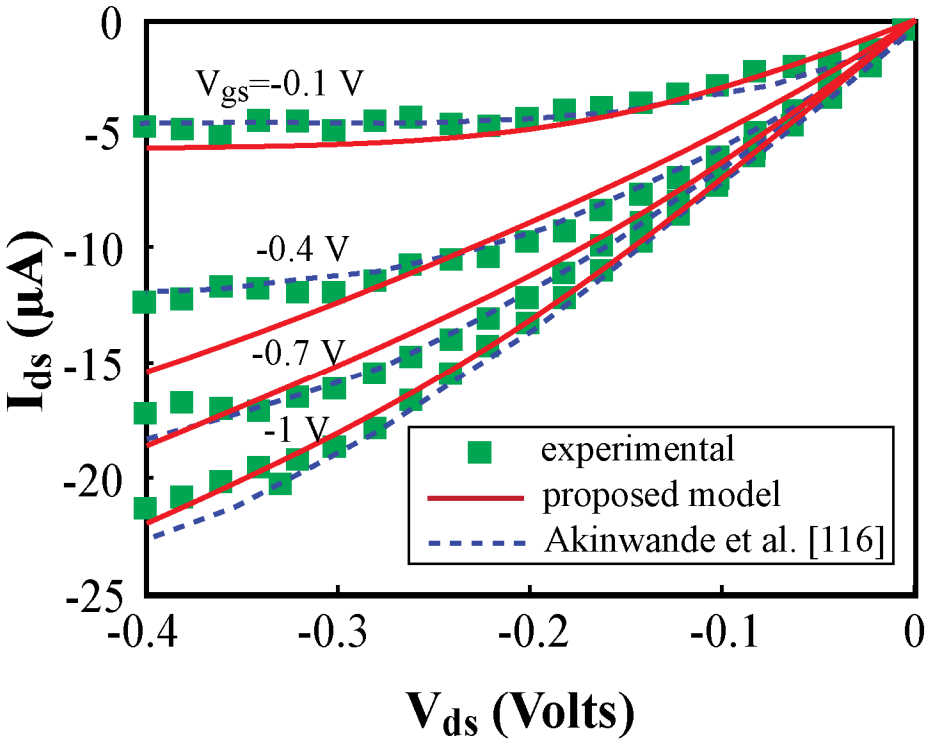



Figure 2.11: I-V characteristics for a self-aligned p-type CNT-FET with Ohmic metallic contacts shown by solid lines. The CNT-FET parameters are: $\kappa = 15$, $t_{ox} = 8$ nm and $d = 1.7$nm. Experimental data shown by rectangles is taken from the work of Javey et al. [49]. Dotted line plots are from the work of Akinwande et al. [116]

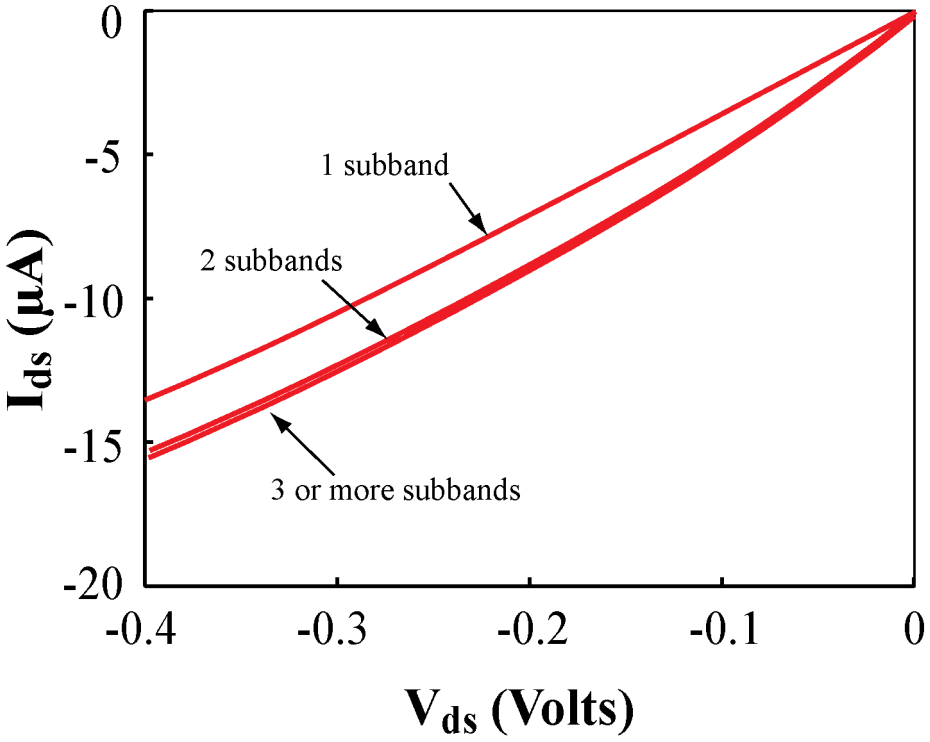



Figure 2.12: I-V characteristics of ballistic CNT-FET (19,5) for different numbers of sub-bands.

New equations are derived to describe the current, capacitance, and so forth. Therefore, old SPICE simulators are not keeping up with the development but Verilog Analog Mixed-Signal (Verilog-AMS) gives a solution. Figure 2.13 shows that much less steps are needed to get the simulator available using Verilog-AMS compared with the SPICE coding. This is because model equations for new devices can be put into the Verilog-AMS coding and simulator will call the code. However, the model equations need to be fit into the SPICE simulator, which means a new simulator need to be built and this is a time consuming job. In our work, we have used Verilog-AMS to describe the CNT-FET static and dynamic models.

Figure 2.14 (a) shows the signal response of an inverter pair, which is composed by two series inverters. The input signal is 10 GHz square wave with 1 ps rise and fall times. The simulation results show that the delay of the inverter pair is about 3.2 ps. Figure 2.14 (b) shows a plot of the inverter pair average delay versus the supply voltages. At the 0.6 V supply voltage, the average delay is 6.95 ps, which suggests that this inverter pair is able to work for up to 100 GHz input signal. Figure 2.15 (a) shows the schematic of the five-stage of ring oscillator which was fabricated by Chen et al. [44]. Figure 2.15 (b) shows the simulation result of the ring oscillator output waveform at 0.92 V supply voltage. Figure 2.15 (c) shows the oscillation frequency with different supply voltage. The observed derivation of experimental results from the modeled characteristic can be attributed to non-optimized fabrication process, such as the CNT is not perfectly straight. Model and experiments show that the oscillating frequency of this ring oscillator is only about 70-80 MHz at 1.04 V supply voltage. This is due to the CNT-FETs in the ring oscillator are 600 nm long and there are parasitic capacitances associated with the metal wire in the ring oscillator. Shorter length of CNT-FETs will increase the oscillating frequency, as shown in Fig. 2.16. This is due to shorter channel length CNT-FETs will give high current and less parasitic capacitance.

## 2.6 Summary

Model equations for surface potentials for non-ballistic and ballistic CNT-FETs are presented. The current transport equations for non-ballistic CNT-FETs are

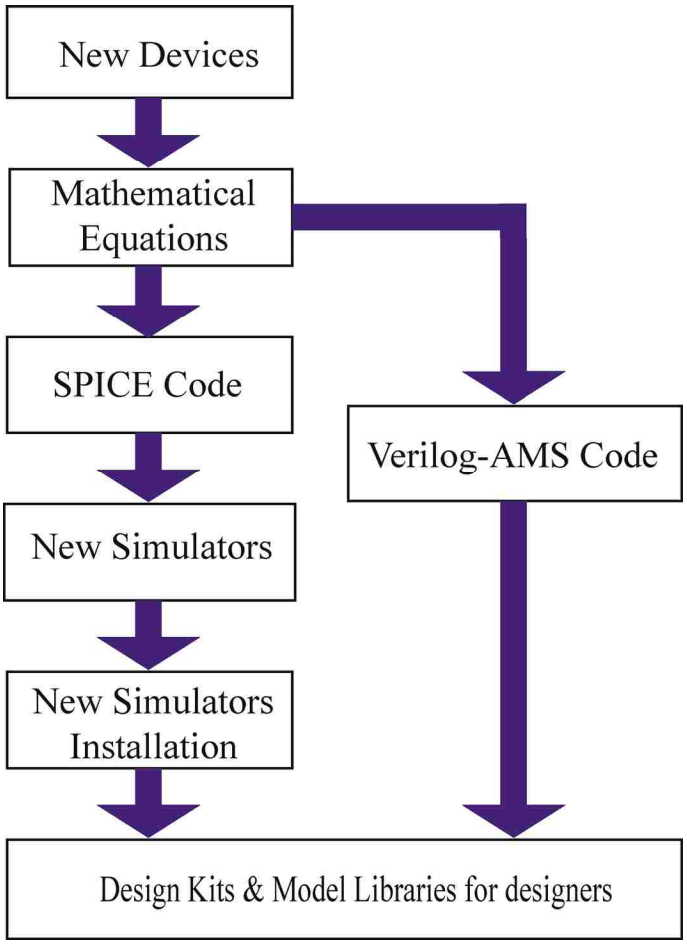



Figure 2.13: Steps to simulate a new device using Verilog-AMS code.

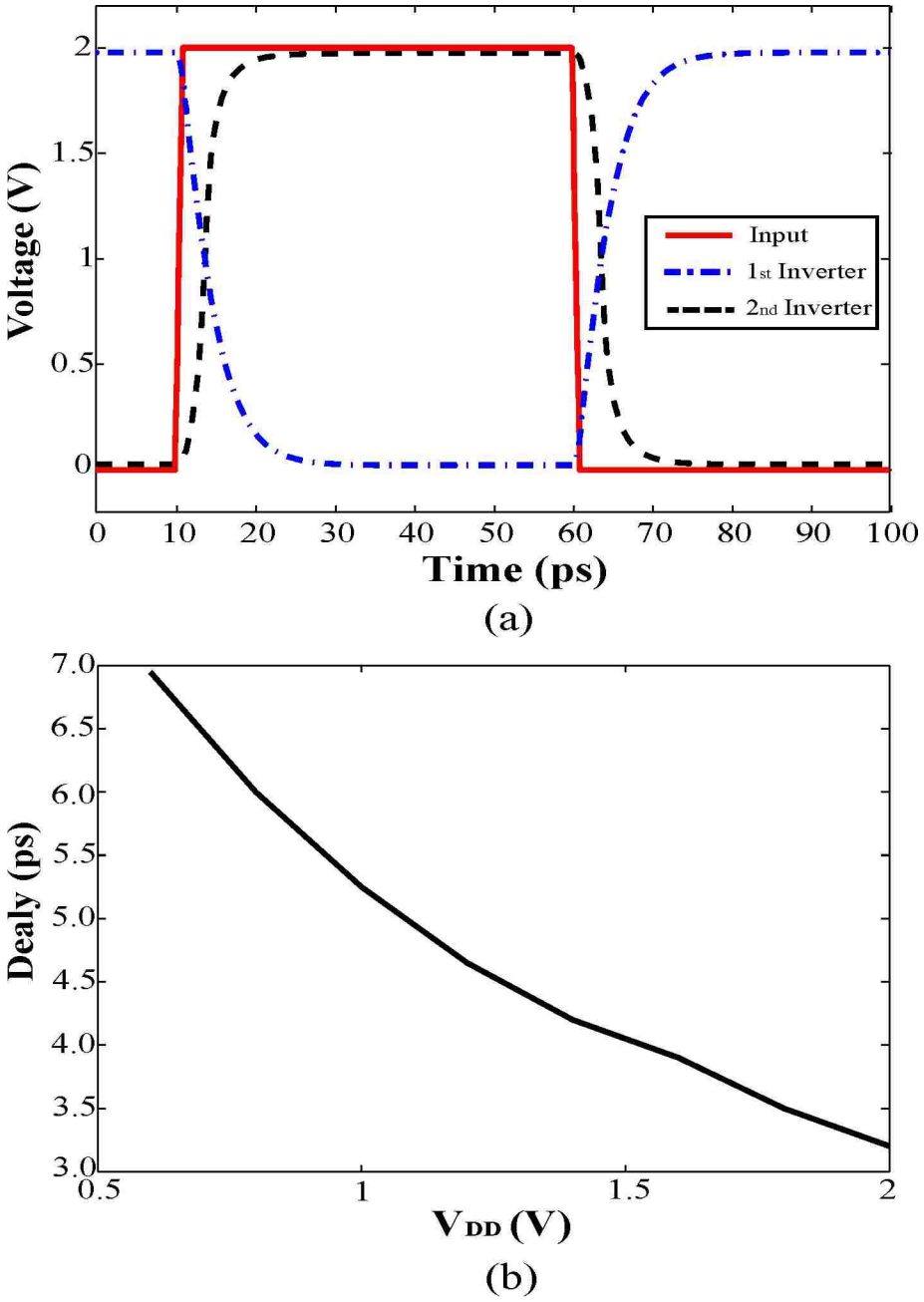



Figure 2.14: (a) Transient behavior of an inverter pair using CNT-FETs (11,9) with $V_{fb}$ = 0 V and $\phi_0 = 0$. The dimensions of both the n-type CNT-FET and p-type CNT-FET are: $T_{ox1}$ = 15 nm, $T_{ox2}$ = 120 nm and L = 250 nm and (b) average delay of the inverter pair versus supply voltage.

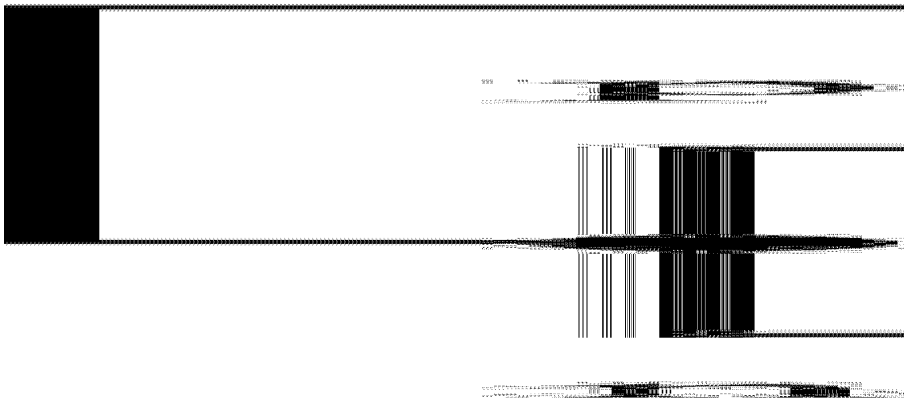


Figure 2.15: (a) Schematic of a 5-stage ring oscillator, (b) output waveform, (c) the oscillating frequency versus supply voltage, $V_{DD}$. The dimensions of both the n-type and p-type CNT-FETs are: d = 2 nm and L = 600 nm.

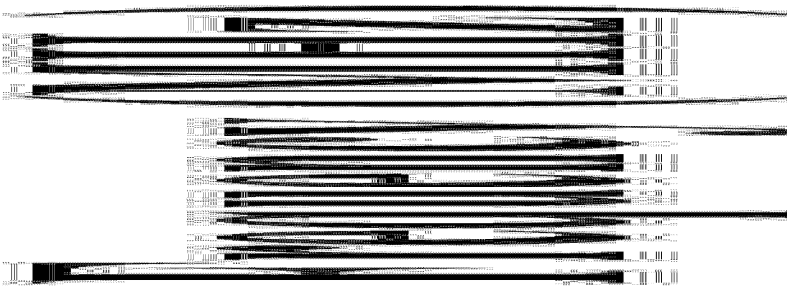


Figure 2.16: Oscillating frequency of the 5-stage ring oscillator versus length of the CNT-FETs.

summarized, which were derived in one of our earlier work [91]. Based on these equations, dynamic model equations for linear and saturation regions of operation of CNT-FETs are derived. The current transport equations for ballistic CNT-FETs are also described. The modeled I-V characterizations are in agreement with the experimental results and the model proposed by Akinwande et al. [116]. By using the static and dynamic models for non-ballistic CNT-FETs, we have studied performances of some basic CNT-FETs circuits, such as the inverter and ring oscillator. The simulation of ring oscillator frequencies fit the experimental data fairly well.

# CHAPTER 3*

# MODELING SINGLE-WALLED CARBON NANOTUBE INTERCONNECTION FOR VLSI

## 3.1 Introduction to Carbon Nanotube Interconnection

The one-dimensional carbon nanotube has excellent electrical, mechanical and thermal properties [22, 25] which has made the CNT one of the promising materials for applications in nanoelectronics [6, 123-125] and micro/nano-systems [126]. In nanoelectronics, CNT-FET is very promising in design of emerging logic devices for nanoscale integration and there is a noticeable amount of published and ongoing research on understanding current transport in CNT-FETs and developing models for use in circuit simulators [7, 14, 53, 85, 88, 91, 101, 105, 127, 128]. In micro/nano-systems, both the CNT and CNT-FET are very promising as sensors for detecting chemicals, gases at molecular levels [126, 129-133]. Carbon nanotube carries a current density of ~ $10^{10}$ A/cm$^2$ which is higher by a two to three orders of magnitude in Cu. Its mean free path is in micrometer range compared to ~40 nm mean free path in Cu. The large mean fee path in CNT allows a ballistic transport over a wider range of micrometers resulting in reduced resistivity, and strong atomic bonds [134] provide tolerance to electromigration [135, 136]. Higher thermal conductivity makes the CNT suitable for use in tall vias of 3D ICs [137-139]. Electrical performance of single and bundled carbon nanotubes have been studied in the work of Plombon et al. [140], Yao et al. [141] and Nougaret et al. [142]. Recently Sarto and Tamburrano [143] have presented analytical derivation of multi-walled carbon nanotubes from the multiconductor transmission line model. Properties of carbon nanomaterials relevant to VLSI interconnects which include single-walled carbon nanotube (SWCNT), multi-walled carbon nanotube (MWCNT), graphene nanoribbons (GNR) and comparison with the properties of Cu interconnect are summarized in the work of Li et al. [137]. Graphene nanoribbons is a recent addition to the interconnect

* Part of the work is reported in the following publications:

1. Y. Xu and A. Srivastava, "A model for carbon nanotube interconnects," *Int. J. Circ. Theor. Appl.,* vol. 38, no. 6, pp. 559-575, August, 2010. Also published online in Wiley InterScience.
2. Y. Xu, A. Srivastava and A. K. Sharma, "A model of multi-walled carbon nanotube interconnects," *Proc. of the 52nd IEEE Midwest Symposium on Circuits and Systems, (MWSCAS 2009)*, Cancun, Mexico, August 2-5, 2009, pp. 987-990.

technology since the discovery of 2D graphene in 2004 [144, 145] and the methods of fabricating GNR are still being developed.

Nanometer CMOS technology especially in 22 nm and below is plagued due to performance degradation of conventional Cu/low-k dielectric as an interconnect material for gigascale integration. In one of the recent published research on interconnect technologies, Koo et al. [135] have mentioned the effect of scaling on surface and grain boundary scattering and electromigration in Cu interconnect [146] and in great detail degradation in its parameters such as the latency and power dissipation. Thus the need for other materials possibly substituting Cu/low-k dielectric interconnections has brought forward other novel interconnect technologies for next generation VLSI interconnects. Optical interconnects have already been suggested for on-chip integration [147-149] but still face serious integration problems. Among newer and novel VLSI interconnection technologies, carbon nanotubes (CNTs) and graphene nanoribbons (GNR) have emerged promising candidates for next generation VLSI interconnects [123-125, 136, 150-153]. An excellent review of these technologies has been presented in one of the recent publications of Li et al. [137]. Though optical interconnect is still being investigated due to its inherent advantages over the Cu interconnect, other new technologies such as the capacitively driven low-swing interconnect (CDLSI) have been also evolved [135]. In search for novel technologies, no such material has aroused so much interest other than carbon nanomaterials since the discovery of carbon nanotube in 1991 by Iijima [19].

A model describing the electromagnetic field propagation along a CNT is indispensable in order to study the interconnection performance of CNT while comparing with traditional metal interconnects. Three theories are used to build different models. Lüttinger liquid theory [92] describes interacting electrons (or other fermions) in one-dimensional conductor and is necessary since the commonly used Fermi liquid model breaks down in one-dimension. Burke [93, 94] regards that electrons are strongly correlated when they transport along the CNT and proposed a transmission line model based on the Lüttinger liquid theory. Another transmission line model was built based on Boltzmann Transport Equation (BTE) [95]. Two-dimensional electron gas, where the charged particles are confined to a plane and neutralized by an inert uniform rigid

positive plane background was studied by Fetter [96, 97]. Based on the work of Fetter [96, 97], Maffucci et al., [98] investigated electron transport along the CNT and proposed a third model, fluid model. In these models [96-98], electron-electron correlation, which is significant in CNTs [154-156], has not been considered. The first model is based on quantum dynamics concepts; the second model requires solving the Boltzmann Transport Equation; the third model has been developed within the framework of the classical electrodynamics and is simple on concepts and mathematical modeling.

Interacting electrons in two and three-dimensions are well described in terms of an approximate model of weakly-interacting quasi-particles, namely Fermi liquid theory. This model has been highly successful in explaining the properties of two and three-dimensional conductors. However, this approximate picture does not hold in one-dimension. Instead, the ground state of an interacting one-dimensional electron gas (1DEG) is a strongly correlated state known as a Lüttinger liquid. Unlike in a Fermi liquid, in a Lüttinger liquid, the low energy excitations are Bosonic sound-like density waves (plasmas). In two-dimension electron gas model [96-98], electron-electron correlation has not been considered in studying electron transport in CNTs. Although Lüttinger liquid model using quantum mechanical concept considers this correlation, the result and expression are too complicated to be solved. As quasi one-dimensional system, quantum effects [157] must be considered to characterize CNT interconnects. Therefore, we have made modification to the two-dimension electron gas model to include electron-electron interactions and built one-dimensional liquid model [158], which is relatively easy to solve and apply in transmission line SWCNT interconnect modeling. The model can be easily used to study S-parameters and group delays of SWCNT interconnect for RF/microwave applications. In the following sub-sections, we will first describe the two-dimensional fluid model and our one-dimensional fluid model of single-walled carbon nanotubes.

## 3.2 Two-Dimensional Fluid Model

A single-walled carbon nanotube (SWCNT) is one atom thick sheet of graphite (called graphene) rolled up into a seamless cylinder with diameter of the order of a nanometer. This results in a nanostructure where the length-to-diameter ratio exceeds

10,000. Since carbon nanotubes are constructed of hexagonal networks, the carbon atoms contain $sp^2$ hybridization. There are four valence electrons for each carbon atom. The first three electrons belong to the σ orbital and are at energies 2.5 eV below the Fermi level; therefore, they do not contribute to the conduction. The fourth valence electron, however, is located in the π orbital, which is slightly below the Fermi level; therefore, this electron is very likely to control conduction and transport properties. This electron corresponds to the valence band of the energy band diagram. The anti-bonding π orbital is slightly above the Fermi level, which corresponds to the conduction band in an energy band diagram. Depending upon the direction of the graphene sheet is wrapped; the SWCNT can be metallic or semiconducting.

If we regard the graphene sheet which is rolled to form the SWCNT is infinitesimally thin, then the conduction electrons are distributed on the lateral surface, s′ of the SWCNT cylinder shell and the electrons are embedded in a rigid uniform positive charge background with a uniform surface number density. Thus, the motion of the electrons is confined to the surface. Furthermore, electrical charge neutrality requires that in equilibrium the conduction electron charge density precisely cancels with that of the background positive ions. According to this analysis, two-dimensional fluid model could be utilized to study the electron transport along the SWCNT. This model is shown in Fig. 3.1. The cylinder shell radius is r and length is *l*. The cylinder axis is oriented along the z-axis of the reference system. Two assumptions have been made to utilize this model. One is the electrons can only move along the z-axis; other is that all other fluid variables, such as the tangential component of the electric field to the nanotube surface, s', are almost uniform in the cross section of the SWCNT. These two assumptions are valid if both the nanotube length and the smallest wavelength of the electromagnetic field are much greater than the nanotube radius [159, 160].

The basic equation in fluid model is Euler's equation with Lorentz force term, which is the Newton's second law applied in fluid dynamics [96] and is given by,

$$mN\left(\frac{\partial}{\partial t}+\vec{V}\cdot\nabla\right)\vec{V}=-\nabla\vec{P}-eN\vec{\mathcal{E}}-mN\nu\vec{V}\,, \tag{3.1}$$

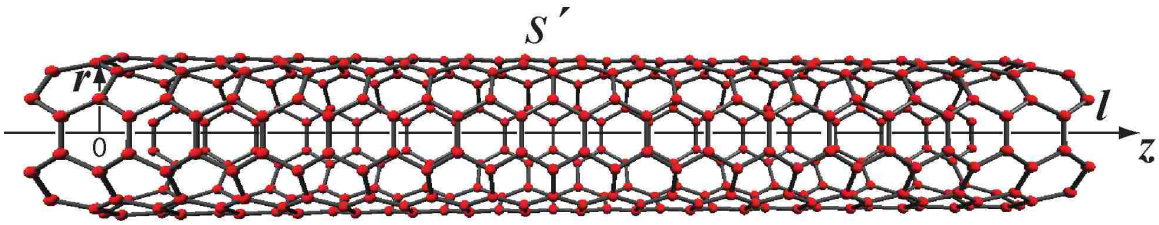



Figure 3.1: Geometry of a single wall carbon nanotube (SWCNT).

where $N(\vec{R},t)$ is the electron three-dimension carrier density, $\vec{V}(\vec{R},t)$ is the electron mean velocity, $\vec{R}$ is the position vector, $\vec{P}$ is the pressure, m is the electron mass, e is the electronic charge and $\vec{\varepsilon}$ is electric field. The last term on the right hand side represents the effect of scattering of electrons with the positive charge background and ν is the electron relaxation frequency. The relaxation frequency, ν is related to the mean-free path, λ as follows,

$$\nu = \frac{v_F}{\lambda}, \tag{3.2}$$

where $v_F$ is the Fermi velocity. The value of λ is decided by the electron scattering mechanism. Experimental and theoretical studies have shown that there are two major scattering in a CNT [141]. One is the elastic scattering with acoustic phonons, which is only dependent on the material and is characterized by a constant mean-free path $\lambda_e$. Other is scattering with optical phonons, which is significant at high electric field intensity. It is characterized by the optical phonons mean-free path, $\lambda_o$ and is given by,

$$\lambda_o = \frac{\hbar v_o}{eE} \tag{3.3}$$

In Eq. (3.3), $v_o$ is the frequency of phonons. Thus, the total mean free path, λ is,

$$\lambda^{-1} = \lambda_e^{-1} + \lambda_o^{-1} \tag{3.4}$$

In fluid model, Eq. (3.1) is simplified to the following form,

$$mn\left(\frac{\partial}{\partial t} + v_z \frac{\partial}{\partial z}\right)v_z = -\frac{\partial p}{\partial z} - en\varepsilon_z\big|_{s'} - mn\nu_z \tag{3.5}$$

where n is the electron density in this one-dimensional system, $v_z$ is the electron mean velocity in z direction, p is the pressure in one-dimensional system. $\varepsilon_z$ is electric field in z direction along the SWCNT surface, s′. In Eq. (3.5), the variables have been changed to the lower case which means that they are functions of the frequency and distributed on the SWCNT surface, s'.

## 3.3 One-Dimensional Fluid Model

Equations (3.1) and (3.5) describe the two-dimensional fluid and need to be modified to be used for carbon nanotubes, which are quasi one-dimensional systems. In a two-dimensional electron fluid, total energy is equal to the kinetic energy. In graphene sheet, the external electrical field drifts electrons in z-direction while the electrons can also distribute in perpendicular (y) direction to form a two-dimensional fluid. This means that the whole energy provided by the external electrical field equals the two-dimensional electron fluid kinetic energy. However, when the graphene sheet is rolled to form a carbon nanotube, which is quasi one-dimensional system, the y-direction shrinks into one point and the distributed electrons in y-direction in a two-dimensional system will be in the same point in one-dimensional system. As a result, the repulsive force among the electrons will be significant. One-dimensional electron fluid energy can thus be considered to consist of two parts, the potential energy and the kinetic energy. The external electric field provides both the potential and kinetic energy to the one-dimensional fluid. Now we define a parameter $\alpha$ as follows,

$$\alpha \equiv \frac{\mathcal{E}_{zP}}{\mathcal{E}_z} = \frac{E_P}{E} = \frac{E_P}{E_K + E_P}, \tag{3.6}$$

where $\mathcal{E}_{zP}$ is the part of the electrical field which provides potential energy to electrons in z-direction. E is the total energy of electrons. $E_P$ and $E_K$ are the potential and kinetic energies of electrons, respectively.

There are two channels in a SWCNT and two different spin electrons in each channel. We can consider that there are four electrons at the same point in one-dimensional SWCNT. We can then calculate the potential energy by moving these four electrons from $\infty$ to the same point of the SWCNT within ~ 1 nm diameter. The potential energy can be defined as follows [161]:

$$E_P = \sum_{n=2}^{4}(n-1) \times \frac{e^2}{2\pi\varepsilon_0}\frac{1}{d} \approx 18eV, \tag{3.7}$$

where d is the diameter of the SWCNT.

We assume that the velocity of these four electrons equals to the Fermi velocity. As a result, the kinetic energy is given by,

$$E_K = 4 \times \frac{1}{2} m v_F^2 \approx 7\text{eV}, \tag{3.8}$$

where $v_F = 3\gamma_0 b/2\hbar = 8\times10^5$ m/s is the Fermi velocity. $\gamma_0$ is the characteristic energy of the graphene lattice and is equal to 2.7 eV and $\hbar$ is Planck constant. The inter-atomic distance, b in a SWCNT is 0.142 nm [98]. Substituting Eqs. (3.7) and (3.8) into Eq. (3.6), we obtain $\alpha \approx 0.7$.

It should be noted that the Lorentz force term, which belongs to body force terms in fluid dynamics, is a source momentum [162]. The external electric field provides both the potential and kinetic energy to the fluid. As a result, one-dimensional fluid model can be expressed as follows [158],

$$mn\left(\frac{\partial}{\partial t} + v_z \frac{\partial}{\partial z}\right) v_z = -\frac{\partial p}{\partial z} - en\left\{(1-\alpha)\boldsymbol{\mathcal{E}}_z\big|_{s'}\right\} - mn\nu v_z, \tag{3.9}$$

The fluid model described by Eq. (3.9) assumes flow of one-dimensional electron fluid under the low external electric fields, $\boldsymbol{\mathcal{E}}_z$. Yao, et al. [141] and Park et al. [67] have studied electronic transport in SWCNTs using low and high resistance contacts under small and large bias-voltages and attempted to explain the conductance behavior from electron-phonon scattering. Yao et al. [141] have also observed linear I-V characteristics from measurement on samples using low resistance contacts with slight deviation near 5V from the linear behavior in some samples. Since current VLSI circuits use low voltage nanometer CMOS technologies where bias voltage is below 1.5 V, deviation in I-V relationship of CNT interconnect toward saturation at large bias-voltages should not be the cause of concern and so the applicability of Eq. (3.9) for CNT interconnects using low resistance contacts.

The difference between our one-dimensional fluid model described in Eq. (3.9) with two-dimensional fluid model [96-98] is the Lorentz force term. In a two-dimensional electron fluid [96], total energy is equal to the kinetic energy. In a graphene

sheet, the external electrical field drifts electrons in z direction while electrons can also distribute in perpendicular (y) direction to form a two-dimensional fluid. This means that the whole energy provided by the external electrical field equals the two-dimensional electron fluid kinetic energy. However, when the graphene sheet is rolled to form a carbon nanotube, which is a quasi one-dimensional system, y direction shrinks into one point and the distributed electrons in y direction in a two-dimensional system will be at the same point in one-dimensional system. As a result, the potential energy due to repulsive force among the electrons will be significant. The external electric field provides both the potential and kinetic energies to the one-dimensional fluid.

Equation (3.9) describes electron transport in SWCNT and can be solved with the continuity equation on the surface, s′,

$$\frac{\partial \sigma}{\partial t} + \frac{\partial j}{\partial z} = \frac{e\partial n}{\partial t} + \frac{\partial (env_Z)}{\partial z} = 0, \tag{3.10}$$

where σ is the charge density and n is the electron density. The current density, $j = env_z$ and $v_z$ is the electron velocity in z-direction.

The following equation which assumes pressure, p, as the only function of the carrier density of conduction electrons, can be expressed as,

$$p = p(n) \tag{3.11}$$

The metallic SWCNT is a good conductor, the electrical field on the surface will be nearly equal to zero. Using perturbation method described in [96, 98] that the system is initially in its equilibrium state and a perturbation is applied, we can write,

$$n(z,t) = n_0 + \delta n \tag{3.12}$$

$$p(z,t) = p_0 + \delta p, \tag{3.13}$$

where $n_0$ and $p_0$ are effective the density of conduction electrons and the pressure in thermal equilibrium, respectively. δn and δp are excess carrier concentrations of electrons and the excess pressure, respectively. Considering Eq. (3.11), we can write,

$$\delta p = \delta n \frac{\mathrm{d}p}{\mathrm{d}n}\bigg|_{n=n_0} = m u_e^2 \delta n \tag{3.14}$$

In Eq. (3.14), $\mathrm{d}p/\mathrm{d}n\big|_{n=n_0} = mu_e^2$ is an abbreviate expression of the thermodynamic derivation [96] and $u_e$ is the thermodynamic speed of sound of the electron fluid under neutral environment, i.e., under no charge present. The term, thermodynamic speed of sound is a thermodynamics term, which can be used to describe response of particles in fluid under external perturbation.

For two-dimensional fluid, total energy is identical to the kinetic energy [96] and is given by,

$$E = E_K = \frac{1}{2}\left(\frac{n_0 \hbar^2 k^2}{2m}\right), \tag{3.15}$$

where multiplier ½ is for the two-dimensional ideal spin -½ Fermi fluid. When we consider one-dimensional fluid, the total energy, E is the sum of potential energy and kinetic energy. Combining Eqs. (3.6) and (3.15), we obtain,

$$E = E_K + E_P = \frac{1}{1-\alpha}\left(\frac{n_0 \hbar^2 k^2}{4m}\right), \tag{3.16}$$

where $k = (2\pi n_0)^{0.5}$ is the Fermi wave number [96]. The pressure is derivative of the total energy with respect to length in one-dimension and is obtained by substituting $k = (2\pi n_0)^{0.5}$ in Eq. (3.16),

$$p = \frac{1}{1-\alpha}\left(\frac{\hbar^2 \pi n_0^2}{2m}\right) \tag{3.17}$$

From Eqs. (3.14) and (3.17) and $k = (2\pi n_0)^{0.5}$, we obtain thermodynamic speed of sound, $u_e$ as follows,

$$u_e = \frac{v_F}{\sqrt{2(1-\alpha)}}, \tag{3.18}$$

where $v_F = \hbar k/m_e$ is Fermi velocity [96]. It should be noticed that Eq. (3.18) is modified from classical $u_e = v_F/\sqrt{2}$ [96], and takes into account electron-election interactions. However, the fluid fails to reach the thermodynamic equilibrium in one oscillation period at higher frequencies. It is corrected by replacing 2 in denominator of Eq. (3.18) by 3/(D+2) [96, 159], where D is the number of dimension. Here D = 1 for one-dimension and Eq. (3.18) reduces to the form,

$$u_e = \frac{v_F}{\sqrt{1-\alpha}} \tag{3.19}$$

In comparison to the mean-free path of electrons in Cu (40 nm) at room temperature, single-walled carbon nanotubes, on the other hand, have electron mean-free paths of the order of a micron [28]. Since the mean-free path of electrons in a SWCNT is close to 1 μm or less, the last term in Eq. (3.9) approach to zero.

Equation (3.9) can be further simplified. We assume that the electron fluid is initially in its equilibrium state and a perturbation is applied. Therefore, we consider first order of variables $v_z$ and $\mathcal{E}_z$ and neglect higher orders. Substituting Eqs. (3.12), (3.13) and (3.14) in Eq. (3.9) and considering that the derivative of $v_z$ with respected to z is zero, we obtain,

$$mn_0 \frac{\partial v_z}{\partial t} = -\frac{\partial \delta p}{\partial z} - en_0\{(1-\alpha)\mathcal{E}_z\} - mn\{\mathrm{sgn}(l)\}\nu v_z, \tag{3.20}$$

where $l$ is the length of SWCNT and sgn($l$) is the sign function defined as follows, $\mathrm{sgn}(l) = \begin{cases} 0 & \text{if} \quad l < l_{mfp} \\ 1 & \text{if} \quad l \geq l_{mfp} \end{cases}$, where $l_{mfp}$ is the electron mean-free path in SWCNTs.

The parameter α in Eq. (3.20) describes the classical electron-electron repulsive force as described previously. In Section 3.5, we will see that the repulsive force has the same effects as the electron-electron correlation described in Lüttinger liquid model [93, 94], which is a quantum phenomenon in one-dimensional system.

The distributions of the surface charge density, σ, and induced current linear density, j, are described as follows [161],

$$\sigma(z,t) = -en(z,t) = -e\{n_0 + \delta n(z,t)\} \tag{3.21}$$

$$j(z,t) = -env(z,t) = -e\{n_0 + \delta n(z,t)\}v(z,t) \tag{3.22}$$

By combining Eqs. (3.14)–(3.22) and considering perturbation, δn, we obtain,

$$\frac{\partial j(z,t)}{\partial t} + \nu j + u_e^2 \frac{\partial \sigma(z,t)}{\partial z} = \frac{e^2 n_0}{m}(1-\alpha)\boldsymbol{\mathcal{E}}_z . \tag{3.23}$$

Equation (3.23) is the transport equation for one-dimension electron fluid in a metallic SWCNT. This equation together Eq. (3.10) gives the relation of electric field, $\boldsymbol{\mathcal{E}}_z$ with electric charge, σ and current density, j.

There are several parameters in Eq. (3.23) which are still unknown. If the third term on the left-hand side of Eq. (3.23) is neglected since metallic SWCNT is a good conductor, we can obtain an equation for current density in frequency domain,

$$\hat{j} = \frac{e^2 n_0}{m}(1-\alpha)\frac{1}{\nu + i\omega}\hat{\boldsymbol{\mathcal{E}}}, \tag{3.24}$$

where $\hat{j}$ and $\hat{\boldsymbol{\mathcal{E}}}$ are, respectively, current density and electric field in frequency domain. Since $\hat{j} = \sigma\hat{\boldsymbol{\mathcal{E}}}$, we obtain,

$$\sigma(\omega) = \frac{e^2 n_0}{m}(1-\alpha)\frac{1}{\nu + i\omega} \tag{3.25}$$

In Eq. (3.25), σ is the frequency-dependent or dynamic conductivity. In microwave and infrared frequency regimes, the axial conductivity of metallic SWCNT is given by [163],

$$\tilde{\sigma}_{ZZ} = \frac{2e^2 v_F}{\pi^2 \hbar r}\frac{1}{\nu + i\omega}, \tag{3.26}$$

where $\tilde{\sigma}_{ZZ}$ is the semi-classical version of the axial conductivity.

Equating Eqs. (3.25) and (3.26), we obtain,

$$\frac{n_0}{m} = \frac{2v_F}{\pi^2 \hbar r}\left(\frac{1}{1-\alpha}\right). \tag{3.27}$$

Equation (3.27) is very useful in deriving parameters of SWCNT transmission line model, which is described in the following section.

## 3.4 Transmission Line Model

We consider a metallic SWCNT above a perfect conducting plane and assume [98] that the propagating EM wave is in quasi-TEM mode. The voltage and current intensity are expressed as follows:

$$i(z,t) = \oint \vec{j} \cdot \vec{z} dl \approx 2\pi r j(z,t) \tag{3.28}$$

$$q(z,t) = \oint \vec{\sigma} \cdot dl \approx 2\pi r \sigma(z,t) \tag{3.29}$$

Following the work of Maffucci et al. [98], combining Eqs. (3.28), (3.29) and (3.23) we obtain,

$$\mathcal{E}_z = Ri + L_K \frac{\partial i}{\partial t} + \frac{1}{C_Q}\frac{\partial q}{\partial z}, \tag{3.30}$$

where

$$R \equiv L_K \,\mathrm{sgn}(l)\nu \tag{3.31}$$

$$L_K \equiv \frac{m}{2\pi e^2 n_0}\frac{1}{1+\alpha} \tag{3.32}$$

$$C_Q \equiv \frac{1}{L_K u_e^2} \tag{3.33}$$

In Eq. (3.32), $L_K$ is the kinetic inductance per unit length of SWCNT because it is not a magnetic inductance and is related to the electron inertia. Substituting Eq. (3.27) in Eq. (3.32), we obtain,

$$L_K \equiv \frac{\pi\hbar}{4e^2 v_F} \tag{3.34}$$

In Eq. (3.33), $C_Q$ is the quantum capacitance per unit length of SWCNT and is related to quantum pressure of the electron fluid. From Eqs. (3.19), (3.33) and (3.34), we obtain,

$$\sqrt{\frac{L_K}{C_Q}} = \frac{\pi\hbar}{4e^2}\frac{1}{\sqrt{1-\alpha}} = \frac{R_0}{4}\frac{1}{\sqrt{1-\alpha}}, \tag{3.35}$$

where $R_0 = \pi\hbar/e^2 = 13\ \text{k}\Omega$ is quantum resistance [93, 98].

The parameter R in Eq. (3.30) is the resistance per unit length of metallic SWCNT. It depends on the electric field $\mathcal{E}_z$. By combining Eqs. (3.31), (3.14) and (3.2), we obtain,

$$R(\mathcal{E}_z) = \text{sgn}(l)\frac{R_0}{4}\frac{\nu}{v_F} = \text{sgn}(l)\frac{R_0}{4}\frac{1}{\lambda}. \tag{3.36}$$

Finally, we need to consider the magnetic inductance and electric capacitance. The magnetic inductance per unit length of a perfect conductor on a ground plane is given by [164],

$$L_M = \frac{\mu}{2\pi}\cosh^{-1}\left(\frac{h}{r}\right) \approx \frac{\mu}{2\pi}\ln\left(\frac{h}{2r}\right). \tag{3.37}$$

The electric capacitance per unit length of a perfect conductor on a ground plane is given by [164],

$$C_E = \frac{2\pi\varepsilon}{\cosh^{-1}(h/r)} \approx \frac{2\pi\varepsilon}{\ln(h/r)}, \tag{3.38}$$

where h is the distance of SWCNT to the ground plane. Equations (3.37) and (3.38) are accurate enough for h > 2r.

The parameters R, L and C, which are obtained above, are needed for building an equivalent circuit of metallic SWCNT interconnects. Typically, a nanotube radius is 1 nm. The oxide thickness over which SWCNT is grown is between 100 Å and 1 μm. R, L and C can be estimated as follows: $L_M \approx 1$pH/μm, $L_K \approx 3.6$nH/μm$>>L_M$ which is close to measurement results [140], $C_Q \approx 90$aF/μm and $C_E \approx 70$aF/μm. The equivalent circuit of a metallic SWCNT interconnect is shown in Fig. 3.2.

In the work of Burke [93], theoretical electrical contact resistance has been expressed as $\pi\hbar/4e^2$. Based on this theoretical contact resistance model, we have proposed an equivalent circuit model of a contact for experimental measurements [165] as shown in Fig. 3.3. In Fig. 3.3, $R_{C1}$ is the theoretical contact resistance and $R_{C2}$ and $C_C$ are parasitic resistance and capacitance, respectively, which are to be measured during test.

## 3.5 Results and Discussion

The impedance, $Z_{in}$ with open circuit termination is one of the parameters used in characterizing the SWCNT transmission line behavior. For the transmission line shown in Fig. 3.2, the $Z_{in}$ can be calculated using,

$$Z_{in} = Z_0 \frac{\cos(l\beta)}{i\sin(l\beta)}, \tag{3.39}$$

where $\beta = u_e/f$ is the propagation constant. $Z_0$ is the characteristic impedance and is given by,

$$Z_0 = \sqrt{\frac{R + j\omega L}{j\omega C}}\,. \tag{3.40}$$

Figure 3.4 shows the frequency dependence of $Z_{in}$ for 0.1 μm, 1 μm, 10 μm and 100 μm lengths of SWCNTs. SWCNT interconnects show resonances at lower frequencies. Resonances of 0.1 μm and 1 μm SWCNT are shown in Fig. 3.4 as an inset. With increasing length, the resonance frequency range increases, thus limiting the use of

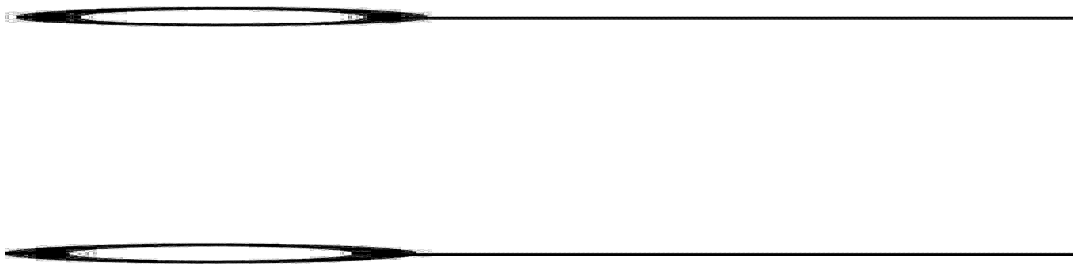


Figure 3.2: The equivalent circuit of a metallic SWCNT interconnect.

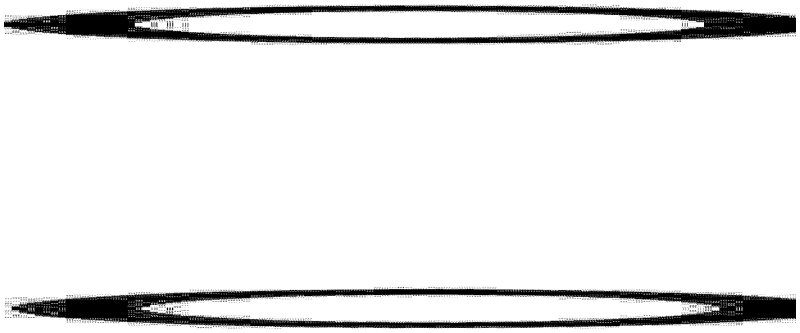


Figure 3.3: Equivalent circuit of a SWCNT contact.

SWCNT interconnects. However, considering the resonances range and applications, SWCNT interconnects are very promising. In short SWCNT interconnects (≤ 1 μm), resonance range is limited to 700 KHz, and thus, shorter length SWCNTs can be used for upper high-frequency (> 1 MHz) applications. Long SWCNT interconnects (100 μm) exhibit no resonance beyond 1 GHz and thus can be still used for ultra-high-speed circuits. The input impedance, $Z_{in}$ of 0.1 μm length SWCNT is much smaller than that of 1 μm. This is due to the mean-free path of electrons in SWCNT which is close to 1 μm and resistance, R of 0.1 μm SWCNT is zero.

Figure 3.5 shows calculations of input impedance, $Z_{in}$ for 10 μm long SWCNT interconnect using the Lüttinger liquid model, two-dimensional (2D) fluid model and our one-dimension (1D) fluid model. The models differ in resonance frequency from each other within 20 MHz and difference in resistance value is less than 16 MΩ at 1 GHz.

The other important parameter is the scattering parameter S of the SWCNT transmission line in a two-port network. In calculating S-parameters of a SWCNT, a comparison with Cu, widely used as interconnects, would be useful. In recent studies, performance of SWCNT and Cu interconnects has been compared [13, 166-169] but the S parameters and group delay have not been studied. In the following, first we will discuss modeling of Cu interconnects in terms of R, L and C parameters. As mentioned in Section 3.1, electron surface scattering and grain-boundary scattering contribute in increasing the resistivity of Cu in dimensions of nm. The following equations describe the resistivity, ρ of Cu [170],

$$\frac{\rho}{\rho_0} = 1 + \frac{3}{4}(1-p)\frac{\lambda_{Cu}}{w} \tag{3.41}$$

$$\frac{\rho_0}{\rho} = 3\left\{\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3\left(1 + \frac{1}{\alpha}\right)\right\} \tag{3.42}$$

where $\alpha = \Gamma/[d(1-\Gamma)]$, $\rho_0$ is the bulk Cu resistivity, p = 0.6 is the fraction of electrons scattered at the surface, w is width of wire, $\lambda_{Cu}$ = 40 nm is the mean free path of electrons

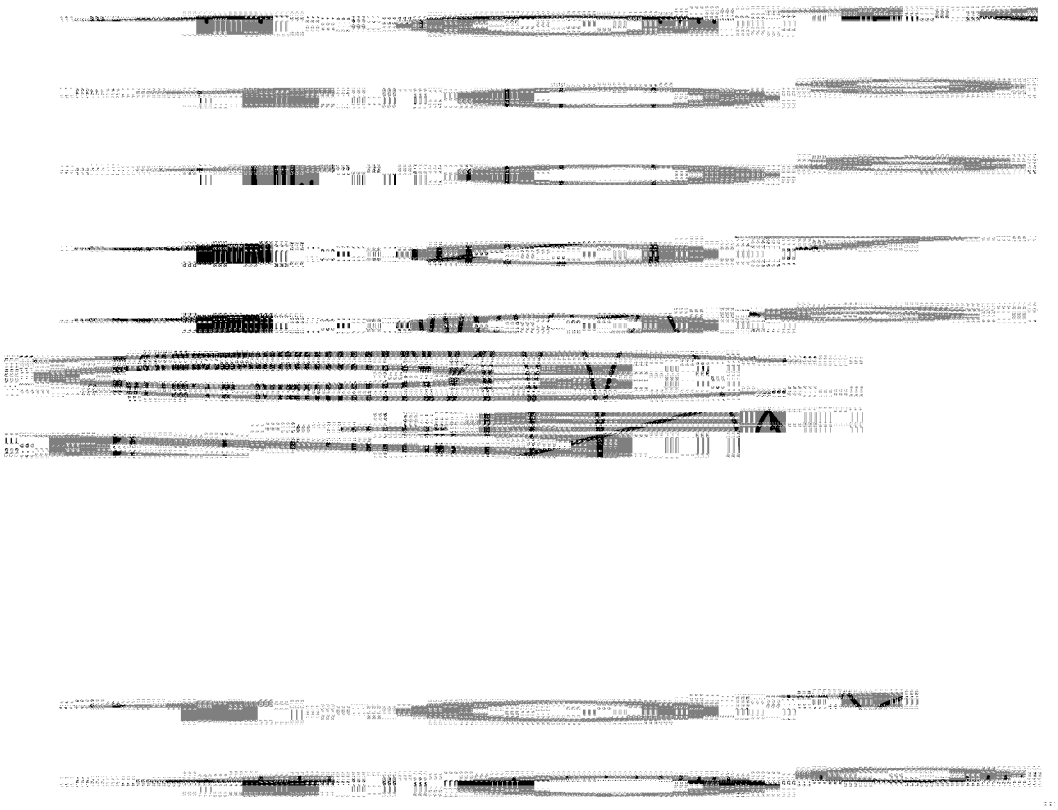


Figure 3.4: $|Z_{in}|$ versus frequency for different lengths of SWCNTs.

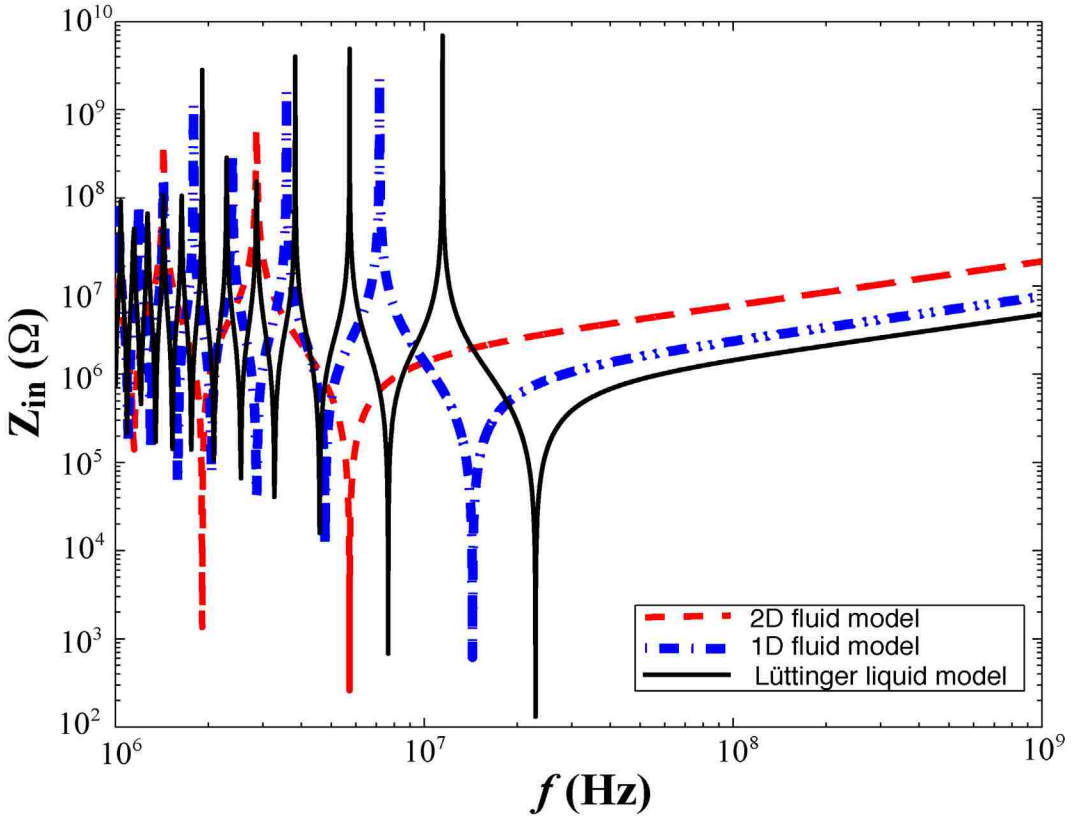



Figure 3.5: $|Z_{in}|$ versus frequency using different model for a 10 μm length SWCNT.

in bulk Cu and d is the average grain size. Γ = 0.5 is the reflection coefficient describing the fraction of electrons which are not scattered by the potential barrier at a grain boundary. Based on the above models, at 22 nm node [171], Cu resistivity for minimum wire width increases to 5.7 μΩcm.

The capacitance of Cu wire can be modeled by the following equation [172],

$$C = \varepsilon\left\{1.15\frac{w}{h} + 2.80\left(\frac{t}{h}\right)^{0.222} + \left[0.06\frac{w}{h} + 1.66\left(\frac{t}{h}\right) - 0.14\left(\frac{t}{h}\right)^{0.222}\right]\left(\frac{h}{x}\right)^{1.34}\right\}, \quad (3.43)$$

where ε is dielectric constant of the insulator, h is thickness of the insulator, t is the thickness of the wire and x is inter-wire spacing. At 22 nm node, typically, h = 216 nm, w = 27 nm, t = 54 nm and x = 27 nm.

The inductance of Cu wire can be modeled by the following equation [173],

$$L = 2\times10^{-7} l_{Cu}\left(\ln\frac{2l_{Cu}}{w+t} + 0.5 + \frac{w+t}{3l_{Cu}}\right), \quad (3.44)$$

where $l_{Cu}$ is the length of the Cu wire.

Figure 3.6 shows the schematic of a 2-port network used in study of S-parameters. In Fig. 3.6, interconnect can be Cu or SWCNT. $R_S$ is the terminating impedance. The terminating impedances of SWCNT and Cu interconnect lines used in S-parameters studies are 3.2 kΩ and 50 Ω, respectively. In the case of SWCNT interconnect lines; the terminal impedance is equal to its contact resistance.

Figures 3.7 and 3.8 show the performance of $|S_{21}|$ and $|S_{11}|$ parameters, respectively, for the SWCNT and Cu interconnects corresponding to 0.1, 1, 10 and 100 μm lengths. The calculations in Figs. 3.7 and 3.8 characterize the SWCNT transmission line with an ideal contact, $R_{contact} = \pi\hbar/4e^2$. Figure 3.7 shows the 3 dB bandwidth for $|S_{21}|$ for both SWCNT and Cu interconnects. The transmission efficiency of both the SWCNT and Cu interconnects decreases with increasing lengths. However, SWCNT transmission line has a larger 3 dB bandwidth when compared with Cu interconnects. Figure 3.7 also

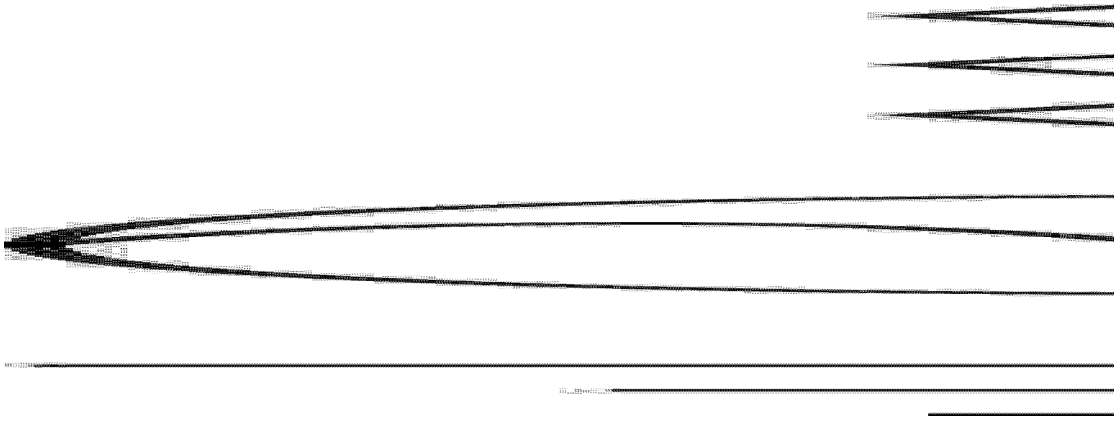


Figure 3.6: Schematic of a 2-port network of interconnects.

shows large $|S_{21}|$ for SWCNT interconnects of 1-100 μm lengths. $|S_{21}|$ for both SWCNT and Cu interconnects approaches to 0 dB for lengths less than 1 μm. Figure 3.7 also shows that the 3 dB bandwidth of short SWCNT interconnect lengths, 0.1 μm or less could exceed 1 THz.

Figure 3.8 shows $|S_{11}|$ for both SWCNT and Cu interconnects. $|S_{11}|$ of interconnects of 10-100 μm lengths show the values close to 0 dB at high frequencies. Whereas both SWCNT and Cu interconnects of 1 μm length show $|S_{11}|$ values close to -10 dB up to ~ 10 GHz then approaches to 0 dB. The performances in $S_{11}$ parameter of SWCNT and Cu interconnects close to 0 dB for lengths more than 10 μm can be attributed to impedance mismatch at the input and output. SWCNT interconnect of 0.1 μm length shows noticeable suppression of $|S_{11}|$ parameter up to 100 GHz in comparison to equivalent length of Cu interconnect due to reactive impedance and then approaches to 0 dB beyond 1 THz.

Figures 3.9 and 3.10 show $|S_{21}|$ and $|S_{11}|$ parameters for 1 μm SWCNT interconnect lengths, respectively, calculated from Lüttinger liquid model, 2D fluid model and our 1D fluid model. The insets in Figs. 3.9 and 3.10 show insignificant difference in $|S_{21}|$ and $|S_{11}|$ parameters calculated from three models. The 3 dB bandwidth obtained from Fig. 3.9 shows that our 1D fluid model gives nearly the same bandwidth as obtained from other two models.

Group delay is an import parameter. The variation from a constant value of group delay means signal distortion. Figure 3.11 shows the variation of group delay for both SWCNT and Cu interconnects with frequency. It is noticed from the Fig. 3.11 that shorter the length, lower is the delay for both SWCNT and Cu interconnects. SWCNT interconnects give group delay larger than the same length Cu interconnects but exhibits larger bandwidths. As an example, in Fig. 3.11, the group delay of 1 μm length Cu interconnect is larger than the 1 μm length SWCNT interconnect in the frequency range < 100 GHz, while it becomes smaller in the frequency range > 100 GHz. On the other hand, 1 μm SWCNT interconnect gives ~ 200 GHz bandwidth while the same length Cu interconnect gives ~ 10 GHz bandwidth. Figure 3.11 also shows significant improvement

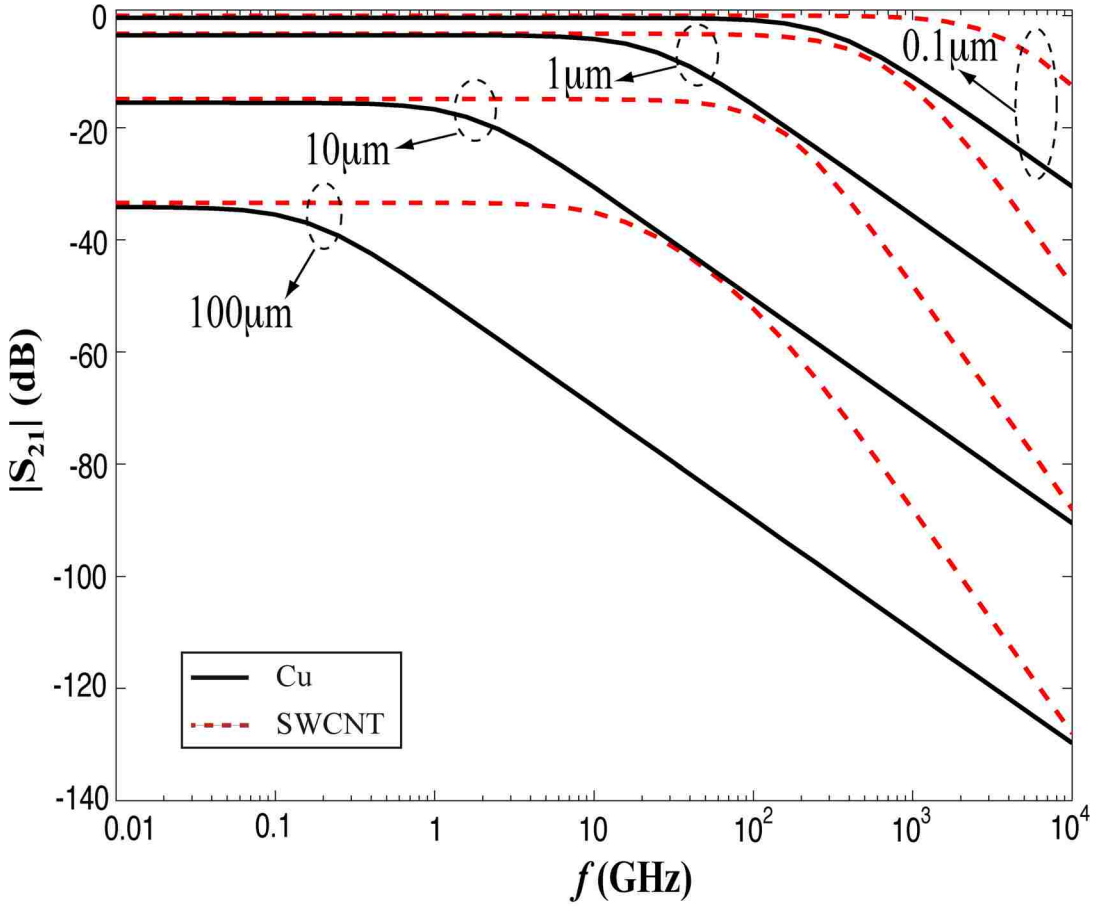



Figure 3.7: $S_{21}$ (amplitude) versus frequency for different lengths SWCNT and Cu interconnects.

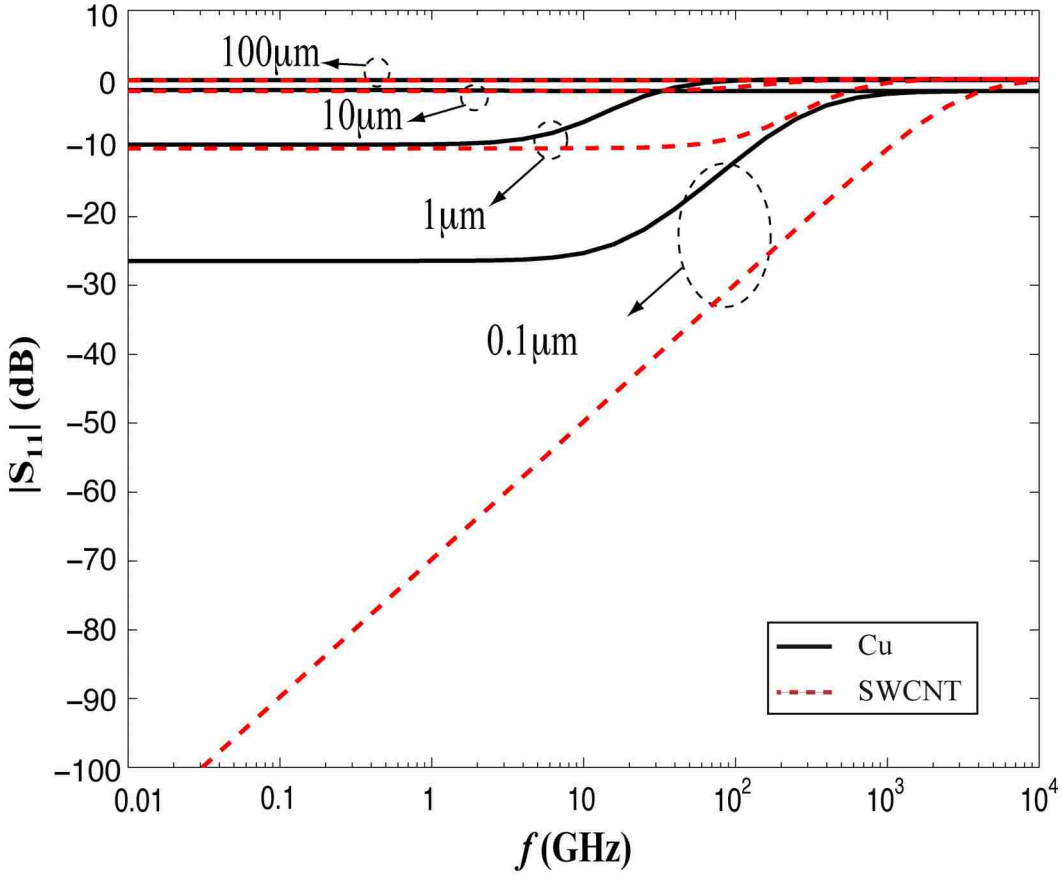



Figure 3.8: $S_{11}$ (amplitude) versus frequency for different lengths SWCNT and Cu interconnects.

Figure 3.9: $S_{21}$ (amplitude) versus frequency using different model for a 1 μm length SWCNT.

Figure 3.10: $S_{11}$ (amplitude) versus frequency using different model for a 1 μm length SWCNT.

in group delay and bandwidth for longer length SWCNTs as noticed for 100 μm SWCNT and Cu interconnect length.

We now consider the sound velocity, $u_e$ in a metallic SWCNT. The relationship shown in Eq. (3.19) is very similar to that shown in Lüttinger liquid model [93, 94]. The ratio of Fermi velocity to the sound velocity in our model is about 0.5 and the ratio of Fermi velocity to the plasmon velocity is ~ 0.2-0.3 from experiments and theoretical estimates [174, 175]. In the Lüttinger liquid model, the difference in Fermi velocity and plasmon velocity is due to electron-electron correlation, which is a quantum concept, referring to the interaction between electrons in a quantum system, the electronic structure of which is being considered. Therefore, the electron-electron correlation is distributed over the length of the SWCNT. The ratio is described by a dimensionless parameter, g. The parameter $g < 1$ for repulsive interactions, with small g meaning strong interactions, $g = 1$ describes the Fermi gas not a Fermi liquid and for attractive interactions, $g > 1$. Experiments in [155, 156] show that there are significant electron-electron correlations in SWCNTs. From earlier measurements and theoretical calculations, the value of g is between 0.2–0.33 [155, 156].

In 1D fluid model, the difference in Fermi velocity and sound velocity is due to electron-electron repulsive interaction, which is a classical concept, referring to the repulsive electrostatic forces only between electrons. Therefore, the electron-electron interaction is distributed over a short range. The ratio of Fermi velocity to sound velocity is described by a dimensionless parameter, $\sqrt{1-\alpha} \approx 0.5$.

## 3.6 Summary

In this chapter, we have proposed a simple method to develop a transmission line model for metallic single-walled carbon nanotube (SWCNT) interconnects using classical electrodynamics. The effective conducting electrons in carbon nanotubes are modeled as one-dimensional fluid considering electron-electron repulsive interactions. This method provides an equivalent circuit for analyzing the SWCNT interconnect as a transmission line. Damping effect is observed in SWCNTs due to its high resistance. It is observed in SWCNTs below 1 MHz for lengths less than 1 μm, and above 100 MHz for length longer

than 100 μm. Thus, short length SWCNTs (< 1 μm) can be used above 1 MHz. Damping thus limits the usable frequency bandwidth since it is dependent on the length. Calculations of group delays show that SWCNT interconnects can also be used above 200 GHz for short interconnects (< 1 μm) and 10 GHz for long interconnect (> 100 μm). Study of S-parameters suggests consideration of impedance matching at the input and output to minimize losses due to reflections for longer SWCNT interconnects.

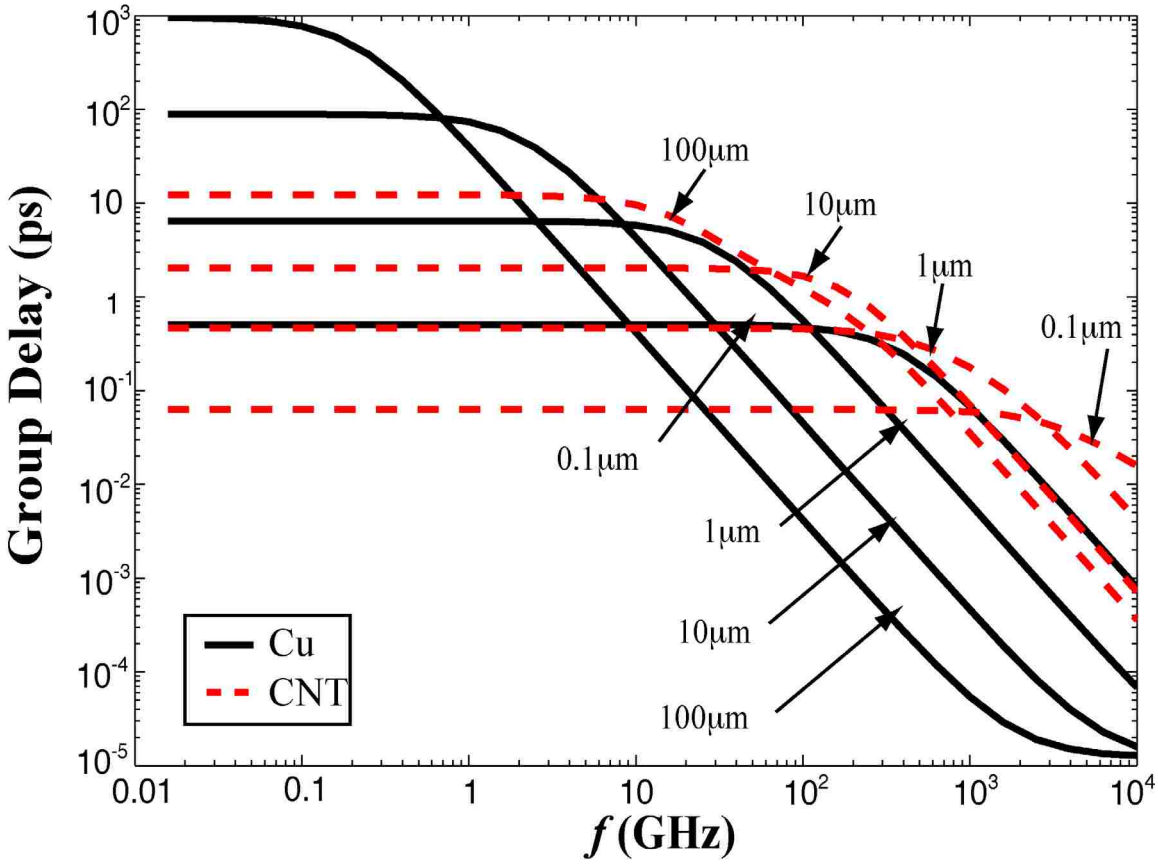



Figure 3.11: Group delay versus frequency for different lengths SWCNT and Cu interconnects.

# CHAPTER 4*

# MODELING MULTI-WALLED AND BUNDLE OF SINGLE-WALLED CARBON NANOTUBES INTERCONNECTION FOR VLSI

A good amount of research has been conducted in modeling SWCNT, SWCNT bundle and MWCNT interconnects [10, 12, 95, 176-182]. SWCNT has very large contact resistance [93, 94, 98], which limits its application as an interconnect for next generation integrated circuits. On the other hand MWCNT and CNT bundle give low contact resistance when used as the circuit interconnects [169, 183-186]. One-dimensional fluid model, which has been applied in modeling of SWCNT interconnect derived in Chapter 3 can also be extended in modeling multi-walled and bundle of single-walled carbon nanotube interconnects [187], which is described in following sections.

## 4.1 MWCNT Interconnection Modeling

MWCNTs have diameters in a wide range of a few to hundreds of nanometers. It has been shown that all shells of MWCNT can conduct if they are properly connected to contacts [183-185] and the contact resistance could reach tens of ohms, a much lower value than that of SWCNT. Naeemi et al. [180] have shown that MWCNTs can have conductivities several times larger than that of Cu or SWCNT bundles for long length interconnects.

The number of shells in MWCNTs varies. The spacing between shells in a MWCNT corresponds to van der Waals distance between graphene layers in graphite, $\delta \approx 0.34$ nm [188]. The number of metallic shells in a MWCNT can be calculated as follows:

$$M = \beta\left[1 + \frac{D_1 - D_N}{2\delta}\right], \tag{4.1}$$

where $D_1$ and $D_N$ are the outermost and innermost shell diameters, respectively. The

* Part of the work is reported in the following publications:

1. A. Srivastava, Y. Xu and A. K. Sharma, "Carbon nanotubes for next generation VLSI interconnects," *Journal of Nanophotonics*, vol. 4, no. 04169, pp.1-26, 17 May 2010.
2. Y. Xu, A. Srivastava and A. K. Sharma, "Emerging carbon nanotube electronic circuits, modeling and performance," *VLSI Design*, vol. 2010, pp. 1-8. 2010.

square bracket term is a floor function and the factor β is the ratio of metallic shells to total shells in a MWCNT. Statistically, one-third of the shells are going to be metallic and the rest semiconductor for $D_1 \leq 10$nm [188, 189]. For $D_1 > 10$nm, β increases due the interaction between adjacent shells for the MWCNT [188].

In one-dimensional fluid model [158], we regard the graphene sheet which is rolled to form a CNT is to be infinitesimally thin. The conduction electrons are then distributed over the lateral surface of the CNT cylinder shell and electrons are embedded in a rigid uniform positive charge background with a uniform surface number density. Thus, the motion of electrons is confined to the surface. Furthermore, electrical charge neutrality requires that in equilibrium the conduction electron charge density precisely cancels with that of the background positive ions. Since the van der Waals force between the carbon atoms in different shells in MWCNTs is negligible compared to valance band between the carbon atoms in the same shell [190], the one-dimensional fluid model described by Eq. (3.9) can be applied to each shell of the MWCNT with modification because the electron-electron interaction in MWCNT is different from that in SWCNT, which means the parameter α needs to be recalculated.

In addition, two assumptions are made: the electrons can only move along the z-axis; all other fluid variables, such as the tangential component of the electric field to the nanotube surface are almost uniform in the cross section plane of the shells in MWCNT. These two assumptions are valid if both the nanotube length and the smallest wavelength of the electromagnetic field are much greater than the nanotube radius [159, 160]. Furthermore, the analysis assumes room temperature operation and on distribution of elections in other directions than in z-direction for the MWCNT and SWCNT bundle interconnections.

We assume that the velocity of these electrons equals the Fermi velocity. As a result, the kinetic energy is given by,

$$E_K = 4M \times \frac{1}{2} m v_F^2 \approx 7M \text{ eV} . \tag{4.2}$$

There are two channels in each shell of MWCNT and two different spin electrons in each channel. So we consider that there are four electrons at the same point in each shell of MWCNT. We can then calculate the potential energy by moving these 4M electrons from ∞ to the same point of the MWCNT. We first consider moving every four electrons into one shell of the MWCNT. The potential energy can be obtained as follows [158, 164]:

$$E_P = \sum_{j=1}^{M}\left[\sum_{i=2}^{4}(i-1)\frac{e^2}{2\pi\varepsilon_0}\frac{1}{d_j}\right] = 6M\frac{e^2}{2\pi\varepsilon_0}\sum_{j=1}^{M}\frac{1}{d_j}, \tag{4.3}$$

where $d_j$ is diameter of shell number j.

We then consider moving all shells from ∞ to adjacent shells to construct a MWCNT. The potential energy can be calculated using following equation:

$$E_P = 6M\frac{e^2}{2\pi\varepsilon_0}\sum_{j=1}^{M}\frac{1}{d_j} + \sum_{j=2}^{M}4(j-1)\times\frac{4e^2}{2\pi\varepsilon_0}\frac{1}{d_j} = 6M\frac{e^2}{2\pi\varepsilon_0}\sum_{j=1}^{M}\frac{1}{d_j} + \frac{16e^2}{2\pi\varepsilon_0}\sum_{j=2}^{M}\frac{j-1}{d_j}, \tag{4.4}$$

The parameter α for the MWCNT can be calculated using Eq. (3.6). For example, if $D_1$ = 10 nm, $D_N$ = 1nm and β = 1 then α ≈ 0.99.

Following the derivation in [158] we can obtain an equation for each shell in a MWCNT,

$$\mathcal{E} = Ri + L_K\frac{\partial i}{\partial t} + \frac{1}{C_Q}\frac{\partial q}{\partial z}, \tag{4.5}$$

where $R \equiv L_K\,\mathrm{sgn}(l)\nu$ is the resistance of each shell in a MWCNT per unit length. $L_K \equiv \pi\hbar/4e^2v_F$ is the kinetic inductance per unit length of each shell. $C_Q \equiv 1/L_K u_e^2$ is the quantum capacitance per unit length of each shell. $u_e = v_F/\sqrt{1-\alpha}$, is the thermodynamic speed of sound of the electron fluid under a neutral environment.

The magnetic inductance per unit length of each shell can also be calculated using

Eq. (3.37). In a SWCNT, magnetic inductance is neglected compared with kinetic inductance; therefore, it can also be neglected in each shell of a MWCNT.

The outermost shell shields inner shells from the ground plane; therefore, the electrostatic capacitance $C_E$ does not exist in inner shells. However, there exists electrostatic capacitance, $C_S$ between the neighboring metallic shells and its value is given by [164, 191]:

$$C_S = \frac{2\pi\varepsilon_0}{\ln\left(D_i/D_j\right)}, \tag{4.6}$$

where $\varepsilon_0$ is the permittivity of vacuum, $D_i$ and $D_j$ are the diameters of the $i^{th}$ and $j^{th}$ metallic shells, respectively and $i < j$.

We assume that the outermost shell is metallic. In a recent work [191], we have derived an equivalent circuit of a metallic MWCNT interconnect as shown in Fig. 4.1. It is simplified as shown in Fig. 4.2 by considering that the RLC parts of all inner shells are identical. If we assume that there are no variation in distributed parameters, R and $L_K$ then R and $L_K$ are same for each shell. The potential across components of each shell in a MWCNT is equal. As a result, a simplified equivalent circuit of a MWCNT interconnect can be derived as shown as Fig. 4.3. $R_C$ in Figs. 4.1-4.3 is the contact resistance and its ideal quantum value is 3.2 kΩ per shell [94].

The values of $C_E$ and $C_Q$ are on same order. $C_Q$ of all metallic shells is in parallel and then serial with $C_E$. As a result, $C_Q$ can be neglected if M is large. Therefore, capacitance of MWCNT interconnect is smaller than that of SWCNT. In addition, the resistance and inductance of all metallic shells are parallel and M times smaller than that of SWCNT.

## 4.2 SWCNT Bundle Interconnection Modeling

Carbon nanotube can also be fabricated as a bundle which means CNTs in a bundle are parallel to each other. The spacing between carbon nanotubes in the bundle is due to the van der Waals forces between the atoms of adjacent nanotubes [71]. One of the

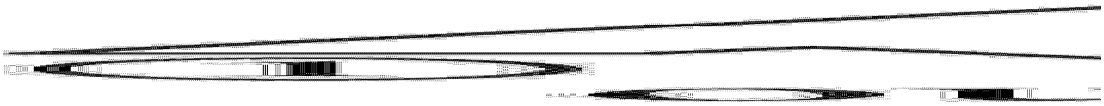


Figure 4.1: Equivalent circuit of a metallic MWCNT interconnect.

Figure 4.2: Simplified equivalent circuit of a metallic MWCNT interconnect.

Figure 4.3: Simple equivalent circuit model of a metallic MWCNT interconnect.

most critical challenges in realizing high-performance SWCNT-based interconnects is controlling the proportion of metallic nanotubes in the bundle. Current SWCNT fabrication techniques cannot effectively control the chirality of the nanotubes in the bundle [6, 192]. Therefore, SWCNT bundles have metallic nanotubes that are randomly distributed within the bundle. Avouris et al. [6] and Liebau et al. [192] have shown that metallic nanotubes are distributed with a probability, $\beta = 1/3$ in a growth process. The proportion of metallic nanotubes can, however, be potentially increased using techniques introduced in [193, 194].

Figure 4.4 shows the cross-section of a SWCNT bundle. In Fig. 4.4, d is diameter of SWCNT, $\delta = 0.34$ nm is the spacing between the SWCNT in the bundle and corresponds to the van der Waals distance between graphene layers in graphite. The distance between adjacent SWCNT is $d_b = \delta + d$. Since van der Waals forces between carbon atoms in adjacent SWCNTs are negligible compared to valance band between carbon atoms in the SWCNT [190], influence of adjacent SWCNTs on transport of electrons in SWCNT can be considered to be very small. Therefore, the one-dimensional fluid model described by Eq. (3.9) can be applied to the each SWCNT in the bundle with some modification. The electron-electron interaction in SWCNT bundle is different from that in a SWCNT, the parameter $\alpha$ needs to be recalculated to account for this effect.

Consider one of the SWCNTs in the bundle, we assume that the electrons in this SWCNT will only be affected by the electrons in the adjacent metallic SWCNTs and semiconducting SWCNTs have no effect on the conductance of the bundle. Here we assume that SWCNTs in the bundle are insulated from each other and no conduction takes place between them. To calculate the potential energy, we first consider the potential energy of each SWCNT and then consider moving SWCNT adjacent to each other to construct a SWCNT bundle. Average potential energy of electrons in a SWCNT bundle can then be described by the following equation:

$$E_P = 6\frac{e^2}{2\pi\varepsilon_0}\frac{1}{d} + \sum_{i=1}^{\Gamma}\frac{16e^2}{2\pi\varepsilon_0}\frac{1}{d_b}, \tag{4.7}$$

where $\Gamma$ is the average number of metallic SWCNTs neighboring to a single SWCNT. As

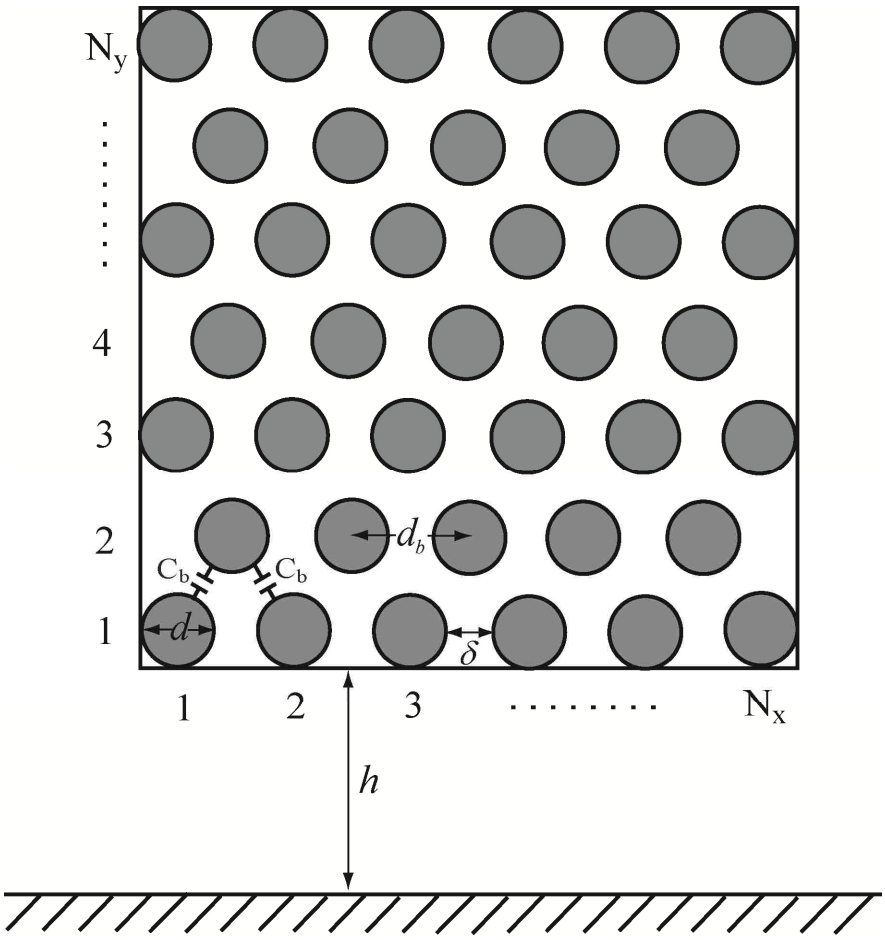



Figure 4.4: Cross-section of a SWCNT bundle interconnect.

shown in Fig. 4.4, e.g., the number of SWCNTs neighboring to the corner SWCNT is 2, the number of SWCNTs neighboring to the edge SWCNT is 4 and the number of SWCNTs neighboring to the inside SWCNT is 6.

Therefore, $\Gamma = \beta \times \left[ \frac{6N_xN_y - 4N_x - 4N_y - 2\lfloor N_y/2 \rfloor}{N_xN_y - 2\lfloor N_y/2 \rfloor} \right]$, where square brackets is the floor function.

The kinetic energy of the electrons in a SWCNT is calculated as follows [158]:

$$E_K = 4 \times \frac{1}{2} m_e v_F^2 \approx 7 \text{ eV}. \tag{4.8}$$

Now the parameter α for SWCNT bundle can be calculated using Eq. (3.6). Total number of metallic SWCNTs is $N = \beta(N_xN_y - [N_y/2])$. Following the derivation in [158] we obtain an equation for each single SWCNT in a bundle,

$$\mathcal{E} = Ri + L_K \frac{\partial i}{\partial t} + \frac{1}{C_Q} \frac{\partial q}{\partial z}, \tag{4.9}$$

where $R \equiv L_K \, \text{sgn}(l) \nu$ is the resistance per unit length of a SWCNT in a SWCNT bundle.

In Eq. (4.9), $L_K \equiv \pi\hbar / 4e^2 v_F$ is the kinetic inductance per unit length of a SWCNT in a bundle and $C_Q \equiv 1/L_K u_e^2$ is the quantum capacitance per unit length of a SWCNT in a bundle. The relation $u_e = v_F / \sqrt{1-\alpha}$ is the thermodynamic speed of sound of the electron fluid under a neutral environment.

The magnetic inductance per unit length of each SWCNT can also be calculated using Eq. (3.37). In a single SWCNT, magnetic inductance is neglected compared with the kinetic inductance. It can also be neglected in each SWCNT of a bundle since magnetic inductance is comparable to the kinetic conductance when the number of SWCNTs is above 4000 in a bundle [176], while this number is only about 500 for the

bundle with 22 nm×44 nm size. This size of the bundle corresponds to interconnections in 22 nm technology.

The SWCNTs at the bottom level shield upper levels SWCNT from the ground plane. Therefore, the electrostatic capacitance, $C_E$ does not exist in the upper SWCNTs. However, there exists electrostatic capacitance per unit length, $C_b$, between the neighboring metallic SWCNTs and its value can be calculated as follows [164],

$$C_b = \pi\varepsilon_0 \Big/ \ln\left(\frac{d_b}{d} + \sqrt{\left(\frac{d_b}{d}\right)^2 - 1}\right). \tag{4.10}$$

Figure 4.5 shows the equivalent circuit of a SWCNT bundle interconnect [195] where $N_a$ is the number of upper level SWCNTs and $N_b$ is the number of bottom level SWCNTs. For a SWCNT bundle, we assume that all SWCNTs in the bundle are identical and each SWCNT has the same potential across it [13, 196]. The circuit can be further simplified as shown in Fig. 4.6. The capacitance, $C_b$ has no effect on the circuit behavior and $\beta N_x \times C_E$ can be regarded as an electrostatic capacitance between SWCNT bundle and the ground plane.

The values of $C_E$ and $C_Q$ are nearly the same in magnitude. $C_Q$ of all metallic SWCNTs are in parallel and then is serial with $C_E$, as a result, $C_Q$ can be neglected if N is large. Therefore, capacitance of the SWCNT bundle interconnects is smaller than that of a SWCNT. In addition, the resistance and inductance of all metallic SWCNTs are in parallel in the bundle and N times smaller than that of a SWCNT.

## 4.3 Performance of MWCNT and Bundles of SWCNT Interconnects

In Section 4.1, we have extended one-dimensional fluid model for the modeling of MWCNT interconnects. To validate the model of MWCNT interconnect, we have compared the calculated resistance of MWCNT interconnect with the corresponding measured resistance from the work of Nihei et al. [183] and Li et al. [184]. The results of the comparison of calculated and measured resistances are summarized in Table 4.1.

As mentioned in Chapter 3, CNT interconnects have great potential in extending

Figure 4.5: Equivalent circuit of a SWCNT bundle interconnect.

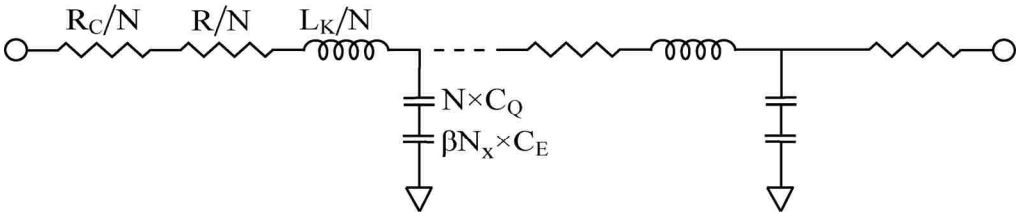



Figure 4.6: Simplified equivalent circuit of a SWCNT bundle interconnect.

the operation of circuits to higher speeds and frequencies. For applications requiring high frequencies where newer interconnect technologies and materials for interconnect are being explored, it is important to study two-port scattering parameters. Slepyan et al. [197] have conducted studies on scattering of electromagnetic waves by a semi-infinite CNT in optical regime. In this work, we focus on studying 2-port network scattering (S) parameters by CNT for interconnect applications on a chip.

We have used schematic shown in Fig. 3.6 to study S-parameters and have utilized the process parameters from the 2016 node (22 nm technology), assumed a 22 nm diameter of MWCNT of 22 nm width and 44 nm thickness of SWCNT bundle [171]. If we assume diameter of the innermost shell in a MWCNT is to be 1 nm then there are nearly 30 shells in 22 nm MWCNT. If we assume diameter of a SWCNT in a bundle is to be 1 nm then there are nearly 500 SWCNTs in 22 nm (width) × 44 nm (thickness) bundle following Fig. 4.4. The resistivity and capacitance of Cu were taken from ITRS 2007 [171]. The inductance of Cu wire can be modeled by the Eq (3.44).

SWCNT has very large contact resistance [93, 94, 98] when used as interconnects, which limits its applications as interconnects for next generation integrated circuits. On the other hand MWCNT and CNT bundle give low contact resistance when used as the circuit interconnects [169, 183-186]. Contact resistance in MWCNT and SWCNT bundle, however, will depend on the number of shells or SWCNTs being metallic. Close et al. [198-200] have demonstrated experimentally that MWCNT can function as an interconnect wire on a chip and successfully transmit GHz digital signals from one transistor to another. In Table 4.2, modeling parameters of MWCNT are compared with the equivalent model parameters from the quantum theory [180, 181]. The difference is about 20 %. However, for large diameter, such as 100 nm diameter, the difference reaches to about 60%. According to quantum theory, the number of channels increases significantly for large values of radius [196] and the semiconducting shells start contributing significantly to the number of conducting channels since their axial conductivity increases with increasing radius [163, 180]. Our semi-classical one-dimensional fluid model assumes that the number of conducting channels in a single metallic CNT shell is fixed, 2, and 0 for semiconducting shells. Therefore, the difference

in values of parameters between our model and quantum theory increases with the increase in diameter of MWCNTs. On the other hand, the parameter $\alpha$ decreases with the increase in diameter and quantum capacitance increases with the increase in diameter which is consistent with the quantum theory [180, 181]. As a result, the difference in values of parameters calculated from our model and quantum theory are not very large for small diameter MWCNTs. The electrostatic capacitance is dependent on the geometry of the structure, it is, thus, considered same for one-dimensional fluid model and quantum model [181].

Figures 4.7 and 4.8 show $S_{21}$ and $S_{11}$ parameters and comparison with the corresponding S-parameters for MWCNTs calculated using model parameters from the work of Li et al. [181]. The dimensions used in comparison correspond to 18, 22 and 32 nm diameters of the outermost shells of MWCNTs which also correspond to nm technologies. The length of MWCNTs used in calculations is 10 μm. Terminal impedance is set equal to contact resistance and $D_I/D_N = 2$ and $\beta = 1/3$. The parameters, $S_{21}$ and $S_{11}$ in both models differs by about 6% corresponding to 18 nm diameter and it is less than 6% for 22 and 32 nm diameters. The phase difference is negligible within the 3dB bandwidths. It can, thus, be stated that the one-dimensional fluid model can be easily used in studying the performance of MWCNT interconnects.

Figure 4.9 (a) and (b) show $S_{21}$ and $S_{11}$ parameters of MWCNT, SWCNT bundle and Cu interconnects of lengths corresponding to ballistic transport (1 μm), local interconnection (10 μm and 100 μm) and global interconnection (500 μm). For comparison, we choose $\beta = 1/3$ and 50 Ω terminal impedance, which is a typical impedance for high frequency transmission lines. For the MWCNT and SWCNT bundle, the electrostatic capacitance depends upon the geometry of the structure and is approximately equal to that of Cu interconnects [13, 152, 181].

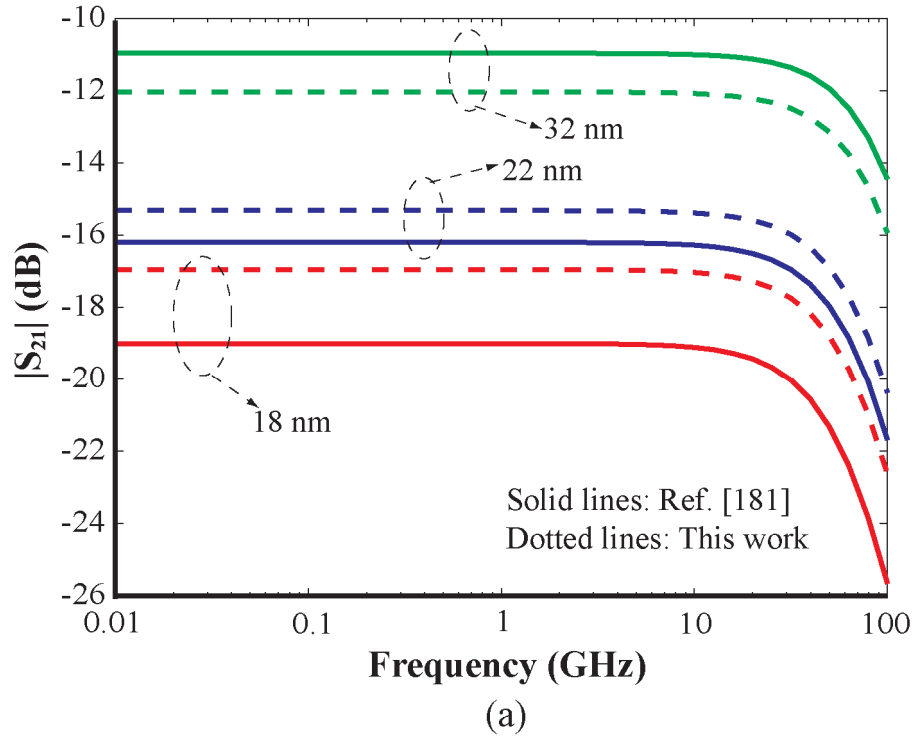
Figure 4.9 (a) shows the 3 dB bandwidths for both the CNT and Cu interconnects. The transmission efficiency of both the CNT and Cu interconnects decreases with increasing lengths. However, Cu interconnect has a larger 3 dB bandwidth in comparison with CNT interconnects. This is because Cu has smaller inductance compared with CNT interconnects. It should also be noticed that the short length CNT interconnects still have

Table 4.1: A comparison of calculated and measured resistances of MWCNT interconnects

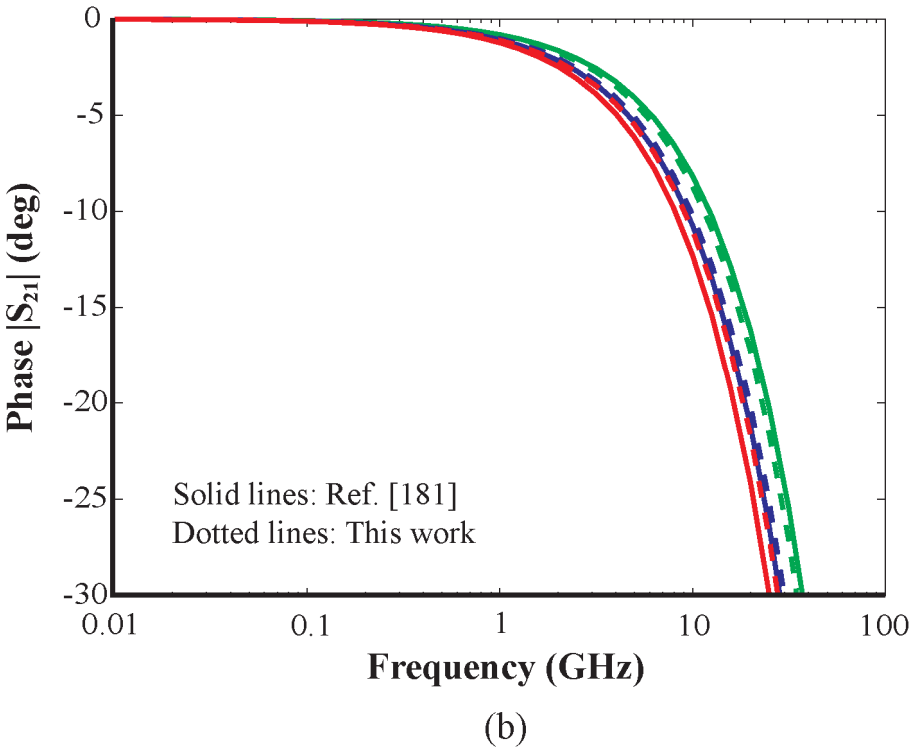
| References | MWCNT Physical Parameters | | | MWCNT Resistance (kΩ) | | |
|---|---|---|---|---|---|---|
| | Length (μm) | $D_1$ (nm) | $D_n$ (nm) | $l_{mfp}$ (μm) | Measured | Our Model |
| Nihei et al. [183] | 2 | 10 | 3.88 | <1 | 1.60 | 1.90 |
| Li et al. [184] | 25 | 100 | 50 | >25 | 0.035 | 0.042 |

Table 4.2: A comparison of MWCNT interconnect model parameters

| MWCNT Diameter (nm) | RC (cal) kΩ | RC [181] kΩ | R (Cal) kΩ/μm | R [181] kΩ/μm | LK (cal) nH/μm | LK [181] nH/μm | CQ (cal) aF/μm | CQ [181] aF/μm |
|---|---|---|---|---|---|---|---|---|
| 18 | 0.81 | 1.05 | 0.81 | 1.05 | 1.00 | 1.31 | 1280 | 1160 |
| 20 | 0.65 | 0.78 | 0.65 | 0.78 | 0.80 | 0.97 | 1600 | 1566 |
| 22 | 0.65 | 0.72 | 0.65 | 0.72 | 0.80 | 0.90 | 1600 | 1682 |
| 25 | 0.54 | 0.55 | 0.54 | 0.55 | 0.67 | 0.68 | 1920 | 2228 |
| 28 | 0.46 | 0.43 | 0.46 | 0.43 | 0.57 | 0.53 | 2240 | 2844 |
| 32 | 0.40 | 0.34 | 0.40 | 0.34 | 0.50 | 0.42 | 2560 | 3622 |
| 90 | 0.16 | 0.06 | 0.16 | 0.06 | 0.21 | 0.08 | 11080 | 19208 |
| 100 | 0.11 | 0.04 | 0.11 | 0.04 | 0.17 | 0.05 | 17680 | 29845 |

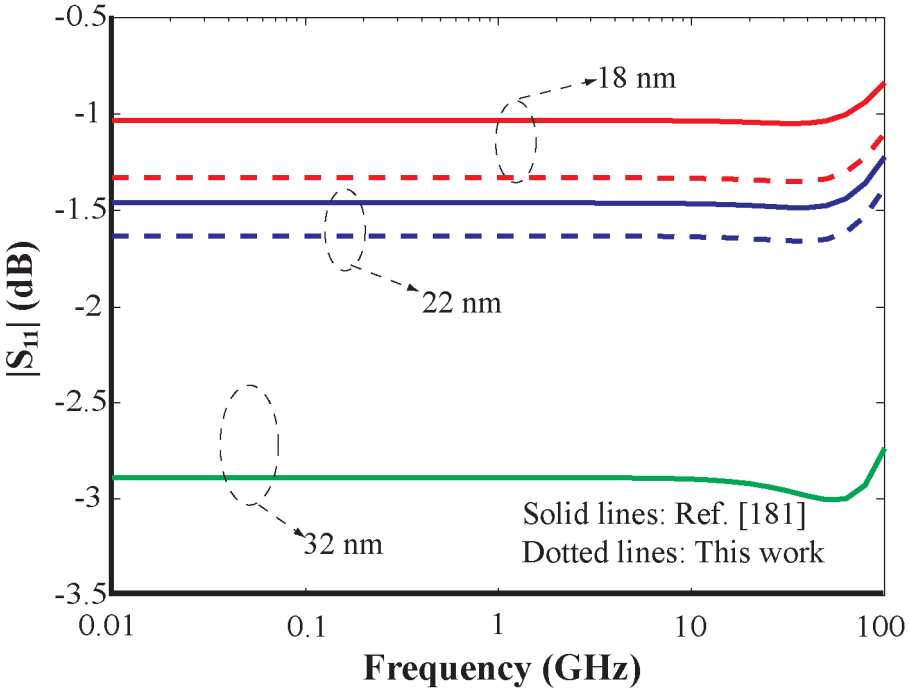



(a)

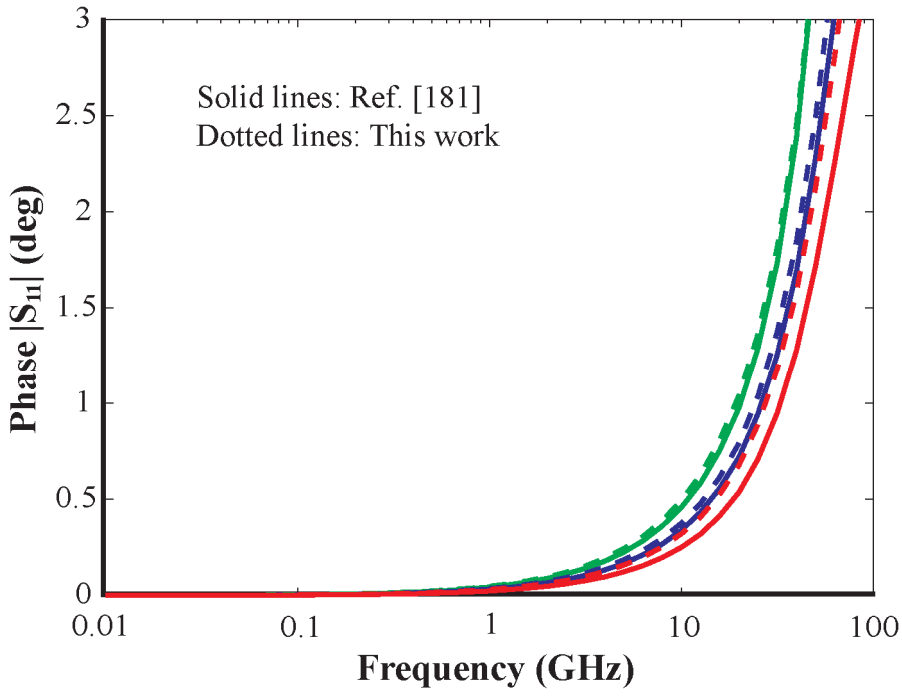



(b)

Figure 4.7: Comparison of $S_{21}$ from our model and Li et al. model [181] for MWCNT interconnects: (a) amplitude and (b) phase.




(a)




(b)

Figure 4.8: Comparison of $S_{11}$ from our model and Li et al. model [181] for MWCNT interconnects: (a) amplitude and (b) phase.

over 100 GHz 3dB bandwidth. Figure 4.9 (a) also shows large $S_{21}$ for SWCNT bundle and MWCNT interconnects than that of the Cu interconnect. This is because SWCNT bundle and MWCNT have much smaller resistances. Furthermore SWCNT bundle has more connection channels than MWCNT, it has larger 3dB bandwidth and $S_{21}$ value, which means larger transmission efficiency. In Fig. 4.9 (b) for $S_{11}$ parameters at frequencies less than 100 GHz, Cu interconnect has the largest reflection losses while SWCNT bundle interconnect has the least reflection losses. The results show that SWCNT bundle interconnect has better performance than the MWCNT interconnect. This can be explained that the number of SWCNTs in the bundle is larger than that of shells in the MWCNT of the same size. It can be shown that for 22 nm width of SWCNT bundle and MWCNT interconnects calculated number of SWCNTs in a bundle from $N = \beta(N_x N_y - [N_y/2])$ and the number of shells in a MWCNT from Eq. (4.1) are approximately 500 and 10, respectively. It means that there are more conducting channels in the bundle according to one-dimensional fluid model.

Figure 4.10 shows the CNT-FET inverter pair at 1V supply voltage. The interconnection can be Cu or MWCNT or SWCNT bundle. The delay analysis includes the CNT-FET models developed by Srivastava et al. [91] and our dynamic models reported in [201]. In this work, Verilog-AMS is used to describe CNT-FET static and dynamic models and simulated CNT-FET circuits in Cadence/Spectre.

Figure 4.11 shows transient response of a CNT-FET inverter interconnected with 10 μm long MWCNT and SWCNT bundle interconnection wires. Figure 4.11 also shows a comparison of transient response for an ideal interconnection (assuming direct connection) and Cu interconnection wire. Input signal is a 100 MHz square pulse. The propagation delays of MWCNT interconnects ($\beta = 1$ and $\beta = 1/3$) are close to ideal interconnect and are smaller than SWCNT bundle and Cu interconnects. As mentioned earlier, the number of SWCNTs in the bundle is larger than the number of shells in the MWCNT. Therefore, the resistance is smaller for the SWCNT bundle interconnect than that of the MWCNT. However, the capacitance of the SWCNT bundle interconnect is much larger than that of MWCNT. As a result, the propagation delay of MWCNT is smaller than that of the SWCNT bundle. The propagation delays are smaller for $\beta = 1$

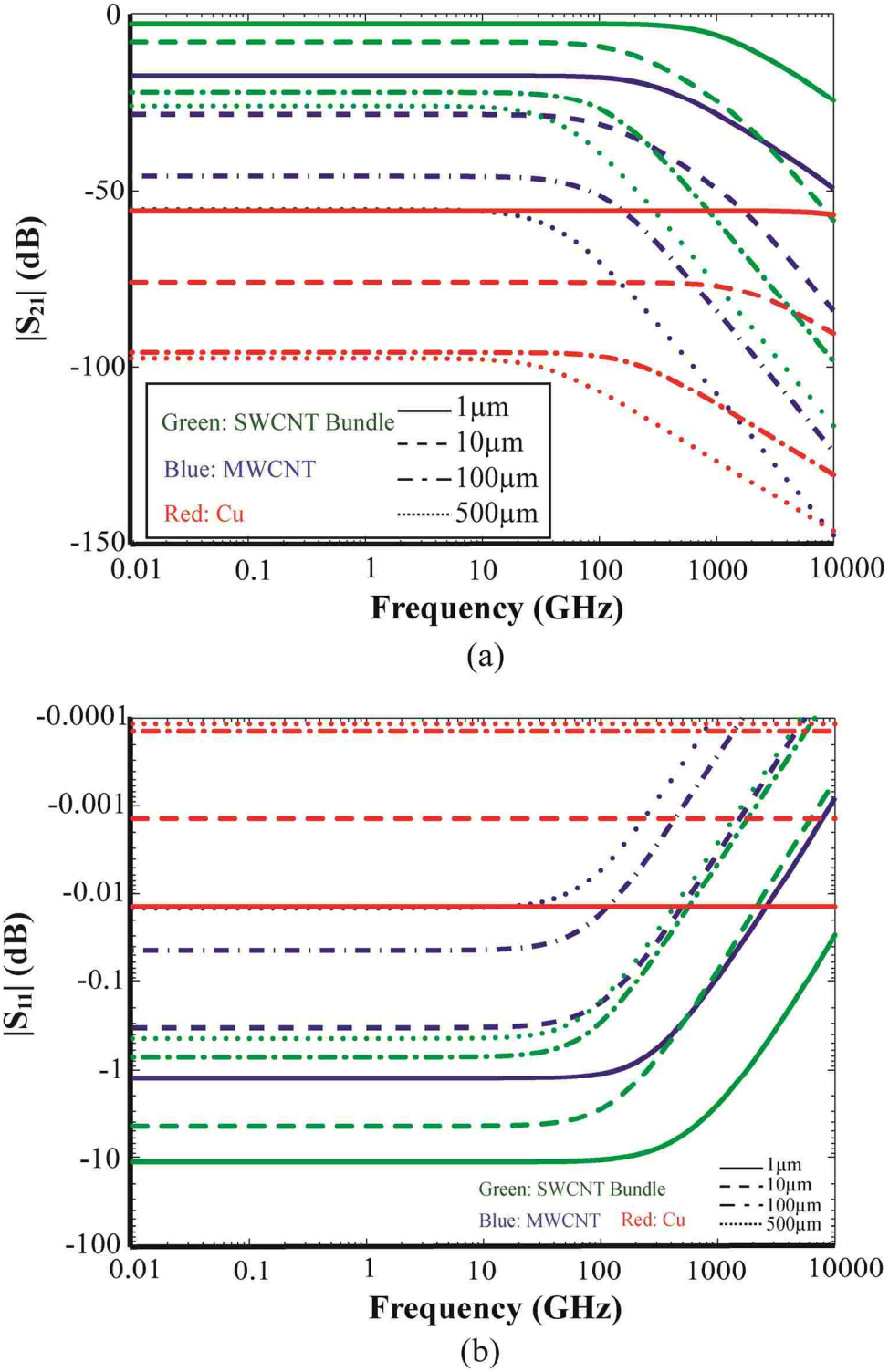



Figure 4.9: Calculated S-parameters of different interconnects: (a) $S_{21}$ (amplitude) and (b) $S_{11}$ (amplitude).

than for β = 1/3 for both MWCNT and SWCNT bundle interconnects. This can be explained by the fact that there are more interconnect channels when β increases.

One of the advantages of CNT interconnect is its large mean free path, which is on the order of several microns as compared to ~ 40 nm for Cu at room temperature. It provides low resistivity and possible ballistic transport in short-length interconnects [28]. We have also simulated a CNT-FET inverter pair with 1 μm Cu, MWCNT and SWCNT bundle interconnects using Cadence/Spectre. Local interconnects are often used for connecting nearby gates or devices with lengths on the order of micrometers. Therefore, these have the smallest cross section and largest resistance per unit length compared to global interconnects. We have utilized the process parameters from the 2016 node for 22-nm technology [171] assuming 22 nm diameter of a MWCNT, 22 nm width and 44 nm thickness of a SWCNT bundle. Relatively global interconnects have larger cross section and smaller resistivity. The lengths are on the order of hundred micrometers. We have utilized the process parameters from the 2016 node of 22-nm technology [171] assuming 33 nm diameter of a MWCNT, 33 nm width and 87 nm thickness of a SWCNT bundle. Simulations are performed for different lengths of Cu, MWCNT and SWCNT bundle interconnects corresponding to ballistic transport length (1 μm), local interconnects (10 μm, 100 μm) to global interconnects (500 μm). The results are shown in Fig. 4.12. Dependence of delay on interconnection length in Fig. 4.12 shows that the increase in delay for Cu interconnects is larger than that of MWCNT and SWCNT bundle interconnects. The delays of MWCNT interconnects (β = 1 and β = 1/3) are smaller than that of SWCNT bundle and Cu interconnects. The delays are smaller for β = 1 than for β = 1/3 for both MWCNT and SWCNT bundle interconnects and is due to more interconnect channels with increase in β.

Power dissipation is another challenge to next generation interconnects. We have simulated power dissipation for MWCNT and SWCNT bundle interconnects in 22-nm technology node and compared with the Cu wire interconnects. Table 4.3 summarizes power dissipation ratio of MWCNT and SWCNT bundle (β = 1/3 and β = 1) to Cu interconnect. CNT interconnects dissipates less power and especially for local

Figure 4.10:  Inverter pair with interconnects.

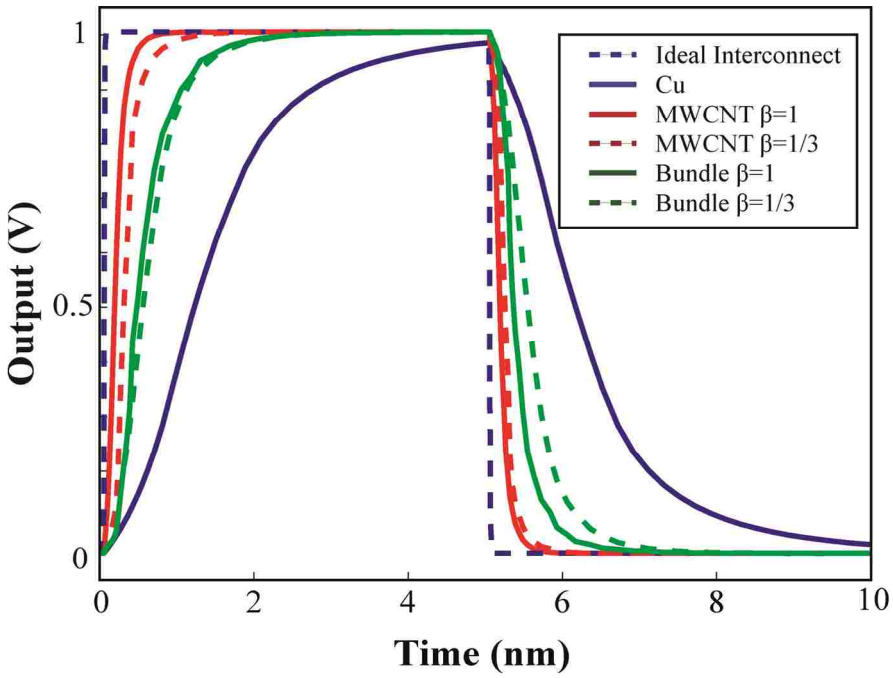



Figure 4.11: Output waveforms of an inverter pair with 10 μm length of different interconnect wires.

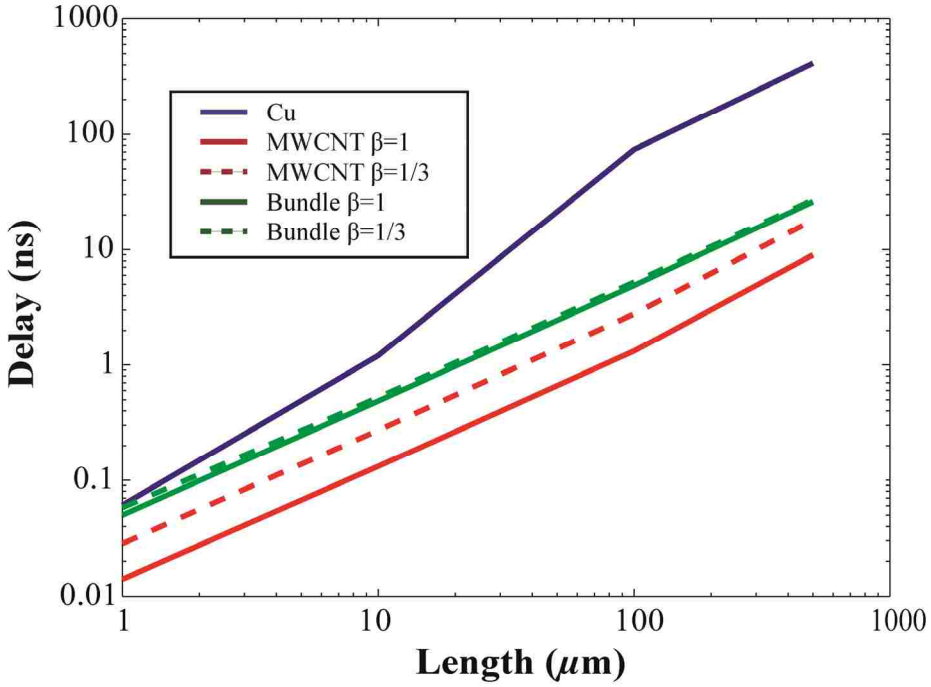



Figure 4.12: Propagation delays of interconnects of different lengths for 22 nm technology.

Table 4.3: Power dissipation ratio of MWCNT and SWCNT bundle to Cu interconnects

| Type of CNT | Normalized Power Dissipation (%) | | | |
|---|---|---|---|---|
| | Length (μm) | | | |
| | 1 | 10 | 100 | 500 |
| **MWCNT (β = 1)** | 0.070 | 0.065 | 0.339 | 1.422 |
| **MWCNT (β = 1/3)** | 0.359 | 0.418 | 2.182 | 7.591 |
| **SWCNT Bundle (β = 1)** | 0.011 | 0.015 | 0.079 | 0.137 |
| **SWCNT Bundle (β = 1/3)** | 0.036 | 0.047 | 0.256 | 0.688 |

**Note:** Normalization parameter is the length of Cu (1, 10, 100 and 500 μm). The technology node is 22 nm.

interconnections. Maximum power dissipation in CNTs interconnections is no more than the 8% of the Cu interconnections.

## 4.4 Summary

In this chapter, models for CNT interconnects, which include MWCNT and SWCNT bundle are discussed based on one-dimensional fluid theory. The one-dimensional fluid model can be applied to CNT interconnects using low resistance contacts in current low-voltage nanometer CMOS technologies. The applicability of MWCNT and SWCNT bundle as interconnect wires for next generation design of integrated circuits has been explored theoretically and compared with Cu interconnects in 22 nm technology node. Results of the one-dimensional fluid theory for SWCNT interconnect extended to MWCNT and SWCNT bundle interconnects show that MWCNT and SWCNT bundle interconnects have better performance than the Cu interconnects. MWCNT and SWCNT bundle interconnects exhibit higher transmission efficiency and lower reflection losses and less power dissipations. This is mainly due to larger conductivity of MWCNT and SWCNT bundle, proportional to the number of conducting shells (M) in MWCNT and conducting shells (N) in SWCNTs, respectively. With no special separation techniques, the metallic nanotubes are distributed with probability $\beta = 1/3$. While the proportion of metallic nanotubes can be potentially increased using techniques introduced by Peng et al. [193] and Zheng et al. [194], the delays in MWCNT and SWCNT bundle interconnects can be further decreased with increase in $\beta$ and approaching to 1. It is also noticed that with the increase in interconnection length, the delay of Cu interconnect increases faster than that of MWCNT and SWCNT bundle interconnects. For applications requiring small circuit delays MWCNT interconnects should be used due to smaller capacitances. Applications requiring large transmission efficiency and low reflection losses, CNT bundles should be used for interconnects since the numbers of conducting channels per shell are more in SWCNTs bundle than the number of conducting channels per shell in MWCNT of the same size. These findings suggest that MWCNT and SWCNT bundle can replace Cu as interconnection wires in next generation of VLSI integrated circuits.

# CHAPTER 5*

# CARBON NANOTUBE WIRE INDUCTOR

It has been demonstrated that the carbon nanotube wire is very likely to replace the Cu interconnect in sub-nanometer CMOS technologies [137]. It has also been shown that CNT wire has reduced skin effect compared to metal conductors such as the Cu and has a great promise for realization of high-Q on-chip inductors for RF integrated circuits [177]. Several models of CNT based on-chip inductor have been presented in the literature [177, 202-204], and a method of fabrication of a planar spiral CNT inductor has also been proposed by [177]. Recently, Srivastava [205] has proposed the use of high-Q on-chip CNT wire inductors in the design of LC-VCO (voltage-controlled oscillator) for phase-locked loop (PLL) systems.

Phase-locked loops are widely used in high-speed and high-frequency data communication systems. One of the important building blocks of the PLL is voltage-controlled oscillator (VCO). Digital cellular communication devices operating in GHz range widely employ VCOs. Commonly used VCO employ LC tuned circuit where quality factor of the inductor becomes crucial to the operation of the oscillator. In the past, inductor has been realized from bonding wires to retain large quality factor [206]. With shrinking device geometries and packaging requirement on-chip inductors have been realized for radio frequency integrated circuits using Al and Cu metallization. Recently Salimath [207] has reviewed the design of several CMOS voltage controlled oscillators and presented an on-chip 1.1 to 1.8 GHz VCO implementation in CMOS for use in RF integrated circuits. However, achieving high-Q inductor is still being researched.

Phase-locked loops operating in 1-2 GHz range suffer from phase noise which results in degradation in performance of RF systems where high frequency phase-locked

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* Part of the work is reported in the following publications:

1. A. Srivastava, Y. Xu, Y. Liu, A. K. Sharma, and C. Mayberry, " CMOS LC voltage-controlled oscillator design using carbon nanotube wire inductor," *Proc. 5th IASTED International Symposium on Circuits and Systems*, Maui, Hawaii, USA, pp. 171-176, August 23 – 25, 2010.
2. A. Srivastava, Y. Xu, Y. Liu, A. K. Sharma, and C. Mayberry, "CMOS LC voltage-controlled oscillator design using multiwalled carbon nanotube wire inductor," *Proc. IEEE International Symposium on Electronic System Design (ISED)*, Bhubaneswar, India, December 20-22, 2010.

loops are used. The LC VCO in PLL is the key contributor to the phase noise which uses metallic wire on-chip integrated inductor. The resistive losses lower the inductor Q-factor in such LC VCO design. In this chapter, we present design of a new 2 GHz LC VCO in TSMC 0.18 μm CMOS process using MWCNT and SWCNT bundle wires as an inductor in the LC tank circuit. We have applied our CNT interconnect model described in Chapter 4 in a well-known π-model [173] to study the properties of MWCNT and SWCNT bundle wire on-chip inductors. We have calculated Q-factors for MWCNT and SWCNT bundle wire inductors and Cu wire inductor for comparison and studied performance of LC VCO.

## 5.1 On-Chip Inductor Modeling

The widely used π model [173] is utilized to model the on-chip inductor as shown in Fig. 5.1. $L_S$ and $R_S$ are the series inductance and resistance of interconnects, respectively. The ac electrical resistivity of copper can be predicted by Drude model [208],

$$\rho(\omega) = \rho_0(1 + j\omega\tau), \tag{5.1}$$

where $\rho_0$ is dc resistivity and $\tau$ is the momentum relaxation time.

The relation between ac electrical conductivity of CNT and frequency is given by [163],

$$\sigma = \frac{\sigma_0}{1 + i\omega\tau}, \tag{5.2}$$

where $\sigma_0 = 1/R_S$, $\tau = l_{mfp}/v_F$ is electron relaxation time in CNT, $v_F$ is the Fermi velocity and $l_{mfp}$ is mean-free path.

At high frequencies, the eddy currents induced in the substrate will significantly decrease the performance of the inductor. Approximate expression for $R_{eddy}$ is given by [202],

$$R_{eddy} = 8l/\sigma tW, \tag{5.3}$$

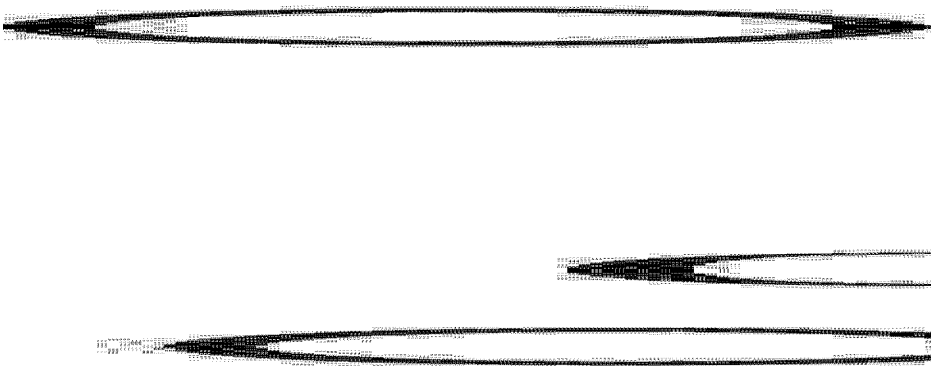


Figure 5.1: $\pi$ model of an on-chip inductor.

where t and W are thickness and width of the interconnect, respectively. σ is the conductivity of the material.

In Fig. 5.1, series capacitance ($C_S$), oxide layer capacitance ($C_{ox}$), substrate resistance ($R_{sub}$) and substrate capacitance ($C_{sub}$) are calculated by using the modeling techniques presented in [173] based on the total length of the inductor.

The performance of CNT bundle wire and MWCNT wire inductors are analyzed and compared to that of Cu inductors. We studied the utilization of CNT bundle and MWCNT wire inductors in 0.18 μm CMOS technology. The inductors considered is a 4.5 turn planar spiral inductor, which has the outermost diameter $D_{out}$ = 250 μm, conductor width W = 15 μm, conductor thickness t = 2 μm, conductor spacing S = 1.5 μm, and oxide and substrate thicknesses of 4 nm and 300 μm, respectively.

The Q factor analysis results are shown in Fig. 5.2. The maximum Q factor of SWCNT bundle (β = 1) inductor can be ~ 600% higher than that of the Cu inductor and the maximum Q factor of MWCNT (β = 1) inductor can be ~200% higher than that of the Cu inductor. Here, β is the probability factor characterizing a SWCNT being metallic in a bundle or a shell being metallic in a MWCNT. This significant enhancement in Q factor arises not only because of the lower resistance of CNTs but also because the skin effect in CNT interconnects is negligible [209]. The Q factors of CNT bundle wire inductors are much higher than that of MWCNT wire inductor because that there are more conductance channel in a bundle compared with a same size MWCNT wire, which means the resistance of a SWCNT bundle wire is smaller than that of a same size MWCNT wire.

## 5.2 LC Voltage-Controlled Oscillator (VCO)

The primary goal in the design of the oscillator is to design active devices to overcome the losses associated with the tank parallel resistance. A cross-coupled CMOS differential oscillator shown in Fig. 5.3(a) was chosen in this work due to its better phase noise performance compared to the cross-coupled single type transistor (NMOS or PMOS) topologies [207]. It consists of three components: LC tank, tail bias transistor and cross-coupled differential pair. LC tank is made by an inductor and a capacitor connected

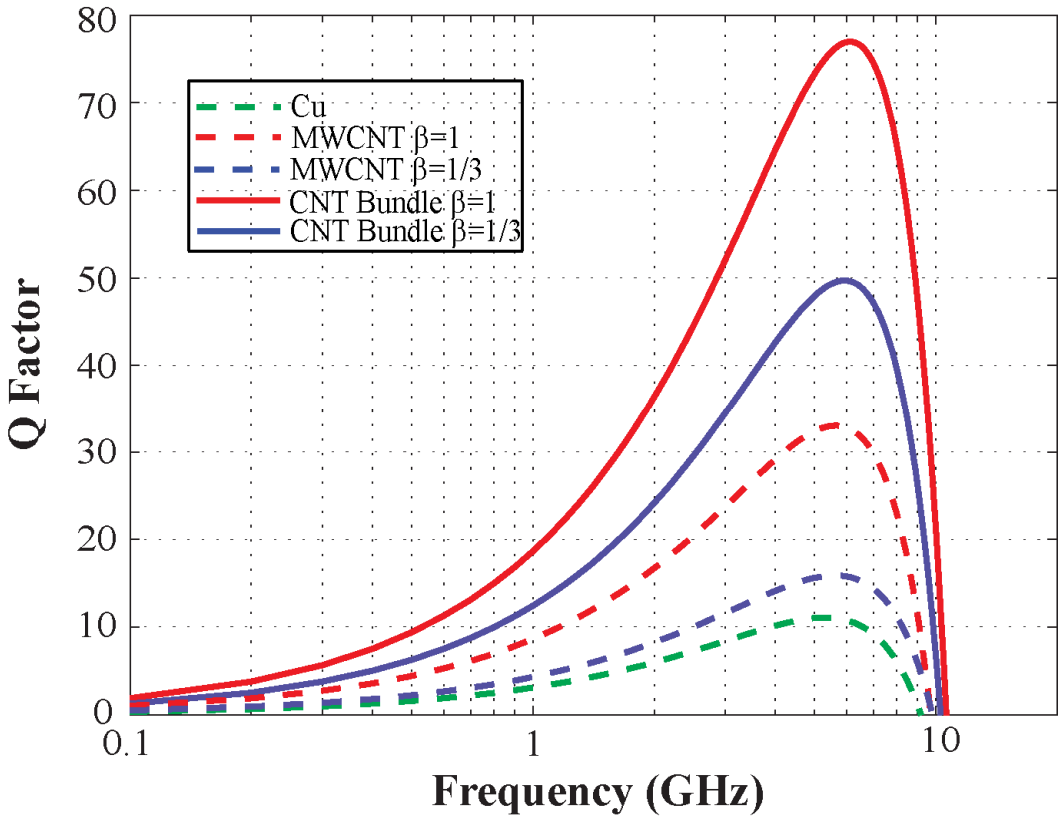



Figure 5.2: Q-factor of inductors based on CNT and Cu.

in cascade or in parallel. Figure 5.3(b) shows the equivalent circuit of this LC VCO. Here $R_C$ and $R_L$ are the resistance of capacitor and inductor, respectively and $R_P$ is frequency dependent shunt resistance.

To compute the $G_m$ of the amplifier, we need first to consider the cross-coupled NMOS transistors shown in Fig. 5.3(c). The cross-coupled CMOS transistors form the negative resistance. This negative resistance is used to offset the positive resistance in the passive components, L and C to produce an oscillation [210]. The resistance, $R_{in}$ seen at the drain of the NMOS transistor pair is given by [207],

$$R_{in} = -\frac{2}{g_m}, \tag{5.4}$$

where $g_m$ is the small-signal transconductance of each transistor. Therefore, the total transconductance of the CMOS pair can be expressed as a parallel combination of the NMOS and PMOS transistor pair negative resistance, $R_{inn}$ and $R_{inp}$,

$$G_m = \frac{1}{R_{inn} // R_{inp}} \tag{5.5}$$

The resonance frequency of LC tank circuit is given by,

$$f_0 = {}^{1}\!\Big/\!_{2\pi\sqrt{LC}}\,. \tag{5.6}$$

We designed a 2 GHz LC VCO in TSMC 0.18μm CMOS process as shown in Fig. 5.3(a) where an inductor in the LC tank circuit is realized from a CNT bundle wire and MWCNT wire. The symmetrical design of the VCO gives good phase noise performance and large voltage swing. The varactor in the circuit of Fig. 5.3(a) is implemented from an nMOSFET with source and drain tied together. The C-V curve of the varactor is shown in Figure 5.4. The voltage-controlled capacitance range is from 200 fF to 2.2 pF which makes the LC VCO to oscillate from 1.6 GHz to 3.3 GHz. If we choose the capacitor's value to be 0.5 pF, from Eq. (5.6), to get the LC VCO oscillation at 3 GHz, the value of the inductor is calculated to be 6 nH. In our 2GHz LC VCO design

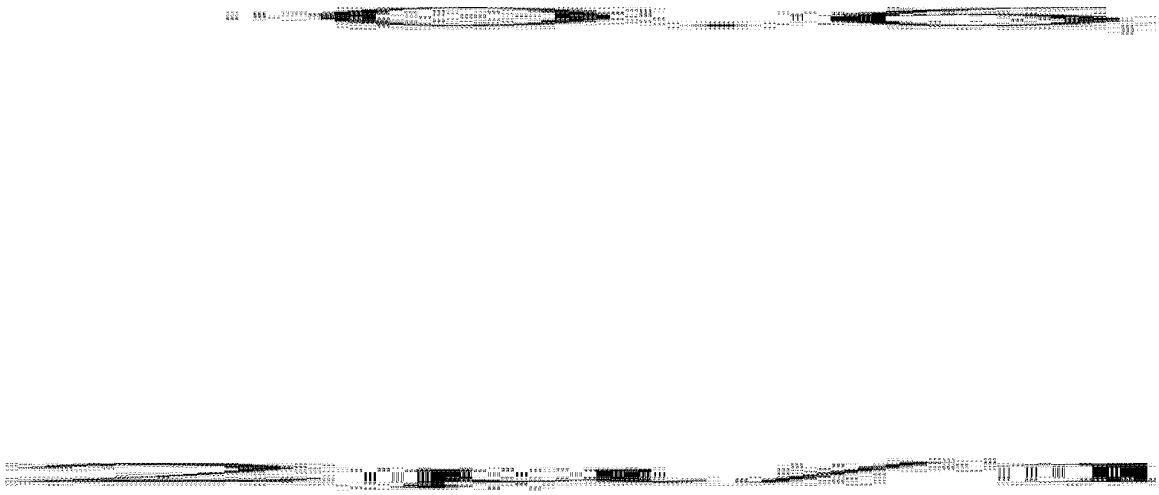


Figure 5.3: (a) Circuit diagram of a CMOS cross-coupled LC VCO, (b) equivalent circuit of LC VCO and (c) circuit to estimate the negative resistance of the cross-coupled pair.

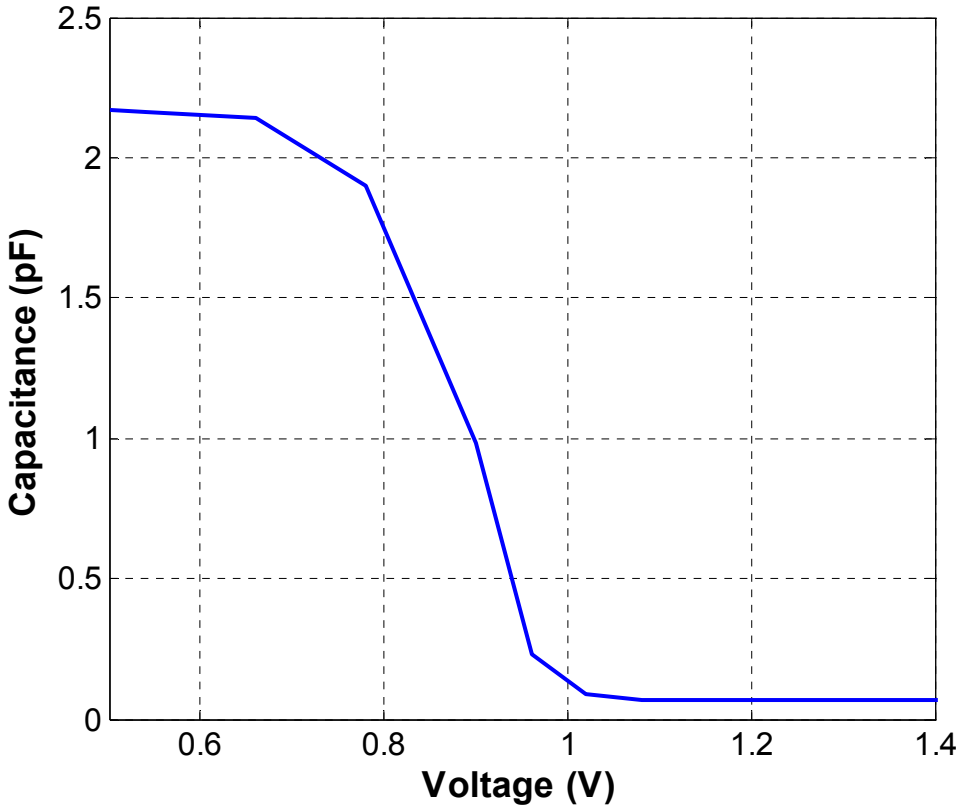



Figure 5.4: C-V curve of a varactor.

we have chosen 6 nH inductor since effective value of inductor may be less due to associated parasitics.

Figure 5.5 shows the LC VCO oscillation frequency versus control voltage for inductor with no losses (ideal), SWCNT bundle (β = 1, 1/3) and MWCNT (β = 1, 1/3) wire inductors and Cu wire inductor. It is also shown that LC VCO with MWCNT wire inductors have higher oscillation frequencies than that with the Cu wire inductor. CMOS LC VCO with SWCNT bundle (β = 1/3) wire inductor oscillates between 1.3 – 2.6 GHz which is higher in comparison to oscillation frequency range 1.1 – 2.4 GHz of LC VCO with Cu wire inductor. It is also shown that VCO with SWCNT bundle wire inductor (β = 1) has higher oscillation frequency than that with the Cu wire inductor. For example, oscillation frequency of CNT bundle (β = 1) wire inductor is higher by ~ 10% at 1.2 V than that with Cu wire inductor. Moreover at this 1.2 V control voltage, the Q factor of Cu inductor is 7 and Q factors of SWCNT bundle inductors are 38 (for β = 1) and 26 (for β = 1/3). Also, the oscillating frequency is higher in VCO with MWCNT and SWCNT bundle wire inductors for β = 1 than that of β = 1/3.

The phase noise is modeled by using the Leeson's phase noise density equation [211]:

$$L(\Delta f) = \left(\frac{1}{8Q^2}\right)\left(\frac{FkT}{P}\right)\left(\frac{f_0}{\Delta f}\right)^2, \tag{5.7}$$

where k is the Boltzmann's constant, T is the temperature, P is the output power, F is the noise factor, Q is the quality factor of the LC tank, $f_0$ is the oscillation frequency and Δf is the offset frequency from $f_0$.

Since resistance of MWCNT and SWCNT bundle wire inductors are smaller than that of Cu wire inductor, the losses are smaller, which make the Q of LC tank circuit higher. Therefore, phase noise decreases following Eq. (5.7). Figure 5.6 shows the phase noise of the LC VCO at 2 GHz tuning frequency. The LC VCO phase noise using inductor with no losses (ideal) is -70dBc/Hz at 10kHz offset frequency from the carrier and -123dBc/Hz at 10MHz offset frequency from the carrier.

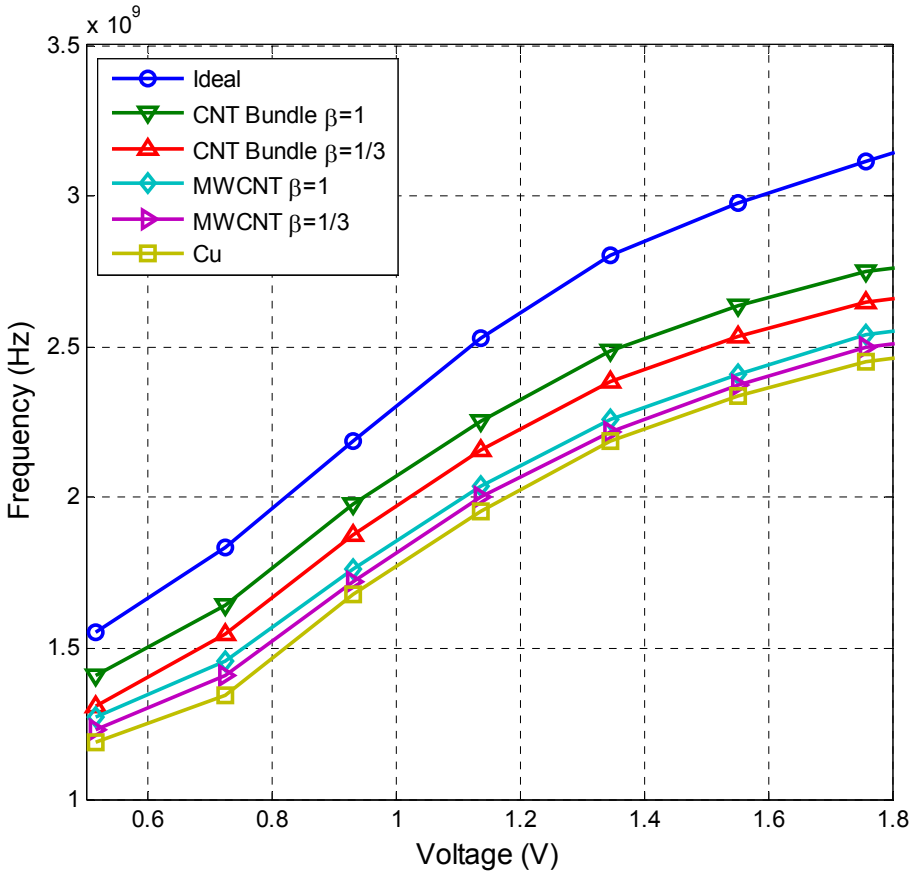



Figure 5.5: VCO oscillation frequency versus control voltage with difference inductors.

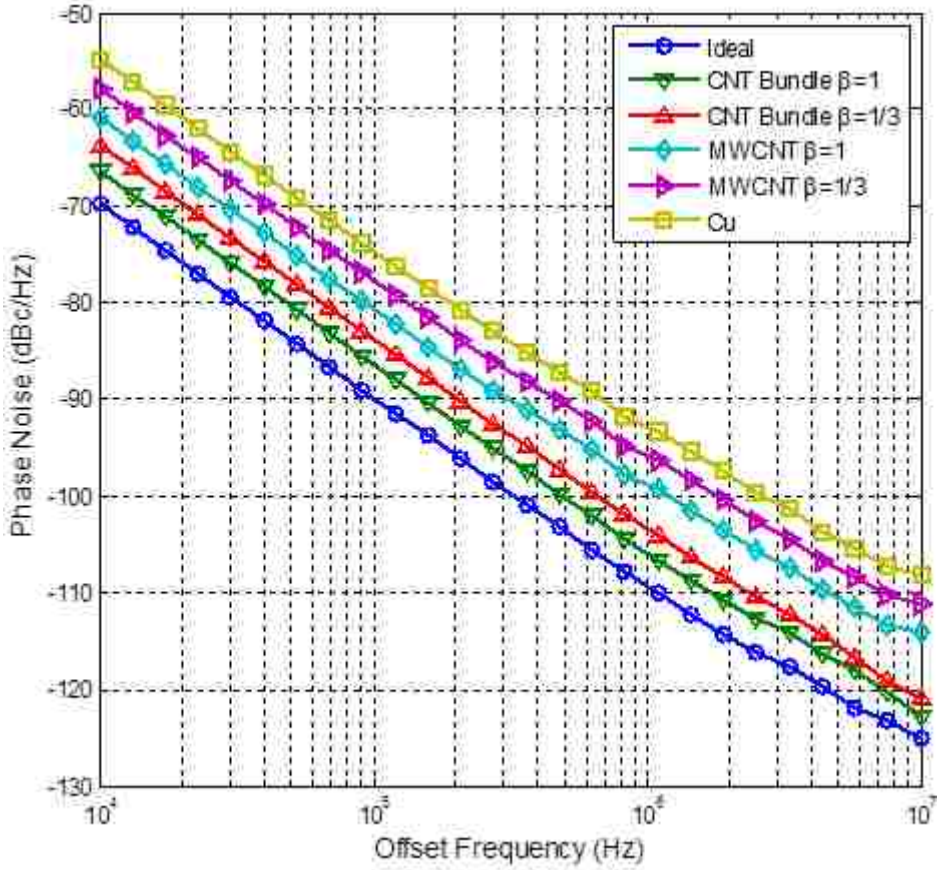



Figure 5.6: VCO phase noise versus offset frequency.

The LC VCO with SWCNT bundle inductors has about 10 dBc/Hz smaller phase noise than that with Cu wire inductors. Moreover, at this 2 GHz tuning frequency, the Q factor of Cu inductor is 7 and Q factor of CNT bundle inductors are 36 (for $\beta = 1$) and 25 (for $\beta = 1/3$). The phase noise is smaller in LC VCO with SWCNT bundle wire inductors for $\beta = 1$ than $\beta = 1/3$. The VCO with MWCNT wire inductors has about 5 dBc/Hz smaller phase noise than that with Cu wire inductors. The phase noise is smaller in LC VCO with MWCNT inductors for $\beta = 1$ than $\beta = 1/3$.

When Q-factors of Cu, MWCNT and SWCNT bundle wire inductors are compared, the SWCNT bundle wire inductor shows high Q at the resonance. Its effect is clearly reflected on the oscillation frequency and phase noise of LC VCO simulations. The LC VCO shows significantly improved performance in oscillation frequency and phase noise using CNT wire inductors as compared to the Cu wire inductor. Furthermore, LC VCO using SWCNT bundle wire inductor shows better performance that the LC VCO using MWCNT wire inductor.

## 5.3 Summary

We have utilized our MWCNT and SWCNT bundle interconnects model in a widely used $\pi$ model to study the performances of MWCNT and SWCNT bundle wire inductors and compared them with Cu inductors. The calculation results show that the Q factors of CNT wire (bundle and MWCNT) inductors are higher than that of the Cu wire inductor. This is mainly due to much lower resistance of CNT and negligible skin effect in carbon nanotubes at higher frequencies. The application of CNT wire inductor in LC VCO is also studied and the Cadence/Spectre simulations show that VCOs with CNT bundle wire inductors have significantly improved performance such as the higher oscillation frequency, lower phase noise, due to their smaller resistances and higher Q factors. It is also noticed that CMOS LC VCO using SWCNT bundle wire inductor has better performance when compared with the performance of LC VCO using MWCNT wire inductor due to its lower resistance and higher Q factor.

# CHAPTER 6*

# ENERGY RECOVERY TECHNIQUES

Energy recovery techniques are playing an import role in modern electronic circuit design due to urgent need of low power dissipation. More so with increasing demand for portable communication and computing systems, power dissipation has become one of the major chip design concerns. Circuit level techniques including energy recovery techniques have been researched for low power design. Compared with energy recovery techniques, special cooling techniques like cryogenics [212] would demand a paradigm shift in the technology and would not be cost-effective. Aggressive scaling of the silicon technology has always been associated with the need to realize low power at higher performance. The conventional approaches for active power reduction are to scale down the supply voltage, to decrease the load capacitances and to reduce signal transitions. However, to maintain sufficient noise margin, a reasonable supply voltage is required. The device dimension and the associated parasitic limit load capacitance scaling. With increasing processing speed, the number of signal transitions per unit time is fast increasing. Furthermore, an exponential increase in transistor count per chip has led to an alarming increase in the power density on the chip. Advancing into an era of nanotechnologies, device dimensions would shrink further and on-chip power density would reach such magnitudes that conventional cooling techniques would not be able to handle. Innovations in the cooling technology should thus be augmented with new ways of circuit design such that the heat dissipated on a chip can be lowered and kept within certain limits.

Energy loss or heat dissipation in a circuit is caused by the following three mechanisms:

I. Energy loss occurs when there is a voltage difference between the source and drain

* Part of the work is reported in the following publications:

1. A. Srivastava, Y. Xu and R. Soundararajan, "Energy recovery techniques for CNT-FET circuits," *Proc. International Symposium on Electronic System Design (ISED)*, Bhubaneswar, India, December 20-22, 2010.
2. Y. Xu and A. Srivastava, "New energy recovery CMOS XNOR/XOR gates," *Proc. 50th IEEE Midwest Symposium on Circuits and Systems (MWSCAS)*, Montreal, Canada, pp. 948-951, August 5-8, 2007.

terminals and the transistor turns on. Energy loss in a conventional logic belongs to this category.

II. Energy loss due to charge transfer from one capacitor to other when these are connected by a switch of finite resistance.

III. Subthrehold operation and gate tunneling cause an increase in leakage current and results in energy loss.

Thus, on-chip power densities will be a big challenge and it is where the energy recovery techniques are expected to play an important role in electronic circuit designs. Energy recovery techniques for CMOS circuits are well developed, and these techniques can be applied to CNT-FET integrated circuit design to examine the effect of power density. Hwang et al. [213] have applied CMOS energy recovery techniques in CNT-FET circuits. However, more research is needed to develop an energy efficient recovery technique for CNT-FET circuits. The exclusive-OR (XOR) and exclusive-NOR (XNOR) gates are well known for their roles in larger circuits such as full adders and parity checkers [214]. Therefore, an optimized design of XNOR/XOR gates using energy recovery techniques can certainly benefit the performance of the larger circuits where these are used. In this work, we present the design of energy recovery CNT-FET circuits which is based on our earlier work in energy recovery CMOS circuits and CNT-FET models [91, 215, 216].

## 6.1 Energy Recovery Logic (ERL)

Different ERL families have been proposed in [213, 215, 217-220] for CMOS circuits and have been used in this work to estimate reduction in on-chip power density of CNT-FET circuits. Some of these ERL design techniques are described as follows:

### 6.1.1 2N-2N2P Logic

The name 2N-2N2P is based on the convention of using the number of transistors in the inverter gate [217]. Figure 6.1 (a) illustrates the CMOS circuit of 2N-2N2P XNOR/XOR logic. 2N-2N2P is a revised version of Efficient Charge Recovery Logic

Figure 6.1: (a) CMOS circuit of 2N-2N2P XNOR/XOR gate and (b) timing for 2N-2N2P XNOR/XOR.

(ECRL) [218]. Similar to ECRL, the pull-down network, which is helpful in fast discharging during the evaluation phase, is complementary to each other. It implements the required logic and its inverse, for XNOR/XOR logic they are $(A\bullet\overline{B})+(\overline{A}\bullet B)$ and $(A+\overline{B})\bullet(\overline{A}+B)$, respectively. In 2N-2N2P, the power supply, Φ is trapeziform wave as shown in Fig. 6.1 (b). In the RESET (first) phase, the inputs (A and B) are low, the outputs are complementary (one high, the other low), and the power supply ramps down. $\overline{Out}$, because its PMOS is held on by the low Out, will "ride" the ramp down so that at the end of the first phase both $\overline{Out}$ and Out will be low. It is adiabatic for $\overline{Out}$ ramping down. In the WAIT (second) phase the power-supply stays low, maintaining both $\overline{Out}$ and Out low (the necessary condition for the next cascaded logical gate, which is delayed by one quarter cycle, to perform its RESET phase) and the inputs are evaluated. In the EVALUATE (third) phase, the power supply ramps up so that $\overline{Out}$ and Out will evaluate to a complementary state and it is adiabatic for $\overline{Out}$ ramping up. At the end of EVALUATE, the outputs will always be complementary. This condition is guaranteed by the cross coupled inverters. In the HOLD (fourth) phase the power supply clock stays high while the inputs ramp down to low. Gate outputs remain valid for the entire phase.

Since there are energy losses due to nonzero voltage drop needed to turn on unidirectional devices, 2N-2N2P is covered under partial Energy Recovery Logic (ERL) family [213].

### 6.1.2 Quasi-Static Energy Recovery Logic (QSERL)

The structure of quasi-static energy recovery logic (QSERL) [219] gate is as shown in Fig. 6.2(a). QSERL is based on static complement logic with two additional diodes which provide the charging and discharging paths. QSERL uses two complementary sinusoidal supply clocks as shown in Fig. 6.2(b), each of which consists of two phases: evaluation and hold. An n-tree and a p-tree realizes the pull down and pull up networks, respectively, similar to static CMOS logic. In this logic, energy consumed to charge the output node capacitance is provided by the clocked power. In the next half cycle, the energy is recovered by the other complementary clocked power. However,

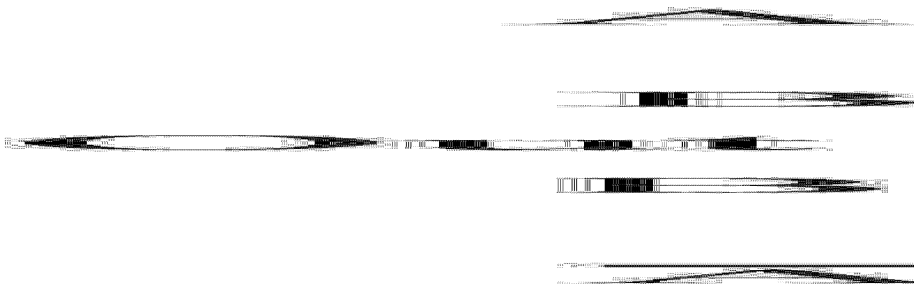


Figure 6.2: (a) Quasi-static energy recovery logic (QSERL), (b) Complementary clocked power supplies, (c) CMOS circuit of QSERL XNOR/XOR gate and (d) separated QSERL XNOR and XOR gates.

energy is lost because of the diode voltage drop along charging and discharging paths. If there is no transition during hold phase, the output signal remains constant. The structure of QSERL XNOR/XOR gate [219], which is studied in our work is as shown in Fig. 6.2(c). Supply clocks are same as in Fig. 6.2(b). This symmetrical design provide complementary outputs and can be regarded as the combination of two QSERL XNOR and XOR gates as shown in Fig. 6.2(d).

### 6.1.3 Clocked Adiabatic Logic (CAL)

Clocked adiabatic logic (CAL) [220] shown in Fig. 6.3 (a) is a dual-rail logic that can operate either from a single-phase ac power clock supply in the adiabatic mode or from a dc power supply in the non-adiabatic mode. By addition of the control switches M1 and M2 in series with the logic trees, logic gate chain can operate with a single clocked power supply Φ. Logic evaluation is enabled by activating the auxiliary clock (CX). In the next clock period, the auxiliary clock is deactivated and outputs hold the value corresponding to the computed during the previous evaluation phase. In the cascade connection, these control switches of each stage are activated alternatively by the auxiliary clock CX and its complementary signal $\overline{CX}$ .

Idealized CAL timing waveforms are shown in Fig. 6.3 (b). In evaluation phase, CX = 1 enable the logic evaluation. For A = 1 and B = 1, XNOR (Out) closely follows Φ. In hold phase, CX = 0 disables the logic evaluation. The previously stored logic is repeated at the Out and $\overline{Out}$ , regardless of the inputs.

### 6.1.4 New CAL XNOR/XOR Gate

Figure 6.4(a) shows new improved CAL XNOR/XOR gates that was proposed in our previous work [215]. Same as CAL, the cross-coupled inverters provide the memory function. Auxiliary timing control clock signal (CX) is used to realize an adiabatic inverter and logic functions with a single power clock [220]. This signal controls transistors M1 and M2 that are in series with the input logic trees, respectively. We have modified CMOS trees to replace traditional NMOS logic trees [221] so that they do not need additional power supply to function as these are separated with the cross-coupled

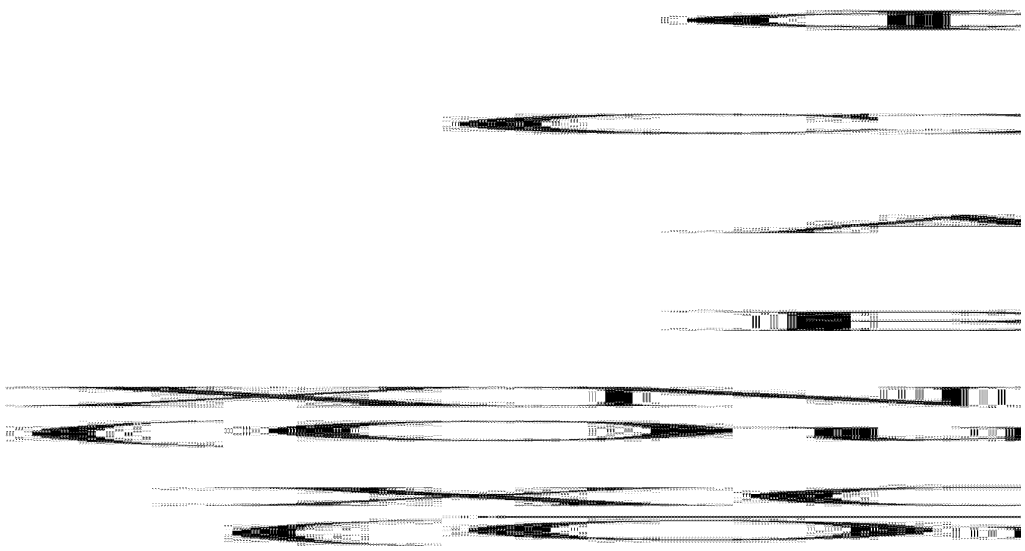


Figure 6.3: (a) CMOS circuit of CAL XNOR/XOR gate and (b) idealized CAL timing waveforms.

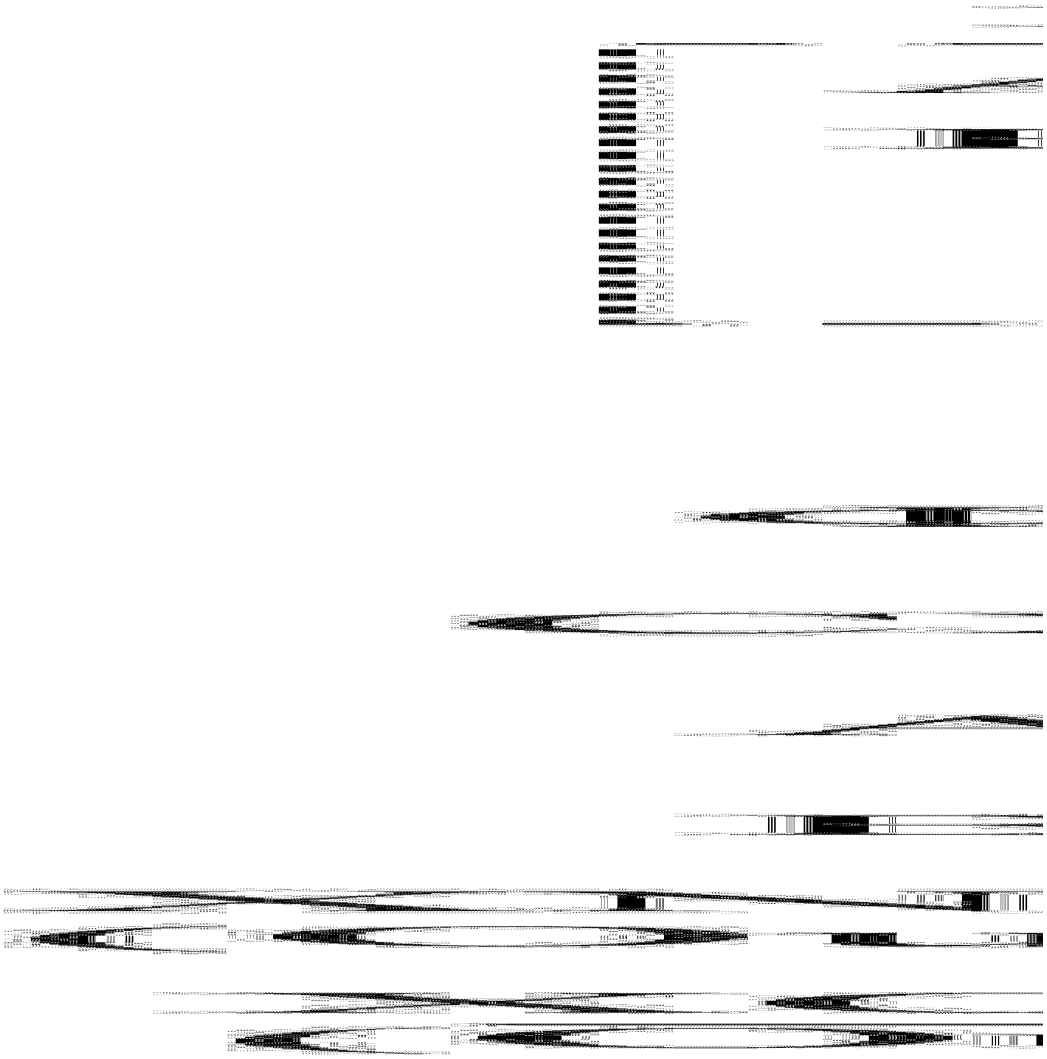


Figure 6.4: (a) CMOS circuit of new CAL XNOR/XOR gate and (b) ideal new CAL input waveforms. Note: XOR(O/P) = $A\overline{B} + \overline{A}B$ and XNOR(O/P) = $AB + \overline{A}\,\overline{B}$.

inverters by M3 and M4.

Input timing waveforms that we used is same as in traditional CAL logic and are shown in Fig. 6.4(b). Φ is trapeziform wave as a power clock and CX is an auxiliary clock to enable the gate function. The inputs are two complementary trapeziform waves. In the evaluation phase, the auxiliary clock CX enables the logic evaluation. For example, A = 1 and B = 1, M2 and M4 are ON, causing $\overline{\text{Out}}$ connected to ground, i.e., $\overline{\text{Out}}$ (XOR) = 0, and thus allowing Out (XNOR) to closely follow the power clock waveform. In the hold phase, the auxiliary clock CX = 0 disables the logic evaluation. The previously stored logic state repeats at outputs regardless of inputs, so that the stage that follows can perform logic evaluation.

### 6.1.5 Simulation Results

We used Predictive Technology Models (PTM)* for 90 nm CMOS and the Cadence/Spectre for circuit simulations. The user defined parameters are: effective length, $L_{eff}$ = 35 nm with 20% tolerance, threshold voltage, $|V_{th}|$ = 0.18 V, $V_{DD}$ = 1.2 V and source drain resistance $R_{dsw}$ = 180 Ω (NMOS) and 200 Ω (PMOS). We simulated the CAL of Fig. 6.3(a), new-CAL of Fig. 6.4(a), 2N-2N2P of Fig. 6.1(a) and QSERL of Fig. 6.2(a) in MHz range. Figure 6.5 shows the input and output waveforms of new CAL that is same as Fig. 6.4(b). Figure 6.6 shows the simulated energy dissipation of ERL XNOR/XOR gates. The clocked power (Φ) frequency of these gates is 20 MHz. The duration of simulation is 100 μs so that the energy dissipation of these four ERLs can be shown clearly.

For conventional non-energy recovery logic the active power dissipation is proportional to the clock frequency. However, for energy-recovery techniques, the power dissipation depends on the rise time of supply clocks and inputs. Figure 6.7 shows the power dissipation versus clocked power frequencies of four kinds of energy recovery XOR/XNOR logic. As the operating frequency increases, rise time decreases thereby

* Predictive Technology Model (PTM). Available: http://www.eas.asu.edu/~ptm/.


Figure 6.5: Simulated New CAL waveforms.

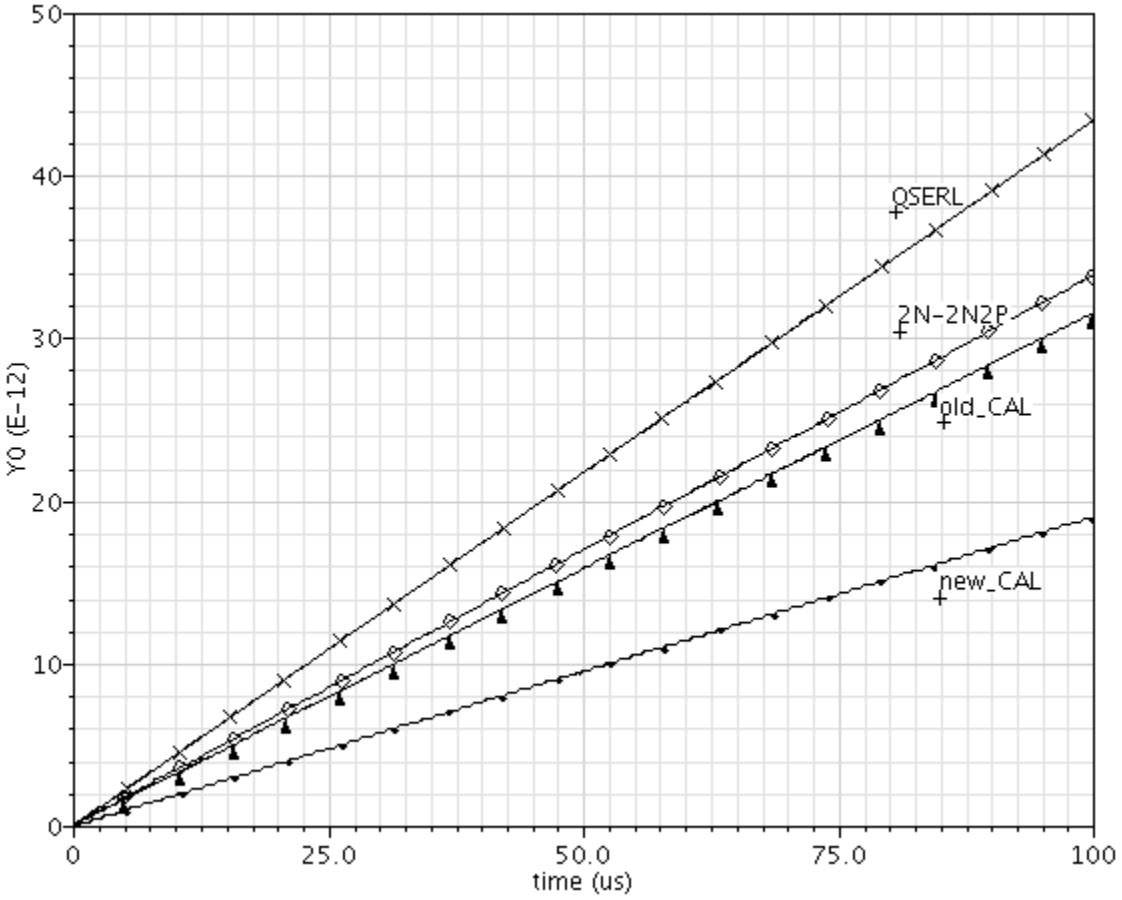



Figure 6.6: Simulated energy dissipation of different ERL XNOR/XOR gates.

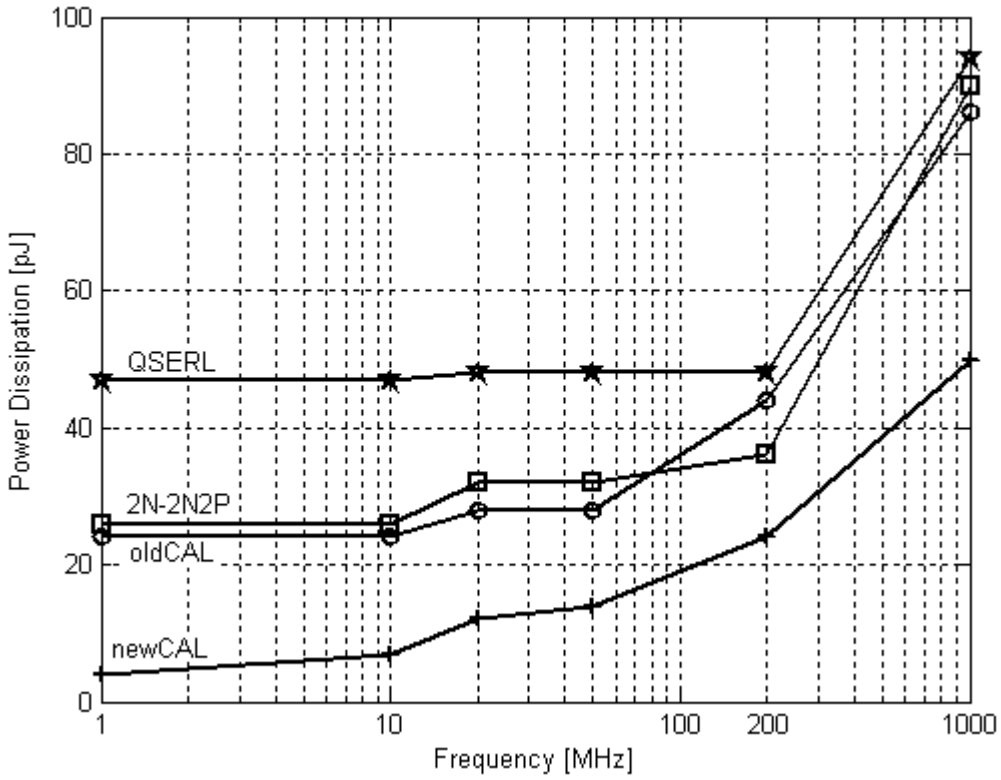



Figure 6.7: Simulated power dissipation versus frequency.

reducing the effectiveness of energy-recovery techniques [213] and is also observed in Fig. 6.7. In other word, the non-energy recovery loss increases and energy can no longer be efficiently recovered at high operating frequencies. The power dissipations rise beyond 200 MHz for all four energy recovery logic techniques. The new CAL XOR/XNOR gates consume less energy than the other three.

### 6.1.6 Experimental Results

Figure 6.8(a) shows the microphotograph of the fabricated chip in standard 0.5 μm n-well CMOS technology. The chip includes a CAL XNOR/NOR gate and three new CAL XNOR/NOR gates. Figure 6.8(b) shows experimental results on the fabricated chip. Comparison of simulation results in Fig. 6.5 with the experimental results in Fig. 6.8(b) shows that new CAL XNOR/XOR gates function properly.

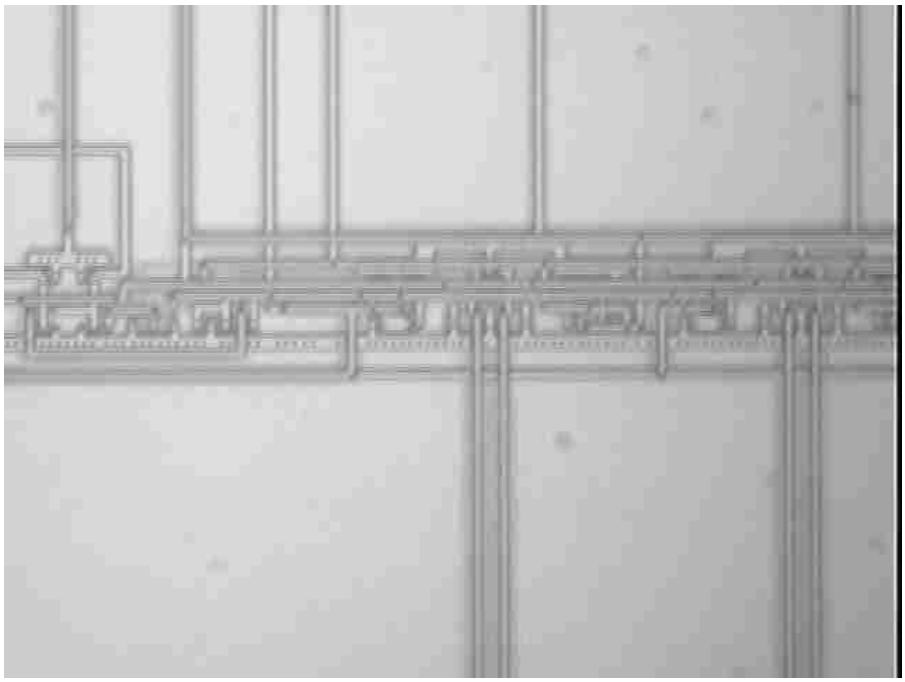
## 6.2 CNT-FET Energy Recovery Circuits

The power density on a chip, $P_D$ can be calculated as follows [213],

$$P_D = \frac{P}{\alpha A} \tag{6.1}$$

where P is the power consumed, A is the total transistor active area and α is the area factor that accounts for the chip area due to routing. We assumed α = 4 [213] in our simulations. Figure 6.9 shows that the power density of a CNT-FET inverter (described in Section 2.5) is higher than the limit of on-chip power density predicted by ITRS [1], especially at high frequency operation range. Therefore, to design CNT-FET integrated circuits, at high frequency operation range, low power designs, such as energy recovery techniques, are necessary to keep the power density lower than the limits predicted by ITRS 2003 [1].

The CMOS energy recovery circuits can be easily implemented using complementary CNT-FETs. For example, Fig. 6.10 shows the new CAL XNOR/XOR using complementary CNT-FETs. Figure 6.11 shows the simulation results of power densities of four types of CNT-FET ERL XNOR/XOR gates at different frequencies. It



(a)


(b)

Figure 6.8: (a) Microphotograph of CAL XNOR/XOR gates and (b) experimental results.

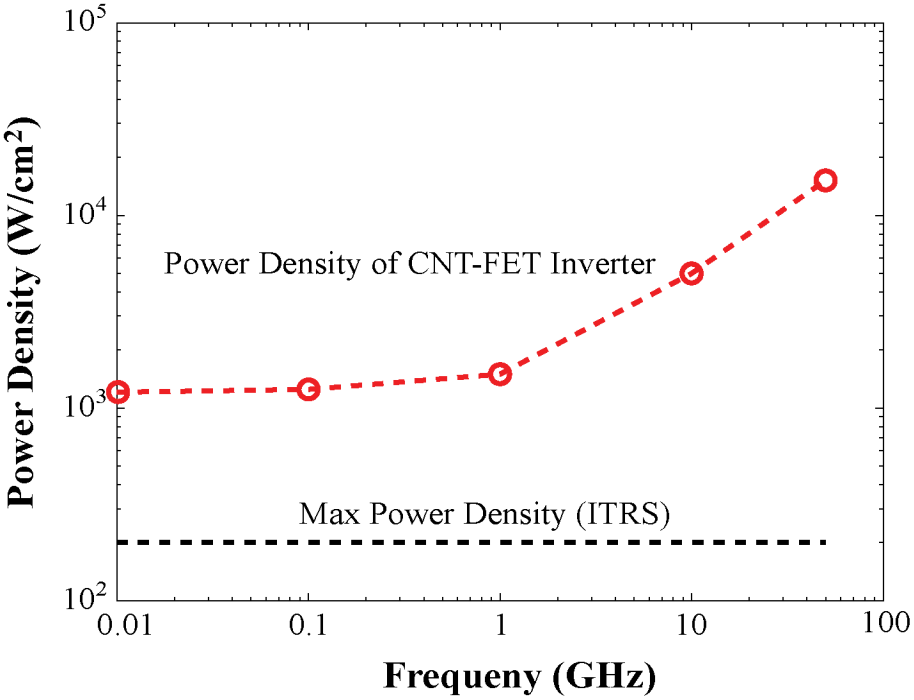



Figure 6.9: Average power density for a CNT-FET inverter. Note: The plot is obtained from Verilog-AMS in Cadence/Spectre.

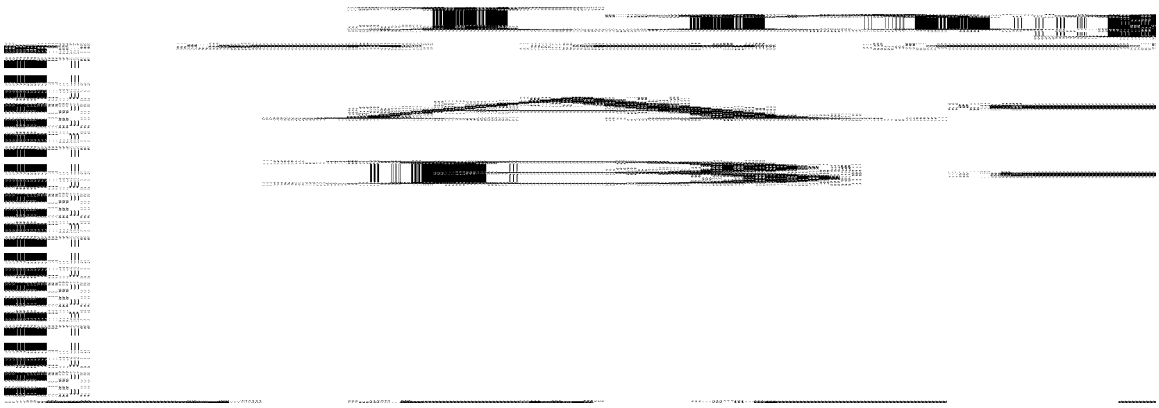


Figure 6.10: CNT-FET New CAL XNOR/XOR. Note: XOR(O/P) = $A\overline{B} + \overline{A}B$ and XNOR(O/P) = $AB + \overline{A}\ \overline{B}$.

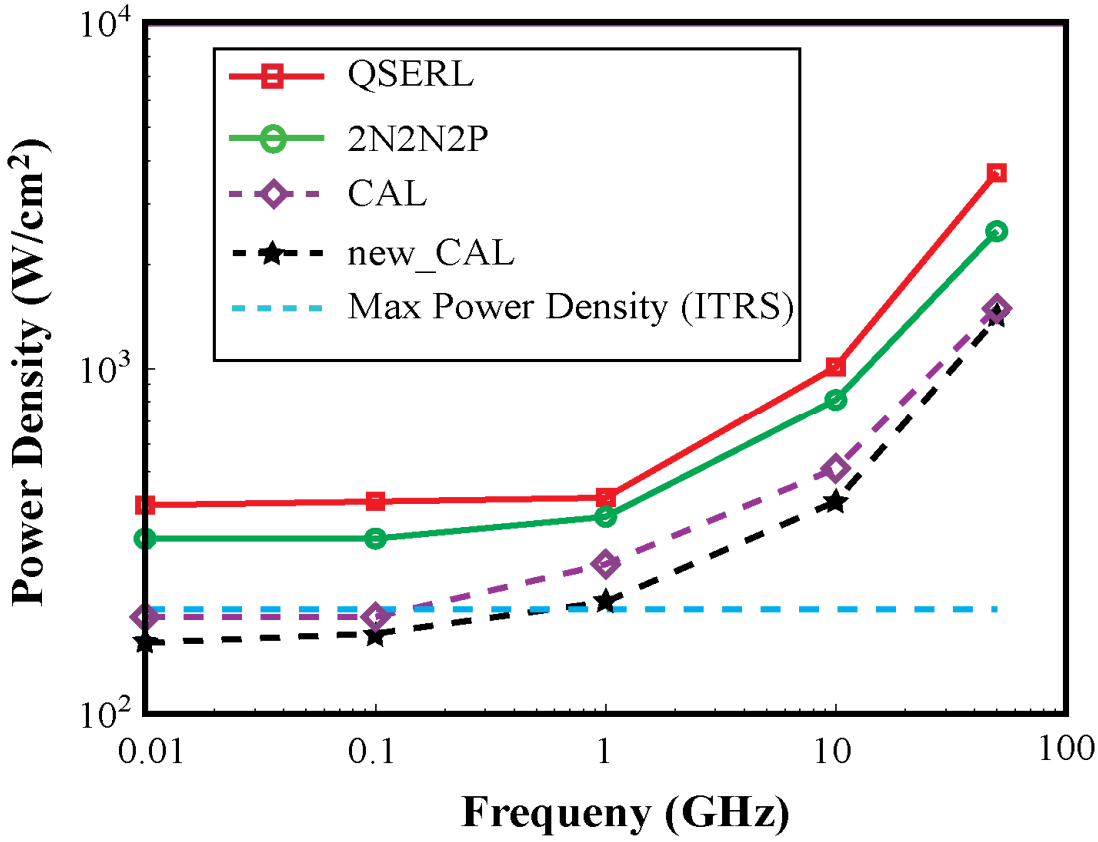



Figure 6.11: Average power density of different CNT-FET XNOR/XOR energy recovery circuits.

shows new CAL ERL has the least power density. However, the power densities of all energy recovery CNT-FET circuits exceed maximum power density limit over 1GHz.

## 6.3 Summary

In this chapter, we have introduced several CMOS energy recovery circuits and focused on XNOR/XOR gates. We have also introduced a new improved clocked diabatic logic (CAL) XNOR/XOR gates which consume significantly less power (30% less) compared to earlier ERL implementations.

Using our CNT-FET models, we have extended the study of CMOS energy recovery logic to CNT-FET energy recovery logic. The simulated behavior shows that the power density of CNT-FET circuits will exceed the maximum power density limit set by the ITRS 2003. Therefore, it is important to adopt circuit design techniques that would reduce on-chip power density for the future technology generations using CNT-FETs. Our simulations also show that energy recovery techniques help in reducing the power density of CNT-FET circuits below 1GHz. Beyond 1 GHz, further work is needed to reduce the on-chip power density. Energy recovery is, thus, can be used as an alternative approach toward circuit designs for reduction of high power density.

# CHAPTER 7*

# FAULT MODELING IN CNT BASED DIGITAL CIRCUITS

Significant amount of research has been conducted in fault modeling of digital CMOS circuits [222-228] due to manufacturing defects, ionizing radiations and single even upsets. Like CMOS digital integrated circuits, CNT-based integrated circuits are also prone to manufacturing defects and soft errors. Therefore, it becomes essential to develop fault models for fault-tolerant design of CNT-based circuits. With increased understanding of CNT-FETs circuits, research has also been conducted for optimal physical design of basic building blocks of CNT-FET based digital circuits [90] and fault modeling in CNT-FET circuits [90, 229].

## 7.1 CNT-FET Logic Gates

Chen et al. [44] have proposed a method of fabricating an inverter on a single carbon nanotube (CNT), as shown in Fig. 7.1 and based on which, they fabricated a ring oscillator [44]. In order to realize a CMOS type scheme on a single carbon nanotube, different work function metal gates, i.e. palladium (Pd) for the p-FET and aluminum (Al) for the n-FET were used [44]. In this work, we have extended the method of Chen et al. [44] to design an n-input NAND and NOR gates on a single CNT as shown in Fig. 7.2. In this design, metal wires can be replaced by metallic carbon nanotubes to achieve improved performance in terms of speed and power dissipation.

In Chapter 2, we have shown that CNT-FET exhibits I-V characteristics similar to CMOS transistors. The voltage transfer characteristics of the CNT-FET inverter are also similar to characteristics of the typical CMOS inverter. Like CMOS circuits, CNT-FET based circuits may also suffer from manufacturing defects. The manufacturing of CNTs is very challenging and CNTs are prone to certain defects unique to its fabrication. In this work, traditional fault modeling in CMOS digital circuits has been examined for possible applications in CNT-based digital circuits. Here, we extend the concept for fault modeling in CNT-based digital circuits.

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* Part of the work is reported in the following publication:

1. Y. Xu, A. Srivastava, and S. Rai, "Fault modeling in carbon nanotube based digital integrated circuits," *Proc. ASEE-Gulf Southwest Conference*, Lake Charles, Louisiana, USA, pp. 1-7, March 24-26, 2010.

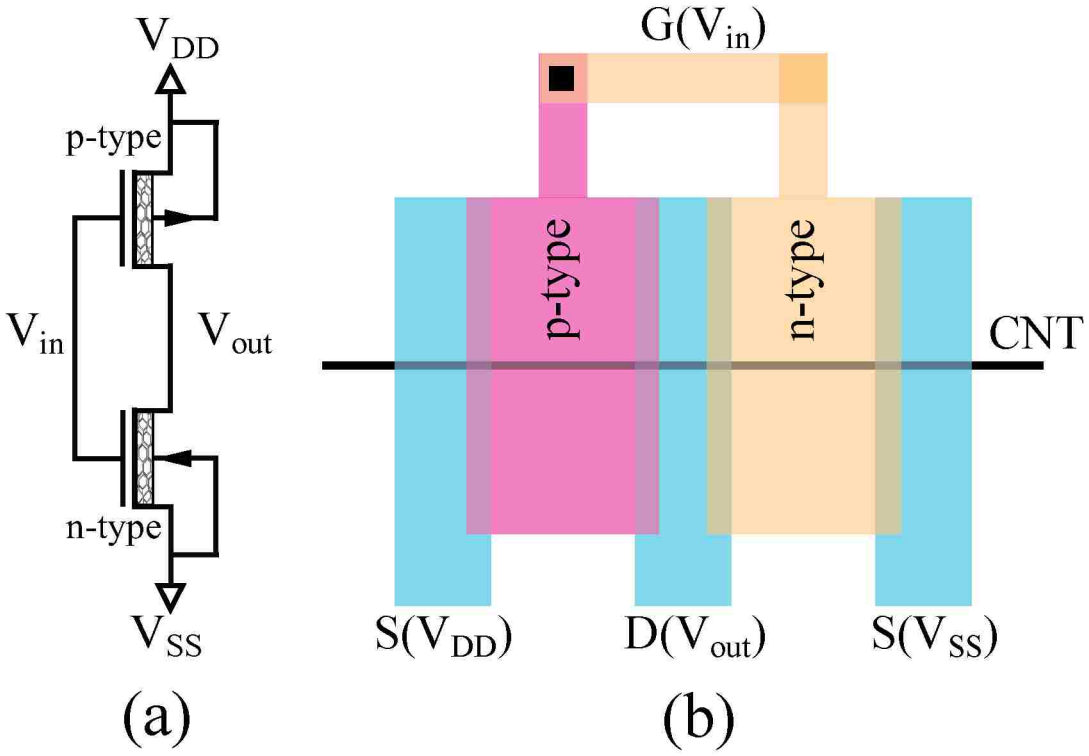


Figure 7.1: (a) CNT-FET inverter and (b) of CNT-FET inverter layout [44].

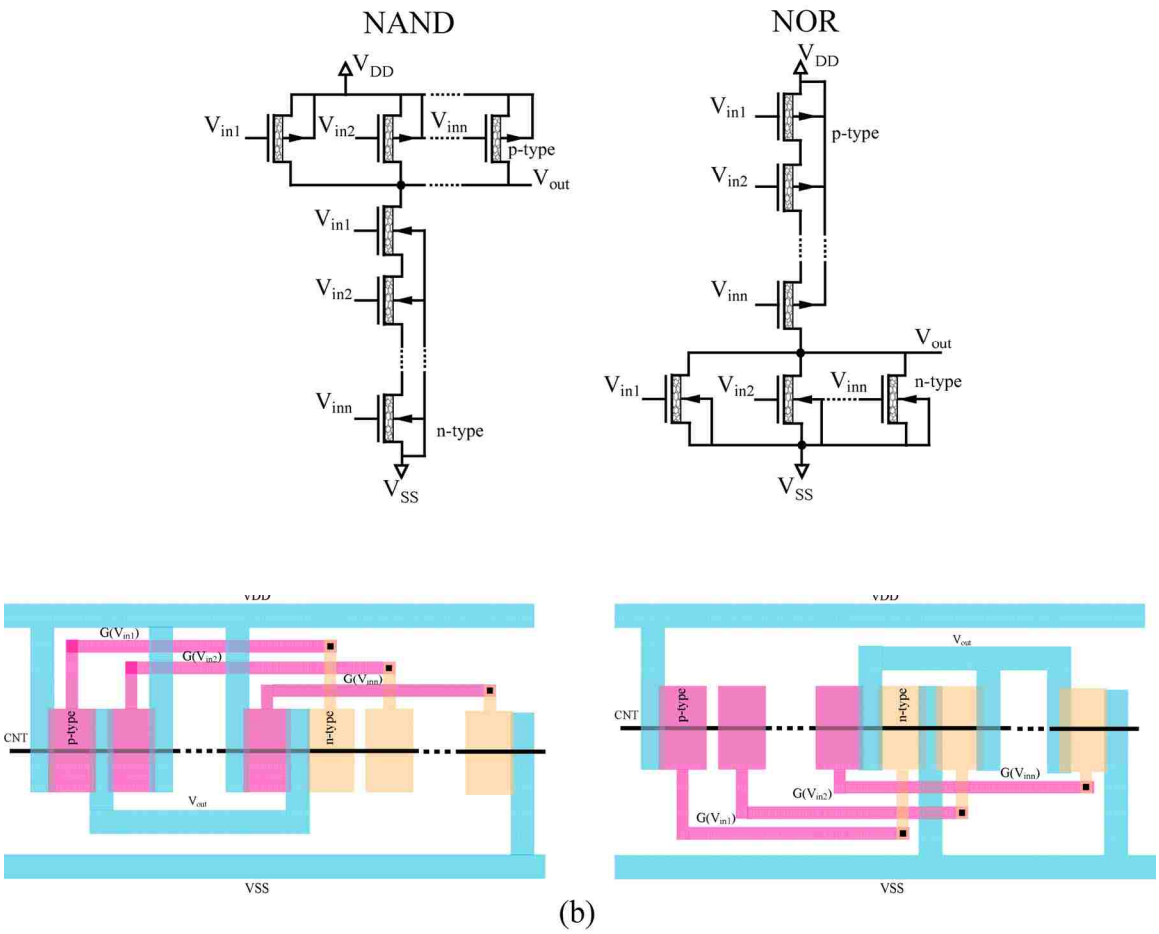


Figure 7.2: (a) CNT-FET NAND and NOR gates and (b) of CNT-FET NAND and NOR gates layouts.

## 7.2 Fault Models

In the following, we describe three basic fault models, stuck-at fault, stuck-open and stuck-on fault models, which we have applied in CNT-FET digital circuits.

### 7.2.1 Stuck-At Fault Model

In stuck-at fault model, the line is permanently at logic 0 (stuck-at 0) or 1 (stuck-at 1) [230]. For CMOS gates, this fault model can detect manufacturing defects, such as the metallization shorts. CNT-FET gates may also suffer this fault due to the metal wire or metallic CNT shorts as shown in Fig. 7.3 by the dotted lines. Single stuck-at fault (SSF) is the most common fault in the stuck-at faults. Figure 7.4 shows the Cadence/Spectre simulation results of a 2-input CNT-FET NAND gate with and without single stuck-at faults. The fault-free output is denoted as Out whereas the outputs in the presence of shorts $S_1$ and $S_2$ are denoted as Out1 and Out2, respectively. As in CMOS gate, the vector ($V_{in1}$,$V_{in2}$) = (1, 1) detects short $S_1$ and vector ($V_{in1}$,$V_{in2}$) = (0, 1) detects short $S_2$.

### 7.2.2 Stuck-Open Fault Model

Stuck-open means a transistor is rendered non-conducting by a fault. In CMOS gates [230], the most common case is one of the transistors in the gate suffering this fault and in CNT-FET gates, this corresponds to the situation that the CNT is broken at a point, shown in Fig. 7.3. Therefore, it requires a two-pattern test to detect this stuck-open fault. Figure 7.5 shows the simulation results of a 2-input CNT-FET NAND gate with and without stuck-open faults. The fault-free output is denoted as Out whereas the outputs in the presence of open $O_1$ is denoted as Out1. As in CMOS NAND gate, the two-pattern test for the stuck-open fault shown in Figures 7.3 and 7.5 is <1 1, 1 0>.

If the metals are replaced by metallic CNTs in the CNT-FET gate, there is likely to be another possible fault because nearly 1/3 of CNTs are metallic after fabrication [6, 192]. As a result, one of the wires will be stuck-open if CNT is not conducting.

### 7.2.3 Stuck-On Fault Model

Stuck-on means a transistor is rendered continuously conducting by a fault [16].

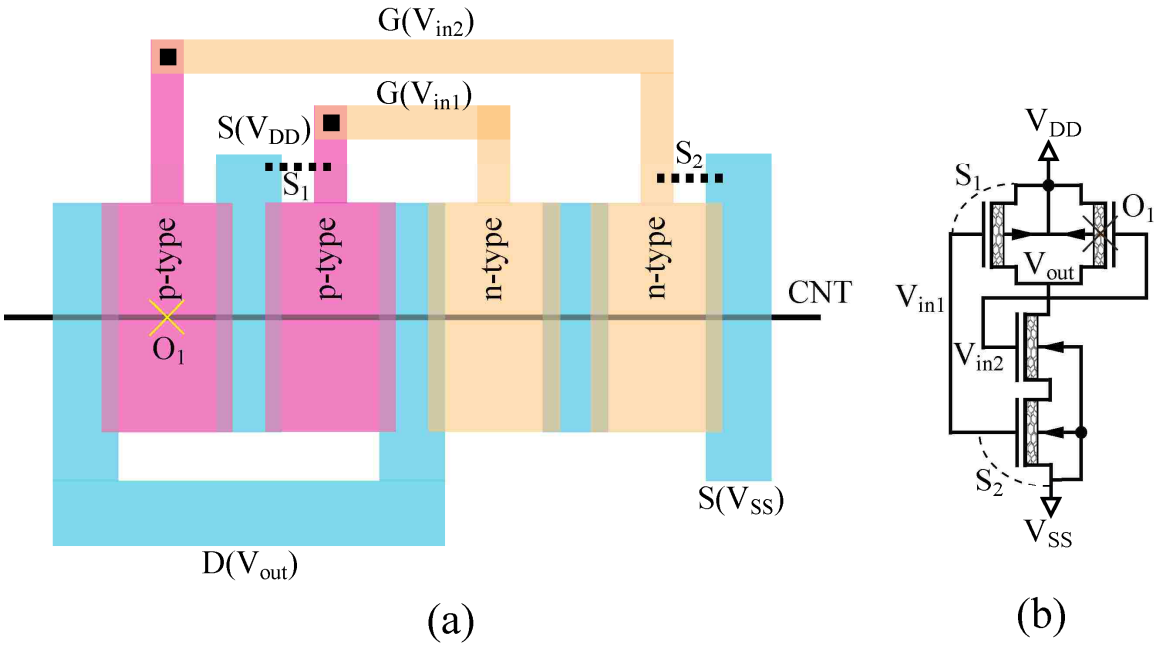


Figure 7.3: (a) Physical layout showing shorts in a CNT-FET NAND gate with stuck-at faults (dotted lines) and (b) open faults shown by X in the circuit.

The number of transistors that experience stuck-on fault varies in CMOS logic gates, while it may be different for CNT-FET logic gates since not all the CNTs are metallic after fabrication [6, 192]. Hashempour et al. [90] have studied defects in metallic CNT based on line-of-diffusion style layout of CNT-FET gates, which utilize two CNTs and concluded that the metallic CNT defects result in stuck-at-1(0) at the output. However, metallic CNT defects result in different output for the logic gates built on a single CNT. If single CNT is metallic, all the CNT-FETs fabricated on it will be stuck-on, which means the supply and ground will be connected and the output is indeterminate. As a result, inputs of the gate have little effect on the output. The current monitoring is the suitable technique to detect this type of fault.

## 7.3 Summary

In this chapter, stuck-at fault, stuck-on fault and stuck-open fault models have been used in fault modeling behavior of CNT-FET inverter and NAND gates and simulated in Cadence/Spectre. Simulation results show that CNT-FET gates exhibits faulty behavior similar to traditional CMOS gates with stuck-at fault and stuck-on fault. CNT-FET gates also have some unique faults such as the metallic CNT faults, which result in CNT-FETs stuck-on and the output of the gate indeterminate.

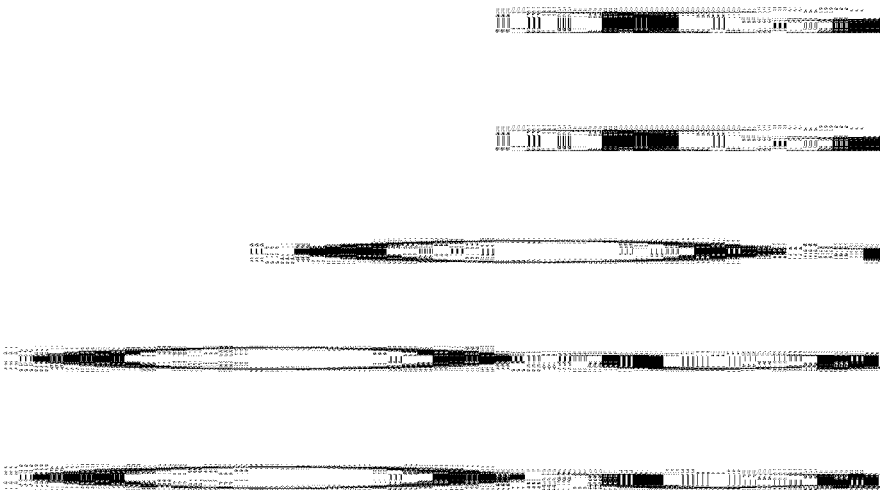

Figure 7.4: Transient simulations of a 2-input CNT-FET NAND gate with and without stuck-at faults.

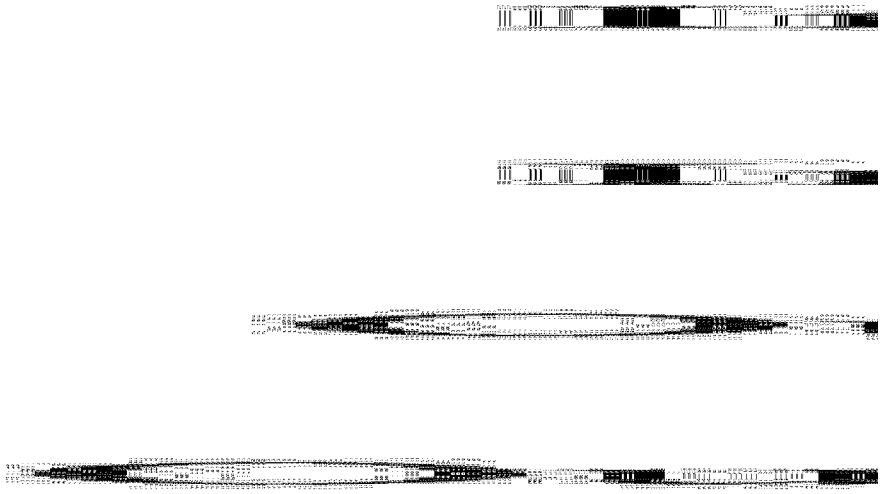

Figure 7.5: Transient simulations of a 2-input CNT-FET NAND gate with and without stuck-open faults.

# CHAPTER 8

# CONCLUSION AND SCOPE OF FUTURE WORK

## 8.1 Conclusion

In this research, model equations for surface potentials for non-ballistic and ballistic CNT-FETs are presented. The current transport equations for non-ballistic CNT-FETs are summarized, which were derived in one of our earlier work [91]. Based on these equations, dynamic model equations for linear and saturation regions of operation of CNT-FETs are derived. The current transport equations for ballistic CNT-FETs are also described. The modeled I-V characterizations are in agreement with the experimental results and the model proposed by Akinwande et al. [116]. By using the static and dynamic models for non-ballistic CNT-FETs, we have studied performances of some basic CNT-FETs circuits such as the inverter and ring oscillator. The simulation results of ring oscillator frequencies are fairly close to the experimental data.

We have proposed a simple method to develop a transmission line model for metallic carbon nanotube (CNT) interconnects using classical electrodynamics. The effective conducting electrons in carbon nanotubes are modeled as one-dimensional fluid considering electron-electron repulsive interactions. This method provides an equivalent circuit for analyzing the SWCNT interconnect as a transmission line. Damping effect is observed in SWCNTs due to its high resistance. It is observed in SWCNTs below 1 MHz for lengths less than 1 μm, and above 100 MHz for length longer than 100 μm. Thus, short length SWCNTs (< 1 μm) can be used above 1 MHz. Damping thus limits the usable frequency bandwidth since it is dependent on the length. Calculations of group delays show that CNT interconnects can also be used above 200 GHz for short interconnects (< 1 μm) and 10 GHz for long interconnect (> 100 μm). Study of S-parameters suggests consideration of impedance matching at the input and output to minimize losses due to reflections for longer SWCNT interconnects.

Models for CNT interconnects, which include MWCNT and SWCNT bundle are discussed based on one-dimensional fluid theory. The one-dimensional fluid model can be applied to CNT interconnects using low resistance contacts in current low-voltage

nanometer CMOS technologies. The applicability of MWCNT and SWCNT bundle as interconnect wires for next generation design of integrated circuits has been explored theoretically and compared with Cu interconnects in 22 nm technology node. Results of the one-dimensional fluid theory for SWCNT interconnect extended to MWCNT and SWCNT bundle interconnects show that MWCNT and SWCNT bundle interconnects have better performance than the Cu interconnects. MWCNT and SWCNT bundle interconnects exhibit higher transmission efficiency and lower reflection losses and less power dissipations. This is mainly due to larger conductivity of MWCNT and SWCNT bundle, proportional to the number of conducting shells (M) in MWCNT and conducting SWCNTs (N) in the bundle, respectively. With no special separation techniques, the metallic nanotubes are distributed with probability $\beta = 1/3$. While the proportion of metallic nanotubes can be potentially increased using techniques introduced by Peng et al. [193] and Zheng et al. [194], the delays in MWCNT and SWCNT bundle interconnects can be further decreased with increase in $\beta$ and approaching to 1. It is also noticed that with the increase in interconnection length, the delay of Cu interconnect increases faster than that of MWCNT and SWCNT bundle interconnects. For applications requiring small circuit delays MWCNT interconnects should be used due to smaller capacitances. Applications requiring large transmission efficiency and low reflection losses, CNT bundles should be used for interconnects since the numbers of conducting channels per shell are more in SWCNTs bundle than the number of conducting channels per shell in MWCNT of the same size. These findings suggest that MWCNT and SWCNT bundle can replace Cu as interconnection wires in next generation of VLSI integrated circuits.

We have utilized our MWCNT and SWCNT bundle interconnects model in a widely used $\pi$ model to study the performances of MWCNT and SWCNT bundle wire inductors and compared them with Cu inductors. The calculation results show that the Q factors of CNT wire (bundle and MWCNT) inductors are higher than that of the Cu wire inductor. This is mainly due to much lower resistance of CNT and negligible skin effect in carbon nanotubes at higher frequencies. The application of CNT wire inductor in CMOS LC VCO is also studied and the Cadence/Spectre simulations show that VCOs with CNT bundle wire inductors have significantly improved performance such as the

higher oscillation frequency, lower phase noise, due to their smaller resistances and higher Q factors. It is also noticed that LC VCO using SWCNT bundle wire inductor has better performance when compared with the performance of LC VCO using MWCNT wire inductor due to its lower resistance and higher Q factor.

We have introduced several CMOS energy recovery circuits and focused on XNOR/XOR gates. We have also introduced a new improved clocked adiabatic logic (CAL) XNOR/XOR gates which consume significantly less power compared to earlier ERL implementations.

Using our CNT-FET models, we have extended the study of CMOS energy recovery logic to CNT-FET energy recovery logic. Our results show that the power density of CNT-FET circuits will exceed the maximum power density limit set by the ITRS 2003. Therefore, it is important to adopt circuit design techniques that would reduce on-chip power density for the future technology generations using CNT-FETs. Our simulations also show that energy recovery techniques help in reducing the power density of CNT-FET circuits below 1 GHz. Beyond 1 GHz, further work is needed to reduce the on-chip power density. Energy recovery is, thus, can be used as an alternative approach toward circuit designs for reduction of high power density.

Stuck-at fault, stuck-on fault and stuck-open fault models have been used in fault modeling behavior of CNT-FET NAND gate and simulated in Cadence/Spectre. Simulation results show that CNT-FET gates exhibits faulty behavior similar to traditional CMOS gates with stuck-at fault and stuck-on fault. CNT-FET gates also have some unique faults such as the metallic CNT faults, which result in CNT-FETs stuck-on and the output of the gate indeterminate.

## 8.2 Scope of Future Work

We have built static model for ballistic CNT-FETs. However, to study the behavior of ballistic CNT-FET circuits, dynamic model of CNT-FET is also needed. Two approaches can be considered: Mayer model or charge-based approach [114]. This dynamic model then can be coupled with present static model and interconnection models

for analysis and design of all ballistic CNT-FET based analog and digital integrated circuits.

Carbon nanotube graphite cylinders are composed of surface atoms. Because of their size, large surface area and hollow geometrical shape, carbon nanotubes are the best-suited materials for gas absorption, storage and molecular filtering [231]. Carbon nanotube exhibits significant changes in its electronic properties when subjected to molecular adsorbates. The unique structure and sensitivity to molecular adsorbates have resulted in use of carbon nanotubes for bio- and chemical sensing applications. Both conductance and capacitance based CNT-sensors have been developed for detecting traces of a wide range of chemical vapors and gases including traces of nerve agents and explosives [129-133]. In our recent work [216], we have studied the application of CNT based circuits in bio- and chemical sensing (described in Appendix B). Experimental CNT based bio- and chemical sensors can be designed and developed based on the current research.

Although we have compared our models of CNT interconnects with other proposed models experiments are needed to verify the models. We suggest a method of characterization of multi-walled carbon nanotubes (MWCNTs) as interconnects based on the method developed by Close et al. [198-200] using commercially available MWCNTs with an average length ~ 5 μm and diameter ~ 70 nm. The method is described in Appendix C. Also more work is needed on carbon nanotube wire inductors and fabrication. New energy recovery techniques are to be developed to reduce the power density of CNT-FET circuit in GHz operation and above. Reliability issue also needs to be considered since faults are likely to be present in the CNT based circuits.

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# APPENDIX A

# VERILOG-AMS CODES FOR NONBALLISTIC CNT-FET MODELING

Verilog-AMS code for n-type CNT-FET

```
// VerilogA for CNTFET, nFET, veriloga

`include "constants.vams"
`include "disciplines.vams"


// Physical Constants
`define pi 3.1416
`define h 4.1357e-015    // planks constant
`define hb 6.5821e-16    // modified plank constant
`define q 1.602e-19      // Charge
`define epo 8.86e-12     // Permittivity of free space
`define kb 1.38e-23      // Boltzmann Constant
`define K 8.612e-5       // Boltzmann Constant
`define ac 1.43       // C-C Bond Length
`define a 2.48        // lattice constant in angstroms
`define Vpi 2.97      // C-C Bond energy
`define gamma 0.5
`define Vpp 2.51
`define vf  8.1e15
`define eo 8.85e-22
`define Depth 2


module nFET(b, d, s, g);
inout b;
electrical b;
inout d;
electrical d;
inout s;
electrical s;
input g;
electrical g;

//Instance Parameters
parameter real Tox1 = 15e-9;     // oxide layer 1 thickness in meter
parameter real Tox2 = 120e-9;       // oxide layer 2 thickness in meter
parameter real T = 300;          // temperature in K
parameter real L = 250e-9;       // length of CNT in meter
parameter real Integral=4.1124;     // intergral parameter
parameter real er1 = 3.9;    // permitivity of oxide layer 1
parameter real er2 = 3.9;    // permitivity of oxide layer 2
parameter real Ecrit = 0.2627;
parameter real Vms = 0;          // in volts
parameter real n =11;
parameter real m = 9;
parameter real Q01 = 0;
```

```
parameter real Q02 = 0;

// Variables

real Vgs,Vds,Vbs,Vgb,Vsb,Vdb; // External voltages
real Cgs,Cgd,Csb,Cdb,Cgb;       //Capacitance
real Ids;
real a1x, a2x,a1y, a2y;      //Lattice Definition in angstroms
real L_R;          //length of R vector in angstroms
real r;            //Radius in Angstroms
real VcbSat;
real VcbMod;
real Nc;
real Ces1;
real Ces2;
real Delta;
real vfb;
real Beta;
real Slope;
real vth;
real VcntL;
real Vcnt0;
real KT;           // in eV
real length;          // length of CNT in angstrums
real Ids_temp;
real Efs;
real Efd;
real Emin;

analog begin

Vgs=V(g)-V(s);
Vds=V(d)-V(s);    //
Vgb=V(g)-V(b);
Vsb=V(s)-V(b);
Vdb=V(d)-V(b);

Vgs=Vgs+0.5;

Emin=1;
length=L*1e10;        //converted to angstroms

KT=$vt;            // unit
a2x=a1x=`a*sqrt(3)/2;    //x of a1 and a2 in angstroms
a1y=`a/2;          //y of a1 in angstroms
a2y=-`a/2;         //y of a2 in angstroms
L_R=sqrt(pow(n*a1x+m*a2x,2)+pow(n*a1y+m*a2y,2));      //find L_R in
angstroms

r = L_R/`pi/2;        //Radius in Angstroms


Nc = 4*KT/(`pi*sqrt(3)*`Vpp*`a)*(1e8);  //in 1/cm
Ces1 =`pi*2*er1*`eo*length/ln(
(Tox1*1e10+r+sqrt(Tox1*Tox1*1e20+2*Tox1*1e10*r))/r); // Capacitance in
Faradays
```

```
Ces2 =`pi*2*er2*`eo*length/ln(
(Tox2*1e10+r+sqrt(Tox2*Tox2*1e20+2*Tox2*1e10*r))/r);  // Capacitance in
Faradays
Delta = `q*length*(1e-8)*Nc/Ces1;                     // in volts
vfb = Vms - Q01/Ces1 - Q02/Ces2 - Q02/Ces1;           // in volts
Beta = 0.12*1e3*Ces1/pow(length*(1e-8),2);
Slope = 0.5*( sqrt(2*Ecrit/KT + 1) - Integral*exp(-`Depth) )/KT;
vth = vfb + Ecrit - `Depth*KT - Integral*exp(-`Depth)/Slope;


//Getting Vcnt0 and VcntL

Slope = 0.5*( sqrt(2*Ecrit*`Depth/KT + `Depth) - Integral*exp(-`Depth)
)/KT;
VcbSat = Vgs +Vsb - vfb - Ecrit + `Depth*KT + Integral/Slope*exp(-
`Depth);
//VcbMod = Vgb - Ecrit - vfb - Depth*KT -
(Delta/KT)*sqrt(2*Ecrit*Depth*KT+power((Depth*KT),2));

if(Vds+Vsb >= VcbSat) begin
    VcntL = Vgs + Vsb - vfb;
end
else begin
    VcntL = (Vgs +Vsb - Delta*Integral*exp(-`Depth) - vfb +
Delta*Slope*(Vds+Vsb + Ecrit - `Depth*KT) )/(1 + Delta*Slope);
end

Efs=VcntL-Vsb;
Efd=VcntL-Vds-Vsb;

Csb=8e-18;
Cdb=8e-18;
Cgb=8e-18;

if(Vgs >= vth) begin     //saturation region
    Cgs=8e-18;
    Cgd=0;
end
else begin        //linear region
    Cgs=8e-18;
    Cgd=7e-18;
end

if(Vgs >= vth) begin         //saturation region
    if(Vsb >= VcbSat)
           Vcnt0 = Vgs +Vsb - vfb;
    else
           Vcnt0 = (Vgs +Vsb - Delta*Integral*exp(-`Depth) - vfb +
Delta*Slope*(Vsb + Ecrit - `Depth*KT) )/(1 + Delta*Slope);

    Ids=((Vgs +Vsb-vfb+KT)*VcntL - 0.5*VcntL*VcntL-(Vgs +Vsb-
vfb+KT)*Vcnt0 + 0.5*Vcnt0*Vcnt0)*Beta;  //Amps
end
else begin //linear region
    Vcnt0 = Vgs + Vsb - vfb;
    Ids = `q*KT/`pi/`hb*( (ln(1+exp(Efs/KT-Emin/KT))) -
```

```
(ln(1+exp(Efd/KT-Emin/KT))) );
end

//current
I(d,s) <+ Ids*1;

//Cap
I(g,s) <+ ddt(Cgs*V(g,s));
//I(s,g) <+ ddt(Cgs*V(g,s));
I(g,d) <+ ddt(Cgd*V(g,d));
//I(d,g) <+ ddt(Cgd*V(g,d));
I(s,b) <+ ddt(Csb*V(s,b));
I(d,b) <+ ddt(Cdb*V(s,b));
//I(g,b) <+ ddt(Cgb*V(g,b));

end //analog
endmodule
```

Verilog-AMS code for p-type CNT-FET

```
// VerilogA for CNTFET, pFET, veriloga

`include "constants.vams"
`include "disciplines.vams"


// Physical Constants
`define pi 3.1416
`define h 4.1357e-015    // planks constant
`define hb 6.5821e-16    // modified plank constant
`define q 1.602e-19      // Charge
`define epo 8.86e-12     // Permittivity of free space
`define kb 1.38e-23      // Boltzmann Constant
`define K 8.612e-5       // Boltzmann Constant
`define ac 1.43       // C-C Bond Length
`define a 2.48        // lattice constant in angstroms
`define Vpi 2.97      // C-C Bond energy
`define gamma 0.5
`define Vpp 2.51
`define vf  8.1e15
`define eo 8.85e-22
`define Depth 2

module pFET(b, d, s, g);
inout b;
electrical b;
inout d;
electrical d;
inout s;
electrical s;
input g;
electrical g;
```

```
//Instance Parameters
parameter real Tox1 = 15e-9;     // oxide layer 1 thickness in meter
parameter real Tox2 = 120e-9;       // oxide layer 2 thickness in meter
parameter real T = 300;          // temperature in K
parameter real L = 250e-9;       // length of CNT in meter
parameter real Integral=4.1124;     // intergral parameter
parameter real er1 = 3.9;    // permitivity of oxide layer 1
parameter real er2 = 3.9;    // permitivity of oxide layer 2
parameter real Ecrit = 0.2627;
parameter real Vms = 0;          // in volts
parameter real n =11;
parameter real m = 9;
parameter real Q01 = 0;
parameter real Q02 = 0;

// Variables

real Vsg,Vsd,Vbg,Vbs,Vbd; // External voltages
real Ids;
real Cgs,Cgd,Csb,Cdb,Cgb;        //Capacitance
real a1x, a2x,a1y, a2y;      //Lattice Definition in angstroms
real L_R;          //length of R vector in angstroms
real r;            //Radius in Angstroms
real VcbSat;
real VcbMod;
real Nc;
real Ces1;
real Ces2;
real Delta;
real vfb;
real Beta;
real Slope;
real vth;
real VcntL;
real Vcnt0;
real KT;           // in eV
real length;          // length of CNT in angstrums
real Ids_temp;
real Efs;
real Efd;
real Emin;

analog begin

Vsg=V(s)-V(g);
Vsd=V(s)-V(d);    //
Vbs=V(b)-V(s);
Vbg=V(b)-V(g);
Vbd=V(b)-V(d);

Vsg=Vsg+0.5;
Emin=1;
length=L*1e10;        //converted to angstroms

KT=$vt;           // unit
a2x=a1x=`a*sqrt(3)/2;    //x of a1 and a2 in angstroms
```

```
a1y=`a/2;          //y of a1 in angstroms
a2y=-`a/2;         //y of a2 in angstroms

L_R=sqrt(pow(n*a1x+m*a2x,2)+pow(n*a1y+m*a2y,2));      //find L_R in
angstroms

r = L_R/`pi/2;         //Radius in Angstroms


Nc = 4*KT/(`pi*sqrt(3)*`Vpp*`a)*(1e8);  //in 1/cm
Ces1 =`pi*2*er1*`eo*length/ln(
(Tox1*1e10+r+sqrt(Tox1*Tox1*1e20+2*Tox1*1e10*r))/r); // Capacitance in
Faradays
Ces2 =`pi*2*er2*`eo*length/ln(
(Tox2*1e10+r+sqrt(Tox2*Tox2*1e20+2*Tox2*1e10*r))/r);  // Capacitance in
Faradays
Delta = `q*length*(1e-8)*Nc/Ces1;                     // in volts
vfb = Vms - Q01/Ces1 - Q02/Ces2 - Q02/Ces1;           // in volts
Beta = 0.12*1e3*Ces1/pow(length*(1e-8),2);
Slope = 0.5*( sqrt(2*Ecrit/KT + 1) - Integral*exp(-`Depth) )/KT;
vth = vfb + Ecrit - `Depth*KT - Integral*exp(-`Depth)/Slope;


//Getting Vcnt0 and VcntL

Slope = 0.5*( sqrt(2*Ecrit*`Depth/KT + `Depth) - Integral*exp(-`Depth)
)/KT;
VcbSat = Vsg +Vbs - vfb - Ecrit + `Depth*KT + Integral/Slope*exp(-
`Depth);
//VcbMod = Vbg - Ecrit - vfb - Depth*KT -
(Delta/KT)*sqrt(2*Ecrit*Depth*KT+power((Depth*KT),2));
if(Vsd+Vbs >= VcbSat) begin
    VcntL = Vsg + Vbs - vfb;
end
else begin
    VcntL = (Vsg +Vbs - Delta*Integral*exp(-`Depth) - vfb +
Delta*Slope*(Vsd+Vbs + Ecrit - `Depth*KT) )/(1 + Delta*Slope);
end

Efs=VcntL-Vbs;
Efd=VcntL-Vsd-Vbs;

Csb=8e-18;
Cdb=8e-18;
Cgb=8e-18;

if(Vsg >= vth) begin     //saturation region
    Cgs=8e-18;
    Cgd=0;
end
else begin        //linear region
    Cgs=8e-18;
    Cgd=7e-18;
end

if(Vsg >= vth) begin         //saturation region
```

```
    if(Vbs >= VcbSat)
            Vcnt0 = Vsg +Vbs - vfb;
    else
            Vcnt0 = (Vsg +Vbs - Delta*Integral*exp(-`Depth) - vfb +
Delta*Slope*(Vbs + Ecrit - `Depth*KT) )/(1 + Delta*Slope);

    Ids=-((Vsg +Vbs-vfb+KT)*VcntL - 0.5*VcntL*VcntL-(Vsg +Vbs-
vfb+KT)*Vcnt0 + 0.5*Vcnt0*Vcnt0)*Beta;  //Amps
end
else begin //linear region
    Vcnt0 = Vsg + Vbs - vfb;
    Ids = -`q*KT/`pi/`hb*( (ln(1+exp(Efs/KT-Emin/KT))) +
(ln(1+exp(Efd/KT-Emin/KT))) );
end

//current
I(d,s) <+ Ids*1;

//Cap
//I(g,s) <+ ddt(Cgs*V(g,s));
I(s,g) <+ ddt(Cgs*V(s,g));
//I(g,d) <+ ddt(Cgd*V(g,d));
I(d,g) <+ ddt(Cgd*V(d,g));
I(b,s) <+ ddt(Csb*V(s,b));
I(b,d) <+ ddt(Cdb*V(s,b));
//I(b,g) <+ ddt(Cgb*V(b,g));

end //analog
endmodule
```

# APPENDIX B

# CARBON NANOTUBE FOR BIO- AND CHEMICAL SENSING

Lee, et al. [232] have shown that conductance of a metallic CNT can increase to 50% with 10 ppm thionyl chloride ($SOCl_2$) adsorption. We can use this electronic behavior to use an inverter pair, interconnected by a metallic SWCNT interconnect wire to detect traces of $SOCl_2$ by comparing the transient behavior before and after $SOCl_2$ adsorption. Figure B.1 shows the signal response of an inverter pair interconnected by a 100 μm long metallic CNT wire before and after $SOCl_2$ adsorption. The average delay is ~10 ns

Kong, et al. [233] and Collins, et al. [231] have demonstrated change in conductance of p-type CNT to certain molecular adsorbates such as the $NH_3$, an electron donor and the $NO_2$, an electron acceptor, resulting in decrease and increase in conductance. Tang et al. [234] have shown that the current in CNT-FETs fabricated from semiconducting CNTs can be increased up to 20% with DNA adsorption. DNA can also be detected by using a ring oscillator circuit whose frequency is current flow dependent. Figure B.2 shows the dependence of 5-stage CNT-FET ring oscillator (RO) frequency dependence on supply voltage, $V_{DD}$. Dashed line in Fig. B.2 shows the change in RO frequency with change in current flow calibrated for DNA detection through CNT-FETs [234].

These simulations based on our models show that CNT-FET circuits are promising for bio- and chemical sensing at molecular levels.

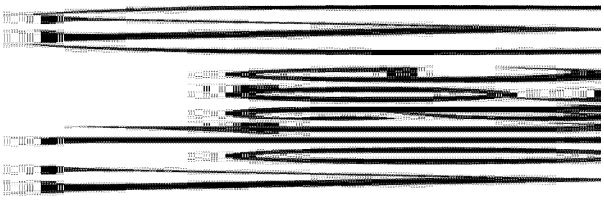

Figure B.1: Transient behavior of an inverter pair inter-connected by 100μm CNT wire length before and after $SOCl_2$ adsorption.

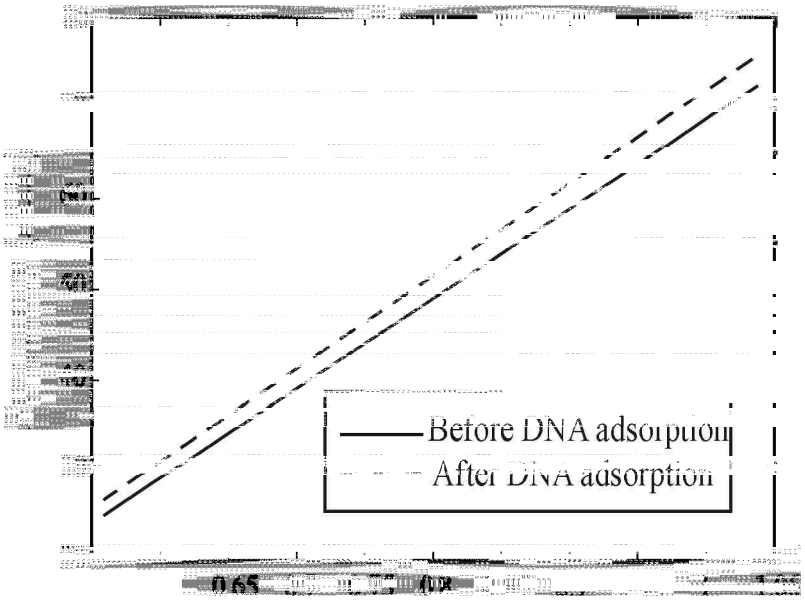


Figure B.2: RO frequency dependence on supply voltage, $V_{DD}$. The dimensions of both the n-type and p-type CNT-FETs are: d = 2 nm and L = 600 nm.

# APPENDIX C

# EXPERIMENTAL CHARACTERIZATION OF CNT INTERCONNECTS

Figure C.1 shows the process to assemble an array of carbon nanotube for interconnects; MWCNT in the present work, for experimental characterization as described by Close et al. [198-200].

Initially an array of gaps is patterned in between gold electrodes. The MWCNTs are dispersed in ethanol. An alternating electric field is then applied to assemble and precisely position the MWCNTs in the gap between the gold electrodes using the dielectrophoresis process. The MWCNTs are then secured in place by metal clamps deposited at both ends of the MWCNTs. Vias are etched through the passivation layer to reveal the topmost aluminum metal layer in the CMOS chip. The vias are finally filled with titanium, thereby establishing electrical connections between the underlying silicon CMOS transistors and the MWCNT interconnects. The post-processed chip is wire bonded to a pin grid array package and mounted onto a printed circuit board for electrical testing.

In the past, our group made attempts to separate single-walled carbon nanotubes (SWCNT) from commercial CNT powder and aligned over a wide gap on silicon to from a cantilever [235]. In this work, we plan to continue our earlier work and that of Close et al. [198-200] to align MWCNTs on silicon and conduct experimental studies for their interconnect behavior based on our developed electrical modeling theory [158, 187]. The method described here has been designed based on the experimental facilities of the LSU Center for Advanced Microstructures and Devices (CAMD). Figure C.2 shows a top-view of the final structure using carbon nanotubes. The substrate is a 4-inch silicon wafer. Three optical lithography steps are required to assemble the CNT interconnect structure. The process flow is as follows.

Step 1: We pattern an array of 5-11 μm gaps in between two dielectrophoresis electrodes (thickness: 25 nm Cr /75 nm Au) by sputtering and metal etching techniques. A droplet of the prepared CNT solution (commercial MWCNTs grown by CVD, available in powder form from Helix Materials and ultra-sonicated in ethanol for 30 min),

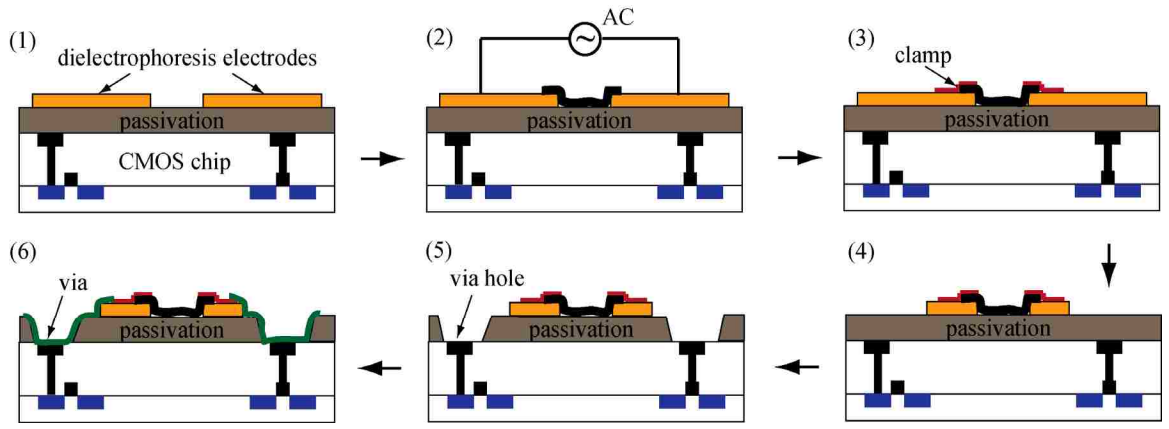


Figure C.1: Process flow to assemble an array of MWCNT interconnects on top of a platform CMOS chip [200].

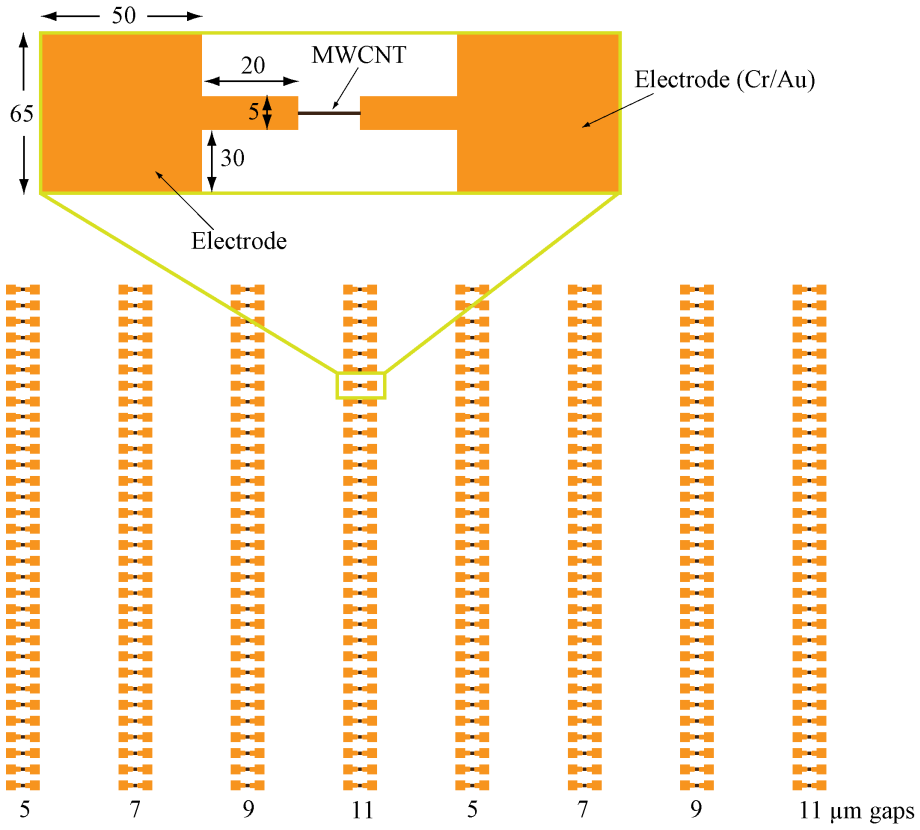


Figure C.2: Top-view of MWCNT interconnects between electrodes (unit: µm).

is dropped on the chip surface while a 24 V peak-to-peak voltage is applied at 500 kHz. The CNTs are aligned themselves in the gaps by dielectrophoresis.

Step 2: 100 nm Au is sputtered onto the ends of the CNTs to clamp them in place and establish electrical contact.

Step 3: Dielectrophoresis electrodes are etched to isolate the CNT from one another in a Cr/Au etchant solution.

Figure C.3 shows the top view of the mask layout for the first lithography step.

Figure C.4 shows the etched pattern after first lithography step and etching the metal. Figure C.5 shows the vertical cross-section. After the electrodes are fabricated on the wafer, a droplet of the prepared MWCNT solution is dropped on the chip surface while a 24 V peak-to-peak voltage is applied at 500 kHz for 30 minutes. MWCNTs will be aligned between the electrodes. The cross-section of the structure is shown in Fig. C.6.

Figure C.7 shows the top-view of the mask for the second lithography step. After this lithography step, 100 nm Au is sputtered and liftoff technique is used to clamp the MWCNTs in place and establish an electrical contact. The vertical cross-section of the structure is shown in Fig. C.8.

Figure C.9 shows the top-view of the mask for third lithography step. The dielectrophoresis electrodes are etched to isolate the CNTs from one another in a Cr/Au etchant solution.

After this photolithography step, the cross-section of the structure as shown in Fig. C.2 is fabricated for experimentation and characterization.

To date, there are no reliable, rapid, and reproducible processes to fabricate complex arrays of nanotube devices. This manufacturing issue is by far the most significant impediment to using nanotubes in electronics applications. There is much work to be done to find methods for reliably preparing only metallic or semiconducting SWCNTs by selective synthesis or through post-synthesis preparation. Till now, there is

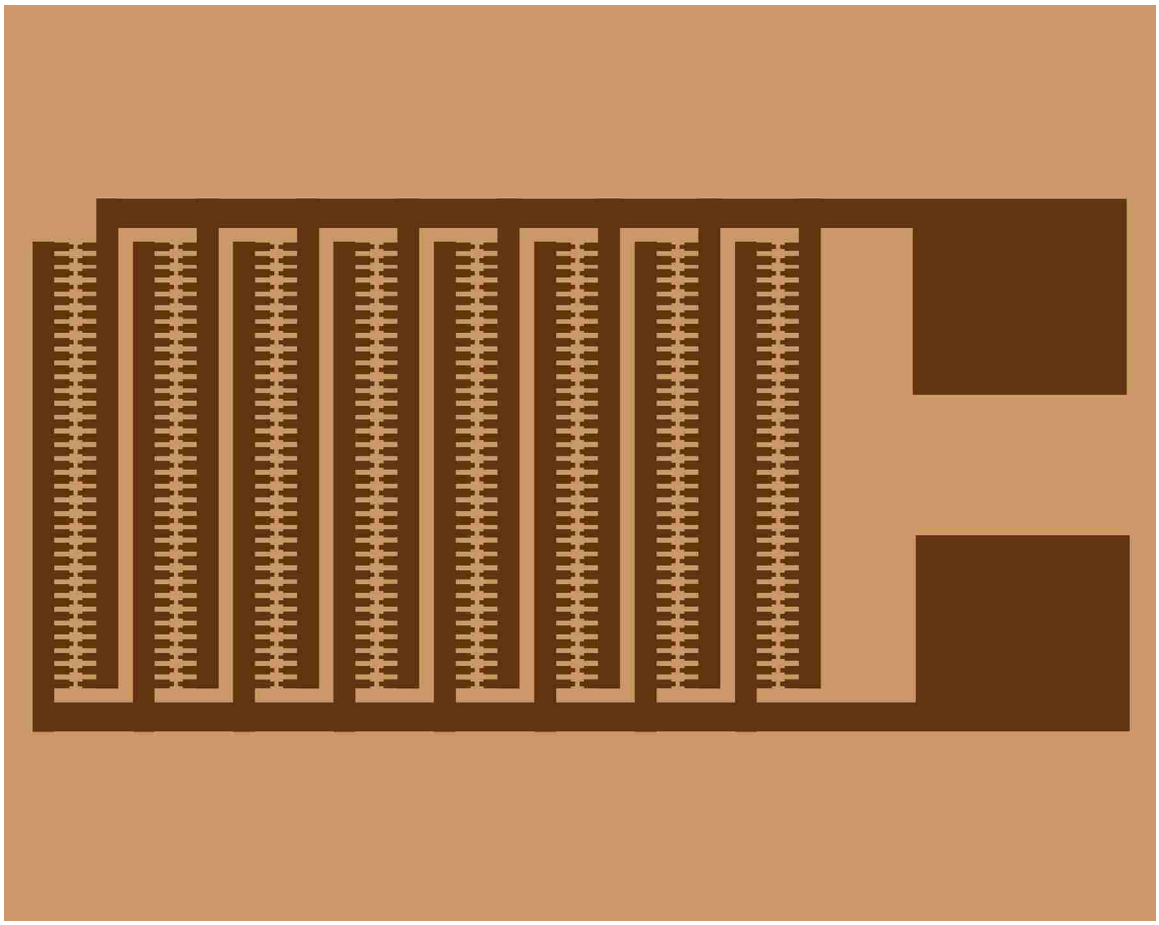

Figure C.3: Top-view of the mask for first lithography step.

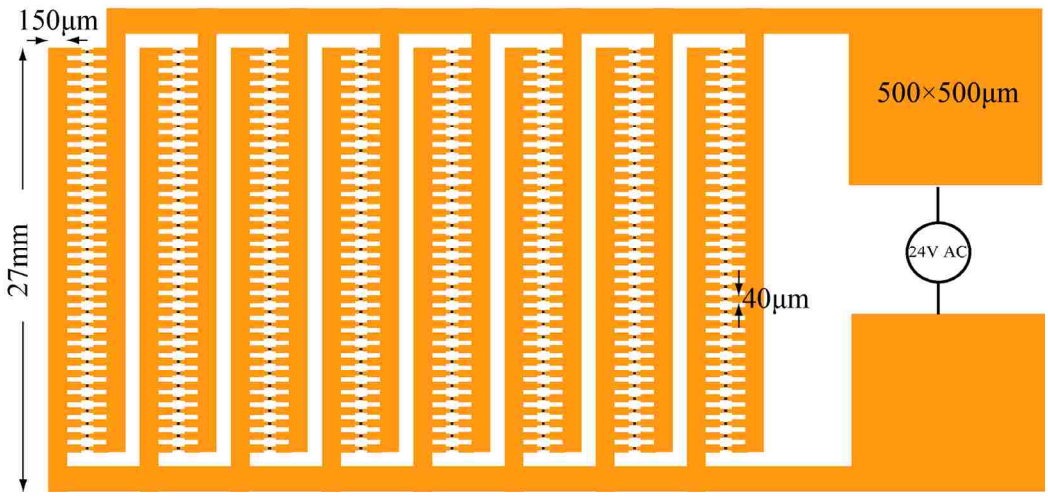


Figure C.4: Top-view of the structure after the first lithography step and metal etching.

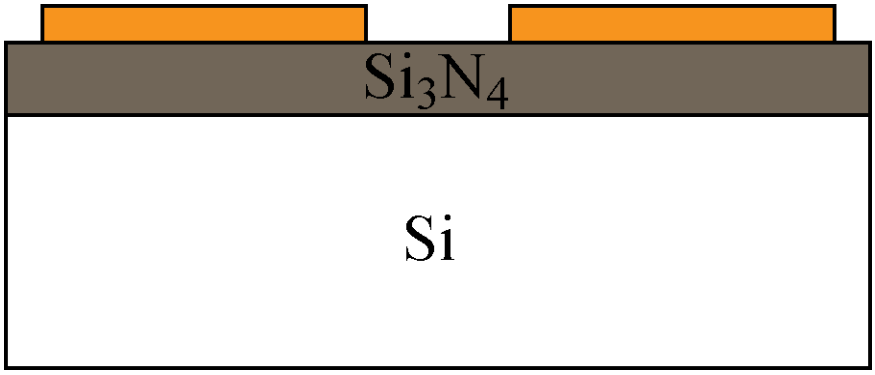


Figure C.5: Cross-section of the structure after the first lithography step and metal etching.

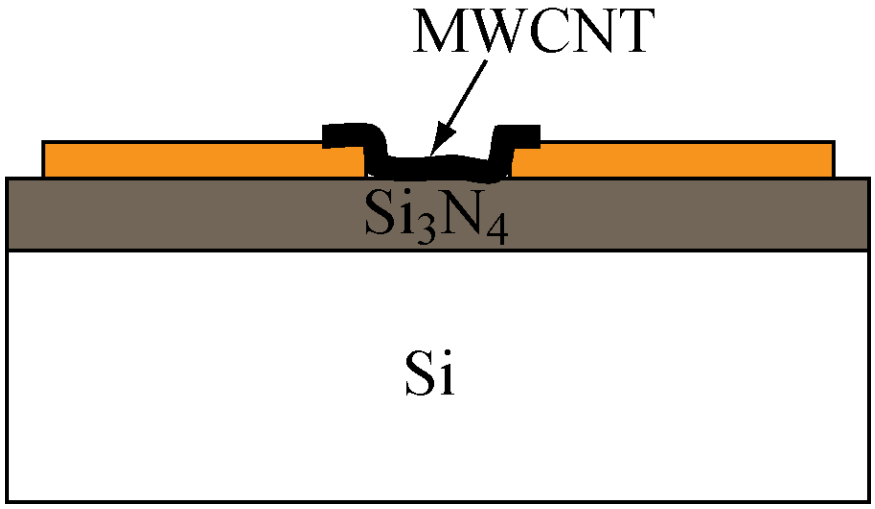


Figure C.6: Cross-section of the structure after MWCNTs are aligned between electrodes.

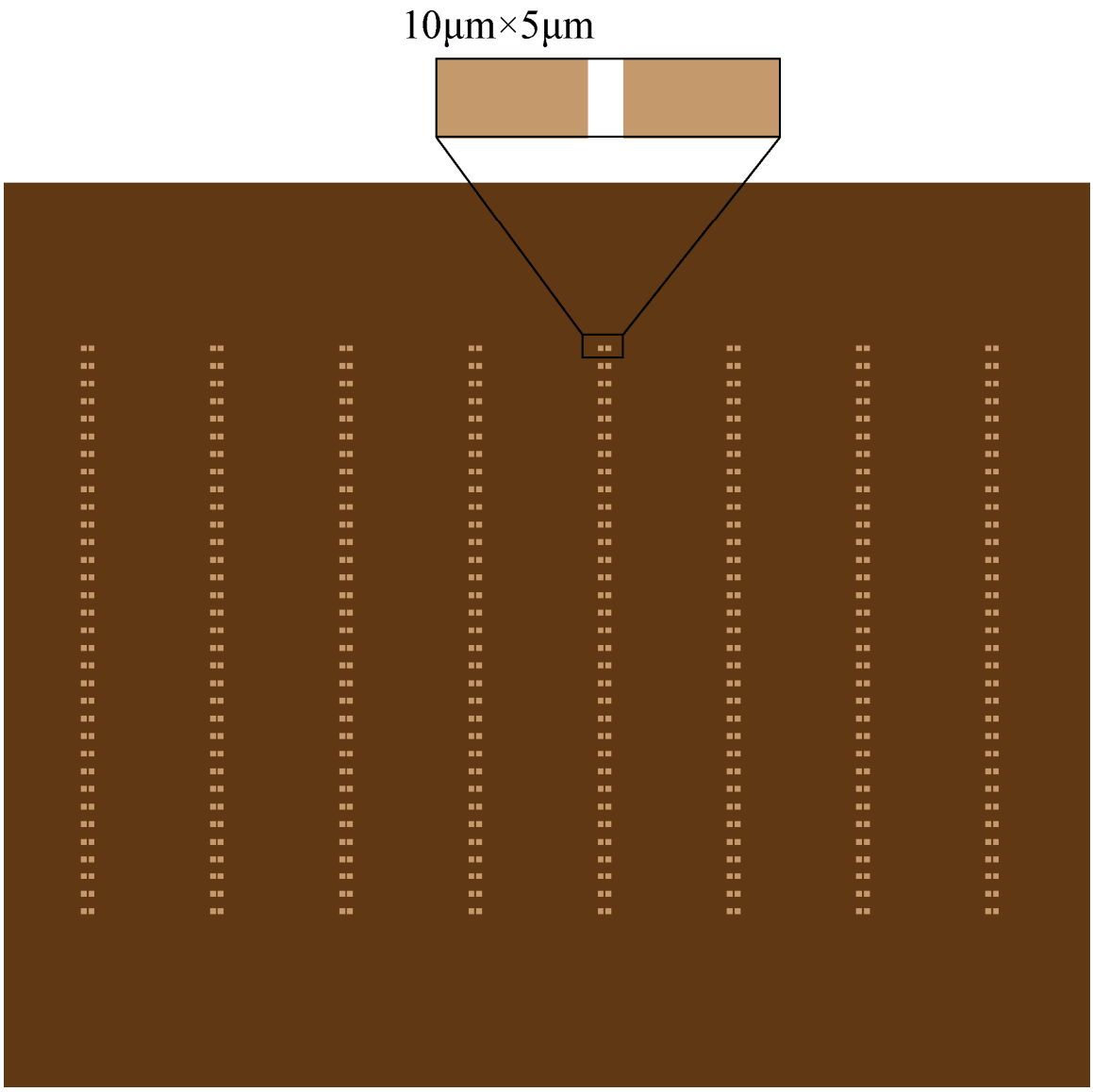


Figure C.7: Top-view of the structure after second lithography step.

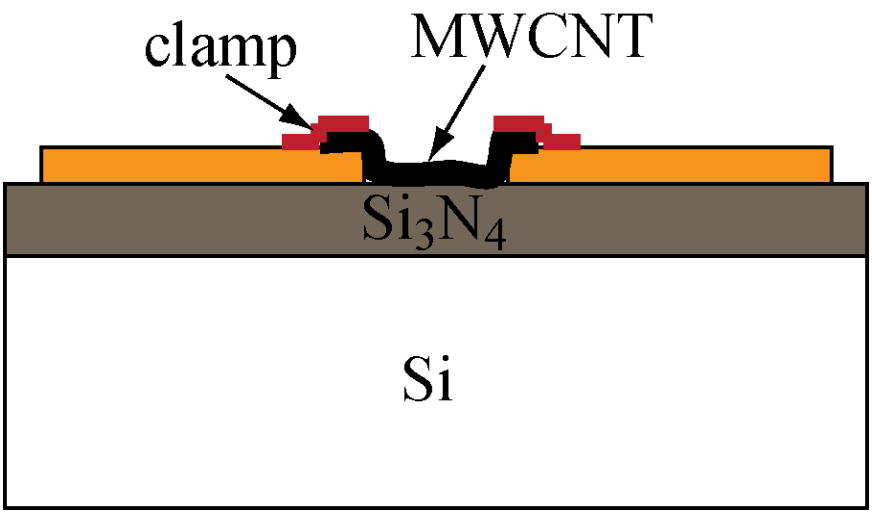


Figure C.8: Cross-section of the structure after second metal deposition (Au).

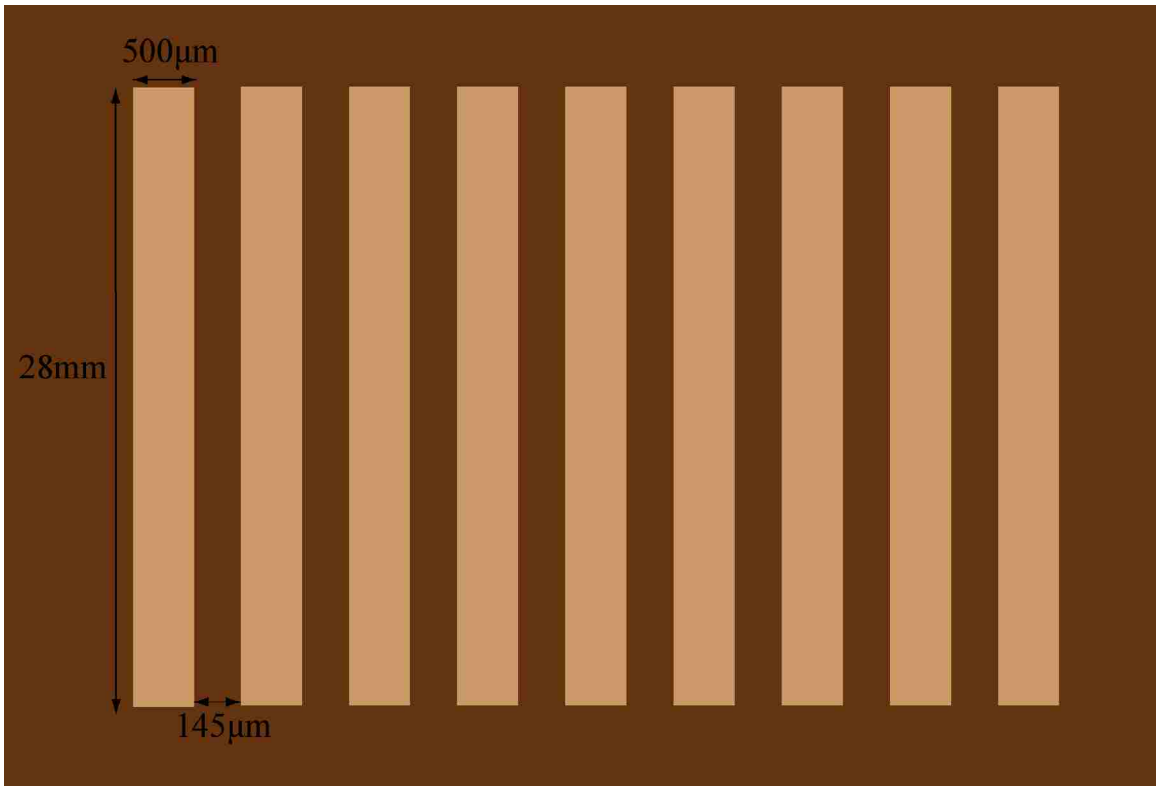


Figure C.9: Top-view of the mask for third lithography step.

only a post-fabrication physical method capable of removing metallic SWCNTs from these ropes or bundles leaving the required semiconducting SWCNTs for CNT-FETs [236].

# VITA

Yao Xu was born in January 1978, in Tianjin, China. He graduated from High School in 1996 in Beijing, China. He came to The United States in 2005 where he enrolled in the graduate program in Louisiana State University. He obtained his Master of Science in Electrical Engineering in 2008. And he is now a candidate for the doctoral degree in electrical engineering. His research interests include carbon nanotube field effect transistor (CNT-FET) modeling/simulation and integration, low power VLSI design, computer aided modeling and nanotechnology.

Mr. Xu's research publications include the following:

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