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Ternary to binary converter design in CMOS using multiple input floating gate MOSFETS

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TERNARY TO BINARY CONVERTER DESIGN IN CMOS USING MULTIPLE INPUT FLOATING GATE MOSFETS

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ABSTRACT

In this work, a ternary to binary converter circuit is designed in 0.5μm n-well CMOS technology. The circuit takes two inputs corresponding to the ternary bits and gives four outputs, which are the binary equivalent bits of the ternary inputs. The ternary inputs range from $(-1,-1)_3$ to $(1,1)_3$ which are decimal -4 to 4 and the four binary output bits are the sign bit (SB), most significant bit (MSB), second significant bit (SSB) and the least significant bit (LSB). The ternary inputs (-1, 0 and 1) are represented in terms of voltages of -3V, 0V and 3V.

Multiple input floating gate (MIFG) MOSFETS are used in the design of ternary to binary converter. The four circuits to generate the SB, MSB, SSB and LSB outputs are designed separately and then connected together to perform the entire conversion. The MIFG MOSFET takes multiple input signals, which are the ternary inputs in this case and calculates the weighted sum of the inputs. This weighted sum of the inputs is called floating gate voltage and is given as input to the CMOS inverter. The CMOS inverter gives a high or low binary output depending on if the floating gate voltage is higher or lower than the threshold voltage of the CMOS inverter.

The circuits are simulated using MOSIS BSIM level 7 model parameters. LEDIT version 13 is used for the layout and a total of 22 transistors are used in the design of the converter circuit. The floating gate of the transistor is simulated by not giving the input directly to the gate of the transistor. Instead inputs are fed to one end of the capacitors and the other end of the capacitors are tied together and given as an input to the inverter. The converter chip occupies an area of $1140 \times 2090\ \mu m^2$.

CHAPTER 1. INTRODUCTION AND LITERATURE REVIEW

1.1 Introduction

1.1.1 Binary Logic

Binary logic has been used widely because of the availability of efficient devices and circuits that work on two state logic. Binary systems have some disadvantages too. The design of these systems requires the use of increased silicon area due to increase in functionality and increase in the density of interconnect wires. There have also been packaging difficulties with binary systems [1]. In any VLSI circuit, around 70 percent of the total area is used for interconnections, 20 percent for insulation and 10 percent for device [2]. This has led to the use of multi-valued circuits or devices that help overcome the disadvantages of the binary systems. Multi-valued circuits or devices are designed to handle more than two logic levels

1.1.2 Multi-Valued Logic

The multi-valued circuits can transmit more information than a binary circuit and hence reduce the number of interconnections inside the chip. This also reduces the complexity of the circuits to a great extent. As discussed above, the number of on and off chip interconnections can also be reduced and hence increasing the transmission speed of information [3]. These advantages have led to the use of multi-valued system over binary systems for certain applications. The commonly used multi-valued radix in use are the ternary radix (radix-3) and the quaternary radix (radix-4).

1.1.3 Ternary Logic

In any numerical system, the number of digits to represent a quantity is inversely proportional to the size of the radix. The number necessary to express a range N is given by $N = R^d$ where R is the radix and d is the necessary number of digits. The cost and complexity of the system is proportional to the digit.

If the cost and complexity of the system is represented as C and the digit capacity is R x d [1], then

$$C = k(R \times d) = k\left[R\frac{\log N}{\log R}\right] \tag{1.1}$$

In Eq.(1.1), k is a constant. Differentiating Eq.(1.1) with respect to R will show that for minimum cost C, R should be equal to e, which is equal to 2.718. Since R must be an integer, rounding the value of R to R = 3 (ternary) would be more economical than binary or any other radix system. Two logic systems are available in ternary logic, balanced ternary logic, which uses logic levels (-1, 0 and 1) and simple ternary logic that uses positive logic levels (0, 1 and 2). Ternary circuits have few advantages over quaternary [3] as 3 is the next higher radix after binary and lower radix than quaternary. The ternary functions and circuits have simpler form and construction than quaternary and also overcome the disadvantages of binary systems. Ternary circuits are also more economical than quaternary circuits and the same hardware can be used for functions like addition and subtraction if balanced ternary logic is used.

The balanced ternary logic level systems have additional mathematical advantages for numerical representation and in arithmetic operations over the simple ternary logic system [1,4]. It can represent both positive and negative numbers without using a unary minus. The negative of a number is obtained by interchanging +1 and –1. Addition and multiplication are almost as simple as for the binary. Both addition and subtraction may be performed in balanced ternary system by sign changes of the addend or subtractend, respectively as required and also using the same hardware. Division is also very simple to perform. The operation of rounding to the nearest integer is by deleting everything to the right of the radix point as in truncation. The number of gates used in balanced ternary is much less in comparison to binary and unsigned ternary systems, the disadvantage though being increased logic delay. In standard CMOS process with

supply voltage of 3V, the logic level -1, 0 and 1 is defined as -3V, 0V and 3V, respectively. Fig.1.1 shows ternary logic with a 3 V supply voltage [5].

In a mixed radix systems using both multi-valued and binary logic, encoding and decoding circuits need to be designed that can perform the required conversion between multi-valued logic and binary logic.

1.2 Literature Review

1.2.1 Radix Conversion Techniques

A number of radix conversion techniques have been proposed previously that can be used to convert binary to higher order radixes. A few such techniques are discussed below.

Olson et al., [6] reported the design of a radix conversion circuit using Radix Converting Read Only Memory (RCROM). In this work, the value to be converted from one radix form to another acts as an address to the memory. The address is decoded to give row and column signals. The row signal turns on a column line and the column signal turns on a transmission gate that gives the output. Few other decoding techniques were implemented by Wu [3] in which ternary to binary conversion was done by changing the width to length ratio of CMOS transistors and multi-threshold CMOS transistors. Ueno *et al*., [6] designed a switched capacitor array technique to convert binary to multi-valued and vice versa. In this technique, for ternary to binary conversion, the ternary inputs are converted into a threshold voltage, V_{th} using Eq.(1.2), where n is the radix and V_{ref} is the reference voltage:

$$V_{th}(k) = \left\{1 - \frac{2k-1}{2(n-1)}\right\} V_{ref}, \text{ (k=1,2,3...,n-1).} \qquad (1.2)$$

These threshold voltages are compared with multi-valued input voltages using a comparator. The output of the comparator is then fed as inputs to the decoding circuit that gives the binary output.

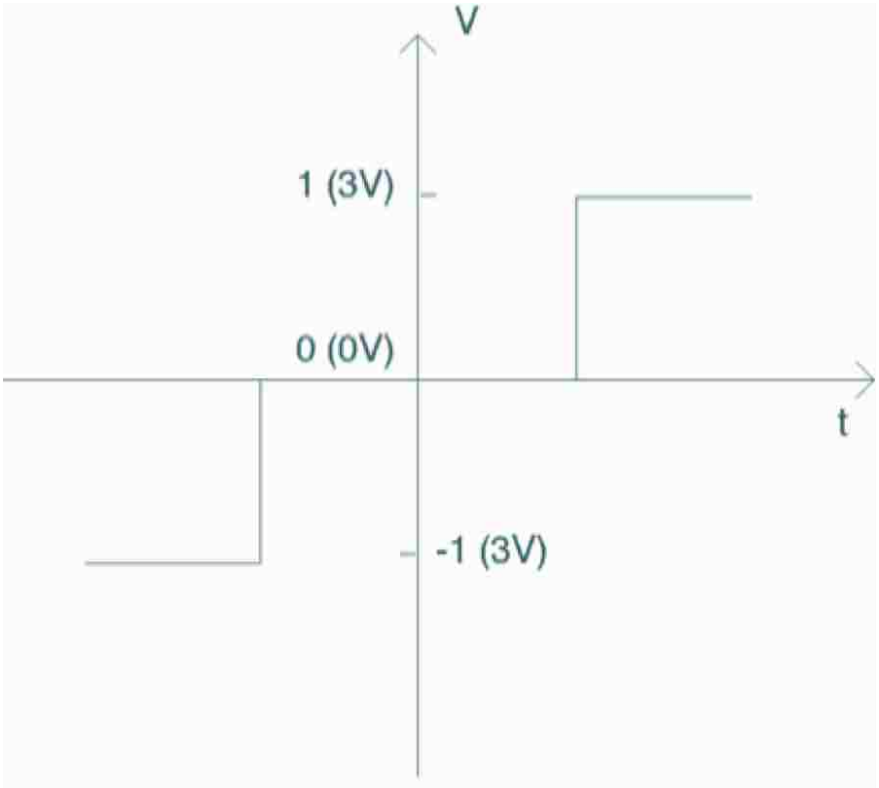

Figure 1.1: Logic levels in balanced ternary logic.

1.2.2 Floating Gate MOSFET

Floating gate MOSFETS also known as neuron MOS transistors simulate the function of biological neurons as described by Shibata and Ohmi [8]. The floating gate MOSFET is a MOS transistor with multiple inputs. The floating gate MOSFET accepts multiple input signals, calculates the weighted sum of all the inputs and then controls the on and off action of the transistor [8]. Since the neuron MOS transistor accepts multiple inputs, it helps reduce the number of interconnections on the chip. Due to the unique operation of these devices they have been used for a number of applications including realization of Boolean logic circuits and to build high performance memories in digital CMOS processes. Floating gate MOSFET'S have been developed in various ways. Initially floating gate MOSFET'S were developed using two levels of polysilicon. Minch and Hasler [9] have presented a design with only one layer of polysilicon. Mondragon-Torres *et al*., [10] have proposed floating gate transistors where the floating gate in MOS device is on top of the n-well. The n-well provides noise isolation for the transistor from the substrate and can be used as an additional input for the threshold voltage control or for signal modulation. Kucic *et al*., [11] have discussed methods by which the charge on the floating gate can be modified by exposure to UV rays. The floating gate charge can also be modified by tunneling through thin oxides or by the acceleration of electrons due to high electric field at the drain.

Floating gate MOSFETS have been used recently for various applications in different fields. One of the applications as described by Zhai and Abshire [12] show the design and analysis of a adaptive first order low pass filter using floating gate MOSFETS. The adaptive filter is used for system identification purposes for which control laws are defined which help in adjusting the parameters of the adaptive system to match the unknown system and thus enabling the identification of the unknown system as shown in Fig.1.2 [12]. The floating gate MOSFET

transistor is made to work in subthreshold range. The transistor along with the filter architecture is used to realize accurate and stable learning rules for the system parameters like output gain and cut-off frequency of a low pass filter.

A low voltage 8-bit analog-to-digital converter has also been designed using floating gate MOSFETS [13]. The floating gate MOSFETS are used in the differential stage of the converter. The 8 bits are given as inputs to the floating gate of one of the transistors. The values of the capacitors are designed in a way that given the 8-bit input, the digital-to-analog converter give the appropriate analog output. This method is shown to have simple architecture along with good accuracy and low power consumption [13].

A low voltage current mirror circuit has been presented in floating gate MOSFETS as shown in Fig.1.3 [14]. Applying and changing a dc bias voltage (V_b) at the gate of the transistor can adjust the threshold voltage at the gate of the transistor. When V_b is made proportional to Iin, V_T can be made proportional to Iin, which is achieved by feeding back Iin. A floating gate current mirror helps increase the operating range of the current mirror.

Another application of floating gate MOSFET in the area of sensors as described by Neng et al., [15] shows the application in sensor applications as CMOS image sensors. There is a need to design image sensors with increased image resolution. This can be done by reducing the pixel size, which in turn is done by reducing the number of pixel transistors to a single pixel. A floating gate MOSFET is used as the pixel transistor. It is used in the place of a photodiode. For reading the signal, the floating gate transistor is operated as a source follower and the same transistor can perform the reset operation by evacuating the charges by the bias control [15]. Thus, the use of a floating gate MOSFET reduces the use of three or more transistors to a single transistor performing all the operations. An increase in conversion speed is also obtained using this design [15].

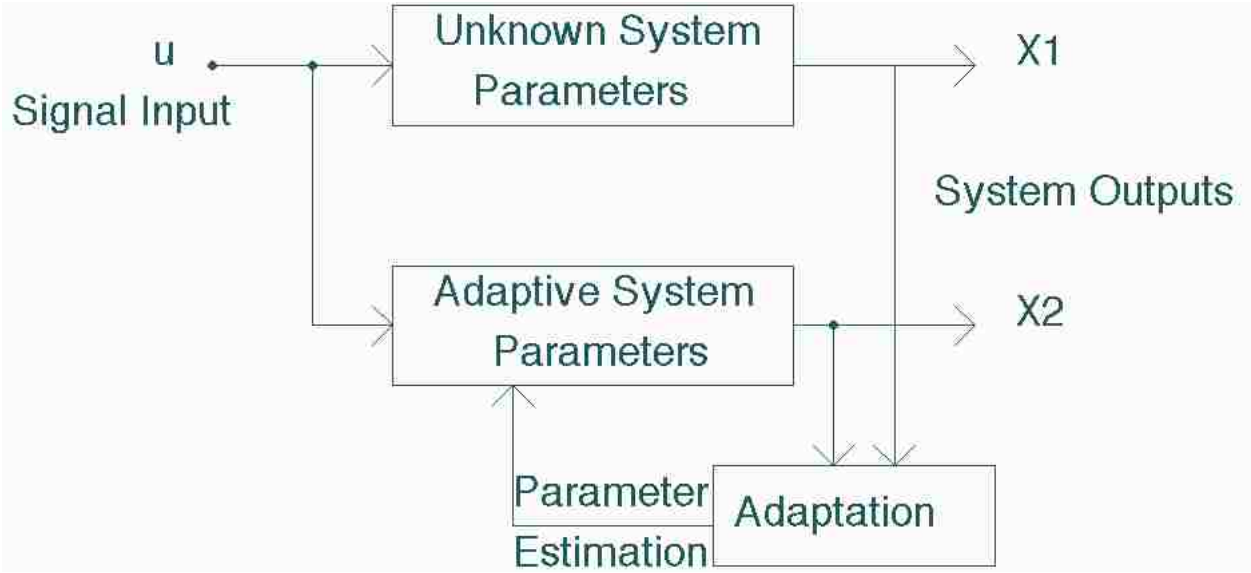

Figure 1.2: Unknown system identification [12].

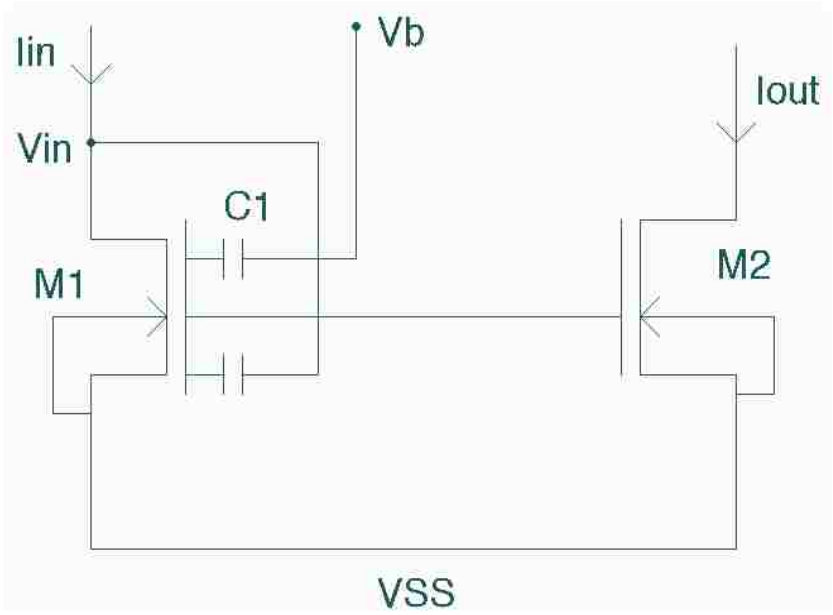

Figure 1.3: Simple floating gate current mirror circuit [14].

Floating gate MOSFETS have also found application in designing electrostatic discharge protection circuits [16]. Protection against electrostatic discharge is a major challenges faced in VLSI design due to shrinking device dimensions. In a recent work of Chou et al., [16], gate protection devices have been replaced by the floating gate MOSFETS as shown in Fig.1.4.

Floating gate MOSFETS have also found wide application in memory design. The design of a two transistor DRAM using floating gates has been shown by Lu et al., [17] and Lu et al., [18]. A conventional DRAM is designed with stack or deep trench capacitor for data storage. This leads to complexity in processing as memories are continuously scaled down. In [17], a two transistor (2T) floating body cell (FBC) is proposed for embedded-DRAM applications. In this design, the charged/discharged body of one transistor (1T) drives the gate of the other. This 2T-FBC structure actually results in a floating-body/gate cell (FBGC) and is shown to reduce the power dissipation and helps in longer data retention and higher memory density. A simplified design of the two transistor design is presented in [18], where the first transistor is converted into a gated diode that enables direct connection of the body of the first transistor to the gate of the second transistor resulting in the cell size reduction.

1.3 Chapter Organization

The basic structure and operation of floating gate devices is discussed in Chapter 2. The design of the ternary to binary converter circuit with simulation results obtained from SPICE is presented in Chapter 3. Chapter 4 includes the experimental results and measurements obtained from the fabricated chip. Chapter 5 concludes the present work. The circuit input files used to find the transfer characteristic of floating gate MOSFETS and simulate the ternary to binary converter circuit are listed in Appendix A. The MOS model parameters of the fabricated chip are presented in Appendix B. Technique to simulate floating gate devices in SPICE is shown in Appendix C.

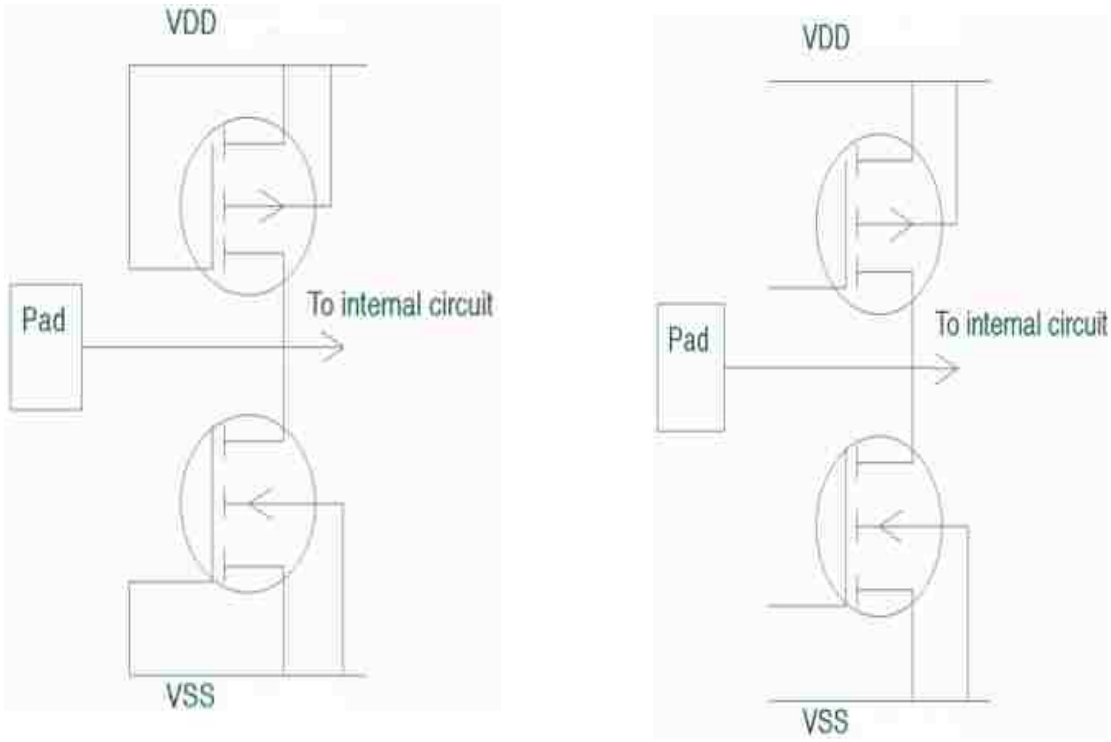

Figure 1.4: ESD circuit (a) Conventional ESD circuit (b) Floating gate ESD circuit [16].

CHAPTER 2. MULTIPLE INPUT FLOATING GATE MOSFET

2.1 Introduction

The multiple input floating gate (MIFG) MOS transistor in addition to performing the switching function of a transistor also helps in significantly reducing the number of interconnections, the layout area and power dissipation, when used in a circuit. The basic device is a MOS transistor with a floating gate. The gate is called floating because it is not directly connected to the input signals but is connected through capacitive coupling. The potential on the floating gate is determined and hence controlled by the signal applied at the input and the values of the coupling capacitors. The MIFG MOSFET can calculate the weighted sum of all the input signals at the gate. It also controls the "off" and "on" state of the transistor based on the result of the weighted sum calculation [19]. The floating gate MOSFETS are implemented in standard analog CMOS process.

2.2 Basic Structure and Operation

The basic structure of the Multiple Input Floating Gate (MIFG) MOSFET [8, 19] is shown in the Fig. 2.1 [5, 20]. It consists of n-channel MOS transistor having a gate electrode, which is electrically floating. The floating gate in the MOSFET extends over the channel and the field oxide. Array of control signals, which are inputs to the transistor, are formed over the floating gate using the second polysilicon layer.

The n-input gates are not directly connected to the gate but are coupled through through capacitors. The capacitive coupling between the multiple input gates and the floating gate and the channel is shown in Fig. 2.2. The capacitors C1, C2, C3, …….., Cn are the coupling capacitors between the floating gate and the inputs and C0 is the coupling capacitor between floating gate and substrate.

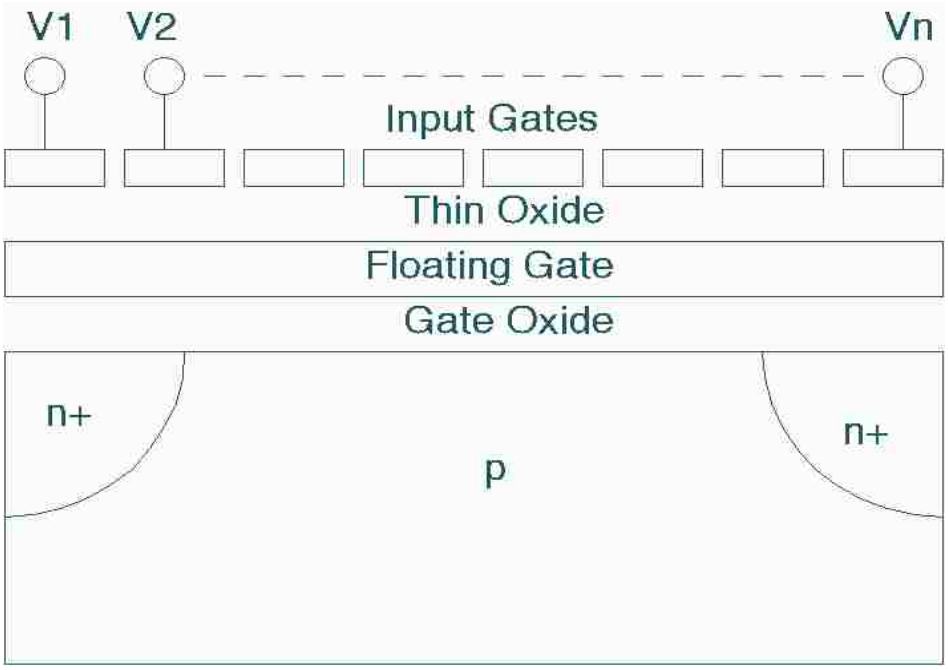

Figure 2.1: Basic structure of MIFG MOSFET.

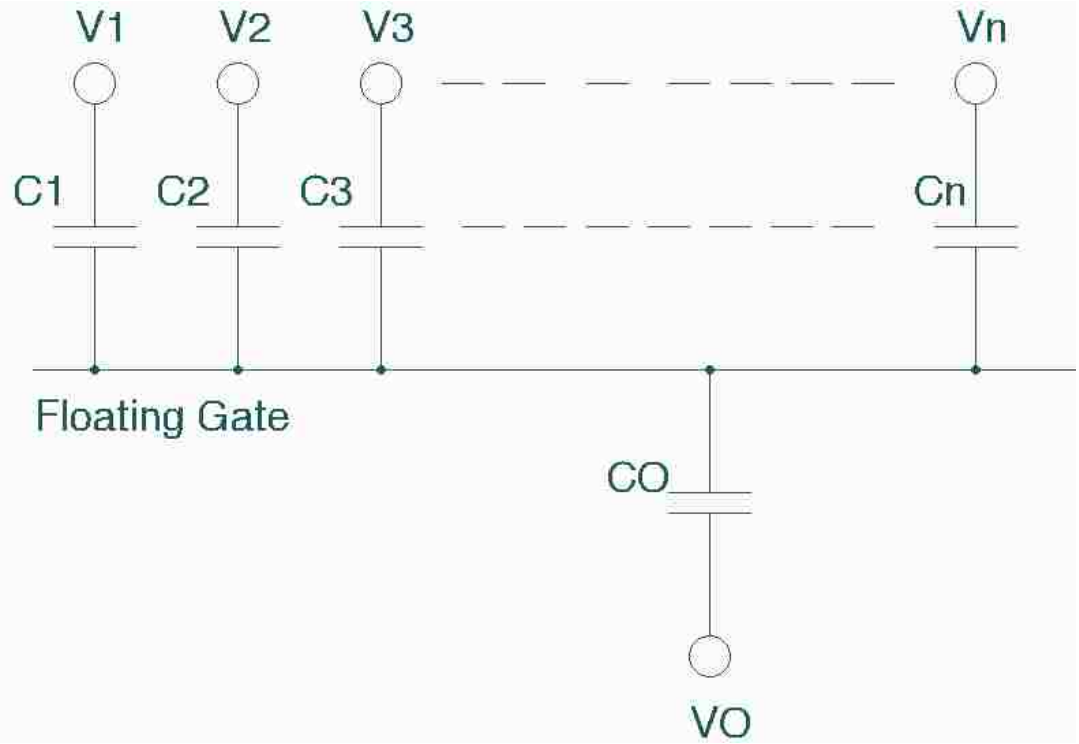

Figure 2.2: Relationship between terminal voltages and coupling capacitors.

2.3 Analysis

A simple analysis is presented to present a relationship to determine the weighted sum of the inputs at the floating gate, also known as the floating gate voltage and to determine the conditions that need to be satisfied to turn-on and turn-off the NMOS and PMOS transistors.

If Q1, Q2, Q3, ..., Qn are the charges stored in corresponding capacitors C1, C2, C3,….., Cn, respectively. At any given time, t, the net charge on the floating gate QF (t) is given by [19],

$$QF(t) = Qo + \sum_{i=1}^{n}\left(-Qi(t)\right) = \sum_{i=0}^{n} Ci\left(\Phi F(t) - Vi(t)\right) \tag{2.1}$$

or

$$QF(t) = \Phi F(t)\sum_{i=0}^{n} Ci - \sum_{i=0}^{n} CiVi(t)\ , \tag{2.2}$$

where n is the number of inputs, Q0 is the initial charge present on the floating gate, Qi (t) is the charge present in the capacitor Ci at time, t and ΦF (t) is the potential at the input of the floating gate. The law of conservation of charge states that the net charge of an isolated system remains constant [19]. Setting V0 = 0 V and applying conservation of charge at the floating gate [19],

$$\Phi F(0)\sum_{i=0}^{n} Ci - \sum_{i=1}^{n} CiVi(0) = \Phi F(t)\sum_{i=0}^{n} Ci - \sum_{i=1}^{n} CiVi(t) \tag{2.3}$$

$$\Phi F(t) = \Phi F(0) + \frac{\sum_{i=1}^{n} Ci - \sum_{i=1}^{n} CiVi(0)}{\sum_{i=0}^{n} Ci} \tag{2.4}$$

Assuming initial charge on the floating gate to be zero, at equilibrium Eq. (2.4) reduces to,

$$\Phi F(t) = \frac{\sum_{i=1}^{n} CiVi(t)}{\sum_{i=0}^{n} Ci} = \frac{\sum_{i=1}^{n} CiVi(t)}{CTOT} \tag{2.5}$$

In Eq. 2.5, CTOT is the sum total of all the capacitances connected at the input of the floating gate. CTOT can also be defined through a floating gate gain parameter, γ which is described by Eq. 2.6 as follows:

$$\gamma = \frac{C1 + C2 + ... + Cn}{CTOT} \tag{2.6}$$

If the coupling capacitor, C1 is the largest, the gate that it is connected to is called the principle gate [19] and its value can be approximated to,

$$C_1 = \frac{\gamma CTOT}{2} \tag{2.7}$$

The transistor is switched ON or OFF depending on whether ΦF (t) is greater than or less than threshold voltage of the transistor. The voltage on the floating gate of the transistor is given by the Eq. (2.6). If VS is the voltage on the source of PMOS transistor, it is ON if,

$$\Phi F - VS < |\text{VTHP}| \tag{2.8}$$

and the transistor is OFF if,

$$\Phi F - VS > |\text{VTHP}| \tag{2.9}$$

If VS is the voltage on the source of NMOS transistor, then [11], it is ON if

$$\Phi F - VS > VTHN \tag{2.10}$$

and the transistor is OFF if

$$\Phi F - VS < VTHN \tag{2.11}$$

where VTHN and $|\text{VTHP}|$ threshold voltage of NMOS and PMOS transistors.

2.4 I-V Characteristics of MIFG Transistors

The symbol of NMOS and PMOS floating gate transistors are shown in Figs. 2.3 and 2.4, respectively [5, 20]. The circuits used to obtain the I-V characteristics of floating gate NMOS (FGNMOS) and PMOS transistors (FGPMOS) are shown in Figs. 2.5 and 2.6, respectively [5].

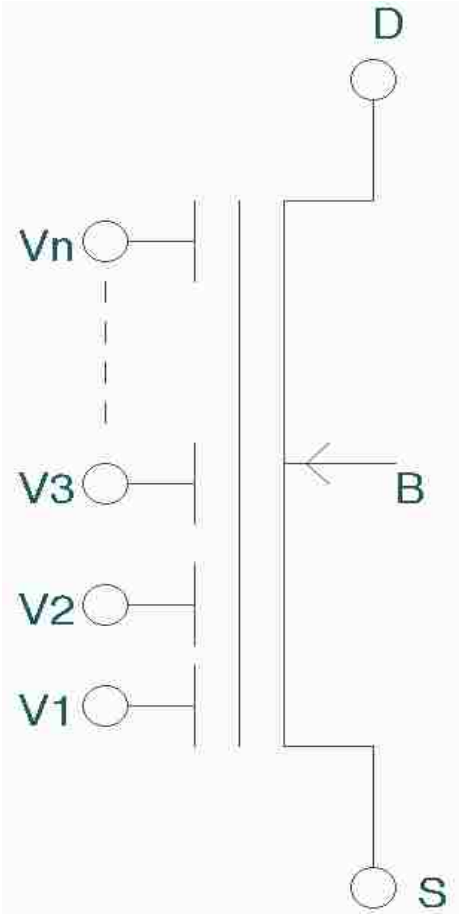

Figure 2.3: Multiple input floating gate NMOS transistor.

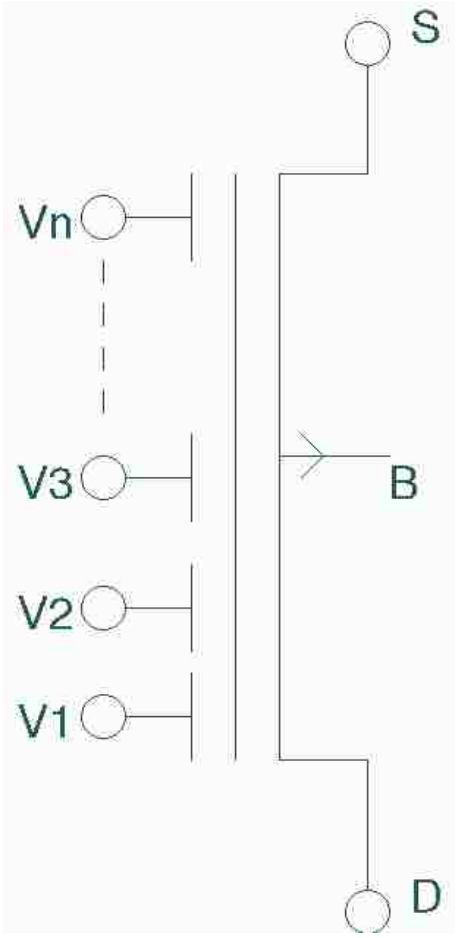

Figure 2.4: Multiple input floating gate PMOS transistor.

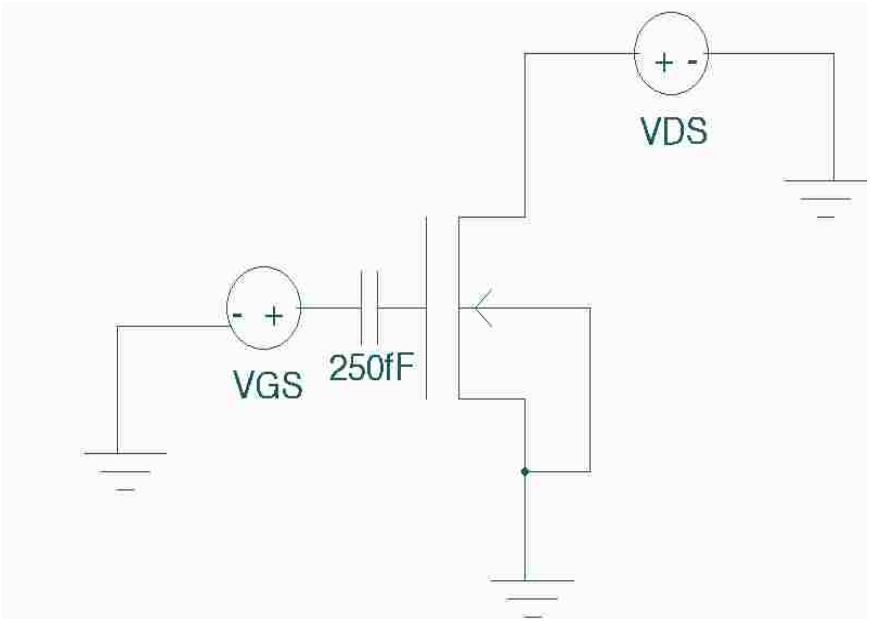

Figure 2.5: Circuit diagram of a floating gate NMOS transistor to obtain the I-V characteristics.

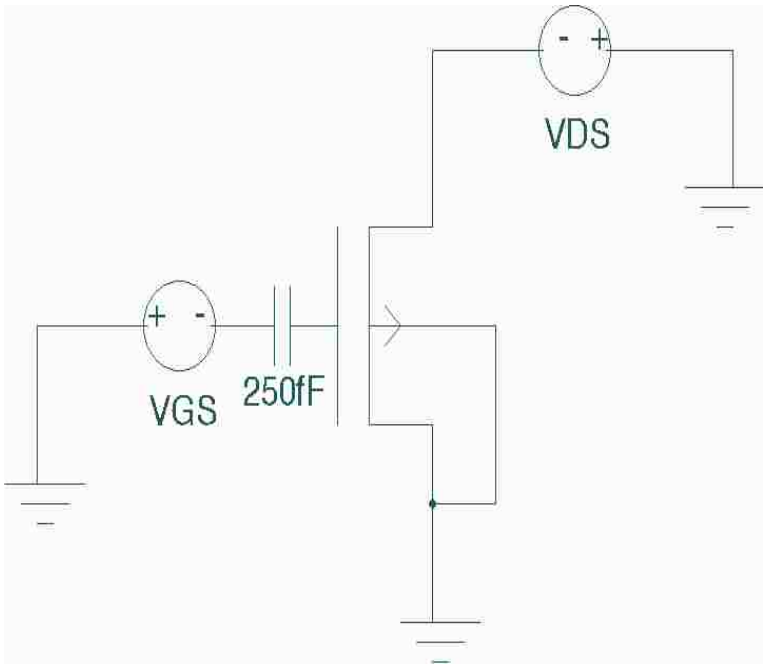

Figure 2.6: Circuit diagram of a floating gate PMOS transistor to obtain the I-V characteristics.

In this work, the value of the capacitors used at the floating gate is equal or greater than 250fF. The transistor dimensions chosen are (W/ L=4.2 μm/2.1 μm). For dc analysis in SPICE, the capacitor becomes an open circuit and no dc input is applied to the gate of the transistor. We thus perform transient analysis instead of dc analysis to obtain the characteristics. A ramp voltage is applied instead of the dc voltage at the floating gate and the circuit is simulated for various values of VGS. The I-V characteristic is then plotted between ID and VDS for various values of VGS as shown in Figs. 2.7 and 2.8 [20]. In Figs. 2.7 and 2.8, VDS is varied from 0 to 3V in steps of 1V and ID is plotted for different values of VGS ranging from 0 to 3V [20].

The transfer characteristics of the NMOS and PMOS transistors have also been plotted as shown in Figs. 2.9 and 2.10, respectively [20]. The input circuit files to obtain these characteristics are included in the Appendix A. BSIM3 MOS transistor model parameters are used which are given in Appendix B.

2.5 MIFG CMOS Inverter

A multiple input floating gate CMOS inverter is used in the ternary to binary converter circuit designed in this work. The multiple-input floating gate MOS inverter is shown in Fig. 2.11 [5, 20]. In Fig. 2.11, V1, V2, V3,……, Vn are the input voltages and C1, C2, C3,….., Cn are corresponding coupling capacitors. Equation (2.5) is used in finding the voltage on the floating gate of the inverter. A weighted sum of all inputs is performed at the gate and is converted into a multiple-valued voltage VM or ΦF at the floating gate. Switching of the floating gate CMOS inverter depends on whether ΦF obtained from the weighted sum is greater than or less than the threshold voltage or switching voltage, ΦT of the CMOS inverter [11,19]. The switching voltage, ΦT is defined as the average of Φgo, the input voltage to obtain logic 1 (3V) at the output and Φs1, which is the input voltage to obtain logic 0 (0 V) at the output.

Hence we can define switching voltage as,

$$\Phi T = \frac{\Phi go + \Phi s1}{2} \tag{2.12}$$

It can be seen that the output (VOUT) of floating gate CMOS inverter is given by,

VOUT = HIGH (3 V) if ΦF < ΦT and VOUT = LOW (0 V) if ΦF > ΦT.

The values of Φgo and Φs1 are obtained from voltage transfer characteristic of a CMOS inverter. The values of Φgo and Φs1 for transistors with sizing $(W/L)_n$=4.2 μm/2.1 μm and $(W/L)_p$= 20.28 μm / 2.1 μm are shown in the Fig. 2.12. Φgo and Φs1 are the input voltages at which the output VOUT is (VDD-0.1) V and 0.1 V, respectively. From Figure 2.12, we can see that Φgo = 1.07V and Φs1 = 1.59V. The calculated threshold voltage ΦT is 1.33V. Now depending on if ΦF is greater or smaller than ΦT the transistor will switch on or off and will give a high or low output.

2.6 Capacitor Network

The capacitor network formed for an n-input floating gate inverter is shown in Fig. 2.13 [5, 20]. The gate oxide capacitance COXP of PMOS transistor is between the floating gate and N-well, which is connected to VDD and the gate oxide capacitance COXN is between the floating gate and substrate, which is connected to VSS. The capacitance CP is the parasitic capacitance formed between the field oxide and substrate, which is connected to VSS. From Fig 2.13, the voltage on the floating gate ΦF is given by,

$$\Phi_F = \frac{V1 \times C1 + V2 \times C2 + V3 \times C3 + ... + Vn \times Cn + VDD \times COXP + VSS \times (CP + COXN)}{C1 + C2 + C3 + ... + Cn + COXP + COXN + CP} \tag{2.13}$$

Setting VSS = 0V, the voltage on the floating gate is given by,

$$\Phi_F = \frac{V1 \times C1 + V2 \times C2 + V3 \times C3 + ... + Vn \times Cn + VDD \times COXP}{C1 + C2 + C3 + ... + Cn + COXP + COXN + CP} \tag{2.14}$$

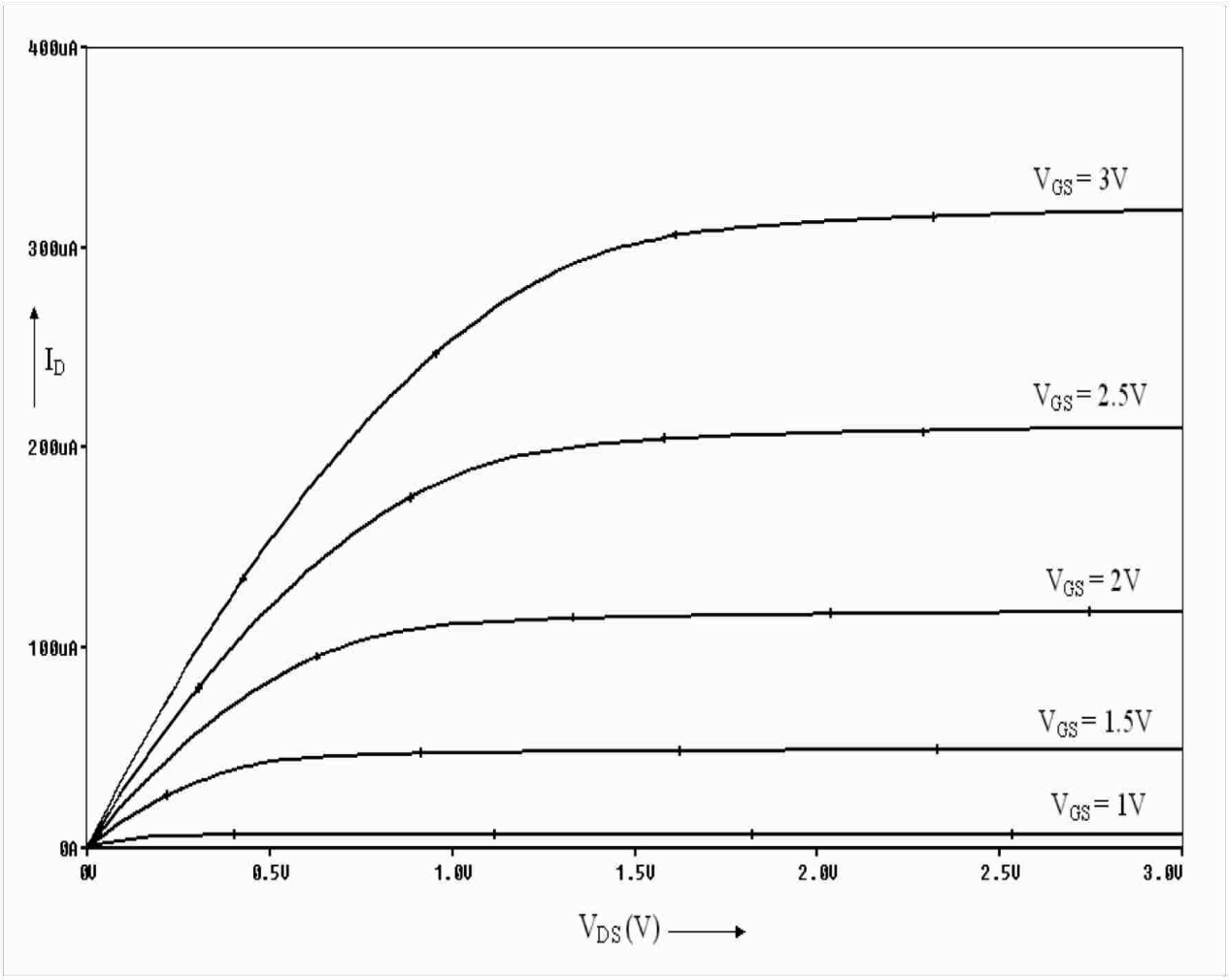

Figure 2.7: I-V Characteristics of a FGNMOS transistor. Note: (W/ L= 4.2 µm /2.1 µm).

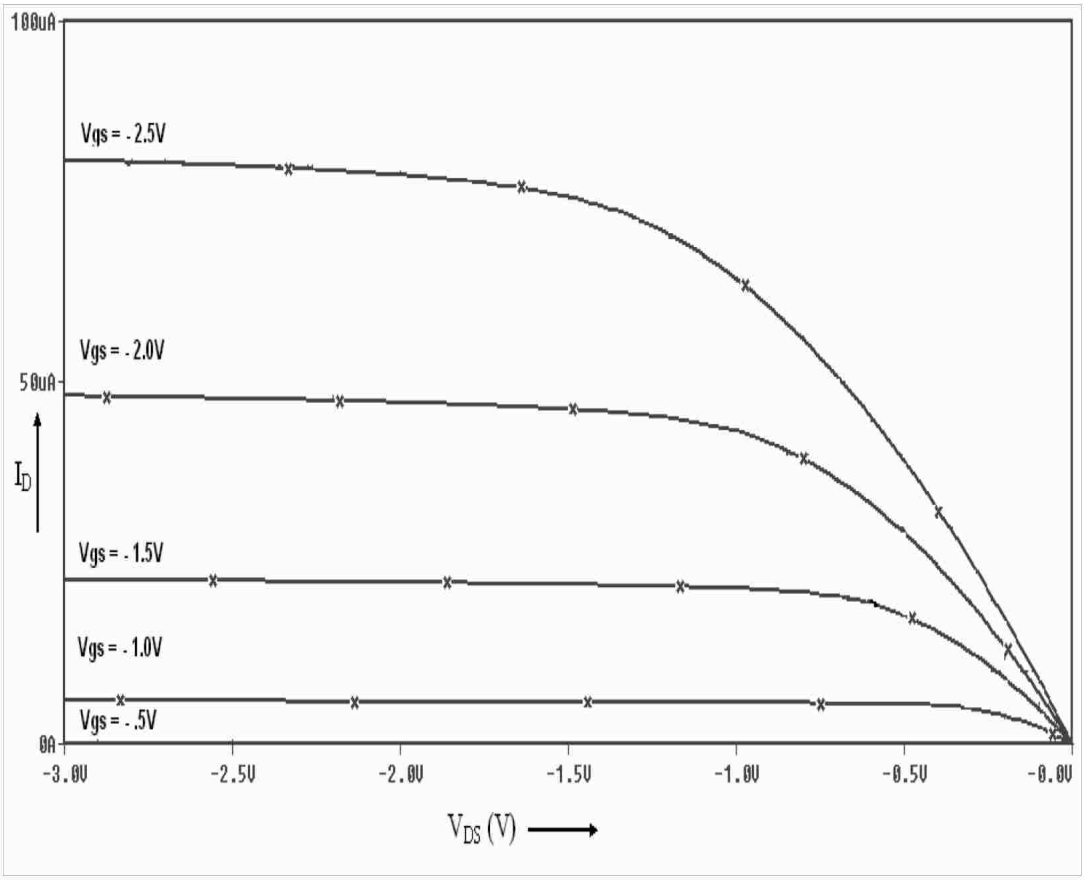

Figure 2.8: I-V Characteristics of a FGPMOS transistor. Note: (W/ L= 4.2 µm /2.1 µm).

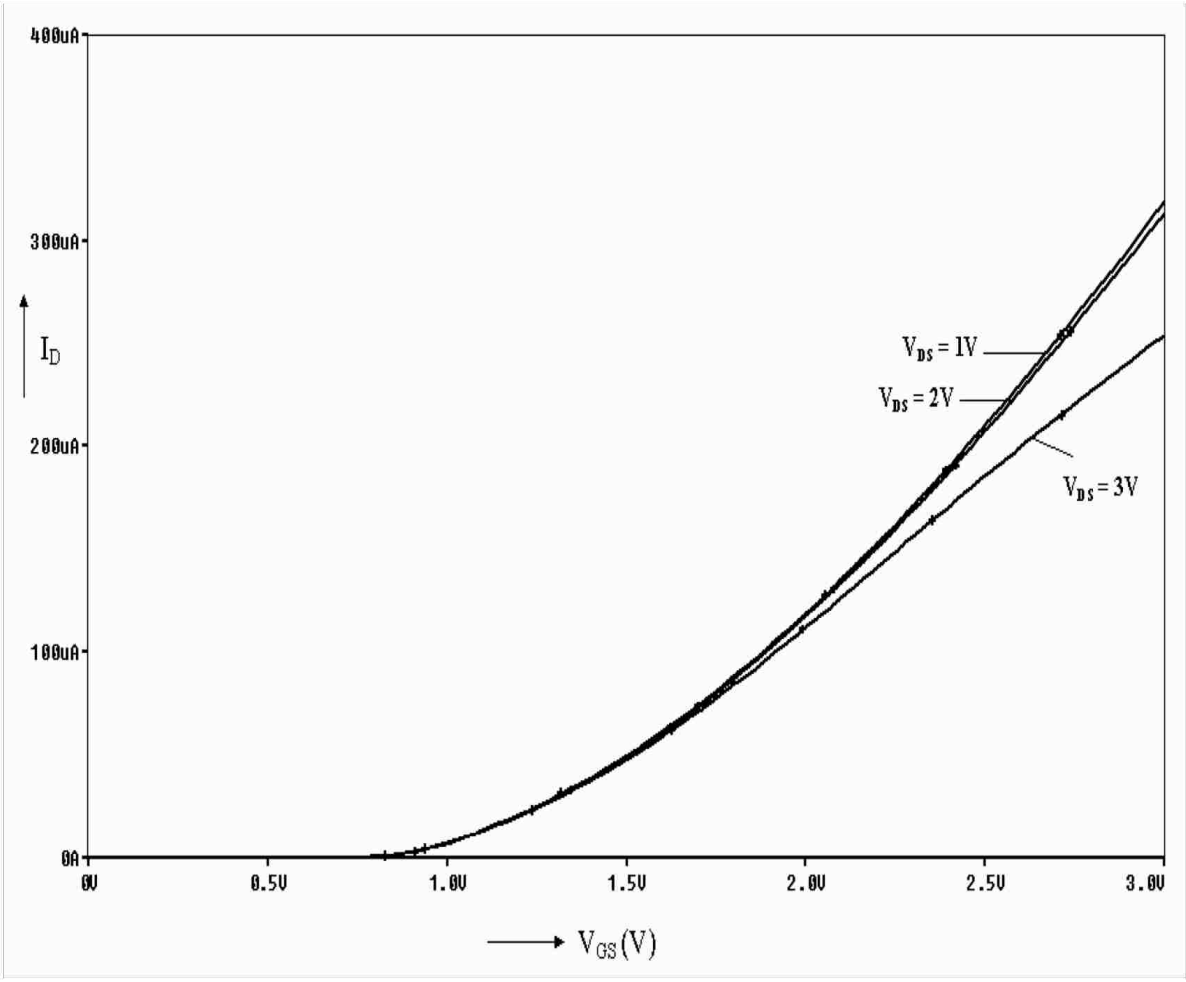

Figure 2.9:Transfer characteristics of a FGNMOS transistor.
Note: (W/ L= 4.2 µm /2.1 µm)

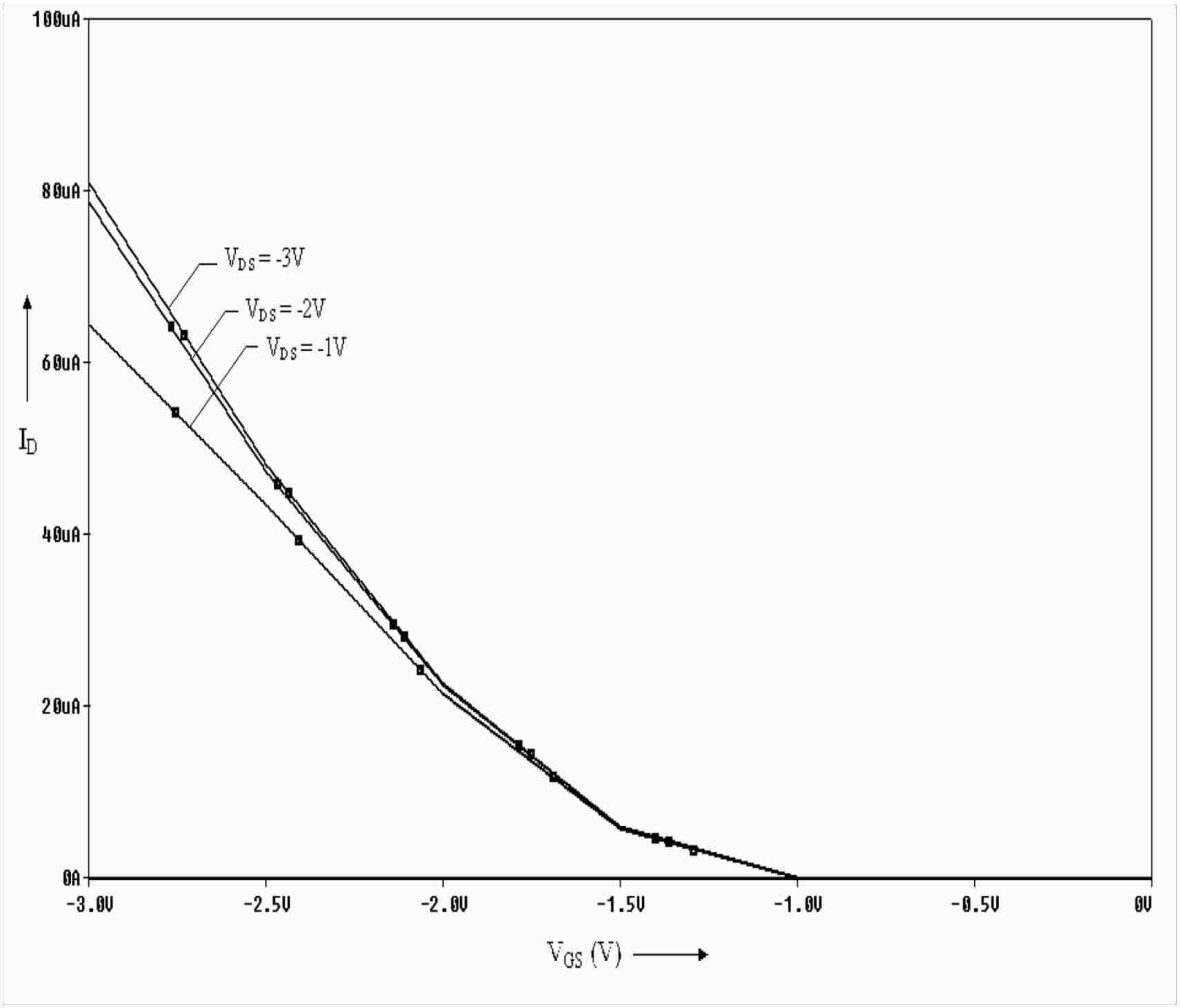

Figure 2.10:Transfer characteristics of a FGPMOS transistor. Note: (W/ L= 4.2 µm /2.1 µm)

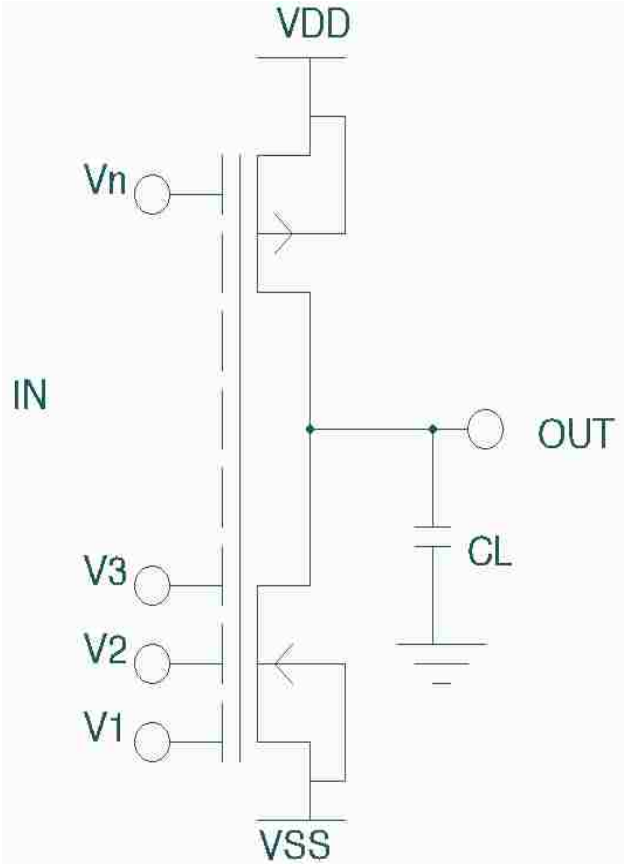

Figure 2.11: MIFG CMOS inverter.

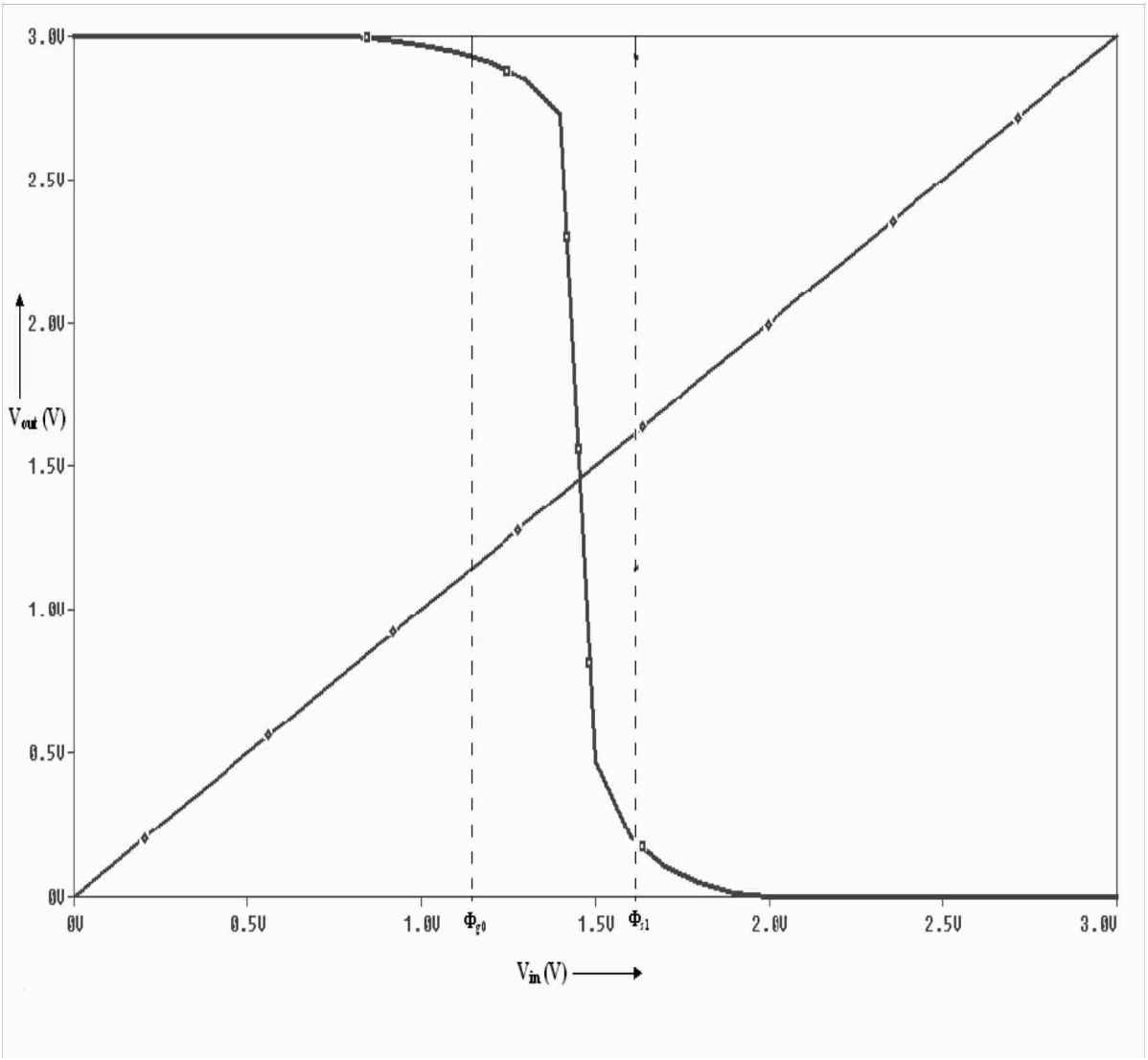

Figure 2.12: Transfer characteristics of a floating gate CMOS inverter. Note: $(W/L)_p$ = 20.28 µm /2.1 µm and $(W/L)_n$ = 4.2 µm /2.1 µm .

There are different technologies available for the implementation of capacitors. We will now look into the implementation of capacitors for the floating gate MOSFETS. A top view of parallel plate capacitor is shown in Fig. 2.14. The value of capacitance excluding the parasitic capacitances is given by,

$$C = AC' \tag{2.15}$$

where A is the total area of top plate of the capacitor and C' is capacitance per unit area of the capacitor. The oxide between the parallel plates of the capacitor in standard CMOS process is usually thicker than the gate oxide in the MOS transistor. There are several ways in which capacitors can be implemented. A popular technology used is the double-polysilicon CMOS technology in which two poly levels are available. The top plate and the bottom plate of the capacitor are made of polysilicon. In a single polysilicon technology, the top plate of the capacitor is made of metal. A high quality thin oxide is formed as an insulator before the top plate is formed.

There are two parasitic capacitances associated with the main capacitor as shown in Fig. 2.15 [5, 20]. The main parasitic capacitance CP1 is between the bottom plate and the substrate. It contributes most to the parasitic capacitance. The capacitance due to wiring of the bottom plate augments this capacitance. The metal wiring used to contact the top plate results in second small parasitic capacitance, CP2. Another parasitic is the resistance, RP of the polysilicon plate. This parasitic is ignored except at high frequencies. The capacitors in Fig. 2.15 are susceptible to interference. Any noise signal on substrate can be coupled to the capacitor through the parasitic capacitances. Also, any voltage variation on the bottom plate of the capacitor can be coupled to the substrate and through that to other components on the chip. Hence if the capacitor is too large, then it should be shielded from the substrate by an n-well under it, which is connected to a dc potential (VDD).

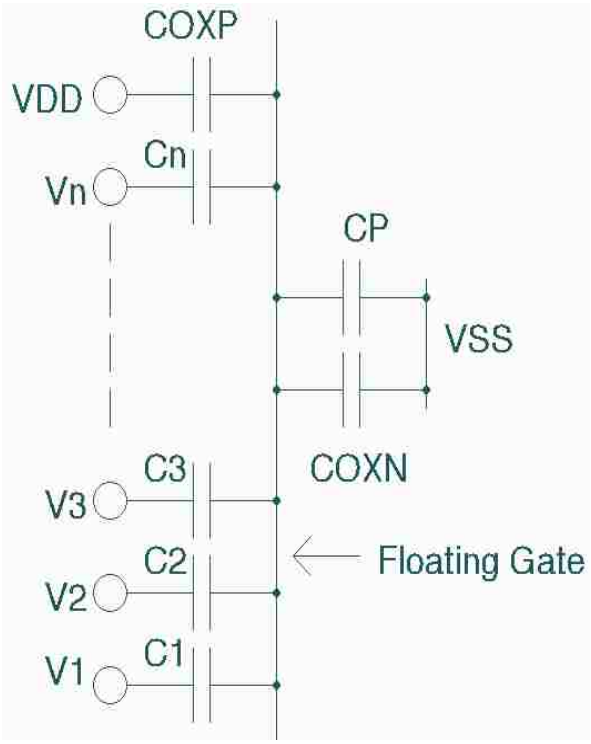

Figure 2.13: Capacitor network formed for a MIFG CMOS inverter.

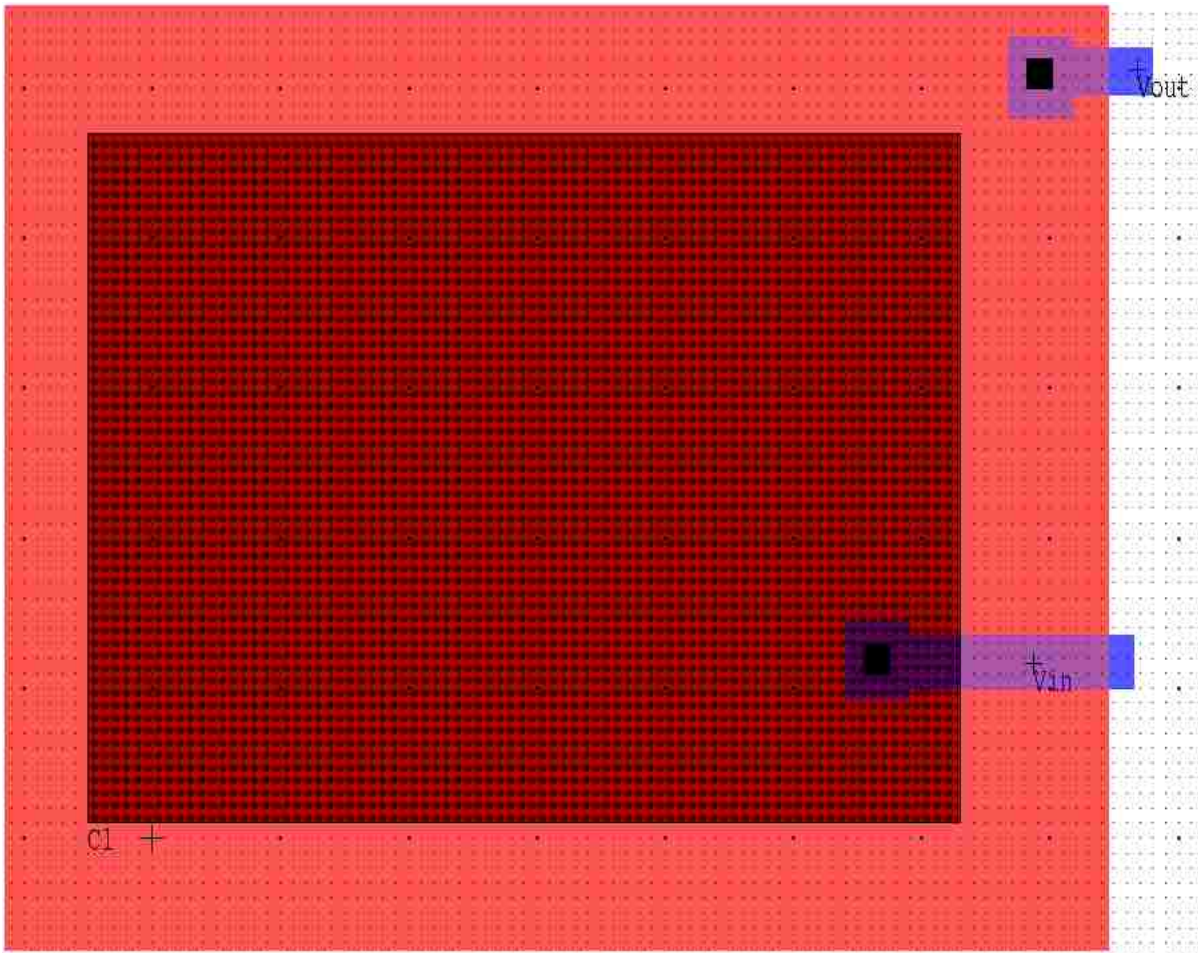

Figure 2.14: Layout of a 250µF capacitor.

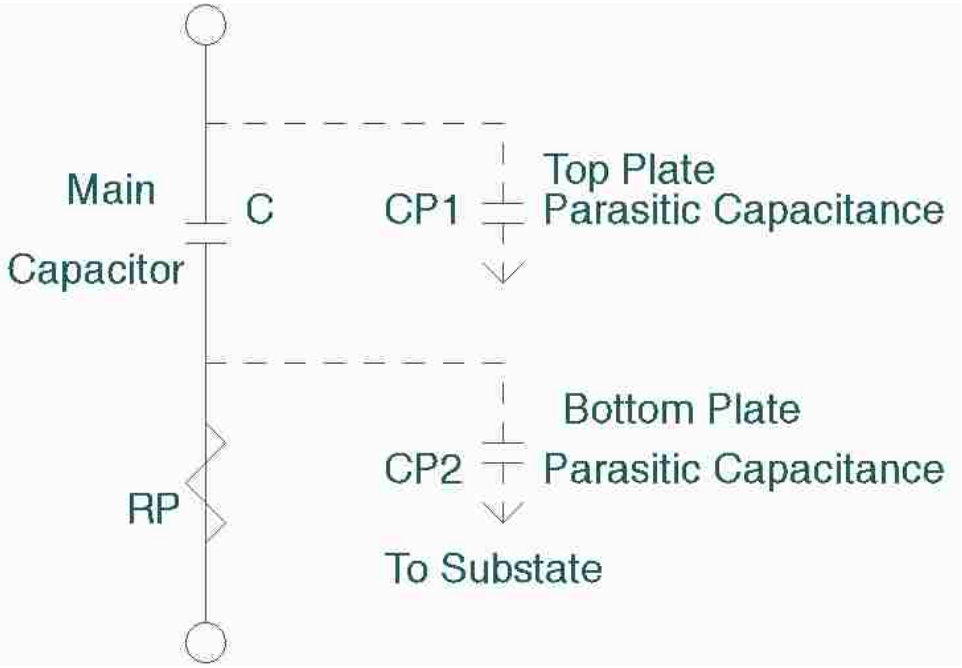

Figure 2.15: A capacitor with its associated parasitics.

2.7 Design Considerations

Floating gate CMOS inverters can give degraded outputs for some set of inputs. The output from the inverter therefore needs to be buffered to generate full logic voltage swing. Simulation of floating gate devices with standard CMOS models provided by the manufacturer requires new simulation techniques. The major problem of simulating floating-gate devices is the inability of the simulator to converge floating nodes. To avoid the problem of floating nodes at the gate of a transistor, different techniques include use of additional networks like resistors and voltage controlled voltage sources (VCVS) for establishing initial floating-gate voltage value.

CHAPTER 3. DESIGN OF TERNARY TO BINARY CONVERTER

3.1 Overview

The balanced ternary logic is expressed as (-1,0,1). In a standard 3V CMOS process, the logic -1, 0, 1 is defined as -3V, 0V, 3V, respectively. The benefits of using ternary logic system are explained in Chapter 1. In spite of these benefits, ternary logic system has not gained importance in the area of integrated circuit design. This is due to lack of efficient interfacing circuits with binary logic. Hence an attempt to design an interface circuit from ternary logic to binary logic has been made. The circuits are designed using multiple input floating gate MOS transistors.

The basic structure and operation of floating gate MOSFETS is explained in Chapter 2. Table 3.1 shows the ternary logic representing the decimal numbers ranging from -4 to +4 and its corresponding binary bits. The conversion of ternary to binary logic for corresponding decimal number is shown using an example. Consider a decimal number "-2", for which the corresponding binary bits are $(1010)_2$. The left most bit is the sign bit, which is "1" represents the number is negative and next three bits "010" represents "2". For the decimal number "-2", the corresponding ternary bits are $(-1,1)_3$. The conversion from ternary logic to decimal number is given by,

$$(-1\times3^1) + (1\times3^0) = (-3) + (1) = -2. \quad (3.1)$$

The remaining ternary to binary bit conversion corresponding different decimal numbers is obtained by similar calculation. This chapter explains design for the conversion circuits from ternary logic to binary logic. The circuit block has two ternary logic inputs (MSB and LSB) and four binary logic outputs, a sign bit (SB), a most significant bit (MSB), a second significant bit (SSB) and a least significant bit (LSB). The design of SB, MSB, SSB and LSB are explained in separate sections.

Table 3.1: Ternary to binary bits. Note: Ternary bit representation is $(MSB, LSB)_3$, Binary bit representation is $(Sign\ bit, MSB, SSB, LSB)_2$.

Decimal	Ternary	Binary
-4	$(-1-1)_3$	$(1100)_2$
-3	$(-10)_3$	$(1011)_2$
-2	$(-11)_3$	$(1010)_2$
-1	$(0-1)_3$	$(1001)_2$
0	$(00)_3$	$(0000)_2$
+1	$(01)_3$	$(0001)_2$
+2	$(1-1)_3$	$(0010)_2$
+3	$(10)_3$	$(0011)_2$
+4	$(11)_3$	$(0100)_2$

3.2 Sign Bit Circuit Design

The procedure for designing circuits using floating gate devices is shown in Chapter 2. The circuits are designed for 0.5 μm n-well CMOS VLSI technology. The switching threshold voltage ΦT is found first from the voltage transfer characteristics of the inverter as explained in Chapter 2. The threshold voltage (ΦT) of a standard CMOS inverter with $(W/L)_p$ = (20.28 μm /2.1 μm) and $(W/L)_n$= (4.2 μm /2.1 μm) was shown in Fig. 2.14 to be 1.33 V.

The next step is to draw the floating gate potential diagram. The ON and OFF states of the floating gate CMOS inverter are solely determined by the potential on the floating gate. For this we represent the floating gate voltage, ΦF as a function of the multiple gate input voltages and analyze the variation of the floating gate voltage with the input voltages. Such a representation is called a floating gate point diagram [FPD] [20]. From Table 3.1 the sign bit is logic HIGH (3V) for inputs. $(-1,-1)_3$ to $(0,-1)_3$ and logic LOW (0V) for inputs $(0,0)_3$ to $(1,1)_3$. Hence the voltage on floating gate ΦF of inverter should be below switching voltage ΦT for inputs $(-1,-1)_3$ to $(0,-1)_3$ and above the switching voltage for inputs $(0,0)_3$ to $(1,1)_3$. The FPD for the sign bit is shown in Fig. 3.1.The switching threshold line is marked in the figure. The circuit is then realized with two input capacitors C2 and C3 controlled by the two ternary inputs VA and VB. The sizes of the capacitors are set to 3:1 according to the weights of MSB and LSB in ternary bits. Using Eq. (2.14) for inputs $(-1,-1)_3$ to $(0,-1)_3$,

$$\Phi F = \frac{VA \times C2 + VB \times C3 + VDD \times COXP}{C2 + C3 + COXP + COXN + CP} < \Phi T(1.33V) \tag{3.2}$$

and for inputs $(0,0)_3$ to $(1,1)_3$,

$$\Phi F = \frac{VA \times C2 + VB \times C3 + VDD \times COXP}{C2 + C3 + COXP + COXN + CP} > \Phi T(1.33V) \tag{3.3}$$

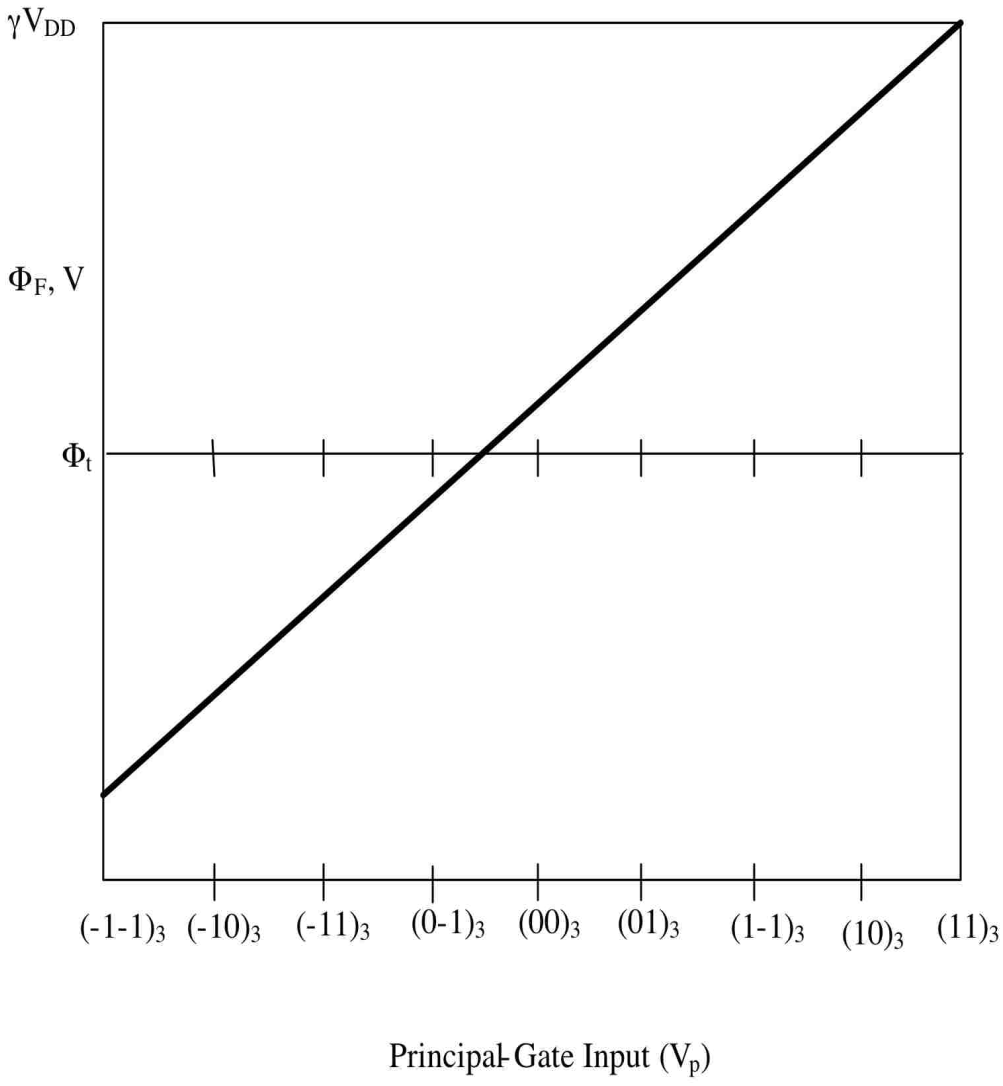

Figure 3.1: Floating gate potential diagram for the sign bit.

In Eq. (3.3), COXN and COXP are the gate oxide capacitance (COX) of NMOS and PMOS transistors, respectively of the inverter and CP is the parasitic capacitance due to capacitors C1 and C2. The gate oxide capacitance COX is given by,

$$COX = \frac{\varepsilon o \varepsilon sio_2}{tox} \times (WL) \tag{3.4}$$

where W and L are width and length of the transistors, εo (8.854 × 10-8 F/cm) is the permittivity of free space, εsio_2 is the permittivity of silicon dioxide and tox is the thickness of gate oxide. The thickness of gate oxide is obtained from model parameters given by MOSIS and is 142 Å. For $(W/L)_p$ = 20.28 μm/2.1 μm and $(W/L)_n$ = 4.2 μm/2.1 μm, using Eq. (3.4), COX of PMOS and NMOS transistors is given by,

$$COXP = \frac{8.854 \times 10^{-12} \times 3.8}{142 \times 10^{-10}} \times \left(20.28 \times 10^{-6} \times 2.1 \times 10^{-6}\right) = 100.9\,fF \tag{3.5}$$

$$COXN = \frac{8.854 \times 10^{-12} \times 3.8}{142 \times 10^{-10}} \times \left(4.2 \times 10^{-6} \times 2.1 \times 10^{-6}\right) = 20.9\,fF \tag{3.6}$$

For input $(0,0)_3$, the inequality (3.3) will not hold good. It is observed that the numerator on LHS ($0V \times C2 + 0V \times C3 + VDD \times COXP$) is negligible when compared to RHS (1.33V) of the inequality.

A solution to this is obtained by introducing a third capacitor, C1 which is connected to supply voltage (VDD) equal to 3V. The size of capacitor C1 is designed such that the voltage on floating gate is greater than switching threshold voltage of the inverter for inputs $(0,0)_3$. The inequality (3.3) is therefore rewritten as,

$$\Phi F = \frac{VA \times C2 + VB \times C3 + 3V \times C1 + 3V \times COXP}{C2 + C3 + COXP + COXN + CP} > \Phi T(1.33V) \tag{3.7}$$

In our design, the smallest value of the capacitor, C that can be chosen is 250fF. The capacitors, C2 and C3 are chosen in the ratio of 3:1. Their corresponding values are therefore chosen as 750fF and 250fF, respectively.

The value of CP is calculated using equation,

$$CP = K \times CP1 \tag{3.8}$$

In Eq.(3.8),CP1 is parasitic capacitance generated due to smallest capacitance "C" (250fF) which is C3 is this case is used. CP1 is found to be 43.5fF from layout extraction and K is given by,

$$K = \frac{C1 + C2 + C3}{C} \tag{3.9}$$

Substituting C3 as C and C2 equal to 3C in Eq. (3.8),

$$K = \frac{3C + C + C3}{C} = 4 + \frac{C3}{C} \tag{3.10}$$

Substituting the value of K, CP is calculated as,

$$CP = 4 + \frac{C3}{250\,fF} \times 43.5\,fF \tag{3.11}$$

Substituting values for input $(0,0)_3$, COXN, COXP, CP in inequality (3.7) we obtain,

$$\Phi F = \frac{0V \times 750\,fF + 0V \times 250\,fF + 3V \times C1 + 3V \times 100.9\,fF}{C2 + C3 + COXP + COXN + CP} > \Phi T(1.33V) \tag{3.12}$$

The smallest value of C1 that satisfies the inequality (3.12) is found to be 1350fF. Substituting the value of C1 in Eq. (3.11) value of CP is found to be 408.9fF. To verify the design, the voltage corresponding to different ternary inputs along with the capacitor values are substituted and the result is tabulated in Table 3.2.

For example for ternary input $(-1,-1)_3$ equation (3.7) is written as,

$$\Phi F = \frac{(-3V) \times 750\,fF + (-3V) \times 250\,fF + 3V \times 1350\,fF + 3V \times 100.9\,fF}{750\,fF + 250\,fF + 1350\,fF + 100.9\,fF + 20.9\,fF + 408.9\,fF} \tag{3.13}$$

The calculated ΦF from Eq. 3.13 should be less than ΦT in order for binary sign bit equivalent at the output of the floating gate inverter to be HIGH. The circuit for sign bit can hence be realized with three capacitors (C1, C2 and C3) as shown in Fig. 3.2. The output of this inverter (VODSB) is given as input to a buffer and the final buffered sign bit output (VODSBB) is obtained.

3.3 MSB Circuit Design

The most significant bit as seen in Table 3.1 is found to be logic HIGH (3V) for the inputs $(-1,-1)_3$ and $(1,1)_3$ and logic LOW (0V) for rest of inputs. The floating gate potential diagram (FPD) for the MSB is shown in Fig. 3.3. The potential on floating gate is below switching threshold voltage ΦT for inputs $(-1,-1)_3$, $(1,1)_3$ and above switching threshold voltage for inputs $(-1,0)_3$ to $(1,0)_3$. Fig. 3.4 shows the circuit design for the MSB. Voltage on floating gate falls below switching threshold voltage once; hence one pre-input gate inverter stage #2 is required to control voltage on floating gate of the main transistor inverter stage #3. Hence the main inverter stage #3 has three input capacitors C6, C7 and C8. The capacitors C7 and C8 are controlled by ternary inputs VA and VB, respectively and capacitor C6 is controlled by the output V11 of the pre-input gate inverter stage #2.

3.3.1 Circuit Design for Main Inverter Stage #3

As described above, the main inverter stage has three input capacitors of which capacitors C7 and C8 are controlled by ternary inputs VA and VB, respectively and capacitor C6 is controlled by the output V11 stage #2. The PMOS and NMOS transistors used in the MSB circuit design have a W/L ratio of $(W/L)_p$=30.15 μm/2.1 μm and $(W/L)_n$=4.2 μm/2.1 μm and has a threshold voltage ΦT=1.5795V. The gate oxide capacitances of PMOS and NMOS transistors of the MSB bit are given as COXP and COXN and are calculated using Eqs. (3.4, 3.5 and 3.6) as shown in Eqs, (3.14 and 3.15).

The values of COXP and COXN are calculated as,

$$COXP = \frac{8.854 \times 10^{-12} \times 3.8}{142 \times 10^{-10}} \times \left(30.15 \times 10^{-6} \times 2.1 \times 10^{-6}\right) = 150\,fF \tag{3.14}$$

$$COXN = \frac{8.854 \times 10^{-12} \times 3.8}{142 \times 10^{-10}} \times \left(4.2 \times 10^{-6} \times 2.1 \times 10^{-6}\right) = 20.9\,fF \tag{3.15}$$

Table 3.2: Floating gate voltage for the sign bit.

Ternary Inputs	Voltage on Floating Gate of Stage #1 Inverter (Φ_F) in V	Floating Gate Voltage of the Transistor of Stage #1
$(-1,-1)_3$	0.4695	$\Phi_F < \Phi_t$
$(-1,0)_3$	0.723	$\Phi_F < \Phi_t$
$(-1,1)_3$	0.99	$\Phi_F < \Phi_t$
$(0,-1)_3$	1.25	$\Phi_F < \Phi_t$
$(0,0)_3$	1.51	$\Phi_F > \Phi_t$
$(0,1)_3$	1.77	$\Phi_F > \Phi_t$
$(1,-1)_3$	2.03	$\Phi_F > \Phi_t$
$(1,0)_3$	2.23	$\Phi_F > \Phi_t$
$(1,1)_3$	2.55	$\Phi_F > \Phi_t$

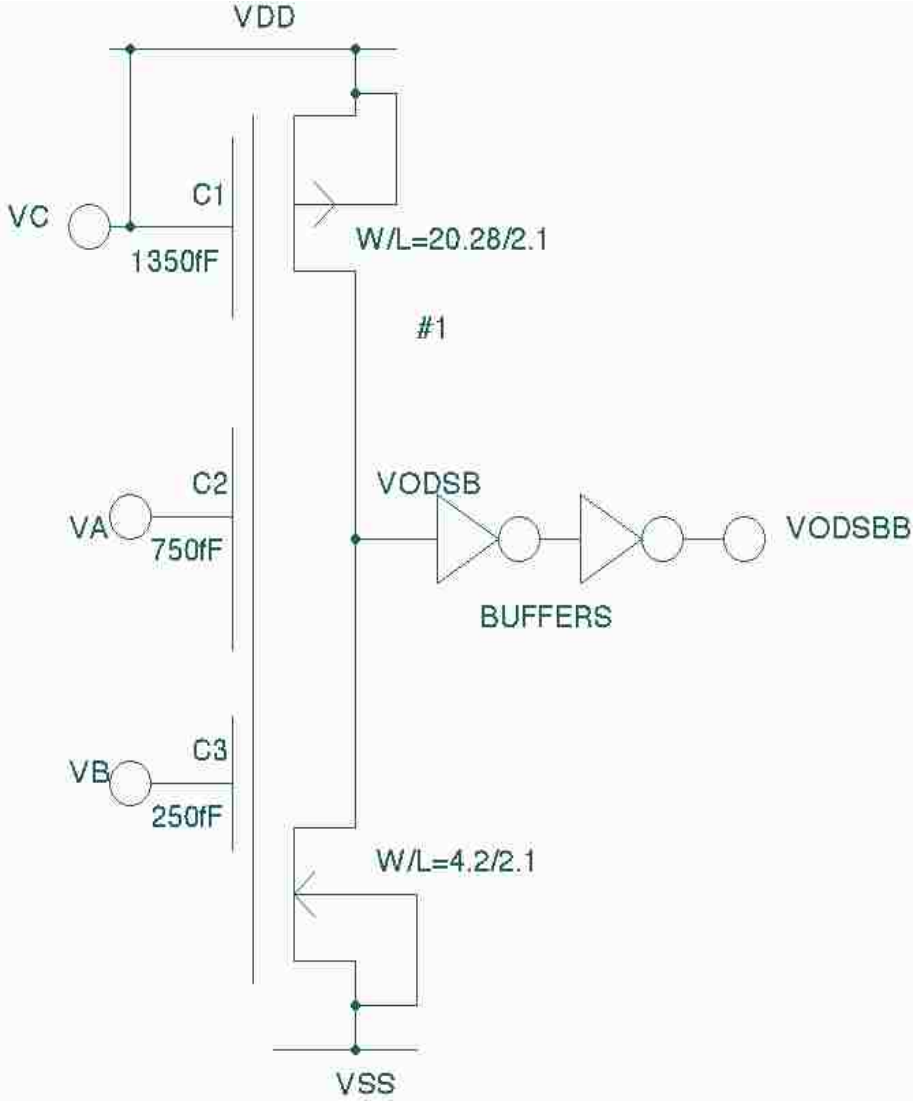

Figure 3.2: Circuit for sign bit.

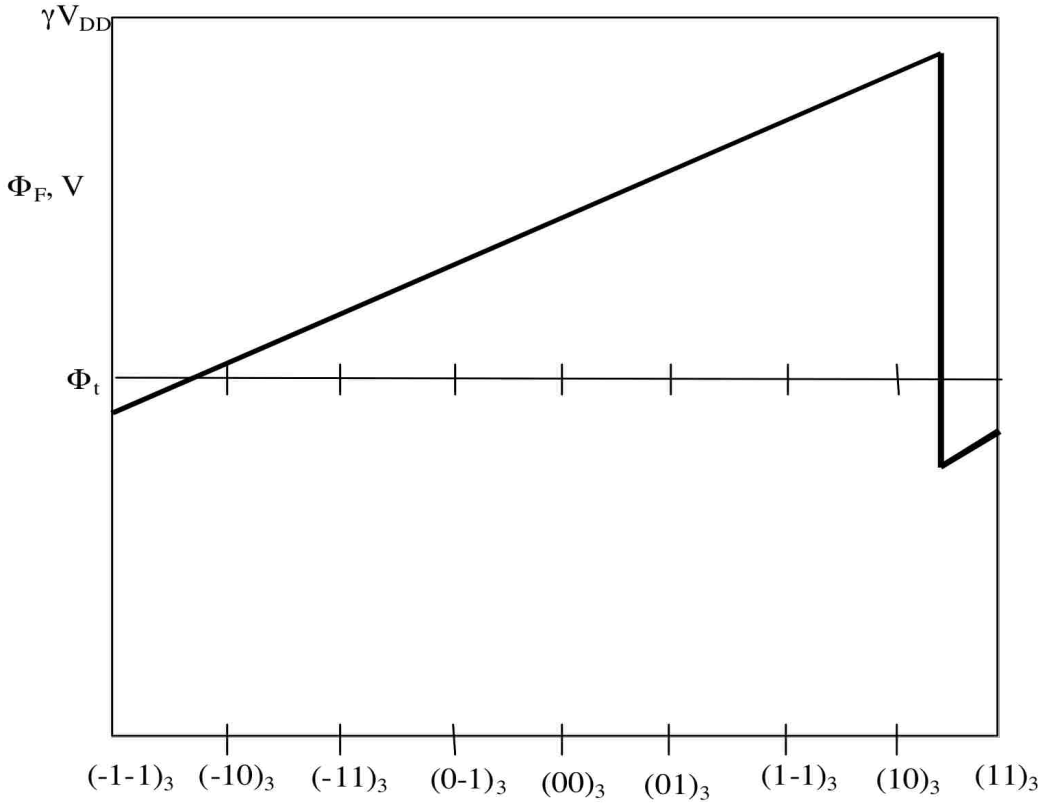

Figure 3.3: Floating gate potential diagram for the MSB.

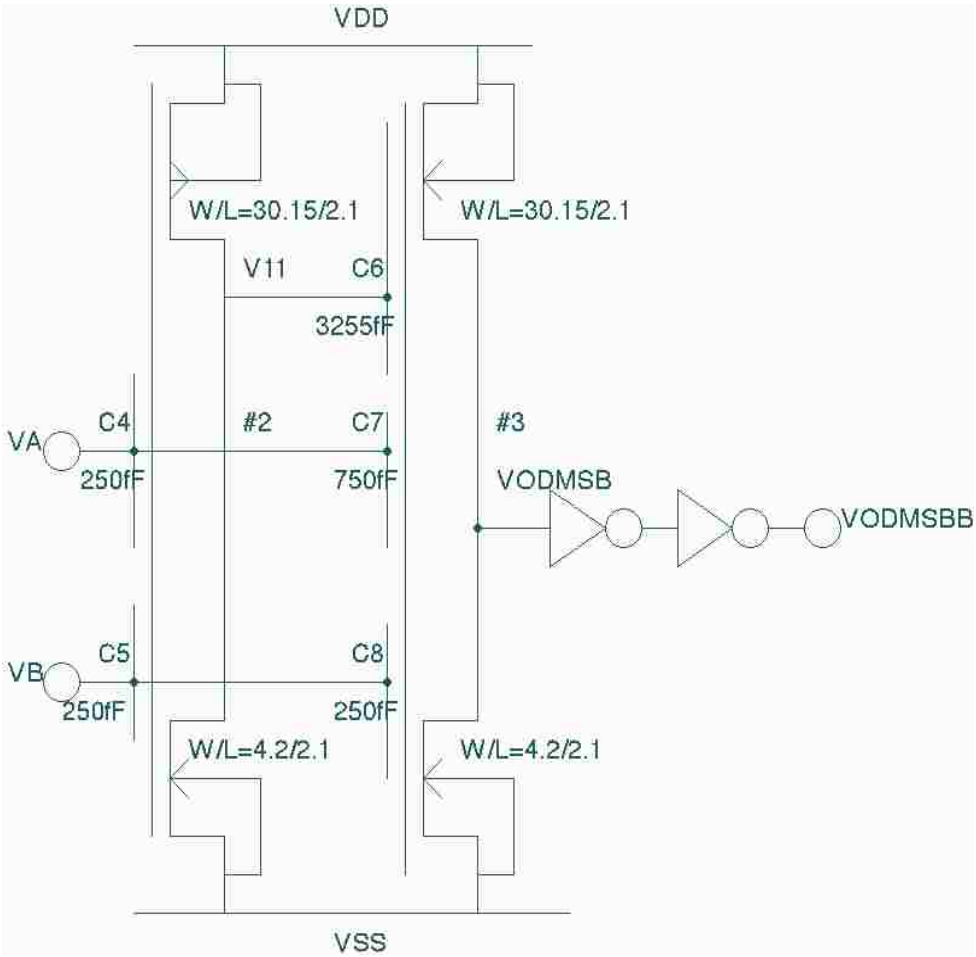

Figure 3.4: Circuit for MSB.

The value of CP is now calculated from C7 and C8. Setting C7 and C8 in the ratio of 3:1 as 750fF and C8 as 250fF, respectively, the value of CP can be calculated using Eqns. (3.8, 3.9, 3.10, 3.11) as

$$CP = 4 + \frac{C6}{250\,fF} \times 43.5\,fF \tag{3.16}$$

Using Eq. (3.6), the inequalities for the third stage which also gives the MSB output for different inputs, can be written as follows:

For inputs $(-1,-1)_3$ and $(1,1)_3$ as seen from Table 3.1,

$$\Phi F = \frac{VA \times 750\,fF + VB \times 250\,fF + V11 \times C6 + 3V \times 150\,fF}{750\,fF + 250\,fF + C6 + 150\,fF + 20.9\,fF + CP} < \Phi T(1.5795V) \tag{3.17}$$

For input $(-1,-1)_3$, the inequality equation (3.15) can be written as,

$$\Phi F = \frac{(-3V) \times 750\,fF + (-3V) \times 250\,fF + V11 \times C6 + 3V \times COXP}{750\,fF + 250\,fF + C6 + COXP + COXN + CP} < \Phi T(1.5795V) \tag{3.18}$$

For input $(1,1)_3$, the inequality (3.16) can be written as,

$$\Phi F = \frac{(3V) \times 750\,fF + (3V) \times 250\,fF + V11 \times C6 + 3V \times COXP}{750\,fF + 250\,fF + C6 + COXP + COXN + CP} < \Phi T(1.5795V) \tag{3.19}$$

In Eqns. (3.17, 3.18 and 3.19), V11 is the output voltage of Stage #2. The inequality (3.18) can be satisfied only if V11 is LOW (0V) for input $(1,1)_3$. Hence the output of pre-input inverter stage #2 is LOW (0V) for input $(1,1)_3$ and HIGH (3V) for rest of the inputs. For the inputs from $(-1,0)_3$ to $(1,0)_3$, voltage on the floating gate should be greater than switching threshold voltage. Hence for these inputs, the Eq. (3.6) can be written as,

$$\Phi F = \frac{VA \times 750\,fF + VB \times 250\,fF + V11 \times C6 + 3V \times 150\,fF}{750\,fF + 250\,fF + C6 + 150\,fF + 20.9\,fF + CP} > \Phi T(1.5795V) \tag{3.20}$$

where CP is defined in terms of C6 in Eq. (3.16). The smallest value of C6 that satisfies the above inequalities represented by Eq. (3.17) and Eq. (3.20) is found by iteration to be 3255fF.

Substituting this value in Eq. (3.16) the value of CP is found to be,

$$CP = 4 + \frac{3255\,fF}{250\,fF} \times 43.5\,fF = 740.37\,fF \tag{3.21}$$

To verify the design, the voltage corresponding to different ternary inputs are substituted and the results are tabulated in Table 3.3.

3.3.2 Circuit Design for Stage #2

The pre-input stage is the stage whose output is fed into the input of the last stage, which is Stage #3 of the MSB circuit. As discussed in Section 3.3.1, for the Stage #3 of the MSB circuit to work as it is designed to work, the output of Stage #2 should be LOW (0V) for the input $(1,1)_3$ and HIGH (3V) for the rest of the inputs .The pre input inverter stage is designed to deliver these outputs.

The circuit can be realized with two input capacitors C4 and C5 into which are fed the inputs VA and VB. The transistors used for this stage are the same as that used for Stage #3 and hence have the same W/L ratios and threshold voltage. The values of COXP and COXN are hence the same as that of Eqs. (3.14 and 3.15) of Stage #3 and are given as 150fF and 20.9fF respectively. The values of C4 and C5 are chosen by iteration to be 250fF for this stage, CP can be therefore be calculated using Eqs. (3.8 and 3.9) in Eq. (3.22).

$$CP = \frac{C4 + C5}{C} \times CP = \frac{2C}{C} \times CP1 = 2 \times 43.5 = 87\,fF \tag{3.22}$$

For input $(1,1)_3$, the inequality is written using Eq. (2.14), as,

$$\Phi F = \frac{3V \times C4 + 3V \times C5 + VDD \times COXP}{C4 + C5 + COXP + COXN + CP} > \Phi T(1.5795V) \tag{3.23}$$

and for the rest of the inputs, the inequality is given as,

$$\Phi F = \frac{3V \times C4 + 3V \times C5 + VDD \times COXP}{C4 + C5 + COXP + COXN + CP} < \Phi T(1.5795V) \tag{3.24}$$

Table 3.3: Floating gate voltage for the final Stage #3 of the MSB.

Ternary Inputs	Output of Stage #2 (V_{11})	Voltage on Floating Gate of Stage #3 (Φ_F) in V	Floating Gate Voltage of the Transistor of the Stage# 3
$(-1,-1)_3$	HIGH	1.396	$\Phi_F < \Phi_t$
$(-1,0)_3$	HIGH	1.5817	$\Phi_F > \Phi_t$
$(-1,1)_3$	HIGH	1.832	$\Phi_F > \Phi_t$
$(0,-1)_3$	HIGH	1.690	$\Phi_F > \Phi_t$
$(0,0)_3$	HIGH	1.977	$\Phi_F > \Phi_t$
$(0,1)_3$	HIGH	2.122	$\Phi_F > \Phi_t$
$(1,-1)_3$	HIGH	2.2676	$\Phi_F > \Phi_t$
$(1,0)_3$	HIGH	2.412	$\Phi_F > \Phi_t$
$(1,1)_3$	LOW	0.667	$\Phi_F < \Phi_t$

Substituting the values of COXP, COXN and CP in the above two inequalities we can calculate the values of ΦF which have been tabulated in Table 3.4. The complete circuit of the MSB stage is shown in Fig. 3.4.

3.4 SSB Circuit Design

It can be seen from Table 3.1 that the output of second significant bit (SSB) is logic LOW (0V) for inputs $(-1,-1)_3$, $(1,1)_3$ and from inputs $(0,-1)_3$ to $(0,1)_3$ and is logic HIGH (3V) for rest of the inputs. The FPD for the SSB is shown in Fig. 3.5, the voltage on floating gate is below switching threshold voltage, ΦT for inputs $(-1,-1)_3$, $(1,1)_3$ and inputs $(0,-1)_3$ to $(0,1)_3$. That is voltage on floating gate falls below switching threshold voltage twice and hence two pre-input gate inverter Stages (#4, #5) are required to control the main inverter stage as shown in Fig. 3.6.

The main inverter Stage #6 has four input capacitors C14, C15, C16 and C17. The capacitors C15 and C17 are controlled by two ternary inputs VA and VB, respectively. The capacitors C14 and C16 are controlled by output of pre-input inverter stages V12 of Stage #4 and V13 of Stage #5, respectively. The output of the pre-input inverter Stage #4 needs to go to LOW (0 V) from inputs $(0,-1)_3$ to $(1,1)_3$ and the output of the pre-input gate inverter Stage #5 should go LOW (0V) for input $(1,1)_3$ in order for the last stage to give the output that is required.

3.4.1 Circuit Design for Main Inverter Stage #6

The transistor used in Stage #6 has a W/L ratio of $(W/L)_p$=50.4μm /2.1μm for PMOS transistor and $(W/L)_n$=4.2μm /2.1μm for NMOS transistor and has a threshold voltage ΦT=1.6012V. The gate oxide capacitances are thus calculated to be,

$$COXP = \frac{8.854\times10^{-12}\times3.8}{142\times10^{-10}}\times\left(50.4\times10^{-6}\times2.1\times10^{-6}\right) = 250.8\,fF \tag{3.25}$$

$$COXN = \frac{8.854\times10^{-12}\times3.8}{142\times10^{-10}}\times\left(4.2\times10^{-6}\times2.1\times10^{-6}\right) = 20.9\,fF \tag{3.26}$$

Table 3.4: Floating gate voltage for the Stage #2 of the MSB.

Ternary Inputs	Voltage on Floating Gate of Stage #2 Inverter (Φ_F), V	Floating Gate Voltage of the Transistor of Stage #2
$(-1,-1)_3$	-1.385	$\Phi_F < \Phi_t$
$(-1,0)_3$	-0.395	$\Phi_F < \Phi_t$
$(-1,1)_3$	0.593	$\Phi_F < \Phi_t$
$(0,-1)_3$	-0.396	$\Phi_F < \Phi_t$
$(0,0)_3$	0.594	$\Phi_F < \Phi_t$
$(0,1)_3$	1.58	$\Phi_F < \Phi_t$
$(1,-1)_3$	0.594	$\Phi_F < \Phi_t$
$(1,0)_3$	1.483	$\Phi_F < \Phi_t$
$(1,1)_3$	2.573	$\Phi_F > \Phi_t$

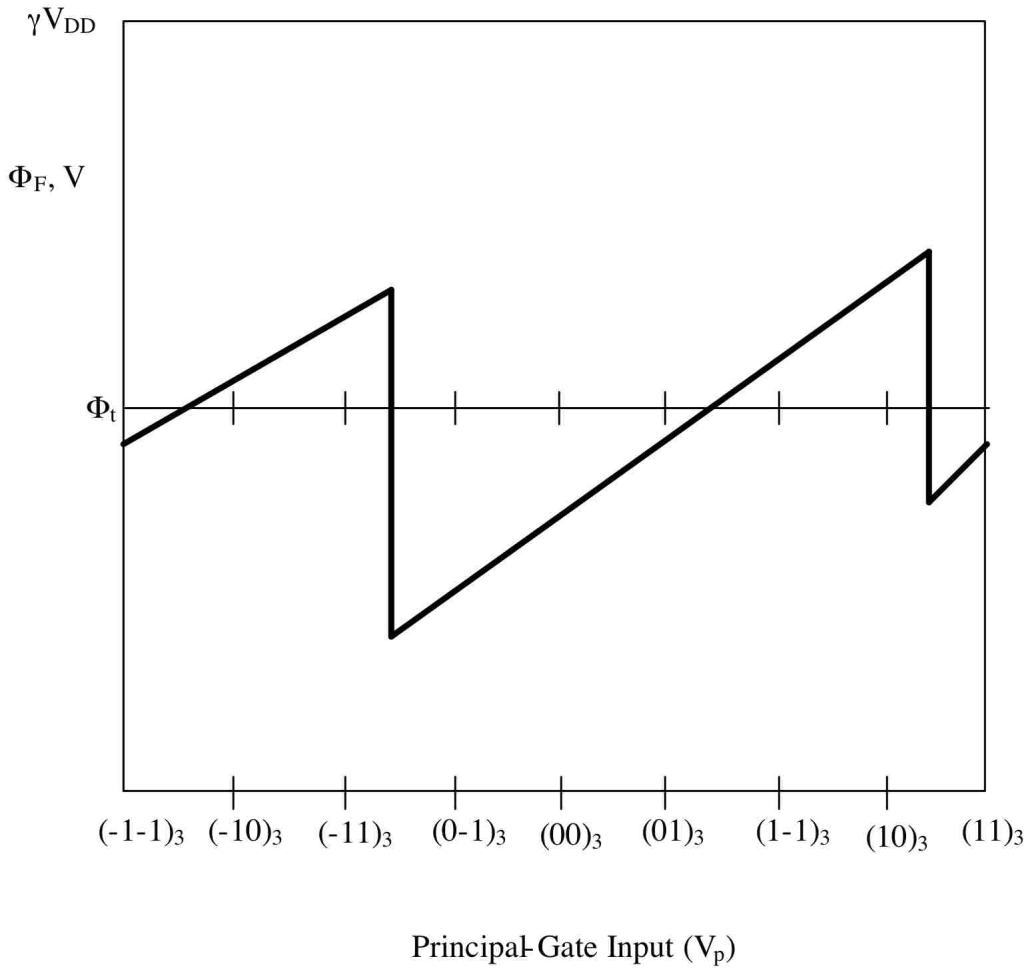

Figure 3.5: Floating gate potential diagram for the SSB.

The sizes of capacitors C16 and C17 are set to 2615fF and 250fF. CP can be calculated using Eqs. (3.8 and 3.9) as,

$$CP = \frac{C14 + C15 + C16 + C}{C} \times CP1 = \frac{C14 + C15 + 2615\,fF + 250\,fF}{250\,fF} \times 43.5 \tag{3.27}$$

For Stage #6, for the input $(-1,-1)_3$, the inequality (2.14) is given by,

$$\Phi F = \frac{VA \times 2615\,fF + VB \times 250\,fF + V12 \times C14 + V13 \times C15 + 3V \times COXP}{C14 + C15 + 2615\,fF + 250\,fF + COXP + COXN + CP} < \Phi T(1.6012V) \tag{3.28}$$

For inputs $(-1,0)_3$ and $(-1,1)_3$, the inequality is

$$\Phi F = \frac{VA \times 2615\,fF + VB \times 250\,fF + V12 \times C14 + V13 \times C15 + 3V \times COXP}{C14 + C15 + 2615\,fF + 250\,fF + COXP + COXN + CP} > \Phi T(1.6012V) \tag{3.29}$$

For the inputs in Eqs. (3.28 and 3.29), the value of V12 and V13 can be HIGH (3V) to satisfy the inequalities. For inputs $(0,-1)_3$ to $(0,1)_3$ the inequality is,

$$\Phi F = \frac{VA \times 2615\,fF + VB \times 250\,fF + V12 \times C14 + V13 \times C15 + 3V \times COXP}{C14 + C15 + 2615\,fF + 250\,fF + COXP + COXN + CP} < \Phi T(1.6012V) \tag{3.30}$$

For inputs $(1,-1)_3$ and $(1,0)_3$, the inequality is,

$$\Phi F = \frac{VA \times 2615\,fF + VB \times 250\,fF + V12 \times C14 + V13 \times C15 + 3V \times COXP}{C14 + C15 + 2615\,fF + 250\,fF + COXP + COXN + CP} < \Phi T(1.6012V) \tag{3.31}$$

For inequalities (3.30 and 3.31), V12 should be LOW (0V) and V13 can be HIGH (3V) to satisfy the inequalities. For input $(1,1)_3$ the inequality is,

$$\Phi F = \frac{VA \times 2615\,fF + VB \times 250\,fF + V12 \times C14 + V13 \times C15 + 3V \times COXP}{C14 + C15 + 2615\,fF + 250\,fF + COXP + COXN + CP} < \Phi T(1.6012V) \tag{3.32}$$

For the Eq. (3.32), both V12 and V13 need to be LOW (0V). The values of C14 and C15 that satisfy above inequalities (3.28 to 3.32) are found by iteration to be 6251fF and 4003fF, respectively. Substituting the value of C14 and C15 in Eq. (3.27), the value of CP is found to be 2282.7fF. After all the values have been substituted in the above inequalities (3.28 to 3.32), we can calculate the values of ΦF, which have been tabulated in Table 3.5.

The output of the circuit needs to be inverted to get the correct output. Hence a CMOS inverter is inserted at the output, which would invert and as well buffer the output. The width of the transistors used in the buffer is (W_p = 3/2.1μm, W_n = 1.5/2.1μm). The circuit diagram for this stage along with the other stages of the SSB circuit is shown in Figure. 3.6.

3.4.2 Circuit Design for Stage #5

As discussed in the previous section, The output (V13) of the pre-input inverter Stage #5 goes LOW (0V) from inputs $(0,-1)_3$ to $(1,1)_3$ and is HIGH (3V) for the rest of the inputs. The inverter Stage #5 can be designed with three input capacitors C11, C12 and C13. In Stage #5, the capacitors, C12 and C13 are controlled by ternary inputs VA and VB, respectively and capacitor C11 is connected to supply voltage VDD (3V).

Let us assume C12 and C13 to be 1250fF and 250fF. The transistor used for this stage has a W/L ratio of W_p/ L_p=41.73 μm /2.1 μm, W_n/ L_n= 6.6 μm /2.1 μm and a threshold voltage ΦT=1.5412 V. The gate oxide capacitances can therefore be calculated as,

$$COXP = \frac{8.854 \times 10^{-12} \times 3.8}{142 \times 10^{-10}} \times \left(41.3 \times 10^{-6} \times 2.1 \times 10^{-6}\right) = 207.6\,fF \tag{3.33}$$

$$COXN = \frac{8.854 \times 10^{-12} \times 3.8}{142 \times 10^{-10}} \times \left(6.6 \times 10^{-6} \times 2.1 \times 10^{-6}\right) = 32.8\,fF \tag{3.34}$$

The parasitic capacitance is given as,

$$CP = \frac{C11 + C12 + C}{C} \times CP1 = \frac{C11 + 1250\,fF + 250\,fF}{250\,fF} \times 43.5 \tag{3.35}$$

Using Eq. (2.14), for the inputs $(-1,-1)_3$ to $(-1,1)_3$,

$$\Phi F = \frac{VA \times C12 + VB \times C13 + C11 \times 3V + 3V \times COXP}{C12 + C13 + C11 + COXP + COXN + CP} < \Phi T(1.5412V) \tag{3.36}$$

Table 3.5: Floating gate voltage for the final Stage #6 of the SSB.

Ternary Inputs	Output of Stage #5 (V_{13})	Output of Stage #4 (V_{12})	Voltage on Floating Gate of Main Inverter (Φ_F) in V	Floating Gate Voltage of the Transistor of Stage #6	Floating Gate Voltage of the Inverter Following Stage #6
$(-1,-1)_3$	HIGH	HIGH	1.464	$\Phi_F < \Phi_t$	$\Phi_F > \Phi_t$
$(-1,0)_3$	HIGH	HIGH	1.619	$\Phi_F > \Phi_t$	$\Phi_F < \Phi_t$
$(-1,1)_3$	HIGH	HIGH	1.659	$\Phi_F > \Phi_t$	$\Phi_F < \Phi_t$
$(0,-1)_3$	LOW	HIGH	1.198	$\Phi_F < \Phi_t$	$\Phi_F > \Phi_t$
$(0,0)_3$	LOW	HIGH	1.246	$\Phi_F < \Phi_t$	$\Phi_F > \Phi_t$
$(0,1)_3$	LOW	HIGH	1.290	$\Phi_F < \Phi_t$	$\Phi_F > \Phi_t$
$(1,-1)_3$	LOW	HIGH	1.699	$\Phi_F > \Phi_t$	$\Phi_F < \Phi_t$
$(1,0)_3$	LOW	HIGH	1.747	$\Phi_F > \Phi_t$	$\Phi_F < \Phi_t$
$(1,1)_3$	LOW	LOW	0.597	$\Phi_F < \Phi_t$	$\Phi_F > \Phi_t$

For inputs from (0,-1)3 to (1,1)3, the inequality is,

$$\Phi F = \frac{VA \times C12 + VB \times C13 + C11 \times 3V + 3V \times COXP}{C12 + C13 + C11 + COXP + COXN + CP} > \Phi T(1.5412V) \quad (3.37)$$

Substituting the value of C12, C13, COXP, COXN in the above inequalities, the value of C11 can be found by iteration to be 3000fF. This value can now be substituted in Eq. (3.35) and value of CP is found to be 784.39fF. The circuit diagram for this stage along with the other SSB circuit stages is shown in Fig.3.6. The results from the above inequalities are tabulated in Table 3.6.

3.4.3 Circuit Design for Stage #4

The output of the pre-input gate inverter Stage (#4) is same as the output of pre-input gate inverter Stage #2 discussed in Section 3.3.2. Hence the output V11 of Stage #2 can be used to control the capacitor C14.

3.5 LSB Circuit Design

The least significant bit is designed on similar lines. The output of the LSB bit is HIGH (3V) for odd decimal numbers (-3, -1, 1, 3) and LOW (0V) for even decimal numbers (-4, -2, 0, 2, 4). From Table 3.1, the FPD for LSB is drawn and is shown in Figure 3.7. From FPD, the voltage on floating gate falls below switching threshold voltage four times, hence four pre-input inverter stages are normally used to control the voltage on floating gate. In this design, two pre-input inverter stages are the same and hence are represented by a single stage. Hence only three pre-input inverter stages will be discussed. Fig. 3.8 shows the circuit level design of LSB and the following sections discuss the design in detail.

3.5.1 Circuit Design for Main Inverter Stage #10

The main inverter stage has six input capacitors C26, C27, C28, C29, C30 and C31. The capacitors C30 and C31 are controlled by the inputs VA and VB, respectively and are taken as 500fF and 350fF respectively. The capacitors C26 and C27 are controlled by the outputs VIN17.

Table 3.6: Floating gate voltage for the Stage #5 of the SSB.

Ternary Inputs	Voltage on Floating Gate of Stage #5 Inverter (Φ_F), V	Floating Gate Voltage of the Transistor of Stage #5
$(-1,-1)_3$	1.396	$\Phi_F < \Phi_t$
$(-1,0)_3$	1.5420	$\Phi_F < \Phi_t$
$(-1,1)_3$	1.690	$\Phi_F < \Phi_t$
$(0,-1)_3$	1.832	$\Phi_F > \Phi_t$
$(0,0)_3$	1.977	$\Phi_F > \Phi_t$
$(0,1)_3$	2.122	$\Phi_F > \Phi_t$
$(1,-1)_3$	2.2676	$\Phi_F > \Phi_t$
$(1,0)_3$	2.412	$\Phi_F > \Phi_t$
$(1,1)_3$	0.667	$\Phi_F > \Phi_t$

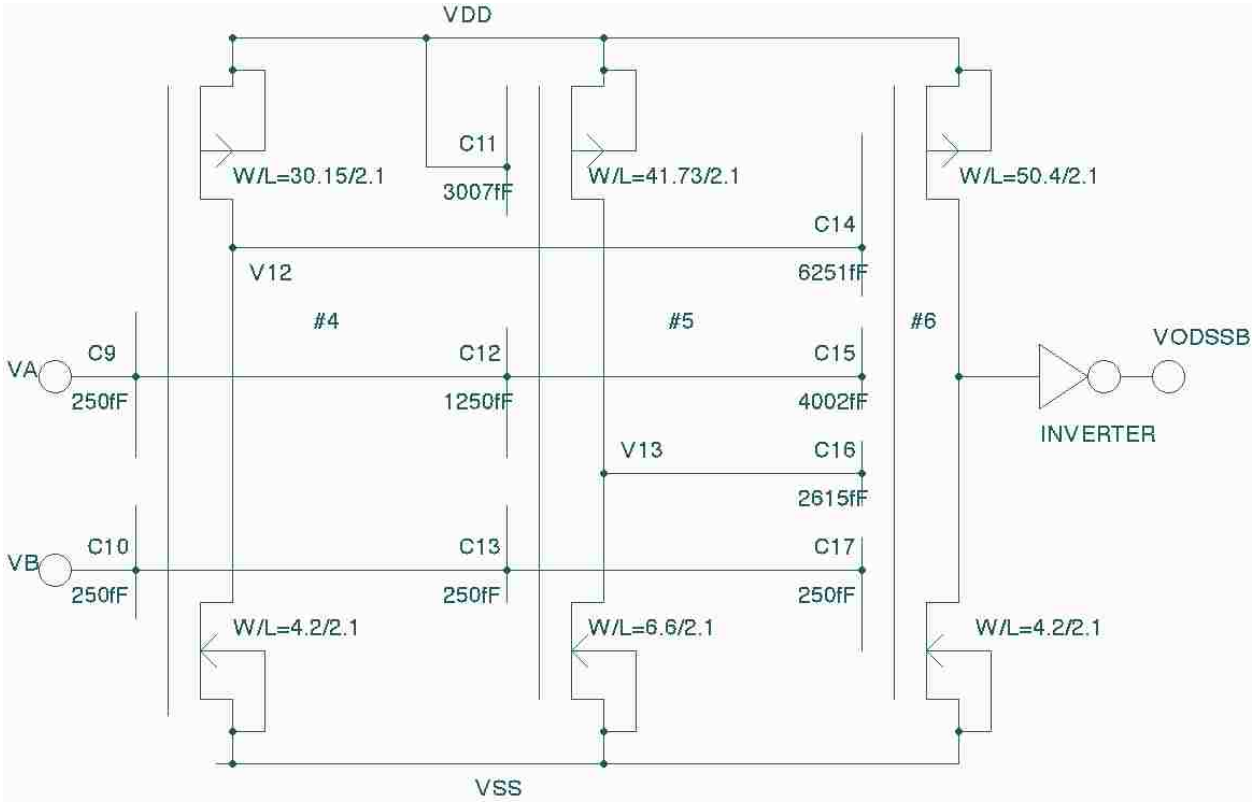

Figure 3.6: Circuit for SSB.

The capacitor C28 is controlled by VIN18 and capacitor C29 is controlled by VIN19 of the pre-input inverter Stages (#7, #8, #9), respectively. The output of pre-input gate inverter Stage #7 goes LOW (0 V) from input $(-1,1)_3$ to $(1,1)_3$, the output of Stage #8 goes LOW (0V) from inputs $(0,0)_3$ to $(1,1)_3$, the output of Stage #9 goes LOW (0V) from inputs $(1,-1)_3$ to $(1,1)_3$. The transistor used in the main inverter stage has a W/L ratio of W_p/ L_p =30.15 μm / 2.1μm and W_n/ L_n =13.2 μm / 2.1μm. The gate oxide capacitances are therefore,

$$COXP = \frac{8.854 \times 10^{-12} \times 3.8}{142 \times 10^{-10}} \times \left(30.15 \times 10^{-6} \times 2.1 \times 10^{-6}\right) = 150\,fF \tag{3.38}$$

$$COXN = \frac{8.854 \times 10^{-12} \times 3.8}{142 \times 10^{-10}} \times \left(13.2 \times 10^{-6} \times 2.1 \times 10^{-6}\right) = 68.6\,fF \tag{3.39}$$

The parasitic capacitance,

$$CP = \frac{C26 + C27 + C28 + C29 + C30 + C31}{C} \times CP1 \tag{3.40}$$

$$CP = \frac{C26 + C27 + C28 + C29 + 500\,fF + 350\,fF}{350\,fF} \times 43.5\,fF \tag{3.41}$$

Using Eq. (2.14), the voltage on floating gate ΦF of the main inverter stage is given by the equation,

$$\Phi F = \frac{VA \times C30 + VB \times C31 + C26 \times V14 + C27 \times V14 + V15 \times C28 + V16 \times C29 + 3V \times COXP}{C26 + C27 + C28 + C29 + C30 + C31 + COXP + COXN + CP} \tag{3.42}$$

For input $(-1,-1)_3$,

$$\Phi F = \frac{-3V \times 500\,fF + -3V \times 350\,fF + C26 \times 3V + C27 \times 3V + 3V \times C28 + 3V \times C29 + 3V \times 150\,fF}{C26 + C27 + C28 + C29 + 500\,fF + 350\,fF + 150\,fF + 68.6\,fF + 509.8\,fF}$$

Here, $\Phi_F < \Phi_t$ (1.4V) (3.43)

For input $(-1,0)_3$,

$$\Phi F = \frac{-3V \times 500\,fF + 0V \times 350\,fF + C26 \times 3V + C27 \times 3V + 3V \times C28 + 3V \times C29 + 3V \times 150\,fF}{C26 + C27 + C28 + C29 + 500\,fF + 350\,fF + 150\,fF + 68.6\,fF + 509.8\,fF}$$

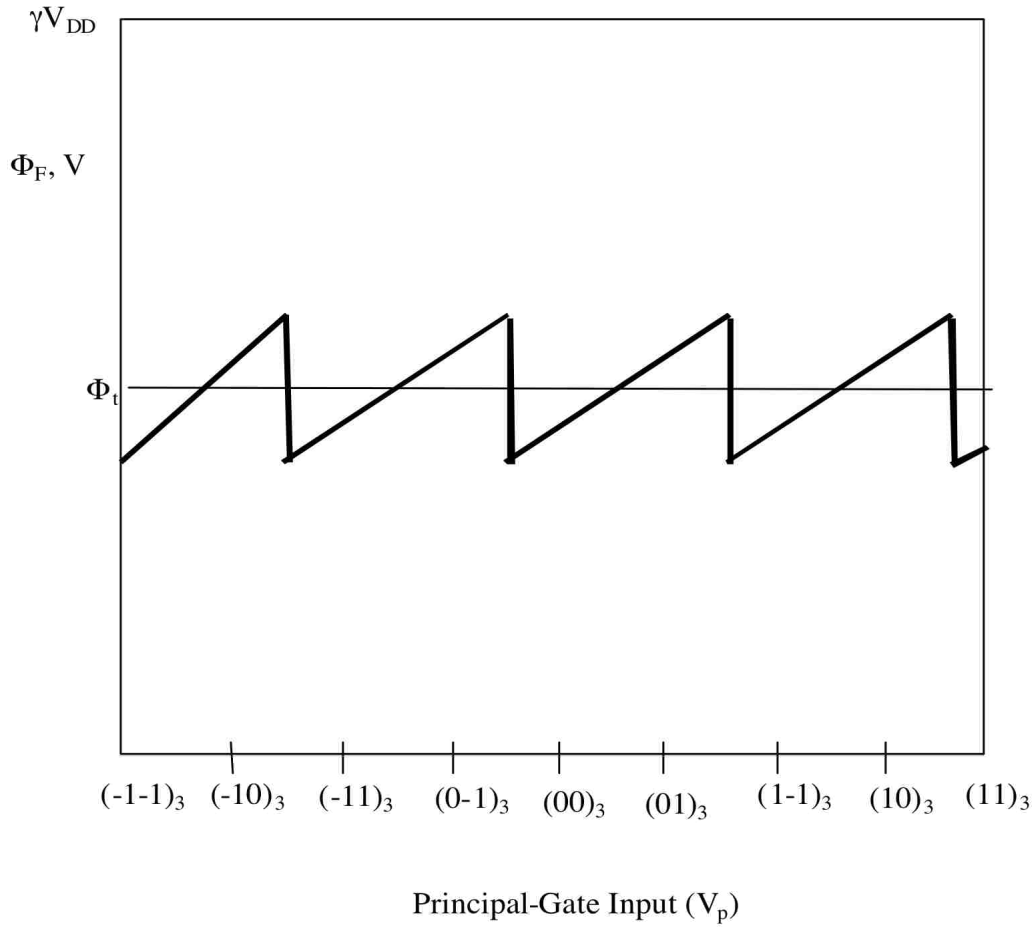

Figure 3.7: Floating gate potential diagram for the LSB.

For inputs, $(-1,0)_3$,

$\Phi_F > \Phi_t\,(1.4V)$ (3.44)

For input $(-1,1)_3$,

$$\Phi F = \frac{-3V \times 500\,fF + 3V \times 350\,fF + C26 \times 0V + C27 \times 0V + 3V \times C28 + 3V \times C29 + 3V \times 150\,fF}{C26 + C27 + C28 + C29 + 500\,fF + 350\,fF + 150\,fF + 68.6\,fF + 509.8\,fF}$$

Here, $\Phi_F < \Phi_t\,(1.4V)$ (3.45)

For input $(0,-1)_3$,

$$\Phi F = \frac{0V \times 500\,fF + -3V \times 350\,fF + C26 \times 0V + C27 \times 0V + 3V \times C28 + 3V \times C29 + 3V \times 150\,fF}{C26 + C27 + C28 + C29 + 500\,fF + 350\,fF + 150\,fF + 68.6\,fF + 509.8\,fF}$$

Here, $\Phi_F > \Phi_t\,(1.4V)$ (3.46)

For input $(0,0)_3$,

$$\Phi F = \frac{0V \times 500\,fF + 0V \times 350\,fF + C26 \times 0V + C27 \times 0V + 0V \times C28 + 3V \times C29 + 3V \times 150\,fF}{C26 + C27 + C28 + C29 + 500\,fF + 350\,fF + 150\,fF + 68.6\,fF + 509.8\,fF}$$

Here, $\Phi_F < \Phi_t\,(1.4V)$ (3.47)

For input $(0,1)_3$,

$$\Phi F = \frac{0V \times 500\,fF + 3V \times 350\,fF + C26 \times 0V + C27 \times 0V + 0V \times C28 + 3V \times C29 + 3V \times 150\,fF}{C26 + C27 + C28 + C29 + 500\,fF + 350\,fF + 150\,fF + 68.6\,fF + 509.8\,fF}$$

Here, $\Phi_F > \Phi_t\,(1.4V)$ (3.48)

For input $(1,-1)_3$,

$$\Phi F = \frac{3V \times 500\,fF + -3V \times 350\,fF + C26 \times 0V + C27 \times 0V + 0V \times C28 + 3V \times C29 + 3V \times 150\,fF}{C26 + C27 + C28 + C29 + 500\,fF + 350\,fF + 150\,fF + 68.6\,fF + 509.8\,fF}$$

Here, $\Phi_F < \Phi_t\,(1.4V)$ (3.49)

For input $(1,0)_3$,

$$\Phi F = \frac{3V \times 500\,fF + 0V \times 350\,fF + C26 \times 0V + C27 \times 0V + 0V \times C28 + 0V \times C29 + 3V \times 150\,fF}{C26 + C27 + C28 + C29 + 500\,fF + 350\,fF + 150\,fF + 68.6\,fF + 509.8\,fF}$$

Here, $\Phi_F > \Phi_t\,(1.4V)$ (3.50)

For input $(1,1)_3$,

$$\Phi F = \frac{3V \times 500\,fF + 3V \times 350\,fF + C26 \times 0V + C27 \times 0V + 0V \times C28 + 0V \times C29 + 3V \times 150\,fF}{C26 + C27 + C28 + C29 + 500\,fF + 350\,fF + 150\,fF + 68.6\,fF + 509.8\,fF}$$

Here, $\Phi_F < \Phi_t\,(1.4V)$ (3.51)

The minimum sizes of the capacitors C26, C27, C28 and C29 controlled by output of pre-input inverter stages, which satisfy above equations are found to be 350fF, 500fF, 800fF and 1602fF, respectively. Substituting the value of all the capacitors in Eq. (3.41), the value of CP is found to be 509.82fF. The values have been substituted in Eqs. (3.41) to (3.50) and the values are tabulated in Table 3.7.

3.5.2 Circuit Design for Stage #7

The pre-input gate inverter stage #7 goes LOW (0V) from inputs $(-1,1)_3$ to $(1,1)_3$. This inverter stage can be designed with three input capacitors C18, C19 and C20. The capacitors C19 and C20 are controlled by ternary inputs VA and VB, respectively and capacitor C18 is connected to supply voltage VDD (3V). Let us assume C19 and C20 to be 750fF and 350fF respectively. The transistor used for this stage has a W/L ratio of W_p/ L_p =30.15 μm / 2.1μm and W_n/ L_n =13.2 μm / 2.1μm and has a threshold voltage ΦT=1.4V.

The gate oxide capacitances can therefore be calculated as,

$$COXP = \frac{8.854 \times 10^{-12} \times 3.8}{142 \times 10^{-10}} \times \left(30.15 \times 10^{-6} \times 2.1 \times 10^{-6}\right) = 150\,fF \quad (3.52)$$

$$COXN = \frac{8.854 \times 10^{-12} \times 3.8}{142 \times 10^{-10}} \times \left(13.2 \times 10^{-6} \times 2.1 \times 10^{-6}\right) = 65.6\,fF \quad (3.53)$$

The value of CP can be calculated using equations as,

$$CP = \frac{C18 + 750\,fF + 350\,fF}{350\,fF} \times 43.5 \quad (3.54)$$

Table 3.7: Floating gate voltage for the final Stage #10 of the LSB.

Ternary Inputs	Output of Stage #7 (V_{14})	Output of Stage #8 (V_{15})	Output of Stage #9 (V_{16})	Voltage on Floating Gate of Main Inverter (Φ_F), V	Floating gate Voltage of the Transistor of Stage #10	Floating Gate Voltage of the Inverter
$(-1,-1)_3$	HIGH	HIGH	HIGH	1.314	$\Phi_F < \Phi_t$	$\Phi_F > \Phi_t$
$(-1,0)_3$	HIGH	HIGH	HIGH	1.948	$\Phi_F > \Phi_t$	$\Phi_F < \Phi_t$
$(-1,1)_3$	LOW	HIGH	HIGH	1.313	$\Phi_F < \Phi_t$	$\Phi_F > \Phi_t$
$(0,-1)_3$	LOW	HIGH	HIGH	1.478	$\Phi_F > \Phi_t$	$\Phi_F < \Phi_t$
$(0,0)_3$	LOW	LOW	HIGH	1.176	$\Phi_F < \Phi_t$	$\Phi_F > \Phi_t$
$(0,1)_3$	LOW	LOW	HIGH	1.411	$\Phi_F > \Phi_t$	$\Phi_F < \Phi_t$
$(1,-1)_3$	LOW	LOW	LOW	0.201	$\Phi_F < \Phi_t$	$\Phi_F > \Phi_t$
$(1,0)_3$	LOW	LOW	LOW	1.463	$\Phi_F > \Phi_t$	$\Phi_F < \Phi_t$
$(1,1)_3$	LOW	LOW	LOW	0.671	$\Phi_F < \Phi_t$	$\Phi_F > \Phi_t$

Using Eq. (2.14), the inequality for this stage would be,

$$\Phi F = \frac{VA \times C19 + VB \times C20 + VC \times C13 + 3V \times COXP}{C19 + C20 + C18 + COXP + COXN + CP} \tag{3.55}$$

For inputs $(-1,1)_3$ to $(1,1)_3$, the Eq. (3.55) can be written as,

$$\Phi F = \frac{VA \times C19 + VB \times C20 + VC \times C13 + 3V \times COXP}{C19 + C20 + C18 + COXP + COXN + CP} > \Phi T(1.4V) \tag{3.56}$$

For the rest of the inputs, the inequality is given as,

$$\Phi F = \frac{VA \times C19 + VB \times C20 + VC \times C13 + 3V \times COXP}{C19 + C20 + C18 + COXP + COXN + CP} < \Phi T(1.4V) \tag{3.57}$$

Substituting the value of C19, C20, COXP and COXN in the above inequalities, the value of C18 can be found by iteration to be 3313fF. This value can now be substituted in Eq. (3.54) and value of CP is found to be 767.86fF. The circuit diagram for this stage along with the other LSB circuit stages is shown in Fig. 3.8. Values of ΦF is calculated from the two inequalities (3.56, 3.57) and tabulated in Table 3.8.

3.5.3 Circuit Design for Stage #8

The pre-input gate inverter Stage #8 goes LOW (0 V) from inputs $(0,0)_3$ to $(1,1)_3$. This inverter stage can be designed with three input capacitors C21, C22 and C23. The capacitors C22 and C23 are controlled by ternary inputs VA and VB, respectively and capacitor C21 is connected to supply voltage VDD (3V). Let us assume C22 and C23 to be 450fF and 250fF respectively. The transistor used for this stage has a W/L ratio of W_p/ L_p =30.15 μm / 2.1μm and W_n/ L_n =13.2 μm / 2.1μm and has a threshold voltage ΦT=1.4V.

The gate oxide capacitances can therefore be calculated as,

$$COXP = \frac{8.854 \times 10^{-12} \times 3.8}{142 \times 10^{-10}} \times \left(30.15 \times 10^{-6} \times 2.1 \times 10^{-6}\right) = 150\,fF \tag{3.58}$$

$$COXN = \frac{8.854 \times 10^{-12} \times 3.8}{142 \times 10^{-10}} \times \left(13.2 \times 10^{-6} \times 2.1 \times 10^{-6}\right) = 65.6\,fF \tag{3.59}$$

The value of CP can be calculated using Eqs. (3.58, 3.59) as,

$$CP = \frac{C18 + 450\,fF + 250\,fF}{250\,fF} \times 43.5 \tag{3.60}$$

Using Eq. (2.14), the inequality for Stage #8 would be,

$$\Phi F = \frac{VA \times C22 + VB \times C23 + VC \times C21 + 3V \times COXP}{C21 + C22 + C23 + COXP + COXN + CP} \tag{3.61}$$

For inputs $(0,0)_3$ to $(1,1)_3$, the Eq. (3.61) can be written as,

$$\Phi F = \frac{VA \times C22 + VB \times C23 + VC \times C21 + 3V \times COXP}{C21 + C22 + C23 + COXP + COXN + CP} > \Phi T(1.4V) \tag{3.62}$$

For the rest of the inputs, the inequality is given as,

$$\Phi F = \frac{VA \times C22 + VB \times C23 + VC \times C21 + 3V \times COXP}{C21 + C22 + C23 + COXP + COXN + CP} < \Phi T(1.4V) \tag{3.63}$$

Substituting the value of C22, C23, COXP and COXN in the above inequalities, the value if C21 can be found by iteration to be 1130fF. This value can now be substituted in Eq. (3.60) and value of CP is found to be 312.42fF. The circuit diagram for this stage along with the other LSB circuit stages is shown in Figure 3.8. Values of ΦF is calculated from the two inequalities (3.62, 3.63) and tabulated in Table 3.9.

3.5.4 Circuit Design for Stage #9

The pre-input gate inverter Stage #9 goes LOW (0V) from inputs $(1,-1)_3$ to $(1,1)_3$. This inverter stage can be designed with three input capacitors C24 and C25. The capacitors C24 and C25 are controlled by ternary inputs VA and VB. Let us assume C24 be 250fF. The transistor used for this stage has a W/L ratio of W_p/ L_p =30.15 μm / 2.1μm, W_n/ L_n =4.2 μm / 2.1μm and has a threshold voltage ΦT=1.5476V.

Table 3.8: Floating gate voltage for the Stage #7 of the LSB.

Ternary Inputs	Voltage on Floating Gate of Stage #7 Inverter (Φ_F), V	Floating Gate Voltage of the Transistor of Stage #7
$(-1,-1)_3$	1.313	$\Phi_F < \Phi_t$
$(-1,0)_3$	1.358	$\Phi_F < \Phi_t$
$(-1,1)_3$	1.703	$\Phi_F > \Phi_t$
$(0,-1)_3$	1.730	$\Phi_F > \Phi_t$
$(0,0)_3$	1.925	$\Phi_F > \Phi_t$
$(0,1)_3$	2.119	$\Phi_F > \Phi_t$
$(1,-1)_3$	2.147	$\Phi_F > \Phi_t$
$(1,0)_3$	2.342	$\Phi_F > \Phi_t$
$(1,1)_3$	2.537	$\Phi_F > \Phi_t$

Table 3.9: Floating gate voltage for the Stage #8 of the LSB.

Ternary Inputs	Voltage on Floating Gate of Stage #8 Inverter (Φ_F), V	Floating Gate Voltage of the Transistor of Stage #8
$(-1,-1)_3$	0.736	$\Phi_F < \Phi_t$
$(-1,0)_3$	1.053	$\Phi_F < \Phi_t$
$(-1,1)_3$	1.371	$\Phi_F < \Phi_t$
$(0,-1)_3$	1.307	$\Phi_F < \Phi_t$
$(0,0)_3$	1.624	$\Phi_F > \Phi_t$
$(0,1)_3$	1.942	$\Phi_F > \Phi_t$
$(1,-1)_3$	1.878	$\Phi_F > \Phi_t$
$(1,0)_3$	2.196	$\Phi_F > \Phi_t$
$(1,1)_3$	2.513	$\Phi_F > \Phi_t$

The gate oxide capacitance COXP can therefore be calculated as,

$$COXP = \frac{8.854 \times 10^{-12} \times 3.8}{142 \times 10^{-10}} \times \left(30.15 \times 10^{-6} \times 2.1 \times 10^{-6}\right) = 150\,fF \tag{3.64}$$

The gate oxide capacitance COXN for Stage #9 is calculated as,

$$COXN = \frac{8.854 \times 10^{-12} \times 3.8}{142 \times 10^{-10}} \times \left(4.2 \times 10^{-6} \times 2.1 \times 10^{-6}\right) = 20.89\,fF \tag{3.65}$$

The value of CP can be calculated using equations as,

$$CP = \frac{250\,fF + C25}{250\,fF} \times 43.5 \tag{3.66}$$

Using equation (2.14), the inequality for this stage would be,

$$\Phi F = \frac{VA \times C24 + VB \times C25 + 3V \times COXP}{C24 + C25 + COXP + COXN + CP} \tag{3.67}$$

For inputs $(1,\text{-}1)_3$ to $(1,1)_3$, the Eq. (3.67) can be written as,

$$\Phi F = \frac{VA \times C24 + VB \times C25 + 3V \times COXP}{C24 + C25 + COXP + COXN + CP} > \Phi T(1.5476V) \tag{3.68}$$

For the rest of the inputs, the inequality is given as,

$$\Phi F = \frac{VA \times C24 + VB \times C25 + 3V \times COXP}{C24 + C25 + COXP + COXN + CP} < \Phi T(1.5476V) \tag{3.69}$$

Substituting the value of C24, COXP, COXN in the above inequalities, the value if C25 can be found by iteration to be 250fF. This value can now be substituted in Eq. (3.66) and value of CP is found to be 87fF. The circuit diagram for this stage along with the other LSB circuit stages is shown in Figure 3.8. Values of ΦF are calculated from the two Eqs. (3.68,3.69) and tabulated in Table 3.10. The complete ternary to binary converter circuit is shown in Figure 3.9.

Table 3.10: Floating gate voltage for the Stage #9 of the LSB.

Ternary Inputs	Voltage on Floating Gate of Stage #9 Inverter (Φ_F), V	Floating Gate Voltage of the Transistor of Stage #9
$(-1,-1)_3$	-1.385	$\Phi_F < \Phi_t$
$(-1,0)_3$	-0.396	$\Phi_F < \Phi_t$
$(-1,1)_3$	0.5937	$\Phi_F < \Phi_t$
$(0,-1)_3$	-0.3958	$\Phi_F < \Phi_t$
$(0,0)_3$	0.5937	$\Phi_F < \Phi_t$
$(0,1)_3$	1.503	$\Phi_F < \Phi_t$
$(1,-1)_3$	1.5937	$\Phi_F > \Phi_t$
$(1,0)_3$	1.583	$\Phi_F > \Phi_t$
$(1,1)_3$	2.573	$\Phi_F > \Phi_t$

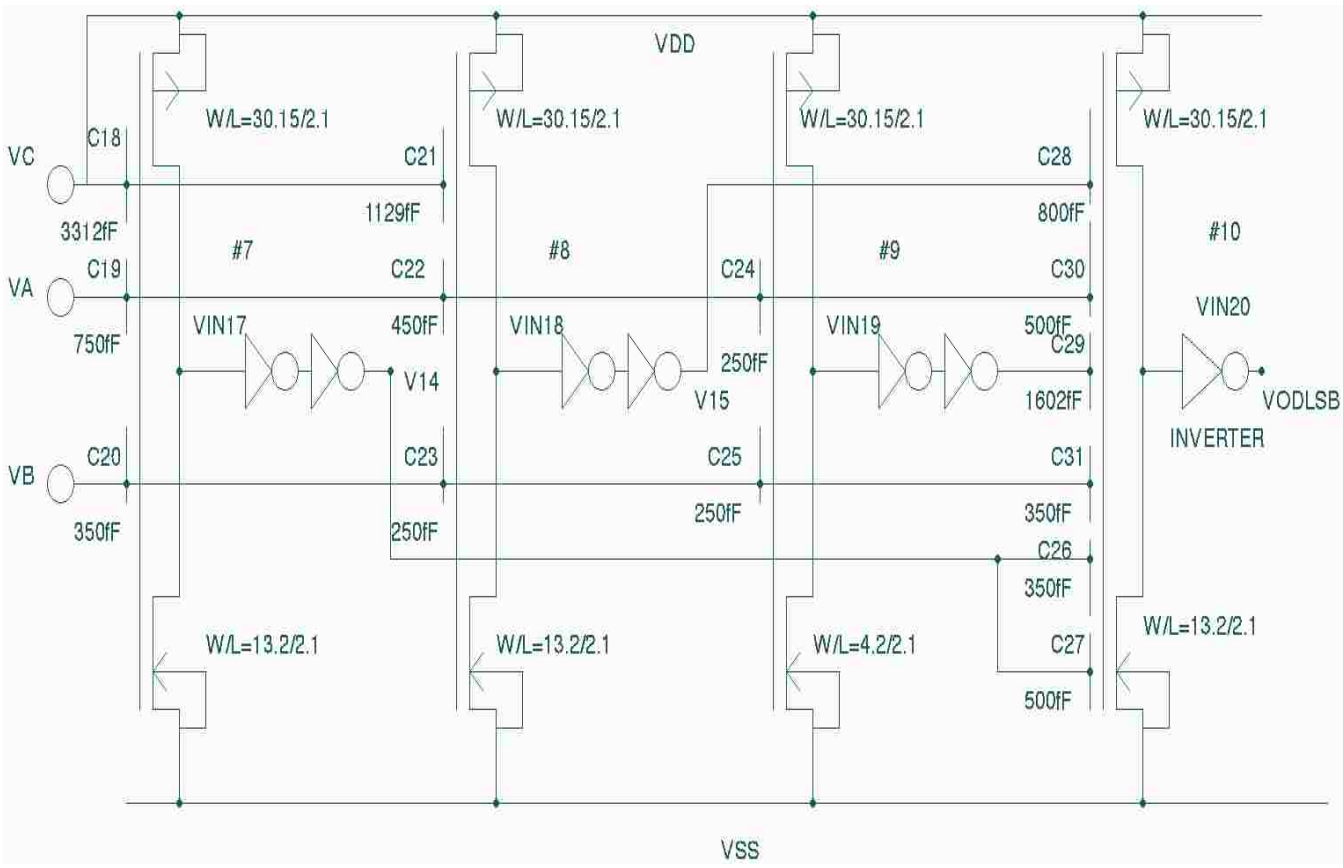

Figure 3.8: Circuit for LSB.

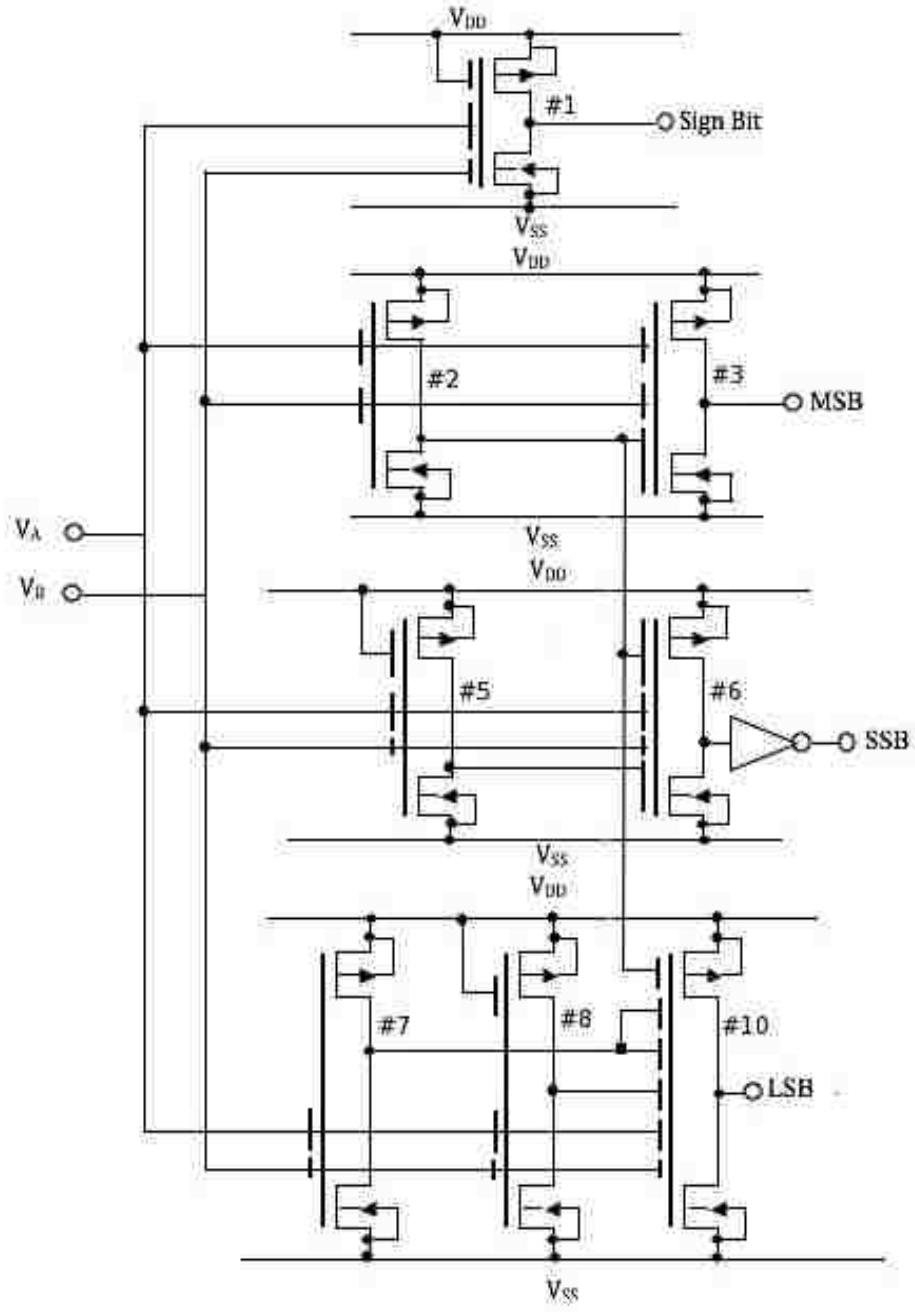

Figure 3.9: Full circuit of the ternary to binary converter

CHAPTER 4. PHYSICAL DESIGN AND SIMULATIONS

4.1 Layout of the Ternary to Binary Converter Stages

The layout for the ternary to binary bit converter is divided into four stages corresponding to the four output bits, which are the SB, MSB, SSB and LSB. The physical design of the stages for each bit is described in this chapter. The layout is done using L-Edit 13.2 in 0.5μm CMOS n-well technology. The layout has been extracted into PSPICE and simulated using BSIM level 7 parameters obtained from MOSIS. The layout of each of the bits consists of a capacitor and transistors. The capacitors perform the function of the floating gate and depending on the voltage at the output of the capacitors, and the voltage that appears at the gate of the transistor the transistor either gives a HIGH (3V) or LOW (0V) at the output. In the design of the Sign Bit (SB) and the Most Significant Bit (MSB), there are additional transistor inverters connected to the output of the primary transistor that act as buffers. In this thesis, individual capacitors have been used instead of the common-centroid design of the capacitors, which uses unit capacitors connected together to form a capacitor of larger value. The use of individual capacitors was because of the need for use of capacitors that were not multiples of the unit capacitor as required in the common-centroid capacitor design.

The layout for Stage #1 of the Sign Bit (SB) is shown in Fig. 4.1.The layout for Stages #2 and #3 of the Most Significant Bit (MSB) is shown in Fig. 4.2. The layout for Stages #4, #5 and #6 of the Second Significant Bit (SSB) is shown in Fig. 4.3. The layout for Stages #7, #8, #9, #10 of the Least Significant Bit (LSB) is shown in Fig. 4.4. Fig. 4.5 shows the complete layout of a ternary-to-binary bit converter in 0.5μm n-well CMOS process. The complete layout of the ternary to binary converter occupies an area of 1140μm x 2090μm. The post-layout output simulations for all the stages for different ternary inputs as indicated in Table 3.1 are shown in Figs. 4.6 to 4.14.

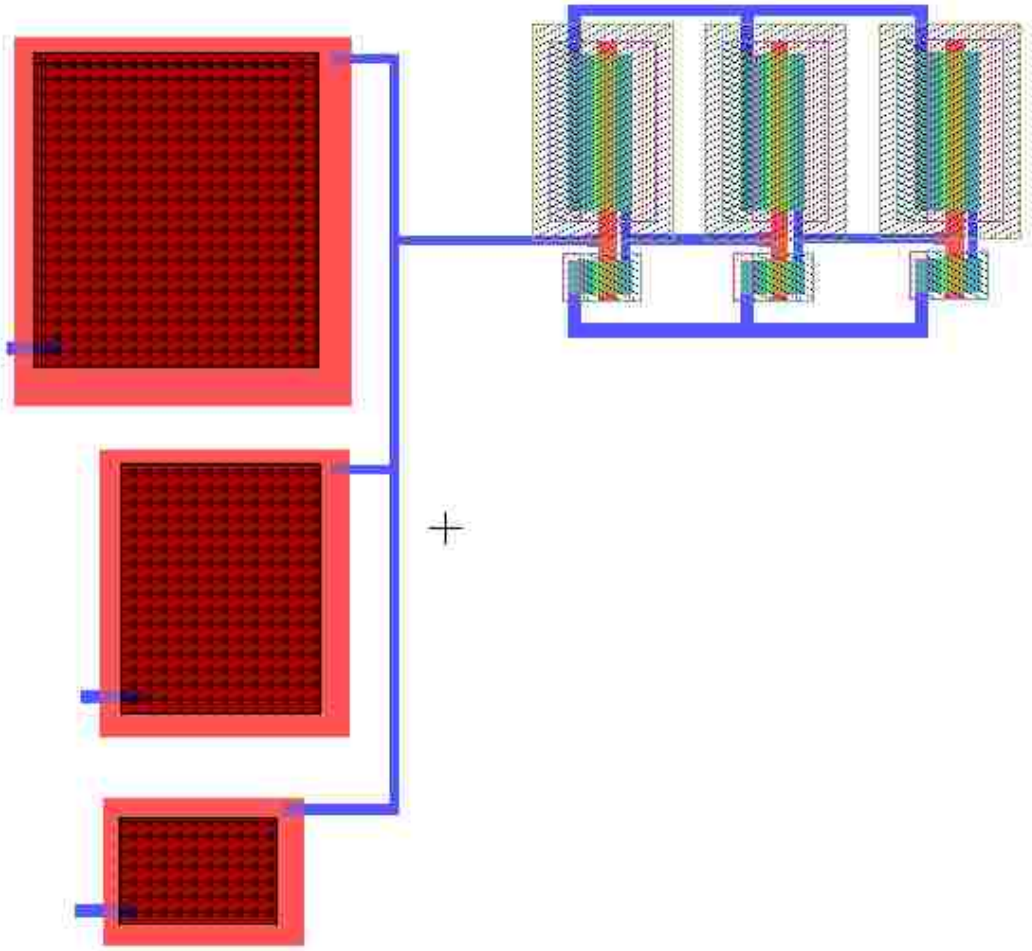

Figure 4.1: Layout of the sign bit circuit.

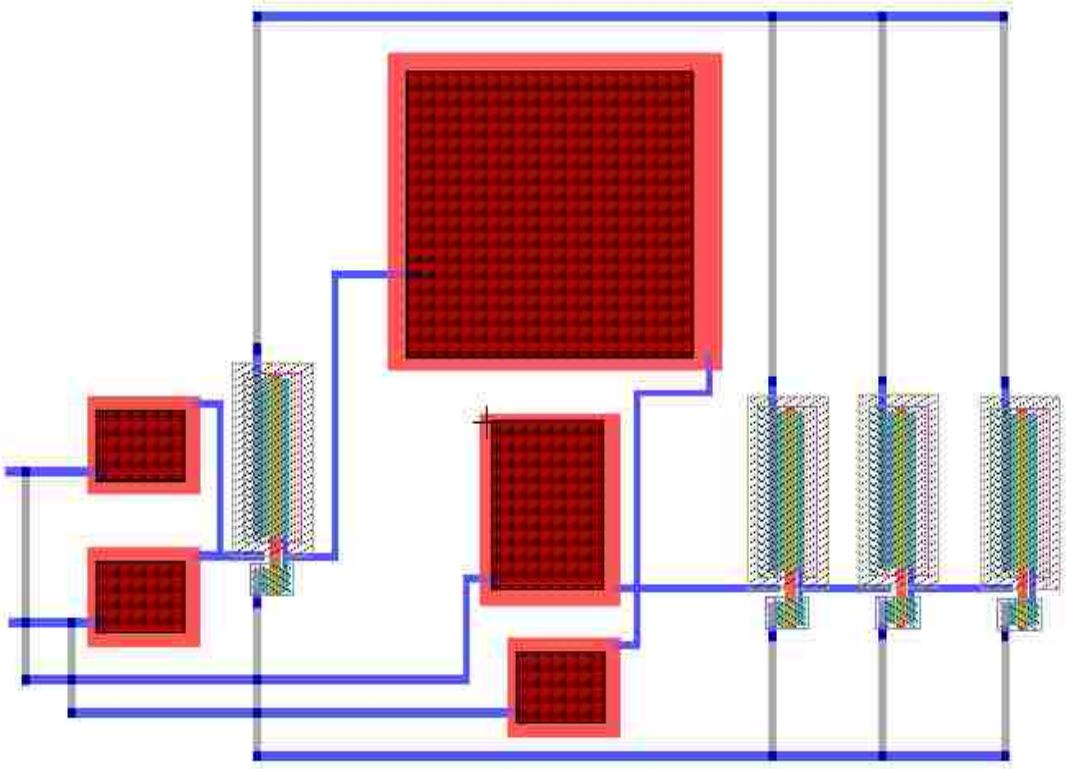

Figure 4.2: Layout of the MSB circuit.

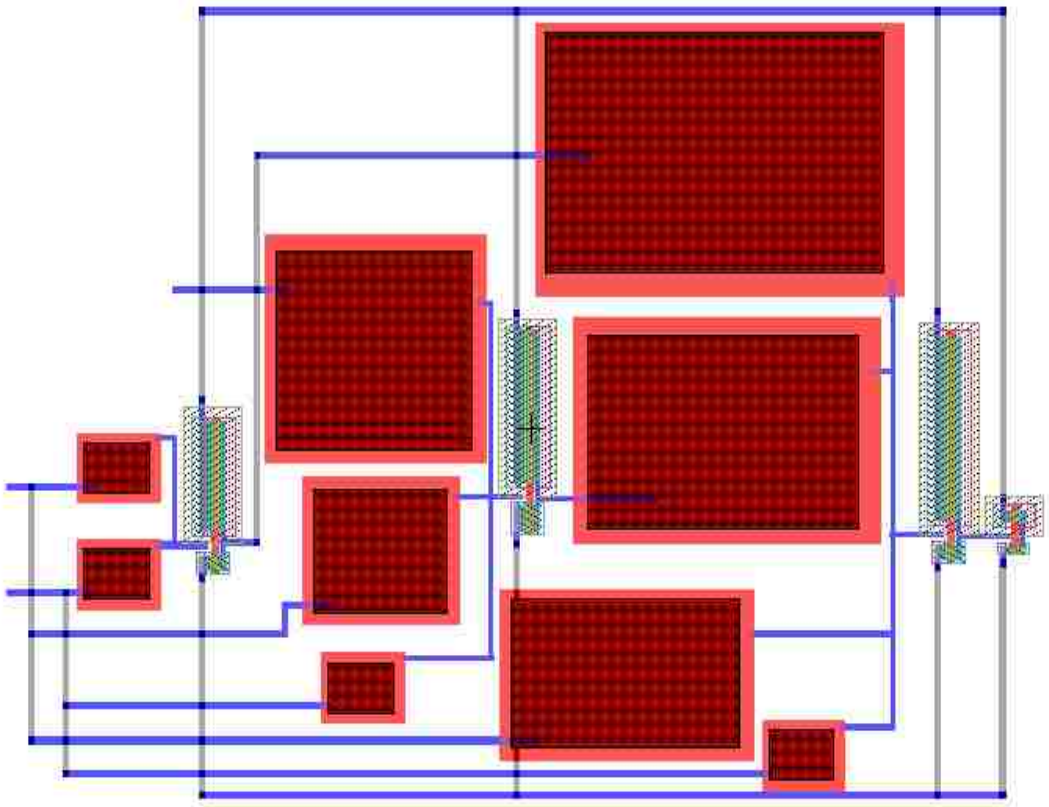

Figure 4.3: Layout of the SSB circuit.

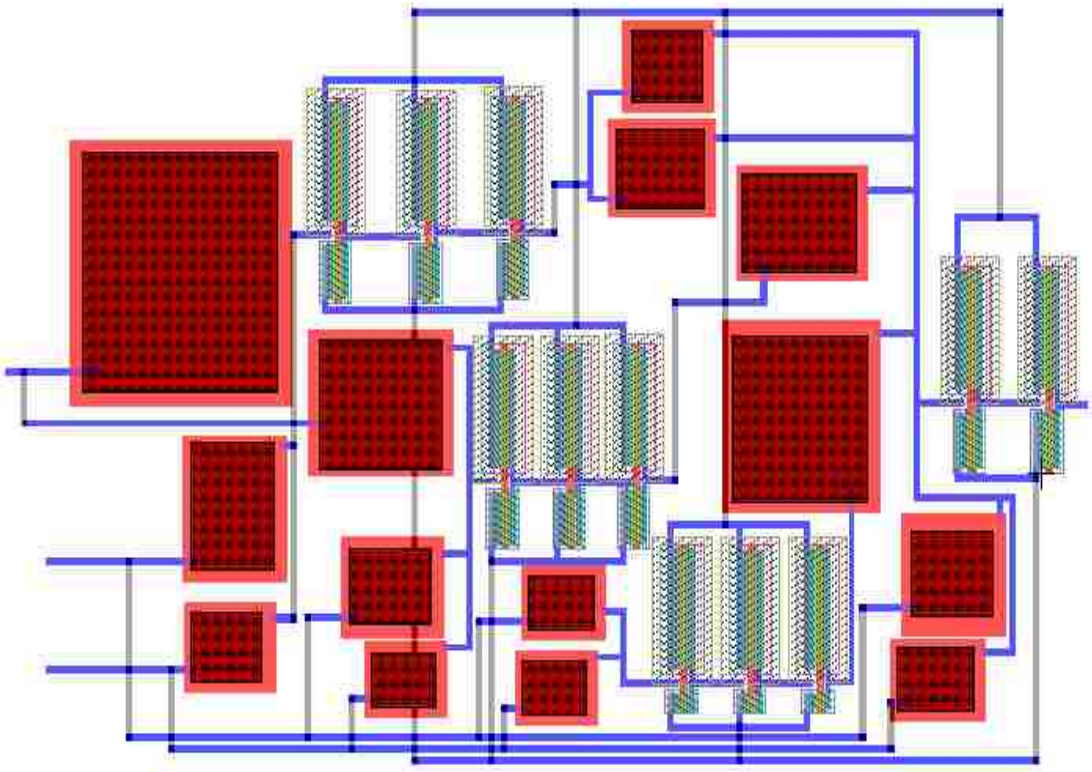

Figure 4.4: Layout of the LSB circuit.

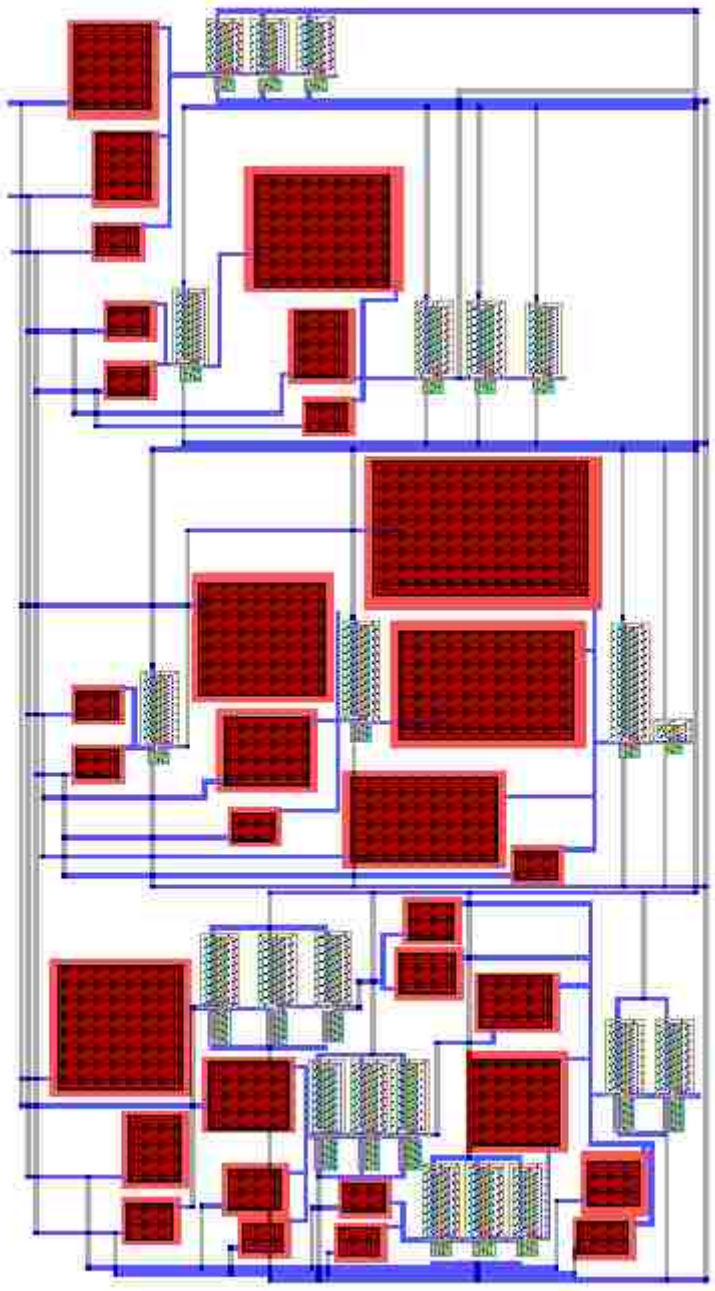

Figure 4.5: Layout of the ternary to binary converter circuit.

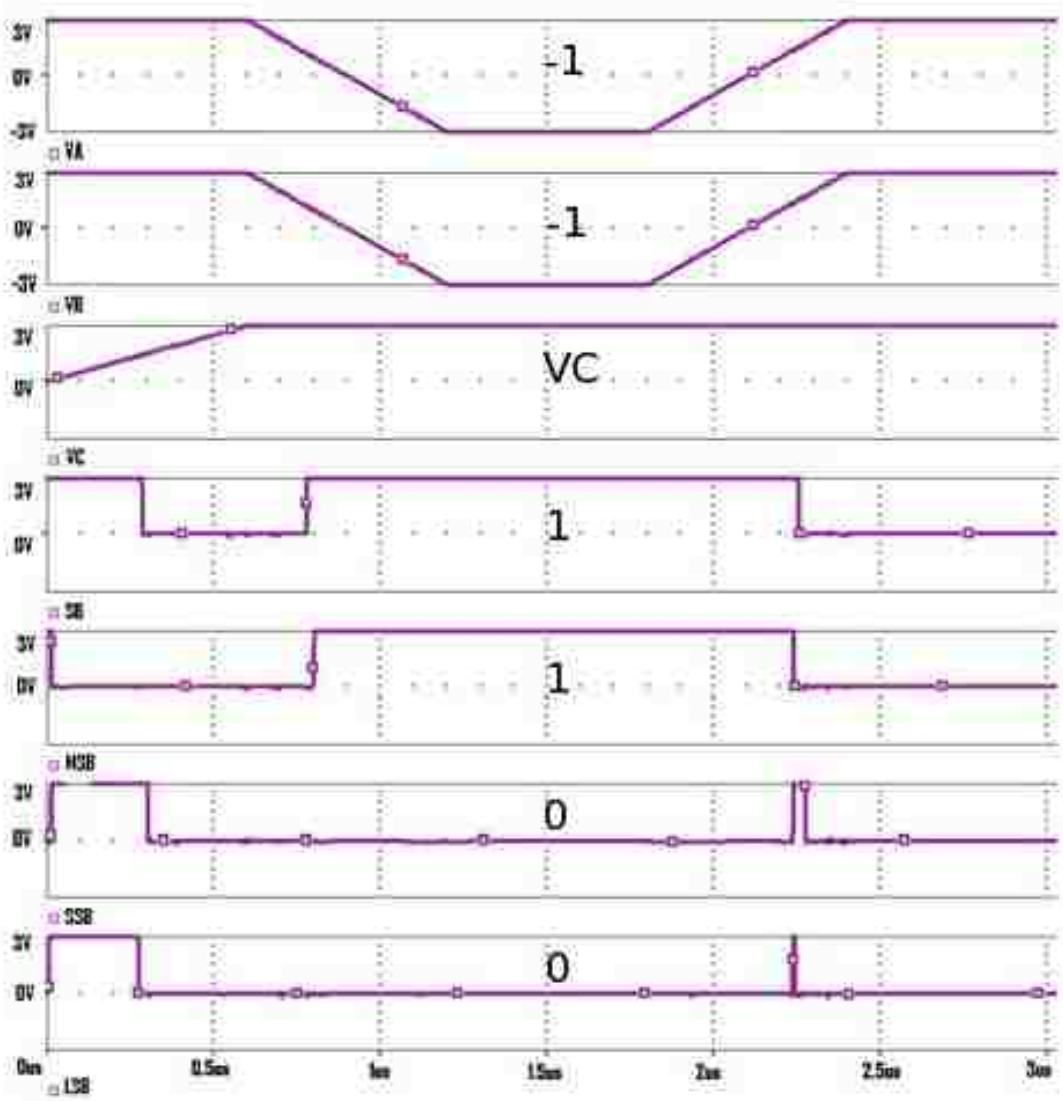

Figure 4.6: Output simulation results for ternary input $(-1,-1)_3$.

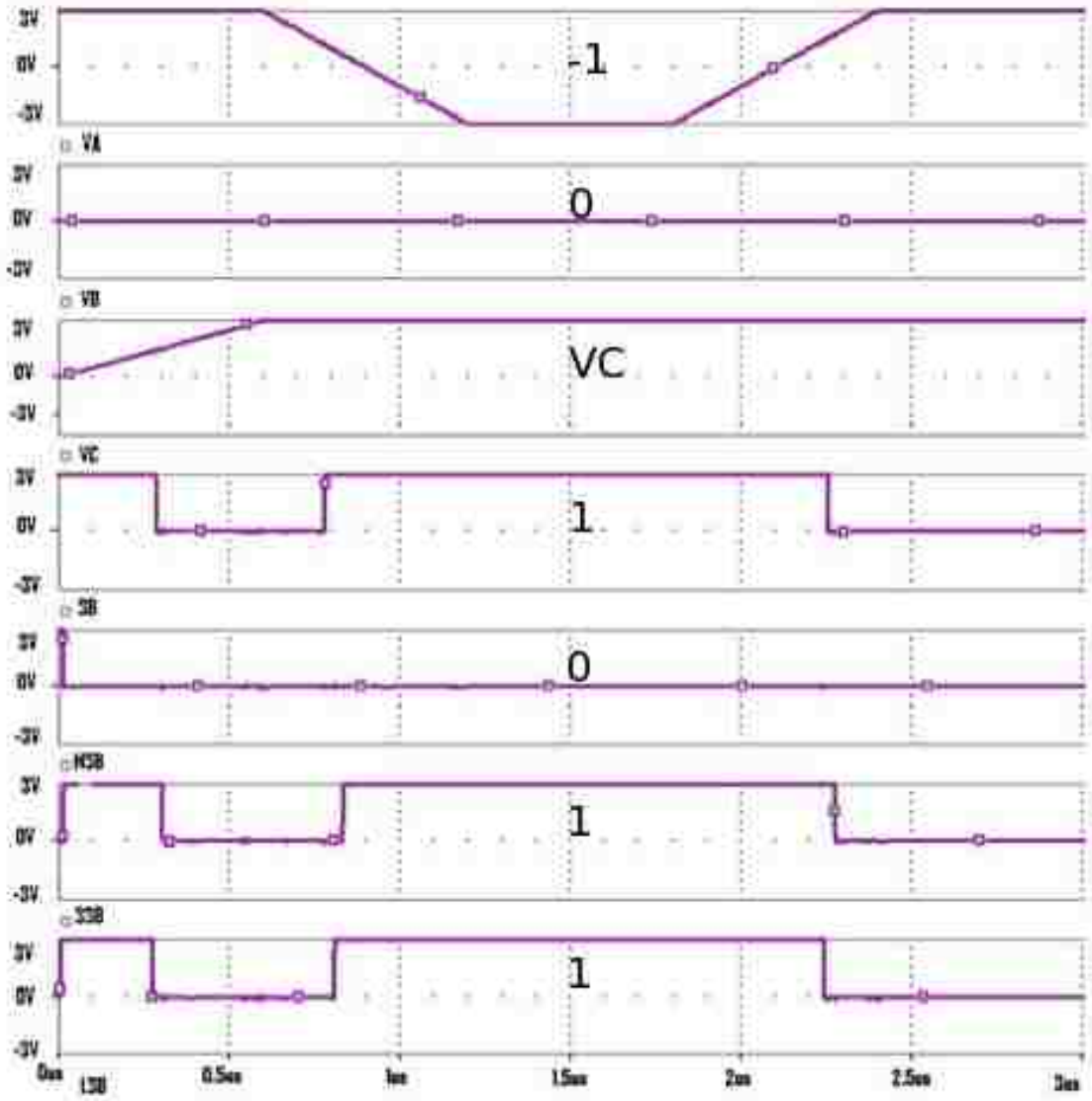

Figure 4.7: Output simulation results for ternary input $(-1,0)_3$.

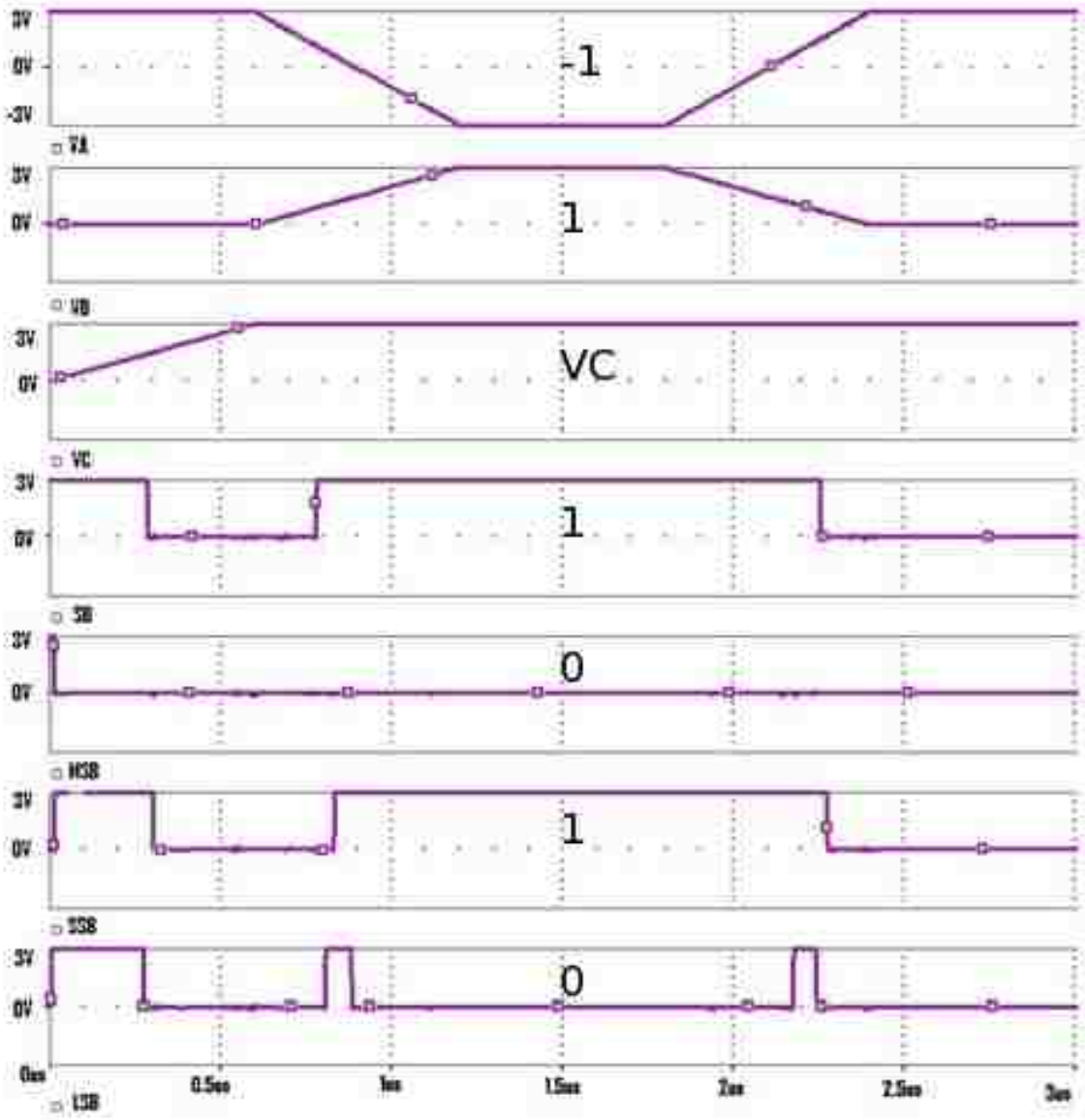

Figure 4.8: Output simulation results for ternary input $(-1,1)_3$.

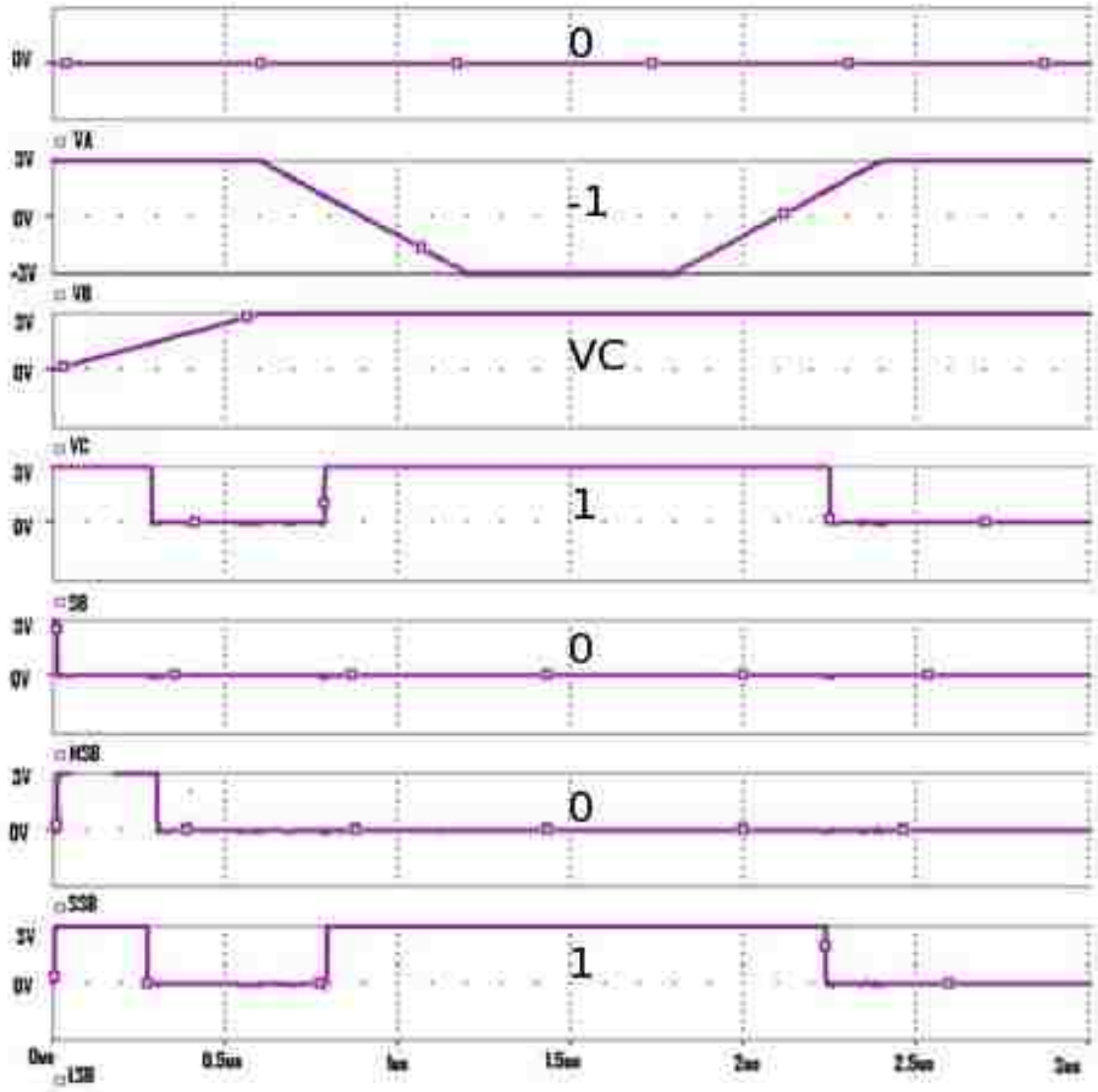

Figure 4.9: Output simulation results for ternary input $(0,-1)_3$.

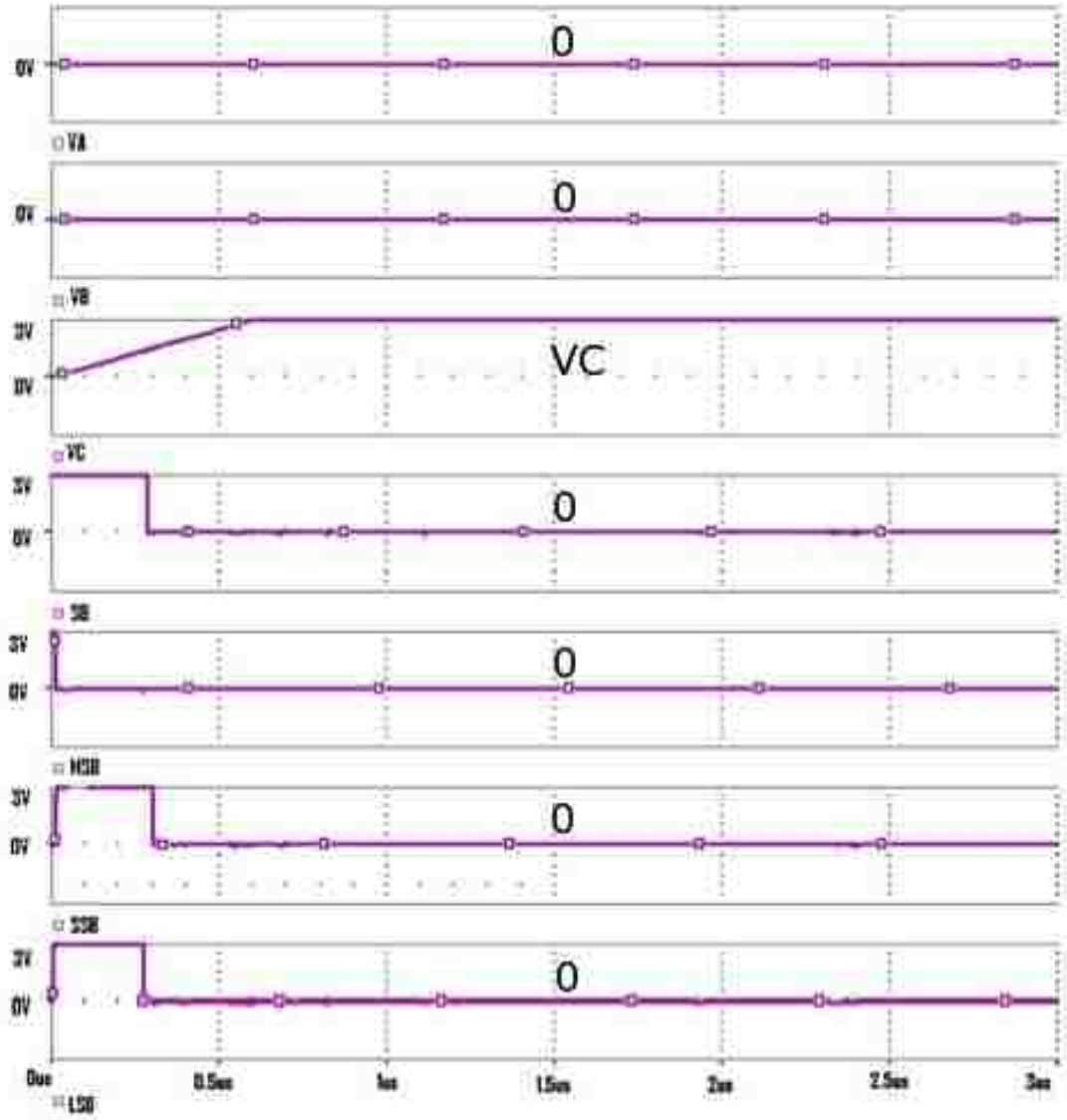

Figure 4.10: Output simulation results for ternary input $(0,0)_3$.

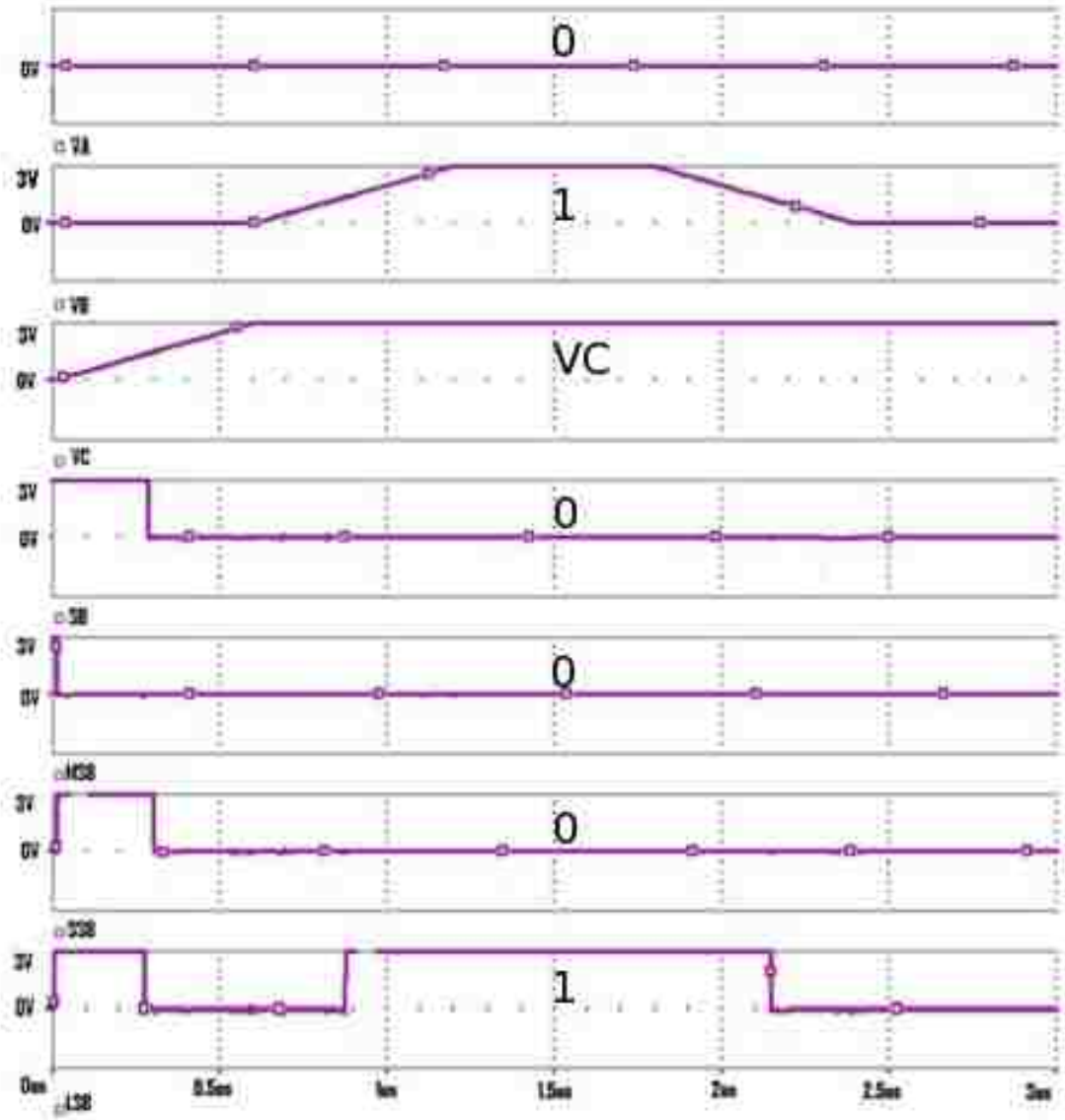

Figure 4.11: Output simulation results for ternary input $(0,1)_3$.

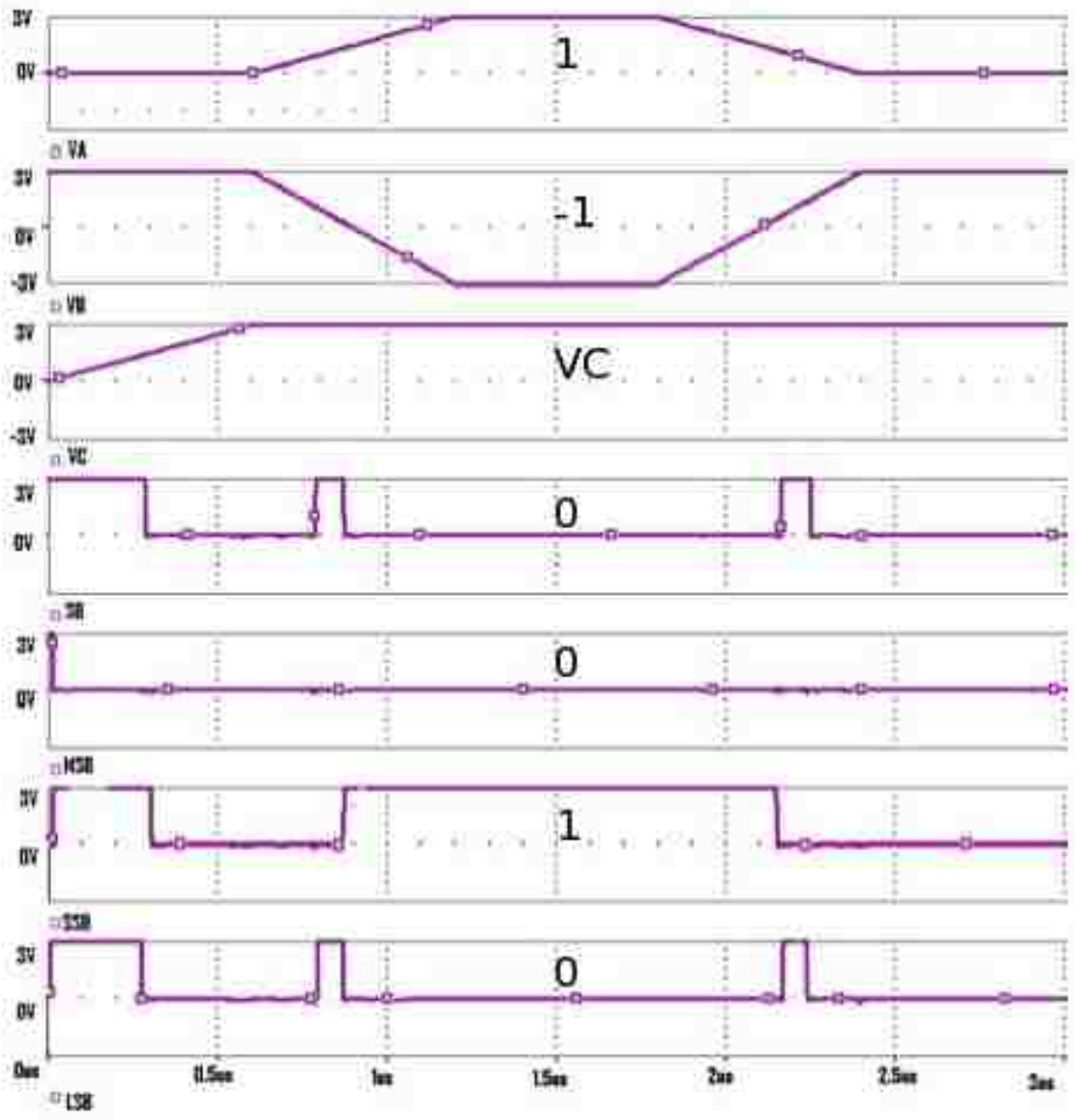

Figure 4.12: Output simulation results for ternary input $(1,-1)_3$.

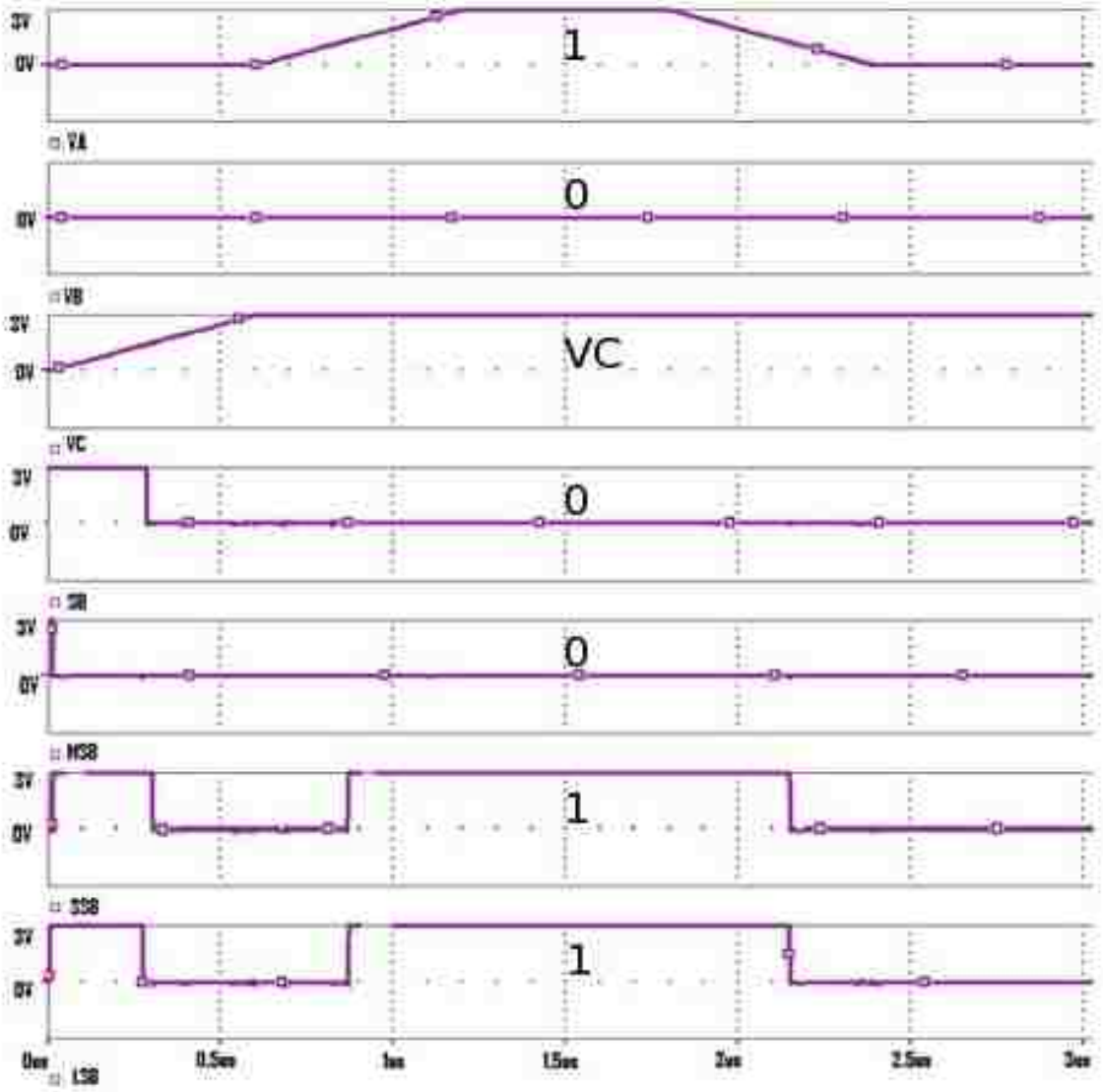

Figure 4.13: Output simulation results for ternary input $(1,0)_3$.

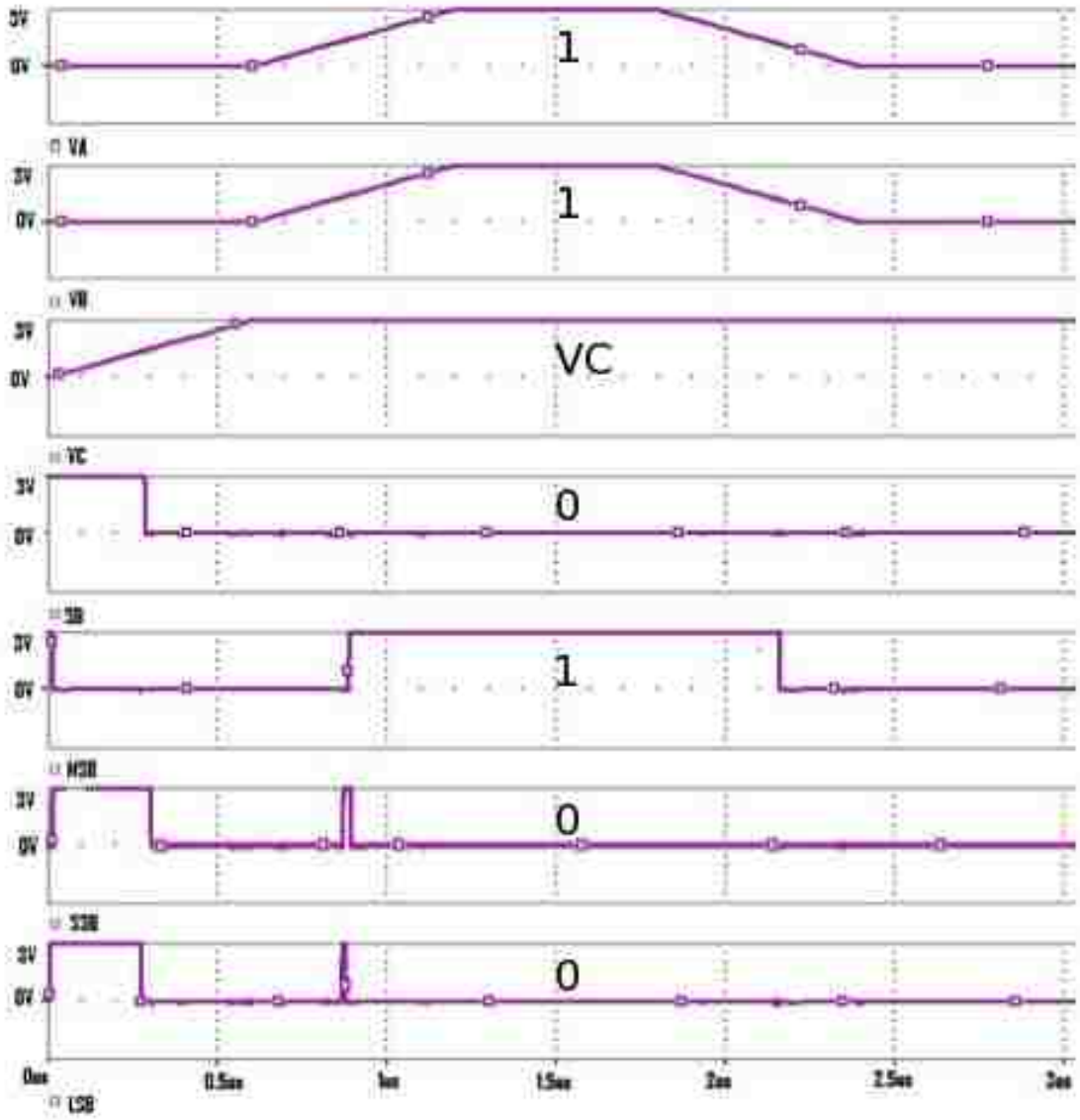

Figure 4.14: Output simulation results for ternary input $(1,1)_3$.

4.2 Padframe Design

The padframe used in this work is shown in Fig. 4.15. The inputs pins are denoted as VA, VB and VC. The inputs VA and VB vary between the ranges of -3V to 3V according to ternary bits. The third input VC acts as a control signal and is a constant 3V. A pulse signal that transitions between the levels -3V, 0V and 3V according to the ternary input under consideration is used to give the inputs. The binary output pins for SB, MSB, SSB and LSB corresponding to the ternary input are VODSBPAD, VODMSBPAD, VODSSBPAD and VODLSBPAD, respectively. The output pins for SB and MSB bits with buffer are given as VODSBBPAD and VODMSBBPAD, respectively. The power supply and ground pins are named as VDD and VSS, respectively.

There is also an inverter that is placed inside the padframe for testing purposes. The input and output pins of the inverter are VINVPAD and VOUTINVPAD, respectively. The pad pin numbers for the input, output and power supply are summarized in Table 4.1 for testability analysis. Fig. 4.15 shows the layout of the ternary to binary converter circuit in 0.5μm n-well CMOS process inside a padframe. Fig. 4.16 shows the microphotograph of the chip in a padframe.

4.3 Experimental Results

The chip is tested with the value of VDD set at 3V and VSS set at 0 V. The testing of this chip requires two arbitrary inputs varying from -3V to 3V, 0V and 3V to -3V corresponding to ternary bits 1,0 and -1, respectively. In order to test this chip, the two inputs were applied according to the combination of the ternary bits for each decimal number and the four bit binary output is obtained. For example, decimal number -3 is represented by ternary inputs (-1,0). Hence for this, VA corresponds to -1 and VB corresponds to 0. Hence a pulse signal is given representing input VA and is varied from 3V to -3V and input VB is connected to ground.

Table 4.1: Pad pin numbers for inputs, outputs and the power supply.

Pin Number	Pin Name	Pin Description
1-4	-	-
5	VODMSBPAD	Output of MSB stage without buffer
6	VODSBBPAD	Output of SB stage with buffer
7	VODSBPAD	Output of SB stage without buffer
8-11	-	-
12	VB2	LSB ternary bit input
13	VA2	MSB ternary bit input
14	VC2	Control signal or third input
15-20	-	-
21	VDD	Power supply
22,24	-	-
23	VOUTINVPAD	Output of test inverter
25	VINVPAD	Input of test inverter
26-34	-	-
35	VODLSBPAD	Output of LSB stage without buffer
36	VODSSBPAD	Output of SSB stage without buffer
37	VODMSBBPAD	Output of MSB stage with buffer
38,39	-	-
40	VSS	Ground

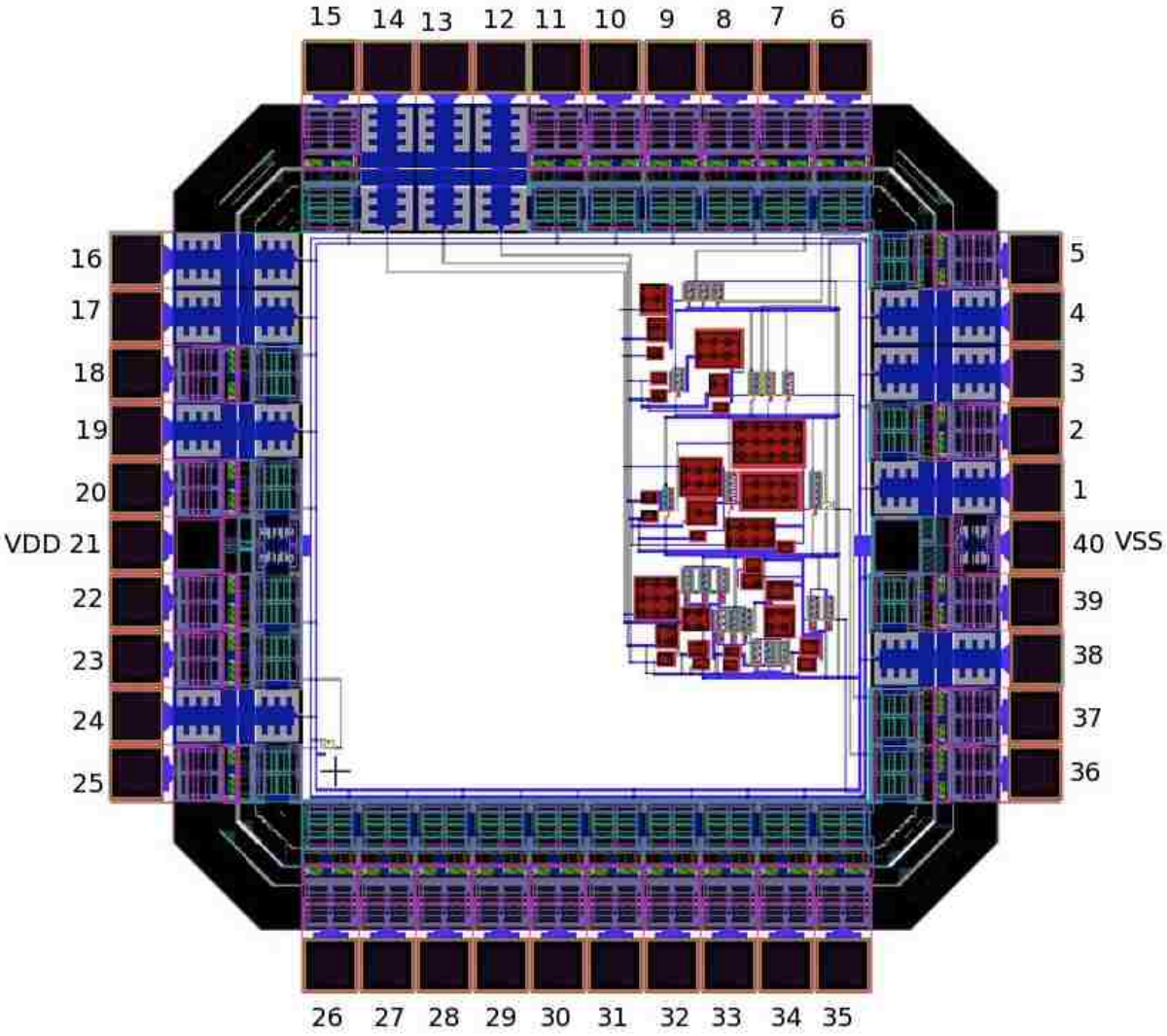

Figure 4.15: Layout of the ternary to binary converter circuit in a padframe.

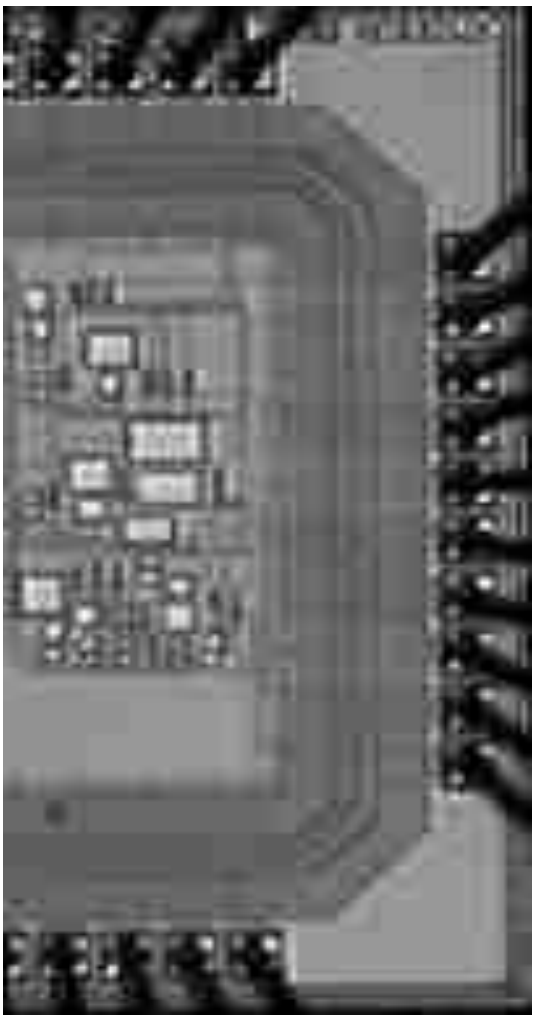

Figure 4.16: Microphotograph of the chip in the padframe.

A pulse that varies from 0V to 3V is given that represents VC. The four bit outputs are obtained from the output pins (VODSB, VODMSB, VODSSB and VODLSB) in the padframe. Snapshots of the four bit outputs obtained experimentally for different ternary inputs ranging from $(-1,-1)_3$ to $(1,1)_3$ are shown in Figs. 4.17 to 4.52. The circuit is verified for all possible transitions of the ternary input.

4.4 Time Delays

The propagation delay for different logic level transition has been measured and tabulated in Table 4.2. The logic transition level -1→-1 indicates that the two inputs VA and VB transition to logic level -1, which is -3V. The propagation delay is measured from 50 percent point of input to 50 percent point of output. For example, for the ternary input $(-1,-1)_3$, the input goes from 3V to -3V and the SB output is 3V. The delay in this case is considered from the 50 percent point of the input that is 0V to the 50 percent point of the output, which is 1.5V in this case. The worst-case delay is t_p=1.27μs for logic level transition of 0 to 1. Few columns of Table 4.2 have not been filled; this is because there is no change in the output of the circuit for the given change in the input.

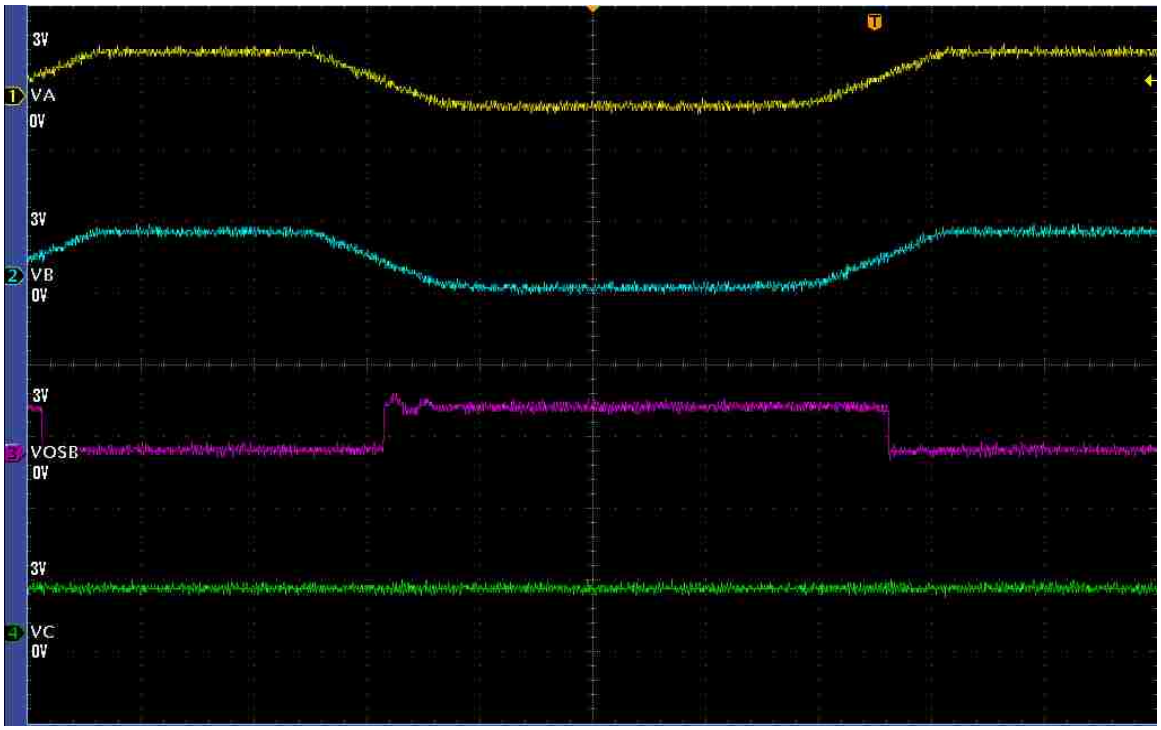

Figure 4.17: SB output for the input $(-1,-1)_3$.

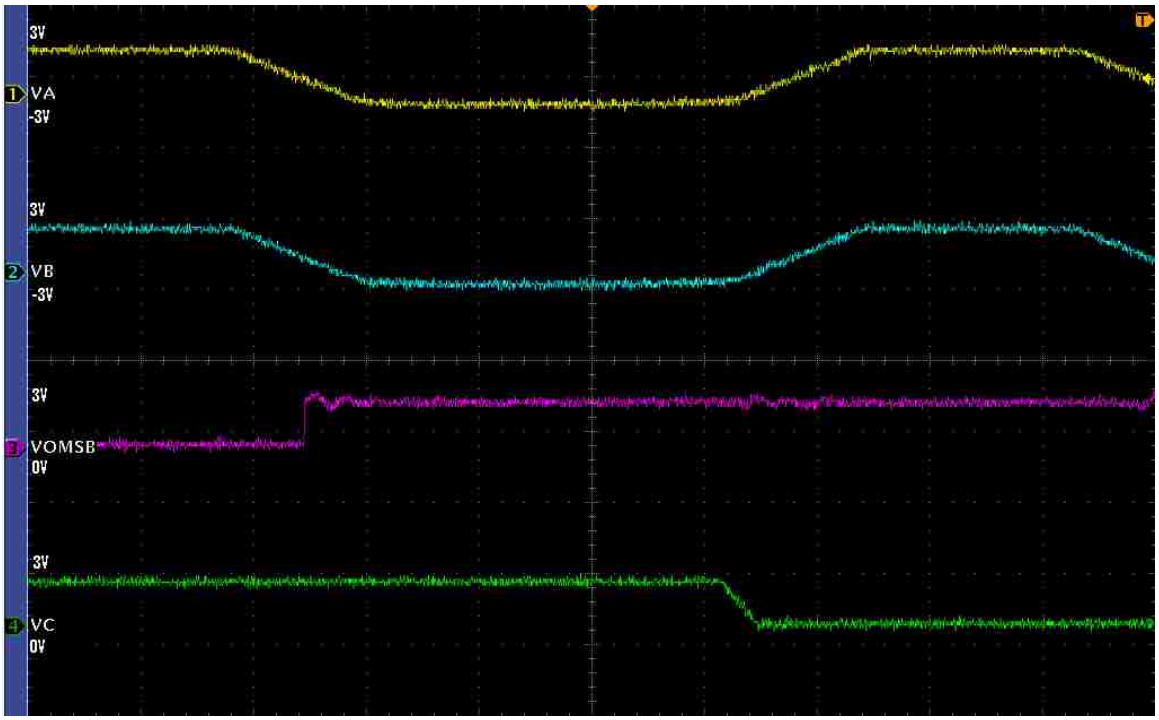

Figure 4.18: MSB output for the input $(-1,-1)_3$.

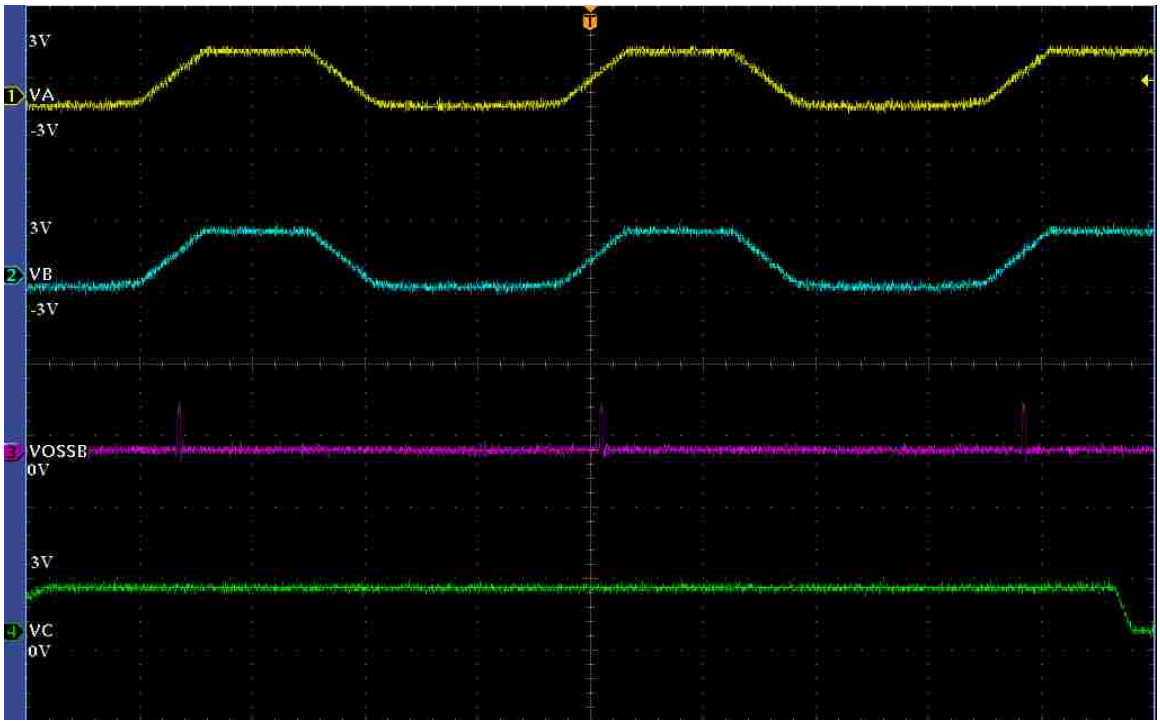

Figure 4.19: SSB output for the input $(-1,-1)_3$.

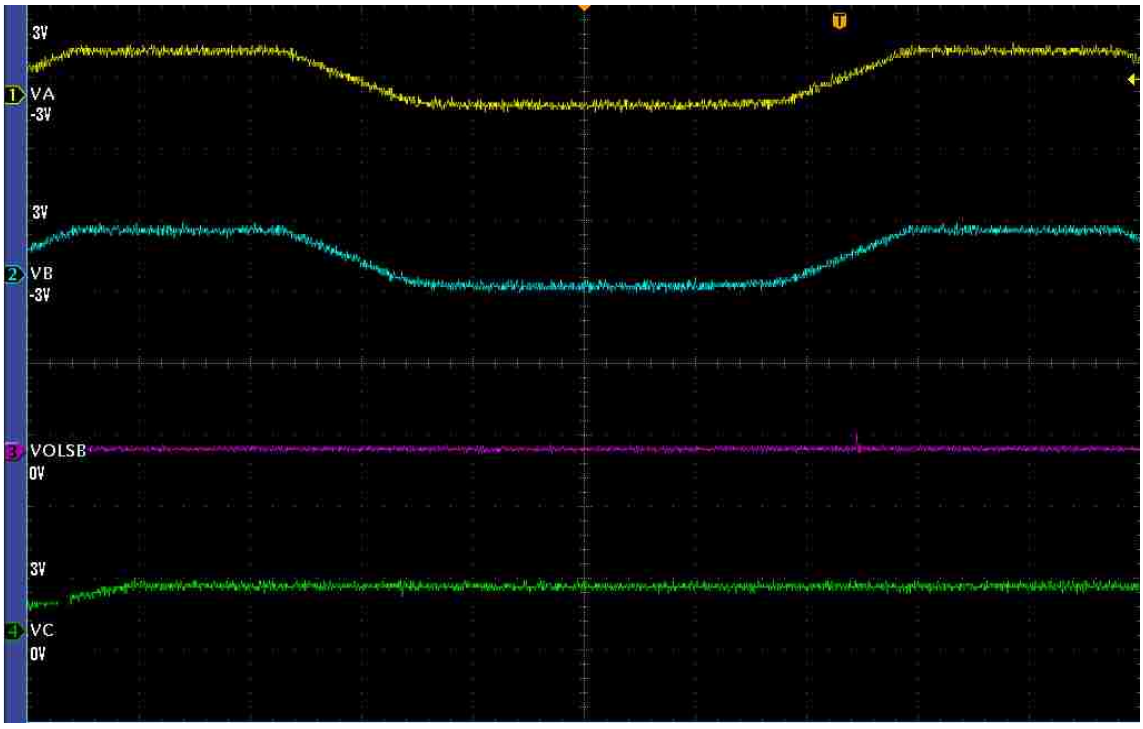

Figure 4.20: LSB output for the input $(-1,-1)_3$.

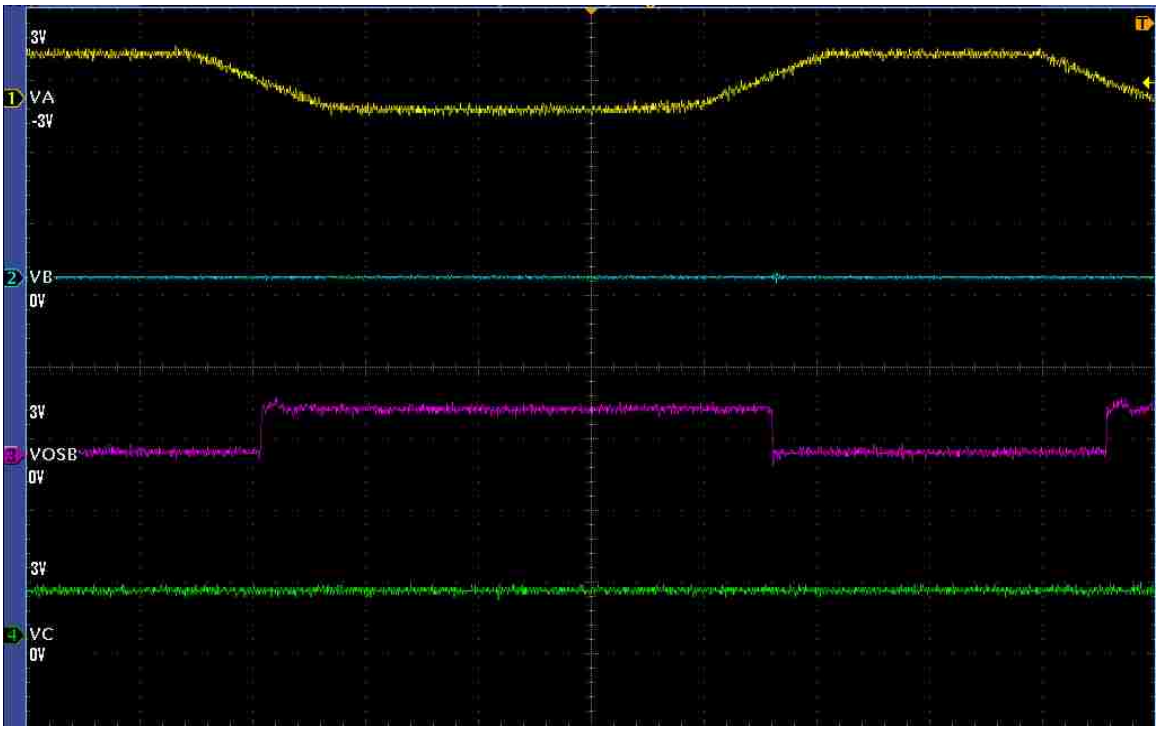

Figure 4.21: SB output for the input $(-1,0)_3$.

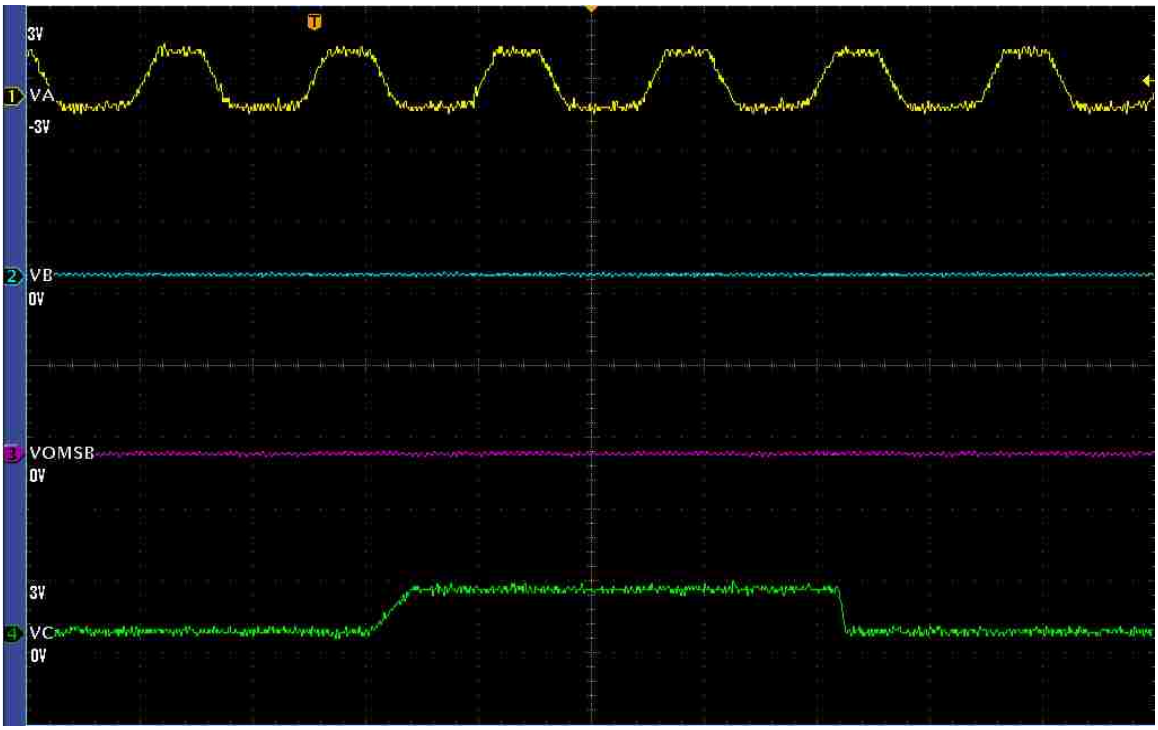

Figure 4.22: MSB output for the input $(-1,0)_3$.

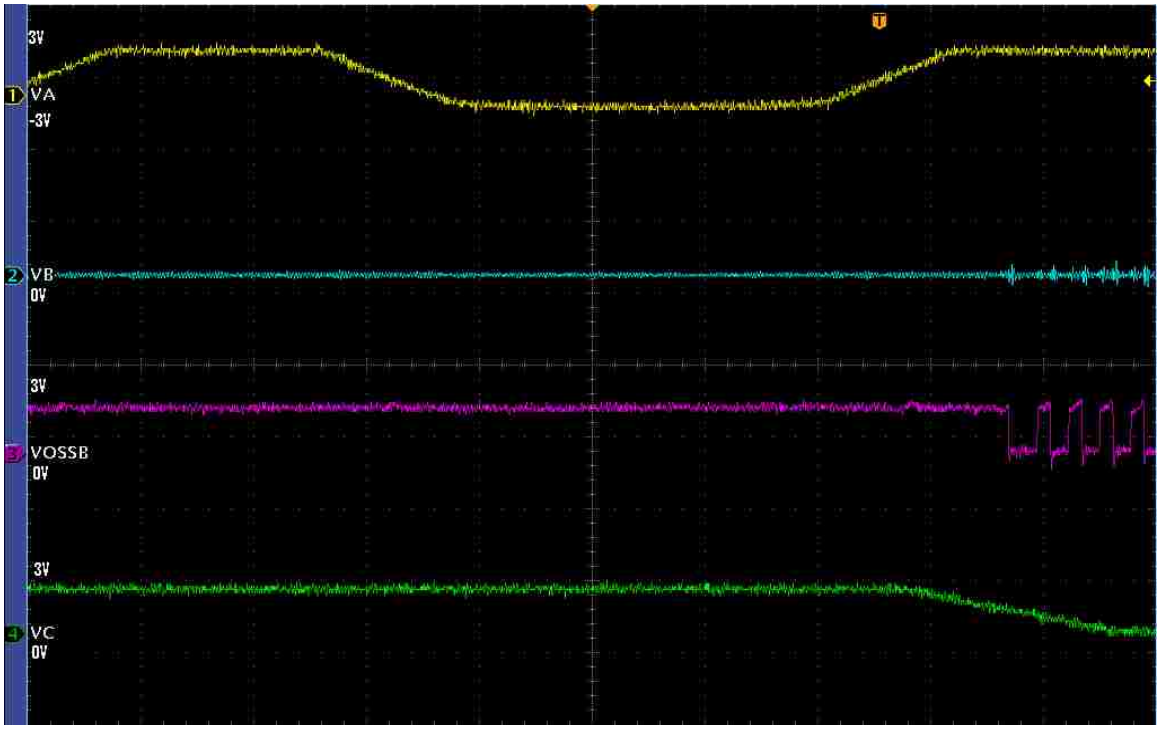

Figure 4.23: SSB output for the input $(-1,0)_3$.

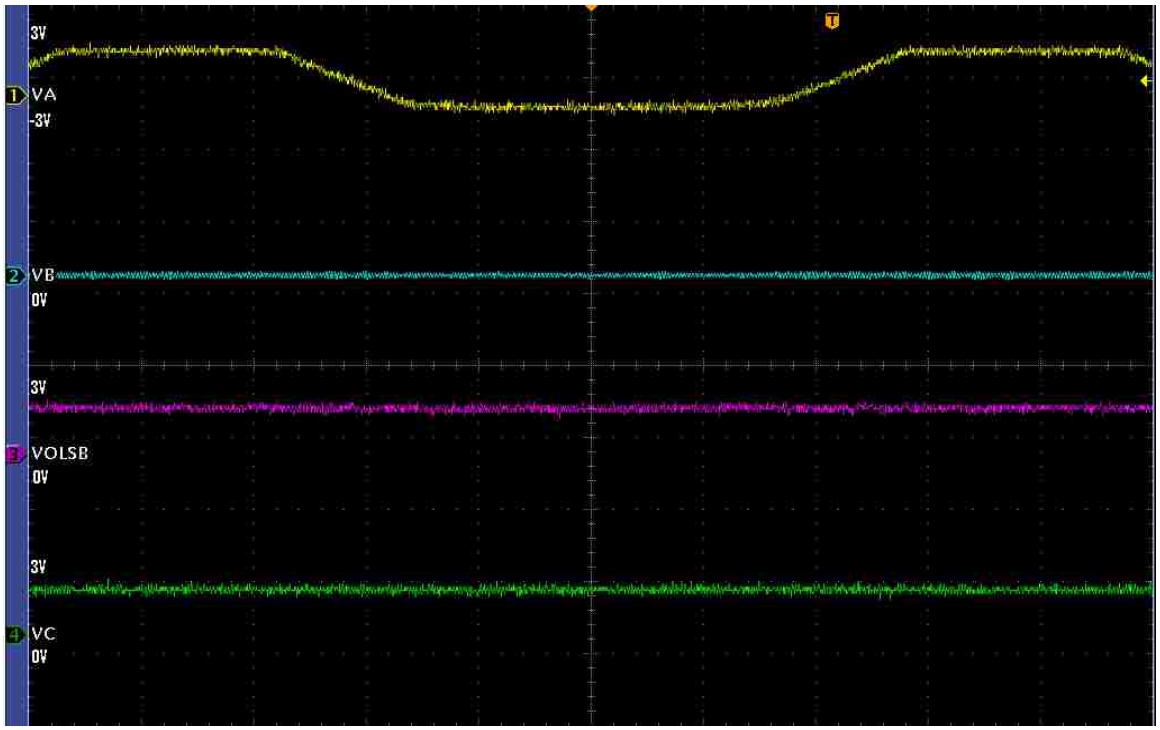

Figure 4.24: LSB output for the input $(-1,0)_3$.

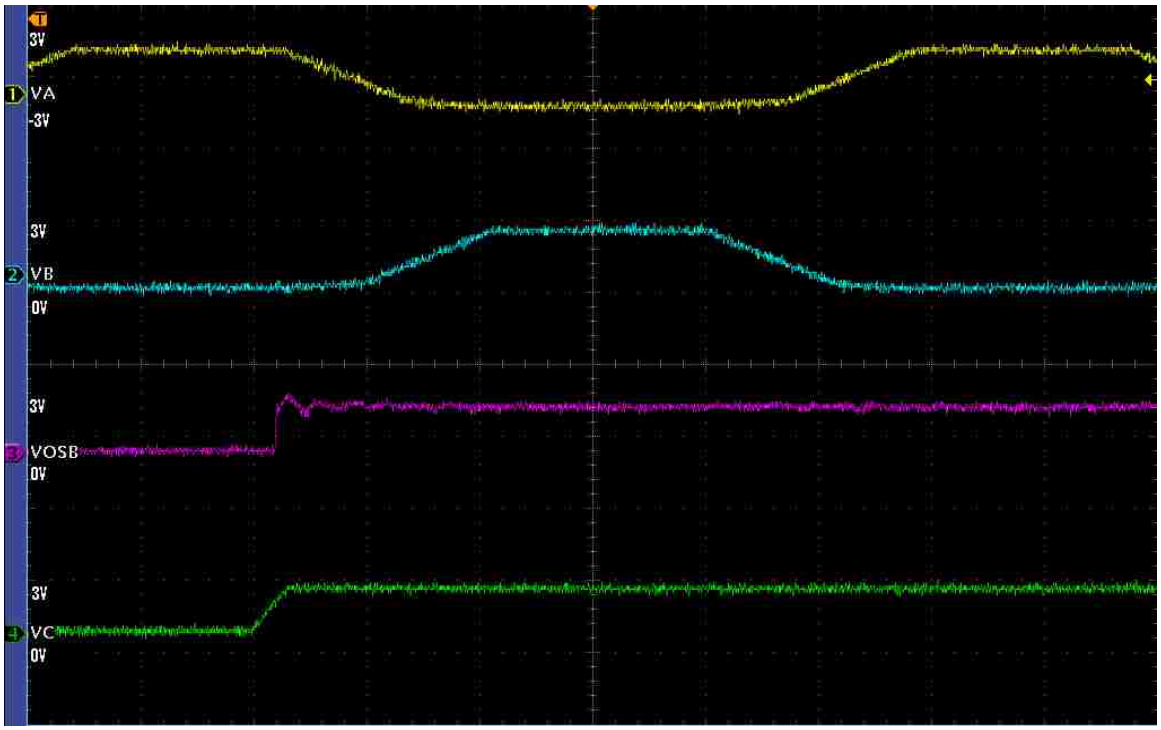

Figure 4.25: SB output for the input $(-1,1)_3$.

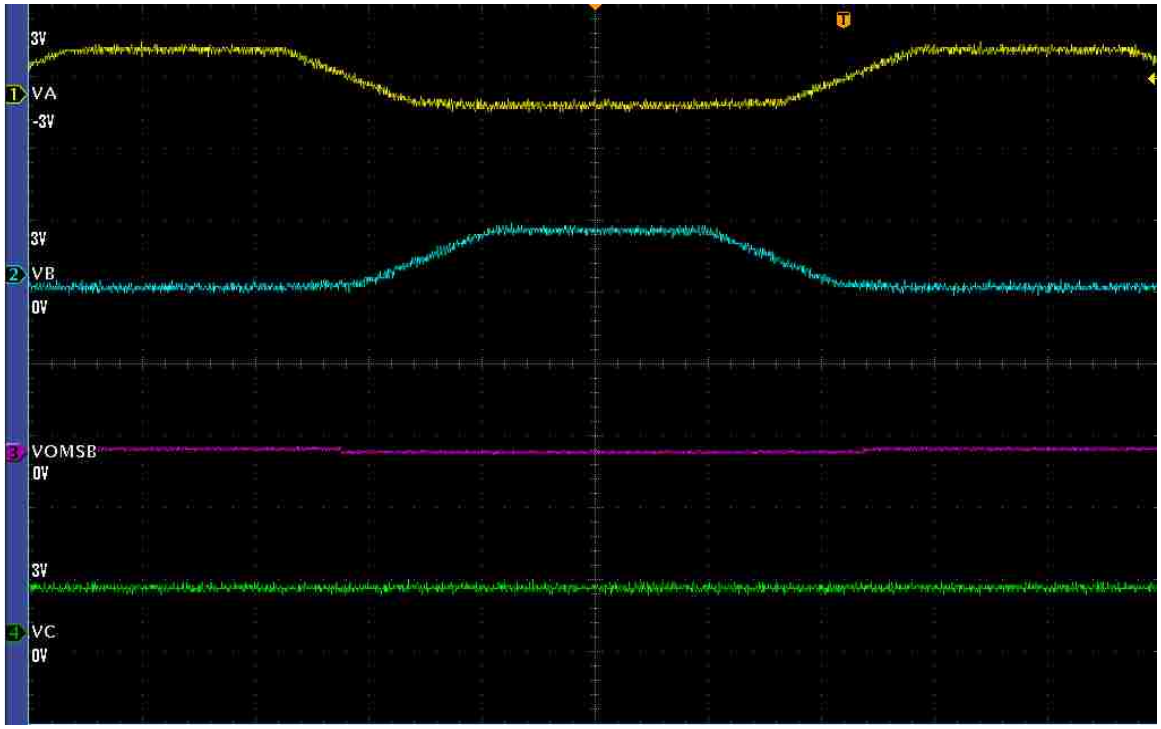

Figure 4.26: MSB output for the input $(-1,1)_3$.

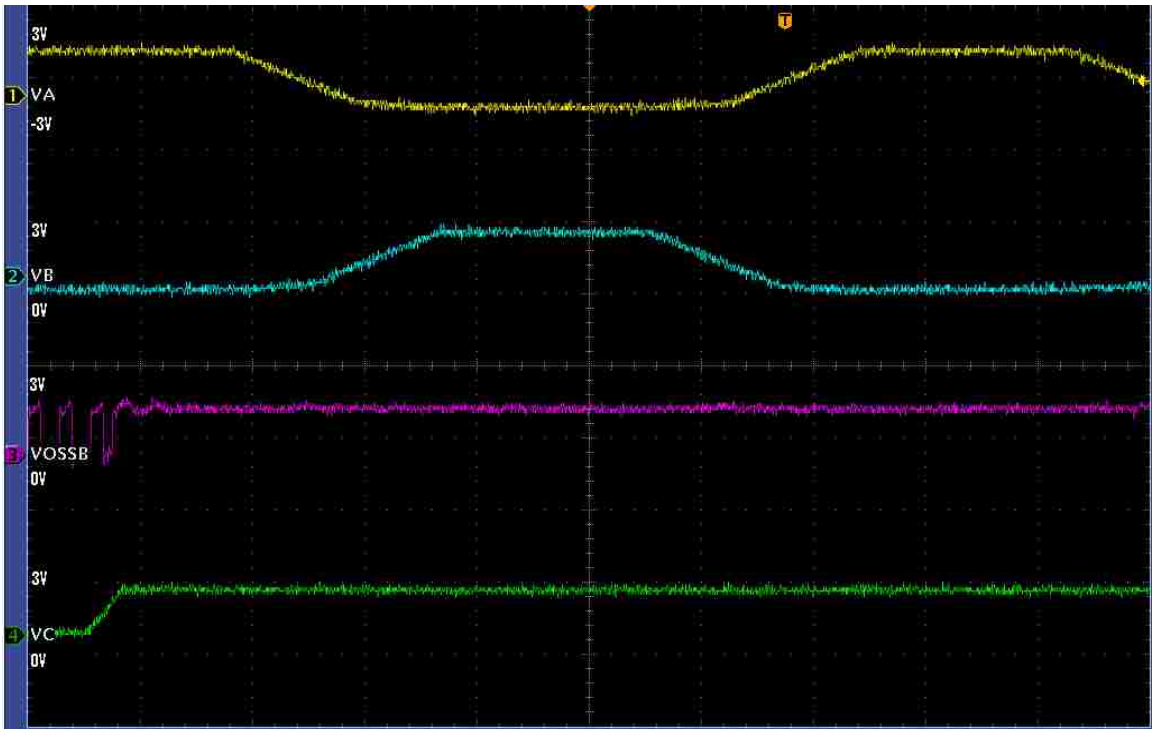

Figure 4.27: SSB output for the input $(-1,1)_3$.

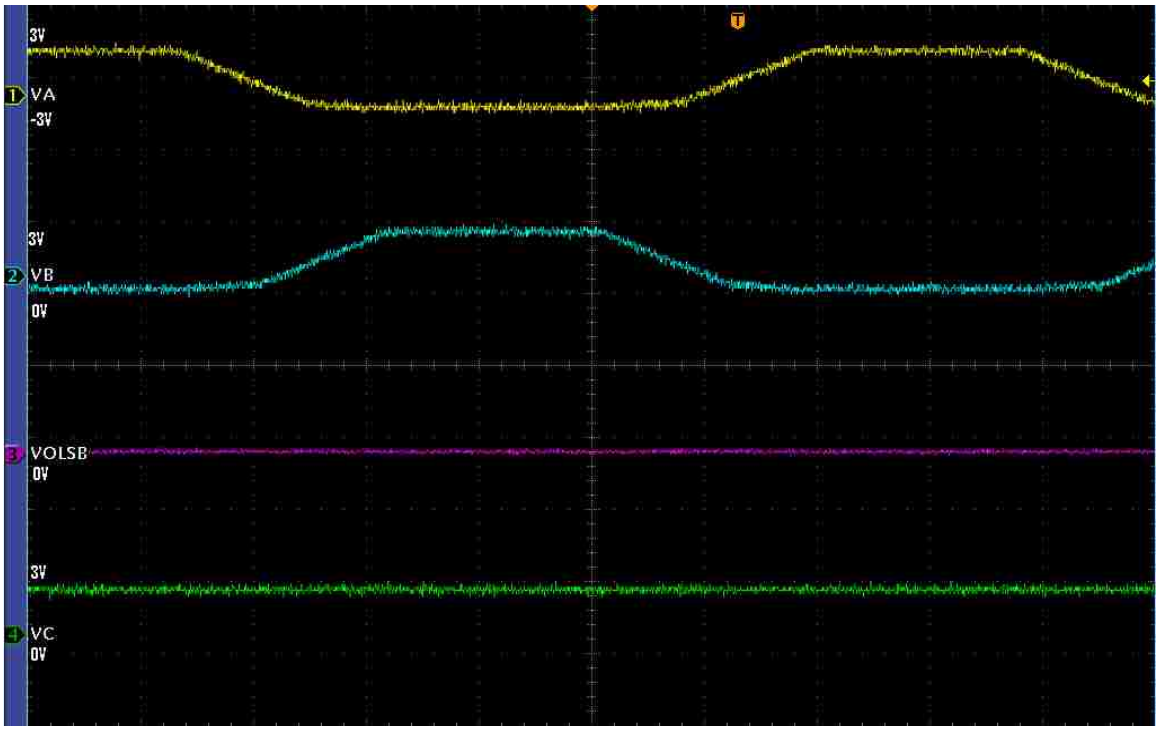

Figure 4.28: LSB output for the input $(-1,1)_3$.

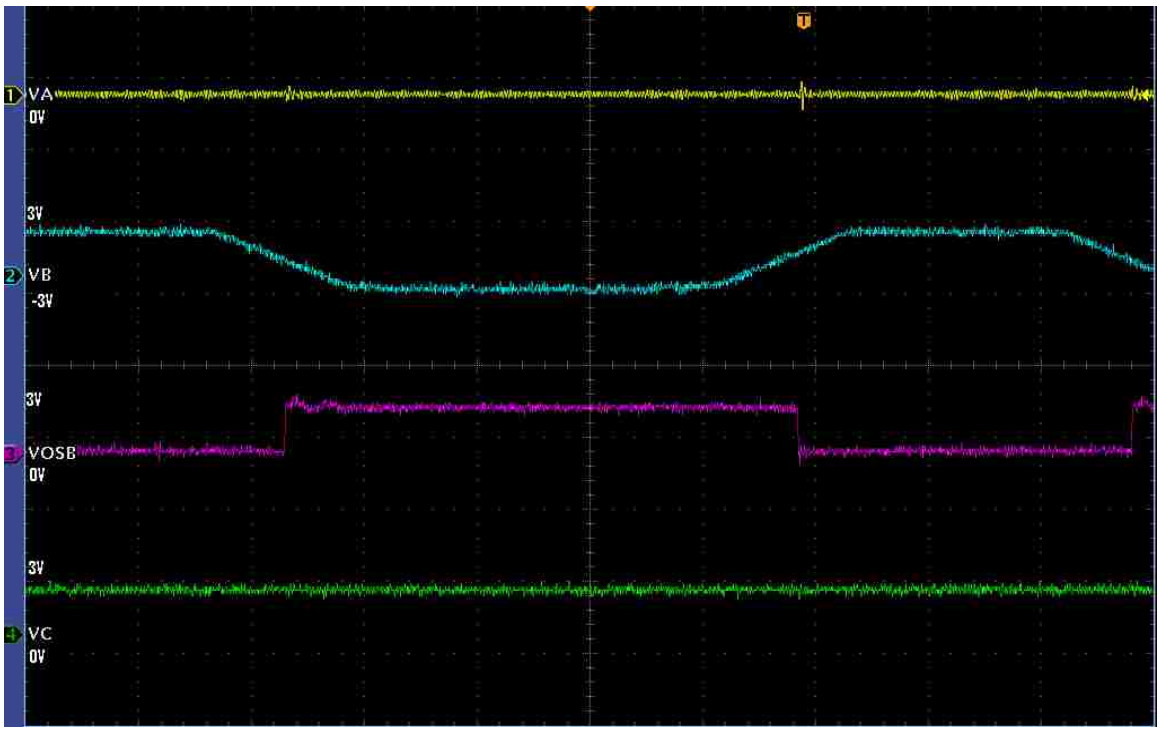

Figure 4.29: SB output for the input $(0,-1)_3$.

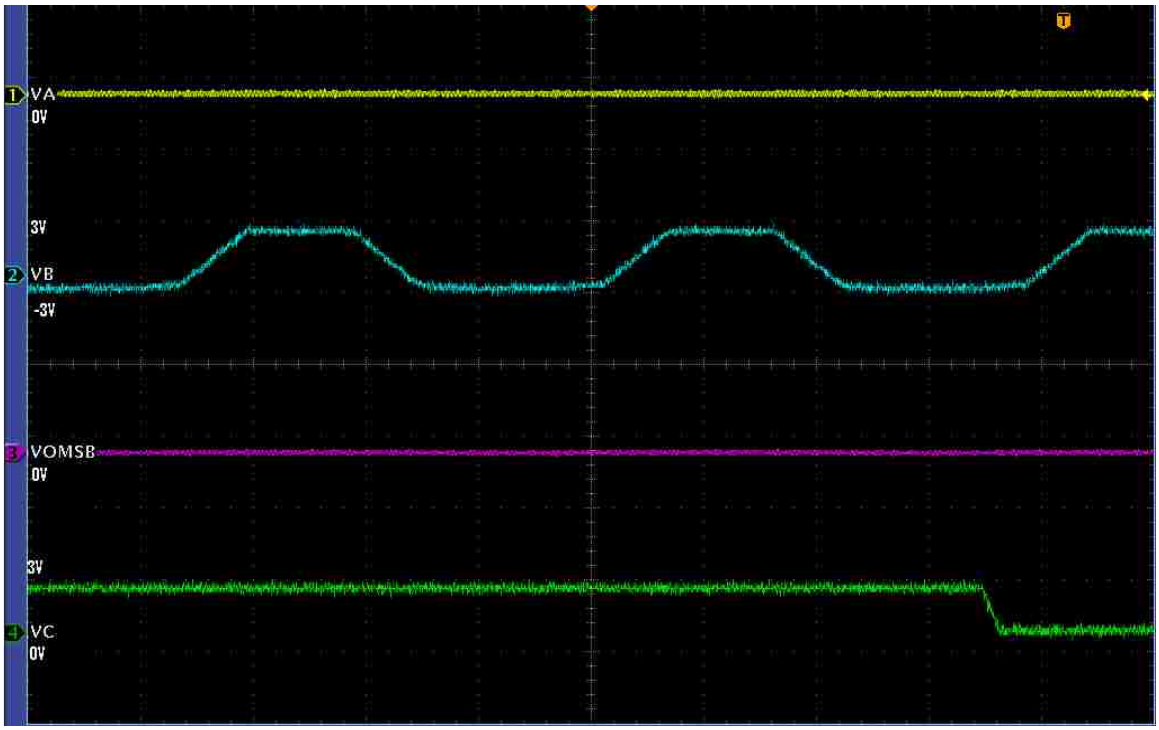

Figure 4.30: MSB output for the input $(0,-1)_3$.

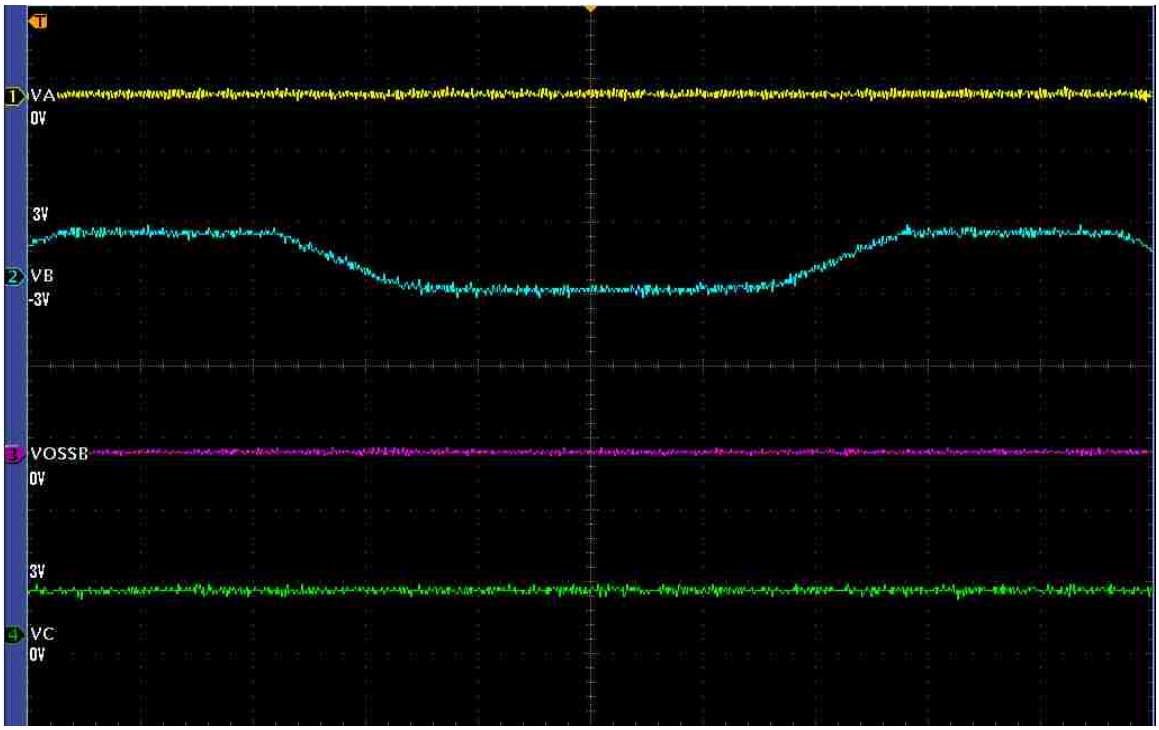

Figure 4.31: SSB output for the input $(0,-1)_3$.

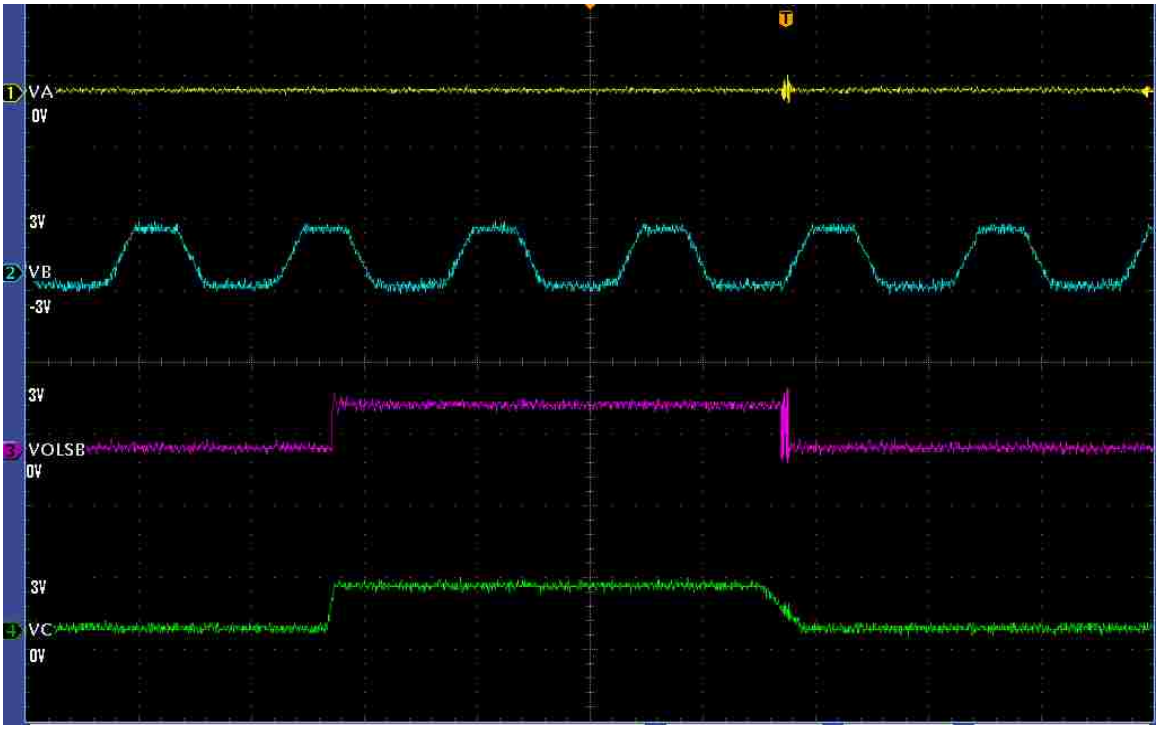

Figure 4.32: LSB output for the input $(0,-1)_3$.

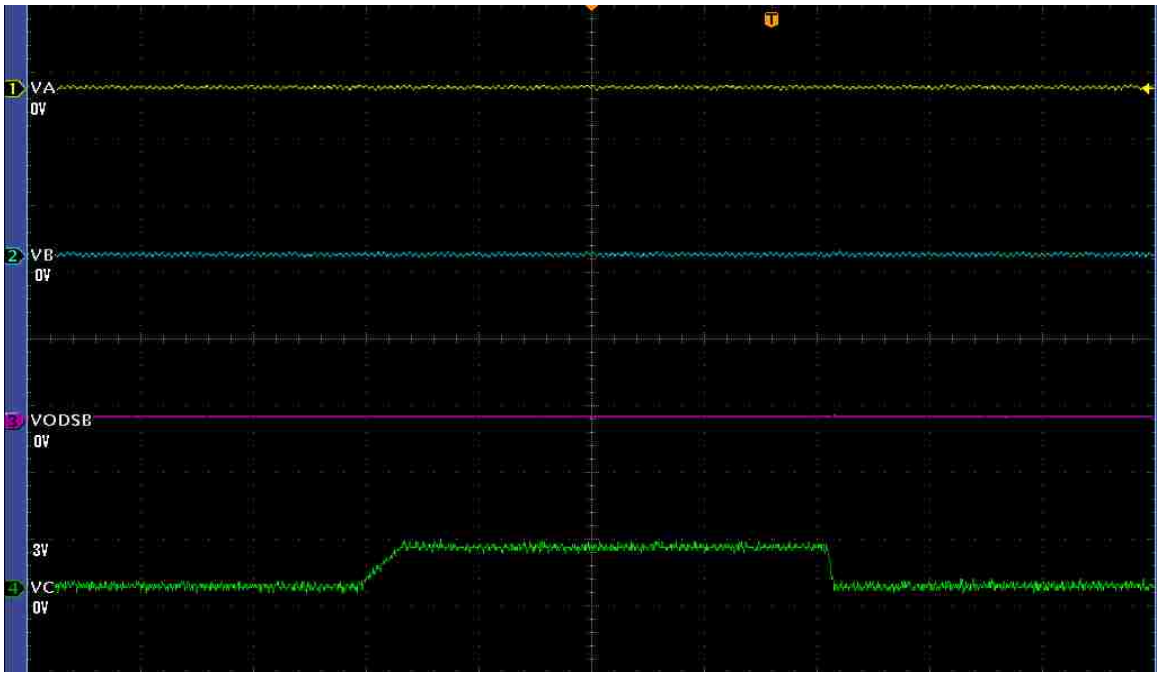

Figure 4.33: SB output for the input $(0,0)_3$.

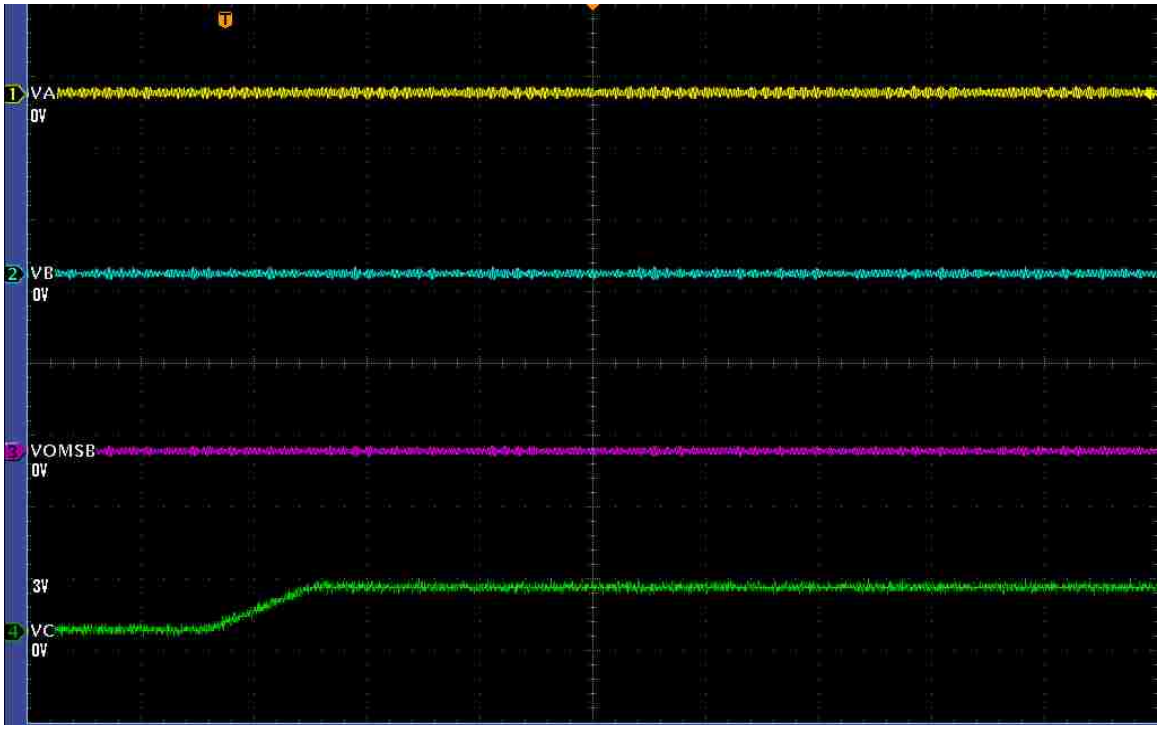

Figure 4.34: MSB output for the input $(0,0)_3$.

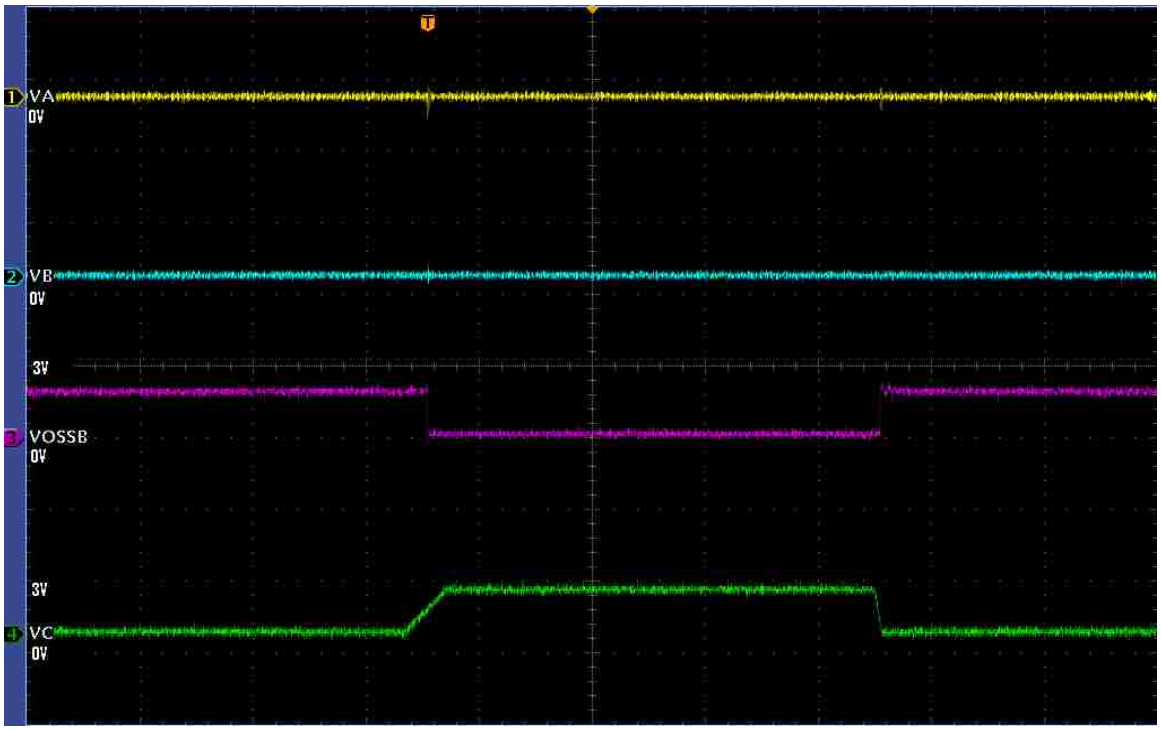

Figure 4.35: SSB output for the input $(0,0)_3$.

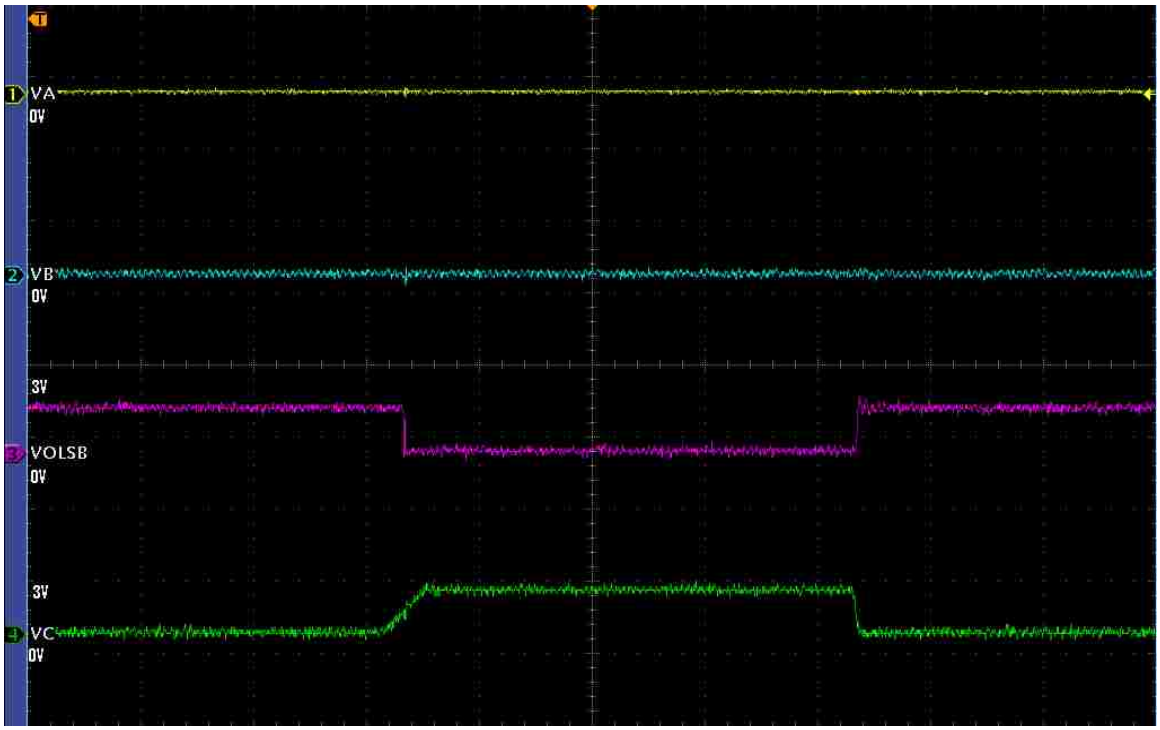

Figure 4.36: LSB output for the input $(0,0)_3$.

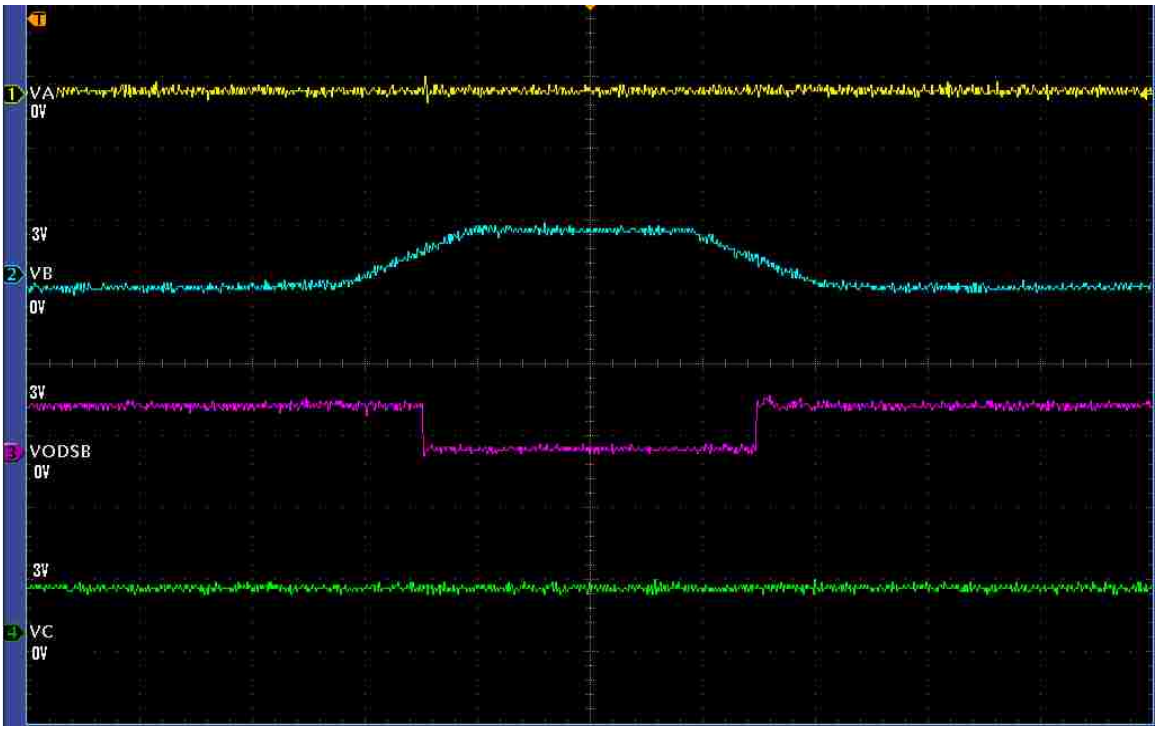

Figure 4.37: SB output for the input $(0,1)_3$.

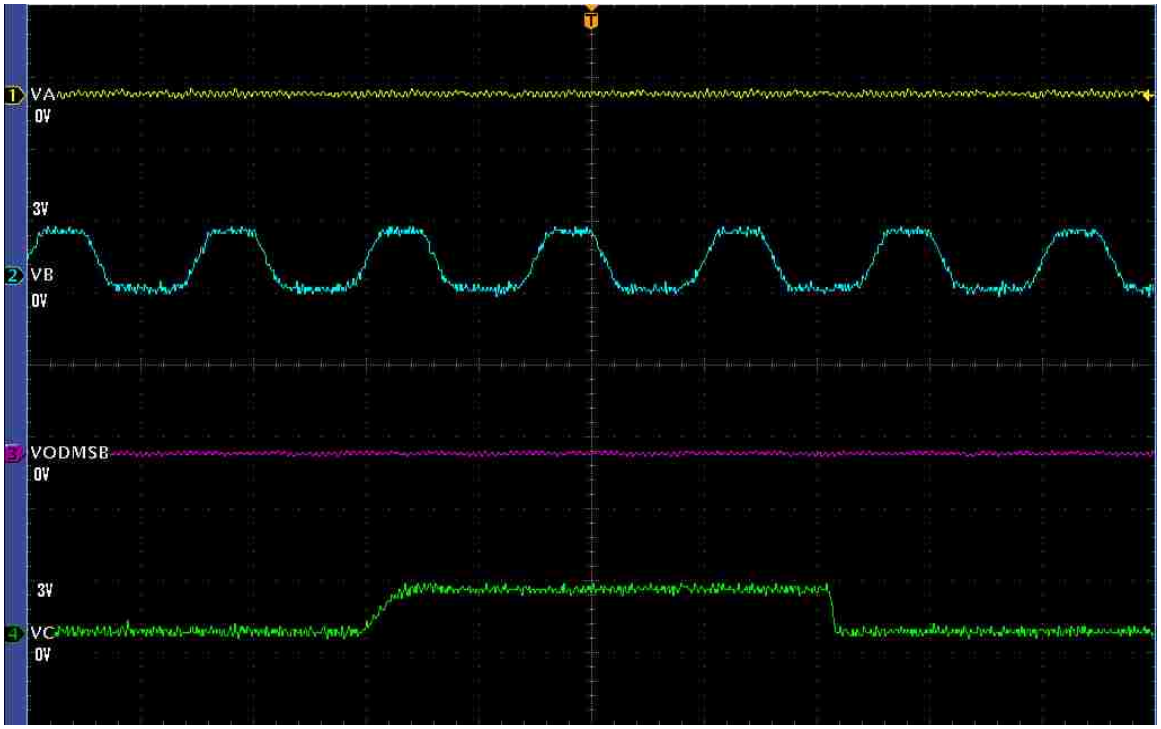

Figure 4.38: MSB output for the input $(0,1)_3$.

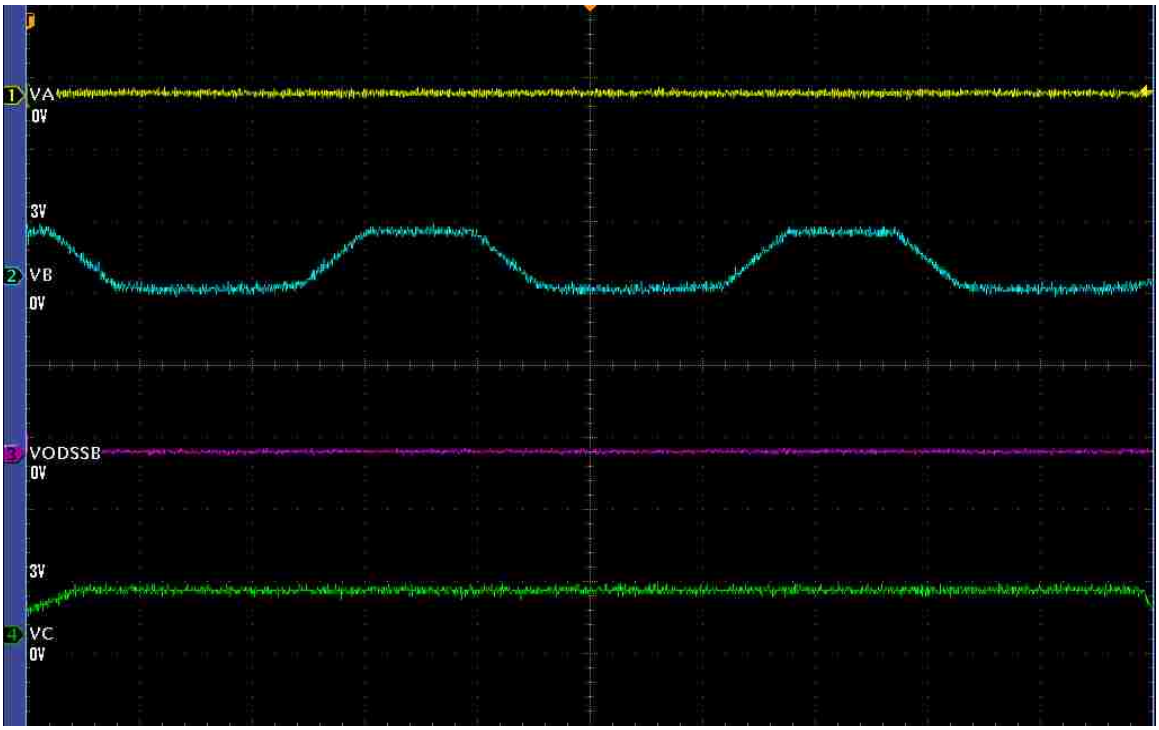

Figure 4.39: SSB output for the input $(0,1)_3$.

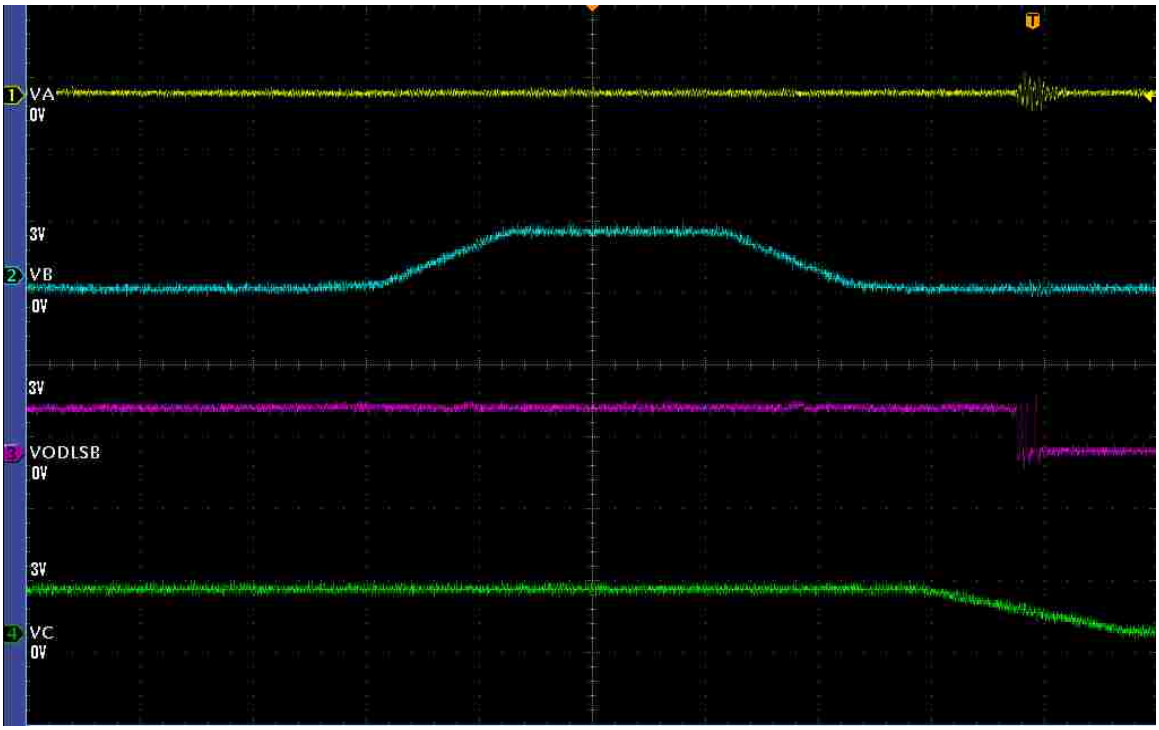

Figure 4.40: LSB output for the input $(0,1)_3$.

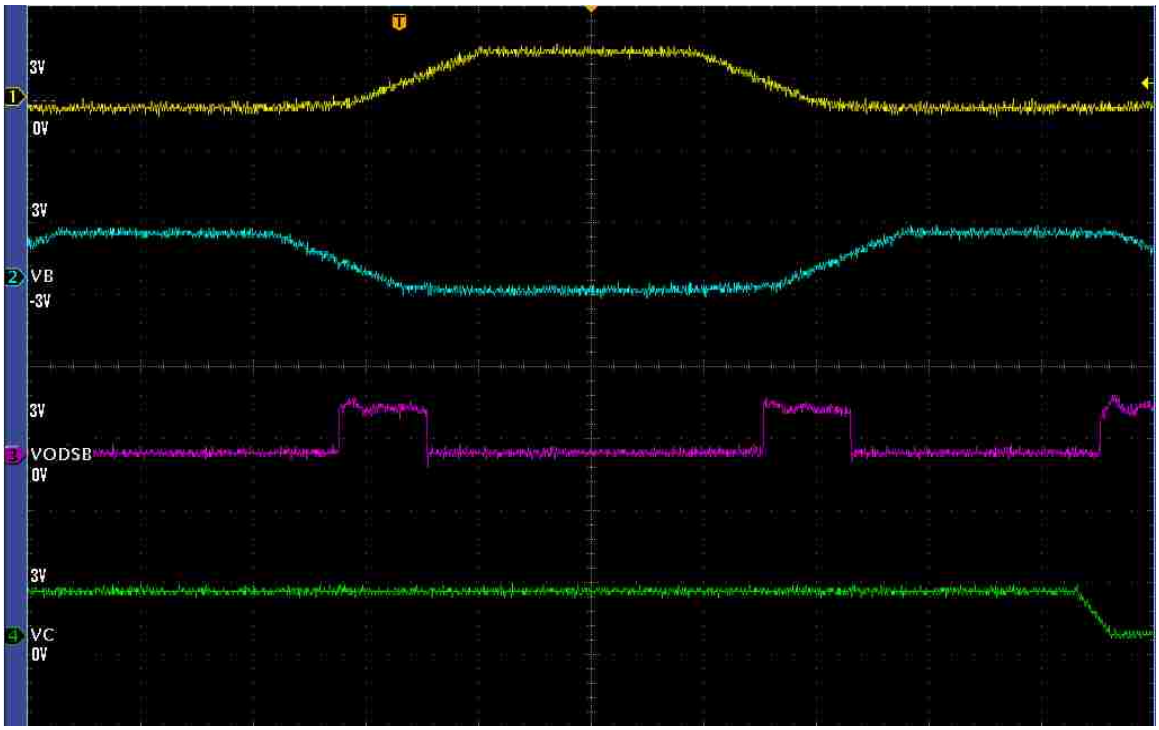

Figure 4.41: SB output for the input $(1,-1)_3$.

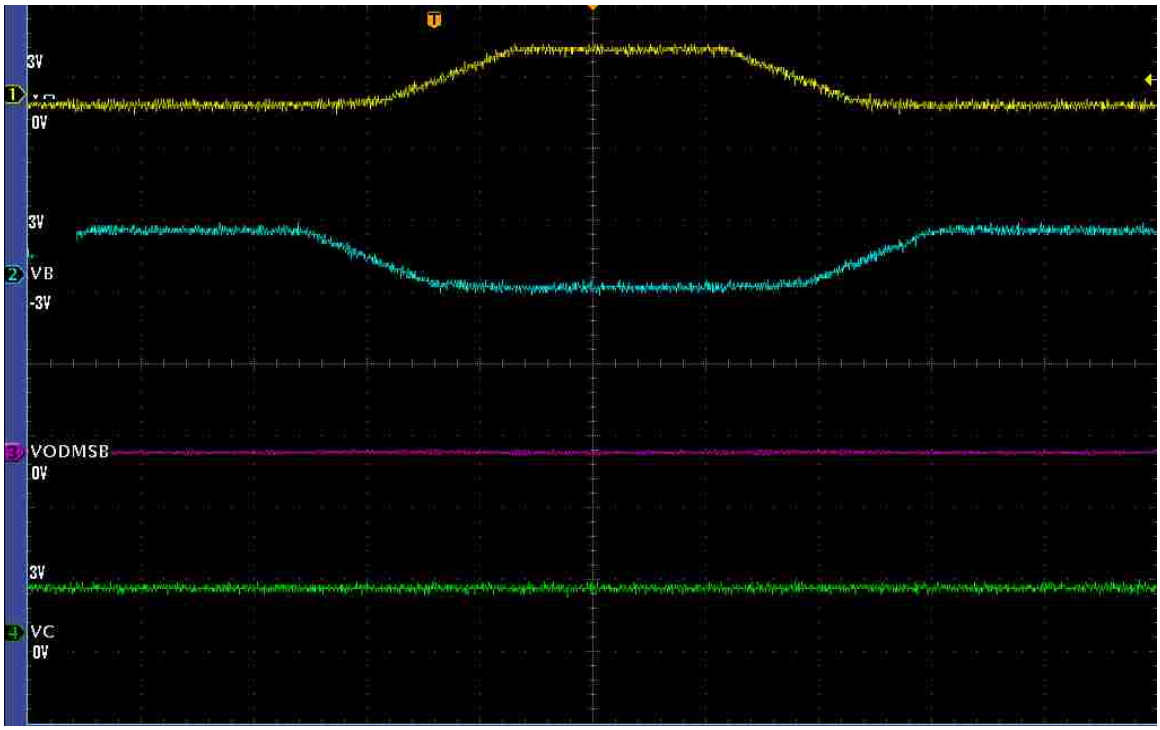

Figure 4.42: MSB output for the input $(1,-1)_3$.

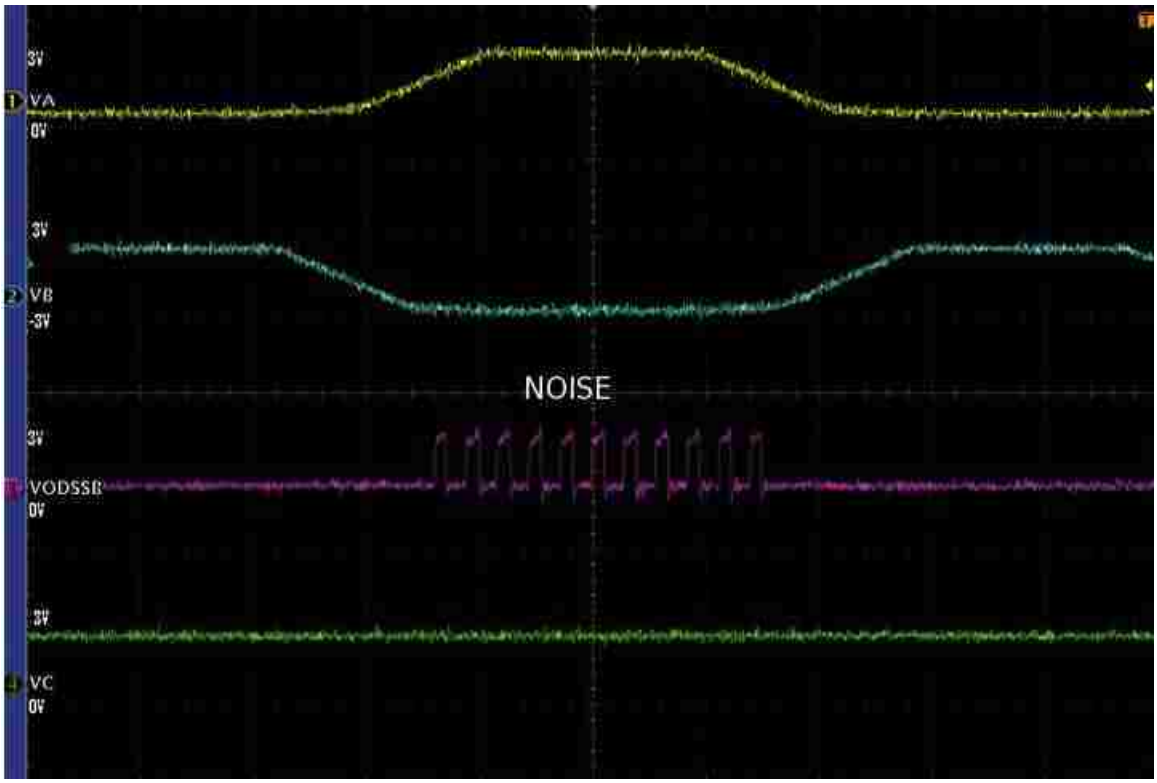

Figure 4.43: SSB output for the input $(1,-1)_3$.

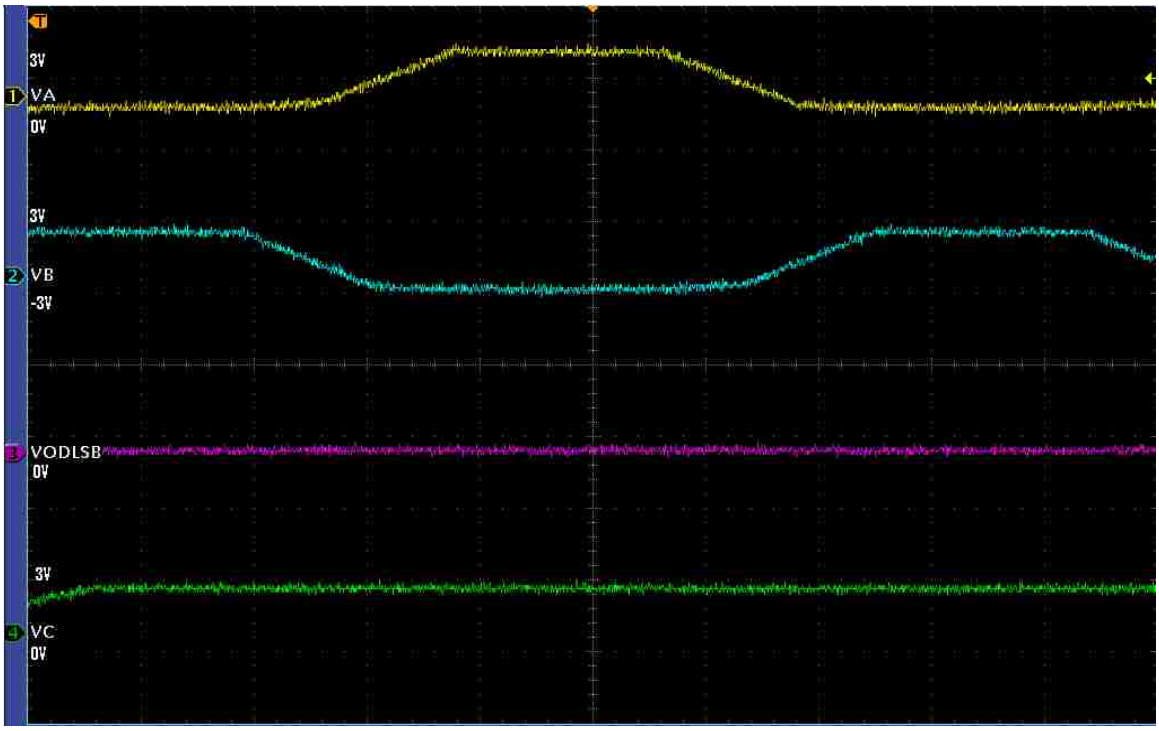

Figure 4.44: LSB output for the input $(1,-1)_3$.

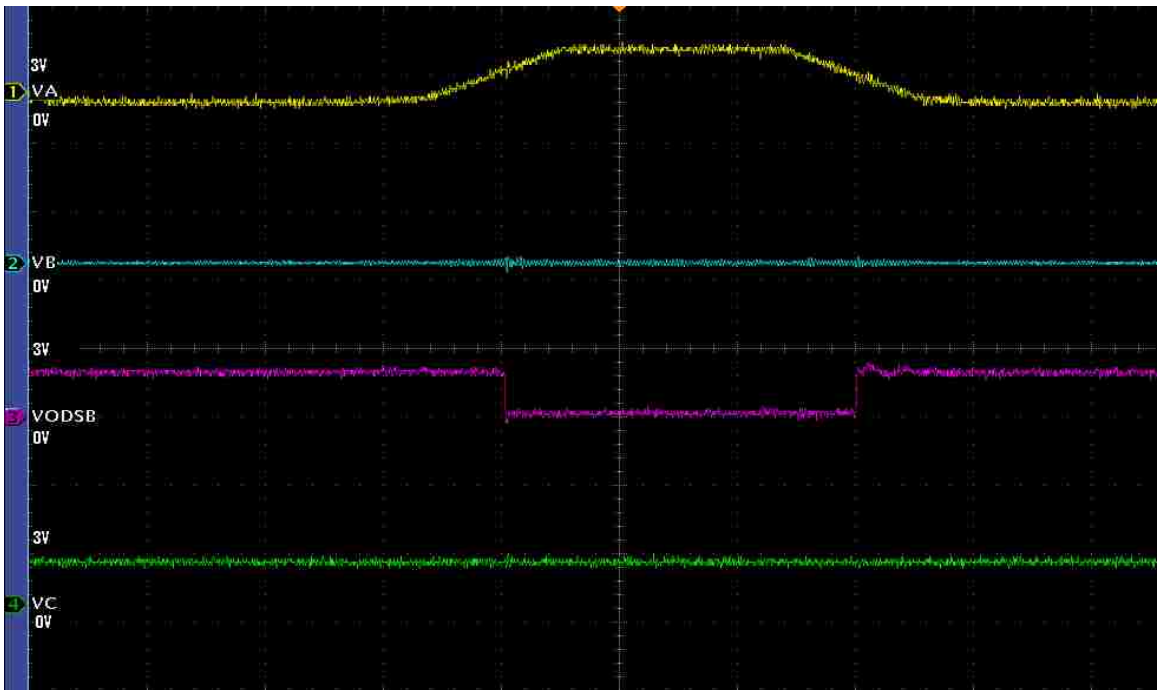

Figure 4.45: SB output for the input $(1,0)_3$.

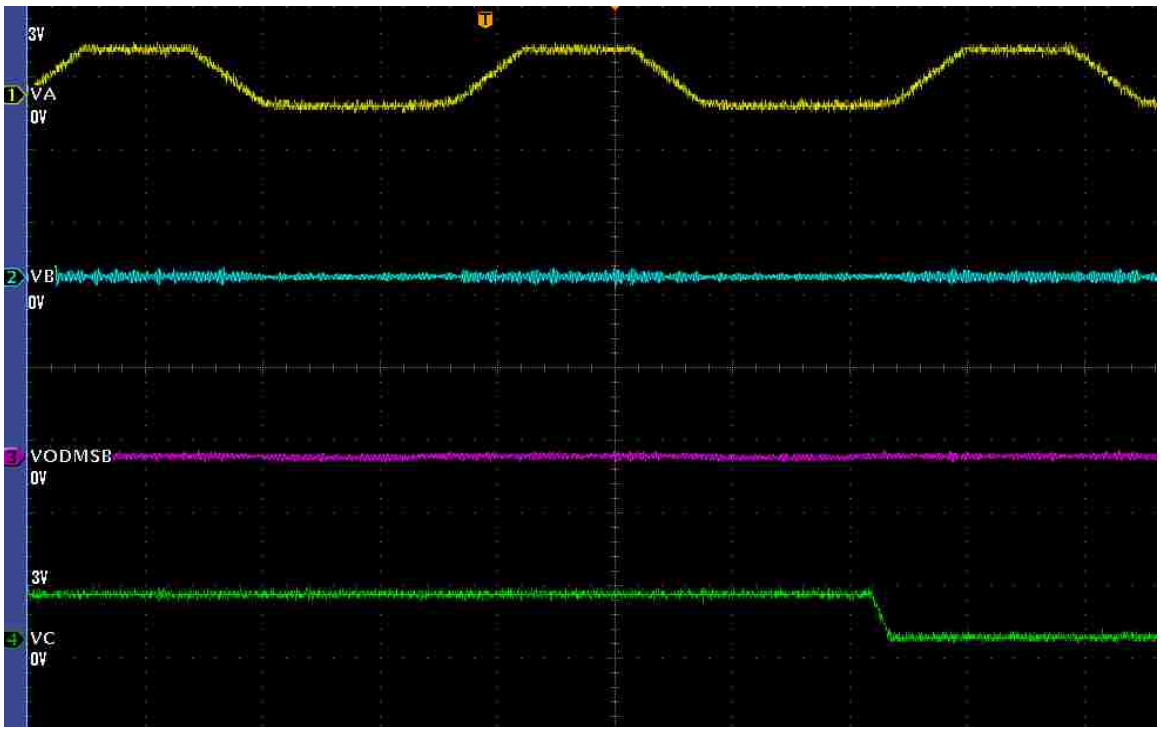

Figure 4.46: MSB output for the input $(1,0)_3$.

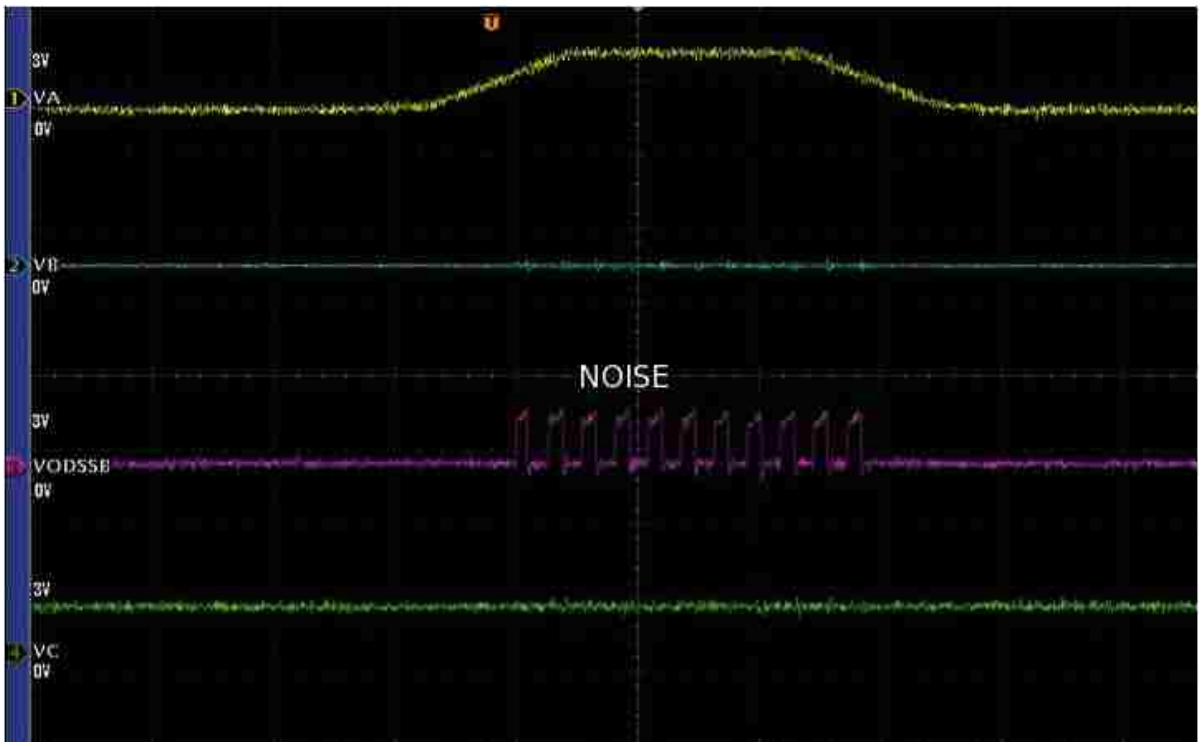

Figure 4.47: SSB output for the input $(1,0)_3$.

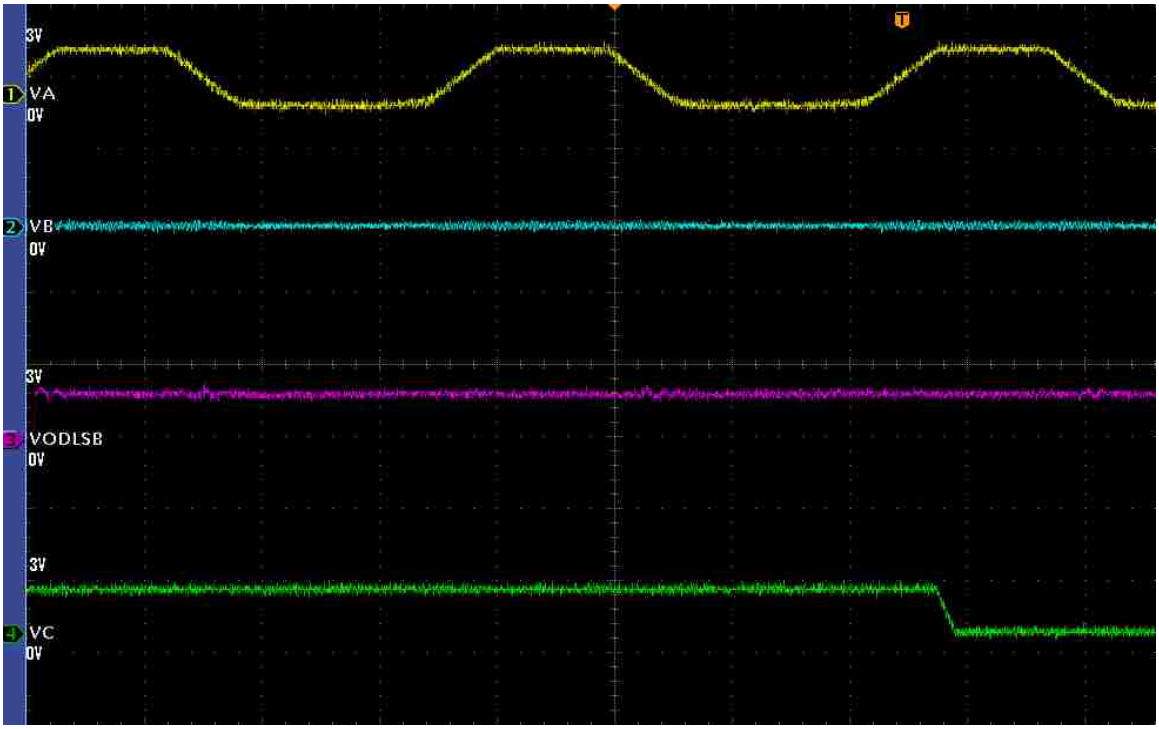

Figure 4.48: LSB output for the input $(1,0)_3$.

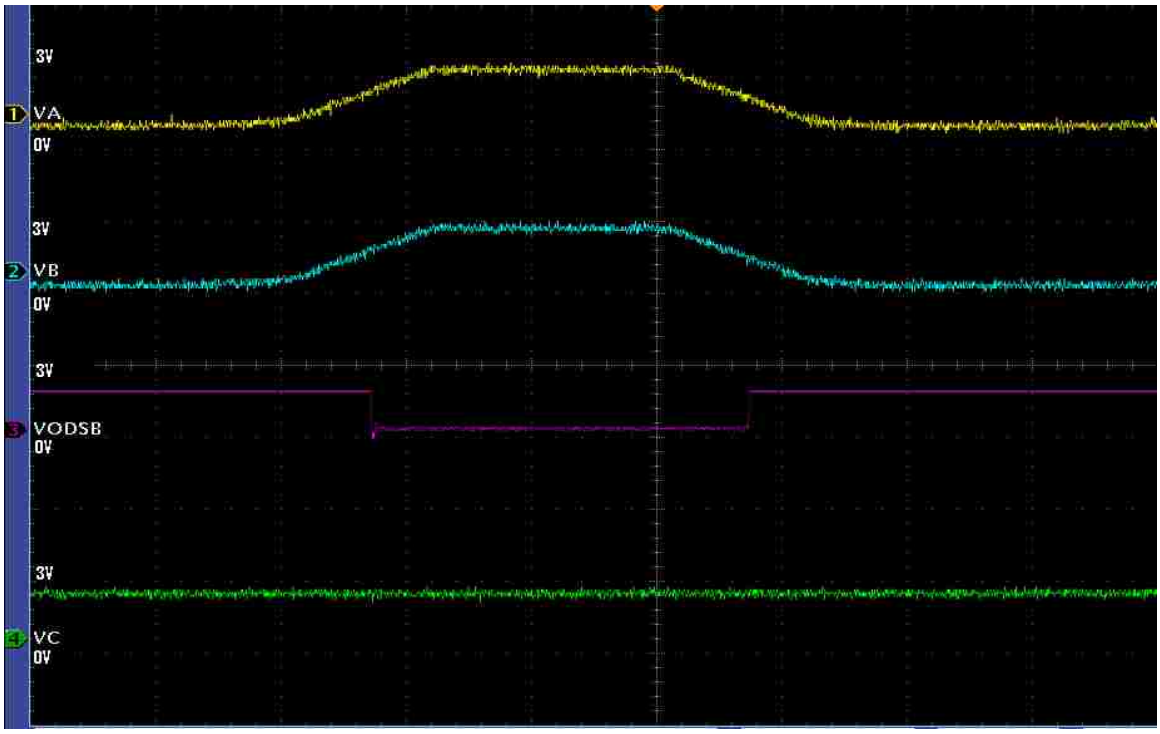

Figure 4.49: SB output for the input $(1,1)_3$.

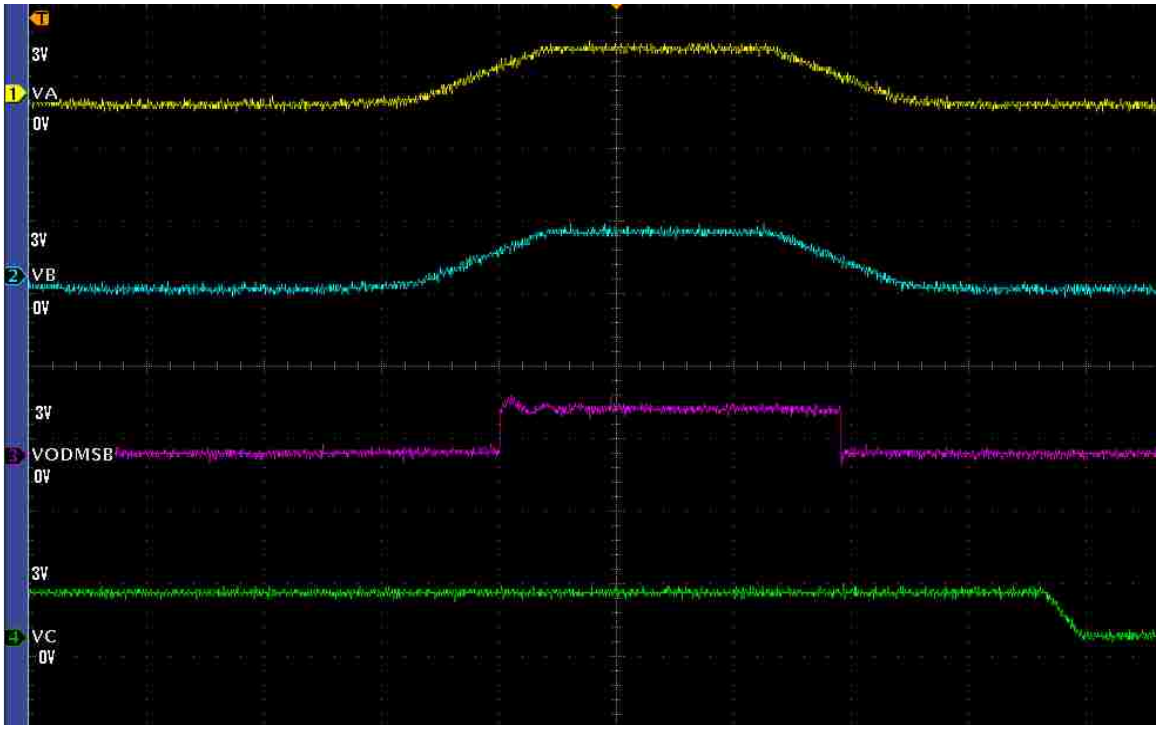

Figure 4.50: MSB output for the input $(1,1)_3$.

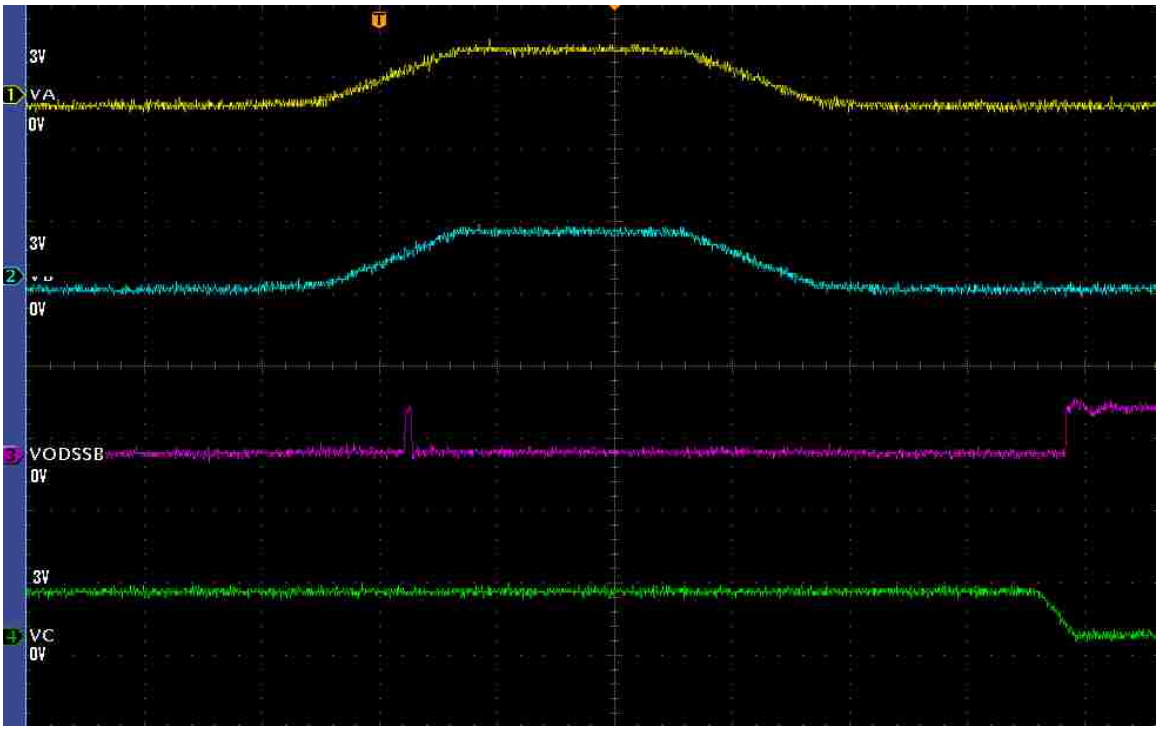

Figure 4.51: SSB output for the input $(1,1)_3$.

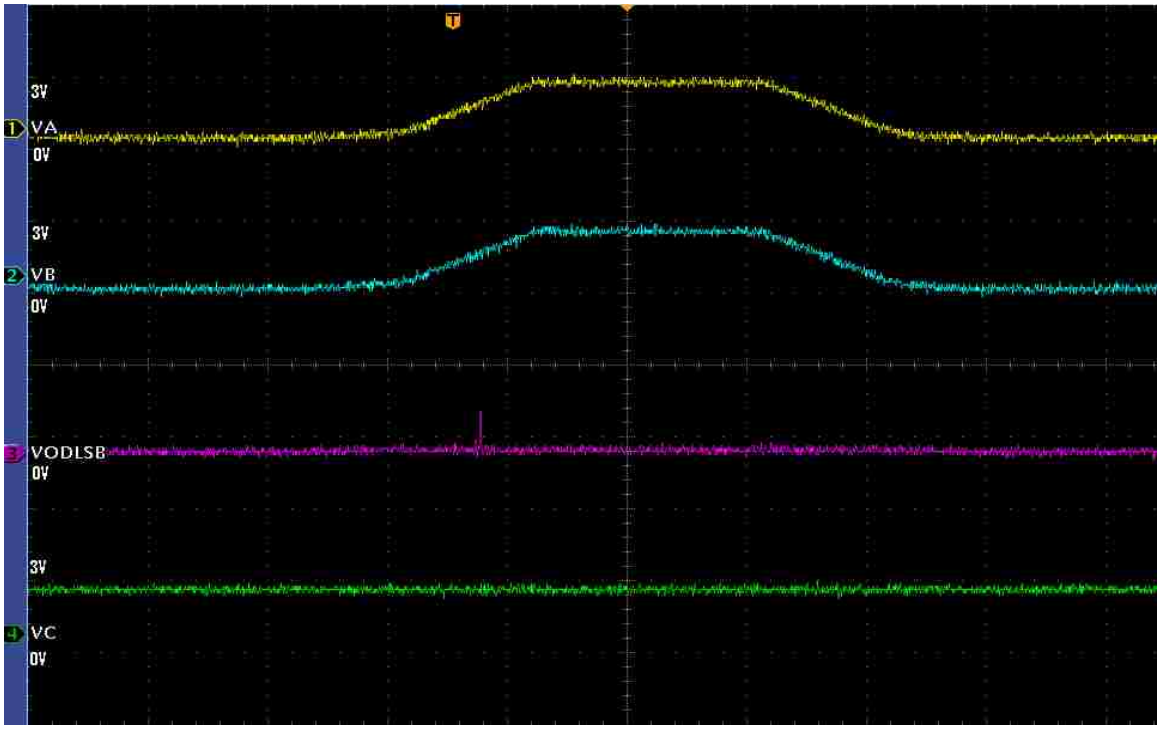

Figure 4.52: LSB output for the input $(1,1)_3$.

Table 4.2: Propagation delay for simulated and measured outputs.

Logic Level Transition (Ternary Logic)	SB (sim) μs	SB (meas) μs	MSB (sim) μs	MSB (meas) μs	SSB (sim) μs	SSB (meas) μs	LSB (sim) μs	LSB (meas) μs
-1→-1	0.059	0.060	0.049	-	-	-	-	-
-1→0	0.059	-	-	0.039	0.023	-	0.015	-
-1→1	-	-	-	-	0.034	-	-	-
0→-1	0.052	0.062	-	-	-	-	0.045	-
0→0	-	-	-	-	-	-	-	-
0→1	-	1.27	-	-	-	-	0.084	-
1→-1	0.076	0.093	0.033	-	0.016	-	0.020	-
1→0	-	0.051	-	-	-	-	0.062	-
1→1	-	0.19	0.0069	0.033	-	-	-	-

CHAPTER 5. CONCLUSIONS AND FUTURE WORK

5.1 Conclusion

In this thesis work, a circuit has been designed for the conversion of ternary logic to binary bits using multiple input floating gate MOSFETS in CMOS. The different stages of the converter are designed by first drawing the floating gate potential diagram. Three inputs, two of them input signals that vary based on the ternary inputs and the third a control signal, which is a constant 3V, is given to the converter circuit. Weighted sum of all inputs at each gate is calculated and is known as the floating gate voltage. The switching transistor turns ON or OFF depending on if the floating gate voltage is greater than or less than the switching threshold voltage of the transistor. In this work, the values the capacitors and the transistor sizing for each stage are chosen in such a way that each stage gives the expected output for the ternary inputs given. The circuit has been designed for balanced ternary logic (-1 0 +1), which is represented, by -3V, 0V and 3V. The minimum value of the capacitor used is 250fF fabricated in standard 0.5μm digital n-well CMOS technology. The circuits are simulated in Cadence PSPICE AD with MOSIS BSIM level 7 model parameters. L-Edit version 13.2 was used in layout and uses a total of 22 transistors. The converter chip occupies an area of 1140 X 2090 μm^2.

5.2 Future Work

In this work, the requirement for an external bias voltage to be supplied at the floating gate of the CMOS as stated in the previous work [20] is no longer needed and hence is more adaptive. The common-centroid design was not used in this work because of the need to use capacitors that were not multiples of a unit capacitor, which in this case would have been 250fF. Use of common-centroid design of the capacitors in this work will help reduce parasitic capacitances and effect of noise on the circuit. Integration of different converter systems like integration of a quaternary [22] and ternary to binary system can also be explored.

BIBLIOGRAPHY

1. S. L. Hurst, "Multiple-valued logic – its status and its future," *IEEE Transactions on Computers*, vol. C-33, December 1984, pp. 1160-1179.

2. K. C. Smith, "The prospects for multivalued logic: A technology and applications view," *IEEE Transactions on Computers*, vol. C-30, No. 9, September 1981, pp. 619-634.

3. X. W. Wu, "CMOS ternary logic circuits," *IEE Proceedings on Devices, Circuits and Systems*, vol. 137, No. 1, February 1990, pp. 21-27.

4. D. E. Knuth, "The Art of Computer Programming – *Volume 2: Seminumerical Algorithms,*" Addison-Wesley, 2nd ed., 1980, pp.190-192.

5. H. N. Venkata, Ternary and Quaternary Logic to Binary Bit Conversion CMOS Integrated Circuit Design Using Multiple Input Floating Gate MOSFETS, M.S (E.E.) Thesis, Louisiana State University, 2002.

6. D. Olson and K. W. Current, "Hardware implementation of supplementary symmetrical logic circuit structure concepts," *Proceedings of 30th International Symposium of Multiple-Valued Logic*, May 2000, pp. 371-376.

7. F. Ueno, T. Inoue, K. Sugitani and Shinji Araki, "A programmable switched- capacitor circuit for multivalued-to-binary and binary-to- multivalued conversions," *Proceedings of Multiple-Valued Logic*, 1989, pp. 195-201.

8. T. Shibata and T. Ohmi, "An intelligent MOS transistor featuring gate-level weighted sum and threshold operations," in *IEDM Tech. Dig.,* 1991, pp. 919-922.

9. B. A. Minch and P. Hasler, "A floating gate technology for digital CMOS processes," *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. 2, June 1999, pp. 400-403.

10. A. F. Mondragon-Torres, M. C. Schneider and E. Sanchez-Sinencio, "Well driven floating gate transistors," *Electronic Letters*, vol. 38, no. 11, 23rd May 2002, pp. 530-532.

11. M. Kucic, P. Hasler and P. Smith, "Design and use based on long-term measurements of analog floating-gate array circuits", *The 45th Midwest Symposium on Circuits and Systems*, vol. 1, August 2002, pp. 295-298.

12. Y. Zhai, P. A. Abshire "Adaptive log domain filters for system identification using floating gate," *Analog Integrated Circuits and Signal Processing,* vol. 56, Issue 1-2, August 2008, pp. 23-36.

13. R. Sehgal, S. S. Rajput "A low voltage 8-bit digital-to-analog converter using floating gate MOSFETS," *Analog Integrated Circuits and Signal Processing,* vol. 56, Issue 3, September 2008, pp. 199-203.

14. S. Sharma, S. S. Rajput "FGMOS current mirror: behavior and bandwidth enhancement," *Analog Integrated Circuits and Signal Processing,* vol. 46, no. 3, March 2006, pp. 281-286.

15. G. Neng Lu, A. Tournier, F. Roy, B. Deschamps "1T pixel floating-body MOSFET for CMOS image sensors," *Sensors,* vol. 9, Issue. 1, January 2009, pp. 1-695.

16. H. M. Chou, J. W. Lee, Y. Li "A floating gate design for electrostatic discharge protection circuits," *Integration, the VLSI journal,* vol. 40, Issue 2, February 2007, pp. 161-166.

17. Z. Lu, J. G. Fossum, W. Zhang, W. P. Trivedi "A novel two transistor floating – body/gate cell for low power nanoscale embedded DRAM," *IEEE Transactions on Electron Devices,* vol. 55, No.6, June 2008, pp. 1511-1518.

18. Z. Lu, J. G. Fossum, W. Zhang, H. R. Harris, W. P. Trivedi, M. Chu, S. E. Thomson "A simplified, superior floating body/gate DRAM cell", *IEEE Electron Device Letters,* vol. 30, March 2009, pp. 282-284.

19. T. Shibata and T. Ohmi, "A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations", *IEEE Transactions on Electron Devices*, vol 39, no. 6, June 1992, pp. 1444 – 1455.

20. S. Subramanian, "Ternary logic to binary bit conversion using multiple input floating gate MOSFETS in 0.5 micron N-well CMOS, M.S (E.E.) Thesis, Louisiana State University, 2005.T.

21. Shibata and T. Ohmi, "Neuron MOS Binary-Logic Integrated Circuits- Part I : Design fundamentals and soft hardware-logic circuit implementation," *IEEE Transactions on Electron Devices*, vol.40, no.3, March 1993, pp 570-576G.

22. A. Srivastava, H. N. Venkata, "Quaternary to binary bit conversion CMOS integrated circuit design using multiple-input floating gate MOSFETS," *The VLSI Journal Integration*, vol. 36, Issue 3, October 2003, pp. 87-101.

23. Zhenqiu Ning, L. De Schepper, R. Gillon and M. Tack, "A floating gate AC nulling (FGAN) technique for characterization of matching properties of MOS capacitors," *IEEE 33rd Conference on European Solid-State Device Research*, September 2003, pp 79-82.

24. W. Weber, S. J. Prange, R. Thewes, E. Wohlrab, "A neuron MOS transistor- based multiplier cell," *IEDM Digest*, 1995, pp. 555 – 558 .

APPENDIX A: INPUT CIRCUIT FILES

A.1 To Find the Transfer Characteristics of the CMOS Inverter

```
NODE NAME ALIASES
1 = VOUTINV (40.6 , 16.8)
2 = VDD (19.6 , 53.6)
3 = VSS (19.3 , -3.3)
4 = VINV (27.4 , 17.4)
VDD 2 0 3v
VSS 3 0 0v
VINV 4 0 DC 3 PWL ( 0ns 0v 120ns 3v)
.DC VINV 0 3.0 0.5
.probe
.END
```

A.2 To Find the Output of the Ternary to Binary Converter

```
VVDD 9 0 3V
VGND 4 0 0V
VA2 6 0  PULSE(0V 3V 600nS 600nS 600nS 600nS 3000nS)
VB2 5 0 PULSE(3V  -3V 600nS 600nS 600nS 600nS 3000nS)
VC2 7 0 PULSE(0V 3V 0S 600nS 100nS 6000nS 6000nS)
VINVPAD 194 0 0V
.tran 1nS 6000nS
.probe
R11  70 0 1E20
R12  79 0 1E20
R13  78 0 1E20
R14  118 0 1E20
R15  109 0 1E20
R16  104 0 1E20
R17  150 0 1E20
R18  149 0 1E20
R19  167 0 1E20
R20 125 0 1E20
.IC V(89) 0V
.IC V(117) 0V
.IC V(116) 0V
.IC V(136) 0V
.IC V(154) 0V
.IC V(153) 0V
.END
```

APPENDIX B: MOSFET MODEL PARAMETERS

B.1 NMOS Model Parameters for 0.5μm Technology

```
.MODEL NMOS NMOS (                      LEVEL   = 7
+VERSION = 3.1          TNOM    = 27            TOX     = 1.42E-8
+XJ      = 1.5E-7       NCH     = 1.7E17        VTH0    = 0.5974554
+K1      = 0.9398437    K2      = -0.1120602    K3      = 26.790632
+K3B     = -8.9497542   W0      = 1.129584E-8   NLX     = 1E-9
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 0.7537178    DVT1    = 0.3372918     DVT2    = -0.4998894
+U0      = 449.3659707  UA      = 1E-13         UB      = 1.387457E-18
+UC      = 1.053526E-12 VSAT    = 1.618503E5    A0      = 0.6727779
+AGS     = 0.1270399    B0      = 2.111191E-6   B1      = 5E-6
+KETA    = -6.946031E-4 A1      = 1.62452E-6    A2      = 0.3505695
+RDSW    = 1.005868E3   PRWG    = 0.100056      PRWB    = 0.0296429
+WR      = 1            WINT    = 2.206503E-7   LINT    = 9.22689E-8
+XL      = 1E-7         XW      = 0             DWG     = -6.427643E-9
+DWB     = 4.666298E-8  VOFF    = 0             NFACTOR = 0.6103976
+CIT     = 0            CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 7.108939E-3   ETAB    = -8.895823E-5
+DSUB    = 0.2015128    PCLM    = 2.8375695     PDIBLC1 = 3.072554E-4
+PDIBLC2 = 2.804908E-3  PDIBLCB = -1.111051E-3  DROUT   = 0.0116129
+PSCBE1  = 6.295255E8   PSCBE2  = 1.71681E-4    PVAG    = 0
+DELTA   = 0.01         RSH     = 84.4          MOBMOD  = 1
+PRT     = 0            UTE     = -1.5          KT1     = -0.11
+KT1L    = 0            KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0            WLN     = 1             WW      = 0
+WWN     = 1            WWL     = 0             LL      = 0
+LLN     = 1            LW      = 0             LWN     = 1
+LWL     = 0            CAPMOD  = 2             XPART   = 0.5
+CGDO    = 2.92E-10     CGSO    = 2.92E-10      CGBO    = 1E-9
+CJ      = 4.262863E-4  PB      = 0.9435289     MJ      = 0.445557
+CJSW    = 3.315293E-10 PBSW    = 0.8           MJSW    = 0.2050229
+CJSWG   = 1.64E-10     PBSWG   = 0.8           MJSWG   = 0.2050229
+CF      = 0            PVTH0   = 0.0744795     PRDSW   = 330.3189931
+PK2     = -0.0736498   WKETA   = -0.01981      LKETA   = -7.470568E-3  )
*
```

B.2 PMOS Model Parameters for 0.5μm Technology

```
.MODEL PMOS PMOS (                      LEVEL   = 7
+VERSION = 3.1          TNOM    = 27            TOX     = 1.42E-8
+XJ      = 1.5E-7       NCH     = 1.7E17        VTH0    = -0.9152268
+K1      = 0.553472     K2      = 7.871921E-3   K3      = 8.5159118
+K3B     = 1.882525     W0      = 1E-5          NLX     = 1.122129E-7
```

```
+DVT0W   = 0           DVT1W   = 0           DVT2W   = 0
+DVT0    = 0.8919374     DVT1    = 0.3084112     DVT2    = -0.1622689
+U0      = 201.3603195   UA      = 2.408572E-9   UB      = 1E-21
+UC      = -1E-10        VSAT    = 9.743465E4    A0      = 0.8128126
+AGS     = 0.0960178     B0      = 1.400296E-7   B1      = 0
+KETA    = -4.865785E-3  A1      = 2.441943E-4   A2      = 0.5732897
+RDSW    = 3E3           PRWG    = -0.0301566    PRWB    = -0.04431
+WR      = 1             WINT    = 2.81961E-7    LINT    = 1.184823E-7
+XL      = 1E-7          XW      = 0             DWG     = -5.849303E-9
+DWB     = -3.393472E-9  VOFF    = -0.0669406    NFACTOR = 0.9248397
+CIT     = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 2.912512E-4   ETAB    = -0.1338923
+DSUB    = 0.8258954     PCLM    = 2.4587036     PDIBLC1 = 0.0650399
+PDIBLC2 = 3.68666E-3    PDIBLCB = -0.01669      DROUT   = 0.2781615
+PSCBE1  = 1E8           PSCBE2  = 3.333972E-9   PVAG    = 7.573917E-4
+DELTA   = 0.01          RSH     = 109.2         MOBMOD  = 1
+PRT     = 0             UTE     = -1.5          KT1     = -0.11
+KT1L    = 0             KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 0.5
+CGDO    = 3.87E-10      CGSO    = 3.87E-10      CGBO    = 1E-9
+CJ      = 7.191563E-4   PB      = 0.99          MJ      = 0.5001571
+CJSW    = 2.661206E-10  PBSW    = 0.99          MJSW    = 0.4094086
+CJSWG   = 6.4E-11       PBSWG   = 0.99          MJSWG   = 0.4094086
+CF      = 0             PVTH0   = 5.98016E-3    PRDSW   = 14.8598424
+PK2     = 3.73981E-3    WKETA   = 0.0197565     LKETA   = -0.0111747 )
*
```

APPENDIX C: SIMULATION OF FLOATING GATE DEVICES.

A main design issue faced with using floating gate devices is the validation of electrical simulation. Since models for floating gate devices are not provided by the manufacturers, techniques to simulate floating gate devices using standard MOS models must be devised. Another difficulty in simulating floating gate devices is the inability of the simulator to converge when floating nodes exists. Hence an initial operation point of the circuit must be introduced. Few approaches for this problem are given in references [11, 23-24]. In reference [11], the solution was to use an initial condition (.IC) as a feature in the simulator. While in [23, 24] they used additional networks formed by resistors and voltage controlled voltage sources (VCVS) to establish initial voltage on floating gate. Villegas et. al., [20], suggests that all the input voltage sources be initialized to zero, before running the simulation, which would allow to set an appropriate operating point when using floating gate devices.

The equivalent circuit of a MIFG inverter when used for electrical simulation is given [5], [20] in Fig. C.1. When the circuit is simulated in SPICE it fails to converge at floating gate. Hence a large resistance in the range of 1E20 ohms was placed from floating gate to ground as shown [5], [20] in Fig. C.2. The resistor gives an initial voltage on floating gate as well as an effect of open circuit from floating gate to ground. The PSpice circuit input file for the operation of the converter in Appendix A reflects the use of initial condition (.IC) and use of high resistance of value IE20 ohms at the floating nodes. If a dc voltage is given as input to any of the capacitors like C_1, the simulator recognizes the capacitor as a dc storage capacitor, instead of an AC coupling capacitance and blocks the voltage. A pulse waveform with rise and fall times is therefore given as the input voltage source signal instead of a dc voltage, using which the simulator simulates the capacitor as a coupling capacitance.

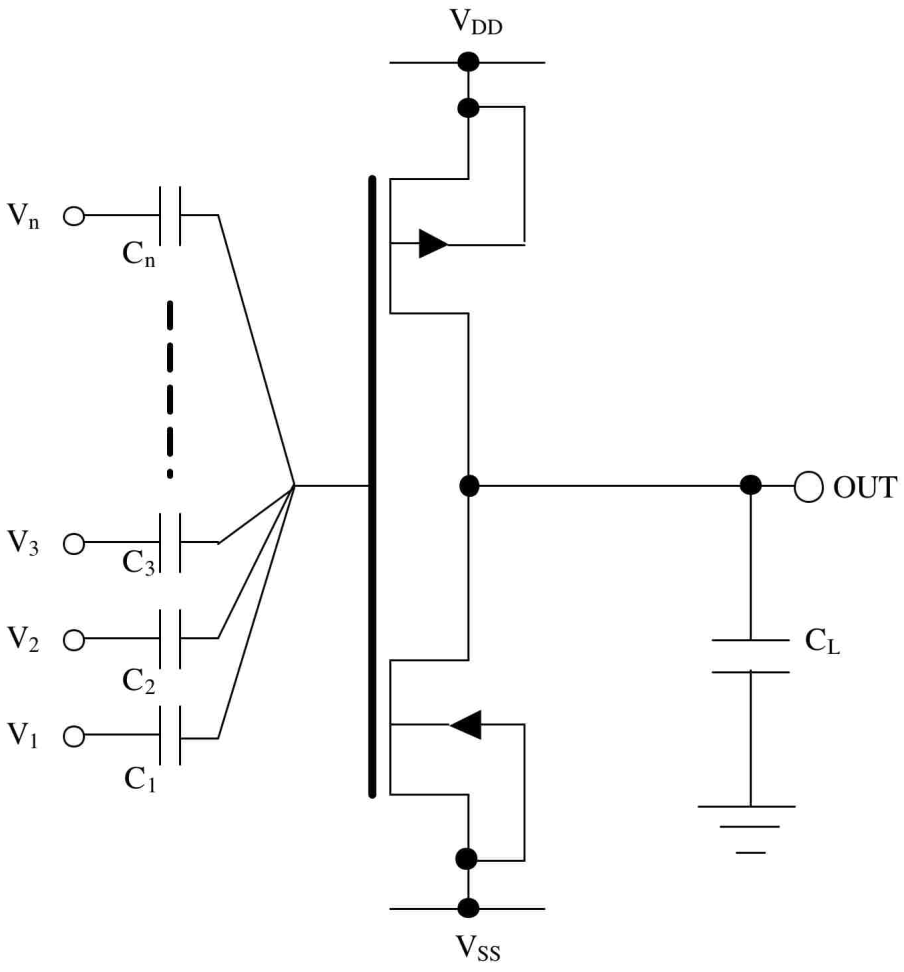

Figure C.1: Equivalent circuit of MIFG inverter for electrical simulations.

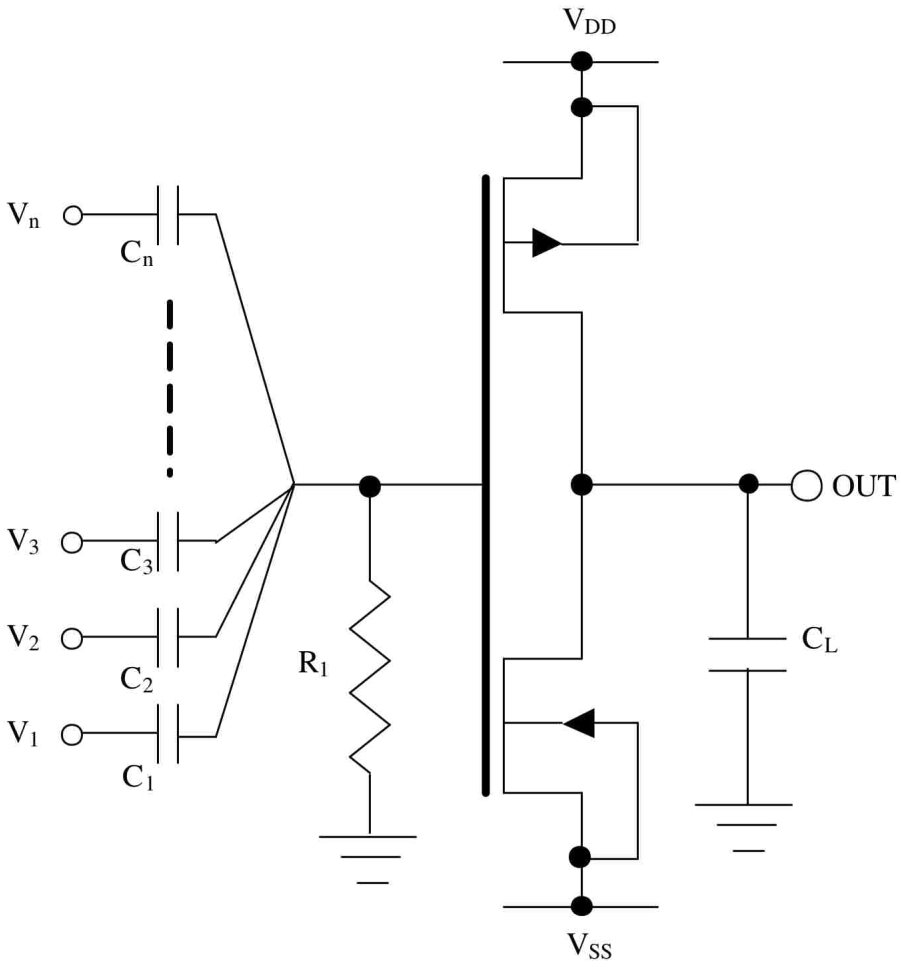

Figure C.2: Adding of resistor to the equivalent circuit for simulation.

VITA

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