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Monolithic integration of high-aspect-ratio microstructures with CMOS circuitry

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MONOLITHIC INTEGRATION OF HIGH-ASPECT-RATIO MICROSTRUCTURES WITH CMOS CIRCUITRY

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Abstract

This work involves developing processing techniques for monolithically integrating a high-aspect-ratio microstructures with CMOS circuitry. A microsystem comprising of a microprobe array and signal processing circuitry is utilized as a test vehicle to demonstrate this fabrication process. One potential application of this microsystem is for recording neural signals from the central nervous system. The main results include thick photoresist processing, DC and pulse electroplating to form high-aspect-ratio microprobes, microprobe sharpening and developing a post-IC monolithic integration process.

SU-8 is utilized for thick photoresist application. This work focuses on realization of a deep microrecess array in thick resists rather than traditional stand-alone SU-8 columns. The former encounters more processing challenges. Several novel techniques are developed including a unique development step, which results in clean microrecesses up to 450 μm deep with the smallest width of 40 μm giving aspect-ratio of 11.

Electroplating is performed in nickel sulfamate electrolyte. DC plating rate is found to depend on probe location, dimension and probe spacing. Nernst diffusion boundary layer model is utilized to estimate Ni ion diffusion coefficient to be 3.3×10^{-6} cm^2/s. Stress in deposit is found to change from compressive to tensile with increasing DC plating current density and with increasing deposit thickness saturating respectively at 92 MPa and 73 MPa.

Stress in pulse plated Ni with long pulses saturates at 54.5 MPa, while short pulse periods produce only compressive stresses between -110 MPa and -160 MPa. Surface morphology of electroplated Ni is related to built-in stress. A one-dimensional simplified model is built to describe the pulse plating process taking fixed and moving boundary approaches. The results are utilized to determine the pulse on time for plating into deep microrecesses.

Nickel wire or probe is sharpened electrochemically with wires giving sharper tips under conditions of 30 °C, 4 V potential in a 0.5 M sulfuric acid electrolyte.

Chemicals are carefully tailored in developing post-IC monolithic integration process to avoid detrimental impact on the CMOS circuitry with processing temperature maintained below 100 °C to avoid circuit degradation. A unique chip-level tape-and-wire bonding technique is developed to perform chip-level monolithic integration.

Chapter 1. Introduction and Literature Review

1.1 Introduction

1.1.1 Integrated Microsystems

MEMS is an acronym for Mirco-Electro-Mechanical-Systems. By employing technologies developed for fabricating integrated circuits (ICs), MEMS structure sizes can be reduced to small dimensions. These micro-miniaturized devices (sensors or actuators) can find a variety of applications for defense, commercial, medical, environmental, analytical and other purposes [1.1-2].

MEMS devices are utilized mostly for sensing or actuation. Signals from MEMS devices are usually transformed into electrical signals. Thus circuitry is needed to process these signals for amplification, feed-back control, decision-making and actuation. Therefore, integration of microstructures with circuitry to form microsystems is necessary to impart intelligence to microstructures.

Integrated microsystems can be categorized into two groups: hybrid or monolithic. In the hybrid case, MEMS devices and circuitry are fabricated separately and then integrated together on a ceramic or other substrate by various external bonding and packaging techniques. In the monolithic case, MEMS devices and circuitry are integrated on the same substrate usually without requiring any additional external bonding between the two. Hybrid integration is often a more convenient and/or cost effective approach but bonding wires or solder-bump connections to electronic circuitry contributes additional parasitic capacitance and also reduces operation reliability. Usually, monolithic integration results in a smaller size and a superior performance but requires more complex fabrication steps. Integrating microsystems with standard CMOS circuitry on the same chip is desirable as it can potentially lead to reduced parasitic capacitance,

higher signal-to-noise ratio, lower cost, lower power consumption, superior performance and compact size.

Monolithic integration can be achieved in three ways depending on when the microstructures are fabricated with respect to the on-chip circuitry. These are called pre-IC, co-IC and post-IC fabrication approaches. In the pre-IC approach, microstructures are fabricated first followed by IC circuit fabrication on the same substrate. In this approach, microstructures must survive the harsh IC fabrication environment. Occasionally the IC fabrication steps may need to be modified to accommodate the fabricated microstructures [1.3]. This is not only inconvenient but also impractical. In order to avoid this inconvenience, one can form a trench on the wafer first to allow the MEMS devices to sit in, and next the standard IC fabrication can then be executed after wafer planarizing [1.4]. However, MEMS devices are still subjected to harsh IC fabrication conditions that are inherent in IC processing, such as high temperatures, and exposure to harsh chemical treatments and radiation ambients. Moreover, the accessibility of this approach is limited because most IC foundries do not provide nor allow for specialized services. The advantage of pre-IC approach is that it eliminates the possibility of the IC circuitry from being damaged during MEMS microstructure fabrication. The co-IC approach integrates microstructure fabrication steps with IC fabrication steps as far as possible. This approach takes advantage of common processing steps needed for both microstructure and IC fabrication thereby reducing the total number of fabrication steps needed. In principle, this reduction in the number of fabrication steps also reduces the fabrication cost. Examples utilizing co-IC approach include references [1.5-7], in which microsystem chip design has been carried out without violating any IC fabrication rules. By utilizing additional processing steps such as etching layers from the front or back of the substrate, the microstructure devices can be released. However, this approach is restricted to planar devices having a small aspect ratio in the direction perpendicular

to the substrate. The metallic or dielectric layers in this approach are also restricted to Al or ploy-Si, and SiO_2 respectively dictated by IC industry without possibility of any significant variation. A major drawback of this approach is that the physical properties of the common processing layers such as poly-Si, metal or dielectric thin films are optimized for CMOS circuitry and may not possess optimal or suitable properties for the microstructures [1.8]. This can significantly compromise the microstructure performance.

In the post-IC approach, microstructures are fabricated after IC circuit fabrication. Most monolithic MEMS integrations are performed this way. It takes advantage of the readily available CMOS foundry services without posing any additional processing requirements and also makes it possible to build microstructures including high-aspect-ratio structures on top of the IC chip. However, this approach does need special attention. The processing temperature for the microstructure fabrication must be held below 450 °C to not degrade the aluminum interconnects commonly utilized by many CMOS foundries. It also requires a relatively mild chemical ambient that does not damage the fabricated CMOS circuits. Also, exposures to high-energy radiation like X-rays or plasma must be significantly restricted to avoid device damage that can negatively affect CMOS circuit performance. A previous work from our research group reported post-IC monolithic integration approach utilizing X-ray lithography, which gave acceptable results but the detrimental effects of the damage caused by radiation on CMOS circuit performance could not be completely eliminated [1.9].

In this work, post-IC monolithic integration is preferred for the reasons stated earlier. X-ray exposure is excluded and the cheaper and readily-available UV light source is used instead. High-aspect-ratio structures will be integrated on application-specific IC (ASIC) chips designed at LSU and fabricated by an IC foundry.

1.1.2 High-Aspect-Ratio Microstructures

High-aspect-ratio microstructures are required for many applications for improving sensitivity, performance or stability. There are three main technologies used for realizing high-aspect-ratio structures namely deep reactive ion etching (DRIE), lithographie galvanoformung und abformung (LIGA - a German acronym for lithography, electroplating and molding), and SU-8 UV lithography. There are also other more exotic technologies reported in literature such as micro-stereo lithography [1.10], which are not discussed here. DRIE, is usually employed to directly etch away unmasked materials like silicon, silicon compounds, or polymers by bombardment and reaction with a mixture of reactive gases and the products are exhausted in vapor form. One example of DRIE can be found in the fabrication of micro needles for intracellular application by etching silicon wafers [1.11]. LIGA technique has been utilized to fabricate very tall microstructures more than 1 mm in height with straight sidewalls and with submicron dimensions. Thick polymethylmethacrylate (PMMA) resists are usually utilized in LIGA applications. X-Rays produced by a synchrotron are generally used as exposure source for PMMA resists. An example of LIGA application can be found in reference [1.12]. A major requirement for LIGA is utilization of X-rays from a synchrotron light source, which can be expensive. In reality, a substantial portion of MEMS applications do not require submicron resolution hence it is very desirable that UV or near-UV resists with lower resolution in the dimensional range from microns to tens of microns are utilized for delineating high-aspect-ratio structures. Moreover, X-rays are detrimental to CMOS circuits as mentioned earlier. These drawbacks motivate work toward high-aspect-ratio structures utilizing cheaper and easier processes based on UV lithography.

PMMA is not sensitive to UV light. A relatively new resist called SU-8 has been available from MicroChem, which can be deposited in a thick layer and can be exposed by UV

light. SU-8 resist was first developed by IBM as a negative tone, epoxy-type, near UV photoresist based on EPON resin that was commercially available from Shell Chemical [13]. This resist allows a coating layer up to several hundred μm in thickness in a single spin cycle utilizing a conventional spin coater. Thicker layer of resist can be achieved by multiple spin coating cycles. Processing SU-8 can yield high-aspect-ratio structures [1.13-14]. However, a major downside of SU-8 resist is the presence of a considerable amount of stress in the resist due to heavily cross-linked features resulting after post-exposure baking. This cross-linking also makes it difficult to remove the exposed resist. By carefully designing the process and using proper chemicals, this removal problem can be reduced.

In this work, SU-8 photoresist has been utilized to realize high-aspect-ratio microstructures. A 3-D neural microprobe array is utilized as a vehicle to demonstrate this high-aspect-ratio microstructure fabrication technique.

1.1.3 A 3-D Neural Microprobe Array Integrated with CMOS Circuitry

As a test vehicle, a 3-D microprobe array is utilized in this work to develop and demonstrate monolithic integration. The microprobe array can be ultimately employed in biomedical applications associated with central nervous system (CNS) though biomedical applications by themselves are not a subject of this work.

CNS comprises the brain and the spinal cord. A heavily-folded layer of gray matter lies underneath the skull of human beings which holds about 100 billion neurons. Depending on their functions, neurons can be categorized as sensory or motor neurons. Information from external stimuli in form of light, heat, taste, touch and sound are collected by ends of neural networks called axon terminals. Their signals in form of voltage pulses are input to the sensory neurons, and then appropriately transmitted to motor neurons to provide output to muscle to excite muscle motion through the brain stem and the spinal cord. This path is schematically shown in Fig. 1.1.

Different regions of the gray matter are denser in different types of neurons, some are primarily rich in sensory neurons and some in motor neurons, as shown in Fig. 1.2. The gray matter can be divided into several layers as indicated in Fig. 1.2.

There is a great need to understand the organization and function of CNS at the cellular level, principally in the sensory and motor areas. Sharpened metal wires have been used as recording electrodes from single neurons [1.15-16]. However, lack of structures capable of multipoint recording from a neural tissue to sense or stimulate a group of neurons has been a serious constriction in neurophysiological research. Such a structure is called a brain-computer-interface (BCI). For paralyzed people, BCI is expected to help regain proper muscle function. Biochemistry usually looks into the reactants and products in the nerve cells or the transportation of electrons and ions that participate in bioreactions to characterize neural actions. However, neural signals are eventually represented as voltage pulses. Hence utilizing microprobes to communicate with the extracellular biopotentials that are generated through bioreactions in nerve cells has been a principle technique to study CNS at the cellular level. In another word, microprobes with corresponding signal processing circuitry is a BCI.

In order to sense or excite, the microprobes need to penetrate into the cerebral cortex. The length of the probes should be approximately 1 mm because large neuron cells (the pyramid cells) are about this distance beneath the surface of the gray matter [1.17]. This is schematically shown in Fig. 1.3.

A 3-D microprobe array is preferred to a single probe or a 2-D array. In a 3-D array, the tips of the microprobes are aligned horizontally. Hence the array can cover a certain number of neurons in close proximity of each other after penetration. Meanwhile, the probe shank size and the exposed tip areas that serve as electrodes need to be manipulated to accommodate signal processing.

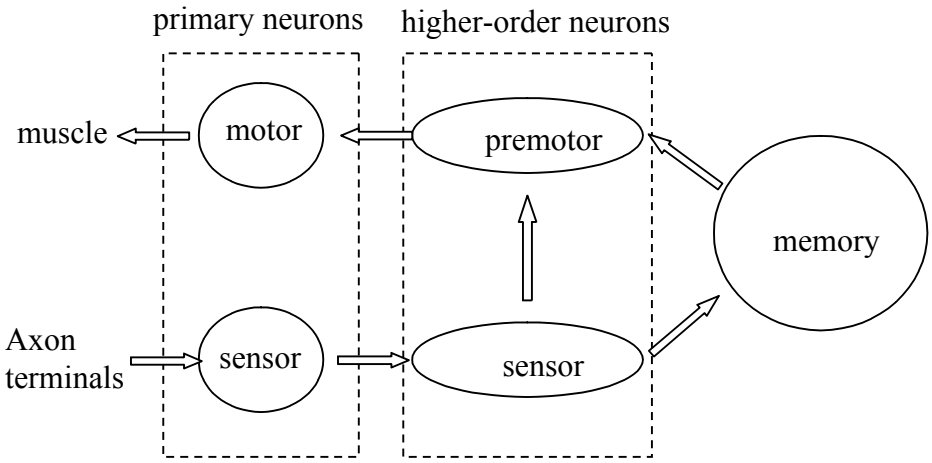


Figure 1.1: A schematic diagram to show how signals travel in the central nervous system.

The amplitude of the neural signals is small, in the range of several tens to several hundreds of μV. Therefore, circuitry is needed to amplify the neural signals. The amplifier voltage gain should be large and produce minimal internal noise. Also, low-power circuitry is desired for both low battery power consumption and for low amount of local in-situ heating.

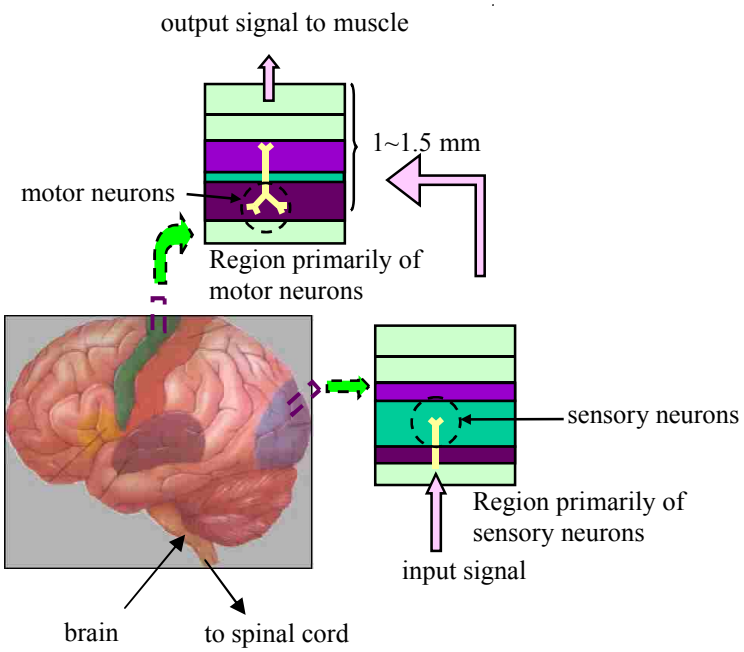


Figure 1.2: Different regions in the gray matter have different structure comprising primarily of motor or of sensory neurons.

In the past three decades, a significant amount of work has been performed in search of an appropriate neural microprobe array [1.18-32]. The probe array dimension has been denoted as 1-D [1.18], 2-D [1.23-27], or 3-D [1.28], with most of the reported work being on 1-D or 2-D probe arrays. A multi-electrode array can be either in a 2-D or a 3-D frame, in comparison to a single electrode, which is called a 1-D probe. The materials used for probes could be silicon [1.18-28], metal [1.31], or polymer [1.32], and most researchers have chosen silicon as a probe shank. Circuitry for processing the neural signals can be either hybrid [1.28] or monolithic [1.24]. Only a small portion of previous work includes processing circuitry and among them hybrid circuitry is generally utilized.

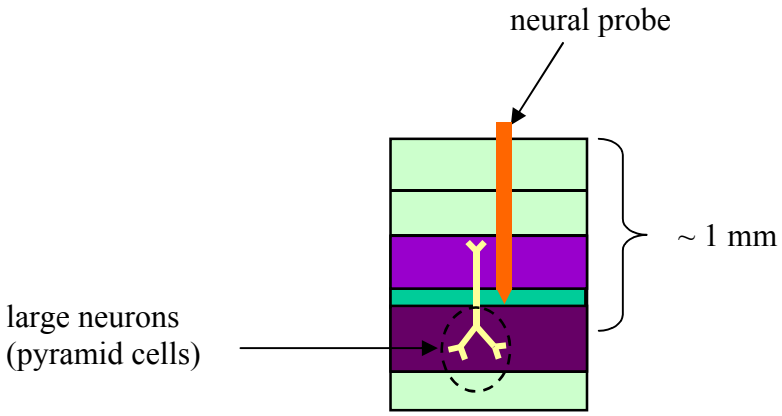


Figure 1.3: The schematic shows a probe that has penetrated into cerebral cortex to reach and sense signals from pyramid cells.

In 1970's, an early version of microelectrode was just a single electrode for implanting into the motor cortex [1.18-19]. Only a limited number of neurons can be in close proximity with this probe. It did show that electrical potential was associated with neural signals. However, if the electrode is damaged or the neurons around this electrode lose their function, the implanted electrode will have no role to play. Moreover, Direct investigation of spontaneous dynamic behavior of a population of neurons can only be achieved on simultaneous observation of large

neuronal aggregates [1.20-21]. Meanwhile, researchers found that a group of neurons in close proximity have similar functions and have similar response to external stimulation [1.21-22]. This observation has led researchers to fabricate multielectrode arrays in order to gather more information or provide stronger external stimulation. In a 2-D array, the tips of the electrodes are aligned in a single row so that when the array is penetrated, it covers a single line.

Almost all of the work on multielectrode array is focused on 2-D array schemes [1.23-27] due to convenience of fabricating such high-aspect-ratio probes. A 2-D array is usually delineated on the surface of a wafer and then released as free probes by etching. An advantage of this approach is that more than one electrode can be present on one side of a single probe and the length of the probes can easily reach over 1 mm. A disadvantage is that this planar process is limited in scope and can not directly realize a 3-D array. Najafi and Wise pioneered this work in 1985 [1.23]. Subsequently, other researchers used similar techniques with minor modifications to realize 2-D probe arrays [1.26-27]. A released stand-free 2-D probe array is schematically shown in Fig. 1.4.

All 2-D probe array work utilized silicon as a supporting substrate on which metal electrodes are embedded in silicon host and the interconnecting leads are made of polysilicon or metal. In order to develop 3-D probe arrays based on this scheme, a special grid needs to be machined as a supporting structure where the 2-D probes can be slipped in and firmly fixed in the grid [1.25]. This requires additional processing steps during fabrication. Furthermore, since the probe tip is not an electrode site, the neurons that make contact with the electrodes may get damaged during the probe penetration which starts at the tip. In order to avoid this drawback, Lucic et al. modified the fabrication steps by utilizing cultured implanted neurons as ‘linking neurons’ which can build a network with healthy neurons after probe penetration [1.26].

In 1991, Jones et al. directly made a 3-D probe array without needing an extra supporting grid [1.28]. This is the only work to date to our knowledge that has directly realized a 3-D array. They used a special diamond saw to execute multiple cuts precisely into a silicon substrate along two orthogonal directions to form an array of silicon columns, followed by a sharpening process to form tapered tips by using a two-step etching process. In order to insulate between probes from the probe root, grooves were cut out from the backside of the substrate and filled with a glass slurry that was fired at 1150 °C as an insulator. This high firing temperature makes it impossible to accommodate post-IC processing. Thus its signal-processing circuitry had to be added on as a hybrid component.

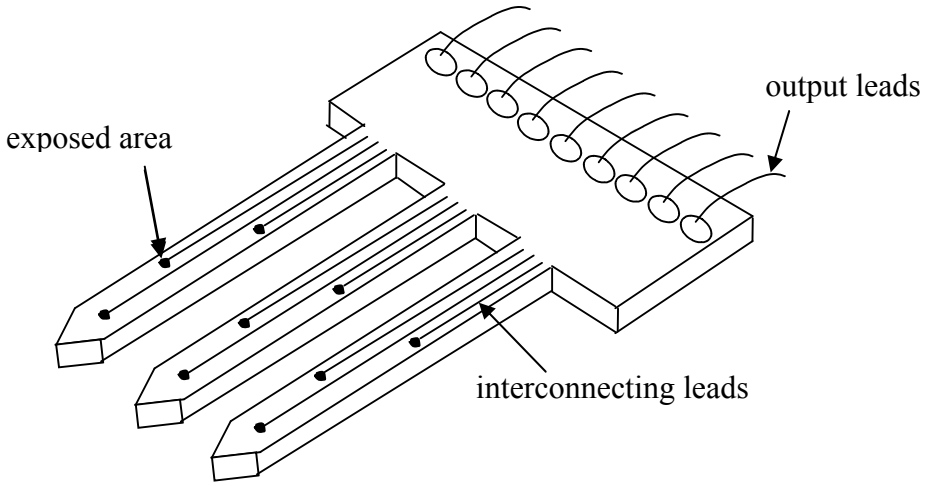


Figure 1.4: A schematic 2-D microprobe array after ref. [1.24].

Until recently, silicon had been the only material for neural microprobes. The advantages of silicon are its biocompatibility [1.29], high mechanical strength with Young's modulus value of approximately 100 GPa, good flexibility when the piece is thin [1.30], well-established processing techniques and ready availability. However, a major disadvantage of silicon is that it is not a good conductor, thus metal electrodes need to be embedded in the silicon substrate and metal wires have to be defined as conduction leads. As a result, the fabrication process becomes

complicated, especially when an extra grid is needed for developing 2-D probe arrays into a 3-D array. Another result of this surface process gives rise to high shunt parasitic capacitance values because over 50 percent of the metal electrodes and wires are in contact with silicon substrate. The amplitude of the neural signals is attenuated by this capacitance.

In 2002, Xu et al. developed a metallic neural microprobe array [1.31]. The metallic material is permalloy ($Ni_{0.8}Fe_{0..2}$). The probe array was first laid out on a silicon substrate as shown in Fig. 1.4. The difference between this work and previous work in Fig. 1.4 lies in the absence of silicon substrate which is etched away completely in a later step in Xu's work and only the metal part is kept as a probe shank. Due to the nature of the probes being parallel to the surface of substrate, it is impossible to obtain a 3-D probe array by this technique. Meanwhile, on-chip circuitry is made impossible because silicon substrate etchant uses an alkaline etchant, which is not compatible with CMOS post-IC processing requirements. However, metallic material is more flexible than silicon and has sufficient strength. Moreover, probes made entirely of a metallic material have higher conductivity compared with silicon probes using only metallic wires as conducting leads.

Another candidate material for neural microprobes is polymer material. From biocompatibility view-point, polymers provide the best choice because there are many biocompatible polymers to choose from. Flexibility is another advantage of polymers but it is also a disadvantage since too much flexibility decreases polymers' ability to penetrate tissues. In early 2004, Takeuchi et al. developed a sandwich shaped polymer probe array [1.32]. This work also started with silicon substrate on which a three-layer polyimide-metal-polyimide structure is applied in sequence. Windows are opened on the polyimide to expose the metal piece as electrodes and the probes are folded up from the substrate thus a 3-D array is formed. However, lack of support at the root of the probes plus lack of significant polymer support resulted in

bending of the probe structure during penetration. The sandwiched metal layer thickness is only 1 μm. Since there is no electrode opening at the tip of the probes, the neurons in close contact with the electrodes may also suffer from damage.

Most of the work described above only focuses on the fabrication of microprobes. But in order to investigate the signal pulses, a signal processing circuitry is necessary. Among the work involving circuitry, most of the reported work so far has used a hybrid approach utilizing commercially available amplifiers. However, monolithic circuitry is preferred in terms of reducing noise and boosting up signal-to-noise ratio. The amplifier circuit needs to meet specific neural applications such as ambient noise level, high voltage gain, sufficiently large bandwidth, low voltage level shift and low power consumption. A very good example of a specially designed circuitry is by Kim and Wise [1.24]. In their work, low power consumption and noise control are both considered. Their complete circuitry includes four blocks: preamplifiers, a multiplexer, a unity-gain broad-band buffer, and a demultiplexer. An amplifier circuit designed particularly for this work by Zhang in our laboratory is published elsewhere [1.33-34].

1.1.4 Probe Sharpening

For all of the above mentioned 2-D probe work, the probes are designed having sharp tips. The latter are fabricated utilizing routine microfabrication steps without requiring any extra treatment on probe morphology. However, for a directly formed 3-D probe array, probe tips are usually not tapered after the formation of probe shanks because traditional lithography is not capable of easily varying geometry in z-direction. Hence a subsequent reshaping step or steps are needed after the probe array is fabricated. Jones et al. employed a two-step acid etching procedure to thin and sharpen the silicon shafts to realize their Utah Intracortical Electrode Array [1.28].

The material used for probe shank in this work is metal. Sharpened metal tips have been widely used either for mechanical probing or as an electron source in various types of electron emission microprobes. As for the proposed 3-D neural probe array in the current work, the nickel probes need to be sharpened at tips in order to penetrate into cerebellum, avoiding damage caused by serious dimpling of the cortex. Blunt tips may also cause probe buckling and probe breaking. A widely used technique for obtaining a sharpened metal tip is by electrochemical method, as compared to the chemical etching method in Jones' work [1.28] in which silicon is not highly conductive. The eventual tip shape obtained electrochemically depends on many factors including electrolytic composition, cell geometry, electrodes setup and configuration, and the cell operating conditions. Almost all of the work from literature on electrochemical tip sharpening involves just a single probe or wire for convenience in handling. They are performed on the same principle as that of electrochemical polishing of metallic materials in which surface finishing is achieved by anodic treatment in an electrolyte.

1.2 Research Goals

The overall goal of this research is to develop a process for monolithic integration of tall or high-aspect-ratio structures with CMOS circuitry by post-IC fabrication technique. This overall goal is to achieve fabrication of a complete microsystem. The microsystem chosen to demonstrate this monolithic integration process is a 3-D microprobe array. The dissertation work is then broken down into the following set of subtasks.

1) High-aspect-ratio probes are realized by utilizing UV lithographic techniques. UV light source is used here instead of X-rays because not only an X-ray source is expensive but also X-ray radiation changes the charge status in the gate oxide and at the oxide-substrate interface in CMOS circuits. This results in a shift in threshold voltage values of MOS devices. Although X-

rays are known to give extremely high-aspect-ratio structures, an alternative LIGA-like process utilizing SU-8 thick resist is developed here.

2) A 3-D probe array is constructed by electroplating. Both DC and pulse electroplating processes are employed in this work and the results from these two techniques are compared. Here the probes are oriented perpendicular to the silicon substrate unlike the case for 2-D probe arrays in which probes are oriented parallel to the substrate. Compared to a 2-D array, a 3-D array is capable of gathering greater amount of information in terms of investigating parallel signal processing in brain tissues since the rhythmic activity of neurons in the cerebellum has been found to be strongly correlated while performing a particular task.

3) Processes for both wafer-level and chip-level monolithic post-IC integration with CMOS circuitry are developed. Usually in manufacturing, one is concerned with wafer-level integration only. However in a university setting, wafer-level processing is not always practical or cost-effective and hence, chip-level processing may have to be employed [1.35]. This results in development of a fabrication technique that is somewhat more complex than the wafer-level integration case.

4) As the device is designed for central nervous system, the probes should be able to penetrate into the cerebellum. Hence the probes are sharpened by an electrochemical technique to form pointed tips.

By taking into account probe array dimension and signal processing circuitry, the goal of this research is to achieve a directly formed three dimensional, metallic neural microprobe array which is monolithically integrated with appropriate CMOS circuitry. This probe array is expected to find potential application in Brain-Computer-Interface (BCI) as a communication conveyor between the brain tissues and an external computer. The developed process must utilize

traditional MEMS fabrication techniques so that the fabricated microsystem does not require any specialized instruments.

Chapter 2 gives an overview on the design of the microsystem. This microsystem includes a microprobe array and a signal processing circuitry. Both components are integrated on a 2 mm × 2 mm silicon chip. Several photoresists have been employed in this work and their processing details especially the ones developed here are presented in chapter 3. SU-8 resists have been utilized extensively and hence are given more emphasis. Chapter 4 will address nickel electroplating processes including both DC and pulse techniques. The plating process is first characterized and stress analysis is performed on the electrodeposited material. A simplified analytic one dimensional electroplating model governed by diffusion mass transport is developed to describe the transient pulse plating process. In chapter 5, attempts to sharpen thin nickel wires and probes are described. The post-IC monolithic integration of nickel microprobes is given in chapter 6. The research work is summarized in chapter 7.

Chapter 2. System Level Design Overview

The probe array and the amplifying circuitry are designed for monolithic integration on the same chip. The chip size is about 2 mm × 2 mm and 250 μm thick. The probe array, the corresponding signal processing circuitry and bonding pads comprise the chip surface topography. The CMOS circuitry is designed in our laboratory and is sent to a foundry for fabrication. A metal probe array is then post-processed on the chip received from the foundry. A schematic drawing of the microsystem is shown in Fig. 2.1. It contains an array of probes on the left side and the CMOS circuitry is located on the right side. The CMOS circuitry can include one multiplexer and one amplifier, or alternatively it can include an array of identical amplifiers without needing a multiplexer. The latter approach is chosen here in this work for convenience. Signals from this probe array comprising of serial voltage pulses will be processed by the amplifiers. The 3-D metal probe array is designed out-of-plane. They are integrated onto the CMOS chip by electroplating. The concept of the device design is novel in that, to our knowledge, it is the first chip-level monolithically integrated metal probe array that is fabricated out of the plane over the chip surface. A test design of an initial simplified probe array in this work is shown in Fig. 2.2, which consists of two sets of probes with each set having four probes with different sizes. The probe spacings in each of the two sets are different. This simplified test design retains all the processing steps necessary for fabricating the 3-D structure shown in Fig. 2.1.

The CMOS circuit design underwent two versions. The layout of the first-version of the chip design is shown in Fig. 2.3 [2.1]. The eight squares delineated in the middle of the chip are the probe areas. These areas are covered with Al, which is a good conductor. Al as the choice of a metal contact layer is determined by the IC foundry since Al is still a popular interconnect material for ASIC CMOS circuits. The top 4-neural microprobes in Fig. 2.3 have varying widths

of 70, 60, 50 and 40 μm and center to center spacings of 195, 175 and 155 μm respectively between the probes. The bottom set of 4-neural microprobes in Fig. 2.3 have varying widths of 40, 50, 60 and 70 μm and respective center to center spacings of 125, 145 and 165 μm between the probes. The size of probes is determined such that it is comparable to the cross-section area of a pyramid nerve cell in order to detect neural signals with optimal ratio. The spacing between two neural cell groups in human cerebrum that have different functions is reported to be in the range of 200 μm to 500 μm which sets bounds for spacings between probes [2.2]. On the far right of the chip are eight identical amplifiers. The amplifiers are designed to have low power consumption, a high ac voltage gain and a low level voltage shift [2.1,2.3].

Figure 2.4 shows a microscope picture of the fabricated chip as received from an IC foundry. The received chip is returned unpackaged. The overall size of the chip from foundry is 2 mm × 2 mm. The nominal chip thickness is 250 μm.

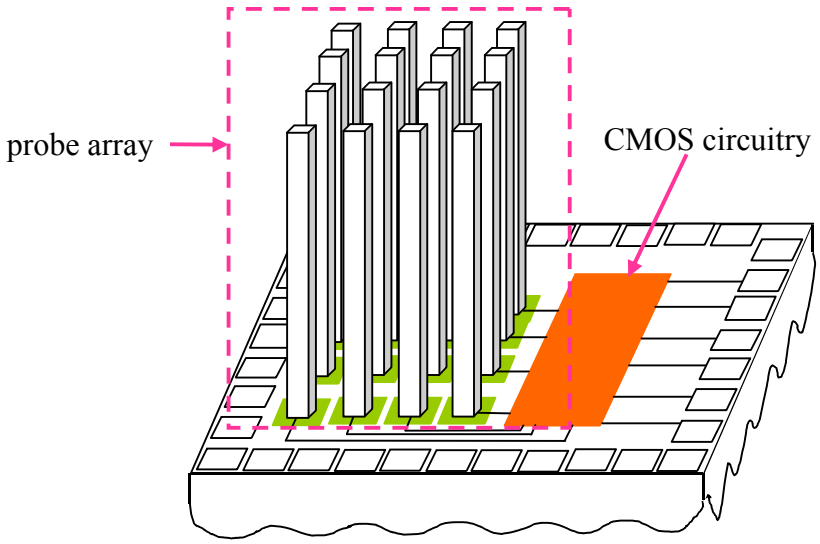


Figure 2.1: A conceptual design that shows a 3-D probe array integrated on a CMOS chip.

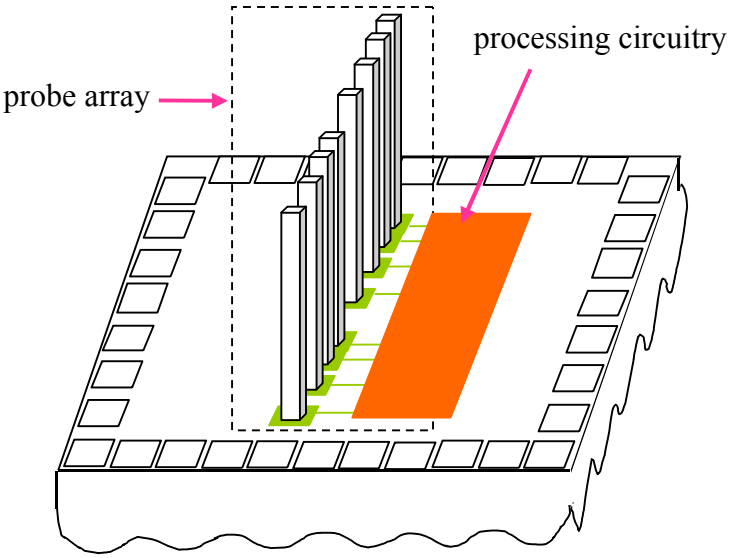


Figure 2.2: A simplified test design that shows eight probes integrated on a CMOS chip.

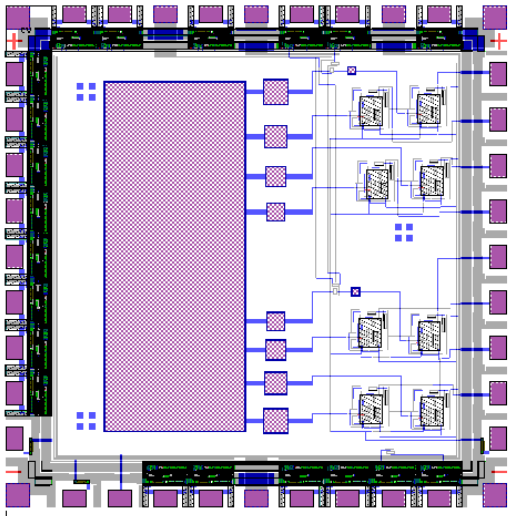


Figure 2.3: Layout of the CMOS test chip.

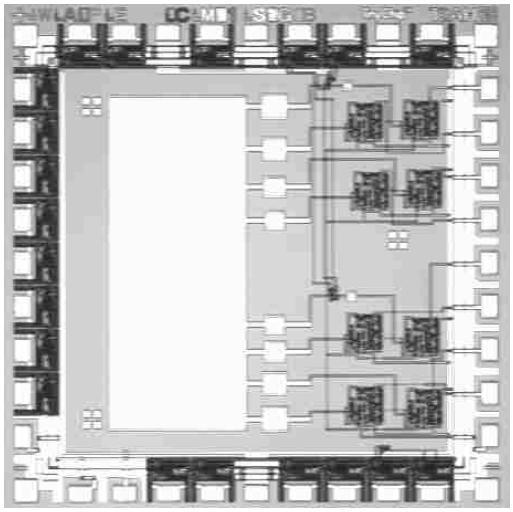


Figure 2.4: Photo-micrograph of a fabricated CMOS test chip.

Due to poor adhesion resulting from presumably the native aluminum oxide over Al interconnect layer as will be detailed in Chapter 3, probes taller than 50 μm detached from the substrate during the photoresist mold removal processing step. Hence a second version of the test chip is designed to solve this problem inherent with the Al metal layer.

In this alternative approach, the Al that covered the probe areas in the earlier version is absent so there is no metal layer on the square bottom probe pad areas. Instead, heavily doped n^+ - silicon is utilized as a conductor. The Al lines connecting between these squares and the amplifiers in the first chip are replaced by heavily doped n^+ - region as well. The second version of the test chip design in CAD layout is shown in Fig. 2.5. A fabricated test chip from the foundry is shown in Fig. 2.6. This approach has its disadvantage as the n^+ - region will increase input probe capacitance, reduce internal parallel resistance and increase series resistance. It will also require reverse biasing of the substrate – n^+ junction.

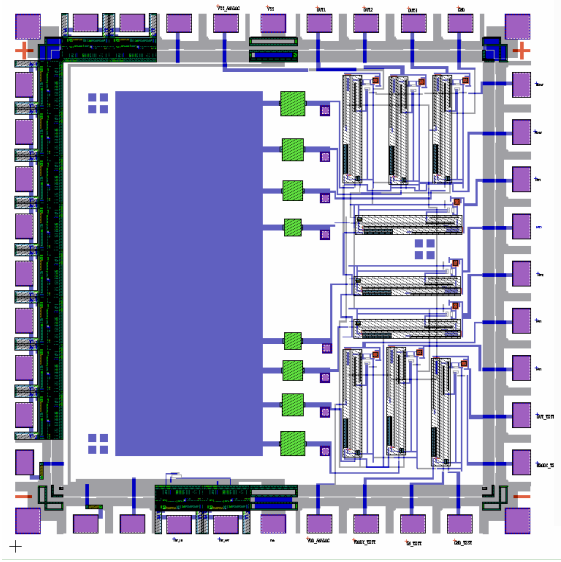


Figure 2.5: Layout of the second version of the test chip design.

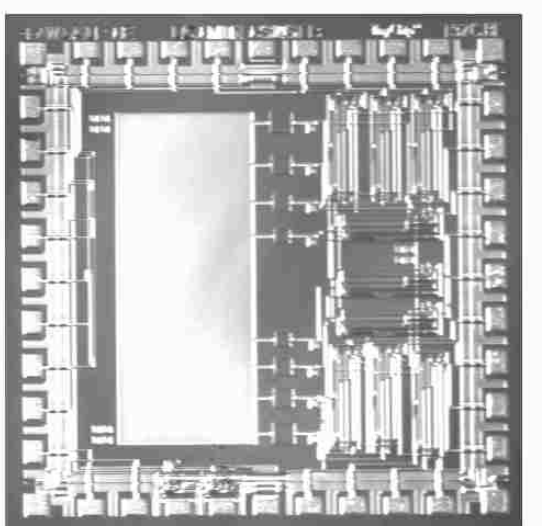


Figure 2.6: Photo-micrograph of the fabricated test chip with layout design shown in Fig. 2.5.

Chapter 3. Thick and Thin Photoresist Processing

3.1 SU-8 Photoresist Processing

SU-8 is a negative-tone photoresist. It was first developed by IBM in 1982. Its application in thick film photolithography was reported in 1995 [3.1]. SU-8 resist has three components which are based on an EPON resin commercially available from Shell Chemical. This resin is dissolved in an organic solvent gamma-butyloracton (GBL) with a photoinitiator salt. The quantity of the solvent determines the viscosity and thereby the range of available resist thickness. The SU-8 resist has good adhesion to silicon, SiO_2, aluminum, Al_2O_3 and gold films but poor adhesion to most commonly used metals such as copper, nickel and iron. In recent years, SU-8 has become a popular phototoresist for fabricating very high-aspect-ratio microstructures by using near-UV lithography. As its major competitor, AZ series resist can be coated by multiple spins to achieve microstructures more that 100 μm thick [3.2]. Microstructures as thick as 1.4 mm have been reported using negative tone JSR photoresist (JSR Micro) but the minimum feature size is in range of hundreds of microns and the quality of sidewall is relatively poor [3.3]. As a comparison, the SU-8 microstructures as thick as 2 mm and with aspect-ratio near 20 have been reported [3.4]. Microstructures as high as 300 μm and slightly over 10 μm in width have also been reported in literature [3.5]. The sidewall characteristics of SU-8 microstructures are extremely good.

The general processing steps for SU-8 photoresist include spin-coat, pre-bake, UV-light exposure, post-exposure bake, development and rinse.

3.1.1 Spin-Coating of SU-8 Photoresist

There are several members in the SU-8 family with viscosity being the major difference among them. Higher serial number in the family corresponds to a more viscous photoresist, which can consequently achieve a greater coating thickness. However, difficulty of maintaining

thickness uniformity across the substrate increases as the coating thickness increases. Among SU-8 resists, SU-8 50 is moderately viscous but still can produce a thick coating while keeping relatively good thickness uniformity across the entire substrate compared to SU-8 100 and SU-8 2075. The latter two are the most viscous resists in SU-8 series. SU-8 50 is chosen in this work for thick resist molds utilized for nickel electroplating. In order to yield a repeatable thickness, it is found that not only the spin cycle needs to be maintained the same from one run to the next, but also the amount of resist applied on the substrate must remain the same. The amount of SU-8 50 resist used in each spin cycle on a 4-inch silicon wafer has been kept constant at 7.5 ml throughout the entire work reported in this dissertation. The resist is poured at the center of the substrate and degassed using a pointed syringe before the start of each spin cycle in order to obtain a pore-free coating. Thickness of SU-8 50 as a function of spin speed for the spin coater in our laboratory (Model P6708, Special Coating systems, Inc.) is shown in Table 3.1. Note that the acceleration or ramping speed does play a role in the final thickness but it is the final rotational speed (RPM) and final dwell time that contribute the most important role in dictating the eventual thickness and uniformity. The plot of resist thickness as a function of final RPM is shown in the Fig. 3.1. It is seen that the thickness of SU-8 50 resist tends to level out as final rotational speed (RPM 3) value increases over 600 RPM.

Photoresist usually accumulates at the edge of the substrate after a spin cycle, leaving a thicker ring of photoresist at the edge of the substrate called an edge bead. The thicker the resist the more serious is the bead problem, as schematically shown in Fig. 3.2. The edge bead can prevent a good contact between the mask and the resist during the contact exposure step. The air trapped between the mask and the resist can compromise the feature profile in resist pattern. In order to reduce edge bead effect, S. Roth et al. [3.6] have included a short but large acceleration step in the middle and at the end of each spin cycle. However, this technique only made the bead

zone narrower but could not affect the peak thickness of the bead. For a complete removal, the bead is manually scraped off using a sharp scalpel after each spin. With care this significantly reduced the air gap between the mask and the resist. The substrate is then allowed to sit on a level flat surface for more than 30 minutes to help further spread the resist evenly across the substrate.

Table 3.1 SU-8 50 resist spin parameters.*

Recipe No.	Rt 1 (s)	RPM 1	Dt 1 (s)	Rt 2 (s)	RPM 2	Dt 2 (s)	Rt 3 (s)	RPM 3	Dt 3 (s)	RDt (s)	Resist coating thickness (μm)
1	5	100	5	5	500	5	5	1100	40	15	100
2	5	100	5	5	500	5	5	900	40	15	115
3	5	100	5	5	450	5	5	800	40	15	125
4	5	100	5	5	400	5	5	700	40	15	140
5	5	100	5	5	350	5	5	600	40	15	170
6	5	100	5	5	300	5	5	500	40	15	200
7	5	100	5	5	250	5	5	400	40	15	260
8	5	100	5	5	200	5	5	300	40	15	450
9	5	100	5	5	150	5	5	200	40	15	650

*Rt denotes ramp time; RPM denotes rotations per minute; Dt denotes dwell time; RDt denotes ramp down time.

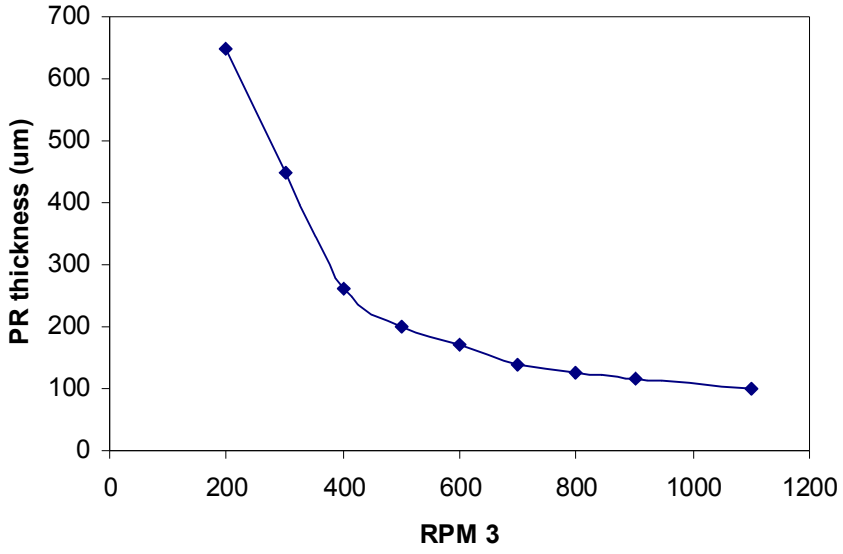


Figure 3.1: Thickness of SU-8 50 photoresist vs. final rotational speed RPM 3.

Figure 3.2: Edge bead usually shows up at the edge of the substrate when resist is thick. The bead profile is exaggerated in the above drawing.

3.1.2 Pre-Bake of SU-8 Photoresist

Pre-bake step follows the spin-coat cycle. This step removes most of the solvent inside the resist so that the resist becomes a solid plate upon cooling after the pre-bake step. A small amount of solvent, however, needs to remain in the resist to adjust appropriate optical properties of the resist. Pre-bake is one of the most important steps in the photoresist application process. It influences the exposure energy, development time, structure definition, the sidewall quality of the resist mold and the feature aspect-ratio [3.7]. In order to allow for the evaporation of the solvent, pre-bake has been most frequently performed on a hot plate in open air. Heat input from the backside of the wafer avoids crust formation on the top surface of the resist in contact with air at room temperature. In this work, a home-designed hot plate is put inside an oven to further avoid the surface crust formation and to help maintain temperature uniformity across the entire resist layer. Another advantage of baking inside an oven is that it avoids the air flow disturbance in open air which may cause a choppy surface on the resist. If the substrate is directly put in contact with the hot plate at the terminal pre-bake temperature, the thick resist tends to flow to the center of the wafer due to a tendency of surface energy reduction. Hence, a ramped temperature treatment has been used to reduce this phenomenon in this work and elsewhere [3.6].

Glass temperature, T_g of SU-8 before UV exposure is approximately 50 °C [3.8]. The pre-pake temperature should be higher than T_g to allow the resist to reflow along with solvent removal. The substrate is first put into oven that is pre-warmed at 65 °C, and oven temperature is ramped up to 96 °C gradually in order to keep thermal stress low. SU-8 resist reflows at the temperature of 65 °C and prior to removal of most of the solvent in the resist. This reflow however introduces a problem if the surface that supports the wafer is not level in that the thickness of the resist layer will not be uniform across the wafer after being baked. A simple calculation indicates that a 0.1 degree tilt of the supporting plate could result in as much as 175 μm thickness difference from edge to edge across a 4 inch wafer as indicated in Fig. 3.3. In reality, this situation is not as severe because reflow of resist reduces as the solvent is gradually removed. The thickness non-uniformity problem gets worse when the resist coating becomes thicker. Experimental measurement reveals that placing a wafer with 400 μm thick SU-8 on the oven rack that is not intentionally leveled has resulted in up to 100 μm thickness difference across a 4-inch wafer. As a result, UV light dose will need to vary with position to compensate for this non-uniformity, but in reality this is usually not feasible for UV mask aligners.

In order to solve this problem, a level-adjustable hot plate is designed and machined in our department machine shop. Leveling is realized by measuring surface flatness of the plate using a digital leveler meter. The surface roughness is ± 1μm rms. The resolution of the digital leveler is 0.05°. The design of this leveling plate is shown in Fig. 3.4. The square plate is 10 inch wide on each side and half an inch thick. It can accommodate up to four 4 inch wafers per load. The material of the plate is high quality stainless steel. Three through holes were drilled on the plate and three screw sets are used to adjust leveling until the digital level reads 0 degree.

During pre-bake, a large percentage of solvent is removed which results in contraction of the resist. This volume contraction consequently results in a considerable built-in tensile stress in the resist. The experimentally measured value of the Young's modulus of SU-8 photoresist is approximately 4.5 GPa [3.9]. The reported values of tensile stress have been between 16 to 19 MPa [3.10]. A 500 μm thick wafer can warp under this stress when the resist layer is very thick. This is shown in Fig. 3.5. In our work, warping is visually seen and becomes an issue when the thickness of SU-8 is over 300 μm.

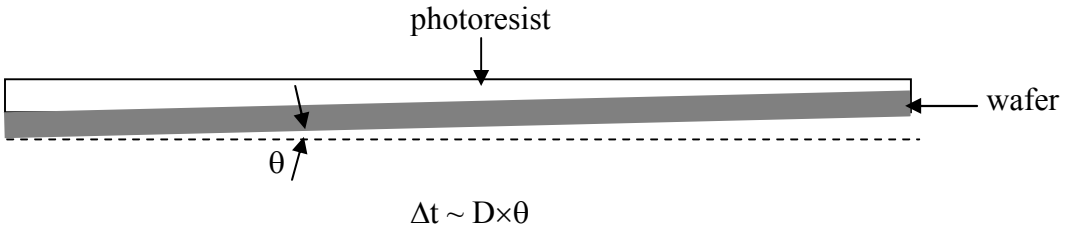


Figure 3.3: Non-uniformity in resist thickness resulting from substrate tilt.

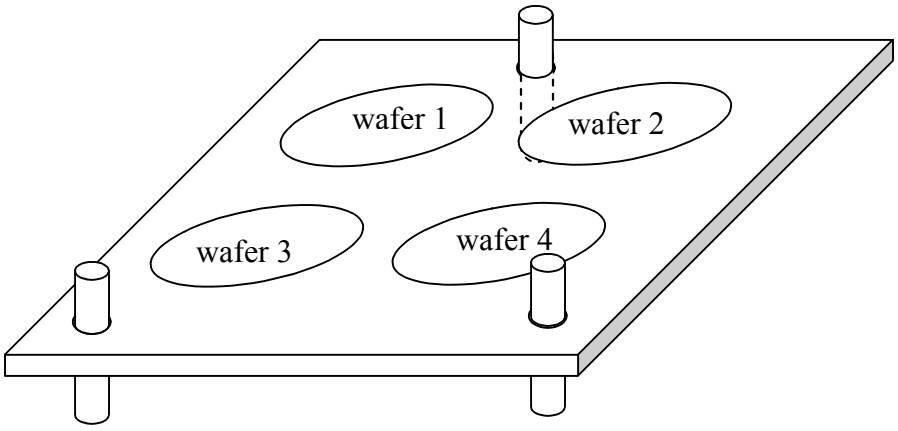


Figure 3.4: Design of a leveling hot plate for use inside an oven. The dimension of the plate is 10 in × 10 in × 0.5 in and the surface roughness is ± 1μm rms.

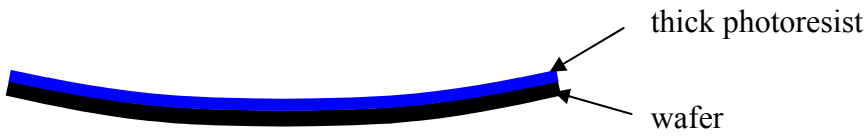


Figure 3.5: Wafer warp is caused by thermal stress generated during pre-baking. Warping is exaggerated to show the wafer bow.

When warping is present, it introduces difficulty during UV exposure because the wafer is not in intimate contact with the vacuum chuck causing a problem during alignment. A solution to remedy this problem is the placement of a thin plastic sealing ring under the substrate such that a nice vacuum can be generated between the substrate and the wafer chuck. This is shown in Fig. 3.6 schematically.

After pre-bake at 96 °C for the designated time, the substrate is annealed inside the oven. The annealing ambient is normal air. Annealing takes over 10 hours. This long duration is to avoid thermal shock and for eventual thermal stress reduction in the resist layer.

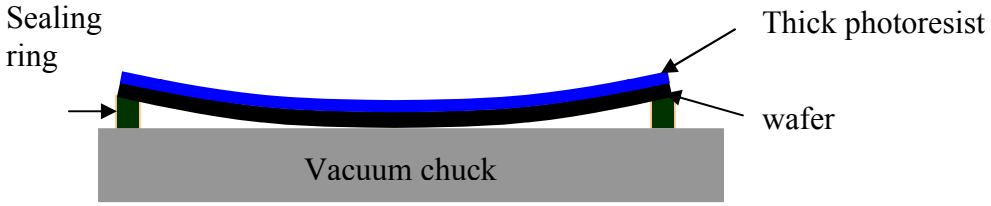


Figure 3.6: A plastic sealing ring is placed underneath the warped wafer during alignment. Wafer warp is exaggerated.

3.1.3 UV Light Exposure of SU-8

A key property that makes the SU-8 resists so attractive in ultra-thick resist applications is their relatively low optical absorption in the near-UV range. This enables UV light to travel deep into the thick resist making it possible to achieve relatively uniform exposure through the

resist thickness. This in turn leads to vertical sidewalls and provides for excellent dimensional control over the entire thickness of the resist. During exposure, the light intensity, I decreases following Arrhenius' relationship along the traveling path into an absorbing medium given by $I = I_0 \exp(-\alpha x)$, where α is the absorption coefficient, x is the penetration depth of UV light into the absorbing medium and I_0 is the incident light intensity. Ling et al. at LSU CAMD have experimentally extracted the absorption coefficient α of SU-8 photoresist for i-line UV light (λ = 365 nm) to be 3985 m^{-1} [3.5]. The reciprocal of α is called penetration length, L_p, which is the distance into the medium where the intensity of light decays to 1/e of its incident intensity. The penetration length of i-line UV in SU-8 is about 250 μm. In our work, SU-8 resist mold as thick as 250 μm have been developed cleanly when other processing parameters are chosen appropriately. SU-8 mold thicker than 300 μm has also been achieved but with significantly increased exposure time. The feature quality after development in the latter case is found to be also not as good compared to the previous case.

UV light intensity plays an important role in the process as well. If the UV light intensity is decreased significantly e.g. to 4~5 mW/cm^2, which may result from serious aging of the UV light lamp, the result after development is very poor for the same or even greater dose of light energy. The exposure time is greatly increased for this case to maintain the same UV dose. As a result, the reacted Photo Acid Generator (PAG) molecules now have longer time to diffuse into their surroundings where the resist is not exposed. These molecules will also cause resin cross-linking during the following post-exposure-bake and will make the size of the opening in the resist smaller, as schematically shown in Fig. 3.7. The lower resist receives less photons and hence has fewer reacted PAG molecules as indicated by a lighter shade in Fig. 3.7. This may also be one of the causes for the so-called T-topping phenomenon that has been frequently

observed in this work. T-topping stands for a trapezoidal resist column after development with upper part having a larger resist dimension or smaller opening. Consequently during electroplating, the electrolyte will have greater difficulty to diffuse into the microrecess because the cross-linked resist around the opening is narrower at the electrolyte entrance at the top.

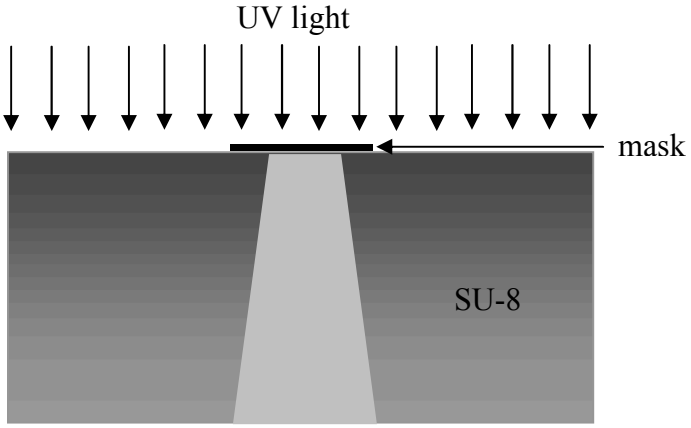


Figure 3.7: Diffusion of reacted photo acid generator (PAG) molecules during an extended UV exposure on thick photoresist. Darker shade stands for an area with more concentrated reacted PAG molecules. The situation gets worse when the incident light intensity is low.

Another reason for T-topping problem is that SU-8 photoresist has a very high absorption rate for UV wavelengths shorter than 350 nm. This shorter wavelength UV light tends to be absorbed near the surface of photoresist. In comparison, the UV light with longer wavelengths have a much lower absorption rate and is able to travel deeper into the photoresist and hence can be used for exposure of thick resist. The surface preferring absorption of UV light with shorter wavelengths can cause skin effect, i.e. overexposure near the photoresist surface. This significantly distorts the pattern near the surface, also resulting in T-topping. To solve this problem, an optical high pass filter (from Omega Optical) was utilized in this dissertation work to filter off most of the UV lights that have wavelengths shorter than 350nm to improve sidewall features of the microstructures. The filter employs multilayered thin film coatings permitting

transmission of light with wavelengths longer than the principle wavelength of 350 nm rather than being reflected. The principle wavelength is determined by precise control and arrangements of different layers of thin films.

Slightly higher exposure energy is required to guarantee light illumination throughout the entire resist layer thickness across the wafer. The exposure is performed on a mask aligner (Quintel S4000) in vacuum contact mode. Vacuum contact mode improves structure definition by reducing diffraction effects caused by air gap. In order to avoid deformation of the resist mold, no post-bake is carried out before the electrodeposition [3.12]. However, a post-exposure bake (PEB) step is performed following UV exposure, specifically for the negative-tone resist as described in the following section. PEB is different from the post-bake in that the former is performed after UV exposure while the latter is performed after development.

3.1.4 Post-Exposure Bake (PEB)

SU-8 is a deep UV (DUV) negative resist, which makes use of chemical amplification. During UV light exposure, the PAG molecules react with the incoming photons and create special acid molecules. These acid molecules then act as catalysts in a subsequent resist bake step (post-exposure bake or PEB) that changes the resist properties in the exposed regions. The key is that the reaction is catalytic, i.e. acid molecule is regenerated after each chemical reaction and may thus participate in tens or hundreds of further reactions. The heat input during PEB provides the energy needed for the catalytic reaction between the acid molecules and the resin groups which induces cross-linking to take place in the exposed parts of the resist.

Pre-bake generates a large internal stress due to solvent evaporation as shown in Figs. 3.5 and 3.6. This stress is largely released during PEB as the resist becomes softened since PEB temperature, 96 °C is higher than T_g (50 °C). However, cross-linking (polymerization) takes place during PEB as another stress-generation mode which contributes to the final internal stress

in the resist. During PEB, stress increases with elevation of temperature and eventually levels as the polymerization i.e. cross-linking at 96 °C is completed. If the photoresist is allowed to remain at 96 °C for a long time, the stress inside the film will slowly decrease due to relaxation. But in practice, temperature has to be lowered back to the room temperature. As a consequence, stress increases due to the CTE mismatch between substrate and photoresist. Lorenz et al. [3.10] have experimentally extracted the CTE of SU-8 as 52 ppm/°C which is a very high value compared to commonly used substrates such as silicon (2.3 ppm/°C) and glass (10 ppm/°C).

Cracking of SU-8 layer after PEB has been observed in this work due to the residual internal stress caused by polymerization during PEB and CTE mismatch after cooling to room temperature. In an effort to avoid this, a relaxation time between pre-bake and UV light exposure was allowed for the resist to rehydrate in open air at room temperature as suggested in reference [3.11].

Thick SU-8 photoresist retains much residual stress after the PEB step causing large exposed resist areas to debond from the substrate, and causing the silicon substrate to bow or even crack. These phenomena were observed in this work and by others [3.12-13] as SU-8 thickness was increased. For a 200 μm thick SU-8 layer spun on a 3-inch 380 μm thick wafer, the wafer bow could be as large as 300 μm for a completely exposed wafer after PEB [3.7]. Hence it is important during the mask design step to avoid large exposure areas in order to reduce the wafer bow caused by polymerization during the following PEB step. This idea has been taken into account during mask design process. Similar approach to alleviate stress is to isolate the exposed area into islands by taking advantage of some stress release by having exposed area surrounded by unpatterned areas.

3.1.5 Development

Each molecule of SU-8 has approximately 16 function side groups that can form a very dense three dimensional network of cross links when the resin is cured during post-exposure bake. In literature, most of the reported SU-8 resist microstructures are either stand alone columns, pillars or similar structures. Use of SU-8 as a photoresist matrix that contains deep microrecessed holes has rarely been reported. The reason for this is partially attributed to difficulties in development of the exposed resist. This is true especially when the microrecesses are deep and narrow making it difficult for the developing agent to diffuse into the recessed holes and dissolve the unexposed resist. Also, it is difficult for the dissolved mass to be transported outside of the narrow recesses. In this work, SU-8 is used as an electroplating mold for high-aspect-ratio microstructures that are deep empty columns. The electroplating mold hence comprises of holes which must be formed by materials removal by the developer. Hence, resist development has been a challenging issue throughout this work.

It is relatively easy to develop thin SU-8 resist with thickness less than 50 μm when the aspect-ratio of the columns typically less than 10. However, as SU-8 becomes thicker, the difficulty of obtaining a cleanly developed recessed hollow column increases significantly. For SU-8 resist layers thinner than 200 μm and with aspect-ratio less than 5, two standard petri-dishes of diameter 150 mm containing SU-8 developer are utilized for resist development. After development for a certain duration in the first dish, the wafer is transported into the other dish containing fresh developer for further development. When the thickness of resist increases, development at room temperature causes cracks in the resist due to release of internal stress. A typical image of cracks in 250 μm thick SU-8 is shown in Fig. 3.8. The development time increases significantly for a thicker resist. In order to reduce development time, a novel strategy of heating the developer is developed in this work. It is found that 10 minutes of development at

55 °C is sufficient to obtain a clean 100 μm deep SU-8 recessed hole column mold. A 200 ~ 250 μm thick SU-8 could be developed successfully in 30 minutes total soak time at 55 °C in a two petri-dish bath described above. In contrast, obtaining the same development results at room temperature took 1 or 2 hours. Mild manual stirring is necessary to help maintain a uniform developing process across the entire wafer. The development process has to be performed under sufficient ventilation inside a chemical hood because the SU-8 developer becomes more volatile as it is heated.

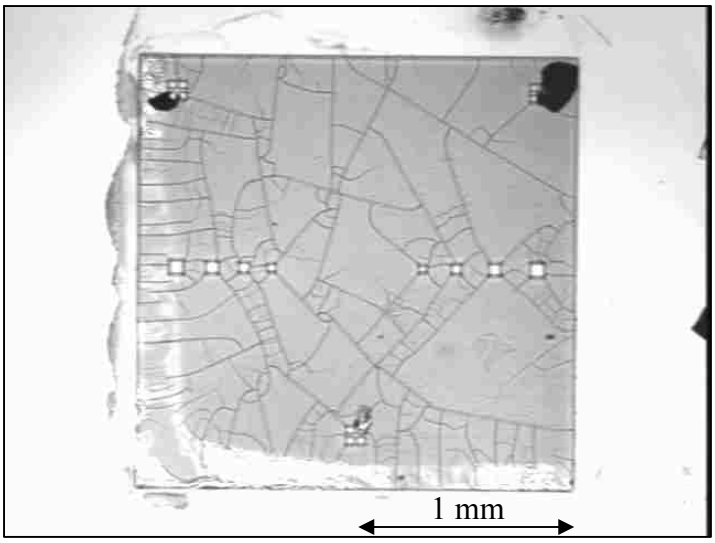


Figure 3.8: A microscope image of cracks in SU-8 resist which result during development at room temperature. The thickness of the resist is 250 μm.

As SU-8 resist thickness becomes even greater, elevated temperature development results in dissolvement of the parts of the resist that are readily accessible but it fails to dissolve unexposed resist at the bottom of the columnar recesses. Ultrasonic agitation helps the developer to diffuse deeper into the recesses but is usually not recommended as it may cause damage to delicate microstructure features that can ultimately lead to mechanical failure. Recently, megasonic tools have been utilized with some success in tackling this difficult problem of development to form deep holes [3.14]. Compared to ultrasonic agitation which operates under

100 kHz, the operation frequency of a megasonic tool is usually higher between 800 to 1000 kHz. The latter can generate much finer cavitation so that the bubble size is much smaller resulting in less damage. However, our laboratory does not have access to this expensive tool and hence necessitates development of alternative new processing techniques.

In this work, a special setup is built for developing thick SU-8 resist. The setup is shown in Fig. 3.9. A quartz tripod stand is designed and assembled at our on-campus glass shop. The substrate is immersed in developing solution with the resist side facing downward. Meanwhile, a magnetic stirrer bar is placed at the bottom of the beaker which rotates at a certain RPM during heat-assisted development at 55 °C. This setup takes the advantage of warm temperature development and a constant mechanical agitation, both of which were helpful in dissolving unexposed resist. Meanwhile, the resist side faces down which makes the agitated developer to enter the deep recesses more efficiently. With this setup, SU-8 mold up to 450 μm has been cleanly developed in our laboratory. A developed 250 μm thick resist mold is shown in Fig. 3.10. Notice that the smallest feature size of 20 μm × 20 μm holes on this sample are still not developed clearly. Also notice that there are still a few cracks existing inside the resist but this is significant improvement compared to Fig. 3.8.

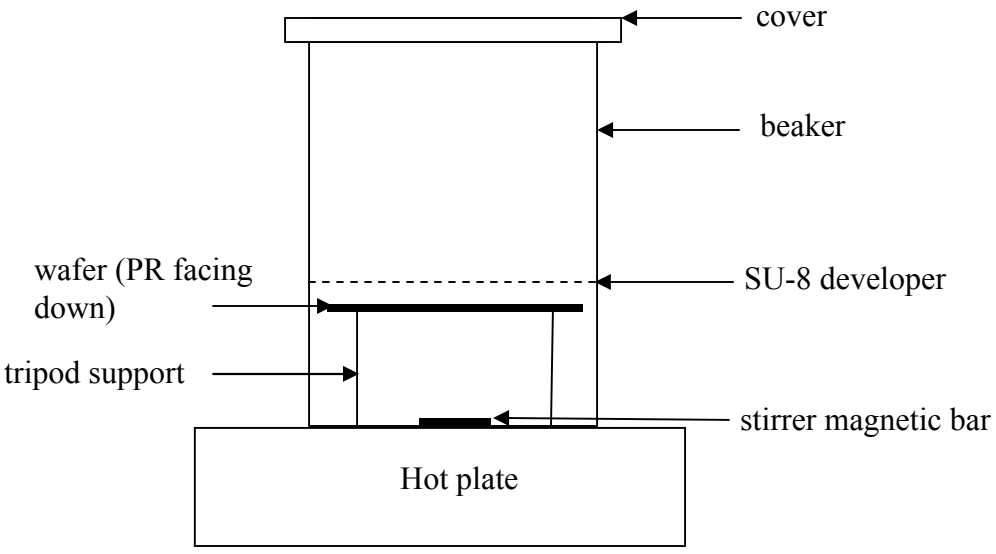


Figure 3.9: A special setup for developing thick SU-8 resist.

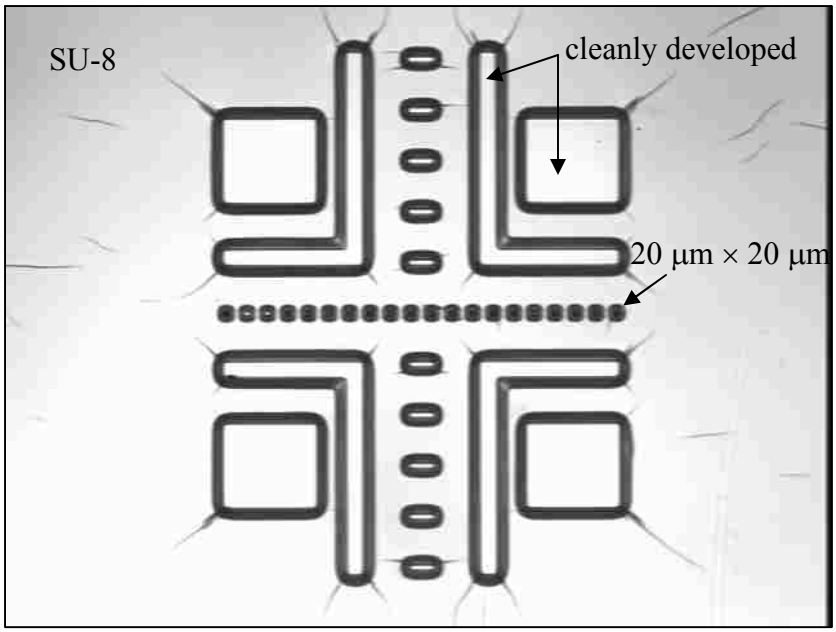


Figure 3.10: A microscope picture showing a cleanly developed SU-8 mold. Note that the smallest feature size of 20 μm is not developed clearly. The SU-8 resist thickness is 250 μm.

After development, the sample is rinsed in isopropyl alcohol (IPA) for about 3 minutes. The IPA is also heated up to the same temperature (55 °C) to avoid resist cracking due to sudden thermal shock. The sample is then put into an oven for dehydrating. The processing parameters are dependent on resist thickness. A couple of examples are given in section 3.2. It is then allowed to cool down naturally to room temperature by turning the oven off. The cool-down period is approximately 10 hours.

Processing of 250 μm and 450 μm thick SU-8 resist is described in the next section to provide examples that incorporate the specialized processing steps discussed above.

3.2 Examples of Thick SU-8 Process

3.2.1 Processing Steps for 250 μm Thick SU-8 50 Resist

The CMOS chips received from the foundry were 250 μm thick. Hence, a 250 μm thick SU-8 50 process is presented here first. An optimized process developed in this work includes

the following steps: spin coating, dwell-time on a flat surface, pre-baking, UV exposure, post-exposure bake, development of resist and cleaning.

The spin-coat process is shown in Fig. 3.11. After spin-coating, the beads are removed from the wafer edges and the wafer is leveled on a flat surface for 30 minutes. During this dwell-time, the resist uniformly levels out across the entire wafer surface.

Pre-bake is performed next. Temperature ramp up steps during the pre-bake cycle are depicted in Fig. 3.12. The substrate is seated on the pre-adjusted leveling hot plate in an oven followed by an in-oven cool down after 230 minutes from the start. The cool down period usually takes over 10 hours to return to room temperature.

After the wafer is cooled down to room temperature in the oven, UV light exposure is performed using a Quintel Model 4000 mask aligner. The light dose is 1350 mJ/cm^2. The UV light is produced by a Hg lamp. Wavelength less than 350 nm is mostly filtered out by an optical filter to avoid over-exposure near the resist surface.

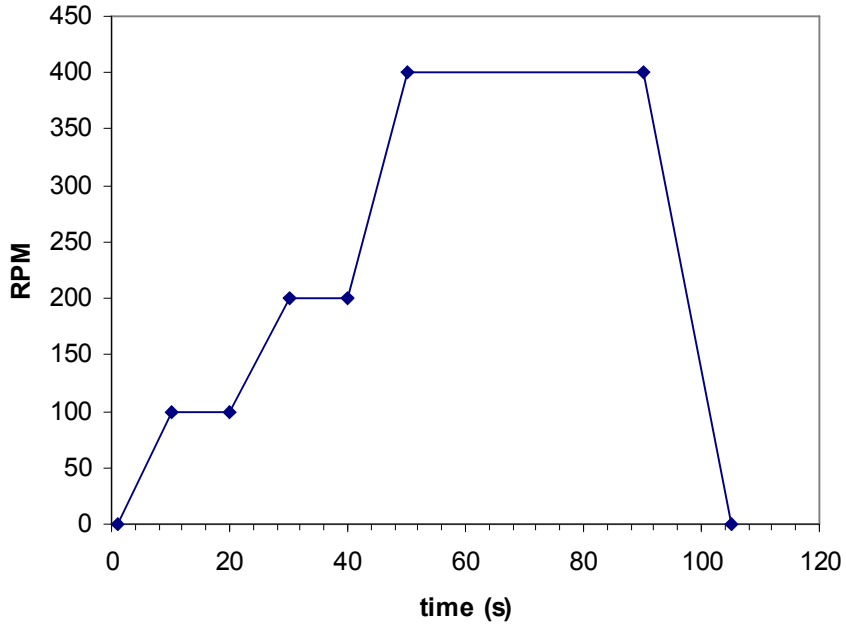


Figure 3.11: Spin-coat cycle for obtaining 250 μm thick SU-8 50.

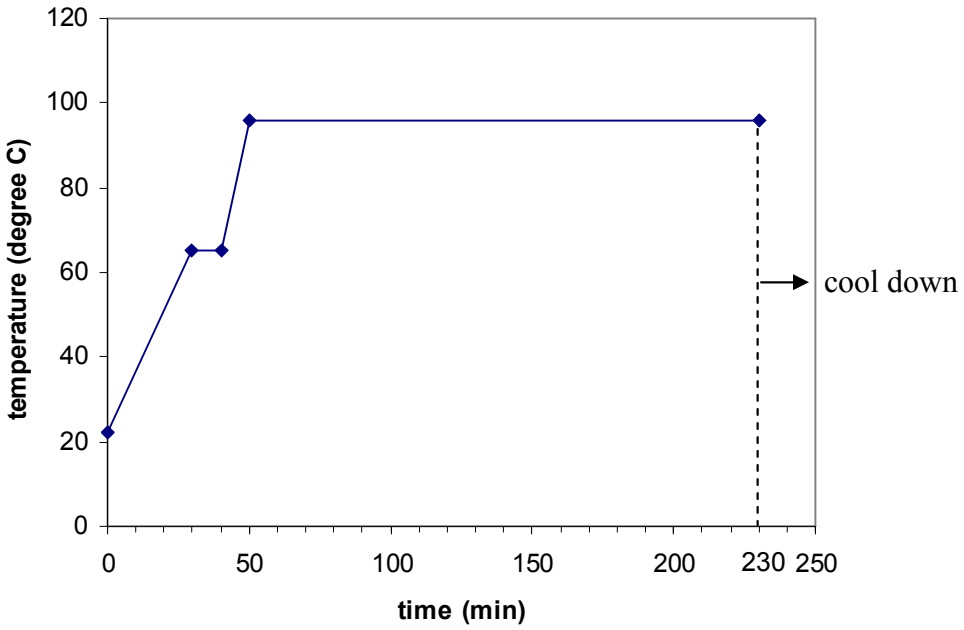


Figure 3.12: Oven pre-bake cycle for 250 μm thick SU-8 50.

The next step is PEB. The thermal cycle for PEB is shown in Fig. 3.13. The oven is switched off after 75 minutes as indicated in Fig. 3.13 and the substrate is allowed to cool down naturally inside the oven. Note that during PEB, the substrate is placed directly on the oven rack and not on a hot plate because the latter would provide heat to the resist from the thick leveling plate at the bottom and cause deformation of the exposed pattern.

The development process has already been stated in Section 3.1.5.

3.2.2 Processing Steps for 450 μm Thick SU-8 50 Resist

The major steps needed to process 450 μm thick SU-8 layers are the same as for the 250 μm thick SU-8 resist. The main differences between the two processes are given in Table 3.2. The differences are: 1) the final spin rate, which is 300 RPM for 40 s for 450 μm case; 2) final pre-bake time for the 450 μm case, which for the same temperature is 5 hr 15 min; 3) the UV dose, which is 1850 mJ/cm^2 for the 450 μm case and 4) the PEB time, which is 30 min for the same temperature. Development needs two baths of fresh SU-8 developer for both cases. The

development is carried out for 20 min in the first bath and for 40 min in the second bath. Optimal development temperature is 55 °C. Development solution is stirred using a magnetic stir bar as shown in Fig. 3.9.

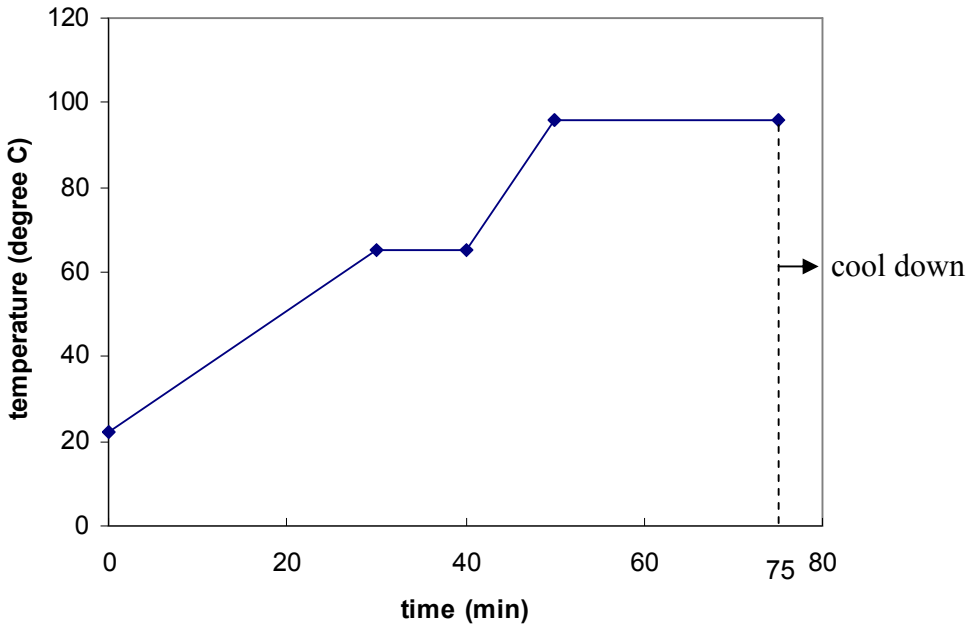


Figure 3.13: Oven thermal cycle for PEB for 250 μm thick SU-8 50 resist.

Table 3.2 Differences in the processing parameter values for the 250 μm and the 450 μm thick SU-8 50 resist cases.

Parameter	**250 μm case**	**450 μm case**	**Comments**
Final spin-coating rate	400 RPM	300 RPM	Same 15 sec ramp down time
Final pre-bake time	3 hrs	5.25 hrs	Same pre-bake temperature
UV exposure dose	1350 mJ/cm^2	1850 mJ/cm^2	Wavelength ≤ 350 nm is filtered out
PEB time	25 min	30 min	Same PEB temperature

3.3 Thin Photoresist Processing

3.3.1 Processing Steps for 2~3 μm Thick SU-8 2 Resist

A thin photoresist layer is also needed in this work to separate the chip surface from the metal seed layer used for electroplating nickel probes for a later step. Lithography is performed on this thin resist layer to open windows for the areas where metal contacts comprising of an adhesion layer and a seed layer for microprobes are needed. The most diluted resist in the SU-8 family that provides a thin coating is SU-8 2 and hence it is chosen here. The spin-coating steps are shown in Fig. 3.14. Pre-bake of such a thin resist layer does not need special care such as bead removal or strict leveling requirement as is the case for thicker resists. After spin coating, the sample wafer is put into an oven at 96 °C without a ramp step and baked for 15 minutes. No in-oven cooling down time is necessary and the wafer can be taken out immediately after the pre-bake cycle since the thermal stresses produced in such a thin layer of resist are small. UV light dose during exposure is 20 mJ/cm^2 and no optical filter is needed as the pattern deformation is negligible for thin resist. PEB step is a short duration bake in an oven at 96 °C for 4 min. Development is performed under room temperature for a short duration of only 30 seconds.

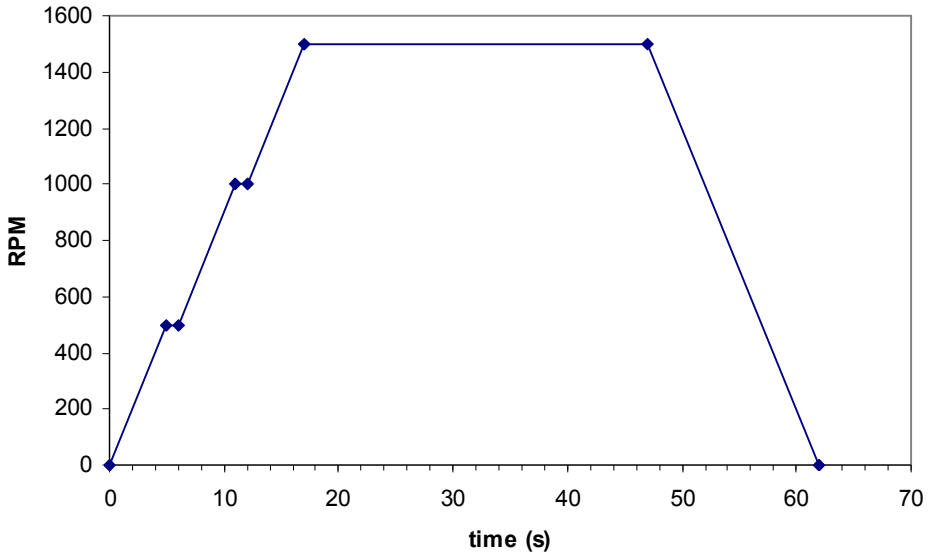


Figure 3.14: Spin-coating cycle for 2 to 3μm thick SU-8 2 resist layer.

3.3.2 Processing Steps for 1 μm Thick HR 200 Resist

A negative tone photoresist, HR 200 can provide an even thinner coating approximately 1 μm thick. The development and final removal process for HR 200 are somewhat more difficult. Therefore, SU-8 2 resist is mostly utilized as a separation layer in this work considering the ease of process integration. The spin-coating cycle of HR 200 is shown in Fig. 3.15 followed by a pre-bake process shown in Fig. 3.16.

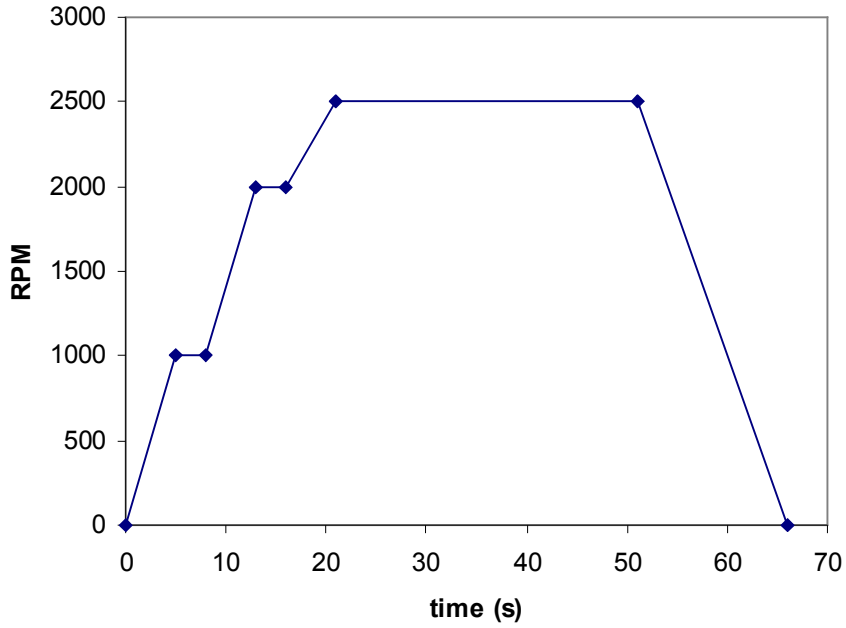


Figure 3.15: Spin-coating cycle for 1 μm thick HR 200 resist.

UV dose to expose 1 μm thick HR 200 resist is 50 mJ/cm^2. Development is performed in WNRD developer (Waycoat Negative Resist Developer, from Olin Corporation). It is difficult to dissolve the unexposed HR 200 resist in a still developer. Usually it takes approximately 5 minutes for complete development in an ultrasonic medium at 20 kHz. The sample is then rinsed in IPA for 5 minutes and then placed in an oven for a short dehydration period.

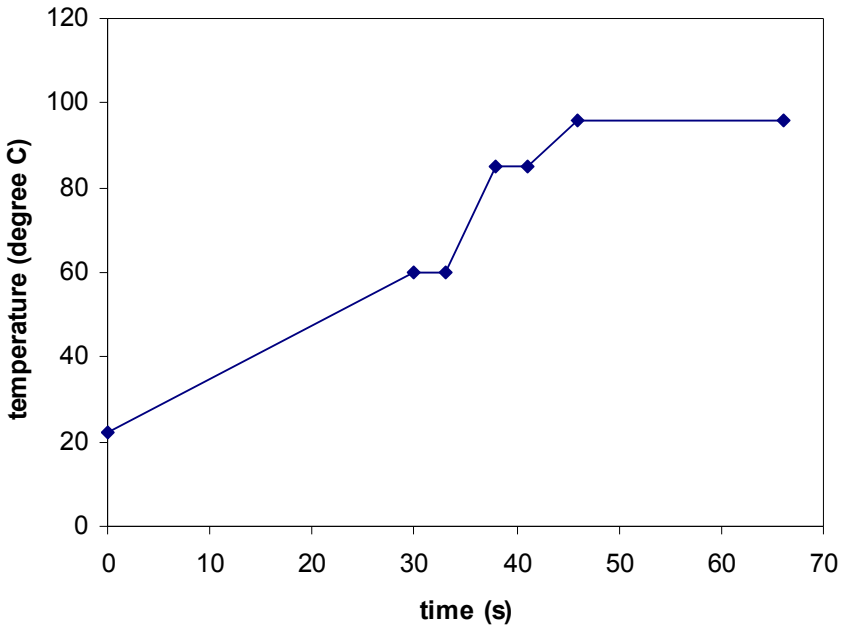


Figure 3.16: Pre-bake cycle for 1 μm thick HR 200 photoresist.

Complete removal of exposed HR 200 is also difficult. Usually immersing exposed resist in acetone for a certain period of time works for complete removal of SU-8 photoresist regardless of how thick it is but it does not work for HR 200, even when it is just 1 μm thick. A complete removal of exposed resist in acetone results in the entire layer of resist swollen by the solvent lifted often with the embedded electroplated microstructures. This process is distinct from being dissolved and hence can not be used when electroplated metal structures must be retained. Immersion in remover PG (MicroChem) at elevated temperature also does not work for this case. Complete removal of HR 200 is accomplished by a dry etch that utilizes a plasma asher (Anatech SP100). The recipe is listed is Table 3.3.

3.3.3 Coating and Processing of S1813 Resist

S1813 is a positive photoresist manufactured by Shipley and can provide resist layer as thin as 1 μm. It is employed as a sacrificial layer during lift-off in this work. It is also used as a

mask during silicon oxide etching step. Spin-coating cycle for S1813 resist is shown in Fig. 3.17. A 50 second spin cycle at 2000 RPM gives a 1 μm thick coating.

Table 3.3 Dry etch process to remove 1 μm thick exposed HR 200 resist in Anatech SP100 barrel asher.

Parameter	Content/Value
Plasma ambient	oxygen
Pressure	450 mTorr
Power	60 W
Time	1 hour
Substrate heating	no

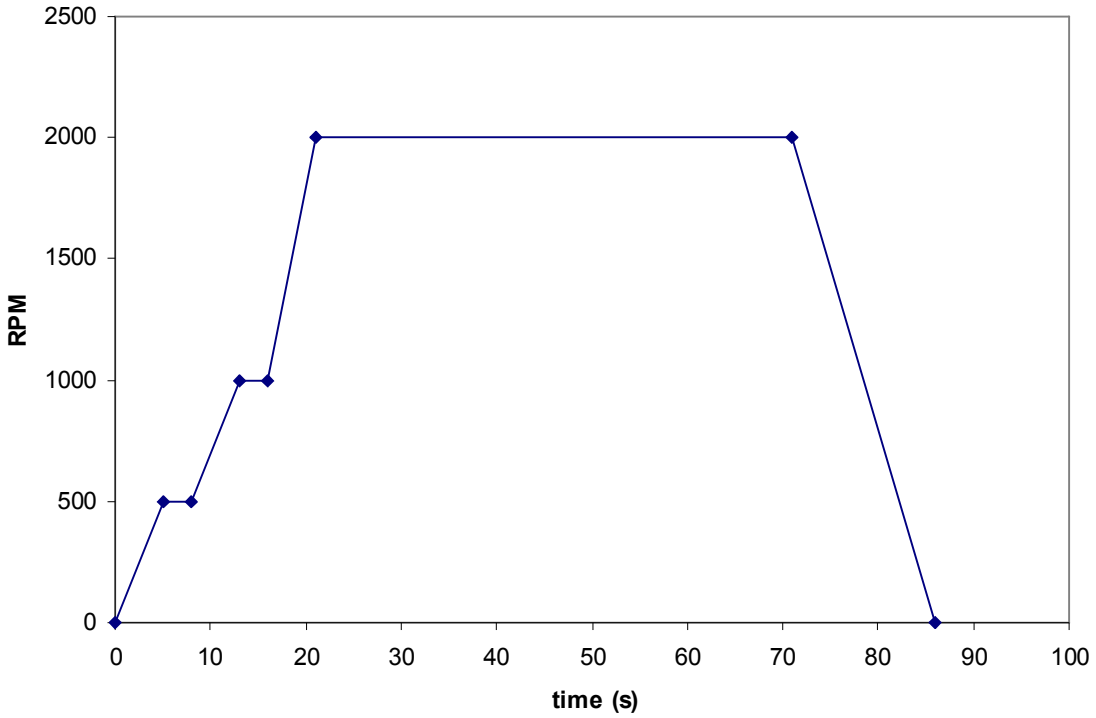


Figure 3.17: Spin-coating cycle of approximately 1 μm thick S1813 positive resist.

Pre-bake cycle is easy for S1813 resist. The oven is pre-heated to 99 °C and the wafer is loaded into the oven, kept for 30 min and then taken out immediately. UV light exposure dosage used is 60 mJ/cm^2. Development is performed in a developer for positive resist, such as MF 354 or MF 319 from Shipley. The wafer is immersed in the developer bath for one minute to

complete the development process. After this, wafer is flushed under running DI water to rinse off the chemical. During post-bake (hard bake), the wafer is loaded into a pre-heated oven at 99 °C and left in for 45 minutes. The wafer then can be immediately removed from the oven for further processing.

3.3.4 Omnicoat Process

Omnicoat (MicroChem) can be employed prior to the SU-8 spin-coating in order to promote adhesion between the resist and the substrate. It has also been shown that it can promote uniformity of the spin-coated photoresist in this work. Omnicoat application includes the following steps: spin-coating, pre-bake at 100 °C in oven for 5 minutes. Removal of Omincoat is a necessary step to expose seed layer after the SU-8 electroplating mold is developed. The Omnicoat layer is removed in an oxygen plasma. Spin-coating cycle is shown in Fig. 3.18. Although Omnicoat can provide better adhesion, it introduces additional complications to the process and is used only at certain specific times in this work.

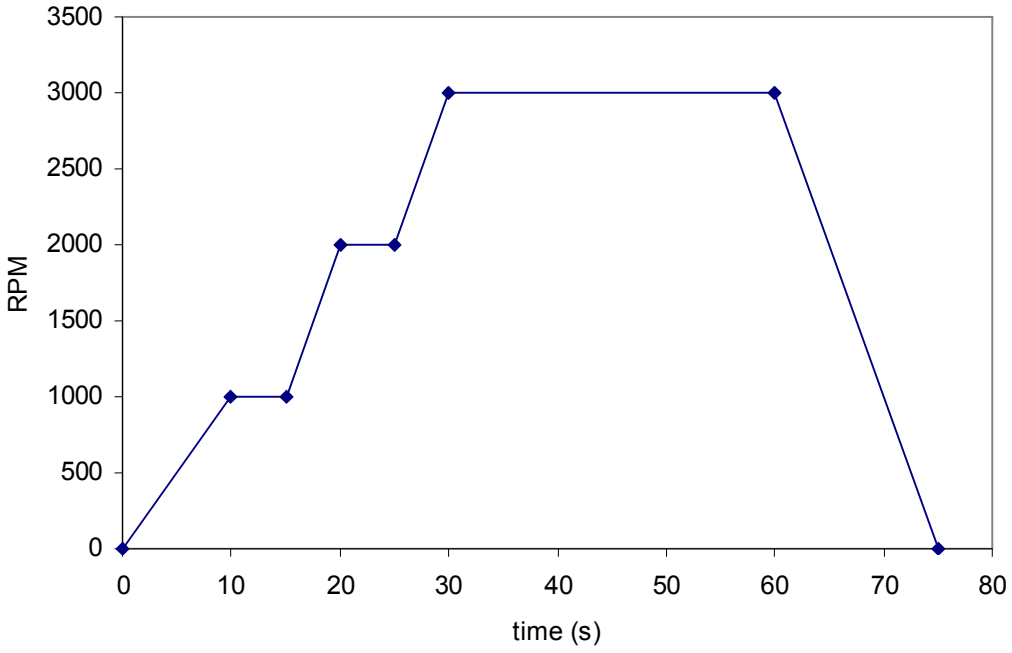


Figure 3.18: Spin-coating cycle for Omnicoat.

3.4 Summary

Thick and thin photoresists processing steps utilized in this work are described in detail in this chapter. The general processing procedures include spin-coating, pre-bake cycle, UV light exposure, post-exposure bake cycle for photoresists containing PAG (such as SU-8 in this work), development, rinsing, dehydration, and necessary post-bake if needed.

For SU-8 resists, special care is required in every processing step, such as sufficiently slow ramping-up and ramping-down during each bake cycle. A very important step is resist development that determines the quality of the electroplating mold. Processing parameters are tailored to satisfy this requirement. A new heat-assisted resist development method that reduces development time is employed in this work thereby significantly accelerating the development process. Much of the work reported in literature on thick SU-8 is for fabrication of resist posts. In contrast, this work involves deep microrecesses that are formed in thick SU-8 resists, which makes the entire fabrication process more difficult, especially during the resist development processing step. A specially designed kit for resist development is utilized in this work for resist thicker than 200 μm. This has helped in obtaining a clean, good quality electroplating mold in SU-8 up to 450 μm thick. Electroplating mold fabrication for an array of recessed holes in SU-8 resist beyond 450 μm thick has not been successful. The latter process may need special processing tool such as a megasonic tool, which is currently not available in our laboratory.

Another challenge in dealing with thick resist such as SU-8 is the presence of considerable built-in stress resulting from multiple thermal cycles due to differences in the thermal expansion coefficients of the substrate and the resist. Internal stress results in resist cracking and in delamination of the resist from the substrate. Among all processing steps, slow cooling cycle, sufficient UV light dose with the use of an optical filter to cut off short

wavelength light and moderate heat input during PEB are among the most important factors to control the internal stress in thick resists.

Chapter 4. Nickel Electroplating

4.1 Introduction

Nickel electroplating setup utilized in this study is similar to other electroplating processes that employ soluble metal anodes. In this work, a 10 cm × 10 cm square nickel plate of 99.99% purity is utilized as an anode. Electroplating requires passage of current between the anode and the cathode immersed in a conductive, aqueous solution of nickel salts. Flow of the current in the circuit loop causes the anode to dissolve causing the nickel atoms to enter the electrolyte as cations, and the cathode to be covered with nickel. The discharge of nickel ions at the cathode is not the only reaction that occurs in this process. For nickel deposition, the electrolyte is usually acidic even though its pH value is not very low. A small percentage of current is hence consumed to discharge hydrogen atoms from water. The discharged hydrogen atoms form bubbles of hydrogen gas that evolve from the cathode surface. As a consequence, the concentration of nickel ion and pH value of the electrolyte increases slowly as electroplating progresses if no pH buffer is present. From another point of view, the increase of nickel ion concentration results from the fact that the anode efficiency is always 100 percent i.e. the current is 100 percent efficient at the anode in dissolving nickel while the cathode efficiency is less than 100 percent i.e. a small portion of current is consumed by side reactions such as hydrogen gas evolution with the remaining portion contributing to nickel deposition.

4.1.1 Electrolyte Composition

Four commonly employed baths for nickel electroplating are Watts bath, chloride bath, sulfamate bath and Woods bath [4.1]. The basic functional plating chemicals include nickel sulfate, nickel chloride, nickel sulfamate and nickel carbonate. The formula and concentration of functional chemicals are listed in Table 4.1.

Table 4.1 Functional chemicals in commonly used electrolytes.

Chemical name	Formula	Nickel weight percentage
Nickel sulfate	$NiSO_4 \cdot 6H_2O$	22.3%
Nickel chloride	$NiCl_2 \cdot 6H_2O$	24.7%
Nickel sulfamate	$Ni(NH_2SO_3)_2$	23.2%
Nickel carbonate	$NiCO_3$	46%

Boric acid, H_3BO_3 is usually added in a nickel electroplating bath as a pH buffer [4.2]. When hydrogen gas forms at the cathode surface, it leaves behind OH^- group that raises pH value at the surface of the cathode. Boric acid has the capability of dissociating into H^+ ions and $H_2BO_3^-$ groups that provide one H^+ ion to neutralize the OH^- group. The pH value is thus maintained at an approximately constant value for a longer electroplating period. Lauryl sulfate is usually added as a surfactant [4.3]. Surfactant is a wetting agent, which reduces the surface tension of water so that the electrolyte can easily wet the photoresist mold surface. The recipe for nickel electroplating solution used in this study is shown in Table 4.2. Electroplating temperature is maintained at 53 °C in a water bath and pH value is kept at 3.6. Electroplating is performed in a home-designed plating cell shown in Fig. 4.1. The distance between two electrodes is maintained at 10 cm. A motor-driven blade stirrer is placed at an equal distance to both electrodes with a constant rotating rate of 200 RPM.

4.1.2 Pretreatment of Substrate

For all the electroplating samples used in this dissertation work, a Ti adhesion layer and a Cu seed layer are applied to the wafer or the chip substrate. The combination layers of Ti and Cu

Table 4.2 Recipe for 1 l nickel sulfamate electrolyte.

Components	**Quantity**
Concentrated nickel sulfamate $[Ni(SO_3NH_2)_2]$, solution in water. 1:1 ratio by weight for salt : water	450 ml
Boric acid	37.5 g
Lauryl sulfate	3 g
DI water	add to make 1 l of solution

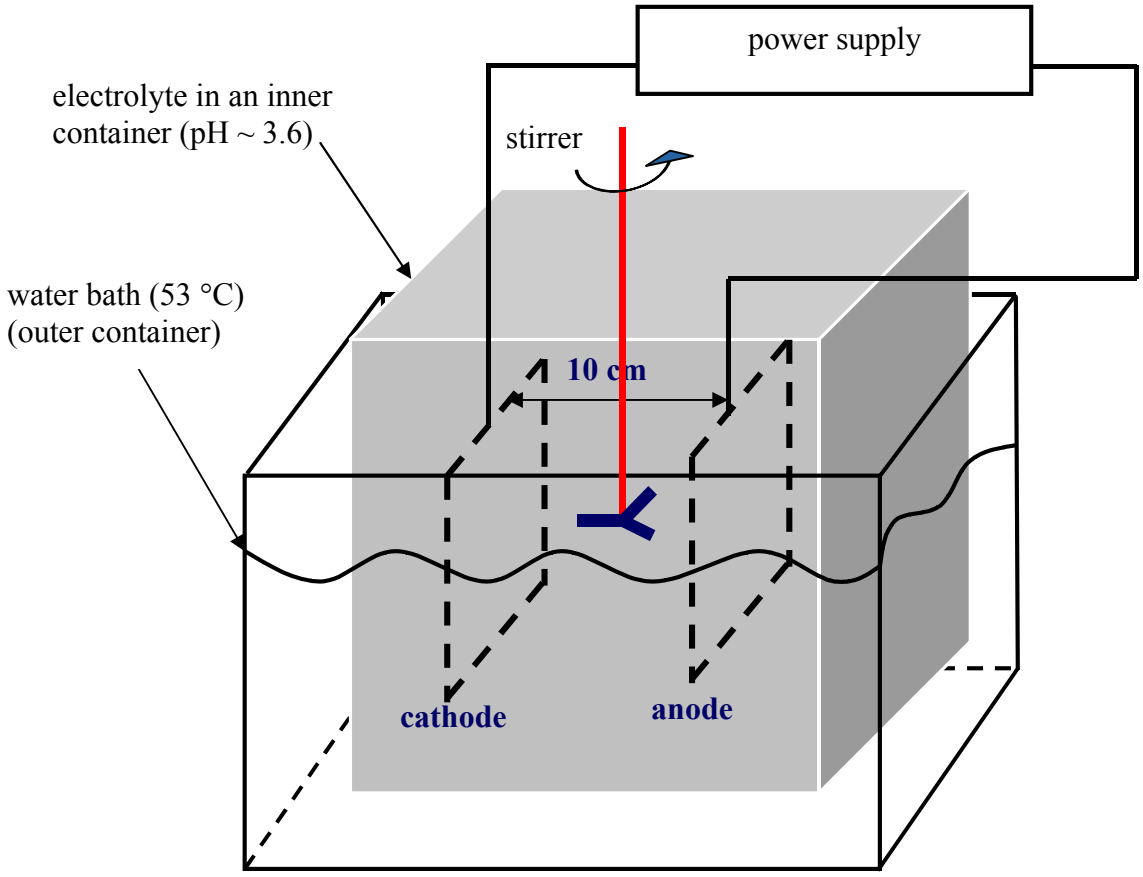


Figure 4.1: Geometry of the electroplating cell.

are sputter-coated in an Edwards 200 multi-target DC/RF sputtering system in an Ar ambient at 200 W. The thickness of deposited Ti layer is 50 nm and that of the deposited Cu layer is 500 nm.

The substrate is pretreated prior to immersion in the electroplating bath in order 1) to remove any native oxide that may have grown on the seed layer in previous processing steps and 2) to reduce surface tension at the time of immersion. The substrate pretreatment steps are listed below.

1. Dip wafer into dilute $CuSO_4$ solution (pH~1.0) for a few seconds to remove any native oxide present on the Cu electroplating base layer.
2. Apply a small amount of IPA to the surface of the electroplating mold. IPA can easily wet the insides of the photoresist walls and guide the electrolyte to reach the base of the electroplating mold. It also readily dissolves in DI water. Caution is needed here since IPA evaporate readily and also carries heat away from the photoresist mold as it evaporates. This can generate additional thermal stress in the resist and consequently may result in cracks in the electroplating mold. This is especially important when the photoresist is thick.

4.2 DC Electroplating

DC plating is the most commonly employed method for electrodeposition, especially in the commercial processes due to its relatively simple equipment and operational requirements [4.4]. DC plating setup is simple, straightforward and cost-effective. Most of the metallic alloys and multilayer systems can be electrodeposited by both DC and pulse plating techniques. In comparison to DC plating where a constant current flows from anode to cathode, pulse plating utilizes current pulses. Pulse plating has been used in electroplating elemental metallic materials, alloys and even composites and often offers process flexibility that can yield superior deposit quality. However, choice of a plating technique for a particular application is based on practical considerations depending on overall need, requirement and cost.

4.2.1 Current Efficiency – Galvanostatic

During plating, multiple reactions may happen at the cathode surface depending on their respective electrode overpotential values. Metal deposition being not the only reaction at the cathode surface can result in current efficiency lower than 100%.

Current efficiency γ is defined as the ratio between the mass m gained through electrodeposition experimentally over theoretical maximum mass m_0 that can be gained as calculated from the Faraday's law: $\gamma = \frac{m}{m_0} \times 100\%$.

From Faraday's law: $m_0 = \frac{sMIt}{nF}$ [4.5], where s is the number of ions involved in each elemental reaction, M is the molar molecular mass, I is the cathodic current, t is the electroplating time, n is the number of electrons associated with the reaction and F is the Faraday's constant, i.e. 96485 C/mole. For nickel electroplating case: $Ni^{2+} + 2e^- \Leftrightarrow Ni$. Here, one nickel ion accepts two electrons to become a neutral atom, thus s =1 and n = 2. M_{Ni} = 58.69 g/mol. Note that m_0 is proportional to the product of I and t.

Current efficiency is investigated for nickel sulfamate electrolyte. The exposed area of metal seed layer is 7.5 cm^2 on a flat Si wafer coated with Ti/Cu base layer. The plating temperature is 53 °C. The concentration of nickel sulfamate is 1.52 M. The experimental data is listed in Table 4.3 and is also shown in Fig. 4.2. It is seen that current efficiency increases with an increase in current density. At lower current density, the current efficiency is lower, indicating a greater portion of the cathodic current is consumed by side reactions. As current density increases to 20 mA/cm^2, the current efficiency approaches to 98%, which implies that at this point almost all of the cathodic current is consumed by nickel electrodeposition. The standard electrode potential in aqueous solution at 25 °C for $Ni^{+2} + 2e^- \Leftrightarrow Ni$ is known to be -0.23 V

versus a standard hydrogen electrode, $2H^+ + 2e^- \Leftrightarrow H_2$. As the applied cathode potential, E, becomes more negative, i.e. greater cathodic current, the portion of cathodic current contributing to H_2 evolution becomes smaller resulting in a higher current efficiency. Similar observations is given in reference [4.6] where current efficiency is found to increase from 60% to almost 100% as current density increases in deposition of sub micron gold wires. Further explanation to the change in current efficiency needs a detail investigation on electrode kinetics.

Table 4.3 Current efficiency γ vs. DC current density for nickel electrodeposition utilizing nickel sulfamate electrolyte. Plating time is 1 hr for all samples.

Run No.	j (mA/cm^2)	Mass before plating (g)	Mass after plating (g)	M (g)	m_0 (g)	γ (%)
1	1	4.648	4.651	0.003	0.0082	37.5
2	5	4.670	4.700	0.03	0.041	73.0
3	10	4.700	4.779	0.079	0.82	96.3
4	20	4.643	4.802	0.159	0.164	98.1

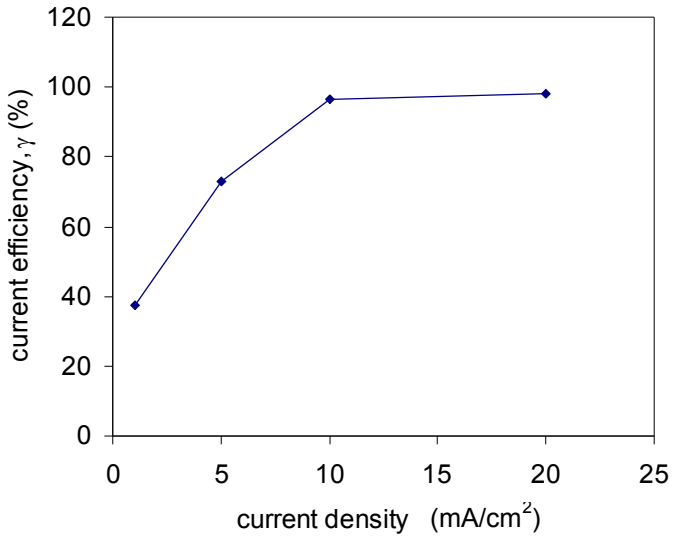


Figure 4.2: Current efficiency vs. DC current density for nickel electrodeposition in a nickel sulfamate electrolyte.

4.2.2 Plating Rate

Electroplating rate vs. current density for DC plating is shown in Fig. 4.3. As can be seen from Fig. 4.3, the electroplating rate increases linearly with the DC current density for current densities greater than approximately 10 mA/cm^2. The slope gives the rate of plating rate increase as a function of current density as 0.904 (μm/hr)/(mA/cm^2). The substrate used in this work is a silicon wafer coated with a Ti adhesion layer and a Cu seed layer.

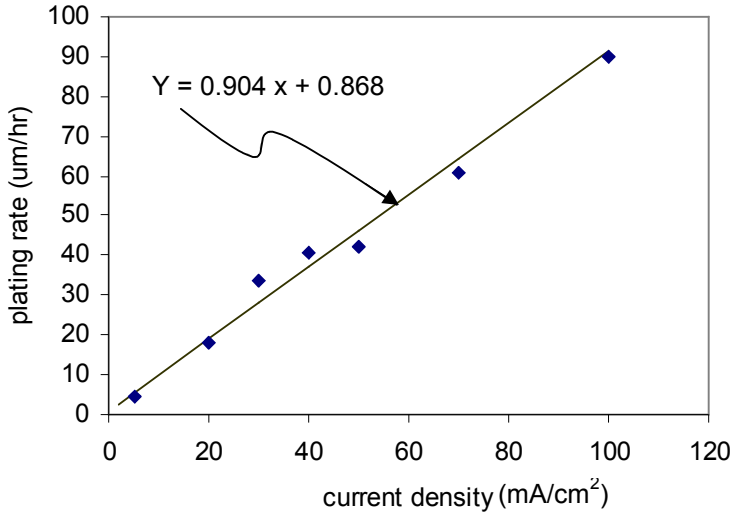


Figure 4.3: Nickel electroplating rate vs. DC current density in nickel sulfamate electrolyte.

4.2.3 Uneven Profile Caused by Non-Uniform Distribution of Field Lines

Electroplating into deep microrecessed molds for high-aspect-ratio microstructures is a complicated process that usually involves mass and heat transport considerations and concepts from fluidics and reaction kinetics [4.7]. In addition, the distribution of electrical field lines is not uniform within the recessed mold. The electric field is usually denser at the edge and sparser at the center, as is schematically shown in Fig 4.4. Correspondingly, thickness of the plated nickel varies from the center to the edges. Figure 4.5 shows a SEM image of a DC plated square probes 70 μm tall and 80 μm on side. Current density was 10 mA/cm^2. Apparently, electroplating rate at

center area is slower than the edge area. Another picture is shown in Fig. 4.6 which is an extreme case. In this latter case, which used nickel sulfate rather than nickel sulfamate electrolyte, the current density was 4 mA/cm^2. The above explanation for field enhanced peripheral deposition does not apply for the case in Fig. 4.6 as the center depression on the probe top is too abrupt. A probably cause is current efficiency due to a low value for current density used, which results in trapping of H_2 gas evolving from side reactions at the cathode surface and blocking the plating process at the center.

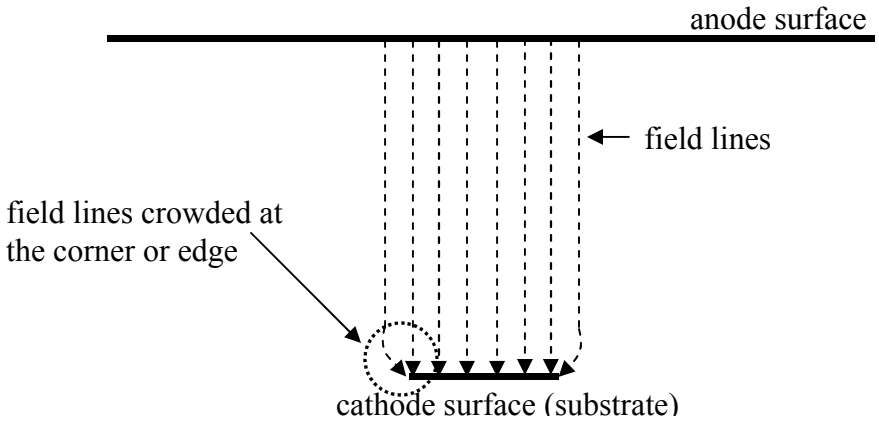


Figure 4.4: A schematic showing fields lines, which are denser at corner or edge of the exposed cathode surface.

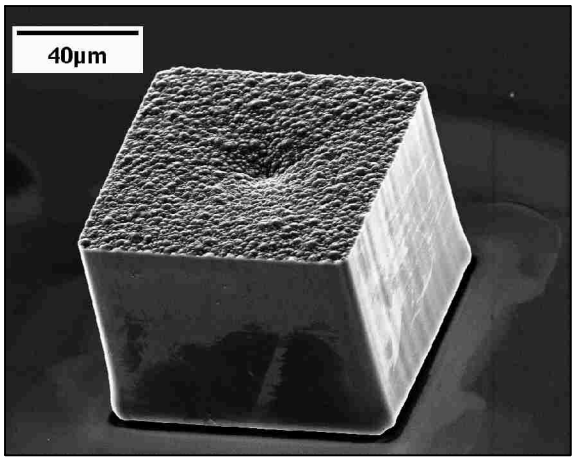


Figure 4.5: A SEM image showing that the peripheral area is plated at a faster rate compared to the center. DC plating, current density is 10 mA/cm^2.

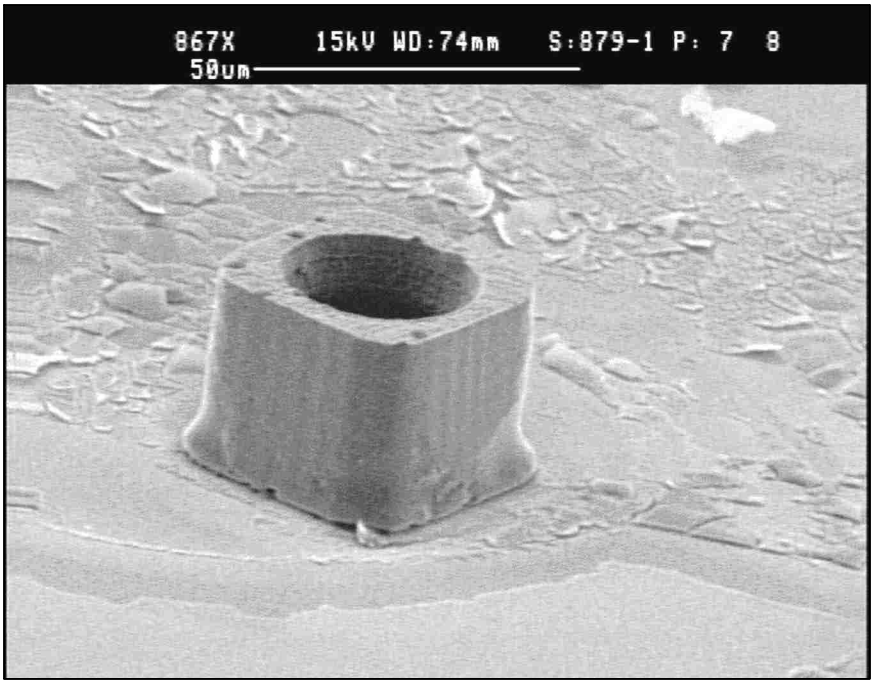


Figure 4.6: Peripheral field effect is even more severe using nickel sulfate electrolyte. DC plating current density is 4 mA/cm^2.

4.2.4 Uneven Probe Heights Caused by Size Differences

Nickel is electroplated into microprobe recesses having different sizes. The edge effect enhancement is seen to depend on the probe dimension. The smaller probes are plated at a faster rate. Profile scanned by a Tencor surface step profiler for structures electroplated at 10 mA/cm^2 current density is shown in Fig. 4.7. The nominal probe widths from left to right are 70 μm, 60 μm, 50 μm and 40 μm, respectively. As can be seen in this figure, the probe having smallest dimension was plated at a slightly faster rate compared to probes with larger dimensions. Another phenomenon is the surface profile at the top of probes with smaller dimensions is smoother compared to larger probes. It will be seen in a section 4.3.1 that the distribution of height versus probe dimension is reversed as diffusion controlled regime for electrodeposition is approached. The smaller recesses will suffer greater diffusion resistance resulting in a slower plating rate.

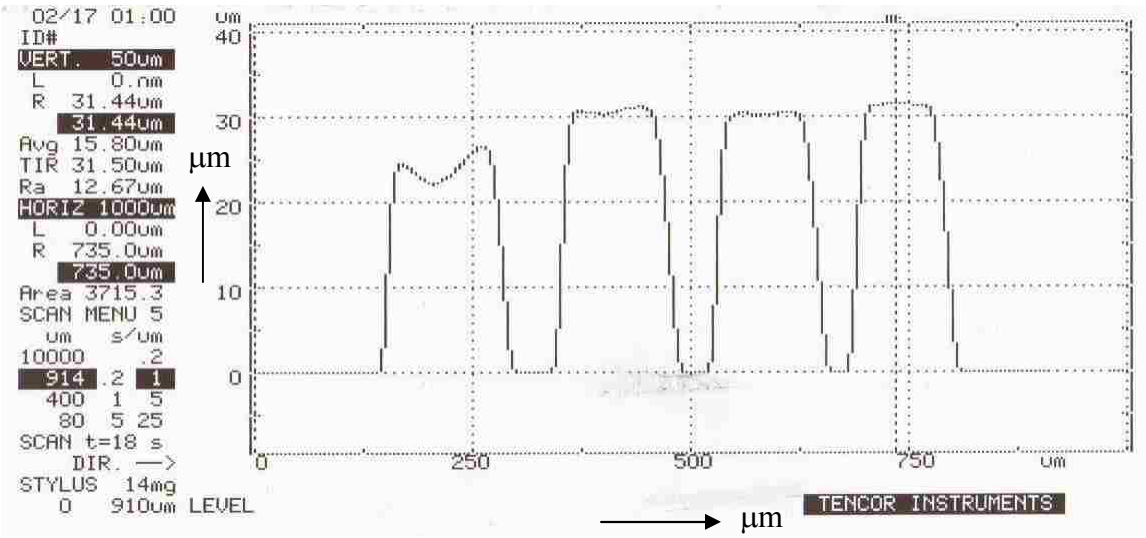


Figure 4.7: Probe height profiles for different probe widths. The plating current density is 10 mA/cm^2. Smaller probes are electroplated at a faster rate under DC plating prior to reaching diffusion controlled regime.

Another phenomenon observed in plating through deep recesses is shown is Fig. 4.8, in which probes with the smallest dimensions are slightly overplated on top compared to probes with larger dimensions. The latter do not show this effect. The nominal probe widths in Fig. 4.8 are 70 μm, 60 μm, 50 μm and 40 μm from left to right, respectively. Probe height in this picture is 210 μm. This also is consistent with our previous observation that smaller probes are plated at a higher rate.

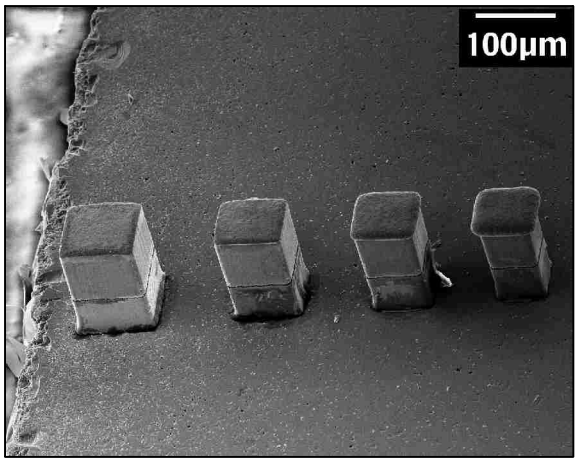


Figure 4.8: Thinner probes plate faster and are prone to overplating for the DC case.

4.2.5 Non-Uniformity of Plating Rate Caused by Probe Spacing

More closely spaced microstructures grow at a faster rate compared to the sparsely spaced microstructures. This is probably also due to a denser field lines distributed on a more concentrated cathode surface area. This is shown in Fig. 4.9. The sparsely spaced four probes having probe widths of 70, 60, 50 and 40 μm pertain to center to center spacings of 195, 175 and 155 μm from left to right, respectively. The closely spaced four probes having varying widths of 40, 50, 60 and 70 μm pertain to respective center to center spacings of 125, 145 and 165 μm from left to right. Figure 4.10 gives a closer view of the set of the densely packed probes, which are seriously overplated. The white color debris between the probes is SU-8 resist. The resist was not completely removed in the small fissures between the probes.

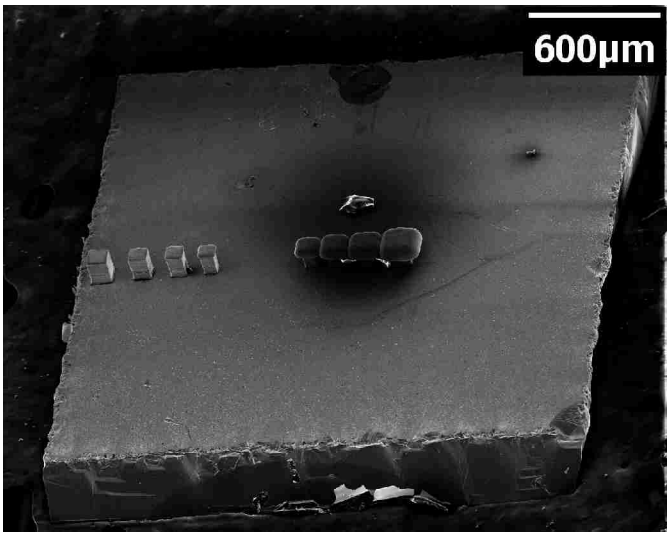


Figure 4.9: A picture showing faster plating rate with overplating on more densely packed probes for the DC case.

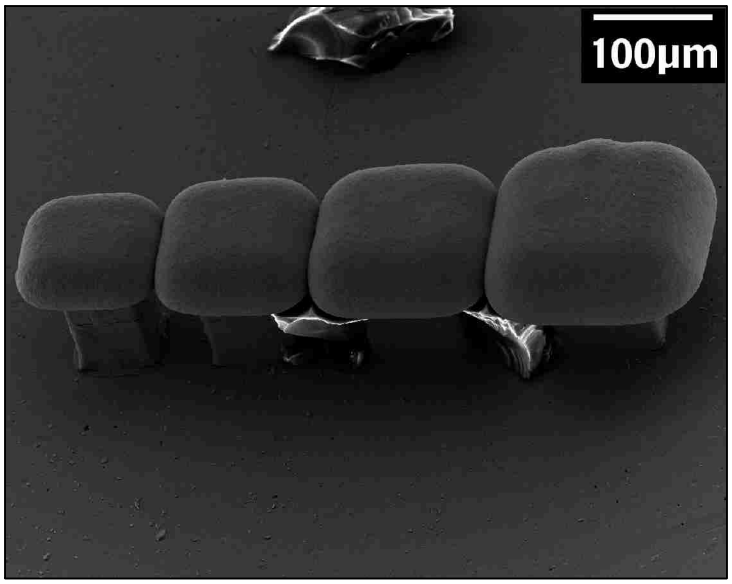


Figure 4.10: Overplated densely spaced nickel columns.

4.3 Diffusion Effects in DC Plating

In either DC plating or in pulse plating during on time, there is a cathodic current flowing through the electroplating circuit. With an increase in the overpotential at the cathode surface, the cathodic current is controlled by three mechanisms in the following sequence: 1) the kinetic controlled regime, 2) the kinetic-diffusion mixed controlled regime, and 3) the diffusion controlled regime [4.5]. This is schematically shown in Fig. 4.11. At first, current density is restricted by the surface reaction kinetics when the cathodic overpotential is relatively low. As the overpotential increases, the mass transport rate can not keep up with the increase of reaction rate at the cathodic surface. Hence, the rate of current increase is slowed down and the diffusion controlled regime gradually phases in. Concentration gradient of reactive species comes into picture when diffusion starts limiting the mass transportation making the concentration at the cathodic surface lower than the bulk value. Further increase of the overpotential will accelerate the reaction rate that eventually depletes all of the reactive species right away as soon as they are

transported to the charge transfer region at the cathode surface. This narrow charge transfer region is called double layer [4.5]. It is in the scale of one nanometer where electric field magnitude is very large, usually in the range of 1 MV/cm [4.5]. Driven by such a large electric field, electrons at the cathode surface quickly neutralize the cations that have been transported adjacent to the double layer zone. As a consequence, the neutralized atoms or molecules are deposited on the cathode surface resulting in electrodeposition or electroplating. The diffusion layer is of the order of a few micrometers to even as large as a few millimeters [4.5]. Figure 4.12 schematically shows the double layer, diffusion layer and bulk region inside the electrolyte. It needs a high current density value, to reach the diffusion controlled regime for the case of plating on flat samples and the corresponding diffusion layer thickness is relatively small. For the entire current density range of in Figs. 4.2 and 4.3, the diffusion controlled regime has not been reached, and both the main and the side reactions if present, are still in the kinetically controlled regime. In contrast, for the case of plating into high-aspect-ratio recesses, due to the resistance to transportation of reactive species to the cathode surface, it becomes relatively easy to enter the diffusion controlled regime at a relatively lower current density values, and the corresponding diffusion layer thickness is approximately the depth of the microrecesses. From this point onward, as applied current from the power supply increases, the current efficiency for the main reaction will decrease and the side reactions at the cathode surface will start to increasingly come into picture.

For the case of a thick photoresist mold with high-aspect-ratio microrecesses, as is the case in this work, the thickness of the photoresist layer is essentially the thickness of the diffusion layer [4.2]. Figure 4.13 a) shows the schematic of the electroplating cell utilized in this work. A thick photoresist layer with a number of recessed holes is located on the substrate. The substrate is covered with a conductive seed layer to serve as cathode. The cathode, anode,

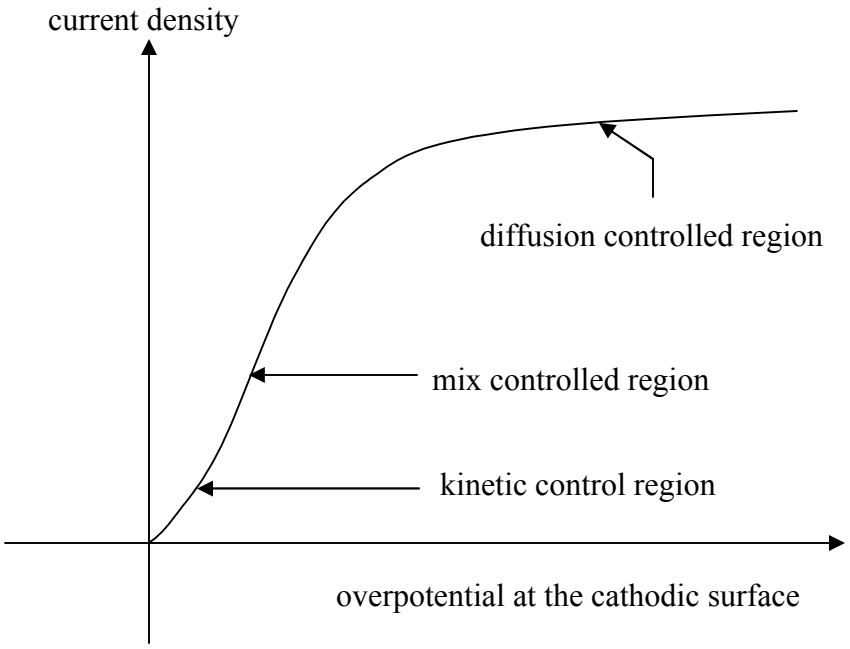


Figure 4.11: A schematic showing different current control regimes with increase of electrode overpotential.

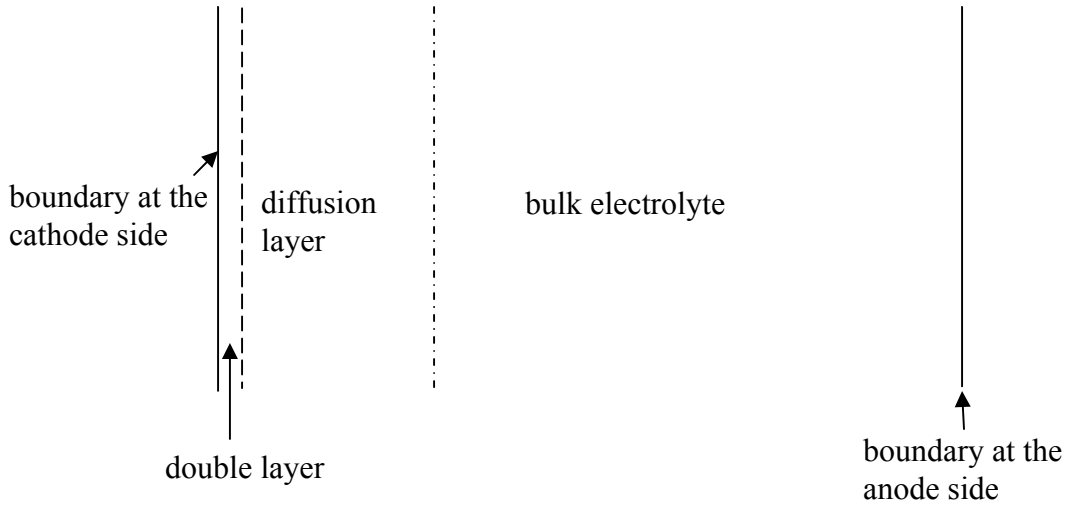


Figure 4.12: A schematic showing different layers existing in the electrolyte.

electrolyte, external electrical connections and power supply form a complete electroplating circuitry. The microrecesses have high-aspect-ratios thus the thickness, δ of photoresist is essentially the thickness of the diffusion layer. Figure 4.13 b) shows the details of a high-aspect-ratio microrecess. Mechanical stirrer makes the bulk solution more uniform but it has little effect on the concentration profile inside the microrecesses. The concentration of reactive species is the maximum towards the entrance of the recess, which is approximately the bulk concentration if sufficient stirring is provided. The concentration decreases and is at its minimum at the bottom of the recess. This concentration gradient will result in a finite value for the limiting current density. Maximum current density, j_{lim} occurs when the concentration at the cathode surface becomes zero. Increase in current density beyond j_{lim} does not increase the electrodeposition rate but contributes to side reactions. Unwanted side reactions result in undesired products and local pH value change. Quality of the deposit may suffer should side reactions occur.

4.3.1 Observations as Diffusion Effect Takes Control

As shown in Fig. 4.11, diffusion effect takes control when cathodic surface overpotential is high. The microrecess having the smallest area will have a greater diffusion resistance since the depths of all recesses are the same. As derived in Appendix A, the diffusion resistance R_d caused by diffusive mass transport is expressed as $R_d = \frac{1}{A}\frac{RT\delta}{(nF)^2 DC_b}\ln(1+\frac{j\delta}{nFDC_b})$, where R is the universal gas constant (8.31 J/mol·K), T is the absolute temperature, δ is the depth of recess, j is cathodic current density, D is the diffusion coefficient, C_b is bulk electrolyte concentration of Ni^{2+} ions, n = 2 is the number of charges carried by each Ni^{2+} ion, and A is the cross-sectional area of the microrecess or cathode surface. As expected, the value of R_d is inversely proportional to the cross-sectional area A of the microrecess. Figure 4.14 shows the profile of microprobes plated with j = 50 mA/cm^2 for the case of δ = 100 μm. At this current density, the heights of

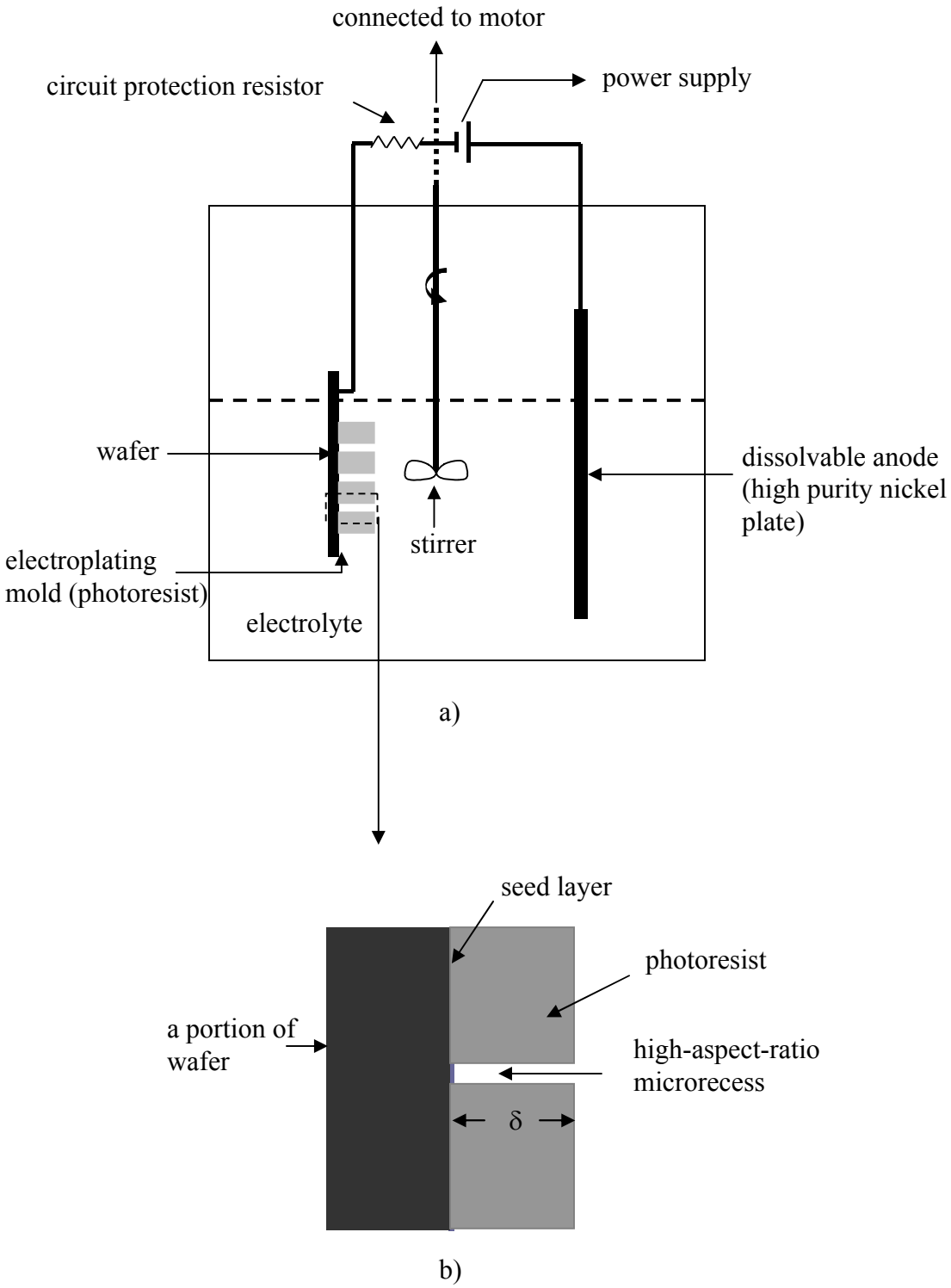


Figure 4.13: a) An electroplating cell showing the components in the cell. b) Details of a high-aspect-ratio microrecess.

plated microprobes are not uniform and the trend is reverse of what is shown Fig. 4.7 for j = 10 mA/cm^2. The probe with smallest dimension is plated at the slowest rate as shown in Fig. 4.14. The nominal probe widths shown in Fig. 4.14 are 70 μm, 60 μm, 50 μm and 40 μm from left to right, respectively.

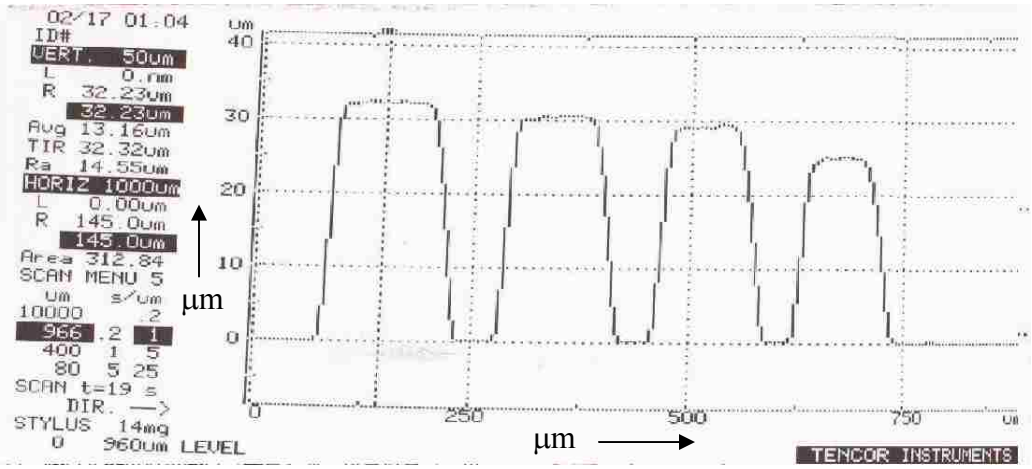


Figure 4.14: Electrodeposited nickel profiles as a function of microstructure recess widths. Thinner probes are electroplated at a lower rate during DC plating under diffusion controlled regime. Current density is 50 mA/cm^2.

As current density is increased, the surface overpotential increases as well, and the electroplating enters a diffusion controlled regime. For current density of 100 mA/cm^2 in this work, the electroplating through microrecesses becomes very poor. Plating rate becomes low and is difficult to control. Also, crystallized green color precipitates are observed around the mouth of the microrecesses. This phenomenon becomes more serious around microrecesses with smaller dimensions. Side reactions at the cathode surface are attributed to causing these observed precipitates. A brief explanation is that as the current density increases, the reactive species become depleted at the base of the electroplating mold and reaches limiting current density dictated by mold geometry. In order to maintain higher current density forced by the

overpotential, a portion of current now contributes to side reactions such as evolution of hydrogen gas at the surface of the cathode. This is schematically shown in Fig. 4.15. Consuming hydrogen ions elevates the local pH value which in turn decreases the saturation concentration of the nickel sulfamate salt in water. This eventually results in the observed precipitation of undesired crystal salt deposits.

4.3.2 Computation of Diffusion Coefficient of Ni Ions

Computation of diffusion coefficient D of nickel ions in nickel sulfamate electrolyte is achieved by utilizing the limiting current relationship and by making use of observations in section 4.3.1. The limiting current during DC plating is expressed as $j_{\lim} = -\frac{nFDC_b}{\delta}$ [4.5]. For $Ni^{2+} + 2e^- \rightarrow$ Ni reaction employed in this work, T = 53 °C, n = 2, C_b = 1.52 M, and δ = 100 μm, which is the depth of the probe mold, F = 96485 C/mole is Faraday's constant. Since the limiting current from experiment is ~ 100 mA/cm^2, the effective value of D turns out to be 3.3 × 10^{-6} cm^2/s. The reported nickel ion diffusion coefficient in an infinitely diluted solution is 6.7 × 10^{-6} cm^2/s for T = 25 °C [4.8]. Thus it is seen that in a concentrated electrolyte (C_b = 1.52 M) and at a higher temperature, the effective diffusion coefficient is reduced by about 50% of its nominal value under complete ionization. A reduction in ionic dissociation at the higher concentration used here may also contribute to the lower effective value of D obtained here. However, it is not obvious which of the above two physical mechanisms dominates. For modeling work in section 4.6, these two effects are combined to give a net effective value for diffusion coefficient D under the assumption of complete ionization.

4.4 Pulse Plating

Compared to DC plating in which a continuous and nearly constant current in maintained, pulse plating technique involves current on and off times, as schematically shown in Fig. 4.16.

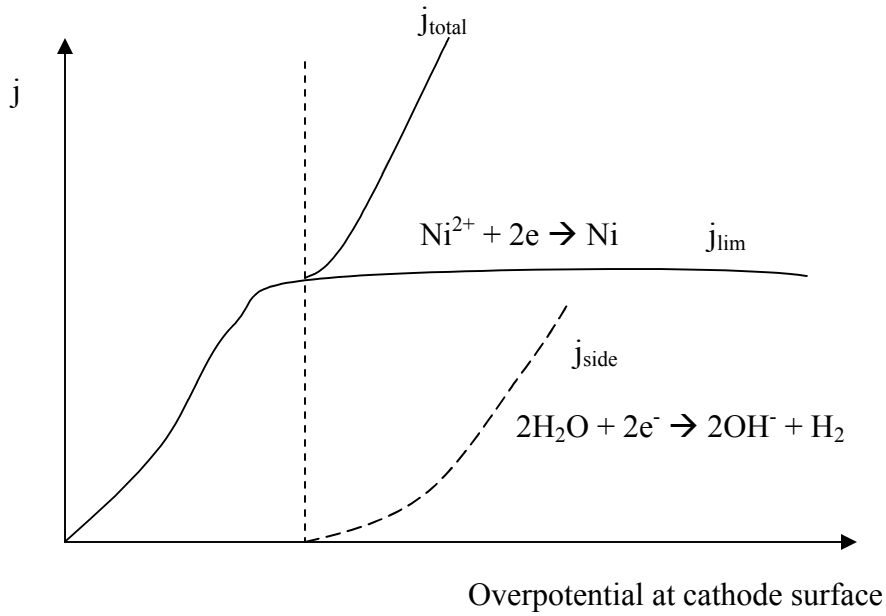


Figure 4.15: Current density as a function of overpotential, indicating the contribution of side reaction to total current density j_{total} at high electrode overpotential.

A cathodic current is supplied during the on time, t_{on}, while no current or a minimal or even a negative or anodic current is supplied during the off time, t_{off}. Pulse plating can improve diffusive mass transport of the reactant species from the electroplating solution bulk to the surface of the working electrode during the pulse off time. The pulse deposition mechanism can also significantly suppress side reactions such as hydrogen gas evolution at the working electrode and hence can improve the quality of the deposit [4.1]. Pulse plating has other advantages over DC plating such as enhancement of electrodeposition nucleation rate due to a higher magnitude of instantaneous current density during the on time. Pulse plating can offer greater flexibility in controlling process parameters compared to the DC plating case. Pulse plating is known to yield higher quality deposits in terms of lower tensile internal stress, greater corrosion resistance, more compact structure, lower porosity, and better adherence to substrate [4.1].

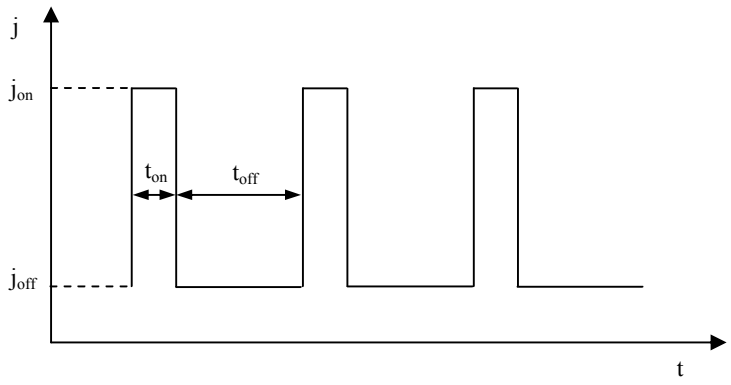


Figure 4.16: The on and off time periods, t_{on} and t_{off}, during pulse plating. The plating current density is denoted by j and t is time.

4.4.1 Relationships between Charge Time, Discharge Time and Transition Time

As is shown in Fig. 4.12, there is a nanometer size double layer near the surface of the cathode. No free charges exist in this zone. Electrons are rapidly swept to cations and the latter become neutralized so that deposition takes place on the cathode. This double layer zone is thus virtually a capacitor, represented by C_{dl}. Figure 4.17 shows a simple equivalent circuitry for pulse plating into deep microrecesses, where R_p is the polar resistance that is reflected by the slope of polarization curve. R_e and R_d respectively stand for resistance values inside a microrecess resulting from the electrolyte conductivity in the recess and the effective resistance caused by diffusion. R_b denotes resistance of the bulk electrolyte. In a normal pulse plating setup on flat samples, the pulsing frequency could reach mega hertz and pulsing current density could be tens of amps per square centimeter [4.1]. In a pulse plating setup for high-aspect-ratio microrecesses, however, the pulsing frequency is much lower due to mass transportation limitation inherent in microrecesses. In both cases, it is important to pay attention to charging and discharging processes of the double layer capacitor.

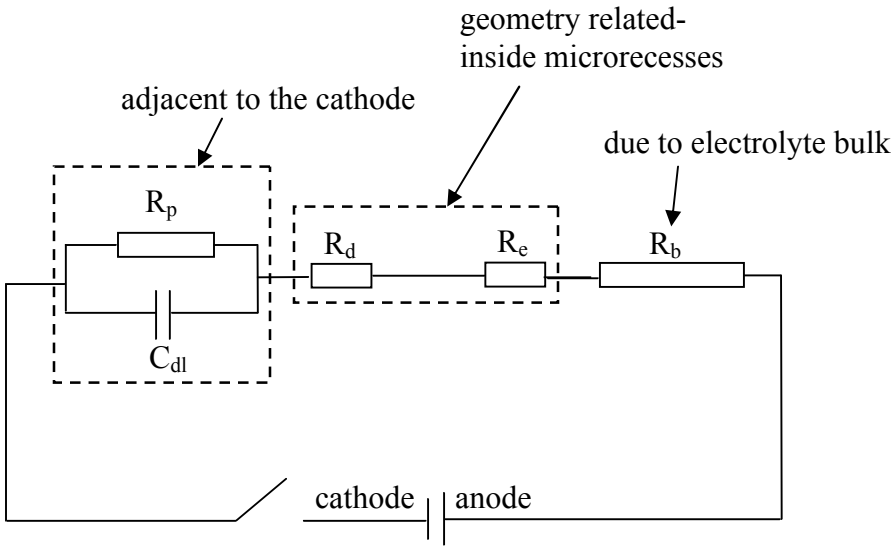


Figure 4.17: A simple equivalent circuit representing pulse plating inside a microrecess.

The double layer capacitor is charged during the on time and discharged during the off time. Therefore the on time and the off time need to be tailored with respect to double layer charge time (t_c) and discharge time (t_d) to retain the advantages of pulse plating. On time needs to be compared with transition time as well. Transition time, τ is defined as the time needed for the cathodic current density to reach the steady state. The Nernst diffusion layer equation is defined as $j = -nFD\frac{dC}{dx}$ at x = 0, i.e. at the cathode surface. Assuming a constant current density whose value exceeds the limiting current density, according to $j = -nFD\frac{dC}{dx}$, a constant concentration gradient is imposed at the cathode and the surface concentration of the reacting species decreases with time until it reaches zero at $t = \tau$ when the gradient becomes $\frac{C_b}{\delta}$. Transition time τ depends on D, δ, i_{lim} and j. For the case of δ greater than 100 μm, typical value of τ is estimated to be in the range of a few seconds to 100 seconds as inferred by the equations and figures given in reference [4.1]. Depending on the relative values of t_{on}, t_c and τ, and that of

t_{off} in comparison to t_d, pulse electroplating can be broadly divided into three cases as shown in Fig. 4.18. The setup current is defined as the galvanostatic current output from power supply.

First, when $t_{on} << t_c << \tau$ and $t_{off} << t_d$, the average current density will tend to approach the value corresponding to DC plating case due to insufficient charging and discharging of C_{dl}, where the DC case stands for the average current density which is denoted by $j_m = j_{on}t_{on}/(t_{on} + t_{off})$ and j_{on} stands for setup current output from the power supply during the on time. In this case, good characteristics inherent by the pulse plating technique are lost and the plating current density is lower than the current setup output value from the power supply and hence the corresponding electroplating rate is lower. Figure 4.18 a) shows this situation.

Second, when $t_c << t_{on} << \tau$, and $t_{off} >> t_d$, the deposit characteristics will benefit from pulse plating, as indicated in Fig. 4.18 b).

Third, when $t_{on} > \tau$, the diffusion control takes effect and plating current density will reach the limiting current density causing side reactions. Quality of deposit will now suffer. This is shown in Fig. 4.18 c).

4.4.2 Choice of On Time and Off Time

From reference [4.9], when plating current density j_{on} is far greater than the exchange current density j_0, i.e. $j_{on} >> j_0$, charge time t_c can be expressed by $t_c = \frac{C_{dl}}{j_p a}$, where $a = \frac{\alpha n F}{RT}$ and C_{dl} is the capacitance of the double layer. Here α is the symmetry factor. Here j_0 is the equilibrium current density for cathodic reaction which in our case is $Ni^{2+} + 2e \Leftrightarrow Ni$. At equilibrium, the cathodic or reduction current j_0 equals to anodic or oxidation current and this result in no net current and no net deposition. For our case T = 326 K, R = 8.314 V·C/(mol·K), and α, the symmetry factor is usually taken as 0.5, which gives a = 35.6/V. Pulse current density,

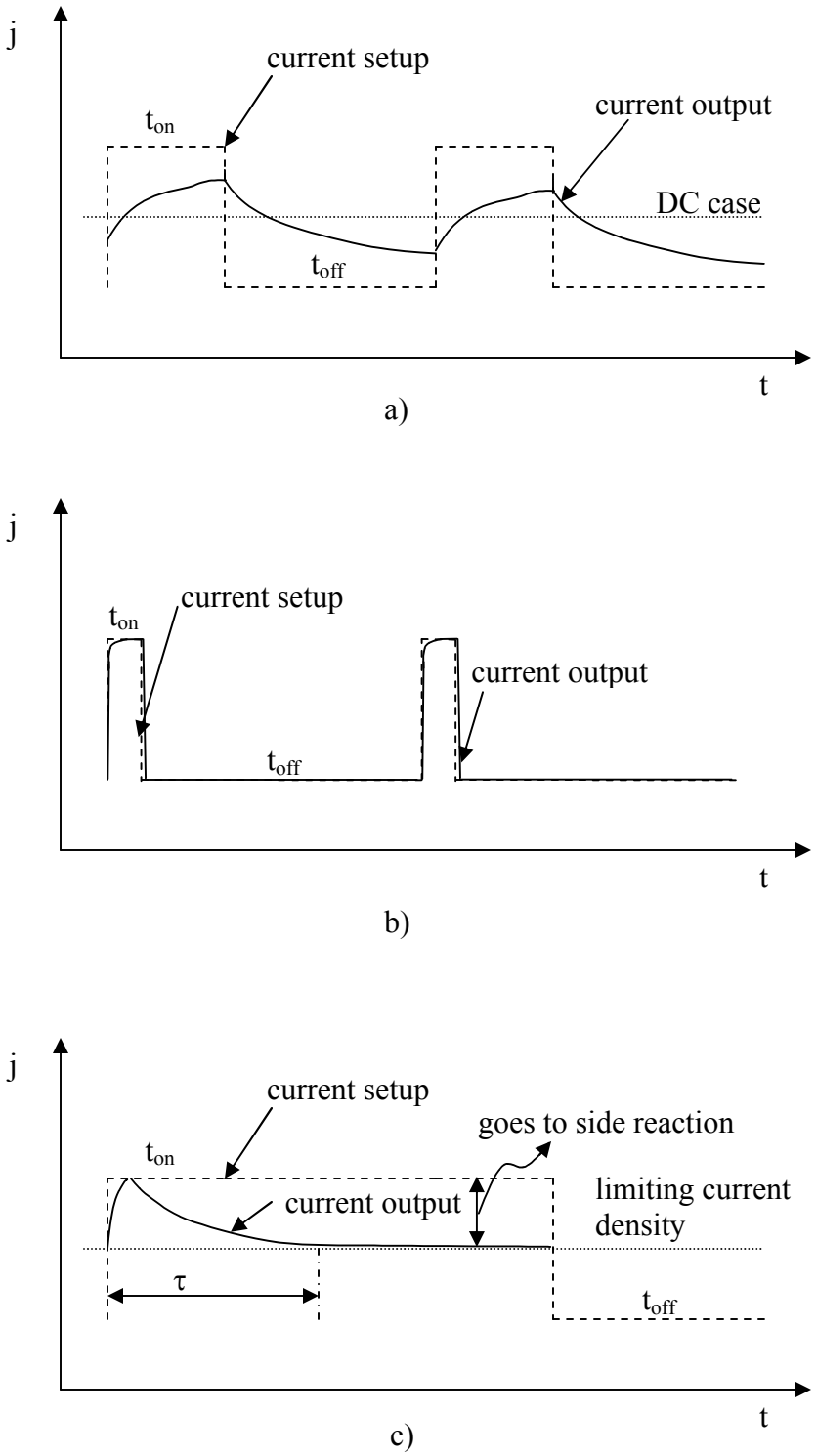


Figure 4.18: Three cases of pulse plating showing the setup of plating current and the actual plating current. a) $t_{on} << t_c << \tau$ and $t_{off} << t_d$; b) $t_c << t_{on} << \tau$, and $t_{off} >> t_d$; c) $t_{on} > \tau$. j denotes plating current density and t is time.

j_{on} has been set at 100 mA/cm^2 through out this work. Double layer capacitance, C_{dl}, for nickel plating case, is given in literature to be approximately 80 μF/cm^2 in an acidic solution which is similar to our case [4.10]. These values yield t_c to be approximately 25 μs. Discharging time, t_d, is usually 6 times as large as t_c [4.1]. As illustrated in the following experiment, on and off time periods have been chosen in the range of seconds to ensure $t_c << t_{on}$ and $t_{off} >> t_d$. Transition time τ is estimated to be approximately 100 seconds for a 250 μm deep recess used in this experiment [4.1]. t_{on} is maintained well below 100 seconds so to satisfy the conditions in Fig. 4.18 b).

Two approaches in terms of varying the on time and the off time are attempted here by 1) keeping t_{on} fixed while varying t_{off}, and by 2) fixing t_{off} and varying t_{on}. The on time current density remains approximately at 100 mA/cm^2 and the off time current density is kept at zero. First, t_{on} is set at 10 s and the t_{off} is varied from 5 s to 25 s in increment of 5 s steps. $t_{on\text{-}total}$ is the total on time through out an electroplating event and is kept the same at 20 min for each combination of t_{on} and t_{off}. The resulting average probe height is found to be approximately 30 μm. Second, t_{off} is set at 10 s and t_{on} is varied from 5 s to 25 s, also in increment of 5 s steps . Again, $t_{on\text{-}total}$ is kept fixed for each combination of t_{on} and t_{off} at 20 min. The resulting probe height on average is also found to be approximately 30 μm for this second set of experiments as well. Therefore, as long as the current density and total on time are kept the same, the plating rate during on time is found to be constant at approximately 90 μm/hr. A 200 μm tall microprobe array obtained by pulse plating is shown in Fig. 4.19. This experiment shows that a well chosen set of on and off time periods in comparison to charging, discharging and transition time periods can satisfy the conditions in Fig. 4.18 b) which is desired for pulse plating and lead to a good quality deposit.

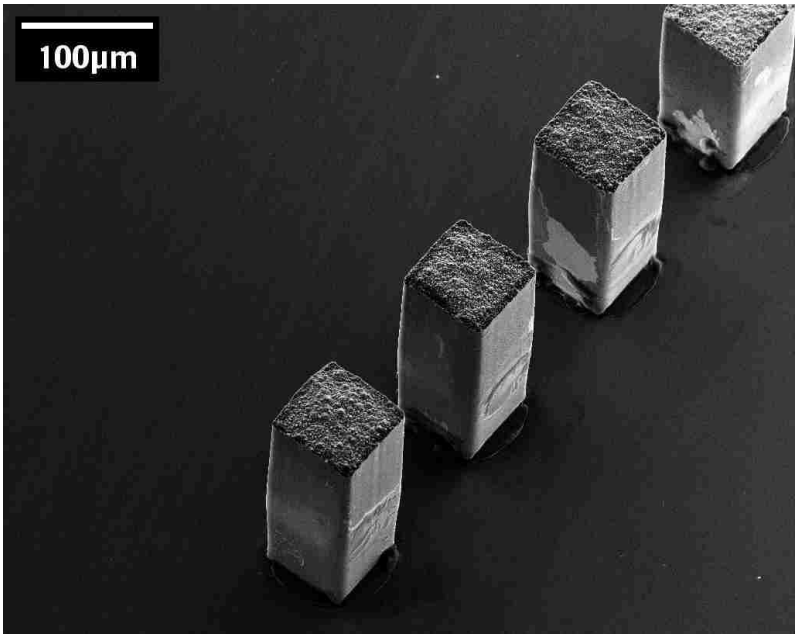


Figure 4.19: A 200 µm tall microprobe array obtained by pulse plating.

4.5 Stress Analysis

Stress is a major concern in electrodeposited materials and microstructures because it may directly lead to microstructure failure due to cracking, detachment from the substrate or corrosion [4.11]. Electrodeposited nickel usually has considerable amount of built-in stress which may compromise the electro-mechanical performance of a microstructure especially for the one having a high-aspect-ratio. This work investigates built-in stress levels in electrodeposited nickel for both DC and pulse electroplating cases and compares the results obtained from these two techniques. Various deposition parameters such as current density, current on time, t_{on}, and current off time, t_{off}, are varied during pulse electrodeposition. Surface grain morphology with changing electrodeposition parameters is also investigated and related to the observed stress levels. Additionally, for the pulse plating case, both long duration periods for t_{on} and t_{off} in the scale of seconds and short duration periods in the scale of milliseconds are examined. For the long duration period experiment, t_{off} is varied while t_{on} is kept fixed. For the

short duration periods case, t_{on} is varied and t_{off} is kept fixed. Stress changes in the electrodeposited nickel are also measured as a function of plating time. One goal is to arrive at electroplating parameters that can lead to a control of the built-in stress in the deposited layer and thereby improve performance of the fabricated microstructures. Another goal is to obtain a better understanding of the nickel electrodeposition process.

Built-in stress is characterized here by a shift in lattice spacing or strain in the deposited nickel (Appendix B). Stress S is expressed as $S = E\ (a-a_0)/a_0$ where a is the lattice constant of deposited metal, a_0 is the lattice constant in a stress-free material and E is the Young's modulus. For nickel, a_0 from literature is 0.352 nm. The reported values for Young's modulus of electroplated nickel are found to be 163 GPa by Cho [4.12] and 205 GPa for plating temperature less than 60 °C by Luo [4.13]. The latter value is close to the bulk nickel, 210 GPa [4.13] but it drastically drops to approximately 100 GPa for samples electroplated at 80 °C. Also, it is reported by Luo [4.13] that the Young's modulus decreases to 85 GPa as the plating current density is increased from 2 mA/cm^2 to 30 mA/cm^2. This result implies that at low current density since the plating rate is low, there is sufficient time for the as-plated nickel atoms to rearrange to form a denser coating that results in a higher E. This result does not agree with the result given by Cho [4.12] where E is shown to stay at 163 GPa at a current density of up to 20 mA/cm^2. Since the plating conditions including solution recipe, pH value, bath temperature used by Cho at CAMD are very similar to our experimental setup, their result of E = 163 GPa is used for both DC and pulse plating for our case.

X-Ray diffraction analysis is employed to evaluate the lattice constant *a* and hence the built-in stress *S*. The X-Ray diffraction analysis is performed on a Rigaku MiniFlex X-Ray Diffractometer.

Both DC and pulse plating are carried out in a nickel sulfamate electrolyte solution at a constant bath temperature of 53 °C with pH maintained at or near 3.6. The substrate is covered with a conductive layer comprising of 50 nm of sputtered Ti as adhesion layer on the flat silicon substrate surface and 480 nm of sputtered Cu layer as the electroplating seed layer. This Ti/Cu combination layer serves as the cathode during electroplating. The electroplating circuit loop comprises of the cathode, the electrolyte, the anode, external wires and the power supply. The electroplating cell which is designed and built in our laboratory is shown in Fig. 4.1. A cathode and an anode are placed parallel to each other and a propeller stirrer is located equidistance between the two electrodes. The power supply is a potentiostat model 2049 from Amel Instruments, which is employed for both DC and pulse electroplating in this work.

4.5.1 DC Plating Case

Electrodeposited nickel samples are prepared by DC plating utilizing different current densities. In order to avoid interference from unwanted characteristic peaks resulting from the 50 nm Ti and 480 nm Cu layers and the silicon substrate, the thickness of the nickel deposition is kept around 30 μm. The value is sufficiently thick to avoid interference from the underlying layers. Corresponding strain and built-in stress values obtained as a function of DC electroplating current density are shown in Fig. 4. 20.

As can be seen from Fig. 4.20 for the DC case, nickel deposits are under negative or compressive stress at lower deposition current densities. As the DC current density increases, stress changes from compressive to tensile or positive. No noticeable change in the positive stress magnitude of approximately 92 MPa is observed for current densities above 30 mA/cm^2. It thus implies that a current density somewhere between 20 and 30 mA/cm^2 will result in a near stress-free nickel deposit for DC plating. This value from Fig. 4.20 obtained by linear interpolation is approximately 26 mA/cm^2. As a comparison, El-Sherik has found that stress in

nanocrystalline Ni electrodeposits always consistently appears compressive on a variety of substrates [4.14]. Our findings agrees with Hearne's work, in which a nickel sulfamate electroplating bath was used and stress transits gradually from compressive (-650 MPa) to tensile (400 MPa) as growth rate increases [4.15]. It is also well established that tensile stresses in electrodeposits are deleterious, with the higher stress resulting in a lower fatigue strength of the electrodeposit [4.16]. Our observed data and the data in related literature demonstrates that the sign and magnitude of stress in the electrodeposited nickel films strongly depends on the deposition rate. The most likely mechanism for generating tensile stress at higher deposition rates is the formation of nanoscale surface roughness given in reference [4.15]. The increase in surface roughness could lead to a process where neighboring grains continually coalesce together during deposition leading to a continual 'zipping' process, as has been observed during amorphous film growth [4.15]. The 'zipping' effect results in a tension between neighboring grains which in turn induce tensile stress.

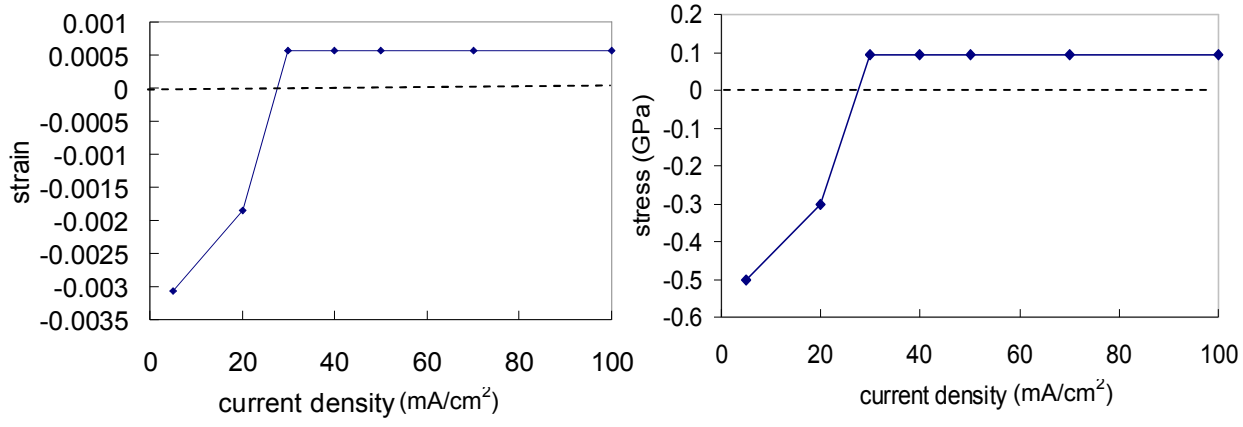


Figure 4.20: a) Measured strain and b) calculated stress variation for E = 163 GPa in electrodeposited nickel as a function of DC electroplating current density. The deposited film thickness is maintained approximately at 30 μm.

Strain and stress level are also characterized as a function of film thickness as shown in Fig. 4.21. The electroplating bath temperature is maintained at 53 °C and the DC current density is maintained at 100 mA/cm^2. As can be seen from this figure, the deposited nickel film is under compressive or negative stress when it is thin (< 8 μm) and transforms rapidly to a tensile or positive built-in tensile stress for thickness values beyond 10 μm. In order to avoid X-Ray peak interference from the underlying layers for thin layers, distinct diffraction peak from {400} lattice planes is chosen here. The tensile stress reaches a value of about 73 MPa for 10 μm thickness and then remains constant with further increase in film thickness. From Fig. 4.21, the stress-free film growth occurs for a thickness of approximately 8.2 μm under plating current density of 100 mA/cm^2 by using linear interpolation. There is an approximately 20% difference between the saturation built-in tensile stress values given in Fig. 4.20 and Fig. 21 for the 30 μm film thickness. We are not able to currently resolve this discrepancy and temporarily attribute it to some unknown artifact associated with the electrolytic deposition process. It could also be a result of inaccuracy of locating the diffraction peak. Another possible reason of this discrepancy may be due to the bath aging effect as there was a long period of time span between these two sets of experiments. As electrolyte ages, the pH buffer, i.e. boric acid level decreases. Abyaneh et al. has reported that the existence of boric acid accelerates nickel deposition rate [4.17]. The deposition rate is found to be linearly proportional to current density as indicated earlier in Fig. 4.3.

A higher deposition rate provides less time for lattice and grain boundaries to rearrange so that a more tensile stress may result. As electroplating bath ages, the concentration of the additives including boric acid decreases which may result in a slower nickel deposition rate as may contribute to the reduction of the magnitude of the tensile stress level in Fig. 4.21 compared

to Fig. 4.20. Reference [4.17] also indicates partial consumption of boric acid decelerates deposition rate which may result in a less tensile stress. In order to suppress the evolution of hydrogen gas, a certain level of boric acid inside the electroplating bath need to be maintained [4.18] as hydrogen evolution results in a poor quality deposit. Hearne et al. investigated stress level as a function of nickel deposit thickness and had made a similar observation [4.15] that the instantaneous stress became more tensile with the increase of film thickness and the stress level remained constant with thicknesses in excess of 50 μm.

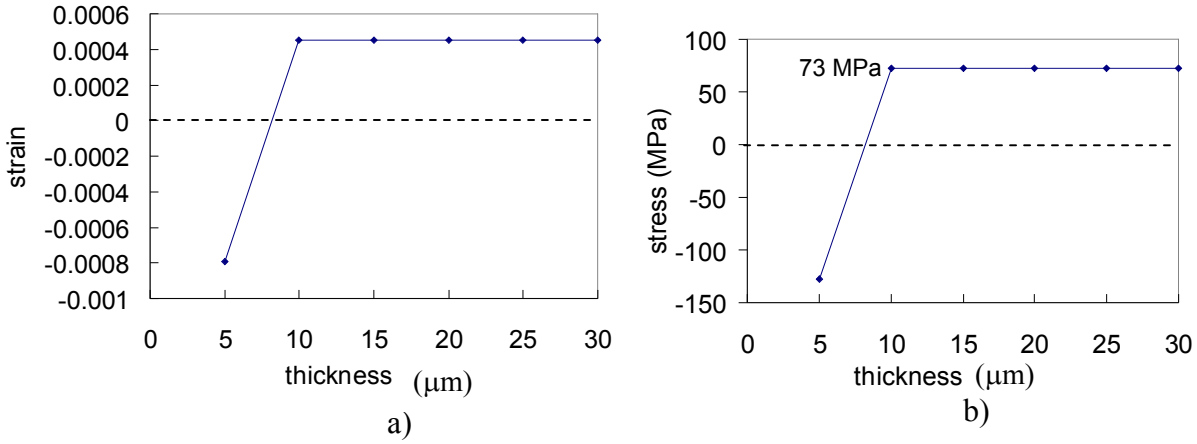


Figure 4.21: a) Measured strain and b) calculated stress variation for E = 163 GPa in electroplated nickel as a function of film thickness. The electroplating DC current density is 100 mA/cm^2.

4.5.2 Pulse Plating Case

Flat silicon wafer substrates with the same combination of adhesion and seed layers are utilized for stress analysis for the pulse plating case as well. Pulse electroplating utilizes a three electrode setup with a saturated calomel electrode being the reference electrode. Potentiostatic pulses are generated from power supply. The on and off time periods, t_{on} and t_{off}, for pulse electroplating shown in Fig. 4.16 are varied. By regularly monitoring the magnitude of overpotential, current density value for j_{on} is maintained at approximately 100 mA/cm^2 during

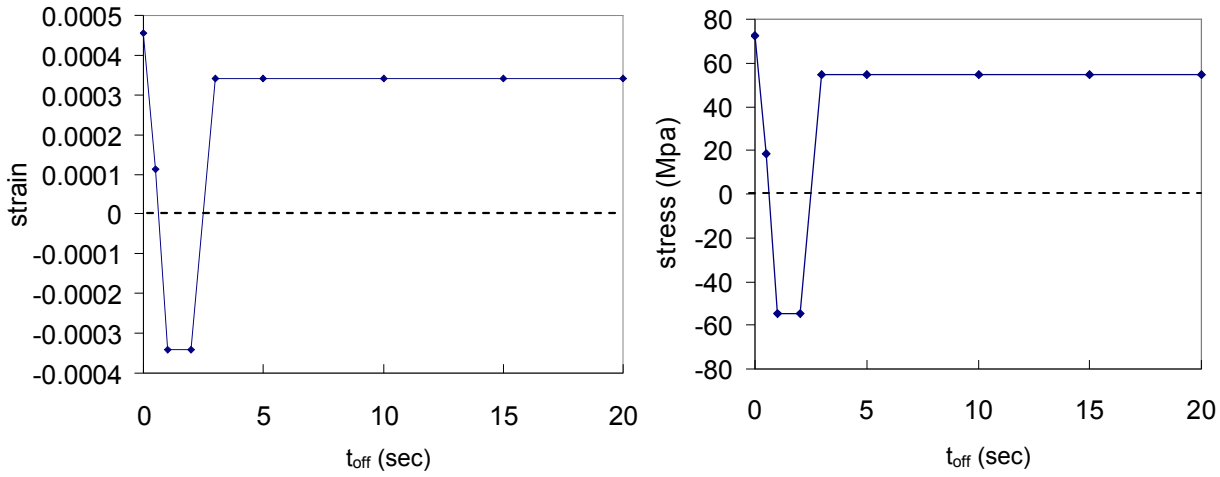
the on time periods in this work similar to the peak current value for the DC case in Figs. 4.20 and 4.21. The substrate samples were also similar to the DC plating cases discussed in section 4.5.1. First, the built-in stress in the deposited nickel is investigated by varying t_{off} from 0 s to 20 s while keeping t_{on} constant at 10 s. The other parameters such as temperature and pH value of the bath are kept the same as for the DC plating case. The thickness of the deposit is also kept at 30 μm as for the DC plating case in Fig. 4.19. The measured built-in stress values with respect to t_{off} are shown in Fig. 4.22.

As can be seen from Fig. 4.22, the duration t_{off} equal to zero situation is analogous to the DC plating case shown in Fig. 4.21. As expected, the magnitude of built-in stress is approximately the same for the two cases. As t_{off} increases from 0 s to 3 s, stress changes from tensile or positive to compressive or negative rather rapidly and then equally rapidly sweeps back to being tensile but at a slightly lower value compared to the DC case. A possible explanation is given below for the above observation on stress variation with respect to t_{off}. When t_{off} is short, a relatively large pulse current is supplied to the cathode surface each time a pulse starts. And the nucleation rate is high at that occasion. When t_{off} is short, it does not provide sufficient time for the deposit to relax. Therefore, the lattice constant remains small, resulting in a compressive stress. For the cases of longer t_{off}, the lattice is allowed to expand and resulting in a less compressive or more tensile stress. For DC plating case, there is no intermittent large nucleation rate at the start of each on pulse. Therefore, no stress swing is observed in DC case.

Nickel deposits are under a constant tensile stress for $t_{off} \geq 3$ s. Comparing data from Fig. 4.21 or DC plating under 100 mA/cm^2 to pulse plating results of Fig. 4.22, it is apparent that except for a small range of values in t_{off} times less than 2 s, both the DC and the pulse plating of nickel results in a built-in tensile stress. However, the pulse plating results in 54.5 MPa of built-in stress, which is about 25% lower than the value obtained for the DC case. As the aspect-ratio

of microstructure increases, built-in stress in the microstructure plays an important role. As a result, replacing DC plating with pulse plating may offer advantages in certain applications.

Typical double layer charging and discharging times during pulse plating are in the order of μs to ms on a flat substrate [4.2]. Hence, pulse electroplating with t_{on} and t_{off} in ms range is investigated as well. Values of t_{on} and t_{off} are determined based on discussion from sections 4.4.1 and 4.4.2. As calculated in section 4.4.2, charge time t_c is approximately 25 μs and discharge time t_d is approximately 150 μs for the case of nickel electroplating. It is shown in section 4.4.1 that the deposit characteristics can benefit from pulse plating only if $t_c << t_{on} << \tau$ and $t_{off} >> t_d$. The transition time τ is in the range of a few seconds to 100 s as indicated in section 4.4.1. Hence in this work, t_{off} is maintained at 4 ms satisfying 4 ms >> 150 μs, and t_{on} is varied from 1 to 100 ms satisfying 25 μs << t_{on} << 1 s .



a) b)

Figure 4.22: a) Measured strain and b) calculated stress variation for E = 163 GPa with respect to t_{off} while t_{on} remains constant at 10 s. The plating current density is 100 mA/cm^2 and the film thickness is kept constant at 30 μm for each case.

Figure 4.23 shows the built-in stress in pulse plated nickel as a function of on time period, t_{on}. As can be seen in this figure, for all time ranges involved, nickel deposits have a built-in compressive stress. A compressive stress implies a lattice constant that is smaller than under stress-free status. A possible explanation for this is that a shorter off time in ms range restrains surface redistribution process at atomic level and lattice relaxation which result in smaller grain size and higher compressive stress [4.1]. Compressive stress is a characteristic of high frequency pulse plating.

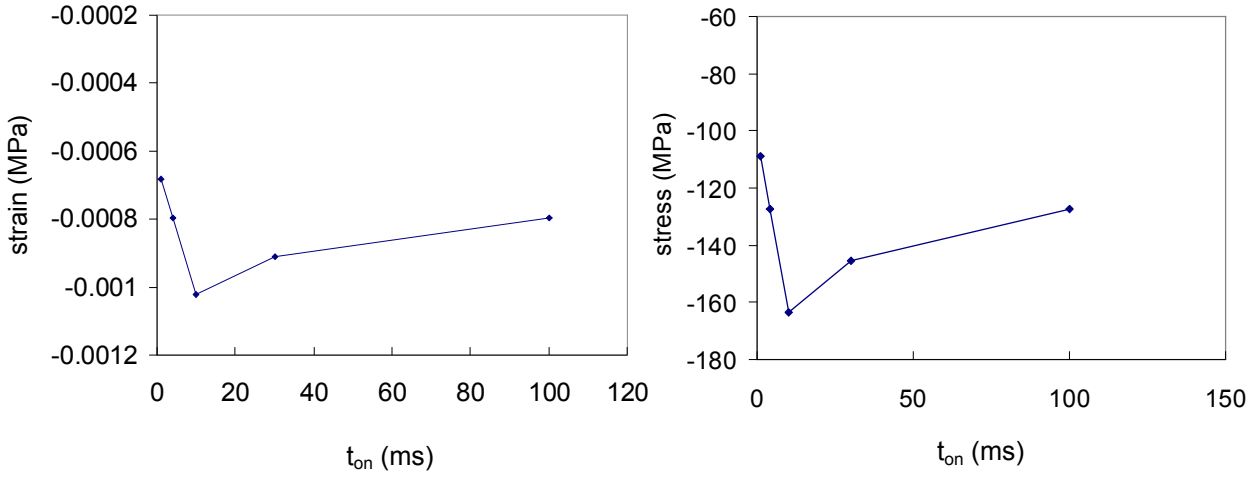


Figure 4.23: a) Measured strain and b) calculated stress variation for E = 163 GPa as a function of t_{on}. Here, t_{off} is constant with a value of 4 ms. Film thickness is kept constant at 30 μm for each case.

4.5.3 Grain Morphology

Grain morphology is investigated by SEM. Figures 4.24 a) – f) depict surface grain morphology of the electrodeposited nickel layers for the samples with t_{off} varying from 0 s (DC case) to 5 s while keeping t_{on} constant at 10 s corresponding to data given in Fig. 4.22. From Figs. 4.24 a) – d), it is noticed that the grain size is smallest for the DC case. The grain size increases as t_{off} value increases from 0 s to 2 s. The grain size then decreases for the 3 s and the 5 s cases but does not become as small as for the DC case. Comparing stress values indicated in Fig. 4.22

and the grain sizes from Figs. 4.24 a) – f), it is apparent that variation in the grain size reflects variation in the built-in stress in the nickel layers. For low frequency or long period pulse plating cases corresponding to Figs. 4.22 and 4.24, smaller grain size reflects relatively a larger tensile or a smaller compressive built-in stress while a larger grain size reflects relatively a smaller tensile or a larger compressive built-in stress.

SEM pictures of surface grain morphology on pulse electroplated nickel with short pulse durations in ms range are shown in Figs. 4.25 a) - c). Here, t_{on} is varied between 1 to 30 ms with t_{off} maintained constant at 4 ms as indicated in Fig. 4.23. From Fig. 4.23, the built-in stress values in these nickel layers are all compressive and large. From Figs. 4.24 and 4.25, it is seen that the short duration pulse electroplating results in grains with somewhat different microstructure. As can be noticed from Fig. 4.25 a) for the case of t_{on} = 1 ms, the facets of the nickel grains are less flat and are marked by choppy surfaces. As t_{on} increases, the facets of nickel grains get more flat and the choppiness in the facet features are reduced. This progress can be seen from Figs. 4.25 a) to c). A clearer comparison can be noticed in Fig. 4.26 a) and b), which respectively show Figs. 4.24 d) and 4.25 a) with a larger magnification. Notice that long duration pulse plated layer has smoother facets while the short duration pulse plated layer has rougher choppier facets. Figure 4.24 d) corresponds to the highest level of compressive stress in Fig. 4.22 while Fig. 4.25 a) corresponds to the least amount of compressive stress in Fig. 4.23 even though the latter is greater in magnitude than the former. The grain size in Fig. 4.26 a) appears larger than in Fig. 4.26 b) even though the latter has a larger magnitude of compressive stress. This observation is in contradiction to the long duration pulse plating case where smaller grain size reflected less compressive or higher tensile stress. It is speculated that for the high frequency (kHz) pulse plating case, the very short off time does not allow the surface atoms to rearrange to grow larger grains and retaining higher compressive stress [4.1].

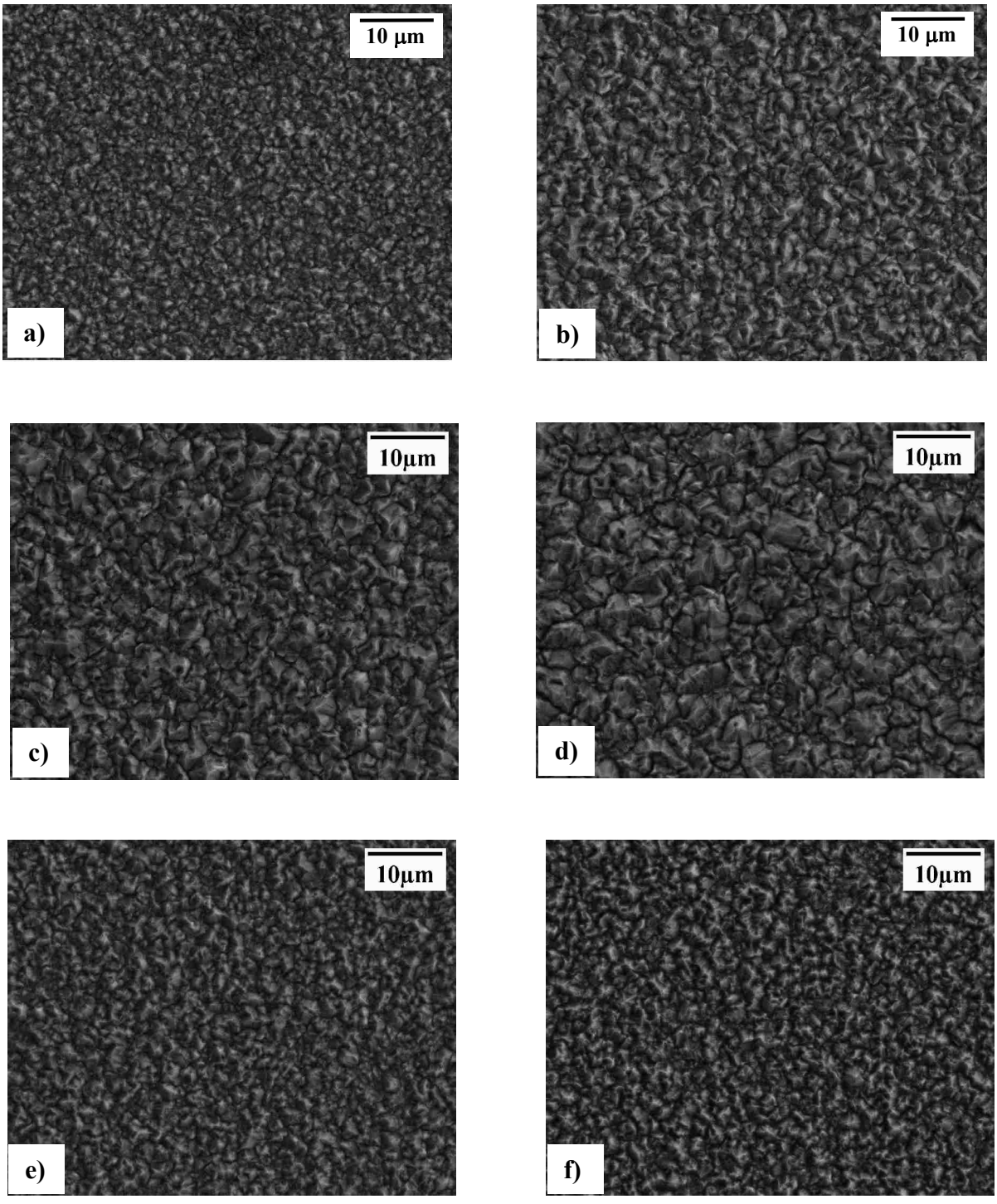


Figure 4.24: SEM pictures showing surface grain morphology in long period pulse electroplated nickel for t_{off} varying from 0 to 5 s with t_{on} kept constant at 10 s. a) $t_{off} = 0$ (DC case), b) $t_{off} = 0.5$ s, c) $t_{off} = 1$ s, d) $t_{off} = 2$ s, e) $t_{off} = 3$ s and f) $t_{off} = 5$ s.

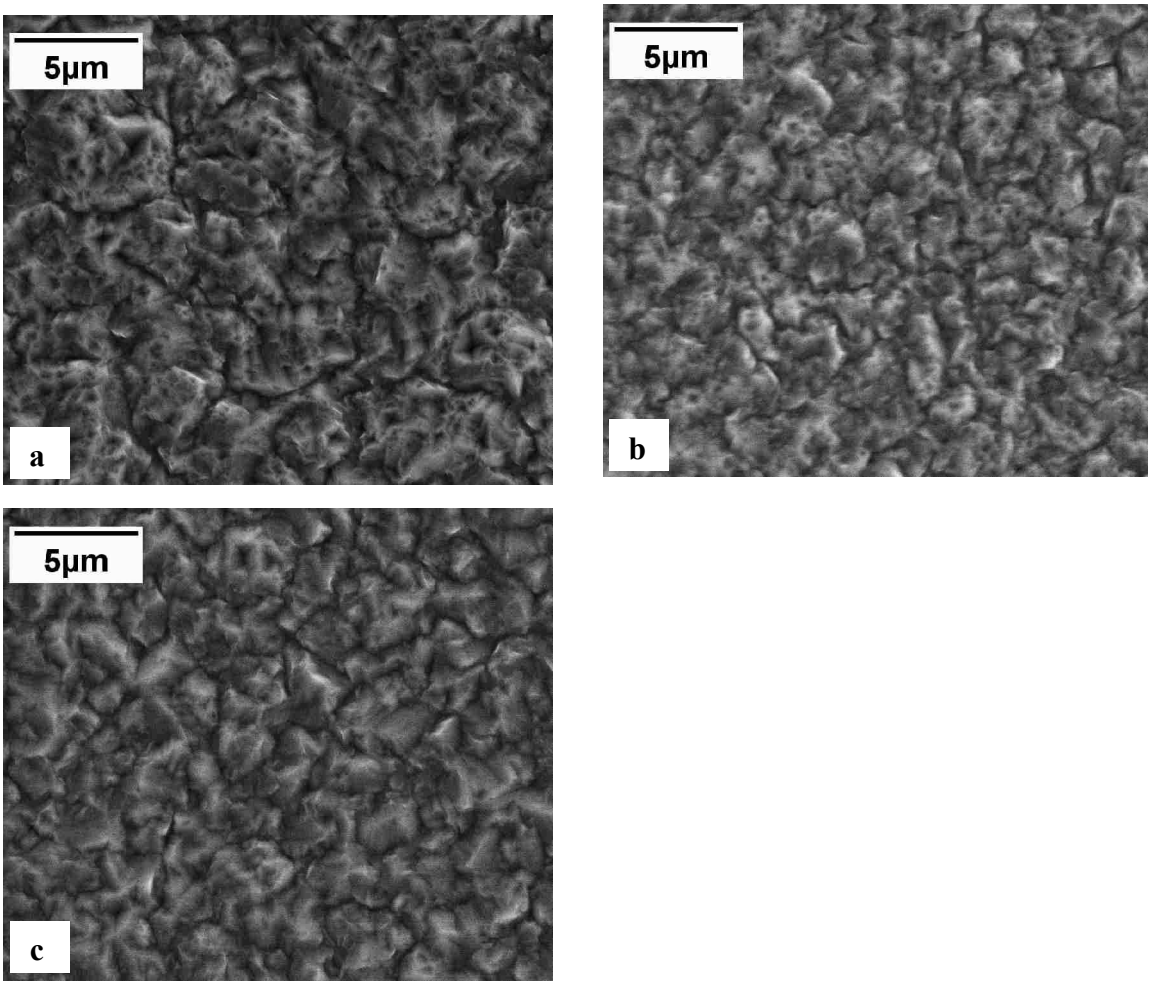


Figure 4.25: Surface grain morphology for pulse electroplated nickel with short duration pulses for different values of t_{on} with a constant value of t_{off} = 4 ms. a) t_{on} = 1 ms, b) t_{on} = 10 ms, and c) t_{on} = 30 ms.

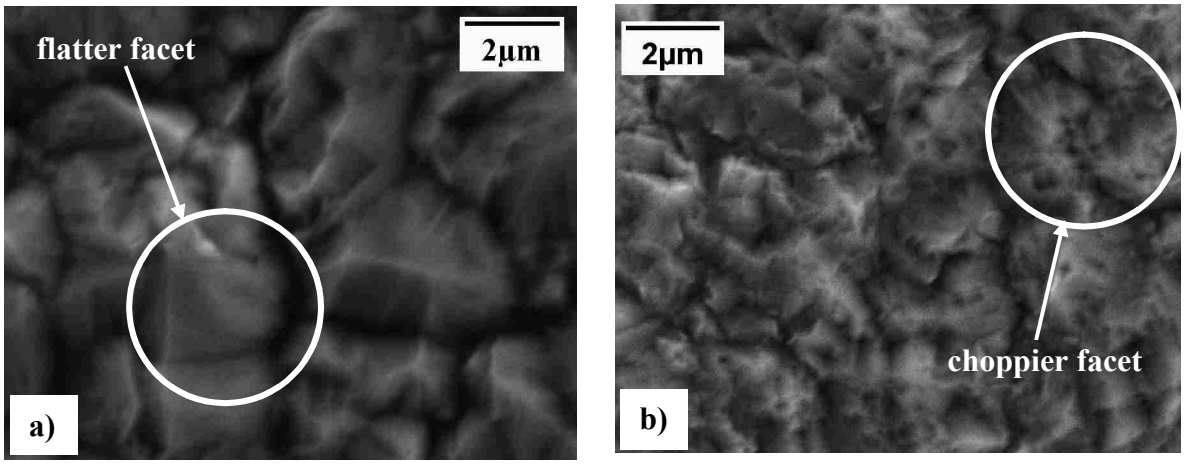


Figure 4.26: A detailed comparison on grain morphology between the long and the short duration pulse plating cases. a) Long duration case corresponding to Fig. 4.24 d), and b) short duration case corresponding to Fig. 4.25 a).

4.5.4 Summary on Stress Analysis

For the DC plating case, it is found that the internal stress in nickel deposit changes from compressive to tensile as cathodic current density is increased. The most likely mechanism for generating tensile stress at high deposition rate is the formation of nanoscale, high-aspect-ratio surface roughness, which in turn could lead to a 'zipping' process. During this 'zipping' process, neighboring grains continually coalesce together during deposition processes and resulting in stretch in the film. The value of stress saturates when the current density is over 30 mA/cm^2. For DC plating, the stress transition from compressive to tensile also occurs with increasing thickness of the nickel deposit and saturates for thicknesses over 10 μm. This is probably caused by lattice mismatch between the base layer and the nickel deposit. As nickel deposit becomes thicker, the interference from base layers disappears hence the stress saturates.

For pulse plating with long duration on-pulses of 10 s, it is found that the nickel deposits undergo transformation from tensile to compressive and back to tensile stress as pulse off time increases from 0.5 to 3 s as indicated in Fig. 4.22. A possible explanation when t_{off} is short is as follows. A relatively high rate of nucleation at the cathode surface at the beginning of each $t_{on.}$ Since t_{off} is short, the deposit does not have sufficient time to relax resulting in a smaller lattice constant and hence a compressive stress. For DC plating case, there is no intermittent large nucleation rate during plating. Also, for the cases of longer t_{off}, the lattice is allowed to expand and resulting in a less compressive or more tensile stress. The stress value saturates as pulse off time increases from 3 s to 20 s. A comparison between the saturated stress values given by DC and long on-pulse electroplating cases under otherwise similar conditions shows that the stress value of 54.5 MPa in the pulse plated deposits is about 25% lower than that of the value of 73 MPa observed in the DC plated deposits.

Pulse plating by short on-pulses in ms range were found to always yield compressive built-in stress between -100 MPa and -160 MPa. This is a characteristic of high frequency pulse plating. Compressive stress implies a lattice constant that is smaller than that under stress-free status. A possible explanation for this is that a very short off time in ms range restrains surface redistribution process at atomic level and also lattice relaxation which result in stresses that are more compressive.

Grain size and morphology variations are inspected by SEM. It is found that the grain size variation in long pulse plating coincides with the variation of stress status and magnitude with larger grain corresponding to more compressive or less tensile stress. For short pulse plating, a unique morphology with choppy faceted grains is observed which significantly differentiates it from the grain morphology produced by DC plating and by long period pulse plating.

4.6 A One-Dimensional Simplified Electroplating Model

Pulse plating takes advantage of the double layer capacitor which is charged during on time and discharged during off time. The discharge current however, is not wasted but partially contributes to electrodeposition during the off time. The discharge of the double layer capacitor results in a local consumption of the cations at the cathode surface that are left at the end of last on time period without requiring additional cations to be transported through the recessed column. This can be inferred by the extreme left loop shown in Fig. 4.17. Therefore, this part of current is not affected by the geometry of the microstructure recesses. This work targets electroplating high-aspect-ratio microstructures, which because of their geometry are usually operating in the diffusion-controlled regime. A model for pulse electroplating process is developed here. Since, the cathodic current is turned on and off in a periodic manner in pulse plating, a transient model needs to be developed.

Electrodeposition is a key process in fabrication of most high-aspect-ratio MEMS microstructures. This process involves multidimensional, transient phenomena that includes metal reduction reaction on a moving surface. It also involves transportation of charged and neutral species through diffusion, migration and convection in a centimeter-scale electrolyte environment and in micron-scaled microrecesses. This complicated process requires a computational model to help understand the deposition mechanisms and to control the process. Griffiths et al. [4.19] were among the first researchers to perform this type of modeling work. They developed one and two-dimensional numerical models for electrodeposition into high-aspect-ratio microrecesses. However, transient and moving boundary effects were not included in their study. Chen and Evans developed and demonstrated a multi-dimensional framework for modeling transient mass transportation caused by diffusion and migration in a dilute electrolyte on a moving surface [4.20]. Like other models, this work started from the basic governing equations that included mass conservation, charge conservation, potential distribution, momentum equation and Butler-Volmer kinetics. It used specially designed finite element software [4.21-23] to solve the multi-physics, multi-dimensional model. Numerical modeling work that contributes to electrodeposition into LIGA or UV-LIGA microstructures has been reported in literature [4.24]. Typical assumptions used in numerical simulations include neglecting migration and/or convective transport effects, simplification of geometry, assuming a constant electrolyte conductivity or a stationary boundary. Geogriadou et al. [4.25] developed a comprehensive model that considers complex geometry and shape evolution in a fully coupled system. This model also account for the effects of additive chemistry.

A simplified analytical one dimensional transient model has been built in this work. Compared to above numerical models, this model solves electrodeposition governing equations analytically. Diffusion controlled regime is assumed throughout the entire deposition process.

The main purpose of the model is to provide qualitative insights into the electrodeposition process inside the microresseses and to offer some guidance on the choice of experimental parameters such as on time duration.

4.6.1 A Fixed Boundary Approach

This model is built in an effort to depict the current density transient process during the course of on time period after a potential step is applied at the cathode surface for the case of pulse plating through a microrecess as shown in Fig. 4.27 to help decide the duration of the on time period. Electroplating into a deep microrecess is actually a moving boundary problem because the base of the microrecess elevates as it is electroplated. Initially this is treated as a fixed boundary problem because electroplating rate is usually kept low in order to retain reasonably good deposition quality. A more precise model that involves a moving boundary is considered in section 4.6.2.

An overpotential step of magnitude ($E_1 - E_0$), is applied to the cathode at the start of each on time, t_0, as indicated in Fig. 4.28. The sign of (E_1 - E_0) is negative for this case. E_0 is the reversible potential for the deposition reaction at the cathode surface determined by thermal dynamics and Nernst equation. E_0 is a function of temperature and the activities of the corresponding components inside the plating solution. At E_0, the current density is the same for both the oxidation process: $Ni \rightarrow Ni^{2+} + 2\ e^-$ and the reduction process: $Ni^{2+} + 2\ e^- \rightarrow Ni$, thus resulting in no nickel deposition. This individual current density component is called the exchange current density, j_0. When a more negative potential E_1 is applied on the cathode, the thermal dynamic equilibrium is broken and the magnitude of reduction current gets larger than the magnitude of oxidation current and nickel deposition takes place on the cathode surface.

Figure 4.29 schematically shows the development of concentration profile inside the microrecess which is shown in Fig. 4.27. Here, C denotes reactive species concentration, C_b and

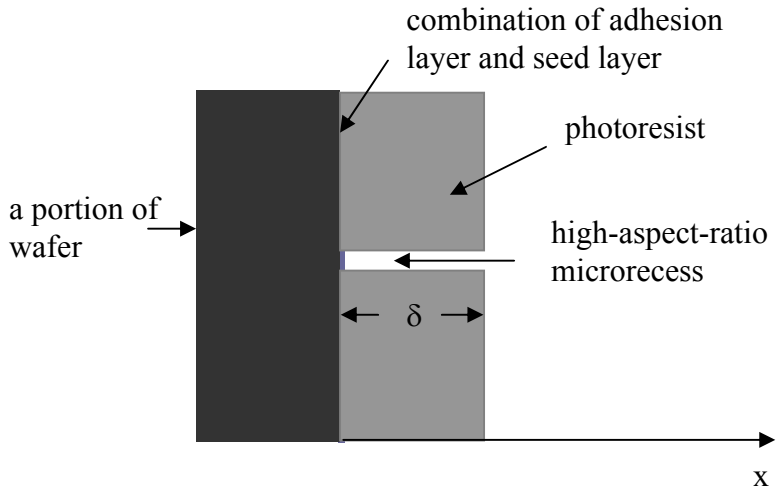


Figure 4.27: Details of a high-aspect-ratio microrecess formed by photoresist. The depth of the microrecess is δ.

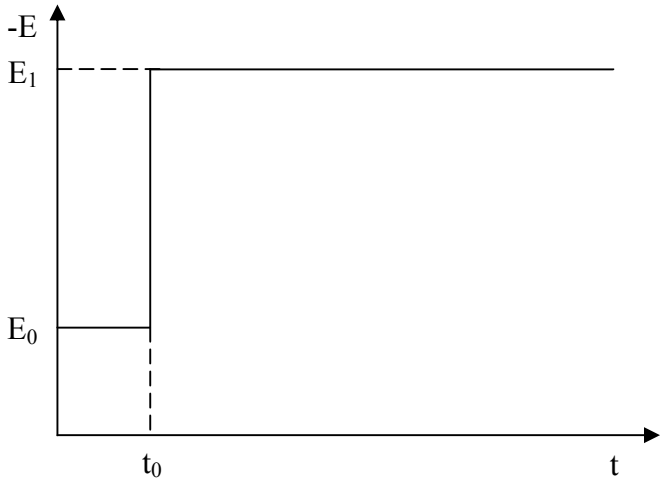


Figure 4.28: A potential step ($E_1 - E_0$) is applied to cathode at time $t = t_0$. E denotes potential.

C_s respectively in the bulk electrolyte and at the cathode surface. δ is the depth of the microrecess along the x axis. At time t_0^-, the concentration of nickel ions, C is assumed to be uniform for the entire solution inside the microrecess and is denoted by the bulk concentration C_b. As soon as an overpotential step ($E_1 - E_0$) is applied, an electric field is built across the

electroplating cell and the concentration of nickel ions at the cathode surface drops to the surface concentration C_s almost instantaneously corresponding to the surface kinetics controlled by overpotential. As a result, the electrochemical reaction must commence at the cathode surface at time t_0^+. The initial current density is very large as the reactive species begin to take part in the reaction and begin to start getting depleted at t_0^+. However, the spatial distribution of the concentration profile of the reactive species is a slower process with the instantaneous concentration of the reactive species at t_0^+ inside the recess staying at the bulk value except at the edge of double layer towards the cathode side. This results in a high value for concentration gradient near the cathode surface. Therefore, the diffusion flux of reactive species towards the cathode surface is instantaneously high resulting in a high value for the current density. As the on time duration progresses, the current density decreases while the concentration profile of the reactive species smoothes out and ultimately reaches a steady state value. The electroplating beyond this point during the on time resembles DC plating.

Hence, if the off time starts well before the above mentioned steady state condition is reached, the large instantaneous current density during each on time can result in a high sustained film growth rate. In this sense, certain advantages of pulse electroplating such as high nucleation rate can be realized. On the other hand, the lower limit on the on time needs to be tailored as well. It should be longer than the time needed to charge up the double layer capacitor. As stated earlier, the on time has to be significantly shorter than the transition time, τ, which is defined as the time needed to reach the steady state condition. The off time duration is not as important as the on time duration but it must also satisfy certain constraints. It needs to be longer than or at least comparable to the time needed to discharge the double layer capacitor. It should not be excessively long either because in the absence of applied potential, the plating solution

which is acidic can chemically etch away some of the deposited material. Hence, it is important to model this process and obtain an estimate of different times involved during pulse plating.

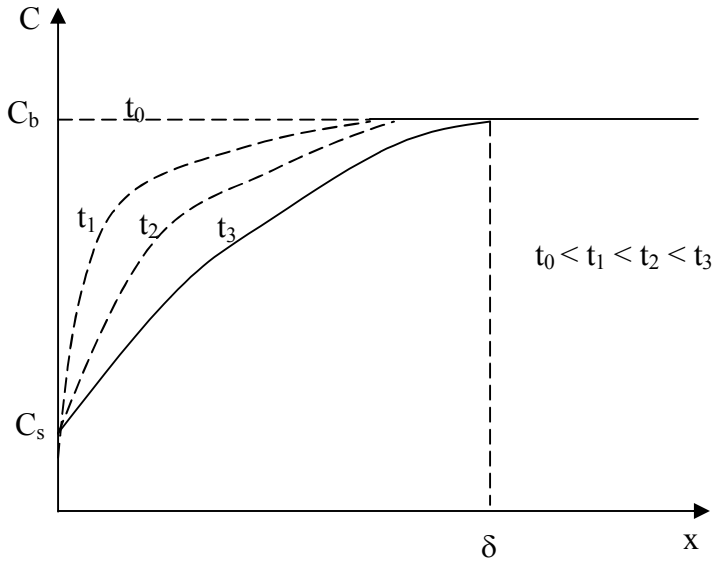


Figure 4.29: Concentration profile inside the microrecess with respect to time t. An overpotential step is applied at $t = t_0$ and the concentration progresses to steady state when $t > t_3$.

Starting with Fick's second law:

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2}, \qquad (1)$$

where C is the concentration of the electroplating reactive species, t is time, x is the distance and D is the diffusion coefficient of a certain reactive species. The boundary conditions are:

1) For $t > 0,\ x = 0,\ C = C_s$. This assumes that initial current density is infinite to lower the concentration from C_b to C_s instantly in Fig. 4.29.
2) For $t > 0,\ x = \delta,\ C = C_b$. Concentration of the reactive species at the recess entrance is always maintained at C_b, the bulk electrolyte concentration.

The initial condition is:

at $t = 0^+$, $C = C_b$, for x ≥ 0.

It is convenient to solve eqn. (1) by making the concentration C dimensionless:

Let $C^* = \dfrac{C - C_b}{C_s - C_b}$.

Substituting C^* into eqn. (1), one obtains:

$$\frac{\partial C^*}{\partial t} = D\frac{\partial^2 C^*}{\partial x^2} \quad . \tag{2}$$

The boundary conditions now become:

1) For $t > 0,\ x = 0,\ C^* = 1$, and

2) For $t > 0,\ x = \delta,\ C^* = 0$.

The initial condition now becomes:

At $t = 0^+$, $C^* = 0$.

Applying Laplace transform to eqn. (2) combined with corresponding initial and boundary conditions, we obtain:

$p\overline{C^*} - C^*(t = 0^+) = D\dfrac{d^2\overline{C^*}}{dx^2}$, where $\overline{C^*}$ is Laplace transform of C^*.

Since, $C^*(t = 0^+) = 0$ gives $p\overline{C^*} = D\dfrac{d^2\overline{C^*}}{dx^2}$

$$or\ \frac{d^2\overline{C^*}}{dx^2} - \frac{p}{D}\overline{C^*} = 0. \tag{3}$$

Eqn. (3) is a linear, homogeneous second-order ordinary differential equation. The solution to eqn. (3) is:

$$\overline{C^*} = C_1 e^{\sqrt{\frac{p}{D}}x} + C_2 e^{-\sqrt{\frac{p}{D}}x},$$

where C_1 and C_2 are constants. Combining the boundary conditions in eqn. (2), C_1 and C_2 can be obtained from boundary conditions:

1) $C^* = 1|_{x=0}$ gives $\overline{C^*} = \frac{1}{p}|_{x=0} = C_1 + C_2$, and

2) $C^* = 0|_{x=\delta}$ gives $\overline{C^*} = 0|_{x=\delta} = C_1 e^{\sqrt{\frac{p}{D}}\delta} + C_2 e^{-\sqrt{\frac{p}{D}}\delta}$ which give

$$C_1 = \frac{-\frac{1}{p}e^{-\sqrt{\frac{p}{D}}\delta}}{e^{\sqrt{\frac{p}{D}}\delta} - e^{-\sqrt{\frac{p}{D}}\delta}} \text{ and } C_2 = \frac{\frac{1}{p}e^{\sqrt{\frac{p}{D}}\delta}}{e^{\sqrt{\frac{p}{D}}\delta} - e^{-\sqrt{\frac{p}{D}}\delta}}. \quad (4)$$

Hence, the concentration is expressed as:

$$\overline{C^*} = \frac{-\frac{1}{p}e^{-\sqrt{\frac{p}{D}}\delta}}{e^{\sqrt{\frac{p}{D}}\delta} - e^{-\sqrt{\frac{p}{D}}\delta}} e^{\sqrt{\frac{p}{D}}x} + \frac{\frac{1}{p}e^{\sqrt{\frac{p}{D}}\delta}}{e^{\sqrt{\frac{p}{D}}\delta} - e^{-\sqrt{\frac{p}{D}}\delta}} e^{-\sqrt{\frac{p}{D}}x}. \quad (5)$$

For the case of high-aspect-ratio recesses where the assumption of diffusive mass transport of reactive species is valid, the current density j is given by Nernst diffusion layer model:

$j = -nFD\left.\frac{\partial C}{\partial x}\right|_{x=0}$ which can be written for dimensionless quantity C^* as

$j = -nFD(C_s - C_b)\left.\frac{\partial C^*}{\partial x}\right|_{x=0}$. Here F is the Faraday's constant, 96485 C/mol and n is the number of charges per ion.

After Laplace transform, j is expressed as:

$\overline{j} = -nFD(C_s - C_b)\left.\frac{d\overline{C^*}}{dx}\right|_{x=0}$. Here $\overline{j}$ is the Laplace transform of j.

Now $\left.\frac{d\overline{C^*}}{dx}\right|_{x=0} = C_1\sqrt{\frac{p}{D}} + C_2(-\sqrt{\frac{p}{D}})$. Substituting C_1 and C_2 from eqn. (4) and assuming $C_s = 0$ for complete depletion of reactive species at the cathode surface yields:

$$\bar{j} = -nFC_b\sqrt{\frac{D}{p}}\coth(\sqrt{\frac{p}{D}}\delta).$$

Now take $a = \frac{\sqrt{D}}{\delta}$ and plug it into above equation to get

$$\bar{j} = -nFC_b\frac{D}{\delta}\frac{1}{a\sqrt{p}}\coth(\frac{\sqrt{p}}{a}).$$

Inverse Laplace transform gives the expression of current density:

$$j = -nFC_b\frac{D}{\delta}[1 + 2\sum_{k=1}^{\infty}\exp(-k^2\pi^2\frac{D}{\delta^2}t)] \qquad (6)$$

Simulation result for current density j with respect to time t is given in Fig. 4.30 after a step potential ($E_1 - E_0$) is applied at the cathode surface. It shows the variation of current density vs. time for the case of δ = 100 μm. The diffusion coefficient value used in the simulation is the effective value obtained from experimental data in Section 4.3.2. The limiting current density obtained from this model for the above simulation is 96.8 mA/cm^2. Experimentally, diffusion controlled regime begins to become important at approximately 50 mA/cm^2 as mentioned in Section 4.3.1. This is shown on the non-uniform probe profile with smaller probe being plated at a slower rate in Fig. 4.14. Agglomeration of green color crystallized salts was also observed near the microrecess openings when DC current density reaches 100 mA/cm^2 as described in Section 4.3.1 for the case of microrecess being 100 μm deep. It is difficult to tell when the salt precipitation starts to agglomerate. But it is inferred that diffusion controlled regime for the DC plating case is between 50 and 100 mA/cm^2. The experimentally observed limiting current

density of 100 mA/cm^2 and the simulated result from the fixed boundary model of 96.8 mA/cm^2 are close. To compute transition time, τ, the current density to reach steady state is defined as 90% of this current density equal to the limiting current density. For the case of δ = 100 μm, this current density is -107.5 mA/cm^2. It takes 7 s for the current density to decay to -107.5 mA/cm^2, as indicated by a cross marker on Fig. 4.30. Figure 4.31 shows the current density variation predicted from the fixed boundary model for the case of δ = 500 μm. The limiting current density is proportionally decreased to -19.4 mA/cm^2 and the transition time to reach steady state is increased to approximately 220 s corresponding to a current density of -21.5 mA/cm^2, as indicated by the cross marker on Fig. 4.31.

The results of the model can be utilized to guide choice of experimental parameters. The power supply used in this work is a general purpose potentiastat. A three-electrode setup is employed in pulse electroplating with nickel plate being the anode, wafer coated with Ti/Cu base layers the cathode and saturated Calomel the reference electrode. An overpotential step is applied at the start of each t_{on}. Therefore, the results from the analytic model which starts at an overpotential step described in this section are approximately applicable. In practice, for all of the pulse plating cases in this work, an average current density approximately 100 mA/cm^2 is maintained during on time transient by regularly adjusting the magnitude of the cathode overpotential for the cases of 100 μm < δ < 200 μm. Since the DC limiting current density is close to 100 mA/cm^2 for δ = 100 μm as described in section 4.3.1, t_{on} can not be much longer than the transient time, τ. Otherwise electroplating can reach steady state and the deleterious side reactions may occur.

The value of τ is 7 s according to the simulation results in Fig. 4.30 and Fig. 4.32 (Section 4.6.2) for the case of δ = 100 μm. In experiments, the value of t_{on} has been chosen

between 5 s to 10 s, which gave a deposition rate 90 μm/hr same as the DC plating case for j = 100 mA/cm^2. However, when t_{on} is greater than 15 s, deposition rate is observed to decrease and crystal agglomeration starts to appear around the mouth of the microrecesses. As the deposition results are good for t_{on} = 10 s which is greater than 7 s indicated by the model, the diffusion process of the reactive species seems somewhat faster than the predicted value. Computation of t_{off} is not included in this model but t_{off} = 15 s for the case of δ = 100 μm has been sufficient according to the plating results and has been utilized throughout this work.

4.6.2 A Moving Boundary Approach

In reality, the diffusion layer thickness, δ is not a constant but is a function of time and it decreases with time. The base of the microrecess elevates as deposition progresses resulting in a

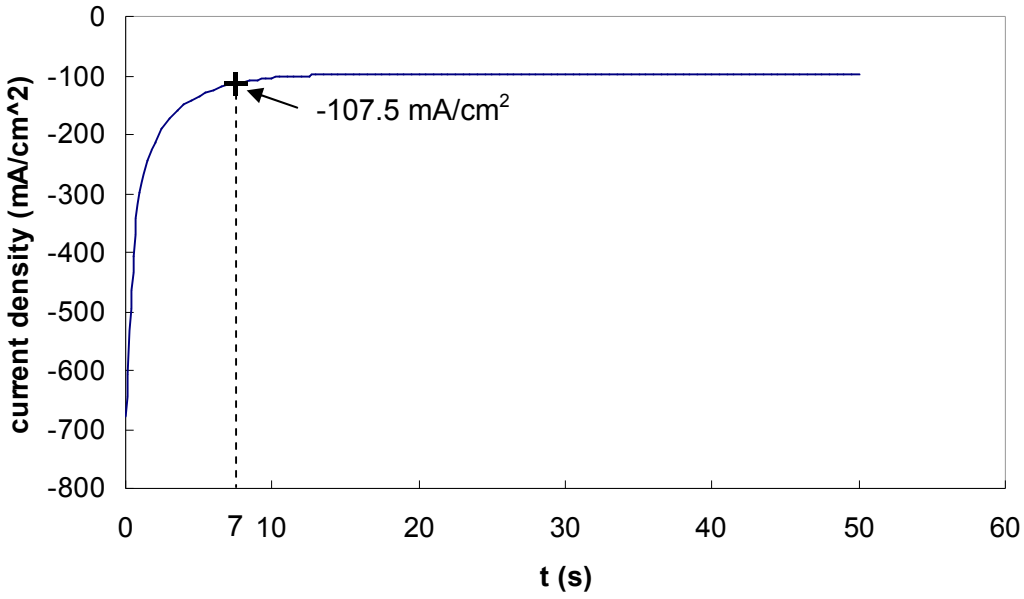


Figure 4.30: Simulated current density j as a function of time after a step overpotential is applied at the cathode surface for the case of δ = 100 μm. D = 3.3 × 10^{-6} cm^2/s (experimental value), C_b = 1.52 M and k = 1 to 3.

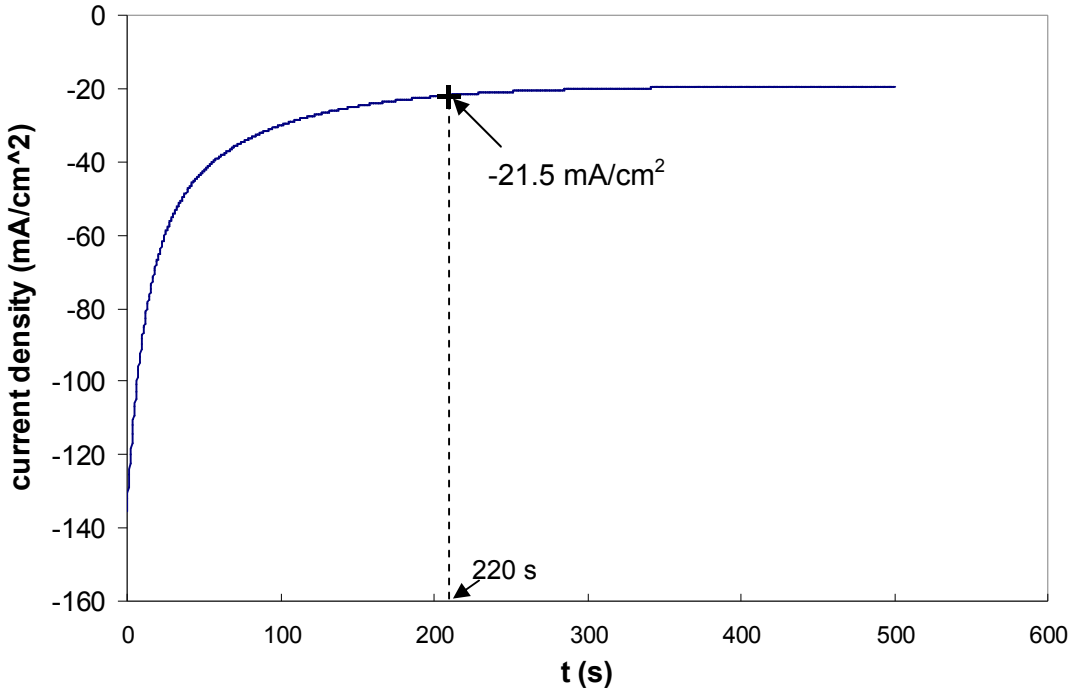


Figure 4.31: Simulated current density as a function of time after a step potential is applied at the cathode surface for the case of δ = 500 μm. D = 3.3 × 10^{-6} cm^2/s (experimental value), C_b = 1.52 M and k = 1 to 3.

moving boundary scenario. However, in order to obtain a high quality deposit, the deposition rate is usually low, i.e. $d\delta/dt$ is small. It is thus reasonable to retain the form of eqn. (6) and prescribe δ as a function of time t such that eqn. (6) is modified to:

$$j = -nFC_b \frac{D}{\delta(t)}[1 + 2\sum_{j=1}^{\infty} \exp(-j^2\pi^2 \frac{D}{\delta(t)^2} t)] . \qquad (7)$$

From this point, the change in j can be divided into two cases assuming both cases satisfying $t_{off} >> t_d$ during which reactive species are replenished in the microrecess:

- Case 1: $t_{on} > \tau$, and $t_{off} >> t_{d.}$
- Case 2: $t_c << t_{on} << \tau$, and $t_{off} >> t_{d.}$

Case 1 applies for long on pulse time case and case 2 applies for short pulse time case. In case 1, when $t_{on} > \tau$, electroplating enters diffusion controlled regime. In order to incorporate time t into

δ, we start from Nerst diffusion boundary layer model, which is a linear approximate to diffusion flux current density that is only valid for diffusion controlled regime:

$$j = -nFD\frac{C_b}{\delta(t)}. \tag{8}$$

At time t, $\delta(t) = \delta_0 - \int_0^t v dt$, (9)

where δ_0 = δ(0) which is the original depth of the microrecess, $v = \frac{sMj}{nF\rho}$ is the theoretic deposition rate obtained from Faraday's law, in which M is the molecular molar weight, j is the current density, F is the Faraday's constant (96485 C/mol), s is the number of ions involved in an elemental reaction, n is the number of charges per ion and ρ is the density of deposit. We then have

$$j(t) = -nFDC_b\frac{1}{\delta_0 - \int_0^t \frac{sM|j(t)|}{nF\rho}dt}. \tag{10}$$

Absolute value of j(t) is taken in eqn. (10) as the cathodic current is negative by default.

For $Ni^{2+} + 2e \Leftrightarrow Ni$, s = 1 and n = 2. Substituting s and n into equation gives

$j(t) = -2FDC_b\frac{1}{\delta_0 + \int_0^t \frac{M}{2F\rho}j(t)dt}$, which is rearranged into

$$-\frac{2FDC_b}{j(t)} = \delta_0 + \frac{M}{2F\rho}\int_0^t j(t)dt. \tag{11}$$

Differentiating both sides of eqn. (11) with respect to t gives:

$2FDC_b\frac{1}{j(t)^2}\frac{dj(t)}{dt} = \frac{M}{2F\rho}j(t)$, which is rewritten as

$$\frac{1}{j(t)^3}dj(t) = \frac{M}{4F^2DC_b\rho}dt. \tag{12}$$

Integrating eqn. (12) on both sides, from j_0 to j_t on the left side and from 0 to t on the right side step by step yields

$$\frac{1}{2} j(t)^{-2}\Big|_{j_0}^{j_t} = -\frac{M}{4F^2 DC_b \rho} t ,$$

$$\frac{1}{j(t)^2} = \frac{1}{j_0^{\,2}} - \frac{M}{2F^2 DC_b \rho} t$$, and its final form becomes

$$j(t) = \pm \sqrt{\frac{1}{\frac{1}{j_0^{\,2}} - \frac{M}{2F^2 DC_b \rho} t}} .$$

Since j is defined negative as current flows into an electrode which is the case of electrodeposition at cathode, the above expression should take the negative sign. Therefore, we have

$$j(t) = -\sqrt{\frac{1}{\frac{1}{j_0^{\,2}} - \frac{M}{2F^2 DC_b \rho} t}} , \qquad (13)$$

where $j_0 = -nFD\frac{C_b}{\delta_0}$, which is in the form of Nernst diffusion boundary layer model. It must be noted that eqn. (13) is valid only for diffusion controlled regime as its derivation starts from Nernst diffusion boundary layer model, eqn. (8). At t = 0, it is easily seen that the current density ends up with j_0. As t increases, the magnitude of current density increases. This makes sense because as long as the conditions of diffusion control are satisfied, δ decreases with the increase of time and the magnitude of current density increases according to Nernst diffusion boundary layer model. Repeating eqn. (9) gives

$$\delta(t) = \delta_0 - \int_0^t vt$$
$$= \delta_0 - \int_0^t \frac{sM|j(t)|}{nF\rho}dt$$
$$= \delta_0 + \frac{M}{2F\rho}\int_0^t j(t)dt. \quad (14)$$

The integral part of eqn. (14) is

$$\int_0^t j(t)dt = \frac{4F^2DC_b\rho}{M}\left[\left(\frac{1}{j_0^{\,2}} - \frac{M}{2F^2DC_b\rho}t\right)^{1/2} - \frac{1}{|j_0|}\right].$$

Substituting this integral into eqn. (14) yields δ(t),

$$\delta(t) = \delta_0 + 2FDC_b\left[\left(\frac{1}{j_0^{\,2}} - \frac{M}{2F^2DC_b\rho}t\right)^{1/2} - \frac{1}{|j_0|}\right]. \quad (15)$$

Substituting eqn. (15) into equation (6) gives a closed form equation for current density, j(t), which is now the solution to a moving boundary case, assuming electrodeposition is under diffusion controlled regime. Figure 4.32 shows the variation of current density vs. time. The current density is instantaneously high as soon as a potential step is applied at the cathode surface. It decreases to a steady state value -97.6 mA/cm^2 and steadily increases again as the recess depth gradually reduces. Note the limiting current density value is greater than the value given by fixed boundary model, i.e. -96.8 mA/cm^2. This is due to the fact that the depth of the microrecess decreases resulting in a greater limiting current density as electrodeposition progresses. The transient time τ is approximately 7 s as well corresponding to a current density -108.4 mA/cm^2 defined as 90% of which equals limiting current density value of -97.6 mA/cm^2.

The depth of the microrecess or diffusion length δ(t) plotted from eqn. (15) is shown in Fig. 4.33. It shows that the depth of microrecess constantly decreases in a nearly linear

relationship with respect to time t. Deposition under diffusion controlled regime is slow and the process is prone to disturbance. Hence, the quality of deposit suffers. As indicated by Figs. 4.32 and 4.33, t_{on} should not be significantly greater than 7 s to suppress side reactions.

The rate of change of δ is plotted in Fig. 4.34. It is seen that dδ(t)/dt is negative. It is also seen that the curvature of dδ(t)/dt is negative as well, which means as long as the step overpotential ($E_1 - E_0$) is maintained, the decrease rate of δ accelerates because the current density increases, as indicated by Fig. 4.32. In experiments, steady increase of current density is observed where nickel is plated into microressed columnar holes by utilizing pulse plating. In order to obtain an approximately constant deposition rate, the overpotential magnitude is constantly adjusted to reduce the current density during t_{on} to the 100 mA/cm^2 level. Galvanostatic setup is not available from the potentiastat utilized in this work and is also not advised because the benefit of high instant nucleation rate at the beginning of each t_{on} will not apply.

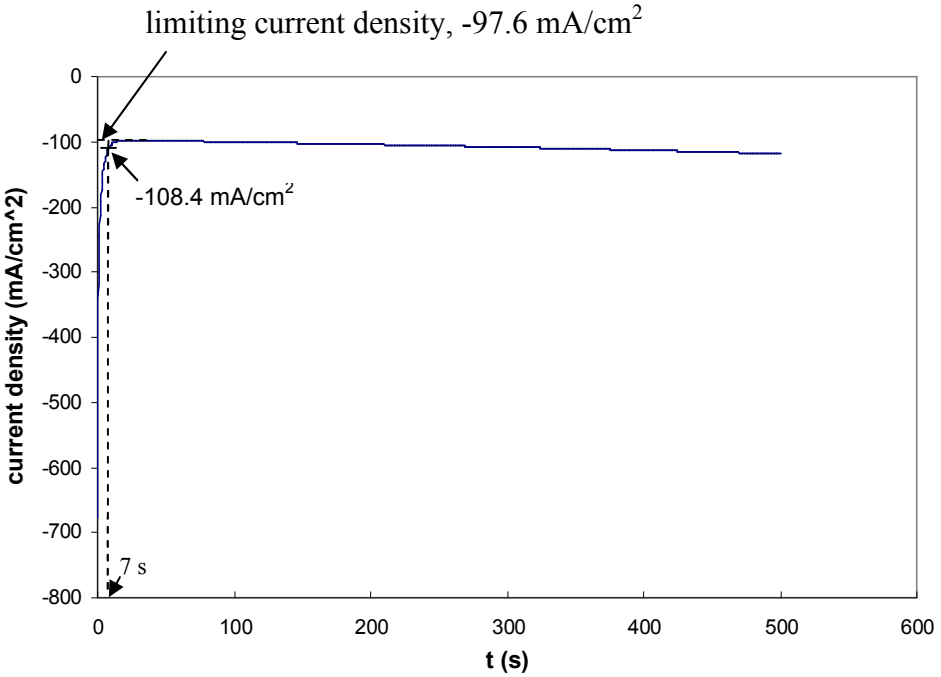


Figure 4.32: Simulated current density as a function of time after a step potential is applied at the cathode surface for the case of δ_0 = 100 μm utilizing the moving boundary model. D = 3.3 × 10^{-6} cm^2/s (experimental value), C_b = 1.52 M and k = 1 to 3.

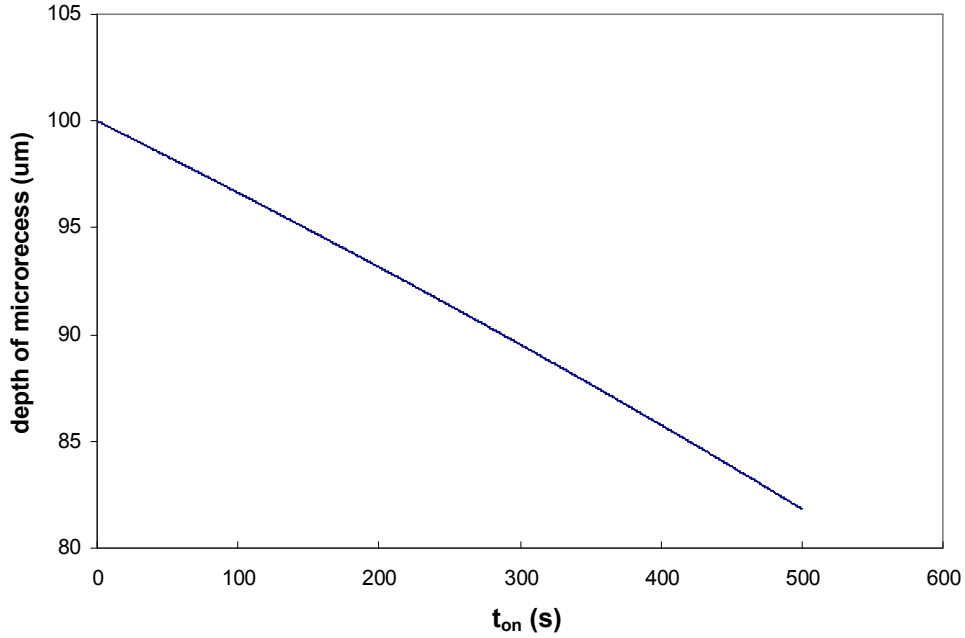


Figure 4.33: Simulated depth of the microrecess, δ as a function of time t_{on} after a step potential is applied at the cathode surface for the case of δ_0 = 100 μm utilizing the moving boundary model. D = 3.3 × 10^{-6} cm^2/s (experimental value), C_b = 1.52 M and k = 1 to 3.

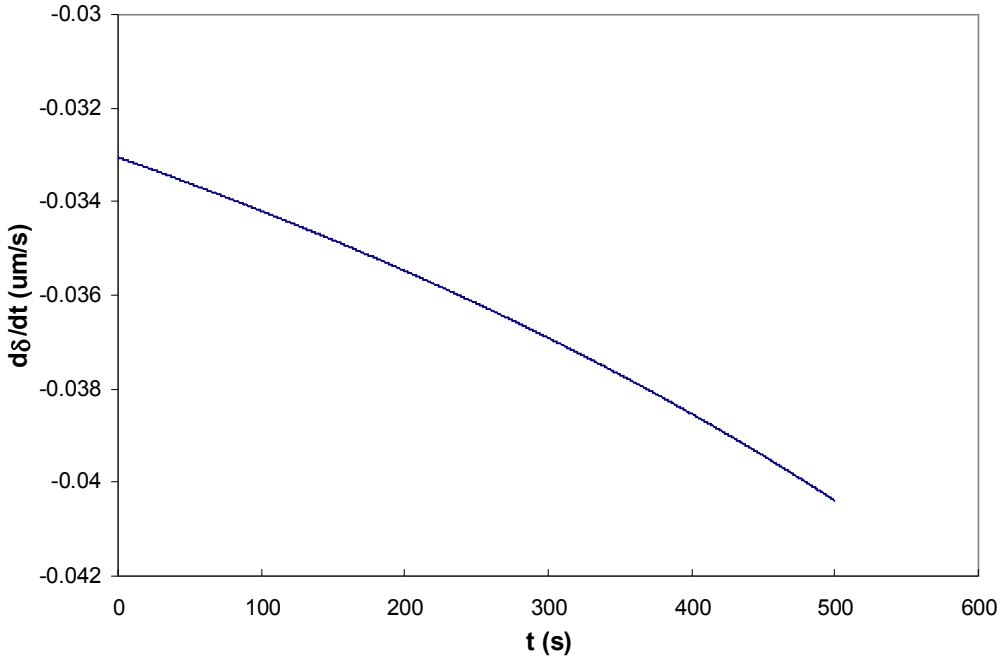


Figure 4.34: Simulated rate of change in δ with respect to total on time. Note that the curvature of dδ(t)/dt is also negative, indicating an acceleration in the rate of δ change. D = 3.3 × 10^{-6} cm^2/s (experimental value), C_b = 1.52 M and k = 1 to 3.

In case 2, $t_c << t_{on} << \tau$. This is the case shown in Fig. 4.18 b) where the electroplating current density during t_{on} is maintained approximately the same as the current output from power supply. This is the desired case for obtaining good characteristics of pulse plating as it takes advantage of large pulse current density without deleterious effects from side reactions by avoiding current-limiting diffusion controlled regime. To obtain the dynamic value of current density j and microrecess depth, δ, a computation flow diagram is given in Fig. 4.35. In this diagram, current density at the start of each t_{on} is computed from eqn. (7) utilizing a new value of δ calculated from eqn. (9). This computation step is repeated at the end of each t_{on}. The current density during each t_{on} is assumed to be constant as the on pulse time period is short. The magnitude of this current density steadily increases with respect to the total on time, t_{on}. This is shown in Fig. 4.36.

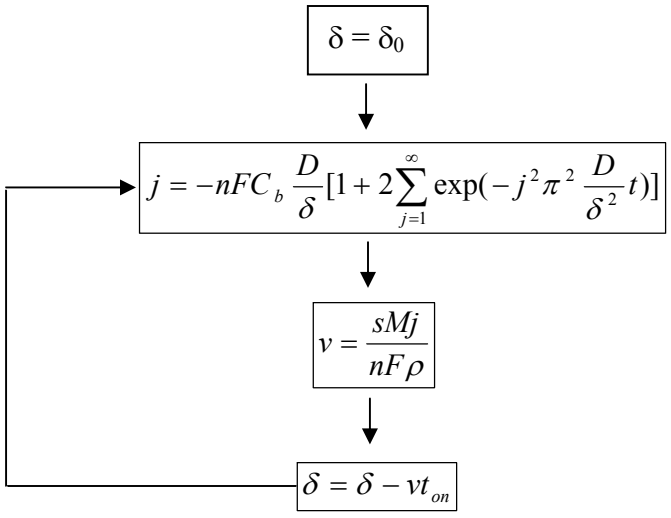


Figure 4.35: Flow diagram to compute dynamic values of current density at the start of each t_{on}, the deposition rate and the microrecess depth for the case of moving boundary approach.

δ decreases with time as shown in Fig. 4.37. The deposition rate steadily increases as a result of the decrease in microrecess depth and the corresponding increase in the current density. This is shown in Fig. 4.38.

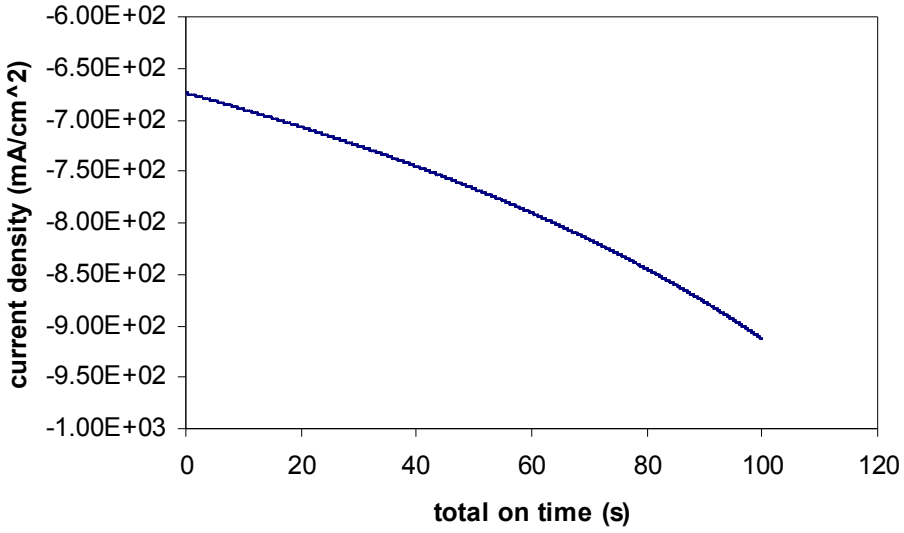


Figure 4.36: Variation of starting current density as a function of total on time, t_{on}.

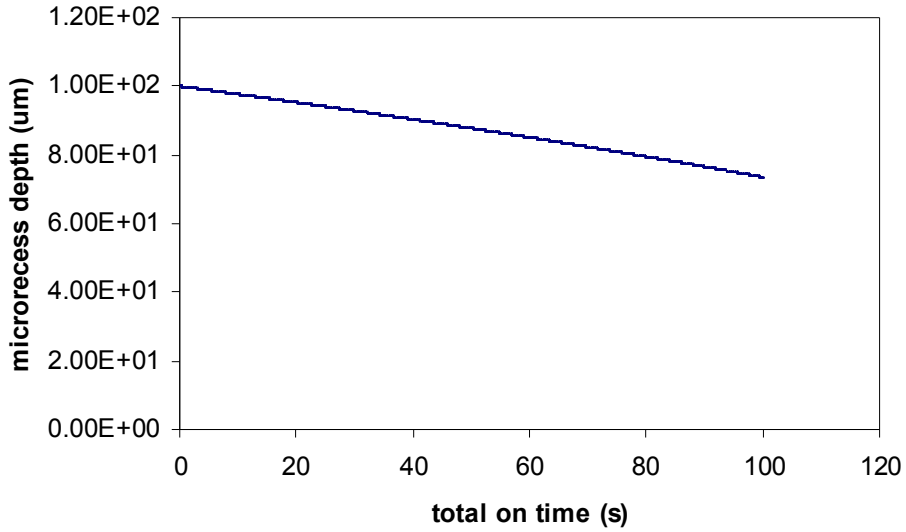


Figure 4.37: Variation of the microrecess depth as a function of total on time, t_{on}.

From the above modeling results, it is seen that utilization of potentiastatic setup for pulse electroplating has its advantage and disadvantages. For case 1, the advantage lies in the instantaneous large current density magnitude at the beginning of each t_{on} which leads to a large nucleation rate. This large nucleation rate can lead to a more compact microstructure with less tensile stress desired in thin film coating and microfabrication. The disadvantages are that the

electroplating process requires a regular adjustment on the magnitude of overpotential to maintain a relatively constant current density and hence plating rate. In experiments, this adjustment is performed manually. A potentiastatic experimental setup favors pulse plating on flat substrates in which case the microrecess structure is not present hence a constant plating rate is obtained without needing regular adjustment on the magnitude of the cathode overpotential. Case 2 is desirable as the entire course of on time electroplating is under a high current density which far exceeds limiting current density. Hence, the microstructure is more compact and the internal stress is either more compressive or less tensile.

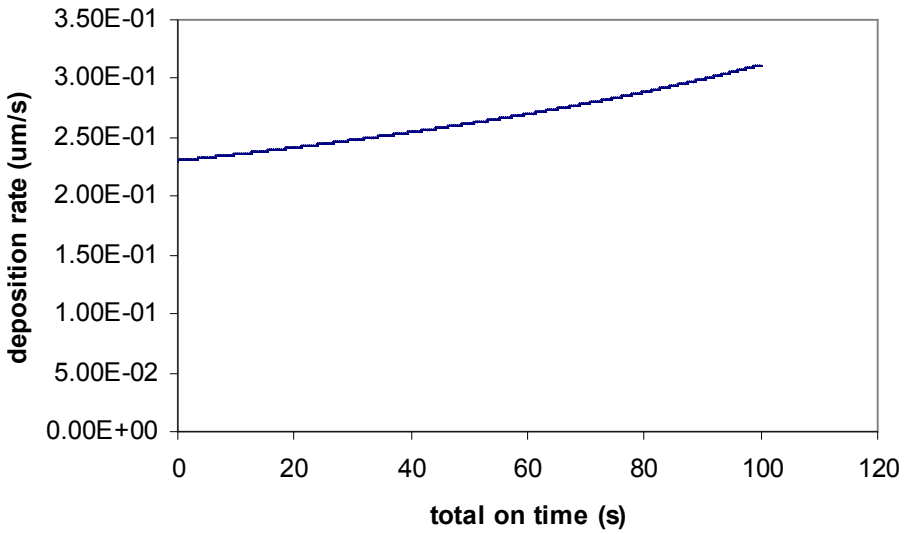


Figure 4.38: Variation of deposition rate as a function of total on time, t_{on}.

4.7 Summary

In this chapter, DC and pulse electroplating of nickel is investigated in detail. Nickel sulfamate is utilized as an electrolyte along with certain amount of pH buffer and surfactant components. It is found that the plating current efficiency increases with increase in cathodic current density but drops considerably after reaching the diffusion controlled regime. Electroplating rate also increases with current density in an approximately linear relationship

prior to reaching diffusion controlled regime. Current efficiency and electroplating rate measurements are performed on flat silicon substrates coated with Ti/Cu combination base metal layers.

During DC plating into microrecesses, the centers of the microprobes are plated at a slower rate compared to the peripheral area, probably due to a non-uniform distribution of electrical field lines within the microrecesses with peripheral areas having denser field lines resulting in a faster plating rate. It was also found that a more closely packed probe array is plated at a faster rate compared to a loosely packed one. This phenomenon is attributed to a more densely packed microrecess array drawing more field lines. As to individual probes, a faster plating rate was found on probes with smaller dimensions when current density is low, i.e. before diffusion controlled mass transport dominates.

However, when the current density increases further so as to reach the diffusion limited transport, the microprobes with smaller dimension were plated at a slower rate. With diffusion-limited transport, increasing plating current density further causes side reactions to take place, which has resulted in undesired precipitation around the microrecess openings. Diffusion coefficient is calculated by using Nernst diffusion boundary layer model. It results in a value of 3.3×10^{-6} cm^2/s for the diffusion coefficient that is about half of the value for the ideal case in a very dilute solution.

Stress is an important issue for nickel deposit and has been analyzed by utilizing X-ray diffraction technique. Samples for stress measurements are deposited on flat silicon wafer coated with adhesion/seed combination layers. For the DC plating case, it is found that the internal stress in nickel deposit changes from compressive to tensile as cathodic current density increases. Stress-free nickel deposits can be obtained at a current density of approximately 26 mA/cm^2. The built-in tensile stress saturates at 92 MPa when the current density is over 30 mA/cm^2. For DC

plating case under a constant current density of 100 mA/cm^2, the internal stress transition from compressive to tensile also occurs along with an increase in nickel deposit thickness and saturates at 73 MPa for thicknesses over 10 μm.

Stress is also characterized for the pulse plating case. For pulse plating with long duration pulse time t_{on} under 10 s and current density of 100 mA/cm^2, the nickel deposits undergo a stress transition from tensile to compressive and back to tensile stress as pulse off time increases from 0.5 to 3 s. The tensile stress value saturates as pulse off time increases from 3 s to 20 s. A comparison between the DC and the long duration electroplating cases, under otherwise similar conditions, shows that the built-in saturation stress value in the pulse plated deposit is 54.5 MPa which is about 25% lower than the corresponding value observed in the DC plated deposit. Pulse plating by short duration on-pulses in ms range are found to always yield compressive built-in stress between -110 MPa to -160 MPa.

Grain size and morphology of nickel deposits have been inspected by SEM. It is observed that the grain size in long duration pulse plating coincides with the type and magnitude of the built-in stress, that is, increasing tensile or decreasing compressive stress results in a smaller grain size. For short duration pulse plating case, the surface morphology of the grains is different compared to the DC plating or the long duration pulse cases with the former showing rougher or choppier grain facet features. This choppiness in the grain facets decreases as the on time of the short duration pulses is increased with off time kept constant at 4 ms.

A one-dimensional simplified electroplating model is described for the case of fixed boundary and for the case of moving boundary in order to describe the pulse electroplating process under a potential step-input. Compared to the numerical approaches taken by most of the modeling work in the literature, this model is analytical and straightforward and has been utilized to give a rough measure on choices of on time during pulse plating. In the fixed boundary

approach where variation in microrecess depth δ is neglected, the model shows that it takes about 7 s to transit to 90% of steady state current density for the case of δ = 100 μm corresponding to a limiting current density -107.5 mA/cm^2. For the case of δ = 500 μm, the transition time is increased significantly to 220 s and the corresponding current density is -21.5 mA/cm^2. In the moving boundary approach, the dynamic change in δ is taken into account. As total on time increases, the diffusion boundary layer thickness, δ decreases. Correspondingly, the current density and the deposition rate also increases under the condition of the magnitude of overpotential being maintained at the same value. Two normal cases are treated in this model. Case 1 treats the situation of long on time pulse, in which diffusion controlled regime is eventually reached. Case 2 treats the situation of a very short on time pulse, in which the plating current density is approximately the same as the output from the power supply. Case 2 is desirable as it takes the advantage of high instantaneous nucleation rate and hence can result in more compact structure and less tensile stress. The models offer a qualitative understanding of the pulse electroplating process and also give a rough measure on choice of on time period. In Chapter 6, an on time period of 10 s has been utilized for the case of δ = 100 μm which is comparable to the computed transition time from the modeling results. However, the models presented above are not as comprehensive as some of the numerical models for which multiple mechanisms have been taken into account.

Chapter 5. Electrochemical Sharpening of Microneedles

5.1 Introduction

Sharpened tips have found applications in various fields such as low-voltage field emission, cell biology, nanolithography and electron microscopy. In recent years, ultrasharp tips have attracted researches' interest primarily for their critical role in STM (scanning tunneling microscopy) and AFM (atomic force microscopy). Sharpened tips can also be utilized as sensors such as neural probes as a potential application that senses the neural signal pulses of the central nervous system. In the latter application, sharpened probes can reduce tissue damage, ease tissue penetration and boost signal-to-noise ratio compared to dull probes.

The procedures reported in literature for producing sharp tips can be divided into two major categories: (1) mechanical or (2) electrochemical. The most widely used techniques for fabrication of sharp tips have been based on electrochemical methods [5.1-3]. These techniques involve using a suitable electrolyte to sharpen metallic wires by rapid local dissolution in an applied electrical field. The conditions used for metallic probe sharpening are similar to those that are used in electropolishing of metals in which the surface smoothness is achieved through anodic treatment in an electrolyte. Electrochemical sharpening is the opposite of electroplating. It is desirable that both macro-smoothening and micro-smoothening are achieved. Macro-smoothening, or leveling is the removal of surface roughness greater than 1 μm; and micro-smoothening or brightening is the removal of surface roughness nominally less than 1 μm. Unfortunately, the above methods that are used to sharpen metallic tips electrochemically are still rather empirical and usually difficult and unreliable.

Electrochemical etching was first reported by Muller to sharpen metallic tips [5.4]. Since then, this technique has been extensively utilized with both DC and AC currents to sharpen a variety of metallic wires such as W, Au, Ta, Te, Pt, Ir and Pt-Ir in an electrolyte bath [5.1,5.5].

The approach takes advantage of a high local etching rate of an immersed wire at the interface between a liquid and air that surrounds the wire. The setup is shown in Fig. 5.1. As a result, the wire is cut into two pieces and the immersed portion of the wire is separated from the top part. In this way, the sharp tips formed at the separation point are preserved but only the tip on the top part of the wire is retained. The reported value for the radius of the sharpened tips is approximately 0.1 mm [5.6-8]. Fotino has given a fairly complete survey of existing tip-sharpening literature and provided details on tip sharpening by electrochemical etching both utilizing the normal technique with tip pointing into the solution and utilizing reverse technique with the tip pointing away from the solution [5.1]. It has been shown that the reverse etching scheme yields ultrasharp tungsten tips by employing so-called bubble dynamics [5.9]. In the normal scheme, the tip of the wire is pointing downward; while in a reverse setup, the wire is curved so that the tip of wire points upwards.

Electrochemical etching of nickel wires is usually carried out in acidic solutions. Nickel tips have been electropolished in H_2SO_4, H_3PO_4, CrO_3, or HCl [5.10-12]. Nikolova et al. have investigated the parameters for sharpening of nickel tips that control the sharpening process with respect to tip geometry in H_2SO_4 diluted in glycerine/water [5.13]. They took the advantage afforded by the large local etching rate offered by a concentrated electrical field to obtain sharpened tips at the broken sections of the wire.

5.2 Experimental Setup

However, this advantage of a faster etching rate at the liquid-air interface can not be exploited in this work because our probes are micro-scale in cross-section and their absolute lengths are short typically less than 1 mm. The magnitude of ripples at the the liquid-air interface could easily swallow and possibly dissolve the entire length of the probe. It is, hence, difficult to ensure a partial immersion of such short probes into the electrolyte. The μSET lab and CAMD at

LSU have performed some work on nickel wire etching and also on LIGA microprobe tips sharpening by electrochemical technique in a KCl aqueous electrolyte [5.14].

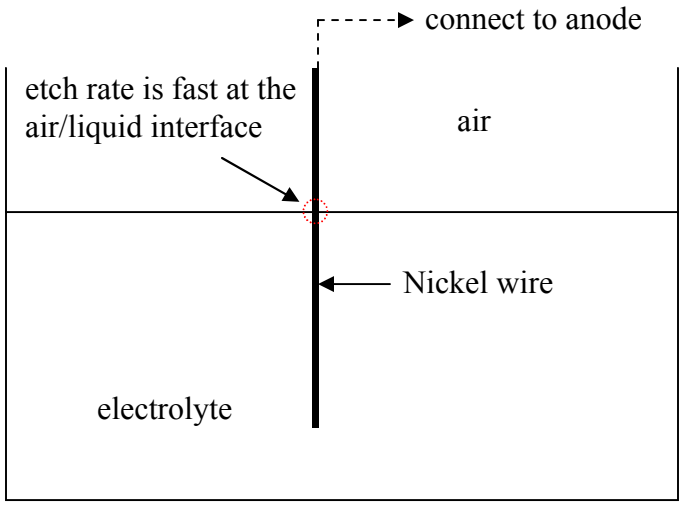


Figure 5.1: A normal experimental setup for separating wire at the liquid/air interface where the etch rate is fastest. A sharpened tip is preserved in the top section of wire. Only the anode connection is shown.

In this work, a simple approach is taken for obtaining sharpened tips. A sulfuric acid solution is used as an etchant. The setup utilizes the normal scheme in which the tip points away from the air/liquid interface. The experiments are first performed on commercially available round nickel wires 50 μm in diameter from Sigma. This size is chosen since it is comparable to the diameter of the microprobes fabricated in this work. Since the nickel wires must mimic the situation present for the microprobes, it is necessary that the sharpening event occur at the end of the wire end and not in the middle. The portion of wire that is exposed at the liquid/air interface, hence, needs to be protected because the etching rate is maximum there. In this work, a small amount of melted paraffin is applied to the wire around the portion of the wire near the liquid-air

interface. The end of the wire that needs sharpening is exposed to the electrolyte. The wire/electrolyte setup is shown in Fig. 5.2.

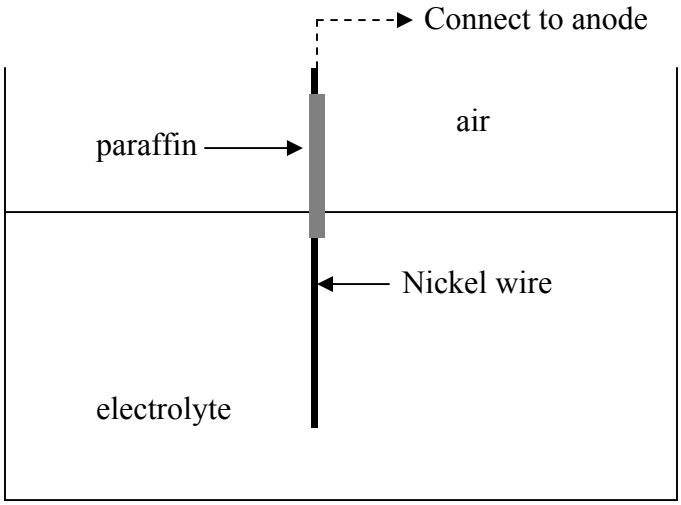


Figure 5.2: A schematic of the setup utilized for nickel wire tip sharpening. Paraffin is used to protect the wire near the liquid-air interface.

The complete experimental setup is shown in Fig. 5.3. A nickel wire is used as the anode. It is fixed to a square Teflon plate, with paraffin protecting the interface section. The cathode is a thin platinum wire that is manually wired into a mesh onto another square Teflon plate of the same size. The distance between the two electrodes is 1 cm.

5.3 Design of Experiment

Dilute sulfuric acid is utilized as the electrolytic etchant. Three major factors that control the tip sharpening process are: 1) concentration of sulfuric acid, 2) temperature and 3) anodic voltage. Each of the three factors is tested at two levels giving a total number of eight combinations as shown in Table 5.1. The experiment employs a two-electrode setup. First of all, each of the eight combinations of these three factors is exhausted in order to identify the

combination that sharpens nickel wires most effectively. Second, for this selected combination, the tip sharpening process as a function of time is recorded using an optical microscope.

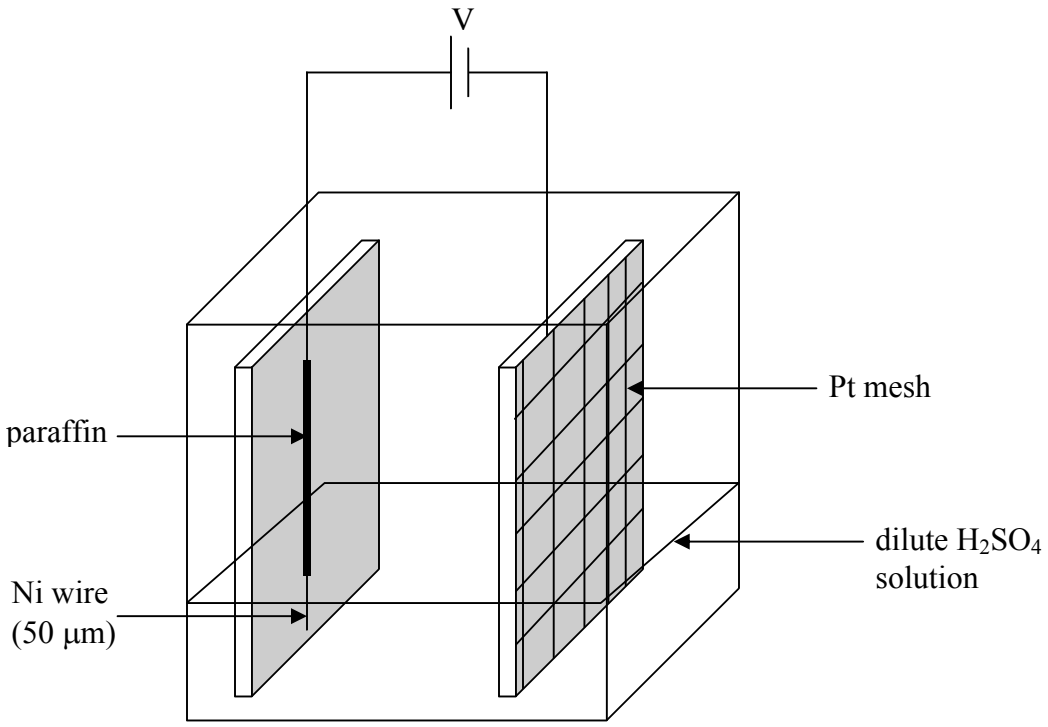


Figure 5.3: The electrochemical etch cell for nickel wire tip sharpening.

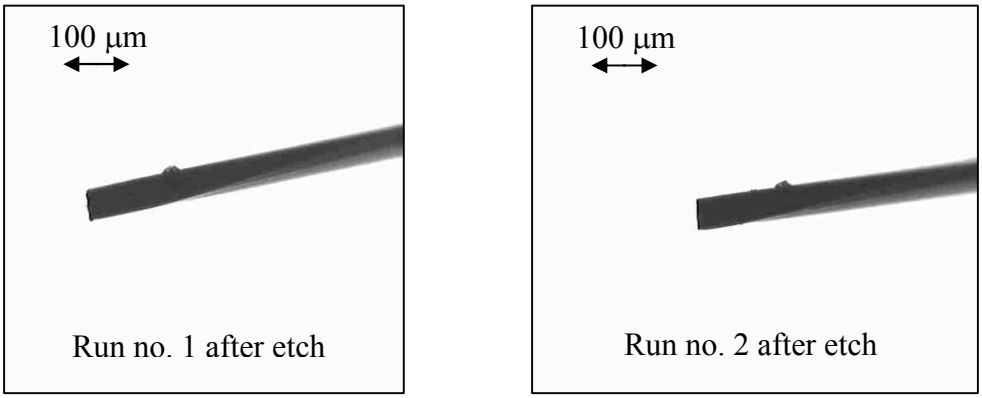
In this experiment, the two concentrations of sulfuric acid used are 0.1 M and 0.5 M; two temperatures chosen are laboratory room temperature (20 °C) and 30 °C; the two voltage values between the two electrodes are 2 V and 4 V. The etching time is kept constant at 30 seconds for each experiment. An additional experiment is performed without applying any anodic voltage at room temperature which serves as a control group to differentiate between pure chemical etching and electrochemical etching. It is found that pure chemical etch rate (Run no. 9 in Table 5.1) does not result in any noticeable change on the wire profile. Figure 5.4 shows the profile of tips under different situations.

Table 5.1 Experiment design for Ni tip sharpening. RT denotes room temperature.

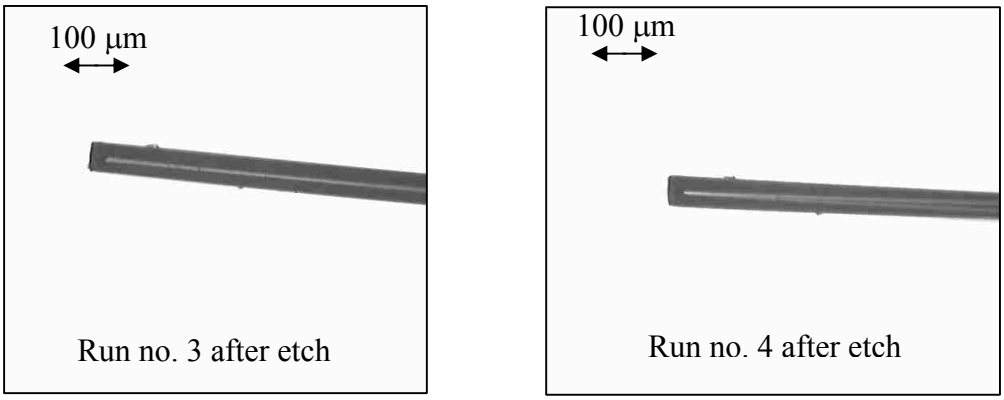
Run No.	$C_{H_2SO_4}$ (M)	Temp (°C)	Voltage (V)	Tip radius change
1	0.1	RT	2	No change
2	0.1	RT	4	No change
3	0.1	30	2	No change
4	0.1	30	4	No change
5	0.5	RT	2	Very small change
6	0.5	RT	4	Some change
7	0.5	30	2	Very small change
8	0.5	30	4	Significant change
9	0.5	RT	0	No change

Comparing Run no. 1 and Run no. 2 in Table 5.1, it is seen that under 0.1 M acid concentration and at room temperature, varying anodic voltage from 2 V to 4 V did not make a noticeable change on the final tip profile. At an elevated temperature, 30 °C, varying anodic voltage from 2 V to 4 V had no effect on the nickel tip profile either. It is only after raising the concentration of sulfuric acid from 0.1 M to 0.5 M that the tip profile started showing some change. A very noticeable change is seen after Run no. 8, in which all of the three control factors are at high levels, i.e. 0.5 M, 30 °C and 4 V. The tip profile at the end of 30 seconds is very sharp.

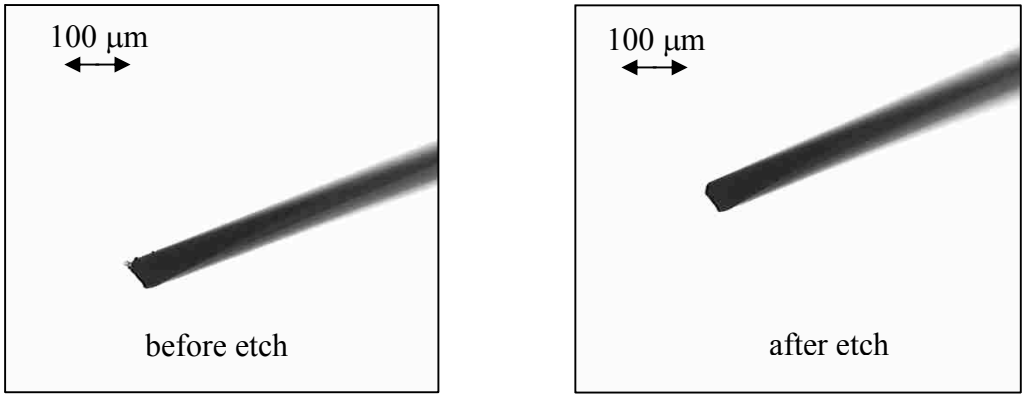
Another observation was that the diameter of nickel wire became smaller after Run nos. 6 and no. 8. This indicates that the body of wire is also etched although the end of wire is etched at the fastest rate.



a) Run no. 1 and Run no. 2 after etch



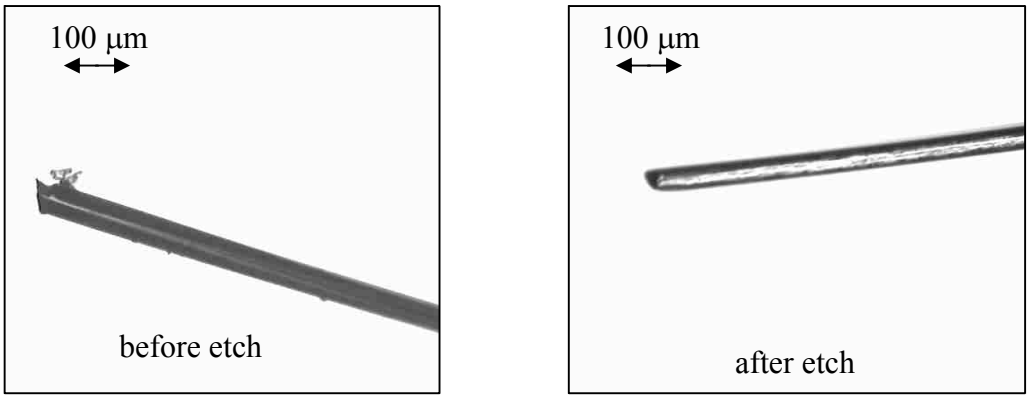
b) Run no. 3 and Run no. 4 after etch



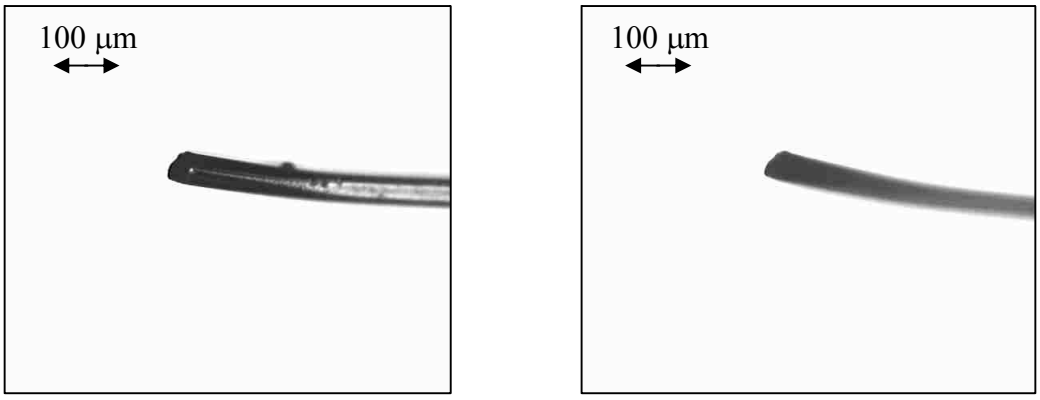
c) Run no. 5 before and after etch

Figure 5.4: Tip profiles resulting from various experimental runs.

(Fig. cont'd)

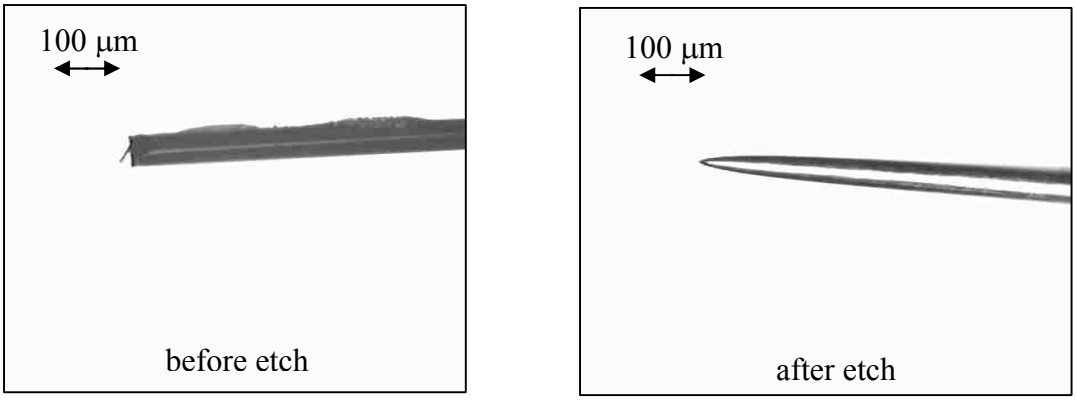


d) Comparison of Run no. 6 before and after etch



before etch after etch

e) Comparison of Run no. 7 before and after etch



f) Comparison of Run no. 8 before and after etch

5.4 Tip Sharpening Progress

From the screening experiments in section 5.3, it is seen that Run no. 8 sharpens the nickel tip most effectively. The parameter values for this run are then utilized for an etching time span between 0 to 45 seconds, as shown in Table 5.2.

Table5.2 Etching time for sharpening nickel tip in 0.5 M H_2SO_4 at 30 °C and 4 V anode voltage.

Sample no.:	1	2	3	4	5	6	7	8
Etching time (s):	0	5	10	15	20	25	35	45

Due to the increased electrical field at smaller radius of curvature, the periphery at the end of the wire is always dissolved first. This is clearly seen in Fig. 5.5 b), compared to the original tip shape in Fig. 5.5 a). With increasing etch time, the wire end rounds off and a sharper tip is gradually developed. This is depicted in Figs. 5.5 c) and d). Once a sharp tip is formed, it dissolves quickly as it now has a smaller radius of curvature. Another edge at the end of the wire with a smaller diameter is now formed, which will be now rounded off. The dissolution along gradually pointed wire end and along the blunt edge of the tip continues till a tip with the smallest radius of curvature is obtained. Along with the tip sharpening, the wire is also shortened and the bulk of the wire gets thinner since the entire section of the immersed wire is exposed to the electrolyte and the electrical field. The bulk section of the wire, however, dissolves at a slower rate as seen from Figs. 5.5 e) - h).

The same parameters, i.e. T = 30 °C, $C_{H_2SO_4}$ = 0.5 M, V = 4 V are also applied to a diced chip with nickel probes 200 μm tall and 70 μm wide, as shown in the Fig. 5.6 a). The metal seed layer on the chip is protected by melted paraffin and the electrical connection from chip to the anode of the power supply is made by attaching gold wires between them. Etching is carried out

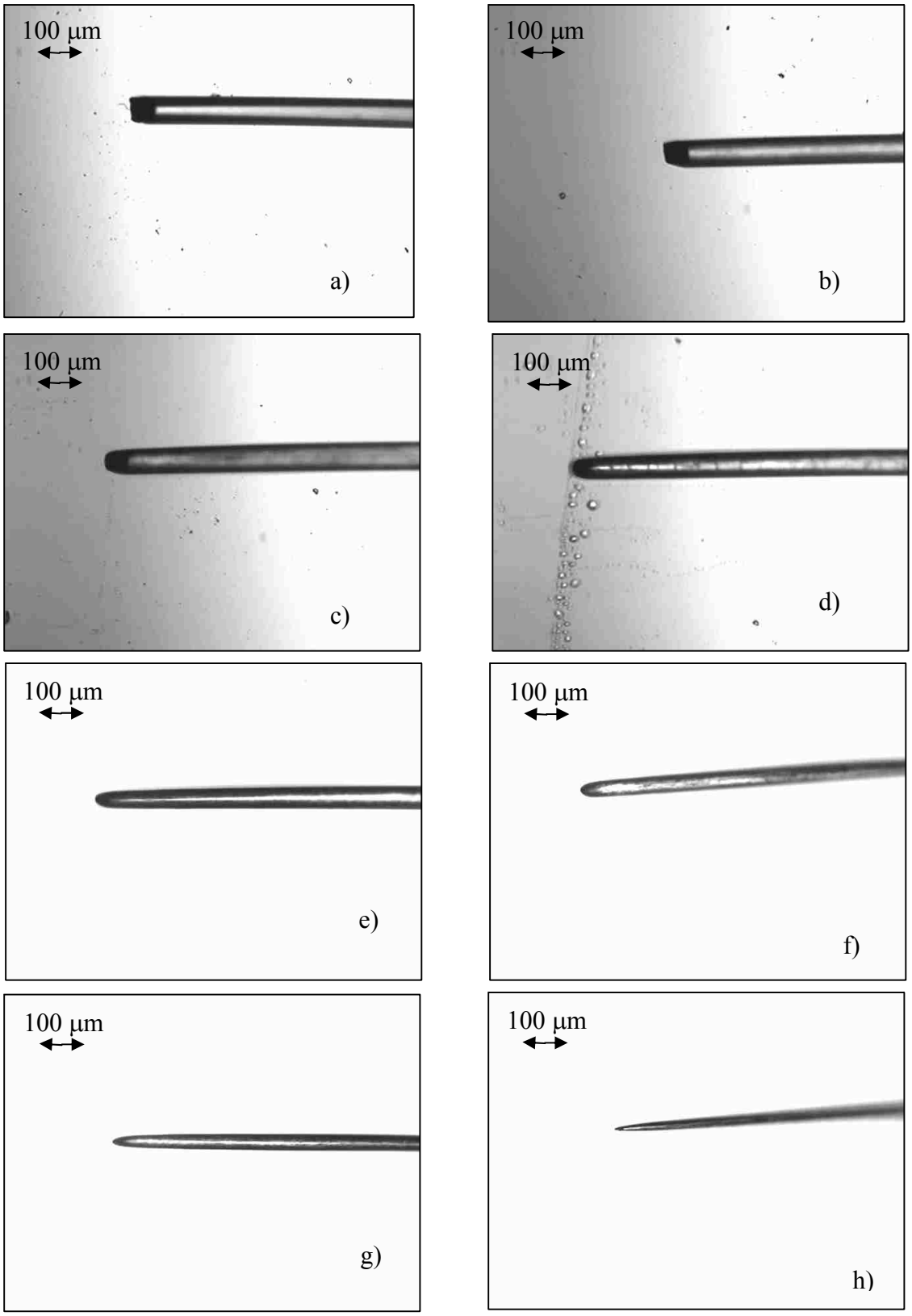


Figure 5.5: Tip profiles after a) 0 s, b) 5 s, c) 10 s, d) 15 s, e) 20 s, f) 25 s, g) 35 s, and h) 45 s etching in 0.5 M H_2SO_4 solution at 30 °C and 4 V anodic voltage.

for 35 seconds. The result is not as good as obtained for sharpening the nickel wires. Figure 5.6 b) shows the microelectrode tips after etching. The top of the probes are rounded but are not very sharp. In addition, the nickel probes are shortened considerably.

There are two differences between sharpening a nickel wire and sharpening a microprobe. The first difference is that the nickel wire has nearly one-dimensional structure that can tolerate shortening. On the other hand, the microprobes are already short in height and can not tolerate further shortening for an elongated etch process. The second difference lies in the property of the nickel material. The electroplated nickel microprobes usually have granular feature with grains ranging from a few nanometers to a few micrometers in diameter. In comparison, the commercial nickel wire is usually formed to have mostly elongated grains. Hence, the latter probably ends up with a denser structure containing fewer grain boundaries. Grain boundary is essentially a two-dimensional defect, which makes it prone to etchant attack. Consequently, the dissolving rate is greater for the case of electroplated microprobes.

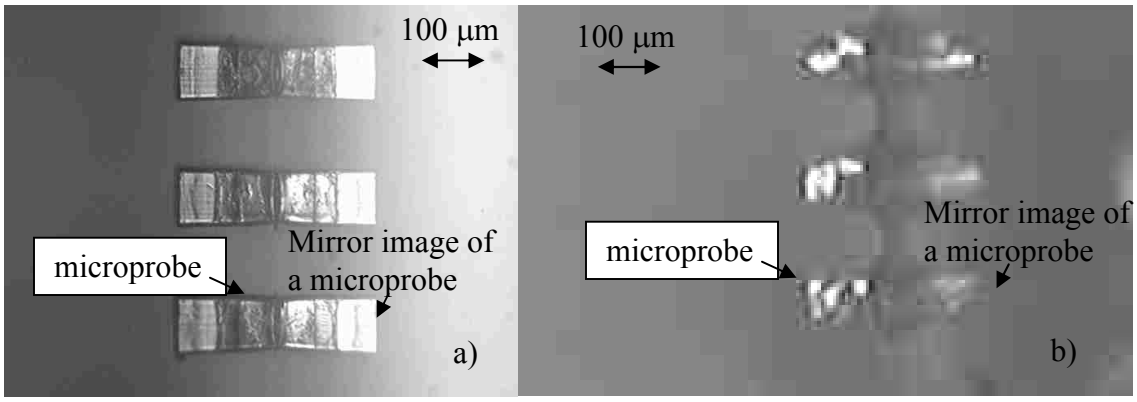


Figure 5.6: Electroplated 200 μm tall, 70 μm wide square nickel microprobes a) before etching and b) after etching. Conditions are same as for Run no. 8 in Table 5.1.

5.5 Summary

In this chapter, sharpening of nickel wire is first attempted as a prelude to sharpening microelectrode tips. Dilute sulfuric acid solution is used as the etching electrolyte. A normal wire orientation scheme is employed here with the nickel wire pointing downward. The air-liquid interface is protected by paraffin wax to avoid wire sectioning due to a faster etch rate at that interface. This approach is different from most of the experimental work reported in literature. A two-level parameter variation experiment was designed by varying temperature, anodic voltage and concentration of acid in electrolyte. It is found that tip sharpening is most effective when all three factors were at their higher levels. This run is then repeated and the tip profile is observed as a function of etching time. The nickel wire became very sharp for etching times of 30 seconds and larger. Another observation was that the wire bulk was also etched simultaneously and that the wire was noticeably shortened. These effects were not as prominent for a set of electroplated nickel microprobes. The microelectrode ends were smoothened but the tips were not very sharp. The etch process needs further improvements to improve microprobe tip sharpening.

Chapter 6. Post-IC Monolithic Integration

6.1 Introduction

As stated in Section 1.1.1, integrated microsystems are usually categorized as either hybrid or monolithic. In the case of monolithic integration, MEMS devices and circuitry are both constructed on a single substrate so that physical compactness and superior functional performance are realized. The easiest approach is hybrid where the CMOS and the MEMS are fabricated independently and mounted on a common substrate. Wire bonding or flip-chip technology is utilized for electrical interconnections. The advantage of this option is that there is no MEMS-related contamination on the CMOS component. One disadvantage is that the signals have to now go through the bonded pads and wires and their associated parasitic capacitances and resistances. This may cause problems in signal integrity especially in high frequency applications. There are some other potential reliability problems associated with wire-bonded systems such as debonding of wire from the substrate and fracture of ball bumps.

Like the pre-IC and the co-IC microstructure fabrication approaches, the post-IC approach does not mandate any specific requirement on the IC fabrication process. However, the latter approach does not compromise on the choice of microstructure material and properties. This makes it possible to build high-aspect-ratio structures side by side or on top of the IC circuitry on the same chip. However, special care is needed to avoid damage to aluminum interconnect contacts and to preserve CMOS circuit performance during the post-IC approach. Most importantly, low temperature and benign chemical and radiation treatments are essential. Problems that limit MEMS fabrication to low temperature in the post-IC approach include the reliability of the aluminum metallization if temperature in excess of 450 °C is utilized. Higher temperature also enhances outward diffusion of various implants and other impurity profiles used during IC fabrication. The post-IC process has worked well with some designs, such as the Texas

Instrument's DMD (Digital Micromirror Device) for the digital light projection system [6.1]. After the 0.8 μm, two-level metal CMOS process for IC circuit fabrication is completed, the MEMS process comprising of several metal layers are formed by deposition and etching to get the needed patterns. Texas Instruments has developed a low temperature surface micromachining process specifically for the DMD. This process preserves the performance of the CMOS circuitry, and requires a custom MEMS process that does not incorporate standard surface micromachining steps. The most affected CMOS transistor component in their process includes the p^+ source-drain implant due to mobile nature of B or BF_2. Another step in their process that needs low temperature considerations during MEMS fabrication is the threshold voltage adjustment implant.

Post-IC integration approach takes advantage of the readily available CMOS foundry services and is employed in this work. The processing temperatures in our post-IC monolithic integration work has been held to less than 100 °C which is well below 450 °C threshold normally used to avoid degradation of the aluminum interconnects. The chemicals used throughout the process are IC-compatible including photoresists, solvents and resist developers for mold fabrication, and the nickel sulfamate electrolyte solution used during electroplating. A KOH based silicon bulk etchant is also used during formation of a chip rest chamber in our process. However, there was no contact between this chamber and the topography on the IC chip and in addition there was a thin photoresist layer present to separate the IC chip from this chamber. X-ray exposure is excluded here in order to avoid damage to CMOS circuits even though this work involves high-aspect-ratio structures. A readily-available UV light source is used instead for resist exposures. High-aspect-ratio microstructures have been integrated on application-specific IC (ASIC) chips designed at LSU and fabricated by an IC foundry. The process flow for chip-level monolithic integration process developed and utilized in this work is shown in Fig. 6.1. It must be noted here that a manufacturing environment calls for wafer-level

processing and not chip-level processing. The former is actually easier to accomplish. However, in university environment, because of practical and cost requirements, one needs to carry out chip-level processing. Hence, it is necessary to develop the chip-level processing steps as well.

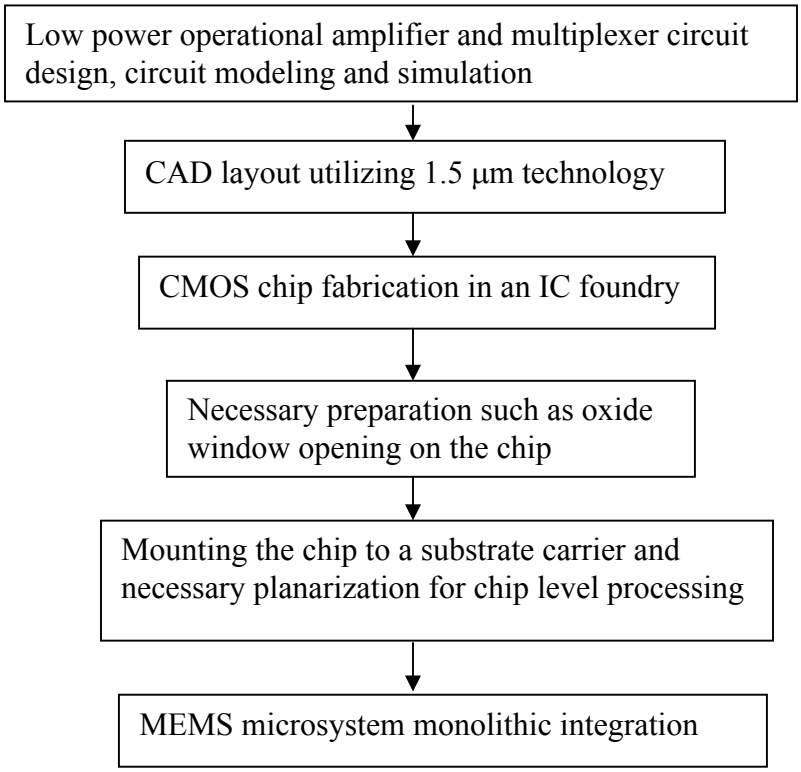


Figure 6.1: Chip-level post-IC fabrication sequence outline utilized in this work for monolithically integrating high-aspect-ratio microstructures with CMOS circuitry.

In order to develop the process, microprobe fabrication is first optimized on a silicon wafer without CMOS circuitry. After the process is fully developed for wafer-level integration, a chip-level integration process is next developed. The latter is first carried out on a scribed silicon wafer piece with similar thickness as that of the IC chip. This scribed wafer piece is seated on a carrier wafer, and the connection between this test chip and carrier wafer is enabled by an electrical bridging step. Finally, monolithic integration is carried out on a fabricated CMOS IC chip after these steps have been fully developed individually.

6.2 Substrate Cleaning

A silicon wafer used as a substrate is ready for use if it is just taken out of its package received from a vendor. If the wafer has been exposed to air for significant time or contaminated, it is treated by a standard RCA cleaning process before use. The standard RCA cleaning process used in this work is given in Table 6.1 [6.2]. It is performed on a wet bench in the chemical treatment room in the Electronic Material and Device Laboratory (EMDL) at LSU.

Table 6.1 Standard RCA cleaning process [6.2].

Step #	Treatment	Temperature and Time	Purpose
1	H_2SO_4/H_2O_2 2:1	120 °C, 10 min	Strips organics and metals especially some photoresists
2	H_2O/HF 20:1	Room Temp., 1 min	Strips chemical oxide
3	DI water rinse	Room Temp.	Removes carryover chemical residues
4	NH_4OH/H_2O_2/DI water 0.5:1:5	85 °C, 10 min	Strips organics, metals and particles
5	DI water rinse	Room Temp.	Removes carryover chemical residues
6	HCL/H_2O_2/DI water 1:1:6	85 °C, 10 min	Strips alkali ions and metals
7	DI water rinse	Room Temp.	Removes carryover chemical residues
8	Spin dry in N_2 ambient	Room Temp.	Removes water molecules

6.3 Wafer-Level Integration

A very limited number of foundry fabricated IC chips with CMOS circuitry are available in this research because of cost. Hence, probe fabrication process is developed and optimized on a separate silicon wafer. Once the process is optimized, it can then be applied for monolithic integration with CMOS circuitry.

6.3.1 Processing Steps

A wafer-level post-IC fabrication process is illustrated in Fig. 6.2. A p-type (100) silicon wafer is used as the substrate. First, a positive tone photoresist S1813 (from Shipley) about 2 μm thick is spun on the wafer and processed by UV lithography to open probe areas as indicated in Fig. 6.2 a). A thin layer of Ti about 50 nm thick is then sputtered as an adhesion layer. A 0.2 μm thick aluminum layer is thermally evaporated uniformly on the wafer to simulate the metal interconnect layer in the IC chip as shown in Fig. 2.3. This is followed by sputtering another thin layer of Ti about 50 nm as an adhesion layer and a Cu layer about 0.5 μm thick as a seed layer as indicated in Fig. 6.2 b). The combination of Ti/Al/Ti/Cu serves as a base over the Si-substrate for Ni electroplating. Ti and Cu layers are deposited by sputtering in an Edwards 200 deposition system. The sputter rate on a clean silicon wafer is 11 nm/min for Ti, and 16 nm/min for Cu utilizing a rotating substrate holder. Aluminum evaporation is performed in an Applied Materials thermal evaporation system. A thick SU-8 50 photoresist is then spun on the substrate followed by UV exposure and development as indicated in Fig. 6.2 c). An electroplating mold is formed in this thick SU-8 50 resist. Electroplating is then performed followed by mold removal to release the probes as shown in Figs. 6.2 d) and e). A successful electroplating is achieved only if a clean adhesion layer and a conductive seed layer at the bottom of the mold are obtained upfront.

6.3.2 Importance of a Clean Electroplating Base Layer

A clean electroplating base is needed in order to obtain electrical conduction between the seed layer and the electrolyte. A regular development and cleaning process includes SU-8 developer immersion followed by rinse in isopropyl alcohol. If organic debris remains on the top of the metal seed layer following this process, it can lead to a high resistive barrier for electroplating. This has resulted in poor deposition or even no deposition, as is shown in Figs.

6.3 and 6.4. A magnified view of a nickel grain cluster formed as a result of unclean seed layer surface is shown in Fig. 6.5.

A clean electroplating SU-8 mold has been obtained by judiciously tailoring the prebaking time, temperature ramp cycle, UV dose, and post exposure temperature/time cycle, cooling time duration and use of proper development techniques such as development at an elevated temperature with stir assistance. The proper processing steps utilized in this work are given in chapter 3. As a result, this problem of organic debris has been eliminated.

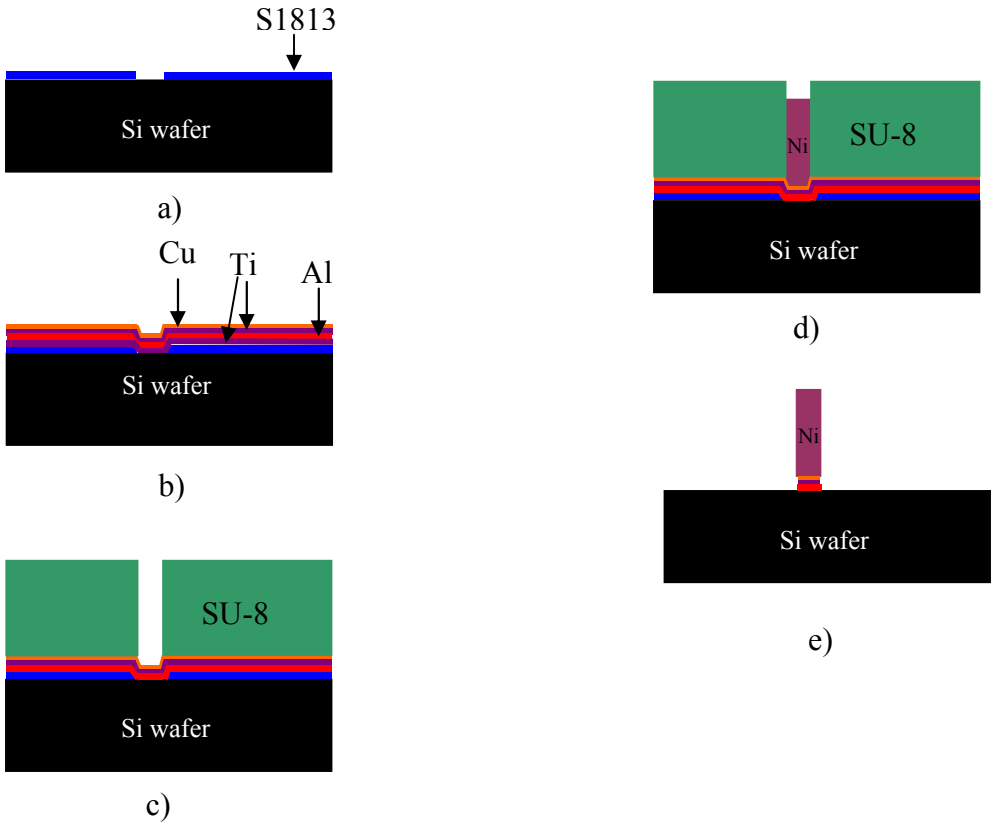


Figure 6.2: Wafer-level post-IC fabrication process. Individual steps are described in the text.

6.3.3 Problem with Al Layer

In the first version of fabricated IC chip received from the foundry, the top level Al interconnect also covered the probe pad areas. Figures 6.6 a) and b) respectively show the chip

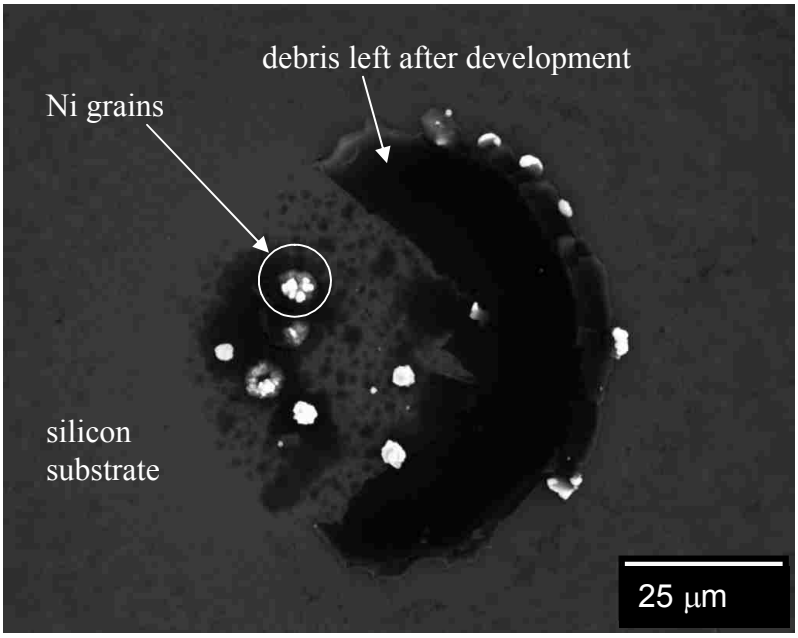


Figure 6.3: Poor electroplating result due to the electroplating base layer not being completely clean over the probe areas following the resist development.

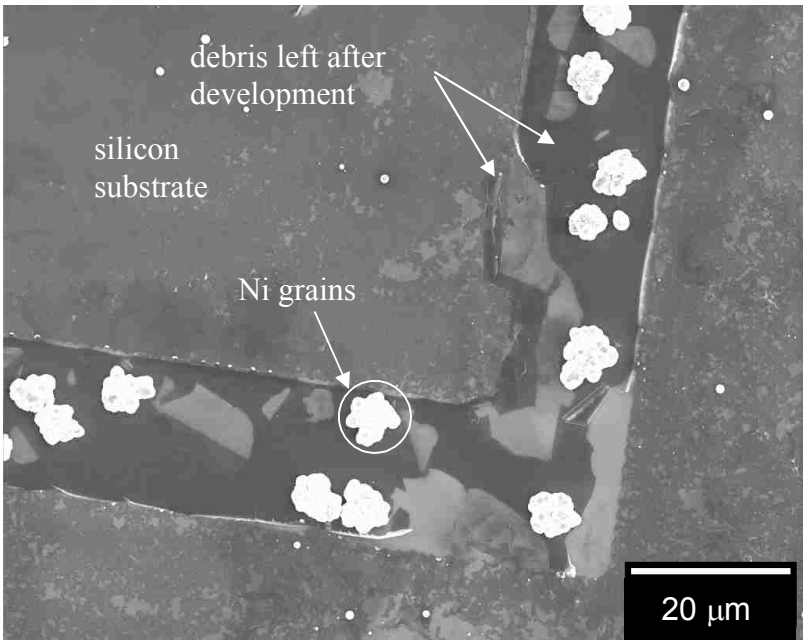


Figure 6.4: Poor electroplating result due to unclean electroplating base over the alignment mark areas.

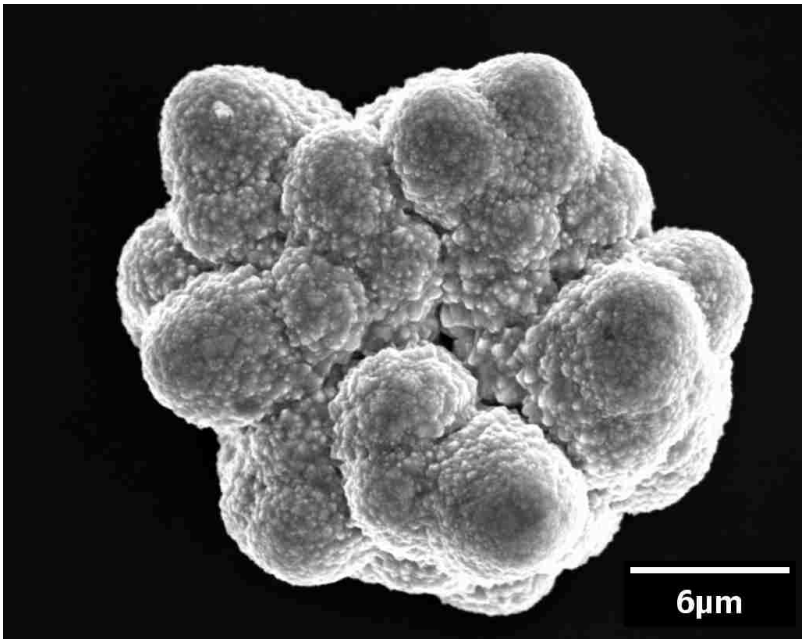


Figure 6.5: A detailed look at a Ni grain cluster resulting from unclean seed layer surface inside the electroplating mold.

design concept and the fabricated chip. Figure 6.7 a) is a photo-micrograph of a probe set, that follows the fabrication steps shown in Fig. 6.2. The probe sizes are same as those specified in Chapter 2 and probe height is about 50 μm. A closer view of a microprobe in Fig. 6.7 b) shows that connection between the bottom of the probe and the substrate is not continuous. Taller probes had a tendency to fall down during the SU-8 mold removal because of this poor connection. Various techniques were attempted to solve this problem. For example, annealing treatment on the interface between the Al and the silicon wafer was carried out below 400 °C. Another technique of zincating the Al surface was also tried. However, none of these techniques succeeded in improving adhesion of the posts to the substrate. This problem was finally attributed to a thin native oxide present on top of the Al layer which in turn weakened the adhesion of aluminum with additional metal layers.

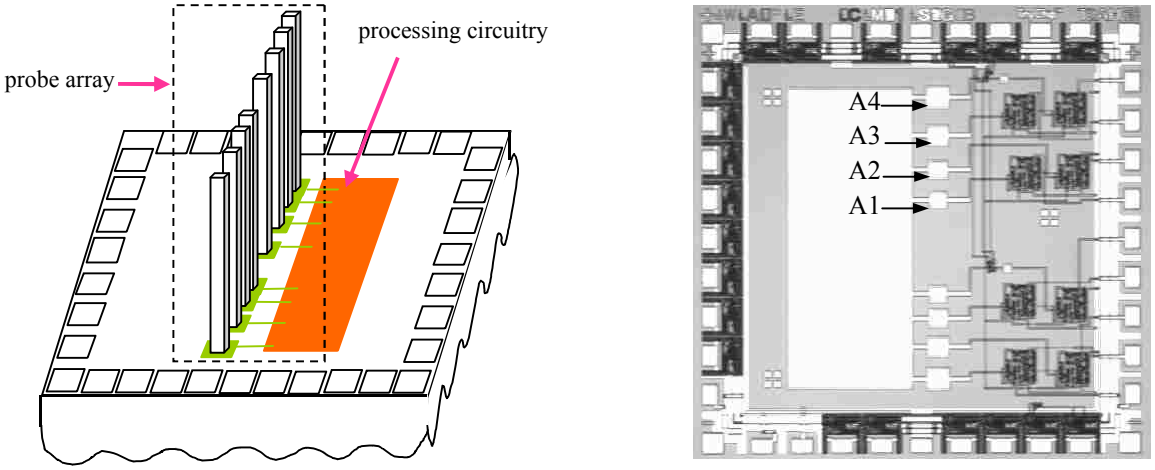


Figure 6.6: a) A conceptual chip design diagram that shows a linear array of the microelectrode posts to be integrated on a CMOS chip b) Photo-micrograph of a fabricated CMOS test chip prior to post-IC fabrication of linear electrode array.

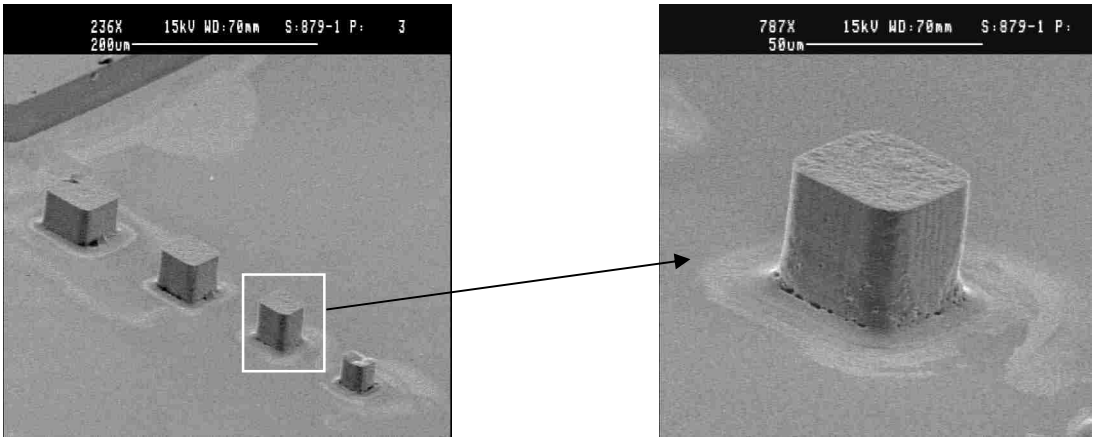


Figure 6.7: a) Photo-micrograph of a fabricated microprobe array of varying dimensions and spacings. b) Details of a single microprobe.

In order to solve this problem, a second version of the IC chip was designed in which the Al layer was absent from the probe areas as stated earlier in chapter 2.

6.3.4 Alternative Approach without the Al Layer

In this alternative approach, the Al that covered the probe areas in the earlier version is absent as there is no metal layer specified in the square bottom probe pad areas during the IC chip fabrication. Instead, heavily doped n^+- silicon is utilized as a conductor. The Al lines connecting between these squares and the amplifiers in the first chip are replaced by heavily doped n^+- regions as well. As before, probes are fabricated on a separate silicon wafer for process development first. The process is the same as shown in Fig. 6.2 except the Al layer deposition shown in Fig. 6.2 b) along with the Ti layer below it are missing. An n^+- doped (100) wafer is used to simulate the n^+- doped probe areas. Ti layer about 50 nm thick and Cu layer about 500 nm thick are sputtered as adhesion and seed layers, respectively. A 250 μm thick SU-8 layer is spun on silicon substrate and processed to have windows open for probes. Developing SU-8 with large exposed areas at room temperature has resulted in cracks in the photoresist because SU-8 becomes heavily cross-linked after the post-exposure-bake. This generates considerable stress in the photoresist itself and at the interface between the photoresist and the silicon wafer. On one hand, this stress is released during development resulting in cracking of resist. On the other hand, the SU-8 developer absorbs heat from both the resist and the substrate as it evaporates which causes a thermal stress due to different heat transfer rates and different temperature coefficients of expansion. The most serious case for room-temperature developing may result in SU-8 completely detaching itself from the wafer. Applying an adhesion promoter layer or primer complicates the process by adding another lithography cycle and a dry-etch cleaning step. Avoiding this cracking problem can be achieved by clever mask design which divides the large exposed area into smaller partitions, developing at an elevated temperature,

careful heat treatment and slow cooling after pre-bake and post-exposure-bake at 96 °C. In this work, resist development is performed at a 55 °C, which gave optimum results. Electrolyte for electrodeposition is nickel sulfamate, and plating is carried out under a current density of 4 mA/cm^2 at 53 °C, and the plating rate is about 2 μm/hr. An SEM probe image is shown in Fig. 6.8. The probe side width is 70 μm and the height is 210 μm giving an aspect ratio of 3:1. It is seen that the removal of Al layer has improved the standing probe height significantly implying superior adhesion to the substrate. Details of the process can be found in sections 3.2.1 and 4.2.

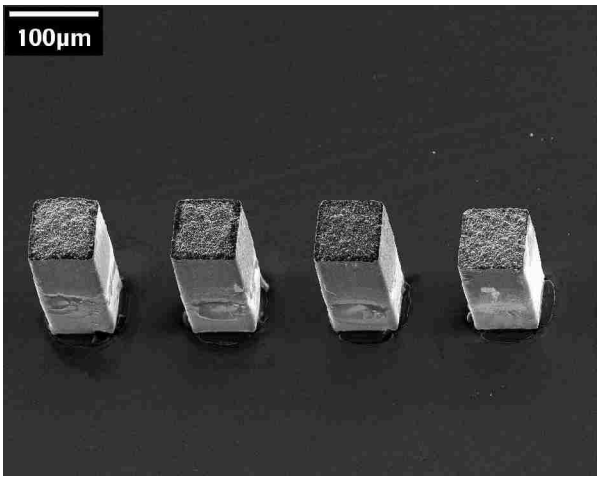


Figure 6.8: An electroplated nickel probe array 210 μm tall and 70 μm wide.

6.4 Chip-Level Integration

Wafer-level integration is desired for mass production in semiconductor industry where one wafer is diced into individual chips after the process is complete. However in a university setting, this is often not practical due to high cost involved for a wafer-level process since only a few chips are needed for research purposes. In order to fulfill research needs in a university laboratory setting with limited resources, chip-level integration is usually necessary [6.3]. Hence, a chip-level process is developed in this work to integrate microprobe arrays onto an unpackaged CMOS IC chip.

6.4.1 Surface Micromachining Approach

To carry out integration, a surface micromachining type approach was first attempted in this work. Surface micromachining is an add-on process. It does not involve bulk etching. Additional layers are processed atop the chip substrate one by one. This process is schematically described in Fig. 6.9. It starts with a silicon wafer, which serves as the chip support. The type and grade of this support wafer are generally not critical. A 250 μm thick SU-8 layer is spun on the wafer and processed to open a mold for the chip as indicated in Fig. 6.9 a). The fabricated IC chip thickness is 250 μm and its size is 2 mm × 2 mm. The SU-8 mold is slightly larger than the chip to guarantee an easy placement of the chip. A very small amount of the same type of SU-8 is applied at the bottom of the mold that serves as an adhesive and the chip is placed into the mold sitting on top of the adhesive as indicated in Fig. 6.9 b). After this, a thin layer of photoresist HR200 is spun on the wafer and windows are opened over the probe areas. Ti/Cu is sputtered on HR200 as shown in Fig. 6.9 c) followed by another thick SU-8 layer spin-coat. The latter is processed to form the electroplating mold as shown in Fig. 6.9 d). Electroplating is then performed as indicated in Fig. 6.9 e). Figure 6.9 f) shows the final integrated microsystem after all the remaining layers are stripped off in a suitable processing sequence and after the fabricated microsystem chip is detached from the silicon support wafer.

The process described above was implemented on the initial chip design shown in Figs. 2.3 and 2.4. In Fig. 6.10 a), the Al pads have been selectively removed from the chip in order to eliminate the problem due to native aluminum oxide and HR200, Ti and Cu have been applied to the chip. In Fig. 6.10 b), the microprobe molds are defined in SU-8 photoresist. A problem was encountered during nickel electroplating in that nickel could hardly be plated inside the mold recess. The suspected likely cause include the poor electrical connection between the chip and the wafer perhaps due to the gap between them, or due to deterioration in the metal layer

sandwiched between two thick photoresist layers during resist heating cycles. In the former case, a 250 μm deep gap is regarded as a suspect in retaining the continuity of the metal layer coating deposited by conventional sputtering. In order to solve this problem, different types of materials were used to fill the gap including paraffin, black wax and SU-8 photoresist but none of them yielded good results. A surface profiler check across the gap after being filled showed sharp kinks and valleys which indicated a difficult challenge to obtain a continuous metal coating across the gap. The choice of SU-8 photoresist as a chip mold was not seen to be appropriate either after careful examination of the fluidic property of SU-8 photoresist. There is a heating cycle necessary at 96 °C on the chip mold photoresist during the processing for the probe mold. This can cause slight reflow in the chip mold photoresist after its glass transition temperature is reached and this can potentially break the electricity continuity. The glass temperature of SU-8 is reported to be about 55 °C which is much lower than 96 °C [6.4]. Either or both of these two possible mechanisms may block the current flow into the probe molds and stop the electroplating process. Therefore, a new choice of chip mold material and a new electrical bridging technique have to be developed.

6.4.2 Tape and Wire Bonding Technique

A novel technique of using a tape and gold bonding wires is developed in this work to overcome the electrical continuity problem mentioned above in section 6.4.1 for chip-level integration. This technique showed significant improvements. In this approach, no gap filling material is utilized. Monolithic integration with this technique is first practiced on a diced chip without any CMOS circuitry. This chip is diced from a 275 μm thick wafer that has approximately the same thickness as the 250 μm thick CMOS IC chip.

The process flow is schematically shown in Fig. 6.11. The first several steps are the same as described in Figs. 6.9 a) - b). After mounting the chip into the SU-8 mold and processing of

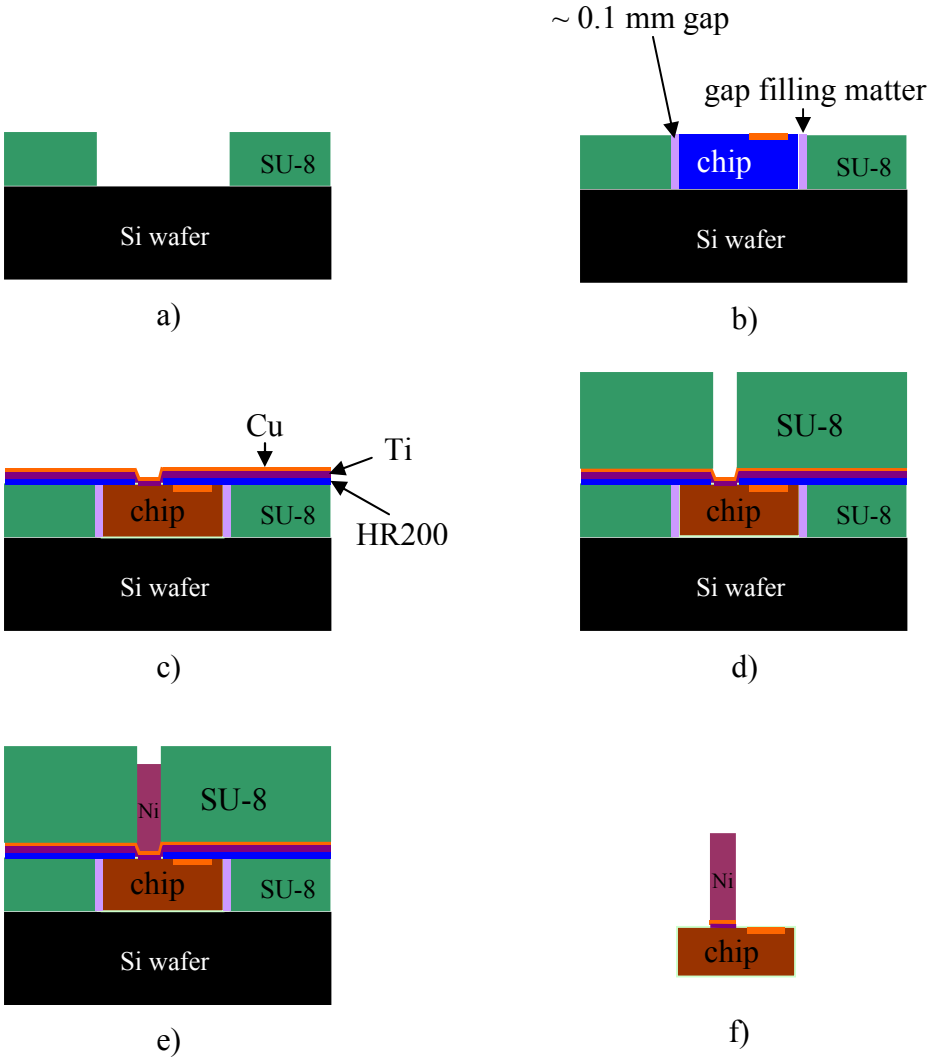


Figure 6.9: A possible process for chip-level probe integration.

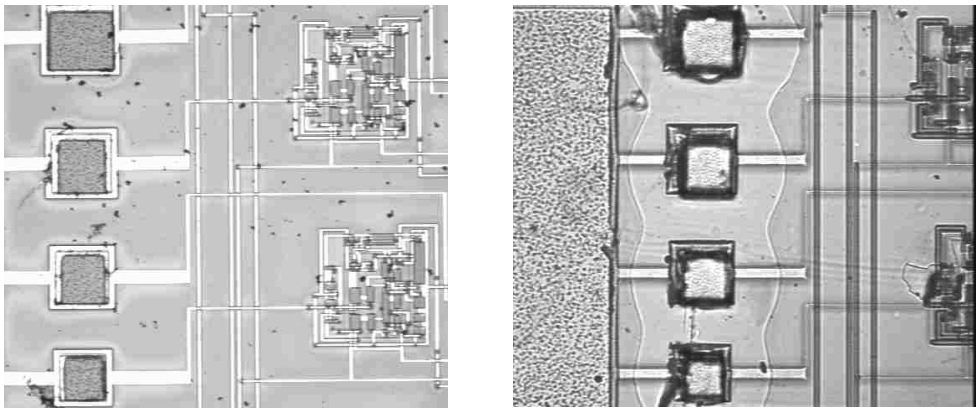


Figure 6.10: a) Photo-micrograph with Al pads removed and with delineated HR200, Ti and Cu layers. b) SU-8 microprobe molds on the chip.

the photoresist HR200, Ti and Cu layers are sputter-coated. In order to obtain a better adhesion between the electroplated microprobes and the substrate, the substrate is bombarded by Ar plasma for a short time as a cleaning step prior to seed layer metallization. This also slightly roughens the substrate before seed layer application to improve adhesion. Multiple gold wires 1 mil in diameter are laid out parallel to each other on the side of a wafer masking tape with adhesive. Then the tape with adhesive is carefully placed on Cu layer facing down intending to electrically bridge between the chip and the top of the support wafer. The tape used here is called "wafer disc" (Harman International), which is specifically used for partial masking of wafer during processing. The thickness of tape is about 80 μm. After this, the whole piece is placed in oven at 96 °C and held there for 10 min. This is for removing any air bubbles that may have been trapped underneath the tape. If this short baking cycle is not performed, bubbles are observed to slip out and roughen the second SU-8 layer atop that is spun on in a later step. After opening windows for the microprobes, Ni is plated into the mold to form the probes.

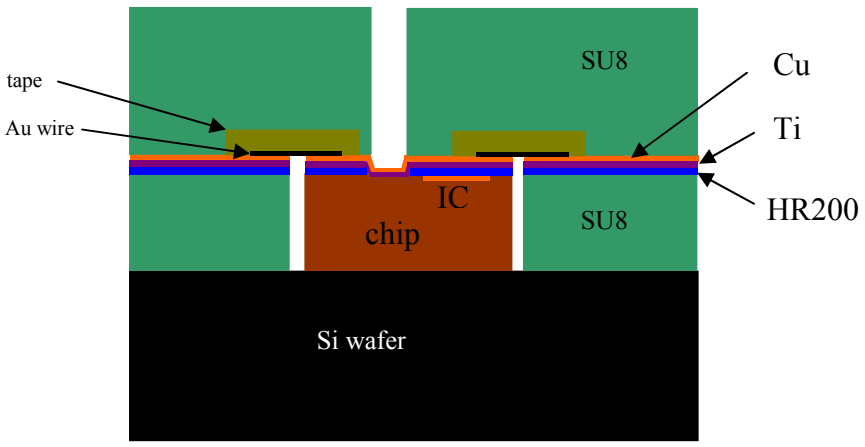
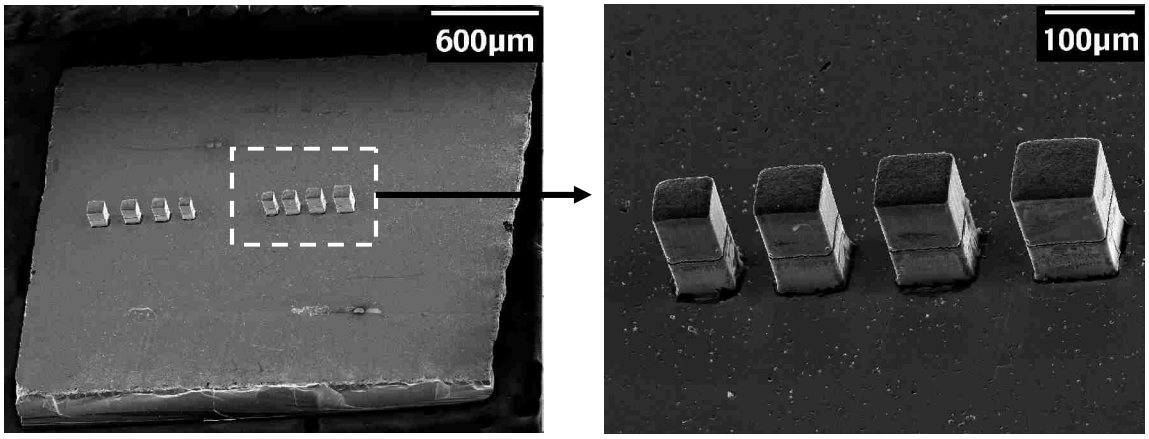


Figure 6.11: A schematic diagram showing the details of the process developed for chip-level integration of microprobes using a tape and wire bonding technique.

It should be noted here that this labor-intensive process is not economically suitable for manufacturing. In a manufacturing environment, one needs wafer-level integration and not chip-

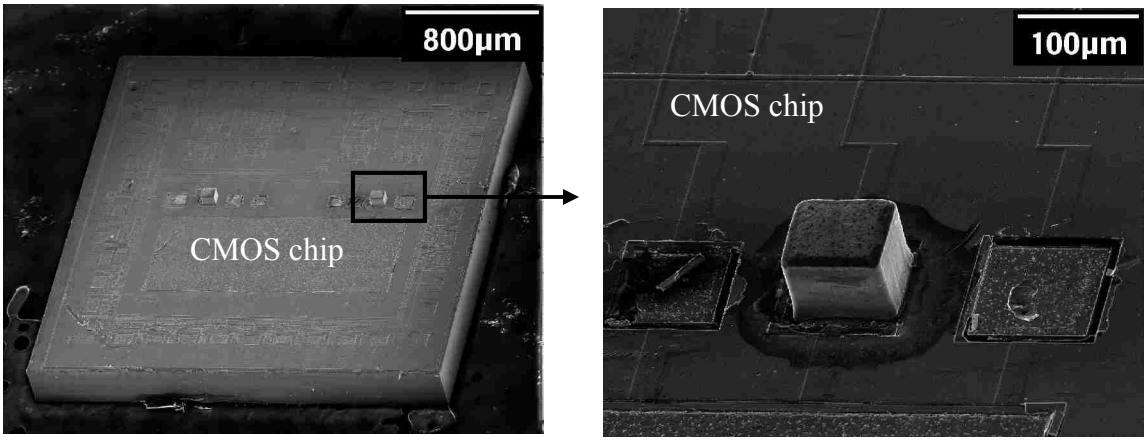
level integration. The basic process developed here is directly applicable to wafer-level integration and is suitable for mass processing applications. However, in a university setting for research purposes requiring several iterations, batch level processing is not practical as processed foundry wafers are prohibitively expensive ($10 k upwards/wafer per iteration) and one has to resort to a practical chip-level integration approach in the absence of access to a local CMOS fabrication capability.

DC plating is employed here under a current density of 4 mA/cm^2, at 53 °C in an electrolyte with PH value of ~ 3.6. Figure 6.12 a) shows eight microprobes standing on a diced chip after the SU-8 mold is removed and the chip is released. The height of the microprobes is about 160 μm and side widths are 70 μm, 60 μm 50 μm, and 40 μm, giving aspect ratios varying from 2:1 to 4:1. Figure 6.12 b) is a closer view of the right four microprobes with smaller spacings. Figure 6.13 a) shows the plating results on an IC chip with CMOS circuitry. After the SU-8 mold was removed, however, only two microprobes remained standing. Figure 6.13 b) is a closer view of one standing microprobes.



a) b)

Figure 6.12: a) SEM picture of electroplated nickel square probes 160 μm high with side widths between 40 μm to 70 μm wide on a test chip. b) An amplified view of the four closely-spaced probes.



a) b)

Figure 6.13: a) A microprobe array on an IC chip with CMOS circuits. b) A closer view of a single microprobe.

6.4.3 Bulk Micromachining Approach

Results in Fig. 6.13 indicate that SU-8 photoresist as the chip mold material may also need to be replaced for generating a smooth current flow path even after employing the novel tape and wire bonding technique. Since a prime grade silicon wafer has an extremely flat surface that unlike SU-8 does not reflow at operating temperatures, it is used next as a chip support. This process is described in Fig. 6.14. First, a (100) oriented p- or n-type Si wafer with thermally grown SiO_2 on the top side is chosen as a substrate carrier as indicated in Fig. 6.14 a). A thin layer of a positive photoresist S1813 is applied and processed to open a window. The size of this window is slightly larger than 2 mm × 2 mm so that the CMOS chip can easily fit within it. One more concern for deciding the size of this window is to accommodate the linear reduction of the window from top to bottom due to the 54.74° angle made by (100) and (111) lattice planes [6.5] following the silicon bulk etch using KOH solution. A buffered oxide etchant (BOE) is then used to etch off the exposed SiO_2. Under room temperature, it takes approximately 10 minutes to etch 1 µm thick SiO_2. After this, the S1813 photoresist is stripped by immersing the entire wafer into acetone followed by a DI water rinse. 1 µm thick thermally grown SiO_2 is used as a mask to etch

bulk silicon at 75 °C in KOH solution comprising of 44g KOH per 100 ml DI water. Silicon etching in KOH solution is anisotropic. The reported etch rate ratio between (100) and (111) lattice planes in KOH solution is 400 : 1 [6.5]. The etching apparatus is designed in our laboratory and is shown in Fig. 6.15. The function of pyrex cover is to restrain liquid evaporation. The magnetic stirring bar is maintained at 150 RPM. During the etching process, no additional KOH pellets are added into the solution to maintain a constant KOH concentration. Therefore, the etching rate is not constant. At T = 75 °C, the initial etching rate is about 1 μm/min. After 40 hours, the etched depth is between 250 μm to 260 μm. So the average etch rate is about 6.5 μm/hr or 0.11 μm/min. The profile of the etched recess is clear and the bottom layer, which acts as a seat for the chip, is smooth. A partially etched silicon recess is shown in Fig. 6.16. Figure 6.17 shows the 54.74 ° angle made by (111) and (100) lattice planes. Figure 6.18 shows the etch depth with respect to etch time.

Surface roughness on (100) lattice plane increases as etchant bath temperature rises. Thermally grown SiO_2 is not an ideal mask for Si bulk etching. Some pinholes are observed across the SiO_2 layer on both front side and backside of the wafer during the etching process, but the bulk portion of SiO_2 mask indeed survived after the long etching process. The next step is to seat the chip into the etched recess. This is done by applying a minimum amount of dilute SU-8 2 photoresist to the bottom of the recess and then locating the chip on this photoresist and lightly pressing with a cleanroom Q-tip. The chip surface now is in level with the surface of the carrier wafer, as shown in Fig. 6.14 b). After this, a thin layer of SU-8 2 photoresist is spun on this wafer and windows are opened over the probe areas, as is shown in Fig. 6.14 c). Figure 6.14 d) shows a thin adhesion layer of Ti that is sputter-coated followed by a seed layer of Cu as the electroplating base. A tape and wire bonding technique described earlier in section 6.4.2 is employed at this time as indicated in Fig. 6.14 e). Next, a thick layer of SU-8 50 is spun on and

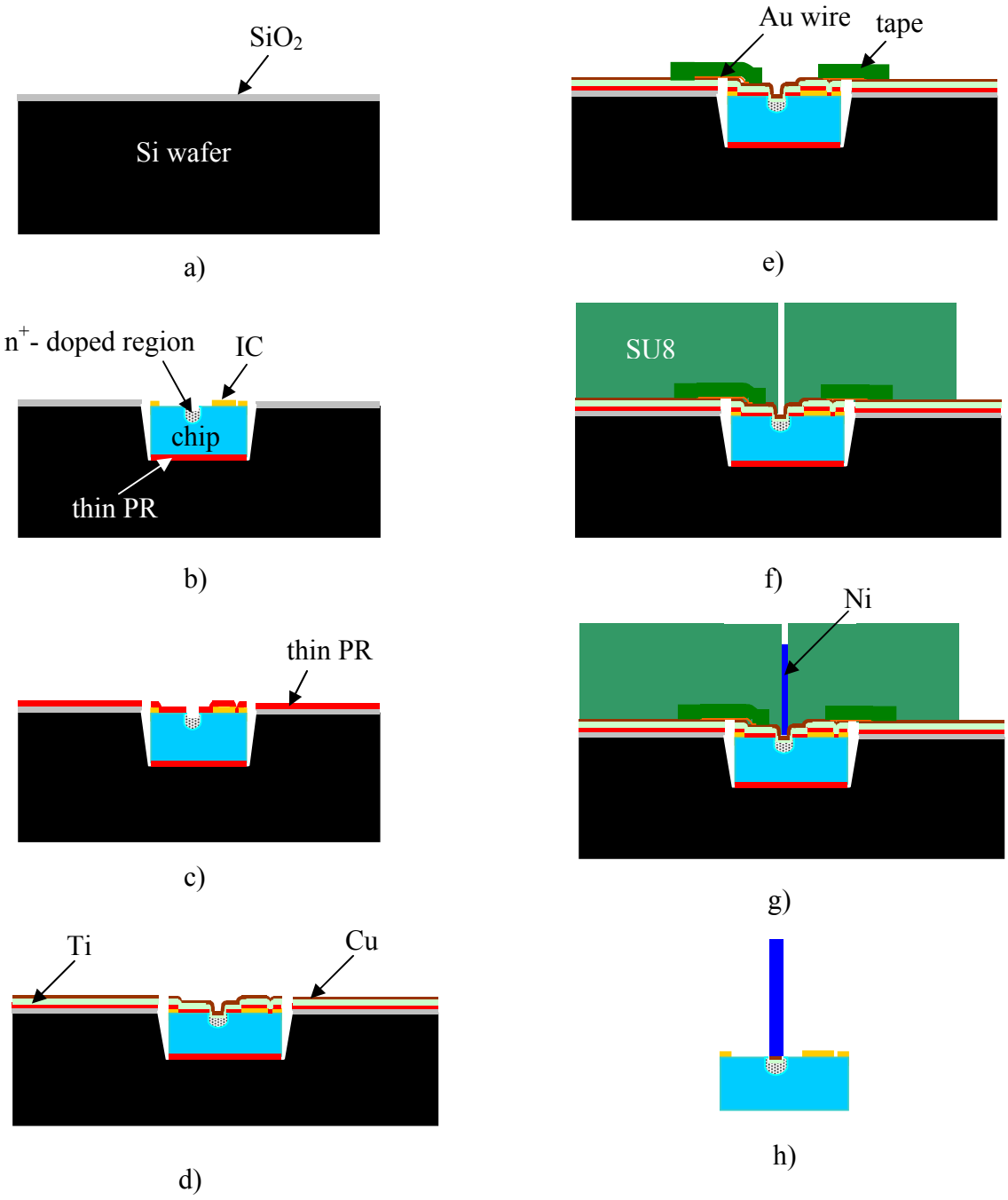


Figure 6.14: Chip-level monolithic integration processing steps utilizing silicon bulk etching technique.

openings are made over the probe areas to form an electroplating mold as indicated in Fig. 6.14 f). Ni is then electroplated into the mold to form the microprobes as is shown in Fig. 6.14 g). The removal of exposed SU-8 photoresist is done by immersing the electroplated piece into Remover PG solution from MicroChem Corp. at 78 °C. This process not only dissolves the thick SU-8 50 photoresist but also dissolves the thin SU-8 2 layer and at the same time lifts off the thin Ti/Cu combination metal layers above it. The released monolithically integrated chip is shown in Fig. 6.14 h).

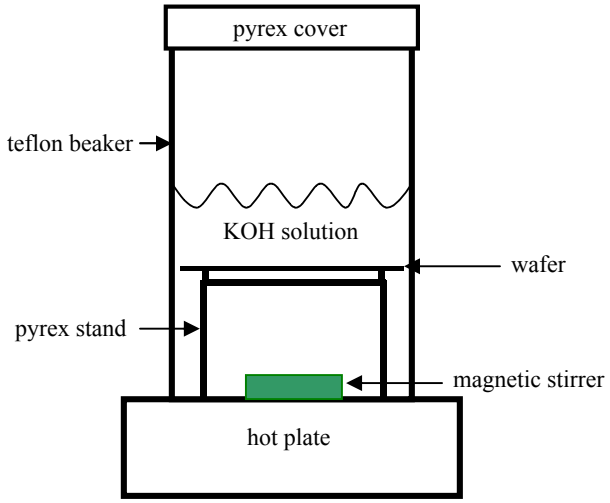


Figure 6.15: Setup for bulk etching of silicon.

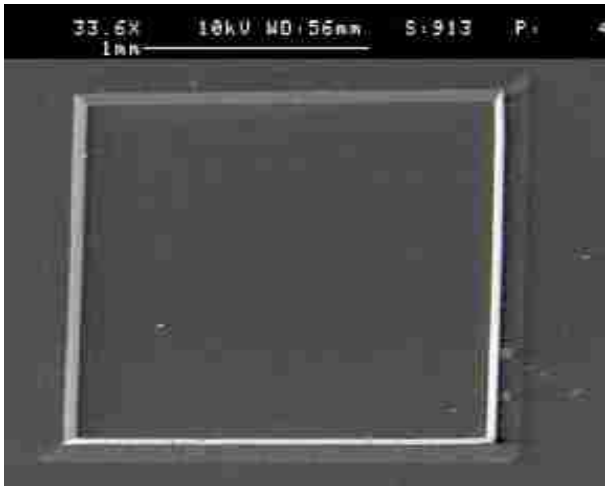
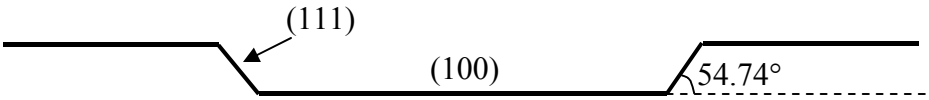
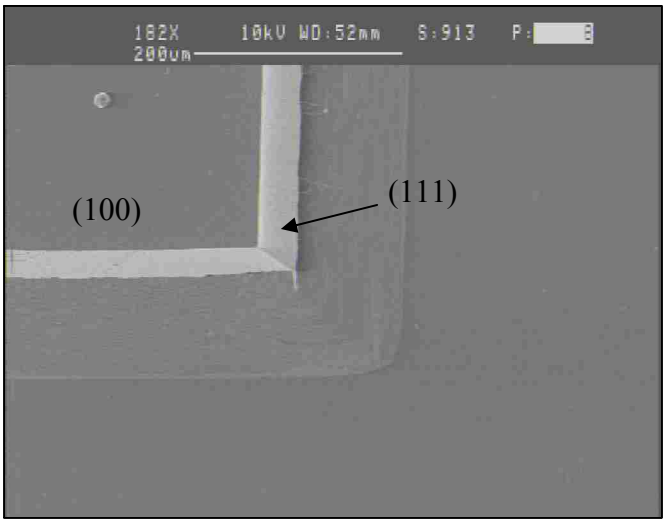


Figure 6.16: Microphotograph of a partially etched silicon wafer to seat the IC chip. The dimension of the recess is 2 mm × 2 mm.



a)



b)

Figure 6.17: a) Anisotropic etch profile on (100) silicon. b) Bulk silicon etch profile after anisotropic etch.

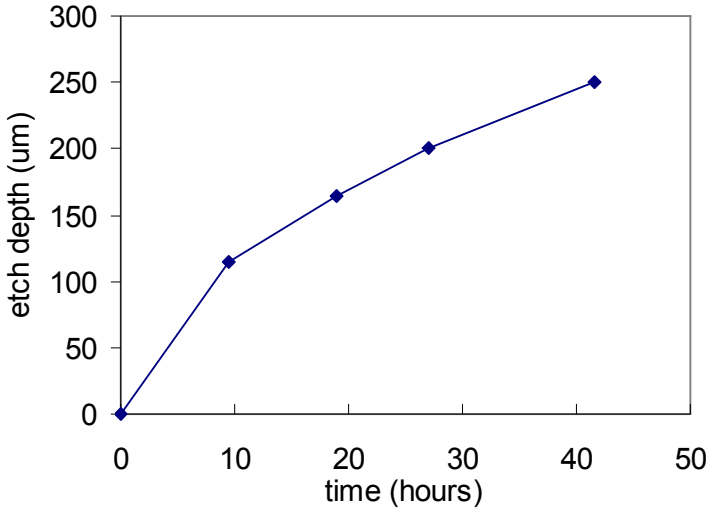
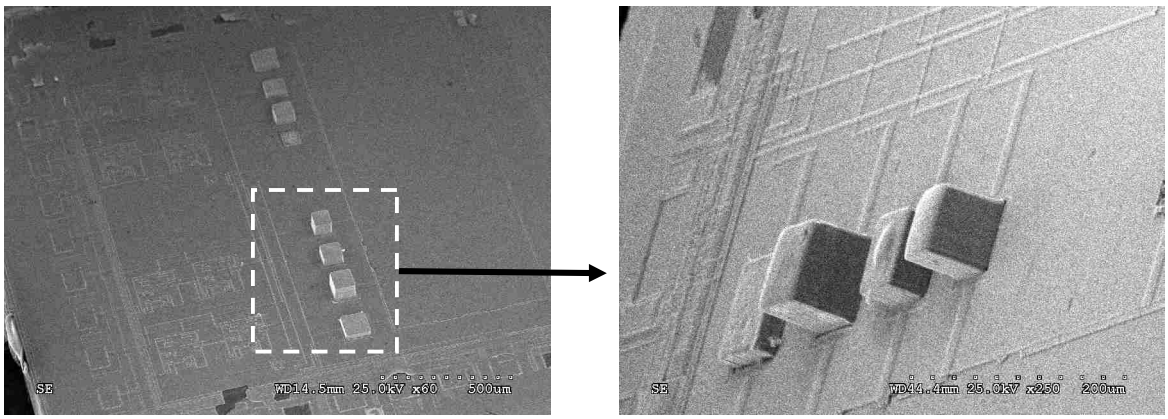


Figure 6.18: Silicon bulk etch depth with respect to etch time in a KOH bath at 75 °C.

Employing the technique described above, probes were first fabricated by DC plating onto a CMOS IC chip. The plating current density is 4 mA/cm^2 in an electrolytic bath at 53 °C with pH value of approximately 3.6. All microprobe recesses are plated with nickel which demonstrates a significant improvement compared to those yielded from the surface micromachining based approach as described in section 6.4.1. However, DC electroplating resulted in uneven probe heights, as shown in Fig. 6.19. This difference indicates different electrodeposition rates at different areas on the chip and may be a result attributed to the chip topography. The roughness of the CMOS chip surface is measured to confirm this hypothesis by an optical surface profiler and the result is shown in Fig. 6.20. It is seen that the total surface roughness of a commercially fabricated as received CMOS chip can be over 3 μm peak-to-peak with narrow bumps and sharp kinks. This roughness may be caused by field oxides and other IC features.



a) b)

Figure 6.19: a) SEM picture of electroplated nickel probes with various height and widths on a chip with CMOS circuitry. b) An amplified view of four such probes.

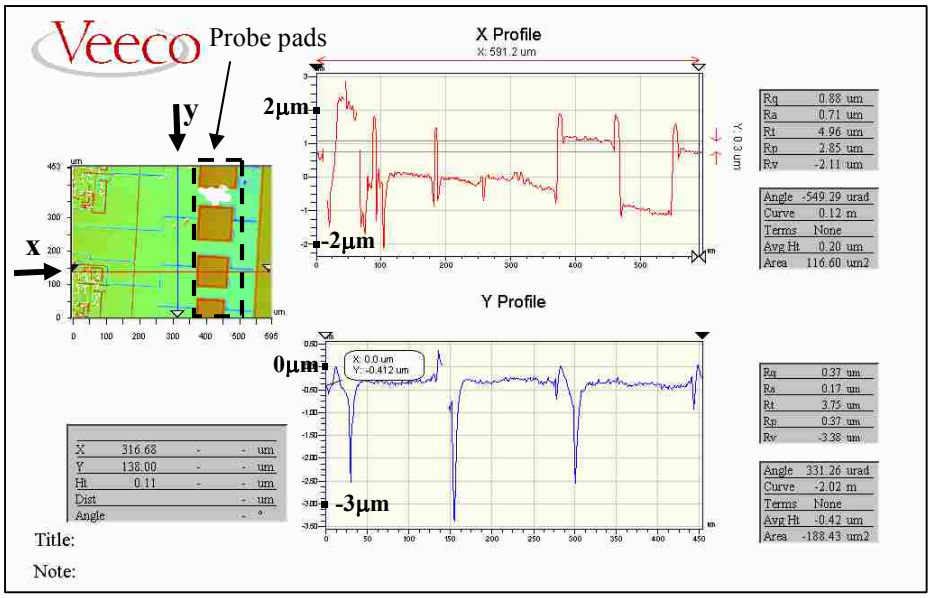
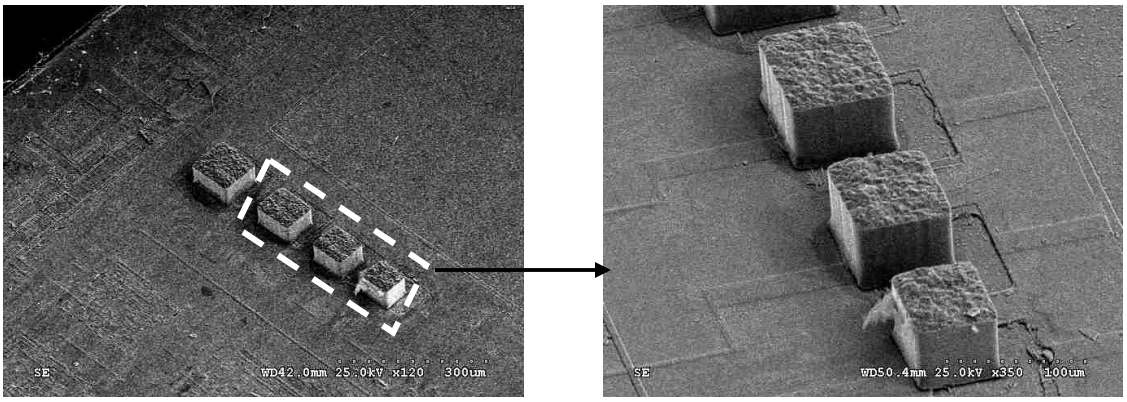


Figure 6.20: Surface roughness of a CMOS IC chip measured using an optical surface profiler. The total surface roughness is over 3 µm.

Pulse plating is then employed on the CMOS chip in order to reduce the built-in stress and solve the problem of uneven probe heights. As described in section 4.4, unlike the case for DC plating, the cathodic current in pulse plating is supplied during t_{on} and no current or only a minimal cathodic or anodic current flows during t_{off}. The existence of t_{off} provides a time during which the cations at the interface of cathode and the electrolyte that may have been largely consumed during the t_{on} period to be replenished from the electrolyte bulk. This can suppress side reactions and improve the quality of deposition. During off time, the plating current is not completely off, as the double layer discharging current now continues the plating process. During this period, the effect of non-uniform ohmic drops due to chip topography and differences in recess mold sizes are mitigated thereby resulting in more uniform deposit over the chip area.

At bath temperature of 53 °C and similar pH value of approximately 3.6, current density of 100 mA/cm^2, pulse durations t_{on} of 10 seconds and t_{off} of 15 seconds are employed during electroplating. This resulted in deposition rate of 0.7 μm/min yielding a 70 μm tall probe array in 100 minutes. This is shown in Fig. 6.21. The probe height is now uniform. For complicated cathode topography such as the microprobes on a CMOS IC chip employed in this work, pulse plating technique yields a microprobe array with more uniform height compared to that resulting from DC plating case attributed partly due to the discharging current of the double layer during off time.



a) b)

Figure 6.21: a) A probe array on a CMOS IC chip formed by pulse electroplating. b) A close view of the same probe array.

6.5 Summary

A novel monolithic integration approach to integrate high-aspect-ratio microstrucutres with CMOS circuitry is explored in this work. The processing steps are carefully tailored to accommodate the post-IC process. These include low temperature processing below 100 °C, chemical treatments in benign ambient and no exposure to detrimental radiation. The CMOS chip design has undergone two iterations. The presence of aluminum at the probe base bottom caused contact problems during nickel electrodeposition in the first version of the CMOS chip.

In the second version, aluminum is replaced with n^+- doped silicon which has resulted in a stronger adhesion between the bottom contact layer and the nickel microprobes.

Processing steps for wafer level integration were first developed. Next, a chip-level integration process was developed. Diced silicon wafer pieces with size and thickness similar to the designed CMOS chip were utilized first to develop the integration steps prior to their application to the CMOS chip. Techniques akin to surface micromachining were first employed in which a thick SU-8 layer was used as a chip carrier. However, MEMS integration was not successful probably due to the reflow nature of SU-8 resist at higher processing temperatures. The latter can break the continuity of the metal layer so that a current passage from cathode to the base of microprobe can be effectively blocked. An alternative integration technique was then introduced which took a bulk silicon micromachining approach. Compared to polymer, silicon as a chip carrier is much more robust and does not cause a physical break of metal layer on top of it. However, this approach results in a fragile connection between the CMOS chip surface and the carrier wafer surface due to the gap around the CMOS chip. The latter was leveled with the carrier wafer with the help of a resist material which also filled this gap. This resist can also cause reflow at higher processing temperatures and can break the metal layer continuity over the gap area. This problem was solved by developing a so-called tape and wire bonding technique that is first introduced in this work. This technique was successfully utilized for electroplating on a CMOS chip. However, perhaps due to surface topographical features present on a fabricated CMOS chip, the electrical continuity varied from one microprobe area to the next resulting in uneven heights of the electroplated microprobes for the DC electroplating case. Use of pulse electroplating significantly reduced this problem with formation of uniform tall microprobe arrays. This work has successfully integrated tall high-aspect-ratio microstructures with CMOS IC chip monolithically.

Chapter 7. Summary, Conclusions and Future Work

In summary, a processing technology to monolithically integrate a microsystem with CMOS circuitry has been developed in this work. A microsystem has been designed, developed, fabricated and integrated with a CMOS chip utilizing a post-IC approach. The test vehicle selected to demonstrate this monolithic integration process is a microsystem comprising of a nickel microprobe array electroplated on an IC chip with corresponding signal processing circuitry. A potential application of this microsystem is to record neural signals of the central nervous system.

Monolithic integration is employed in this work to couple CMOS signal processing circuitry with a functioning MEMS structure taking advantage of reduced parasitic resistance, capacitance and inductance associated with wire bonding and extra packaging that are inherent in the hybrid integration technology. This is especially important when the amplitude of signal is small and the background noise level is high as in the case for measuring neural signals. A system level design of a metal microprobe array with a lab-designed CMOS chip is described in Chapter 2. The dimension of a CMOS chip in this work is 2 mm × 2 mm × 250 μm. The sizes of square microprobes vary from 40 μm to 70 μm on each side with an increment of 10 μm. The spacing of the microprobes also varies from 125 μm to 195 μm. The size and spacing of the microprobes are selected such as to be comparable to the size and spacing of pyramid neurons in the central nervous system of primates.

Post-IC approach is employed in this work. Compared to pre-IC and co-IC approaches, the former takes the advantage of the readily available CMOS chips from IC foundries. In order to prevent detrimental impacts to CMOS circuitry, the processing temperature has been maintained lower than 100 °C and benign chemical treatments are considered so that metal interconnects and silicon oxide dielectrics on the CMOS chip are not damaged. UV light source

is utilized to process all photoresists involved in this work. Even though tall microstructures are fabricated in this work, the traditional use of X-ray exposure is completely avoided to prevent any adverse effect on CMOS devices on the IC chip.

A negative-tone photoresist, SU-8 50 is utilized in this work to form electroplating mold for high-aspect-ratio microstructures. The processing parameters are characterized in this work for all critical steps including spin-coat, pre-bake, UV exposure, post-exposure bake and development. To maintain thickness uniformity of the photoresist across the substrate wafer during pre-bake, a home-designed hot plate with adjustable leveling is placed in the oven and the tilt angle is adjusted to be less than 0.05° monitored by a digital leveler. Baking on a hot plate allows heating from the wafer backside thereby avoiding surface crust formation on the photoresist. Also, in-oven bake avoids interference from open air flow to the photoresist. In this work, the high-aspect-ratio microstructure mold has deep microrecessed holes rather than stand-alone SU-8 columns or thin walls. It is the latter structures that have been mostly reported in literature. The microrecessed hole structures present processing challenges in terms of stress control and resist development. The processing steps to achieve high-aspect-ratio microrecesses have been developed in this work to avoid built-in internal stress related problems in the thick resist layers. A high pass UV filter is chosen in this work which filters out UV light with wavelengths less than 350 nm. This effort significantly helps in reducing skin effect and in reducing T-topping effect thereby resulting in straight sidewalls in thick photoresists. Both pre-bake and post-exposure-bake need long in-oven annealing times to lower the level of internal stress of photoresist caused by thermal shock. Usually this annealing time is over 10 hours. A customized development kit is designed in our laboratory to achieve a clean electroplating mold. Stirring-assisted development is introduced with a special setup having photoresist facing downward to improve developer access. A more efficient technique utilized in this work is to

develop the photoresist at elevated temperature of 55 °C, which results in cleaner electroplating mold and reduces development time by 50% to 75% compared to room temperature processing. Further details of processing steps of thick resist layers of SU-8 50 and thin layer resists including S1813, SU-8 2 and HR200 are given in Chapter 3.

Nickel electroplating is performed to fabricate microprobes inside the SU-8 microrecesses. This work has been described in detail in Chapter 4. Fundamental research was first carried out on flat substrates prior to microprobes electroplating, such as characterization of current efficiency and nickel plating rate as a function of current density. The DC plating current efficiency is seen to increase with increasing current density and reaches 98% at 20 mA/cm^2 indicating negligible side reactions at higher current densities. Plating rate is found to be approximately linear with DC plating current density resulting in a slope of 0.904 $(\mu m/hr)/(mA/cm^2)$. Both DC and pulse electroplating have been employed to form nickel microprobes. In DC plating, it is found that the non-uniform distribution of electrical field lines can cause uneven probe topography with center of probe having a slower deposition rate. The non-uniform distribution of field lines can also cause a probe of smaller dimension being plated faster than a probe of larger dimension. The same cause can result in a more closely spaced probe array being plated at a faster rate as well. However, it is found that electroplating into deep microrecesses falls into the diffusion-controlled regime when the current density is greater than 50 mA/cm^2. Phenomena such as non-uniform probe height and electrolyte precipitation at the electroplating mold recess entrance have arisen as a result of inefficient diffusive mass transfer of cations onto the cathode surface. In this case, the probes of smaller dimensions suffer more from diffusion inefficiency and result in a slower plating rate. For 1.52 M concentrated nickel sulfamate electrolyte utilized in this work, diffusion coefficient D is calculated based on the observation of diffusion effects and Nernst's diffusion boundary model. The measured D value is

found to be 3.3×10^{-6} cm^2/s which is approximately half of the reported value for an infinitely dilute solution. In order to achieve a higher plating rate while retaining good deposit quality, pulse plating technique is utilized in microprobe fabrication. The periods of the pulse on time and off time are tailored against the lengths of charge time and discharge time of the double layer capacitor and the transition time in such a way that the good characteristics resulting from pulse plating are retained. Under a current density 100 mA/cm^2, pulse plating rate is found to be 90 μm/hr during pulse on time, which is about the same value as DC plating on flat substrate under the same current density. Meanwhile, the probe topography and height becomes uniform and the diffusion effect is not observed for the pulse plating case under a high current density of 100 mA/cm^2.

Stress has been a major concern for the electrodeposited nickel. It is especially important in MEMS since it may lead to mechanical failures. In Chapter 4, stress level has been characterized by varying current density and film thickness for the DC plating case, and by varying the on time and off time periods for the pulse plating case. For DC plating case, compressive stress is observed when current density is less than 20 mA/cm^2 and tensile stress results as current density is over 30 mA/cm^2. The results indicate that a stress-free deposit or a deposit with minimized stress can be obtained at a current density 26 mA/cm^2. The stress becomes saturated at approximately 92 MPa for current density between 30 mA/cm^2 and 100 mA/cm^2. As the film thickness increases, stress changes from compressive to tensile as well and saturates at approximately 73 MPa for thickness over 10 μm. For pulse plating, two cases are considered for stress evaluation. For pulse plating with long duration on-pulses of 10 s, it is found that the nickel deposits undergo transformation from tensile to compressive and back to tensile stress as pulse off time increases from 0.5 to 3 s. The stress saturates at 54.5 MPa which is 25% lower than 73 MPa for the DC plating case. Pulse plating by short on-pulses in ms range

were found to always yield compressive built-in stress between -110 MPa and -165 MPa. This is a characteristic of high frequency pulse plating.

Grain size and morphology variations are inspected by SEM. It is found that the grain size variation in long pulse plating coincides with the variation of stress status and magnitude with larger grain corresponding to more compressive or less tensile stress. For short pulse plating, a unique morphology with choppy faceted grains is observed which significantly differentiates it from the grain morphology produced by DC plating and by long period pulse plating.

A simplified one dimensional analytical model has been developed in this work in order to further characterize the pulse plating process. This model describes the transient process of pulse plating during the on time period under an applied potential step. Both a fixed boundary approach and a moving boundary approach are taken into account in the model. In the fixed boundary approach, the variation in microrecess depth δ is neglected during the on time pulse duration. The model estimates the transient time to reach a current density 90 % of which equals the steady state current density. The transition time for the case of δ = 100 μm to be 7 s with the corresponding steady state current density -96.8 mA/cm^2. For the case of δ = 500 μm, the transition time is increased significantly to 220 s and the corresponding steady state current density drops to -19.4 mA/cm^2. In the moving boundary approach, the dynamic change of δ is taken into account. As total on time increases, the diffusion boundary layer thickness, δ decreases. Correspondingly, the current density and the deposition rate also increases under the condition that the magnitude of the overpotential is maintained at the same value. Two cases are treated in this model. Case 1 treats the situation of long on time pulse, in which diffusion controlled regime is eventually reached. Case 2 treats the situation of a very short on time pulse, in which the plating current density is approximately the same as the output from the power supply. Case 2 is desirable as it takes the advantage of high instantaneous nucleation rate and

hence results in a more compact structure and less tensile stress. The model offers a qualitative understanding of the pulse electroplating process and also gives a rough measure on choice of on time period. On time period of 10 s has been utilized for the case of δ = 100 μm in this work which is comparable to the computed transition time from the modeling results.

Chapter 5 describes techniques to sharpen nickel probes. Both nickel wires and nickel microprobe array are sharpened electrochemically. Constrained by the dimension of the on-chip microprobes, the advantage of faster etching rate at the interface of air and electrolyte can not be exploited though it has been utilized in much of the literature on the subject. In contrast, the nickel at the air-electrolyte interface is protected in order to preserve probe integrity and to only sharpen its tip. The etching process is performed in a dilute sulfuric acid solution. A sharp nickel wire is obtained in sulfuric acid concentration at 0.5 M, at 30 °C, and at 4 V anode bias. The microprobe array, however, is not as sharp as the commercial nickel wires after etching under the same conditions. Future work is needed to optimize the etching process for integrated nickel microprobe array.

Chapter 6 describes the complete post-IC monolithic integration process. A wafer-level integration process is first developed and optimized. However, because of limited availability of fabricated IC chips from the foundry, a chip-level integration process is also developed in this work. A clean electroplating mold base is found to be critical to obtain sufficient adhesion strength between the nickel microprobes and the substrate. In the first version of the chip design, the Al contact pads utilized in a standard CMOS chip were found to weaken the adhesion between the electroplated nickel probes and the substrate. This is attributed to a presence of native aluminum oxide. As a result, Al is removed from the contact pads and is replaced with n^+-doped silicon in the revised version of the IC chip design. This approach significantly promoted

the adhesion of the nickel microprobes to the substrate and free-standing microprobes with aspect-ratio up to 3:1 and heights of up to 210 μm have been successfully electroplated.

The chip-level integration process underwent two versions of development. First, in the surface micromachining approach, SU-8 50 photoresist is utilized to form a chip rest chamber to level the chip topography with the rest chamber. However, microprobe electroplating was not successful utilizing this approach. The reason for failure is attributed to discontinuity in the Cu seed layer for current passage caused during the thermal treatment step that induces resist flow in SU-8. This problem has been solved by taking a bulk micromachining approach. In the latter approach, a silicon wafer is bulk etched by a KOH etchant. The depth of the chamber is precisely controlled to equal the thickness of the IC chip. However, KOH etch is anisotropic and results in a gap between the chip and the carrier wafer. In order to electrically bridge between the chip and the carrier wafer, a novel tape and wire bonding technique has been developed that successfully fulfilled the bridging purpose. Nickel microprobes with an aspect-ratio as high as 4:1 and as tall as 160 μm have been obtained on a test silicon chip by using this technique. A separate issue is the CMOS chip topography which is measured to be about 3 μm. This surface roughness of the CMOS chip resulted in uneven probe height of nickel microprobes processed by DC electroplating. The probe heights on the CMOS chip became even after pulse plating technique was utilized.

Future work should include: 1) fabrication of taller probes with higher-aspect-ratio, 2) sharper probe tips to ease tissue penetration, 3) signal integrity verification between the input and the output and 4) biocompatibility issues if this micro system is utilized in a living tissue. Taller probes may be achieved by multilayer application of thick SU-8 resist. Potential issues by taking this approach include thermal budget tolerance of earliest applied resist, alignment challenge between different layers and difficulty in resist development. Sharper probes may be achieved

through improving the quality of the electroplated microprobes and optimizing the etching process. In terms of biocompatibility, polyimide is a proven biocompatible material, thus an excellent choice for neuroprosthetic applications which can be used to wrap the bulk of nickel microprobes. The sensing probe tips can be coated with a noble metal layer to exclude non-biocompatible nickel from body fluids.

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Appendix A. Concentration Overpotential

A.1 Origin of Concentration Overpotential

For the cases of DC electroplating and for pulse plating with long on time periods, an overpotential called concentration overpotential is associated with mass transport limitation. This overpotential starts to play a role when the plating current density is high and is limited by concentration gradient between the cathode surface and the bulk electrolyte. This phenomenon is readily observed in the case of electroplating into a deep microrecess compared to the case of electroplating onto a flat substrate. Concentration overpotential results in a diffusion resistance, R_d as indicated in the equivalent circuit in Fig. 4.17. Figure 4.17 is shown here again as Fig. A.1 for convenience. Here, R_p is the polar resistance that is reflected by the slope of the polarization curve, R_e, R_d respectively represent equivalent resistance values inside a microrecess resulting from the electrolyte conductivity and by diffusion, and R_b is the resistance of the bulk electrolyte.

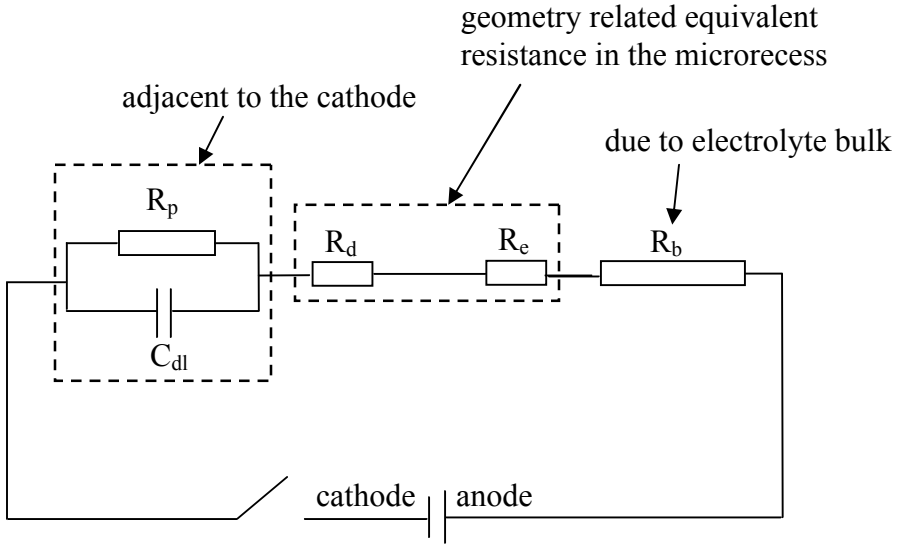


Figure A.1: A simple equivalent circuit representing electroplating into a microrecess (same as Fig. 4.17).

In order to model an electrochemical system, some assumptions are made in conjunction with appropriate engineering approximations so that simplified equations can still reflect

fundamental physical concepts. One common assumption is that of a dilute solution so that the concentrations of electro-active species are extremely low, thereby only solute and solvent interactions are considered and the solute-solute interactions are ignored. Under this condition, a general expression to describe the flux of an ionic species is

$$N_i = -z_i \mu_i F c_i \nabla \phi - D \nabla c_i + c_i v \qquad (1)$$

where N_i is the flux $(cm^2 \cdot sec)^{-1}$, z_i is the charge number per ion, μ_i is the mobility of the ion ($cm^2 \cdot mol/J \cdot s$), F is Faraday's constant, i.e. 96485 C/mol of unit charges, c_i is the species molar concentration, $\nabla\phi$ is the potential gradient, D_i is the diffusion coefficient, and **v** is the bulk fluid velocity. The first term on the right-hand side the eqn. (1), stands for flux caused by electrical field, the second term caused by ionic diffusion due to a concentration gradient and the third term caused by mechanical bulk electrolyte motion. Current density results from the net motion of all charged species and is given by

$$j = F \sum_i (z_i N_i) . \qquad (2)$$

Substitution of eqn. (1) into eqn. (2) yields

$$j = -F^2 \nabla \phi \sum_i (z_i^{\,2} \mu_i c_i) - F \sum_i (z_i D_i \nabla c_i) + F v \sum_i (z_i c_i) . \qquad (3)$$

The last term on the right of eqn. (3) is zero demanded by electroneutrality. The first term is essentially the Ohm's law: current density is proportional to the gradient of the electrical potential with $k = F^2 \sum_i (z_i^{\,2} \mu_i c_i)$ being the conductivity of the electrolyte. $\nabla\phi$ can then be obtained by rearranging eqn. (3):

$$\nabla \phi = -\frac{j}{k} - \frac{F}{k} \sum_i (z_i D_i \nabla c_i) . \qquad (4)$$

The first term on the right-hand side of eqn. (4) stands for the potential drop due to ohmic drop, and the second term represents the potential drop contributed by concentration gradient which results in the diffusion potential, or concentration overpotential.

A.2 Derivation of Concentration Overpotential

The Nernst equation which describes thermodynamic equilibrium at the electrode surface is

$$E_{rev} = E_0 + \frac{RT}{nF}\ln\left(\frac{\prod a_{ox,i}^{S_{ox,i}}}{\prod a_{red,i}^{S_{red,i}}}\right) \tag{5}$$

where E_{rev} is reversible potential of a particular reaction, R is the universal gas constant (8.31 J/mol·K), T is the absolute temperature, E_0 is the reversible half cell potential under standard conditions, i.e. 25 °C and 1 atm, $a_{ox,\,i}$ is the activity of the i^{th} type of species in oxidized state, $a_{red,\,i}$ is the activity of the i^{th} type of species in reduced state and S is the corresponding stoichiometric coefficient. For $Ni \Leftrightarrow Ni^{2+} + 2e^-$, considering only nickel ions in the solution, eqn. (5) is simplified to

$$E_{rev} = E_0 + \frac{RT}{nF}\ln\left(\frac{C^1_{Ni^{2+}}}{1}\right). \tag{6}$$

Here, the activity for solid nickel deposit is usually taken as unity, and the activity for ions in a dilute solution is taken to be the value of its concentration.

At equilibrium, $j = 0$, $C_s = C_b$ states that there is no concentration gradient at the cathode surface. Here, C_s stands for the concentration of Ni^{+2} at the cathode surface and C_b is the concentration of Ni^{+2} in the bulk electrolyte. Eqn. (6) then becomes

$$E_{rev} = E_0 + \frac{RT}{nF}\ln C_b. \tag{7}$$

When a large net current exists, a concentration gradient results with the surface concentration dropping from C_b to C_s ($j \neq 0$), and eqn. (7) becomes

$$E = E_0 + \frac{RT}{nF} \ln C_s . \tag{8}$$

Subtracting eqn. (7) from eqn. (8) yields

$$\eta_c = \frac{RT}{nF} \ln \frac{C_s}{C_b} . \tag{9}$$

where η_c is the overpotential caused by concentration gradient. Using Nernst boundary model, current density can be expressed as

$$\frac{j}{nF} = -D \frac{C_b - C_s}{\delta} , \tag{10}$$

which equalizes the current density before arriving at limiting current density. Also, j_{lim} obeys Nernst boundary layer model:

$$\frac{j_{\lim}}{nF} = -D \frac{C_b}{\delta} , \tag{11}$$

which is the limiting current density at which the reactive species has been completely depleted at the cathode surface.

Dividing eqn. (10) by eqn. (11) gives

$$\frac{j}{j_{\lim}} = 1 - \frac{C_s}{C_b} . \tag{12}$$

Substituting eqn. (12) into eqn. (9) yields

$$\eta_c = \frac{RT}{nF} \ln(1 - \frac{j}{j_{\lim}}) . \tag{13}$$

Differentiating η_c with respect to j yields diffusion resistance, R_d

$$R_d = \frac{1}{A} \frac{RT\delta}{(nF)^2 DC_b} \ln(1 + \frac{j\delta}{nFDC_b}) , \tag{14}$$

where A is the cross-section area of the microrecess. It is seen from this equation that, as expected, the value of R_d is inversely proportional to the cross-sectional area A of the microrecess.

Appendix B. Calculation of Stress from Lattice Constant

X-Ray diffraction technique (XRD) is usually employed to detect the lattice constant of a crystalline material. In this work, XRD technique is utilized to characterize the strain in the electroplated nickel films which is then used to characterize the built-in stress S by using the elastic stress-strain relationship $S = E\,(a-a_0)/a_0$, where a is the lattice constant of deposited metal, a_0 is the lattice constant in the same material free of stress and E is the Young's modulus.

Figure B.1 shows that the reflected X-ray beams from two adjacent lattice planes can become constructive as the glancing angle θ made by the incident X-ray and the surface of the sample satisfies $2d_{\{h\,k\,l\}} \sin\theta = \lambda$, where $d_{\{h\,k\,l\}}$ is the distance between two adjacent {h k l} lattice planes and λ is the wavelength of the incident X-ray. For a cubic lattice, the lattice constant a and the lattice plane spacing $d_{\{h\,k\,l\}}$ has the relationship of $d_{\{hkl\}} = \frac{a}{\sqrt{h^2+k^2+l^2}}$. Once a is known, the internal stress S is expressed by $S = E\,(a-a_0)/a_0$. Here, refraction peak from lattice planes {400} is utilized to obtain the value of a.

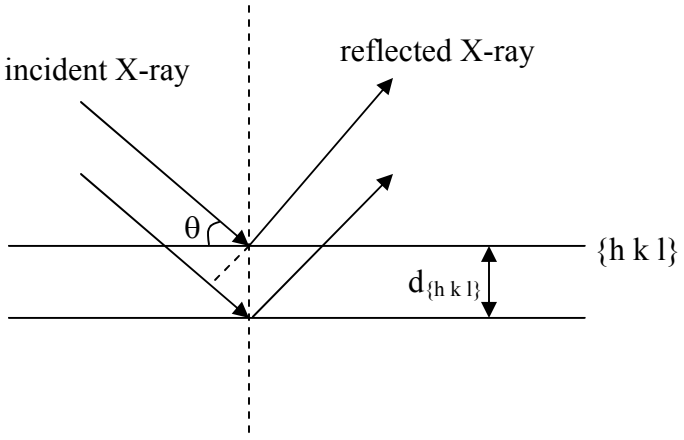
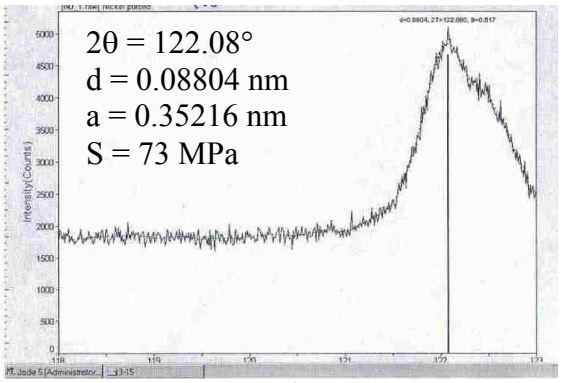


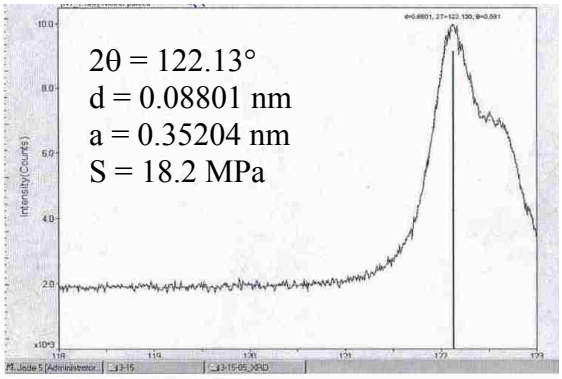
Figure B.1: A diagram showing the relationship between the glancing angle θ and the lattice plane spacing $d_{\{h\,k\,l\}}$. A constructive interference between the two adjacent {h k l} lattice planes occurs when $2d_{\{h\,k\,l\}} \sin\theta = \lambda$ is satisfied.

As an illustration, Figure B.2 shows the original XRD patterns as a function of t_{off} by keeping t_{on} constant at 10 s. Fig. 4.22 is the corresponding stress analysis plot. The stress and

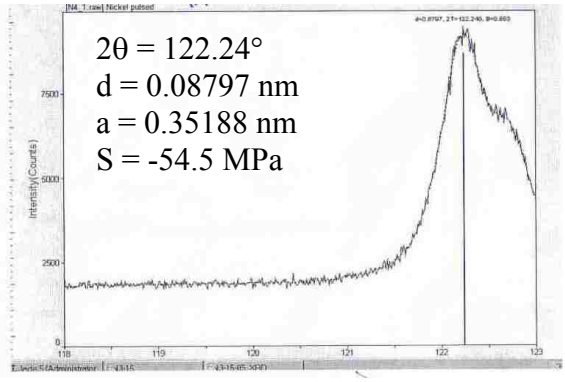
strain relationship with respect to t_{off} is given in section 4.5.2. Lattice planes {400} are used to characterize the lattice constant in this work. Figure B.2 a) shows the case for $t_{off} = 0$ s. Here, the lattice constant is greater than the one corresponding to the stress-free case giving a tensile stress value of 73 MPa. Figure B.2 b) shows the case for $t_{off} = 0.5$ s corresponding to a stress value of 18.2 MPa. Figure B.2 c) represents the XRD pattern for the cases of $t_{off} = 1$ s and $t_{off} = 2$ s corresponding to a stress value of -54.5 MPa in Fig. 4.22. Figure B.2 d) represents the XRD pattern for cases of $t_{off} = 3$ s to $t_{off} = 20$ s representing the saturated stress value of 54.5 MPa in Fig. 4.22.



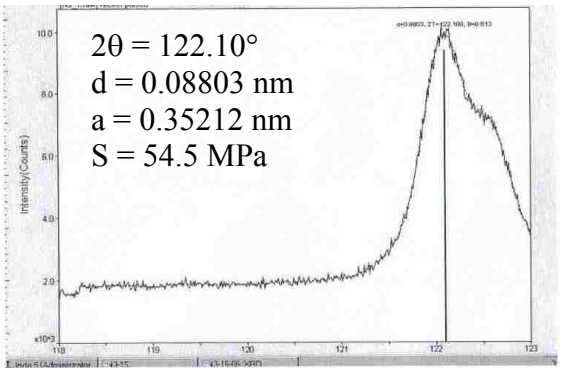
a)



b)



c)



d)

Figure B.2: XRD patterns showing refraction intensity as a function of glancing angle 2θ for the pulse plating case in Fig. 4.22 with t_{on} fixed at 10 s. a) $t_{off} = 0$ s, b) $t_{off} = 0.5$ s, c) $t_{off} = 1$s and 2s, d)) $t_{off} = 3$ s to 20 s.

Vita

Tinghui Xin was born in Cangzhou, Hebei province, China, on October 7, 1972, the first son of Yiuyun Pang and Xiaosheng Xin. After completing high school at Nankai High School, Tianjin, China, in 1992, he attended Shanghai Jiao Tong University from 1992 to 1999. He graduated with a Bachelor of Science degree in 1996 and a Master of Science degree in 1999, both from the Department of Materials Science and Engineering. He then entered the Louisiana State University at Baton Rouge, Louisiana, in the fall of 1999. He obtained a Master of Science degree from the interdisciplinary program of engineering science in May 2001 and a Master of Science degree from the Department of Electrical and Computer Engineering in December 2003. He currently is a doctoral student in the Department of Electrical and Computer Engineering. Since January 2006, he is employed as an applied research engineer at Lexmark International.