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TWO-DIMENSIONAL MICROSCANNERS WITH T-SHAPED HINGES AND PIEZOELECTRIC ACTUATORS

A Thesis
Submitted to the Graduate Faculty of the
Louisiana State University and
Agricultural and Mechanical College
in partial fulfillment of the
Requirements for the degree of
Master of Science in Electrical Engineering
in
The Department of Electrical and Computer Engineering

By Wenyu Song B.S., JiLin University, 2004 May 2009

ACKNOWLEDGEMENTS

I would like to thank Dr. Dooyoung Hah, my advisor, for his endless help and rich idea, continuing encourage and patience throughout the time of this project. Without his support this work would never have been.

I would like to thank Dr. Martin Feldman and Dr. Theda Daniels-Race for their invaluable guidance and for being part of my graduate committee.

I would like to acknowledge Mr. Golden Hwuang of the Electronic Materials and Devices Laboratory (EMDL) of Louisiana State University (LSU) for his help and invaluable suggestions.

I want to dedicate this to my family member, who have always supported me and encouraged me to continue my study.

Finally, thanks to all of my friends and lab mates I have met over two years here. You all play a wonderful role in my life.

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ABSTRACT

For a wide range of application areas such as medical instruments, defense, communication networks, industrial equipment, and consumer electronics, microscanners have been a vibrant research topic. Among various fabrication methodologies, MEMS (microelectromechanical system) stands out for its small size and fast response characteristics. In this thesis, piezoelectric actuation mechanism is selected because of its low voltage and low current properties compared with other mechanisms, which are especially important for the target application of biomedical imaging. Although 1- and 2-dimensional microscanners with piezoelectric actuators have been studied by several other groups, this thesis introduces innovative improvements in design of the piezoelectric MEMS microscanner. A novel T-shaped hinge geometry is proposed, which is flexible in whole six directions and also free from the crosstalk issue found in the earlier designs by other groups.

The piezoelectric actuator of the microscanner is comprised of five layers; a top electrode, a piezoelectric layer (lead zirconate titanate or PZT), a bottom electrode, a dielectric layer, and a mechanical support. The microscanners were analyzed using both analytical formulas and numerical simulations. Based on the analysis, the microscanners were designed and fabricated with four mask levels—top electrodes, bottom electrodes, bonding pads, and substrate etching windows. During the silicon substrate wet etching process in KOH, ProTEK[®] B3 was coated in the front to protect the devices.

Polarization-voltage (*P-V*) measurement of deposited PZT was performed using RT66B. Actuation of the piezoelectric cantilevers were observed under a microscope by applying voltage.

CHAPTER 1. INTRODUCTION

With a number of advantages including small size, light weight, and fast speed compared to conventional bulky scanners, MEMS (microelectromechanical system)-based optical microscanners have been drawing attention for a wide range of applications such as microscopes [1.1-1.2], display systems [1.3-1.4], and barcode readers [1.5]. They are particularly interesting for biomedical imaging applications with the aforementioned merits, and one of the best examples is a probe head for the Endoscopic Optical Coherence Tomography (EOCT) [1.6-1.8]. This thesis covers the development of a MEMS-based piezoelectric microscanner with novel T-shaped hinges (figure 1.1) for the EOCT application.

To have a sufficient angular range, most of the MEMS microscanners reported so far require either high voltage or high current both of which are hazardous and dangerous for *in vivo* biomedical imaging applications. High voltage or high current electric signal also has the potential to cause electromagnetic interference (EMI) to affect other medical equipment. Therefore, the aim of this thesis is to develop MEMS microscanners operated by low voltage as well as low current without sacrificing the scan range.

This chapter is organized as follows. Introduction to optical coherence tomography (OCT) is provided in section 1.1. Then, review on the various MEMS actuation mechanisms is presented in section 1.2. Finally, piezoelectric effect and the related phenomenon are discussed in section 1.3.

1.1 Optical Coherence Tomography

Optical coherence tomography is an emerging technology for biomedical imaging, first reported to be used in medicine in 1990 [1.9-1.13]. Because of its micrometer-resolution both in

axial and transversal directions, minimal invasiveness, and real time imaging capability, OCT is considered to be one of the most prominent imaging techniques for a wide range of applications such as ophthalmology, endoscopy, functional imaging, and guided surgery.

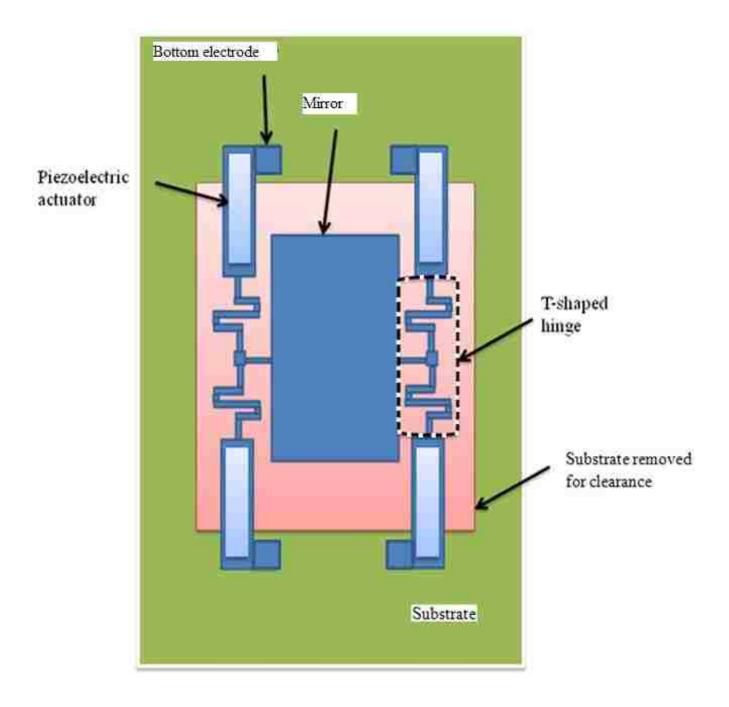


Figure 1.1. Schematic diagram of the proposed piezoelectric microscanner with T-shaped hinges.

Similar to ultrasound imaging, OCT is based on reflectometry, i.e. backscattering due to index mismatch. However, instead of using acoustic waves, it utilizes light waves and measures the backscattered intensity from a sample as a function of depth. A diagram of the OCT imaging system is shown in figure 1.2. Its basic structure resembles the Michelson interferometer. Light from the source is divided into two paths—one path is called a sample arm and the other a reference arm—by a 2 x 2 coupler. Light traveling in the sample arm is reflected from the sample and that in the reference arm from a mirror at its end. When the reflected light signals are recombined at the same 2 x 2 coupler, interference may occur. A low coherence light source is used so that strong interference occurs only when the lengths of two optical paths are very close to each other. By changing the path length at the reference arm with a delay scanning device, the index changes of the specimen along the depth direction can be observed. Transversal information, either 1- or 2-dimensional, can be achieved by lateral scanning of the optical beam in the sample arm. In this thesis, a MEMS scanner is developed for this lateral scanning function.

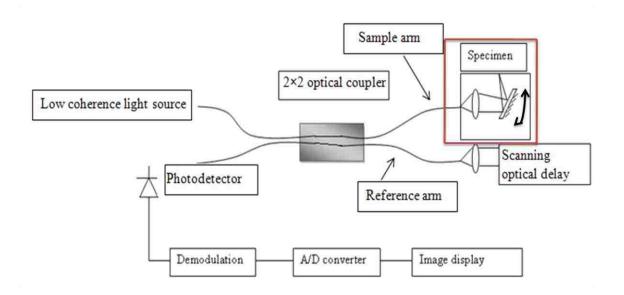


Figure 1.2. Schematic diagram of an OCT system [1.14].

1.2 MEMS Scanner Actuation Methods

Several actuation mechanisms have been used to rotate MEMS microscanners, such as electrostatic, electromagnetic, electro-thermal, and piezoelectric methods [1.15-1.25]. Electrostatic actuation [1.15-1.18] requires low standing power consumption and is relatively easy to be integrated with electronic integrated circuits. However, it requires high actuation voltage, typically over 100 V. Electromagnetic actuation [1.19-1.21] requires low actuation voltage and is also easily integrable with electronic circuits. However, it requires high actuation current, typically over 100 mA, and hence high standing power consumption. It also needs either a permanent magnet or an external coil to generate the magnetic field. Although electro-thermal actuation [1.22] provides larger rotation angles compared to the two aforementioned mechanisms, it is slower than those methods, and it also requires large standing power consumption.

On the other hand, piezoelectric actuation [1.3],[1.23] requires low voltage, low current, and low standing power consumption, which makes it the most attractive method for *in vivo* biomedical devices. However, most of the piezoelectric microscanners reported so far have not demonstrated a sufficient scanning range. The reason behind this will be discussed in the following chapter. Qualitative comparison among different actuator mechanisms is summarized in table 1.1.

1.3 Piezoelectricity

Piezoelectricity is a property of certain non-conductive materials, which couples between mechanical stress or strain and electric polarization. The direct piezoelectric effect, i.e. electricity generated by applied stress was discovered in 1880 by Pierre and Jacques Curie. However, they

did not predict that crystals exhibiting the direct piezoelectric effect would also exhibit the converse piezoelectric effect, i.e. strain generated in response to applied electric field.

Table 1.1. Comparison of different MEMS actuation methods

	Electromagnetic	Electrostatic	Electro-thermal	Piezoelectric
Driving type	Current	Voltage	Current	Voltage
Speed	Fast	Fast	Slow	Fast
Force	High	Low	High	High
Standing Power Consumption	High	Very low	High	Very low

In 1881, the converse effect was mathematically predicted by Lippmann from fundamental thermodynamic principles, and experimentally proved by the Curie brothers. Until 1920, this phenomenon was just a laboratory curiosity. From 1920 to 1940, first generation applications were demonstrated with natural crystals, such as microphones and accelerometers. From 1940 to 1965, the second generation applications were realized with piezoelectric ceramics, such as the ceramic audio tone transducer and relay. Then, several types of piezo ceramic signal filters were developed for television, radio, and communication equipment markets [1.24].

1.3.1 Piezoelectric Materials

Piezoelectric materials in the microfabrication field can be divided into three categories. The first group is piezoelectric substrates that include quartz (SiO₂), lithium niobate (LiNbO₃), and gallium arsenide (GaAs). Another group is thin-film piezoelectrics such as zinc oxide (ZnO),

aluminum nitride (AlN), and lead zirconate titanate (Pb(Zr,Ti)O₃ or PZT). The last group is polymer-film piezoelectrics such as polyvinylidene fluoride (PVDF). Among these materials, PZT has the largest piezoelectric coefficients (table 1.2), which is desirable for most applications.

All crystals can be divided into 32 classes or point groups. Among them, 21 classes do not possess a center of symmetry, and within those 21, 20 groups are piezoelectric. The lack of center of symmetry means that a net movement of the positive and negative ions with respect to each other as a result of stress produces an electric dipole. Most of the piezoelectric materials have the perovskite crystal structure (figure 1.3), and it is found that materials with this crystal structure, especially lead zirconate titanate (PZT) have the best piezoelectric properties [1.25].

Table 1.2. Piezoelectric coefficients of selected piezoelectric materials.

Material	Piezoelectric coefficients
Quartz	$d_{11} = -2.3 \text{ pm/V}, d_{14} = 0.7 \text{ pm/V}$
Barium titanate	$d_{33} = 85.6 \text{ pm/V}; d_{31} = -34.5 \text{ pm/V}$
Lithium niobate	$d_{33} = 6 \text{ pm/V}, d_{15} = 68 \text{ pm/V}$
Lead zirconate titanate	$d_{31} = -180 \text{ pm/V}, d_{33} = 360 \text{ pm/V}$
Aluminum nitride	$d_{33} = -0.2 \sim -4.5 \text{ pm/V}$
Zinc oxide	$d_{33} = 12.4 \text{ pm/V}$
Gallium arsenide	$d_{33} = 18 \text{ pm/V}$
Polyvinylidene fluoride	$d_{3I} = 20 \text{ pm/V}, d_{33} = 30 \text{ pm/V}$

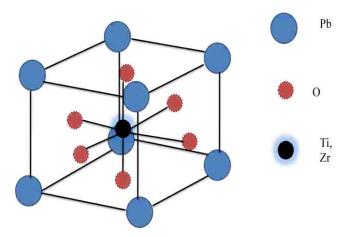


Figure 1.3. Perovskite structure, example with PZT.

The perovskite structure may transform into two crystallographic forms. Above a critical temperature, the Curie point, each perovskite crystal in a fired ceramic element exhibits a simple cubic symmetry with no dipole moment (figure 1.4a). At temperatures below the Curie point, however, each crystal has tetragonal or rhombohedral symmetry and a dipole moment (figure 1.4b).

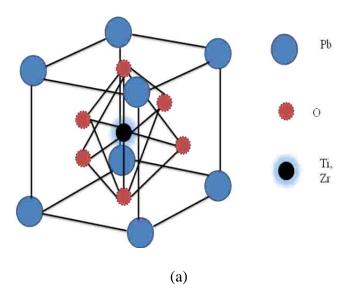
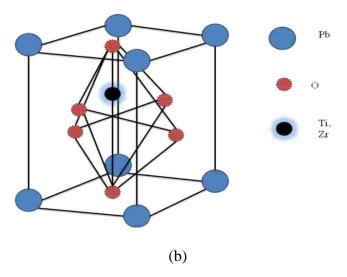


Figure 1.4. Transformation of the perovskite crystal structure due to temperature change. (a) Above Curie point, cubic symmetry with no dipole moment. (b) Below Curie point, tetragonal or rhombohedral symmetry with dipole moment. (Figure continued on next page)



Adjoining dipoles which form regions of local alignment are called domains in which the alignment gives a net dipole moment to the domain, or a net polarization. The directions of polarization among neighboring domains are random; therefore, the ceramic element has no overall polarization (figure 1.5a). The domains in a ceramic element can be aligned by exposing the element to a strong and sufficiently high electric field, usually at a temperature slightly below the Curie point (figure 1.5b), such that the domains rotate and switch in the direction of the electric field. During this poling process, there is a small expansion of the material along the poling axis and a contraction in both directions perpendicular to it. When the electric field is removed most of the dipoles are locked into a configuration of near alignment (figure 1.5c). The element now has a permanent polarization, i.e. the remanent polarization, and is permanently elongated.

Ferroelectricity is a subgroup of piezoelectricity; all ferroelectric materials also have piezoelectricity but not all piezoelectric materials show ferroelectricity. Therefore examining ferroelectricity of a material is an indirect way of probing piezoelectricity. In fact, the material constants expressing the two phenomena are interrelated.

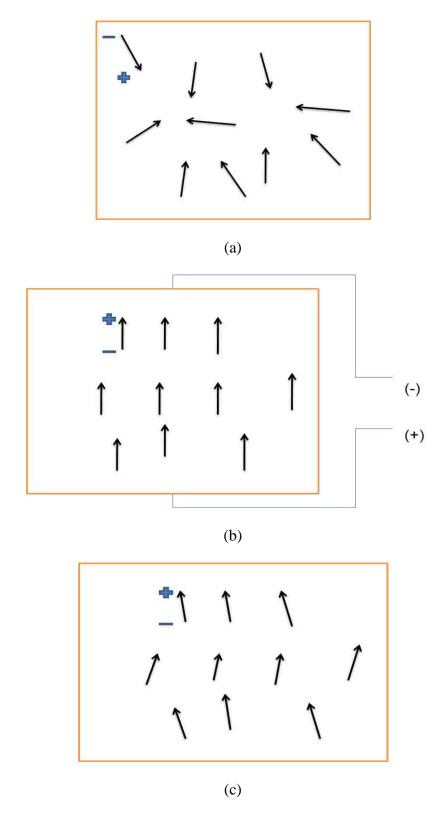


Figure 1.5. Domains. (a) Neighboring domains are randomly oriented. (b) The domains in a ceramic element are aligned by exposing it to electric field. (c) After the electric field is removed.

The basic equation representing the ferroelectricity is

$$D = \varepsilon E + P, \tag{1.1}$$

where D, ε , E, and P are electrical displacement, permittivity of the material, external electric field, and polarization, respectively. Similar to the hysteresis of magnetic materials, in the case of ferroelectric materials, application of the electric field causes the domains to reorient so that a net polarization is obtained, which gives rise to hysteresis in the relation between them as depicted in figure 1.6.

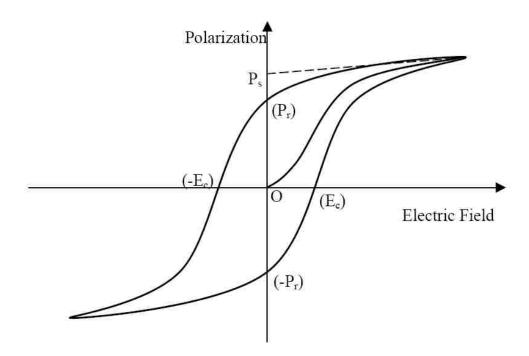


Figure 1.6. Ferroelectric hysteresis loop.

From this figure, it can be seen that applying low electric field yields a linear response as the field is not sufficient to reorient the domains. Applying electric field beyond the positive coercive field E_c "switches" the domains into the direction of the field. At some extent, switching

decreases as the number of un-switched domains is depleted and the material reaches the highest point at which all the domains have switched (saturation). As the field is decreased to zero, most of the domains retain their new orientations while a few of the domains switch back to their original orientations. P_s is named as saturation polarization, and P_r is called as the remanent polarization of the material. To invert the orientation of the domains, electric field has to be applied in the reverse direction, and the field required to make the net polarization zero is the coercive field $(-E_c)$. Further increase of the reverse field will cause the domains to continue to switch to the opposite direction until saturation in this direction is reached. Upon reducing the applied reverse electric field to zero, some of the domains will switch back to their original orientations, but most of the domains retain their orientations creating a negative remanent polarization $(-P_r)$, which should be equivalent in magnitude to the positive remanent polarization P_r . Increasing the field once again causes the domains to switch back into the initial direction of polarization. The positive coercive field E_c should be equivalent in magnitude to the negative coercive field $-E_c$. The area inside the loop represents the energy dissipated within the sample as heat.

In the piezoelectric materials, the coupling between electric field and stress can be expressed in constitutive equations as follows [1.26]:

$$\epsilon_I = \sum_I S_{II}^E \sigma_I + \sum_j E_j d_{jI} \tag{1.2}$$

$$D_i = \sum_J d_{iJ} \sigma_J + \sum_j \varepsilon_{ij}^{\sigma} E_j \tag{1.3}$$

where $i, j \in [1,2,3]$ are indices of electric constituents, $I, J \in [1,...,6]$ are indices of mechanical constituents, ϵ_I the mechanical strain, S_{IJ}^E the compliance matrix at constant electric field, σ_J the mechanical stress, E_j the applied electric field, ϵ_{ij} the dielectric permittivity, and d_{iJ} the strain-

electric-field piezoelectric coupling coefficient. Detailed discussion can be found in [1.27]. The relation between the piezoelectric constant d_{31} and the remanent polarization P_r is expressed by the following equation [1.28]:

$$d_{31} = 2Q_{12}\varepsilon_0\varepsilon_r P_r \tag{1.4}$$

where Q_{12} is the electrostrictive constant (-0.03 m⁴/C² for PZT), ε_0 the vacuum permittivity $(8.85 \times 10^{-12} \text{ F/m})$, and ε_r the relative dielectric constant. Since the magnitude of d_{31} is proportional to P_r , high value of P_r is desirable.

It is a well-known fact that within PZT material, (111) dominated PZT shows the highest d_{31} . It is also reported that when the PZT has a composition of 48% Ti and 52% Zr, a morphotropic phase boundary occurs where the tetragonal (easy poling axis is oriented in the <100> direction) and rhombohedral (easy poling axis is oriented in the <111> direction) phases co-exist resulting in the largest piezoelectric coefficients. A bottom electrode plays a crucial role in formation of (111) dominated PZT layer because it has high influence on nucleation of the PZT film. (111) platinum is preferred because its lattice constant is very close to that of (111) PZT—only 4% mismatch. Besides, it has high thermal conductivity and good stability in high-temperature oxidizing ambient. In addition, it may prevent interfacial chemical reactions and Pb-Si inter-diffusion during PZT layer deposition in strongly oxidizing conditions and at elevated temperature conditions between 500 °C and 700 °C. To achieve good adhesion between Pt and the underlying silicon dioxide layer, a titanium layer is inserted in-between.

The structure of this thesis is as follows. In chapter 2, design of microscanners including simulation results with ANSYSTM is provided, followed by mask layout design. Chapter 3 is dedicated for the fabrication of the device. Chapter 4 presents the experiment results. Finally, the

thesis is summarized and future works are presented in chapter 5.

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CHAPTER 2. TWO-DIMENSIONAL MICROSCANNER DESIGN

In this chapter, design of the MEMS-based microscanners is presented. There have been several groups who demonstrated one- and two-dimensional (1- and 2D) microscanners with piezoelectric actuators [1.7], [1.23], [2.1]. Schroth et al demonstrated 2D scanning with four PZT actuators [1.23]. They obtained scan angles of 2.5 ° and 6.5 ° at resonance but DC operation was not reported. They reported a problem of the actuator deformation caused by residual stress, which changed the behavior of the actuators. Tsaur et al reported a novel double layer PZT actuator design which can double the deflection for the given actuation voltage and compensate the residual stress of PZT [1.7]. The drawback of this design is the complexity in fabrication. Yee et al utilized a gimbal structure which can minimize the crosstalk between rotations about two axes [2.1]. However, the tilt angles of the mirror were smaller than ± 0.75 °at 15 V.

The common problem of the microscanners utilizing piezoelectric actuators reported so far is the inefficient conversion of deflection to rotation due to bending, tensile, and torsion constraints. In this thesis, the proposed microscanner is featured with novel T-shaped hinges to address this problem. Because the T-shaped hinge is flexible in whole six directions (three translational and three rotational), it can considerably improve the conversion efficiency, and hence can widen the scan range and reduce the required actuation voltage.

ANSYSTM, a multiphysics finite-element-method (FEM) simulation software is used to analyze the actuation of piezoelectric microscanners. For a single piezoelectric cantilever, a basic constituent of the microscanner, the simulation result is compared to that from simple analytic formulas, which will be described in 2.1. In 2.2, because of the complexity, only numerical simulation is used to analyze the microscanners with T-shaped hinge structures. In 2.3, the mask layout design will be illustrated.

2.1 Theoretical Analysis of the Piezoelectric Cantilever Structure

Figure 2.1 shows the schematic diagram of the proposed microscanner. Dimensions of the microscanners are given in both tables 2.1 and 2.2. The structure of the microscanner is designed to have four piezoelectric actuators connected to a mirror in the center through T-shaped hinges. By applying various combinations of voltages (positive and/or negative) to V_1 through V_4 , rotation in two dimensions and out-of-plane translation can be obtained. Details of the operation principle will be presented in section 2.2. In this section, actuation of the piezoelectric cantilever as the basic constituent of the microscanner will be discussed based on both calculation using analytic formulas and simulation using ANSYSTM.

Figure 2.2 shows the cross-sectional view of the piezoelectric cantilever which is comprised of a piezoelectric layer (PZT) and a mechanical supporting layer (silicon). When a voltage is applied across the piezoelectric layer so that it contracts in y-direction—since PZT has strong d_{3l} (negative value), i.e. when electric field is applied in the 3^{rd} dimension, strain is generated in the 1^{st} dimension, eventually, the cantilever bends upward in z-direction because the supporting layer tries to hold it back. When a voltage of opposite polarity is applied so that the piezoelectric layer stretches, the cantilever bends downward for the same reason. The relationship among structural parameters (δ – tip deflection, α – tilt angle at the tip, ν – displaced volume of the entire cantilever), electrical parameters (Q – charge on the surface of the piezoelectric layer, V – applied voltage), and mechanical loads (M – moment, F – force, p – pressure) of the piezoelectric cantilever can be expressed as in equation (2.1) [2.2].

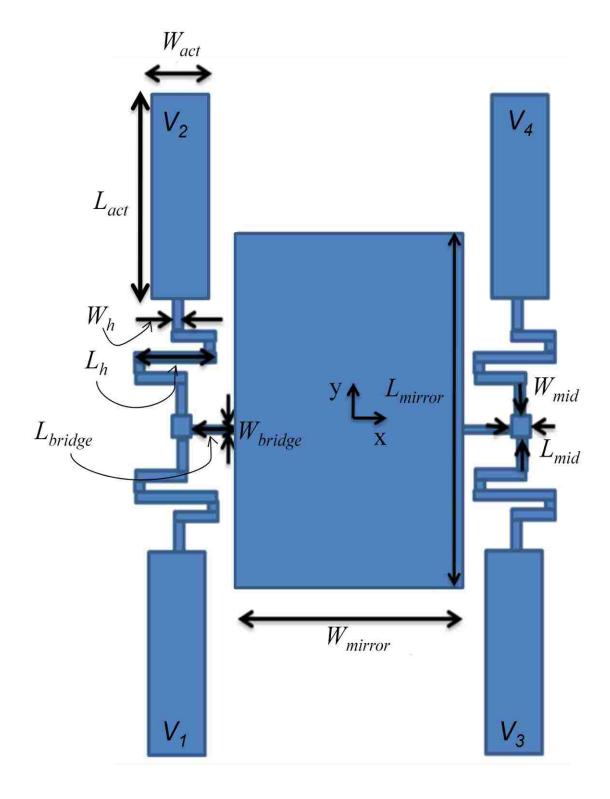


Figure 2.1. Schematic diagram of the mircoscanner with geometric parameters and definitions of the voltage application, V_1 through V_4 .

The equation is as follows:

$$\begin{pmatrix} \alpha \\ \delta \\ v \\ Q \end{pmatrix}$$

$$= A \begin{bmatrix} \frac{12L_{act}}{KW_{act}} & \frac{6L_{act}^{2}}{KW_{act}} & \frac{2L_{act}^{3}}{K} & \frac{6d_{31}BL_{act}}{K} \\ \frac{6L_{act}^{2}}{KW_{act}} & \frac{4L_{act}^{3}}{KW_{act}} & \frac{3L_{act}^{4}}{2K} & \frac{3d_{31}BL_{act}^{2}}{K} \\ \frac{2L_{act}^{3}}{K} & \frac{3L_{act}^{4}}{2K} & \frac{3L_{act}^{5}W_{act}}{5K} & \frac{d_{31}BL_{act}^{3}W_{act}}{K} \\ \frac{6d_{31}BL_{act}}{K} & \frac{3d_{31}BL_{act}^{2}}{K} & \frac{d_{31}BL_{act}^{3}W_{act}}{K} & \frac{L_{act}W_{act}}{Ah_{p}} \left(\epsilon_{33}^{T} - \frac{d_{31}^{2}h_{si}\left(S_{11}^{si}h_{p}^{3} + S_{11}^{p}h_{si}^{3}\right)}{K}\right) \end{bmatrix}$$

$$(2.1)$$

A, B and K are:

$$A = S_{11}^{\ si} S_{11}^{\ p} \left(S_{11}^{\ p} h_{si} + S_{11}^{\ si} h_{p} \right) \tag{2.2}$$

$$B = \frac{h_{si}(h_{si} + h_p)}{(S_{11}{}^p h_{si} + S_{11}{}^{si} h_p)}$$
 (2.3)

$$K = (S_{11}^{si})^{2} (h_{p})^{4} + 4S_{11}^{si} S_{11}^{p} h_{si} (h_{p})^{3} + 6S_{11}^{si} S_{11}^{p} (h_{si})^{2} (h_{p})^{2} + 4S_{11}^{si} S_{11}^{p} (h_{si})^{3} h_{p} + (S_{11}^{p})^{2} (h_{si})^{4}$$

$$(2.4)$$

 S_{II}^{si} and S_{II}^{p} are the (1,1) entries of the compliance tensors of silicon and PZT, respectively. h_{si} and h_{p} are the thicknesses of silicon and PZT, respectively.

$$S_{11}^{\ \ si} = \frac{1}{E_{si}} = 5.92 \times 10^{-12} m^2 / N$$

$$S_{11}^{p} = \frac{1}{E_p} = 8.33 \times 10^{-11} m^2 / N$$

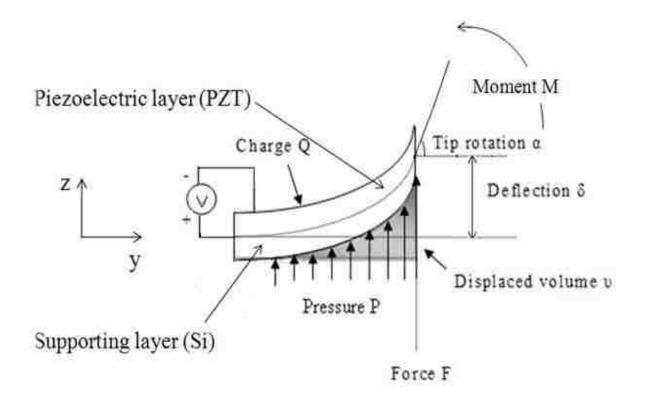


Figure 2.2. A piezoelectric bimorph with external and internal parameters. [2.3]

$$h_{si} = 3 \times 10^{-6} m$$

 $h_p = 1 \times 10^{-6} m$
 $L_{act} = 3.9 \times 10^{-4} m$
 $d_{31} = -171.12 \text{ pC/N}$

The tip deflection δ is expressed as,

$$\delta = A \frac{3d_{31}BL_{act}^{2}V}{K}$$

$$= \frac{3S_{11}^{si}S_{11}^{p}d_{31}h_{si}(h_{si} + h_{p})L_{act}^{2}V}{(S_{11}^{si})^{2}(h_{p})^{4} + 4S_{11}^{si}S_{11}^{p}h_{si}(h_{p})^{3} + 6S_{11}^{si}S_{11}^{p}(h_{si})^{2}(h_{p})^{2} + 4S_{11}^{si}S_{11}^{p}(h_{si})^{3}h_{p} + (S_{11}^{p})^{2}(h_{si})^{4}}$$

$$20$$

$$= 3.25 \times 10^{-6} [C/N] \times V = 3.25 [\mu m/V] \times V \tag{2.5}$$

For example, for the applied voltage of 30 V, the deflection δ is 97.35 μ m. The values of d_{31} , S_{11}^{si} and S_{11}^{p} were obtained from the literature.

The actuation of the piezoelectric cantilever was simulated with ANSYSTM as well. Figure 2.3 shows the simulated deformation of the cantilever when 30 V is applied across the PZT layer. The dimension of the cantilever is the same as the one used in the analytical calculation. The simulation result shows that the tip deflection is 77.0 μ m. This is about 19% smaller than the result from the analytical formulas. One of the reasons is considered to be the difference between full 3-dimensional simulation and analysis with one-dimensional slender beam approximation. Material parameters used in the simulation, d the piezoelectric tensor, and S the compliance tensor are given below. The ANSYSTM simulation code is provided in APPENDIX A.

$$d = \begin{pmatrix} 0 & 0 & -171.12 \\ 0 & 0 & -171.12 \\ 0 & 0 & 374.236 \\ 0 & 584.071 & 0 \\ 584.071 & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \times 10^{-12} \begin{bmatrix} \frac{C}{N} \end{bmatrix}$$

$$(2.6)$$

$$S = \begin{pmatrix} 16.41 & -5.704 & -7.226 & 0 & 0 & 0 \\ -5.704 & 16.41 & -7.226 & 0 & 0 & 0 \\ -7.226 & -7.226 & 18.81 & 0 & 0 & 0 \\ 0 & 0 & 0 & 47.51 & 0 & 0 \\ 0 & 0 & 0 & 0 & 47.51 & 0 \\ 0 & 0 & 0 & 0 & 0 & 44.21 \end{pmatrix} \times 10^{-12} \left[\frac{m^2}{N} \right]$$

$$(2.7)$$

2.2 ANSYS Simulation of Microscanners: Model and Results

The definitions of x- and y-axis, and V_1 through V_4 are given in figure 2.1. Figure 2.4

shows the simulation results illustrating the operation principle of the proposed microscanner. It shows the correlation between the voltage assignments to the four piezoelectric actuators and the two-dimensional rotation of the mirror. Taking the case A of figure 2.4b for an example, applying positive voltages (V/2) to V_2 and V_4 , and equal-but-negative voltages (V/2) to V_1 and V_3 will make the microscanner to rotate about the x-axis counterclockwise (seen from the center of the mirror, and hence marked as positive on x-axis in figure 2.4a).

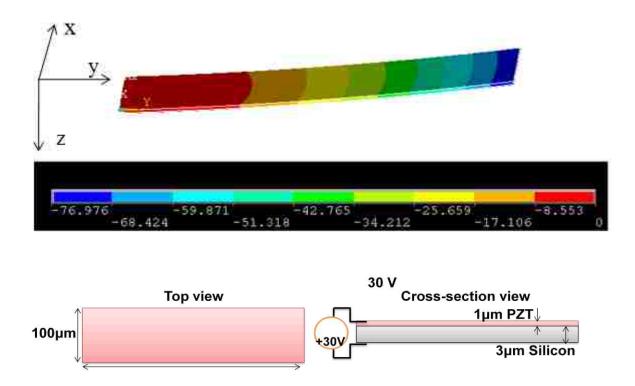


Figure 2.3. Deformed shape of a piezoelectric cantilever, simulation result by ANSYSTM. Top layer: PZT, 1 μm. Bottom layer: silicon, 3 μm. Cantilever width: 100 μm. Cantilever length: 390 μm. Unit of the color code for deflection: μm.

Applying positive voltages (V/2) to V_1 and V_2 , and equal-but-negative voltages (-V/2) to V_3 and V_4 will make it rotate about y-axis counterclockwise so that this case is marked as positive on y-axis. If positive voltage (V) is applied to V_2 , equal-but-negative voltage (V) is applied to V_3 , and V_4 are remained zero, it rotates counterclockwise both about V_3 -axis and V_4 -axis (point

B in figure 2.4a). In this manner, by applying appropriate voltages to V_I through V_4 , continuous two-dimensional rotation of the mirror is possible, which has been verified by simulation. Figures 2.4c, 2.4d, and 2.4e show the ANSYS simulation results of mirror rotation about x-axis (case E), y-axis (case C), and both axes (case D), respectively. The ANSYS simulation program code is provided in APPENDIX B. More than $\pm 7^{\circ}$ of mechanical tilt angles were demonstrated about both axes through the simulation with the maximum applied voltage of 30 V.

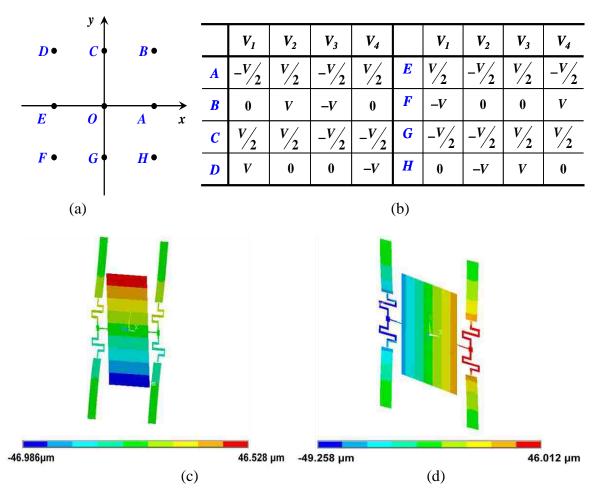
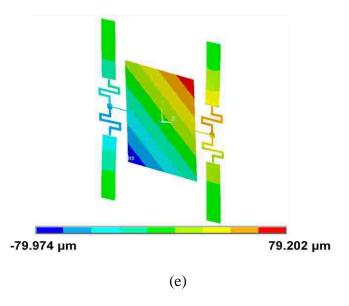


Figure 2.4. Operation principle of the proposed microscanner and ANSYSTM simulation results (microscanner 1 in table 2.1). (a) Map illustrating directions of mirror rotation in relation to the voltage assignments summarized in (b). Counterclockwise rotation is defined as positive and clockwise as negative. All seen from the center of the mirror. (c-e) Simulation results of rotation about (c) x-axis; case E, (d) y-axis; case C, and (e) both x- and y- axes; case D. (Figure to be continued on next page)



For comparison, two previously reported microscanners with different designs were simulated with ANSYSTM—one with four-side-actuators design [2.4] and the other with gimbaltype design [2.5]. For fair comparison, the same values were used for most of the microscanner dimensions such as the thickness of each layer, size of the mirror, width and length of hinges, width and length of actuators, as the proposed design. The simulated deformation of the fourside-actuators type microscanner is presented in figure 2.5. In this example, -30 V is applied to the top actuator and 30 V to the bottom actuator while the left and right actuators are left without voltage applied. The tilt angle about x-axis is 7.68° which is comparable to that of the proposed microscanner. However, the mirror also rotates about y-axis by 1.09°, which is undesirable and makes the control of the microscanner complicated. The simulated deformation of the gimbal type microscanner is presented in figure 2.6. The figure shows an example of the simulation when 30 V is applied to the outside top actuators and -30 V to the outside bottom actuators while inside actuators are left without voltage applied. The simulation results show that the microscanner can rotate $\pm 3.25^{\circ}$ about x-axis and $\pm 9^{\circ}$ about y-axis when the maximum voltage of 30 V is applied, which are not sufficient for many applications.

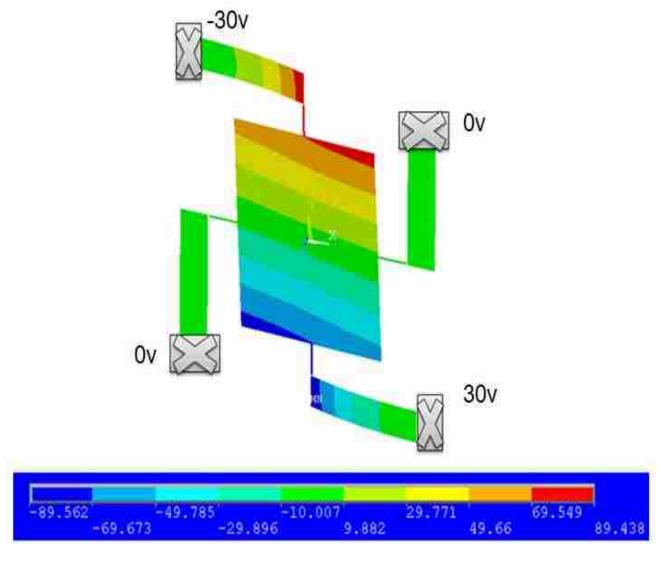


Figure 2.5. Simulated deformation of the four-side-actuators type microscanner [2.4]. Unit of the color code for deflection: μm .

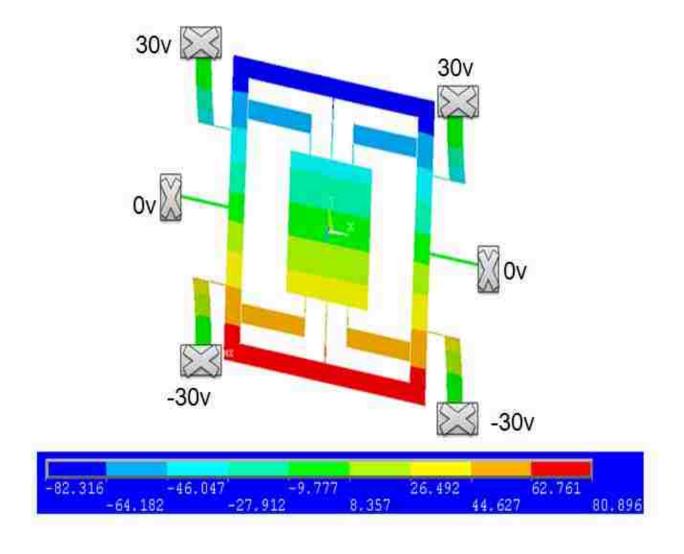


Figure 2.6. Simulated deformation of the gimbal type microscanner [2.5]. Unit of the color code for deflection: µm.

To study the effects of dimension change in various parts of the microscanner on the scanning performance, simulation was performed for various dimensions. Based on the simulation, twelve different microscanners were included in the mask layout as summarized in table 2.2 with the microscanner 1 as a reference whose geometries are given in table 2.1. The simulation results in terms of tilt angles for those twelve designs are provided in table 2.2 as well when maximum voltage of 30 V is applied.

Table 2.1. Geometric parameters of microscanner 1 (unit: μm). Definitions of the parameters are given in figure 2.1.

L_{mirror}	W_{mirror}	L_{bridge}	W_{bridge}	L_{act}	W_{act}	L_{mid}	W_{mid}	L_h	W_h
700	500	100	10	390	100	38	38	120	18

Table 2.2. Simulation results of various microscanner designs.

	Tilt angles (±°)		Difference from microscanner 1.	
	About <i>x</i> -axis	About y-axis	(unit: μm)	
Microscanner 1	7.62	7.55		
Microscanner 2	7.16	6.91	$W_{act} = 60, W_h = 10$	
Microscanner 3	8.71	8.62	$W_{act} = 160, W_h = 26$	
Microscanner 4	4.49	2.81	L_{act} = 195	
Microscanner 5	2.79	1.62	L_{act} = 390	
Microscanner 6	6.25	19.07	$L_{act} = 780$	
Microscanner 7	5.42	7.00	Meander turns of hinge: 0.5	
Microscanner 8	9.14	8.32	Meander turns of hinge: 1.5	
Microscanner 9	10.01	8.84	Meander turns of hinge: 2	
Microscanner 10	6.53	6.01	$W_{act} = 20, L_{mid} = 20, W_{mid} = 20, W_h = 4$	
Microscanner 11	6.41	7.36	$L_{bridge} = 100$, $L_h = 60$, $W_h = 18$	
Microscanner 12	6.79	7.06	$L_{bridge} = 160, L_h = 240, W_h = 18$	

First, by comparing the microscanners 1, 2, and 3 (table 2.2 and figure 2.7), it can be deduced that W_{act} and W_h do not have significant influence upon the tilt angles. Second, by comparing the microscanners 1, 4, 5, and 6 (table 2.2 and figure 2.8), it can be learned that the tilt angle about y-axis is strongly dependent on the actuator lengths (L_{act}) while its effect on the angle about x-axis is not as distinct. Third, by comparing the microscanners 1, 7, 8, and 9, it can be concluded that increasing number of meander turns helps to increase the tilt angles. Finally, from the results of the microscanners 10, 11, and 12, it can be understood that other parameters like L_{bridge} , L_{mid} , W_{mid} , and W_h do not have much of an effect on the tilt angles.

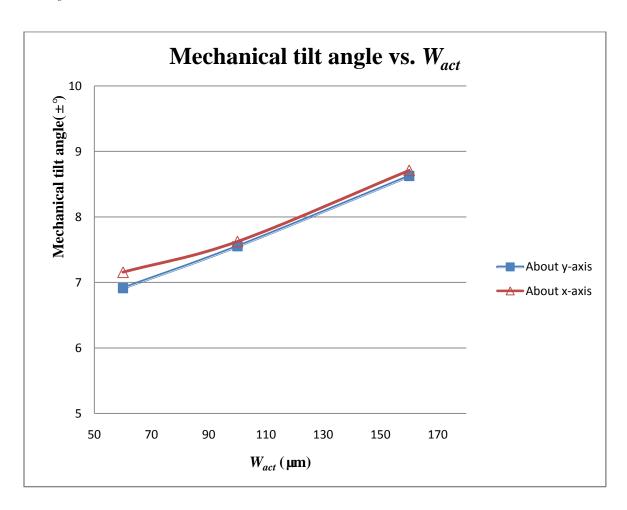


Figure 2.7. Simulated mechanical tilt angles vs. W_{act} . Maximum applied voltage is 30 V.

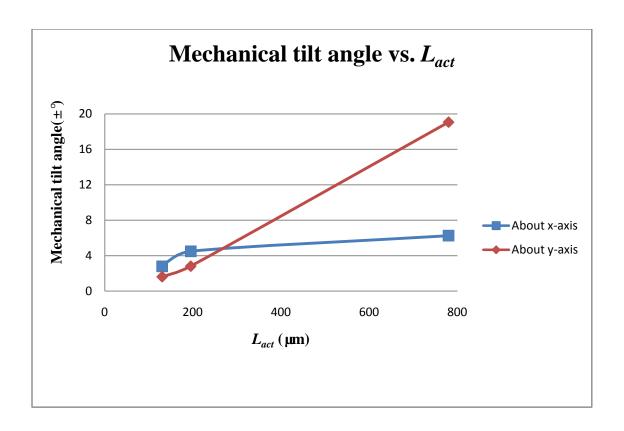


Figure 2.8. Simulated mechanical tilt angles vs. L_{act} . Maximum applied voltage is 30 V.

2.3 Mask Layout Design

Figure 2.9 shows the images of the designed mask layout with all layers overlaid together—individual layers can be found in APPENDIX C1-C4. It is composed of 4 levels: top electrodes, bottom electrodes, bonding pads, and substrate etching windows. The usage of each mask level will be described in chapter 3. Total twelve different microscanner designs were included in a 1 inch \times 1 inch chip area as listed in table 2.2 to find a design that performs best. In addition, test structures such as free-standing piezoelectric cantilevers, piezoelectric actuators connected by T-shaped hinges, and simple cantilevers are also included. Metal-PZT-metal capacitors for polarization-voltage (P-V) measurements and thickness monitoring patterns are included as well.

The fourth mask level is used to produce an etching window for each microscanner to etch a silicon substrate from the back, to make the release step much simpler, and to give a mirror sufficient room for rotation. Silicon will be etched in KOH anisotropically, and different crystal planes have different etch rates which also depend on the concentration and temperature of KOH. Etch rates of (100) and (110) planes are much faster than that of (111) plane in silicon anisotropic etching. If a square etching window is opened on the (100) plane and its sides are aligned to [110] directions, the resulting etched cavity has an inverted pyramidal shape. If the square is tilted off from [110] directions with some angle, a bigger cavity results because the etched cavity is eventually determined by the (111) planes. The survived (111) planes have an angle of 54.74 °with the (100) surfaces as depicted in figure 2.10.

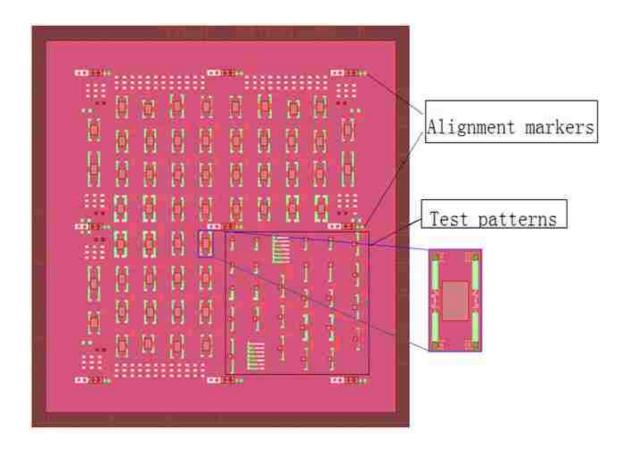


Figure 2.9. Image of the designed mask layout with all four layers overlaid.

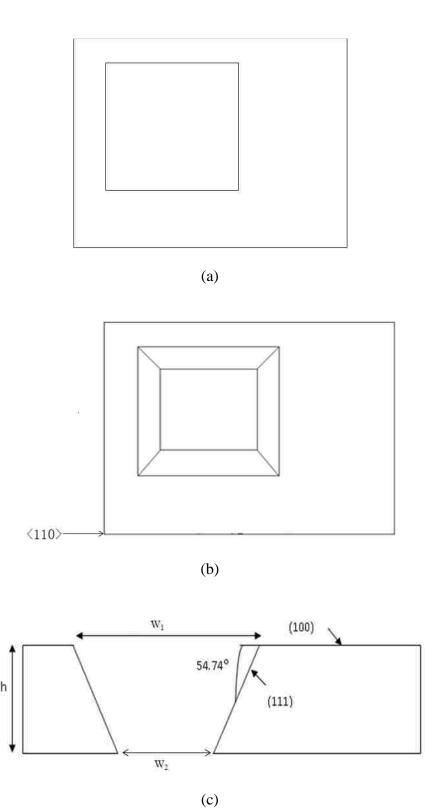


Figure 2.10. Silicon anisotropic etching to form an inverted pyramidal cavity (a) before etching (top view), (b) after etching (top view), and (c) after etching (cross-section view).

According to [2.6], the etch depth h has a relationship with the widths of the etching window W_1 and W_2 as

$$W_2 = W_1 - \sqrt{2}h \tag{2.6}$$

Difference between the opening of etching window at the backside and the resulted opening in the front is calculated to be $2 \times (283 \pm 10 \,\mu\text{m})$ by (2.6) when the thickness of the silicon substrate is $400 \pm 15 \,\mu\text{m}$ as shown in figure 2.11.

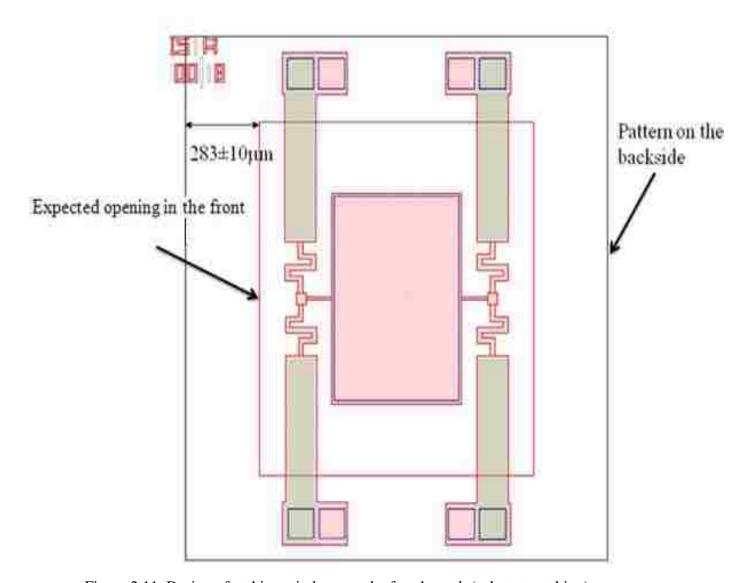


Figure 2.11. Design of etching windows on the fourth mask (substrate etching).

In summary, a new design of microscanners with T-shaped hinges and piezoelectric actuators has been proposed. The operation principle of the microscanner has been demonstrated through ANSYSTM simulation. Parametric simulation has been carried out to optimize the performance of the microscanner. Finally, the mask layout has been designed based on the simulation results. The fabrication process flow has been designed also as explained in the next chapter.

2.4 References

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CHAPTER 3. FABRICATION

In this chapter, the fabrication process flow of the microscanner is described in detail. It includes three critical steps: bottom seed metal layer deposition, PZT process, and front side protection during the silicon substrate etching process.

To apply electric field through PZT, it needs to be sandwiched by two electrodes. However, PZT cannot be grown directly on silicon because of the interfacial chemical reactions and Pb-Si inter-diffusion as mentioned earlier in chapter 1. In formation of (111) orientation dominated PZT for the strong piezoelectric effect, a bottom seed layer plays a crucial role. (111) platinum is used as the seed layer because its lattice constant is very close to that of (111) PZT – only 4% mismatch. Detailed description will be provided in section 3.3.

In the PZT thin film process, temperature control during pyrolysis and annealing is important to obtain a high quality PZT layer. The PZT layer will be pyrolyzed at $450 \, \text{C}$ to remove organics and annealed at $650 \, \text{C}$ to produce a perovskite structure. Failing to control the temperature in these processes will result in non-perovskite structure, and hence no piezoelectric effect. The detailed process will be explained in section 3.4.

Front side protection during the silicon substrate etching process has never been trivial. Various methods such as wax and mechanical clamp were reported to protect the front side structures in the silicon wet etching process in KOH or TMAH [3.1]. However, wax residue is not easy to remove completely and the etchant penetrates along the interface sometimes. Manual labor of mechanical clamping method is complex and requires special care to implement. Recently, an alternative way was introduced, i.e. ProTEK® B3 (Brewer Science, inc) protection

layer coating. This method was selected, which will be detailed in section 3.9.

The fabrication process flow is summarized in figure 3.1 and figure 3.2.

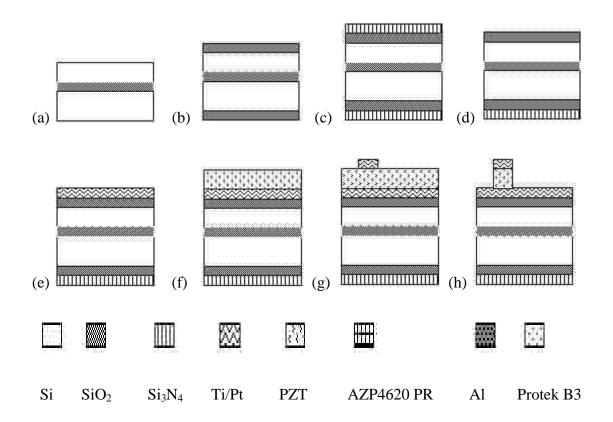


Figure 3.1. The fabrication process flow. (a) SOI wafer cleaning with piranha solution. (b) Thermal oxidation. (c) Si₃N₄ deposition using LPCVD. (d) Removal of front side Si₃N₄ in hot phosphoric acid with S1813 as an etching mask on the backside. (e) Bottom Pt/Ti layer deposition by sputtering. (f) Spin coating and annealing of a PZT layer. (g) Top Pt/Ti electrode formation. Spin coating of S1813 photoresist, photolithography using the first mask level, descumming S1813 residues by O₂ RIE, Pt/Ti deposition by sputtering, and lift-off process. (h) Wet etching PZT using top Pt/Ti as an etching mask.

Microscanners were fabricated on a 1 inch ×1 inch substrate diced from a 6 inch Silicon-On-Insulator (SOI) wafer (Shin-Etsu Handotai Co., Ltd). The specification of the SOI wafer is listed in table 3.1. The reason to use the SOI wafer in the current research is related to the non-uniformity in silicon anisotropic etching to release MEMS structures. To make the last release step more controllable and reliable, an etch stop layer is necessary between the structural layer

and the substrate. The buried oxide layer of an SOI wafer is a perfect fit for this purpose. In addition, silicon is known to be a good mechanical material, and single crystalline silicon has a lower degree of residual stress compared to polycrystalline silicon.

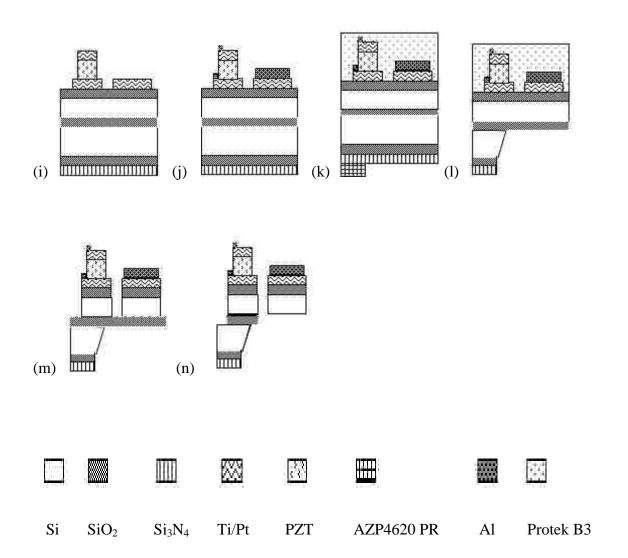


Figure 3.2. The fabrication process flow (continued). (i) Photolithography (second mask level) and dry etching of the bottom Pt/Ti layer. (j) Photolithography (third mask level) and lift-off process to form bonding pads. (k) Front side protection with ProtekTM B3, photolithography (fourth mask level), and consecutive wet etching of backside Si₃N₄ and SiO₂ layers. (l) Silicon substrate etching in KOH. (m) Removal of ProtekTM B3 and consecutive dry etching of top SiO₂ and silicon device layers from the front side. (n) Wet etching of buried SiO₂ to release the device.

Table 3.1. Specification of an SOI wafer used.

Thickness (µm) dev ¹ /box ² /sub ³	Type dev ¹ /sub ³	Orientation dev ¹ /sub ³	Diameter (mm)	Resistance (Ω cm) dev^1/sub^3
3 ±0.5 / 1 ±0.1 / 400 ±15	P/N	<100>/<100>	150.00 ± 0.20	0.01~0.02 / 1.00~30.0

dev¹: silicon device layer

box²: buried silicon dioxide layer

sub³: silicon substrate

3.1 Wafer Cleaning (Figure 3.1a)

The SOI wafer was cleaned in the following sequence:

1. Piranha cleaning

 $40\% \text{ H}_2\text{SO}_4: 30\% \text{ H}_2\text{O}_2 = 4:1 \text{ at } 90\% \text{ for } 20 \text{ minutes.}$

- 2. Acetone with ultrasonic agitation for 5 minutes, methanol with ultrasonic agitation for 5 minutes, and DI water rinse.
- 3. RCA cleaning
- a. RCA1 DI water : 27% $NH_4OH : H_2O_2 = 5:1:1$
 - i. In RCA1 solution at 70 ± 5 °C for 15 minutes to remove particulate contaminants and desorb trace metals (Au, Ag, Cu, Ni, etc).
 - ii. Rinse in DI water for 3 minutes.
 - iii. 49% HF: DI water = 1:10 at room temperature for 5 minutes.
 - iv. Rinse in DI water for 3 minutes.

b. RCA2 – DI water : 37% HCl : $H_2O_2 = 6:1:1$

i. In RCA2 solution at 70 ± 5 °C for 15 minutes to dissolve alkali ions and hydroxides of

Al³⁺, Fe³⁺, Mg³⁺ and desorb complex residual metals.

ii. Rinse in DI water for 5 minutes and dehydrate on a hot plate at 120°C for 10 minutes.

3.2 Growth of Isolation and Etching Mask Layers (Figure 3.1b-d)

The cleaned SOI wafers were loaded into an oxidation furnace (Axcess Integrated Loader

of MRL) to be thermally oxidized at 1000°C for 20 hours with flow rate of 2.5 sccm. 400 nm

silicon dioxide layers were grown on both sides.

It has been reported that silicon nitride is a more reliable and robust etching mask in

KOH etching than Cr, SU-8 photoresist, and silicon dioxide [2]. The etching selectivity of silicon

over LPCVD silicon nitride is more than 1000 in KOH etching. Therefore, 150 nm LPCVD

silicon nitride layers were grown on both sides of the wafer on top of the silicon dioxide layers at

the Nano Fabrication Center of University of Minnesota.

It has been also reported that PZT on Pt/Ti/SiO₂ is more dominated by (111) orientation

compared to that on Pt/Ti/Si₃N₄. Therefore, front side silicon nitride is preferred to be removed.

It was reported that S1813 photoresist hard baked at 185°C for 4.5 hours can protect the silicon

nitride on the backside during the front side silicon nitride etching in phosphoric acid at 155 ±

5°C for 1 hour [3.3]. Details are described below.

1. Coat S1813 on sample surface with the recipe in Appendix D.

2. Bake in oven at 185 $^{\circ}$ C for 4.5 hours.

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- 3. Etch silicon nitride in 80% phosphoric acid at $160 \, \text{C}$ for 1 hour. Etch rate is 0.2 $\mu \text{m/hour} [3.4]$.
- 4. Rinse in DI water and dry with nitrogen.
- 5. Strip backside S1813 photoresist by oxygen plasma (System VII) at 120 W for 1 hour.
- 6. Clean in piranha solution (98% H_2SO_4 : 30% H_2O_2 = 1:1) at 90 °C for 15 minutes to remove the S1813 photoresist residues.

3.3 Bottom Platinum Deposition (Figure 3.1e)

As mentioned earlier, piezoelectric material needs to be sandwiched by electrodes for operation. Pt is selected because of the lattice matching consideration with PZT. Ti is inserted to promote adhesion between Pt and the underlying SiO₂ as well as to prevent the Pt silicide formation [3.5]. Two different methods were attempted to deposit Pt/Ti: thermal evaporation and sputtering. The former was only partially successful.

3.3.1 Thermal Evaporation

There have been reports of e-beam evaporation of Pt thin film from many research groups [3.6]. However, due to limitation of the e-beam evaporator in the lab, thermal evaporation was tried instead. The chamber base pressure was 1×10^{-5} Torr and the current applied was about 20 A. Pt/Ti was deposited on the wafer with partial success. The major difficulty was the poor repeatability—the thickness of the deposited thin film varied too much from run to run for the similar amount of the source. The reason is thought to be too high boiling temperature of Pt, 3825° C, which makes it require high precision in terms of thermal energy supply.

3.3.2 Sputtering

An alternative method to deposit Pt/Ti layer is sputtering. The chamber base pressure was ~ 10⁻⁶ to 10⁻⁵ Torr, and working pressure was 1.3 mTorr. Deposition rate of Pt was 30 nm/min with 200 W DC, and that of Ti was 4 nm/min with 150 W RF when the samples were rotated inside the chamber. The target thicknesses were 150 nm for Pt and 10 nm for Ti. It is very important to obtain high base vacuum to achieve good quality of bottom seed Pt/Ti layer. Insufficient vacuum resulted in poor quality Pt/Ti which was delaminated during the PZT annealing process as shown in figure 3.3.

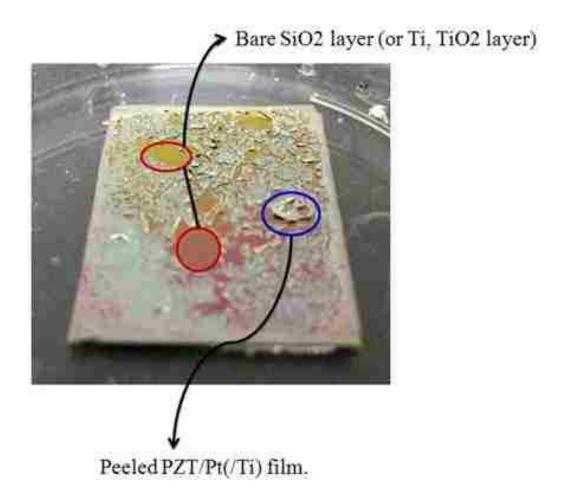


Figure 3.3. Delaminated films because of poor Pt/Ti quality.

3.4 PZT Layer Formation (Figure 3.1f)

Various techniques exist for PZT film deposition, such as sol-gel, RF planar magnetron sputtering, RF diode sputtering, electron beam evaporation, ion beam deposition, MOCVD, ECR, and laser ablation [3.4], with the first two methods being most commonly used. For its simple process and good film quality, the sol-gel method was selected for the current research. Since a single coating can only produce a film thickness of 100~200 nm from a purchased solgel solution (Type B, Inostek Inc., Korea), multiple coating technique was used to achieve a target thickness of 1 µm. The detailed process sequence is summarized in figure 3.4.

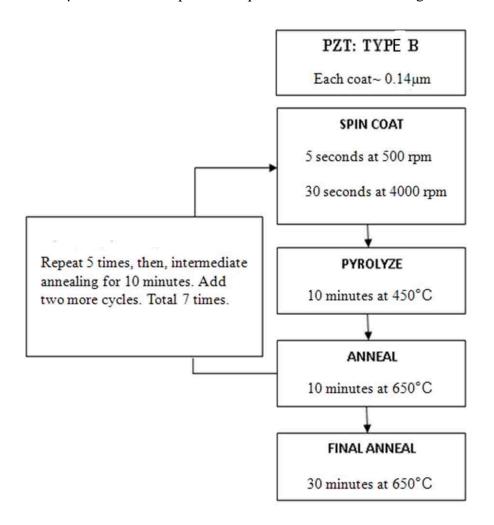


Figure 3.4. A PZT thin film process flow – multiple coating.

The freshness of the PZT solution is also fairly important. If the solution passes the shelf life or is exposed to air for too long, sedimentation appears in the solution, and the solution cannot be used any longer.

The crystal orientation of the PZT film was examined by the X-ray diffraction (XRD) technique, and the results will be presented in section 4.1. It was reported that the grain size at the PZT film surface is around 0.1 µm with well-defined grain boundaries [3.7-3.8]. To examine the grain size of the grown PZT film, scanning electron microscopy (SEM) was tried but it was the beyond the capability of the equipment available on campus.

3.5 Top Platinum Deposition and Patterning (Figure 3.1g)

The next step is to deposit and pattern the top electrodes on the sample $(PZT/Pt/Ti/SiO_2/SOI/SiO_2/Si_3N_4)$ by the lift-off process. The process sequence is as follows.

- Photolithography using the first mask level (APPENDIX C1) and S1813 photoresist. The
 details are provided in APPENDIX D. It is important to align the mask to <110>
 direction of the substrate as explained in section 2.3.
- 2. Descum S1813 photoresist in RIE with the following conditions:
 - O₂ plasma, 120 W RF, 250 mTorr, 3 minutes.
- 3. Deposit Pt/Ti by sputtering. However, to avoid deposition on the sidewall, samples are not rotated during deposition. The samples are loaded right above the target. Deposition conditions: Ti (10 nm) 150 W RF, 1 minute, and Pt (150 nm) 200 W DC, 1.25 minute.

- 4. Dip the sample in acetone with ultrasonic agitation for 10 minutes to lift off and form the patterned Pt/Ti on the PZT layer.
- 5. Dip the sample in methanol for 5 minutes, and then rinse with DI water for 3 minutes. Dry with N_2 .

Special care needs to be taken in regards to photoresist residues that may cause failure in the lift-off process as shown in figure 3.5 (a). Well-lifted-off patterns are shown in figure 3.5 (b) for comparison. A microimage after lift-off process is shown in figure 3.6.

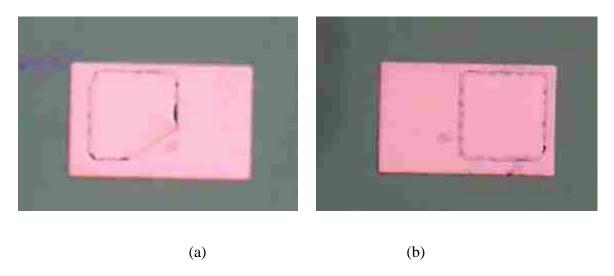


Figure 3.5. Microimages of test patterns. (a) Failed lift-off and (b) successful lift-off.

3.6 PZT Wet Etching (Figure 3.1h)

PZT can be etched either by a dry [3.9] or by a wet method [3.10]. In this thesis, the wet method was selected to avoid using toxic gases required in dry etching. Using patterned top platinum layer as an etching mask, the PZT layer was etched by the following sequence:

- 1. HCl (64%) + BOE (31%) + DI water (5%) for 5 minutes
- 2. HNO_3 : DI water = 2:1 for 2.5 minutes to remove PZT residues [3.10]

The etch rate in the step 1 is 0.25 µm/min at room temperature. Extra care needs to be given in terms of etching time because too much of over-etching may cause severe undercut in PZT and/or significant damage to the remaining PZT film.

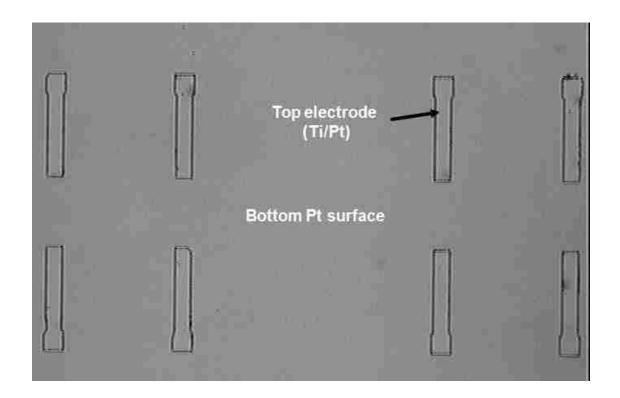


Figure 3.6. A microimage of top Pt/Ti electrodes.

3.7 Bottom Electrode Patterning and Etching (Figure 3.1i)

Pt can be etched either by a dry [3.11] or by a wet method [3.12]. Both methods were tried and the dry etching method was selected eventually. Since our facility does not have the capability to handle toxic gases, the samples were sent to an external facility for this step.

3.7.1 Wet Etching

Platinum is known to be very stable and highly resistant to most of the chemicals. It is also known that aqua regia (standard composition -37% HCl : 70% HNO₃ = 3:1) can etch Pt

[3.13, 3.14]. Etching of Pt in standard aqua regia was attempted at 85°C while the temperature was controlled by a heated water bath. Samples with Pt/Ti (150 nm/10 nm) layers were immersed in the etching solution. However, the etching result was extremely unpredictable. In one case, the total 150 nm of Pt was completely etched in 2 hours. But in other case, no clear

sign of etching was observed even for 6 hours—since Ti is etched in hot aqua regia in no time,

this clearly indicates that Pt has not been etched. Various etching results are shown in figure 3.7.

Meanwhile, various etching masks were tried for Pt etching in aqua regia. It was reported

that evaporated Cr is not etched in diluted aqua regia [3.15]. However, a 130 nm-thick Cr layer

was completely etched in aqua regia at 85°C within half an hour. It was also reported that SU-8

can be used as an etching mask. However, partial delamination of SU-8 was observed in aqua

regia (80°C) in 40 minutes. In conclusion, no suitable Pt wet etching mask was found.

3.7.2 Dry Etching

Several Pt dry etching methods have been reported, including reactive ion etching (RIE)

[3.16] and inductively-coupled plasma (ICP) RIE [3.9, 3.17]. Milkove et al. reported RIE etching

of Pt using Cl₂/Ar gas mix [3.16]. Even though increase of Ar concentration in the mix reduced

the Pt etch rate, it was reported that even 100% Ar can etch Pt in RIE. Due to unavailability of

Cl₂ in the lab, Pt RIE was attempted with 100% Ar. However, no etching occurred.

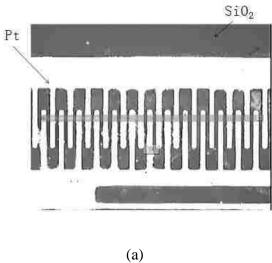
Therefore, Pt dry etching was pursued from an outside facility, the Nanolab facility at

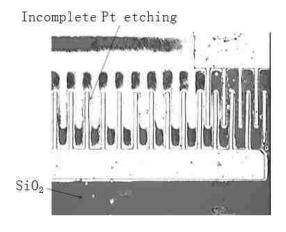
University of California at Los Angeles. The conditions of the ICP RIE are as follows.

• BCl_3 : $Cl_2 = 8:5$, working pressure: 10 mTorr

RIE: 150 W and ICP: 800 W

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(b)

Incomplete Pt etching (c)

Figure 3.7. Pt etching in aqua regia. (a) Well etched. (b) Incomplete etching. (c) Incomplete etching.

Photolithography was performed using the second mask level (APPENDIX C2) and AZP4620 photoresist. The details are provided in APPENDIX E. With the patterned photoresist as an etching mask, the bottom Pt/Ti layer was etched. Figure 3.8 shows microscanners after bottom platinum etching.

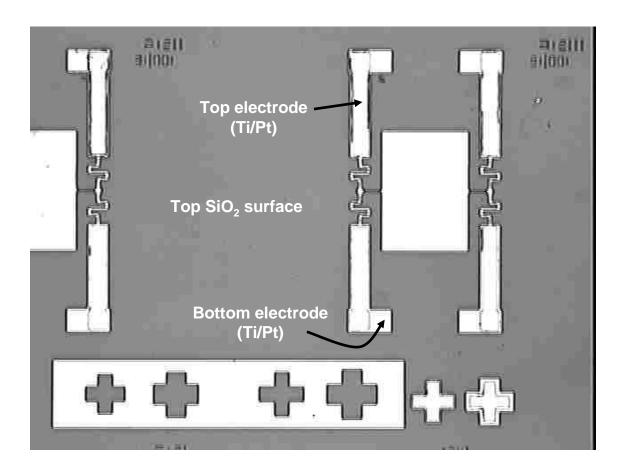


Figure 3.8. A microimage after bottom Pt/Ti etching by ICP RIE.

3.8 Photolithography with Double-Side Alignment for Silicon Substrate Etching and Etching of Backside Silicon Nitride (Figure 3.1k)

Backside silicon nitride was etched to create windows for silicon substrate etching. Double-side alignment was performed in the lithography to align the etching windows to the patterns on the front surface. For silicon nitride etching, both dry and wet methods were

considered. To avoid complication of front side protection, dry etching was chosen. Details are as follows.

S1813 was spin-coated on both sides using the same conditions as the earlier processes.
 The fourth mask level was aligned to the front side bottom Pt patterns. Double side alignment configuration is drawn in figure 3.9.

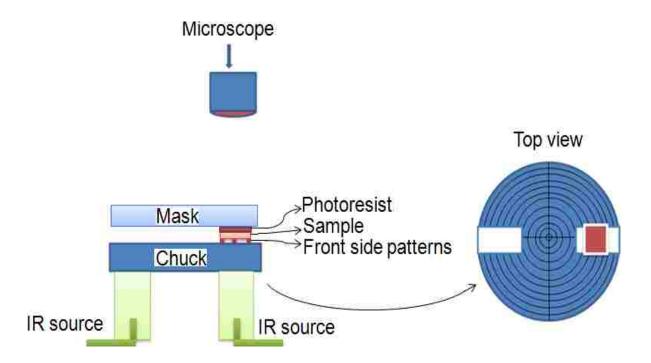


Figure 3.9. Double-side alignment lithography configuration.

2. Si₃N₄ was etched in RIE with the following conditions.

CF₄ flow rate: 100sccm, RF: 200 W, working pressure: 250 mTorr.

The estimated etch rate is 15 nm/min.

3.9 Front Surface Passivation (Figure 3.1k)

Front surface passivation is necessary to protect it from KOH during silicon substrate

etching. As mentioned earlier, ProTEK® B3 (Brewer Science Inc.) was selected and used. The process sequence recommended by the manufacturer is as follows.

1. ProTEK® B3 Primer Coating:

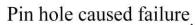
- Static dispense, accelerate at 1000 rpm/sec to final spin speed of 1500 rpm and spin for 60 seconds.
- ii. Bake at 205 $^{\circ}$ C for 60 seconds on a hot plate.

2. ProTEK® B3 Coating:

- i. Static dispense, acceleration at 1000 rpm/sec to final spin speed of 1500 rpm and spin for 60 seconds.
- ii. Bake at $140 \, \mathbb{C}$ for 120 seconds and then a final bake at $205 \, \mathbb{C}$ for 60 seconds on a hot plate.

The coated film was inspected under a microscope and no apparent defect was discovered. However, the film was delaminated and/or had some pinholes (figure 3.10) after being dipped in 30% wt KOH solution at 80% for 2 hours.

Two steps were taken to resolve this issue. The first was thorough cleaning. It was suspected that uncleanliness of the surface created pinholes in the Protek B3 material. The sample was cleaned by Trichloroethylene (TCE)-Acetone-Methanol-DI water cleaning process. Though there are other stronger cleaning processes available, due to the presence of metals, this metal cleaning process was selected. The second was double coating of ProTEK® B3—single ProTEK® B3 primer and double ProTEK® B3. Combination of these two methods helped to improve the quality of the protection layer. Delamination was limited to less than 3 mm from corners in 30%wt KOH solution at 80 °C for 7 hours which is enough to etch 400 µm of Si. Images of the ProTEK® B3 after this step are shown in figure 3.11.



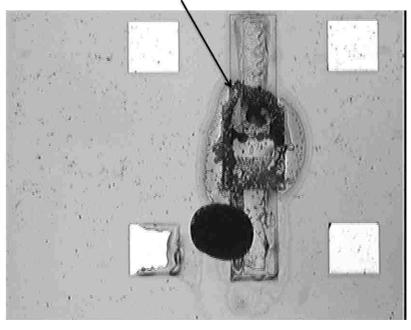
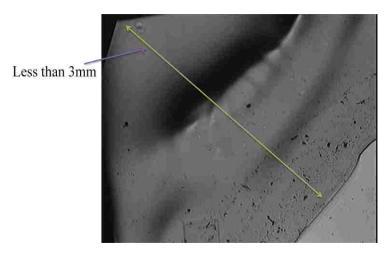
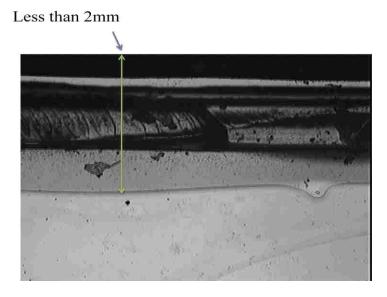


Figure 3.10. Pinhole-caused failure on a ProTEK® B3-coated silicon sample.



(a) Delamination of ProTEK® B3 layer from a corner.

Figure 3.11. Images of delamination of double-coated ProTEK® B3 after immersion in 30% wt KOH solution at 80% for 7 hours. (Figure to be continued on next page)



(b) Delamination of ProTEK® B3 layer from an edge.

3.10 Silicon Anisotropic Wet Etching (Figure 3.11)

Bulk silicon etching is a well-established process in MEMS technology. It can be done either by deep RIE or anisotropic wet etching. Comparison between these two methods is listed in table 3.2.

The wet etching method was selected for the current work. Table 3.3 shows a comparison between two commonly used silicon anisotropic wet etching solutions, KOH and TMAH [3.18]. KOH was selected for the current work for its better selectivity between (100) and (111) planes. Table 3.4 summarizes the dependence of the etch rate on the concentration and temperature of KOH [3.19, 3.20]. Based on this, the etching condition of 30% KOH at 80 °C was selected.

3.11 Structure Release

One of the most challenging steps in the current fabrication process is the structure release. Both wet release and dry release methods were considered. The former releases the structures by final wet etching of the buried oxide in the buffered oxide etch (BOE) solution (6

Table 3.2. Comparison between two bulk silicon etching methods.

	Anisotropic wet etching	Deep RIE (DRIE)
Mechanism	Pure chemical	Physical (ion bombardment) and chemical
Advantages	Low cost, easy to implement High etch rate Several materials available as good etching masks	 Capability of vertical etching for any pattern shape, insensitive to wafer orientation High etch rate Several materials available as good etching masks
Disadvantages	 Significant etching slope in (100) wafer, large footprint Potential of chemical handling hazards Complicacy in passivating the other surface. 	Requires expensive equipment Low throughput

Table 3.3. Comparison between TMAH and KOH as a silicon anisotropic wet etching solution.

	КОН	TMAH
	(34.0wt%, 70.9 ℃)	(20.0wt%, 79.8 ℃)
Etch rate	[µm/min]	[
(100) plane	0.629	0.603
(110) plane	1.292	1.114
(111) plane	0.009	0.017
Etching selectivity		
(100)/(110)	0.49	0.54
(100)/(111)	74	37
(110)/(111)	151	68

Table 3.4. Etch rate of (100) silicon in KOH (µm/min).

Temperature	KOH concentration				
(°C)	20%	30%	40%		
20	0.025	0.024	0.02		
40	0.188	0.108	0.088		
60	0.45	0.41	0.33		
80	1.4	1.3	1.1		
100	4.1	3.8	3.1		
Comment	The etch rate is the fastest.	The surface is smoother than the lower concentration.	The etch rate is higher than the higher concentration.		

parts 40% NH₄F and 1 part 49% HF), and the latter by final dry etching of the silicon device layer. For the dry etching process of the top silicon dioxide layer and the silicon device layer, common to the both release methods, different mixture of CF_4 and O_2 were tested aiming the

best selectivity between SiO₂ and Si. Based on the results as plotted in figure 3.12, 30% of the gas mixture was selected.

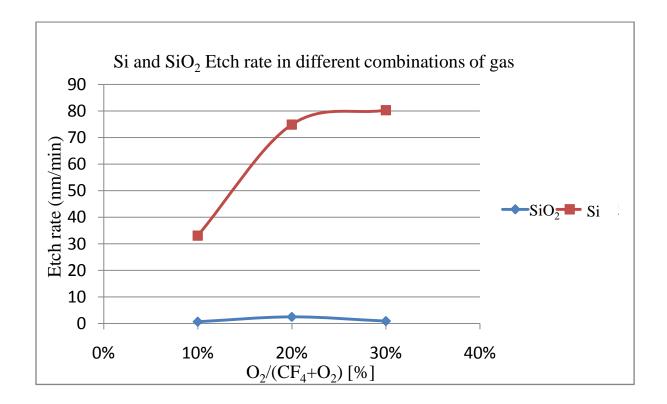


Figure 3.12. Etch rate of Si and SiO₂ with various combination of CF₄ and O₂.

3.11.1 Wet Release (Figure 3.1m-n)

Following steps were taken to wet-release the structures.

- 1. Remove ProTEK® B3 with the following sequence [3.21].
 - i. Bath 1: ACT® XT-1100 at 23 ℃ for 30 minutes.
 - ii. Bath 2: ACT® 412 at 80 ℃ for 20 minutes.
 - iii. IPA: 5 minutes.
 - iv. DI water: 2 minutes.
 - v. Air dry.

- 2. Remove the top silicon dioxide in BOE for 5 minutes.
- 3. Dry etch the silicon device layer.

 CF_4 : $O_2 = 7:3$, working pressure: 250 mTorr, and RF power: 200 W.

4. Structure release by etching the buried oxide layer in BOE for 7 minutes, DI water rinse, immersing in methanol, and air dry.

3.12 Dry Release (Figure 3.11a-d)

The major advantage of the dry release method is that the so-called "stiction problem" that causes structural damage during or after wet release due to the surface tension of water, can be avoided. Following steps were taken to dry-release the structures (figure 3.13).

- 1. Remove the buried silicon dioxide in BOE for 13 minutes.
- 2. Remove ProTEK® B3.
- 3. Remove the top silicon dioxide in BOE for 5 minutes.
- 4. Dry etch the silicon device layer.

 CF_4 : $O_2 = 7:3$, working pressure: 250 mTorr, and RF power: 200 W.

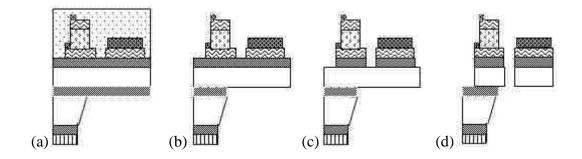
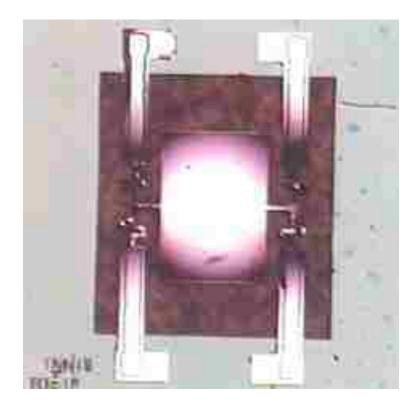


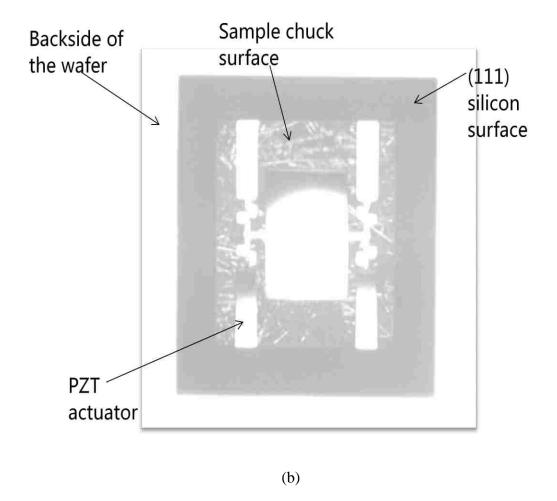
Figure 3.13. Process flow of the dry release method. (a) After silicon substrate etching in KOH, with the front side double protection ProTEK® B3 layer. (b) Buried silicon dioxide layer removal, and the front side protection layer removal. (c) Etching top silicon dioxide. (d) Etching front side silicon in RIE to finish the dry release step.

Eventually, because of the uniformity issue of the RIE equipment in the lab for silicon etching, the wet release method was selected. The images of the fabricated microscanner from top (figure 3.13a) and from bottom (figure 3.13b) after final release steps are shown in figure 3.13. Both images indicate that the released structure has non-negligible initial deformation due to significant residual stress. In the first fabrication trial, the connections between the hinges and mirrors were not strong enough to bear the weight of the mirrors, therefore, no intact microscanners were fabricated after the wet etch release process. Design changes were made to the connection parts in the second mask level, and many mirrors survived the release step in the second trial as shown in figure 3.14.



(a)

Figure 3.14. Images of the fabricated microscanner after final wet release viewed from (a) top and (b) bottom. (Figure continued on next page)



In this chapter, the details of the fabrication process flow have been presented. The bottom and top Pt/Ti electrodes were deposited by sputtering. The PZT layer was formed by the sol-gel method. During the anisotropic etching of the silicon substrate, the front side devices were protected by the double-coated ProTEK® B3 film. A double-side alignment lithography method was used to align the substrate etching windows on the backside to the front side patterns. Finally, the microscanners were released by etching the buried oxide layer in HF. The measurement results of the fabricated devices will be provided in the following chapter.

3.13 References

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CHAPTER 4. RESULTS

4.1 Characterization of the Deposited PZT Thin Film

Although the piezoelectric property of the deposited PZT thin film can be measured more accurately by direct methods such as pneumatic loading method, piezoresponse force microscopy (PFM), and laser double beam interferometry, indirect methods such as crystal orientation study and ferroelectricity measurement were used for qualitative study of the deposited film.

4.1.1 Crystal Orientation Study

To study crystal orientation of a substrate, X-ray diffraction (XRD) is commonly used. The principle of XRD measurement is based on Bragg's Law. Diffraction occurs when waves interact with a regular structure whose period is about the same as the wavelength. XRD is used in the atomic arrangement study because X-rays have wavelengths on the order of a few angstroms, which is comparable to typical interatomic distances in crystalline solids. When the necessary geometric requirements are met, X-ray scattering from a crystalline material will constructively interfere, producing a diffracted beam. By Bragg's law, the angle θ of this diffraction has the following relation with the interatomic spacing of the material d.

$$n\lambda = 2d\sin\theta$$
, (4.1)

where λ is the wavelength of X-ray, and n is any integer. In XRD measurement, the intensity of the diffracted X-ray is recorded as a function of a 2θ , and the plot of this information is known as the diffraction pattern. Figure 4.1 shows the diffraction pattern of the deposited PZT film. It has a strong peak in 38.2 degree, which corresponds to (111) PZT.

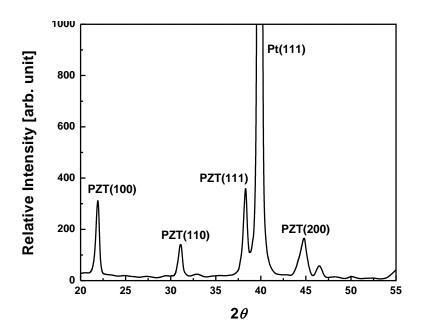


Figure 4.1. X-ray diffraction pattern of a PZT film on Pt/Ti/SiO₂/(100)Si.

4.1.2 Polarization-Voltage (P-V) Measurement

To examine ferroelectricity of the deposited PZT film, *P-V* measurement was performed. A schematic diagram of the measurement setup for the metal-PZT-metal capacitor is depicted in figure 4.2. It includes polarization measurement equipment, RT66B (Radiant Technologies, Inc.) The strong hysteresis shown in the measured *P-V* curve (figure 4.3) indicates that the deposited PZT film has the piezoelectric property.

4.1.3 Breakdown Voltage Measurement

Breakdown voltage of the PZT film was measured to determine the maximum voltage that can be applied across the film. Twenty PZT capacitors of which layers are Pt (150 nm)/Ti (10 nm)/PZT (1 μ m)/Pt (150 nm)/Ti (10 nm) were tested. The average breakdown voltage was 74.8 V, with the minimum being 58 V. Therefore, it is safe to apply less than 58 V to the 1 μ m-thick PZT layer.

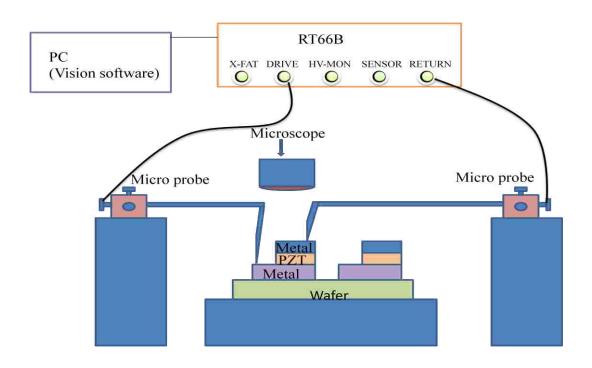


Figure 4.2. Setup for *P-V* measurement.

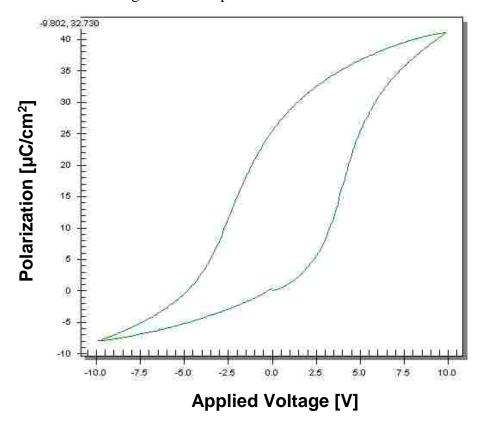


Figure 4.3. *P-V* hysteresis curve of a PZT film on Pt/Ti/SiO₂/(100)Si.

4.2 Piezoelectric Cantilevers

PZT cantilevers were actuated with AC voltage (10 V_{pp} , 6 Hz). Images of a cantilever before and during actuation are presented in figure 4.4.

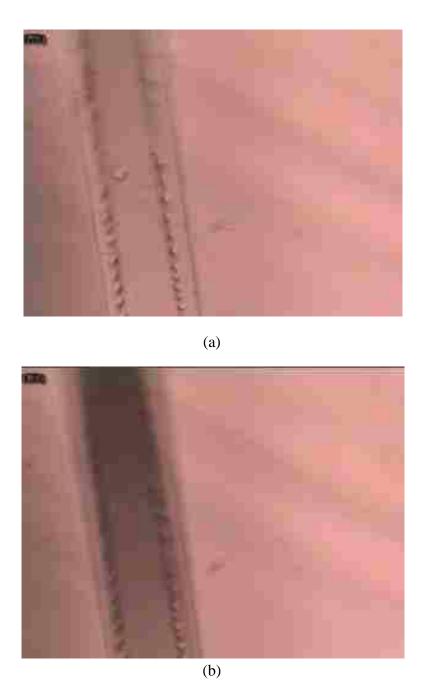


Figure 4.4. Images of a PZT cantilever, (a) before and (b) after applying AC voltage (10 V_{pp} , 6 Hz).

Residual-stress-induced initial deformations of the PZT cantilever test structures were examined under a microscope. Deformation at the tip of the cantilever was roughly measured by adjusting the focus of the image, and using the known step height as a reference. Figure 4.5 shows the tip deformations of two types of cantilevers measured by this method—one with Pt (150 nm)/Ti (10 nm)/SiO₂ (400 nm)/Si (3 µm) and the other with Pt (150 nm)/Ti (10nm)/PZT (1 µm)/Pt (150 nm)/Ti (10 nm)/SiO₂ (400 nm)/Si (3 µm). This result indicates that increasing the silicon device layer will reduce the stress-induced initial deformation.

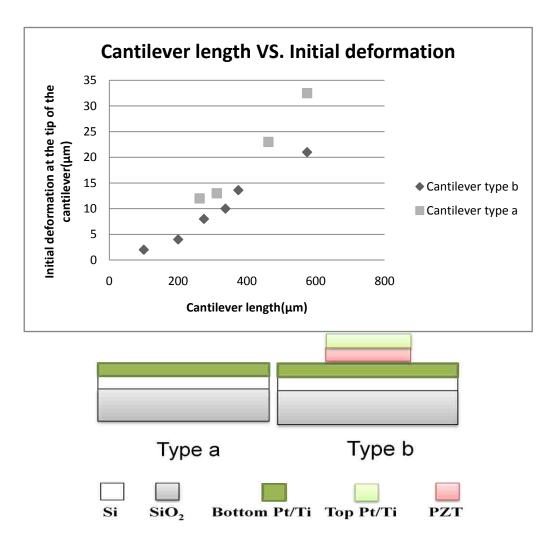


Figure 4.5. Stress-induced initial deformation at the tip vs. length of the PZT cantilevers. Cantilever type a: Pt (150 nm)/Ti (10 nm)/SiO₂ (400 nm)/Si (3 μ m), and cantilever type b: Pt (150 nm)/Ti (10nm)/PZT (1 μ m)/Pt (150 nm)/Ti (10 nm)/SiO₂ (400 nm)/Si (3 μ m).

In summary, both X-ray diffraction and *P-V* measurement results indicate the presence of strong piezoelectricity in the deposited PZT layer. The fabricated piezoelectric cantilevers were actuated by applying low-frequency ac voltages.

CHAPTER 5. SUMMARY AND FUTURE WORK

In this thesis, two-dimensional microscanners with novel T-shaped hinges and piezoelectric actuators were proposed for optical coherence tomography applications. Incorporation of the T-shaped hinges is to improve the conversion efficiency from deflection of the piezoelectric actuators to two-dimensional rotation of the mirror attached to them. The microscanners have been designed and simulated using a finite-element-method-based numerical simulation program, ANSYSTM. It was estimated that more than $\pm 7^{\circ}$ of mechanical tilt angles can be achieved in two dimensions at the maximum voltage of 30 V by the simulation. PZT was selected as the piezoelectric material for its strong piezoelectric effect and the sol-gel method was used to produce 1 µm-thick PZT layer. Pt/Ti was used for the two (top and bottom) electrodes for the PZT actuation, which was deposited by sputtering system. X-ray diffraction was used to examine the crystal orientation of the deposited PZT film which showed strong (111) orientation that is desirable for good piezoelectric effect. RT66B was used to measure the P-V characteristics of the metal-PZT-metal capacitors. Strong hysteresis curves were observed from the fabricated capacitors. In the KOH silicon bulk etching step, silicon nitride was used as an etching mask, and ProTEK® B3 functioned as a protection layer of the front side.

The entire fabrication process has been run several times. However, mechanical operation of the microscanners is yet to be demonstrated. One reason is considered to be insufficient piezoelectric constant of the coated PZT layer. It was reported that poling can enhance the piezoelectric effect [5.1-5.2]. The conditions of the poling process (figure 5.1) suggested by the maker of the sol-gel solution are

• DC voltage: 10-15V

• Temperature and duration: 120 ℃ for 5 minutes.

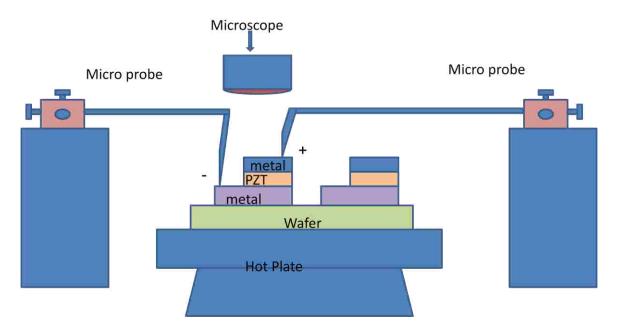


Figure 5.1. The poling setup.

5.1 References

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APPENDIX A. ANSYS PROGRAM CODE FOR A PIEZOELECTRIC CANTILEVER STRUCTURE

! Bimorph deformation calculation with PZT	
FINISH	
/CLE	
/TITLE,PZT Bimorph	
/PMETH,OFF,1	
KEYW,PR_SET,1	
KEYW,PR_STRUC,1	
KEYW,PR_THERM,0	
KEYW,PR_FLUID,0	
KEYW,PR_ELMAG,1	
KEYW,MAGNOD,0	
KEYW,MAGEDG,0	
KEYW,MAGHFE,0	
KEYW,MAGELC,1	
KEYW,PR_MULTI,0	
KEYW,PR_CFD,0	
/COM uMKS unit	
! Define design parameters	
1=390	! Length of the bimorph
w=100	! Width of the bimorph
t_si=3	! Thickness of the lower layer (silicon)

 $t_pzt=1$

! Thickness of the upper layer (PZT)

Y_si=169e3

! Young's modulus of silicon = 169GPa

V1=30

! Drawing the structures

/PREP7

block, 0, w, 0, 1, 0, t_si

! Lower layer (silicon)

block, 0, w, 0, 1, t_si, t_pzt+t_si

! Upper layer (PZT)

vglue, 1, 2

! Define material properties and element type

ET, 1, 92

! 3-D 10-Node tetrahedral structural solid

ET, 2, 98, 3

! 3-D tetrahedral coupled-field solid, ux, uy,

uz, volt

mp, ex, 1, Y_si

! Material definition for silicon

emunit, epzro, 8.854e-6

Tb, anel, 2

! Material definition for PZT

Tbdata, 1, 11.96e4, 7.438e4, 7.451e4

! Anisotropic elastic material stiffness

Tbdata, 7, 11.96e4, 7.451e4

Tbdata, 12, 11.04e4

Tbdata, 16, 2.262e4

Tbdata, 19, 2.105e4

Tbdata, 21, 2.105e4

Tb, piez, 2

! e matrix $[C/m^2] = [pC/um^2]$

Tbdata, 1, 0, 0, -5.3096

Tbdata, 4, 0, 0, -5.2028

Tbdata, 7, 0, 0, 15.8153

Tbdata, 10, 0, 0, 0

Tbdata, 13, 0, 12.2947, 0

Tbdata, 16, 12.2947, 0, 0

mp, perx, 2, 918

mp, pery, 2, 918

mp, perz, 2, 827

allsel

vsel, s, volu, , 1

vatt, 1, 1, 1

vsel, s, volu, , 3

vatt, 2, 1, 2

allsel

!Mesh

smrt, 10 MSHKEY,0 ! free meshing (mapped meshing is 1) MSHAPE, 1, 3-D ! tetrahedral for 3-D vmesh,all finish /solu /com voltage loading ! Apply voltage on PZT layer nsel, s, loc, z, t_si d, all, volt, 0 nsel, s, loc, z, t_si+t_pzt d, all, volt, V1 allsel asel, s, loc, y, 0 da, all, ux, 0 ! Fix the anchored surface in angle and translation da, all, uy, 0 da, all, uz, 0 /STATUS, SOLU **SOLVE**

finish

/POST1

set, last

!/VSCALE,1,0.1,1

/EFACET,1

PLNSOL, U,Z, 0,1.0

APPENDIX B. ANSYS PROGRAM CODE FOR THE MICROSCANNER

FINISH

/CLE	
/TITLE,PZT scanner	
/PMETH,OFF,1	
KEYW,PR_SET,1	
KEYW,PR_STRUC,1	
KEYW,PR_THERM,0	
KEYW,PR_FLUID,0	
KEYW,PR_ELMAG,1	
KEYW,MAGNOD,0	
KEYW,MAGEDG,0	
KEYW,MAGHFE,0	
KEYW,MAGELC,1	
KEYW,PR_MULTI,1	
KEYW,PR_CFD,0	
/COM uMKS unit	
! Define design parameters	
L_mirror=700	! Length of the mirror
W_mirror=500	! Width of the mirror
L_bridge=100	! Length of the bridge between the mirror and the T-hinge
W_bridge=20	! Width of the bridge
L_act=390	! Length of the actuator
W_act=100	! Width of the actuator
L_mid=38	! Length of the middle section of the T-hinge 73

W_mid=38

! Width of the middle section of the T-hinge

L_h=120

! Length of the spring

W_h=18

! Width of the spring

L 1=40

 $L_2=L_mid/2+L_1$

 $L_3=L_2+5*W_h+L_1$

W_1=W_mirror/2+L_bridge+W_mid/2

 $t_si=3$

! Thickness of the lower layer (silicon)

 $t_pzt=1$

! Thickness of the upper layer (PZT)

Y_si=169e3

! Young's modulus of silicon = 169GPa

V1=30

V2 = 0

V3 = 0

V4=-30

! Drawing the structures

/PREP7

/COM Left-hand-side actuators (1 and 2)

block, -W_mid/2-W_1, W_mid/2-W_1, -L_mid/2, L_mid/2, 0, t_si

block, -W_h/2-W_1, W_h/2-W_1, L_mid/2, L_2+W_h, 0, t_si

block, -W_h-L_h/2-W_1, -W_h/2-W_1, L_2, L_2+W_h, 0, t_si

block, -W_h-L_h/2-W_1, -L_h/2-W_1, L_2+W_h, L_2+3*W_h, 0, t_si

block, -L_h/2-W_1, L_h/2-W_1, L_2+2*W_h, L_2+3*W_h, 0, t_si

block, L_h/2-W_1, L_h/2+W_h-W_1, L_2+2*W_h, L_2+4*W_h, 0, t_si

block, -W_h/2-W_1, L_h/2+W_h-W_1, L_2+4*W_h, L_2+5*W_h, 0, t_si

block, -W_h/2-W_1, W_h/2-W_1, L_2+5*W_h, L_3, 0, t_si

block, -W_act/2-W_1, W_act/2-W_1, L_3, L_3+L_act, 0, t_si

block, -W_act/2-W_1, W_act/2-W_1, L_3, L_3+L_act, t_si, t_si+t_pzt

block, -W_h/2-W_1, W_h/2-W_1, -L_2-W_h, -L_mid/2, 0, t_si

block, -W_h-L_h/2-W_1, -W_h/2-W_1, -L_2-W_h, -L_2, 0, t_si

block, -W_h-L_h/2-W_1, -L_h/2-W_1, -L_2-3*W_h, -L_2-W_h, 0, t_si

block, -L_h/2-W_1, L_h/2-W_1, -L_2-3*W_h, -L_2-2*W_h, 0, t_si

block, L_h/2-W_1, L_h/2+W_h-W_1, -L_2-4*W_h, -L_2-2*W_h, 0, t_si

block, -W_h/2-W_1, L_h/2+W_h-W_1, -L_2-5*W_h, -L_2-4*W_h, 0, t_si

block, -W_h/2-W_1, W_h/2-W_1, -L_3, -L_2-5*W_h, 0, t_si

block, -W_act/2-W_1, W_act/2-W_1, -L_3-L_act, -L_3, 0, t_si

block, -W_act/2-W_1, W_act/2-W_1, -L_3-L_act, -L_3, t_si, t_si+t_pzt

/COM Right-hand-side actuators (3 and 4)

block, -W_mid/2+W_1, W_mid/2+W_1, -L_mid/2, L_mid/2, 0, t_si

block, -W_h/2+W_1, W_h/2+W_1, L_mid/2, L_2+W_h, 0, t_si

block, -W_h-L_h/2+W_1, -W_h/2+W_1, L_2, L_2+W_h, 0, t_si

block, -W_h-L_h/2+W_1, -L_h/2+W_1, L_2+W_h, L_2+3*W_h, 0, t_si

block, -L_h/2+W_1, L_h/2+W_1, L_2+2*W_h, L_2+3*W_h, 0, t_si

block, L_h/2+W_1, L_h/2+W_h+W_1, L_2+2*W_h, L_2+4*W_h, 0, t_si

block, -W_h/2+W_1, L_h/2+W_h+W_1, L_2+4*W_h, L_2+5*W_h, 0, t_si

block, -W_h/2+W_1, W_h/2+W_1, L_2+5*W_h, L_3, 0, t_si

block, -W_act/2+W_1, W_act/2+W_1, L_3, L_3+L_act, 0, t_si

block, -W_act/2+W_1, W_act/2+W_1, L_3, L_3+L_act, t_si, t_si+t_pzt

block, -W_h/2+W_1, W_h/2+W_1, -L_2-W_h, -L_mid/2, 0, t_si

block, -W_h-L_h/2+W_1, -W_h/2+W_1, -L_2-W_h, -L_2, 0, t_si

block, -W_h-L_h/2+W_1, -L_h/2+W_1, -L_2-3*W_h, -L_2-W_h, 0, t_si

block, -L_h/2+W_1, L_h/2+W_1, -L_2-3*W_h, -L_2-2*W_h, 0, t_si

block, L_h/2+W_1, L_h/2+W_h+W_1, -L_2-4*W_h, -L_2-2*W_h, 0, t_si

block, -W_h/2+W_1, L_h/2+W_h+W_1, -L_2-5*W_h, -L_2-4*W_h, 0, t_si

block, -W_h/2+W_1, W_h/2+W_1, -L_3, -L_2-5*W_h, 0, t_si

block, -W_act/2+W_1, W_act/2+W_1, -L_3-L_act, -L_3, 0, t_si

block, -W_act/2+W_1, W_act/2+W_1, -L_3-L_act, -L_3, t_si, t_si+t_pzt

/COM Mirror and the bridges

block, -W_mirror/2, W_mirror/2, -L_mirror/2, L_mirror/2, 0, t_si

block, -W_mirror/2-L_bridge, -W_mirror/2, -W_bridge/2, W_bridge/2, 0, t_si

block, W_mirror/2, W_mirror/2+L_bridge, -W_bridge/2, W_bridge/2, 0, t_si

vglue, all

! Define material properties and element type

1 1

ET, 2, 5, 3 uz, volt

ET, 1, 45

mp, ex, 1, Y_si

! 3-D 10-Node tetrahedral structural solid

! 3-D tetrahedral coupled-field solid, ux, uy,

! Material definition for silicon

emunit, epzro, 8.854e-6

Tb, anel, 2

Tbdata, 1, 11.96e4, 7.438e4, 7.451e4

Tbdata, 7, 11.96e4, 7.451e4

Tbdata, 12, 11.04e4

Tbdata, 16, 2.262e4

Tbdata, 19, 2.105e4

! Material definition for PZT

! Anisotropic elastic material stiffness

Tbdata, 21, 2.105e4

Tb, piez, 2

! e matrix $[C/m^2] = [pC/um^2]$

Tbdata, 1, 0, 0, -5.3096

Tbdata, 4, 0, 0, -5.2028

Tbdata, 7, 0, 0, 15.8153

Tbdata, 10, 0, 0, 0

Tbdata, 13, 0, 12.2947, 0

Tbdata, 16, 12.2947, 0, 0

mp, perx, 2, 918

mp, pery, 2, 918

mp, perz, 2, 827

allsel

vsel, s, volu, , 40, 49

vsel, a, volu, , 54, 80

vatt, 1, 1, 1

allsel

vsel, s, volu, , 50, 53

vatt, 2, 1, 2

! vatt, mat, real, type

allsel

lsel, s, loc, z, 0

lsel, a, loc, z, t_si

lsel, r, loc, x, -W_mirror/2-1, W_mirror/2+1

lsel, r, loc, y, -L_mirror/2-1, L_mirror/2+1

lesize, all, , , 10

allsel

vsweep, all

finish

/solu

/com voltage loading

nsel, s, loc, z, t_si

nsel, r, loc, x, $-W_1-W_act$, $-W_1+W_act$

nsel, r, loc, y, -L_3-L_act,-L_3

d, all, volt, 0

nsel, s, loc, z, t_si+t_pzt

nsel, r, loc, x, $-W_1-W_act$, $-W_1+W_act$

nsel, r, loc, y, -L_3-L_act,-L_3

d, all, volt, V1

nsel, s, loc, z, t_si

 $nsel,\,r,\,loc,\,x,\,-W_1-W_act,\,-W_1+W_act$

! Apply voltage loading to each actuator

nsel, r, loc, y, L_3, L_3+L_act d, all, volt, 0

d, all, volt, V2

$$\label{eq:nsel} \begin{split} & nsel,\, s,\, loc,\, z,\, t_si+t_pzt \\ & nsel,\, r,\, loc,\, x,\, -W_1-W_act,\, -W_1+W_act \\ & nsel,\, r,\, loc,\, y,\, L_3,\, L_3+L_act \end{split}$$

nsel, s, loc, z, t_si
nsel, r, loc, x, W_1-W_act, W_1+W_act
nsel, r, loc, y, -L_3-L_act, -L_3
d, all, volt, 0

nsel, s, loc, z, t_si+t_pzt

nsel, r, loc, x, W_1-W_act, W_1+W_act

nsel, r, loc, y, -L_3-L_act, -L_3

d, all, volt, V3

nsel, s, loc, z, t_si
nsel, r, loc, x, W_1-W_act, W_1+W_act
nsel, r, loc, y, L_3, L_3+L_act
d, all, volt, 0

nsel, s, loc, z, t_si+t_pzt

nsel, r, loc, x, W_1-W_act, W_1+W_act

nsel, r, loc, y, L_3, L_3+L_act

d, all, volt, V4

allsel

asel, s, loc, y, L_3+L_act

asel, a, loc, y, -L_3-L_act

da, all, ux, 0

da, all, uy, 0

da, all, uz, 0

! Fix the anchored surface in angle and translation

/STATUS, SOLU

SOLVE

finish

/POST1

set, last

/EFACET,1

PLNSOL, U,Z, 0,1.0

allsel

nsel, s, loc, x, 0

nsel, r, loc, y, L_mirror/2

 $nsel,\,r,\,loc,\,z,\,t_si$

```
*get, n_top, node, 0, num, max
```

allsel

nsel, s, loc, x, 0

nsel, r, loc, y, -L_mirror/2

nsel, r, loc, z, t_si

*get, n_bottom, node, 0, num, max

*get, z_bottom, node, n_bottom, u, z

allsel

nsel, s, loc, x, -W_mirror/2

nsel, r, loc, y, 0

nsel, r, loc, z, t_si

*get, n_left, node, 0, num, max

*get, z_left, node, n_left, u, z

allsel

nsel, s, loc, x, W_mirror/2

nsel, r, loc, y, 0

nsel, r, loc, z, t_si

*get, n_right, node, 0, num, max

*get, z_right, node, n_right, u, z

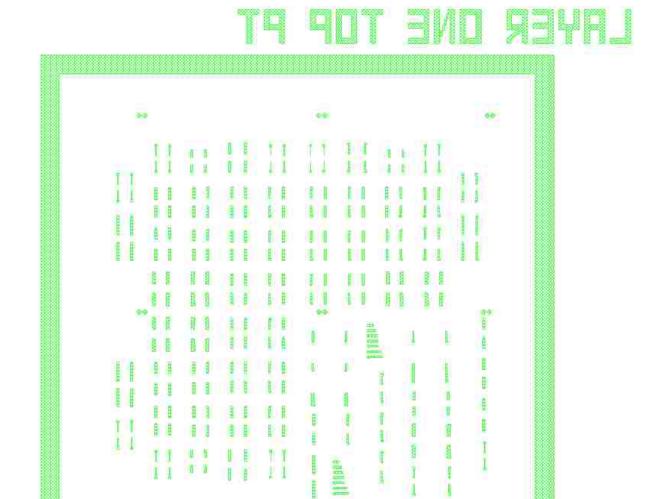
 $angle_i = 57.3* (z_bottom - z_top) / L_mirror$ $angle_o = 57.3* (z_right - z_left) / W_mirror$

! Express the bending of mirror in degree

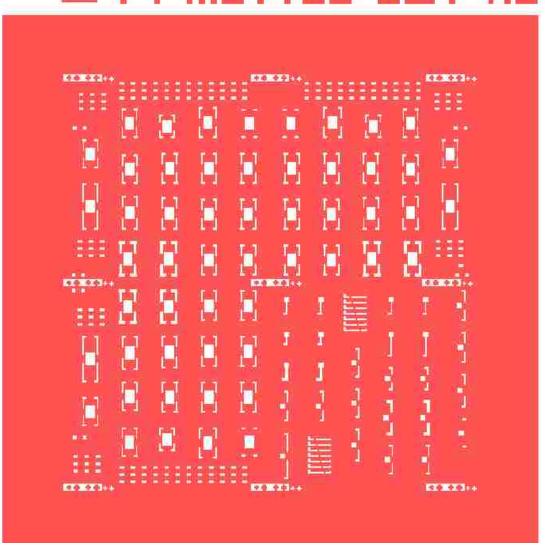
/color, wbak, white /plopts, logo, off /replot

*stat

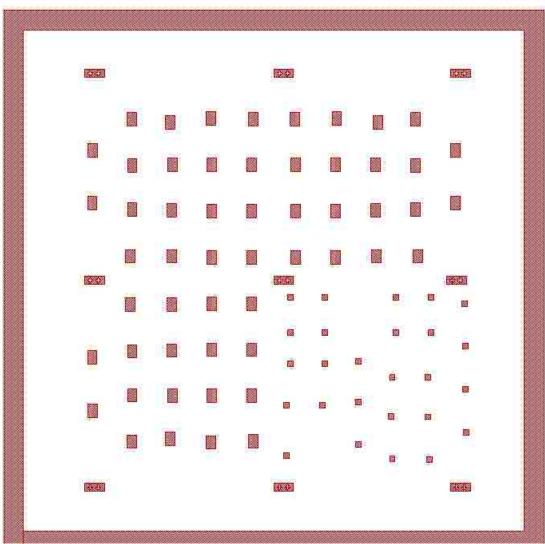
APPENDIX C1. LEVER 1 MASK LAYOUT



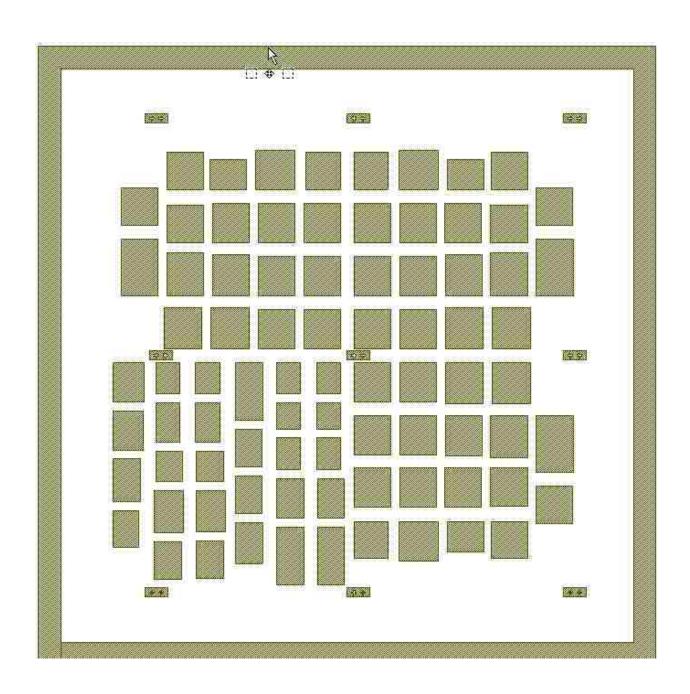
APPENDIX C2. LEVER 2 MASK LAYOUT



APPENDIX C3. LEVEL 3 MASK LAYOUT



APPENDIX C4. LEVEL 4 MASK LAYOUT



APPENDIX D. PHOTOLITHOGRAPHY PROCESS CONDITIONS WITH THE POSITIVE PHOTORESIST, S1813

- 1. Spin-coating of S1813 starts at 500 rpm for 10 seconds.
- 2. Ramp up the spinning speed to 2500rpm and stay for 40 seconds.
- 3. Soft bake at $115 \, \text{°C}$ for 3 minutes.
- 6. UV exposure for 12 seconds at room temperature (Quintel aligner).
- 7. Develop in MF 319 for 40 seconds.
- 8. Rinse in DI water for 3 minutes.
- 9. Dry with N_2 .

APPENDIX E. PHOTOLITHOGRAPHY PROCESS CONDITIONS WITH THE POSITIVE PHOTORESIST, AZP 4620

- 1. Spin-coating of AZP 4620 starts at 300rpm for 3 seconds.
- 2. Ramp up the spinning speed to 2500rpm and stay for 60 seconds.
- 3. Soft bake at 90 $^{\circ}$ C for 2 minutes 45 seconds.
- 4. UV exposure for 40 seconds at room temperature (Quintel aligner).
- 5. Develop in AZ 400K : DI water = 1:3 for 1 minute.
- 6. Rinse in DI water.
- 7. Dry with N_2 .

VITA

Wenyu Song was born in Jilin province of People's Republic of China in December, 1982. She obtained her Bachelor of Science degree in Electrical and Information Department and Bachelor of Art degree in the Department of Business English from Jilin University, Jilin, P.R.China, in June 2004. She is expecting her Master of Science in Electrical Engineering degree from Louisiana State University, Baton Rouge, Louisiana, in May, 2009. Her master's research area is optical MEMS and micro actuators.