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FABRICATION OF SINGLE WALLED CARBON NANOTUBE (SW-CNT) CANTILEVERS FOR CHEMICAL SENSING

A Thesis

Submitted to the Graduate Faculty of the
Louisiana State University and
Agricultural and Mechanical College
In partial fulfillment of the
requirements for the degree of
Master of Science in Electrical Engineering

In
The Department of Electrical and Computer Engineering

By
Jui-Ching Hsu
B.S., National Taiwan University
Taipei, Taiwan, 2002
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With the blessing of the GOD, I can keep myself with high motivation and pursuit my happiness in this Electronic field.

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ABSTRACT

With the discovery of carbon nanotubes (CNTs), many applications have been implemented based on their unique electronic, mechanical, chemical and optoelectronic properties. One area of applications is in gas sensors for detecting, oxygen, flammable and toxic gases. In our work, the focus is on the fabrication of carbon nanotube (CNT) cantilever sensors for integration with CMOS readout chip which offer increased sensitivity. The higher surface-to-bulk ratio enhances the property and performance of the gas sensor by nanocantilevers. In this work, we present the detection method based on the change in capacitance of the single walled carbon nanotube (SWCNT) cantilever.

Carbon nanotubes are capable of interacting with the gaseous species either directly or indirectly by using a polymer analyte coated on its surface. The capacitance variation technique of measuring cantilever deflection was used to measure the bending rate. The capacitance between the cantilever and the fixed electrode varies as a function of the magnitude of the bending of the cantilever which is in turn proportional to the concentration of the gas species in the surrounding environment. To measure the variation in the capacitance value, the CNT cantilever beam is considered as one of the electrodes of the capacitor and the metal film as the other. The air between the plates acts as the dielectric material.

Simulations including both ANSYS for nanocantilevers and SPICE for CMOS readout chip and experimental results are presented in this research. Integration and packaging issues are also discussed in our research.

CHAPTER 1
INRODUCTION

1.1 Motivation

Since carbon nanotubes (CNTs) have been discovered by S. Iijima in 1991 [1], many novel applications have been implemented based on their unique electronic, mechanical, chemical and optoelectronic [2] properties. Carbon nanotubes have great potential for the applications of electronic devices, especially for the single-walled carbon nanotubes' (SWCNT) applications in nanoscale.

In the modern world, people are more sensitive to protecting themselves and the environment; the demand for sensors is thus steadily increasing. Chemical sensors and gas sensors have been widely used in areas such as, homeland security, automotive, industry and environmental control to monitor the distribution of chemical and gas concentration. The current gas sensors are needed for 1) oxygen, 2) flammable gases and 3) toxic gases. For example, carbon monoxide (CO) sensors are used to detect the concentration of CO in environment. As many American homes have fireplaces and attached garages, the CO sensors can alert people and prevent them from staying in the high CO environments. The main advantages of gas sensors over the analytical methods for sensing target gases are: low cost, low power, compact size and ability to integrate with readout electronics [3, 4]. In this work, the focus is on the design of a single chip chemical detection system in CMOS that integrates carbon nanotube (CNT) nanocantilever sensors which offer increased sensitivity [5]. The enhancement of the property and performance of gas sensors by nanocantilevers is due to higher surface-to-bulk ratio [5].

Cantilever also plays an important role in the integration of the sensor, the signal conditioning and wireless telemetry on the same chip [6]. Cantilever sensors based on frequency variation have been known of for a long time. MEMS (Micro-Electro-Mechanical System) technology has added a new dimension to cantilever sensor technology, which has now advanced to commercially available microcantilevers sensors for chemical, physical and biological detection with increased sensitivity. A wide variety of highly sensitive physical, biological and chemical sensors have been fabricated and are based upon the deflection and resonant frequency variation of microcantilevers when exposed to vapor [7].

Several methods have been presented to detect the signal. These methods include the switched-capacitor based readout technique [8, 9], a ring oscillator [10, 11], analog-to-digital conversion [12], diode-quad circuit [13] and voltage to frequency conversion [14]. A sensitive external circuit [15] which can detect the output voltage or shift in frequency has been used to measure the difference between the reference capacitance and the change of capacitance. In this work, we present the detection method for the change of capacitance.

1.2 Literature Survey

Carbon nanotubes have many special properties; there is a lot of research that focuses on the applications of carbon nanotubes. Using carbon nanotubes in gas sensor mechanisms is a brand new technology; CNTs can provide a more sensitive detection limit and a shorter response time [16]. Based on these findings, we choose CNTs as a detection material to measure the concentration of gases. This application will be the main stream for gas sensors in the future.

Several design techniques are using the principle of switched-capacitor (SC), including the switched-capacitor rectifiers [17], filters and sensors. Low power consumption and easy implementation mean the switched-capacitor has wide applications. In the switched-capacitor circuits, diodes have been used as the switching element on the circuit. Recently, researchers have used MOS transistors for the on-off switching. The CMOS bridge circuit [18, 19] is one of the most popular examples for the MOS application.

1.3 Overview of the Research

This thesis is divided in seven chapters. The first chapter has a brief introduction of the thesis and the basic concepts of the research. A detailed explanation of this research is given in Chapter 2, which also includes the properties of carbon nanotube cantilever beams and the basic concepts of switched-capacitor and capacitive sensor. Chapter 3 includes the design and simulation of cantilevers and Chapter 4 focuses on the fabrication. The circuit simulation and layout design are described in Chapter 5. Packaging issues are discussed in Chapter 6. Future work and conclusions are included in Chapter 7.

CHAPTER 2
PRINCIPLE OF CHEMICAL DETECTION USING CNT NANOCANTILEVERS

2.1 Introduction of Carbon Nanotubes (CNTs)

Since the discovery of carbon nanotubes in 1991 by Iijima [1], the structure of carbon nanotubes have been studied extensively. Currently, carbon nanotubes are grown in different forms from regular cones to other shapes. CNTs are available in multi-walled and single-walled shapes. In our research, we will focus on use of single-walled carbon nanotube (SWCNT) structure. Also the properties of CNTs have semiconductor and metallic CNTs. Figure 2.1 shows the image of SWCNTs tangles together. SWCNTs have three different chiralities: (a) armchair structure, (b) zigzag structure and (c) chiral structure [2, 20].

2.2 Principle of Chemical Detection

The basic principle of chemical detection behind most of the gas sensors depend on a change in the physical or chemical property of the sensing material (analyte) by the absorption /desorption or chemical reaction with the gas to be sensed. This variation in the physical and chemical property of the sensing material can be recorded by the readout circuit by monitoring variations in the electrical or other properties of the material such as conductance, resistance, work function, resonance frequency, optical characteristics or energy released by the gas/solid interaction. The variation in the property of the sensing material is proportional to the concentration of the gas species to be detected in the surrounding environment. The device can be calibrated to give a continuous readout. Using the basic principle, a chemical detection system can be designed using CNT

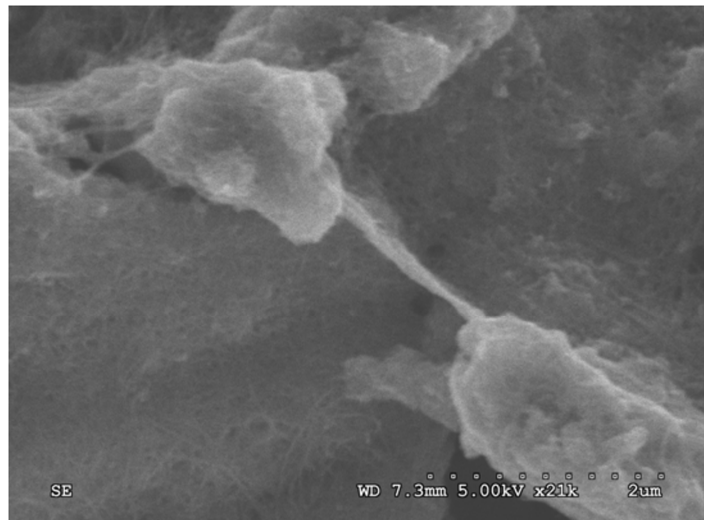


Figure 2.1. SWCNTs accumulate as a bridge.

cantilevers [4, 5, 20]. Carbon nanotubes are capable of interacting with gaseous species either directly or indirectly by using a polymer analyte coating on their surface.

When they come in contact with the gas species to be detected, they absorb the gas species. This causes the mass of the cantilever beam to change which in turn bends the beam or changes the resonant frequency as shown in Figure 2.2 [7, 21]. This magnitude of bending or change in resonant frequency is directly proportional to the concentration of the gas species in the surrounding environment. By measuring the magnitude of bending or the change in resonant frequency, the concentration of the gas in the surrounding environment can be determined. Furthermore, by calibrating the device, it can be made to give a continuous value of the concentration of the gas species.

The CMOS readout interface circuit can use either a static or dynamic designed approach. The first approach uses a technique, designed to sense the static bending of the cantilever, due to an increased surface stress caused by the increased mass of the adhering analyte due to the adsorption of the gas species. This is done by measuring the change in the capacitance value and comparing with a specific reference capacitor. The present work uses this approach. The other approach uses cantilevers that are excited at their resonant frequency. The additional mass of the analyte molecules causes a change in the resonant frequency upon bending. This change in the resonant frequency is detected by using a Wheatstone bridge [14].

2.3 Principle of Switched-Capacitor Technique

Switched-capacitor (SC) circuits are composed of an array of periodically operated switches. A simple switched-capacitor with its equivalent resistor circuit is shown in Figure 2.3 [8, 22]. In the Figure 2.3 (a) represents the switched-capacitor

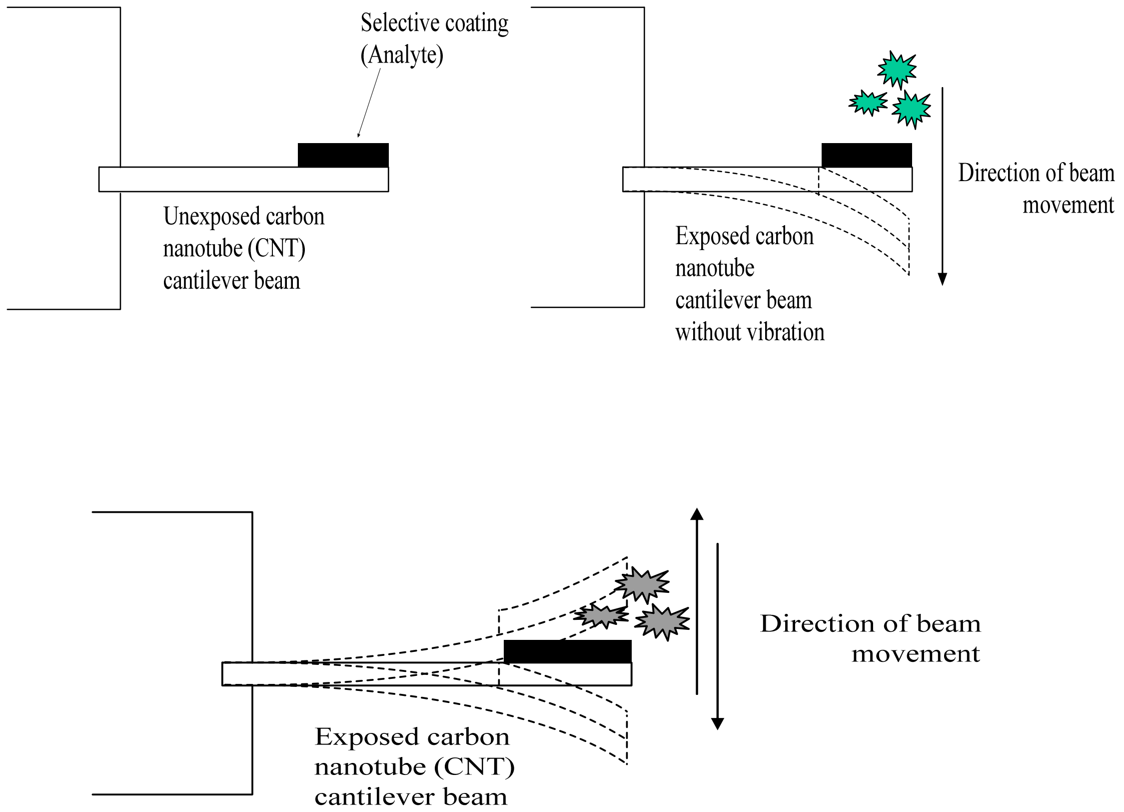


Figure 2.2. Mass sensitive cantilever beam based chemical detection [7, 21].

circuit and the Figure 2.3 (b) represents the equivalent circuit of the switch-capacitor is same as a resistor.

This SC is designed to operate so that when the Single-Pole Double Throw (SPDT) switch S, which is switched to the input, the capacitance will charge to the voltage V, and, when the switch connects with the output, and the capacitor will discharge. If the capacitance is C, V is the input voltage, and the switching period is T_s, then the average current i_{av} is defined as

$$i_{AV} = \frac{CV}{T_S} \tag{2.1}$$

The equivalent resistor r is defined as

$$r = \frac{V}{i_{AV}} = \frac{T_s}{C} \tag{2.2}$$

The implementation of the switched-capacitor circuit, which uses MOS devices, is shown in Figure 2.4. In Figure 2.4 (a), the switch S is represented by two toggle switches S_1 and S_2. These switches are fabricated by two n-type MOS transistors as shown in Figure 2.4 (b). Two of them are driven by two non-overlapping complementary clock signals (ϕ_1, ϕ_2) shown in Figures 2.4 (c) and (d) with frequency of the signals being

$$f_c = 2/T_s \tag{2.3}$$

T_S represents the switching period, which can control the period of these two n-type MOS transistors on and off as switches. The operation of the circuit is as follows. When ϕ_1 is on, ϕ_2 goes off, and the capacitor C will charge input to voltage V. Assuming ϕ_1 is off, and ϕ_2 goes on, the capacitor connects to the output which provides a virtual

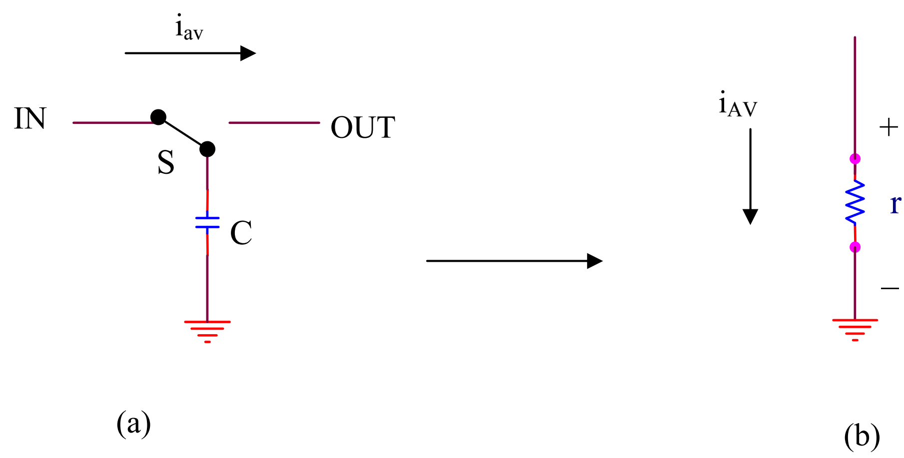


Figure 2.3. Switched-capacitor equivalent resistor [8, 22].

ground to capacitor that will discharge it through the ϕ_2 until capacitance reaches zero. This principle demonstrates the operation of capacitive sensors in a read out circuit.

2.4 Theory of Capacitive (MOS C-V) Sensors [23]

Capacitive sensors are also called variable-capacitance sensors. In the operation of capacitive sensors, we must combine with other circuits to conduct the detection. When we apply a current to charge a capacitor, the changing rate of the voltage is dV/dt and the current is given by

$$I = C\, dV/dt \tag{2.4}$$

$$C = \varepsilon\, A/d \tag{2.5}$$

The formula (2.5) is the basic formula for capacitance, C whose, A is the area of the conductive plate, ϵ is the permittivity of the dielectric material, also called the dielectric constant and d is the distance between two conductive plates. A basic idea for the capacitive sensor is that the distance d between two parallel plates is varied. The example is shown in Figure 2.5. In a two-plate capacitive sensor, the fixed electrode can be a metal plate with dielectric material and another movable electrode also has to be a conductive plate. The moving electrode can change the value of capacitance.

We try to use this property in our gas sensor device. We use carbon nanotubes as the movable electrode and the air as the dielectric material, with the dielectric constant, "1."

If several capacitors are connected in parallel, total capacitance, C_{Total} is given by

$$C_{Total} = C_1 + C_2 + \ldots\ldots + C_N \tag{2.6}$$

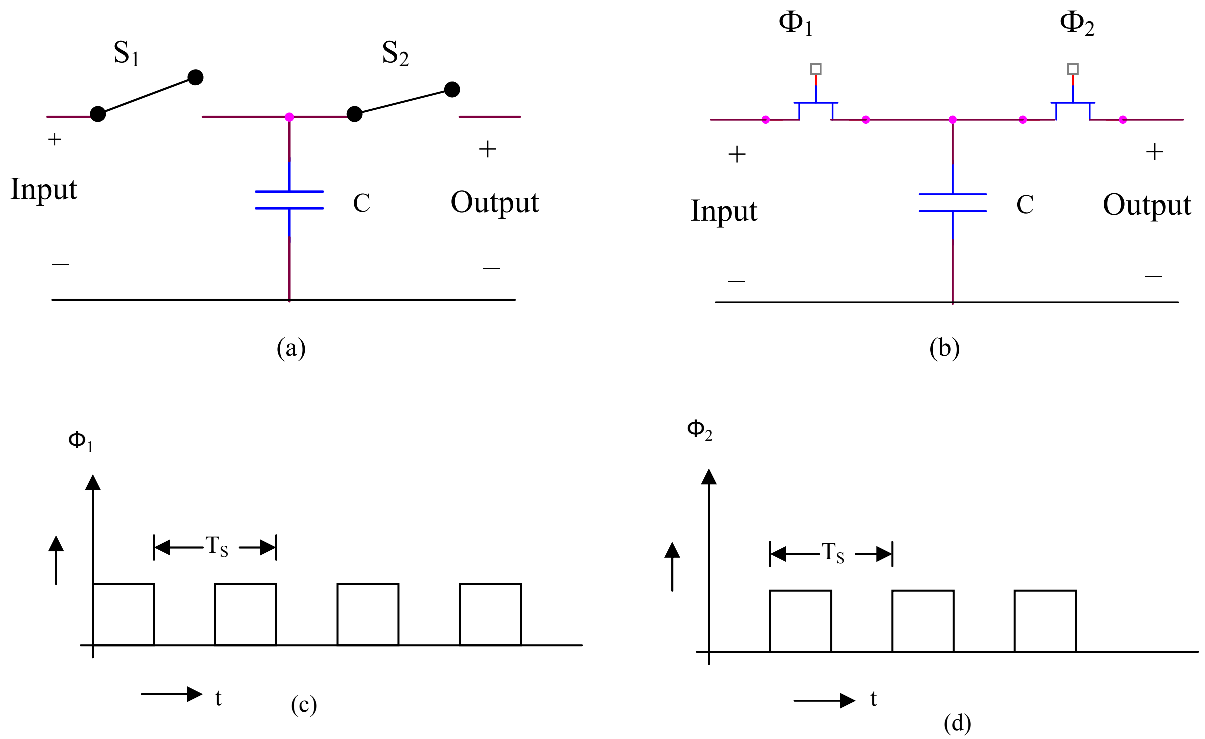


Figure 2.4. A switched-capacitor circuit: (a) toggle switches, (b) MOS switches, (c) and (d) clock signals [8, 22].

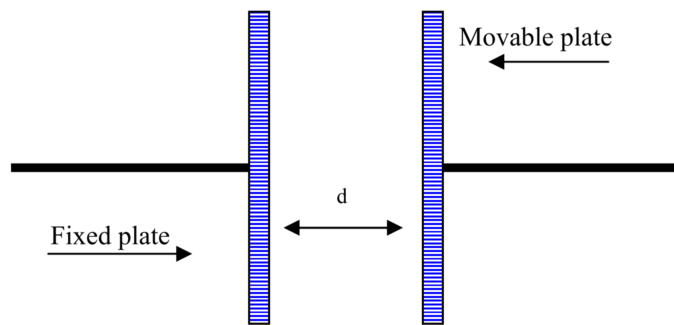


Figure 2.5. Variable capacitor structure [23].

For several series capacitors are connected, capacitor serial, C_{Total} is given by

$$C_{Total} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + ... + \frac{1}{C_N}} \tag{2.7}$$

There are three basic configurations of capacitive sensors, which are shown in Figure 2.6. In our research, we have chosen Figure 2.6 (a) as the capacitive sensor device. The reason we have chosen this configuration is that it is not very difficult to fabricate.

In order to prevent our capacitive sensor from picking up unwanted signals from nearby circuitry, we added a guard electrode to eliminate the noise from other circuitry.

The guard electrode is larger than the moveable plate and is driven by voltage which is same as the sensing electrode. Since the guard electrode connects to the output of the amplifier which provides low impedance that drives the guard electrode to eliminate unnecessary noise. There is no voltage potential between the guard and sensing electrodes [23]. The driven electrode is driven by an ac input voltage or a switching circuit. Figure 2.7 illustrates the basic diagram of our capacitive sensor device [23]. Although the Figure 2.7 looks like that there are two serial capacitors, only the guard and sensing electrodes contact to the amplifier directly.

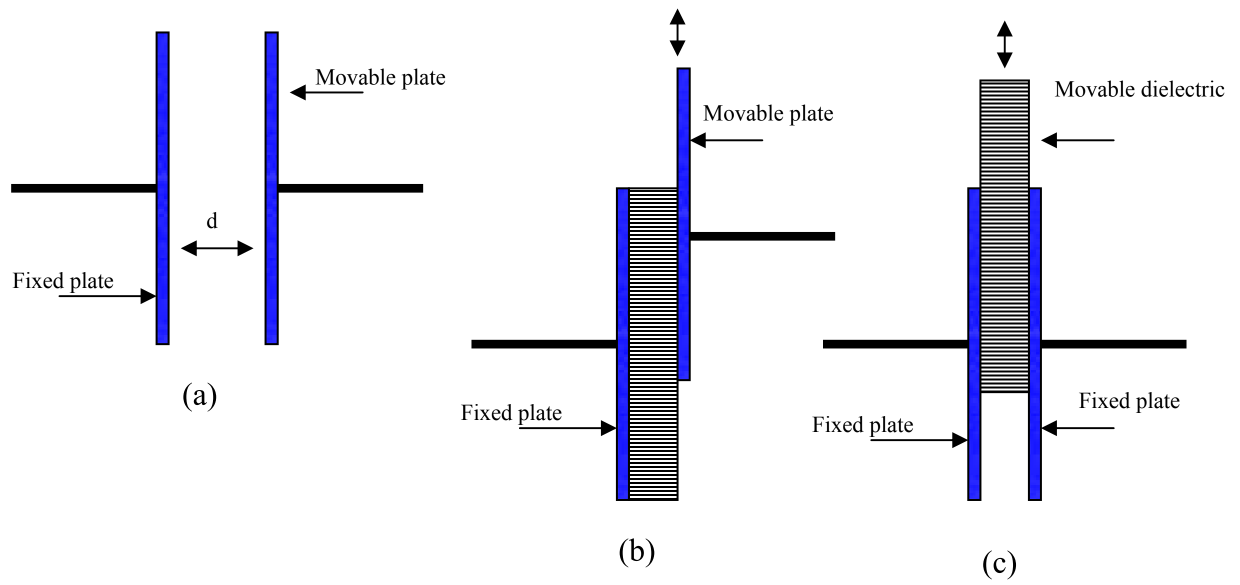


Figure 2.6. Variable capacitance in response to a variation in linear position: (a) variable spacing, (b) variable area and (c) variable dielectric constant [23].

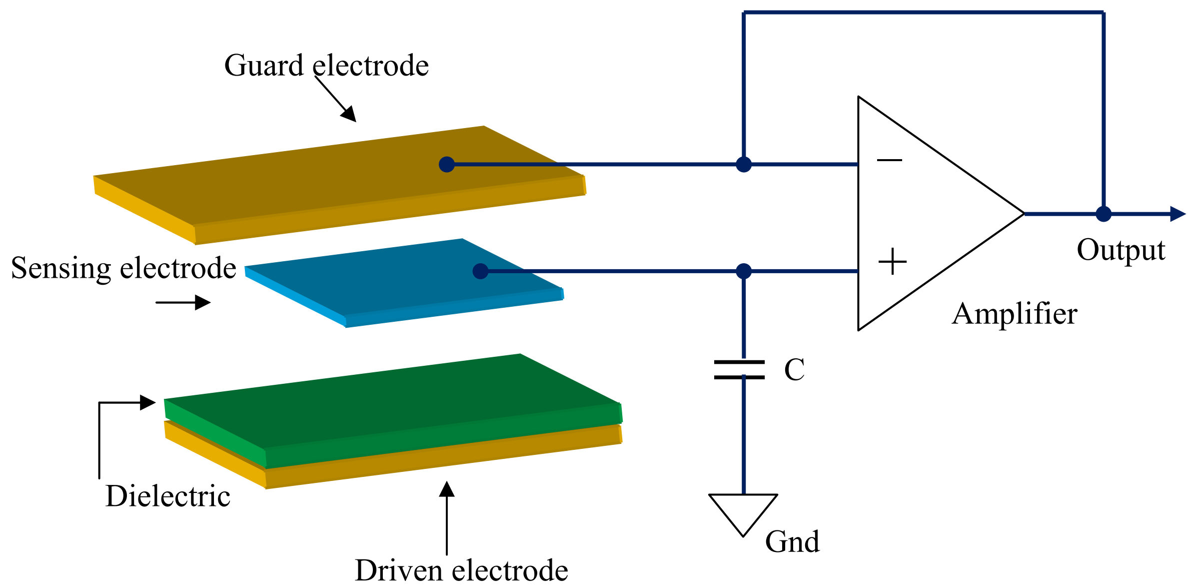


Figure 2.7. Capacitive sensor with guard electrode [23].

CHAPTER 3
CARBON NANOTUBE CANTILEVER DESIGN AND SIMULATION

The design, simulation and implementation of the capacitive sensor interface circuit will be discussed in this chapter. The design and simulation of the operational amplifier, which is also a main component, will be discussed in this chapter as well.

3.1 Interface Capacitive Sensor Device

The interface capacitive sensor device, which has been explained in Chapter 2, is a key component to connect with the gases and the environment. The design is based on the changing of capacitance when the carbon nanotube absorbs gas molecules. The basic design has been shown in Figure 2.7.

3.2 Design and Simulation

In the interface capacitive sensor device, we use carbon nanotubes as the sensing electrode, which can move after the nanotubes absorb the gas molecules. The distance "d" between the sensing electrode and driven electrode will be changed by moving the sensing electrode. In order to make sure the nanotube cantilever beam (sensing electrode) can move by absorbing the gas molecule, we have used ANSYS V10.0 to simulate the bending of the nanotube. The simulation parameters [24] and results are shown in Table 3.1 and Figures 3.1-3.6. We notice that the simulation results for carbon nanotubes are often similar to metal materials. Because there are two different types of carbon nanotubes, which have two different properties (one has metal properties and another has semiconductor properties) [26, 27]. In our research, we use the metal CNTs [25]. The simulation results have helped us to understand the moving property of carbon nanotubes. After finishing these simulations, we have developed confidence to implement our capacitive sensor.

Table 3.1. ANSYS simulation parameters and simulation results.

Parameter	**Original Data**	**1 gas particle**	**10 gas particles**	**100 gas particles**
Young's Modulus	1054Gpa [24]	1054Gpa	1054Gpa	1054Gpa
Poisson's Ratio	0.16	0.16	0.16	0.16
Density	2.6g/cm^3	2.6g/cm^3	2.6g/cm^3	2.6g/cm^3
Length	1um	1um	1um	1um
Diameter	5.2 nm	5.2 nm	5.2 nm	5.2 nm
Inner Diameter	0.2 nm	0.2 nm	0.2 nm	0.2 nm
Bulk-to-surface ratio	>400 m^2/g [25]	>400 m^2/g	>400 m^2/g	>400 m^2/g
Mass of CNT	2.041×10^{-8}g	2.041×10^{-8}g	2.041×10^{-8}g	2.041×10^{-8}g
Effective surface area	8.16×10^{-2} cm^2	8.16×10^{-2} cm^2	8.16×10^{-2} cm^2	8.16×10^{-2} cm^2
Simulation Result Displacement (μm)	NA	0.176×10^{-18} (0.176×10^{-14}Å)	0.176×10^{-17} (0.176×10^{-13}Å)	0.176×10^{-16} (0.176×10^{-12}Å)
Stress (N/m^2)	NA	0.137×10^{-9}	0.137×10^{-8}	0.137×10^{-7}

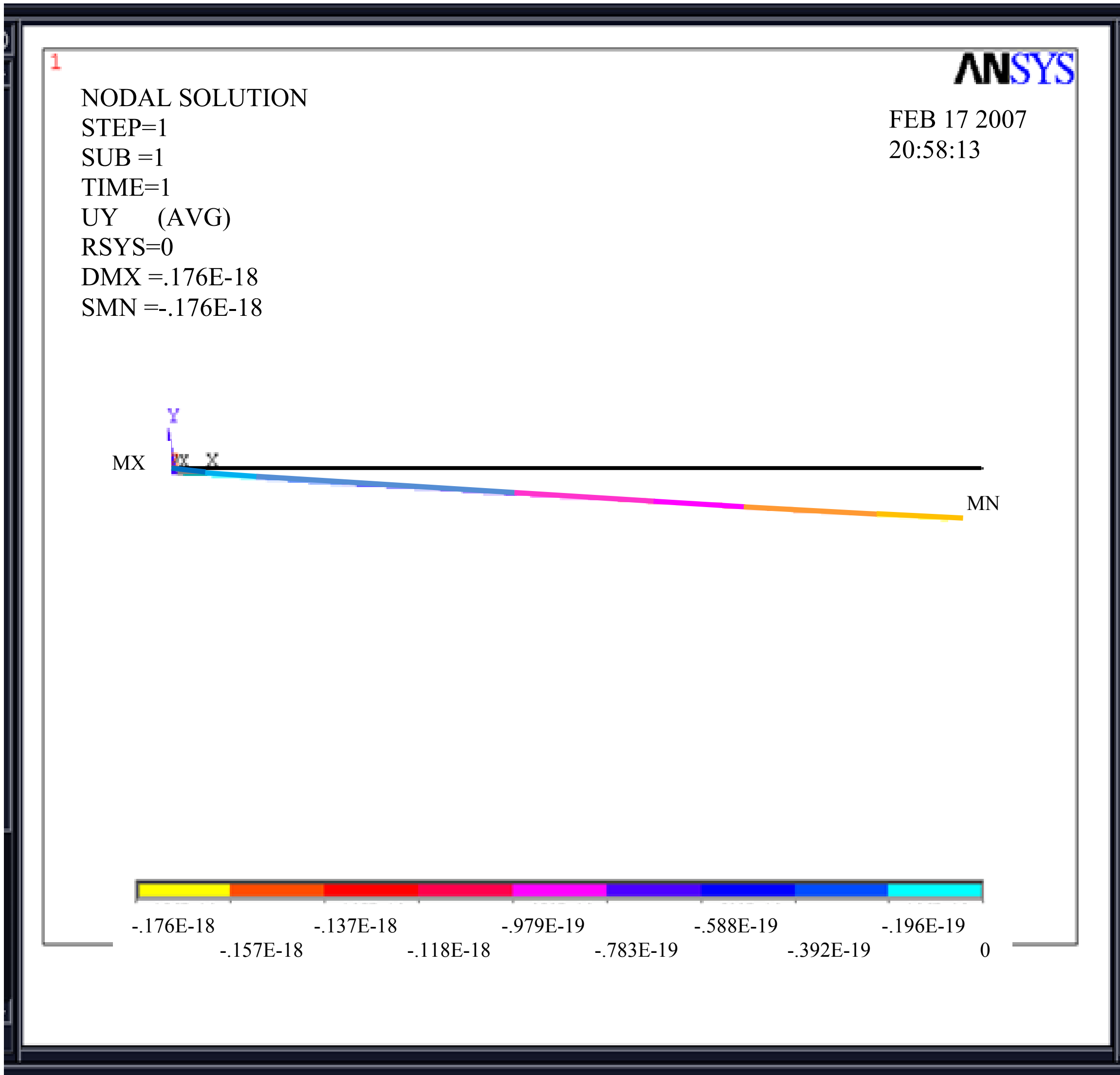


Figure 3.1. One oxygen gas particle displacement simulation result.

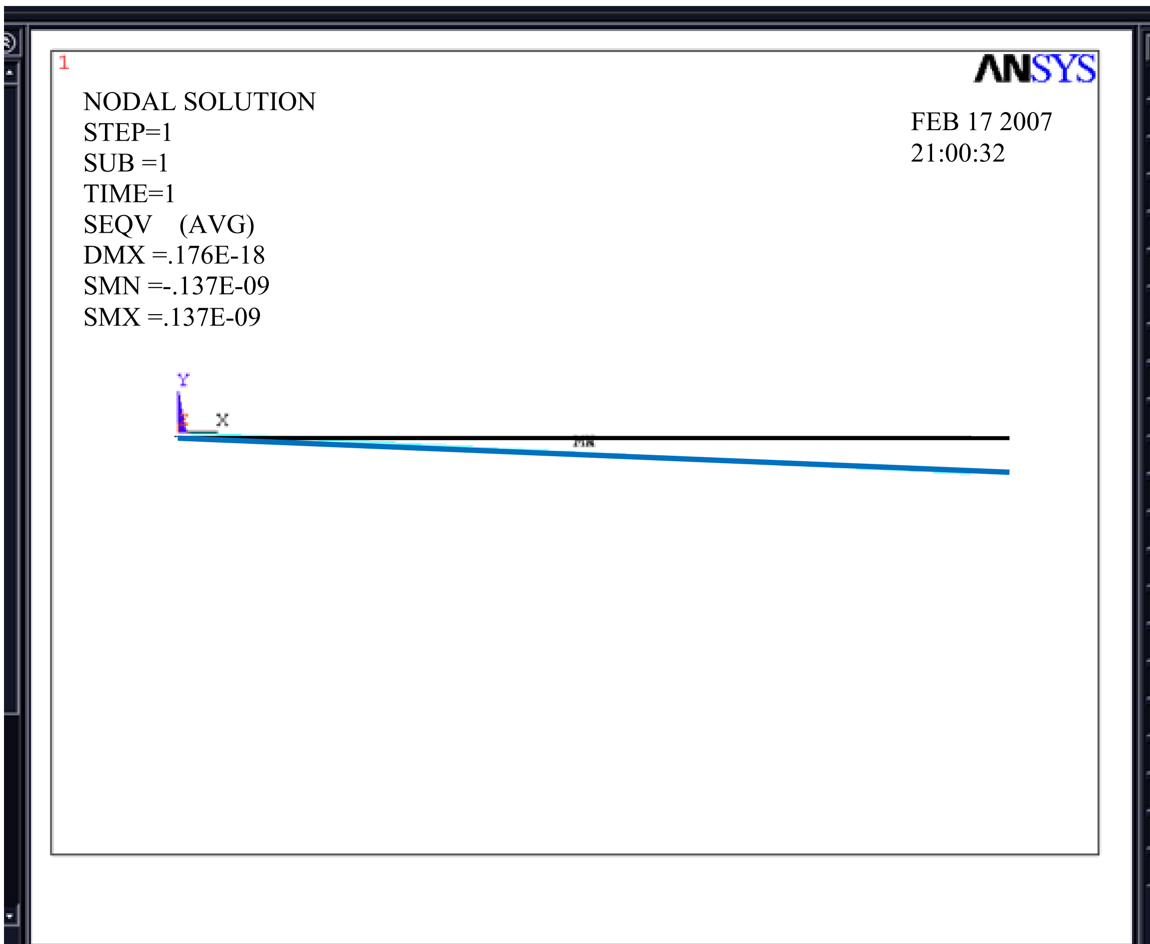


Figure 3.2. One oxygen gas particle stress simulation result.

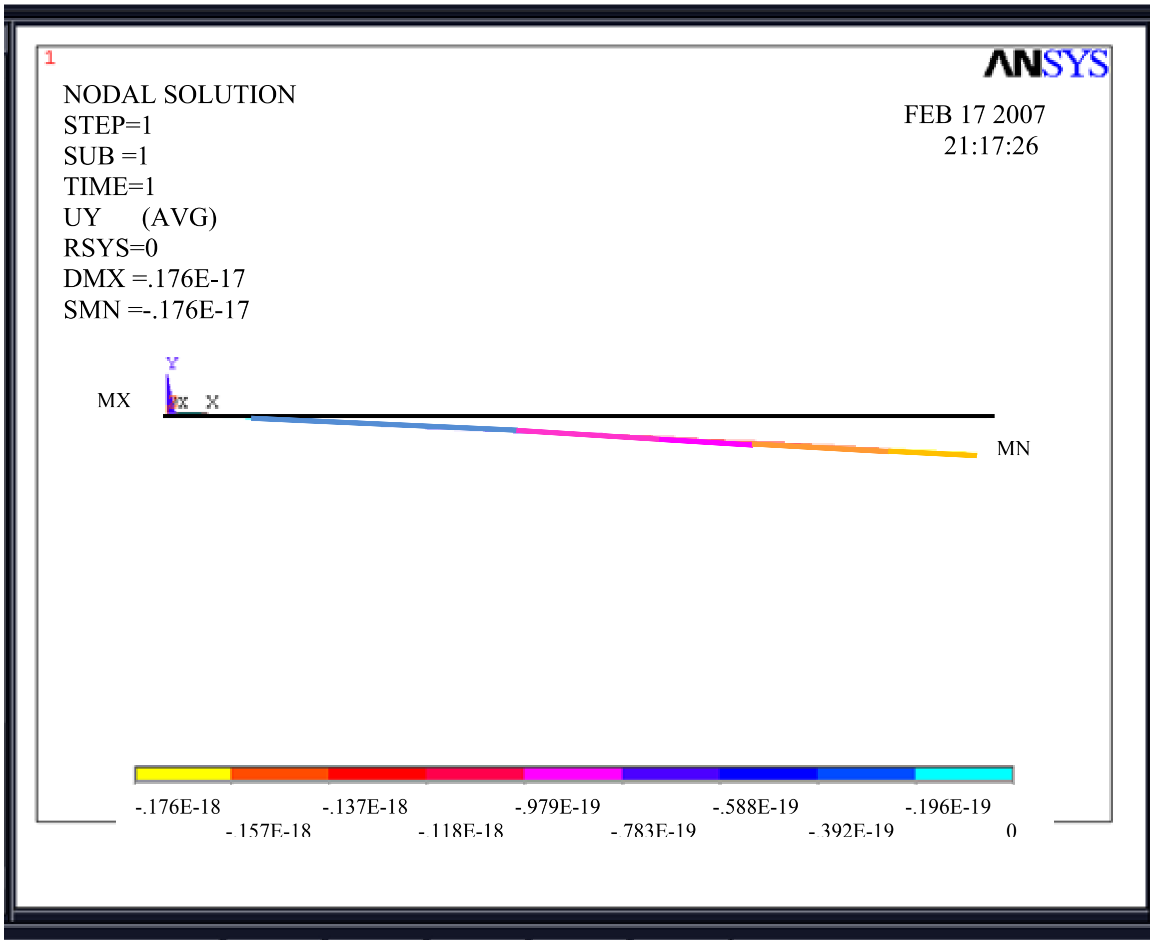


Figure 3.3. Ten oxygen gas particles displacement simulation result.

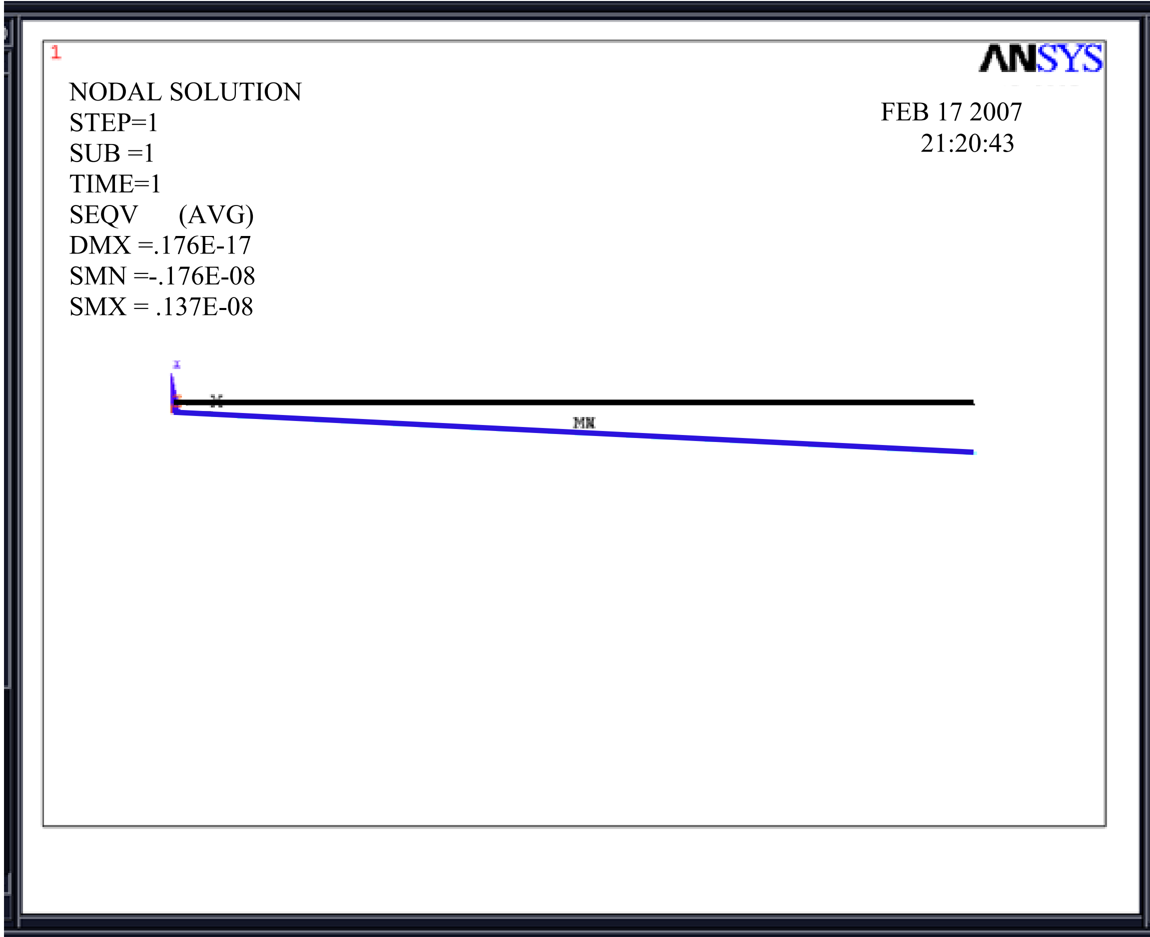


Figure 3.4. Ten oxygen gas particles stress simulation result.

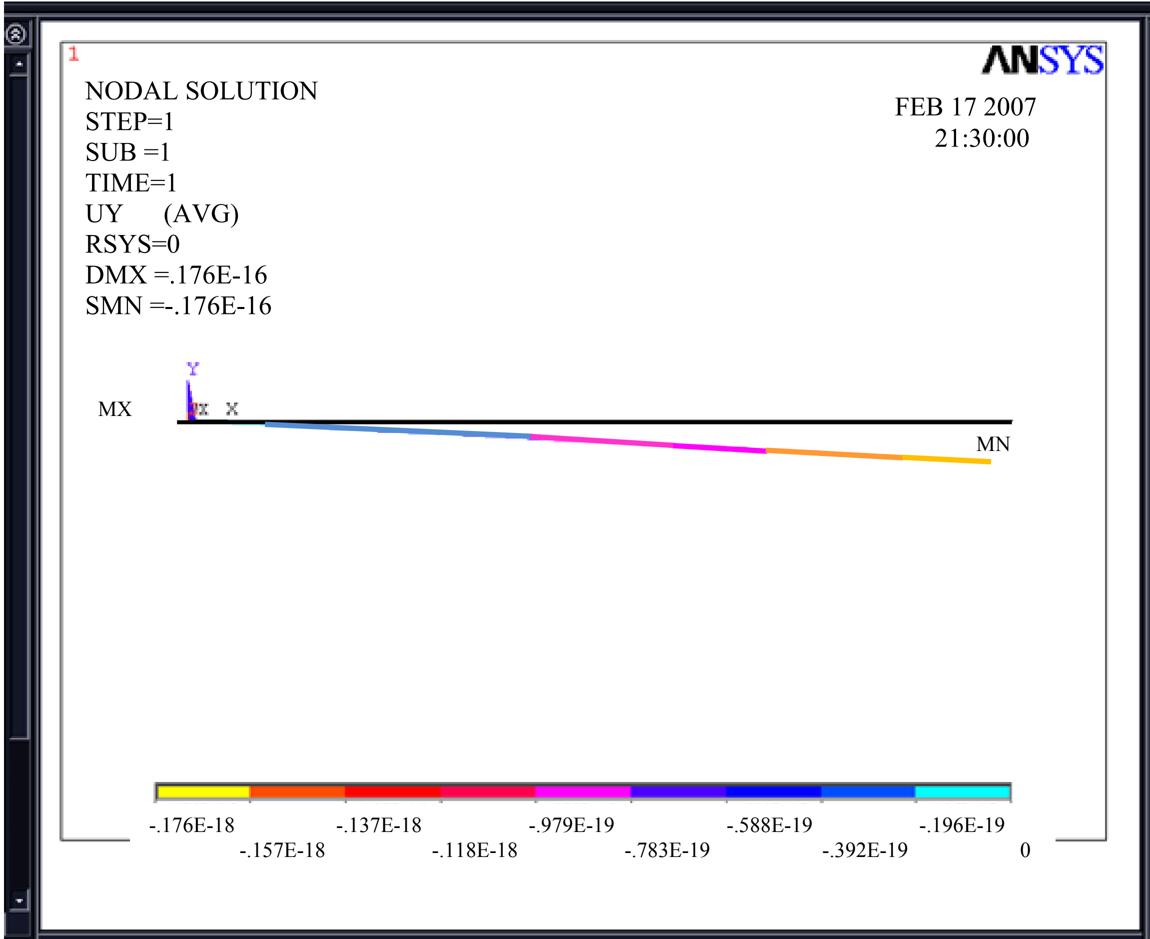


Figure 3.5. One hundred oxygen gas particles displacement simulation result.

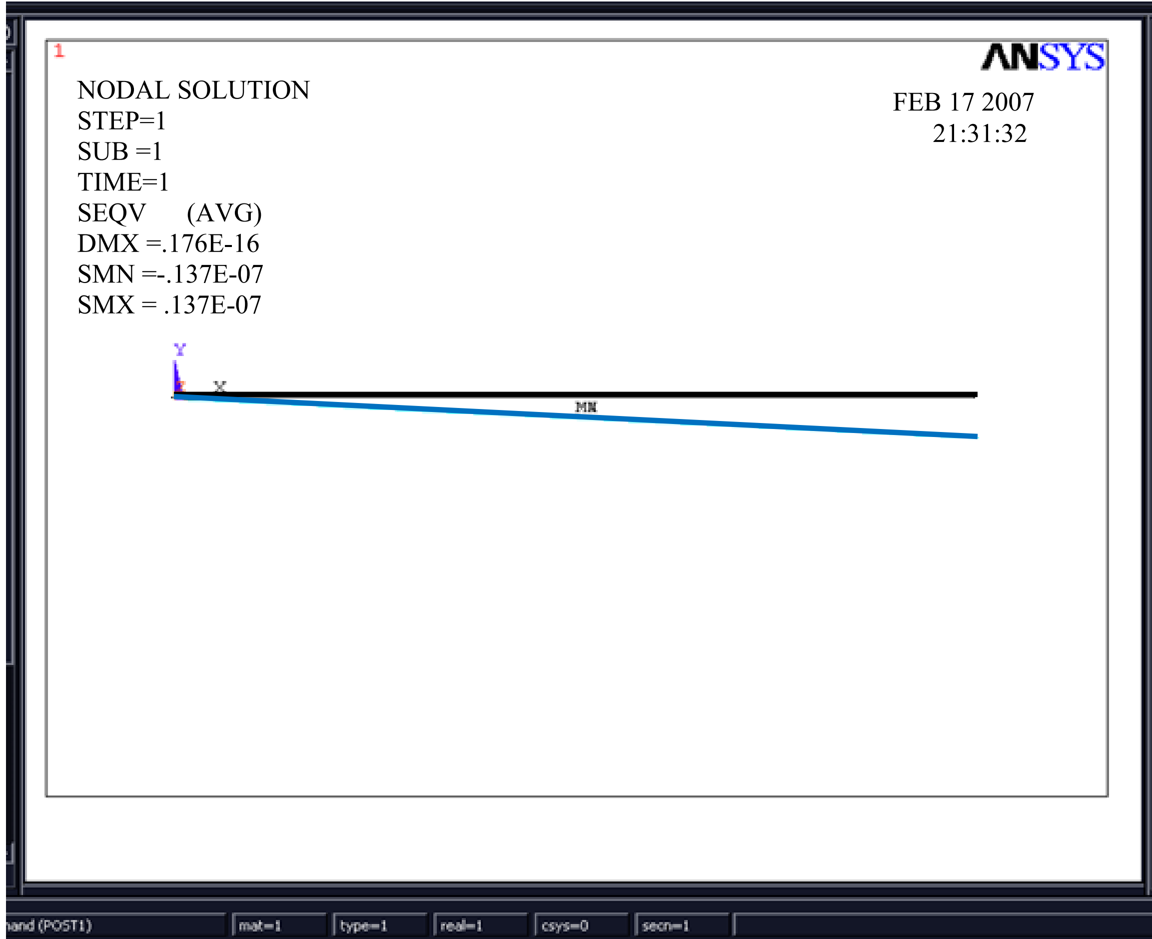


Figure 3.6. One hundred oxygen gas particles stress simulation result.

CHAPTER 4
FABRICATION

4.1 Principle of the Fabrication of the Cantilever Beam

In our research, we have used carbon nanotube cantilevers for the gas detection mechanism, which is based on the capacitive sensing principle that the cantilevers will react with gas molecules. The fabrication of the carbon nanotube cantilever is the most critical step in this research. CVD techniques have been used for CNT [28] growth. In our research, we have chosen another approach to fabricate CNT cantilevers over a silicon gap photolithographically defined [28, 29].

In order to fabricate cantilevers, we need to create a gap as small as possible, but the photolithography has it own machinery limitation, and the one we have created dose not have the technology to create a small gap mask. The lift-off process [28] is our approach to create the small gap. The gaps we have created as small as possible are around 100nm-1μm in size and can easily assemble the CNTs crossing the gaps. Precisely assembling the CNTs across the gap is the most critical step. In our work, we have achieved SWNT over the silicon gap by applying the AC field [30]. The method is explained as follows.

4.2 Principle of the AC Manipulation in CNTs

An ac voltage can attract and orient CNTs between electrodes [30]. Dielectrophoretic force and electrophoretic forces [30, 31] will be used here to help the nanotubes assemble; dielectrophoretic force can be created in an inhomogeneous electric field, where the frequency is between 10 kHz to 10MHz [28, 30]. Since ac field can manipulate the CNTs, we have the confidence to setup the experiment and apply an external ac field to fabricate CNT cantilever [30].

The CNT powder is obtained from Nanostructured & Amorphous Material, Inc., Houston, TX, which provides many carbon nanotube related products. In our experiment, CNTs were dissolved in a dichloro-benzene solution for more than twenty-four hours with the ultrasonic to untangle the CNTs powder solution.

4.3 Fabrication of Micrometer Size Gap Over the Silicon Substrate

A brief overview of the fabrication of gap will be provided below. Our concept is that a small gap has to be created by the lift-off process and we must apply the ac field to manipulate CNTs. A dielectric film Si_3N_4 has been chosen because it can provide better oxidation prevention [28]. The various steps in the formation of small gaps are shown and discussed in Figure 4.1-4.10.

Single-crystal silicon with (100) orientation and 15 Ω-cm resistivity were used in our μm-gap fabrication. In order to prevent any contamination in the surface of the silicon wafers, the RCA cleaning method [32] was used to remove particles and organic contaminants on the surface of the silicon wafers. This process can remove particles and help us grow a uniform film on the surface of wafers. A brief explanation of the RCA cleaning method will be introduced in this paragraph. The RCA cleaning method is an industry standard that can remove the organic residue and films from silicon wafers. In the cleaning process, the chemicals oxidize the silicon and remove a thin oxide from the surface of the wafer.

The chemicals we need for this RCA are water, ammonium hydroxide (NH_4OH) and hydrogen peroxide (H_2O_2). The mixing ratio for these three materials is 5 (H_2O):1 (NH_4OH):1 (H_2O_2).

The RCA cleaning method has three steps as describes below:

1. Organic Clean: Removal of insoluble organic contaminants with a 5:1:1 H_2O : H_2O_2 : NH_4OH solution for 10 minutes.
2. Oxide Strip: Removal of a thin silicon dioxide layer where metallic contaminants may have accumulated as a result of 1, using a diluted 50:1 H_2O: HF solution for 15 seconds.
3. Ionic Clean: Removal of ionic and heavy metal atomic contaminants using a solution of 6:1:1 H_2O : H_2O_2 : HCl for 10 minutes.

The procedure has to be conducted under the chemical hood for respiration safety. The process is first to pour 500 ml DI water in a pyrex beaker, add 100 ml NH_4OH then put the beaker on the hot plate and heat to 70° C. Remove the beaker from hot plate and add 100 ml H_2O_2.

In Figure 4.1, the solution will generate some bubbles. Wait for 2 minutes and put the bare wafer in the solution for 15-20 minutes. After 20 minutes, take the wafer from the beaker and rinse it by flowing DI water for 10 minutes. A nitrogen gas can blow the DI water out. Put the wafer on the hot plate to bake for 30 minutes at 80° C to dehydrate.

After the cleaning process, in Figure 4.2, a silicon nitride (Si_3N_4) film of approximately 4,000 Å is deposited by RF-sputtering for 2 hours over the clean silicon wafer surface. The deposition rate of Si_3N_4 is much slower than other metal films if we compare Si_3N_4 film 1000 Å for 30 minutes and Al film 1200 Å for 10 minutes. Silicon nitride film is used in this process over silicon-dioxide because of its excellent quality [28, 33]. Also, when silicon dioxide is used, the nanotubes have an affinity to easily burn out in an oxygen rich environment at elevated temperatures [28].

The following step is the deposition of aluminum (Al) film of thickness 1200 Å by RF-sputtering in Figure 4.3. Aluminum is the most popular metal layer in IC fabrication and can be easily dry etched metal. The Al film we use as a sacrificial layer in the lift-off process, will give us a high possibility to create a small gap. The size of the narrow gap is dominated by the width of the Al film bridge that comes after a photolithography process for the Al gap definition and before the Cr film deposition.

Followed by the pattern using a positive photoresist, the Shipley S1813 photoresist in Figure 4.4 is employed to help define the undercut of Al film for the μm gap. The desired thickness of this layer is 1 - 2 μm so that the spin coating recipe will ramp from 0-100 rpm and hold in 100 rpm for 5 seconds, ramp to 500 rpm and hold in 500 rpm for 5 seconds, and final ramp to 1500 rpm hold for 35 seconds. Soft baking for S1813 photoresist after spin-coating is around 100 °C for 45 minutes.

The spin-coated wafer is exposed through a mask under UV for 10 sec, which can define the gap size on the Al film. A subsequent immersion in a developer solution is carried out for 2 minutes to get the pattern of the gap shown in Figure 4.5.

A DI water rinse can remove the developer residue and following 90°C baking for 30 minutes can dry the hydrate. An Al etchant solution will remove unnecessary Al film within 1 to 2 minutes and kept the photoresist film. After the Al etching process, a DI water rinse will clean the residue of Al etchant shown in Figure 4.6.

In Figure 4.7, acetone can be used as a photoresist remover to get rid of S1813 photoresist. We immerse the wafer in acetone solution until we remove the photoresist completely and a following DI water rinse can help clean the wafer.

Figure 4.8 shows the cross-section of the Chromium (Cr) film of 500 Å deposited by RF-2 sputtering process. Cr film can anodize with Al film literally [34, 35].

Figure 4.9 shows the cross-section after Al lift-off using NaOH (Sodium hydroxide) solution as the Al etchant. The NaOH solution is made by 8g of NaOH mixed with 100ml water. A processed wafer is immersed in the solution until the unnecessary Al film has been removed. Silicon nitride is then removed by RIE with Ar gas and Si is etched by KOH etchant. The lift-off process of using Al film as a sacrificial layer has allowed us to achieve a narrow gap. The smallest gap size which can be obtained by the above method is ≈150 nm.

Figure 4.10 shows the cross-section of the etched silicon gap. Silicon etch is a complex process. There are several silicon etching methods. We have chosen the KOH etching process to etch the silicon because the KOH etch is safer and easier than other methods. The concept of the KOH etch is based on the hydroxide etching of silicon.

First, the etchant will oxidize the silicon by forming silicate, and a process of reduction of water will follow. The silicate layer will react with hydroxyls to form a water-soluble complex. A typical KOH etching recipe is shown below:

– 230 g KOH

– 140 ml isopropyl alcohol (C_3H_8O)

– 630 ml H_2O

–Keep the temperature of water at 80°C -82°C to agitate the process.

The etch rate of silicon is around 1 mm/min for (100) Si.

KOH can be mixed in a quartz or pyrex beaker.

Select a small quartz or pyrex beaker in which we will place the KOH solution; place a watch glass on top of the solution beaker to collect condensation and prevent spillage of the KOH solution onto the hot plate surface.

Pour the desired volume of KOH into the smaller beaker; concentrations of KOH are selected by the requirements. Dilute the KOH crystals using water and mix the desired concentration; normal concentrations used in the lab are 30%. This concentration will etch at approximately 60 Å.

KOH Etching of Silicon - 2

– Hot plate & stirrer.

– Keep covered or use reflux condenser to keep propanol from evaporating.

– Presence of alkali metal (potassium, K) makes this completely incompatible with CMOS processing.

The nanocantilevers or the CNT cantilever can be grown either by the CVD process or by aligning the CNTs in the gap formed by the application of the electric fields as shown in Figure 4.11. Some of the published works have shown that CVD and chemical patterning methods [36] can grow and align the CNTs successfully. However, these methods cannot be achieved under room temperature with basic equipment. In our approach, an electric field method has been chosen to assemble CNTs across a gap and found the most suitable.

In Figure 4.11, the schematic diagram shows ac biased method for the CNTs cantilever assembly. In this process, we use the electric field [30] to align and assemble the CNTs across a small gap within the room temperature; moreover, the probabilities of successfully assembling the CNTs across a gap are higher than CVD.

Figure 4.1. Silicon wafer.

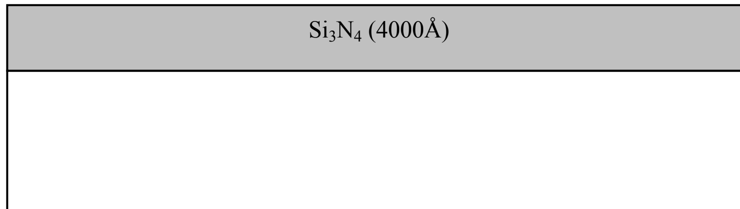


Figure 4.2. Cross-section showing Si-Si_3N_4 structure.

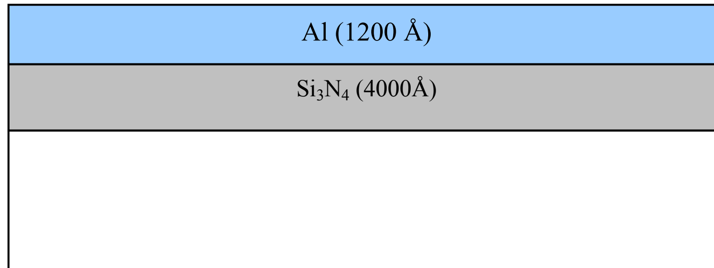


Figure 4.3. Al film (1200Å) deposition by sputter.

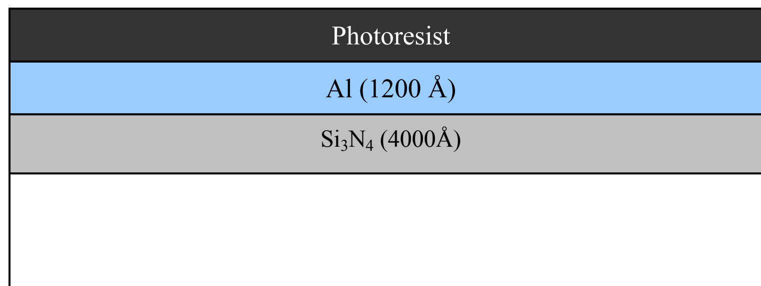


Figure 4.4. Al patterning using a positive photoresist.

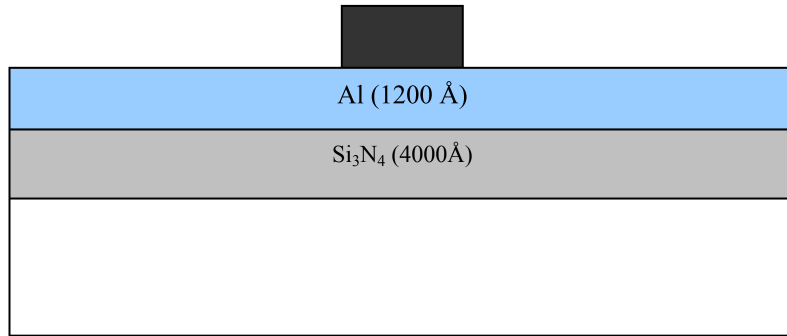


Figure 4.5. Pattern development and photoresist removal.

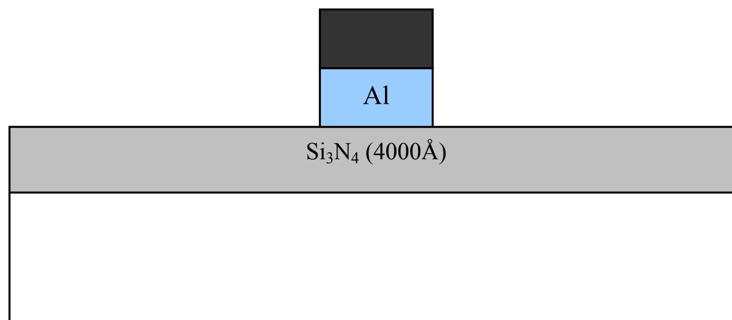


Figure 4.6. Al film removal.

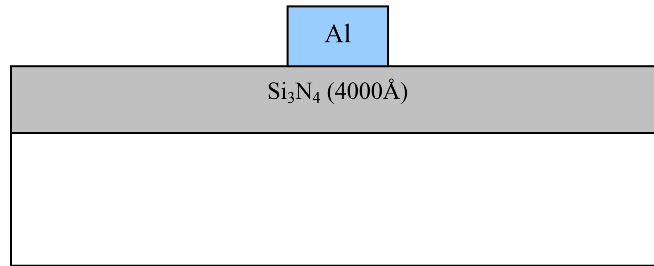


Figure 4.7. Photoresist removal.

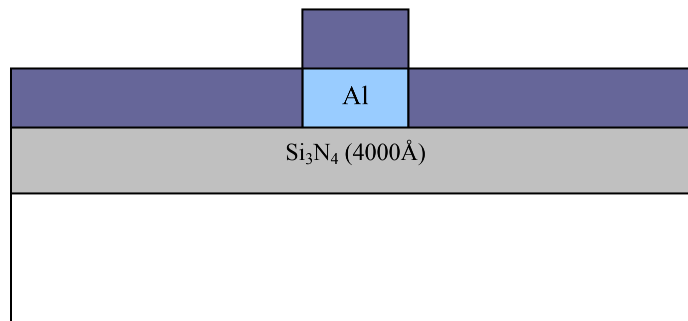


Figure 4.8. Cr film deposition.

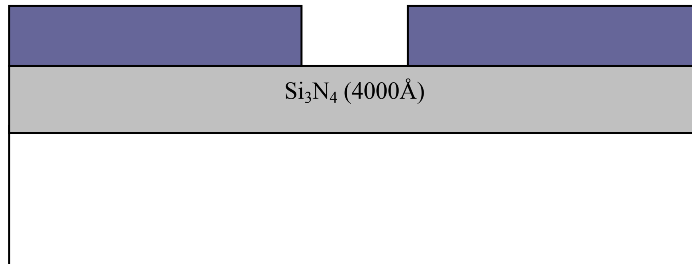


Figure 4.9. Al film lift-off.

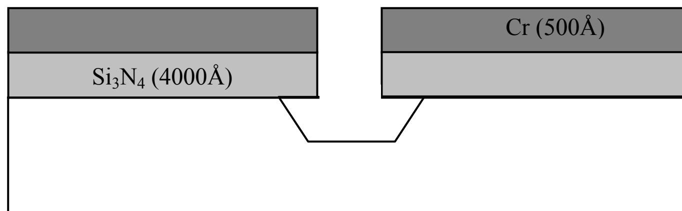


Figure 4.10. Cross-section showing gap formation by anisotropic RIE and KOH etching.

The AC field can attract and align the CNTs across the gap as well as fully provide the dielectrophoretic force when the frequency range is between 10 kHz to 10 MHz [28, 30]. That will give the momentum and orient the CNTs to achieve the alignment. Since we applied the ac field by a power generator with 5 MHz and 10 Vp-p for 15 minutes [37] to align and dry the solution, the CNTs can be aligned on the surface of the Cr electrode. This experiment is highly reproducible. In this experiment, it is obvious that the electric field can polarize carbon nanotubes. The dipole moments of the carbon nanotubes in the parallel are stronger than that in the perpendicular direction. Therefore, the ac field can align the carbon nanotubes along with the field direction. Different peak to peak voltages can have different aligned results. A high ac field can increase the alignment rate and in our experiment, we applied 10 Vp-p. The magnitude of the ac field dominates the alignment speed [37].

A small drop of the CNT solution on the top of the gap can be made by a micropipette. In this setup, we have also used a capacitor (22μF) connected in parallel to a large resistor (1MΩ), which enables the ac voltage passing through the circuit a small current without burning the CNTs [28].

In Figures 4.12 and 4.13, the microscope photos demonstrate the sonication of CNTs in dichloro-benzene for different hours. More hours of sonication can get a better separation result in the CNTs.

Figure 4.14 shows the SEM (Hitachi 3500) photo of the CNT cantilever beam formed over the gap. After the CNT cantilever is aligned over the gap, AFM can be used to cut one side of the CNT to obtain the cantilever beam.

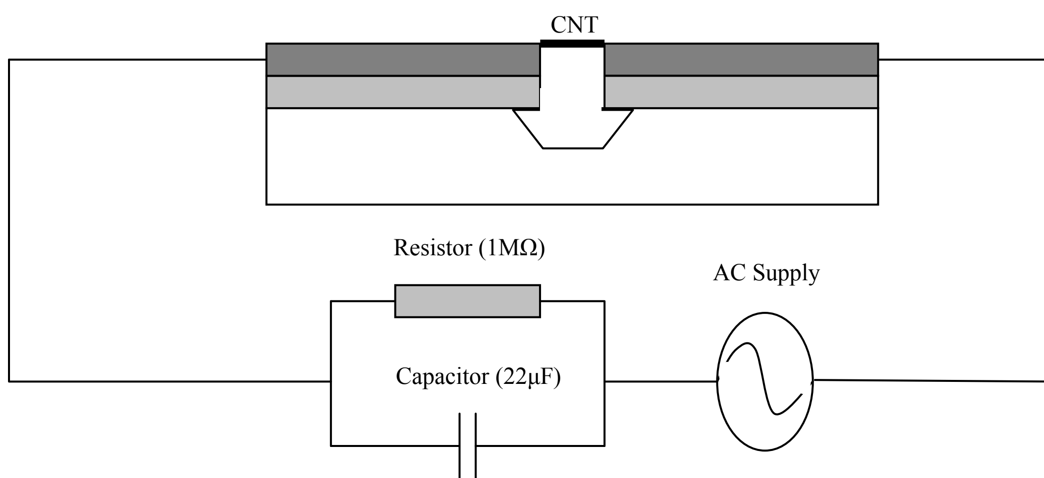


Figure 4.11. CNT cantilever deposition method [28].

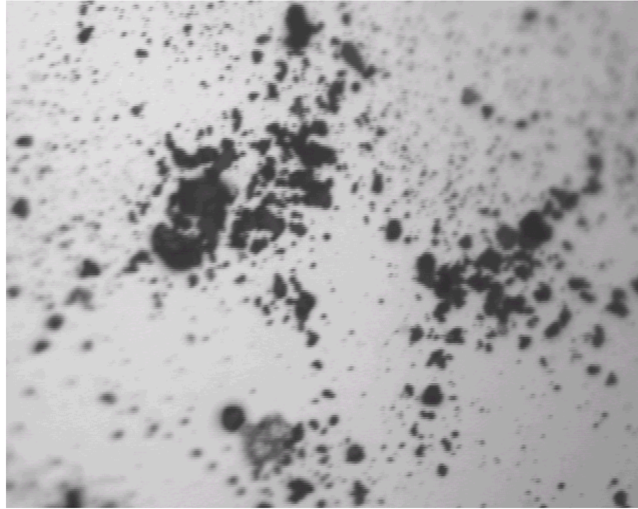


Fig. 4.12. CNT solution under sonication for 12 hours.

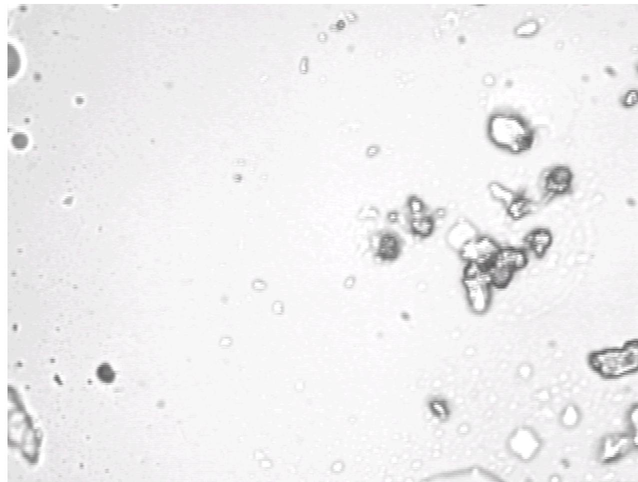


Fig. 4.13. CNT solution under sonication for 24 hours.

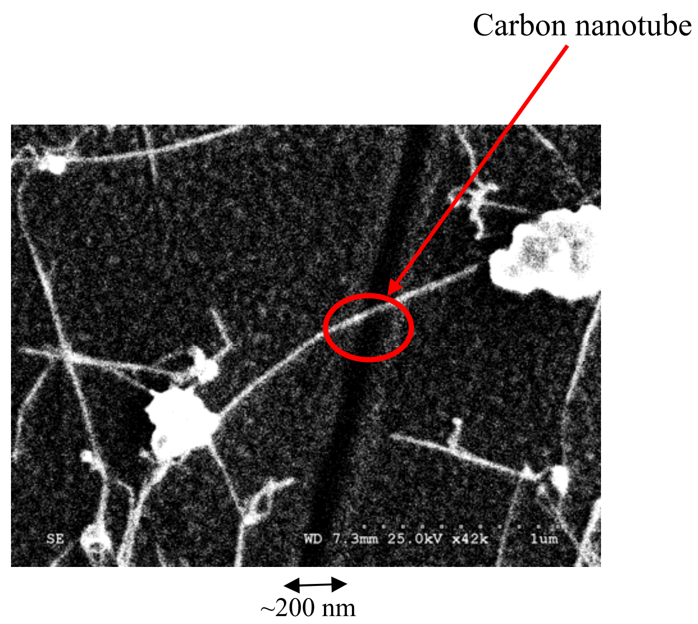


Fig. 4.14. SEM photo taken by Hitachi 3500.

CHAPTER 5
READOUT CIRCUIT DESIGN AND SIMULATION

This chapter provides the capacitive circuit design diagram and simulation results. The operational amplifier is the main component in this device, and the switched-capacitor interface circuit is also discussed in this chapter.

5.1 Overview of Operational Amplifier and Switched-Capacitor Circuit

In our design, a MOS operational amplifier is used for sensing the signal from the CNT cantilever. The most popular MOS amplifier is the two-stage operational amplifier, which provides the advantage of an isolation of the gain and output swing requirement. Figure 5.1 [22] shows the block diagram of the readout circuit using switched capacitor technique. The corresponding circuit diagram is shown in Figure 5.2. The first stage provides a high input impedance to minimize loading of the source. The second stage offers the most desired voltage gain and low output impedance. The loading effect of the next stage must be considered since the input impedance of the stage acts as the load for the current stage. The current source and active resistor are two important components in the two-stage operational amplifier. These two components play important roles in the circuit.

5.2 Simulation Results

Figure 5.3 shows the readout chip layout of the circuit diagram shown in Figure 5.2. The reference capacitor (C_R) is 50 pf. The space is separated on the chip for integrating each cantilever. Figure 5.4 shows the relationship between output voltage V_{OUT} and the simulated sense capacitance C_S. The reference capacitor, C_R is 50 pf.

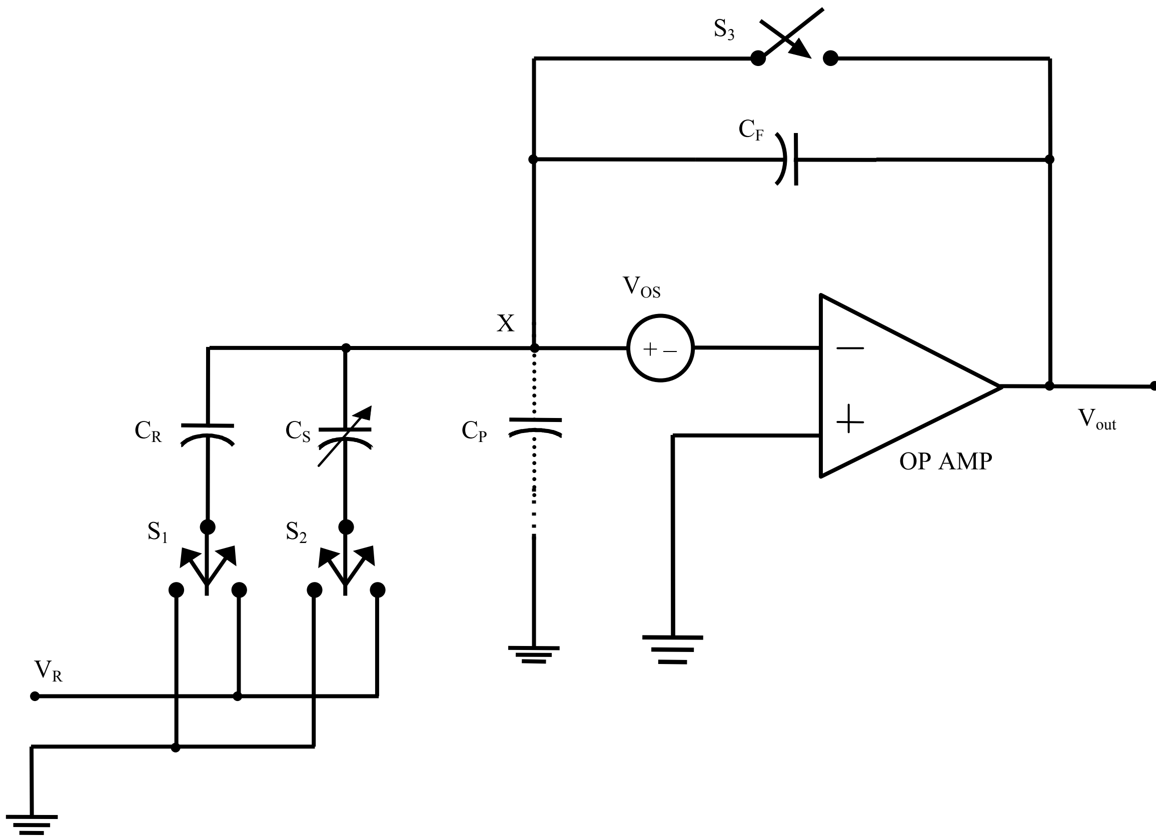


Figure 5.1. Two stage op-amp with switched-capacitor circuit [22].

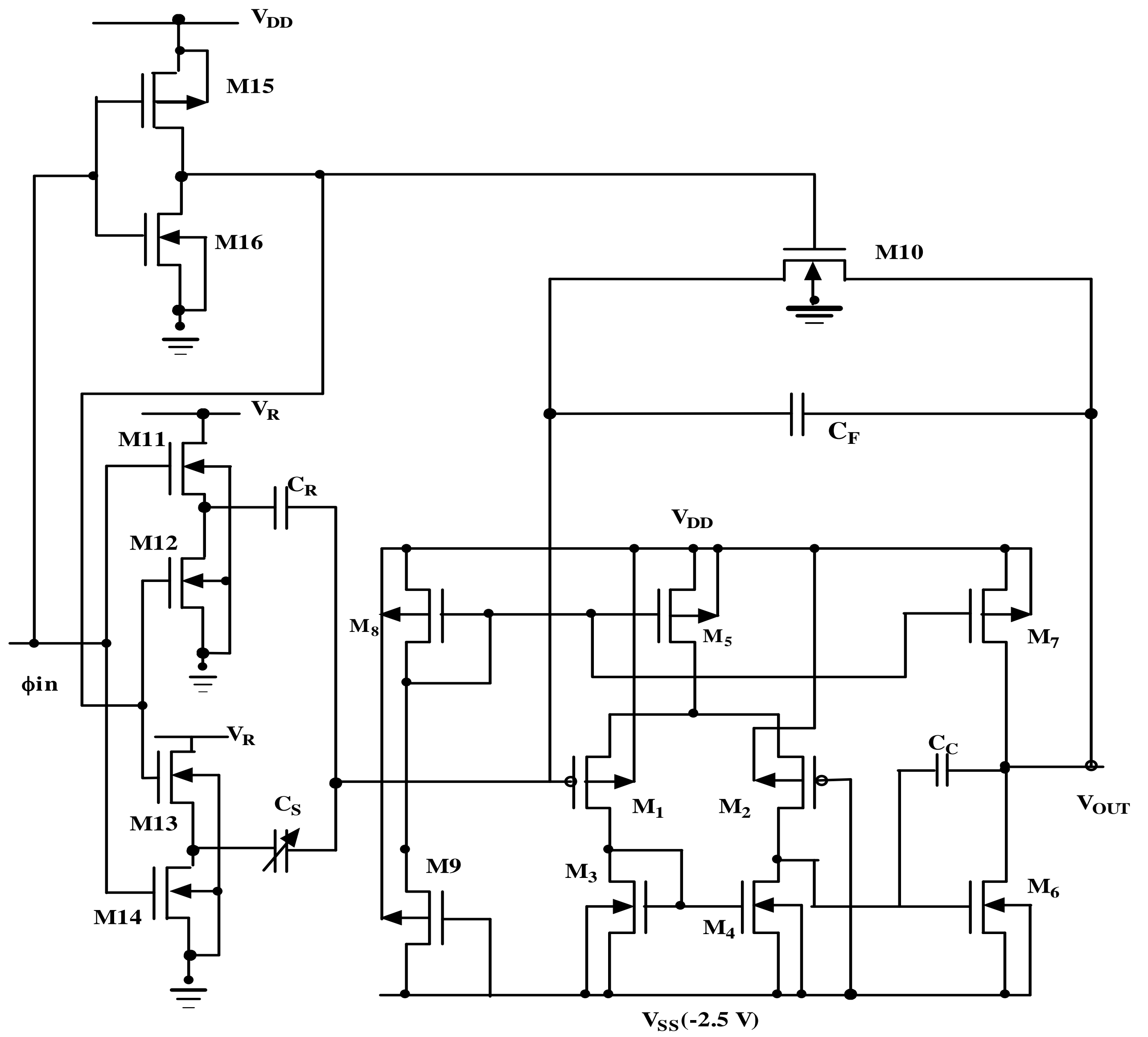


Figure 5.2. Switched-capacitor circuit with two stage OP-AMP [22].

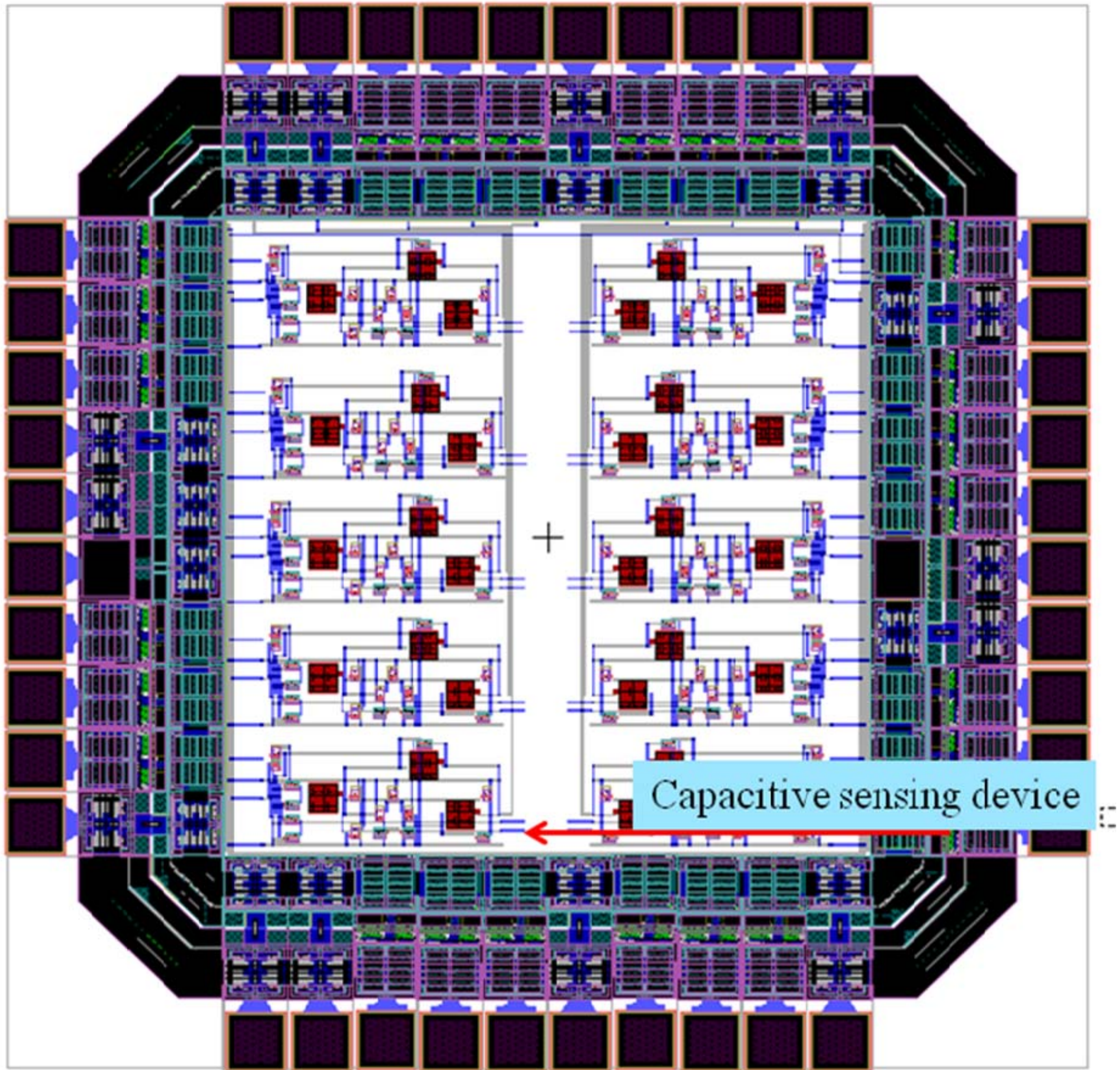


Figure 5.3. Readout chip layout [21].

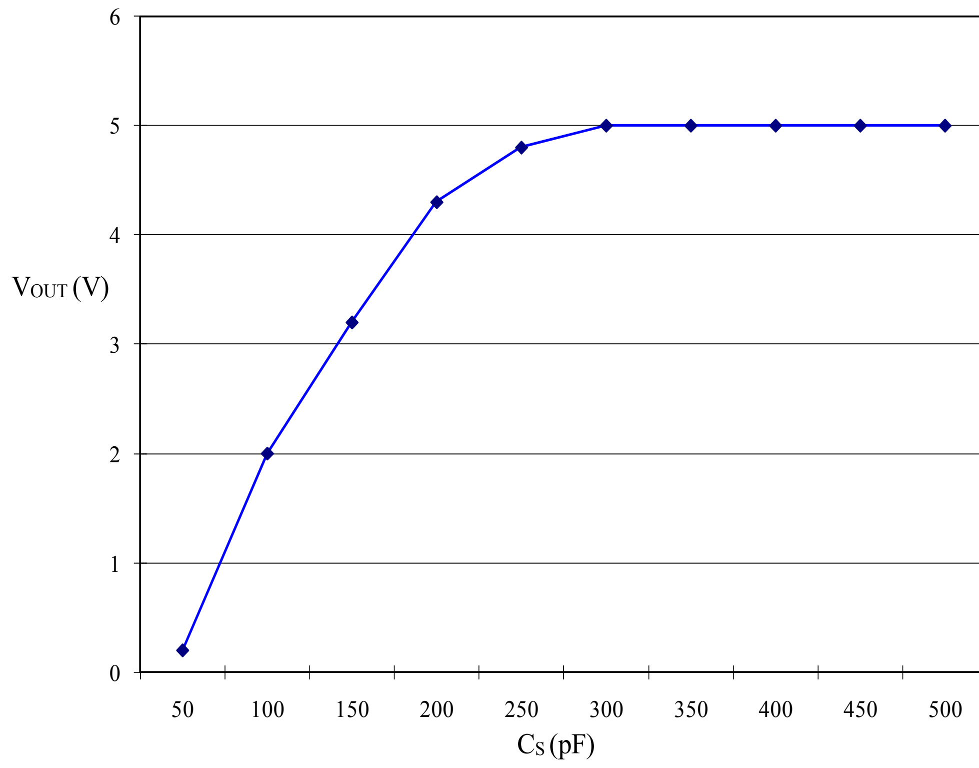


Figure 5.4. The V_{OUT} versus C_S variation.

CHAPTER 6
INTEGRATION AND PACKAGING ISSUES

6.1 Integration

In our work, to integrate carbon nanotubes with our circuits is a tremendous challenge because the size of carbon nanotubes is extremely small. Thus integration requires the lead equipment which we don't have. Researchers at Rensselaer Polytechnic Institute have developed a new method [38] to bond materials that do not normally stick together. This new method is explained in [39].

The new nanoglue method provides a connective molecular nanolayer that can bond any two different surfaces together. This new nanoglue can stick these different materials together very well. In Figure 6.1 [39], normally, around 400°C, a nanolayer (yellow plate: copper film, blue plate: silicon wafer) would degrade or detach from a surface. But when a thin copper film on the top of the silica binds strongly with the nanolayer, heat causes the nanolayer to create strong chemical bonds to the silica underlayer, thus gluing the copper-silica together. This technique produces the thin film sandwich's adhesion strength and allows the nanolayer to sustain temperatures of at least 700°C. Nanoelectronic technology and semiconductor manufacturing may get benefit from this new discovery that bonds nearly any two surfaces together. Other new applications include adhesives for high-heat environments and even some medical research and biotechnology.

We can use this method to attach carbon nanotubes with CMOS circuits without causing unwanted damages in the circuit. In Figure 6.2, we show the integration of the

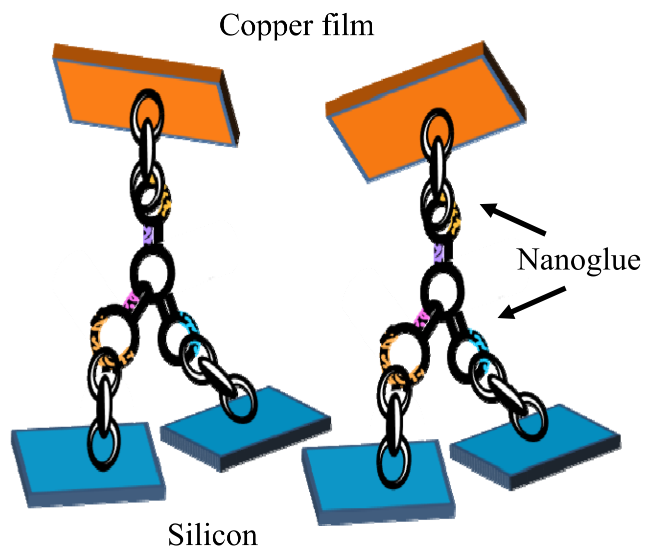


Figure 6.1. Annealing –induced interfacial bonding using molecular nanolayers [39].

sensing device and carbon nanotube cantilever, which will be attached to the amplifier circuit by the 3-mercapto-propyl-tri-methoxy-silane (MPTMS). In this device, the dielectric material is the air that will allow us to sense the desired gas particles.

(3-mercaptopropyl) trimethoxysilane (MPTMS) is synthesized through sol-gel processes. The MPTMS is material which possesses functional groups of thiol and silane. The MPTMS sol-gel is a non-cytotoxic material. Moreover, the MPTMS had been successfully implanted into the muscle tissues of rats for twenty eight days that without causing any inflammation in animal body that proved the MPTMS sol-gel is a biocompatible material and can be used in humans. The MPTMS sealing effectiveness was evaluated through a MPTMS sealed gold/glass tube assembly by a home-made CO_2 sensor apparatus. The MPTMS sol-gel can serve as a coating material to seal gaps between gold and glass [40].

There are two devices in Figure 6.2, one is the capacitive sensing device and another device is the carbon nanotube cantilever. The capacitive sensing device with two sensing electrodes (Figure 2.7) shows that one sensing electrode is guard electrode, which can reduce unwanted noise from the nearby circuitry and another is the driven electrode. The fabrication of this capacitive sensing device is shown from figures 6.3 to 6.12. In Figure 6.3, a SiO_2 film with thickness 500 nm needs to be deposited on a clean wafer surface. Before we deposit the SiO_2 film, the cleanness of silicon wafer is important. The RCA process has to be conducted to clean the surface of the silicon wafer in this integration device. This entire RCA cleaning process is same as we mentioned in the Chapter 4.

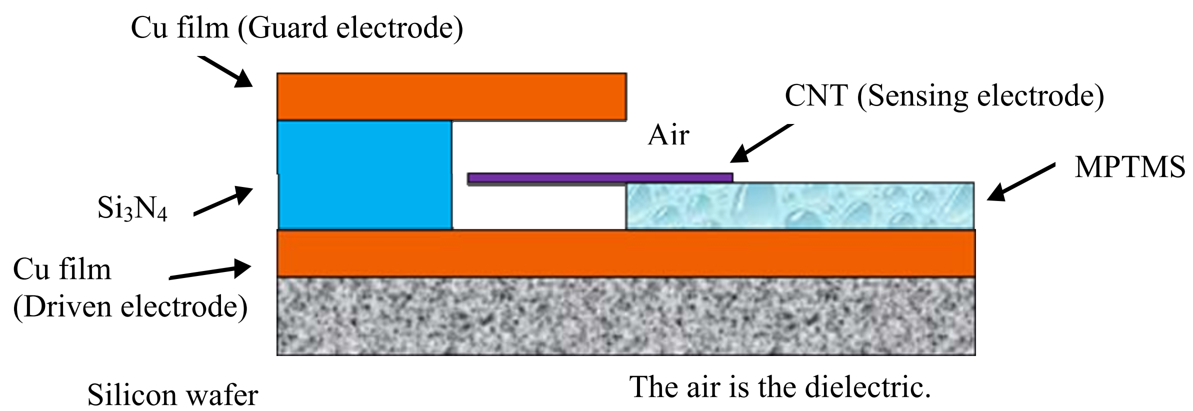


Figure 6.2. The integration of nanocantilever and capacitive sensing device.

In Figure 6.3, we deposit a SiO_2 layer with thickness around 20 to 50 Å, which can prevent our silicon wafer from reacting with oxygen in the environment at room temperature. The thickness of this SiO_2 layer is enough to block the oxygen reacting with our bare silicon wafer. In EMDL, the rf sputtering machine can deposit the silicon dioxide.

In Figure 6.4, a Cu film can be deposited by thermal evaporator with thickness around 2000 Å. This layer will be one of our electrodes in the capacitive sensing device which will connect to our circuit.

In order to create a cantilever electrode, a sacrificial layer is necessary for this fabrication. Before we remove this sacrificial layer, this layer is a support for the cantilever electrode. In Figure 6.5, we use amorphous silicon (a-Si) [41] with the thickness of 2 μm, by the low-pressure chemical vapor deposition (LPCVD). Amorphous silicon provides some advantages in this process. One of the main advantages of amorphous silicon over crystalline silicon is that this material can be deposited under a low temperature process. Moreover, the amorphous silicon is full of defects naturally, these defects make this material easy to be removed as we require in a sacrificial layer.

In Figure 6.6, a Si_3N_4 film with thickness ~ 2 μm can be deposited by rf sputtering for almost 2 hours. This layer separates two of these electrodes that provide a certain distance for electrodes. Si_3N_4 has a higher dc resistivity [33] than SiO_2 that provides better isolation for these electrodes. SiO_2 does not have any resistivity at 500 ºC, but Si_3N_4 provides resistivity $\sim 2 \times 10^{13}$ (ohm-cm).

In Figure 6.7, a Cu film will be deposited by thermal evaporator with thickness around 2000 Å, which would be another electrode in the capacitive sensing device. But for this Cu film, we will etch part of this film to make a cantilever electrode.

In Figure 6.8, a silicon nitride film will be deposited to a thickness ~ 300 Å by rf sputtering. Although this layer is thin, it prevents any future curling distortion from happening in Cu film [42] that can help the formation of the cantilever electrode.

After the deposition of silicon nitride, in Figure 6.9, the RIE process can be used to remove unnecessary Cu film to uncover the a-Si film for future sacrificial layer etching. In this RIE etching process, a pair of parallel electrodes and a 13.56 MHz rf power are required in the RIE reactor. Cl_2 (Chlorine) gas would be used in our experiments, but other gases, such as HCl or HBr also get similar etching results.

$$Cu + Cl_2 \longrightarrow CuCl + Cl \quad (6.1)$$

This etching process also can be preceded at 25°C substrate temperature. The diluted hydrogen chloride solution in 6 % deionized water can be used to remove the copper reaction compounds at room temperature.

Figure 6.10 shows the exposure of the a-Si layer after we remove the copper film. Removing copper film is the first step for us to etch the a-Si layer in this experiment. An aluminum film ~100 Å thick is deposited by dc sputtering on the top of the Si_3N_4 film after the removal of the Cu film. Figure 6.11 shows this Al film can cover the Si_3N_4 to form the electrode and also protects the Si_3N_4 film from being etched by future etching process.

Chromium (Cr) is a highly corrosion resistant material in the semiconductor process. Because of this property, Cr has been applied in many metallic industries. Our

experiment uses Cr film as a protection film which prevents the etching process damaging other layers [35].

Figure 6.12 shows that the sacrificial layer of the amorphous silicon removed by the xenon difluoride (XeF_2) [43, 44, 45]. A sacrificial layer must provide high etch rate that can be removed quickly and a large diffusion coefficient, which can penetrate narrow gap etch region. Xenon difluoride vapor is appropriate as a sacrificial layer because the after processed microstructure will not create capillary force in liquid etching. That is after the narrow gap etching process, it is unnecessary to dry the narrow gap because the micro- liquid amount will not accumulate in these gaps. The basic etch mechanism of the xenon difluoride is that xenon difluoride (XeF_2) discomposes as xenon (Xe) and fluorine (F) on the silicon wafer. The silicon etching process is dependent in fluorine.

$$2XeF_2 + Si \longrightarrow 2Xe + SiF_4 \qquad (6.2)$$

In order to streamline the silicon etching process, a buffer oxide etching (BOE) pre-etch process for 10 seconds is adapted to remove any oxide on the surface of silicon wafer. A drying process is necessary at 120° C for 10 minutes to prevent any moisture residue on the surface of the silicon which may cause HF formation. Moreover, native oxide may retard the etching process and cause an unsmooth etch surface. Figure 6.13 shows the cross-section after XeF_2 etching.

After this etching process, two parallel electrode devices are available for the capacitive sensing device as shown in Figure 6.14, which needs to be integrated with the CNT cantilever. The entire integration processes fabricate the driven and guard electrodes that will be integrate with readout CNT circuit and cantilever beams. The packaging will combine these devices.

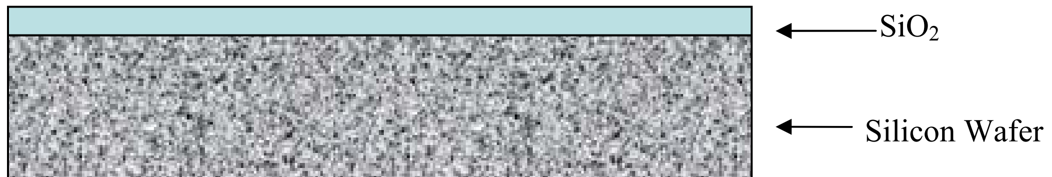


Figure 6.3. Oxidized silicon wafer.

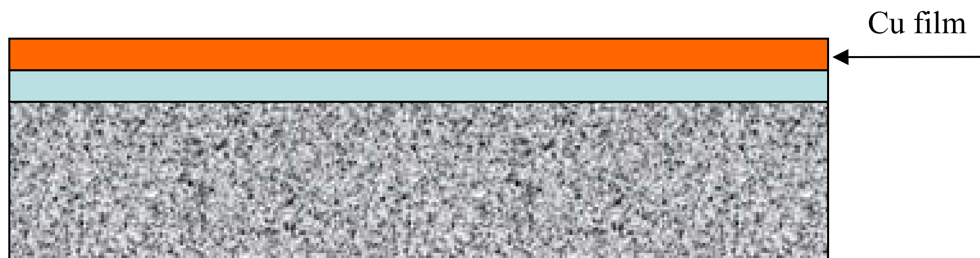


Figure 6.4. Cu film deposition.

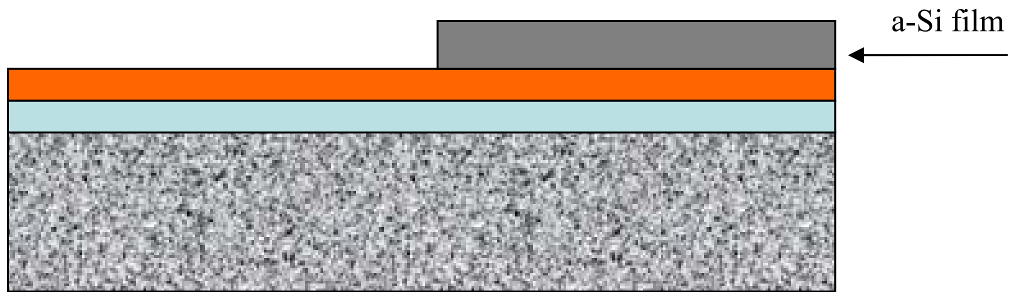


Figure 6.5. Amorphous silicon (a-Si) film deposition.

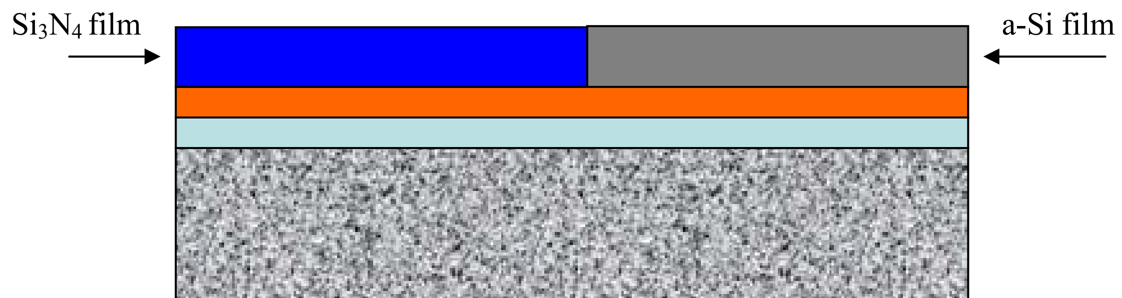


Figure 6.6. Si_3N_4 film deposition.

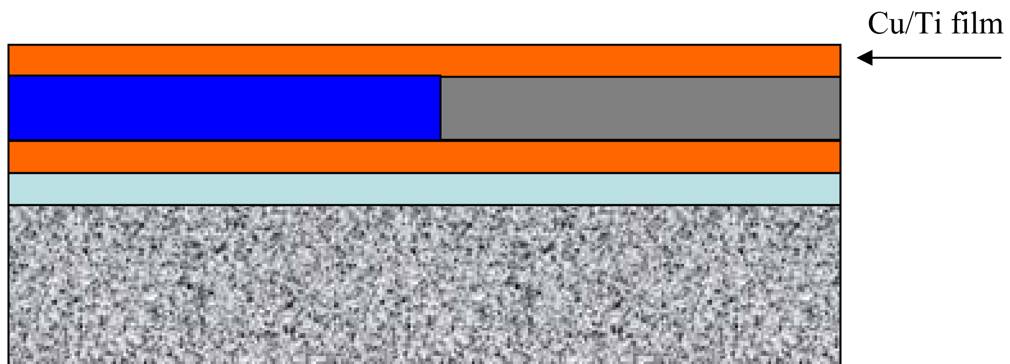


Figure 6.7. Cu/Ti film deposition.

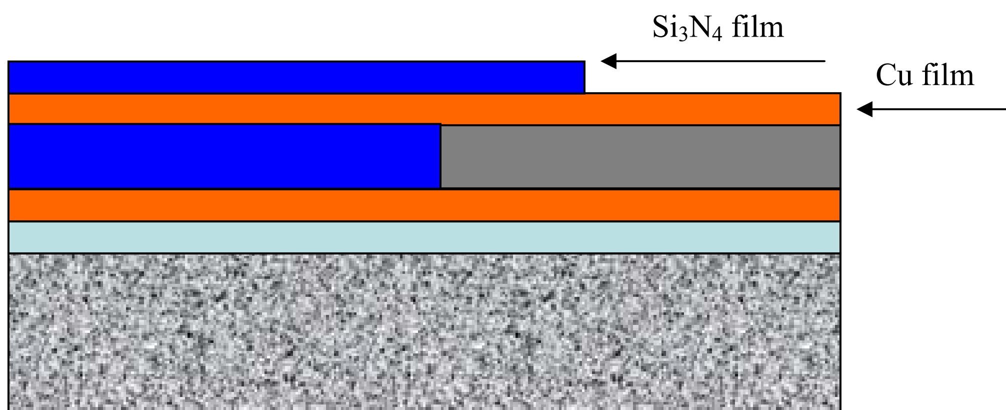


Figure 6.8. Si_3N_4 film deposition for the formation of electrode.

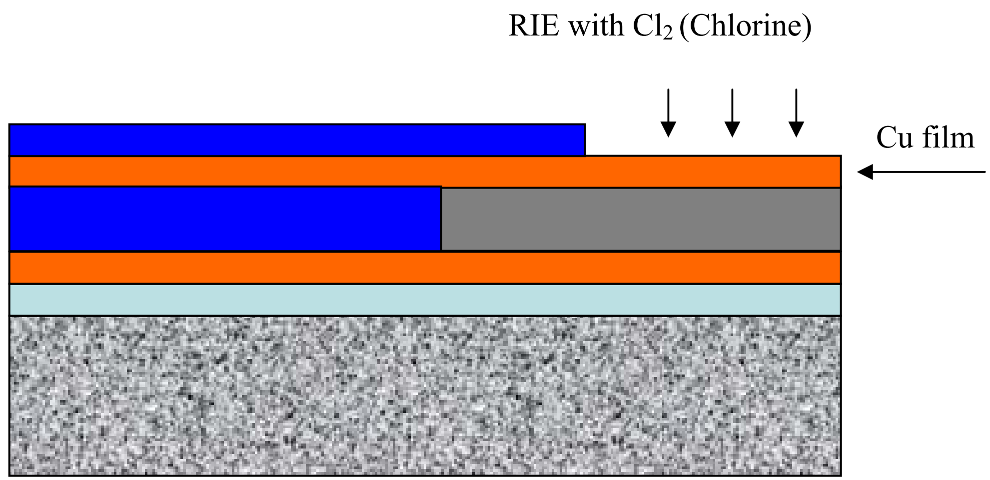


Figure 6.9. RIE process for the sacrificial layer etching.

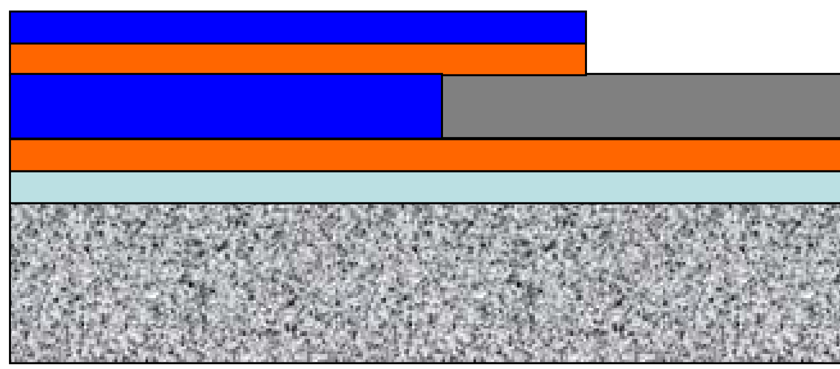


Figure 6.10. Process after RIE.

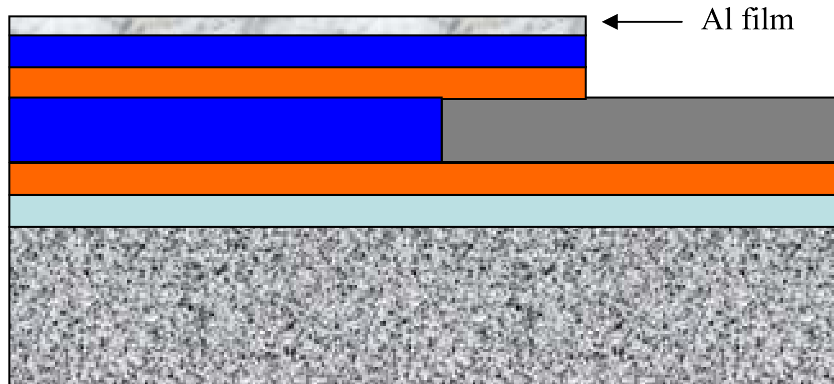


Figure 6.11. Al film deposition.

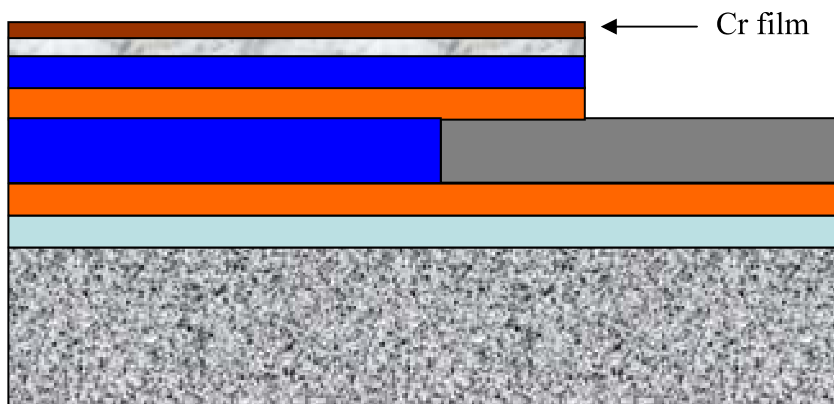
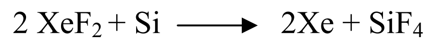


Figure 6.12. Cr film deposition.



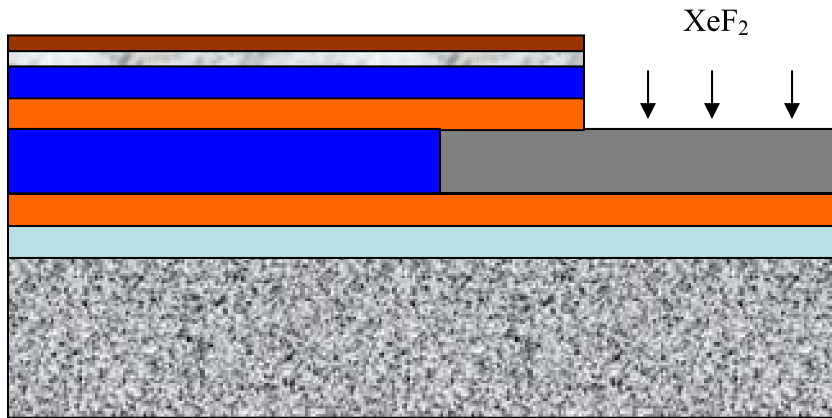


Figure 6.13. Etching process of the xenon difluoride.

Figure 6.14. Formations of the two electrodes.

6.2 Packaging

In order to protect and integrate the silicon chip, packaging is a necessary process to prevent the silicon chip from being damaged by the environment and integrate the electronic system. This packaging process will increase the thermal resistance from the chip to the ambient, increase the electrical delay because of parasitic capacitances and impedances.

Semiconductor packages have a large variety of packages because different companies have their own products. These differences increase the complexity of the semiconductor package. Although these package types are based on vendors' design, there are some characteristics that can be used to evaluate these packages. These criteria are packaging efficiency, leadcount, thermal performance and electrical performance.

6.2.1 Package Efficiency

Packaging efficiency is a parameter to evaluate the effectiveness of the packaging. The definition of the packaging efficiency is defined as:

$$E_P = \frac{A_{SC}}{A_P} \tag{6.7}$$

In equation (6.7), E_P is the packaging efficiency, A_{SC} is the silicon chip area and A_P is the package area. The weight of the entire chip and size also influence the packaging efficiency. The packaging efficiency has to be high for all packaging types. For example, if a package provides 100% efficiency this means that the silicon chip area equals the size of the package. In our research, we do not intend to pack our device completely because the CNT cantilever beam has to contact with the air.

6.2.2 Leadcount

Leads are the interconnection for silicon chips that are embedded in the package to the entire circuit devices. A packaged silicon chip must have several leads to connect the device and power with other components. These leads increase the resistance and capacitance of the semiconductor.

6.2.3 Thermal Performance

Electrical components need power for their operation, as the same time, the power consumption generates heat because of the resistance of the circuits. This heat has to be transferred to the environment to prevent the temperature from rising over the safe operating temperature and cause further permanent damage to these chips. Thermal resistance, as the unit in terms of °C/Watt, is the parameter to measure the ability of heat transfer from the chip to the ambient. The safe operating temperature needs to be maintained at less than 100 °C that keeps circuits within a normal operation condition.

6.2.4 Electrical Performance

Electrical performance of a circuit is highly correlated to the delay, crosstalk and supply voltage. These three parameters influence the performance of IC. Interconnection is the main cause of a delay because the more interconnection the more time needed for the signal transmission. Crosstalk is another cause of delay of the circuit because of the electromagnetic induction of voltage between two neighboring lines. If the switching rate of the circuit is very high and the distance between two neighboring line is very low, the crosstalk may cause a seriously problem. Supply voltage also influences IC performance. During the fast switching rate of circuits, the supply voltage can not follow the fast transient status that creates the voltage dip in the current supply. Because the inability to follow the fast transient current and the voltage dip problem, noise will be

generated by these phenomenon. Lower supply voltage can reduce the noise problem and heat generation.

6.3 Interconnection

In semiconductor packaging processes, the interconnection is a key process which dominates the transmission of the signal from silicon chip to the entire circuits. There are two categories in the package; one is the die-to-substrate interconnection, and interconnection on substrates. In our research, we will focus on the die-to-substrate interconnection. Wire bonding, tape automated bonding (TAB) and controlled collapse chip connection (C4) are the most popular interconnection methods for the die-to-substrate connection.

6.3.1 Wire Bonding

Wire bonding is the oldest and most popular interconnection method. Gold or aluminum wires are used for the interconnection. In EMDL, we use gold wire for the wire bonding. Wire bonding is done after the die has been attached on the leadframe. Between the leadframe and the silicon chip, a conductive epoxy or polymer will be used to attach the chip to the leadframe. After the chip is right on the position, the bonding machine places the gold wire on the pad through a thermo compression or the ultra sonic process which is generated by the transducer. Figure 6.15 shows the structure of the wire bonding that the substrate may use ceramic or leadframe. Wire bonding provides low cost as an advantage but the process is slow because this machine only can bond one wire each time.

6.3.2 Tape Automated Bonding

The tape automated bonding process was developed by General Electric. A conductive pattern of copper film is created by the photolithography process as a leads on the polyimide tape which will attach or support the silicon chip.

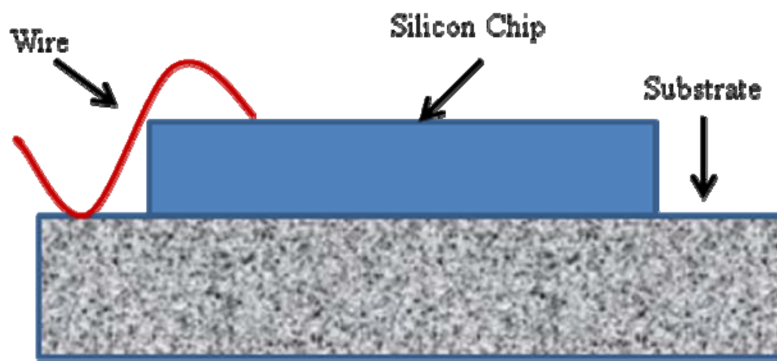


Figure 6.15. The structure of a wire bond assembly.

This film will be moved to the required location on the printed circuit board. An inner lead bonding process will help the connection between the tape and the silicon chip and the outer lead connection can bond the printed circuit board with the silicon chip. This process provides the shortest connection between the silicon and package that reduces unnecessary resistance and capacitance from the wire connection. The taped automated bonding method is presented in Figure 6.16 [46].

6.3.3 Controlled Collapse Chip Connection (C4)

This packaging technology was developed by IBM to create a reliable and high productivity packaging approach. This method also is known as flip-chip technology, which flips chips upside down and mounts the silicon chip with a package. The solder bump will be put on the mold pad, after the process, the wafer will be aligned on the top of the bump pad which has the sold bump. A mounting process bonds the wafer and sold bump together. This technique provides the shortest interconnection between silicon chip and package. Figure 6.17 and 6.18 [47] show the details of entire process.

6.4 Packaging of Our Devices

In last section, we mentioned three different packaging approaches. Considering these approaches, the wire bonding is appropriate for our design if we evaluate the cost, equipment and the complexity. The first step in this packaging process is to attach the device on the Cu lead frame by the conductive epoxy. The wire bonding is done after this device is attached on the Cu lead frame, which can help the heat dissipation of the circuit. The plastic compound can be used in the package after the wire bonding. In order to make contact with the air, this package can not be completely covered so this device has to contact with the air to allow carbon nanotubes to react with certain gas species. The structure of this gas capacitive sensor is shown in Figure 6.19.

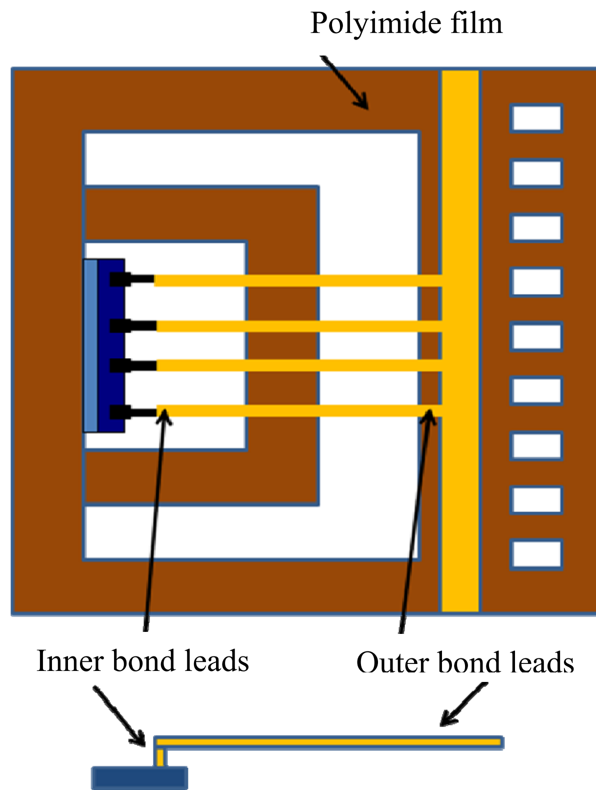


Figure 6.16. Tape automated bonding structure [46].

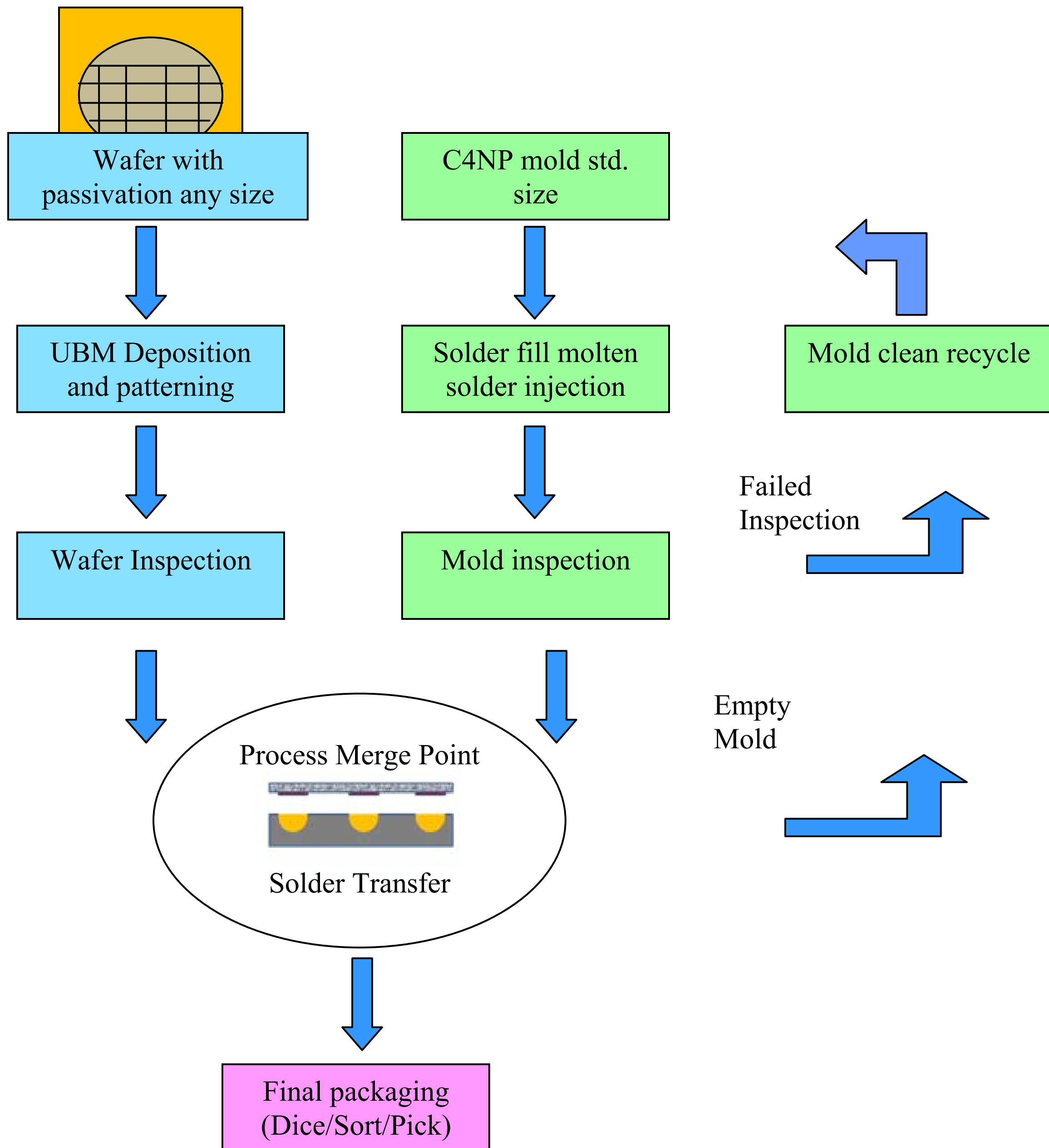


Figure 6.17. The controlled collapse chip connection concept [47].

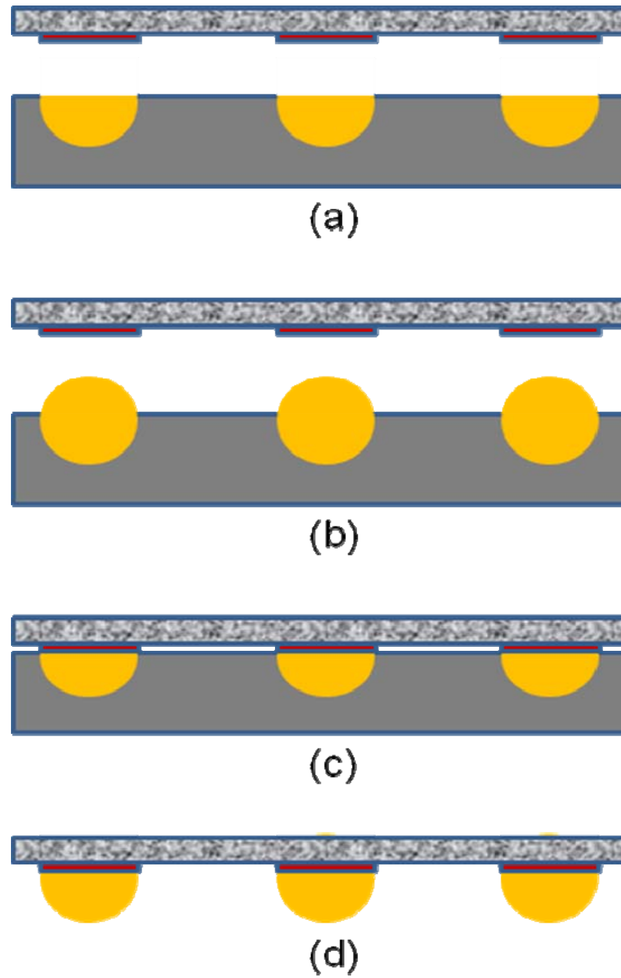


Figure 6.18. Controlled collapse chip connection process: (a) wafer and solder are aligned, (b) increase the temperature of the mold to liquefy the solder, (c) mount the wafer and mold together and (d) after the separation of the wafer and mold, solder attaches on the wafer [47].

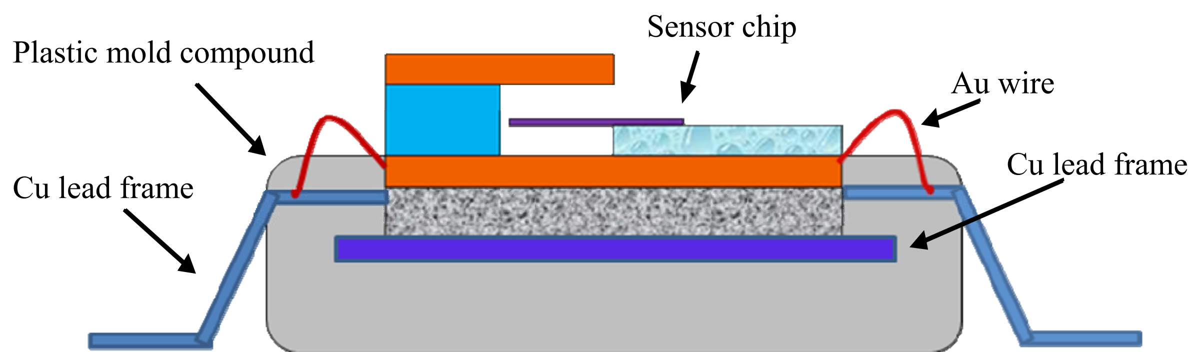


Figure 6.19. Structure of the gas sensing device with package.

CHAPTER 7
CONCLUSION AND FUTURE WORK

7.1 Conclusions

1. The single walled carbon nanotube cantilever vibration has been simulated by ANSYS, which shows the SWCNTs will vibrate after react with gas particles.
2. The nanotube cantilever beam has been fabricated over a µm size gap on silicon that provides a single nanotube to react with gas particles.
3. The capacitive-sensing circuit has been presented to convert the vibration of CNT cantilever into capacitance. Circuit layout and the SPICE simulations have been done. SPICE simulation results show that the increasing of capacitance will also increase the output voltage.
4. Integration and packaging issues have been discussed. Integration has provided the solution for combination of circuit and nanotube cantilever.

7.2 Future Work

In our research, SWCNT cantilever beam formation over the gap (nm-µm) in silicon was the prime objective. We used one of the popular methods for the fabrication. However, precise alignment of the CNTs in a required position is still a challenge.

AFM and SEM techniques have been used to manipulate carbon nanotubes, but the operation process is extremely slow and unstable. In order to align the SWCNT in the required position, we propose a new idea for our future work as shown in Figure 7.1 which is similar to earlier processes except that each side of gap has a Cr triangle film that can provide ac voltage to connect CNT to the tip of the triangle.

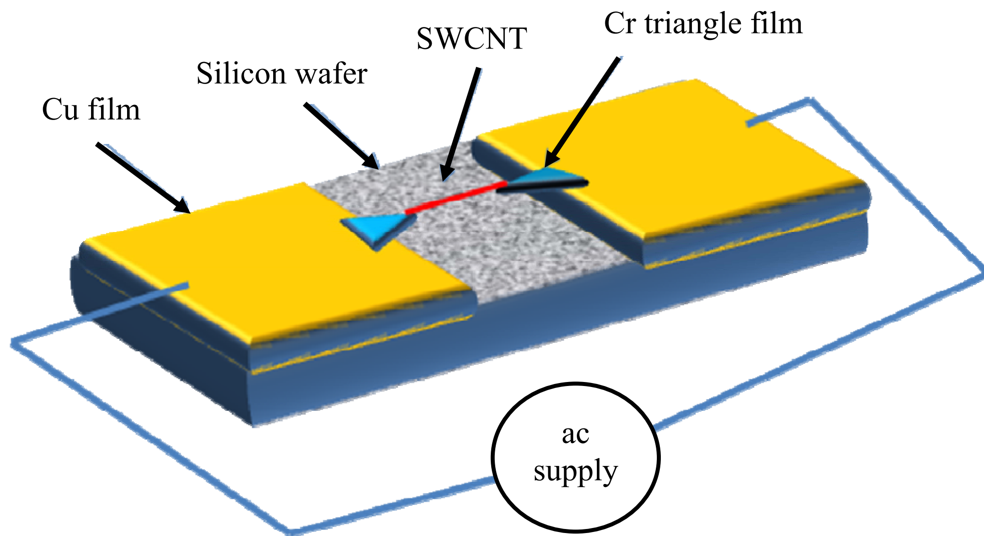


Figure 7.1. SWCNT fabrication on a triangle Cr film.

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VITA

Jui-Ching Hsu was born in Taichung, Taiwan. He received his bachelor degree of science from National Taiwan University. He is enrolled in the Department of Electrical and Computer Engineering at Louisiana State University, Baton Rouge, Louisiana, to attend graduate school. His research interests include circuit design and nanotechnology.