2008

Quiescent current testing of CMOS data converters

Siva Yellampalli
Louisiana State University and Agricultural and Mechanical College, syella1@lsu.edu

QUIESCENT CURRENT TESTING OF CMOS DATA CONVERTERS

A Dissertation

Submitted to the Graduate Faculty of the
Louisiana State University and
Agricultural and Mechanical College
in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

in

The Department of Electrical and Computer Engineering

by
Siva Yellampalli
Bachelor of Engineering, Jawaharlal Nehru Technological University, India 2001
M.S., Louisiana State University, Baton Rouge, U.S.A. 2004
December, 2008

ACKNOWLEDGMENTS

I dedicate my work to my parents Mr. Nageswara Rao and Mrs. Vijaya Lakshmi, my brother and sister-in law Mr. Sapta Nag and Mrs. Parimala and my grandparents Mr. Gandhi and Mrs. Sambrajam for their constant support and encouragement throughout my life.

I am very grateful to my advisor Dr. A. Srivastava for his guidance, patience and understanding throughout this work. His suggestions and discussion helped me to get deep insight into the field of VLSI design and testing.

I like to thank Dr. M. Cherry, Dr. M. Feldman, Dr. S. Rai, Dr. J. Trahan, and Dr. M. Tom for being a part of my committee.

I am thankful to Dr. H. Wu, Mr. G. Hwuang, Dr. S. McGuire and Dr. G. Powe for their help and guidance at times I needed them.

I thank Electrical and Computer Engineering Department, Center for Academic Success, and Office of Strategic Initiatives for supporting me financially during my stay at LSU.

I would like to thank my friends Abhilash, Chetan, Chi, Dattu, Jose, Kalyan, Kishore(KK), Mani, Naga, Prashant, Pavan, Richard, Satish, Sudheer, Vani and Vinod for there support, help and encouragement. I also like to thank all my friends and roommates here who made my stay at LSU enjoyable and memorable one.

Above all I thank GOD for keeping me in good health and spirits throughout my stay at LSU.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

Power supply quiescent current (I_{DDQ}) testing has been very effective in VLSI circuits designed in CMOS processes detecting physical defects such as open and shorts and bridging defects. However, in sub-micron VLSI circuits, I_{DDQ} is masked by the increased subthreshold (leakage) current of MOSFETs affecting the efficiency of I_{DDQ} testing. In this work, an attempt has been made to perform robust I_{DDQ} testing in presence of increased leakage current by suitably modifying some of the test methods normally used in industry.

Digital CMOS integrated circuits have been tested successfully using I_{DDQ} and ΔI_{DDQ} methods for physical defects. However, testing of analog circuits is still a problem due to variation in design from one specific application to other. The increased leakage current further complicates not only the design but also testing. Mixed-signal integrated circuits such as the data converters are even more difficult to test because both analog and digital functions are built on the same substrate. We have re-examined both I_{DDQ} and ΔI_{DDQ} methods of testing digital CMOS VLSI circuits and added features to minimize the influence of leakage current. We have designed built-in current sensors (BICS) for on-chip testing of analog and mixed-signal integrated circuits. We have also combined quiescent current testing with oscillation and transient current techniques to map large number of manufacturing defects on a chip. In testing, we have used a simple method of injecting faults simulating manufacturing defects invented in our VLSI research group.

We present design and testing of analog and mixed-signal integrated circuits with on-chip BICS such as an operational amplifier, 12-bit charge scaling architecture based digital-to-analog converter (DAC), 12-bit recycling architecture based analog-to-digital converter (ADC) and operational amplifier with floating gate inputs. The designed circuits are

fabricated in 0.5 μm and 1.5 μm n-well CMOS processes and tested. Experimentally observed results of the fabricated devices are compared with simulations from SPICE* using MOS level 3 and BSIM3.1 model parameters for 1.5 μm and 0.5 μm n-well CMOS technologies†, respectively. We have also explored the possibility of using noise in VLSI circuits for testing defects and present the method we have developed.

* SPICE: Simulation Program with Integrated Circuit Emphasis originated from UC Berkley in the early seventies.
† URL: www.mosis.org.

CHAPTER 1
INTRODUCTION

Testing is an integral part of integrated circuit manufacturing [1]. In the days when the integrated circuits manufactured had no more than few hundred devices, circuit design engineers and test engineers worked in isolation, test engineers became part of the manufacturing cycle only after the design was complete. With the increase in the density of transistors on a chip and the complexity of the design in integrated circuits, testing has been integrated with the design and production cycles. Designers use testability measures to identify portions of a circuit that would be difficult to test. Such inaccessible circuits are said to have poor controllability or observability. Controllability is a measure of the ease with which a test engineer can control signals in a circuit from the input pins. Similarly, observability is a measure of the ease of determining the behavior of a circuit from the output pins. After identifying a general section of a chip that has poor controllability or observability the engineer can then modify the circuit to be more testable, this method of design process is called design-for-testability (DFT) [2].

Testing methods are broadly classified into operational tests and defect based tests. Operational tests are further sub-divided into logic based testing and scan based testing. In logic based testing, input vectors are given to the circuit and the logic levels at different nodes are observed for fault detection [3]. Boundary scan test method has two modes of operation: normal mode and scan mode. In scan mode, input is shifted through the shift registers and observed at the output pin which has been added for the sole purpose of testing [1]. Thus additional circuitry is needed to convert circuit under test (CUT) into a shift register in scan mode.

Fault detection in high density transistor chips using operational test has become very

complex and challenging due to increase in input vectors [1]. Testing techniques such as divide and conquer have been proposed [4, 5] to increase the efficiency of fault detection in integrated circuits. In this technique, a partitioned circuit would be designed with a test mode that would connect the input and output of each partitioned block to the output pins of the chip such that the block could be observed. In this test method each block is extensively tested with a built-in test circuit for fault identification. Partitioning the circuit is advantageous for implementing built-in current testing approach for defect based testing. Built-in current testing approach has been found advantageous for power supply quiescent current (I_{DDQ}) testing which is a defect based testing [6]. When combined with the traditional logic testing, better quality levels than those achievable by a single technique are obtained [7].

Integrated Circuits (ICs) are classified into digital and analog integrated circuits. Mixed signal integrated circuits are those that contain both digital and analog circuits on the same chip, they consist combinations of amplifiers, filters, switches, ADCs, DACs and other types of specialized analog and digital functions. Mixed signal integrated circuits are used today in broad application areas such as telecommunications, consumer electronics, computers, multimedia, automotive systems, biomedical instrumentation and aerospace [8]. The main advantages in having both analog and digital circuits on the same chip are the reduction in size of the circuit, increase in speed of operation, reduction in power dissipation, increase in design flexibility and increased reliability. Due to these advantages and the increasing complexity of electronic systems more and more system functionalities have been integrated onto a single chip in recent years. Consequently an increasing number of chips that combine digital and analog functions are designed. The increase in circuit complexity is posing a major challenge in design and testing of mixed signal integrated circuits [9].

1.1 Need for Testing Mixed Signal Circuits

Integrated circuits are fabricated using a series of photolithographic processes such as etching and doping. Like any photographic process, the IC process is subject to blemishes and imperfections. These imperfections may cause either catastrophic failures in the operation of any individual IC or minor variations in the performance from one IC to the next [9]. The faults causing catastrophic failures are called catastrophic faults or hard faults and the faults that cause minor variation in performance are referred to as soft faults or parametric faults. The short and open defects are generally classified as hard faults. These are caused due to dust particles, over etching or extra metal extensions which join the lines.

1.1.1 Bridging Faults

The short circuit faults in very large scale integrated circuits are popularly termed as bridging faults. With I_{DDQ} measurement, a bridging fault can be detected between two nodes having opposite logical values in the fault free circuit [7]. Bridging faults can appear either at the logical output of a gate or at the transistor nodes internal to a gate. Inter-gate bridges between the outputs of independent logic gates can also occur. Bridging fault can occur between any of the following nodes of the transistor: drain and source, drain and gate, source and gate, bulk and gate and within the circuit. Figure 1.1 shows example of bridging faults in an inverter chain in the form of low resistance bridges (R_1, R_2, R_3 and R_4). Figure 1.2 shows examples of gate to source and gate to drain bridging faults in a NAND gate circuit.

1.1.2 Gate Oxide Short Defects

The oxide faults are one of the prominent faults in submicron CMOS technology due to decreasing oxide thickness. The physical reasons responsible for gate oxide shorts (GOS) are due to the breakdown of the gate oxide and manufacturing spot defects due to pinholes in

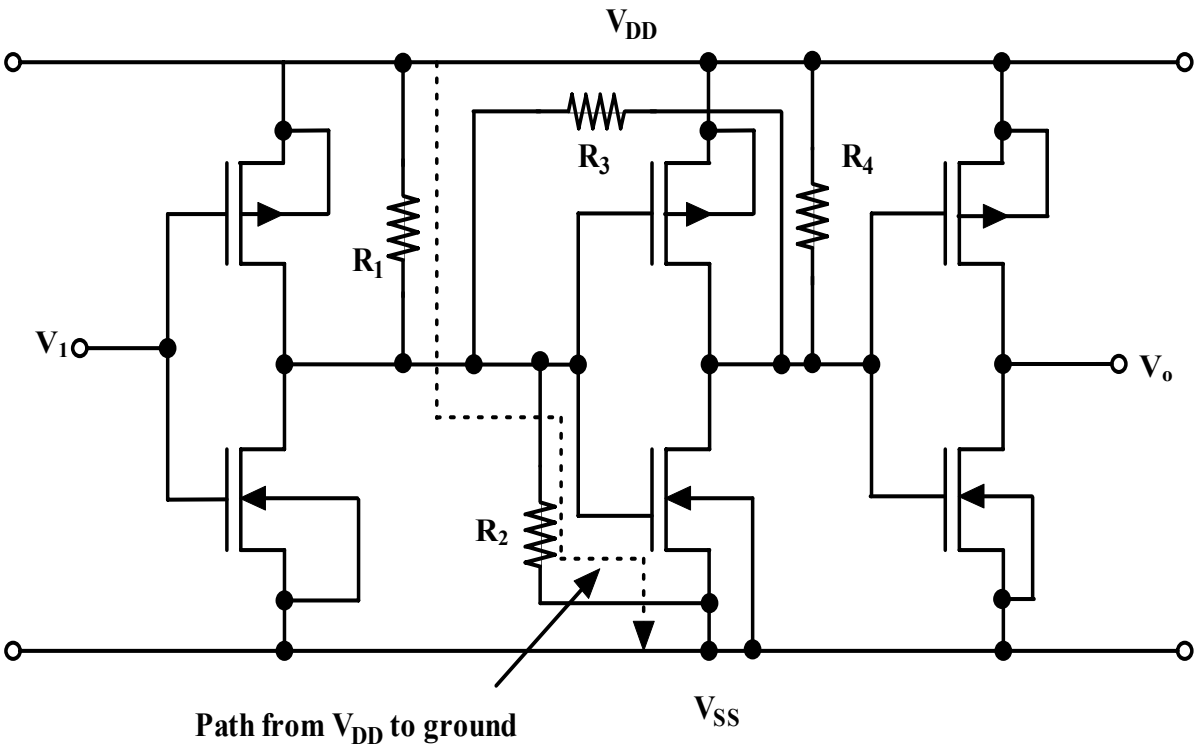


Figure 1.1: An example of bridging faults in an inverter.

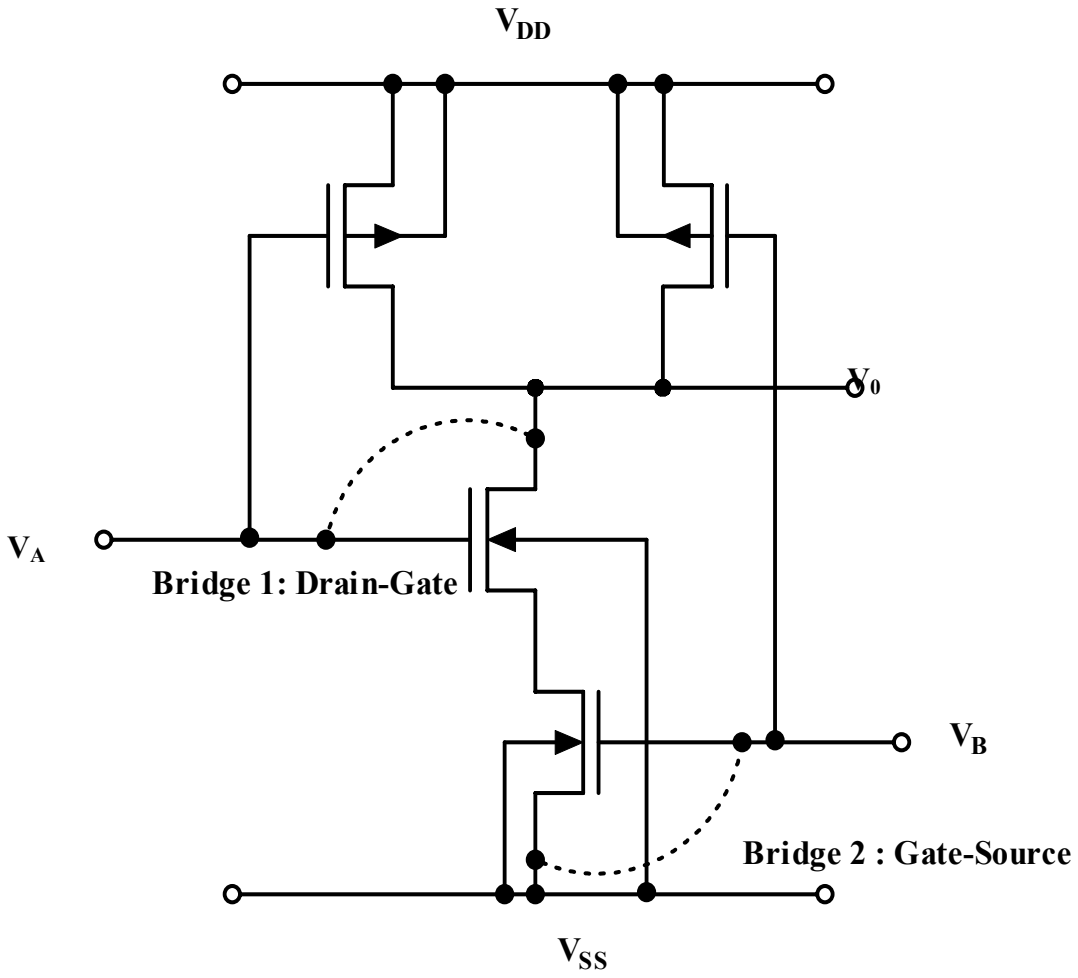


Figure 1.2: An example of drain-gate and gate-source bridging faults in an NAND gate.

lithography and processes on the active area and polysilicon masks [10, 11]. These faults are formed between the gate and the channel and gate and source or drain. The gate oxide defects cause current to flow from the gate into substrate affecting the MOSFET behavior [12].

1.1.3 Open Faults

Figure 1.3 shows a 2-input NAND gate with open circuit defect. In Figure 1.3 node V_B is floating. Logic gate inputs that are unconnected/floating are usually in high impedance state and may, or may not, change I_{DDQ} current. An open defect might make the transistor partially conducting as the floating-gate may assume a voltage because of parasitic capacitances and hence, a single floating-gate may not cause a logical malfunction. It may cause only additional circuit delay and abnormal bus current [13]. In Figure 1.3, when the node voltage (V_B) reaches a steady state value, the output voltage correspondingly exhibits a logically stuck behavior and this output value can be a weak or a strong logic voltage. Open faults however may cause only small rise in current so they are sometimes difficult to detect.

1.2 Testing Mixed Signal Integrated Circuits

Testing digital circuits has earned enough maturity in terms of the availability of CAD tools and structured test strategies [1] but testing of analog integrated circuits has not reached that stage. Testing digital circuits is simplified due to the logical relationship between input and output, such relationship does not exist for analog circuits making it complex and difficult to model. Analog circuits are often non-linear and binary pass and fail distinction for fault detection is not possible in them. Their performance is heavily dependent on circuit parameters and a small variation in them cause performance degradation. Modeling the variation in analog circuit performance is very complex. Digital test schemes based on structural division of the circuit, when applied in analog domain are also largely unsuccessful because their impact on circuit performance. In analog circuits, there are no well established

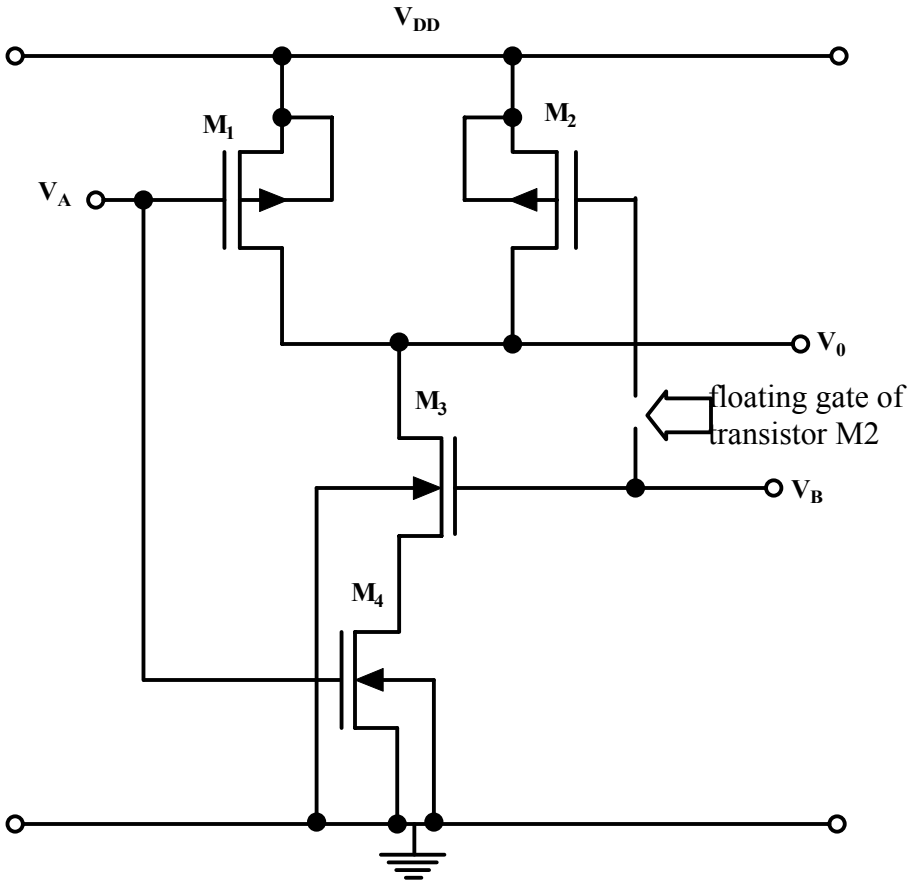


Figure 1.3: Floating gate transistor (M_2) in a 2 input NAND gate.

fault models available like digital circuits. The absence of acceptable fault models, the testing of analog circuits has been largely functional in nature [14]. Analog functional testing is costly and time consuming because each specification needs a different test setup.

In addition, compared with the analog test, the test for mixed-signal circuits has even more problems because both analog and digital circuits are built on the same substrate. The performance of mixed-signal test is affected not only by external influences such as the supply voltage variation but also by the internal influences such as noise from the digital parts which may effect the functioning of the analog parts. Combining both analog and digital circuits has lead to non standard test strategies and results in complex and expensive mixed-signal automatic test equipment (ATE) [14]. Recently, design-for-test (DFT) and built-in self test (BIST) for analog and mixed-signal circuits have received the growing attention to alleviate increasing test related difficulties [14].

Among frequently used mixed signal circuits, data converters are typical mixed signal circuits. Analog-to-digital converter (ADC) provides the interface from analog-to-digital domain; meanwhile digital-to-analog converter (DAC) sets up the bridge from the binary digital domain to the analog world. The converters are widely used in modern measurements, control instrumentation and systems. They are also employed in pairs by the application in fields such as the wireless telecommunications, data exchange systems and satellite communications systems. Testing of data converters can be divided into functionality based testing and fault detection based testing. Extensive research has been done on the functionality based testing of data converters and analog and mixed-signal integrated circuits. Performances used for testing the functional behavior of ADC are the offset voltage, gain, differential non linearity (DNL), integral non linearity (INL), signal-to-noise ratio (SNR) and the effective number of bits (ENOB). Tests for analog circuit blocks within a mixed-signal

design are generally derived from their functional descriptions and are specification oriented. Methods such as VBIST and IBIST [15], ADC and DAC BIST [16], BIST for converters on a CODEC chip [17], HBIST [18], MADBIST [19], OBIST [20], T-BIST [21], BIST for ADC [22], histogram test technique based BIST [23], BIST scheme for an SNR test [24], practical BIST approach for functional testing to measure offset, gain, linearity and differential linearity errors without test equipment [25] have been proposed in literature for functional based testing. Defect oriented testing has been introduced as an alternative to functional based testing for analog and mixed signal circuits because each specification is tested in a different manner making analog functional testing expensive and time consuming. Defect oriented testing method has been well established for digital circuits because of standardized fault models but its application on analog circuits is still limited because analog circuits performance is parameter dependent [14]. By adapting the typical defect-oriented tests, such as scan based testing, voltage and current monitoring based test methods, some latent defects for functional tests can be effectively caught [26]. To improve the effectiveness of defect oriented testing, design methods such as multiplexing-based approach [27] have been used in designing the circuit under test. In this method, the observability and controllability of mixed signal integrated circuit is enhanced by isolating the embedded analog components from the digital components by adding external switching circuitry. Defect oriented testing is done using either off-chip or on-chip sensors. Off-chip testing is done by copying the bias current off-chip to support wafer level current testing [28] for fault detection in analog and mixed-signal circuits. On-chip testing is done by using a built-in sensor to detect the fault. In this work, we concentrate on built-in sensors based testing.

In mixed signal circuits, the boundary-scan path is designed to test the digital part of the mixed signal circuit [29]. Figure 1.4 illustrates a mixed signal integrated circuit that

contains a large digital block and an ADC converter. The analog input signal is given to ADC converter and the generated digital signal is given to the digital logic block. For boundary scan test the provision of access to the analog/digital interface separates the analog and digital blocks and allows them to be tested individually using the test techniques best suited to the block designs. For the boundary scan test the input to the system is given through pin TD0 and output is observed at pin TD1. Tests for the digital block can be performed without having to propagate signals through the analog block and the analog block can be tested without having to propagate signals through the potentially complex digital block. Some of the complexity in testing a complete mixed-signal circuit arises due to the inherent tolerances such as voltage fluctuations and noise in an ADC. Due to these tolerances any given voltage applied at the analog input can give rise to one of a range of digital codes at the converters output. During testing, such uncertainty in the pattern applied to the digital circuit block is difficult to accommodate because digital testing requires precise knowledge of the pattern being applied at any test step. Logic BIST has been combined with scan chain segmentation and automation test point insertion techniques for maximum fault coverage [30-32]. Hardware systems have been used for weighted random pattern generation in a boundary scan based testing [33]. Cellular automation registers (CARs) testing or linear feedback registers (LISRs) have been used as a source of random patterns.

Current based defect oriented testing methodology based on the observation of quiescent current on power supply lines allows a good coverage of physical defects such as gate oxide shorts, floating-gates and bridging faults, which are undetectable by conventional logic tests [7]. In addition, I_{DDQ} testing can be used as a reliability predictor due to its ability to detect defects that may result in functional failures at an early stage of circuit life. Due to obvious quality and reliability improvements, this approach became powerful complement to

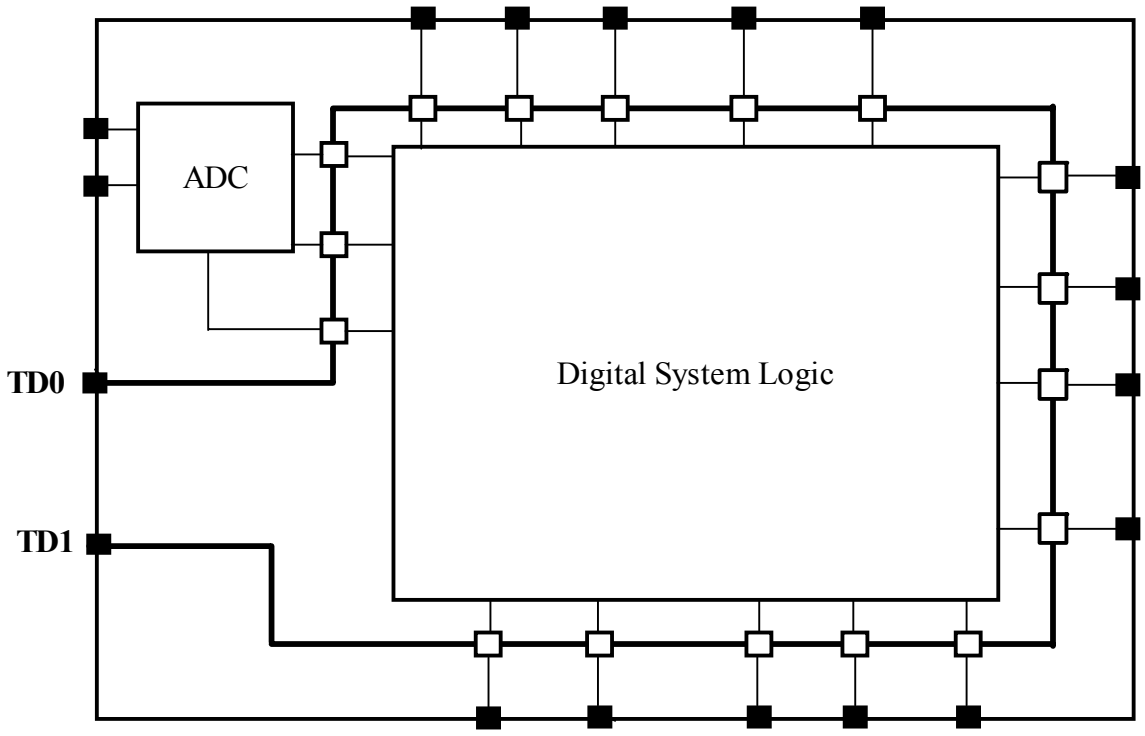


Figure 1.4: The location of a boundary scan path at the analog/digital interface [29].

the conventional logic testing. Quiescent current monitoring is considered as an interesting and efficient technique for mixed-signal testing, where fault detection in analog parts requires the precise measurement of I_{DDQ} current. In analog circuits, the quiescent current may be in the order of μA or even mA. Under fault conditions, the normal values of I_{DDQ} currents may increase or decrease. Thus, fault detection can be accomplished by monitoring the I_{DDQ} current.

1.3 Quiescent Current (I_{DDQ}) Testing

I_{DDQ} testing is a physical defect oriented test method that measures device supply current under steady state conditions for fault detection. The present form of quiescent current (I_{DDQ}) measurement based testing for CMOS VLSI, known as I_{DDQ} testing was first proposed by Levi in 1981 [34] and was used in detection of bridging faults [35]. In the following years, a number of laboratories reported that monitoring quiescent current is an effective method to detect various physical defects such as the bridging, gate oxide shorts, inter-gate shorts, stuck-on faults etc. [7, 10]. I_{DDQ} testing started to gain industrial importance in early 1990 after simulation methods such as *Inductive Fault Analysis* showed that many defects do not map onto stuck-at faults and cannot be detected by conventional testing [36]. The reasons such as cost effectiveness, negligible or no area overhead or increase in die size and a small number of vectors in I_{DDQ} test set were also responsible for I_{DDQ} test gaining popularity.

Since I_{DDQ} testing is a physical defect oriented testing, some researchers considered I_{DDQ} testing as a part of reliability testing, although many others considered it as a supplement to the functional/logical testing. In mid 1990's, a number of studies were conducted to correlate the effectiveness of I_{DDQ} testing with conventional reliability screening and burn-in tests [37, 38]. In 2001, Semiconductor Research Corporation (SRC)

task force identified I_{DDQ} and defect oriented testing as one of the key test methodologies with other methodologies such as core test of late 1990s [39].

As mentioned above, I_{DDQ} test is a defect based test that measures device supply current under steady state conditions. Fully static CMOS circuits consume little power in steady state because there is no direct path between V_{DD} and ground neglecting leakage currents. If an integrated circuit draws a large amount of current under static operation it is a defective circuit [34, 35].

I_{DDQ} test is capable of detecting shorts between two switching nodes, node and a power supply or between V_{DD} and ground [40]. The major advantage of current-based testing is that it does not require propagation of a fault effect to be observed at the output, it requires only exciting the fault model and then measuring the current from the power supply. The fault effect observance is the measurement of current, and the detection criterion is the current flow value exceeding some threshold limit. The current passing through V_{DD} or GND terminals is monitored during the application of an input stimulus for fault detection.

Current variations can be monitored using an on-chip or off-chip current sensors. On-chip or built-in current sensors (BICS) have speed and resolution enhancements over off-chip current sensors because they bypass the large transient currents in the output drivers. This makes on-chip current testing both time-efficient and sensitive to measure small variations in the quiescent current.

Figure 1.5 shows the block diagram of the I_{DDQ} testing with BICS. I_{DDQ} testing can be done by adding BICS in series with V_{DD} or GND lines of the circuit under test. For I_{DDQ} testing a series of input stimuli is applied to the device under test while monitoring the current of the power supply (V_{DD}) or ground (GND) terminals in the quiescent state conditions after the inputs have changed and prior to the next input change. For effective

I_{DDQ} testing subthreshold current in the transistors, which are 'off' in a CMOS static circuit should be negligibly small.

1.4 ΔI_{DDQ} Testing

In VLSI circuits designed in sub-micron/deep submicron CMOS processes, the reference I_{DDQ} is masked by the increased subthreshold (leakage) current of MOSFETs [41-43]. The I_{DDQ} testing has become even more difficult due to increased density of MOSFETs in a VLSI chip.

The problems related with I_{DDQ} testing in digital VLSI circuits designed in submicron CMOS processes are known and attempts have been made to re-examine the conventional I_{DDQ} testing [42, 44-51]. Isern and Figueras [52] have presented a detailed review of I_{DDQ} test and diagnosis of CMOS VLSI circuits. Soden et al., [53], Athan et al., [54] and William et al., [55] have presented limitations of I_{DDQ} testing due to increased subthreshold current in MOSFETs. Tsiatouhas et al., [56] have presented a new scheme for I_{DDQ} testing in deep submicron CMOS circuits. In a recent work, Vazquez and de Gyvez [57, 58] summarized several improved techniques utilizing standard approaches and some of the newer methods such as current ratios, DECOUPLE and Delta-I_{DDQ} [59-71]. An excellent review on I_{DDQ} testing is presented by Ferre et al., [41] and testing in nanometer technologies by Tsiatouhas [43].

Vazquez and de Gyvez [57, 58] implemented a BICS for submicron digital CMOS IC testing which takes into consideration increased leakage current of the circuit and variance due to process variations. Their method is based on a well known Keating-Meyer [72] approach for I_{DDQ} testing reported in 1987 and off-chip I_{DDQ} measurement Quick-Mon circuit reported by Wallquist et al., [73]. The method provides a better solution of testing submicron CMOS ICs with speed and reliability.

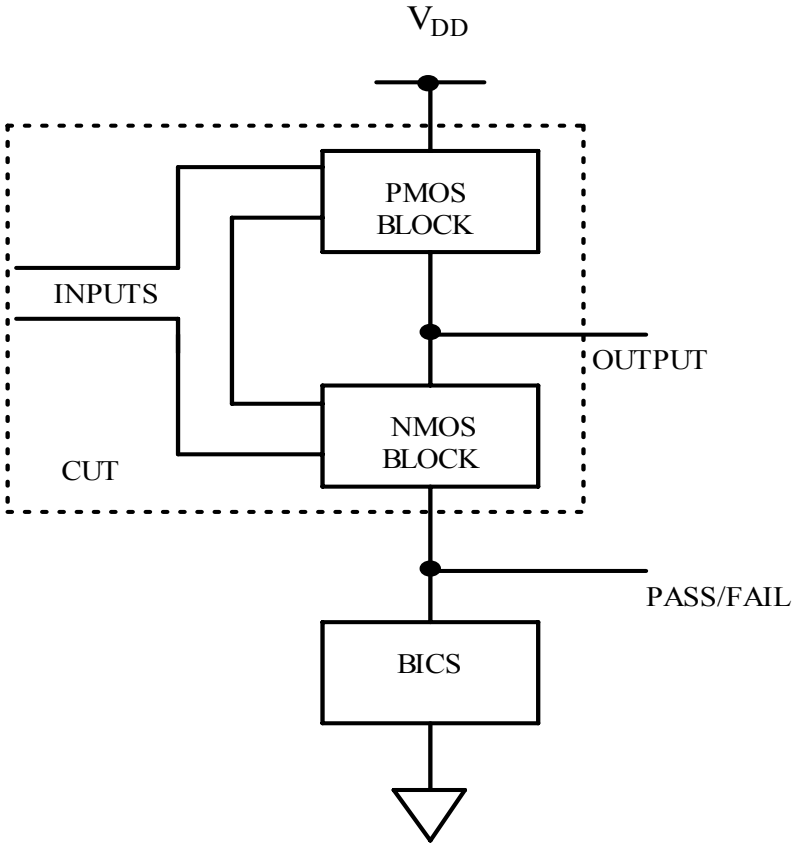


Figure 1.5: Block diagram of I_{DDQ} testing [119].

Digital CMOS ICs have been tested successfully using I_{DDQ} and ΔI_{DDQ} methods for physical defects. Fault equivalence method, initially used in digital testing, has been also applied to analog circuit testing [74-76]. However, testing of analog circuits is still a problem due to variation in design from one specific application to other. The increased leakage current further complicates not only the design but also testing. Mixed-signal circuits are even more difficult to test. A general and efficient solution for testing mixed-signal integrated circuits is still not available.

Functional test approaches applied to analog and mixed-signal integrated circuit is based on empirical development of a test set [77, 78]. This approach needs a reasonably large number of sample circuits for collecting the test data. The approach also does not have any inherent test metric to measure the achievement of a test goal. Design for testability is another widely used method. Oscillation test strategy is based on the design for testability (DFT) technique [79, 80], which gives good fault coverage and does not require any test vectors. However, the method is difficult to apply in complex integrated circuits since it is not usually possible to divide the circuit into the fundamental blocks such as current mirrors, loads, amplifiers and multiplexers. Built-in self-test method (BIST) with on on-chip analog signal generators is used to automatically test offset voltage, linearity, differential linearity error and gain error of data converters [25, 81]. The method does not cover mapping physical defects.

The steady state quiescent current (I_{DDQ}) testing which has been very efficient in testing digital circuits for physical defects has also been applied in testing of analog circuits and data converters [82-85]. Recently Srivastava et al., [86] have implemented a simple BICS for I_{DDQ} testing of CMOS sigma-delta analog-to-digital and charge scaling digital-to-analog converters. The faults simulating physical defects were modeled by MOSFETs as

switches rather using permanent shorts or opens. However, their work is applicable to CMOS mixed-signal ICs where leakage current is significantly lower than the reference quiescent currents. In this work, we use the Keating-Meyer approach [72] for ΔI_{DDQ} testing of CMOS 12-bit ADC and 12-bit DAC designed in standard 0.5 μm n-well CMOS process. In a recent work [87], we have reported testing of 12-bit DAC for shorts simulating manufacturing defects using ΔI_{DDQ} testing with analog output for fault detection. However, it was limited to a limited set of faults and analog encoding for fault detection. The BICS design in present work is very similar to MEAS block of ΔI_{DDQ} monitor of Vazquez and de Gyvez [57, 58] except that the single p-MOSFET switch connecting the power supply (V_{DD}) and the circuit-under-test (CUT) is replaced by two CMOS switches for better isolation from V_{DD}. The BICS uses digital encoding for fault detection. In another recent work, [88], in ΔI_{DDQ} testing, we have considered physical defects such as device shorts and simulated using fault injection transistors as switches combined with fault equivalence. Since ΔI_{DDQ} testing requires use of a large number of input/output pins, we have also applied logic scan-path method in testing digital parts of data converter circuits using fault equivalence combined with fault injection transistors. Similarly analog parts of data converters are tested. ΔI_{DDQ} testing also takes into account effect of process variations on BICS performance.

1.5 Combined Oscillation, Quiescent Current and Transient Current (I_{DDT}) Testing

Test methodologies such as functional test, oscillation based testing and transient current testing can be used along with I_{DDQ} testing to improve its efficiency. Functional test approaches applied to analog and mixed-signal integrated circuit is based on empirical development of a test set [77]. This approach needs a reasonably large number of sample circuits for collecting the test data. The approach also does not have any inherent test metric

to measure the achievement of a test goal. Oscillation test strategy is based on the design for testability (DFT) technique [79], which gives good fault coverage. Oscillation test methodology is a vector less test method for analog and mixed-signal circuits based on rearranging the circuit under test (CUT) as an oscillator. A Design-for-Test (DFT) based oscillation-testing methodology (OTM) [79] suitable for both functional and defect oriented testing, has been successfully applied to CMOS analog circuits [89] such as the analog-to-digital converters, digitally programmable switched-current bi-quadratic filters, active RC filters, and to circuitry used as embedded blocks [80, 90, 91]. In this method, the complex analog circuit is partitioned into functional building blocks such as the amplifier, comparator, filter, voltage reference, etc. or a combination of these blocks. This test methodology has two modes of operation normal mode and test mode, during test mode each of these blocks is converted into a circuit producing sustained oscillation using additional circuitry. A change in the oscillation frequency from its nominal value indicates the possibility of faults in the CUT. OTM is shown to be an effective functional 'go' and 'no-go' test to verify if the circuit under test conforms to the required specifications. The method achieves good fault-coverage removing test vector generation and output evaluation, while reducing test complexity, area overhead, and test cost. However, the method is difficult to apply in complex integrated circuits since it is not usually possible to divide the circuit into the fundamental blocks such as current mirrors, loads, amplifiers and multiplexers.

Transient current testing (I_{DDT}) has been often cited as an alternative and/or testing for I_{DDQ} test. CMOS circuits use very little power when in steady state because there is no ideal path between V_{DD} and V_{SS} of the circuit. Any change in this steady state current is used for fault detection by I_{DDQ} test method. When the CMOS circuit switches a momentary path exists between V_{DD} and V_{SS} of the circuit, which gives rise to I_{DDT} current. I_{DDT} testing offers

all the advantages of I_{DDQ} testing such as no propagation requirement, high fault coverage to vector ratio, etc., I_{DDT} testing offers additional advantages compared to I_{DDQ} like speed as it does not require the internal circuit activity to settle down. However, all I_{DDT} methods necessarily require high speed measurement circuitry with high accuracy. It was observed that I_{DDT} tests are capable of detecting open faults and delay faults [92, 93].

1.6 Noise Modeling Based Testing

This is a test method for detecting faults in CMOS analog integrated circuits based on noise modeling of the MOSFET. The faults in circuit under test (CUT) are detected by observing the variation in noise at the output of CUT. The noise at the output is sum of noise contributed from each component in the circuit. The noise in each MOSFET is represented by an equivalent voltage generator as the noise in each MOSFET is independent of each other [94]. When a fault is introduced, the noise at the output deviates from the fault free condition of the CUT. A fault is said to be detected if it causes the output noise to deviate significantly from fault free condition. In the present work, we have used a CMOS op-amp as a CUT for the noise based testing [95].

1.7 Fault Injection Transistors

In literature, resistors were used to model open and short faults [96]. Short faults are modeled by a small resistor (~ 100 Ω) and open faults are modeled by a very high resistance (~ 10 MΩ). The disadvantage with this method is that we need two circuits to study the behavior of the circuit with and without faults. To over come this defect, fault injection transistors (FITs) have been proposed [86, 97]. Figure 1.6 shows a fault-injection transistor. To create an internal bridging fault, the fault injection transistor is connected to opposite potentials. When the gate of fault-injection transistor (M_E) is connected to V_{DD}, a low resistance path is created between its drain and source nodes and a path from V_{DD} to GND is

formed. In Figure 1.7, an internal bridging fault is created in the CMOS inverter between the drain and source nodes using the fault injection transistor. Logic '0' is applied at the input of the inverter. Therefore, the output of the inverter is at logic '1' or V_{DD}. When the logic '1' is applied to the gate (V_E) of the n-MOS fault-injection transistor (M_E), it turns on. This causes a low resistance path between the output of the inverter and the V_{SS}. This gives rise to an excessive I_{DDQ} as a path from V_{DD} to GND is created, which can be detected by the BICS. In this work, fault-injection transistors have been used in testing of CMOS data converters.

1.8 Scope of Research

In Chapter 2, we present a difference in quiescent current (ΔI_{DDQ}) testing of 12-bit recycling architecture based CMOS analog-to-digital data converter circuit designed in submicron CMOS process. The built-in current sensor (BICS) follows the method of capacitive voltage discharge across the circuit under test. The faults simulating manufacturing defects such as the shorts in MOSFETs are injected using fault injection transistors with resistors in series combined with fault equivalence in 12-bit ADC designed in 0.5 μm n-well CMOS process for 2.5 V operations. The logic scan-path method is also used for digital CMOS part of data converters testing in combination with the ΔI_{DDQ} testing for introducing a large number of faults. The experimentally observed results of the fabricated devices are compared with simulations from SPICE.

In Chapter 3, we present ΔI_{DDQ} testing of a 12-bit digital-to-analog converter (DAC) chip designed in 0.5 μm n-well CMOS process. The built-in-current sensor (BICS) uses frequency as the output for fault detection in circuit under test (CUT). A fault is detected if it causes the output frequency to deviate more than ±10% from the reference frequency. The experimentally observed results of the fabricated devices are compared with simulations from SPICE.

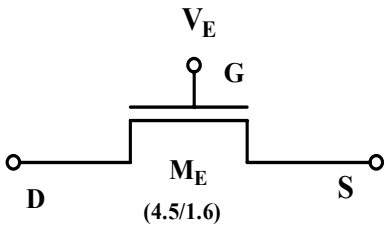


Figure 1.6 : Fault-injection transistor (FIT).

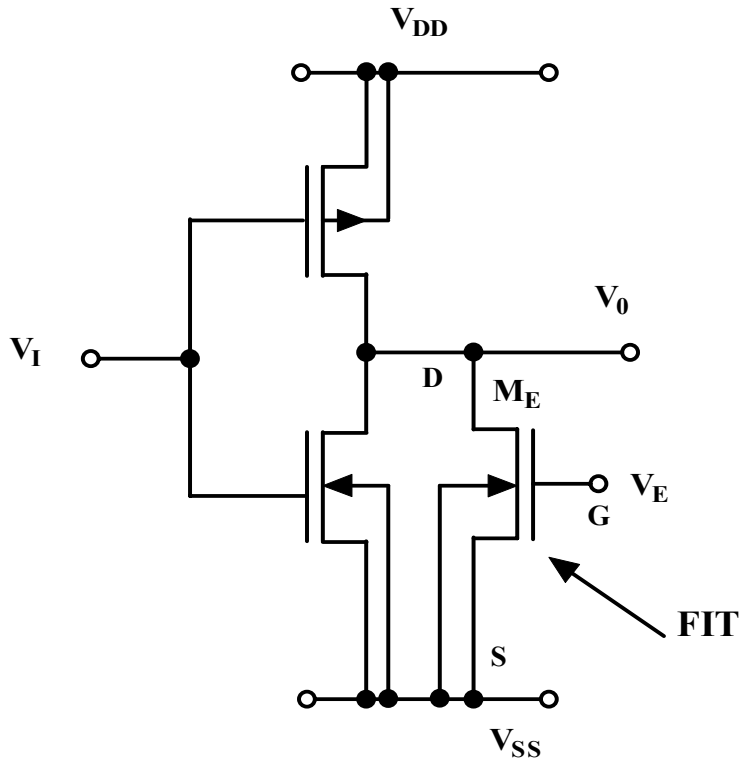


Figure 1.7 : Fault-injection transistor between drain and source nodes of a CMOS inverter.

In Chapter 4, we present a simple test methodology combining oscillation and quiescent power supply current (I_{DDQ}) testing for detecting bridging and open faults in a CMOS amplifier circuit designed for operation at $\pm$ 2.5 V in 1.5 μm n-well CMOS process. The testing is performed at room temperature (300 K) and also at liquid-nitrogen temperature (77 K) to enhance fault detection. An on-chip built-in current sensor (BICS) has been integrated to monitor I_{DDQ} of the circuit under test (CUT). It is shown that all faults can be detected through a combined oscillation and I_{DDQ} testing method. Theoretical results obtained from SPICE simulations are compared with the corresponding experimental results on fabricated devices.

The above test methodology was also extended to include transient power supply current testing. The combined test methodology including oscillation, quiescent current and transient current testing has been used for fault detection in an other op-amp with floating gate input transistors designed for operation at $\pm$ 2.5 V in 1.5 μm n-well CMOS process.

In Chapter 5, we provide a summary of the work presented and scope for future work.

Three appendices are provided which are as follows. Appendix A describes the noise based testing of a CMOS amplifier and simulation results from SPICE are provided for detecting injected faults. The MOS model parameters used for designing the circuit under test for implementing I_{DDQ}, power supply and oscillation testing are given in Appendix B. The MOS model parameters used for designing the circuit under test for implementing ΔI_{DDQ} testing is given in Appendix C. The list of publications related to the work presented is given in Appendix D.

CHAPTER 2[‡]

ΔI_{DDQ} TESTING OF CMOS ANALOG-TO-DIGITAL CONVERTER

2.1 Introduction

This chapter presents a difference in quiescent current (ΔI_{DDQ}) testing of CMOS data converter circuits designed in submicron CMOS process. The built-in current sensor (BICS) follows the method of capacitive voltage discharge across the circuit under test. The faults simulating manufacturing defects such as shorts in MOSFETs are injected using fault injection transistors with resistors in series combined with fault equivalence in 12-bit ADC and 12-bit DAC designed in 0.5 μm n-well CMOS process for 2.5 V operations. The logic scan-path method is also used for digital CMOS part of data converters testing in combination with the ΔI_{DDQ} testing for introducing a large number of faults. The combined methods have allowed testing 520 introduced faults in 12-bit ADC, 60 faults in 12-bit DAC with at least 90% fault coverage from post-layout simulation experiments. ADC and DAC fabricated designs were also tested experimentally for a small sub-set of five injected faults using fault injection transistors due to die size and input/output pin limitations. ΔI_{DDQ} test method has taken into consideration effects of process variations through process transconductance and threshold voltage parameters of the MOSFET.

In Section 2.2, a description of BICS and principle of ΔI_{DDQ} method is presented. ADC and DAC design descriptions are presented in Section 2.3. Post-layout simulation experiments over a large number of introduced faults, and experimental results on fabricated

---

[‡] Part of the work is reported in following publications:

1. S. Yellampalli and A. Srivastava, "ΔI_{DDQ} testing of CMOS data converters," *Journal of Active and Passive Electronic Devices,* 2008 (Accepted).

2. S. Yellampalli and A. Srivastava, "ΔI_{DDQ} testing of a 12-bit recycling architecture based ADC," *Proceeding of IEEE Region 5 Technical Conference*, pp. 370 - 373, 2007.

designs with injection of a small sub-set of simulated faults are presented in Section 2.4 followed by conclusion in Section 2.5.

2.2 ΔI_{DDQ} BICS Design

Figure 2.1 shows the circuit diagram of the BICS which is slightly modified from the MEAS block of ΔI_{DDQ} monitor described in [57, 58] where a p-MOSFET switch has been replaced by two transmission gates TG1 and TG2 as switches for better isolation of node X from V_{DD}. Unlike p-MOSFET as a switch, there is no signal degradation from a CMOS transmission gate as a switch. Unlike the BICS design in [57, 58] wherein the capacitor is off-chip, in this work, the capacitor is integrated with the BICS for better testability. The output of the switch TG2 is given to a comparator. Its pulse output is fed to a 4-bit binary counter whose output is a function of the input pulse width which is the output of the comparator. The purpose of the use of two transmission gates as switches is to isolate CUT from the BICS when it is powered by V_{DD} and disconnect from V_{DD} when the on-chip capacitor, C (500 fF) is being discharged. The switches are turned-on by a short pulse, V_{TG} of 100 μs duration and 1 μs pulse width. The block diagram of the circuit-under test (CUT) is included in Figure 2.1 for describing operation of the BICS. When TG1 is turned-on, and TG2 is turned-off, the capacitor, C is fully charged to V_{DD} and CUT is powered by the supply voltage, V_{DD}. During the same period, when TG1 is turned-off and TG2 is turned-on, the CUT is disconnected from V_{DD} and the capacitor, C is allowed to discharge to a set reference voltage, V_{REF} (1V).

The discharging voltage across the capacitor, C is compared with V_{REF} through a comparator. The 4-bit binary counter then records the final number of count at the end of the

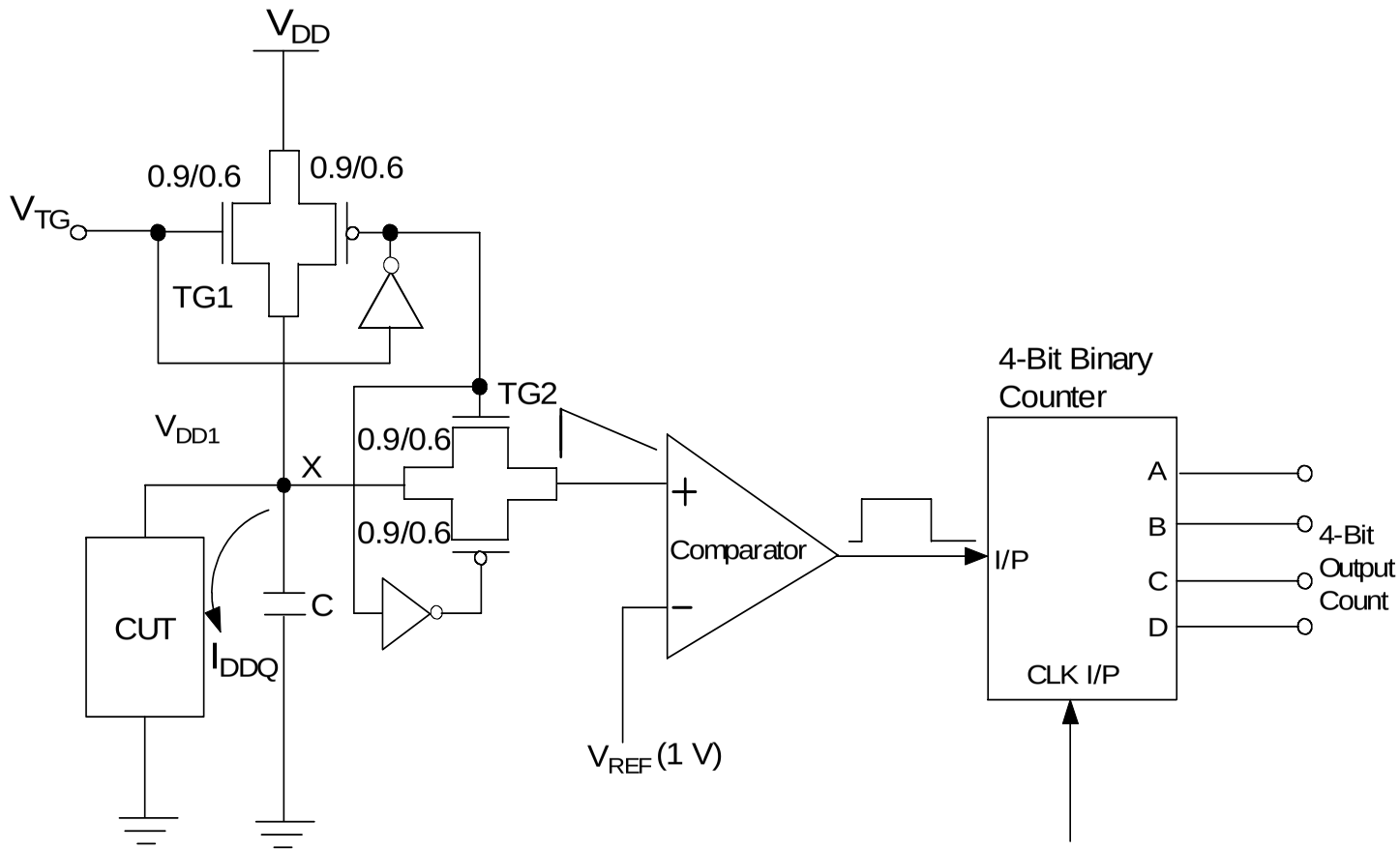


Figure 2.1 : ΔI_{DDQ} built-in current sensor (BICS).

pulse width of the input pulse which is taken as a reference count. When a fault is injected in to CUT, capacitor discharging time changes and results in change of width of the pulse at the output of comparator. With the result a new count is obtained from the counter which is then compared with the reference count thereby signaling the existence or non-existence of the fault. Figure 2.2 shows the discharging of the capacitor under the fault-free (reference) and faulty conditions [57, 58]. The solid and dotted lines in Figure 2.2 corresponds to the capacitive voltage discharge for fault free and faulty conditions, respectively. The discharging quiescent current is given by

$$I_{DDQ} = C\frac{\Delta V}{\Delta t}, \tag{2.1}$$

where $\Delta V = V_{DD} - V_{REF}$. The time, Δt, which takes the capacitive discharging voltage to reach a V_{REF} is measured in number of counts (m) during the clock frequency, T_{CK}. By replacing Δt by mT_{CK}, where $T_{CK} = 1/f_{CK}$, f_{CK} being the clock frequency, we obtain from Eq. (2.1),

$$m = \frac{C}{I_{DDQ}}\Delta V f_{ck} \ . \tag{2.2}$$

In Eq. (2.2), the count value 'm' of the binary counter is inversely proportional to I_{DDQ} and directly proportional to $C, \Delta V$ and f_{ck}. An important observation emerges from Eq. (2.2); for reduced values of the I_{DDQ}, the discharge time increases resulting in increased count values.

2.3 12-Bit ADC Design

ADC design uses a two-step recycling architecture [98]. This particular architecture has been selected for relatively low power dissipation and occupying small area on a chip compared to other architectures. Figure 2.3 shows the schematic block diagram of the ADC which can be used either as a high speed 6-bit ADC or high resolution 12-bit ADC depending

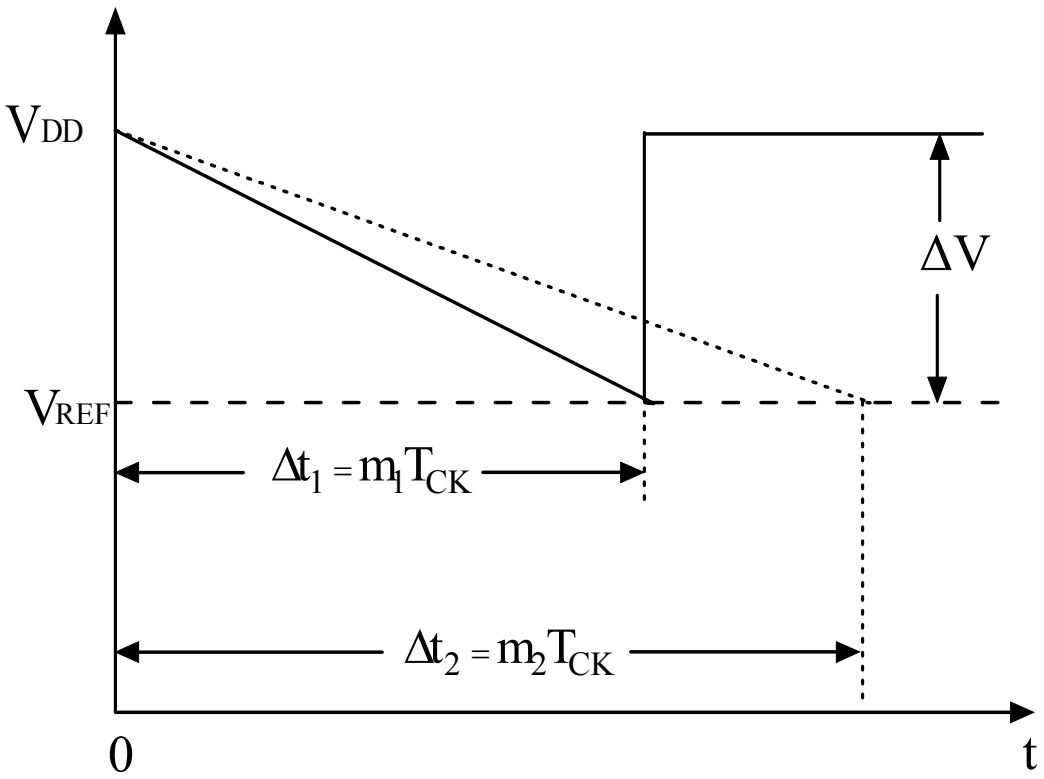


Figure 2.2: Capacitor discharge transient voltage of the CUT [57, 58] under fault free and faulty conditions. Solid line: fault free condition, dotted line: faulty condition.

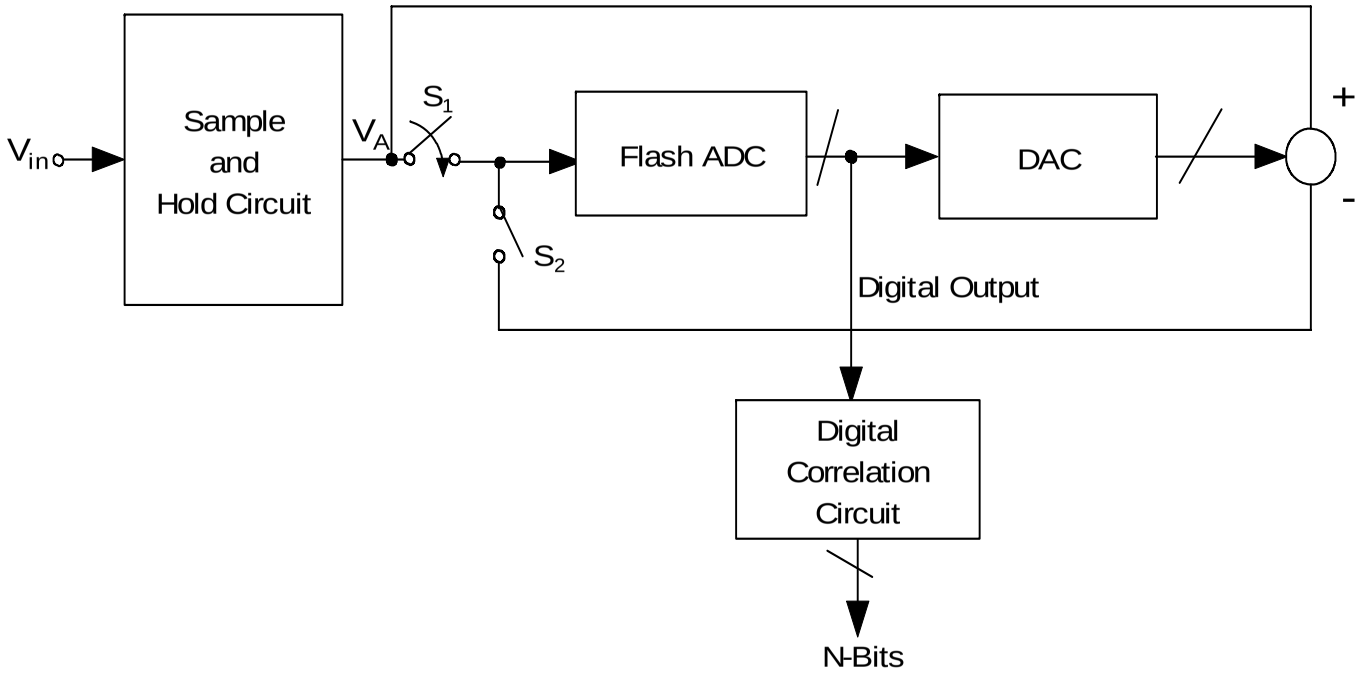


Figure 2.3: Schematic block diagram of a two-step recycling analog-to-digital converter (ADC) [98].

on the requirement and application. When used as a 12-bit ADC, it requires three clock cycles to complete one conversion. The three clock cycles are for sampling, coarse decision and fine decision. In the first clock cycle, the sample and hold circuit samples the input and gives the voltage, V_A. In the second clock cycle, the voltage V_A is quantized into coarse N digital bits through ADC. These N bits are stored in the digital correlation circuit. DAC then converts this output into an analog voltage and subtracted from V_A by the subtractor at the output. During first and second clock cycles when this conversion takes place, the switch, S_1 is closed and the second switch, S_2 remained open. In the third clock cycle, fine conversion takes place. The switch, S_1 is opened and switch, S_2 is closed, thereby isolating ADC and DAC from the sample and hold circuit. It forms a feedback connection between the subtractor output and input of flash ADC the output of which is quantized into fine N digital bits.

The 12-bit recycling architecture ADC has been designed such that it has 6 coarse bits and 6 fine bits. The 6-bit ADC design uses the pipelined architecture wherein 3-bit ADC design uses the flash architecture as a compromise over the speed and space. Figure 2.4 shows the architecture of the 12-bit recycling ADC. Insert in Figure 2.4 shows the i^{th} stage of a 3-bit per stage of the ADC. In Figure 2.4, the input, $V_{i-1,}$ is sampled and held followed by a 3-bit ADC-DAC operation. The output of the 3-bit ADC is the converted bits for the stage. The output of the 3-bit DAC is subtracted from the input forming a residual voltage and is available for the next stage.

Figure 2.5 shows the schematic of the sample-and-hold circuit used in ADC design. It consists of a transmission gate switch (TG-switch), a storage capacitor, C_H and a unity gain buffer. The operation mechanism is as follows. The TG-switch is operated by the $V_{CONTROL}$ signal and is closed during the *sample* interval and opened during *hold*. During *sample*, the

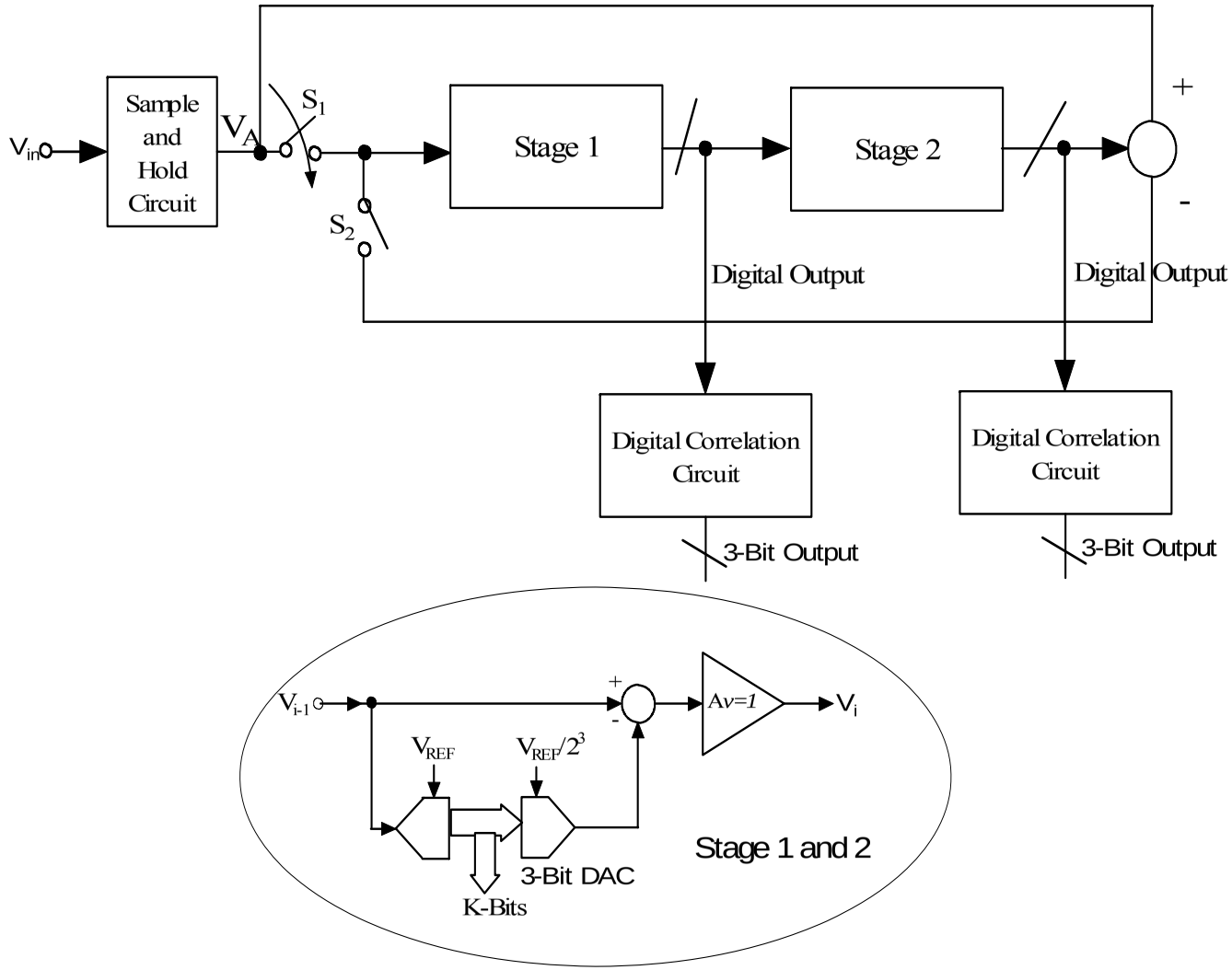


Figure 2.4 : Schematic of 12-bit recycling ADC. Insert shows the i^{th} stage of a K-bit per stage pipeline ADC.

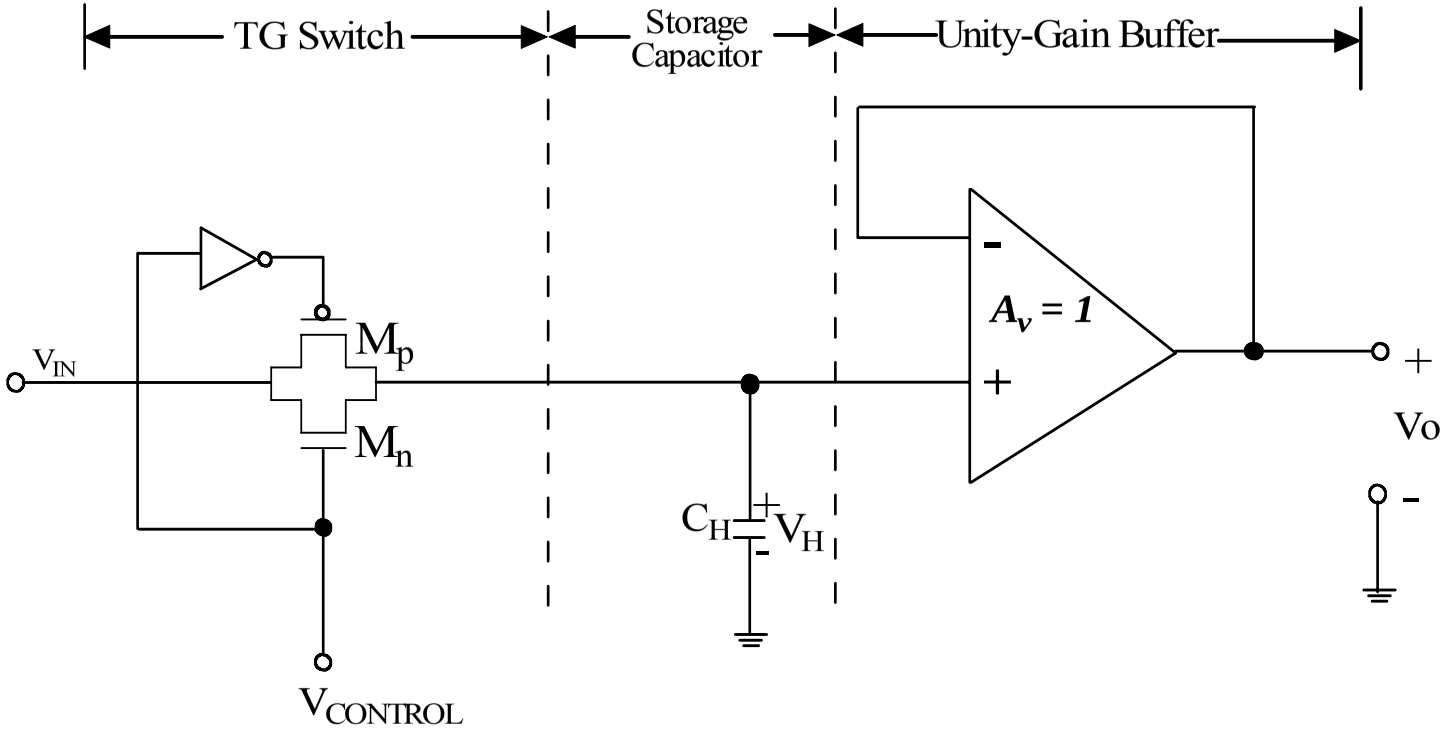


Figure 2.5 : Schematic of the sample-and-hold circuit.

circuit is connected to promote rapid charging of the storage capacitor, C_H and during *hold*, the capacitor; C_H is disconnected from its charging source and ideally retains its charge. The capacitor is connected to a unity gain buffer whose output follows the charge held by the storage capacitor. The unity gain buffer is used at the output to avoid the large overshoot, which might occur, on the output when the input changes rapidly. In the present design, C_H is 1.2 pF. Operational amplifier which is also used as a unity gain amplifier is an essential part of both ADC and DAC designs. Its design is presented in [87] and following Chapter 3.

Figure 2.6 shows a 3-bit flash (parallel) ADC [98, 99] where the reference voltage, V_{REF} is divided into eight values using the resistors as shown. Each of these resistor values is applied to the negative terminal of a comparator. The outputs of the comparators are taken to a digital encoding network that determines the digital word from the comparator outputs. The flash ADC converts the analog signal to a digital word in one clock cycle that has two phase periods. During the first phase period, the analog input voltage is sampled and applied to the comparator inputs. During the second phase period, the digital encoding network determines the correct output digital word. The performance of the flash ADC depends on the ability to sample the input without jitter. The jitter can be controlled in flash ADC by using either sample and hold circuit at the input or clocked comparators. The comparators should be clocked simultaneously to avoid jitter. However, it reduces the resolution at high speeds. Therefore, we used sample and hold circuit to decrease the jitter. Furthermore, the value of the last resistor in the string is adjusted to 0.5R and the value of the MSB resistor closest to the reference voltage is 1.5R. The quantization error is centered around 0 LSB. In this design R is 1 kΩ.

Figure 2.7 shows the CMOS circuit diagram of a comparator used in 3-bit ADC design of Figure 2.6. Transistors M_1, M_2 constitute the n-channel differential stage with M_3,

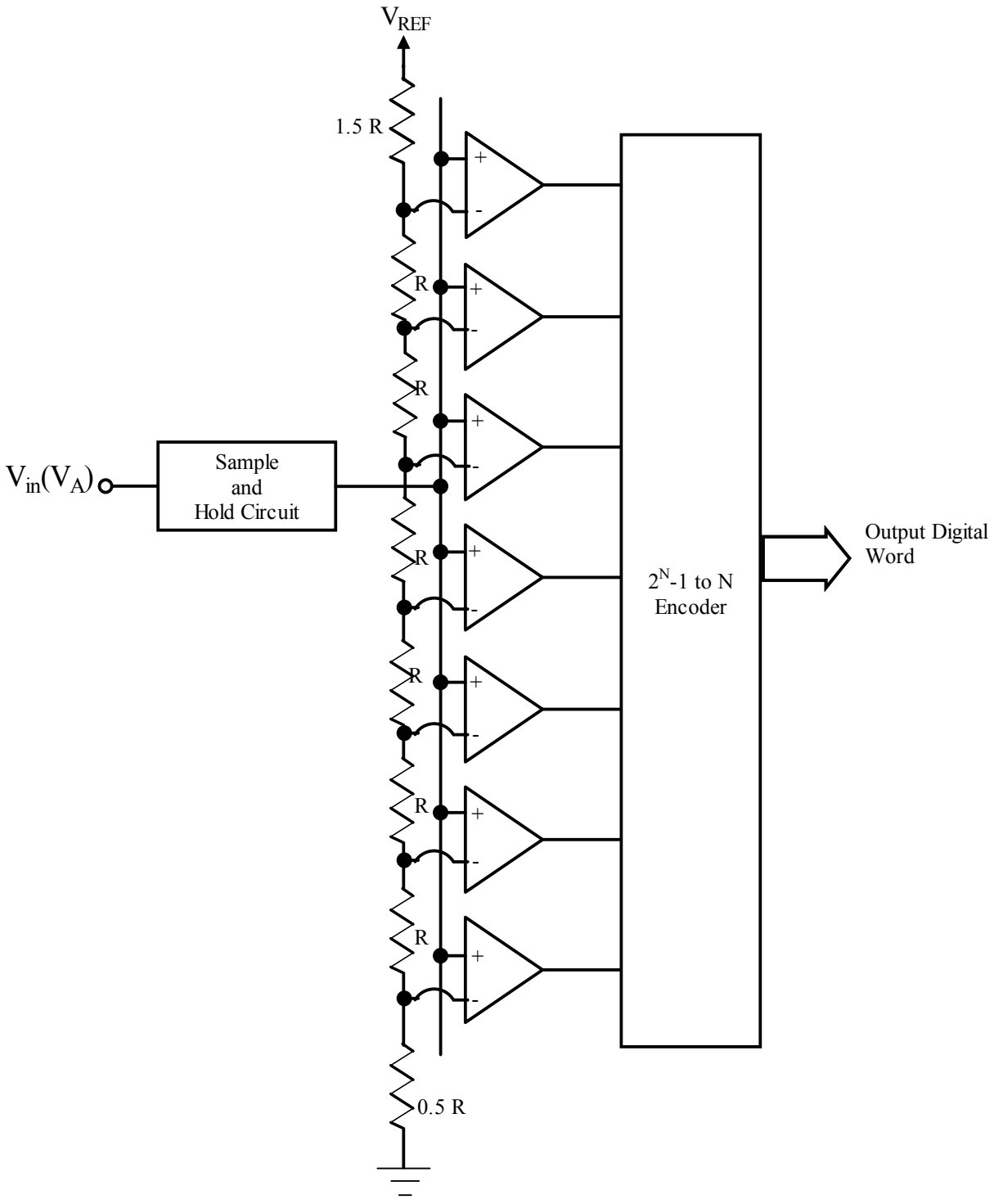


Figure 2.6: Schematic of 3-bit flash ADC [98, 99].

M4 as current source loads. Transistors M_5, M_6 and M_7 constitute the double ended to single ended conversion stage. Transistors M_8-M_9, M_{10}-M_{11}, M_{12}- M_{13} constitute three inverters which act as buffer for the output stage. The same comparator design has been also used in design of BICS of Figure 2.1.

Figure 2.8 shows the schematics of the 3-bit charge scaling DAC [100]. The reference voltage is 2.0 V. The least significant change in the output value is given by,

$$\text{LSB} = \frac{2}{8} = 0.25 \text{ mV}. \tag{2.3}$$

In physical layout, capacitors used for charge scaling DAC are connected in a centroid formation to overcome the gradient during fabrication.

The DAC converts a 3-bit digital input word to a respective analog signal by scaling a voltage reference. The various blocks in DAC include a voltage reference, binary switches, a scaling network, an operational amplifier and a sample and hold circuit. The multiplexer circuit connected to the other end of each capacitor selects the voltage which is either V_{REF} or 'GND' to which the capacitor is charged depending upon the control signal 'V_S'. Initially, the control signal for all multiplexer switches is set to LOW before giving any specified input so that GND is supplied to the capacitor network to reset. Then the capacitor network is supplied with the digital word by switching the particular multiplexer switch for each bit to the desired value of either V_{REF} for "1" or GND for "0". The capacitors whose ends are connected to V_{REF} are charged to +2 V and those, which are connected to GND are charged to 0 V. Since the capacitor network is connected in parallel, the equivalent voltage is calculated by,

$$V_{OUT} = (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \ldots\ldots + B_N 2^N) V_{REF}. \tag{2.4}$$

The capacitor at the end of the network is used as a 'terminating capacitor'. Depending on

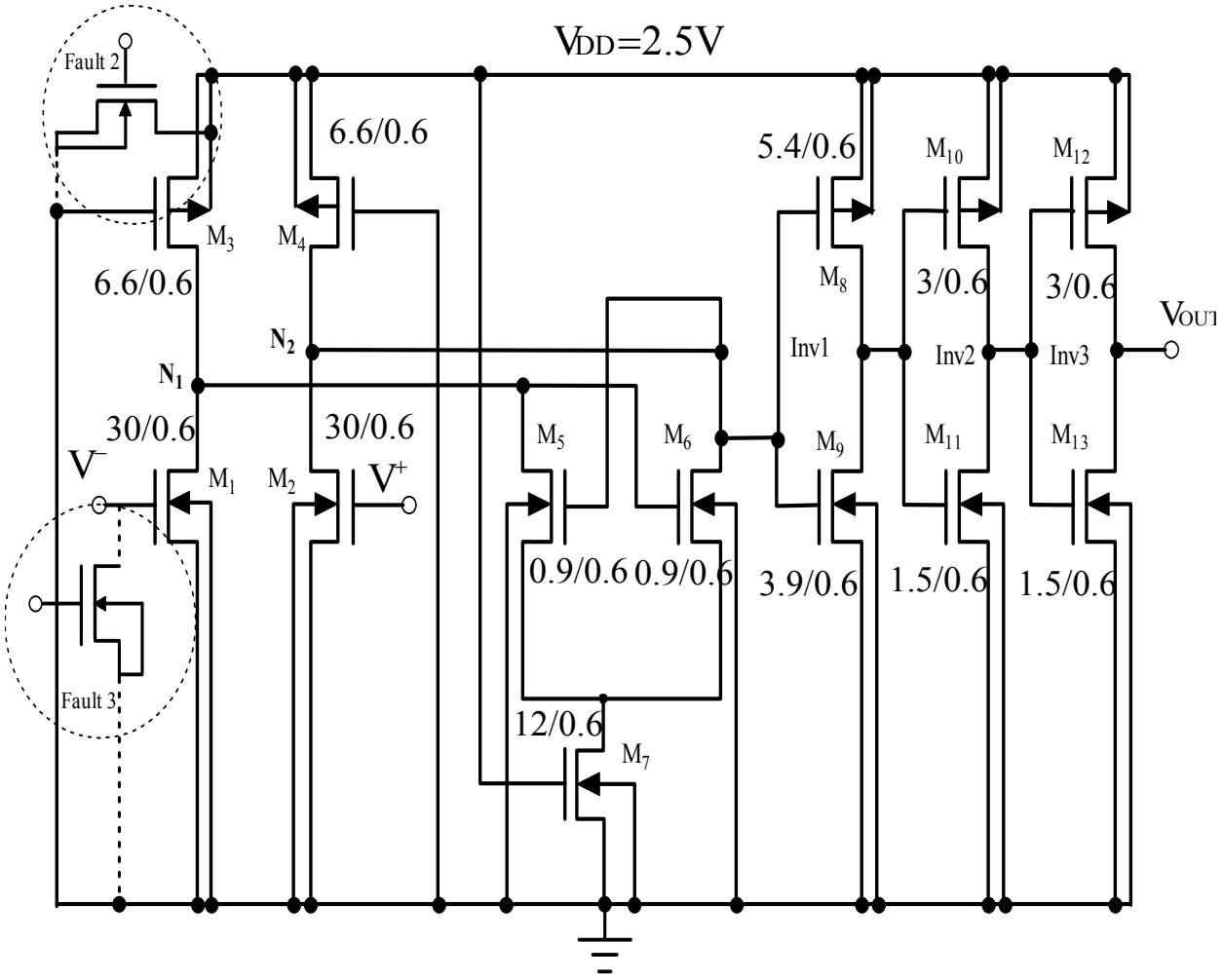


Figure 2.7: Circuit diagram of a comparator used in 3-bit ADC design of Fig. 2.6. Note: Fault injection transistors are shown by dotted line connections.

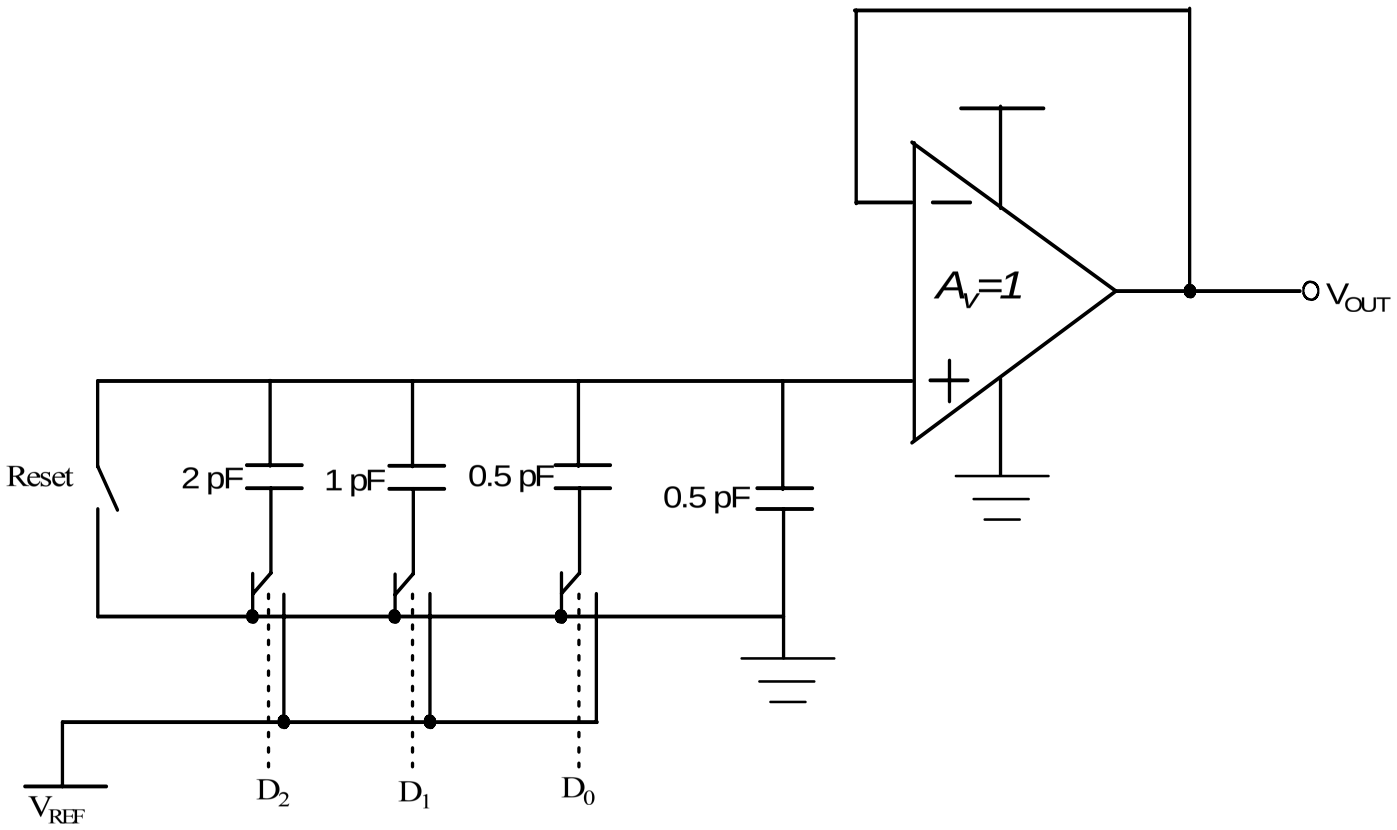


Figure 2.8 : Schematics of the 3-bit charge scaling digital-to-analog converter (DAC) [100].

the capacitors, which are charged to different voltages based on the input digital word, the effective resultant analog voltage is calculated for the respective digital combination. The 12-bit DAC uses the same architecture. More insight into 12-bit DAC design can be found in [87] and in Chapter 3.

A parallel-in parallel-out 3-bit register is used as a digital correlation circuit. After the coarse cycle, all digital outputs are stored in this till the fine cycle is completed. Final 12 bits are available at the output after the end of fine cycle.

2.4 Results and Discussion

Figure 2.9 shows the chip layout of 12-bit ADC designed for operation at 2.5 V in 0.5 μm n-well CMOS process with a small sub-set of five faults introduced using fault injection transistors (FITs) as switches[86, 97]. Figure 2.10 shows the layout of 12-bit ADC in 40-pin padframe. The design integrates an on-chip BICS of Figure 2.1 for ΔI_{DDQ} testing for physical defects such as shorts in MOSFETs. The ADC occupies 890 × 712 μm^2 area of the chip. The BICS occupies 498 × 75 μm^2 area of the chip. Figure 2.11 shows the microphotograph of the fabricated 12-bit ADC-BICS chip. Figure 2.12 shows the simulated and experimentally measured output characteristics of the 12-bit ADC with INL within ±1LSB and DNL within ±1LSB. ADC was tested with a 2.5 V 100 KHz sinusoidal wave function. The fault injection transistors are activated externally by connecting their gates directly to signals of amplitude, V_{DD}. The W/L ratio of the FIT in the present design is 1.05 μm/0.6 μm. When an error signal of amplitude, V_{DD} is applied to a fault injection transistor, it creates a short between two bridging nodes. In post-layout simulation experiments, defects are simulated using fault injection transistors in series with a resistor of value determined by the resistance of the faulty transistor. The resistance varies in 1-60 KΩ range. Figure 2.13 shows the logic scan-path method of testing as applied in digital correlation part of the ADC. It consists of a 3-bit

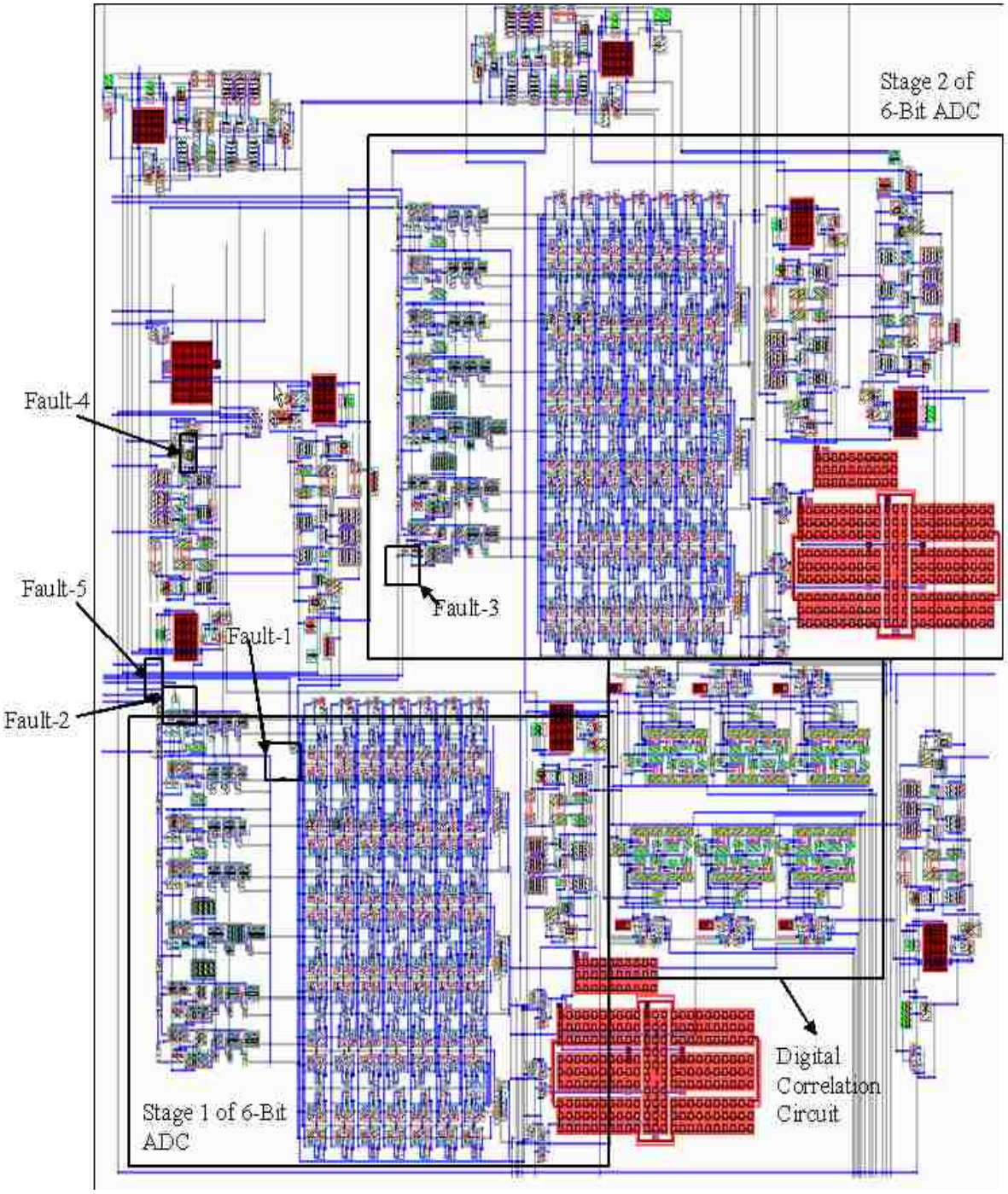


Figure 2.9: Chip layout of 12-bit ADC-BICS.

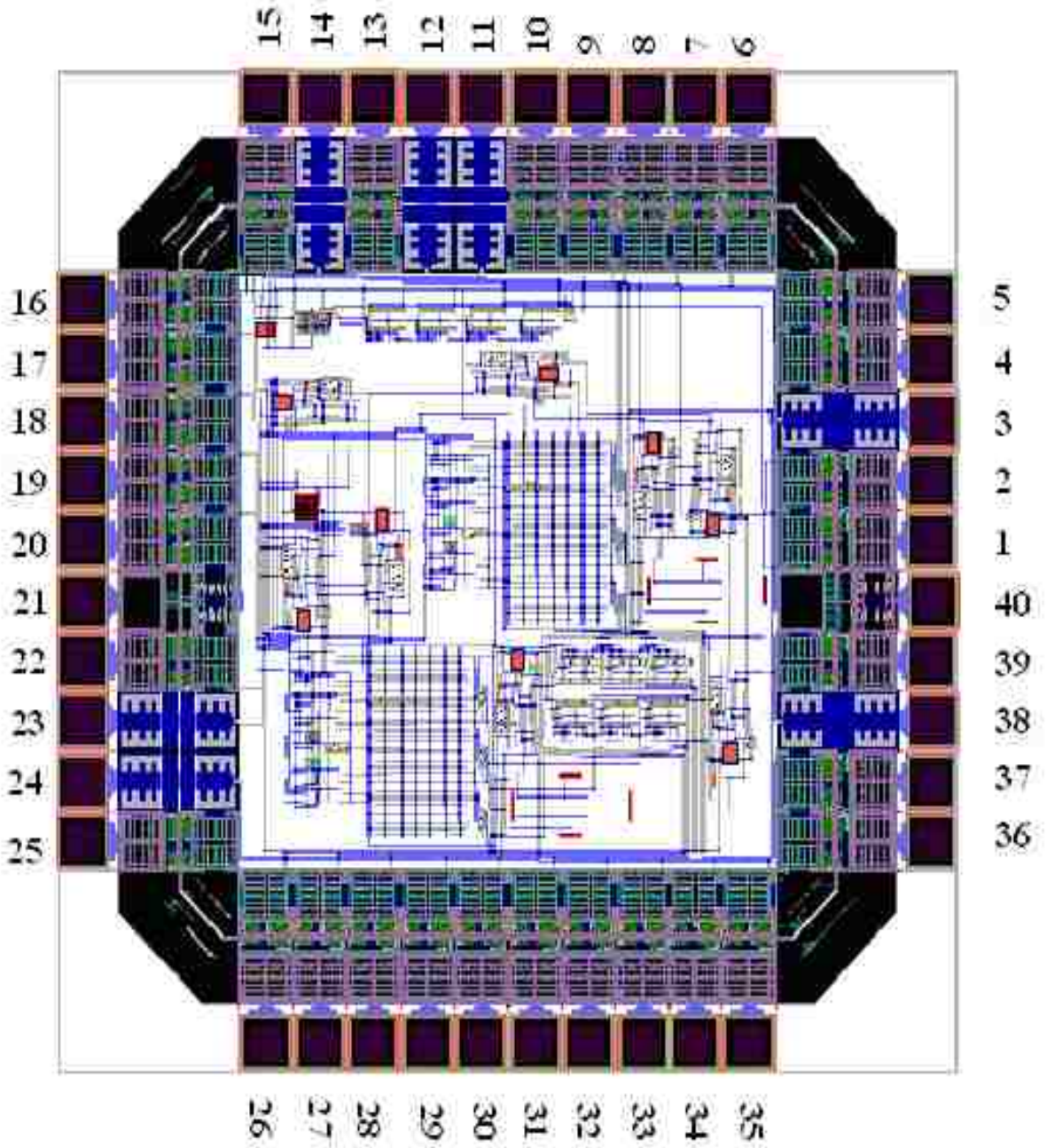


Figure 2.10: Chip layout of 12-bit ADC-BICS in 40-pin padframe.

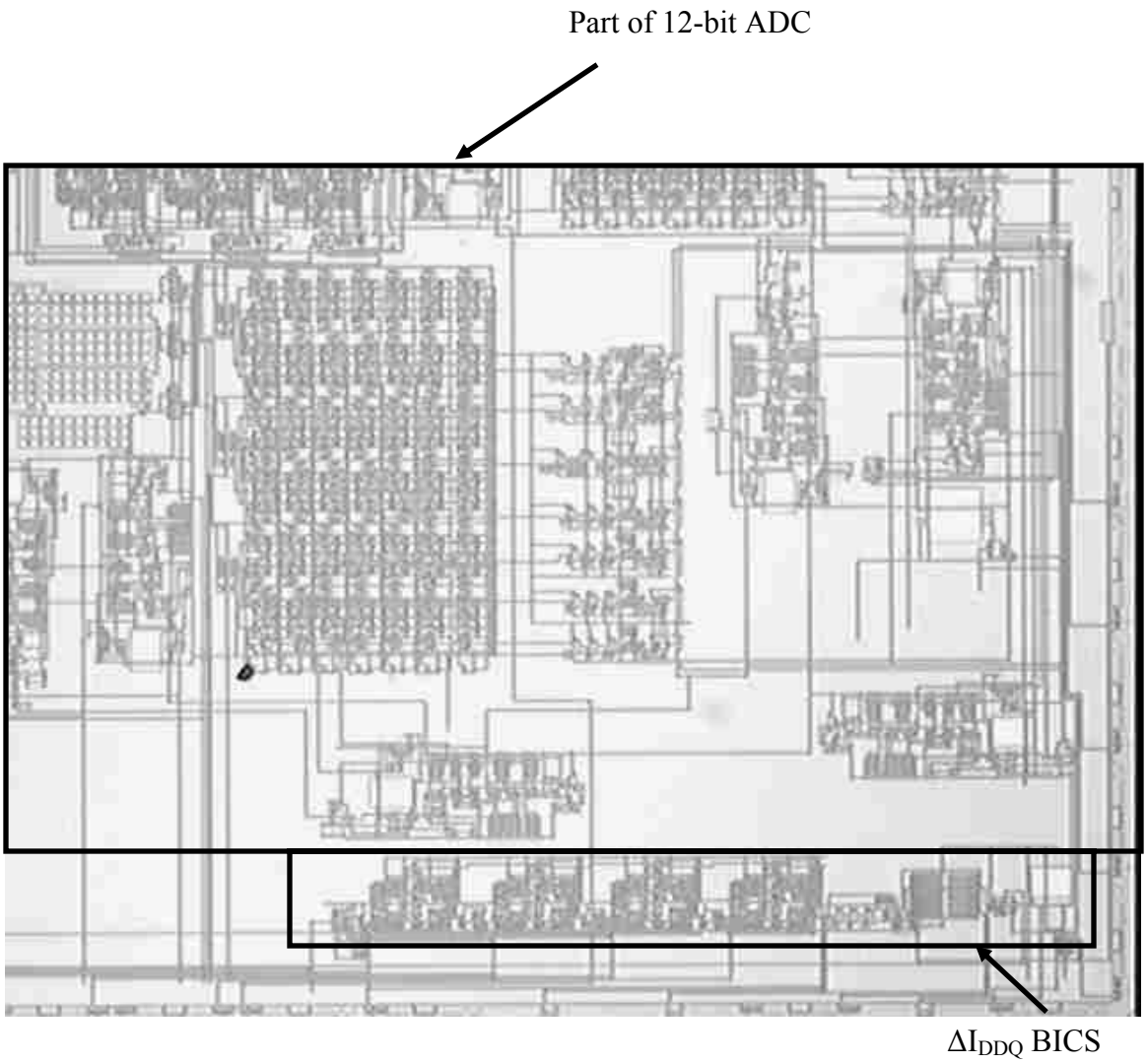


Figure 2.11: Microphotograph of the fabricated 12-bit ADC-BICS chip.

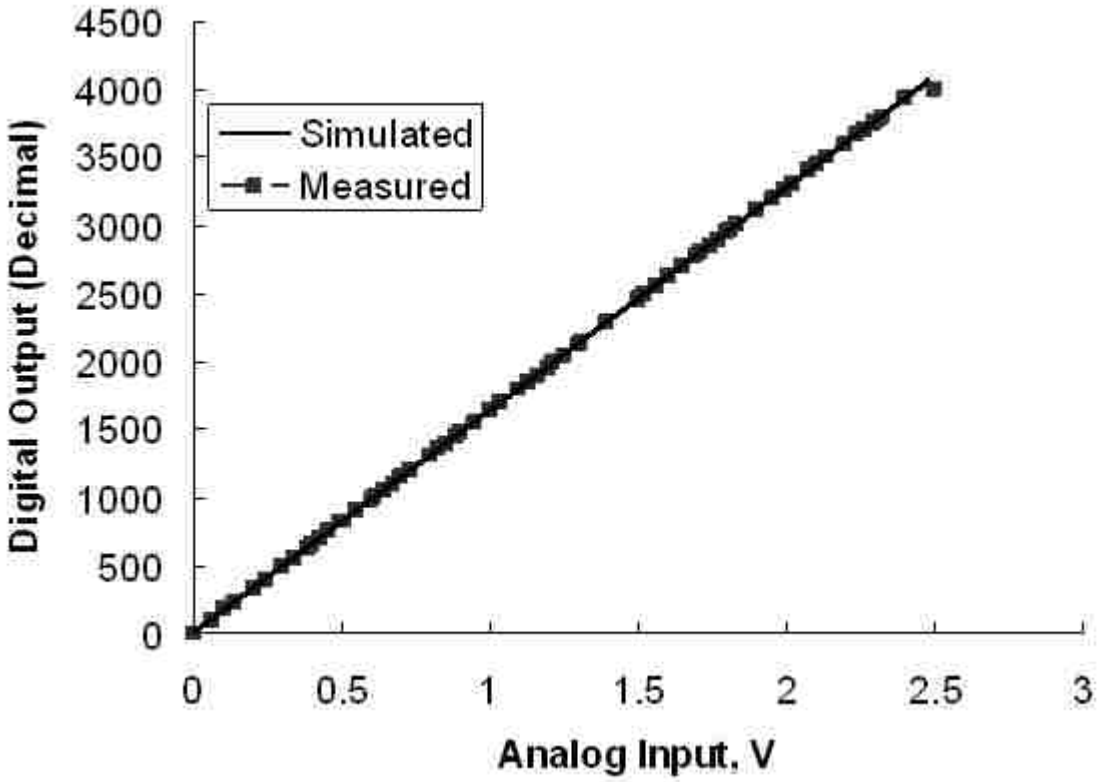


Figure 2.12: Simulated and experimentally measured output characteristics of the 12-bit ADC.

parallel-in and parallel-out registers. The scan-path test has normal and test modes of operation. The normal test mode bypasses the scan-path test by disabling ("0") Scan-Path_IN and Scan-Path_Mode Control signals. In test mode, registers are isolated from ADC inputs V_1, V_2 and V_3 and are connected in series by enabling ("1") Scan-Path_IN and Scan-Path_Mode Control signals. The fault is identified if the Scan-Path_OUT changes from "1" to "0". Using fault equivalence, gates in digital correlation circuit are converted into single-port networks as shown in Figure 2.14 (a) which is then combined with the fault injection transistors in series with resistors (FIT in series with a resistor) for testing. This method is also applied in testing of analog parts of ADC – amplifier and comparator as shown in Figure 2.14 (b) thereby allowing coverage of a large number of faults with reduced input/output pins.

A major part of testing in the present work is focused on post-layout simulation experiments due to die size limitation and availability of number of input/output pins. In the circuit layout of Figure 2.9 of ADC, 520 short and bridging faults were introduced. The fault distribution is as follows. One hundred forty eight shorts including their multiple combinations were introduced in digital correlation circuits consisting of six registers and tested independently by both the scan-path and ΔI_{DDQ} methods. In ΔI_{DDQ} testing, effect of process variations on BICS operation is considered by introducing ±5% variation in process transconductance parameter (k) and threshold voltage (V_{th}) of I_D-V_{DS} characteristics of the MOSFET. A range of discharge time for 12-bit ADC was identified which is 14.15 – 15.75 μs and the fault is identified if the discharge time is beyond this range. Both methods individually tested positively for all 148 introduced faults. In addition, three hundred seventy two short faults and their multiple combinations were introduced in amplifier and comparator of ADC and tested with ΔI_{DDQ} method. A total of 340 faults were tested positively and 32

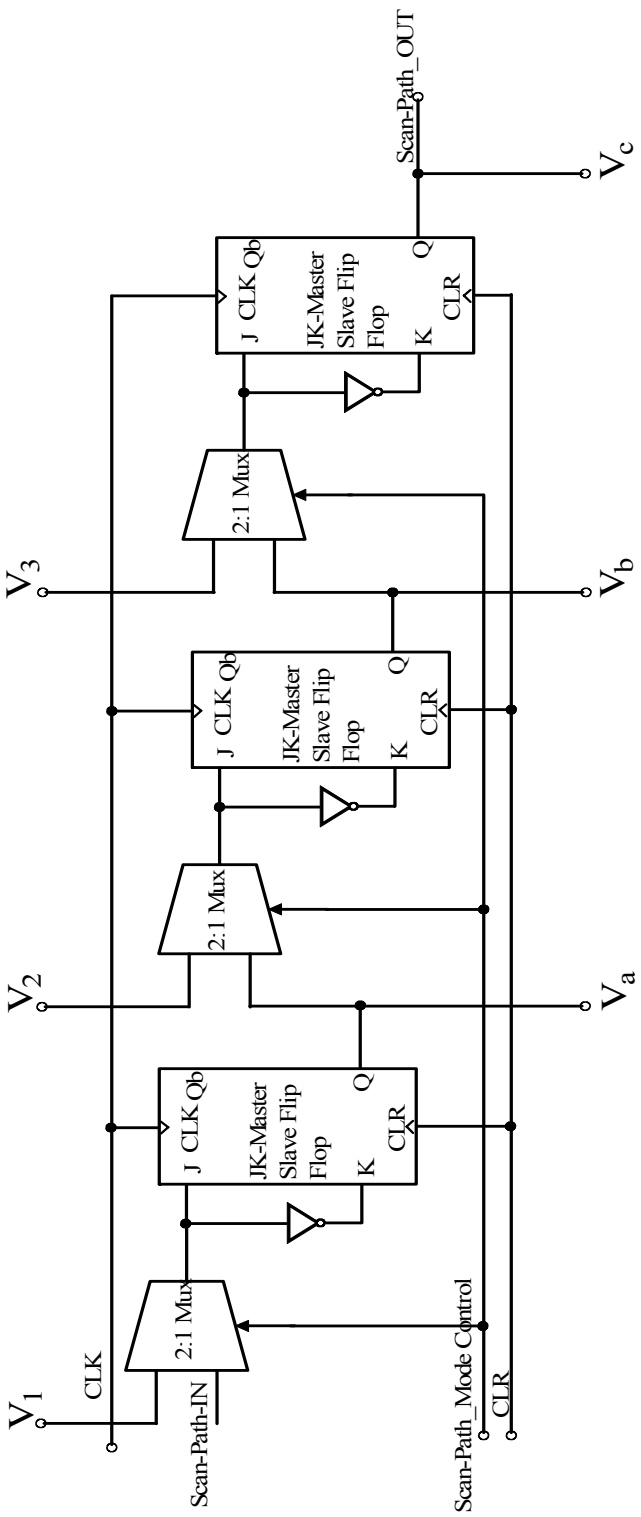
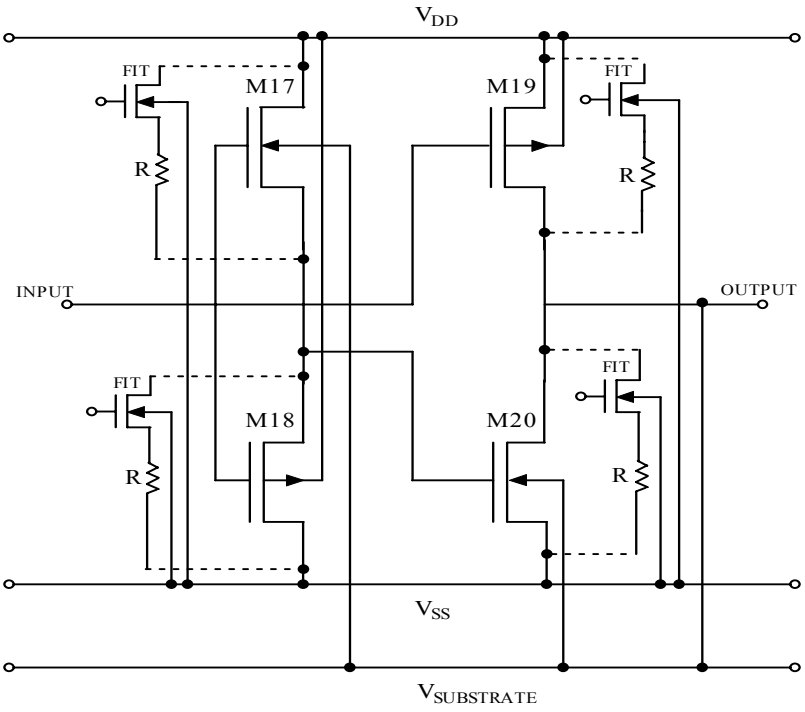
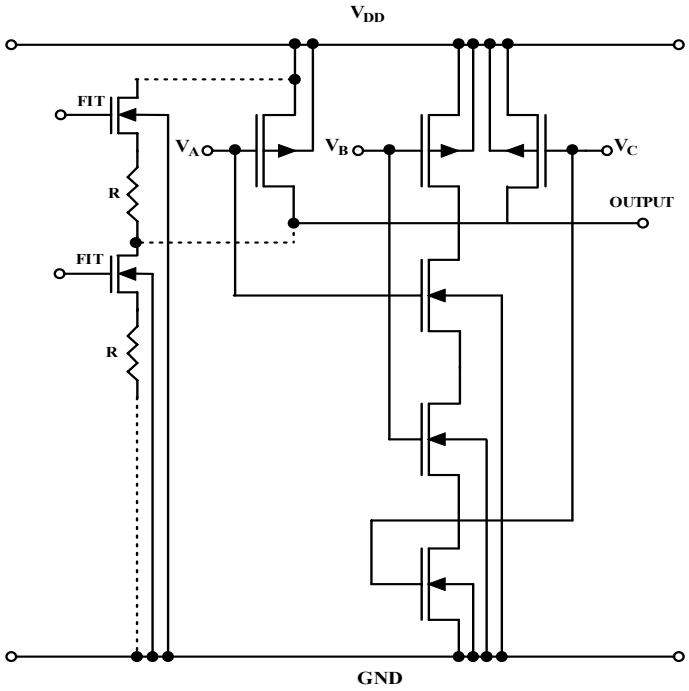


Figure 2.13 : Logic scan-path method of testing as applied to CMOS data converters.



(a)



(b)

Figure 2.14: Fault equivalence using one-port network: (a) CMOS digital circuits (3-input NAND gate) and (b) CMOS analog circuits.

faults could not be tested. Thus, overall the fault coverage is about 94%.

Apart from post-layout simulation experiments, 12-bit ADC was also tested experimentally from ΔI_{DDQ} method by injecting a small sub-set of five faults using fault injection transistors spread around different parts of chips and taking into consideration effects of process variations. In Figure 2.9 and the fabricated chip shown in Figure 2.11, the Fault-1 simulates a physical short between drain and substrate of one of the transistors of encoder circuit of Figure 2.9, Fault-2 simulates a physical short between gate and substrate of the transistor (M_3) of the circuit of Figure 2.7, Fault-3 simulates a physical short between gate and source of transistor (M_1) of Figure 2.7, Fault-4 simulates a physical short between drain and substrate of transistor (M_4) of the amplifier circuit of Figure 2.5 [87] and Fault-5 simulates a physical short between gate and drain of transistor (M_{13}) of the amplifier circuit of Figure 2.5 [87]. Figure 2.15 show the simulated (in SPICE) capacitor discharge voltage of the BICS for the CUT (12-bit ADC) without fault injections, obtained at the comparator output and 12 clock pulses (1100) counted from the 4-bit counter output. The simulated pulse width is 14.74 μs. Figure 2.16 show the corresponding experimentally measured capacitor discharge voltage at the comparator output of the BICS which is 14.8 μs. HP 1660CS Logic Analyzer was used for counting the numbers from the output of the counter. Table 2.1 summarizes simulated count values from SPICE and experimentally measured values for all five injected faults in 12-bit ADC. For the activated Fault-1, which is in one of the transistors of the encoder circuit in Figure 2.9, the numerical count value is 0 (0000) and is same as the experimentally measured value. For the activated Fault-2, which is in transistor, M_3 of the comparator circuit of Figure 2.7 and stage-1 6-bit ADC of Figure 2.9, the numerical count value is 0 (0000) and is same as the experimentally measured value. For the activated Fault-3, which is in the transistor, M_1 of the comparator circuit of Figure 2.7

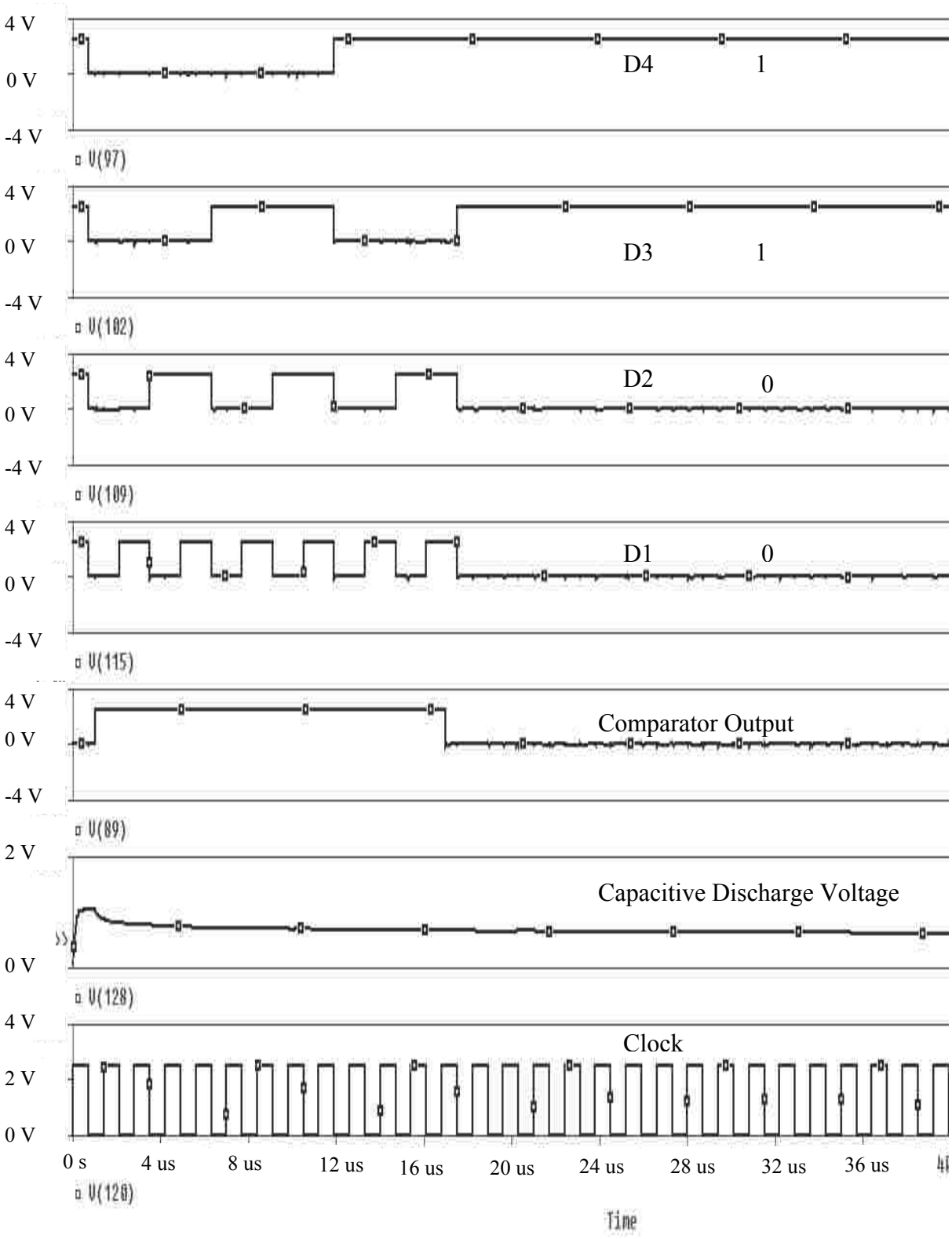


Figure 2.15: Simulated capacitive discharge voltage at the output of the comparator of the BICS for the CUT (12-bit ADC) without injected faults.

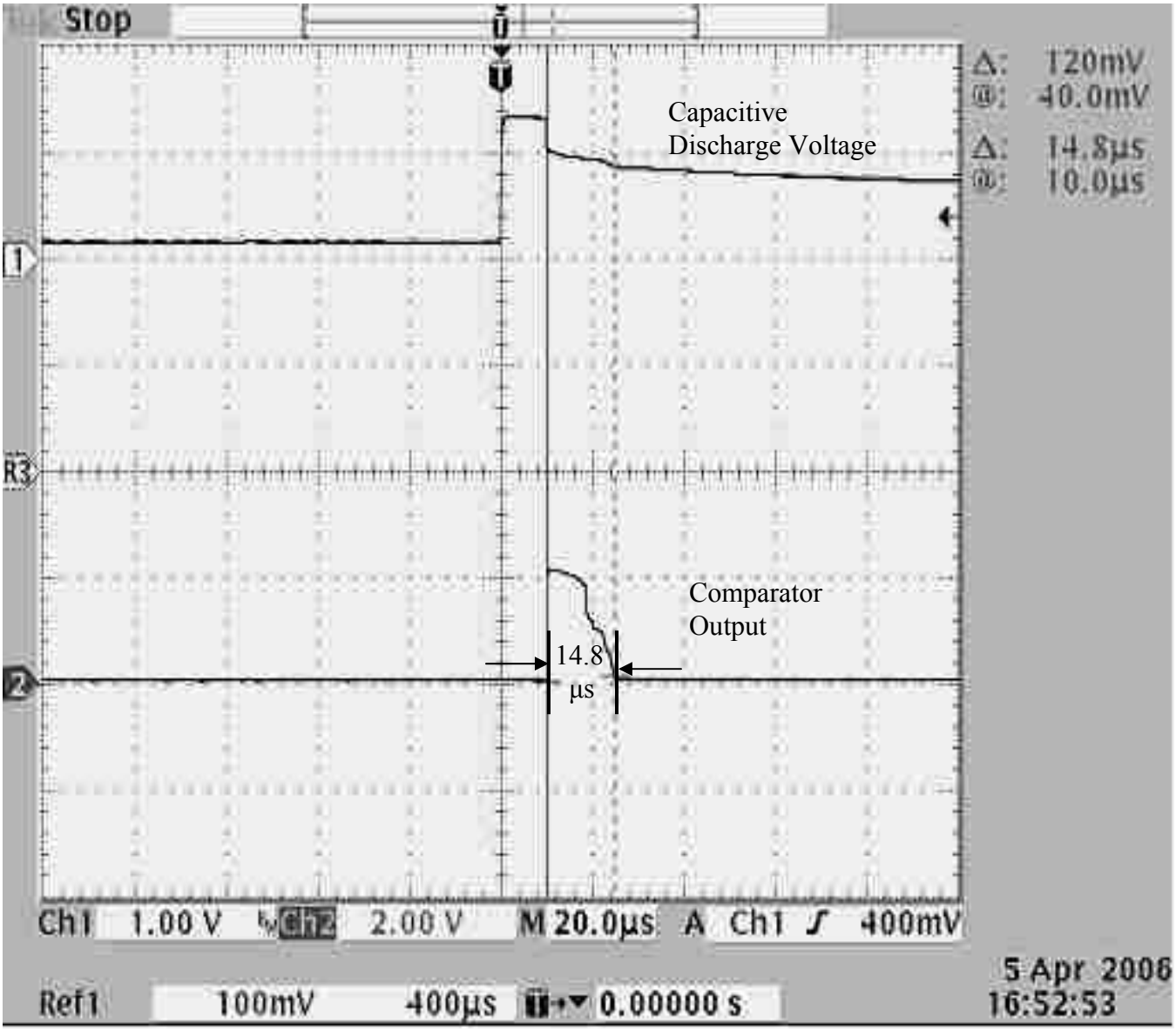


Figure 2.16: Experimentally observed capacitive discharge voltage at the output of the comparator of the BICS for the CUT (12-bit ADC) without injected faults.

Table 2.1: Simulated count values from SPICE and experimentally measured values for all five injected faults distributed in different blocks of the 12-bit ADC

Fault Condition	**Count Values Decimal (Binary Bits) (simulated)**	**Count Values Decimal (Binary Bits) (measured)**
No fault	12(1100)	12(1100)
Fault-1 (drain-substrate short)	0(0000)	0(0000)
Fault-2 (gate-substrate short)	0(0000)	0(0000)
Fault-3 (gate-source short)	15(1111)	15(1111)
Fault-4(drain-substrate short)	1(0001)	0(0000)
Fault-5 (gate-drain short)	8(1000)	8(1000)

and stage 1 6-bit ADC of Figure 2.9, the numerical count value is 15 (1111) and is same as the experimentally measured value. For the activated Falut-4, which is in transistor, M_4 of the op-amp circuit of Figure 2.5 [87], the numerical count value is 1 (0001) and the experimentally measured value is 0 (0000) and the difference is negligible. For the activated Fault-5, which is in is transistor, M_{13} of the op-amp circuit of Figure 2.5 [87], the numerical count value is 8 (1000) and is same as the experimentally measured value. The simulated and experimental results of ΔI_{DDQ} testing show that except Fault-3, rest of the injected faults in 12-bit ADC have been effectively detected.

Figure 2.17 shows the chip layout of the 12-bit DAC designed for operation at 2.5 V in 0.5 μm n-well CMOS process with a small sub-set of five defects introduced using fault injection transistors (FITs) as switches [86, 97]. The design integrates an on-chip BICS of Figure 2.1 for ΔI_{DDQ} testing for physical defects such as shorts in MOSFETs. The DAC occupies 504 × 501 μm^2 area of the chip. The BICS occupies 498 × 75 μm^2 area of the chip. Figure 2.18 shows the microphotograph of the fabricated 12-bit DAC-BICS chip. Figure 2.19 shows the simulated and experimentally measured output characteristics of the 12-bit DAC with INL within ±1LSB and DNL within ±0.7LSB. DAC was tested with all inputs tied to ground.

Similar to 12-bit ADC testing for faults, 12-bit DAC was also tested by the ΔI_{DDQ} method using fault equivalence combined with fault injection transistors in series with resistors. The effect of ±5% process variations was taken into consideration and a range of discharge time was identified for fault identification which is 21.4 – 60.32 μs. The scan-path method was not used in DAC since its digital part consists of few multiplexers implemented using CMOS switches. Sixty short faults were introduced in unity gain amplifier and buffer parts of the DAC. A total of 55 faults were tested positively and 5 faults could not be tested.

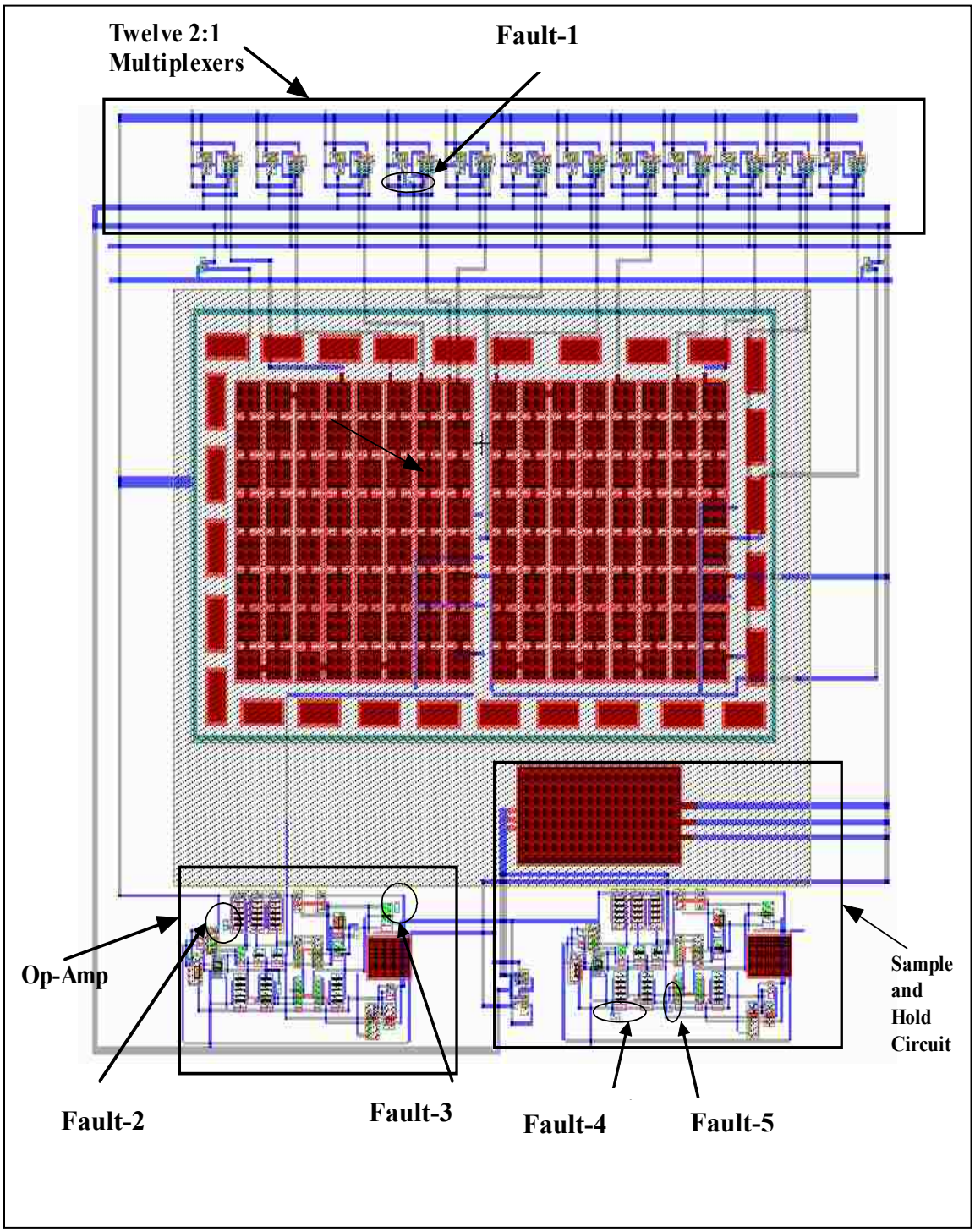


Figure 2.17: Chip layout of 12-bit charge scaling DAC.

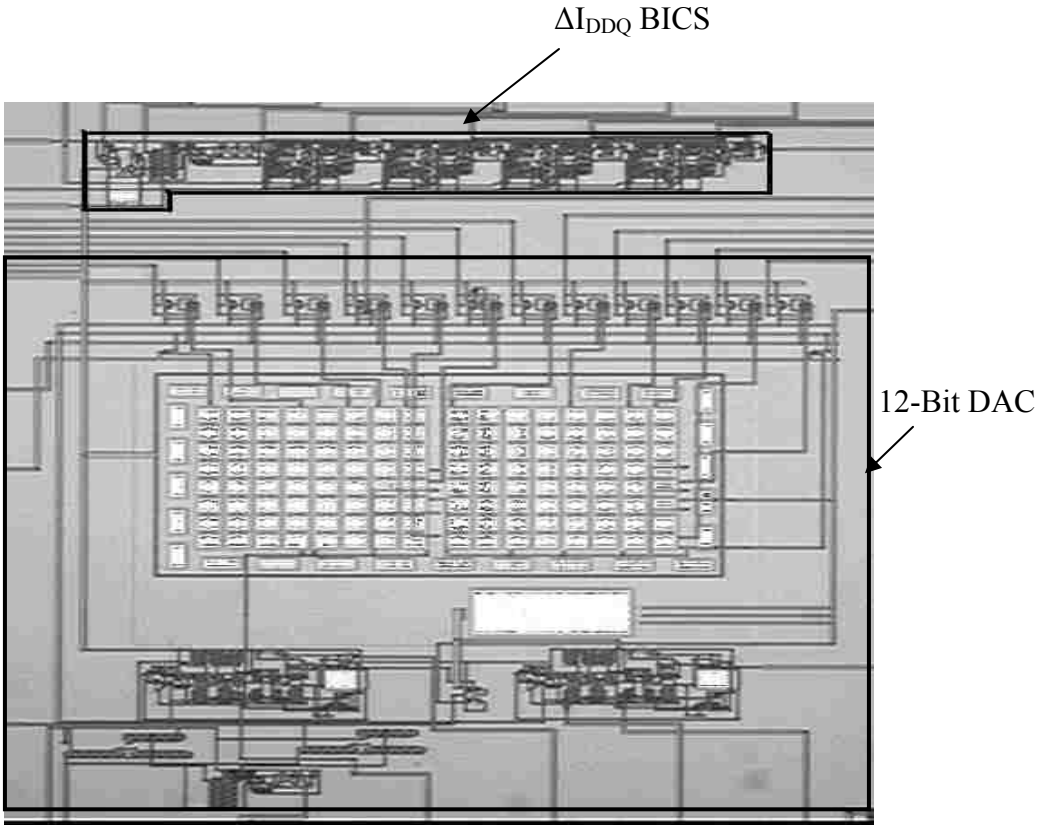


Figure 2.18: Microphotograph of the fabricated 12-bit DAC-BICS chip.

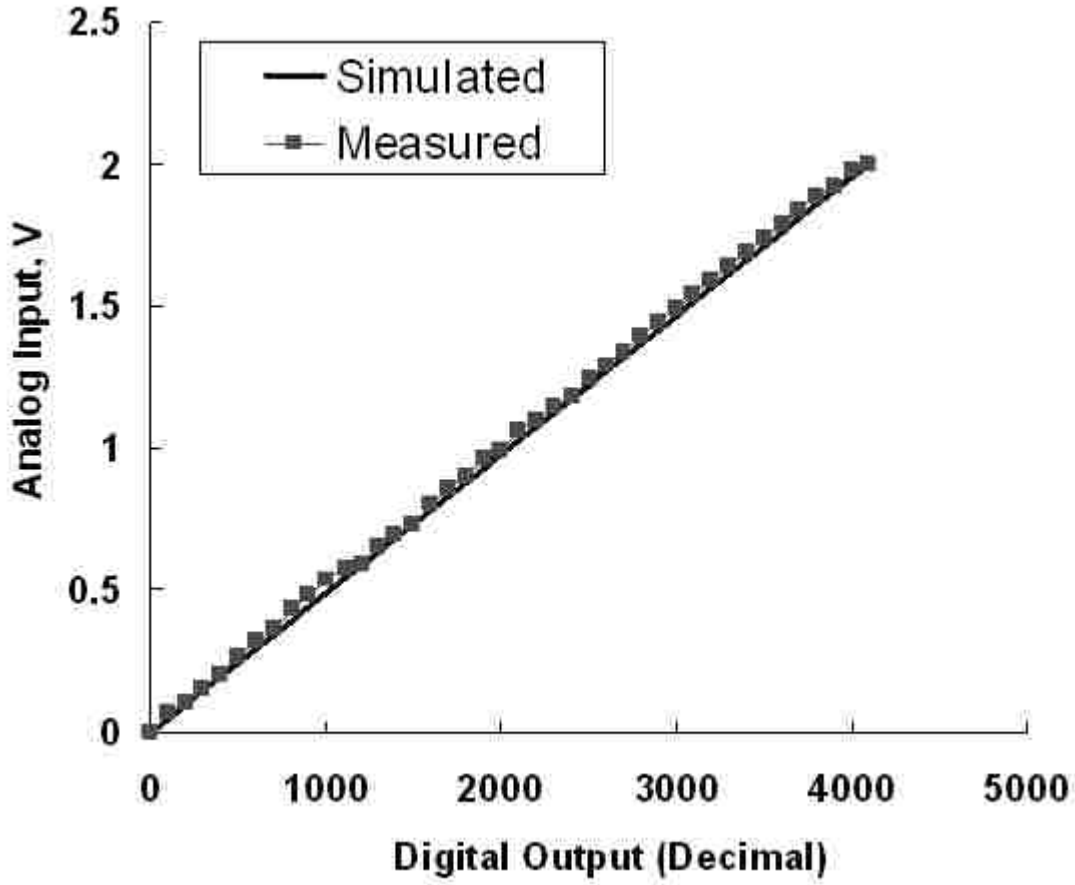


Figure 2.19: Simulated and experimentally measured output characteristics of 12-bit DAC.

Thus, overall the fault coverage is about 92%.

The 12-bit DAC fabricated design was also tested experimentally by the ΔI_{DDQ} method for a small sub-set of five injected faults using fault injection transistors as in 12-bit ADC. In Figure 2.17 and the fabricated chip shown in Figure 2.18, Fault-1 simulates a physical short between drain and source of one of the transistors in multiplexer part of the circuit of Figure 2.17 , Fault-2 simulates a physical short between drain and source of one of the transistors of the op-amp part of the circuit of Figure 2.17, Fault-3 simulates a physical short between gate and drain of one of the transistors of the op-amp part of the circuit of Figure 2.17, and Fault-4 simulates a physical short between source and substrate of one of the transistors of the sample-and-hold circuit part of the circuit of Figure 2.17. Fault-5 simulates an inter-gate short between two transistors of the unity gain amplifier which is the part of sample and hold circuit of Figure 2.17. Figure 2.20 shows the simulated (in SPICE) capacitor discharge voltage of the BICS for the CUT (12-bit DAC) without fault injections, obtained at the comparator output and 10 clock pulses (1010) counted from the 4-bit counter output. The simulated pulse width is 51 μs. Figure 2.21 shows the corresponding experimentally measured capacitor discharge voltage at the comparator output of the BICS which is 49.6 μs. HP 1660CS Logic Analyzer was used for counting the numbers from the output of the counter.

Table 2.2 summarizes simulated count values from SPICE and experimentally measured values for all five injected faults randomly distributed in different blocks of the 12-bit DAC. For the activated Fault-1, the numerical count value is 1(0001) and is same as the experimentally measured value. For the activated Fault-2, the numerical count value is 14 (1110) and is same as the experimentally measured value. For the activated Fault-3, the numerical count value is 9 (1001) and is same as the experimentally measured value.

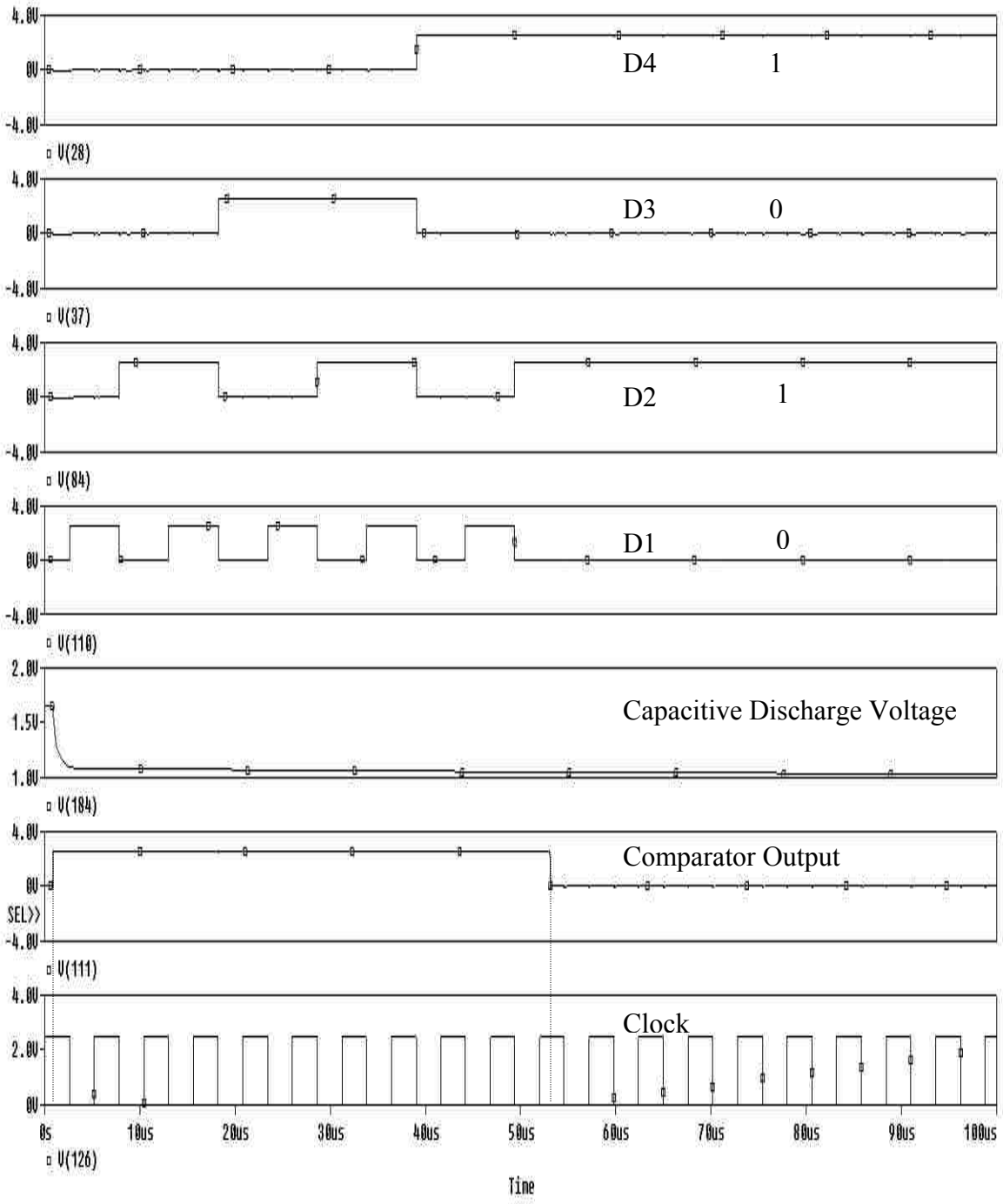


Figure 2.20: Simulated capacitive discharge voltage at the output of the comparator of the BICS for the CUT (12-bit DAC) without injected faults.

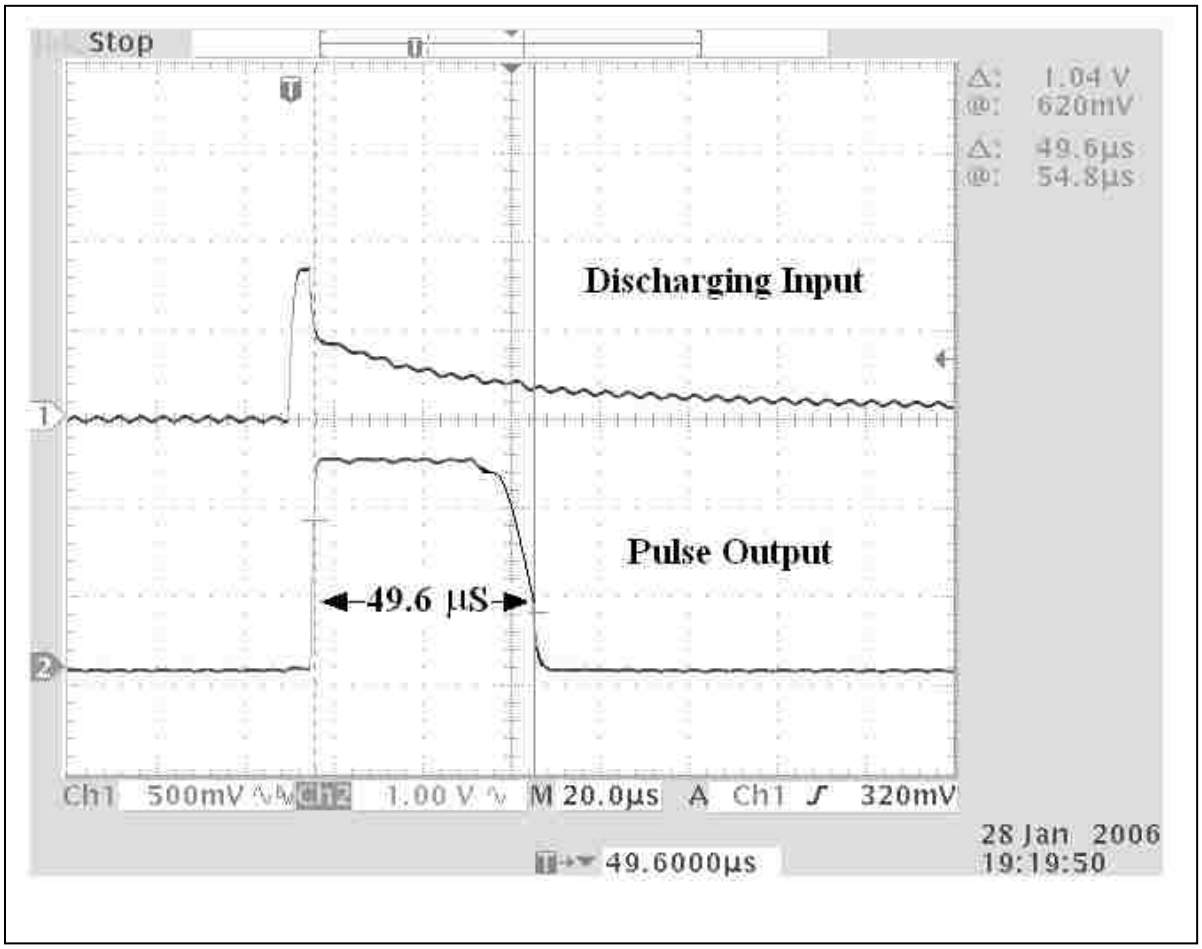


Figure 2.21: Experimentally observed capacitive discharge voltage at the output of the comparator of the BICS for the CUT (12-bit DAC) without injected faults.

For the activated Falut-4, the numerical count value is 2 (0010) and is same as the experimentally measured value. For the activated Fault-5, the numerical count value is 7 (0111) and is same as the experimentally measured value. The simulated and experimental results of ΔI_{DDQ} testing show that except Fault-2, rest of the injected faults in 12-bit DAC were effectively detected.

2.5 Conclusion

A simple BICS which measures difference in power supply quiescent current under the capacitive discharge voltage across the CUT has been used for testing of physical defects such as shorts in CMOS data converter circuits. The design of BICS follows from the work of Keating and Meyer [72], off-chip Quick-Mon of [73], and Vazquez and de Gyvez [57, 58] for digital ICs. The BICS used in the present work is slightly modified for data converters using two CMOS transmission gates replacing a single p-MOSFET switch connecting CUT and V_{DD} for better isolation from V_{DD}. It can detect current to an accuracy of 0.5 μA. The data converters used as CUT are 12-bit ADC and 12-bit DAC designed in 0.5μm CMOS process and tested for normal operation under fault free conditions. The ADC uses recycling architecture and DAC uses charge scaling architecture for design. The method of ΔI_{DDQ} testing has been combined with logic scan-path method for digital testing and fault equivalence in combination with fault injection transistors in series with resistors for introduction of a large number of faults. The combined methods have allowed introducing 520 faults in ADC and 60 faults in DAC with approximately 94% faults coverage in ADC and 92% in DAC, respectively from post-layout simulation experiments. A small sub-set of 5 faults were also experimentally tested from ΔI_{DDQ} method with the exception of one fault in

Table 2.2: Simulated count values from SPICE and experimentally measured values for all five injected faults randomly distributed in different blocks of the 12-bit DAC

Fault Condition	**Count Values Decimal (Binary Bits) (simulated)**	**Count Values Decimal (Binary Bits) (measured)**
No fault	10(0101)	10(0101)
Fault-1(drain-source short)	1(0001)	1(0001)
Fault-2(drain-source short)	14(1110)	14(1110)
Fault-3 (drain-gate short)	9(1001)	9(1001)
Fault-4(source-substrate short)	2(0010)	2(0010)
Fault-5(inter-gate short)	7(0111)	7(0111)

both ADC and DAC. The method also includes the effect of process variations on BICS performance by considering ±5% variation in process transconductance and threshold voltage parameters of the MOSFET. ΔI_{DDQ} testing combined with the scan-path method, fault equivalence combined with fault injection transistors technique have been very effective in testing 12-bit CMOS ADC and DAC circuits with at least 90% or more fault coverage.

In the present work, the BICS is tested experimentally on fabricated 12-bit ADC and 12-bit DAC chips for a small sub-set of injected faults. A large set of injected faults could not be tested experimentally because of limitation on chip size due to cost and number of available pins for testing. In our case it is a tiny chip in 40-pin DIP. The test results obtained from simulations are in close agreement with the corresponding experimentally measured results on fabricated chips. However, a large number of faults have been detected through post-simulation experiments using scan-path and fault equivalence methods. The flash ADC design in the present work is generic which may cause some static non-linearity in its output[101]. However, no such non-linearity is observed at the output of 12-bit ADC. This is achieved by adjusting the slew rate of op-amp circuit and speed of 3-bit flash ADC in design. The simple BICS combined with the fault injection method combined with fault equivalence techniques and the logic scan-path can be applied in testing of mixed-signal integrated circuits designed in submicron CMOS processes.

CHAPTER 3*

ΔI_{DDQ} TESTING OF CMOS DIGITAL-TO-ANALOG CONVERTER

3.1 Introduction

In this chapter, ΔI_{DDQ} testing of a 12-bit digital-to-analog converter (DAC) chip designed in 0.5 μm n-well CMOS process is presented. The built-in-current sensor (BICS) uses frequency as the output for fault detection in circuit under test (CUT). A fault is detected if it causes the output frequency to deviate more than ±10% from the reference frequency. A set of eight faults simulating manufacturing defects in CMOS devices were injected using fault-injection transistors (FITS). It is shown that the present method detected all injected faults.

3.2 Built-in Current Sensor for ΔI_{DDQ} Testing

The BICS design is based on Keating-Meyer approach for I_{DDQ} testing [72] and is a modification of MEAS block of delta I_{DDQ} BICS by Vazquez and de Gyvez [57, 58]. Figure 3.1 shows the circuit diagram of the BICS up to comparator stage and follows the operation as described in Chapter 2. The BICS of Figure 3.1 differs from the BICS of Figure 2.1 of Chapter 2 as follows. The output of the comparator is used as an input to the NMOS switch (MX) which charges the capacitor C_2 shown in Figure 3.1. The comparator circuit used in the BICS is shown in Figure 3.2 [100]. The voltage across C_2, V_{CTRL} in Figure 3.1 depends on the time MX switch is on which in-turn depends on the discharge time of the capacitor (C_1). The voltage across the capacitor, V_{CTRL} with a time constant equal to 2.2RC, is given to voltage controlled oscillator which is shown in Figure 3.3 where R is in series with C_2. The

---

* Part of the work is reported in following publications:
S. Yellampalli and A. Srivastava, "ΔI_{DDQ} based testing of sub-micron CMOS integrated circuits," *Journal of Active and Passive Electronic Devices*, vol.3, pp. 341-353, 2008.

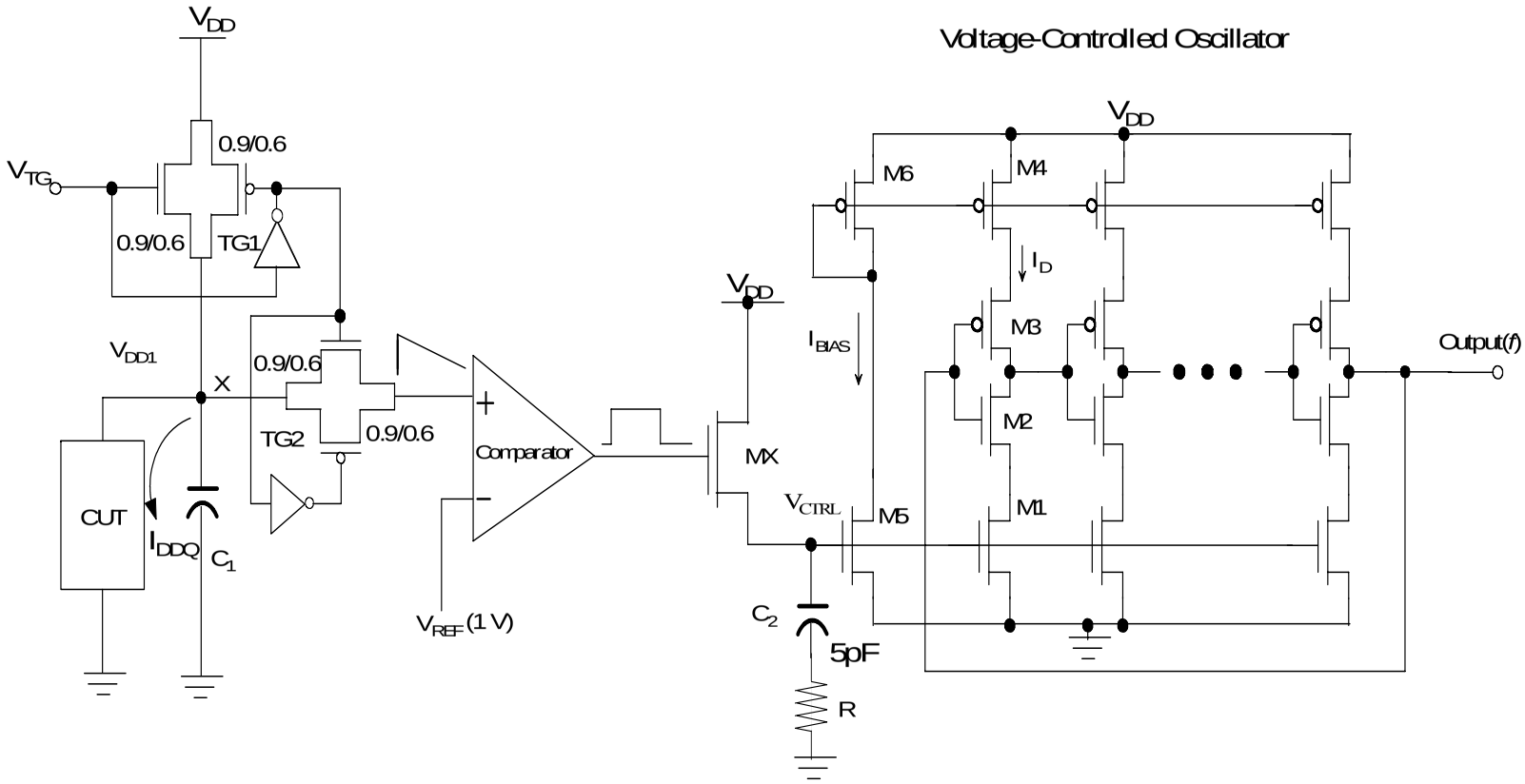


Figure 3.1 : ΔI_{DDQ} built-in current sensor (BICS) circuit.

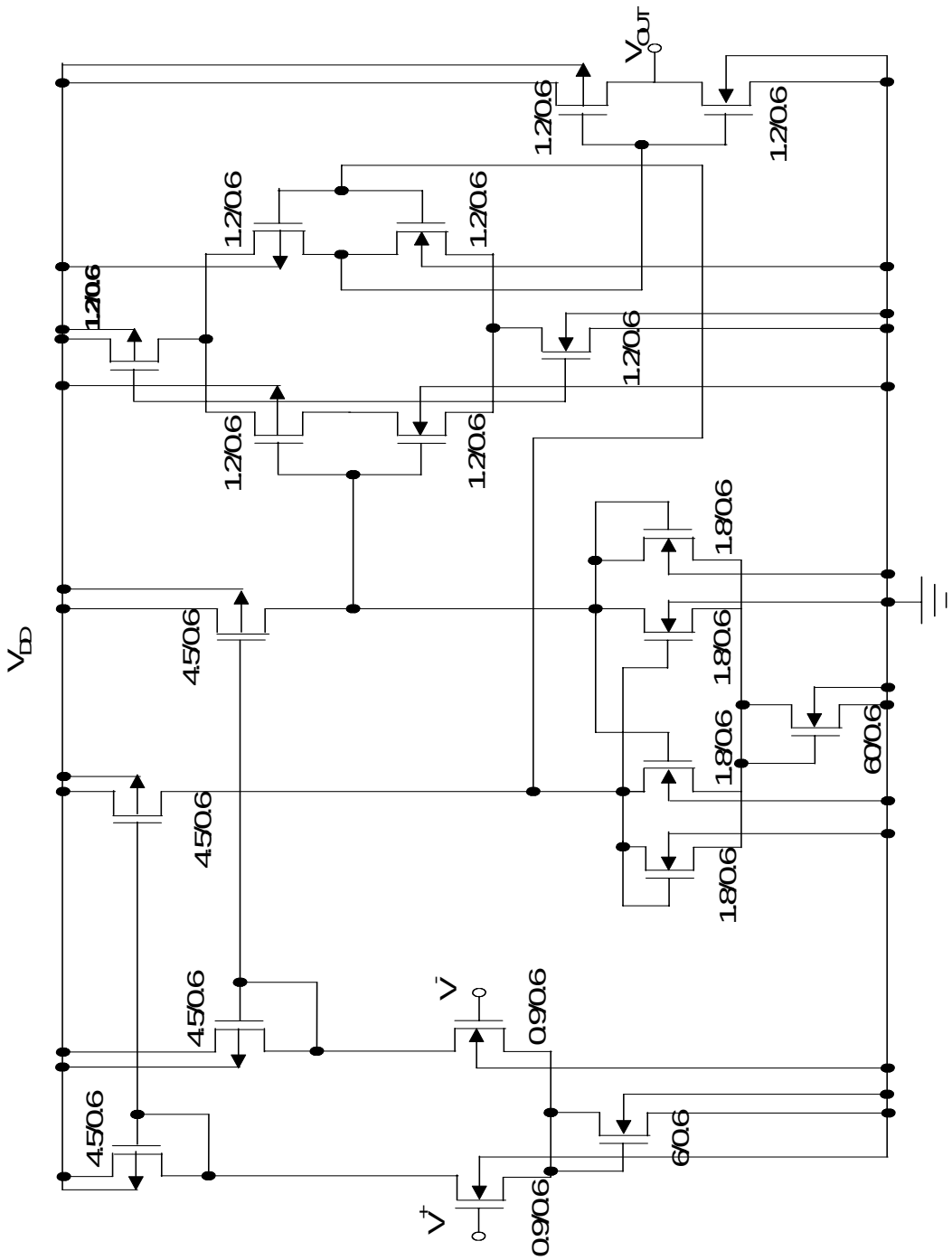


Figure 3.2 : CMOS comparator circuit [100].

reference voltage of the comparator output changes due to change in quiescent current when a defect is introduced which changes V_{CTRL} as shown in Figure 3.3 and thus the output frequency.

The output of a VCO is a clock signal, the frequency of which is dependent on V_{CTRL}. Its operation is similar to a ring oscillator. MOSFETs M_2 and M_3 operate as an inverter while MOSFETs M_1 and M_4 operate as current source and sink, which limit the current available to the inverter or in other words the inverter is starved of the current. MOSFETs M_6 and M_5 are mirrored in each inverter current source and sink stage. The oscillation is achieved by charging and discharging the equivalent output capacitance in each stage of the VCO. The oscillation frequency of the current starved VCO for n (an odd number ≥ 3) of stages is given by [102],

$$f_O = \frac{1}{n\left(t_r + t_f\right)} \approx \frac{I_D}{n \cdot \left(C_{out} + C_{in}\right) \cdot V_{DD}} \tag{3.1}$$

where t_r and t_f are the rise time and the fall time, respectively, and n is the number of stages. V_{DD} is the power supply voltage. I_D is the biasing current of M_2 and M_3. C_{out} and C_{in} are the output and input capacitance of the inverter.

3.3 12-Bit Digital-to-Analog Converter Design

The 12-bit DAC design uses a charge scaling architecture [100]. The block diagram of a 12-bit charge scaling DAC using spilt array method is shown in Figure 3.4. The DAC converts a 12-bit digital input word to a respective analog signal by scaling a voltage reference. The various blocks in DAC include a voltage reference, binary switches, a scaling network, an operational amplifier and a sample and hold circuit. The multiplexer circuit connected to the other end of each capacitor selects the voltage which is either V_{REF} or

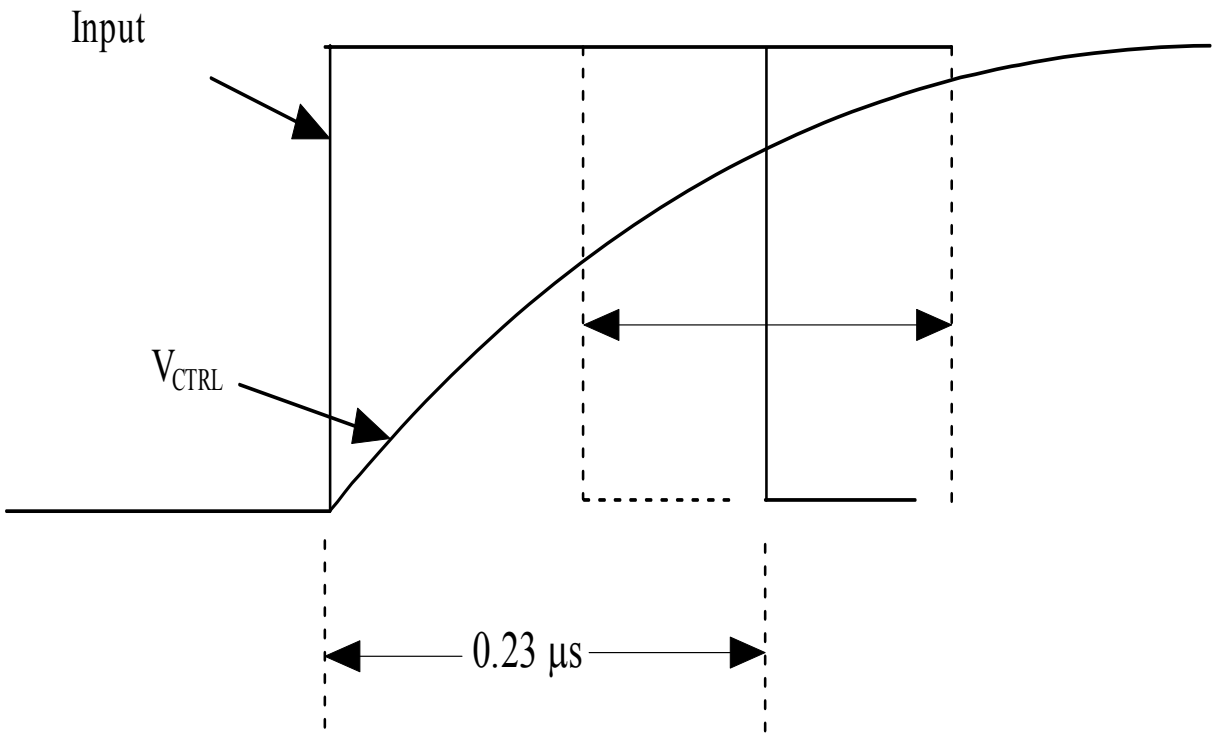


Figure 3.3: Rise time of RC circuit.

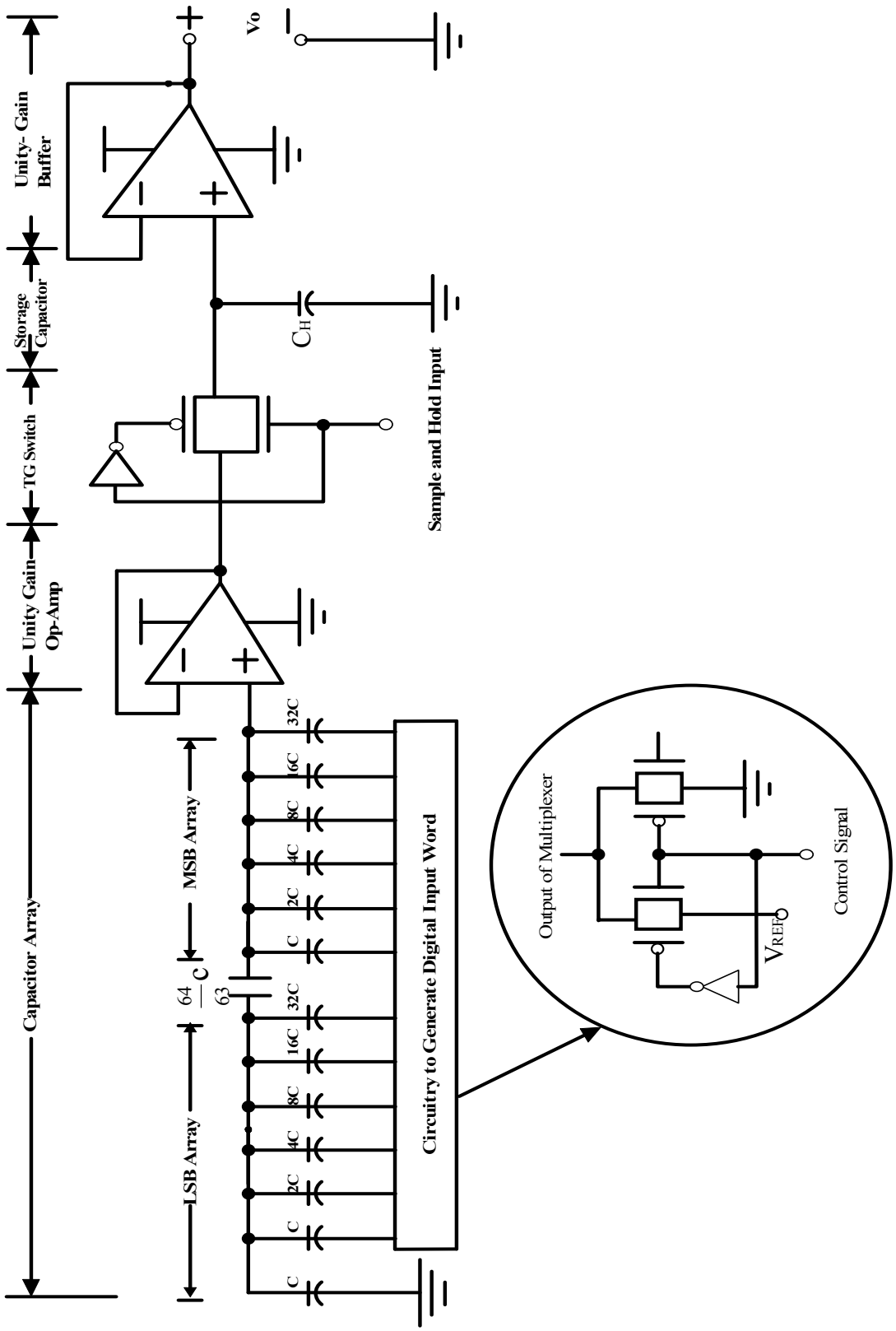


Figure 3.4 : Schematic of 12-bit charge scaling digital-to-analog converter (DAC).

'GND' to which the capacitor is charged depending upon the control signal 'V_S'. Initially, the control signal for all multiplexer switches is set to LOW before giving any specified input so that GND is supplied to the capacitor network to reset. Then the capacitor network is supplied with the digital word by switching the particular multiplexer switch for each bit to the desired value of either V_{REF} for "1" or GND for "0". The capacitors whose ends are connected to V_{REF} are charged to +2 V and those, which are connected to GND are charged to 0 V. Since the capacitor network is connected in parallel, the equivalent voltage is calculated by,

$$V_{OUT} = (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \ldots\ldots + B_N 2^N) V_{REF}. \quad (3.2)$$

The capacitor at the end of the network is used as a 'terminating capacitor'. Depending on the capacitors, which are charged to different voltages based on the input digital word, the effective resultant analog voltage is calculated for the respective digital combination. The analog voltage is passed through the op-amp and through the sample-and-hold circuit and appears as an analog voltage.

The op-amp and comparator used in DAC is designed for 2.5V operation and is shown in Figure 3.5. It is also used as a unity gain amplifier. The input stage of the amplifier consists of two transistors M_1-M_2 which constitute a simple n-channel differential amplifier. Transistors M_{15}, M_3 and M_4 act as PMOS current mirrors serving as a current source and transistors M_{16} and M_5 act as n-MOS current mirror serving as a current sink. The signal currents of the differential output are folded through the transistors M_6 and M_7 and converted into a single-ended output with the n-channel current mirror (M_8 and M_9). Transistors M_{12}, M_{11}, M_{25} and M_{10} constitute the high swing cascode current source for the op-amp. We notice from Figure 3.5 that the saturation voltage, V_{GS}-$|V_{th,p}|$ of M_4 is V_{ON} which gives the

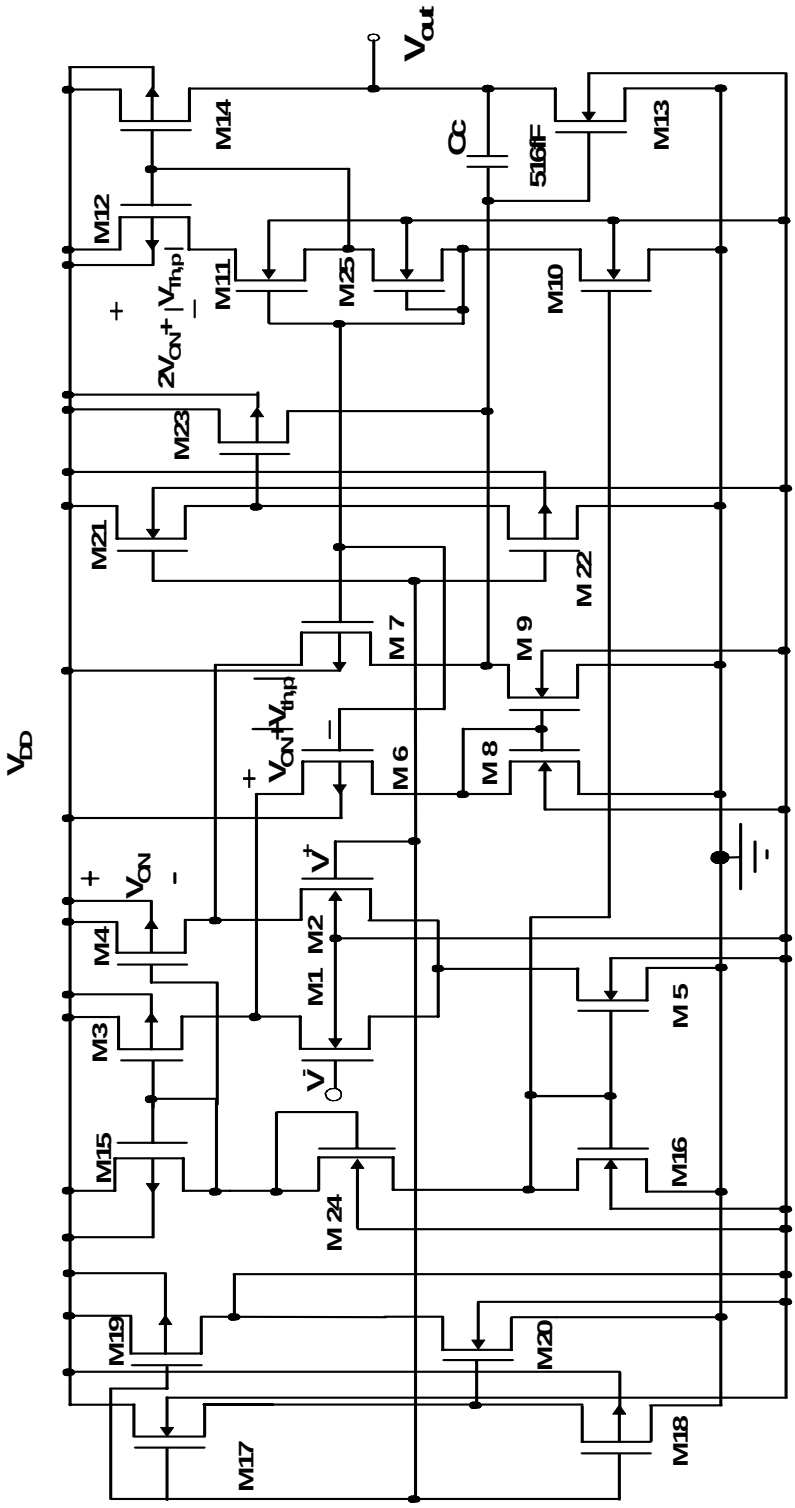


Figure 3.5 : CMOS amplifier circuit.

gate-source voltage of M_6 and M_7 as $|V_{th,p}| + V_{ON}$, which in turn makes the voltage across M_{12} as $|V_{th,p}| + 2V_{ON}$. This is the minimum voltage required at a drain of M_{11} so as to allow a large range of V_{OUT} values. Transistors M_{17}, M_{19}, M_{18} and M_{20} constitute the bulk driving circuitry. This circuitry acts to enable n-channel transistors of the differential pair to respond to voltages below 0.7 V. The amplifier is operated at 2.5V. C_C is the pole splitting capacitor. The output stage consisting of transistors M_{13} and M_{14} is class-A amplifier. The op-amp has an open loop gain of 28 dB, phase margin of 89° and a 3 dB bandwidth of 40 KHz. W/L ratios of transistors in CMOS amplifier circuit of Figure 3.5 are given in Table 3.1.

3.4 Result and Discussion

Figure 3.6 shows the chip layout of the 12-bit DAC designed for operation at 2.5 V in 0.5 μm n-well CMOS process with eight defects introduced using fault injection transistors (FITs) as switches [86, 97]. Figure 3.7 shows the chip layout of 12-bit DAC-BICS in a 40-pin padframe. The design integrates an on-chip BICS of Figure 3.1 for ΔI_{DDQ} testing for physical defects such as shorts in MOSFETs. The DAC occupies 504 × 501 μm^2 area of the chip. The BICS occupies 670x75 μm^2 area of the chip. Figure 3.8 shows the simulated output characteristics of the 12-bit DAC with INL within ±1LSB and DNL within ±0.7LSB. The fault injection transistors are activated externally by connecting their gates directly to signals of amplitude, V_{DD}. The W/L ratio of the FIT in the present design is 1.05 μm/0.6 μm.

In Figure 3.6, Fault-1 and Fault-2 simulate a physical short between drain and source of two of the transistors in multiplexer part of the circuit. Fault-3 and Fault-4 simulate a physical short between gate and source and drain and source in two of the transistors in the op-amp part of the circuit in Figure 3.6. Fault-5 and Fault-6 simulate a gate-substrate and gate-drain short in two of the transistors pf the op-amp part of the circuit in Figure 3.6.

Table 3.1: Device dimensions used in the amplifier circuit of Figure 3.5

Transistor Numbers	**W/L (µm/ µm)**	**Transistor Numbers**	**W/L (µm/ µm)**	**Transistor Numbers**	**W/L (µm/ µm)**
M1	3.0/1.2	M10	6.0/0.6	M19	3.3/1.8
M2	3.0/1.2	M11	3.0/6.0	M20	5.7/3.0
M3	9.0/0.6	M12	0.9/0.9	M21	3.0/0.6
M4	9.0/0.6	M13	2.7/2.7	M22	1.8/2.4
M5	6.0/0.6	M14	0.9/0.9	M23	2.1/2.1
M6	3.3/0.6	M15	6.0/0.6	M24	3.0/1.5
M7	3.3/0.6	M16	6.0/0.6	M25	0.9/1.8
M8	3.0/0.9	M17	3.0/0.6		
M9	3.0/0.9	M18	2.7/0.6		

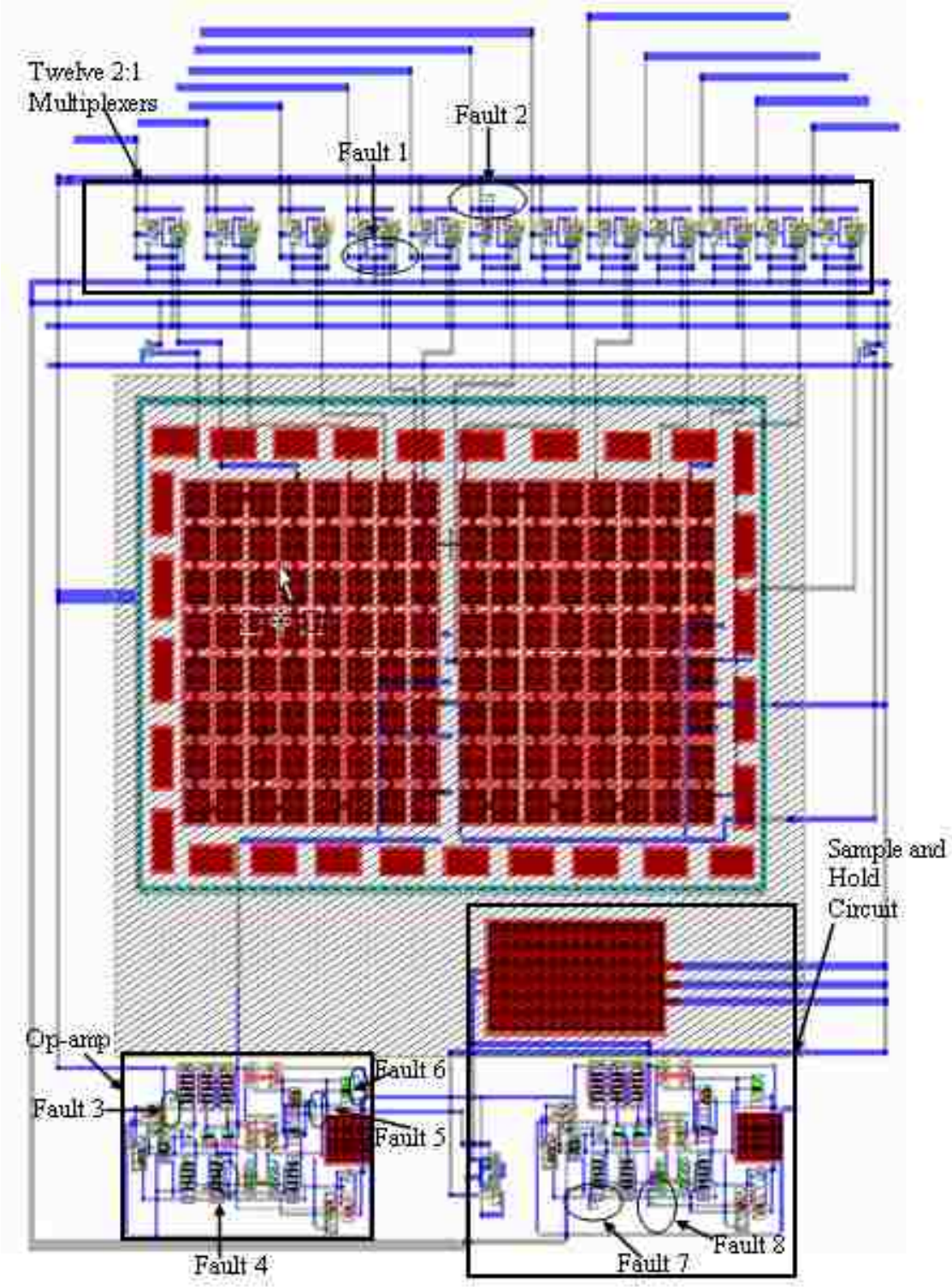


Figure 3.6: Chip layout of 12-bit DAC with randomly distributed faults.

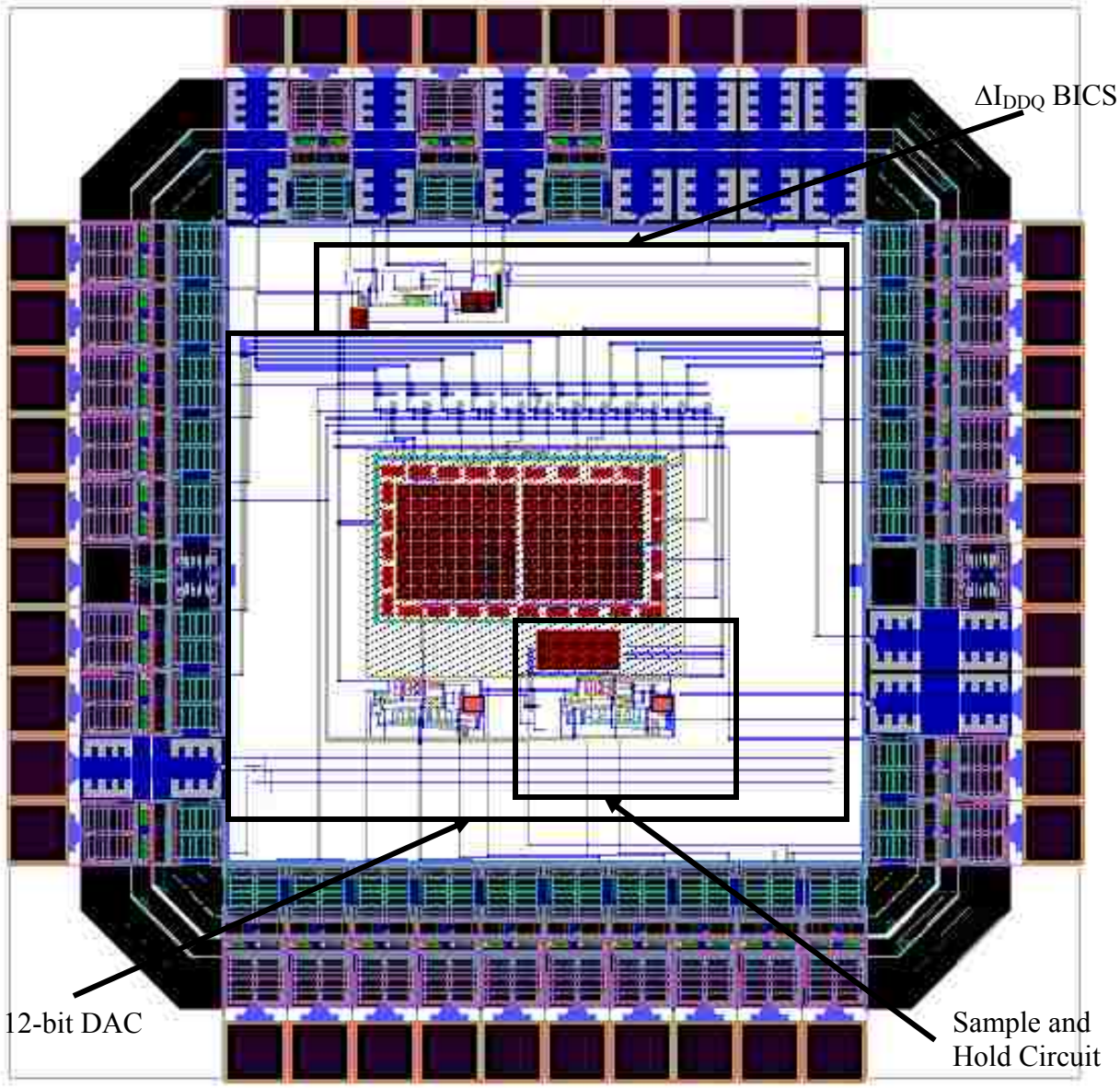


Figure 3.7: Chip layout of 12-bit DAC-BICS in 40-pin padframe.

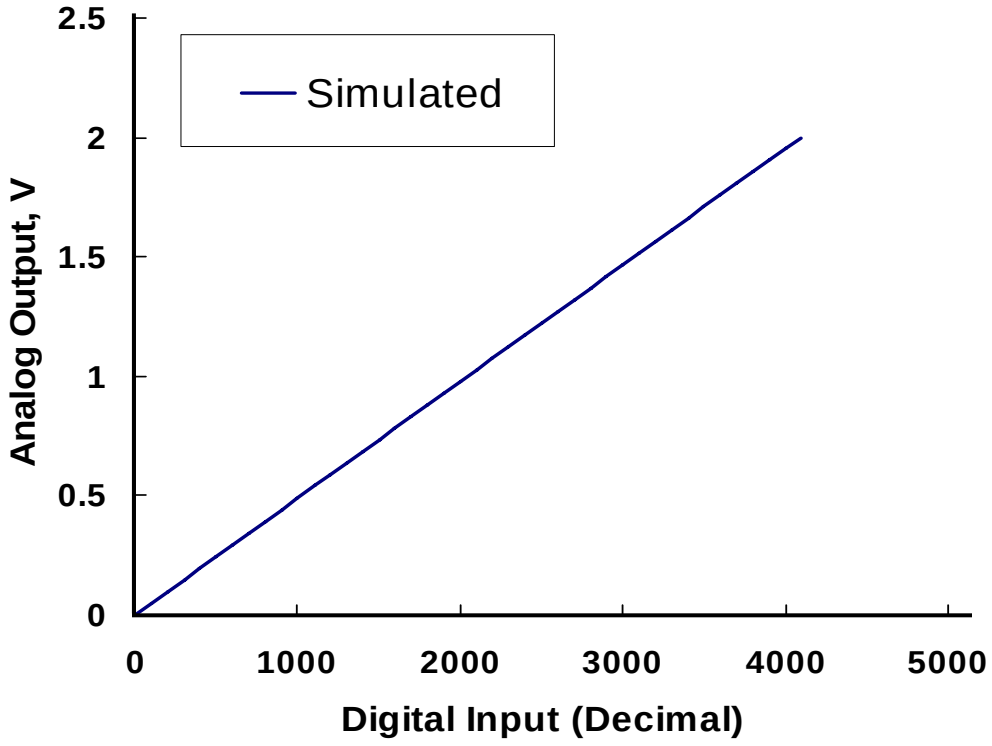


Figure 3.8: Output characteristics of the 12-bit DAC.

Fault-7 simulates a source-substrate short of one of the transistors of the sample-and-hold circuit part of the circuit of Figure 3.6, and Fault-8 simulates an inter-gate short between two transistors in the unit gain op-amp of the sample-and-hold circuit. Table 3.2 summarizes deviation (%) in frequency of the BICS of the CUT under these fault injection conditions with respect to fault free condition. The reference frequency (f_R) of BICS of the fault free CUT is 7.27 x 10^6 Hz. The circuit is considered faulty if the deviation is ±10%.

3.5 Conclusion

The BICS presented in this work is based on the method proposed by Keating and Mayer [72] and Vazquez and de Gyvez BICS [57, 58], has been modified for fault detection for analog and mixed signal integrated circuits designed in submicron CMOS process. The BICS uses the voltage controlled oscillator where frequency as its output is used as a curser for detecting faults. A CUT with ±10% deviation from the reference frequency is considered as faulty. The circuit under test is a 12-bit digital-to-analog converter which is designed in 0.5 μm n-well CMOS process. Eight faults were injected using fault injection transistors simulating manufacturing defects. These faults were injected in CMOS devices and randomly distributed. All eight faults were detected using the BICS. The faults were limited to eight because of the tiny chip limited in size (2.2 x 2.2 mm^2). The method can be applied in testing of other CMOS mixed-signal VLSI circuits.

Table 3.2: Deviation (%) in frequency output of BICS under fault injection conditions

Injected Faults	**Pulse width (μS) (Output of Comparator)**	**V_{C2} (V) (C_2=5pF)**	**Frequency @ BICS Output (MHz) C_2=5pF**	**Frequency Deviation from f_R (%) (f_R =7.27 MHz)**
No Fault	0.230	1.236	7.27	00.00
Fault 1	0.108	1.175	8.65	18.98
Fault 2	0.109	1.165	8.07	11.00
Fault 3	0.216	1.210	4.82	-33.70
Fault 4	0.215	1.215	4.65	-36.04
Fault 5	0.215	1.215	4.63	-36.31
Fault 6	0.229	1.220	4.42	-39.20
Fault 7	0.215	1.217	4.40	-39.48
Fault 8	0.256	1.248	4.17	-42.64

CHAPTER 4*

COMBINED OSCILLATION, TRANSIENT POWER SUPPLY CURRENT AND QUIESCENT CURRENT TESTING OF CMOS AMPLIFIER CIRCUITS

4.1 Introduction

In this chapter, a simple test methodology combining oscillation and quiescent power supply current (I_{DDQ}) testing for detecting bridging and open faults in a CMOS amplifier circuit designed for operation at $\pm$ 2.5 V in 1.5 μm n-well CMOS process is presented. The testing is performed at room temperature (300 K) and also at liquid-nitrogen temperature (77 K) to enhance fault detection. An on-chip built-in current sensor (BICS) has been integrated to monitor I_{DDQ} of the circuit under test (CUT). A simple fault-injection technique has been used for simulating manufacturing defects. Part of the testing results which were reported in [103] have been reproduced here for completeness.

The test methodology is also extended to include transient power supply current testing. The combined test methodology including oscillation, quiescent current and transient current testing has been used for fault detection in an op-amp with floating gate input transistors. The amplifier was designed for operation at $\pm$ 2.5 V in a standard 1.5 μm n-well CMOS process. Theoretical results obtained from SPICE simulations are in close agreement with the corresponding experimental results on fabricated devices. Part of the testing results which were reported in [104] have been reproduced here for completeness.

---

* Part of the work is reported in following publications:

1. A. Srivastava, S. Yellampalli, P. Alli and S. S. Rajput, "Combined oscillation and I_{DDQ} testing of a CMOS amplifier circuit," *International Journal of Electronics,*2008 (Accepted).
2. S. Yellampalli, A. Srivastava and V. Pulendra, "A combined oscillation, power supply current and I_{DDQ} testing methodology for fault detection in floating gate input CMOS operational amplifier," *Proceeding of 48th IEEE International Midwest Symposium on Circuits and Systems,* pp. 503-506, 2005.

Oscillation test methodology is a vector less test method for analog and mixed-signal design-for-test (DFT) method based on oscillation-test methodology (OTM) [79] suitable for both functional and defect oriented testing, has been successfully applied to CMOS analog circuits [105-107] such as the analog-to-digital converters, bi-quadratic filters and active RC filters [80, 90, 91]. This test methodology has normal and test modes of operation. During the test mode, a change in the oscillation frequency of the CUT from its nominal value indicates the possibility of faults. Such OTM is shown to be an effective functional 'go' and 'no-go' test to verify if the circuit under test conforms to the required specifications.

Power supply quiescent current (I_{DDQ}) testing has shown to be very efficient for improving the test quality [108-111]. The test methodology based on the observation of the quiescent current I_{DDQ} [111] allows testing of physical defects such as gate-oxide shorts, floating gates and bridging faults due to manufacturing.

Power supply transient current (I_{DDT}) testing is a test method in which the average transient current of the V_{DD} power supply is measured [112]. The measurement is done when the input changes from logic level '1' to logic level '0' or from logic level '0' to logic level '1'. When the input level is changed the power supply current instantaneously varies before all the gates stabilize. If power supply current increases or decreases significantly due to a fault in the CUT, the fault is considered to be I_{DDT} testable.

In this chapter, a design-for-testability (DFT) method for CMOS analog integrated circuits, based on combined oscillation test methodology, I_{DDQ} and I_{DDT} testing has been presented. The advantage is that faults which could not be detected by I_{DDQ} and I_{DDT} testing can be probably detected at the oscillation level and vice-versa. A CMOS amplifier has been considered for the applicability of the method as well as for the demonstration because amplifier is one of the commonly used building blocks in analog and mixed-signal integrated

circuits. Apart from testing at room temperature, CMOS amplifier has been also been tested at 77 K. Testing at 77 K has been done to improve detection of faults since subthreshold current component in I_{DDQ} and noise in the CUT can be easily suppressed. The nominal frequency range of the CUT is determined using a Monte-Carlo analysis taking into account the tolerance of significant technology and design parameters. The faults which result in deviation of oscillation frequency from fault free condition are then tested through I_{DDQ} testing at 300 K and 77 K. A recently reported simple built-in current sensor (BICS) design [86, 113] has been used. The BICS used in the present design introduces insignificant performance degradation in CUT. In normal mode, the operation of CUT is independent of BICS. The injected faults are simulated using a simple fault-injection technique [86, 97] for manufacturing defects.

4.2 Oscillation Testing Method

Figure 4.1 shows the circuit diagram of a two-stage, internally compensated CMOS amplifier as a CUT for testing which is designed for operation at $\pm$ 2.5 V [103]. It is designed in a standard 1.5 μm n-well CMOS process. The circuit is simulated in SPICE using MOS level 3 model parameters. During test mode, the CUT is separated from its normal external inputs using a DFT [80] procedure and is then converted into an oscillator using a RC-delay circuit in the feedback path, such that the total phase shift around the loop is zero. Figure 4.2 (a) shows an operational amplifier, which is converted into an oscillator using the RC feedback network for OTM [80]. Figure 4.2 (b) [103] shows the CMOS oscillator circuit in which the CMOS amplifier circuit of Figure 4.1 is used in Figure 4.2 (a) configuration. The transfer function of the feedback circuit of Figure 4.2(a) is given by [80],

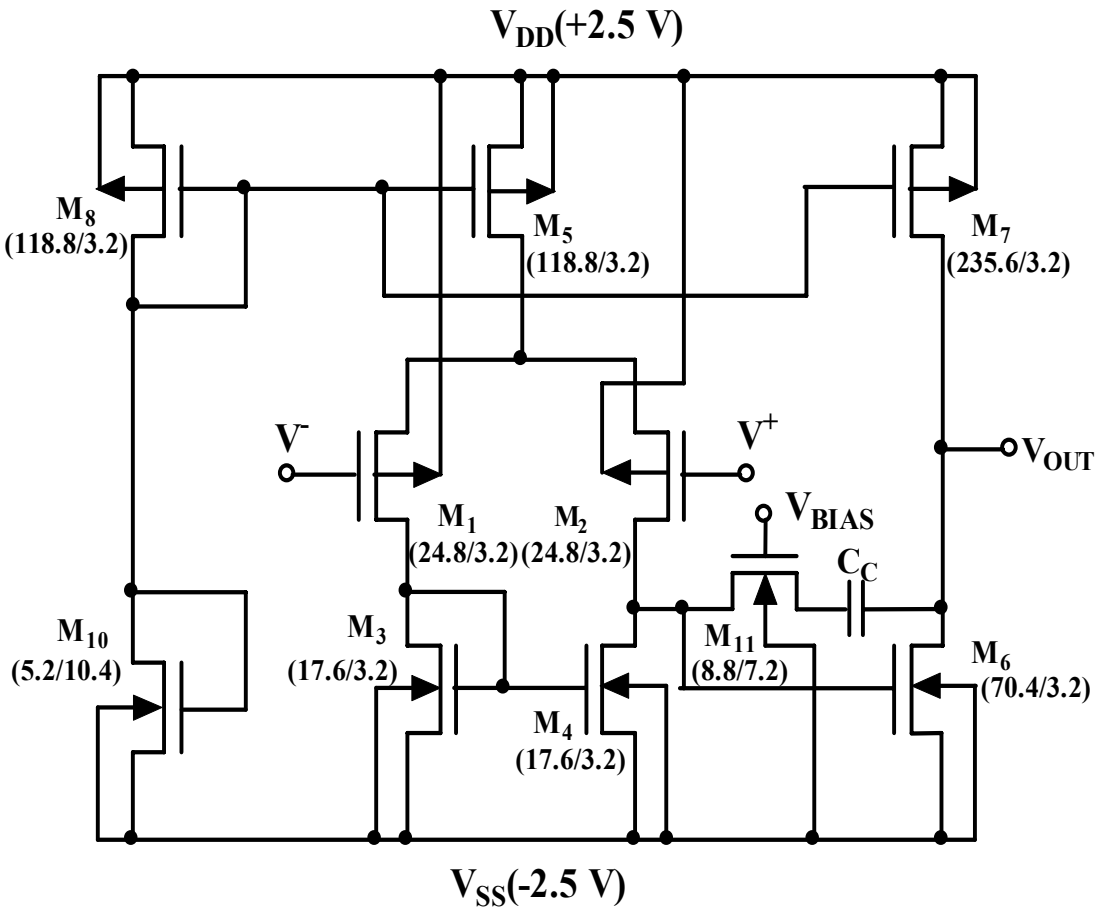
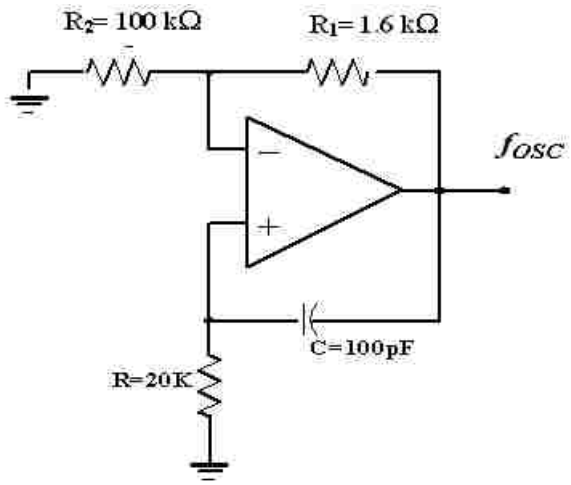
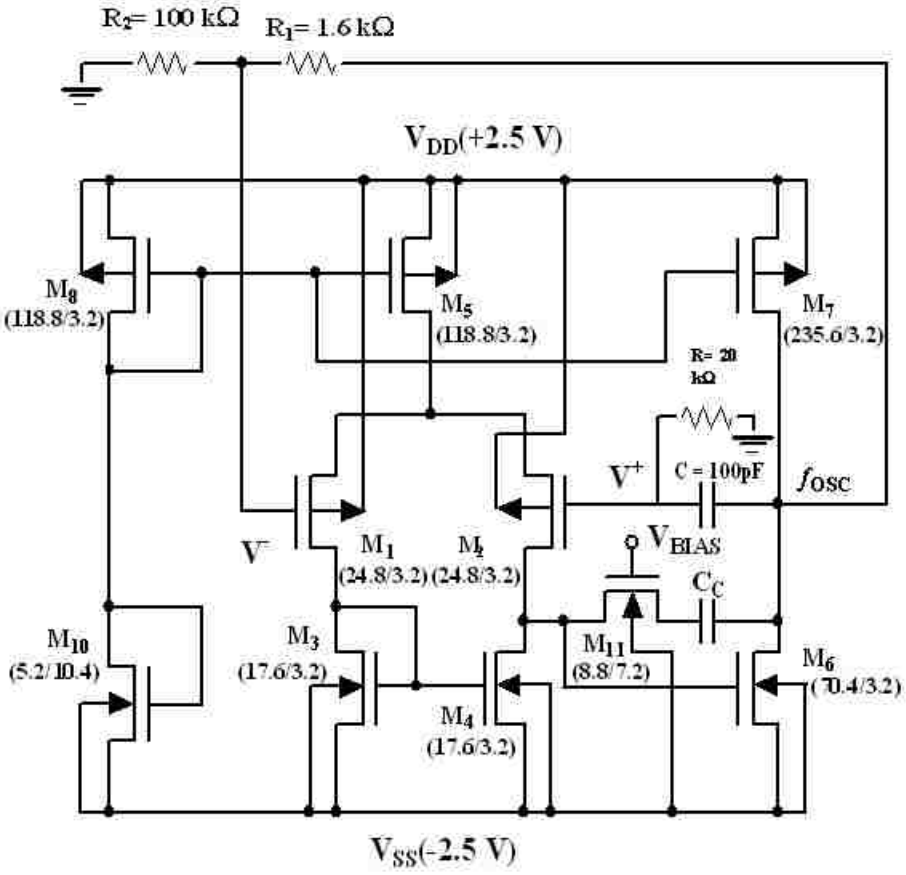


Figure 4.1: A two-stage CMOS operational amplifier circuit [103].



(a)



(b)

Figure 4.2: (a) A second order oscillator and (b) a CMOS oscillator circuit configured from Figure 4.2(a) [103].

$$A_V(s) = \frac{a_V(s)}{\{1 + a_V(s) f(s)\}} \tag{4.1}$$

where $a_V(s)$ the approximated single pole transfer is a function of the compensated operational amplifier and is given by

$$a_V(s) = \frac{a_V}{\left(1 - s/p_1\right)} \cong \frac{-a_V p_1}{s}, \tag{4.2}$$

assuming $s/p_1 >> 1$ for high frequencies.

The feedback function $f(s)$ is the net negative feedback and is given by

$$f(s) = G - \left(\frac{-s/p_2}{1 - s/p_2} \right), \tag{4.3}$$

where G is a constant and is given by

$$G = \frac{R_2}{R_2 + R_1} \quad \text{and} \quad p_2 = -1/RC. \tag{4.4}$$

Substituting *f(s)* and G from Eq. (4.3) and Eq. (4.4) in Eq. (4.1) and using Eq. (4.2), we obtain,

$$A_V(s) = \frac{a_V p_1 (p_2 - s)}{[s^2 + \{(1-G)a_V p_1 - (p_1 + p_2)\} + (G a_V p_1 p_2 + p_1 p_2)]} \tag{4.5}$$

The poles for the transfer function described by Eq. (4.5) are obtained by equating its denominator to zero. In order for the circuit to oscillate with constant amplitude, the poles must be placed on the imaginary (jω) axis. In practice, the poles must be placed on the right half of the s-plane. For the poles to be placed in the right half of the s-plane,

$$G \geq 1 - \frac{(p_1 + p_2)}{a_V p_1}. \tag{4.6}$$

With $G = 1 - \frac{(p_1 + p_2)}{a_V p_1}$, i.e., for the imaginary axis of s-plane, the natural frequency of oscillation (ω_{osc}) can be described by,

$$\omega_{OSC}{}^2 = G a_V p_1 p_2 + p_1 p_2 = a_V p_1 p_2 - p_2{}^2. \tag{4.7}$$

4.3 I_{DDQ} Testing Using BICS

Figure 4.3 shows the circuit diagram of a BICS integrated with the CUT. It is inserted in series with GND or V_{SS} line of the CUT [86, 113]. It consists of a current differential amplifier (M_2, M_3) and two current mirror pairs (M_1, M_2 and M_3, M_4). The n-MOS current mirror (M_1, M_2) is used to mirror the current from the constant current source which is used as the reference current I_{REF} for the BICS. The current mirror (M_3, M_4) is used to mirror the difference current (I_{DEF}-I_{REF}) to the current inverter, which acts as a current comparator. The differential pair (M_2, M_3) calculates the difference current between the reference current I_{REF} and the defective current I_{DEF} from the CUT. Therefore, $I_{D3} = I_{DEF}$-I_{REF}. The BICS takes into consideration the normal power supply quiescent current of 374 μA of the amplifier. It requires only nine transistors to generate a PASS/FAIL signal at the output. The BICS works in two modes: the normal mode and the test mode. In the normal mode, the BICS is isolated from the CUT by connecting "EXT" pin to V_{SS} so that the operation of the CUT is not affected by the BICS. Since one leg of the current mirror in BICS is connected to V_{SS} during normal mode their will be no effect of reference current on the circuit. In the test mode, BICS is enabled by connecting V_{ENABLE} to V_{SS} and "EXT" is floating. In the test mode, when

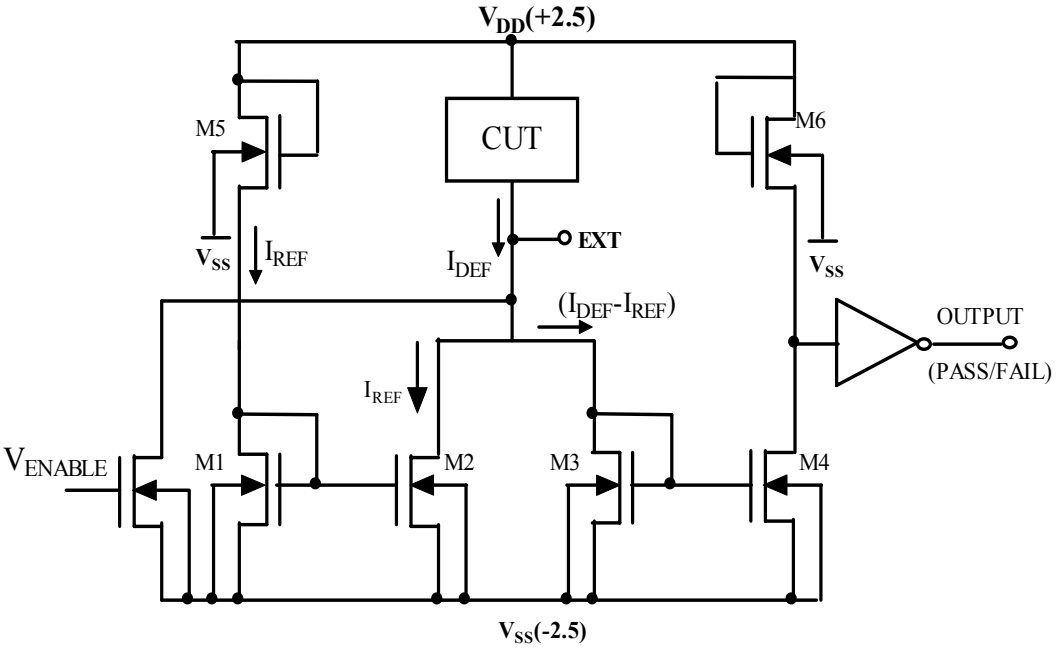


Figure 4.3: CMOS BICS and the CUT.

the current from CUT (I_{DEF}) which is the quiescent current (I_{DDQ}) is greater than the reference current (I_{REF}), the current differential amplifier calculates the difference (I_{DEF}-I_{REF}) and the output signal PASS/FAIL is set to logic HIGH, which indicates the existence of defects. When the quiescent current is less than the reference current, the output signal PASS/FAIL is set to logic LOW which indicates the non-existence of defects

4.4 I_{DDT} Testing

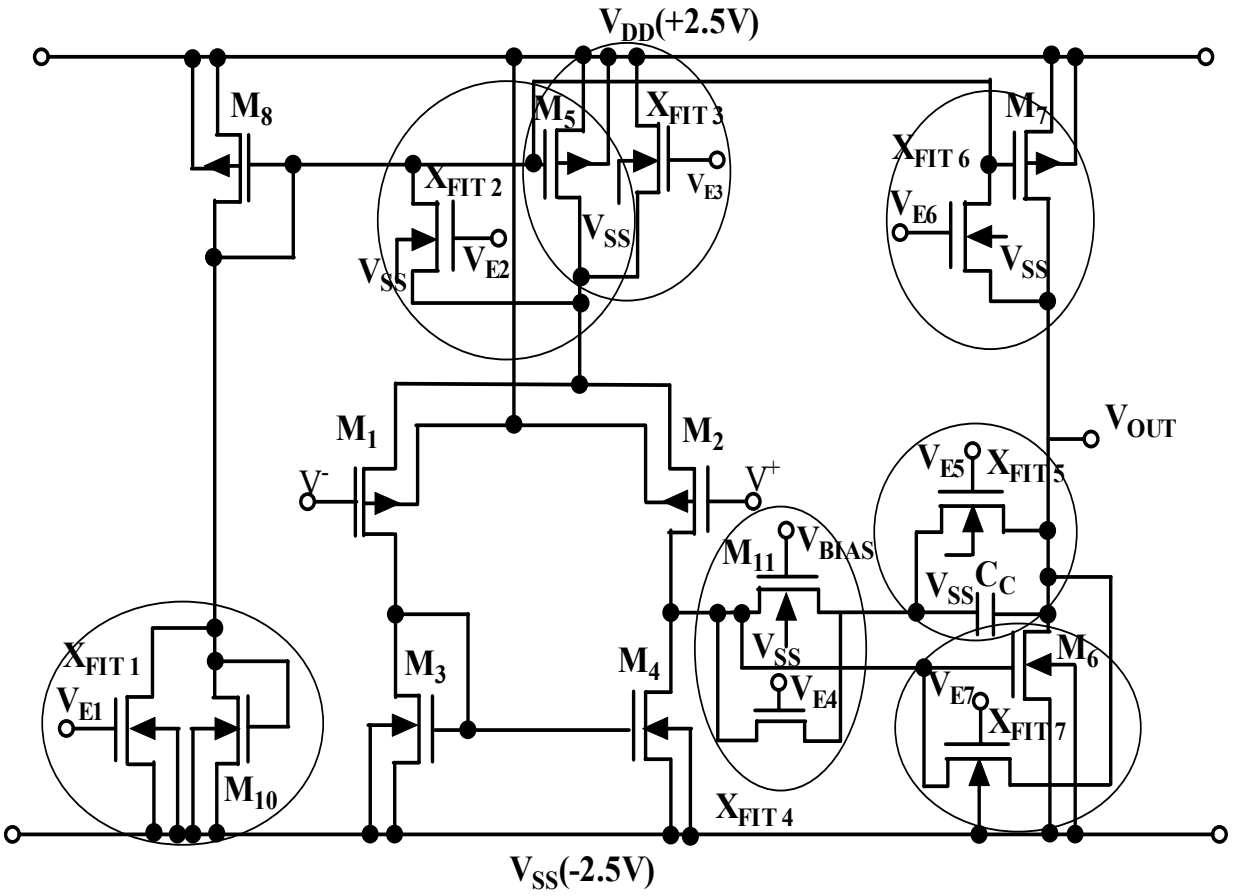
In analog circuits, the power supply current is a function of input signal, state of the circuit (faulty or faulty free) and value of the parameters of the circuit. The presence of fault in the circuit causes some degree of change in currents in some branches. Those changes in branch currents will result in a more or less significant change in the power supply current [114]. In the present work, the ac ripple in the power supply current, $I_{DDT,}$ passing through V_{DD} under the application of an ac input stimulus is measured to detect injected faults in the CUT. A small resistor is used to measure the voltage corresponding to the power supply current. The resistor does not affect the performance of the CUT.

Power supply current through V_{DD} is measured with and without injected faults with a periodic pulse input. Input signal to the CUT should produce a noticeable amount of difference between the power supply current of each faulty case and fault-free case. In the present work, the tolerance limit for the magnitude of I_{DDT} with no injected faults is defined as ±5%, such that it will take into account the deviations of significant technology and design parameters. The magnitude of power supply current, I_{DDT} is determined with every injected fault. If the simulated I_{DDT} value falls out of the tolerance limit the fault is detected.

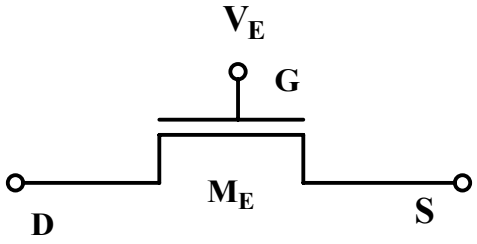
4.5 Combined Oscillation and I_{DDQ} Test Methodology

Figure 4.4 (a) shows the CMOS amplifier circuit of Figure 4.1 with fault-injection transistors (FITs) simulating manufacturing defects. Figure 4.4 (b) shows a simple fault-

injection transistor [86, 97]. The fault injection transistors are activated by connecting the gate of the transistors to V_{DD}. The use of a fault-injection transistor for the fault simulation prevents permanent damage to the operational amplifier by introduction of a physical metal short. All fault injection transistors embedded are of uniform size 4.5um/1.6um. Eight faults have been introduced into the amplifier circuit of Figure 4.4 (a). Seven faults are injected into the amplifier using fault injection transistors and the eighth fault which is an open fault is introduced by connecting the gate of transistor M_{11} to $V_{SS.}$ The injected faults in the amplifier are as follows: Fault-1: M_{10} drain-source short (M10DSS), Fault-2: M_5 gate-drain short (M5GDS), Fault-3: M_5 drain-source short (M5DSS), Fault-4: M_{11} drain-source short (M11DSS), Fault-5: compensation capacitor short (CCS), Fault-6: M_7 gate-drain short (M7GDS), Fault-7: M6 gate-drain short (M6GDS) and Fault-8: M_{11} gate to V_{SS} ($M11GV_{SS}S$). Figure 4.5 and Figure 4.6 shows the layout and microphotograph of the fabricated chip. Figure 4.7 shows the measured gain versus frequency dependence behavior of the CMOS amplifier circuit. It can be observed from Figure 4.7 that the open loop gain has increased from 65.4 dB at 300 K to 69.2 dB at 77 K and the 3 dB bandwidth of the amplifier has increased from 3.5 kHz at 300 K to 9.5 kHz at 77 K. The amplifier circuit of Figure 4.4 (a) has been converted into an oscillator circuit according to Figure 4.2 (b) and has been simulated in SPICE for the injected oscillation-based faults. The Fast-Fourier Transform (FFT) analysis has been performed to determine the natural oscillation frequency and is shown in Figure 4.8. The natural oscillation frequency of the CUT oscillator is 875 kHz at 300 K and 1.858 MHz at 77 K. Figure 4.9 shows the Monte-Carlo simulated results of the parametric (threshold-voltage, V_{th} of the CUT transistors, R_1, R_2, R, C) tolerances (5%) gives a deviation of [-2.91%, 3.79%] at 300 K and [-3.12%, 4.95%] at 77 K from their respective



(a)



(b)

Figure 4.4: (a) Injected I_{DDQ} and oscillation testable faults. Note: X_{FIT} is an n-MOS fault-injection transistor. $X_{FIT\ 1}$ and $X_{FIT\ 3}$ are I_{DDQ} testable faults. $X_{FIT\ 1\text{-}7}$ are oscillation testable faults and (b) fault-injection transistor (FIT).

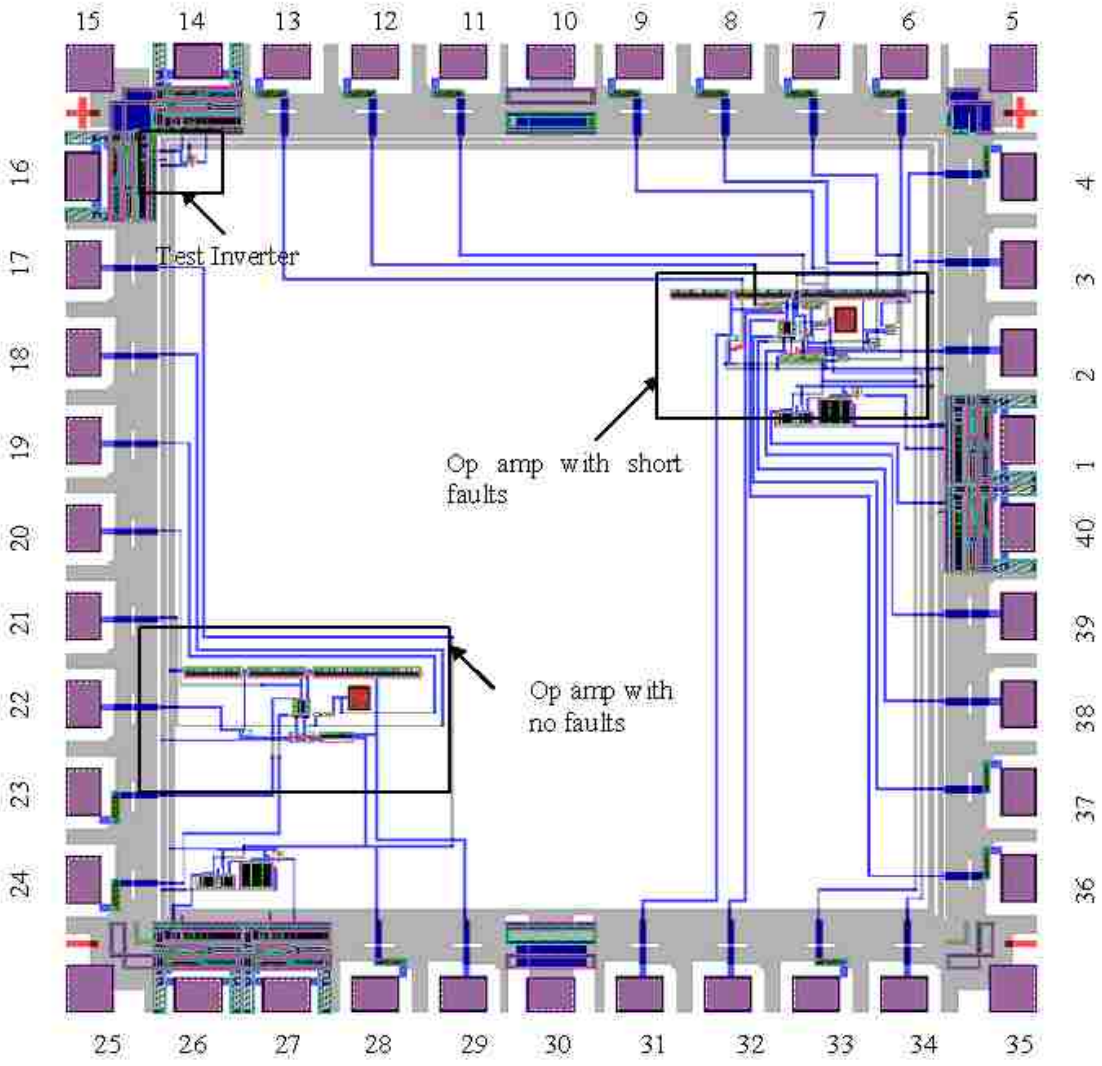


Figure 4.5: Layout of the fabricated CMOS chip [103].

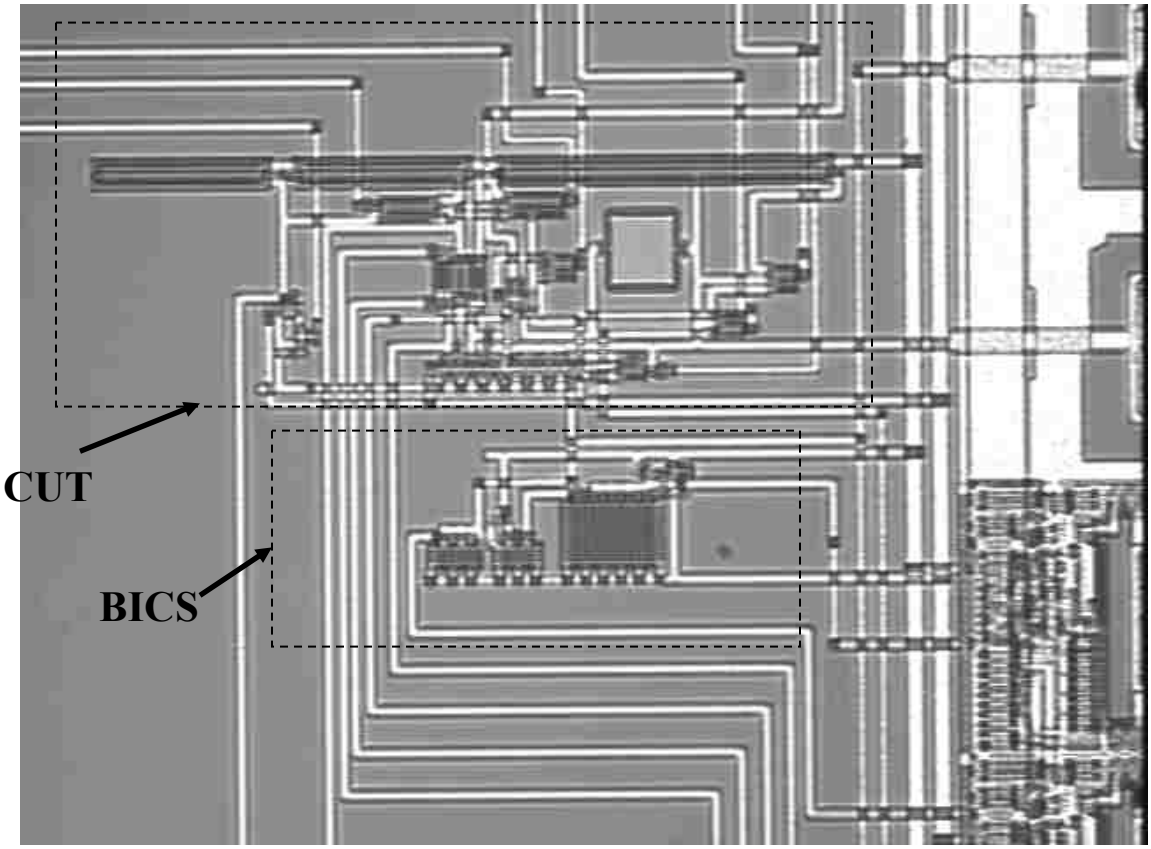


Figure 4.6: Microphotograph of the fabricated CMOS chip [103].

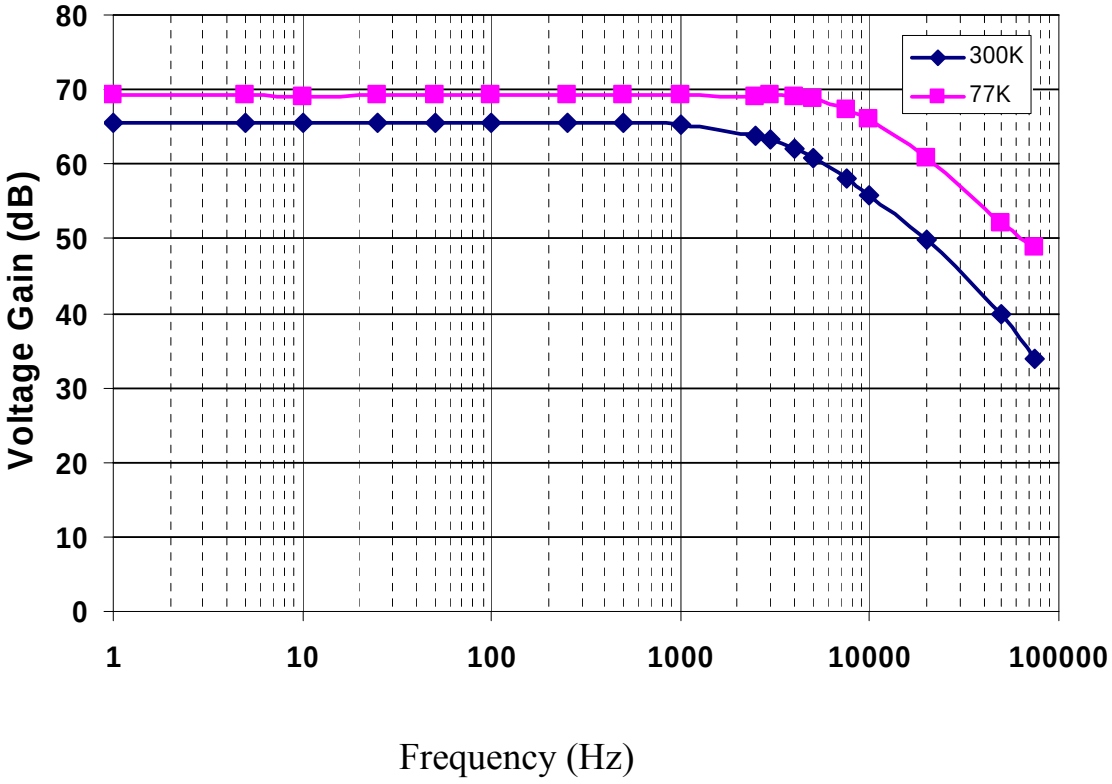


Figure 4.7: Measured gain versus frequency response characteristics of the fabricated CMOS amplifier circuit.

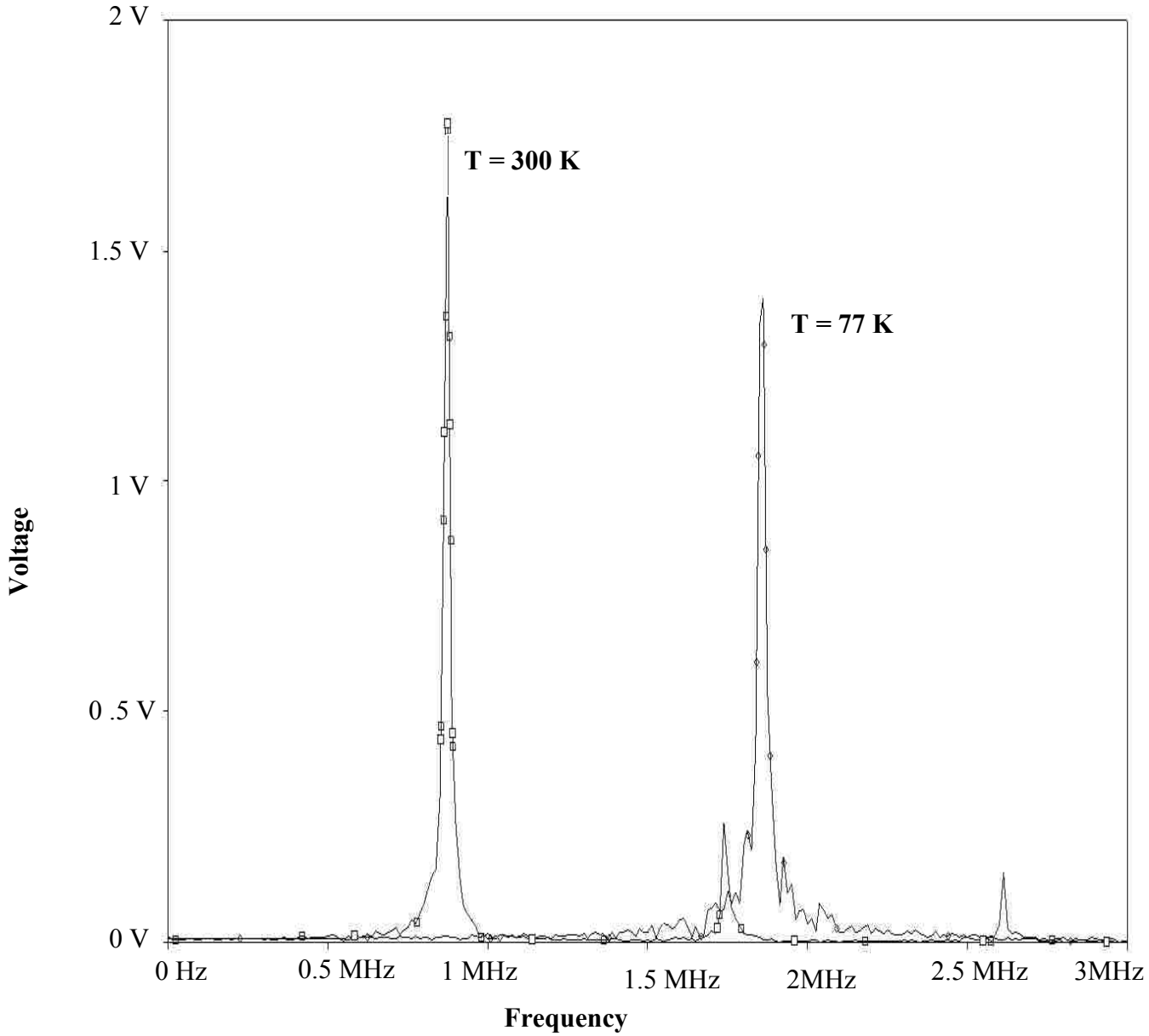


Figure 4.8: FFT analysis of the output signal from the circuit of Figure 4.2 (b) for determining natural oscillation frequency.

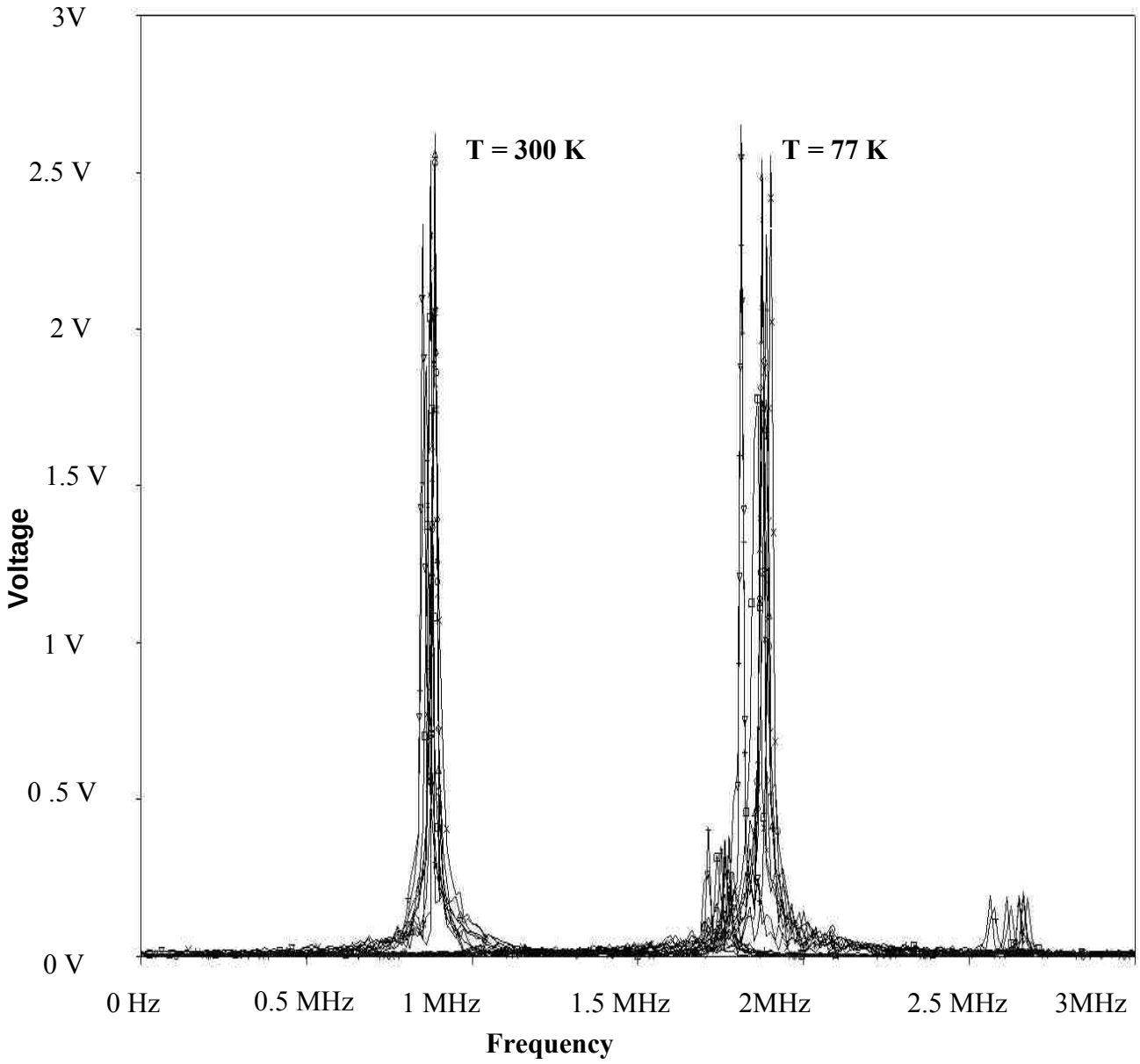


Figure 4.9: Monte-Carlo analysis of the parametric tolerances of the oscillator circuit of Figure 4.2 (a). Note: Range of frequencies: (Tolerance band: [-2.91%, 3.79%] at 300 K and [-3.12%, 4.95%] at 77 K). Tolerance band is calculated as follows:

Min = $(f_{MIN} - f_{NAT})/ f_{NAT}$
Max = $(f_{MAX} - f_{NAT})/ f_{NAT}$
f_{MIN} = Upper limit of minimum acceptable frequency in Monte-Carlo analysis
f_{MAX}= Lower limit of maximum acceptable frequency in Monte-Carlo analysis

natural oscillation frequencies. This can be seen as result of increased gain and bandwidth of the amplifier at 77 K compared to 300 K and suppression of the subthreshold current.

Table 4.1 summarizes the measured natural oscillation frequency and oscillation frequency due to faults at 300 K and 77 K. Table 4.2 summarizes the deviation in measured frequency due to injected faults. As the deviation of the frequency due to faults lie beyond the limit calculated by Monte-Carlo simulation, we can conclude that all the injected faults except the open fault have been detected by the oscillation testing at 300 K. All the faults which have been detected at 300 K have been also detected at 77 K. The open fault (Fault-8) which was not detected at 300 K was detected at 77 K as shown in Table 4.2. This demonstrates improved fault detection at 77 K. Table 4.3 summarizes the simulated and experimental I_{DDQ} results for Faults 1-8 and the corresponding PASS/FAIL signal through the BICS output. Table 4.3 includes only 300 K testing results since there is no observed difference in I_{DDQ} testing results at 300 K and 77 K. It can be noticed from Table 4.3 that only two faults (Faults – 1 and 3) out of seven injected faults could be detected by I_{DDQ} testing. Figures 4.10 (a) and (b) and Figures 4.11 (a) and (b) show the measured PASS/FAIL signal from the BICS output under fault-injection conditions corresponding to one of the faults M10DSS (Fault-1) at 5 KHz and 1 MHz, respectively, obtained from HP1660CS Logic Analyzer. Logic HIGH indicates a FAIL signal. The output signal PASS/FAIL set to logic HIGH indicates the existence of the fault while the output signal PASS/FAIL set to logic LOW indicates the non-existence of the fault which implies that the fault is not detectable. Similarly other injected faults were also tested. In Table 4.3, PASS refers to a fault detection and FAIL to a non-detectable fault.

Table 4.1: Measured oscillation frequencies

Fault type	**Oscillation Frequency (kHz) at T = 300 K**	**Oscillation Frequency (kHz) at T = 77K**
No faults	324	489
Fault -1 (M10DSS)	400	616
Fault-2 (M5GDS)	69	-
Fault-3 (M5DSS)	410	600
Fault-4 (M11DSS)	277	471
Fault-5 (CCS)$^{+}$	-	-
Fault-6 (7GDS)$^{+}$	-	-
Fault-7 (M6GDS)$^{+}$	-	-
Fault-8($M11GV_{SS}$)	319	563

$^{+}$Loss of oscillation

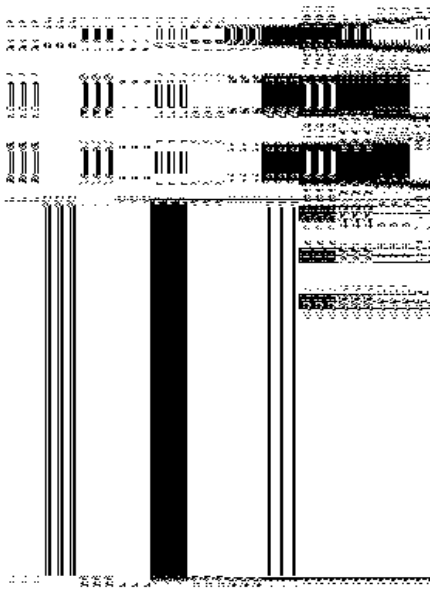
Table 4.2: Measured frequency deviations under fault-injections

Fault injected	**Deviation from natural f_{osc} (T=300 K)**	**Deviation from natural f_{osc} (T=77 K)**
Fault-1	+23.21	+25.85
Fault-2	-78.66%	Loss of oscillation
Fault-3	+26.3%	+22.46%
Fault-4	-14.6%	-3.8%
Fault-5	Loss of oscillation	Loss of oscillation
Fault-6	Loss of oscillation	Loss of oscillation
Fault-7	Loss of oscillation	Loss of oscillation
Fault-8	-1.58%	+7.5%

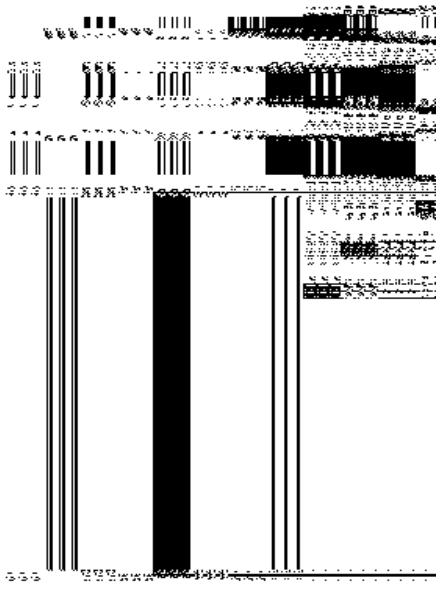
Table 4.3: Simulated and experimental BICS output.

Faults	**Simulated BICS Output (5 KHz) PASS/FAIL**	**Experimental BICS Output (5 KHz) PASS/FAIL**	**Simulated BICS Output (1 MHz) PASS/FAIL**	**Experimental BICS Output (1 MHz) PASS/FAIL**
Fault-1	PASS	PASS	PASS	PASS
Fault-2	FAIL	FAIL	FAIL	FAIL
Fault-3	PASS	PASS	PASS	PASS
Fault-4	FAIL	FAIL	FAIL	FAIL
Fault-5	FAIL	FAIL	FAIL	FAIL
Fault-6	FAIL	FAIL	FAIL	FAIL
Fault-7	FAIL	FAIL	FAIL	FAIL
Fault-8	FAIL	FAIL	FAIL	FAIL

PASS: Fault detectable
FAIL : Fault not detectable

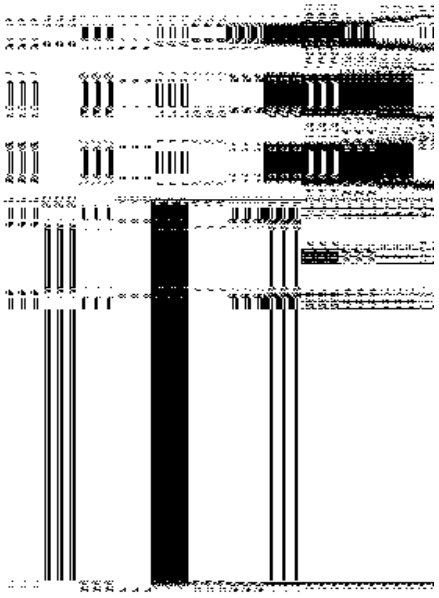


(a)

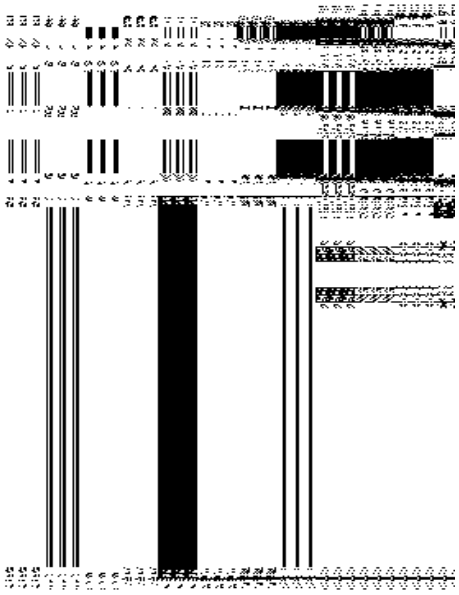


(b)

Figure 4.10: BICS showing PASS/FAIL output from HP1660CS Logic Analyzer corresponding to a fault M10DSS.
(a) V_{ENABLE} and V_{ERROR} connected to 5 kHz signal at 300 K.
(b) V_{ENABLE} and V_{ERROR} connected to 5 kHz signal at 77 K.



(a)



(b)

Figure 4.11: BICS showing PASS/FAIL output from HP1600CS Logic Analyzer corresponding to a fault M10DSS.
(a) V_{ENABLE} and V_{ERROR} connected to 1 MHz signal at 300 K.
(b) V_{ENABLE} and V_{ERROR} connected to 1 MHz signal at 77 K.

Figure 4.12 shows the post-layout simulation results of I_{DDQ} testing corresponding to following two detected faults: Fault-1 and Fault-3 [103]. The fault free I_{DDQ} is approximately 374 μA at 300 K and 371 μA at 77 K. The difference in I_{DDQ} at 300 K and 77 K is marginal due to large size of MOS transistors in CMOS amplifier circuit of Figure 4.3 (a). The faulty current, which the BICS detects, is nearly equal to or greater than 410μA. Thus, the designed BICS has a resolution of nearly of 70 μA. The BICS has been designed to be sensitive for a wide range of faulty currents. As such the Fault-1 (M10DSS) provides a large current of 869 μA while the Fault-3 (M5DSS) provides a current of 444 μA as shown in Figure 4.12. A combination of these two faults provides a current of 940 μA Here the results are shown for only two faults for demonstration of the method used. Similarly the method was tested for remaining faults which were found to be non-detectable contrary to oscillation-based testing. The reason is that the fault free I_{DDQ} was chosen approximately to 371-374 μA which is on the higher side. This estimation of I_{DDQ} did not allow BICS to detect other faults.

Figure 4.13 shows an influence of BICS on V_{SS} [103]. The virtual $-V_{SS}$ is not at -2.5 V in test mode. The virtual $-V_{SS}$ is at -2.47V for V_{ENABLE} HIGH (BICS- shorted) and -2.11 V for V_{ENABLE} LOW (BICS- active).

4.6 Combined I_{DDT}, Oscillation and I_{DDQ} Test Methodology

The combined test methodology has been applied to an op-amp with floating gate inputs. The schematic of the op-amp with floating gate input which is used as CUT is shown in Figure 4.14 [104, 115]. The amplifier has been designed in 1.5 μm n-well CMOS process. The floating gate transistor uses 512 fF capacitor each at its input which has been designed in an integer multiple of 256 fF unit size capacitor. The capacitors have been designed using two poly layers: poly 1 and poly 2. The capacitors are surrounded with dummy capacitors

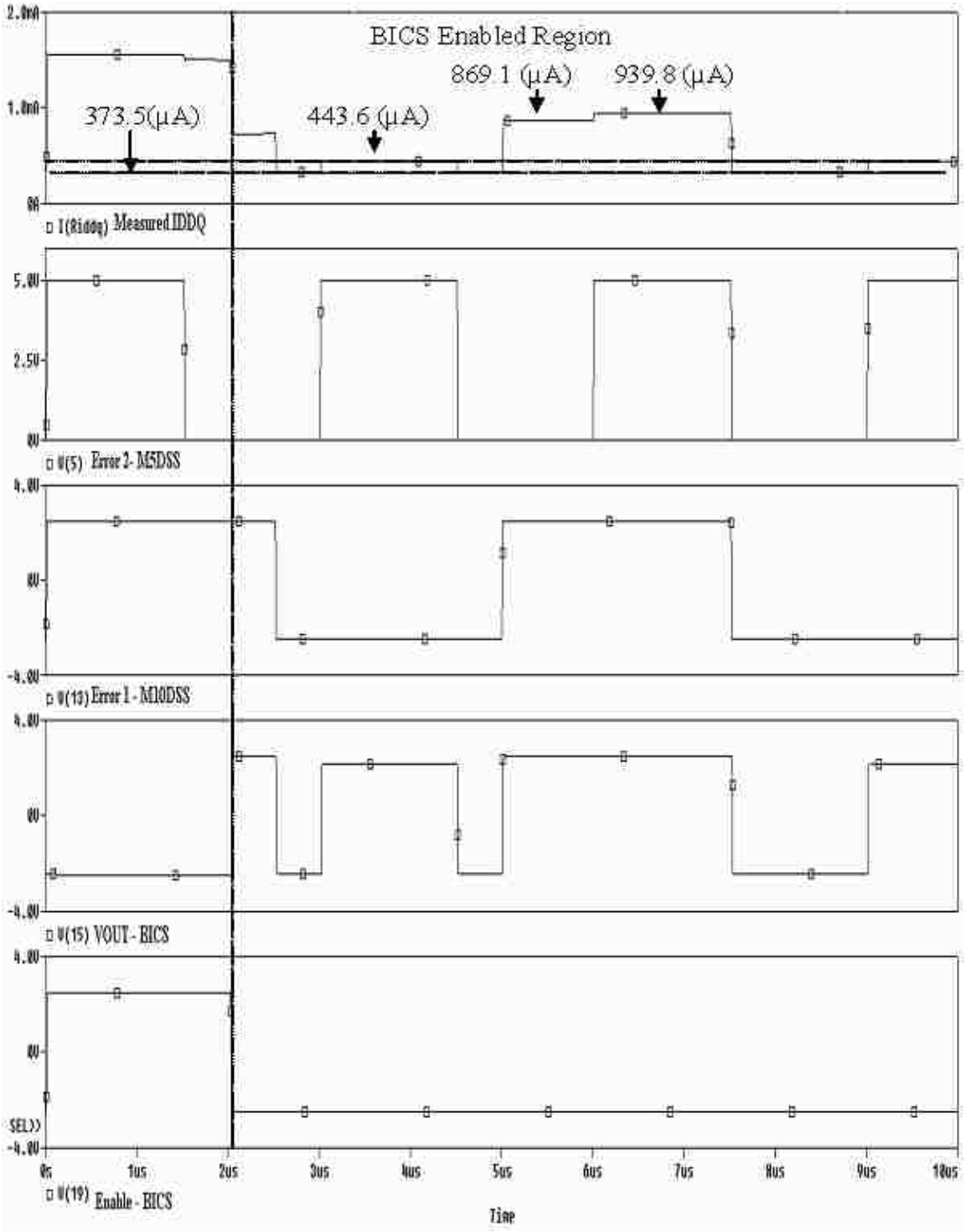
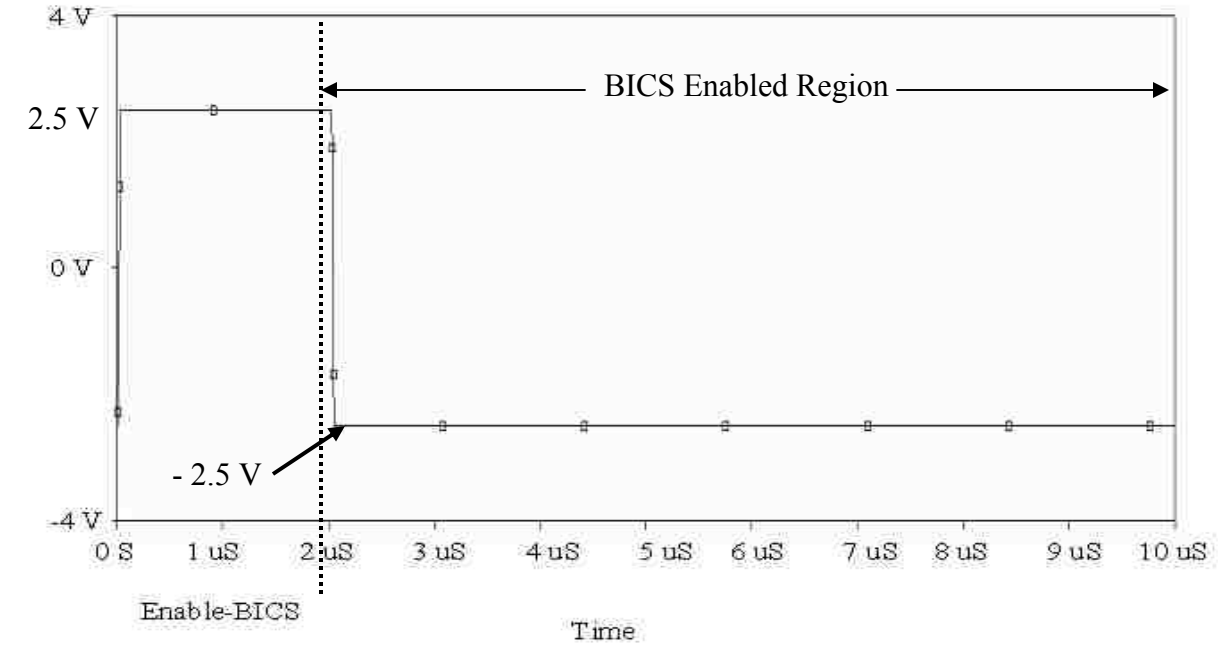
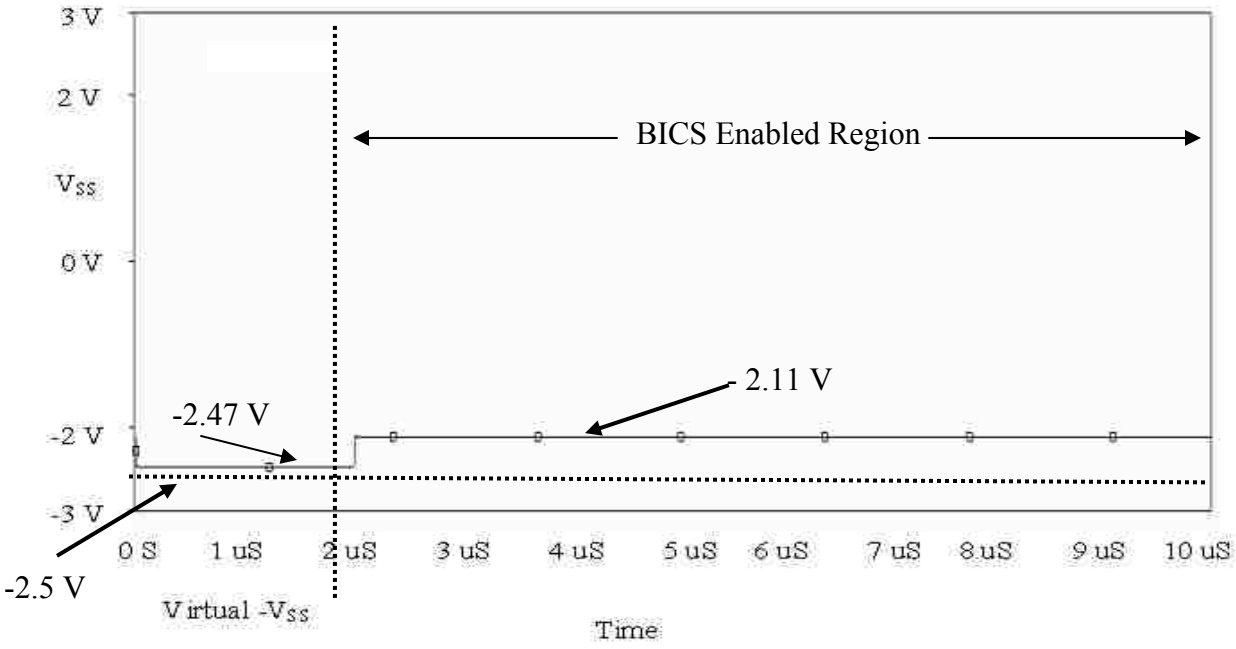


Figure 4.12: Simulated I_{DDQ} of the circuit of Figure 4.4. Note: 77 K plot is nearly same and differs marginally from 300 K plot.



(a)



(b)

Figure 4.13: Influence of BICS on V_{SS}. Note: There is insignificant difference between plots at 300 K and 77 K.
(a) BICS enable signal.
(b) Voltage at point EXT of the circuit of Figure 4.3.

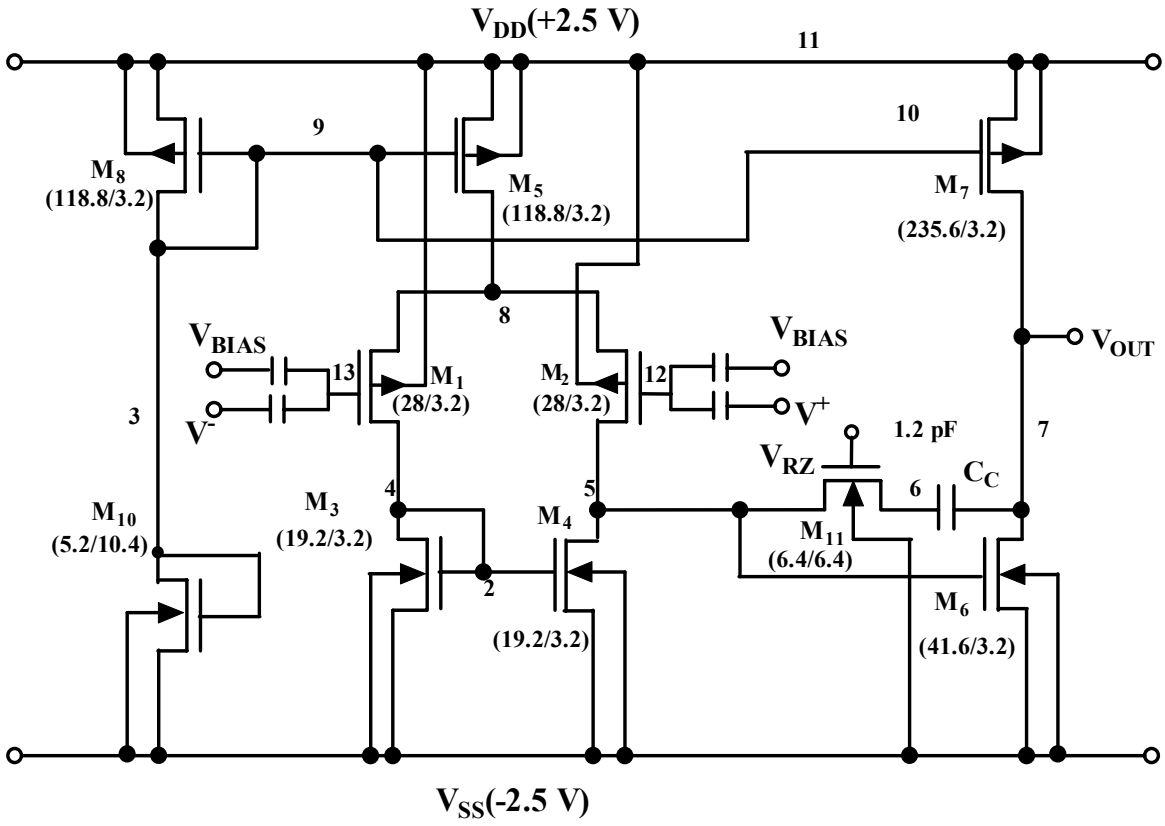


Figure 4.14: A two stage floating gate input CMOS op-amp [104].

and guarded by the n^+ - guard ring in n-well to minimize parasitic capacitances. A common centroid layout scheme is employed in the design.

In CUT, the faults simulating possible manufacturing defects have been introduced using the fault injection transistors [86, 97]. The existence of short fault between two nodes is represented as $S_{a, b}$ where subscripts a and b denote the corresponding node numbers. The open fault (broken wire) is represented as O_a , where the subscript a denotes the node number. The faults under consideration are gate-drain shorts, broken wires, floating gates, drain-source shorts, compensation capacitor short and short circuit between different nodes. We have considered CUT with only short faults and considered combined short and open faults separately. Figure 4.15 and Figure 4.16 show the layout of op-amp designs with short faults and combined open and short faults, respectively [104]. Figure 4.17 shows the part of the corresponding microphotographs of the fabricated floating gate input op-amp designs [115].

The circuit of Figure 4.14 is simulated in SPICE using MOS level 3 model parameters [116] for the three testing methods. In oscillation test method, Fast-Fourier Transform (FFT) analysis has been performed on the oscillator circuit of Figure 4.18 to determine the natural oscillation frequency. The simulated natural oscillation frequency of the CUT as an oscillator is 7 kHz and 2.3 kHz for short and combined open and short faults, respectively. Experimental measurements are performed with R=36 kΩ, R_1=400 Ω R_2=71 kΩ and C=0.1 μF for short faults (Figure 4.15) and R=60 kΩ, R_1=1.8 kΩ, R_2=153 kΩ and C=0.1 μF for combined short and open faults (Figure 4.16).

A 1 kHz 4V peak-to-peak input pulse is applied to the CUT in the power supply current based testing. This input stimulus shows significant difference in the power supply

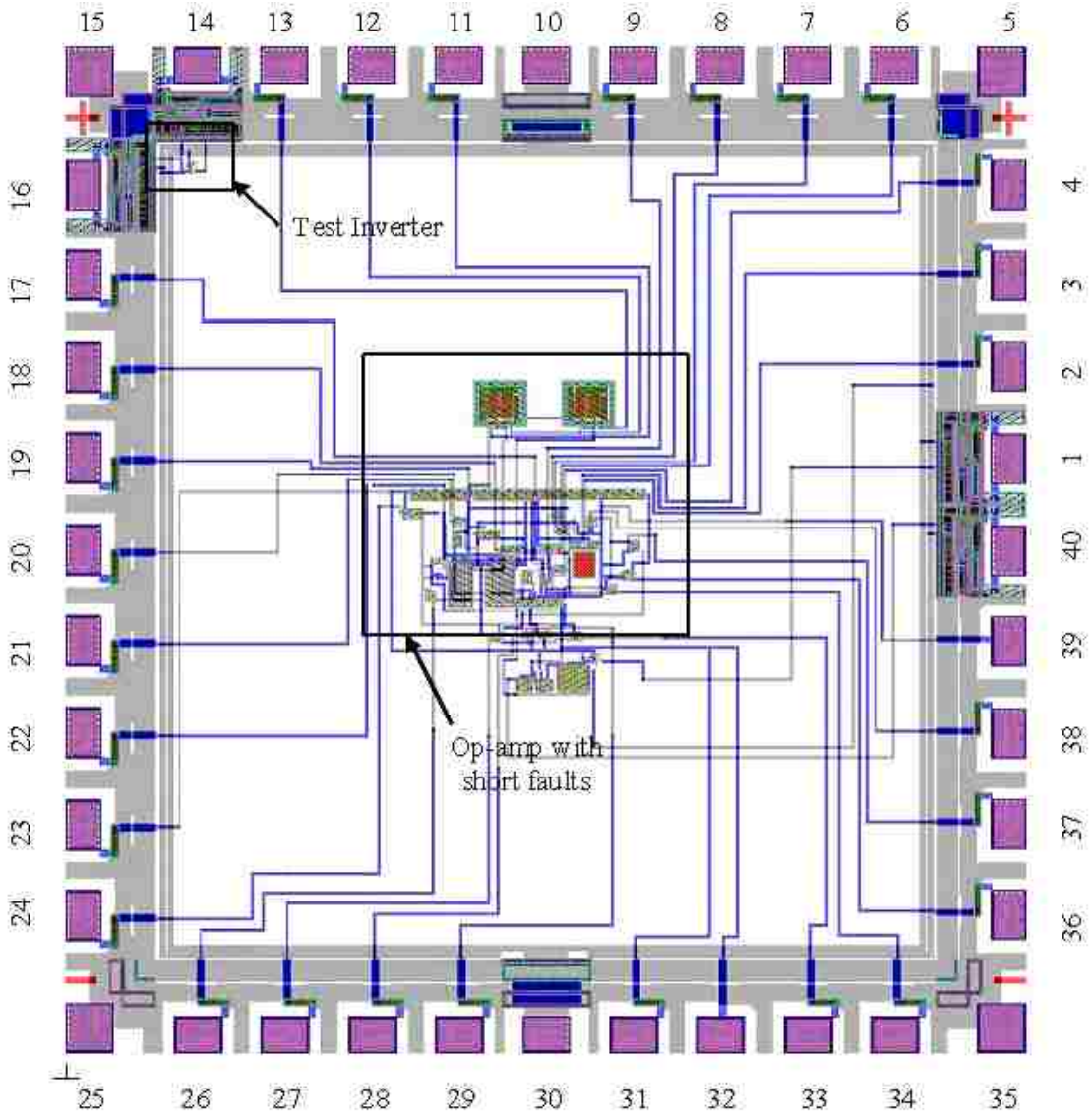


Figure 4.15: Layout for floating-gate input op-amp with only short faults.

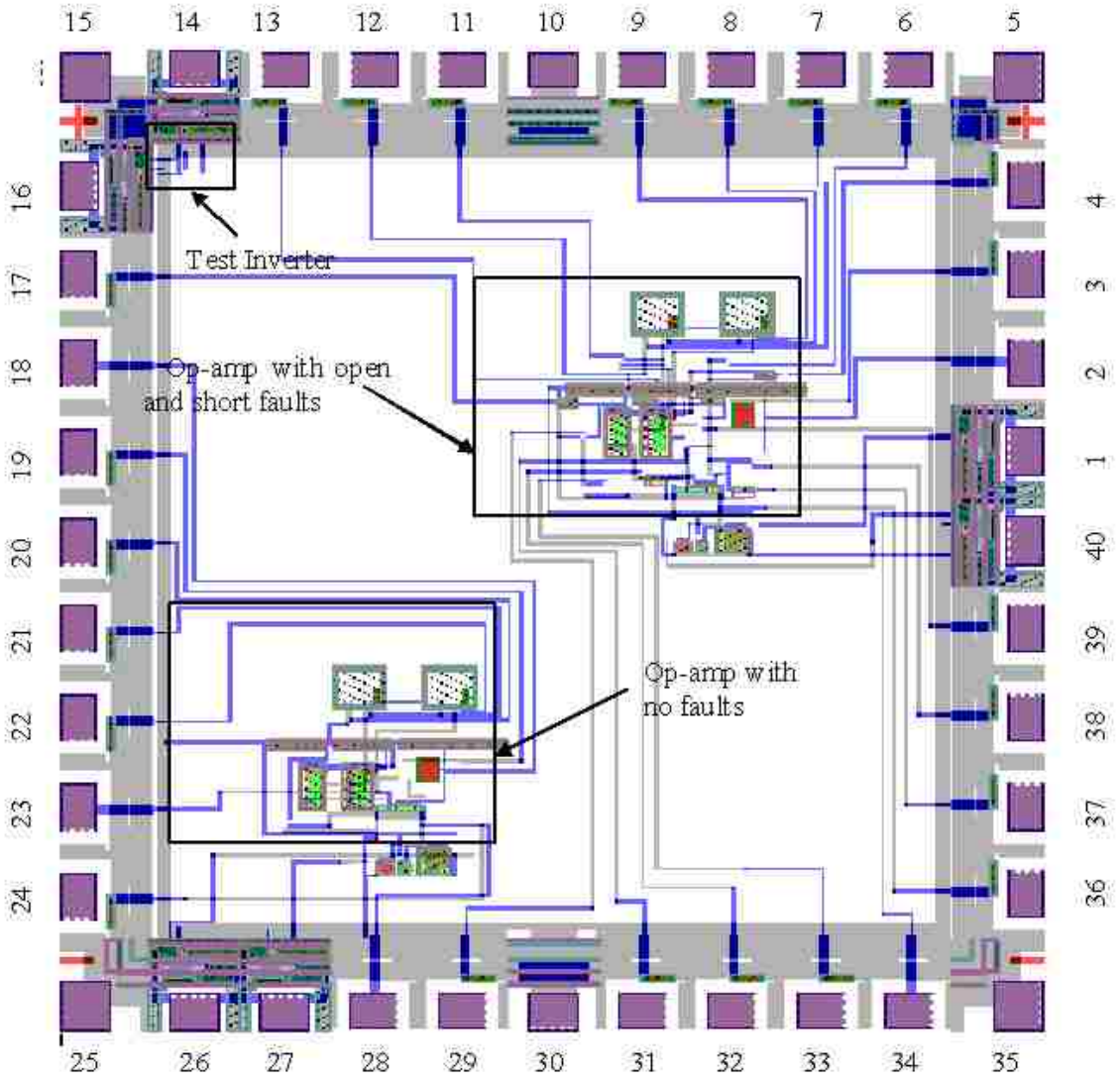
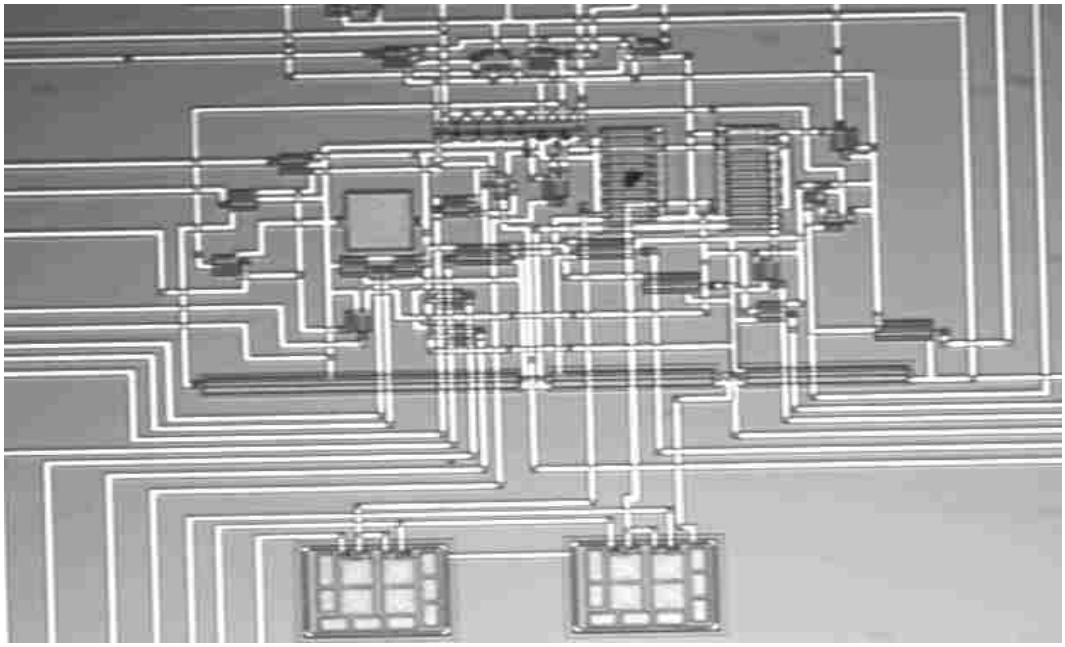
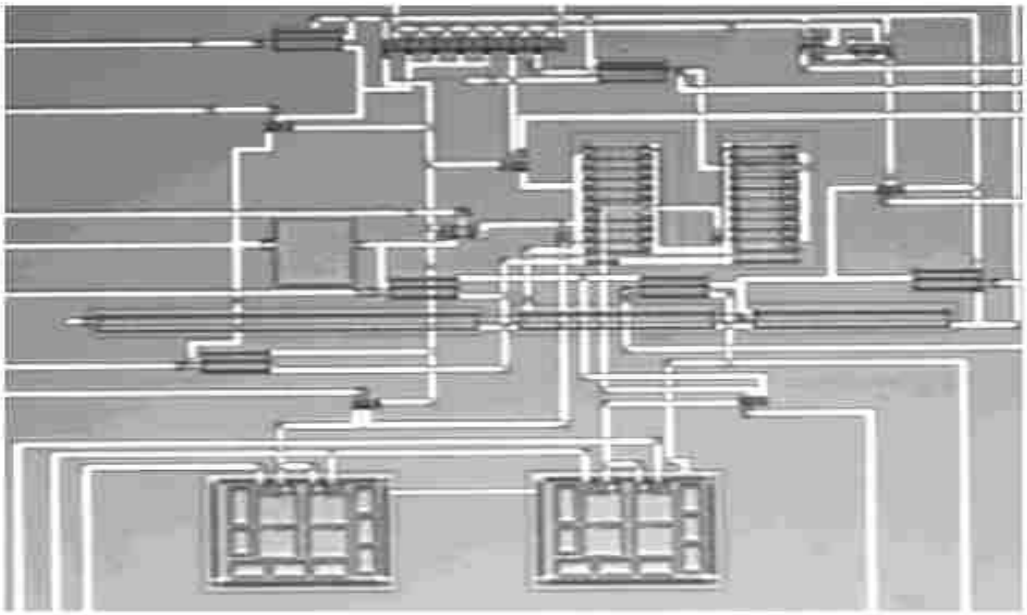


Figure 4.16: Layout of floating gate input op-amp with combined open and short faults.



(a)



(b)

Figure 4.17: Microphotograph of the fabricated design with a) short faults and b) combined open and short faults.

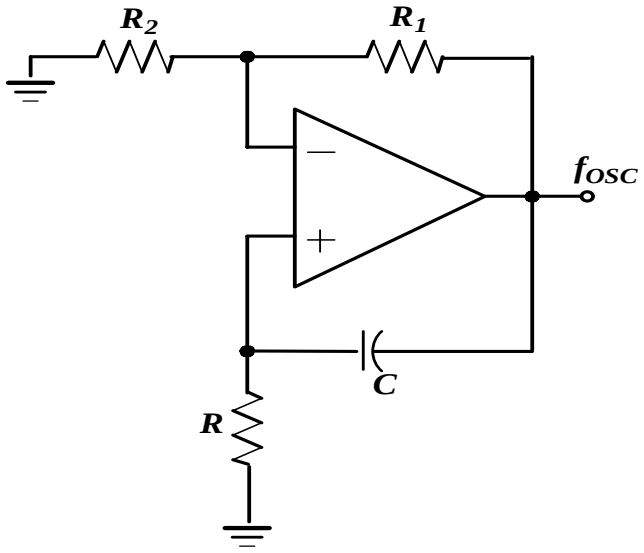


Figure 4.18: CUT as an oscillator.

current between each of the faulty case and fault-free case. The voltage, V_R is simulated and measured experimentally across a 100 Ω resistor as shown in Figure 4.19.

Table 4.4 summarizes the simulated and measured results using oscillation and I_{DDT} test methods for the floating gate input CMOS amplifier with short faults. From the SPICE simulations shown in Table 4.4, it can be observed that for the faults $S_{7,2}$ and $S_{5,6}$, the CUT oscillated with the natural frequency and hence these were not detected from simulations. However, faults $S_{7,2}$ and $S_{5,6}$ showed a large deviation from natural oscillation frequency when measured experimentally. All injected short faults have been detected experimentally using this method of testing. It is also seen from Table 4.4 that no fault I_{DDT} is 153 μA and a ±5% tolerance gives minimum and maximum I_{DDT} limits as 145 μA and 161 μA. From the simulated results of $I_{DDT,}$ injected faults $S_{7,2,}$ $S_{7,11,}$ $S_{5,6}$ and $S_{8,11}$ fall within the tolerance range and were not detected. Simulated I_{DDT} for $S_{4,1}$ is 137 μA which is close to lower tolerance limit and is considered as not detected. The experimental results closely follow the simulation results. The simulated value of I_{DDT} for $S_{1,3}$ and $S_{3,11}$ shows a large variation from fault free value but the measured I_{DDT} for these faults was not as large as shown by SPICE. The fault $S_{6,9}$ showed decrease in measured I_{DDT} where as the fault $S_{1,5}$ showed an increase. However, for faults $S_{6,9}$ and $S_{1,5}$ measured I_{DDT} for these faults was far away from the tolerance range, and faults were detected.

In the I_{DDQ} test method, PASS/FAIL signal was measured from the BICS output using a HP1660CS Logic Analyzer with every injected fault. Faults $S_{3,8,}$ $S_{1,3,}$ $S_{7,10}$ and $S_{7,11}$ were detected using this method. The fault $S_{7,11}$ did not show significant variation in I_{DDT} from the fault free case. However, it was detected by I_{DDQ} test method and oscillation test method.

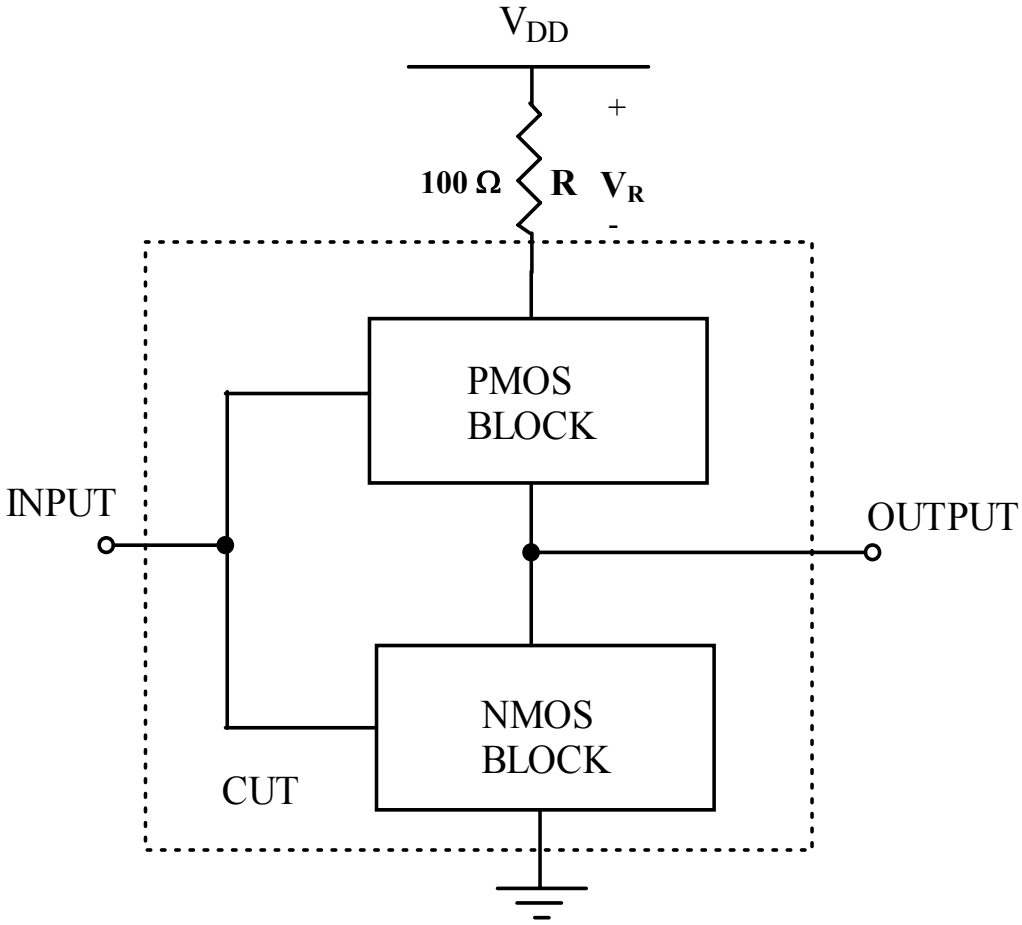


Figure 4.19: Block diagram of power supply current, I_{DDT} based testing.

Table 4.4: SPICE simulated and experimental results for CUT with only short faults

Short Faults	Oscillation Frequency (kHz)				I_{DDT} (µA)			
	SPICE	Fault detection	Exp.	Fault detection	SPICE	Fault detection	Exp.	Fault detection
No fault	7	-	5	-	153	-	154	-
$S_{3,8}$	Loss of oscillation	Yes	Loss of oscillation	Yes	190	Yes	184	Yes
$S_{4,1}$	2	Yes	1.36	Yes	137	No	130	No
$S_{4,9}$	Loss of oscillation	Yes	Loss of oscillation	Yes	88	Yes	66	Yes
$S_{8,9}$	3	Yes	1	Yes	90	Yes	68	Yes
$S_{1,3}$	3	Yes	1	Yes	670	Yes	326	Yes
$S_{3,11}$	Loss of oscillation	Yes	Loss of oscillation	Yes	940	Yes	374	Yes
$S_{1,8}$	Loss of oscillation	Yes	Loss of oscillation	Yes	0	Yes	0	Yes
$S_{2,8}$	Loss of oscillation	Yes	Loss of oscillation	Yes	0	Yes	0	Yes
$S_{2,11}$	Loss of oscillation	Yes	Loss of oscillation	Yes	20	Yes	22	Yes
$S_{5,11}$	Loss of oscillation	Yes	Loss of oscillation	Yes	71	Yes	74	Yes
$S_{5,8}$	Loss of oscillation	Yes	Loss of oscillation	Yes	0	Yes	0	Yes
$S_{1,7}$	Loss of oscillation	Yes	Loss of oscillation	Yes	0	Yes	0	Yes
$S_{7,10}$	Loss of oscillation	Yes	Loss of oscillation	Yes	206	Yes	208	Yes
$S_{7,2}$	7	No	1	Yes	153	No	140	No
$S_{7,8}$	Loss of oscillation	Yes	Loss of oscillation	Yes	0	Yes	0	Yes
$S_{7,11}$	Loss of oscillation	Yes	Loss of oscillation	Yes	152	No	140	No
$S_{6,11}$	Loss of oscillation	Yes	Loss of oscillation	Yes	74	Yes	58	Yes
$S_{5,6}$	7	No	1	Yes	152	No	140	No
$S_{8,11}$	2	Yes	1	Yes	136	No	140	No
$S_{6,8}$	Loss of oscillation	Yes	Loss of oscillation	Yes	0	Yes	0	Yes
$S_{6,9}$	Loss of oscillation	Yes	Loss of oscillation	Yes	298	Yes	64	Yes
$S_{1,5}$	Loss of oscillation	Yes	Loss of oscillation	Yes	19	Yes	44	Yes

Note : No fault I_{DDT} =153 µA. With ±5 % tolerance, I_{DDT} (minimum) =145 µA and I_{DDT} (maximum) = 161µA.

The experimental results of the combined testing methods show that all injected faults in CUT with short faults have been detected. For the combined open and short faults case, I_{DDQ} test method did not detect any of the injected faults using SPICE and experimental measurements. The possible reason could be the high resistance offered by fault injection transistors. Table 4.5 summarizes the simulated and measured results for the CUT with combined open and short faults, using oscillation and I_{DDT} test methods. Oscillation test method showed loss of oscillation for all injected open faults and short faults except for faults $S_{9,11}$ and $S_{10,11}$ which did not deviate from the natural oscillation frequency and were not detected. In oscillation test method, SPICE simulated results are in close agreement with the corresponding experimental results except for the fault $S_{3,1}$. The measured oscillation frequency for this fault is 0.9 kHz, where as it showed loss of oscillation in SPICE.

From Table 4.5 I_{DDT} current for no faults case is 120 μA. A ±5% tolerance results in a maximum and minimum I_{DDT} of 126 μA and 114 μA respectively. The SPICE simulated results in Table 4.5 show I_{DDT} = 0 μA for all injected open faults except for fault O_{12}. However, fault O_{12} showed a considerable deviation of I_{DDT} (182 μA) from the fault free case (128 μA) when measured experimentally. Hence, this fault is detected experimentally. Faults O_5 and O_7 resulted in insignificant I_{DDT} when measured experimentally and were detected by this method. From SPICE and experimental results shown inTable 4.5, faults $S_{9,11}$, $S_{10,11}$ and $S_{6,11}$ do not show much deviation from the fault free case and are not detectable with I_{DDT} test method. Faults $S_{9,11}$ and $S_{10,11}$ were not detected by the oscillation testing and faults $S_{9,11}$, $S_{10,11}$ and $S_{6,11}$ were not detected by I_{DDT} testing. Fault $S_{6,11}$ which was not detected by I_{DDT} testing was however detected by oscillation testing. All faults except faults $S_{9,11}$ and $S_{10,11}$ have been detected by the combined test methodology.

Table 4.5: SPICE simulated and experimental results for CUT with open and short faults

Open Short Faults combined	**Oscillation Frequency (KHz)**				**I_{DDT} (µA)**			
	SPICE	***Fault detection***	***Exp.***	***Fault detection***	***SPICE***	***Fault detection***	***Exp.***	***Fault detection***
No fault	2.3	-	2.3	-	120	-	128	-
O_{12}	Loss of oscillation	Yes	Loss of oscillation	Yes	120	No	182	Yes
O_{13}	Loss of oscillation	Yes	Loss of oscillation	Yes	0	Yes	0	Yes
O_3	Loss of oscillation	Yes	Loss of oscillation	Yes	0	Yes	0	Yes
O_5	Loss of oscillation	Yes	Loss of oscillation	Yes	0	Yes	18	Yes
O_7	Loss of oscillation	Yes	Loss of oscillation	Yes	0	Yes	20	Yes
$S_{9,11}$	3	No	3	No	113	No	126	No
$S_{10,11}$	3	No	3	No	113	No	126	No
$S_{2,1}$	Loss of oscillation	Yes	Loss of oscillation	Yes	0	Yes	10	Yes
$S_{3,1}$	Loss of oscillation	Yes	0.9	Yes	0	Yes	12	Yes
$S_{7,1}$	Loss of oscillation	Yes	Loss of oscillation	Yes	0	Yes	16	Yes
$S_{6,11}$	Loss of oscillation	Yes	Loss of oscillation	Yes	105	Yes	132	No
$S_{7,11}$	Loss of oscillation	Yes	Loss of oscillation	Yes	737	Yes	780	Yes

4.7 Conclusion

A method combining oscillation and I_{DDQ} testing methodologies for fault detection has been presented. A CMOS amplifier embedded with seven bridging type faults using fault injection transistors and an open fault has been used as a CUT. At 300 K, except the open fault, oscillation testing has been able to detect all seven bridging faults: M10DSS (Fault-1), M5GDS (Fault-2), M5DSS (Fault-3), M11DSS (Fault-4), CCS (Fault-5), M7GDS (Fault-6), and M6GDS (Fault-7). At 77 K, oscillation based testing detected all seven bridging faults and the open fault.

I_{DDQ} testing at 300 K and 77 K was able to detect two of the eight faults, faults-1 and 3 (M10DSS and M5DSS). However, other detectable faults could not be detected because of over estimation of I_{DDQ}. In the present work, use of the combined oscillation and I_{DDQ} testing methods have enabled simultaneous testing of manufacturing defects (bridging and open faults). The presented approach is attractive because of its simplicity and fault observability. The method can also be applied in testing of CMOS mixed-signal integrated circuits. Though 77 K testing has been used in suppressing the subthreshold current for improved fault detection, however, it can be very effective in suppressing subthreshold current (leakage current) in analog integrated circuits designed in submicron CMOS process.

The above work was extended by combining transient power supply current testing with oscillation testing and I_{DDQ} testing for fault detection. The combined test methodology was used for fault detection in an amplifier with floating gate inputs. Two designs one with short faults and other with a combination of open and short faults have been fabricated. Change in the performance of the op-amp has been studied when short faults and a combination of short and open faults are introduced using FITs. It is observed that the performance of the op-amp with open and short faults has been degraded. Experimental

results show that the combination of the three testing methods increase the efficiency of fault detection.

CHAPTER 5
CONCLUSIONS AND SCOPE FOR FUTURE WORK

In this work, the testing of CMOS analog/mixed-signal circuits using built-in-current sensors (BICS) has been presented. The testable circuits are operational amplifier, operational amplifier with floating-gate inputs, 12-bit charge scaling architecture based DAC and 12-bit recycling architecture based ADC. Fault injection transistors (FITs) have been used to introduce faults into the designed circuits. The faults introduced into the circuits replicate fabrication faults such as short and open faults. The experimentally observed results on fabricated designs are also presented and compared with simulations from SPICE.

In VLSI circuits designed in sub-micron/deep sub-micron CMOS processes, the reference I_{DDQ} is masked by the increased subthreshold (leakage) current of MOSFETs. The conventional I_{DDQ} testing has become even more difficult due to increased density of MOSFETs in VLSI circuits. To overcome the problem of leakage current in testing, two built-in current sensors based on ΔI_{DDQ} testing and test methodology combining power supply transient current, I_{DDQ} and oscillation test method are presented in this work.

The first designed ΔI_{DDQ} BICS measures difference in power supply quiescent current under the capacitive discharge voltage across the CUT for testing of physical defects such as shorts in CMOS data converter circuits. The design of BICS follows from the work of Keating and Meyer [72], off-chip Quick-Mon of [73], and Vazquez and de Gyvez [57, 58] for digital ICs. The BICS used in the present work is slightly modified for data converters using two CMOS transmission gates replacing a single p-MOSFET switch connecting CUT and V_{DD} for better isolation from V_{DD}. It can detect current to an accuracy of 0.5 μA. The data converters used as CUT are 12-bit ADC designed in 0.5μm n-well CMOS process and

tested for normal operation under fault free conditions. The ADC uses recycling architecture for design. The method of ΔI_{DDQ} testing has been combined with logic scan-path method for digital testing and fault equivalence in combination with fault injection transistors in series with resistors for introduction of a large number of faults. The combined methods have allowed introducing 520 faults in ADC with approximately 94% faults coverage in ADC and 92% in DAC, respectively from post-layout simulation experiments. A small sub-set of 5 faults were also experimentally tested from ΔI_{DDQ} method with the exception of one fault in ADC and DAC. The method also includes the effect of process variations on BICS performance by considering ±5% variation in process transconductance and threshold voltage parameters of the MOSFET. ΔI_{DDQ} testing combined with the scan-path method, fault equivalence combined with fault injection transistors technique have been very effective in testing 12-bit CMOS ADC and DAC circuits with at least 90% or more fault coverage.

In the present work, the BICS is tested experimentally on fabricated 12-bit ADC and 12-bit DAC chips for a small sub-set of injected faults. A large set of injected faults could not be tested experimentally because of limitation on chip size due to cost and number of available pins for testing. In our case it is a tiny chip in 40-pin DIP. The test results obtained from simulations are in close agreement with the corresponding experimentally measured results on fabricated chips. However, a large number of faults have been detected through post-simulation experiments using scan-path and fault equivalence methods. The flash ADC design in the present work is generic which may cause some static non-linearity in its output [110]. However, no such non-linearity is observed at the output of 12-bit ADC. This is achieved by adjusting the slew rate of op-amp circuit and speed of 3-bit flash ADC in design. The simple BICS combined with the fault injection method combined with fault

equivalence techniques and the logic scan-path can be applied in testing of mixed-signal integrated circuits designed in submicron CMOS processes.

The second designed ΔI_{DDQ} BICS is based on Keating and Meyer [72] approach for I_{DDQ} testing and is a modification of MEAS block of ΔI_{DDQ} BICS by Vazquez and de Gyvez [57, 58]. The BICS uses the voltage controlled oscillator where frequency as its output is used as a curser for detecting faults. A CUT with ±10% deviation from the reference frequency is considered as faulty. The circuit under test is a 12-bit digital-to-analog converter which is designed in 0.5 μm n-well CMOS process. Eight faults were injected using fault injection transistors simulating manufacturing defects. These faults were injected in CMOS devices and randomly distributed. All eight faults were detected using the BICS. The faults were limited to eight because of the tiny chip limited in size (2.2 x 2.2 mm^2). The method can be applied in testing of other CMOS mixed-signal VLSI circuits such as sigma-delta modulators, PLL etc.

A method combining oscillation and I_{DDQ} testing methodologies for fault detection has been presented. A CMOS amplifier embedded with seven bridging type faults using fault injection transistors and an open fault has been used as a CUT for applying combined oscillation and I_{DDQ} test methodoly. The amplifier was designed for operation at ± 2.5 V in a standard 1.5 μm n-well CMOS process. An on-chip BIC has been integrated to monitor I_{DDQ} of the CUT. At 300 K, except the open fault, oscillation testing has been able to detect all seven bridging faults: M10DSS (Fault-1), M5GDS (Fault-2), M5DSS (Fault-3), M11DSS (Fault-4), CCS (Fault-5), M7GDS (Fault-6), and M6GDS (Fault-7). At 77 K, oscillation based testing detected all seven bridging faults and the open fault. I_{DDQ} testing at 300 K and 77 K was able to detect two of the eight faults, faults-1 and 3 (M10DSS and M5DSS). However, other detectable faults could not be detected because of over estimation of I_{DDQ}.

In the present work, use of the combined oscillation and I_{DDQ} testing methods have enabled simultaneous testing of manufacturing defects (bridging and open faults). Theoretical results obtained from SPICE simulations are in close agreement with the corresponding experimental results on fabrication devices. The presented approach is attractive because of its simplicity and fault observability. The method can also be applied in testing of CMOS mixed-signal integrated circuits. Though the 77 K testing has been used in suppressing the subthreshold current for improved fault detection, however, it can be very effective in suppressing subthreshold current (leakage current) in analog integrated circuits designed in submicron CMOS process.

The combined I_{DDQ} and oscillation test method was further extended to integrate transient power supply transient current, I_{DDT}. The combined test methodology was used for fault detection in an amplifier with floating gate inputs designed in 1.5 μm n-well CMOS process for ±2.5 V operation. Two designs one with short faults and other with a combination of open and short faults were fabricated. Change in the performance of the op-amp has been studied when short faults and a combination of short and open faults are introduced using FITs. It is observed that the performance of the op-amp with open and short faults has been degraded. Experimental results show that the combination of the three testing methods increase the efficiency of fault detection.

5.1 Scope of Future Work

The designed built-in current sensors and test methodologies can be extended to different analog/mixed-signal circuits such as phase-locked loop circuits, sigma-delta modulators and filters.

Leakage current is one of the main challenges I_{DDQ} testing is facing in submicron technology. Test methods such as the ΔI_{DDQ} can be used. The effectiveness of ΔI_{DDQ} testing

can be further improved by suppressing the total leakage current of the CUT. Suppression techniques such as switched-source-impedance [117] and power supply gating [118] have been implemented in literature. By combining the BICS for I_{DDQ} testing and leakage current suppression techniques the effectiveness of I_{DDQ} testing can be improved in submicron technology.

REFERENCES

[1] M. Abramovici, M. A. Breuer and A. D. Friedman, *Digital Systems Testing and Testable Design*, Computer Science Press, 1994.

[2] T. W. Williams and K. P. Parker, "Design for testability - a survey," *Proceedings of IEEE,* vol. 71, no. 1, pp. 98-112, January 1983.

[3] A. Miczo, *Digital Logic Testing and Simulation*, John Wiley & Sons Inc., New Jersey, 2003.

[4] J. P. Hayes, "On modifying logic networks to improve their diagnosability," *IEEE Transactions on Computers,* vol. C-23, no. 1, pp. 56-62, January 1974.

[5] S. N. Bhatt, F. R. Chung and A. L. Rosenberg, "Partitioning circuits for improved testability," *Algorithmica,* vol. 6, no. 1, pp. 37-48, December 1991.

[6] W. Maly and P. Nigh, "Built-in current testing - feasibility study," *Proceedings of IEEE International Conference on Computer-Aided Design*, pp. 340-343, 1988.

[7] R. Rajsuman, I_{DDQ} *Testing for CMOS VLSI*, Artech House, 1994.

[8] URL: http://focus.ti.com/general/docs/gencontent.tsp?contentId=31183.

[9] J. Galiay, Y. Crouzet and M. Vergniault, "Physical versus logical fault models MOS LSI circuits: impact on their testability," *IEEE Transactions on Computers,* vol. C-29, no. 6, pp. 527-531, June 1980.

[10] C. F. Hawkins and J. M. Soden, "Reliability and electrical properties of gate oxide shorts in CMOS ICs," *Proceeding of the IEEE International Test Conference*, pp. 443-451, 1986.

[11] A. Chan, D. Lam, W. Tan and S. Y. Khim, "Electrical failure analysis in high density DRAMs," *Proceeding of IEEE International Workshop on Memory Technology, Design and Testing*, pp. 26-31, 1994.

[12] J. M. Soden and C. F. Hawkins, "Test considerations for gate oxide shorts in CMOS ICs," *IEEE Design & Test of Computers,* vol. 3, no. 4, pp. 56-64, August 1986.

[13] P. Nigh and W. Maly, "Test generation for current testing," *IEEE Design & Test,* vol. 7, no. 1, pp. 26-38, January 1990.

[14] M. Sachdev and J. P. d. Gyvez, *Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits*, 2nd ed, vol. 34, Springer, 2007.

[15] C. L. Wey and S. Krishnan, "Built-in self test (BIST) structures for analog circuit fault diagnosis with current test data," *IEEE Transcations on Instrumentation and Measurement,* vol. 41, no. 4, pp. 535-539, August 1992.

[16] S. K. Sunter and N. Nagi, "A simplified polynomial-fitting algorithm for DAC and ADC BIST," *Proceedings of the IEEE International Test Conference*, pp. 389 - 395, 1997.

[17] E. Teraoka, T. Kengaku, I. Yasui, K. Ishikawa, T. Matsuo, H. Wakada, N. Sakashita, Y. Shimazu and T. Tokuda, "A built in self test for ADC and DAC in a single chip speech CODEC," *Proceedings of the IEEE International Test Conference*, pp. 791-796, 1993.

[18] M. J. Ohletz, "Hybrid built in self test (HSBIT) for mixed analogue/digital integrated circuits," *Proceedings Eupropean Design and Test Conference*, pp. 307-316, 1991.

[19] M. F. Toner and G. W. Roberts, "A frequency response, harmonic distortion, and intermodulation distortion test for BIST of a sigma-delta ADC," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing,* vol. 43, no. 8, pp. 608-613, August 1996.

[20] K. Arabi and B. Kaminska, "Oscillation built-in self test (OBIST) scheme for functional and structural testing of analog and mixed-signal integrated circuits," *Proceedings of the IEEE International Test Conference*, pp. 786-795, 1997.

[21] M. Slamani, B. Kaminska and G. Quesnel, "An integrated approach for analog circuit testing with a minimum number of detected parameters," *Proceedings of the IEEE International Test Conference*, pp. 631-640, 1994.

[22] R. Maghrebi and M. Masmoudi, "A BIST structure for IP multi-slope A/D converter testing," *Measurement Science Review,* vol. 3, pp. 65-73, 2003.

[23] F. Azais, S. Bernard, Y. Bertrand and M. Renovell, "Towards an ADC BIST scheme using the histogram test technique," *Proceedings of the IEEE European Test Workshop*, pp. 53-58, 2000.

[24] M. F. Toner and G. W. Roberts, "A BIST scheme for an SNR test of a sigma-delta ADC," *Proceedings of the IEEE International Test Conference*, pp. 805 - 814, 1993.

[25] K. Arabi, B. Kaminska and J. Rzeszut, "A new built-in self-test approach for digital-to-analog and analog-to-digital converters," *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, pp. 491-494, 1994.

[26] Y. Xing, "Defect-oriented testing of mixed-signal ICs: some industrial experience," *Proceedings of the IEEE International Test Conference*, pp. 678-687, 1998.

[27] K. D. Wagner and T. W. Williams, "Design for testability of mixed signal integrated circuits," *Proceedings of the IEEE International Test Conference*, pp. 823-828, 1988.

[28] A. Richardson, A. Lechner and T. Olbrich, "Design for testability strategies for mixed signal & analogue designs-from layout to system," *Proceedings of IEEE International Conference on Electronics, Circuits and Systems*, pp. 425-432 1998.

[29] C. M. Maunder and R. E. Tulloss, *The Test Access Port and Boundary Scan Architecture*, *IEEE Computer Society Press Tutorial*, Los Alamltos, California, 1990.

[30] L. Liyang, J. H. Patel, T. Rinderknecht and A. W. T. Cheng., "Logic BIST with scan chain segmentation," *Proceedings of the IEEE International Test Conference*, pp. 57-66, 2004.

[31] Y. Savaria, M. Youssef, B. Kaminska and M. A. Koudil, "Automatic test point insertion for pseudo-random testing," *Proceedings of IEEE International Sympoisum on Circuits and Systems*, pp. 1960-1963 1991.

[32] N. Tamarapalli and J. Rajski, "Constructive multi-phase test point insertion for scan-based BIST," *Proceedings of the IEEE International Test Conference*, pp. 649-658, 1996.

[33] F. Brglez, C. Gloster and G. Kedem, "Hardware-based weighted random pattern generation for boundary scan," *Proceedings of the IEEE International Test Conference*, pp. 264-274, 1989.

[34] M. Levi, "CMOS is most testable," *Proceedings of the IEEE International Test Conference*, pp. 217-220, 1981.

[35] Y. K. Malaiya and S. Y. H. Su, "A new fault model and testing technique for CMOS devices," *Proceedings of the IEEE International Test Conference*, pp. 25-34, 1982.

[36] H. Walker and S. W. Director, "VLASIC: a catastrophic fault yield simulator for integrated circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 5, no. 4, pp. 541-556, October 1986.

[37] S. R. Mallarapu and A. J. Hoffman, "I_{DDQ} testing on a custom automotive IC," *IEEE Journal of Solid-State Circuits,* vol. 30, no. 3, pp. 295-299, March 1995.

[38] T. Barrette, V. Bhide, K. De, M. Stover and E. Sugasawara, "Evaluation of early failure screening methods," *Proceedings of IEEE International Workshop on I_{DDQ} Testing*, pp. 14-17, 1996.

[39] A. Allan, D. Edenfeld, W. H. Joyner, Jr., A. B. Kahng, M. A. Rodgers and Y. A. Zorian, "2001 technology roadmap for semiconductors," *Computer,* vol. 35, no. 1, pp. 42-53, January 2002.

[40] A. D. Singh, H. Rasheed and W. W. Weber, "I_{DDQ} testing of CMOS opens: an experimental study," *Proceedings of the IEEE International Test Conference*, pp. 479-489, 1995.

[41] A. Ferre, E. Isern, J. Rius, R. Rodriguez-Montanes and J. Figueras, "I_{DDQ} testing: state of the art and future trends," *Integration, the VLSI Journal,* vol. 26, no. 1-2, pp. 167-196, December 1998.

[42] J. Figueras and A. Ferre, "Possibilities and limitations of I_{DDQ} testing in submicron CMOS," *IEEE Transactions on Components, Packaging and Manufacturing Technology- Part B,* vol. 21, no. 4, pp. 352-359, November 1998.

[43] Y. Tsiatouhas, Y. Moisiadis, T. Haniotakis, D. Nikalos and A. Arapoyanni, "A new technique for I_{DDQ} testing in nanometer technologies," *Integration, the VLSI Journal,* vol. 31, pp. 183-194, 2002.

[44] J. Rius and J. Figueras, "Detecting I_{DDQ} defective CMOS circuits by depowering," *Proceedings of IEEE VLSI Test Symposium*, pp. 324-329, 1995.

[45] A. E. Gattiker and W. Maly, "Current signatures," *Proceedings of the 14th IEEE VLSI Test Symposium*, pp. 112-117, 1996.

[46] B. Lisenker and Y. Mitnick, "Fault model for VLSI circuits reliability assessment," *Proceedings of IEEE International Reliability Physics Symposium*, pp. 319-326, 1999.

[47] P. Maxwell, P. O'Neill, R. Aitken, R. Dudley, N. Jaarsma, M. Quach and D. Wiseman, "Current ratios: a self-scaling technique for production I_{DDQ} testing," *Proceedings of the IEEE International Test Conference*, pp. 1148-1156, 2000.

[48] S. Sabade and D. M. H. Walker, "Neighbor current ratio (NCR): a new metric for I_{DDQ} data analysis," *Proceedings of the 17th IEEE International Symposium on Defect and Fault-Tolerance in VLSI Systems*, pp. 381-389, 2002.

[49] S. Sabade and D. M. H. Walker, "Immediate neighbor difference I_{DDQ} test (INDIT) for outlier identification," *Proceedings of the 16th International Conference on VLSI Design*, pp. 361-366, 2003.

[50] C. Thibeault, "On new current signatures and adaptive test technique combination," *Proceedings of IEEE VLSI Test Symposium*, pp. 59-64, 2004.

[51] Y. Tsiatouhas, T. Haniotakis, D. Nicolos and A. Arapoyanni, "Extending the viability of I_{DDQ} testing in the deep submicron era," *Proceedings of the 3rd International Symposium on Quality Electronic Design*, pp. 100-105, 2002.

[52] E. Isern and J. Figueras, "I_{DDQ} test and diagnosis of CMOS circuits," *IEEE Design & Test of Computers,* vol. 12, no. 4, pp. 60-67, December 1995.

[53] J. M. Soden, C. F. Hawkins and A. C. Miller, "Identifying defects in deep-submicron CMOS ICs," *IEEE Spectrum,* vol. 33, no. 9, pp. 66-71, September 1996.

[54] S. P. Athan, D. L. Landis and S. A. Al-Arian, "A novel built-in current sensor for I_{DDQ} testing of deep submicron CMOS ICs," *Proceedings of 14th VLSI Test Symposium*, pp. 118-123, 1996.

[55] T. W. Williams, R. H. Dennard, R. Kapur, M. Mercer and W. Maly, "I_{DDQ} test: sensitivity analysis of scaling," *Proceedings of the IEEE International Test Conference*, pp. 786-792, 1996.

[56] Y. Tsiatouhas, Y. Moisiadis, T. Haniotakis, D. Nikolos and A. Arapoyanni, "A new scheme for effective I_{DDQ} testing in deep submicron," *Proceedings IEEE International Workshop on Defect Based Testing*, pp. 9-14, 2000.

[57] J. Vazquez and J. de. Gyvez, "Built-in current sensor for ΔI_{DDQ} testing of deep submicron digital CMOS ICs," *Proceedings of the IEEE 22nd VLSI Test Symposium (VTS 2004)*, pp. 53-58, 2004.

[58] J. Vazquez and J. de. Gyvez, "Built-in current sensor for ΔI_{DDQ} testing," *IEEE Journal of Solid-State Circuits,* vol. 39, no. 3, pp. 511-518, March 2004.

[59] C. Thibeault, "A novel probabilistic approach for IC diagnosis based on differential quiescent current signatures," *Proceedings of the IEEE VLSI Test Symposium*, pp. 80-85, 1997.

[60] C. Thibeault and L. Boisvert, "Diagnosis method based on ΔI_{DDQ} probabilistic signatures: experimental results," *Proceedings of the International Test Conference*, pp. 1019-1026, 1998.

[61] C. Thibeault, "Diagnosis method using ΔI_{DDQ} probabilistic signatures: theory and results," *Journal of Electronic Testing: Theory and Applications,* vol. 16, no. 4, pp. 339-353, August 2000.

[62] C. Thibeault, "Improving ΔI_{DDQ} based test methods " *Proceedings of the IEEE International Test Conference*, pp. 207-216, 2000.

[63] C. Thibeault, "Efficient diagnosis of single/double bridging faults with delta I_{DDQ} probabilistic signatures and viterbi algorithm," *Proceedings of the 18th IEEE VLSI Test Symposium*, pp. 431-438, 2000.

[64] Y. Okuda, "DECOUPLE: defect current detection in deep submicron I_{DDQ}," *Proceedings of the IEEE International Test Conference*, pp. 199-206, 2000.

[65] W. R. Daasch, J. McNames, D. Bockelman and K. A. Cota, "Variance reduction using wafer patterns in I_{DDQ} data," *Proceedings of the IEEE International Test Conference*, pp. 189-198, 2000.

[66] T. J. Powell, J. Pair, M. John and D. A. Counce, "ΔI_{DDQ} for testing reliability," *Proceedings of the IEEE VLSI Test Symposium*, pp. 439-443, 2000.

[67] P. Lee, A. Chen and D. Mathew, "A speed dependent approach for ΔI_{DDQ} implementation," *Proceedings of the IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 280-286, 2001.

[68] B. Kruseman, R. van Veen and K. van Kaam, "The future of ΔI_{DDQ} testing," *Proceedings of the IEEE International Test Conference*, pp. 101-110, 2001.

[69] S. Dragic and M. Margala, "A 1.2V built-in architecture for high frequency on-line $I_{DDQ}/\Delta I_{DDQ}$ test," *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, pp. 148-153, 2002.

[70] Y. Nishizaki, O. Nakayama, C. Matsumoto, Y. Kimura, T. Kobayashi and H. Nakamura, "Testing DSM ASIC with static, ΔI_{DDQ}, and dynamic test suite: implementation and results " *Proceedings of the IEEE International Test Conference*, pp. 85-94, 2003.

[71] O. Semenov, A. Vassighi and M. Sachdev, "Leakage current in sub-quater micron MOSFET: a perspective on stressed ΔI_{DDQ} testing," *Journal of Electronic Testing: Theory and Applications,* vol. 19, pp. 341-352, June 2003.

[72] M. Keating and D. Meyer, "A new approach to dynamic I_{DD} testing," *Proceedings of IEEE International Test Conference*, pp. 316-321, 1987.

[73] K. Wallquist, A. Righter and C. Hawkins, "A general purpose I_{DDQ} measurement circuit," *Proceedings of the IEEE International Test Conference*, pp. 642 - 651, 1993.

[74] M. Soma, "Probabilistic measures of fault equivalence in mixed-signal systems," *Proceedings of the IEEE VLSI Test Symposium*, pp. 67-70, 1991.

[75] M. Slamani and B. Kaminska, "Multifrequency testability analysis for analog circuits," *Proceedings of the IEEE VLSI Test Symposium*, pp. 54-59, 1994.

[76] M. Worsman, M. W. T. Wong and Y. S. Lee, "Analog circuit equivalent faults in the DC domain," *Proceedings of the 9th Asian Test Symposium*, pp. 84-89, 2000.

[77] C. Chao, H.-J. Lin and L. Miler, "Optimal testing of VLSI analog circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 16, no. 1, pp. 58-77, January 1997.

[78] C. Pan and K. Cheng, "Pseudorandom testing for mixed-signal circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 16, no. 10, pp. 1173-1185, October 1997.

[79] K. Arabi and B. Kaminska, "Testing analog and mixed-signal integrated circuits using oscillation-test method," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 16, no. 7, pp. 745-753, July 1997.

[80] K. Arabi and B. Kaminska, "Design for testability of embedded integrated operational amplifiers," *IEEE Journal of Solid-State Circuits,* vol. 33, no. 4, pp. 573-581, April 1998.

[81] B. Dufort and G. W. Roberts, "On-chip analog signal generation for mixed-signal built-in self-test," *IEEE Journal of Solid-State Circuits,* vol. 34, no. 3, pp. 318-330, March 1999.

[82] S. Tabatabaei and A. Ivanov, "A built-in current monitor for testing analog circuit blocks," *Proceeding of the IEEE International Symposium on Circuits and Systems*, pp. 109-114, 1999.

[83] R. Mozuelos, Y. Lechuga, M. Martinez and S. Bracho, "Test of a switched-capacitor ADC by a built-in charge sensor," *Microelectronics Journal,* vol. 36, no. 12, pp. 1064-1072, July 2005.

[84] Y. Miura, S. Naito and K. Kinoshita, "A case study of mixed-signal integrated circuit testing: an application of current testing using the upper limit and lower limit," *Proceeding of the International Symposium Circuits and Systems*, pp. 77-80, 1994.

[85] Y. Miura, "Real-time current testing for A/D converters," *IEEE Design & Test of Computers,* vol. 13, no. 2, pp. 34-41, June 1996.

[86] A. Srivastava, S. Aluri and A. K. Chamakura, "A simple built-in current sensor for I_{DDQ} testing of CMOS data converters," *Integration, the VLSI Journal,* vol. 38, no. 4, pp. 579-596, April 2005.

[87] S. Yellampalli and A. Srivastava, "ΔI_{DDQ} based testing of submicron CMOS digital-to-analog converter circuits," *Journal of Active and Passive Electronic Devices,* 2008 (in press).

[88] S. Yellampalli and A. Srivastava, "ΔI_{DDQ} testing of CMOS data converters," *Journal of Active and Passive Electronic Devices,* 2008 (accepted).

[89] K. Arabi, H. Ihs, C. Dufaza and B. Kaminska, "Digital oscillation-test method for delay and stuck-at fault testing of digital circuits," *Proceedings of the IEEE International Test Conference*, pp. 91-100, 1998.

[90] D. Vazquez, G. Huertas, G. Leger, A. Rueda and J. L. Huertas, "Practical solutions for the application of the oscillation-based-test in analog integrated circuits," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. I-589-I-592, 2002.

[91] G. Huertas, D. Vazquez, E. J. Peralas, A. Rueda and J. L. Huertas, "Practical oscillation-based test of integrated filters," *IEEE Design & Test of Computers,* vol. 19, no. 6, pp. 64-72, December 2002.

[92] M. Ishida, D. S. Ha, T. Yamaguchi, Y. Hashimoto and T. Ohmi, "I_{DDT} testing : an efficient method for detecting delay faults and open defects," *Proceedings of the IEEE International Workshop on Defect Based Testing*, pp. 23-28, 2001.

[93] A. Singh, C. Patel, S. Liao, J. Plusquellic and A. Gattiker, "Detecting delay faults using power supply transient signal analysis," *Proceedings of the IEEE International Test Conference*, pp. 395-404, 2001.

[94] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley, 2001.

[95] S. Yellampalli and A. Srivastava, "A simple noise modeling based testing of CMOS analog integrated circuits," *Proceeding of SPIE, Noise in Devices and Circuits III,* vol. 5844, pp. 276-283, 2005.

[96] Y. Lechuga, R. Mozuelos, M. Martinez and S. Bracho, " Built-in dynamic current sensor for hard-to-detect faults in mixed-signal ICs," *Proceedings Design, Automation and Test in Europe Conference and Exhibition*, pp. 205-211, 2002.

[97] A. Srivastava, *I_{DDQ} testing of CMOS mixed-signal integrated circuits*, U.S. patent no.: 6,930,500, August 16,2005.

[98] B. Razavi, *Principles of Data Conversion System Design*, p.124, 1st Edition, IEEE Inc., 1995.

[99] URL: http://www.maxim-ic.com/appnotes.cfm/appnote_number/810.

[100] R. Baker, H. Li and D. Boyce, *CMOS Circuit Design Layout and Simulation*, IEEE Press, 2003.

[101] V. Srinivas, S. Pavan, A. Lachhwani and N. Sasidhar, "A distortion compensating flash analog-to-digital conversion technique," *IEEE Journal of Solid-State Circuits,* vol. 41, no. 9, pp. 1959-1969, August 2006.

[102] K. Kishine, K. Fujimoto, S. Kusanagi and H. Ichino, "PLL design technique by a loop-trajectory analysis taking decision-circuit phase margin into account for over-10-Gb/s clock and data recovery circuits," *IEEE Journal of Solid-State Circuits,* vol. 39, no. 5, pp. 740-750, May 2004.

[103] P. Alli, *Testing a CMOS Operational Amplifier Circuit Using a Combination of Oscillation and I_{DDQ} Test Methods*, M.S. (EE) Thesis, ECE Department, Louisiana State University, Baton Rouge, 2004.

[104] V. Pulendra, *Power Supply Current [I_{PS}] Based Testing of CMOS Amplifier Ciruit with and without Floating Gate Input Transistors*, M.S. (EE) Thesis, ECE Department, Louisiana State University, Baton Rouge, 2005.

[105] U. Kac and F. Novak, "Oscillation test scheme of SC bi-quad filters based on internal reconfiguration," *Journal of Electronic Testing: Theory and Applications,* vol. 23, no. 6, pp. 485-495, October 2007.

[106] K. Arabi and B. Kaminska, "Testing digital-to-analog converters based on oscillation-test strategy using sigma-delta modulation," *Proceedings of the International Conference on Computer-Aided Design*, pp. 40-46, 1998.

[107] M. S. Zarnik, F. Novak and S. Macek, "Design of oscillation-based test structures for active RC filters," *IEE Proceedings~Circuits, Devices and Systems,* vol. 147, no. 5, pp. 297 - 302, 2000.

[108] W. Maly and M. Patyra, "Design of IC's applying built-in current testing," *Journal of Electronic Testing: Theory and Applications,* vol. 3, no. 4, pp. 397-406, December 1992.

[109] B. D. Brown and R. D. McLeod, "Built-in current mode circuits for I_{DDQ} monitoring," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 30.6.1-30.6.4, 1993.

[110] C. Hsue and C. Lin, "Built-in current sensor for I_{DDQ} test in CMOS," *Proceedings of the IEEE International Test Conference*, pp. 635-641, 1993.

[111] J. B. Kim, S. J. Hong and J. Kim, "Design of a built-in current sensor for I_{DDQ} testing," *IEEE Journal of Solid-State Circuits,* vol. 33, no. 8, pp. 1266-1272, August 1998.

[112] M. Yinghua and L. Zhongcheng, "I_{DDT} testing versus I_{DDQ} testing," *Journal of Electronic Testing: Theory and Applications,* vol. 13, no. 1, pp. 51-55, 1998.

[113] A. Srivastava and S. Aluri, "A novel approach to I_{DDQ} testing of mixed signal integrated circuits," *Proceedings of the 45th IEEE International Midwest Symposium on Circuits and Systems*, pp. 270-273, 2002.

[114] G. Gielen, Z. Wang and W. Sansen, "Fault detection and input stimulus determination for the testing of analog integration circuits based on power-supply current monitoring," *Proceedings of IEEE International Conference on Computer-Aided Design*, pp. 495-498, 1994.

[115] S. Yellampalli, A. Srivastava and V. Pulendra, "A combined oscillation, power supply current and I_{DDQ} testing methodology for fault detection in floating gate input CMOS operational amplifier," *Proceeding of the 48th IEEE International Midwest Symposium on Circuits and Systems*, pp. 503-506, 2005.

[116] URL: www.mosis.org.

[117] M. Horiguchi, T. Sakata and K. Itoh, "Switched-source-impedance CMOS circuit for low standby subthreshold current giga-scale LSI's," *IEEE Journal of Solid-State Circuits,* vol. 28, no. 11, pp. 1131-1135, November 1993.

[118] S. Bhunia, H. Mahmoodi, D. Ghosh, S. Mukhopadhyay and K. Roy, "Low power scan design using first level supply gating," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 13, no. 3, pp. 384-395, March 2005.

[119] J. B. Kim, S. J. Hong and J. Kim, "Design of a built-in current sensor for I_{DDQ} testing," *IEEE Journal of Solid-State Circuits,* vol. 33, no. 8, pp. 1266-1272, August 1998.

APPENDIX - A*

A SIMPLE NOISE MODELING BASED TESTING OF CMOS ANALOG INTEGRATED CIRCUITS

A.1 Introduction

In this work, a technique for testing CMOS analog integrated circuits based on the analysis of the noise behavior of the circuit under test (CUT) is presented. The CUT in the present work is an integrated CMOS amplifier circuit designed in 1.5 μm n-well CMOS process for operation at ± 2.5 V. The bridging faults simulating possible manufacturing defects have been introduced using the fault injection transistors. The faults in the CUT are detected by observing the variation in the noise at the output of the CUT, which is the sum of the noise contributed by each component in the circuit. An analytical noise model of the CUT has been developed with and without faults and results are compared with the corresponding data obtained from the simulation studies using SPICE for fault detection.

Analog circuits are the essential building blocks of mixed-signal circuits. There are established techniques like oscillation testing, testing using ATPG, scan based testing, ΔI_{DDQ} testing, I_{DDQ} testing and BIST for testing digital circuits [1-6]. Testing analog circuits is also difficult since there is no binary relation between the input and output of analog circuits similar to digital circuits. The output of analog circuits is also very sensitive to design and technology parameters. An efficient test method needs to be sensitive enough to precisely identify the deviations of characteristic parameters beyond the tolerance limit [7-8]. The proposed method uses the input referred noise in the CMOS amplifier which is modeled

* Part of the work is reported in following publication:
S. Yellampalli and A. Srivastava, "A simple noise modeling based testing of CMOS analog integrated circuits," *Proceeding of SPIE: Noise in Devices and Circuits III,* vol. 5844, pp. 276-283, 2005.

using the noise model of a MOSFET [9, 10] to obtain the noise at the output of the amplifier. The amplified output is used for the fault detection. This chapter is organized as follows. In Section A.2, noise model of the MOSFET is presented. The noise analysis of the CMOS amplifier circuit is presented in Section A.3. In Section A.4, simulated and calculated results of the CMOS amplifier with and without injected faults are compared and faults are detected. Summary of the result and analysis is presented in conclusion.

A.2 Noise in a MOSFET

A MOSFET is associated with the following noises: thermal noise, flicker noise and shot noise [9]. Thermal noise and flicker noise in a MOSFET can be lumped into a single noise generator, $\overline{i_d^2}$. The combination of thermal and flicker noise is given by [9]

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT\left(\frac{2}{3}g_m\right) + K_1\frac{I_D^a}{f} \tag{A.1}$$

where I_D is the drain bias current, K_1 is a constant for the given device, a is a constant whose value lies between 0.5 and 2, g_m is the transconductance, f is the corner frequency, K is the Boltzmann Constant and T is the absolute temperature. The corner frequency, f in Eq. (A.1) is given by [10],

$$f = \frac{k}{c_{ox}WL}g_m\frac{3}{8kT}. \tag{A.2}$$

Shot noise is described by

$$\frac{\overline{i_s^2}}{\Delta f} = 2qI_D \tag{A.3}$$

where $\frac{\overline{i_s^2}}{\Delta f}$ is the noise spectral density and I_D is the drain current of a MOSFET.

Total noise in a MOSFET is given by the sum of noise described by Eqs. (A.1) and (A.3). Figure A.1 shows the small signal noise model of an n-MOSFET [9]. In Figure A.1, $\overline{i_g^2}$ is the gate leakage current noise generator, $\overline{i_d^2}$ is the drain current noise generator, $\overline{i_s^2}$ is the substrate leakage current noise generator and $g_m v_{gs}$ is the current source due to gate source voltage, $g_{mb} v_{bs}$ is the current source due to body source voltage, r_d is the small signal output resistance and c_{gb}, c_{gd}, c_{gs}, c_{sb} , c_{db} are the parasitic capacitances. In the noise analysis of a MOSFET, $\overline{i_s^2}$ is normally neglected because the source and substrate are at the same voltage. For the present design, it is considered since source and substrate are at different voltages. The equivalent input noise-current generator, $\overline{i_i^2}$ for the MOSFET can be calculated by open circuiting the input of the circuit and expressing the output current in terms of the input current [9]. It is given by

$$i_i \frac{g_m}{j\omega c_{gs}} = i_g \frac{g_m}{jwc_{gs}} + i_d - i_s \frac{g_{mb}}{j\omega c_{sb}}. \tag{A.4}$$

Since the noise sources are independent, Eq. (A.4) can also be written in the following form,

$$\frac{\overline{i_i^2}}{\Delta f} = \frac{\overline{i_g^2}}{\Delta f} + \frac{i_d^2}{\Delta f}\frac{\omega^2 c_{gs}}{g_m^2} - \frac{\overline{i_s^2}}{\Delta f}\frac{c_{gs}^2}{c_{sb}^2}\frac{g_{mb}^2}{g_m^2} \tag{A.5}$$

where

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT\left(\frac{2}{3}g_m\right) + K_1\frac{I_D^a}{f}, \frac{\overline{i_g^2}}{\Delta f} = 2qI_G \text{ and } \frac{\overline{i_s^2}}{\Delta f} = 2qI_S. \tag{A.6}$$

Thermal noise density is given by [9],

$$\frac{\overline{i_i^2 thermal}}{\Delta f} = \frac{i_d^2}{\Delta f}\frac{\omega^2 c_{gs}^2}{g_m^2} = \left(4kT\left(\frac{2}{3}g_m\right) + K_1\frac{I_D^a}{f}\right)\frac{\omega^2 c_{gs}^2}{g_m^2}. \tag{A.7}$$

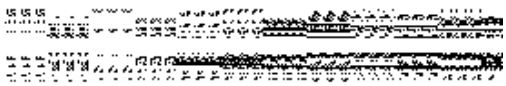


Figure A.1: Small signal noise model of an n-MOSFET [9].

The shot noise density is given by [11],

$$\frac{\overline{i_i^2 shot}}{\Delta f} = 2qI_G - \frac{\overline{i_s^2}}{\Delta f}\frac{c_{gs}^2}{c_{sb}^2}\frac{g_{mb}^2}{g_m^2} \approx -2qI_{so}(e^{-V_{sb}q/kT} - 1)\frac{c_{gs}^2}{c_{sb}^2}\frac{\gamma^2}{4(2\phi_f + V_{SB})} \tag{A.8}$$

The shot noise density is given by [11],

$$\frac{\overline{i_i^2 shot}}{\Delta f} = 2qI_G - \frac{\overline{i_s^2}}{\Delta f}\frac{c_{gs}^2}{c_{sb}^2}\frac{g_{mb}^2}{g_m^2} \approx -2qI_{so}(e^{-V_{sb}q/kT} - 1)\frac{c_{gs}^2}{c_{sb}^2}\frac{\gamma^2}{4(2\phi_f + V_{SB})} \tag{A.8}$$

where

$$\frac{g_{mb}^2}{g_m^2} = \frac{\gamma^2}{4(2\phi_f + V_{SB})}. \tag{A.9}$$

A.3 Noise Analysis of the CMOS Amplifier Circuit

The noise in a CMOS amplifier circuit can be calculated using the noise model of the MOSFET described in Section A.2. The noise in each MOSFET is represented by an equivalent noise input voltage generator as shown in Figure A.1 as the noise in each MOSFET is independent of each other. The equivalent noise voltage $\overline{v_{eqt}^2}$ can be calculated as follows:

$$\overline{v_{eqt}^2} = \overline{v_{eq1}^2} + \overline{v_{eq2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2\left(\overline{v_{eq3}^2} + \overline{v_{eq4}^2}\right) \tag{A.10}$$

The input transistors contribute mostly to the noise in an amplifier. The contribution due to loads is reduced by the square of the ratio of their transconductance to that of the input transistors [9]. Following are the noise model equations for thermal and shot noise, which are obtained by converting current noise generators in Eqs. (A.7) and (A.8), into voltage noise generators:

$$\overline{v_i^2 thermal} = \frac{i_d^2}{\Delta f}\frac{1}{g_m^2} = \left(4kT\left(\frac{2}{3}g_m\right) + K_1\frac{I_D^a}{f}\right)\frac{1}{g_m^2} \tag{A.11}$$

$$\frac{\overline{v_i^2 shot}}{\Delta f} = \frac{\overline{i_s^2}}{\Delta f}\left|z^2\right|\frac{g_{mb}^2}{g_m^2} = -2qI_{so}\left(e^{-v_{SB}q/kT}-1\right)\left(r_{equ,s}\,//\,\frac{1}{\omega c_{sb}}\right)^2\frac{\gamma^2}{4\left(2\Phi_f+v_{SB}\right)} \tag{A.12}$$

where Z is the equivalent load impedance. In Eq. (A.12), an equivalent resistance $r_{equ,s}$ has been added for practical consideration. This is the equivalent resistance of the current source which is parallel to ωc_{sb}. Ideally the value of $r_{equ,s}$ will be infinite for ideal current source. The term $\left(r_{equ,s}\,//\,\frac{1}{\omega c_{sb}}\right)$ will come into effect only at high frequencies and has no effect on the total noise at low frequencies. Substituting Eqs. (A.11) and (A.12) in Eq. (A.10), equivalent mean square noise voltage model equation is obtained and is given by,

$$\overline{v_{eqt}^2} = \left(\frac{8kTg_{m1}}{3}+K_1\frac{I_D^a}{f}\right)\frac{2}{g_{m1}^2} - 4qI_{so}\left(e^{-v_{SB}q/kT}-1\right)\left(r_{equ,s}\,//\,\frac{1}{\omega c_{sb}}\right)^2 + \frac{\gamma^2}{4\left(2\phi_f+v_{SB}\right)}$$
$$+\left(\frac{g_{m3}}{g_{m1}}\right)^2\left(\left(\frac{8kTg_{m3}}{3}+K_1\frac{I_D^a}{f}\right)\frac{2}{g_{m3}^2} - 4qI_{so}\left(e^{-v_{SB}q/kT}-1\right)\left(r_{equ,s}\,//\,\frac{1}{\omega c_{sb}}\right)^2\right). \tag{A.13}$$

Equation (A.13) gives the input referred noise which is transferred as an amplified output set by the gain of the amplifier.

A.4 Results and Discussion

Figure A.2 shows the circuit diagram of a CMOS operational amplifier. Figure A.3 shows the corresponding layout in 1.5 μm n-well CMOS process. Figure A.4 shows the microphotograph of a fabricated CMOS chip. The circuit of Figure A.2 is simulated in SPICE using MOS level 3 model parameters [13]. Figure A.5 shows the variation of the total

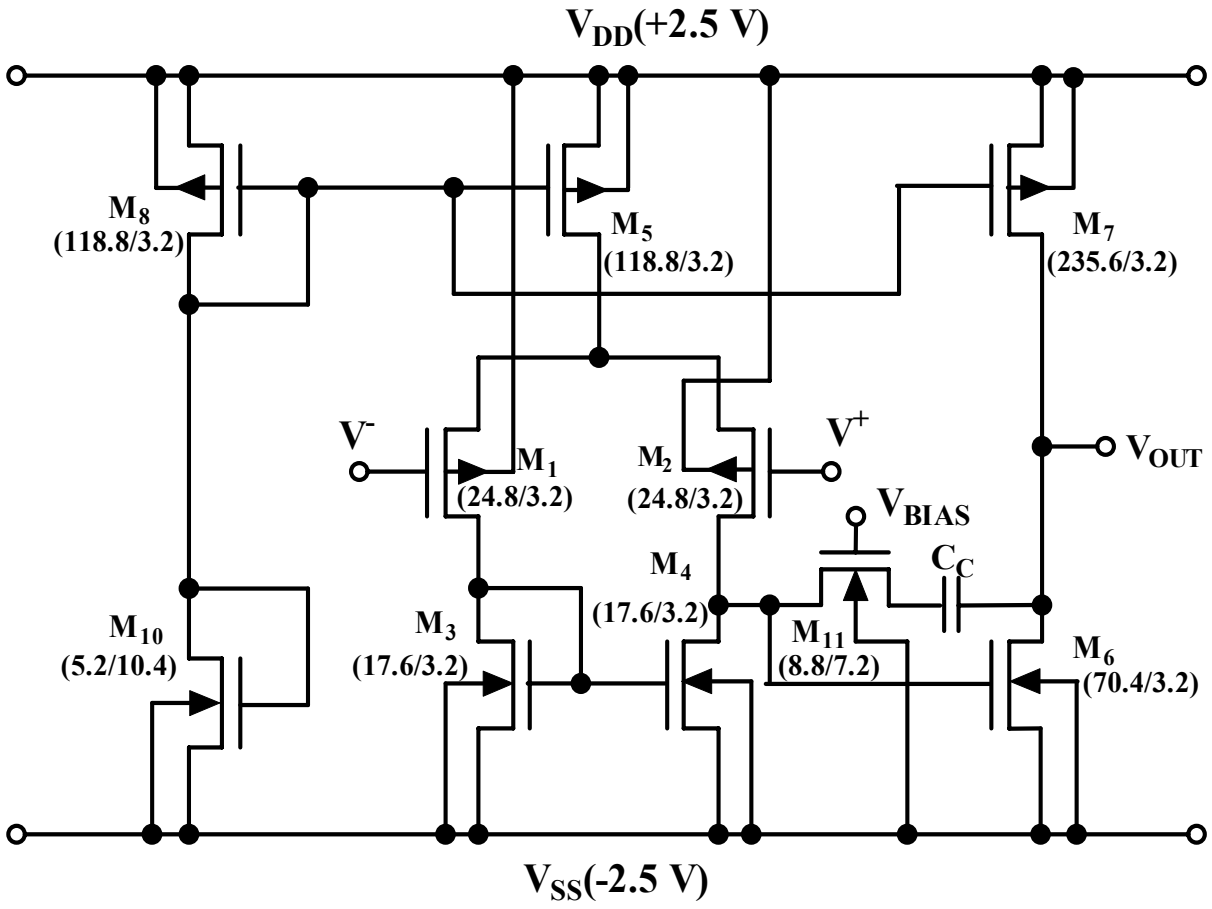


Figure A.2: A two-stage CMOS amplifier circuit.

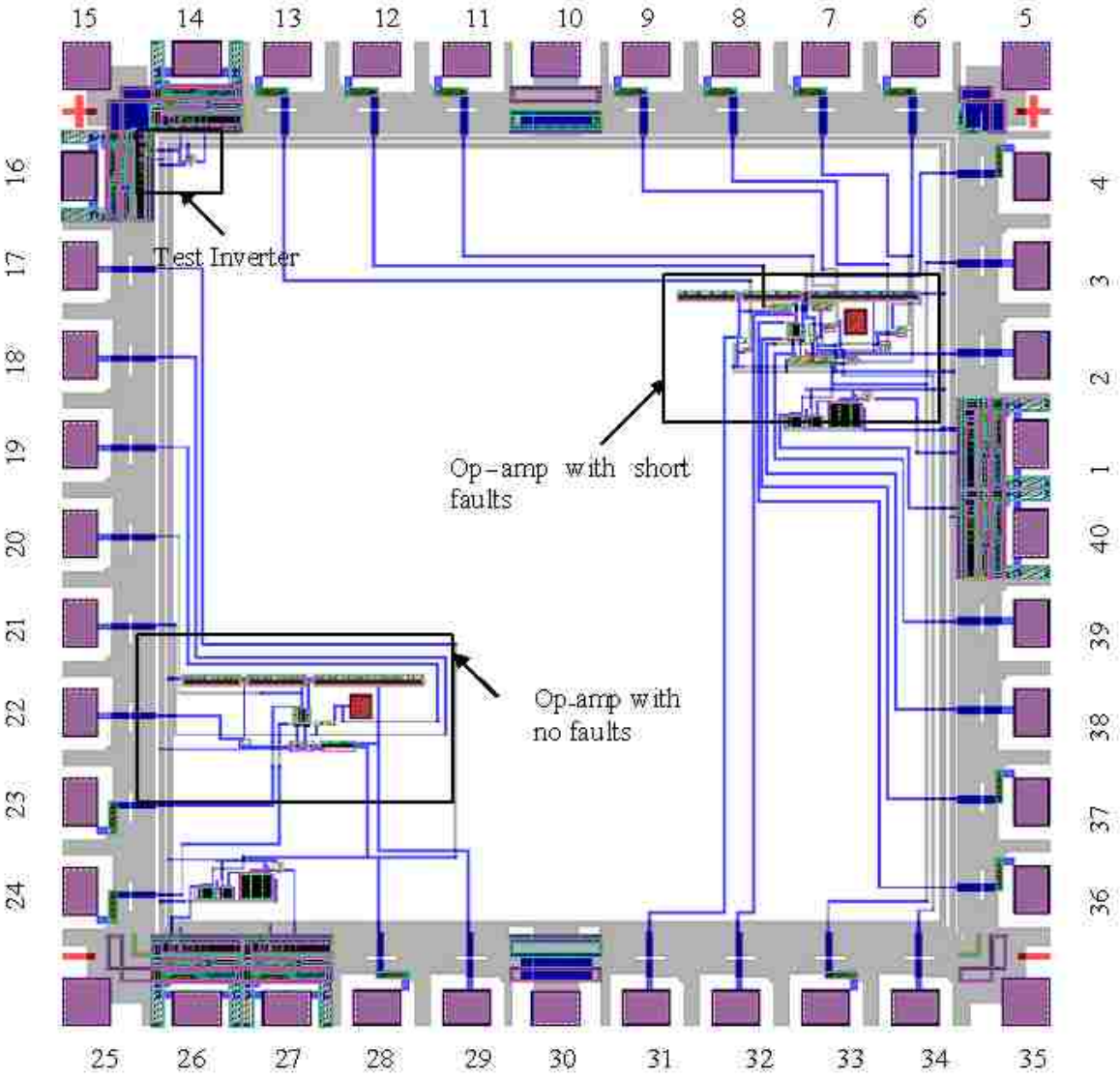


Figure A.3: Layout of a CMOS amplifier circuit of Fig. A.2.

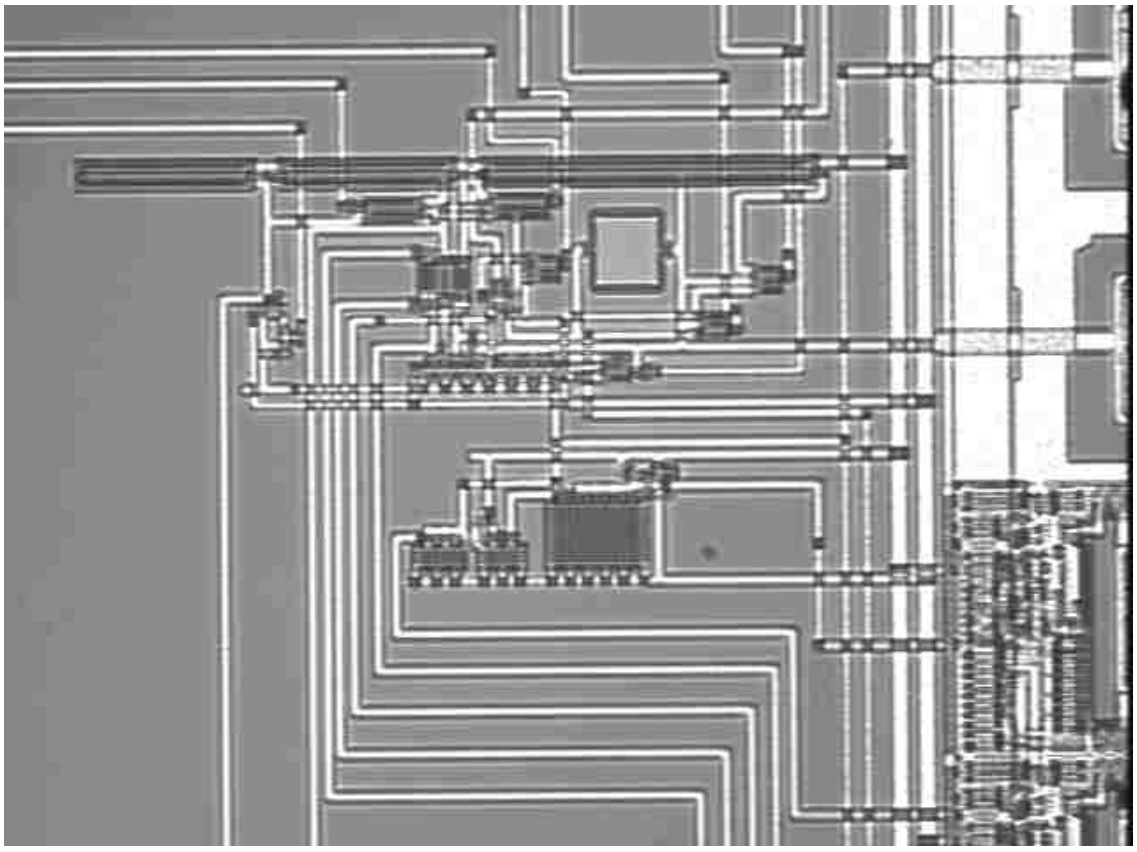


Figure A.4: Microphotograph of the fabricated CMOS chip.

noise of the CMOS amplifier circuit with frequency. In Figure A.5, dotted line corresponds to SPICE simulations and solid line corresponds to Eq. (A.13). The modeled output noise without injected faults obtained from Figure A.5 is 215 μV , which is in close agreement with the corresponding SPICE simulated noise of 254 μV . The total input referred noise is 19 nV/$\sqrt{Hz}$. Seven faults are injected in the amplifier circuit using fault injection transistors (FITs) [4] which are distributed as shown in Figure A.6. The injected faults in the amplifier are as follows: Fault 1: M10 drain-source short (M10DSS), Fault 2: M5 gate-drain short (M5GDS), Fault 3: M5 drain-source short (M5DSS), Fault 4: M11 drain-source short (M11DSS), Fault 5: compensation capacitor short (CCS), Fault 6: M7 gate-drain short (M7GDS) and Fault 7: M6 gate-drain short (M6GDS). These faults simulate bridging type faults due to manufacturing defects. When a fault is introduced, the noise at the output deviates from the value which corresponds to a fault-free condition. A detectable fault would deviate significantly from the corresponding fault-free condition. Table A.1 summarizes the calculated and simulated total noise and gain of the CMOS amplifier. Table A.2 summarizes the deviation of the noise from the fault-free condition.

It is noticed from tables A.1 and A.2 that all faults except the Fault 4 have been detected by the proposed noise model analysis. For the Fault 4, deviation of noise voltage at the output obtained from both simulation (SPICE) and noise modeling (Eq. 13) is negligible. It is also noticed from tables A.1 and A.2 that the amplifier output degrades so much for faults 5 and 7 that no measurable output noise is observed.

A.5 Conclusion

A new testing methodology for detecting faults in CMOS analog CMOS integrated circuits is proposed which is based on the noise modeling of the MOSFET. The circuit under

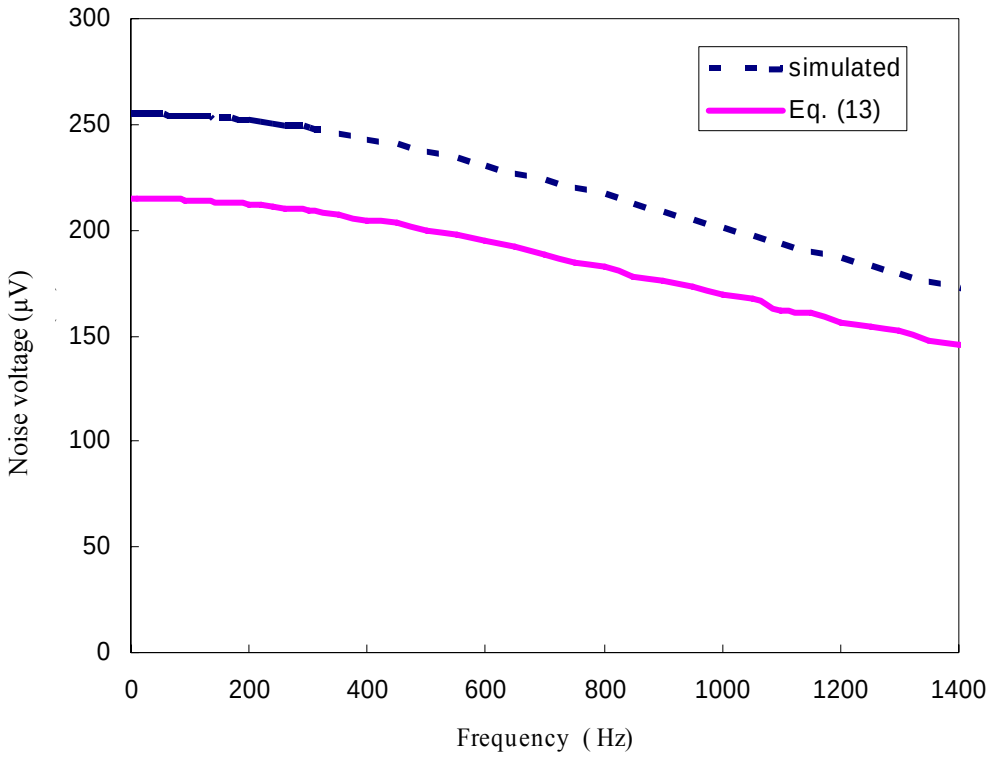


Figure A.5: SPICE simulated output noise variation with frequency of the CMOS amplifier circuit of Figure A.2 and the corresponding layout in Figure A.3.

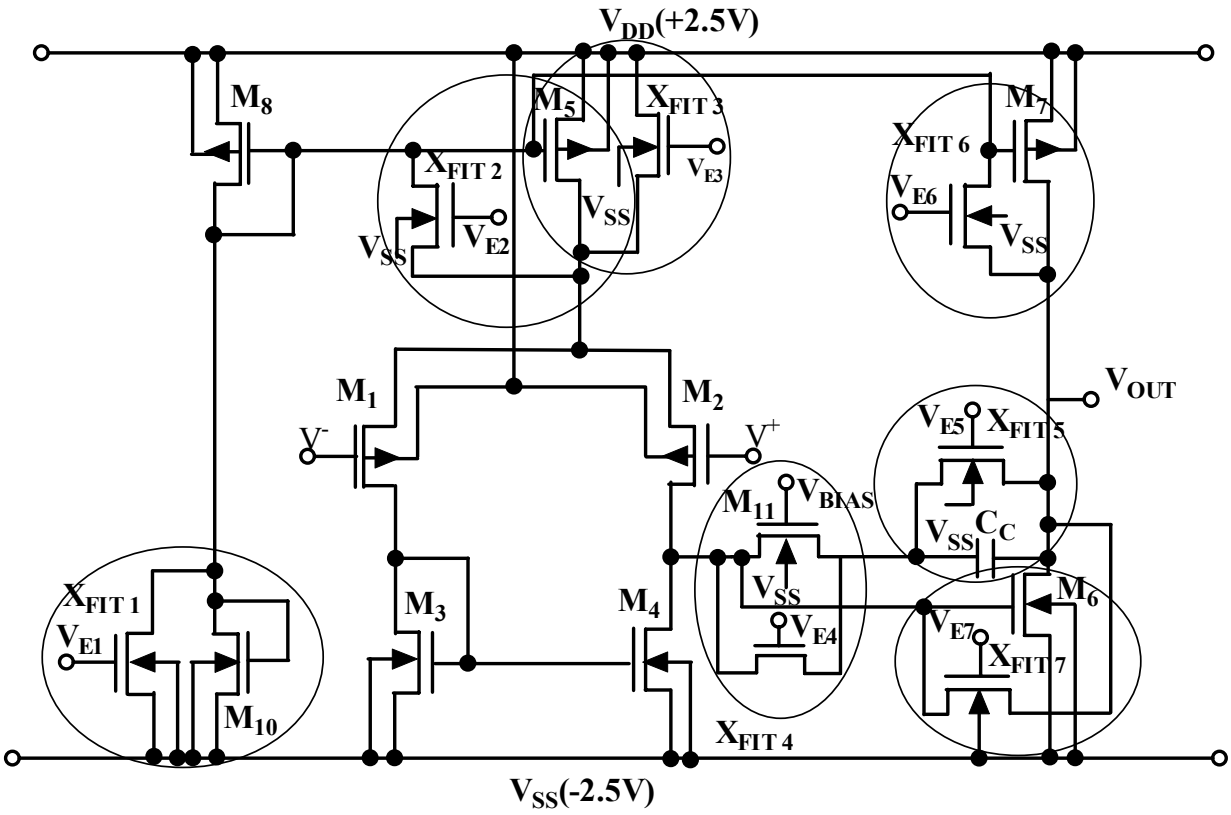


Figure A.6: CMOS operational amplifier circuit of Figure A.2 with injected faults.

Table A.1: SPICE simulated and calculated noise at 50 Hz -150 Hz

Fault Number	**Noise at the Output (μV) (simulated)**	**Noise at the Output (μV) (Eq. 13)**	**Amplifier Gain**
No fault	254	215	11,267
Fault 1	1.3	1.2	66
Fault 2	2.5	1.5	80
Fault 3	0.3	0.3	14
Fault 4	251	212	11,162
Fault 5[+]	-	-	0
Fault 6	18	16	823
Fault 7[+]	-	-	0

[+]Loss of output noise

Table A.2: Noise deviations under fault-injections at 50 Hz -150 Hz

Fault Number	**Deviation from Output Noise (%)**
No Fault	0
Fault 1	99
Fault 2	99
Fault 3	100
Fault 4	1.2 (No deviation)
Fault 5	100
Fault 6	93
Fault 7	100

test (CUT) is a ± 2.5 V CMOS amplifier designed in 1.5 μm n-well CMOS process. In CMOS amplifier circuit, the input referred noise due to faults is amplified to the output by the gain factor. Seven injected faults simulating manufacturing defects were distributed across the amplifier circuit and all were identified by the proposed method. The new method is simple and requires no additional circuit for detection of faults except the fault injection transistors simulating bridging type faults due to manufacturing defects

A.6 References

1. K. Arabi, H. Ihs, C. Dufaza and B. Kaminska, "Digital oscillation-test method for delay and stuck-at fault testing of digital circuits," *Proceeding of the IEEE International Test Conference*, pp. 91-100, 1998.

2. P. Gupta and M.S. Hsiao, "High quality ATPG for delay defects," *Proceeding of the IEEE International Test Conference*, pp 584-591, 2003.

3. I. Pomeranz and S.M. Reddy, "On improving the stuck-at fault coverage of functional test sequences by using limited scan operations," *Proceeding of the IEEE International Test Conference*, pp. 211- 220, 2001.

4. J.R. Vazquez, and J.P. Gyvez, "Built-in current sensor for ΔI_{DDQ} testing of deep submicron digital CMOS ICs," *Proceeding of VLSI Test Symposium,* pp. 53-58, 2004.

5. T. Calin, L. Anghel and M. Nicolaidis, "Built-in current sensor for I_{DDQ} testing in deep submicron CMOS," *Proceeding of IEEE VLSI Test Symposium*, pp.135-142, 1999.

6. S. Manich, L. Garcia, L. Balado, E. Lupon, J. Rius, R. Rodriguez and J. Figueras, "BIST technique by equally spaced test vector sequence," *Proceeding of IEEE VLSI Test Symposium*, pp.206-211, 2004.

7. J. Roh and J. Abraham, "A comprehensive signature analysis for oscillation-test," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 10, pp.1409-1423, October 2003.

8. S. Bhunia and K. Roy, "Dynamic supply current testing of analog circuits using wavelet transform," *Proceeding of IEEE VLSI Test Symposium*, pp. 302-310, 2002.

9. P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrate Circuits*, pp. 748-802, John Wiley, New York, 2001.

10. B. Razavi, *Design of Analog CMOS Integrated Circuits*, pp. 215-218, Mc-Graw Hill, New York, 2001

11. C. Zhang, A. Srivastava and P.K. Ajmera, "Noise analysis in a 0.8V forward body-bias CMOS op-amp design," *Fluctuation and Noise Letters* (special issue on *Noise in Devices and Circuits),* vol. 2**,** L 403-412, 2004.

12. A. Srivastava, S. Aluri and A. Chamakura, "A simple built-in current sensor for I_{DDQ} testing of CMOS data converters," *Integration, the VLSI Journal*, vol.38, no.4, pp. 579-596, April 2005.

13. URL: www.mosis.org

APPENDIX - B

SPICE LEVEL 3 MOS Model PARAMETERS FOR MOSIS 1.5 µm n-WELL CMOS TECHNOLOGY*

n-MOS Transistor Model Parameters

.MODEL NMOS NMOS LEVEL=3 PHI=0.700000 TOX=3.0700E-08 XJ=0.200000U TPG=1 VTO=0.687 DELTA=0.0000E00 LD=1.0250E-07 KP=7.5564E-05 UO=671.8 THETA=9.0430E RSH=2.5430E01 GAMMA=0.7822 NSUB=2.3320E16 NFS=5.9080E11 VMAX=2.0730E05 ETA=1.1260E-01 KAPPA=3.1050E-01 CGDO=1.7294E-10 CGSO=1.7 294E-10 CGBO=5.1118E-10 CJ=2.8188E-04 MJ=5.2633E-01 CJSW=1.4770E-10 MJSW =1.00000E-01 PB=9.9000E-01

p-MOS Transistor Model Parameters

.MODEL PMOS PMOS LEVEL=3 PHI=0.700000 TOX=3.0700E-08 XJ=0.200000U TPG=-1 VTO=-0.7574 DELTA=2.9770E00 LD=1.0540E-08 KP=2.1562E-05 UO=191.7 THETA =1.2020E-01 RSH=3.5220E00 GAMMA=0.4099 NSUB=6.4040E15 NFS=5.9090E11 VMAX=1.6200E05 ETA=1.4820E-01 KAPPA=1.0000E01 CGDO=5.0000E-11 CGSO =5.0000E-11 CGBO=4.2580E-10 CJ=2.9596E-04 MJ=4.2988E-01 CJSW=1.8679E-10 MJSW=1.5252E-01 PB=7.3574E-01

* www.mosis.org

APPENDIX - C

SPICE LEVEL 7 MOS MODEL PARAMETERS FOR MOSIS 0.5 µm n-WELL CMOS TECHNOLOGY*

n-MOS Transistor Model Parameters

.MODEL NMOS NMOS (LEVEL = 7 VERSION = 3.1 TNOM = 27 TOX = 1.41E-8 XJ = 1.5E-7 NCH = 1.7E17 VTH0 = 0.6514502 K1 = 0.8975307 K2 = -0.1023922 K3 = 21.0118887 K3B = -9.1502081 W0 = 1.027766E-8 NLX = 1E-9 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 2.813583 DVT1 = 0.4130089 DVT2 = -0.1304193 U0 = 455.604305 UA = 2.12588E-12 UB = 1.472871E-18 UC = 7.804818E-12 VSAT = 1.700249E5 A0 = 0.5923038 AGS = 0.1283106 B0 = 2.725433E-6 B1 = 5E-6 KETA = -3.75434E-3 A1 = 2.058505E-5 A2 = 0.3461214 RDSW =1.238815E3 PRWG = 0.0615689 PRWB = 0.0284451 WR = 1 WINT = 2.84243E-7 LINT = 6.883307E-8 +XL = 1E-7 XW = 0 DWG = -1.092125E-8 DWB = 2.305846E-8 VOFF = -1.469698E-4 NFACTOR = 0.8218504 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0 ETA0 = 2.022152E-3 ETAB = -1.147152E-4 DSUB = 0.0609844 PCLM = 2.5534167 PDIBLC1 = 0.89509 PDIBLC2 = 2.178635E-3 PDIBLCB = -0.0431266 DROUT = 0.9624497 PSCBE1 = 6.373594E8 PSCBE2 = 2.083578E-4 PVAG = 0 DELTA = 0.01 RSH = 82.4 MOBMOD = 1 PRT = 0 UTE = -1.5 KT1 = -0.11 KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9 UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 1.93E-10 CGSO = 1.93E-10 CGBO = 1E-9 CJ= 4.251439E-4 PB = 0.9135497 MJ = 0.4301033 CJSW = 3.024808E-10 PBSW = 0.8 MJSW = 0.2016702 CJSWG = 1.64E-10 PBSWG = 0.8 MJSWG = 0.2016702 CF = 0 PVTH0 = 0.02801 PRDSW = 184.7714978 PK2 = -0.0296629 WKETA = -0.0148191 LKETA = 2.357923E-3)

* www.mosis.org

p-MOS Transistor Model Parameters

.MODEL PMOS PMOS (LEVEL = 7 VERSION = 3.1 TNOM = 27 TOX = 1.41E-8 XJ = 1.5E-7 NCH = 1.7E17 VTH0 = -0.9466358 K1 = 0.5481062 K2 = 9.549988E-3 K3 = 8.5908941 K3B = -0.692963 W0 = 1.023511E-8 NLX = 3.508036E-8 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 2.2298106 DVT1 = 0.5218895 DVT2 = -0.1097804 U0 = 221.3803157 UA = 3.165435E-9 UB = 1E-21 UC = -5.70021E-11 VSAT = 1.991652E5 A0 = 0.9786255 AGS = 0.1693214 B0 = 7.643345E-7 B1 = 5E-6 KETA = -3.884897E-3 A1 = 1.647386E-3 A2 = 0.3009517 RDSW = 3E3 PRWG = -0.0424191 PRWB = -0.019512 WR = 1 WINT = 3.04017E-7 LINT = 9.636994E-8 XL = 1E-7 XW = 0 DWG = -2.119135E-8 DWB = 1.954661E-8 VOFF = -0.0720341 NFACTOR = 0.8541704 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0 ETA0 = 0.2210385 ETAB = -0.0921525 DSUB = 1 PCLM = 2.0466156 PDIBLC1 = 0.0503212 PDIBLC2 = 4.087026E-3 PDIBLCB = -0.051149 DROUT = 0.2274261 PSCBE1 = 1.180315E10 PSCBE2 = 1.114074E-9 PVAG = 0.1042846 DELTA = 0.01 RSH = 103.9 MOBMOD = 1 PRT = 0 UTE = -1.5 KT1 = -0.11 KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9 UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 2.62E-10 CGSO = 2.62E-10 CGBO = 1E-9 CJ = 7.230488E-4 PB = 0.9490806 MJ = 0.494932 CJSW = 2.543104E-10 PBSW = 0.99 MJSW = 0.2926045 CJSWG = 6.4E-11 PBSWG = 0.99 MJSWG = 0.2926045 CF = 0 PVTH0 = 5.98016E-3 PRDSW = 14.8598424 PK2 = 3.73981E-3 WKETA = 5.901673E-3 LKETA = -2.868828E-3)

APPENDIX - D

LIST OF PUBLICATIONS

S. Yellampalli and A. Srivastava, "ΔI_{DDQ} based testing of submicron CMOS digital-to-analog converter circuits," *Journal of Active and Passive Electronic Devices,* vol. 3, pp. 341-353, 2008.

S. Yellampalli and A. Srivastava, "ΔI_{DDQ} testing of CMOS data converters," *Journal of Active and Passive Electronic Devices,* 2008 (accepted).

A. Srivastava, S. Yellampalli, P. Alli and S. S. Rajput, "Combined oscillation and I_{DDQ} testing of CMOS amplifier circuit," *International Journal of Electronics,* 2008 (accepted).

S. Yellampalli and A. Srivastava, "ΔI_{DDQ} testing of a 12-bit recycling architecture based ADC," *Proceedings of IEEE Region 5 Technical Conference Program*, pp. 370 - 373, 2007.

S. Yellampalli and A. Srivastava, **"**A comparator-based I_{DDQ} testing of CMOS analog and mixed-signal integrated circuit," *Proceedings of IEEE International Midwest Symposium on Circuits and Systems,* pp. 179 - 182, 2005.

S. Yellampalli and A. Srivastava, "A combined oscillation, power supply current and I_{DDQ} testing methodology for fault detection in floating gate input CMOS operational amplifier," *Proceedings of IEEE International Midwest Symposium on Circuits and Systems,* pp. 503-506, 2005.

S. Yellampalli and A. Srivastava, "A simple noise modeling based testing of CMOS analog integrated circuits," *Proceeding of SPIE: Noise in Devices and Circuits III,* vol. 5844, pp. 276-283, 2005.

A. Srivastava, S. Yellampalli and K. Golla, "Delta-I_{DDQ} testing of a CMOS 12-bit charge scaling digital-to-analog converter," *Proceedings of IEEE International Midwest Symposium on Circuits and Systems*, pp. 443-447, 2006.

A. Srivastava, S. Yellampalli and V. Pulendra, "A combined noise analysis and power supply current based testing of CMOS analog integrated circuits," *Proceeding of SPIE, Noise in Devices and Circuits III,* vol. 5844, pp. 230-237, 2005.

S. Yellampall and A. Srivastava, "Testing of CMOS VLSI circuits due to manufacturing defects", *Louisiana Materials and Emerging Technologies Conference*, October 23-24, 2006. (poster paper).

VITA

Siva Yellampalli was born in Tenali, India. He graduated from Grandhi Mallikarjuna Rao Institute of Technology, an affiliate to Jawaharlal Nehru Institute of Technology, Hyderabad, India, with a degree in Bachelor of Technology in Electrical and Electronics Engineering in June 2001. After he received his undergraduate degree, he enrolled in the Department of Electrical and Computer Engineering at Louisiana State University, Baton Rouge, Louisiana, in August 2002 to attend graduate school. He received a Master of Science degree in December 2004 before beginning a doctoral program. His research interests include analog and digital integrated circuits design and testing.