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The design and fabrication of pentacene acoustic charge transfer devices

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THE DESIGN AND FABRICATION OF PENTACENE ACOUSTIC CHARGE TRANSFER DEVICES

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

Acoustic charge transport (ACT) devices are used to transfer electrical signals by surface acoustic waves (SAW), which are generated by interdigital transducers (IDT) on piezoelectric crystal substrates. In order to reduce fabrication cost, pentacene ACT is desired to transfer charge packages because of its reduced cost in. As some researchers reported, pentacene is a p type organic semiconductor, and can get high carrier mobility by growing in very pure crystalline structure under some specified growing conditions. In this project, charge transfer channel was made of crystal pentacene to form and carry the charge packages following SAW propagation.

The pentacene ACT consists of IDT, input/output probes, metallic parabolic horns, and pentacene charge channel which are deposited on lithium niobate ($LiNbO_3$) piezoelectric substrate. In addition, the frequency of SAW in this device was designed to be 284 MHz. IDT and probes were made by bilayer lift-off process, and the resolution is 3 μm. The pentacene channel was deposited through a silicon shadow mask in thermal evaporator. Some facilities were designed for the above process, such as chromium glass masks, print out film mask, and $LiNbO_3$ wafer holder. Semiconductor fabrication techniques such as photolithography and wet/dry etch were also involved in making this device.

Another project, Gallium arsenide epitaxial film is also under consideration to be charge transfer channel in ACT. This project involved epitaxial film lift-off and wafer or film bonding technique. Further work will be required to produce this device.

1 INTRODUCTION

This project focuses on fabrication of a surface acoustic wave (SAW) device to transfer electric signals. Normally, SAW devices can be implemented as filters, oscillators, transformers, and sensors due to its ability to transduce electric energy to mechanical energy. Generally, piezoelectric materials play an important role in the energy transduction. Currently, SAW filters are successfully utilized in cell phone market. In addition, SAW sensors can also be found in chemical, optical, thermal, pressure, acceleration, torque and biological research areas [1].

1.1 SAW Devices

The inventor of SAW is Lord Rayleigh, who was the first person to confirm that SAW is an elastic vibration in solid material surface in 1885. Before Rayleigh published his research on SAW, the piezoelectric effect, which is the basic technique for SAW, was already discovered by Curie brothers in 1880 [2]. Actually, piezoelectric effect is about energy transfer, transferring electric energy to mechanic energy and vice versa. Under the Curie brothers' classical experiments in Laboratory of Mineralogy, Sorbonne, the definition of piezoelectric effect was described: mechanical stresses can produce electric fields, and oppositely, electric fields can also cause mechanic stresses or strains on piezoelectric crystalline insulators [3]. According to the principle of piezoelectric effect, acoustic wave can be generated by alternating current (AC) electric field on a piezoelectric substrate by interdigital transducer (IDT). As the acoustic wave propagating along the surface of the substrate, the wave amplitude decays approximately exponentially with the depth of the piezoelectric substrate [1]. Normally, acoustic wave devices work in a frequency ranging from 10 MHz to 1 GHz [4].

Since SAW devices have a wide frequency range, SAW sensors are ideally produced at a high frequency to achieve a high speed response. However, many applications are required to slow down the signals in order to have time to treat the signals. Therefore, the variety frequency of SAW attracts many researchers to achieve their expected purposes.

After the inventor of SAW, a lot of scientists have been working on it and developing into diverse applications. One of the first applications is ultrasonics, developed by Langevin who made acoustic wave travel through water and receive the wave signal. This technique is utilized in many applications, such as medical imaging and material character analysis. Another important SAW application is piezoelectric resonator, produced by Cady in 1910s, become the foundation technique of radio transmission and electronic filter. For military application, SAW was developed to delay lines for radar and sonar applications in 1950s. Moreover, SAW was cooperated to microelectronics in 1960s, White and Voltmer [2] used lithography method to make interdigital transducers on piezoelectric substrates to generate SAW. With advancing lithography technique, SAW manufactures are able to create SAW device at a high frequency in the recent years. Therefore, SAW devices are widely applied in telecommunications operated as a filter, demodulator, and oscillator. Furthermore, in the field of high frequency telecommunication, the main application of SAW diverted to military for radar and sonar [2]. The other important application of SAW is chemistry sensor, which is for gas and liquid-phase analysis [2].

In this project, the main task is to design, fabricate, and test a SAW device, which transfers a variety signal processing through a lithium niobate subtracts. It is expected to be working at 284 MHz frequency.

1.2 Thesis Organization

The thesis consists of six chapters. Chapter 2 introduces the foundation of SAW devices, which involved the generation of SAW, ACT transfer electrons packages, and the power requirement of SAW. Chapter 3 is about design of pentacene acoustic charge transport device. It describes how to design IDT, parabolic metalized horn beamwidth compressor and pentacene charge transfer channel. Chapter 4 is the main body of the thesis, which described the fabrication process of the expected pentacene ACT device and related discussions. Chapter 5 is another ACT project, GaAs epitaxial film charge transfer channel on $LiNbO_3$, which will be accomplished in the future. Finally, the last chapter is conclusion and future work.

2 FOUNDATION OF SAW DEVICES

SAW devices normally consist of piezoelectric substrate, IDT, acoustic charge transfer (ACT), and accessories, which work together to generate SAW, transfer SAW with electrical signals (charge packages), and output the proper signals.

2.1 Piezoelectric Material

According to piezoelectric effect, SAW have to be excited by AC electrical field on a piezoelectric material, and propagate along the surface of the substrate according to piezoelectric effect principle. During the transfer period, piezoelectric material works as a mass-spring system, in which some electrons are displaced by the input electric field, as result of the expected transferring signal. Since the bonding situation of a particle at surface is different from internal particles in the material, the surface particles can form an acoustic wave bound to the surface, and the wave will approximately exponentially decay beneath the surface of piezoelectric substrate. SAW can propagate in two plane boundaries in a solid plate [5]. The following figure 1 shows that three kinds of waves propagate in solid. Figure 1 (a) is an ideal bulk longitudinal wave, figure 1 (b) is an ideal bulk transverse wave, and figure 1 (c) is the SAW present in piezoelectric substrate. In particular, λ is the wavelength as displayed in the figure 1.

The piezoelectric materials commonly used in SAW devices are single crystalline, such as quartz, lithium tantalate ($LiTaO_3$), and lithium niobate ($LiNbO_3$). During waves traveling in the substrate, they can be influenced by reflection, deflection, absorption, and waveguide, etc. These interferences lead to insertion loss, thereby requiring high power input in order to have been able to transfer signals as expected [6]. In order to achieve

low cost while preserving accuracy, the materials with high piezoelectric coupling coefficient (k^2) and high propagation velocity (ν), such as the above mentioned materials are mostly selected by SAW devices. Table 1 [7] lists the piezoelectric parameters of some materials. In this project, lithium niobate was chosen as the substrate because of its high k^2 and fast ν.

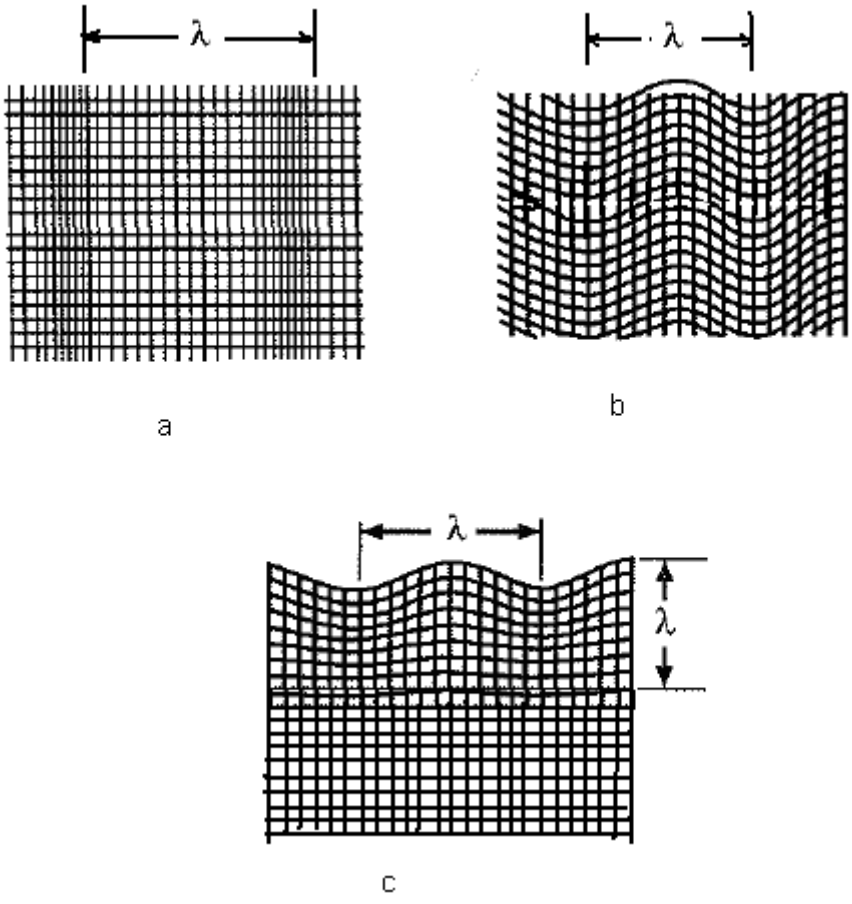

Figure 1 Representations of elastic waves in solids. (a) Bulk longitudinal wave. (b) Bulk transverse wave. (c) Surface wave. (edited from [5])

Table 1 Property of piezoelectric substrates [7]

Substrate	Propagation Velocity ν (m/s)	Piezoelectric Coupling Coefficient k^2 %	Temperature Coefficient of Frequency, TCF (ppm/°C)
Quartz (ST-X)	3158	0.14	0
$LiNbO_3$ (128° Y-X)	3992	5.3	-75
$LiNbO_3$(Y-Z)	3488	4.5	-94
$LiTaO_3$ (X-112° Y)	3288	0.6	-18
$LiTaO_3$(Y-Z)	3254	0.72	-35
AIN Film (C-axis)	4800	0.15-0.8	-26
ZnO Film (C-axis)	2600	0.6-1.9	-25
Mg-doped GaN Film (C-axis)	5806	4.3	-18.3

2.2 Interdigital Transducer (IDT)

The IDT is used to make a transducer for SAW devices. It is the simplest way to excite and receive SAW on a piezoelectric substrate. Generally, the IDT consists of two interleaved metallic fingers as shown in figure 2. The left one is input IDT, which can generate SAW by supplied AC voltage, and the right one is output IDT, which can pick

up SAW to electrical signal properly. However, the two interleaved metallic fingers are connected to two different probes to form electrical fields between the fingers.

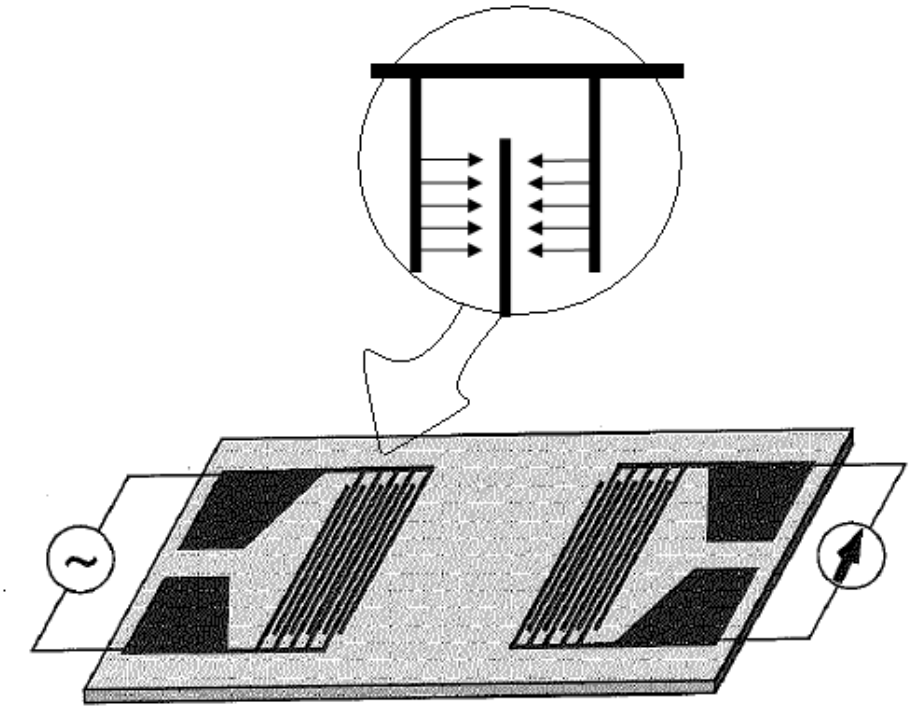

Figure 2 Typical SAW device with two IDTs. (after [2] with additions)

When the AC voltage creates electric field between IDT fingers in the input IDT (left IDT in figure 2), due to piezoelectric effect, mechanic strains present as waves on the surface of substrate, and the waves propagate across the substrate at critical speed that varies depending on the material. On the output IDT (the right IDT in figure 2) fingers, the mechanical strains also can generate electric field between the fingers, and output electric signals by the output IDT. This SAW transmittal process is schematically

depicted in figure 3 as following. In particular, the SAW relationship of wavelength and propagation velocity is:

$$\lambda = \frac{v}{f} \tag{2.1}$$

In the above equation, λ is the SAW wavelength, ν is the propagation velocity, and f is the center frequency.

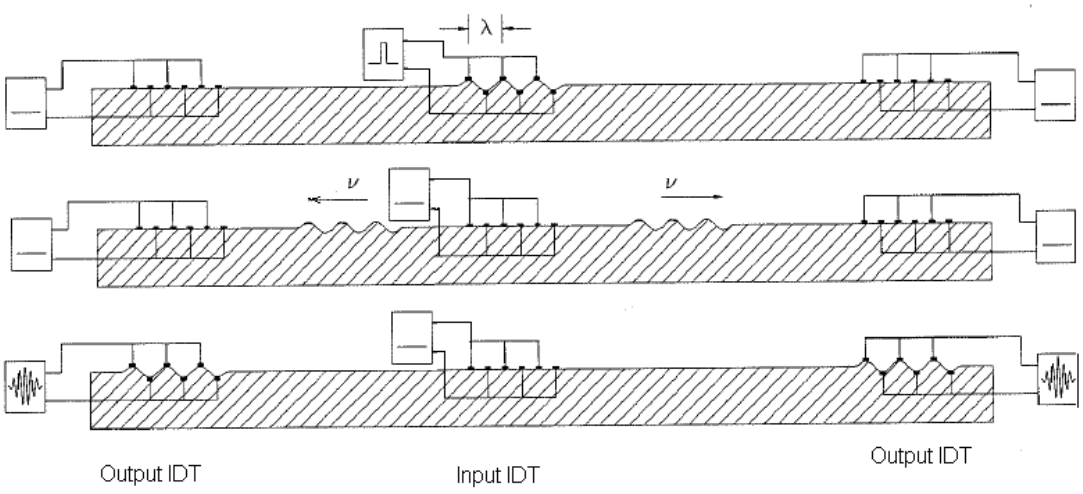

Figure 3 Schematics of SAW transmittal process. (edited from [3])

In practice, IDTs can be designed for a variety of applications. For example, filters, resonators, and delay line used different IDT styles. The following figure 4 displays some of the most important SAW devices developed recently [7].

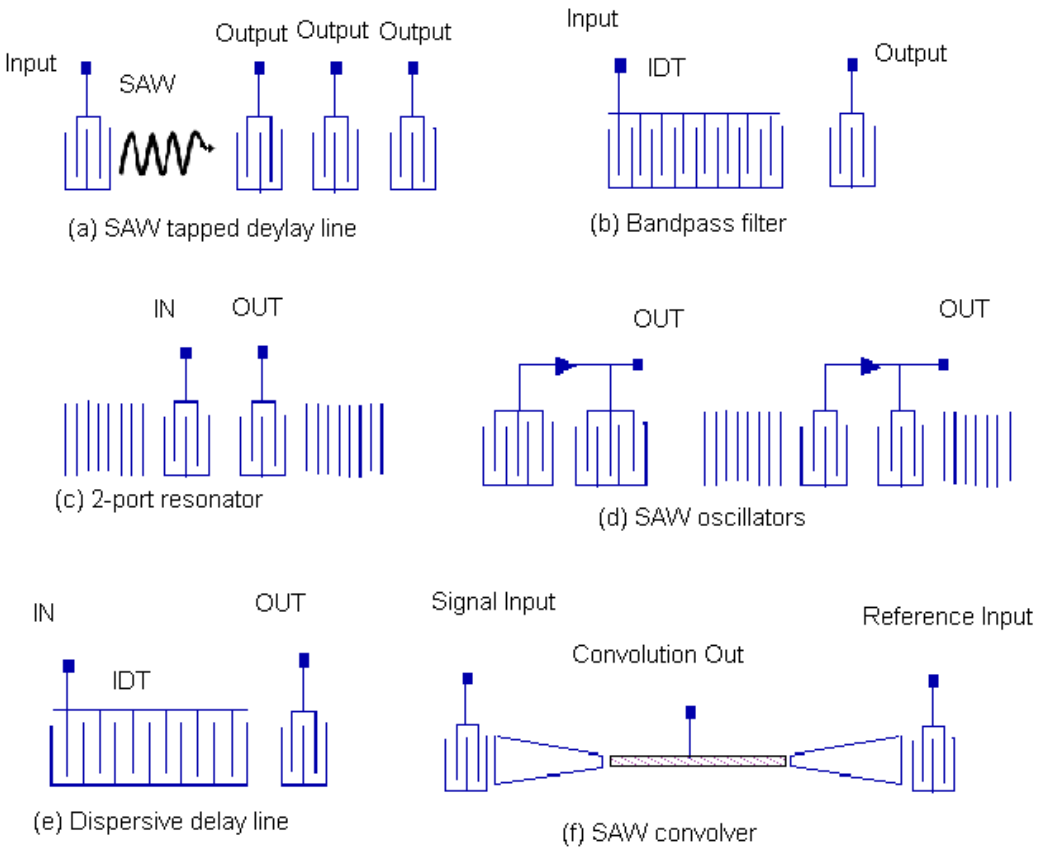

Figure 4 Typical IDTs in practice. (edited from [7])

2.3 Acoustic Charge Transport (ACT) Working Principle

A sinusoidal potential is created properly when SAW travels through a thin semiconductor layer. This layer is normally called transport channel, which needs a sharp interface on the piezoelectric substrate. At this point, each positive peak of the potential

can bunch electrons together and pushes them through the transport channel while the SAW is traveling. A delay line is a simple type of ACT device, whose operation is easily understood by the illustration in figure 5.

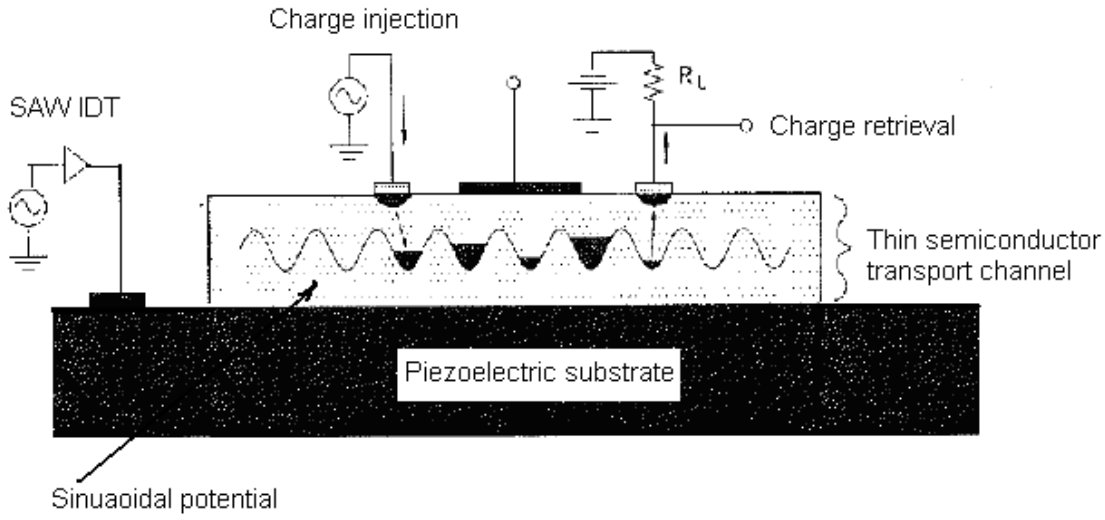

Figure 5 Cross section of an ACT delay line. (edited from[3])

There is no difference in electron packages transported by the SAW if no signal is present on the transport channel. Otherwise, the confined packets of charges can be changed by supplying voltages through ohmic contacts on the transfer channel. Each signal voltage applied to the Schottky contact controls the amount of electrons in each packet, SAW potential "well". These electron packets are transported through the channel at the SAW velocity, and represent the basic input electrical signals. The ohmic contacts (output IDT) at the end of the channel collects the charges from the passing wells, and recreates a signal delay, which is proportional to the length of the channel [8].

2.4 Power Requirement of SAW Devices [9]

The purpose of ACT is to transfer electron packages through the transport channel with the SAW. In order to transport the electron packages from the input IDT to output IDT continually and without corruption by a SAW, the peak to peak amplitude of the SAW must be large enough to avoid electrons from "leaking" between the SAW potential wells. The relationship of the electric field and the SAW potential amplitude is as following:

$$E = \frac{2\pi V}{\lambda} \tag{2.1}$$

In the above equation (2.1), λ is the SAW wavelength, and V is the amplitude of the piezoelectric voltage generated on the surface of a substrate by the SAW. In addition, V also can be described as: [10]

$$V = \Phi_0 \sqrt{(P/A)/2\pi f} \tag{2.2}$$

In the above equation (2.2), Φ_0 is the normalized electric potential coefficient, f is the SAW center frequency, P is acoustic SAW power and A is the length of the transducer's acoustic aperture perpendicular to the SAW propagation direction. Substituting (2.2) into (2.1), following equation is obtained:

$$E = \frac{2\pi\Phi_0}{\lambda}\sqrt{(P/A)/2\pi f}\ . \tag{2.3}$$

According to the above equation (2.3), a relationship between the electric field E and the SAW power P can be deduced. It means that if a minimum value of the electric field E is required, the SAW power P also has a minimum requirement. This requirement is affected by two parameters.

The first parameter is the charge mobility, which requires that the electric field must be strong enough to push the electrons at the velocity of the SAW in the transport channel. This criterion can be shown by the following equation:

$$E > v/\mu \tag{2.4}$$

In the above equation (2.4), v is the velocity of the SAW and μ is the carrier mobility in the transport channel. Substituting (2.4) into (2.3), the relationship of SAW power with SAW velocity and carrier mobility is shown as:

$$P/A > \frac{\lambda v^3}{2\pi\mu^2\Phi_0^2} \tag{2.5}$$

The above equation (2.5) gives the minimum SAW power required per unit length of acoustic aperture, *P/A* that can satisfy the first criterion.

The second parameter is the thermal criterion, to prevent electrons in charge packages from diffusing to their neighbor packages, which can affect initial electrons amount in each packages. It means that the potential difference between SAW troughs

and crests must be much larger than the thermal energy in order to obstruct the electrons' diffusion between adjacent charges packets. Generally, the charges are limited in two dimensions, and are only free in one dimension. Therefore, the thermal energy, $\sim k_B T$, (where k_B is Boltzmann's constant, and T is absolute temperature) divided by electron charge should be the potential voltage. Since the required V must be greater than $k_B T/e$, say $V=10k_B T/e$. The minimum SAW power required per unit length of acoustic aperture is

$$P / A = 2\pi f \left(\frac{10 k_B T}{e \Phi_0} \right)^2 \tag{2.6}$$

2.5 The Type of Acoustic Charge Transport

The function of ACT channel is not only to offer a place to transfer charge packages with SAW, but also to limit them traveling only in the channel, and will not allow any other current to go around the channel. In the ACT developing history, several types of them were studied and applied in industries and research works. They are thick-channel, backgating, double heterojunction, single heterojunction, and petancene ACT etc., which will be introduced in the following sections.

2.5.1 Thick-channel ACT

The earliest ACT channel reported was a thick-channel with light n type doped region with a p type GaAs layer underneath and a metal layer on the top of the GaAs. The structure is shown in the following figure 6. The junction is reverse-biased, and both of doped GaAs depletion edges just touch. At this point the SAW can carry the electrons packages, which are affected by the electric input signal on the channel plate.

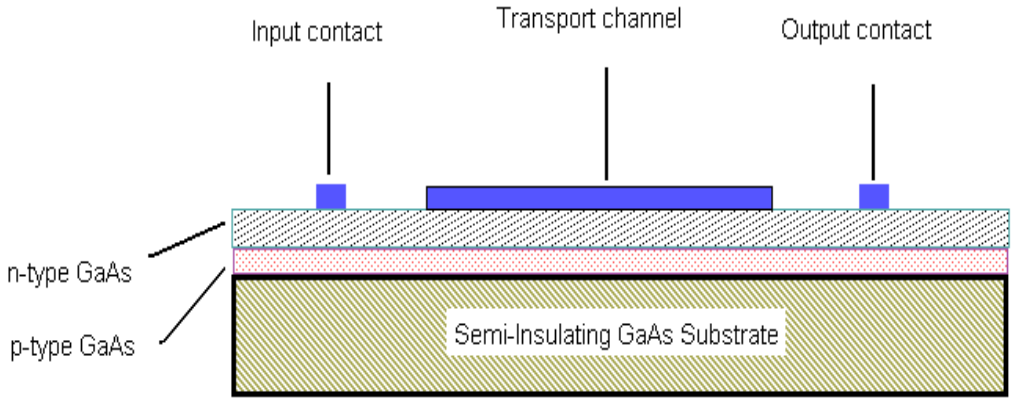

Figure 6 Schematics of epitaxial thick channel ACT structure. (edited from [3])

2.5.2 Backgating ACT

By inspection, the p type region in the above thick channel ACT will not have a uniform depletion region, and the potential distribution is also affected by the SAW when it travels through the channel. Therefore, the electrons packages can not exactly represent the input signals. In order to avoid the problem caused by p type layer, a backgating structure ACT channel was used later. Its cross section is displayed in figure 7 [3].

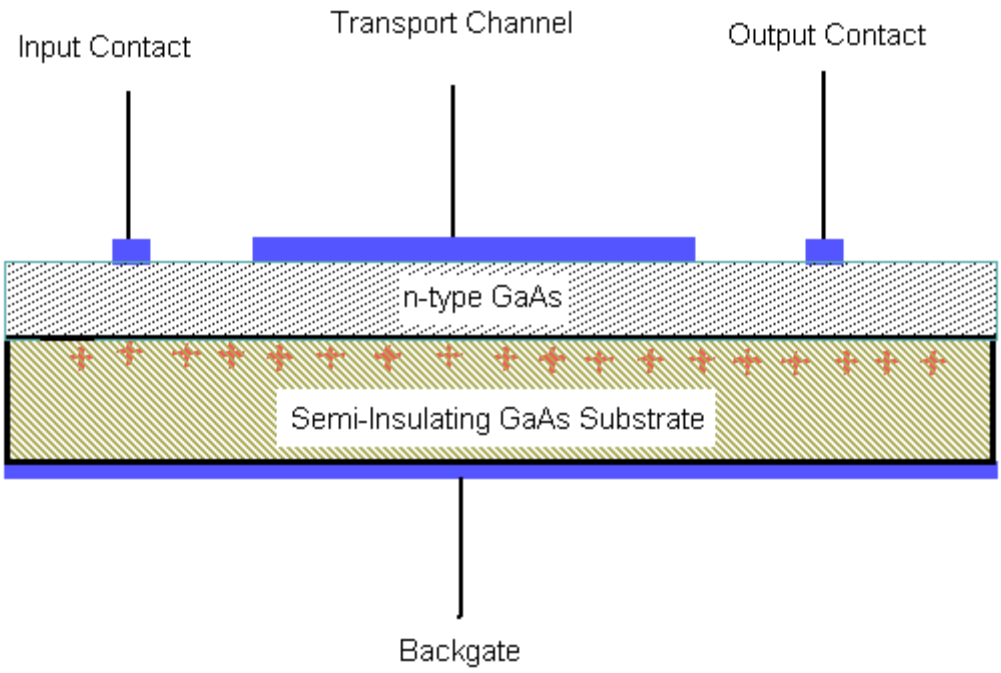

Figure 7 The backgating ACT structure. (edited from[3])

2.5.3 Double Heterojunction ACT (HACT)

Though the backgating ACT structure solved the p layer problem, it is difficult to achieve the uniform doping profile in the epitaxial n type layer. This can not produce uniform electron packages even through no input signal introduced. Therefore, the SAW can not push the proportional electron packages with the input signals through the device.

In order to get uniform charges distribution in vertical direction, quantum well technique was introduced to ACT transport. According to GaAs high mobility and different bandgap but similar crystal structure composition material, AlGaAs, the GaAs/AlGaAs hetero layered ACT was introduced as charge channel [11]. The schematic HACT was displayed in figure 8 and 9.

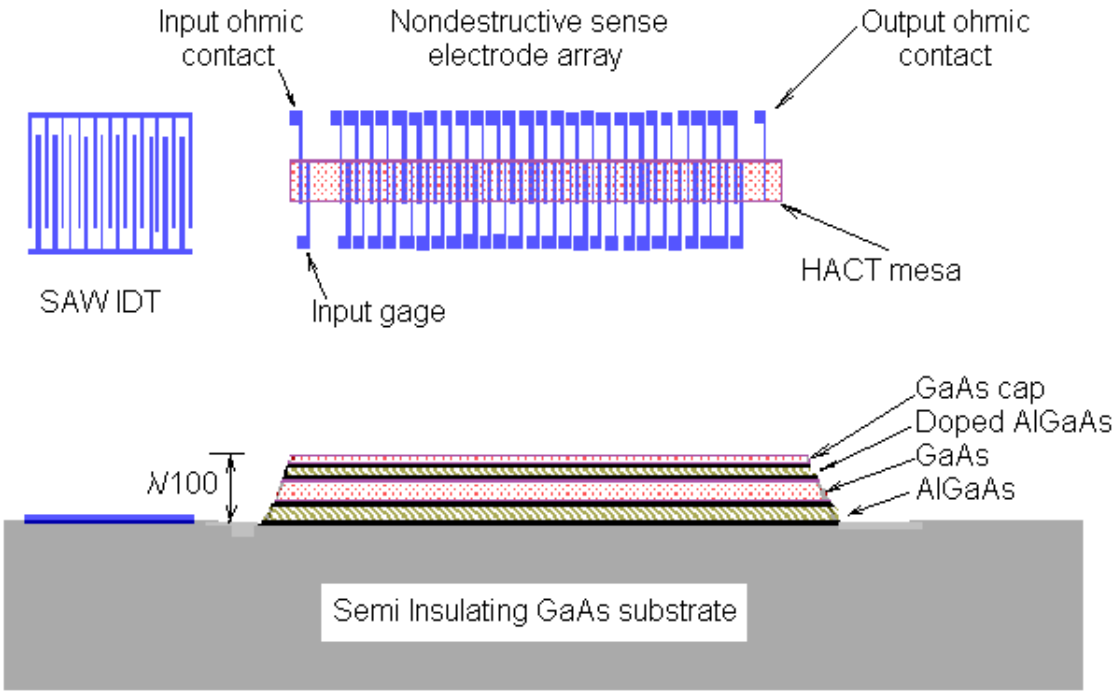

Figure 8 Typical heterojunction ACT cross section structure. (edited from [3])

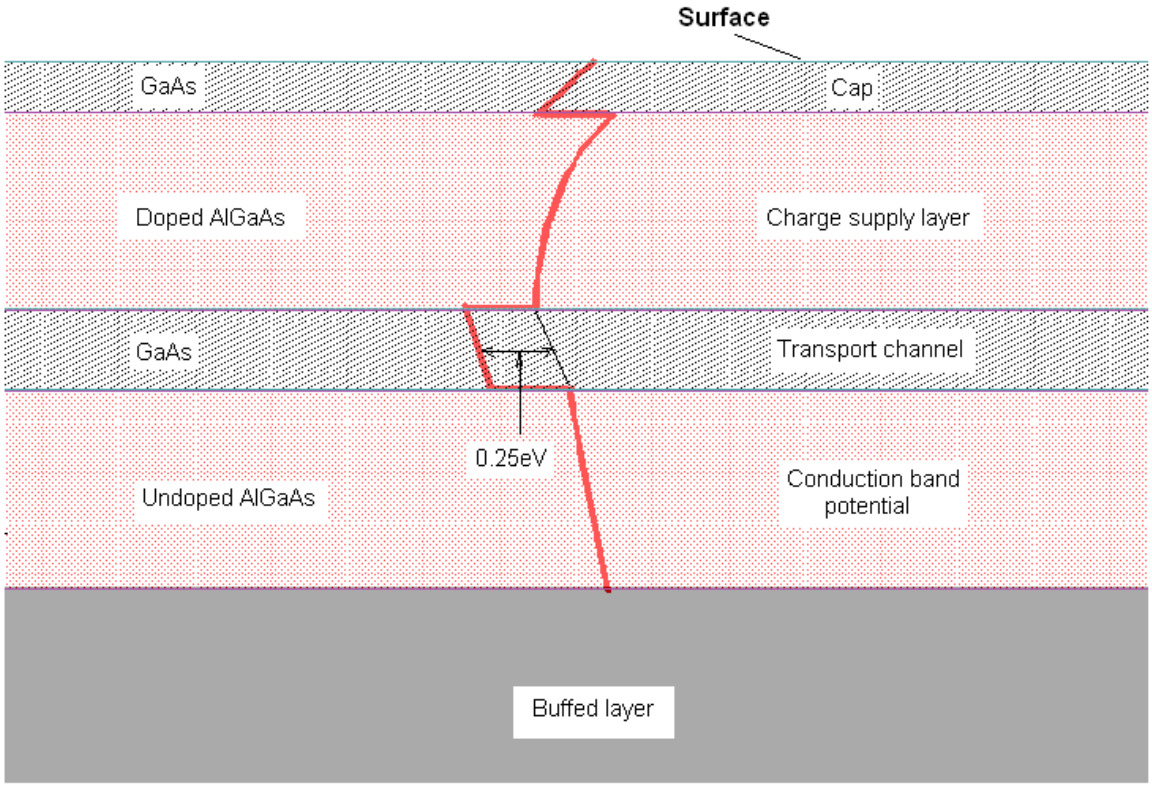

Figure 9 HACT quantum well of GaAs/AlGaAs. (edited from [11])

Normally, the bandgap of GaAs is 1.42 eV at 300K, and $Al_xGa_{(1-x)}As$ depends on the fraction x. For example, if x =32%, AlGaAs conduction level is 0.25eV, higher than GaAs [11]. The quantum well structure is shown in detail in figure 9.

In figure 9, quantum well is formed in the layer of GaAs (Transport channel). Therefore, the electrons in the layers of AlGaAs drift to the transport channel by the effect of electron potential. In this way, electrons are trapped to the transport channel, forming the uniform charge transport channel.

2.5.4 Single Heterojunction ACT

Though double heterojunction ACT can get uniform charges in the transport layer, the double heterojunction ACT has no practical advantage over single heterojunction ACT [12]. Therefore, single heterojunction was studied as a practical ACT channel structure. Its schematics are demonstrated as following figure 10. According to the property of quantum well, electrons will drift to the undoped GaAs layer to form a uniform electron transport channel [13].

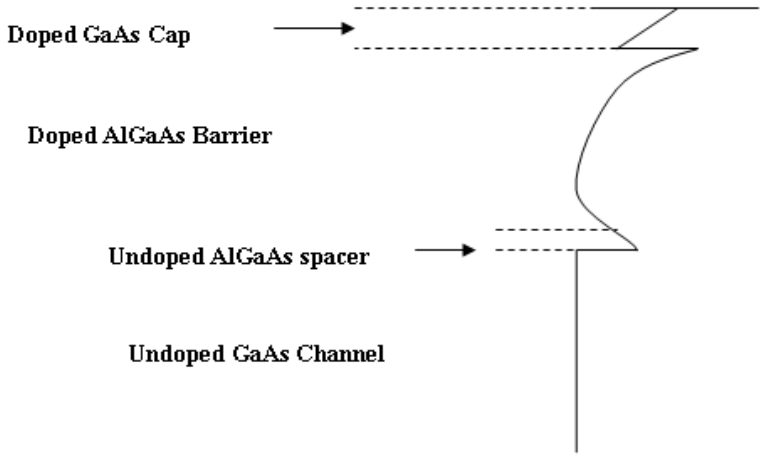

Figure 10 Schematics of single heterojunction ACT structure.

2.5.5 Pentacene ACT

A heterojunction ACT must be produced by molecular beam epitaxial (MBE), which is expensive and complex. Therefore, heterujunction ACT has less practical advantage for further development. Thus, monolayer ACT is studied due to its easy form and low cost. Pentacene channel, due to its high mobility fro an organic material, easy

and low temperature fabrication, becomes a potential high active charge transfer material in recent years. ACT will be introduced in the next chapter in detail, because this project will use pentacene channel to transfer charges.

3 DESIGN OF PENTACENE ACOUSTIC CHARGE TRANSPORT DEVICE

In this project, the desired ACT devices consist of IDT, input/output probes, pentacene ACT channel, and SAW beam compressor.

3.1 Design Interdigital Transdusor (IDT)

SAW are produced by radio frequency (RF) voltage supplied by interdigital transducers (IDT) which are placed on piezoelectric substrate. The IDT consists of two interleaved metallic finger electrodes. The two group probes are connected to the RF voltage to generate oscillating electric field on the surface of the substrate, and cause oscillating mechanical stresses in the substrate, by the piezoelectric effect. The oscillating mechanical stresses are the surface acoustic wave (SAW), which can be used to transfer electrons packages in semiconductor. The transferred electron packages were explained in detail in section 2.3.

The design and fabrication of IDT was accomplished by Xu [18], and the fabrication part is optimized in this thesis, including bi-layer lift-off process on lithium niobate substrate and improvement of the successful rate and resolution.

Because the purpose of IDT is to supply electric field to the piezoelectric substrate, the IDT must have low resistance. Therefore, aluminum was selected to make the IDTs due to its low resistance and good adhesion to lithium niobate, and it is inexpensive. In order to reduce insertion loss, the number of IDT electrodes and thickness of IDT metal layers are also under consideration. By computer simulation [14], while the number of IDT electrodes and the thickness of IDT metal layers increase, minimum insertion loss will increase, but the center frequency at minimum insertion loss will decrease. In addition, as the result of the program simulation [15], the aperture of IDT is

required as big as about 50 λ to avoid SAW diffraction. In order to obtain less insertion loss and high center frequency, in this project, the number of IDT electrodes is 30, and 200 nm thickness aluminum metal layers were carefully chosen as required. The aperture of IDT is 30λ (λ=12μm), 360 μm followed practical experiences.

There is other factors should be under consideration, such as SAW power. In section 2.4, the requirement of SAW minimum power per unit length was described in equation (2.5) as: $P/A > \frac{\lambda v^3}{2\pi\mu^2\Phi_0^2}$. According to Lithium niobate (X-Y) propagation velocity ν in Table 1, Z direction propagating velocity, ν=3488m/s, normalized electric potential coefficient Φ_o=14500Vm$^{-1/2}$J$^{-1/2}$ [16], and the pentacene carrier mobility at room temperature vacuum deposition is μ>10^{-4} m^2/Vs [17], the SAW need power per unit length is 3.86×10^{4}W/m. As Xu [18], the IDT will generate SAW to propagate in two opposite directions. Therefore, the required power per unit length should be 7.72×10^{4}W/m, and multiplying by 360 μm (the IDT aperture width) to get the total power of 27.8 W. This is too high for efficient operation, and also too high for most IDTs to handle (maximum ≈3 W in practice). In practice, there are several techniques to compress SAW beamwidth to achieve a high SAW power density in the transfer channel. As the analysis by Xu shows [18], a thin-film metalized straight edge horn, thin-film metalized parabolic horn, multistrip coupler, and chirped IDTs were considered. Finally the parabolic metalized horn method was chosen due to its easy design.

3.2 Design Parabolic Metalized Horn Beamwidth Compressor and Pentacene Charge Transfer Channel

According to Xu's calculation [18], SAW beam have to compress to 3λ aperture, and in order to avoid compressed wave from diffracting to large apertures, a topographic

waveguide is required. The analysis and calculation is clearly described in section 5.2 of Xu's thesis [18] and Auld [16]. The parabolic metalized horn will compress SAW from 12λ aperture to 3λ aperture to reduce the required electrical drive power, and get high SAW power density. In addition, the pentacene waveguide can slow the propagating velocity of the SAW, and limit the SAW waves only to transfer within the waveguide channel. The operation principle of parabolic SAW beam compressor is shown in the simple schematics in figure 11. The figure shows the wave's reflection tracks in both of the horn and waveguide, and the important factor is to let the waveguide achieve total the internal reflection of the SAW beam. In particular, the transfer velocity in the horn and waveguide is slower than that is outside, which is caused by the extra mass of the Aluminum horn and pentacene channel.

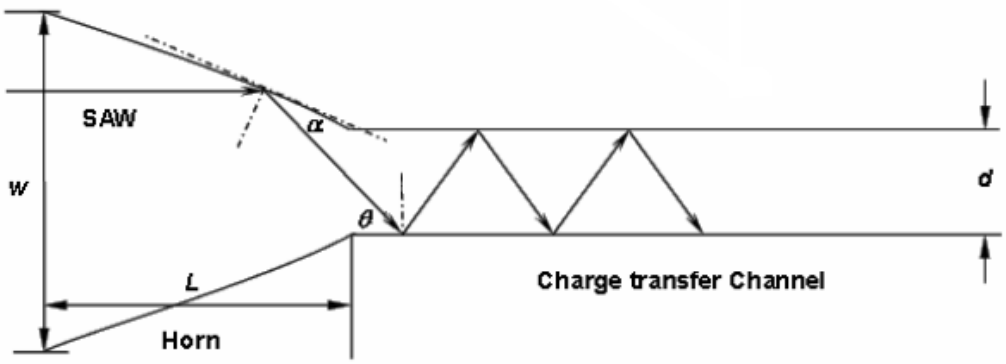

Figure 11 The schematics of parabolic horn and charge transfer channel. [18]

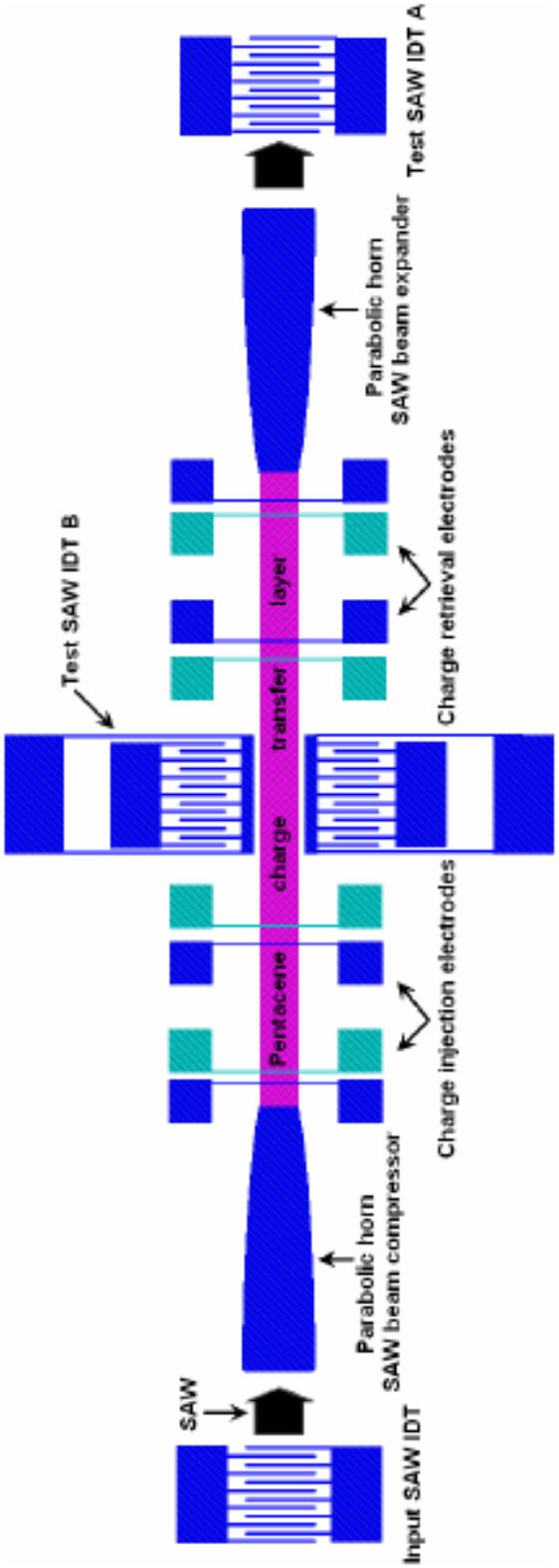

Figure 12 The schematics of pentacene ACT device. [18]

According to Xu's calculation, the pentacene is 3λ (36μm) width, 6mm length, and 1 μm thickness. The total device schematics are shown in figure 12 as the previous page. From the bottom of the figure, the carrier SAW is generated by the input SAW IDT, and compressed by horn SAW beam compressor to increase the SAW power density. After being compressed, the SAW propagates through the pentacene charge transfer while electric signals (electron packages) are injected to the passing SAW "well" by charge injection electrodes. Afterwards, the SAW, which is with electric signals, is expanded by SAW beam expander and go through the test SAW IDT A (output IDT), which can pick up the electron packages and output the electric signals injected in pentacene layer. Additionally, some test accessories like test electrodes and test IDTs are also set in the device for the further device measurement.

4 FABRICATE PENTACENE ACOUSTIC CHARGE TRANSPORT DEVICE

In order to fabricate the pentacene ACT device as described in Figure 12, there are three layers to make. The metal layers are used to form ohmic contacts. In order to reduce power loss, the contacts must have less resistance. In practical, Al and Au are chosen because of their good adhesion and conductivity. Using IDT to generate SAW is a complex process, the material and thickness of electrodes of IDT are the main factors, which can affect the power loss. Au can make much power loss than Al [19]. Therefore, IDT normally are made of Al, and Au is used to be ohmic contact pads for the further packaging purpose. The first layer, Al layer (blue) includes the SAW IDT, SAW beam compressor, and charge injection/retrieval electrodes. The second layer, Au layer (green) includes charge injection/retrieval electrodes and ohmic contact pads. The last layer (pink) is the pentacene charge transfer layer.

However, micro-scale resolution devices normally involve photolithography technique, and some specialist equipment required to accomplish the work, such as lithography masks. In this project, there are two chromium glass masks used to fabricate the first two metal layers. These include three sizes of cross alignment markers in each mask to adjust the exact position between the different layers. In addition, a silicon shadow mask and $LiNbO_3$ wafer holder were designed to deposit the pentacene channel on the right position. Finally, some high resolution patterns were printed on a transparency to be the UV mask in lithography process to make the above mentioned silicon shadow mask.

Likewise, there are several specific fabrication methods chosen to build the device. First, lift-off process technique was used to form the metal layers, which include Al and Au layers. Second, the pentacene layer has to use a shadow mask to form the

patterns because pentacene will be dissolved by any organic solution so that conventional photolithography could not be used. However, the shadow mask fabrication used wet/dry etches processes in order to meet the requirement of the pentacene layer. In this chapter, the fabrication technique will be described in detail.

4.1 Lift-off Process

According to Xu's experiment [18], the prior standard lift-off process had to be improved to a bilayer lift-off process because of poor success with lift-off for Al or Au layer from photoresist and deposition evaporator equipment NRC 3177 available, previous work used an e-beam depositor, BJD1800 producing well-directed evaporation [18]. At this point, there is a need for a reliable undercut lithography construction to successfully separate the unwanted regions from the desired patterns.

Up to now, there are two kinds of lift-off process, which can form undercut after develop in UV lithography, Chlorobenzene and bilayer lift-off.

4.1.1 Chlorobenzene Lift-off Process

Lift-off is a simple way to deposit patterned thin film on substrate. The patterns are formed by photoresist using photolithography technique on substrate. Afterwards, the thin film, usually metallic film, is deposited all over the substrate. While, only the film where the photoresist is already removed and can directly adhere to the substrate, the others are covered to the photoresist. When the sample immersed in chemical remover, photoresist will be dissolved and removed with the metal. Therefore, the metal patterns are deposited directly on the substrate. Unfortunately, the standard photoresist lift-off by itself can not completely separate the IDT fingers. This is because the isotropic (random

direction) thermal evaporation will deposit the metal not only on the substrate and horizontal photoresist layer, but also on the photoresist sidewall, which is formed at the edges of the patterns with an angle less than 90°. Since the metal film on sidewall, the expected part of metal will connect to the sacrificial layer, which is just on the photoresist layer, and some of the metal on sidewall will survive after photoresist is removed. These result in the rough edges of the patterns.

In order to separate the desired patterns completely, an overhang profile is required of the photoresist. After exposing the sample under UV aligner and before development, the sample is immersed in chlorobenzene solution, the top of the photoresist will absorb more chlorobenzene and reduce the dissolved rate in developer. The different dissolve rate will form overhangs on the photoresist surface [20] [21]. The following figure 13 shows the profile of the photoresist overhang profile.

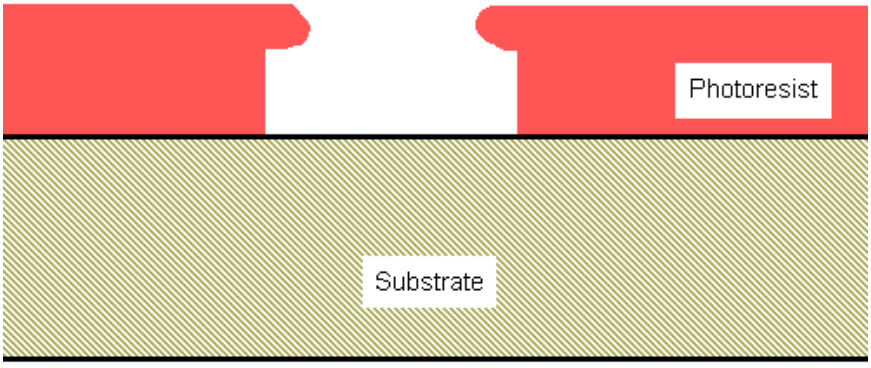

Figure 13 Overhang profile of photoresist in chlorobenzene lift-off.

The chlorobenzene lift-off operation process is as the following.

1. Micro Chem S1813 was spun at the speed of 2500RPM to get 1.5 um thickness photoresist layer. This was soft-bake at 110°C for 2min.
2. UV exposure by Karl Suss, MJB3 for 18 second at 13.5 mW/cm^2.
3. Sample immersed in chlorobenzene at room temperature for 16 minute.
4. Dried with nitrogen gas.
5. Developed in Micro Chem MF 319 for 5 minute.
6. Rinsed in DI water and dried by nitrogen gas.
7. Al layer 200 nm thickness thermally evaperated.
8. Lift-off in Micro Chem 1165 remover for 20min at 60°C and ultrasonic for 2 minute.
9. DI water cleaned and nitrogen dried.

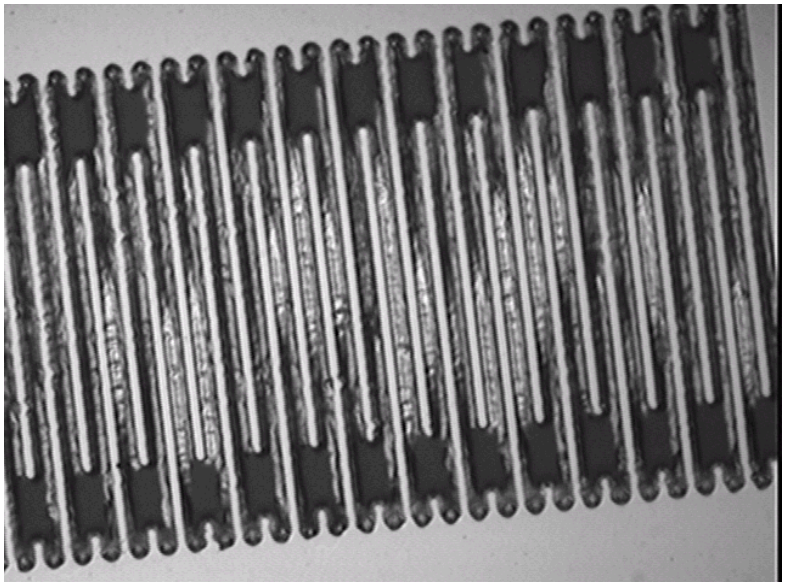

Figure 14 Schematics of chlorobenzene lift-off IDT result.

Some patterns are desired after chlorobenzene lift-off, such as electrodes, but a few patterns still get wings on them as the figure 14, especially in IDT patterns. This result probably was caused by the high density fingers. Therefore, chlorobenzene lift-off is not reliable in high density patterns.

4.1.2 Bilayer Lift-off Process

Since chlorobenzene to harden the surface of photoresist is not reliable in the IDT making, the bilayer lift-off process is introduced here. This is the best way to get undercut profile in lift-off.

Photoresist (S1813), lift-off resist (LOR 3B), developer (MF 319), and remover (1165 remover), supplied by MicroChem, are needed [22]. This method can get very reliable lift-off result by its constant undercut size. In this process, in order to properly get undercut, the LOR resist bake temperature and time are very important. Because these two parameters determine the develop time and undercut size, which should be handled easily by hand. The MicroChem LOR data sheet is based on silicon wafer substrate. For the $LiNbO_3$ substrate, the temperature can not be very high because it is easy to crack during the cooling period. Therefore, here the bake temperature is chose to be the lowest limit, 150°C. The bake time, 12 minute obtained by the easily controlled developing time, 50 second. The following is the process in detail.

1. Micro Chem LOR 3B spun at 2500 RPM to get about 500 nm thickness layer. Soft-baked at 150°C for 12 minute.
2. S1813 spun at 2500 RPM to get 1.5 μm layer. Soft-baked at 110°C for 2minute.

3. UV exposure by Karl Suss, MJB3 for 18 second at 13.5 mW/cm^2.

4. Developed in MF 319 for 50 second.

5. Rinsed in DI water.

6. Dried by nitrogen.

7. Thermal evaporated Al layer of 200 nm thickness.

8. Lift-off in 1165 remover for 20minute at 60 °C and ultrasonic for 2 minute.

9. DI water cleaned and nitrogen dried.

The figure 15 shows the bilayer operation process [23]. This shows how LOR 3B lift-off resist can separate the desired patterns from the undesired film.

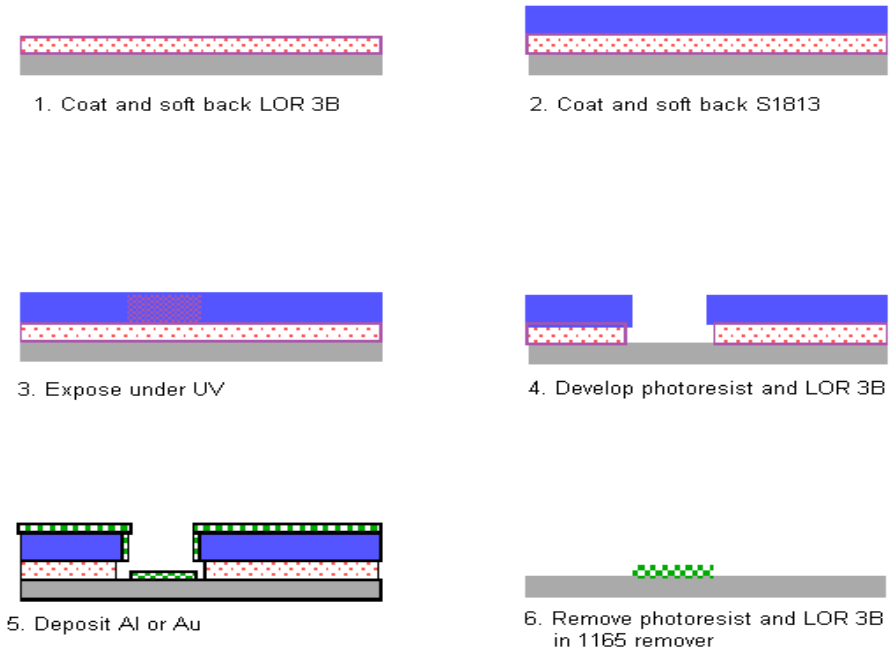

Figure 15 Schematics for bilayer lift-off process.

Using bilayer lift-off method, clear patterns can be obtained everywhere on the substrate. The following figure 16 shows the IDT fingers under optical microscope.

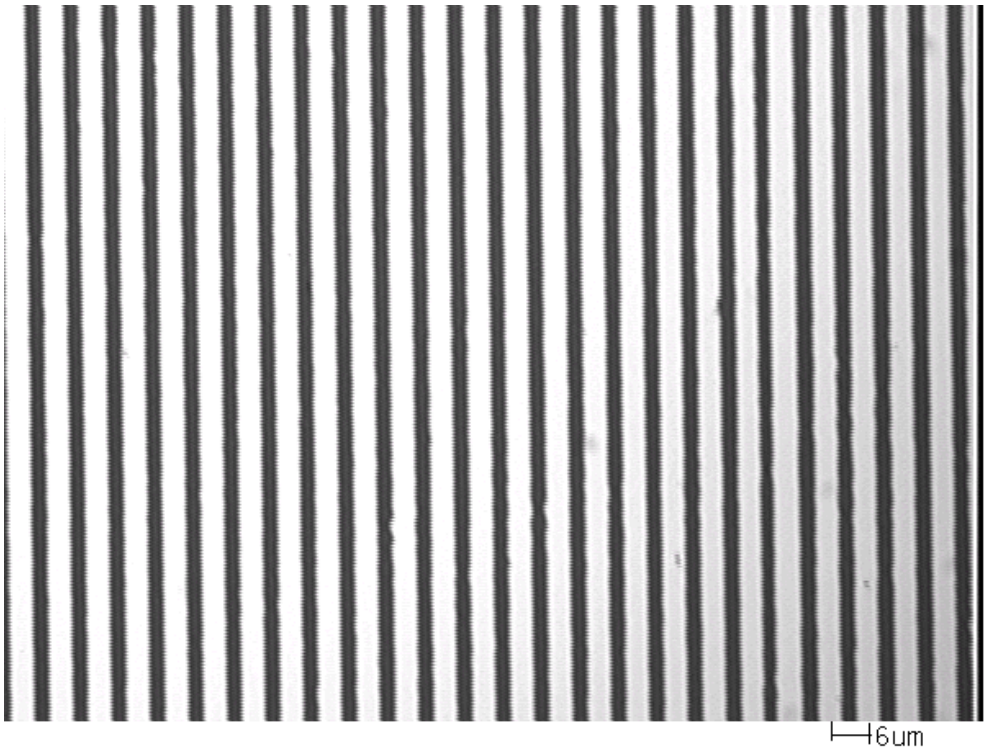

Figure 16 Al IDT fingers.

The patterns in two metal layers of Al and Au can be deposited easily and lift-off successfully by bilayer lift-off process. The real patterns are depicted in figure 17&18.

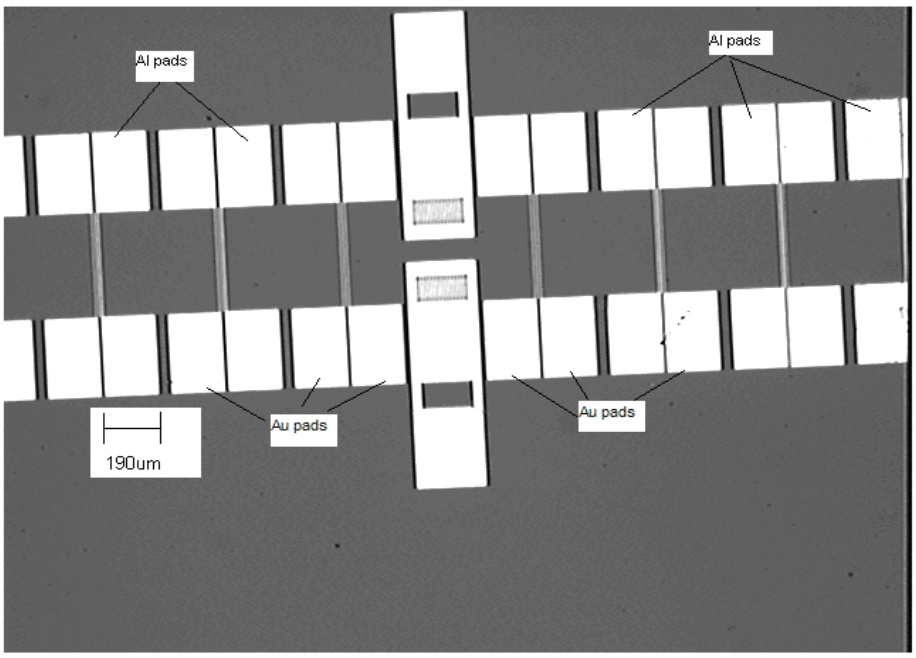

Figure 17 Test IDT and Al & Au pads.

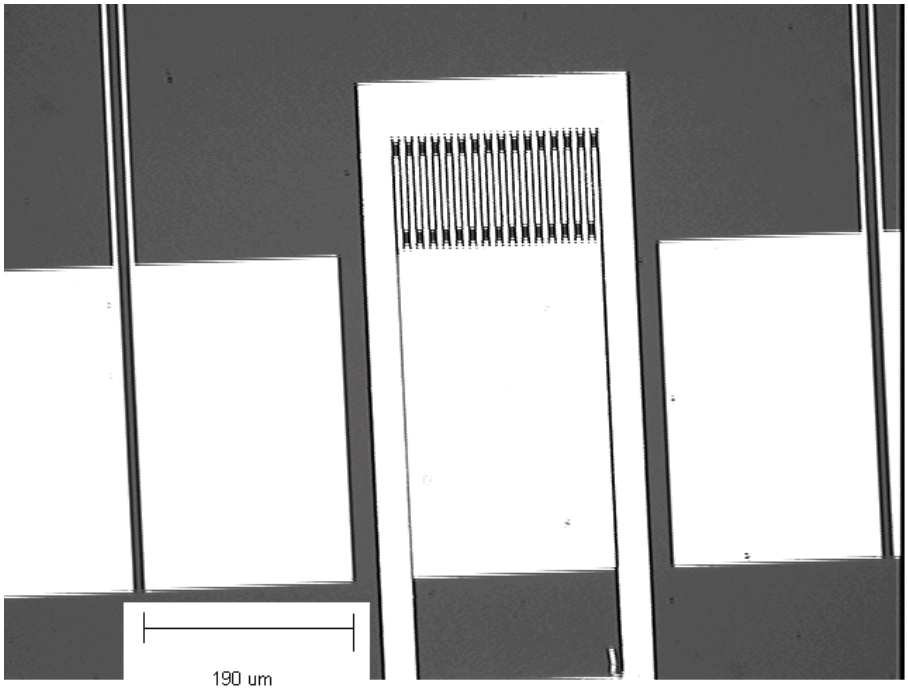

Figure 18 Test IDT and pads.

4.2 Pentacene Shadow Silicon Mask Design and Fabrication

Pentacene shadow mask needs to open some accurate rectangular windows on a silicon wafer. Therefore, the etch through-wafer technique is involved here. Up to now, there are two kinds of method usually used to etch through silicon.

One is dry or plasma enhanced ion etch, accurately called deep reactive ion etch (DRIE), which can form a highly anisotropic etch process, and normally the aspect ratios also can reach 20:1 or more. This method can fabricate almost truly vertical walls [24]. Essentially, the etchant, chemically reactive plasma is generated under low pressure (vacuum), and is used to remove the material exposed to the high energy ion plasma. Accordingly, the etch process is not only a chemical process, but also a physical process. At this point, the etch selectivity and anisotropy etch profile can be controlled. Up to now, there are many successful silicon etch through-wafer experiment being reported. Thus, DRIE is probably a workable technique for opening window on a silicon wafer.

Another method is wet etch or chemical etch. The etchant is heated potassium hydroxide and water (KOH solution). KOH etches silicon anisotropically, and has a unique character. It can give a different etch rate, which depend on the silicon crystal lattice orientation, KOH concentration, and etch temperature. Moreover, the KOH etch facility is easy to prepare. Consequently, for the micro-scale resolution, KOH etch is the ideal choice.

According to the above mentioned KOH etch rate depends on silicon lattice direction, KOH will form a unique 3 dimension profile because silicon is a diamond lattice crystal material. It has the main lattice plane as (100), (110), and (111). In fact, KOH is a fast anisotropic etch model except in the silicon (111) plane. For example, if a

square pattern is on the (100) plane, the final etch profile is a pyramidal shape leaving the (111) plans survived. Moreover, one of the square sides should parallel to the (110) edge in order to get the accurate square size. Otherwise, a circle pattern on the (100) plane only can form a pyramidal shape. This attribute are shown in figure 19. At this point, only rectangular patterns can be exactly transferred to the final etch shape. The pyramidal cross section describes the angle between (111) and (100) plane in figure 20 which is 54.7°.

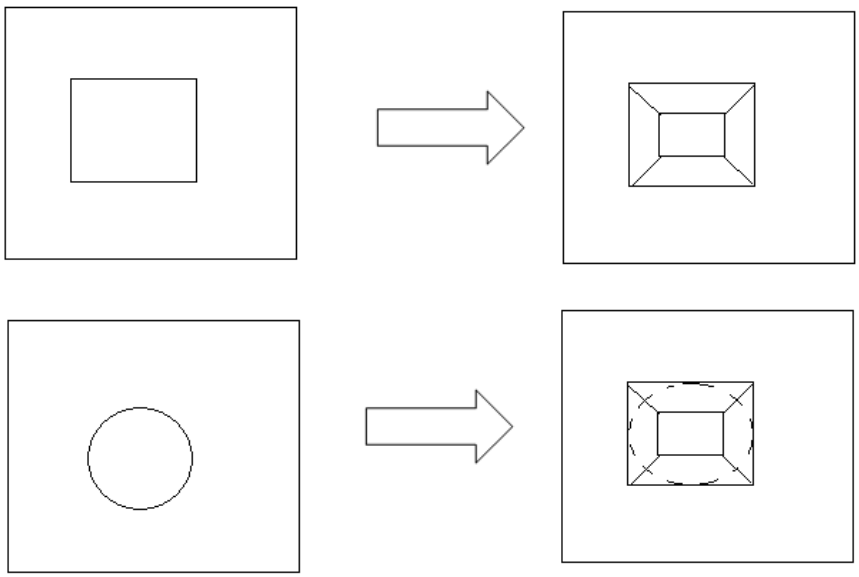

Figure 19 Square and circle patterns in KOH etch process.

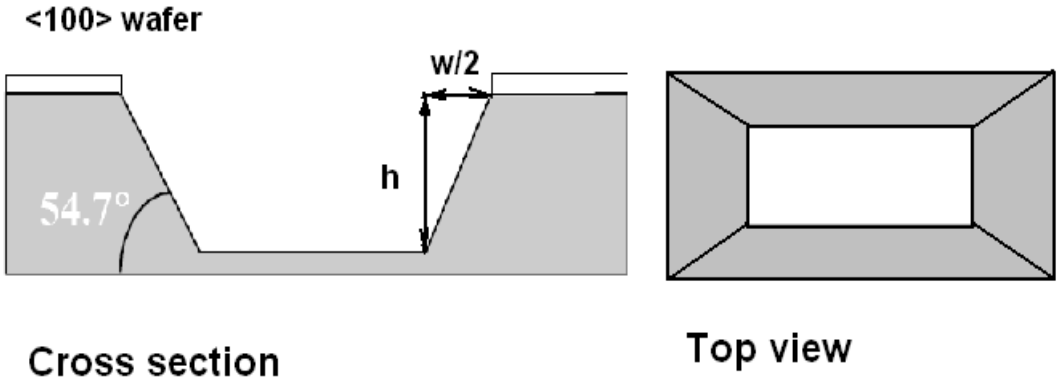

Figure 20 Silicon V-groove character. (after [25] with additions)

According to figure 20, the etch depth h have a relationship with the surface width was

$$\sqrt{2}h = w \quad [26] \tag{4.1}$$

Furthermore, the etched surface quality is affected by the KOH concentration and etching temperature. The following table shows the etch rate and the V groove quality.

Table 2 KOH etch rate in (100) silicon wafer (μm/min) *

Temperature (°C)	20% KOH concentration	30% KOH concentration	40% KOH concentration
20	0.025	0.024	0.02
40	0.188	0.108	0.088
60	0.45	0.41	0.33
80	1.4	1.3	1.1
100	4.1	3.8	3.1
Comment	The etch rate is the fastest under this concentration	The surface is smoother than the lower concentration.	The etch rate is slower than the higher concentration.

- The data in table 2 is from [27].

In order to get a smooth etch surface and fast etch rate, in this project, 30% concentration and 80 °C etch temperature was selected as the optimum etching condition [27].

The shadow mask is good to use double side polished (100) n type 100 mm 300 ±2 um silicon wafer as the mask in order to obtain rectangular etched windows on silicon wafers to match the pentacene channel size, 36μm×6mm [28] [29]. The V groove etching technique was used to fabricate the shadow mask, and 30% KOH etchant was used. The silicon V groove characters are illustrated in figure 19, and etch depth relationship with top surface window size is also described clearly in the above equation (4.1). In order to

finally obtain the pentacene channel size, 36μm×6mm at the bottom of silicon, the windows size, which is on the top of the silicon, should be 463.1μm×6431μm before KOH etch.

However, a protection mask is very important and necessary in transferring patterns to silicon wafer. The mask should have a high selectivity of silicon in 80 °C KOH solution in order to keep the patterns during the long time etching. Furthermore, the mask requires a good adhesion to silicon to avoid etchant penetrating through the edge of the mask to damage the shape or size. Some material was reported as the KOH etching mask, chromium, thermal silicon dioxide, SU8 photoresist, and LPCVD silicon nitride. Except LPCVD, the above etching mask material can be deposited on silicon wafers using available equipment.

First, chromium film was tested as a possible etching mask in KOH process. The etch rate of evaporated chromium in KOH is 4.2 nm/min [30]. The through-wafer etching process takes about 4 hours. Therefore, 1 μm chromium film was deposited on a silicon wafer by thermal evaporator, NRC 3177. Unfortunately, the experimental etch rate of this chromium in KOH was about 7.1 nm/min, and many defect dots appeared after KOH etching test. Increasing the thickness of chromium is not too hard, but the defect dots will expose silicon and etch them out during KOH etching, consequently destroying the desired patterns. At this point, using chromium film is not a good choice.

Second, thermal silicon dioxide is another suggestion in some reports [29]. Thermal silicon dioxide etch rate in KOH is 7.7 nm/min [30]. By calculation, at less 2 μm thickness silicon dioxide films should grow on the silicon wafer to avoid silicon etched during KOH through-wafer etch. Using available equipment, the gas system can only

supply oxygen and nitrogen for thermal growing oxide for safety reason. In this way, thermal silicon dioxide only can be grown using dry way oxidation, but dry thermal growing method can not get over 1 μm thickness silicon dioxide even if growing process keeps working a whole week. For this reason, the possibility of silicon dioxide mask was rejected.

Third, SU8 negative photoresist was also under consideration. Though SU8 photoresist is not affected by KOH etching, it is very sensitive to thermal stress and has a very poor adhesion to any material. Several tests were undertaken to find if SU8 can be the etching mask in KOH. The operation process was as follows.

1. SU8 spin coated on silicon wafer.
2. Wafer left on a horizontal plate for 2 hour to prevent edge-beads.
3. Pre-bake: 65°C on hot plate for 10 minute, afterwards, 95°C on hot plate for 1 hour. Wafer cooled in air.
4. UV exposure for 40 second.
5. Post-baked at 65°C on hot plate for 1 minute, afterwards, 95°C on hot plate for 6 minute, and cooled in air.
6. Developed for 6 minute.
7. Hard-baked foundation is: Baked from 65°C to 250°C at 5°C/min rise rate, and baked for over 40 minute at 250°C on hot plate.
8. Cooled at 5°C/min to 30°C.
9. 30% KOH etched at 80°C for about 4 hour.

After the above process, SU8 was still on the silicon wafer, and the silicon was etched through. Unfortunately, the patterns were not exactly transferred to the silicon because the poor adhesion caused KOH to penetrate the edges and etch silicon out around the windows on SU8. Furthermore, the SU8 film would peel off when it is in the thermal evaporation to deposit pentacene. In summary, SU8 can not keep the patterns during the petacene deposition due to the thermal stress affect. Therefore, SU8 can not be the KOH mask.

The last method, silicon nitride, is reported as a reliable etching mask for KOH process [28]. It is confirmed that nitride can be the suitable hard mask to transfer patterns to silicon during long time KOH etching because of the high etch selectivity (>1,000) [29] compared to silicon. In order to get a high quality silicon nitride layer on silicon, LPCVD silicon nitride is the only one which can exactly transfer patterns to silicon during through-wafer etching. 200 nm LPCVD silicon nitride was grown by Nano Fabrication Center of University of Minnesota on double polished (100) n type and 300 ±2 um silicon wafers. To pattern the silicon nitride, wet etch silicon nitride was used. Many experiments show that photoresist can not be the hard mask for wet silicon nitride etches [29]. They prefer methods using LTO (low temperature oxide) silicon dioxide as the mask to transfer patterns to silicon nitride after standard lithography. After lithography, dry etch or BOE (buffered oxide etch) etch can transfer patterns to silicon dioxide layer, then to silicon nitride. Unfortunately, the LTO silicon dioxide process was not available. Some researchers described that photoresist may probably work as a hard mask when nitride was under wet etch process [31]. By testing several hard bake temperatures, 185 °C was chosen because under this temperature, the patterns edge on

silicon nitride will be very rough. The rough edge is shown in figure 21. After testing hard bake temperatures, photoresist does work as the hard mask in transfer patterns to silicon nitride if the process is properly chose [31]. The important factor is to bake the wafer at 185 °C for over 4.5 hour after standard lithography.

Figure 21 Patterns on silicon nitride with rough edge.

The silicon shadow mask patterns were designed based on Xu's chromium glass lift-off masks and the geometry of an etched silicon V groove. The mask was printed by CAD/Art Services, Inc. at 10,000DPI resolution. Figure 22 is part of the mask. Some alignment markers in the metal layers were designed to match the square windows in the

pentacene silicon shadow mask, which are used to align the silicon shadow mask with the $LiNbO_3$ wafer under Karl Suss, MJB3 aligner.

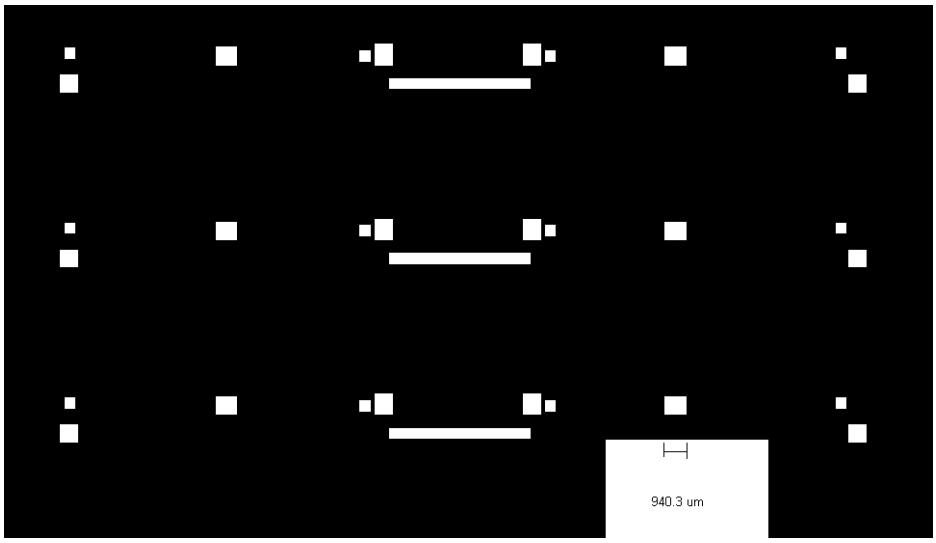

Figure 22 Silicon shadow mask film.

According to the above analysis, the silicon shadow mask fabrication process is described as the following.S1813 double-sided spun at 2500 RPM to obtain 1.5 μm layers on each side. Soft-baked at 90 °C for 25 minute in oven.

1. UV exposure by Karl Suss, MJB3 for 23 second at 13.5 mW/cm^2.
2. Developed in MF 319 for 70 second.
3. Rinsed in DI water.
4. Dried by nitrogen gas.

5. Hard baked at 185 °C in oven for 4.5 hour.
6. Etched in 80% phosphoric acid for 1 hour at 160 °C. The silicon nitride etch rate was 0.2 μm/hour in phosphoric acid [31].
7. DI water cleaned and nitrogen dried.
8. Stripped photoresist by oxygen plasma in System VII, Plasma Therm at 120 W for 30 minutes.
9. Etched in 30% KOH at 80 °C for about 4 hour. Wafer condition was checked frequently.
10. DI water cleaned and nitrogen dried.
11. Removed silicon nitride in phosphoric acid.

Figure 23-27 show the above process.

Figure 23: LPCVD silicon nitride grown both sides.

Figure 24 UV lithography for transferring patterns to silicon nitride.

Figure 25 Phosphoric acid etch for transferring patterns to Si wafer.

Figure 26 KOH etch through process to form shadow mask patterns.

Figure 27 The silicon shadow mask after removing silicon nitride.

After KOH etching, the pentacene channel windows were generated on the silicon wafer. The part of channel is shown in figure 28. By using the silicon shadow mask, the pentacene channel will be formed onto $LiNbO_3$ wafer, which are with IDT and connection pads metal layers to complete the ACT device.

Figure 28 Pentacene channel window on silicon wafer.

4.3 Align Shadow Mask to $LiNbO_3$ Wafer

In order to set the shadow mask on the right position to fix the pentacene channel just between the two parabolic metalized horn beamwidth compressor without any gap, the shadow mask need to be aligned to the already existed devices on $LiNbO_3$ wafer. Thermal evaporator with microscope aligner was not available. Therefore, the shadow mask should be already aligned with $LiNbO_3$ wafer before putting them into thermal evaporator. The aligning work has to use the Karl Suss, MJB3 UV aligner.

However, the operation in Karl Suss UV aligner is to move and rotate a platform which holds the $LiNbO_3$ wafer by its vacuum chuck to the silicon shadow mask that is fixed on the mask holder by vacuum. In order to easily carry the silicon shadow mask and $LiNbO_3$ wafer together, a suitable facility, which can safely hold the two wafers fixed together, was needed. A $LiNbO_3$ wafer holder was necessary to fix the $LiNbO_3$ wafer and shadow mask together. The $LiNbO_3$ wafer holder is shown in figure 29. It consists of three different parts, steel plate, thin steel plate, and silicon chip. All of the parts must have precision flatness to let the wafer holder move freely when it aligns under Karl Suss in separate condition. Mostly, the separate gap in Karl Suss is a few microns between the wafer and the mask. This tolerance can be achieved by precision grinding. Additionally, the thickness of the thin steel part should be less than the $LiNbO_3$ wafer to avoid any gap between the wafer and the mask when they are in contact condition under the mask aligner. After aligning the wafer and mask, the UV aligner makes them contact and use three strong magnets to stick them together to avoid any movement between them. At this time, silicon shadow mask has been put on the exact position against the $LiNbO_3$ substrate.

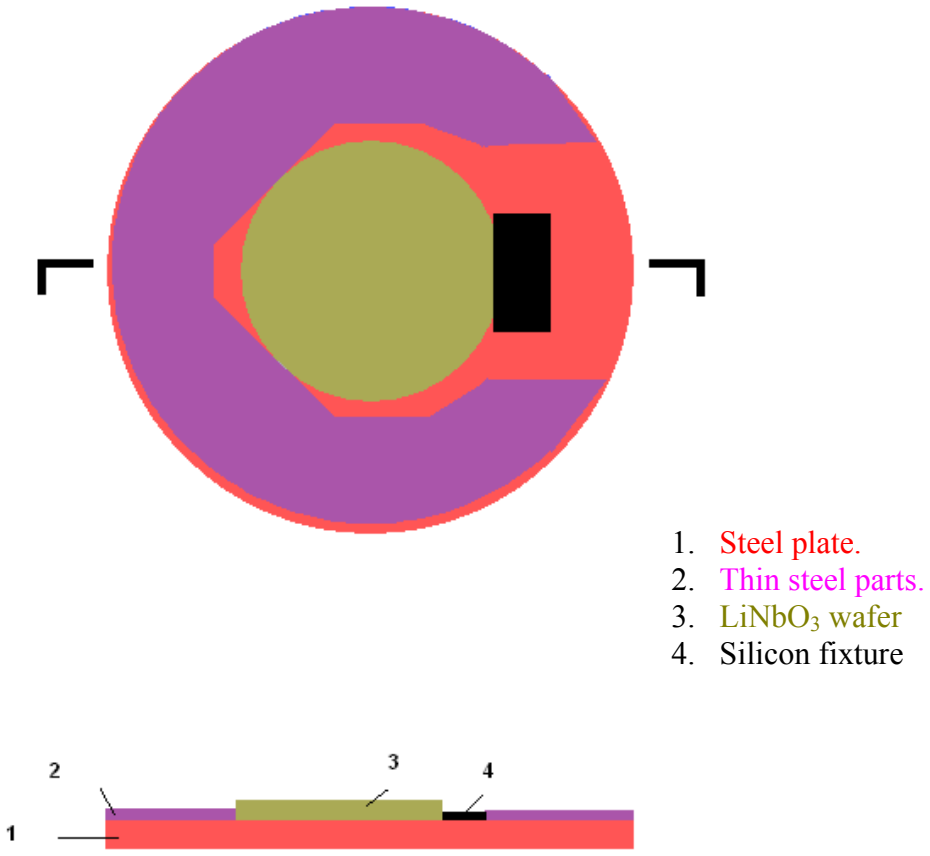

Figure 29 The schematics of wafer holder.

4.4 Pentacene Deposition

Pentacene is a p type organic semiconductor. It can be dissolved in organic solvents. Therefore, the conventional lift-off method does not work on pentacene deposition. Currently, there is no better way to deposit pentacene than thermal evaporation through shadow masks. Some experiments reported that pentacene quality, such as crystallization, which depends on the purity of pentacene source, growing rate, growing vacuum pressure, and growing temperature. Furthermore, the crystallization defines the hole mobility, which is one important semiconductor property. Therefore, the

deposition process is crucial to get a high mobility pentacene thin film. The optimization process was reported as that low deposition rates (about 1 Å/sec), criteria deposition temperature (60 °C), and low deposition vacuum pressure (around 10^{-6} mbar) with prior purification pentacene that can get higher crystallization [32]. The highest mobility reported as 35 cm^2/Vs to 58 cm^2/Vs by grown in 2×10^{-7} mbar and low growing rate with purified pentacene [33]. In addition, pentacene should be stored in dark and nitrogen protection environment since it is sensitive with UV and oxygen [34]. Otherwise, the mobility will be different, usually a smaller value. For example, if the pentacene source (98% Aldrich chemical) was directly deposited under room temperature in 10^{-6} mbar at 10 Å/sec deposition rate, and about 800 nm thickness pentacene, the mobility obtained is only 0.001 cm^2/Vs [35].

In this project, the pentacene layer was deposited by 98% Aldrich using a Denton Vacuum DR-502A thermal evaporator. Since this can only pump to 2.67×10^{-4} mbar, and has no any sensor in the chamber, the deposition process can not allow reading the growing rate. The sample was grown under 15 A current to get about 700 nm thickness pentacene films. Generally, the conventional carrier mobility measurement is Hall Effect, and it has the advantages of easy preparation of measurement samples and equipment. Additionally, if the thickness of pentacene is known, the measurement results are not only the carrier mobility, but also the hole concentration. Unfortunately, the high resistance of the electrodes and pentacene channel difficultly caused in measurement because of continually changing reading. The pentacene mobility can be obtained by field effect transistor mobility [36] and timed resolved microwave conductivity [37] in some researchers' reports.

Finally, the Aldrich pentacene was deposited through the silicon shadow mask onto the $LiNbO_3$ wafer which has metal IDT and electrodes layers already on it. Under microscope, the pentacene channel is exactly between the two aluminum parabolic horns since they have already aligned by Karl Suss, MJB3 UV aligner. Figure 30 clearly illustrates the result, using three images combined because of its long narrow size. Figure 31, shows channel under low magnification.

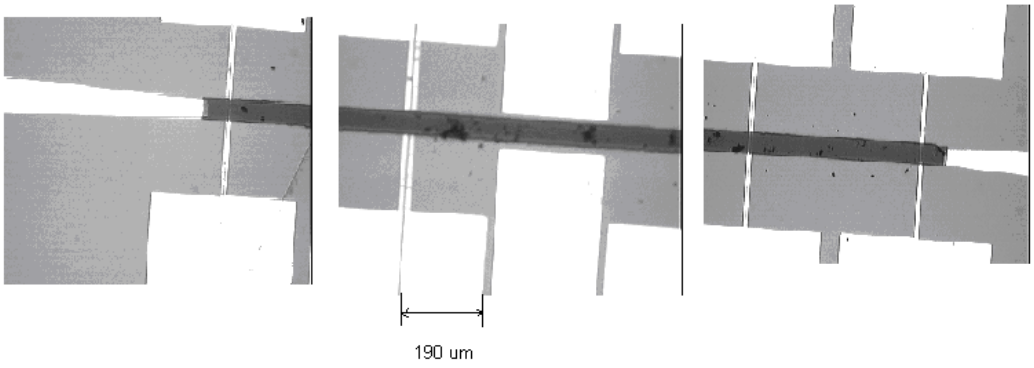

Figure 30 Pentacene channel schematics combined with three images.

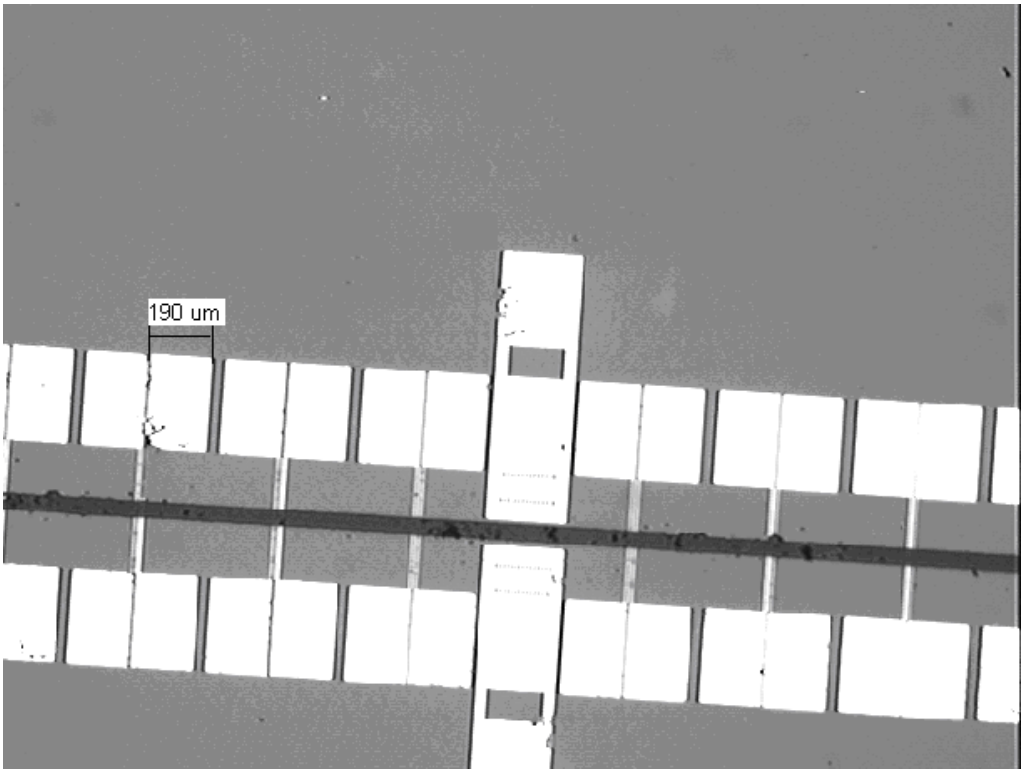

Figure 31 Pentacene channel under low magnification.

4.5 Conclusion

In order to fabricate pentacene acoustic charge transport device on $LiNbO_3$ substrate, several techniques were involved, and some may need to be improved in the future. The important part is IDT lift-off fabrication since there are thirty 3 μm width fingers separated by 3 μm gaps, which need no figure broken and clear figure edges to avoid any connection between them. At this point, undercut structure is necessary to successfully form such high density fingers by bilayer lift-off process. Furthermore, the lift-off resist dissolved rate and thickness defines the size of undercut to form these figures with clear edges. Moreover, the lift-off resist dissolved rate is decided by its soft baking temperature, the substrate material and substrate size. In this project, the soft baking temperature, 150 °C is only for 1 mm thickness and 2 inch diameter $LiNbO_3$

wafer to get the lift-off resist (LOR 3B) dissolved rate at about 50 nm/sec. If the substrate or deposit layer is changed, the soft baking process has to change accordingly to get the right undercut.

The other important part of the pentacene ACT device is the pentacene charge transfer channel. The main fabrication process is KOH etching silicon shadow mask for thermal evaporating pentacene powder source to the $LiNbO_3$ substrate. Furthermore, the channel should exactly connect to the two parabolic horns without any gap. In order to get high pentacene hold mobility, pentacene thermal evaporation parameter may under the following optimized circumstances to get the highest crystallization. It is deposited at the about 1 Å/sec growing rate, 60 °C deposition temperature, and around 10^{-6} mbar vacuum pressure with prior purification pentacene. The highest mobility was described as 35 cm^2/Vs to 58 cm^2/Vs by grown in 2×10^{-7} mbar which is better than this pentacene ACT device supposed, 1 cm^2/Vs.

5 EPITAXIAL GaAs LIFT-OFF BONDING TO $LiNbO_3$

The function of ACT channel which is described in section 2.5 is to transform charge packages defined by input signals and limit them only moving within the channel to avoid leaking electrons. In order to get high frequency SAW device, ACT channels must be made of high mobility materials. Some experiments indicated that GaAs is a suitable material which has a high mobility [38]. Besides using pentacene film as the ACT channel, GaAs is also under consideration.

The epitaxial GaAs has high mobility because epitaxial growing method can get fewer defects crystalline structure. In order to avoid mismatch in the interface between the GaAs film and substrate, the epitaxial GaAs will be grown on a crystalline GaAs substrate instead of the $LiNbO_3$. At this point, the epitaxial film has to be bonded to the substrate after its growing. This used a technique named “epitaxial lift-off”, which is indicated by some successful experiments.

5.1 Epitaxial Lift-off

First of all, an epitaxial GaAs film should grow on a crystal GaAs substrate with a sacrificial etching stop layer which can separate epitaxial film from the substrate. Due to its extremely high etching rate in dilute 10% hidrofloric acid and similar crystalline structure with GaAs, $Al_{0.8}Ga_{0.2}As$ layer is selected to be the etching stop layer between epitaxial film and the substrate [38].

However, the condition of bulk material etching is different with a few micrometer thickness sacrificial film etching, which is between two other materials,

because the etchant can hardly reach the sacrificial material within the very narrow space. The method, which forces the slit open with a weight, is necessary [39].

As reported in [39], apiezon wax of about 200 μm thickness was melted on epitaxial film, and stuck on a metal foil to avoid cracking the film. A weight was hung up the foil to bend the film during the etching process to open the slit to enhance the etching rate. The process is illustrated in figure 32. In addition, the etching rate is influenced by the film size (L) and the weight. The etching rate function is described in [39].

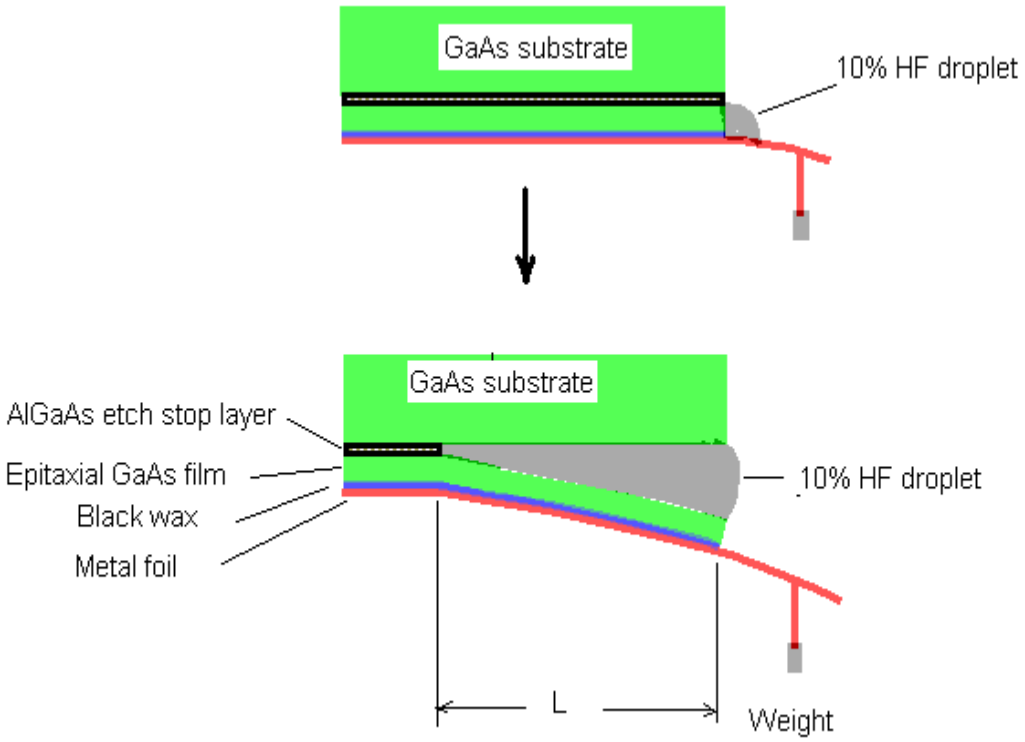

Figure 32 Schematic of epitaxial film lift-off structure.

During the etching process, one droplet of 10% HF should be kept in the slit to continuously etch the sacrificial film, and the action has to seal in a container at 50 °C temperature. Next, the epitaxial GaAs film is moved to bond to $LiNbO_3$ substrate.

5.2 Cleaning Bonding Surface

The bonding forces which can put the GaAs epitaxial film to the $LiNbO_3$ include van der Waals forces, capillary forces, electronstatic forces, and chemical bonds between the particles and surface [40]. In order to get a tight bond, the bonding surfaces must be treated to remove free particulate, organic, and metallic contamination. Generally, the cleanliness of the bonding surfaces will not only affect the structure, but also affect the electrical properties of the bonding interfaces. Furthermore, the bonding surfaces should be treated to be hydrophilic surface property to strengthen the bonding forces [40]. The following cleaning and etching process was used to remove the contaminant and flat the surfaces.

Firstly, the process to clean GaAs film used NH_4OH: H_2O_2: H_2O (1:4:20) for 10 minute to remove particles, organics and metallic contaminates, then H_2O: H_2O_2: HCl (5:1:1) for 10 minute to remove ions and oxidations, H_2SO_4: H_2O_2 (1: 1) to make hydrophilic surface, as the following DI water and nitrogen dry to accomplish the cleaning process [40].

Finally, the standard process to clean $LiNbO_3$ wafer used acetone, methanol, DI water, and nitrogen dry.

During all the above cleaning treatment, the bonding interfaces were not touched to avoid contaminating, because any careless touch may cause the bonding failure.

5.3 Bonding the GaAs Epitaxial Film to $LiNbO_3$ Substrate

The main bonding force is van der Waals force and hydrogen bridge forces. Using vacuum pen, the film was placed on the substrate with black wax covered on the film to avoid any touch on the bonding surfaces. Additionally, the bonding surfaces must be wet to make a hydrogen bridge force. After the above operation, the stacked sample was softly pressed to squeeze out air between the interfaces, and was put then into a vacuum bag to get a continuously uniform pressure to bond them together by van der Waals force. The flat epitaxial film can be bent to keep a very tiny distance to the polished substrate under the uniform pressure, and form van der Waals bonding. In order to release the H_2O between the interfaces, heating the vacuum bag in 100 °C for 2 hour evaporated water out. No more high temperature can strengthen the bonding force because of the thermal expansion mismatch [41]. After slowly cooling the sample in oven, the black wax was removed by TCE, and epitaxial GaAs was bonded to $LiNbO_3$ wafer.

5.4 GaAs / $LiNbO_3$ Wafer Bonding and Aluminum Film/ $LiNbO_3$ Bonding Test

In this project, before bonding GaAs film to $LiNbO_3$ wafer, two kinds of bonding tests were done in Mricoelectronics Research Center (MRC) of Iowa State University (ISU).

In order to test the cleaning process, 5mm square GaAs 400 μm thickness wafer chip and 1 inch square $LiNbO_3$ 3 mm thickness wafer were selected to bond together. The cleaning process was explained at detail in 5.2 section. After putting them together in a wet environment, a 30.79 g weight was put on the sample to make a pressure. Afterward, an annealing operation was taken at 90 °C in an oven for 12 hour. Finally, though this operation gets a very strong bonding, only a small area of the sample is under the bonding

by watching the color changed on $LiNbO_3$ wafer. This unbonded area is caused by two wafers interface not close enough for van der Waals bonding. At this point, an epitaxial film will be easily bent to the substrate to form van der Waals forces. Furthermore, the above cleaning process was to be a possible method for GaAs and $LiNbO_3$. The wafer bonding test result shows in figure 33.

Figure 33 GaAs and $LiNbO_3$ wafers bonding result.

The film bonding test process used 1 μm thickness Al thermal evaporation film with photoresist as the sacrificial layer on a microslide to stack on a 1 inch square $LiNbO_3$ wafer. A 3 μm thick apiezone wax was covered on Al film to hold it when transferring it to the substrate. The film lift-off process was as follows.

1. 3g apiezon wax was dissolved in 10 ml TCE (Trichloroethyene) at room temperature for 1 hour.
2. 0.6 ml wax solution dropped on Al film surface by glass syringe.

3. Sample placed in hood to completely release TCE on a horizontal plate to get 3 μm thick apiezone wax layer.
4. Al film lift off in acetone for a few minute.
5. Vacuum pen used to hold the Al film onto a $LiNbO_3$ wafer and into a vacuum bag.
6. Vacuum bag was heated to 100 °C in oven for 2 hour, and then cool down.

The bonding test result shows that film bonding can get much stronger bonding than wafer bonding because of the attached and flexible property of film.

5.5 Conclusion

According to the above testing result, the solution of NH_4OH, HCl, and H_2SO_4 probably can remove the metallic, oxidative, and ionic particles and get hydrophilic surfaces. These treatments are necessary for van der Vaals bonding surfaces. The further testament of Al (film)/ $LiNbO_3$ (wafer) bonding process is the simulation of epitaxial GaAs (film)/ $LiNbO_3$ (wafer) bonding approach.

The next step of future work will be to grow an epitaxial GaAs thin film for bonding as a charge transport channel onto $LiNbO_3$.

6 CONCLUSION AND FUTURE WORK

6.1 Conclusion

Pentacene acoustic charge transport (ACT) device was fabricated by bilayer lift-off and silicon shadow mask. Unlike standard lift-off and chlorobenzene lift-off, the bilayer lift-off technique can make a reliable lift-off process because of its controlled undercut structure. Especially in high density patterns intergrades transducer (IDT), if there is no undercut, the fingers in IDT probably can not be formed. The thickness of the lift-off resist, and its baking temperature are the main factors that can affect the undercut structure. Therefore, careful selection of the lift-off resist is necessary. Besides bilayer lift-off technique, silicon KOH etch through-wafer technique was also involved in pentacene ACT fabrication to make silicon shadow mask for pentacene charge transfer channel by thermal evaporation. Among the many methods in KOH process, hard baked positive photoresist and LPCVD silicon nitride were chosen to be the pattern transfer mask. Finally, the pentacene ACT was accomplished at 3 μm resolution.

GaAs epitaxial film bonding charge transducer is another suggestion to make high frequency ACT. Due to high carrier mobility in an epitaxial GaAs film, epitaxial lift-off technique is proposed to bond a GaAs channel on piezoelectric substrate, $LiNbO_3$. In epitaxial lift-off process, the method for cleaning bonding surface and film moving and bonding has been successfully tested. This project needs further works to be accomplished.

6.2 Future Work

In order to get high carrier mobility in pentacene charge transfer channel, pentacene must be grown under the optimization process, which was reported in [32]. The thermal evaporator will deposition condition such as low deposition rates (about 1 Å/sec), optimal deposition temperature (60 °C), and low deposition vacuum pressure (around 10^{-6} mbar) with prior purification pentacene. Besides the promotion of thermal evaporator, the mobility measurement and petacene ACT device measurement are also to be taken in the future.

GaAs epitaxial film ACT not only needs to find a way bond to the $LiNbO_3$ substrate, but also should be patterned and fixed on the particular position between the IDTs on the substrate. Additionally, the mobility measurement of epitaxial GaAs should be taken under consideration.

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