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# Programmable CMOS Analog-to-Digital Converter Design and Testability

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# PROGRAMMABLE CMOS ANALOG-TO-DIGITAL CONVERTER DESIGN AND TESTABILITY

A Dissertation

Submitted to the Graduate Faculty of the
Louisiana State University and
Agricultural and Mechanical College
in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

in

The Division of Electrical and Computer Engineering

by
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December 2012

To my parents Soundararajan and Saraswathi Soundararajan,

To my wife ShreeRevathy Rajendran,

To my daughter Vibha Rajiv,

and

To my sister Lakshmi Priya and family,

Without their patience, love, values and understanding support,

the completion of this dissertation would not have been possible.

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# ABSTRACT

In this work, a programmable second order oversampling CMOS delta-sigma analog-to-digital converter (ADC) design in 0.5µm n-well CMOS processes is presented for integration in sensor nodes for wireless sensor networks. The digital cascaded integrator comb (CIC) decimation filter is designed to operate at three different oversampling ratios of 16, 32 and 64 to give three different resolutions of 9, 12 and 14 bits, respectively which impact the power consumption of the sensor nodes. Since the major part of power consumed in the CIC decimator is by the integrators, an alternate design is introduced by inserting coder circuits and reusing the same integrators for different resolutions and oversampling ratios to reduce power consumption. The measured peak signal-to-noise ratio (SNR) for the designed second order delta-sigma modulator is 75.6dB at an oversampling ratio of 64, 62.3dB at an oversampling ratio of 32 and 45.3dB at an oversampling ratio of 16.

The implementation of a built-in current sensor (BICS) which takes into account the increased background current of defect-free circuits and the effects of process variation on $\Delta I_{DDQ}$ testing of CMOS data converters is also presented. The BICS uses frequency as the output for fault detection in CUT. A fault is detected when the output frequency deviates more than ±10% from the reference frequency. The output frequencies of the BICS for various model parameters are simulated to check for the effect of process variation on the frequency deviation.

A design for on-chip testability of CMOS ADC by linear ramp histogram technique using synchronous counter as register in code detection unit (CDU) is also presented. A brief overview of the histogram technique, the formulae used to calculate the ADC parameters, the design

implemented in 0.5µm n-well CMOS process, the results and effectiveness of the design are described. Registers in this design are replaced by 6T-SRAM cells and a hardware optimized on-chip testability of CMOS ADC by linear ramp histogram technique using 6T-SRAM as register in CDU is presented. The on-chip linear ramp histogram technique can be seamlessly combined with $\Delta I_{DDQ}$ technique for improved testability, increased fault coverage and reliable operation.

# CHAPTER 1

# INTRODUCTION

The integration of digital, analog and mixed-signal circuits in a System-on-Chip (SOC) has been growing steadily in recent years and has paved the way for more compact and efficient implementations of circuits and systems [1]. The main advantage in having digital, analog and mixed-signal circuits on the same chip are the reduction in size of the circuit, increase in speed of operation, reduction in power dissipation, increase in design flexibility and increased reliability. The increase in circuit complexity is posing a major challenge in design and testing of mixed-signal SOC integrated circuits [2]. Mixed-signal circuits in SOC usually include data converters (analog-to-digital and digital-to-analog) as important interface components along with digital signal processing (DSP) or digital circuits, and they form an integral part of most applications in the communication, consumer, automotive, computers, biomedical, military and space electronics. These digital circuits use digital technologies that offer fast transistor biased at low voltages and therefore the data converter design becomes the most challenging interface circuit. Hence it is desired to use data converter architecture which trade accuracy for speed or vice versa as per the application it is designed for.

Due to availability of dedicated digital signal processing technique [3, 4], faster analog design needing less complex and lower performance circuits to attain a given conversion accuracy are used in data converter implementation. Delta-Sigma ($\Delta\Sigma$) analog-to-digital converter is a low-cost, low-bandwidth, low-power, high resolution ADC and has varied applications in data acquisition, communications, signal processing, instrumentation and wireless

sensor networks. Integrating an analog delta-sigma (ΔΣ) modulator with a digital decimator forms a delta-sigma ADC. The digital signal processing in the delta-sigma ADC is done at the decimator stage, which is a cascaded integrator comb (CIC) decimation filter. This CIC decimation filter also performs down sampling of high frequency, low-resolution digital output from the oversampling delta-sigma modulator to lower Nyquist frequency, high-resolution digital output [4]. Hence the decimation stage is responsible for achieving higher resolution and able to program the decimator, offers further advantage of operating the ADC at different input channel bandwidth and with different oversampling ratios [5]. This is of significant advantage as decimation stage requires large silicon area and incurs higher dissipation as it contains fast switching circuits.

Also in a mixed-signal SOC due to the increasing level of integration and complexity, the test cost and the need for faster and complex test equipment has increased. Among the test cost, mixed-signal test cost for data converters is becoming one of the most important factors in SOC [6]. Hence the necessity to develop new and efficient low-cost test techniques and methodologies with significant capabilities has increased. Automated Test Equipment (ATE) is currently being used to solve the problem of testing ADC and DAC for device characterization and parameter test [6, 7]. But high resolution mixed-signal ATE's are expensive and increases the test cost and time for data converter testing drastically. Therefore, built-in-self-test (BIST) can be used as an effective test technique to prevent the dependence on mixed-signal testers, wherein the stimulus generation and measurements are done on-chip. The BIST techniques for data converters have been the focus of many research activities recently [8-12].

Testing of data converters can be divided into functionality based testing and fault detection based testing. Many functionality based testing have been proposed for data converters over the years. But since they are specification oriented and does not cover physical defects, fault based testing has been introduced. In the fault based testing, quiescent current ($I_{DDQ}$) testing has been very efficient in testing for physical defects such as gate oxide shorts, floating-gates and bridging faults in mixed signal circuits and data converters. $I_{DDQ}$ testing is a defect based test that measures device supply current under steady state condition. Recently built-in current sensors (BICS) for $I_{DDQ}$ testing of CMOS sigma-delta (or delta-sigma) analog-to-digital converters and charge scaling digital-to-analog converters have been designed and implemented [13-16]. Based on this method we have developed a BICS for $\Delta I_{DDQ}$ testing of CMOS data converters that takes into account the effect of process variation and increasing background current. In this work, we have considered physical defects such as device shorts and open faults introduced in the circuit under test (CUT) and tested.

To improve the efficiency of the quiescent current ($I_{DDQ}$) testing, functional test methods for data converters like histogram technique [17] can be used along. In functional testing, the performance metrics for data converters used are the offset error, gain error, nonlinearity error, signal-to-noise error and effective number of bits.

In this work, we have presented design of a programmable second order oversampling delta-sigma analog-to-digital converter comprising a second order oversampling delta-sigma modulator and a programmable cascaded integrator comb decimation filter. We have also presented the $\Delta I_{DDQ}$ testing of CMOS data converter considering process variation effects.

Functional testing of data converters using on-chip linear ramp histogram technique to calculate the static parameters has been designed and presented. Further area optimization of the on-chip linear ramp histogram technique has been researched and presented using 6T-SRAM cells. The proposed histogram technique can be seamlessly combined with the quiescent current testing to improve the fault coverage achieved.

## 1.1 Motivation for Programmable Second Order Oversampling CMOS Delta-Sigma ADC

The programmable second order oversampling analog-to-digital converter (ADC) designed by combining a second order oversampling delta-sigma modulator and a programmable cascaded integrator comb decimation filter can be programmed to generate different resolution depending on the oversampling ratio. The output resolution of the ADC depends directly on the oversampling ratio and the order of the modulator and the decimation filter. In the decimation filter, the output resolution can be increased by increasing the oversampling ratio which results in large silicon area and higher power dissipation. Hence we have focused on designing a programmable second order oversampling delta-sigma ADC to generate different resolutions for different oversampling ratio by reusing the design. In the design, we have focused on achieving an area efficient second order oversampling delta-sigma ADC by integrating a second order delta-sigma modulator with the programmable CIC decimation filter. The design can be programmed to operate at three different oversampling ratios of 64, 32 and 16 to generate a 14-bit, 12-bit and 9-bit output, respectively. The integrator stages in the decimator have been reused for different oversampling ratio, by enabling programmability of the decimator. The design also

includes an internal clock divider capable of producing three different clock signals for three different oversampling ratios for achieving three different resolutions.

## 1.2 Motivation for $\Delta I_{DDQ}$ Testing of CMOS Data Converter Considering Process Variation Effects

During the fabrication of designed integrated circuits using photolithographic process, imperfection and blemishes occur leading to either catastrophic failure in the operation or any individual IC or minor variation in the performance from one IC to other [2]. In sub-micron/deep submicron CMOS processes fabrication, the gap between the defective and defect-free quiescent current is narrowing due to increasing background current [2] and process variations pose very severe threat. Process variation affects the threshold voltage of the circuit and thus the effective leakage current in the circuit. Also, process variation changes MOS model parameters and have detrimental effects specifically in the reliability and performance of mixed-signal and analog integrated circuits. Hence, designing BICS for sub-micron CMOS process considering process variation effects is becoming difficult. Many new techniques have been proposed and presented in literature by many researchers to minimize these effects in $I_{DDQ}$ testing. As discussed earlier in this chapter, built-in current sensors (BICS) for $I_{DDQ}$ testing of CMOS delta-sigma (or sigma-delta) analog-to-digital converters and charge scaling digital-to-analog converters have been designed and implemented [13-16] earlier in our research group. Based on this method we have developed an attractive BICS for $\Delta I_{DDQ}$ testing of CMOS data converters that takes into account the effect of process variation and increasing background current. In this method, the differential measurement successfully suppresses the impact of background current and process variation.

## 1.3 Motivation for On-Chip Functional Testability of CMOS ADC using Linear Ramp Histogram Technique

In functional testing of data converters, the linear ramp histogram technique is the most prominent and one among the most classical approaches to test ADC. In the linear ramp histogram technique, a linear ramp waveform is applied at the ADC input and the number of time each code appears is recorded. These recorded samples can be then used along with the theoretical samples in a linear computation to derive ADC static parameters line offset, gain, differential and integral non-linearity [17]. Mostly histogram technique has been used for external testing of ADC using FPGA or off-shelf components or test boards. This is due to the reason that on-chip implementation of histogram technique requires large area to accommodate the additional circuitry. But to achieve a faster test time and reduce the dependency on complex test equipment, the feasibility of on-chip implementation of linear ramp histogram technique by optimizing the hardware resources has been the focus of this research.

In this design, we have used the linear ramp as the input signal to the ADC and is generated on chip using a linear ramp generator. The linear histogram technique allows the reduction of the required memory for the storage of the ideal histogram rather than the sinusoidal one and due to the uniform distribution of the histogram, simple linear computation can be used to derive the ADC parameters. In histogram based BIST, to collect the HPC for an n-bit ADC, we require access to $2^n$ on-chip memory. In this work, we have designed the on-chip memory or register by using synchronous counter and then optimized the complete design by using 6T-SRAM cell as register. The design also includes an in-built linear ramp generator to generate the input signal needed for the functional testing and hence can be seamlessly integrated with other

functionality based testing and/or fault detection based testing to improve testability coverage and detection.

## 1.4 Goals

To summarize, the goal of this research are as follows:

- Designed and fabricated a programmable second order oversampling delta-sigma ADC using a second order oversampling delta-sigma modulator and a programmable third order cascaded integrator comb (CIC) decimation filter.
- Designed and implemented a quiescent ($\Delta I_{DDQ}$) current testing technique for CMOS data converters considering process variation effects.
- Designed and implemented an on-chip functional testability of CMOS delta-sigma analog-to-digital converters using linear ramp histogram method.
- Optimize the on-chip functional testability of CMOS delta-sigma analog-to-digital converters using linear ramp histogram method by using 6T-SRAM cells for registers in place of the synchronous counters to calculate the parameters of ADC on-chip.

## 1.5 Chapter Organization

In the following chapters, design and operation of a programmable analog-to-digital converter, quiescent ($\Delta I_{DDQ}$) current testing and on-chip linear-ramp histogram testing have been described.

In **Chapter 1**, motivation and goals for the research are presented.

In **Chapter 2,** the overview and the literature review of the analog-to-digital converter have been discussed in detail. The classifications of the ADC and its performance metrics have also been presented.

In **Chapter 3,** design and implementation of a programmable second order oversampling delta-sigma analog-to-digital converter is described. In this design, a second order oversampling delta-sigma modulator and a third order cascaded integrator comb (sinc) decimation filter have been implemented. The delta-sigma modulator was fabricated in 0.5µm n-well CMOS processes and its complete performance metrics have been presented.

In **Chapter 4,** the concept of $I_{DDQ}$ testing, design and implementation of the built-in current sensor are presented. The effects of process variation on the quiescent current testing in data converters have also been focused in this chapter.

In **Chapter 5,** the design and implementation of on-chip testability of CMOS analog-to-digital converters using linear ramp histogram technique is described. In this design, the register to store the recorded samples is designed using an 8-bit synchronous counter and read/write enable circuit. The 8-bit synchronous counter is designed using JK flip-flop and AND gates and consist of eight JK flip-flops and six 2-input AND gates. The design also consist of a built in linear ramp generator. The block diagram and layout of the fabricated design and its components are explained in detail.

In **Chapter 6,** the design and implementation of on-chip testability of CMOS ADC using linear ramp histogram technique with hardware area optimization is presented. The register to store the recorded samples are designed by using 6-T SRAM cells instead of synchronous

counter. This design is area optimized and has been implemented successfully to functionally test a 7-bit ADC. The block diagram and layout of the design and its components are explained in details in this chapter.

## 1.6 References


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# CHAPTER 2

# OVERVIEW AND LITERATURE REVIEW

Analog-to Digital Converters (ADC) are the link between analog world of sensors and transducers and the digital world of signal processing and data handling in mixed-signal System-On-Chip (SOC). Most of the modern communication systems (like wireless sensor network) utilize digital signal processing (DSP) to resolve the transmitted information. Therefore, between the sensed analog signal and the DSP system, an analog-to-digital (A/D) interface is necessary. This analog-to-digital interface achieves the digitization of the sensed signal to a sampling rate requirement of the DSP system. As discussed in the earlier chapter, the trend of increasing integration level has forced the A/D interface to reside on the same silicon with large DSP or digital circuits. These digital circuits use digital technology that offers fast transistor biased at low voltages; therefore the ADC becomes the most challenging interface block. The tendency is therefore to use ADC architecture which trade accuracy for speed or vice versa as per the application. Now let us look at the ADC fundamentals, classification of ADC and ADC performance metrics in detail.

## 2.1 ADC Fundamentals

The analog-to-digital (A/D) conversion is a process in which the analog input signal is converted to create digital words from the set of reference voltages. Here, the complete analog input signal is divided into $2^N$ levels, where N is the resolution or number of output bits of ADC and each level is represented by a unique digital word. The input analog voltage is thus

represented as a digital word of resolution N corresponding to the level in which the input analog voltage falls [1]. The block diagram of an ADC is as shown in Figure 2.1.

In the block diagram of an ADC, a pre-filter or anti-aliasing filter is used to remove the high frequency components in the incoming analog signal to avoid the aliasing of higher frequency signals back into the baseband of the ADC. The sample/hold circuit follows the antialiasing filter, which samples the analog input voltage at regular sampling interval and holds it for converting to an equivalent output digital code. This conversion is accomplished with the help of the quantizer, which maps the output analog voltage of the sample/hold circuit to the corresponding digital word. The encoder then encodes the digital word into an N-bit binary digital output. Hence, within the conversion time, an analog input signal is converted to an equivalent digital output code [1].

## 2.2 Classification of ADC

Based on the architecture used for the implementation of A/D converters, there are four main different types namely flash A/D converters, pipeline A/D converters, successive approximation A/D converters and delta-sigma (ΔΣ) A/D converters [2, 3]. The comparative graph with respect to resolution and bandwidth of four architectures discussed above are as shown in Figure 2.2. ΔΣ ADC has the capability of trading off speed for resolution and at the same time is quite insensitive to component mismatches. As shown in the graph, delta-sigma A/D converters have the highest resolution in amplitude and lowest resolution in time (bandwidth). Hence these A/D converters are used for low frequency applications. Also, data converters have been classified into two categories based on the sampling frequency.

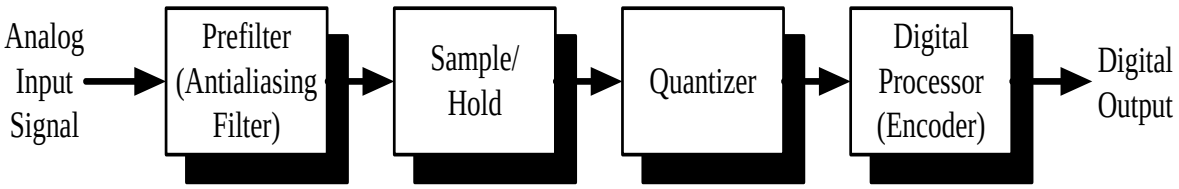


Figure 2.1. Block Diagram of an ADC [1].

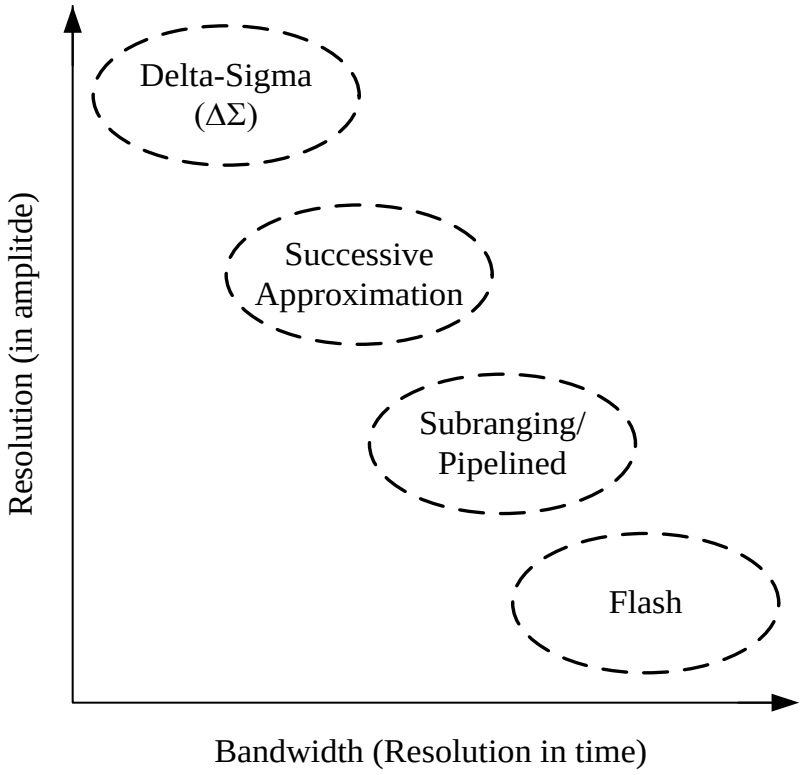


Figure 2.2. ADC technologies comparative graph, with respect to resolution and bandwidth.

### 2.2.1 Nyquist-Rate Converters

In Nyquist-rate ADCs, the analog input signal is sampled at the Nyquist frequency ($f_n$) such that $f_s = f_n = 2 \times B$, where $f_s$ is the sampling frequency and B is the bandwidth of the input signal. These converters derives its name from the sampling theorem known as Nyquist theorem, which states that $f_s$ should be at least twice larger than the highest frequency component present in the analog input signal to avoid aliasing and for successful reproduction of the signal after filtering [1, 2, 3]. Each analog input sample is processed separately and doesn't depend on the earlier analog input sample, thus the converter has no memory. In the Nyquist-rate converters, the linearity and accuracy is determined by matching the accuracy of the analog components used in building the converter. The Signal-to-Noise Ratio (SNR) of a Nyquist-rate converter is given by Eq. (2.1), where N is the resolution of the converter [1].

$$\mathrm{SNR} = 6.02N + 1.76\,\mathrm{dB} \tag{2.1}$$

### 2.2.2 Oversampled Converters

In oversampling ADCs, the analog input signal is sampled at a sampling rate ($f_s$) much higher than the Nyquist frequency ($f_n$).The input signal is sampled at an oversampling frequency $f_s = K \times f_n$ where K is the oversampling ratio and is given by Eq. (2.2) [1].

$$K = (f_s/2B) \tag{2.2}$$

In these converters output is generated by utilizing the current analog input with all preceding analog input values and thus the converter has memory element in its architecture. Thus, one-to-one relation between the input and output samples are destroyed in oversampling converters. Oversampling converters typically employ switched-capacitor circuits and hence the

need for sample and hold circuits are removed. Delta-Sigma (ΔΣ) ADC is classified under the oversampling converters.

## 2.3 ADC Performance Metrics

The commonly used terms to measure the performance of a data converter in particular an ADC have been presented here. An ideal 3-bit ADC is considered for explaining the ADC's performance metrics [1, 2, 3]. The transfer curve of the ideal 3-bit ADC is as shown in Figure 2.3. The analog input in the ADC can have an infinite number of values between $V_{ref-}$ and $V_{ref+,}$ while the digital output code can be one from the finite set of codes dependent on the converter's output word length (resolution). Hence, as discussed earlier, the ADC approximates each input level with one of the digital output codes.

### 2.3.1 Static Characteristics of ADC

The performance metrics that define the static characteristics of the ADC are differential nonlinearity (DNL), integral nonlinearity (INL), offset error, gain error and monotonicity.

**Differential nonlinearity (DNL)** is the measure of the separation between two consecutive code transition points on the input axis from the ideal value of 1 LSB.

**Integral nonlinearity (INL)** is the maximum deviation between the actual finite resolution characteristic and the ideal finite resolution characteristic measured in percent or LSBs. It is the cumulative effect at any given input of all the DNL values and can be calculated by numerically integrating the DNL value for each code.

**Offset error or Offset** is the analog value of the digital output word for the input signal which should have ideally produced a zero output. It is the horizontal difference between the

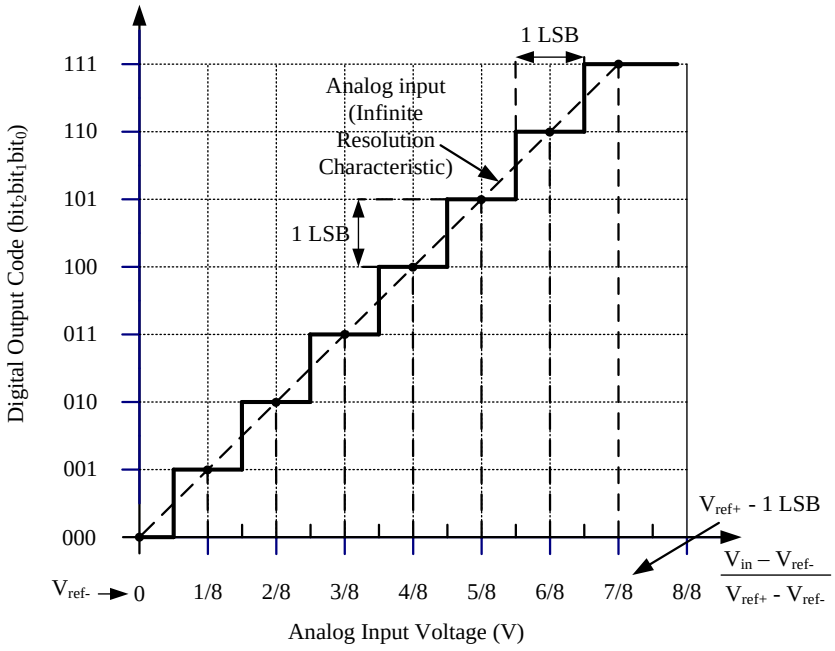


Figure 2.3. Ideal input-output transfer curve of a 3-bit ADC.

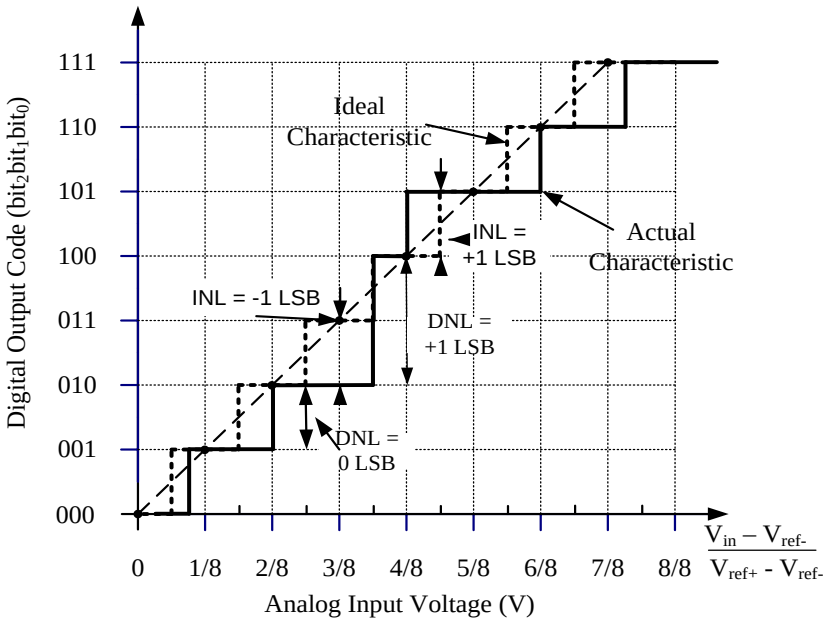


Figure 2.4. DNL and INL illustration for a 3-bit ADC.

actual finite resolution and the ideal finite resolution characteristic. Figure 2.5 illustrates the example of offset error for a 3-bit ADC.

**Gain Error or Gain** is the difference between the actual characteristic, and the ideal characteristic (infinite resolution characteristic) when the offset error and other nonlinearity has been reduced to zero. This can also be thought as a change in the slope of the infinite resolution line from ideal 1. Gain error can be measured as the horizontal difference between the actual and ideal infinite resolution characteristic at highest digital code as illustrated in Figure 2.6.

**Monotonicity**: In a monotonic converter, the output always increases as the input increases. Hence nonmonotonicity occurs when a vertical jump in the output is negative and can be detected by DNL. When the vertical jump is 2 LSBs or greater, missing output code occurs and when the vertical jump is less than 0 LSBs, nonmonotonicity occurs as in Figure 2.7.

### 2.3.2 Dynamic Characteristics of ADC

**Dynamic Range (DR)** is defined as the range of the amplitudes the ADC can effectively resolve. When the signal is too large it overloads and when it is too small it gets lost in the quantization noise.

**Signal-to-Noise Ratio (SNR)** is defined as the ratio of the signal power to total noise power at the ADC output. The sampling frequency is twice the signal bandwidth in a Nyquist converter and the SNR [1] is given by Eq. (2.3),

$$\mathrm{SNR} = 6.02\mathrm{N} + 1.76\,\mathrm{dB} \tag{2.3}$$

**Signal-to-Noise Distortion Ratio (SNDR)** is defined as the ratio of the signal power to the total noise and the harmonic power at the output.

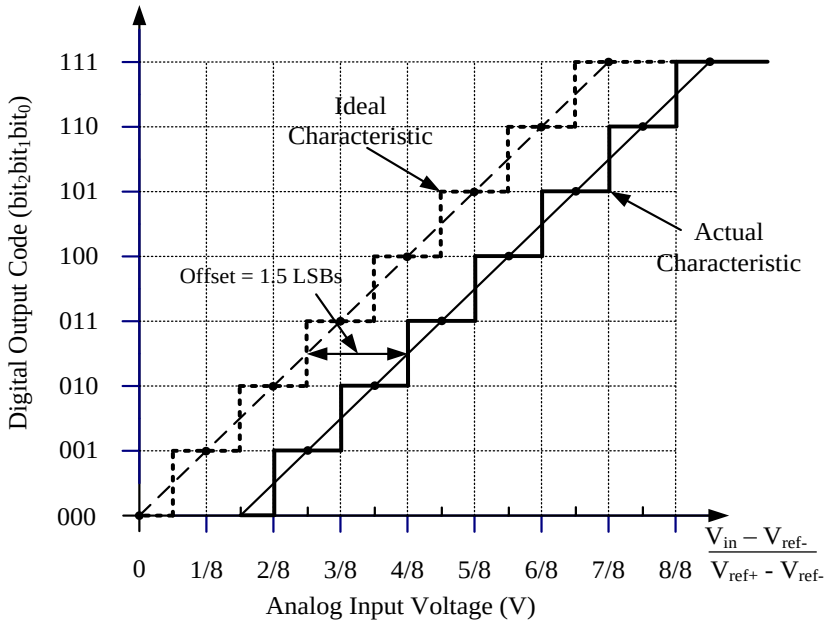


Figure 2.5. Offset Error illustration for a 3-bit ADC.

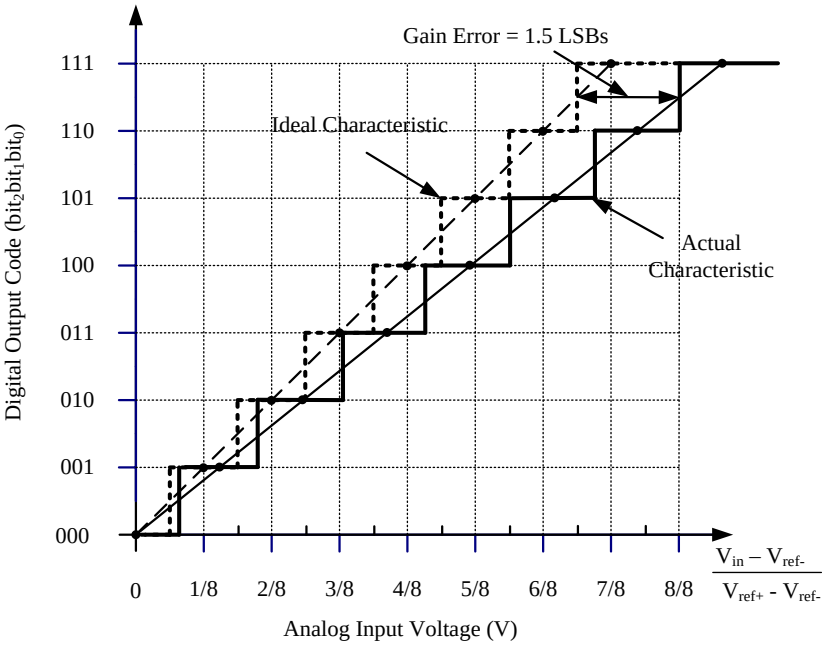


Figure 2.6. Gain Error illustration for a 3-bit ADC.

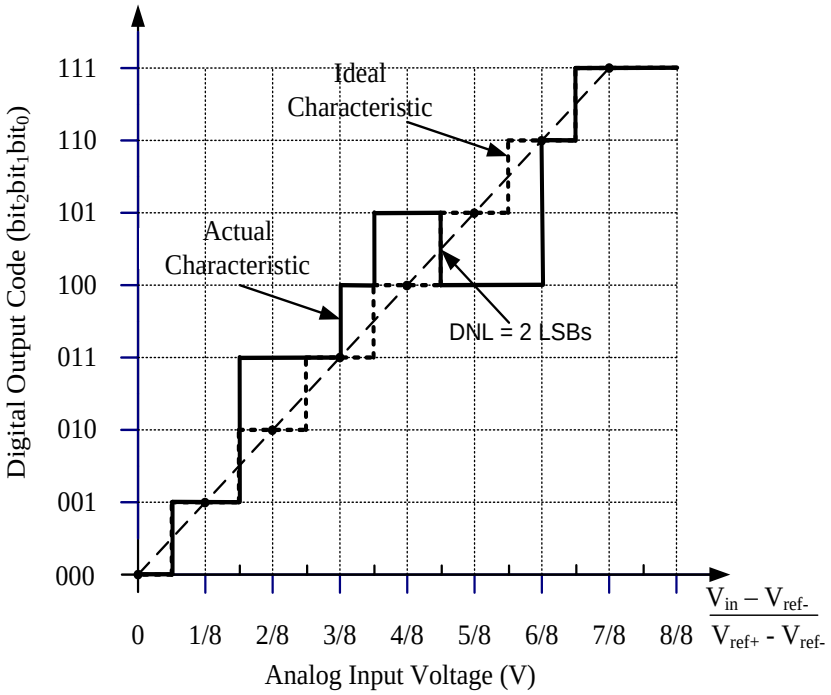


Figure 2.7. Monotonicity illustration for a 3-bit ADC.

**Spurious Free Dynamic Range (SFDR)** is defined as the ratio of the RMS value of the input sine wave for an ADC to the RMS value of the peak spur observed in the frequency domain. SFDR is expressed in decibels (dB) and is of importance in certain communications system.

**Total Harmonic Distribution (THD)** is defined as the ratio of the sum of the power of all harmonic frequencies above the fundamental frequency to the power of the fundamental frequency and is expressed as a percentage.

**Effective Number of Bits (ENOB)** is derived from the SNR and is given by the following equation [1].

$$ENOB = \frac{SNR_{actual} - 1.76}{6.02} \tag{2.4}$$

**Accuracy** is defined as the difference between the expected and the actual transfer response. The absolute accuracy includes the offset, gain and the linearity errors and relative accuracy is defined to be the accuracy after the offset and gain errors have been removed.

## 2.4 Delta-Sigma ADC

The delta-sigma (ΔΣ) converters trade resolution in time (bandwidth) for resolution in amplitude, so that imprecise analog circuits can be used in the design. ΔΣ converters are well suited for low bandwidth, high resolution and low cost making them a good ADC choice for many applications [3]. Delta-sigma (ΔΣ) analog-to-digital converters have been successful in realizing high resolution consumer audio products, such as MP3 players and cellular phones for some time now and recently in wireless sensor application. As explained earlier, ΔΣ converters are well suited for low bandwidth, high-resolution acquisition, and low cost, making them a good ADC choice for many applications. Delta-sigma converters combine an analog delta-sigma modulator with a more complex digital filter. Accuracy depends on the noise and linearity performance of the modulator, which uses high performance amplifiers. Delta-Sigma modulators trade resolution in time for resolution in amplitude such that the use of imprecise analog circuits can be tolerated [3, 4].

A block diagram of an analog-to-digital converter using delta-sigma modulator is shown in Figure 2.8. Delta-sigma converters come into the category of oversampled converters. Oversampling is simply the act of sampling the input signal at a frequency much greater than the

Nyquist frequency. One significant advantage of the method is that analog signals are converted using only a 1-bit ADC and analog signal processing circuits having a precision that is usually much less than the resolution of the overall converter. The penalty paid for the high resolution achievable with delta-sigma is that the hardware has to operate at the oversampled rate, much larger than the maximum signal bandwidth, thus demanding great complexity of the digital circuitry. Because of this limitation, these converters have traditionally been relegated to high-resolution, very-low frequency applications. In delta-sigma ADC, the digital low pass filter (decimation) stage which is responsible for achieving higher resolution and able to program a decimator offers further advantage of operating the ADC at different input channel bandwidths and with different oversampling ratios [3] which has been the focus of this research in Chapter 3.

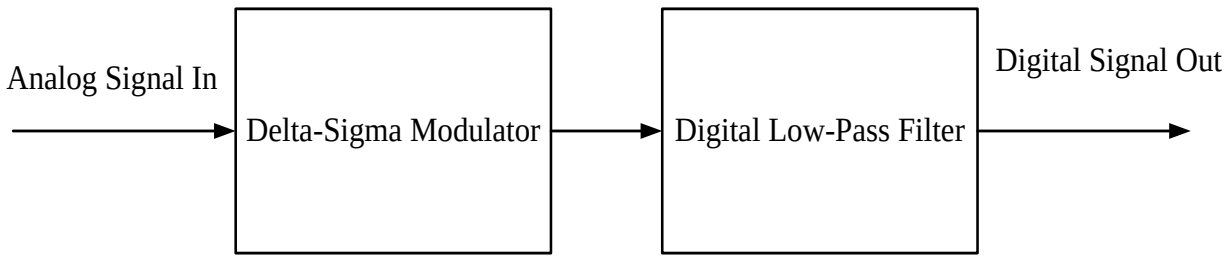


Figure 2.8. Block diagram of A/D converter.

The programmable ΔΣ ADC consists of an analog second order oversampled delta-sigma modulator and a digital third order decimator. Since it is difficult to program the analog second order delta-sigma modulator, the designed third order digital decimator of cascaded integrator comb filter type is made programmable to operate at three different oversampling ratios to give three different resolutions [5, 6]. Also in the designed programmable oversampling delta-sigma ADC, the decimator occupies most of the die area and consumes most of the power. In the

decimator, as the major part of powers consumed is by the integrator that operates at the higher sampling rate, introducing programmability by inserting coder circuits and reusing the same integrators for different resolutions and oversampling ratio has resulted in better optimized design in terms of area and power efficiency [3].

In the design to avoid the bit overflow in the integrator sections, 2's complement representation is used. In the design, coder circuits are used to reuse the same integrator for different resolutions and oversampling ratios and are designed by using multiplexer to sign extend the MSB and substituting it for appropriate bits. The performance metrics for the designed second order programmable oversampling delta-sigma ADC has also been investigated and presented in the following chapter.

## 2.5 Testability of CMOS Data Converters

Systems for defense, homeland and security and space applications use off-the shelf electronic components especially integrated circuits designed and fabricated globally. There have been reported several techniques where malicious hardware Trojan circuits can be embedded into a system hardware [7, 8]. Detection techniques have been developed where inserted Trojans either can become detectable or their effects reduced thereby safeguarding the security of the system in use [9]. Some of the other techniques are based on information hiding and constraint manipulation based trusted IC design [10]. Fault-tolerant techniques are effective against failures and mistakes due to natural causes [11]. Deliberate faults or intelligent attackers work in stealth mode and use non-fault-tolerant hardware where hardware Trojans helps to perform their malicious goals.

The process variations pose very severe threat in current CMOS technologies. The process variation changes MOS model parameters and has detrimental effects specifically in the reliability and performance of mixed-signal and analog integrated circuits. Thus, modification can also be done during the manufacturing of integrated circuits in pretext of manufacturing defects assuming no tampering has been in the tape-out of the design file data. Thus, there is an urgent need to develop technology of detection of piracy of integrated circuits before these are put to use in actual systems. It also becomes extremely important since not all integrated circuits may be tested for actual use in military and space applications.

Testing of integrated circuits has hence become an integral part of manufacturing cycle. The focus of present research is on testing of analog-to-digital converters as these integrate both digital and analog integrated circuits and testability has been complex, costly and time consuming. Hence, these could be used as bench mark circuits for developing testing methodologies for detecting Trojans and possible unnoticeable manipulation at any level of design and technology implementations. As explained in the earlier chapter, testing of data converters can be divided into fault detection based testing and functionality based testing.

Individual traditional fault detection based testing methods such as the quiescent current testing, oscillation test methodology and the logic Scan-Path method in presence of faults and manufacturing defects have been examined by our research group and attempt to combine some or all of these testing methods for better testability and detecting possible Trojans in fabricated circuits [12, 13] under simulated conditions. Combination of multiple testing methods allowed simulated faults or manufacturing defects, introduced during design phase of integrated circuits,

testing simultaneously at multiple levels thereby increasing fault coverage and reducing the testing time needed for traditional testing.

Based on the built-in current sensors (BICS) for $I_{DDQ}$ testing of CMOS delta-sigma (or sigma-delta) analog-to-digital converters and charge scaling digital-to-analog converters designed and implemented [14-17] earlier in our research group, the presented research highlights an attractive BICS for $\Delta I_{DDQ}$ testing of CMOS data converters that takes into account the effect of process variation and increasing background current. In this method, the differential measurement successfully suppresses the impact of background current and process variation.

To improve the fault coverage and efficiency of the testability for analog-to-digital converter, functionality based linear ramp histogram testing technique [18] has been designed. The designed linear ramp histogram technique consists of a linear ramp generator, circuit-under-test (CUT), code detection unit, and interface/control unit. The code detection unit was first designed by using the synchronous counter and read/write interface/enable circuit to record the sample or occurrence. The synchronous counter is designed by using the JK flip flop and AND gate. Also an optimized version of the code detection unit using 6T SRAM cells instead of the synchronous counter was designed, implemented and tested as a part of this research. The designed histogram technique can be seamlessly combined with other testability technique to improve the fault coverage.

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# CHAPTER 3

# PROGRAMMABLE SECOND ORDER OVERSAMPLING CMOS DELTA-SIGMA ANALOG-TO-DIGITAL CONVERTER*

## 3.1 Introduction

Recent evolutions in integrated circuit and low-power design have led to the development of many low-cost, low-power battery operated wireless sensor networks [1]. Wireless sensor networks allow device mobility, fast and easy installation and relocation according to needs. These sensor networks can be used in many applications such as the natural habitat, environmental and structural health monitoring, health care and warning against bio-warfare agents [1-4]. The wireless sensor network consists of a large number of sensor nodes which are autonomous and spatially distributed to measure the environmental and physical conditions to be sensed as shown in Figure 3.1 [4]. These sensor nodes consist of sensing module, data processing with internal or external memory, communication module and power module as shown in Figure 3.2 [4]. The sensing module in the sensor node includes a sensing device to monitor and produce an analog signal which is converted to a digital output through an analog-to-digital converter (ADC).

* Part of the work in this chapter was previously reported in following publications:

1. R. Soundararajan, A. Srivastava and J. Kamar, "A programmable second order oversampling CMOS sigma-delta analog-to-digital converter for wireless sensor networks," *Proceedings of the 12th International Conference on Information Technology (ICIT 2009)*, pp. 227-232, December 21-24, 2009.
2. R. Soundararajan and A. Srivastava, "A programmable second order oversampling CMOS sigma-delta analog-to-digital converter for low-power sensor interface electronics," *Proceedings of SPIE: Nano-, Bio-, and Info-Tech Sensors and Systems*, vol. 7646, pp. 7646P-1-7646P-11, March 7-11, 2010.
3. R. Soundararajan and A. Srivastava, "A programmable oversampling CMOS delta-sigma analog-to-digital converter for low-power interface electronics," *Journal of Low Power Electronics*, vol. 8, No. 3, pp. 336-346(11), June 2012.

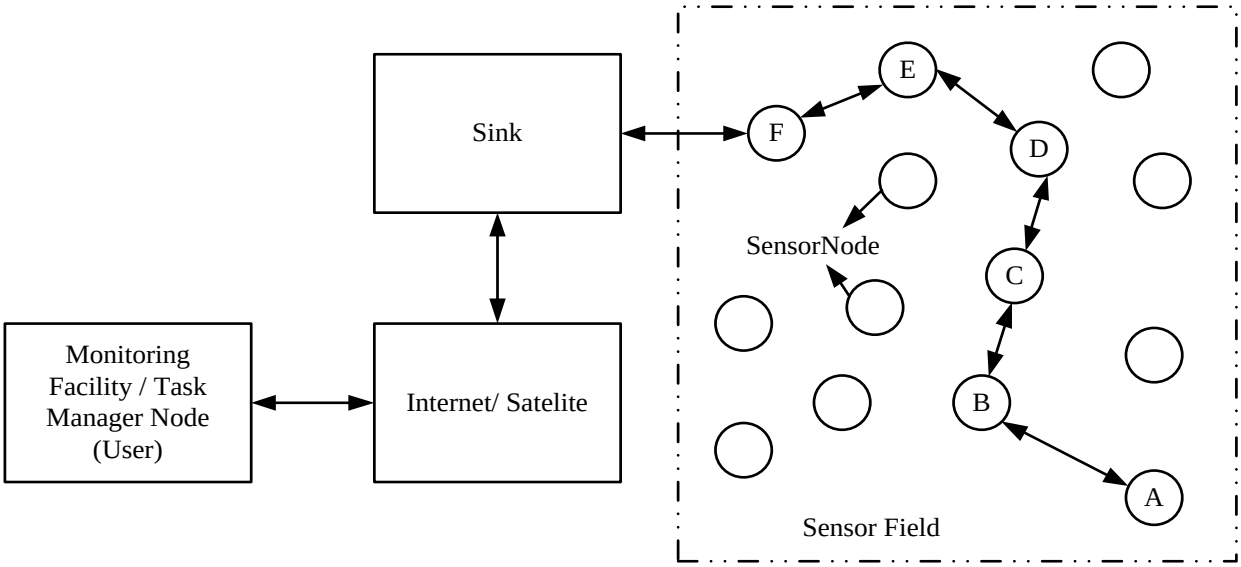



Figure 3.1. Sensor network [4].

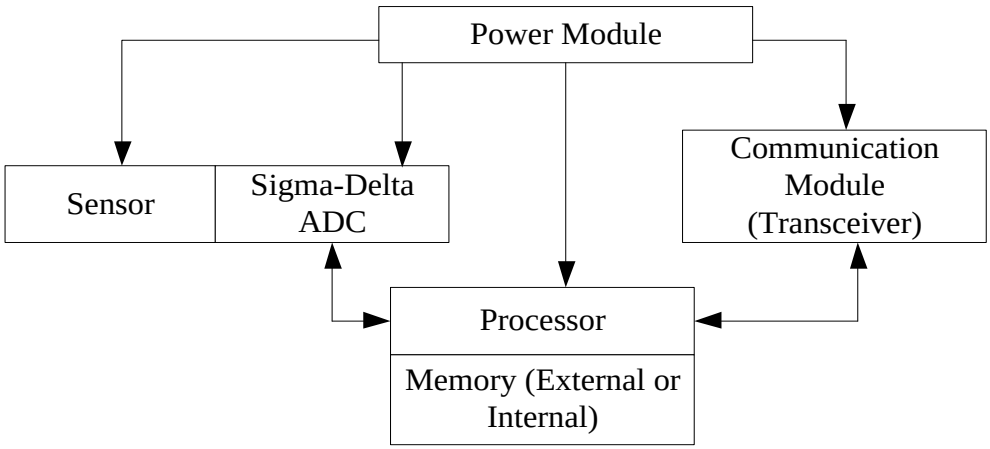



Figure 3.2. Block diagram of a sensor node [4].

In wireless sensor networks, the effective and efficient use, its design and architecture are influenced by many factors such as the fault tolerance, scalability, production cost, operating conditions, sensor network topology, hardware constraints, transmission media and most importantly the power consumption to maximize the network lifetime, add flexibility, facilitate data collection and minimize the need for maintenance of the sensor node. This becomes important due to the fact that the sensor nodes are mostly equipped with limited power source for mobility and relocation, and cannot be easily replenished. Recently, most of the research in the sensor network has been focused on the development of low-power and energy efficient hardware [4-6], because the lifetime of the sensor node shows a strong dependence on the batter lifetime. The roles of the communication module and the processor in the power consumption have been widely addressed by several researchers [4-6] which led to new architectures. In the sensor module, the resolution of the ADC has direct impact on energy consumption of the module since every bit consumes significant power. Hence, high resolution is not needed in a sensor node and so the work focuses on ADC that can be of programmable type, thereby allowing programming the resolution depending upon the need.

The focus is on design and implementation of a programmable second order oversampling CMOS delta-sigma (ΔΣ) analog-to-digital converter using programmable cascaded integrator comb (CIC) decimation filter in 0.5µm n-well CMOS processes for integration in sensor nodes for wireless sensor networks. We have selected the delta-sigma ADC as they provide very high resolution by oversampling and modulation and utilize low-performance analog circuitry by shifting the burden on the digital circuitry.

## 3.2 Programmable Second Order Oversampling Delta-Sigma (ΔΣ) ADC

The second order oversampling delta-sigma ADC consists of an analog second order oversampled delta-sigma modulator and a digital third order decimator. The second order delta-sigma modulator samples the analog input signal at much higher frequencies set by the oversampling ratio (K) and convert the analog input signal into a 1-bit pulse density modulated digital output containing both the original input signal and the unwanted out-of-band noise. Sigma (Σ) stands for the summation in the modulator and delta (Δ) is used because of the delta (difference) modulation. The density of the pulses in the modulator output represents the average value of the signal over a specific period. Hence, most of the pulses are high at the positive peak of the sine wave and low at the negative peak of the sine wave. In between the pulses are distributed between low and high depending on the value of the sine wave. The modulator is then followed by the digital third order decimator as shown in Figure 3.3.

The decimator acts as a digital low pass filter, which attenuates the quantization noise above the baseband and suppresses the out-of-band spurious signals, and also down samples the 1-bit encoded output from the modulator to an N-bit high resolution digital output code at the Nyquist rate. The decimator works on the same principle of an averaging filter. The resolution of the delta-sigma ADC is set by the oversampling ratio, K and also the order of the modulator and the decimator [7]. Both the modulator and the decimator are operated with the same oversampling clock. As it is desirable to design an ADC for the sensor node which gives outputs of different resolutions and work at different frequencies and since it is difficult to program analog second order oversampled delta-sigma modulator [8], digital decimator of Cascaded

Integrator Comb (CIC) filter type in the present work, is designed to operate at three different oversampling ratios of 16, 32 and 64 to give three different outputs of resolutions of 9, 12 and 14 bits, respectively [9].

### 3.3 Second Order Delta-Sigma Modulator Theory and Design Implementation

The second order oversampled delta-sigma modulator is the analog part of the ADC and consists of two discrete analog time integrators and a 1-bit quantizer (ADC) in the forward path and a 1-bit digital-to-analog converter (DAC) in the feedback path of a single feedback loop system as shown in Figure 3.4 [10]. The number of integrators in the forward path determines the order of the modulator. The discrete time integrator consists of operational amplifier and switched capacitor circuits [9-11]. The 1-bit quantizer is implemented by using a latched comparator and is an important component as it is required to work at high oversampling clock and low resolution and is in synchronization with the other components of the circuit [12-14]. The 1-bit DAC in the feedback loop is implemented by using a multiplexer circuit controlled by the output of the latched comparator and connected with the reference voltage ($V_{ref+}$ and $V_{ref-}$).

When the integrator output is greater than the reference voltage at the comparator input, the comparator gives an output ‘high’. This output high controls the DAC which gives an output of $V_{ref+}$ which is subtracted from the input of the modulator in order to move the integrator output in the negative direction. Similarly when the integrator output is less than the reference voltage at the comparator input, the feedback path moves the integrator output in the positive direction. Therefore, the integrator accumulates the difference between the input and quantized output signals and tries to maintain the integrator output around zero. A zero integrator output implies

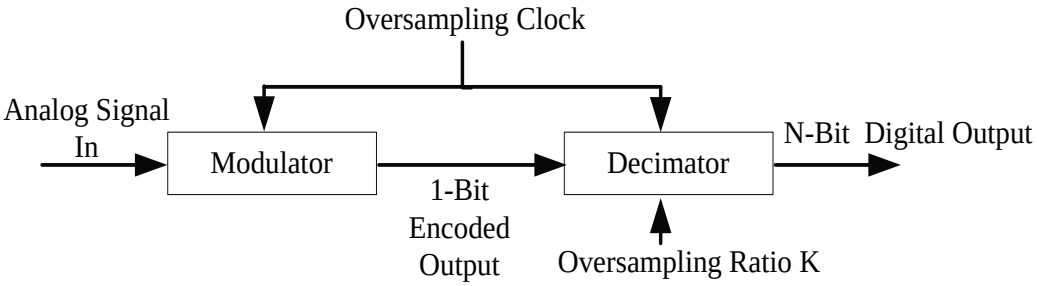



Figure 3.3. Block diagram of a second order oversampled delta-sigma ADC [7].

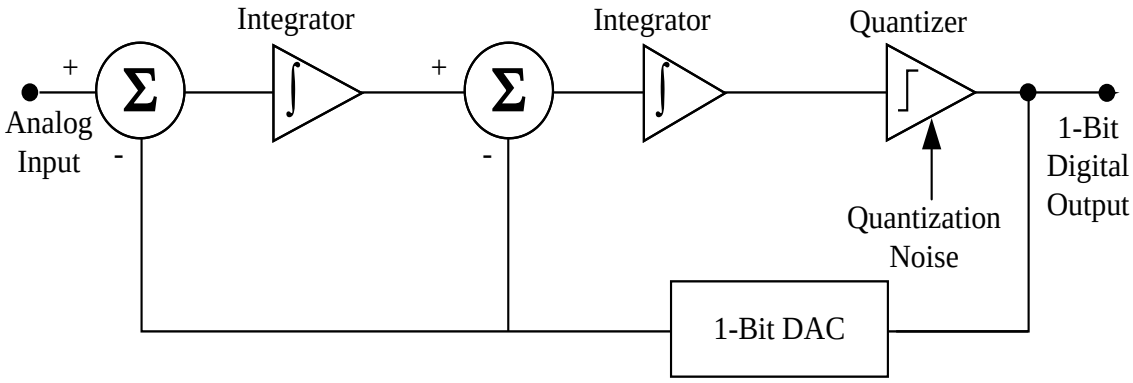



Figure 3.4. Second order delta-sigma modulator [9].

that the difference between the input signals and the quantized output is zero. Thus the average value at the output will be equal to the value at input.

Since delta-sigma modulator uses the principle of oversampling, the need for anti-aliasing filter is eliminated and the analog input signal can be directly sampled using the oversampling clock [11]. Hence, the accuracy of the analog circuitry can be compromised with the speed. The second order oversampling delta-sigma modulator is selected to provide a better signal-to-noise ratio. The modular output is described by the following expression which consists of a delayed, unchanged replica of the input and a differentiated version of the quantization noise [9].

$$Y(z) = z^{-1}X(z) + \left(1 - z^{-1}\right)^2 N(z) \tag{3.1}$$

The quantization noise in the second order delta-sigma modulator is thus pushed to higher frequencies or beyond the bandwidth of the signal of interest which can be filtered out by using a low-pass decimation filter in the next stage [15].

### 3.3.1 Discrete Analog Integrator Design Implementation

The discrete time analog integrator is designed by using switched-capacitor parasitic insensitive technique which consists of a sampling capacitor $C_S$, an integrating capacitor $C_f$ and MOS switches driven by a non-overlapping clock and an operational amplifier [9, 11], as shown in Figure 3.5. Hence, the modulator does not use sample and hold circuits unlike in other ADC architectures. Since the output of the modulator is a pulse density modulated signal, the modulator is able to construct these pulses in real time, and so it is not necessary to hold the input value and perform the conversion. The clock signals $\Phi_1$, $\Phi_2$, $\Phi_{1d}$ and $\Phi_{2d}$ form the non-overlapping clock signals driving the MOS switches and are generated by using the circuit

shown in Figure 3.6. The clocking sequence for the non-overlapping clock signals generated by the circuit is also shown in the figure. The common mode voltage, $V_{CM}$ falls halfway between the mixed-signal systems 'high' and 'low' reference voltages. In the designed modulator, the high reference voltage is +2.5V and low reference voltage is -2.5V and hence the common mode voltage $V_{CM}$ will be 0V.

The values of capacitances are $C_S$= 0.5pF and $C_F$ = 0.5pF so that the gain of the integrator is 1. The gain should be kept at 1 or less than 1 to make the second order modulator loop stable and also to avoid integrator from saturating. The capacitance ratio is important than the individual values of the capacitors. Even smaller capacitances can be used but to avoid charge leakage problem and also the droop rate of the hold capacitor they were chosen to be large.

The capacitors are designed using two poly layers, poly1 and poly2 as shown in Figure 3.7 (a). During the fabrication process of on-chip capacitors, the capacitance value of a single capacitor can vary up to 10 to 30 percent from the desired value. Hence to compensate, capacitance ratios are used in design so that the relative error is cancelled since capacitance is expressed in integral multiples of a unit size capacitor. A common-centroid layout is used to reduce the mismatch of the capacitance values as shown in Figure 3.7 (b). The substrate noise present in the substrate can be coupled to the designed capacitor through its parasitic capacitor and also any voltage variation present is also coupled to other components of the chip. To avoid this coupling, the capacitor array is shielded from the substrate with N-well under it and connecting it to a quiet DC potential [16]. The guard rings are used in the layout around the capacitor array to prevent from any sought of interference.

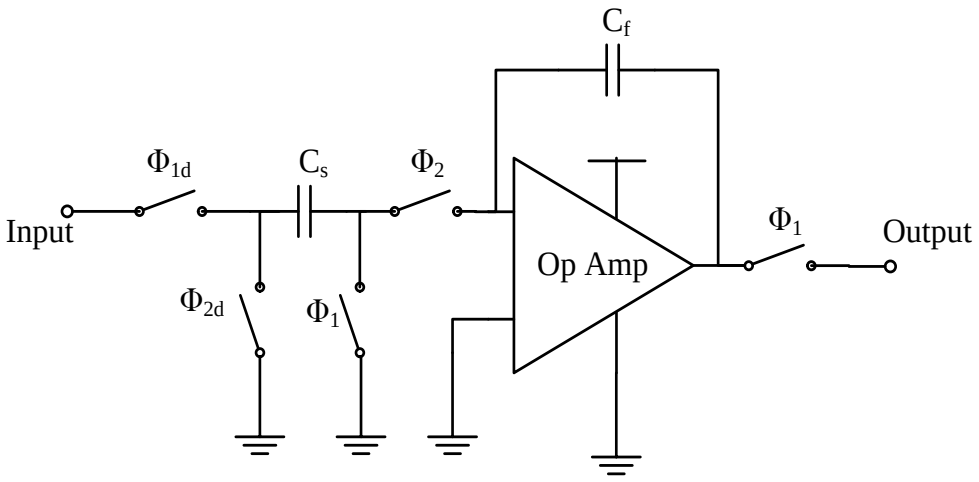



Figure 3.5. Parasitic insensitive switched capacitor discrete analog integrator [9].

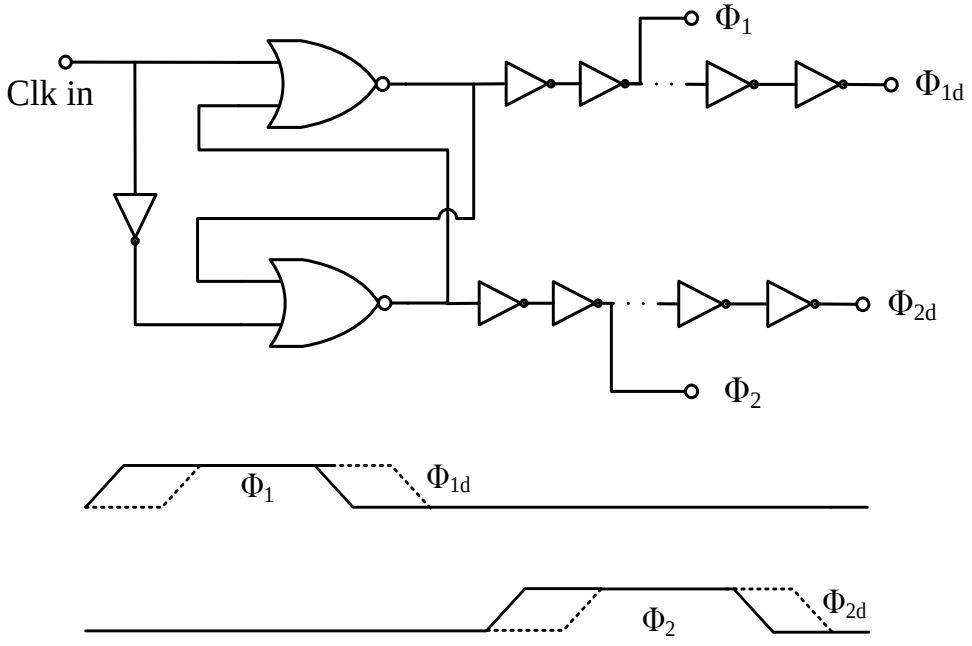
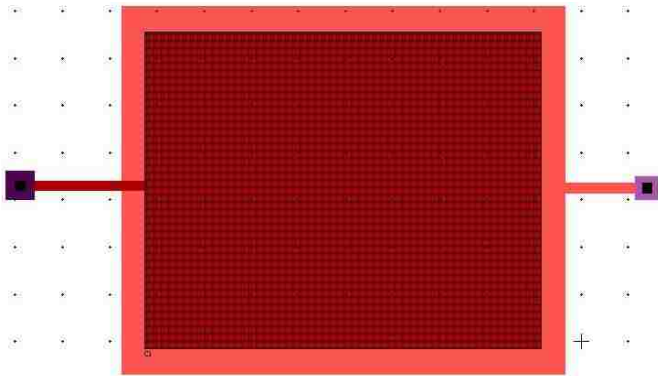
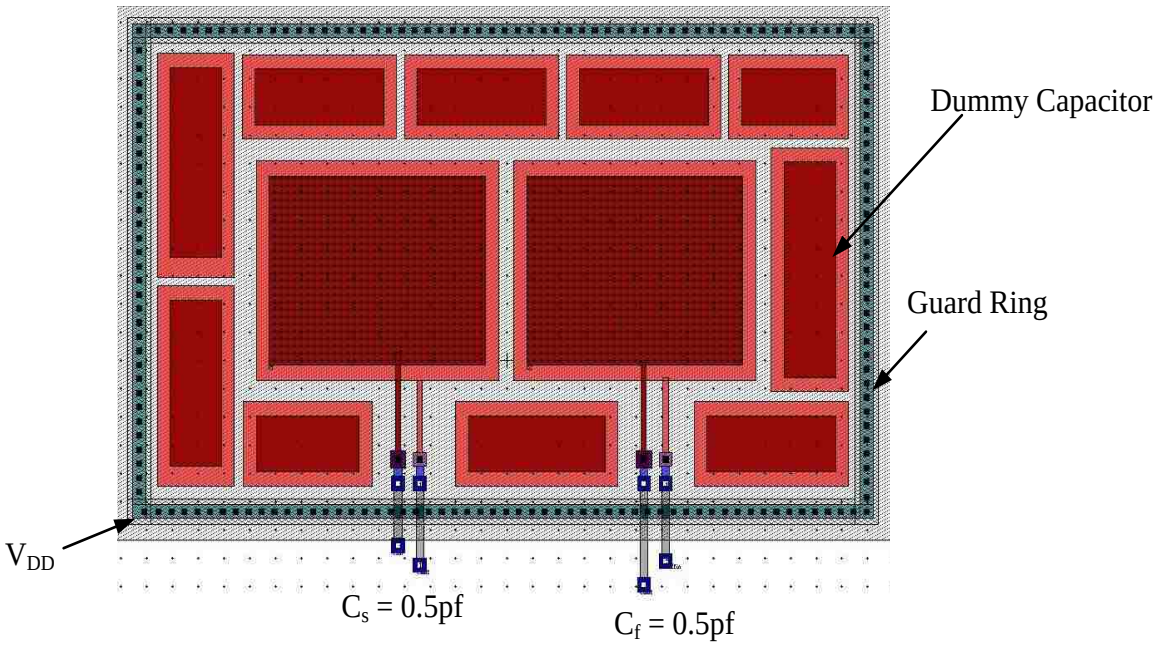



Figure 3.6. Non-overlapping clock phase generator circuit with clocking sequence.



(a)




(b)

Figure 3.7. (a) Layout of a capacitor made of poly1 and poly2 and (b) Layout of the capacitors using common-centroid technique.

3.3.1.1 Design of Operational Amplifier

In this design, the operational amplifier is the core element and designed using a two-stage CMOS amplifier, providing good voltage gain, common-mode range, high bandwidth, high input impedance, low output impedance and good output swing [9, 17, 18]. It consist of four main functional blocks, input differential gain stage, differential to single-ended conversion stage, DC level shift stage and second gain stage as shown in Figure 3.8 [19]. The input differential gain stage amplifies the voltage difference between the input terminals, independently of their average or common-mode voltage. Most of the critical parameters of the operational amplifier like the input noise, common mode rejection ratio (CMRR) and common mode input range (CMIR) are decided by this stage. This stage is followed by the differential to single-ended conversion stage, responsible for producing a single-ended output which can be referenced to ground. The next stage is the DC level shift stage and is needed to bias the second gain stage properly. The second gain stage is used to obtain additional gain.

Figure 3.9 shows two-stage CMOS operational amplifier architecture and consist of an input differential gain stage followed by a second gain stage [9, 17, 18]. The first stage consist of p-channel differential pair M1-M2 with an n-channel current mirror load M3-M4 and a p-channel tail current source M7. This stage gives a good differential gain and also performs the differential to single-ended conversion. The second stage consists of an n-channel common source amplifier M5 with a p-channel current load M6. The operational amplifier is designed for operation at ±2.5 V. The aspect ratio of the various transistors in the two-stage CMOS operational amplifier is also shown in the Figure 3.9.

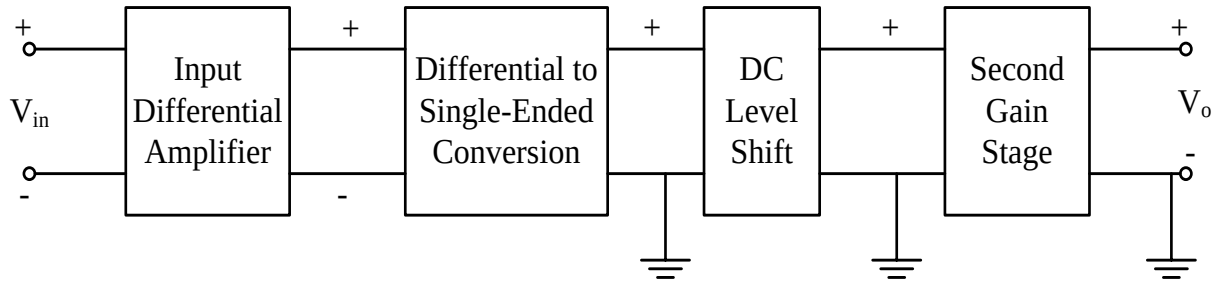



Figure 3.8. Block diagram of a two stage CMOS operational amplifier [19].

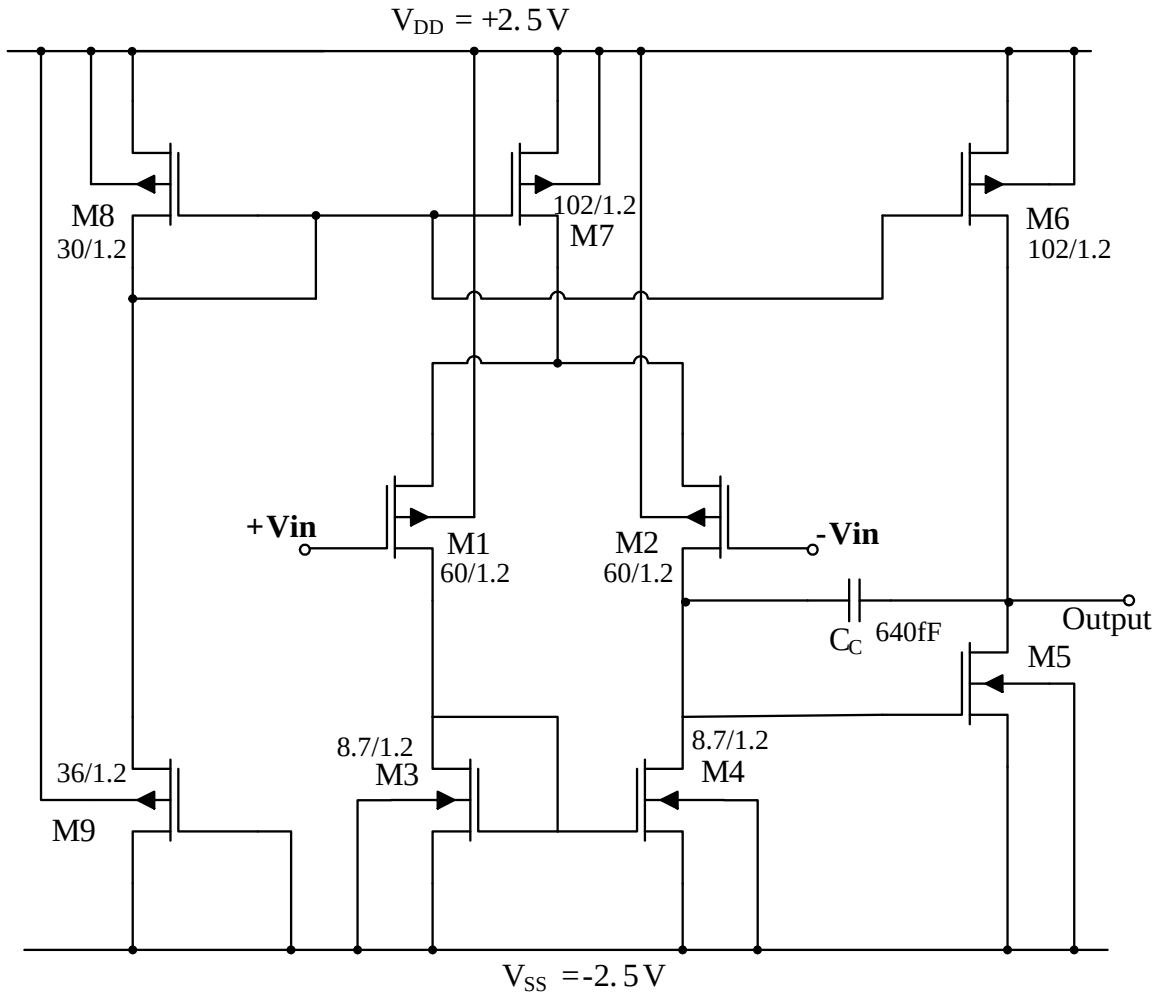



Figure 3.9. Schematic of two-stage operational amplifier.

3.3.1.2 Discrete Analog Integrator Results

The complete layout of the digital analog integrator block as in Figure 3.5 is shown in Figure 3.10. The output of the integrator when a square wave is used as an input ($V_1$) is as shown in Figure 3.11. In the integrator, voltages $V_2$ and $V_{CM}$ are connected to ground while simulating the integrator. The integral of the square wave, triangular wave is obtained at the output. The triangular wave has a maximum of +2.5V and minimum of –2.5V. The output will saturate and remains constant if it crosses the maximum and minimum limits. Since the output depends on the beginning output value, it takes times to settle to the final steady state value.

### 3.3.2 1-Bit Quantizer (ADC) Design Implementation

A 1-bit analog-to-digital converter (ADC) acts as the quantizer in the second order delta-sigma modulator design. Since the quantizer (ADC) is of 1-bit it has only two levels either a ‘1’ or a ‘0’. A ‘1’ implies that $V_{DD}$ =+2.5V and a ‘0’ implies that $V_{SS}$ =-2.5V. If the output of the integrator is greater than the reference voltage (0V) it has to give an output of ‘1’ and if the integrator output is less than reference voltage then the output of the ADC should be a ‘0’. A latched comparator is used as a quantizer in this design and performs the required function efficiently. Given a reference level of 0V, a comparator gives an output of $V_{DD}$ when the signal is greater than 0V and an output of $V_{SS}$ when signal is less 0V. Thus two-stage operational amplifier can be used as a comparator. The only change needed is that the comparator doesn’t require the compensation capacitor which is required by the operational amplifier. The latched comparator design is as shown in Figure 3.12 [9].

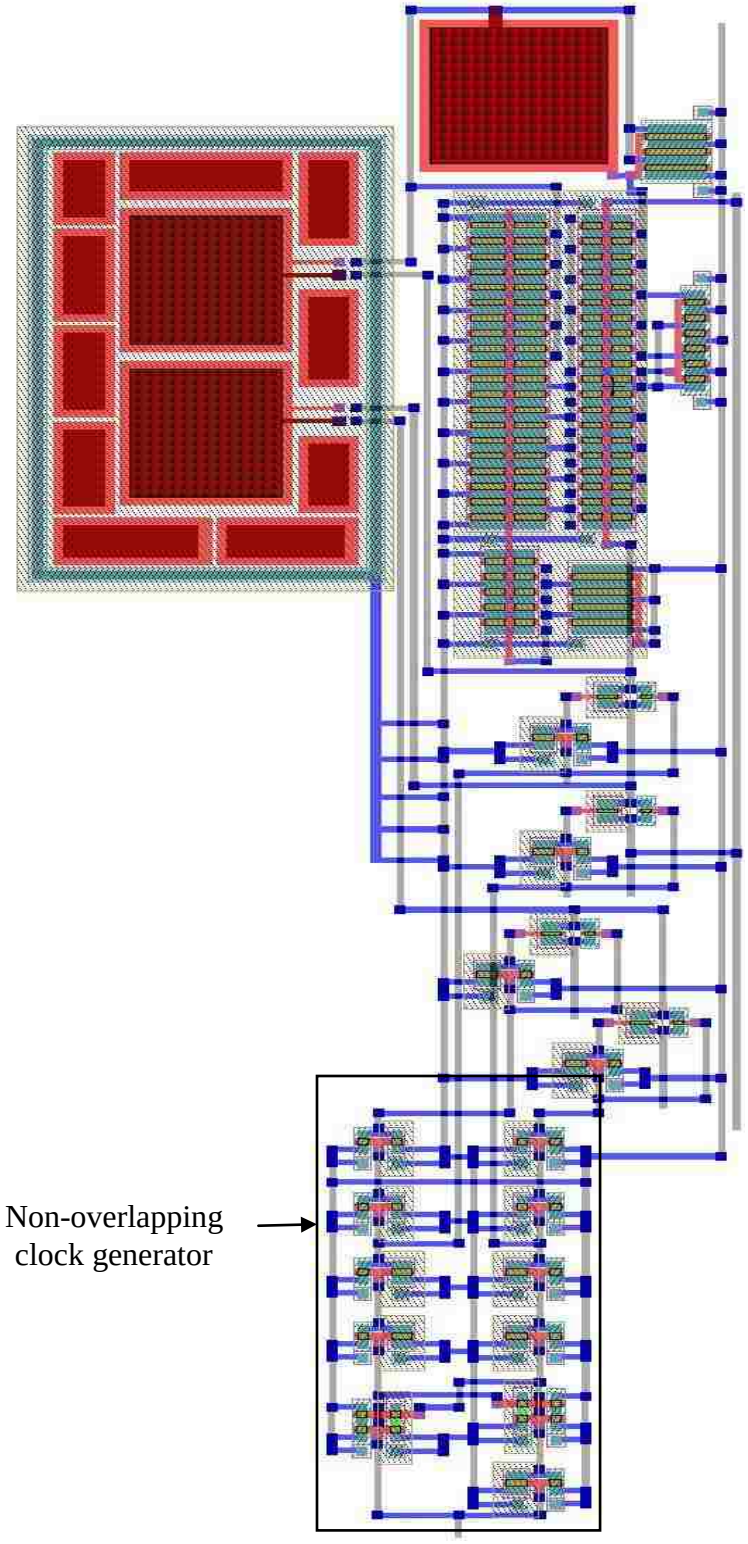



Figure 3.10. Complete layout of the discrete analog integrator with non-overlapping clock generator.


Figure 3.11. Transient response from post layout simulation of discrete analog integrator.

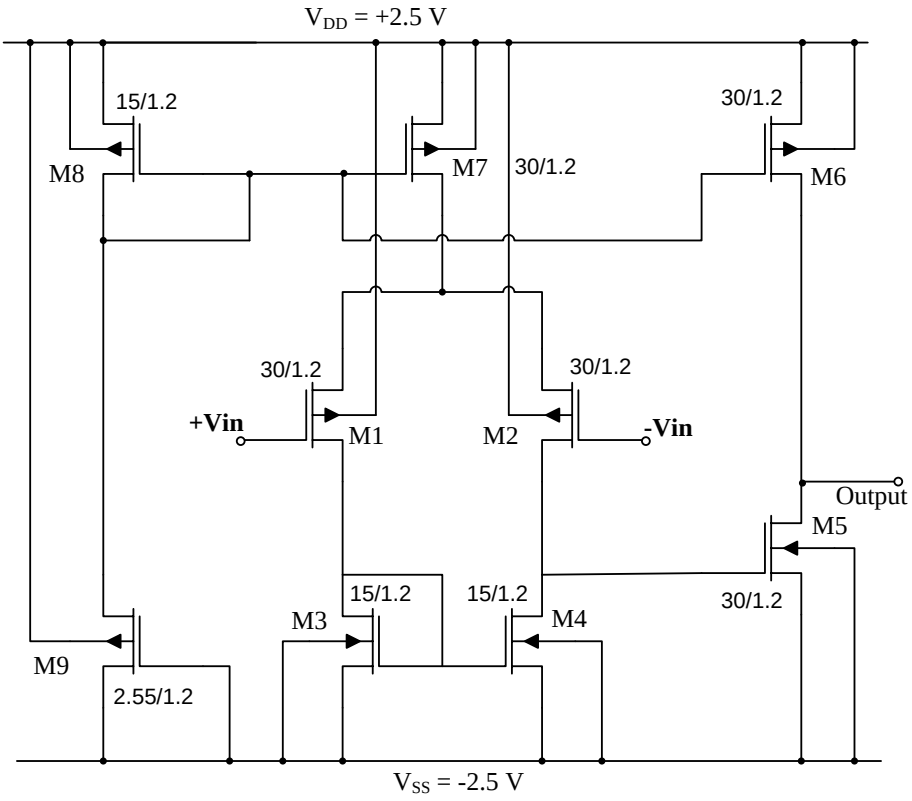



Figure 3.12. Schematic diagram of a two-stage comparator.

### 3.3.3 1-Bit Digital-to-Analog Converter (DAC) Design Implementation

The 1-bit digital-to-analog converter (DAC) is used in the design to convert the 1-bit digital output of the latched comparator to the analog signal. As the DAC used is 1-bit, the corresponding analog output will also have two reference levels ($V_{ref+}$ =+2.5V and $V_{ref-}$ =-2.5V) and is almost similar to the digital input from the latched comparator output. If the digital input is '1' then the DAC output will be $V_{ref+}$ and if the input is '0' then the output will be $V_{ref-}$. The 1-bit DAC can be designed using a simple multiplexer circuit as stated earlier and selects between the $V_{ref+}$ and $V_{ref-}$ signals depending on the 1-bit digital input signal. Figure 3.13 and Figure 3.14 show the schematic and layout of the simple multiplexer circuit diagram used as a 1-bit DAC.

## 3.4 Third Order Programmable Decimator Theory and Design Implementation

The third order programmable decimator acts as a low pass filter, which attenuates the quantization noise above the baseband and suppresses the out-of-band spurious signals, and as a downsampler, downsampling the filtered signal to the Nyquist rate. The output word rate of the decimator is down sampled by the factor K (oversampling ratio). The cascaded integrator comb (CIC) decimation filter used in this design consist of a combination of digital integrator and digital differentiator stages which perform the operation of digital low pass filtering and decimation [20]. The CIC filters do not require any multiplier circuits and hence are very economical for implementation in hardware and the problems with cascading faced by the accumulate-and-dump circuit are also overcome with the CIC design. In the CIC decimation filter, the averaging operation is performed first followed by the decimation. An area efficient

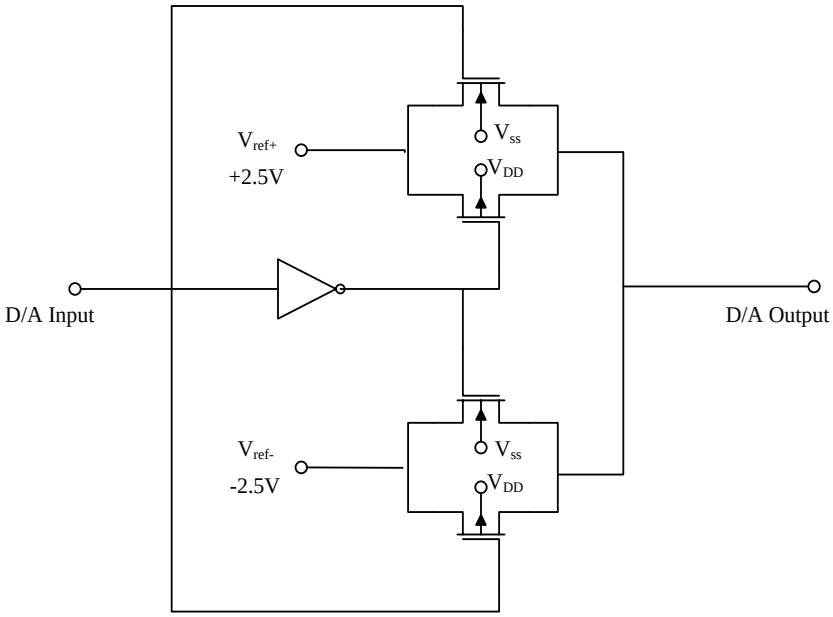



Figure 3.13. Schematic diagram of 1-bit DAC.

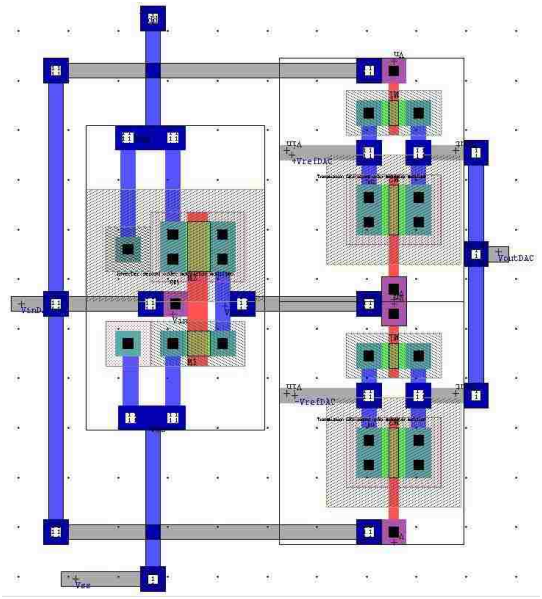


Figure 3.14. Layout of 1-bit DAC.

implementation of a first order CIC decimation filter by implementing a clock divider in between the integrator and differentiator stages is as shown in Figure 3.15. This design doesn't require any additional hardware to implement the decimation.

The clock divider circuit divides the oversampling clock signal by the oversampling ratio K. By dividing the clock frequency by K the number of delay elements used in the differentiator can be reduced to just one instead of K as in a traditional design. Also, in this design the integrator operates at the sampling clock frequency, $f_s$ while the differentiator operates at down sampled clock frequency of $f_s/K$. By operating the differentiator at lower frequencies, a reduction in the power consumption is achieved. The CIC decimator in the design is made to operate at three different resolutions by including the programmability feature in it. Since a second order modulator is used, a third order CIC decimator is required based on the following Eq. (3.2) [9].

$$L = M+1 \tag{3.2}$$

In Eq. (3.2), L is the order of the decimator and M is the order of the modulator. Figure 3.15 shows the block diagram of a third order CIC decimator [20]. It consists of a combination of three integrator sections working at a high sampling rate equivalent to the oversampling clock, followed by the down sampler and three differentiator (comb) sections working at the reduced sampling rate dependent on the oversampling ratio, K. The transfer function H(z) of the third order decimator shown in Figure 3.16 is given by [9, 20],

$$H(z) = \left( \frac{1}{K} \frac{1 - z^{-K}}{1 - z^{-1}} \right)^3 \tag{3.3}$$

The digital integrator is pipelined in the design and acts as an infinite impulse response (IIR) filter and contributes to a pole while, the differentiator also called the comb filter is also pipelined in the design and acts as a finite impulse response (FIR) filter and contributes to a zero.

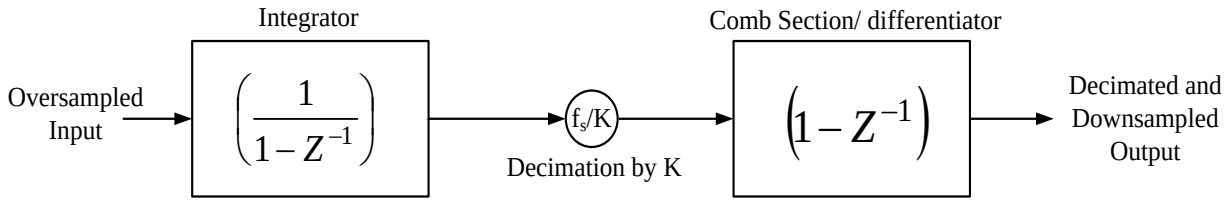



Figure 3.15. Block diagram of first order CIC decimation filter.

The time domain representation of the basic digital integrator is shown in Eq. (3.4) and its output is the sum of the present input and the past output [9, 20].

$$Y(nT_s) = X(nT_s) + Y\{(n-1)T_s\} \tag{3.4}$$

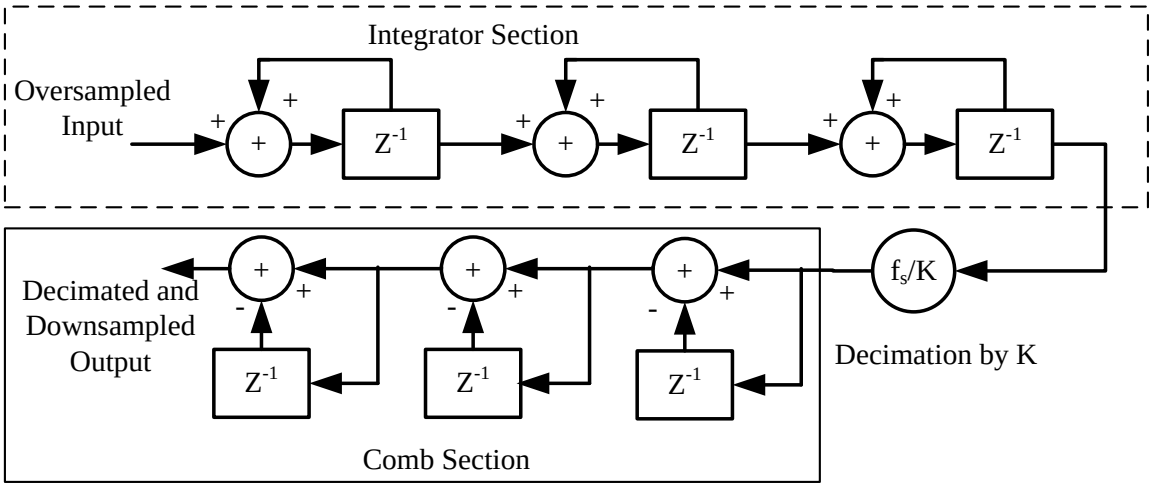



Figure 3.16. Block diagram of third order CIC decimator [9].

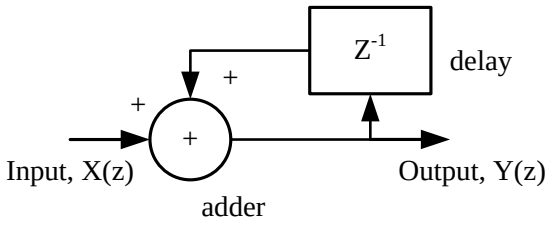
The stick diagram representation of the basic and pipelined digital integrator modeled is as shown in Figure 3.17 (a) and (b) respectively, based on Eq. (3.4). The delay element is designed using a memory element and is used to delay the output signal by one clock period and also to pipeline the output to create a pipelined integrator. A simple D-flip flop can be used to achieve the delay. In the digital integrator, to avoid register overflow two's complement coding scheme is used. The time domain representation of the basic digital differentiator is shown by Eq. (3.5) and its output is the difference between the present input and the past input [9, 20].

$$Y(nT_s) = X(nT_s) - X\{(n-1)T_s\} \tag{3.5}$$

The stick diagram of the digital differentiator modeled from the time domain representation in Eq. (3.5) is as shown in Figure 3.18. The two's complement output of the final integrator stage is applied to the input of the differentiator and hence the differentiator also uses the two's complement coding scheme. The final output of the differentiator, has to be in binary form for further processing and so the two's complement output is converted back to binary form.

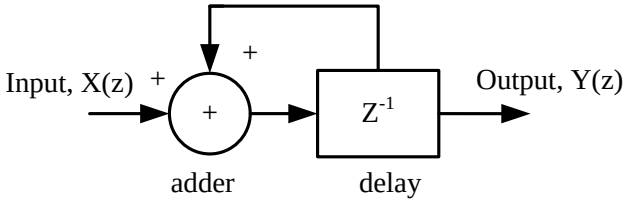
Both the digital integrator and digital differentiator consist of an adder and a delay element. In addition, the digital differentiator operates at a different clock frequency compared to that of the clock frequency of the digital integrator and hence the circuits act as individual blocks. They can be cascaded to form a cascaded integrator comb filter.

In the programmable oversampling delta-sigma (ΔΣ) ADC, the CIC decimator occupies most of the die area and consumes most of the power. In the CIC decimator, the major part of power consumed is attributed to the integrator which operates at the highest sampling rate (fs),




(a)

$$Y(z) = X(z) + z^{-1} Y(z)$$




(b)

Figure 3.17. Stick diagram of a (a) basic and (b) pipelined digital integrator.

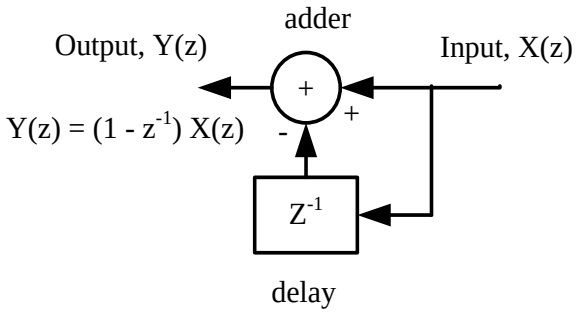



Figure 3.18. Stick diagram of a digital differentiator (comb filter).

compared to the differentiator ($f_s$/K). In the CIC decimator designed, each integrator consumes an average power of approximately 725 µw at a sampling frequency of 256 kHz. Hence, in this work, an alternate design has been investigated and modification has been done in the integrator stages by inserting coder circuits and reusing the same integrators for different resolutions and oversampling ratios, K as shown in Figure 3.19. This modified new design has been found to be better optimized in terms of area and power efficiency [9].

In each integrator section, the register growth (bit length) is increased by $Log_2K$ [20], where K is the oversampling ratio. Hence in the third order CIC decimator for the maximum oversampling ratio, K = 64, the output of integrator Section-1 has a maximum 7 bits resolution, the output of integrator Section-2 has a maximum 13 bits resolution and the output of integrator Section-3 has a maximum resolution of 19 bits [9, 20]. Similarly, the output resolution of each integrator section is 6, 11 and 16 bits for oversampling ratio K = 32, and 5, 9 and 13 bits for oversampling ratio K = 16. Thus, the modified CIC decimator design reuses integrator sections for the three oversampling ratios by introducing the coder circuits in between the integrator sections. Coder circuit-1 is used to create 7-bit 2's complement equivalent for the 1-bit oversampled output from the second order sigma-delta modulator. The 2's complement representation helps to avoid the bit overflow in the integrator sections.

Figure 3.20 shows the block diagram of coder circuits which are designed by using multiplexers. In coder circuit-2, for oversampling ratio, K = 64, the 7-bit output of the integrator section-1 is converted to 13-bit 2's complement by sign extending the MSB (bit 7) and substituting it for bit 7 through bit 13. This 13-bit data is used as the input for the integrator

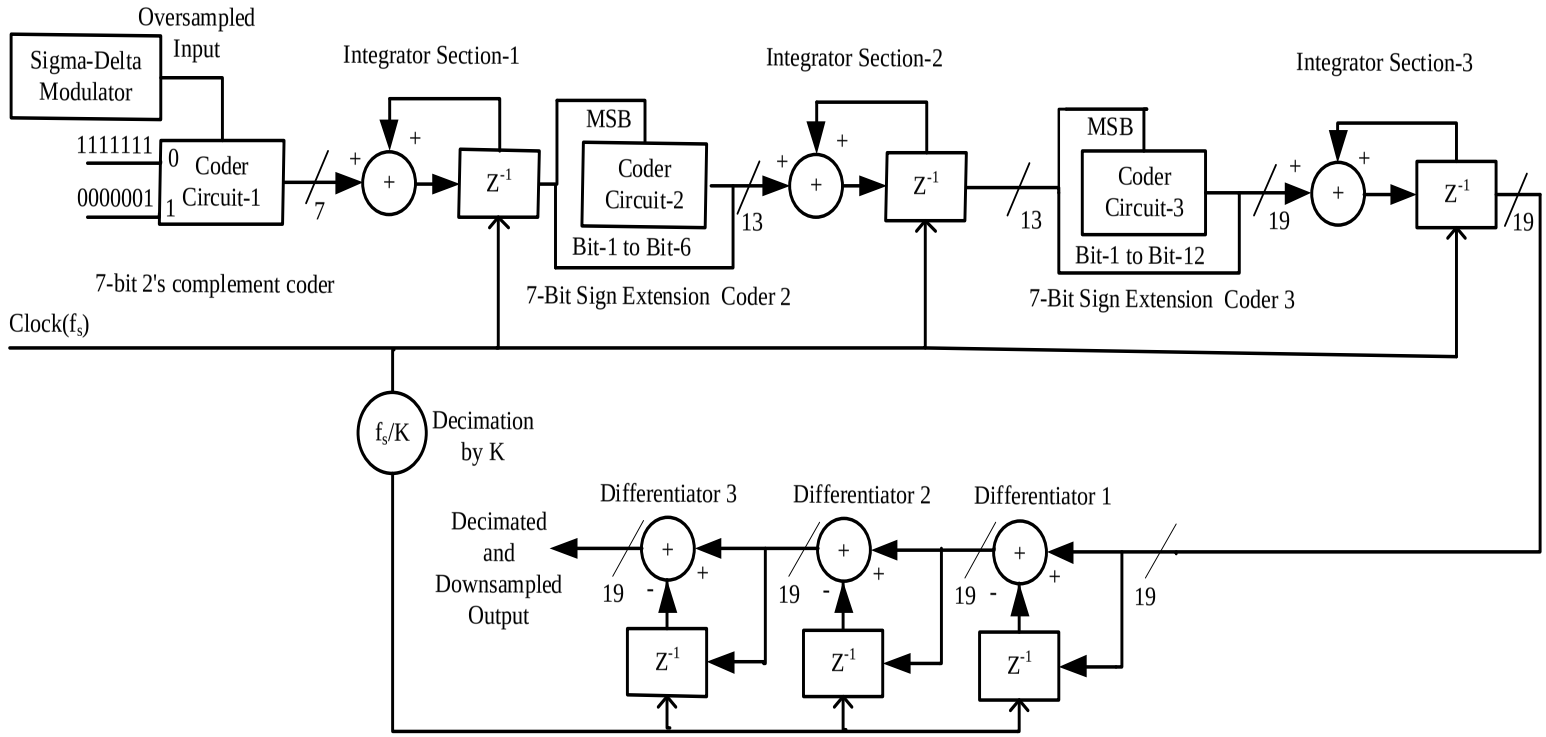



Figure 3.19. Block diagram of modified third order CIC decimator (K = 64) [23, 24, 25].

Section-2. Similarly for oversampling ratio, K = 32, the 6-bit output of the integrator Section-1 is sign extended to provide 11-bit data at the input of the integrator Section-2 and for oversampling ratio, K = 16, the 5-bit output of the integrator Section-1 is sign extended to provide 9-bit data at the input of the integrator Section-2. For example, in the case of oversampling ratio, K = 64 if the 7-bit output of the integrator Section-1 is (0)101010 (decimal equivalent 42), coder circuit-2 converts it into a 13-bit 2's complement by sign extending the MSB (bit 7) and substituting it for bit 7 through bit 13 and the 13- bit data (0000000)101010 (decimal equivalent 42) is achieved.

Similarly in coder circuit-3, for oversampling ratio, K = 64, the 13-bit output of integrator Section-2 is converted to 19-bit 2's complement by sign extending the bit 13 and substituting it for bit 13 through bit 19. The 19-bit data is used as the input for integrator section-3. Similarly for oversampling ratio, K = 32, the 11-bit output of the integrator Section-2 is sign extended to provide 16-bit data at the input of the integrator Section-3 and for oversampling ratio, K = 16, the 9-bit output of the integrator Section-2 is sign extended to provide 13-bit data at the input of the integrator Section-3 [21].

The coder circuit-2 and coder circuit-3 are programmed by using the enable signals (Enable-1 and Enable-2), which allow the integrator stages to be reused for different oversampling ratios. The clock signal fed to the differentiator stages is also programmed for 3 different oversampling ratios (K = 64, 32 and 16) by using a clock divider circuit and a multiplexer (MUX) controlled by the enable signals (Enable-1 and Enable-2) as shown in Figure 3.21.

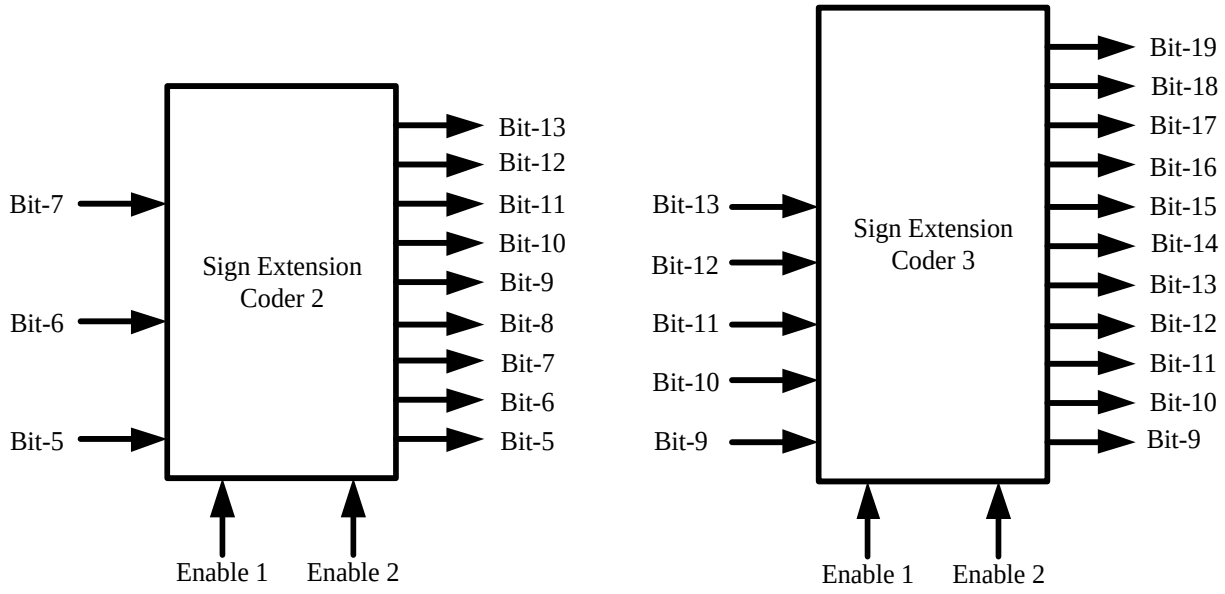



Figure 3.20. Block diagrams of coder circuits 2 and 3 [23, 24, 25].

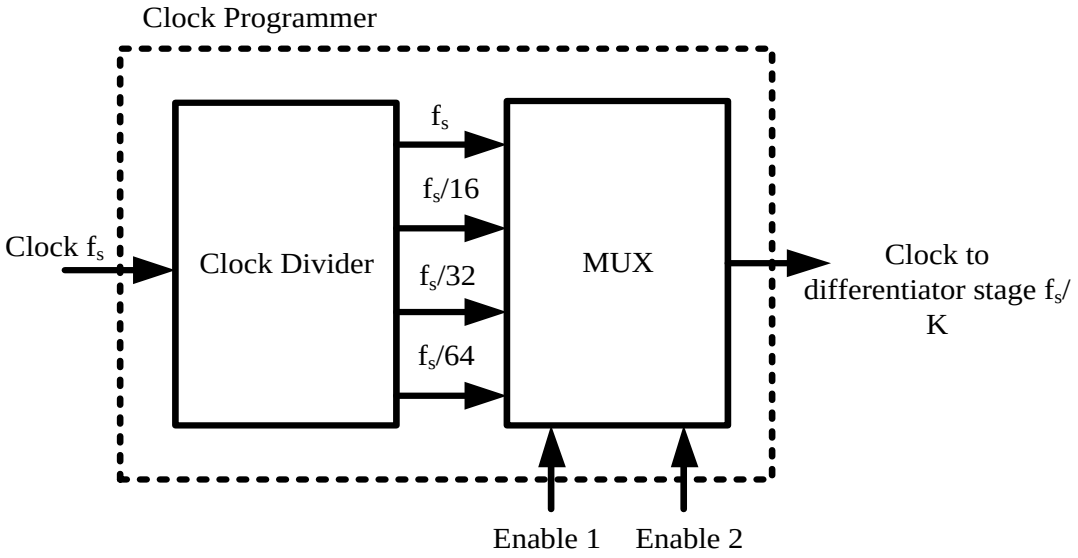



Figure 3.21. Block diagram of a clock programmer circuit for three different oversampling ratios (K = 64, 32 and 16) [23, 24, 25].

In Figures 3.20 and 3.21, when enable signals are set to low (Enable 1 is 0 and Enable 2 is 0), oversampling ratio, K = 64 is selected, and coder circuit-2 sign extends the bit 7 to provide bits 7 to 13 and passes bits 5 and 6 directly; coder circuit-3 sign extends bit 13 to provide bits 13 to 16 and passes bits 9 to 12 directly and the clock programmer circuit shown in Figure 3.21 selects $f_s/64$ (clock frequency/64). Similarly, when Enable-1 is set to low and Enable-2 is set to high, oversampling ratio, K= 32 is selected, and coder circuit-2 sign extends the bit 6 to provide bits 6 to 13 and passes bit 5 directly while disregarding bit 7; coder circuit-3 sign extends bit 11 to provide bits 11 to 19 and passes bits 9 and 10 while disregarding bits 12 and 13 and the clock programmer selects $f_s/32$ (clock frequency/32).

Similarly, in Figures 3.20 and 3.21 when Enable-1 is set to high and Enable-2 is set to low, oversampling ratio, K = 16 is selected, and coder circuit-2 sign extends the bit 5 to provide bits 5 to 13 and disregards bits 6 and 7; coder circuit-3 sign extends the bit 9 to provide bits 9 to 19 and disregards bits 10 to 13 and the clock programmer selects $f_s/16$ (clock frequency/16). Hence the coder circuit becomes necessary in between each integrator section to increase the 2's complement bit length by $\log_2 K$ and reuse the integrator section for three different oversampling ratios.

The output resolution of the second order delta-sigma ADC with an oversampling ratio K, is given by [9, 10],

$$N_{input} + N_{inc} \text{ where}$$

$$N_{input} = 1$$

and

$$N_{inc} = \left( \frac{50 \log K - 12.9}{6.02} \right) \tag{3.6}$$

In Eq. (3.6), $N_{input}$ is the 1-bit encoded output of the modulator and $N_{inc}$ is the increase in resolution in the decimator. Based on Eq. (3.6), the output of the second order sigma-delta modulator for K = 64 is 14 bits and is obtained by dropping the lower 5 bits in the 19 bit output. Similarly the output resolution for K = 32 and 16 are 12 bits and 9 bits, respectively. These are obtained by taking the lower 16 bits and dropping the lower 4 bits for K = 32, and taking the lower 13 bits and dropping lower 4 bits for K = 16, respectively. The output is then converted from 2's complement to binary offset format by complementing the MSB.

In this design, 1-bit modulator output is in the range of $V_{ref-}$ to $V_{ref+}$ (i.e., -2.5V to +2.5V) which requires a voltage level shifter at the input of the CIC decimator to convert the $V_{ref-}$ to $V_{ref+}$ range of the 1-bit modulator output to the 0 to 5V range for the decimator.

The design implementation of the third order programmable decimation filter for integration with the second order delta-sigma modulator designed and presented in the earlier section to form a complete delta-sigma ADC will be presented in detail. The hardware implementation was done using Tanner® LEDIT in 0.5µm n-well CMOS technology.

### 3.4.1 Level Shifter Circuit

As discussed earlier, a level shifter circuit is used to level shift the output voltage range of the modulator from -2.5V – +2.5V to 0 V – 5V. It's used to interface the second order delta-sigma modulator and the third order programmable CIC decimation filter. The designed second order delta-sigma modulator operates with a voltage range of ±2.5V for the purpose of biasing

the operational amplifier and proper functioning of the component circuits and setting the reference voltage to 0V. The third order programmable CIC decimation filter is a digital circuit and operates with a voltage range 0 to 5V. Due to the different voltage range, it becomes a need to have a circuit at the input stage of the decimation filter that can provide a voltage level shift to 0 to 5V. Figure 3.22 shows the transistor level schematic and Figure 3.23 shows the layout of the level shifter circuit.

The level shifter circuit is based on a simple buffer circuit, where the first inverter stage is modeled such that the output of the inverter is 0V when the input is +2.5V and the output is 5V when the input is -2.5V. The output from the first inverter stage is used as the input for the second inverter stage. Hence when the input to the level shifter circuit is 2.5V the output of the second inverter is 5V and when the input is -2.5V the output of the second inverter is 0V. The W/L ratios of the NMOS in the first inverter stage is increased as in the schematic, to avoid the internal node between the inverter stages in the buffer circuits been at an intermediate voltage value between 0V and 5V.

### 3.4.2 Clock Divider Circuit

In this work, the second order delta-sigma modulator and the third order CIC decimation filter are both operated at the same oversampling clock with a frequency $f_s$ but the differentiator in the decimation filter needs another clock signal of frequency $f_s/k$, where k is the oversampling ratio and is selected as 64, 32 and 16. Since the designed CIC decimation filter is programmable to work with three different oversampling ratios of 64, 32 and 16 as explained earlier, the clock divider circuit is designed to generated three different clock signals with frequencies $f_s/64$, $f_s/32$

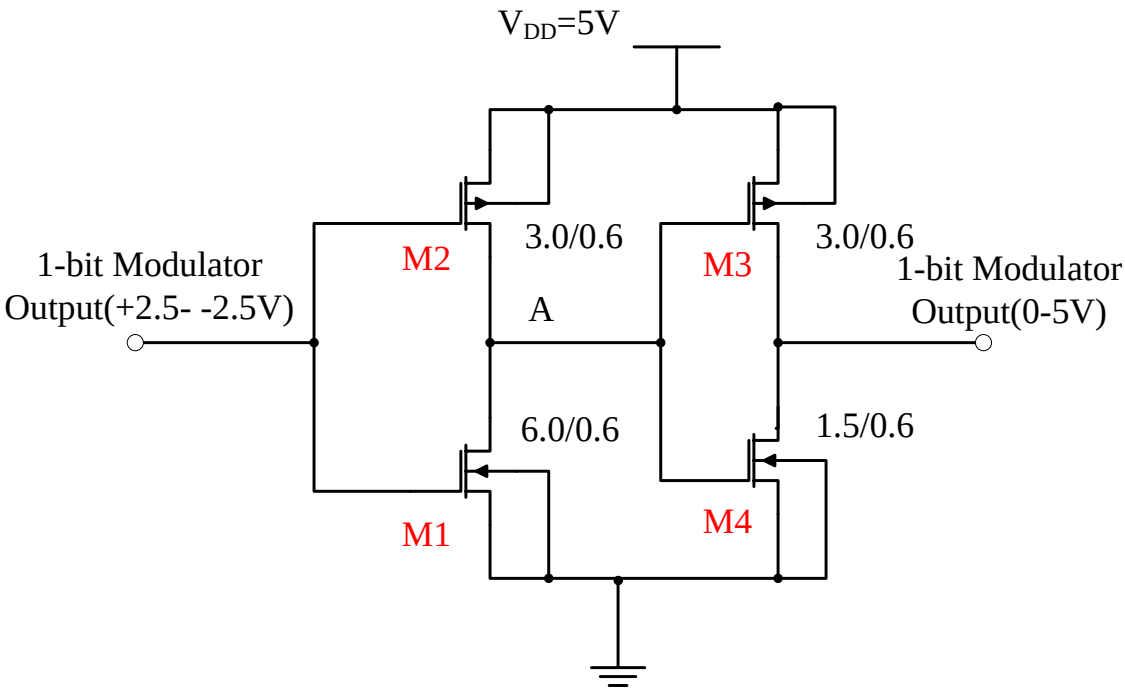



Figure 3.22. Transistor level schematic of level shifter circuit.

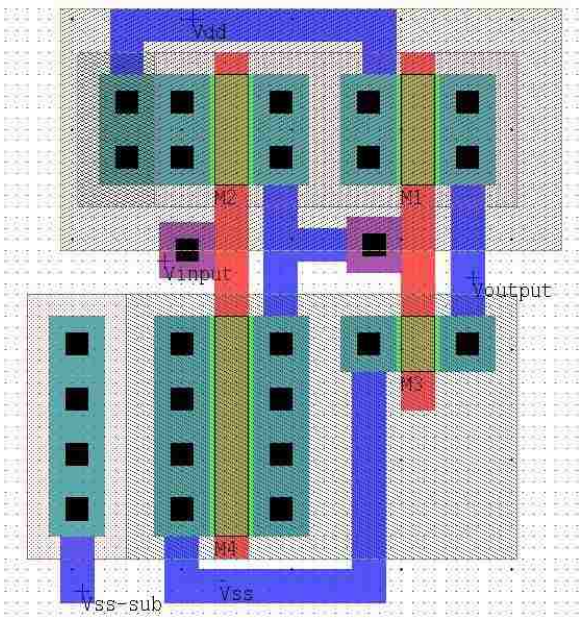



Figure 3.23. Layout of level shifter circuit.

and $f_s/16$. In clock divider circuit, the oversampling clock is used as the input and three different clock outputs are achieved. An MUX is used to select one clock out of the three clock output using two enable signals as discussed earlier. The clock divider circuit is implemented using negative edge triggered T-flip flop and AND gates and is a sequential circuit. A T-flip flop is a single input with clock being the input and single output and is designed using a D-flip flop. The output is also a clock signal with the frequency reduced by a factor of 2 from the input clock frequency.

In order to design an area efficient clock divider, a single circuit that provides three different clock signals for oversampling ratio K of 64, 32 and 16 is designed. Since the output of a single stage T-flip flop for a clock input of frequency of f is f/2, N number of cascaded design of T-flip flop will provide a frequency division $2^N$. The clock divider gate level schematic used to generate the three different clock pulses with a clock frequency of $f_s/64$, $f_s/32$ and $f_s/16$ is as shown in Figure 3.24. To implement an area efficient clock divider circuit, a single cascaded 6-stage T-flip flop design as shown in Figure 3.24 is designed. Whenever the input and output of a T-flip flop are given as inputs to an AND gate, only the ON time of the input clocks to the AND gate are transmitted and the output of the AND gate remains at logic '1' during that time. Based on the logic, the three different clocks with frequency of $f_s/64$, $f_s/32$ and $f_s/16$ are generated using the clock divider circuit. The layout of the complete clock divider circuit as discussed in this section has been designed using Tanner® LEDIT and is as shown in Figure 3.25. The simulated output of the clock divider circuit for K=64 is also shown in Figure 3.26.

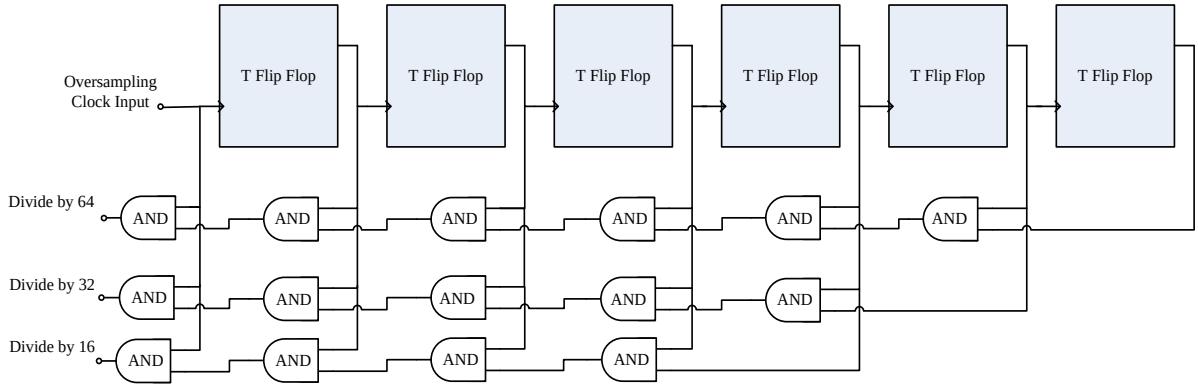



Figure 3.24. Clock divider gate level schematic used to generate the three different clock pulses.

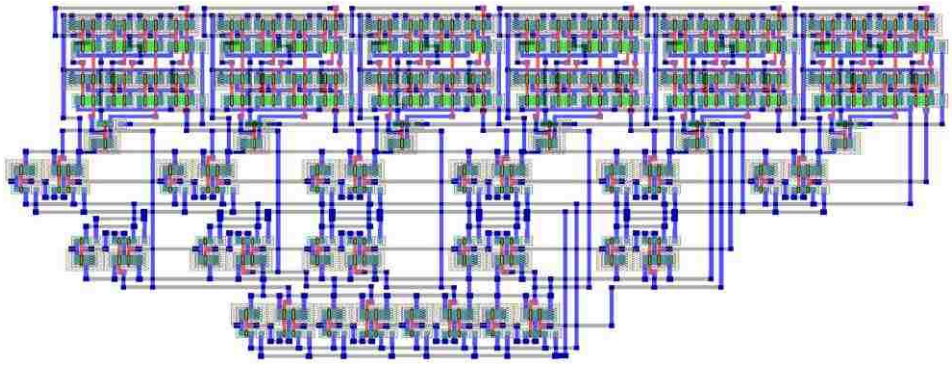


Figure 3.25. Layout of the complete clock divider circuit.

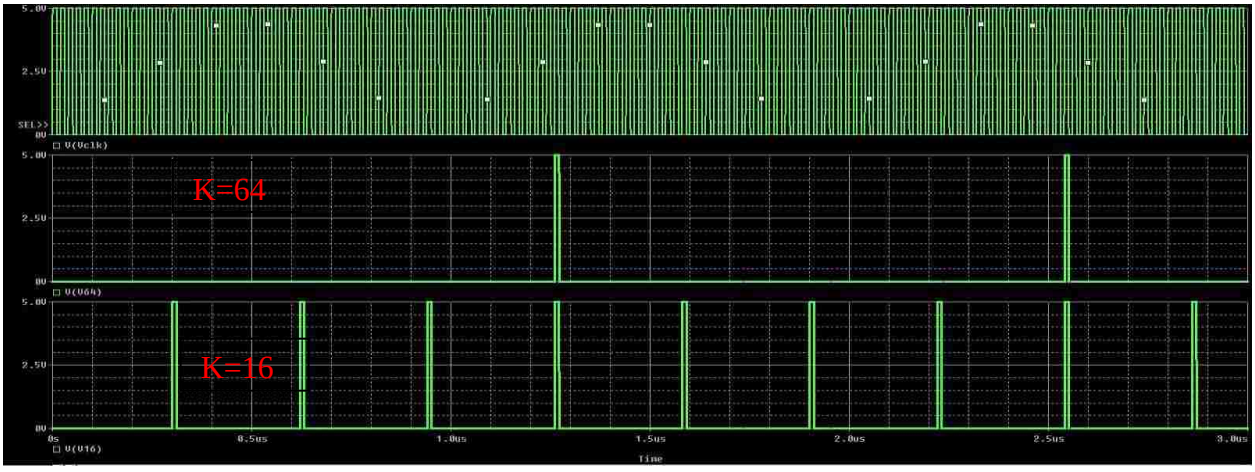



Figure 3.26. Simulated output of the clock divider circuit for K=64 and K=16.

### 3.4.3 Adder Circuit

In the design of the third order programmable CIC decimation filter, adder circuits are very crucial and are used in the design of digital integrator and digital differentiator to perform the addition and subtraction operation on the input bits as discussed in the earlier theory. In this work, a binary full adder circuit is designed and its truth table is as shown in Table 3.1. A and B are the two binary inputs, $C_{in}$ is the carry-in from earlier stage for the adder and the output of the adder are the sum bit and the carry bit $C_{out}$. The expression for Sum and $C_{out}$ for the binary full adder circuit is given by the Eq. (3.7) and is used in the truth table.

$$Sum = A \oplus B \oplus C_{in}$$

$$C_{out} = AB + AC_{in} + BC_{in} \tag{3.7}$$

Using the above equation and careful optimization, an area efficient design of the binary full adder is created with minimum number of transistors. A tradeoff between the area and speed of operation exists during optimization. The optimization is done both at the logic level and at the circuit level [22]. In this design, a binary full adder circuit is designed and optimized for area and uses the minimum number of transistors. Since the designed ADC operates at low frequencies, area of the adder circuit becomes the critical specification.

The binary full adder circuit designed for use in the CIC decimation filter uses transmission gates. The circuit schematic of the binary full adder circuit implemented is as shown in Figure 3.27. Transmission gates are used in the adder design because the design has minimum number of transistors. A total count of 18 transistors is used in the design of the adder [22]. Since the decimator uses adder circuit in every bit operation, optimizing the adder yields an

Table 3.1. Truth table of a binary full adder.

| A | B | $C_{in}$ | Sum | $C_{out}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

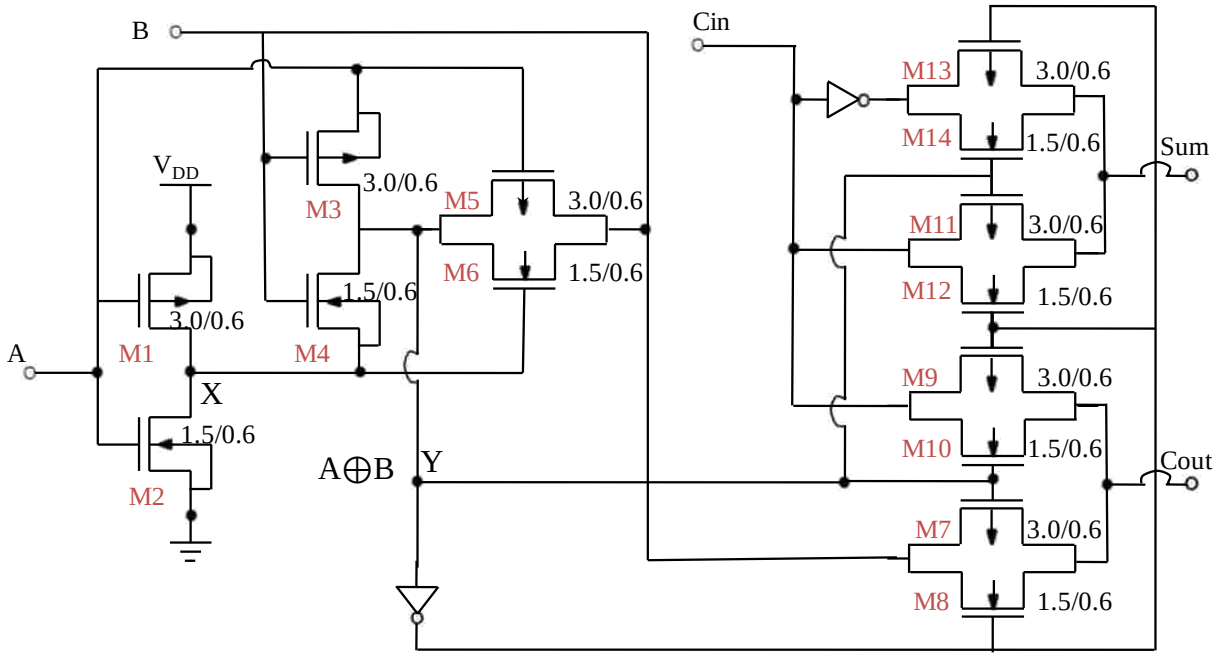



Figure 3.27. Schematic of the 18 transistor binary full adder circuit [22].

area efficient design. The sizing of the transistors in the design is shown in Figure 3.27. In the adder circuit, the transistor combination formed by transistors M1 through M6 performs the XOR operation taken at node Y. The operation of the XOR gate formed by using these six transistors is explained as follows. When signal A is high, node X is low disconnecting the transmission gate formed by transistors M5 and M6 and signal B appears at node Y as B. When signal A is low, node X is high disconnecting the inverter formed by transistors M3 and M4 and signal B appears at node Y.

The sum output of the binary full adder in Figure 3.27 is given by the XOR $((A \oplus B) \oplus C_{in})$ operation and is performed by transistors M11 through M14 where $C_{in}$ is the carry input. The carry output of the binary full adder, is equal to $C_{in}$ when node Y $(A \oplus B)$ is 1 and $C_{out}$ is either A or B when node Y $(A \oplus B)$ is 0 as shown in the truth table in Table 3.1. The designed binary full added uses the minimum number of transistor and has equal Sum and Carry delay times. The layout of the area optimized binary full adder circuit is shown in Figure 3.28. In the layout, the output carry bit $C_{out}$ of the adder is applied as the input carry $C_{in}$ of the next adder. The transition of all the three inputs to the next adder has to be applied at the same time to avoid glitches in the output. Hence in the layout the $C_{out}$ of the binary full adder is placed such that it is close to the $C_{in}$ of the next adder. As the decimator design requires large number of adders in the design as discussed earlier, it is very crucial to design the binary full adders with minimum delays. The simulation results of the 18 transistor binary full adder are shown in Figure 3.29.

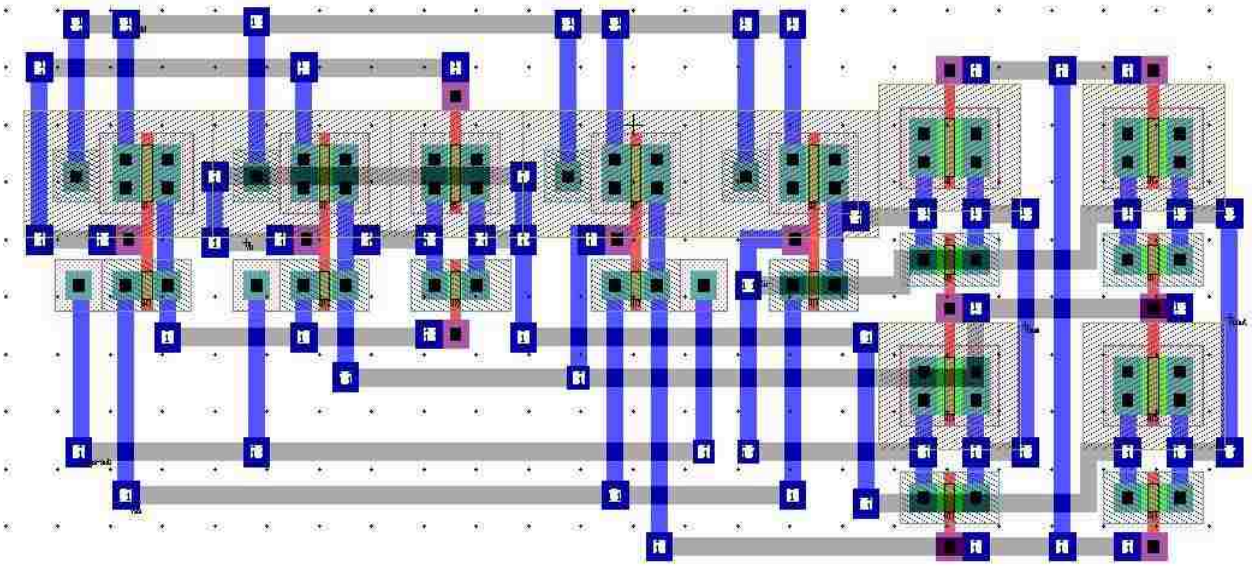


Figure 3.28. Layout of the area optimized 18 transistor binary full adder.

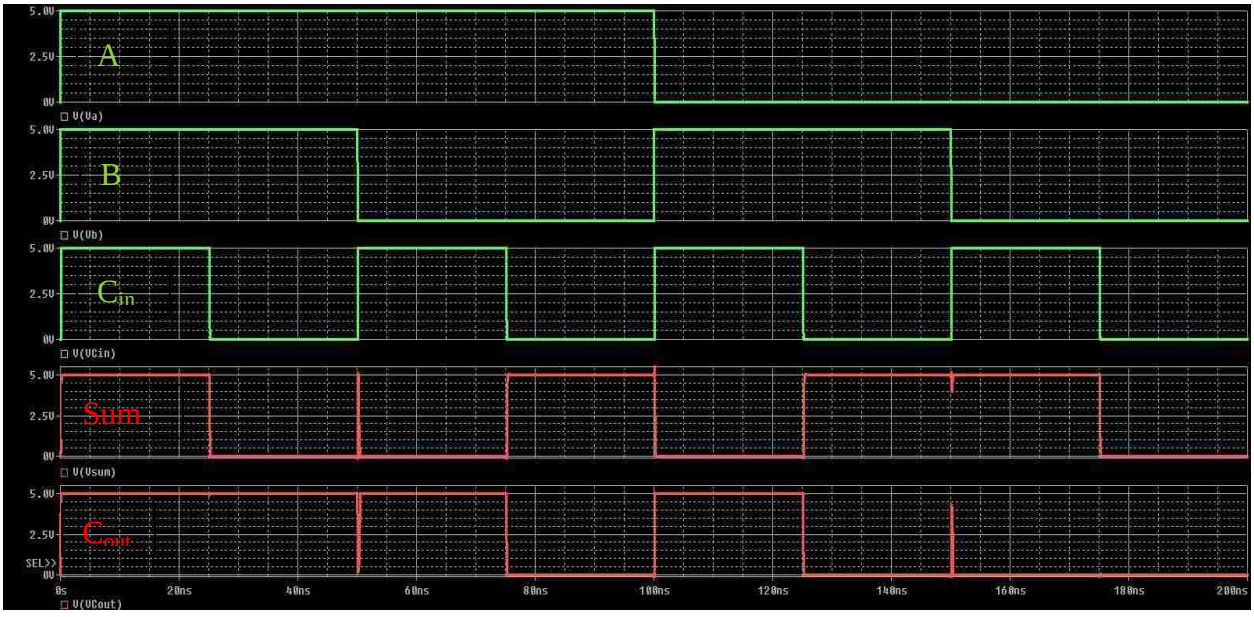



Figure 3.29. Simulation results for the 18 transistor binary full adder.

### 3.4.4 Delay Element

In the work, the delay element is designed using a register circuit to provide a delay of one clock period. The integrator and differentiator circuits in the CIC decimation filter requires delay circuits and hence it is important to design delay circuits which is area efficient and has smaller rise and fall time. The delay element in this design is implemented using a combination of switches and inverters. The circuit implementation of the delay circuit used to delay the input by an oversampling clock time period is shown in Figure 3.30. Simple NMOS switches are used for data transfer from left to right in alternate clock cycles of the oversampling clock. When clock signal is HIGH, switch S1 is closed and the inverted input is available at node A. Switch $S_2$ is operated with $\overline{clock}$ and is open and no transfer occurs through this switch. When the clock transitions to LOW, switch $S_1$ is opened and the input is disconnected from the delay circuit. Now when clock transition to HIGH, switch S2 is closed and the previous inverted input stored on the node A is inverted and transferred towards the node B. During the next cycle when clock transitions to HIGH, the value stored on node B is transferred to the output and fed to the stages following the delay element. From the above explanation, it is observed that an input bit takes one clock cycle to reach to the output. Hence the delay element works fine in providing a delay by one clock period. The time delay is achieved by data transfer using two non-overlapping clock signals. But in practice, the two non-overlapping clocks exhibit clock skew, if the clock skew is large then the delay circuit does not work as delay element. To avoid this condition an NMOS switch based design is used here instead of a transmission gate based design. Since the transmission gates requires two non-overlapping clocks to work as a switch, the presence of

clock skew can degrade the signal. Hence by using the NMOS as switches, non-overlapping clocks can be applied to two different switches and the problem of clock skew is neutralized with the delay of the inverters. Also, this delay design has better driving capability in driving the loads connected to the circuits. The delay element layout is shown in Figure 3.31. The simulated output of the delay element is as shown in Figure 3.32.

### 3.4.5 Digital Integrator Block Design

In the $3^{rd}$ order CIC decimation filter, as discussed earlier, a $3^{rd}$ order integrator is used. The integrator is the most important circuit in the design and for achieving increase in resolution. The schematic block diagram of the $3^{rd}$ order integrator circuit is as shown in Figure 3.33. The integrator cells in the $3^{rd}$ order integrator schematic design are clocked by an oversampling clock of frequency $f_s$. The pipelined 1-bit integrator contains an adder and a delay element as discussed earlier. The oversampling clock is used in the delay element to provide a delay in the adder output by one clock period. The output of the delay element is also used as one of the input to the adder circuit. The output of the coder circuit is given as the other input to the adder, and the carry out $C_{out}$ of the preceding significant bit adder is used as Carry in $C_{in}$. The carry input for the least significant bit adder is taken as 0 and the carry out for the most significant bit adder is ignored.

In the $3^{rd}$ order CIC decimation filter, the resolution of each integrator stage increases by $\log_2 K$ as discussed earlier in the chapter. The $3^{rd}$ order integrator block is designed to work for three different oversampling ratios of 16, 32 and 64. For, K = 64, the output of integrator section-1 has a maximum 7-bits resolution, the output of integrator Section-2 has a maximum 13 bits resolution and the output of integrator Section-3 has a maximum resolution of 19 bits [9,20] as

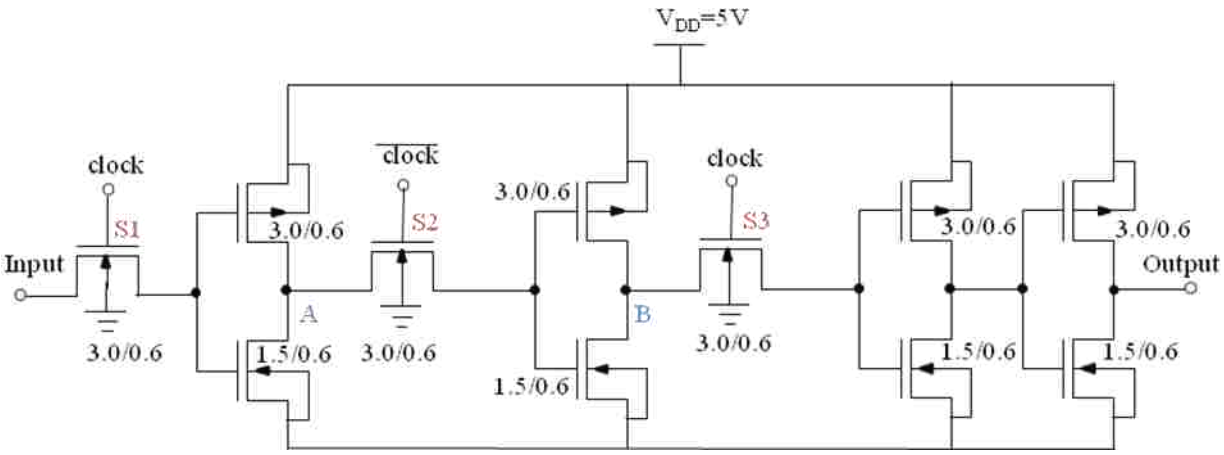



Figure 3.30. Schematic diagram to design delay element.

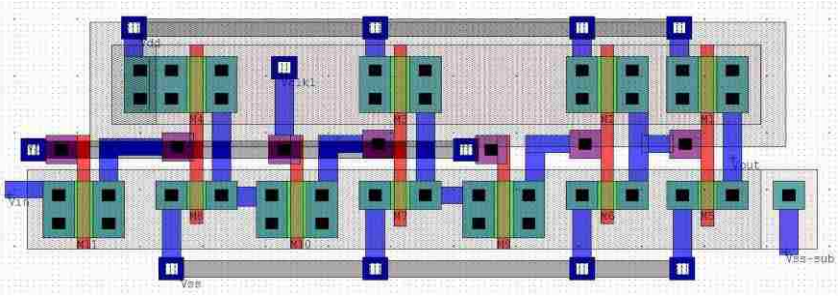


Figure 3.31. Layout of delay element design for achieving delay by two clock cycles.

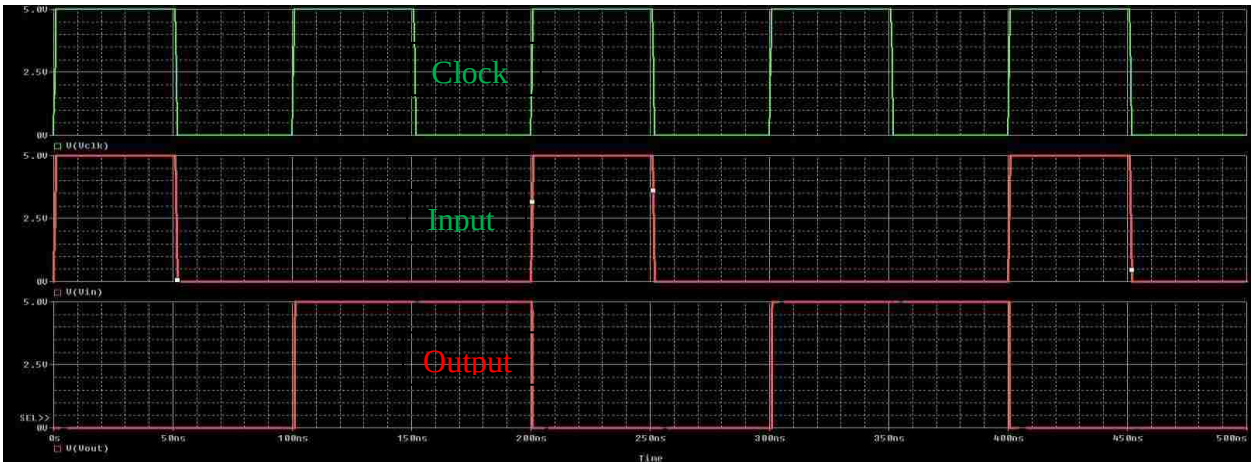



Figure 3.32. Simulated input and output of the delay element.

discussed earlier. Similarly, the output resolution of each integrator section is 6, 11 and 16 bits for oversampling ratio K = 32, and 5, 9 and 13 bits for oversampling ratio K = 16. By using additional circuit for programmability and coder circuits, the same integrator sections are reused for the three oversampling ratios.

#### 3.4.5.1 Coder Circuits

In the 3rd order integrator block schematic, three coder circuits are used to adjust the resolution of the integrator stages. The coder circuits are also used to convert the binary form into two's complement representation. The data loss due to register overflow is avoided by using the two's complement method of coding as explained earlier. The coder circuit-1 is used to convert the 1-bit output of the 2nd order delta-sigma modulator explained earlier to two's complement 7-bit data. The 1-bit modulated output from the modulator is either 1 or 0 and the output of the coder circuit-1 is 7-bit for K=64, 6-bit for K=32 and 5-bit for K=16. The gate level schematic of the coder circuit-1 is as shown in Figure 3.34 (a). Coder circuit-2 and coder circuit-3 are used by the second and third integrator stage to sign extend the two's complement for achieving the required bit growth for the integrator stages as shown in Figure 3.34 (b). The outputs of the three coder circuits are tabulated as shown in Table 3.2.

#### 3.4.5.2 Circuit for Programmability

In this work, the CIC decimation filter has been designed to work for three different oversampling ratios of 16, 32 and 64 to give three different outputs of resolutions of 9, 12 and 14 bits, respectively. The circuits for programmability in this work uses enable signals (Enable-1 and Enable-2) and interfaced with the coder circuit-2, coder circuit-3 and clock divider circuit.

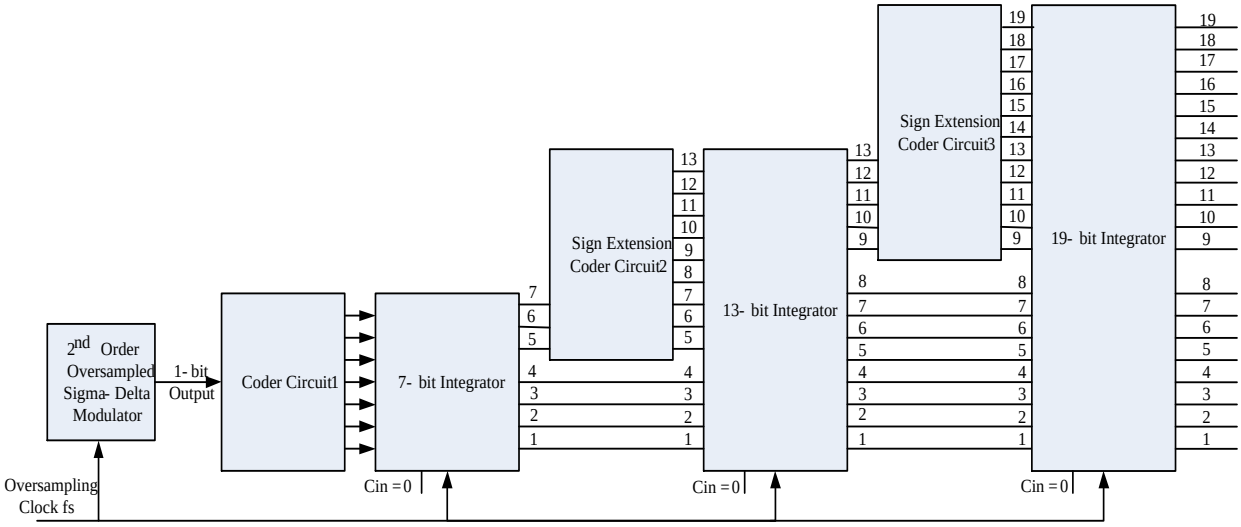



Figure 3.33. Block diagram of third order integrator circuit.

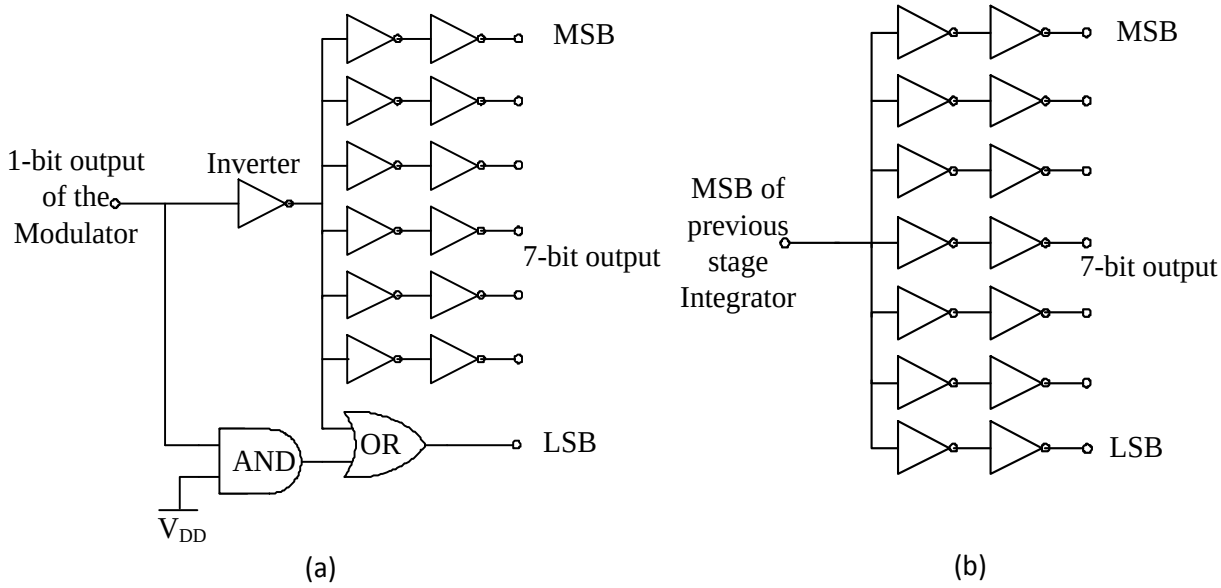



Figure 3.34. (a) Gate level schematic of coder circuit-1. (b) Gate level schematic of coder circuit-2 and coder circuit-3.

As discussed earlier, for K=64 the MSB of the 7-bit output of the first stage integrator is sign extended by the coder circuit-2 and extended to form a 13-bit data so that the second stage integrator can work with 13-bits of data. For K=32, the second stage integrator should work with 11-bit data and only the lower 6-bits of the first stage integrator output should be considered. The 6-bits from the first integrator stage is sign extended to 11-bit two's complement data by passing the lower 5-bits and sign extending the $6^{th}$ bit output of the first stage integrator and substituting it from $6^{th}$ bit to the $11^{th}$ bit. Also, for K=16 the second stage integrator should work with 9-bit data and only the first 5-bits of the first stage integrator output should be considered. For K = 16 case, the 5-bits from the first stage integrator are to be extended to 9-bits two's complement data and to do this the $5^{th}$ bit output of the first stage integrator has to be sign extended and substituted from $5^{th}$ bit to the $9^{th}$ bit.

Similarly, for K=64 the MSB of the 13-bit output of the second stage integrator is sign extended by the coder circuit-3 and extended to form a 19-bit data so that the third stage integrator can work with 19-bits of data. For K=32, the third stage integrator should work with 16-bit data and only the lower 11-bits of the second stage integrator output should be considered. The 11-bits from the second integrator stage is sign extended to 16-bit two's complement data by passing the lower 10-bits and sign extending the $11^{th}$ bit output of the second stage integrator and substituting it from $11^{th}$ bit to the $16^{th}$ bit. Also for K=16, the third stage integrator should work with 13-bit data and only the first 9-bits of the second stage integrator output should be considered. For K = 16 case, the 9-bits from the first stage integrator are to be extended to 13-bits two's complement data and to do this the $9^{th}$ bit output of the first stage integrator has to be

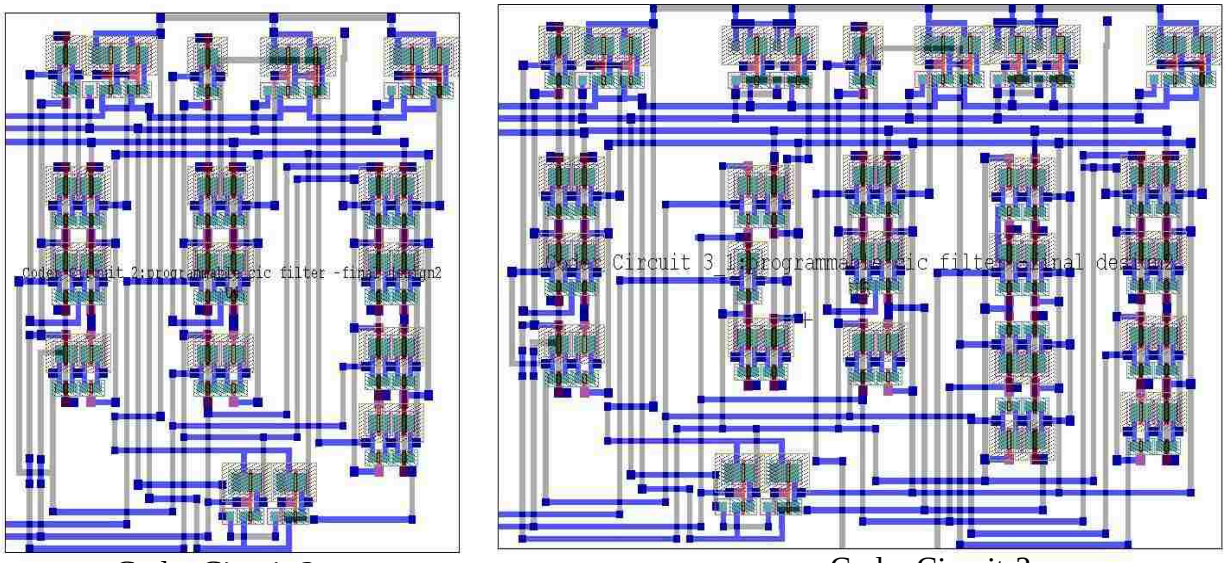
sign extended and substituted from $9^{th}$ bit to the $13^{th}$ bit. Hence, to reuse the same integrator stage in the CIC decimation filter for the three oversampling ratios of 64, 32 and 16, a circuit has to be designed which can program bit 5 to bit 13. The circuit for programmability is designed using MUX circuit controlled by Enable-1 and Enable-2. When enable signals are set to low (Enable-1 is 0 and Enable-2 is 0), oversampling ratio, K = 64 is selected, and coder circuit-2 sign extends the bit 7 to provide bits 7 to 13 and passes bits 5 and 6 directly; coder circuit-3 sign extends bit 13 to provide bits 13 to 16 and passes bits 9 to 12 directly and the clock programmer circuit shown in Figure 3.21 selects $f_s/64$ (clock frequency/64). Similarly, when Enable-1 is set to low and Enable-2 is set to high, oversampling ratio, K = 32 is selected, and coder circuit-2 sign extends the bit 6 to provide bits 6 to 13 and passes bit 5 directly while disregarding bit 7; coder circuit-3 sign extends bit 11 to provide bits 11 to 19 and passes bits 9 and 10 while disregarding bits 12 and 13 and the clock programmer selects $f_s/32$ (clock frequency/32).

Similarly, when Enable-1 is set to high and Enable-2 is set to low, oversampling ratio, K=16 is selected, and coder circuit-2 sign extends the bit 5 to provide bits 5 to 13 and disregards bits 6 and 7; coder circuit-3 sign extends the bit 9 to provide bits 9 to 19 and disregards bits 10 to 13 and the clock programmer selects $f_s/16$ (clock frequency/16). The circuit for programmability is designed using MUX and is interfaced with the coder circuits and the layout for the circuit for programmability with the coder circuits are shown in Figure 3.35.

The layout of the complete $3^{rd}$ order integrator circuit is shown in Figure 3.36. The layout contains three integrator stages, three coder circuits, circuit for programmability and the level shifter circuit.

Table 3.2. Table representation of input and output values of the designed coder circuits.

| | Coder Circuit-1 | | Coder Circuit -2 / Coder Circuit-3 | |
|---|---|---|---|---|
| | Input | Output | Input | Output |
| **For K = 64** | 1 | 0000001 | 1 | 1111111 |
| | 0 | 1111111 | 0 | 0000000 |
| **For K = 32** | 1 | 000001 | 1 | 111111 |
| | 0 | 111111 | 0 | 000000 |
| **For K = 16** | 1 | 00001 | 1 | 11111 |
| | 0 | 11111 | 0 | 00000 |



Coder Circuit-2 Coder Circuit-3

Figure 3.35. Layout of the circuit for programmability used with coder circuit -2 and coder circuit -3.

Figure 3.36. Layout of the complete 3rd order integrator.

### 3.4.6 Differentiator Block Design

The digital differentiator circuit (comb filter) acts as a low pass filter as discussed earlier. The 19-bit output of the integrator is applied to the input of the differentiator. The differentiator circuit is clocked by a clock whose frequency is 1/K times the oversampling clock frequency. The block diagram of the digital differentiator circuit is shown in Figure 3.37 and the complete layout is as shown in Figure 3.38. The circuit shown is of $3^{rd}$ order and has three fixed 19-bit differentiator stages. A simple 1-bit differentiator circuit is explained earlier in the chapter. The differentiator circuit is used to calculate the difference between the one 1-bit and the other input bit delayed by $KT_s$, where $T_s$ is the time period of the oversampling clock. In two's complement, the difference operation of two inputs is done by the summation of the first input with the complement of the second input. In hardware, the second input is delayed by a time $KT_s$ compared with the original input, complemented using an inverter circuit. The carry input $C_{in}$ to the adder circuit is set at 1 (logic HIGH). In the differentiator circuit, at the beginning of the CIC decimation filter circuit there is no meaningful output for three cycles of $KT_s$. The first differentiator stage has a valid output only after $KT_s$ because the delay element delays the input by $KT_s$. Similarly the second and third differentiator stages also require $KT_s$ to have a valid output. Hence in the differentiator, the output should be considered after three cycles of $KT_s$ has elapsed. The differentiator uses two's complement and output is a 19-bit data. The data are converted to binary form and also the least significant bits can be dropped in order to achieve the required resolution as discussed earlier.

Hence as explained, for K=64 the final resolution is 14 bits and is obtained by dropping the lower 5 bits in the 19 bit output. Similarly the output resolution for K = 32 and 16 are 12 bits and 9 bits, respectively. These are obtained by taking the lower 16 bits and dropping the lower 4 bits for K = 32, and taking the lower 13 bits and dropping lower 4 bits for K = 16, respectively. The output is then converted from 2's complement to binary offset format by complementing the MSB.

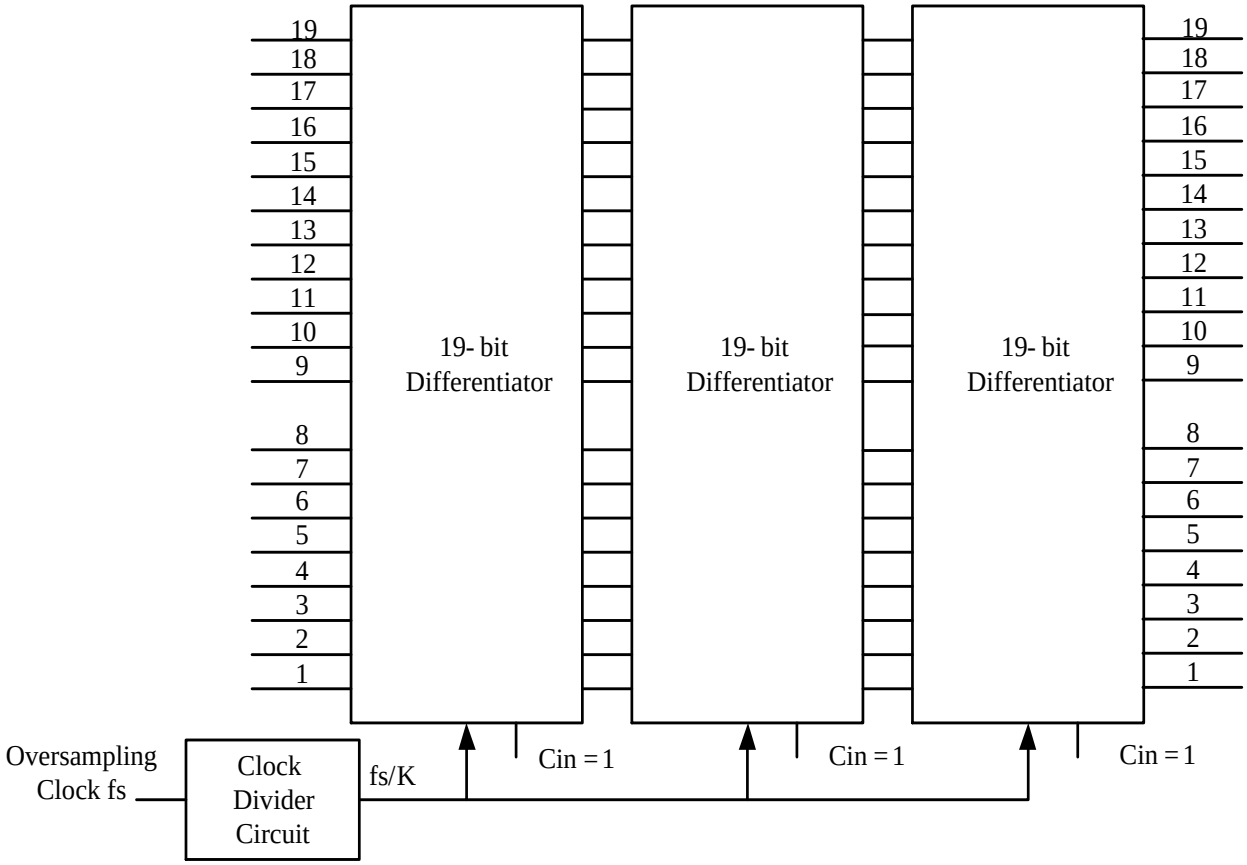



Figure 3.37. Block diagram of the complete 3rd order differentiator.

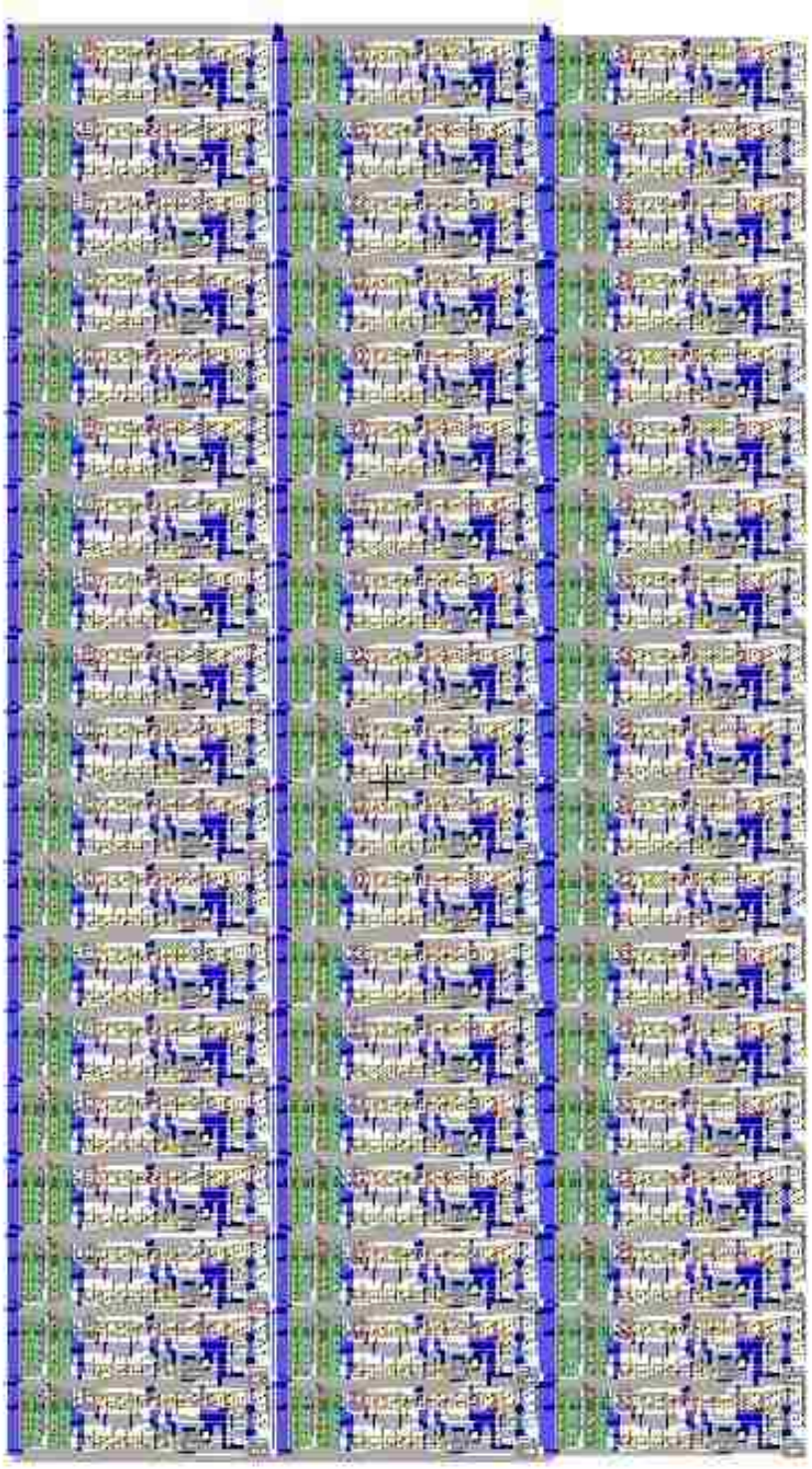


Figure 3.38. Layout of the complete 3rd order differentiator.

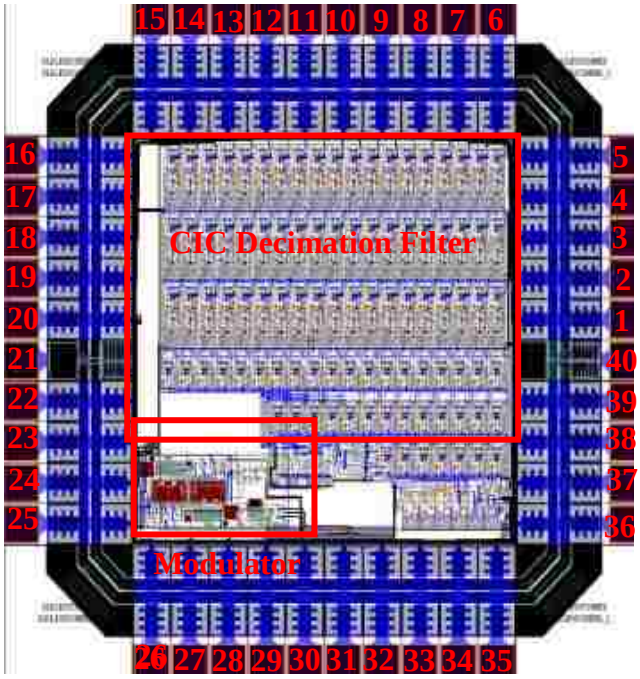
## 3.5 Results and Discussion

The second order delta-sigma modulator and the third order CIC decimator are designed and fabricated in 0.5µm n-well CMOS process and tested. The layout and the microphotograph of the fabricated chip in 40 pin padframe are shown in Figure 3.39.

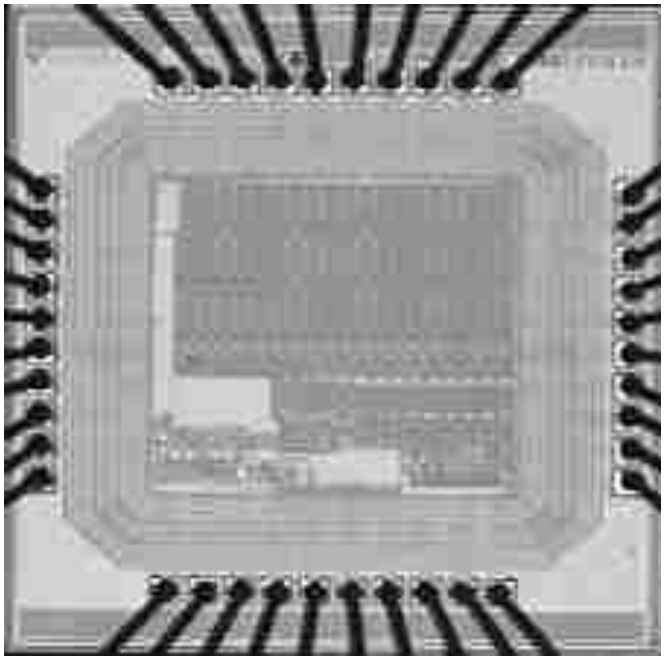
The experimental test setup for the complete programmable second order oversampling delta-sigma ADC is shown in Figure 3.40. The modulator and decimator used in the experimental setup are two integrated circuits from the same design fabricated in 0.5µm n-well CMOS and the output of the modulator is fed as the input of the CIC decimation filter. The input to delta-sigma modulator is an analog signal and is fed from the function generator. The programmable decimation CIC filter can deliver three different output resolutions of 14, 12 and 9 which are observed through a logic analyzer. The modulator and CIC decimator are clocked by an oversampling clock and are supplied externally using a clock generator.

### 3.5.1 Second Order Delta-Sigma Modulator

The second order delta-sigma modulator is first tested with a 1 kHz, 4Vpp input sinusoidal signal and 2 kHz bandwidth. A DC power supply of +2.5V and -2.5V are given from a power supply. The Nyquist frequency is equal to the twice that of the bandwidth, i.e., 4 kHz and the oversampling clock frequency is given by the product of the oversampling ratio K and the Nyquist frequency. For experimental simulation, the oversampling clock frequency is 256 kHz. The output is analyzed through an oscilloscope and the measured 1-bit modulated digital output of the fabricated modulator is shown in Figure 3.41. In 1-bit modulated digital output of the modulator, during the positive half of the input sine wave signal, there are more 1’s and




(a)



(b)

Figure 3.39. (a) Chip layout in 40-pin padframe and (b) microphotograph of a second order delta-sigma ADC [23, 24, 25].

during the negative half there are more 0's and hence meets the required specification. This 1-bit modulated digital output from the modulator is used as the input for the third order CIC decimation filter.

To further analyze the second order delta-sigma modulator output, an FFT is performed on the 1-bit modulated output signal to obtain the frequency spectrum of the signal as shown in Figure 3.42. Using the frequency spectrum, it can be experimentally found that second order noise shaping in the delta-sigma modulator occurs with a measured SNR (signal-to-noise ratio) of 75.6dB at oversampling ratio of 64, 62.3dB at oversampling ratio of 32 and 45.3dB at oversampling ratio of 16. The SNR for the 3 different oversampling ratios of 64, 32 and 16 were also simulated for comparing with the measured experimental SNR and is plotted as shown in Figure 3.43. The close agreement between the simulated and measured experimental SNR is obtained.

The input dynamic range (DR) of the modulator is found to be approximately 70dB for oversampling ratio of 64, 58dB for oversampling ratio of 32 and 45dB for oversampling ratio of 16 from the Figure 3.43. The Spurious Free Dynamic Range (SFDR) and Signal-to-Noise Distortion Ratio (SNDR) are also measured from frequency spectrum to be approximately 72.3dB and 71dB at oversampling ratio of 64, 57dB and 55.5dB at oversampling ratio of 32 and 41.6dB and 40.4dB at oversampling ratio of 16.

### 3.5.2 Second Order Delta-Sigma ADC

As shown in the experimental setup of Figure 3.40, the second order delta-sigma modulator output is applied to the integrator stage of the third order CIC decimation filter

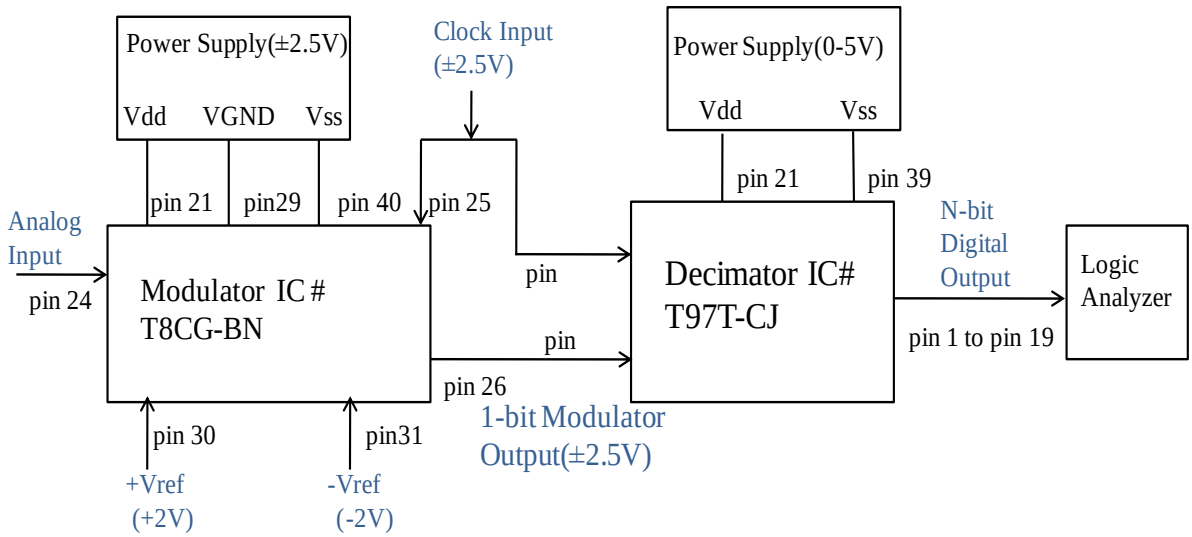



Figure 3.40. Experimental setup to test programmable second order oversampling delta-sigma ADC.

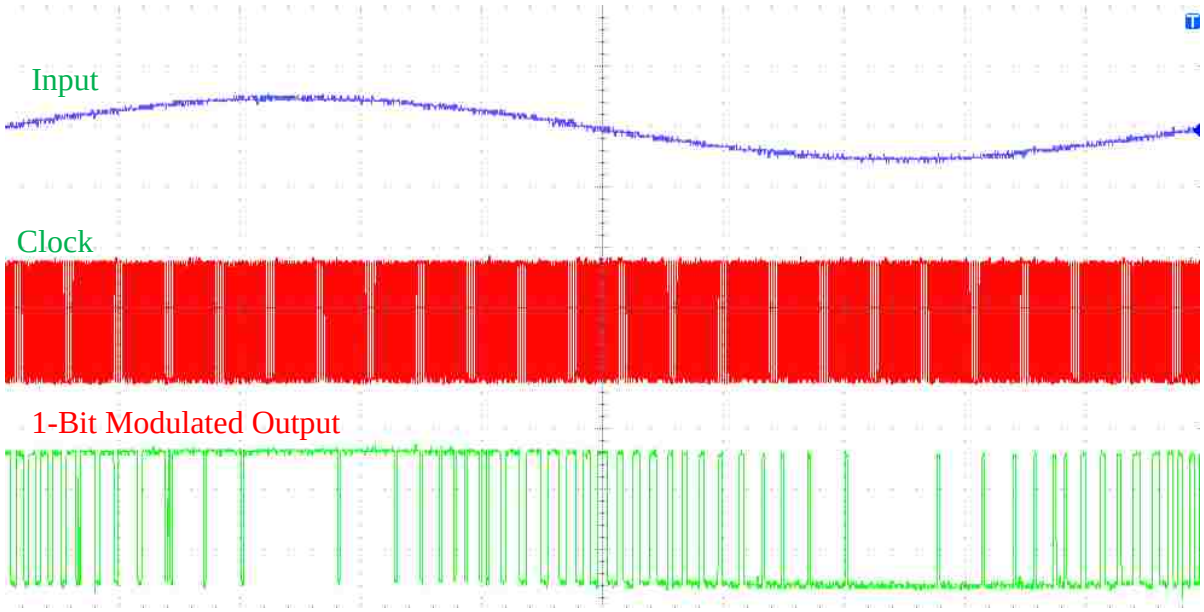



Figure 3.41. Experimental results for second order delta-sigma modulator chip showing 1-bit modulated digital output.

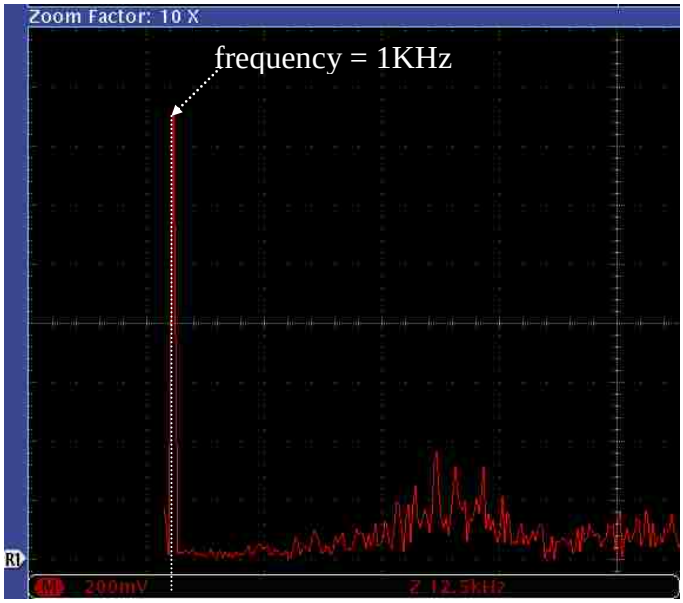



Figure 3.42. Frequency spectrum of 1-bit modulated output in Figure 3.41 using FFT.

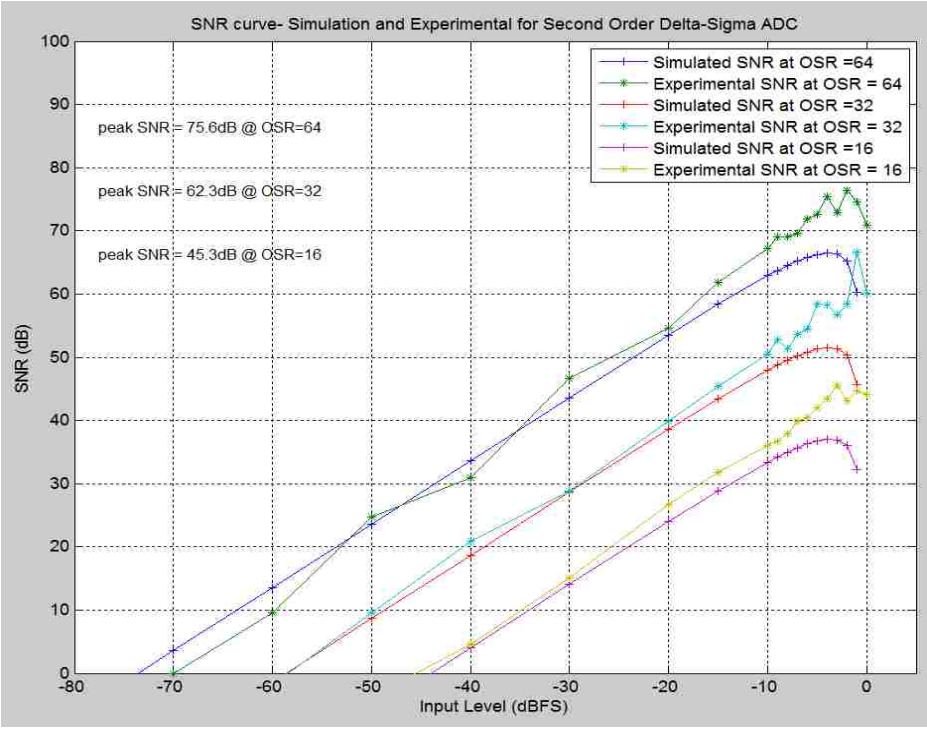



Figure 3.43. Plot of output SNR vs. Input Range showing a dynamic range for OSR = 64, 32 and 16.

through a level shifter to boost the resolution from 1-bit to higher resolution of 14, 12 and 9 bits for K= 64, 32 and 16, respectively. The output of programmable CIC decimation filter is an N-bit binary data occurring at twice the input signal bandwidth. In the second order delta-sigma ADC, LSB is given by the equation [9],

$$1LSB = \left( \frac{V_{FSR}}{2^N} \right) = \left( \frac{V_{ref+} - V_{ref-}}{2^N} \right) = V_{LSB} \tag{3.8}$$

where $V_{FSR}$ is the full scale range of the modulator and N is the number of bits in the output. In testing the design, $V_{FSR}$ of $4V_{pp}$ is chosen. For example, when K = 64, the number of bits, N = 14 and hence 1 LSB = 0.244mV. Similarly for K = 32 and 16, 1 LSB = 0.9766mV and 7.81mV, respectively. In the experimental testing for the oversampling ratio K = 64, the Nyquist rate is 4 kHz, the sampling clock of frequency 256 kHz (K x Nyquist rate) is used. Similarly for oversampling ratios 32 and 16, respectively sampling clock frequency 128 kHz and 64 kHz are used. Hence data samples occur at the output at a rate of 4 kHz. Also since the input frequency is 1 kHz and $V_{FSR}$ is $4V_{pp}$, difference between the consecutive samples is approximately 2V.

3.5.2.1 K = 64 Case

The oversampling clock of frequency 256 KHz is applied to both the modulator and the CIC decimation filter. The enable signals are set to low (Enable 1 is 0 and Enable 2 is 0), so that oversampling ratio, K = 64 is selected. As explained earlier in this chapter, the output resolution of the second order programmable oversampling delta-sigma ADC for K = 64 is 14-bits. The experimental results for K = 64 is as shown in Table 3.3 and shows the 14-bit recorded output, equivalent binary offset, its decimal equivalent, analog equivalent and the actual analog voltage.

In the Table 3.3, the first two output samples are 10011110100101 and 00101000000011 and are read in the order they are written with the MSB being the left most bit and LSB being the right most bit. They are converted to the binary offset by inverting the MSB of the recorded from the logic analyzer in experimental setup. The decimal equivalent is then calculated by multiplying the bit coefficient with the respective powers of 2. From the calculated decimal equivalent the analog equivalent can be calculated by multiplying the decimal equivalent with the value of 1LSB. For the above recorded output, the calculated analog equivalents are 0.477783203 and 2.625732422, respectively. The calculated analog equivalents represent the voltage range from 0 to 4V. Hence to represent the actual analog input voltage which ranges from -2V to +2V a drop of 2V in the value of analog equivalent is done as shown in the last column of the Table 3.3.

The logic analyzer experimental output results for the above recorded output are shown in Figure 3.44.We have also shown a set of 4 readings for oversampling ratio K=64, with a sine wave of 4Vpp superimposed on the actual analog voltage recorded as shown in Figure 3.45. The logic analyzer output lab0 represents the output of the clock divider circuit and lab1 to lab15 represent the 14-bit digital output for K = 64. The output of the decimator exists only at the output of the clock divider circuit and since the clock divider circuit has an output at the Nyquist frequency, the decimator output is also at Nyquist frequency.

3.5.2.2 K = 32 Case

The output of the programmable second order oversampling delta-sigma ADC for K = 32 has an output resolution of 12 as explained earlier. The experimental results for K = 32 are represented in Table 3.4. As in K = 64, the table has been divided into columns representing the

Table 3.3. Experimental output of a programmable second order oversampling CMOS delta-sigma ADC for K = 64.

| **Recorded Output** | **Binary Offset Equivalent** | **Decimal Equivalent** | **Analog Equivalent Voltage (Volt) [A]** | **Actual Analog Voltage (Volt) [A-2]** |
|---|---|---|---|---|
| 10011110100101 | 00011110100101 | 1957 | 0.477783203 | -1.522216797 |
| 00101000000011 | 10101000000011 | 10755 | 2.625732422 | 0.625732422 |
| | | | | |
| 01001101110111 | 11001101110111 | 13175 | 3.216552734 | 1.216552734 |
| 11001011000101 | 01001011000101 | 4805 | 1.173095703 | -0.826904297 |
| | | | | |
| 00100000100100 | 10100000100100 | 10276 | 2.508789063 | 0.508789063 |
| 01011110110111 | 11011110110111 | 14263 | 3.482177734 | 1.482177734 |
| | | | | |
| 01010010100011 | 11010010100011 | 13475 | 3.289794922 | 1.289794922 |
| 01001000100101 | 01001000100101 | 4645 | 1.134033203 | -0.865966797 |
| | | | | |
| 10001010010111 | 00001010010111 | 663 | 0.161865234 | -1.838134766 |
| 00001011101110 | 10001011101110 | 8942 | 2.183105469 | 0.183105469 |

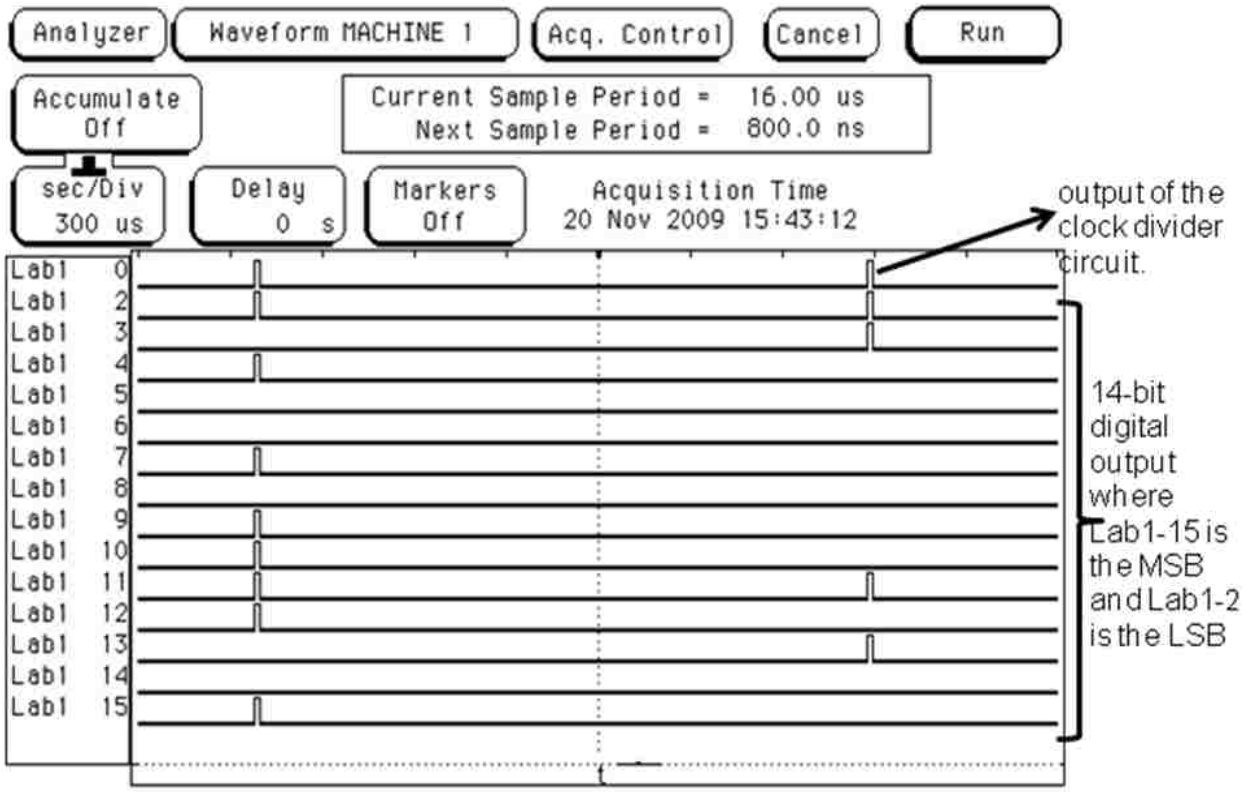



Figure 3.44. Experimental results showing the waveforms for two digital output codes 10011110100101 and 00101000000011.

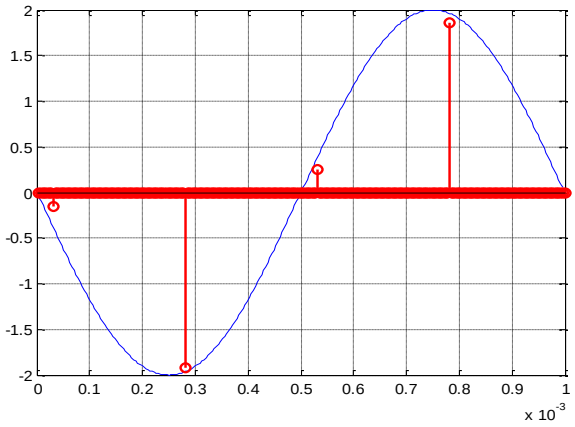



Figure 3.45. Experimental output of the programmable second order CMOS delta-sigma ADC for oversampling ratio K = 64 with a superimposed sine wave of 4Vpp.

Table 3.4. Experimental output of a programmable second order oversampling CMOS delta-sigma ADC for K =32.

| **Recorded Output** | **Binary Offset Equivalent** | **Decimal Equivalent** | **Analog Equivalent Voltage(Volt) [A]** | **Actual Analog Voltage(Volt) [A-2]** |
|---|---|---|---|---|
| 011011010000 | 111011010000 | 3792 | 3.703125 | 1.703125 |
| 000101010000 | 100101010000 | 2384 | 2.328125 | 0.328125 |
| | | | | |
| 101111110110 | 001111110110 | 1014 | 0.990234375 | -1.009765625 |
| 001110101110 | 101110101110 | 2990 | 2.919921875 | 0.919921875 |
| | | | | |
| 110010110111 | 010010110111 | 1207 | 1.178710938 | -0.821289063 |
| 010010111001 | 110010111001 | 3257 | 3.180664063 | 1.180664063 |
| | | | | |
| | | | | |
| 000110101010 | 100110101010 | 2474 | 2.416015625 | 0.416015625 |
| 011001000000 | 111001000000 | 3648 | 3.5625 | 1.5625 |
| | | | | |
| 001010000001 | 101010000001 | 2689 | 2.625976563 | 0.625976563 |
| 101001011101 | 001001011101 | 605 | 0.590820313 | -1.409179688 |

recorded output, equivalent binary offset code, its decimal equivalent, analog equivalent voltage and the actual analog voltage. As explained in K = 64 case, the actual analog voltage is calculated.

3.5.2.3 K = 16 Case

The output of the programmable second order oversampling delta-sigma ADC for K = 16 has a resolution of 9 and is shown in Table 3.5. The table represents the recorder output, equivalent binary offset code, its decimal equivalent, analog equivalent voltage and the actual analog voltage.

## 3.6 Conclusion

In this chapter, design of programmable oversampling $2^{nd}$ order delta-sigma ADC's in 0.5µm n-well CMOS process is presented for use in low-power sensor interface electronics in wireless sensor networks. The $2^{nd}$ order delta-sigma ADC consist of the modulator designed using two switched capacitor discrete time integrator and a latched comparator in the forward path and a 1-bit DAC in the feedback path. The decimation filter is designed using a programmable CIC filter which uses sign extension two's complement coder to take advantage of the low power consumption and is based on the earlier work. The fabricated $2^{nd}$ order oversampled delta-sigma ADC can be programmed to work at three different oversampling ratios, 64, 32 and 16 with output resolution of 14, 12 and 9 bits, respectively. The programmability feature can be effectively and efficiently used and taken advantage in sensor module of the sensor node to create energy efficient and low-power interface electronics for varied sensor applications.

Table 3.5. Experimental output of a programmable second order oversampling CMOS delta-sigma ADC for K =16.

| **Recorded Output** | **Binary Offset Equivalent** | **Decimal Equivalent** | **Analog Equivalent Voltage (Volt) [A]** | **Actual Analog Voltage(Volt) [A-2]** |
|---|---|---|---|---|
| 111110101 | 011110101 | 245 | 1.9140625 | -0.0859375 |
| 100001010 | 000001010 | 10 | 0.078125 | -1.921875 |
| | | | | |
| 000100101 | 100100101 | 293 | 2.2890625 | 0.2890625 |
| 011011100 | 111011100 | 476 | 3.71875 | 1.71875 |
| | | | | |
| 011100110 | 111100110 | 486 | 3.796875 | 1.796875 |
| 111100100 | 011100100 | 228 | 1.78125 | -0.21875 |
| | | | | |
| 110100111 | 010100111 | 167 | 1.3046875 | -0.6953125 |
| 010110100 | 110110100 | 436 | 3.40625 | 1.40625 |
| | | | | |
| 100111100 | 000111100 | 60 | 0.46875 | -1.53125 |
| 000111110 | 100111110 | 318 | 2.484375 | 0.484375 |

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# CHAPTER 4

# $\Delta I_{DDQ}$ TESTING OF A CMOS DATA CONVERTER CONSIDERING PROCESS VARIATION EFFECTS[†]

## 4.1 Introduction

Quiescent current ($I_{DDQ}$) testing has become an effective and efficient testing method for detecting physical defects such as gate-oxide shorts, floating gates (open) and bridging faults [1] in circuits. Conventional $I_{DDQ}$ testing is based on the fact that quiescent current in a defect free circuit is less compared to the quiescent current of the circuit with defects. Several available $I_{DDQ}$ test methodologies can be classified into two groups, external (off-chip) and internal (on-chip) $I_{DDQ}$ testing. External $I_{DDQ}$ testing monitors power supply current through the power pins of the integrated circuit package while internal $I_{DDQ}$ testing monitors power supply current through the built-in current sensors (BICS) [2]. On-chip built-in current sensors are advantageous over off-chip current sensors for detecting the defective quiescent current due to better discrimination and higher testing speeds [3].

Figure 4.1 shows the block diagram of $I_{DDQ}$ testing using on-chip built-in current sensor connected in series with the $V_{DD}$ or GND lines of the circuit under test (CUT). During $I_{DDQ}$ testing a series of input test stimuli are applied to the CUT and the current of the power supply ($V_{DD}$) or ground (GND) terminal is monitored in the quiescent state after the inputs have

[†] Part of the work in this chapter was previously reported in following publications:

1. R. Soundararajan, A. Srivastava and S. Yellampalli, "Process variation effects on $\Delta I_{DDQ}$ testing of CMOS data converters," *Proceedings of the 53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2010)*, pp. 284-287, August 1-4, 2010.
2. R. Soundararajan, A. Srivastava, and S. Yellampalli, "$\Delta I_{DDQ}$ testing of a CMOS digital-to-analog converter considering process variation effects," *Circuits and Systems*, vol. 2 No. 3, pp. 133-138, doi: 10.4236/cs.2011.23020, July 2011.

changed and prior to the next input change [3]. The sub-threshold current in the transistors should be negligibly small for effective testing.

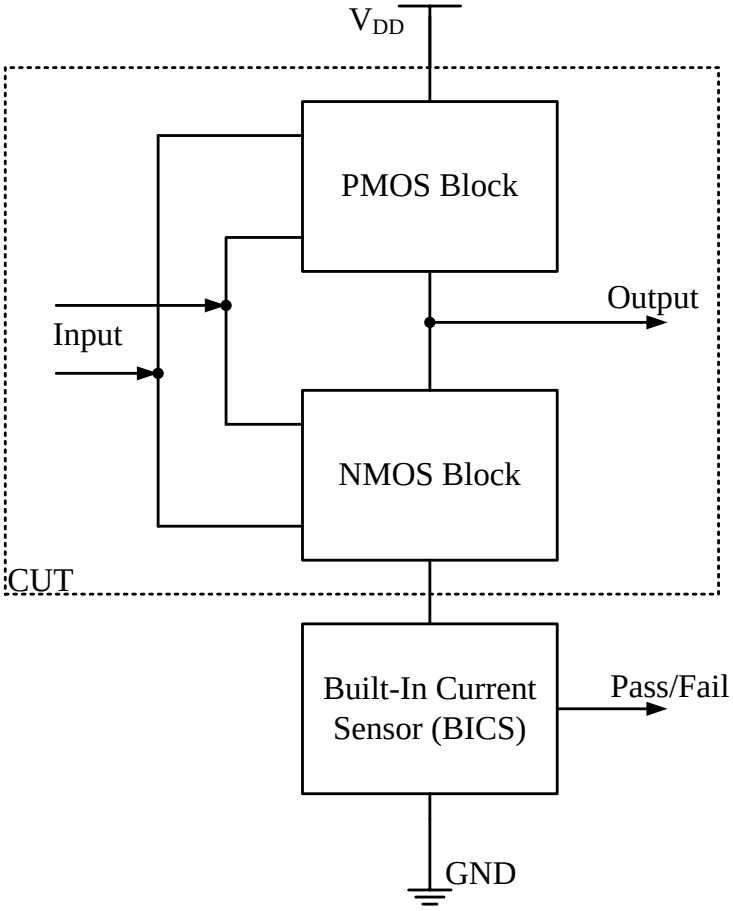


Figure 4.1. Block diagram of $I_{DDQ}$ testing.

Currently in VLSI circuits designed in sub-micron/deep sub-micron CMOS processes, the gap between the defective and defect-free quiescent current is narrowing due to increasing background current [4-6]. Process variation also impacts digital, analog/mixed-signal integrated circuits fabricated in sub-micron/deep sub-micron CMOS technology. Process variation affects the threshold voltage of the circuit and thus the effective leakage current in the circuit. Hence,

designing BICS for sub-micron CMOS process is becoming difficult. However, problems related with $I_{DDQ}$ testing in digital VLSI circuits designed in submicron CMOS processes are well known and have been researched extensively [7]. Many new testing techniques have been proposed and presented in literature to minimize the effect of increased background current and the impact of process variation on the $I_{DDQ}$ measurements to improve defect detection. Among those, delta $I_{DDQ}$ ($\Delta I_{DDQ}$) testing is particularly attractive because the differential measurement suppresses the impact of the background current. Vazquez and de Gyvez [8, 9] have reported a $\Delta I_{DDQ}$ BICS which has both on-chip and off-chip components. Most of these new testing techniques to improve the effectiveness of $I_{DDQ}$ testing have been successfully implemented for digital circuits. However testing of analog circuits using $I_{DDQ}$ in submicron CMOS is still a problem due to variation in design parameters from one specific application to other. Hence, in testing of analog circuits the tolerance on the circuit parameters has to be taken into account because it can cause a significant difference between the quiescent current of a manufactured circuit and its nominal value. A simple pass/fail test is not a good measure for fault detection. Mixed-signal types of circuits such as data converters are even more difficult to test using $I_{DDQ}$. We have extensively researched and presented the $\Delta I_{DDQ}$ testing for sub-micron CMOS mixed-signal circuits in our previous work [10, 11]. In this work, effects of process variation on $\Delta I_{DDQ}$ testing for CMOS data converters are studied and presented.

In this chapter, we present the design and implementation of a built-in-current sensor for delta $I_{DDQ}$ testing in a 0.5µm n-well CMOS process for a 12-bit digital-to-analog converter (DAC) to study the effects of process variation. This chapter is organized as follows: Section 2

describes the proposed sensor and its circuit implementation, Section 3 describes 12-bit DAC which is being used as the circuit under test (CUT), Section 4 presents the results and discussion and Section 5 gives the conclusion.

## 4.2 Built-in Current Sensor for Delta $I_{DDQ}$ Testing

### 4.2.1 Proposed Design

The proposed sensor combines the concepts of multi-parameter testing and delta $I_{DDQ}$ testing to detect defective currents and is based on Keating-Meyer approach for $I_{DDQ}$ testing [12] and is a modification of $I_{DDQ}$ measurement (MEAS) block of delta $I_{DDQ}$ BICS by Vazquez and de Gyvez [8, 9]. Multi-parameter testing helps in suppressing the high background current while delta $I_{DDQ}$ testing helps in decreasing $I_{DDQ}$ variance. Figure 4.2 [8, 9] summarizes the sensor's operation; it has two curves corresponding to low and high leakage. After applying an input pattern to the CUT, the on-chip capacitor is allowed to charge and discharge until it reaches the reference voltage $V_{REF}$.

The expression associated with this discharge is given by [8-11],

$$I_{DDQ} = C\frac{\Delta V}{\Delta t} \tag{4.1}$$

where $\Delta V = V_{DD} - V_{REF}$ and C is the total circuit capacitance including the discharging capacitor. The time $\Delta t$ taken by the decaying voltage of the capacitor to reach $V_{REF}$ is measured as frequency by using a comparator and a voltage controlled oscillator (VCO) as shown in Figure 4.3. The comparator gives an output $V_{CTRL}$, which is used as an input by the VCO to give the output frequency.

In the design, the BICS is on-chip for better testability and higher testing speeds. The proposed sensor also takes into account the process variation after fabrication and self-adjusts for fault detection. This is done by calculating the output frequency of the VCO and subtracting it from the output frequency of the ring oscillator to obtain the final output frequency.

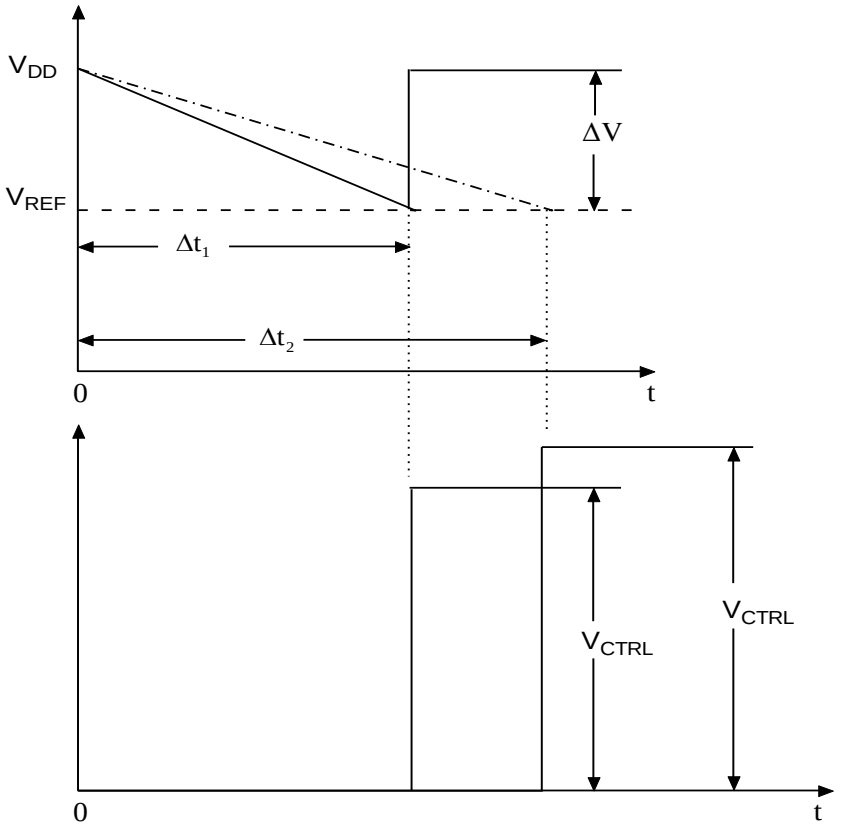


Figure 4.2. Capacitor discharge transient voltage of the CUT under high and low leakage [8-11]. Solid line: fault free condition, dotted line: faulty condition.

### 4.2.2 Circuit Implementation

Figure 4.3 shows the circuit diagram of the BICS where p-MOSFET in earlier MEAS block [8, 9] has been replaced by two transmission gates $TG_1$ and $TG_2$ as switches. The two

transmission gates are used to isolate CUT from the BICS depending on the mode of operation (normal mode or test mode). In the normal mode of operation, the supply voltage $V_{DD1}$ is given to CUT and the BICS is isolated, so that there will be no performance degradation in the CUT.

In the test mode of operation, the supply voltage is given to $V_{DD}$. In this mode, initially transmission gate $TG_1$ between the supply voltage and the CUT is turned on charging the capacitor to $V_{DD}$, transmission gate $TG_2$ between the BICS and the CUT is turned off isolating them during this period. A single clock has been used to turn on and off both $TG_1$ and $TG_2$ as shown in Figure 4.3. For fault detection, $TG_1$ is turned off and $TG_2$ is turned on discharging the capacitor $C_1$ through the CUT. When $TG_2$ is turned on, the node X of the capacitor $C_1$ gets connected to the comparator and the voltage at the node X keeps reducing as the capacitor gets discharged through the CUT. The voltage at node X is compared to the reference voltage through the comparator to give a pulse output. The reference voltage to comparator is given externally so that the width of the pulse at the output of the comparator can be controlled. The output of the comparator is used as input to the NMOS switch which in turn charges the capacitor $C_2$ as shown in Figure 4.3.

The voltage across the capacitor $C_2$, $V_{CTRL}$ depends on the time NMOS switch is on, which in-turn depends on the discharge time of the capacitor $C_1$. The voltage across the capacitor $V_{CTRL}$ is then given to a VCO. The output of a VCO is a clock signal, whose frequency is dependent on $V_{CTRL}$. Its operation is similar to that of a ring oscillator. The oscillation frequency of the current starved VCO for n number (an odd number $\geq 3$) of stages is given by,

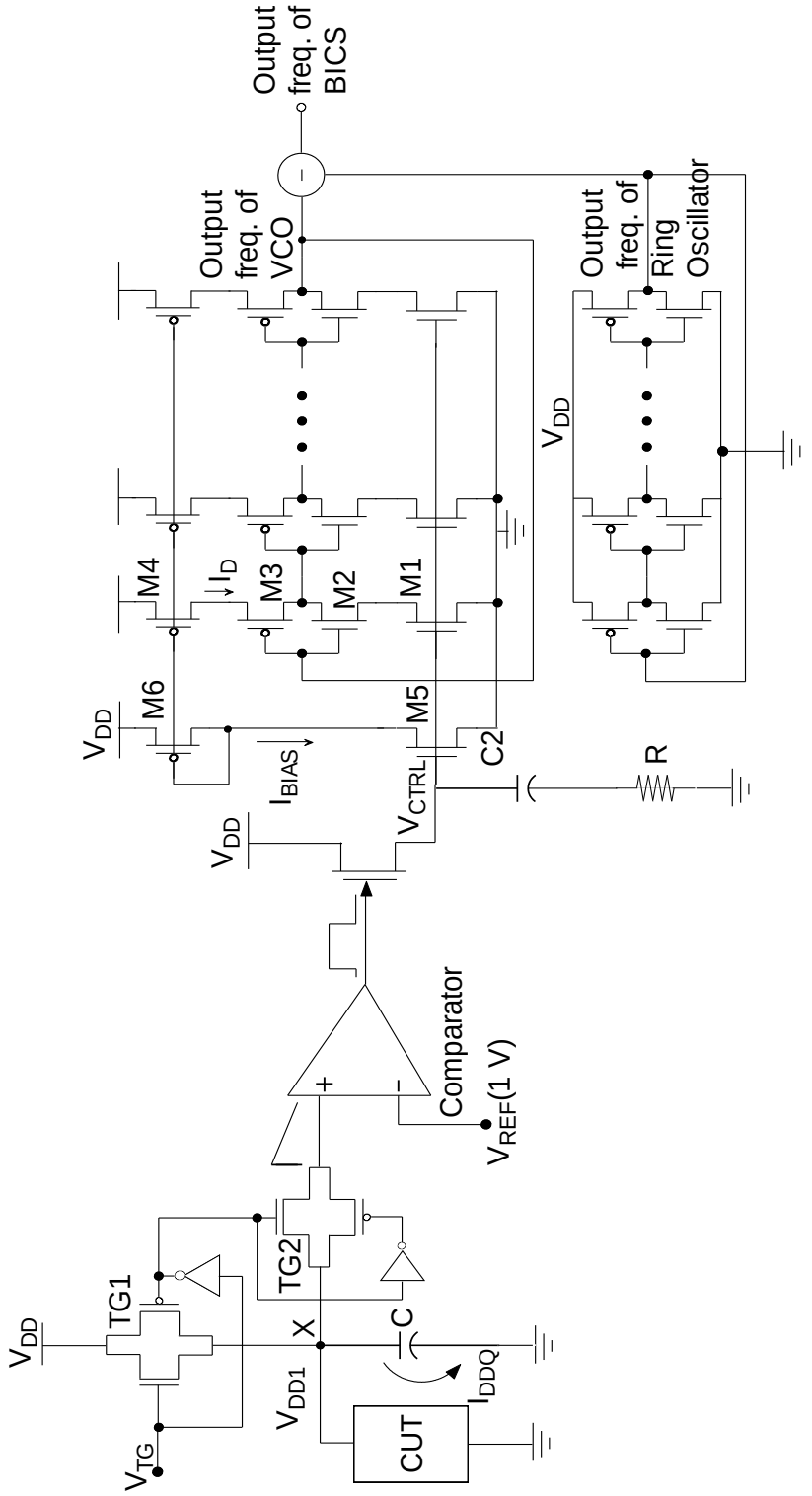


Figure 4.3. $\Delta I_{DDQ}$ built-in current sensor (BICS) [10, 17, 18].

$$f_O = \frac{1}{n\left(t_r + t_f\right)} \approx \frac{I_D}{n \cdot \left(C_{out} + C_{in}\right) \cdot V_{DD}} \tag{4.2}$$

where, $t_r$ and $t_f$ are the rise time and the fall time, respectively, and n is the number of stages. $V_{DD}$ is the power supply voltage. $I_D$ is the biasing current. The biasing current can be adjusted by varying the control voltage, which in turn changes the oscillation frequency. The output frequency of the voltage controlled oscillator is subtracted from the frequencies of the ring oscillator to obtain BICS final output frequency as shown in Figure 4.3. This method helps to overcome the process variation in sub-micron CMOS technology.

## 4.3 12-bit DAC Design (CUT)

The 12-bit DAC design uses a charge scaling architecture and the block diagram is shown in Figure 4.4 [13]. The DAC converts a 12-bit digital input word to a respective analog signal by scaling a voltage reference. The DAC consists of voltage reference, binary switches, scaling network, an operational amplifier and a sample and hold circuit. The multiplexer circuit connected to the other end of each capacitor, selects the voltage which is either $V_{REF}$ or GND to which the capacitor is charged depending upon the control signal '$V_S$'. Initially, the control signal for all multiplexer switches is set to LOW before giving any specified input so that GND is supplied to the capacitor network and reset. Then the capacitor network is supplied with the digital word by switching the particular multiplexer switch for each bit to the desired value of either $V_{REF}$ for "1" or GND for "0". The capacitors whose ends are connected to $V_{REF}$ are charged to +2V and those, which are connected to GND, are charged to 0V. Since the capacitor network is connected in parallel, the equivalent voltage is calculated by [13],

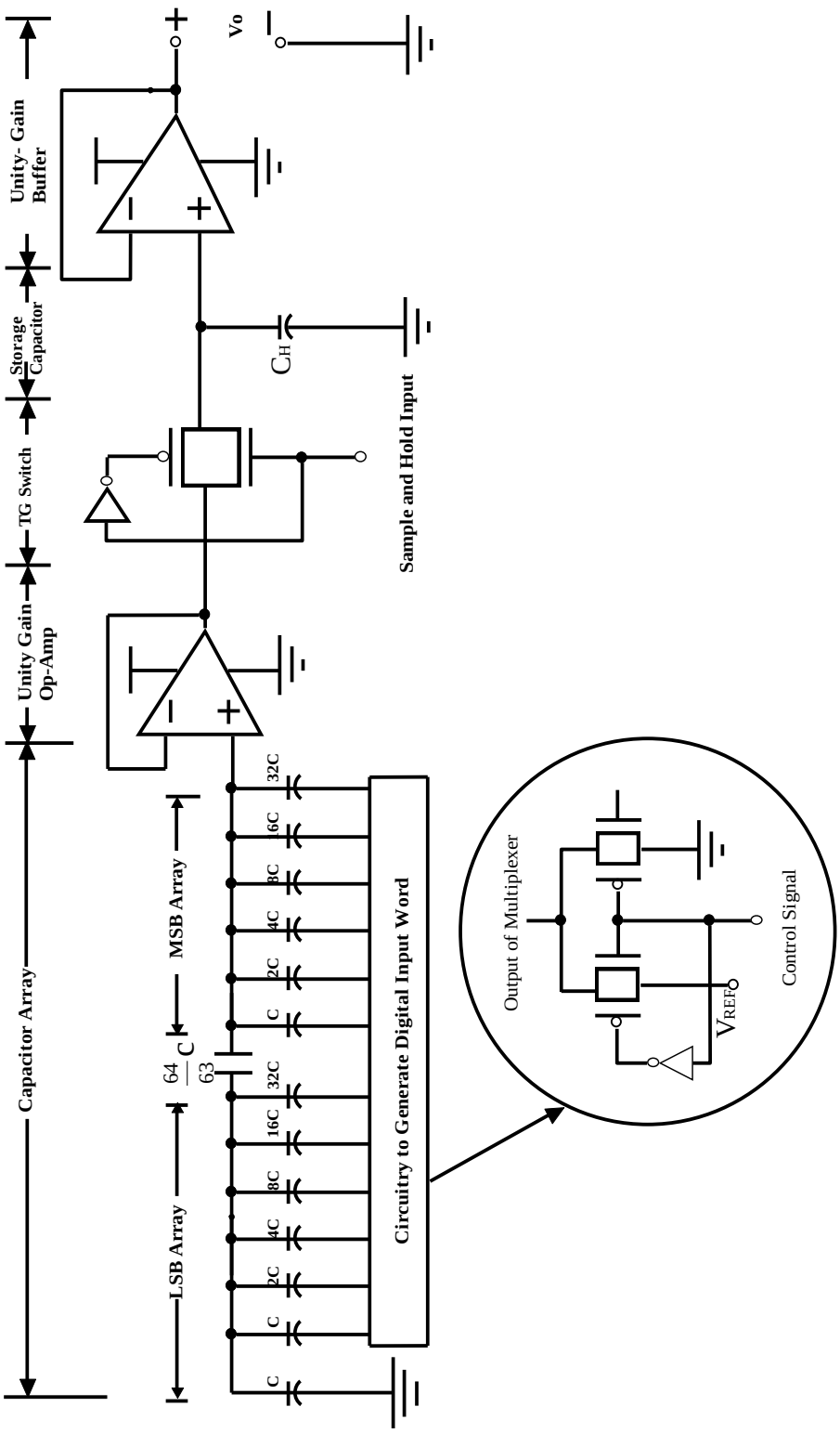


Figure 4.4. Schematic of a 12-bit charge scaling DAC [10, 17, 18].

$$V_{OUT} = (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \ldots\ldots + B_N 2^N) V_{REF} \quad (4.3)$$

The capacitor at the end of the network is used as a 'terminating capacitor'. Depending on the capacitors, which are charged to different voltages based on the input digital word, the effective resultant analog voltage is calculated for the respective digital combination. The analog voltage is passed through the op-amp and the sample-and-hold circuit and appears as an analog voltage. The op-amp and comparator used in DAC is designed for 2.5V operation.

## 4.4 Results and Discussion

Figure 4.5 shows the chip layout of a 12-bit DAC designed for operation at 2.5V in 0.5μm n-well CMOS process with eight defects introduced using fault injection transistors (FITs) as switches [14]. The design integrates an on-chip BICS of Figure 4.3 for $\Delta I_{DDQ}$ testing of physical defects such as shorts in MOSFETs. The DAC occupies 504 X 501$\mu m^2$ area of the chip. The BICS occupies 20% (670 X 75$\mu m^2$) of the total chip area.

In testing of analog and mixed signal circuits, the dependence of the power supply current on the circuit parameters has to be considered. This can result in a significant difference between the fabricated (manufactured) circuit and its nominal value. So a fault-free circuit can be considered as faulty and vice-versa [10, 11, 15]. This problem is overcome in the present work by considering a tolerance limit of ±10% on the fault free output frequency value. It thus takes into account the variations due to significant technology and design parameters. The circuit has been designed using the model parameters T69K [16] and the frequency output of the BICS is

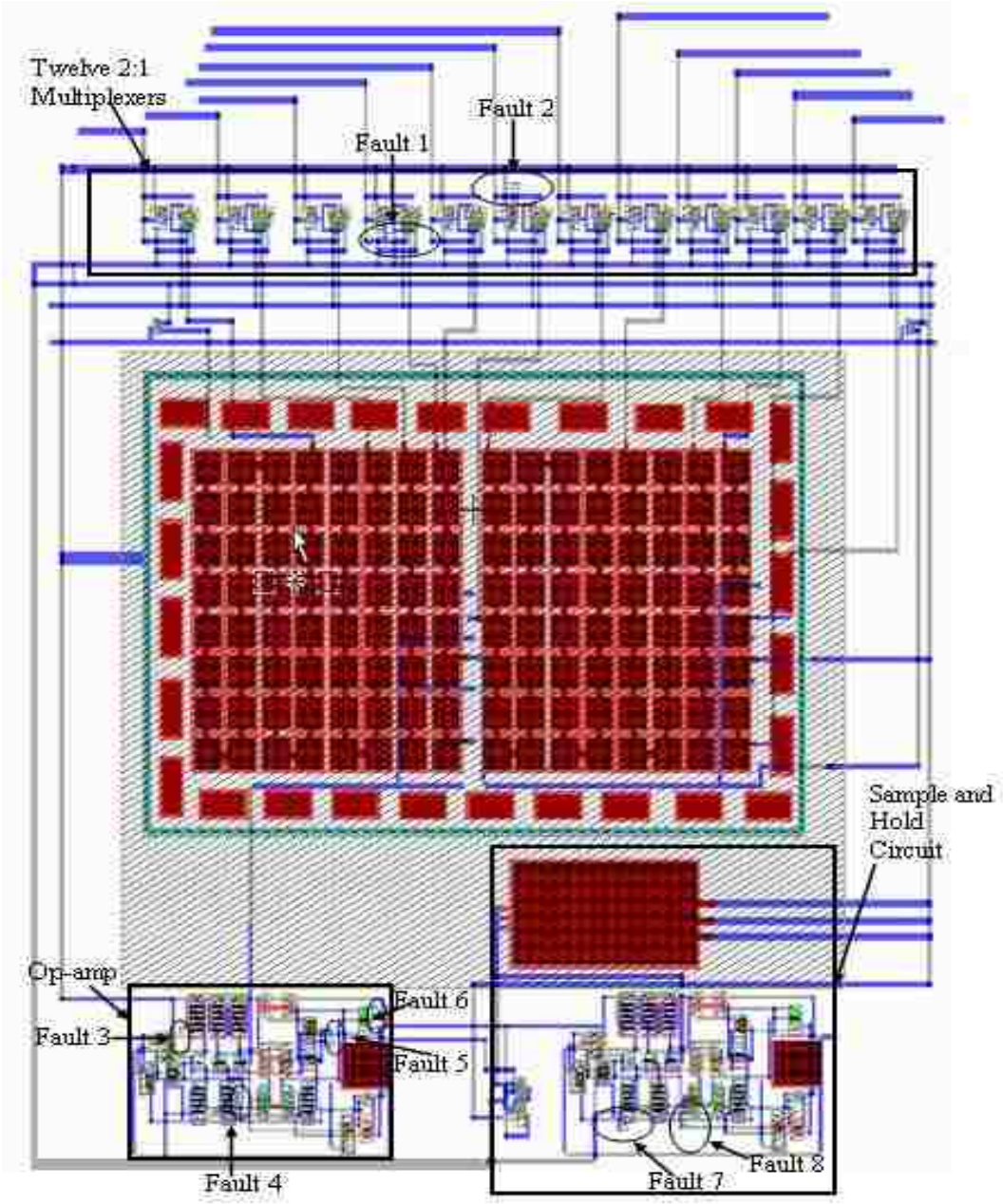


Figure 4.5. Chip layout of 12-bit DAC and BICS with induced faults [10, 17, 18].

called the natural frequency ($f_N$). The BICS has been simulated with various model parameters to check for the effects of process variation on the deviation of the output frequencies from the natural frequency. The results are presented in Figure 4.6.

From Figure 4.6, it can be observed that the deviation of the output frequency of the BICS is less than ±10 % for all the model parameters except T5CX [16], T51T [16], T3CU [16] thus falling within the tolerance limit. To check the robustness of the BICS against the process variation, the output frequencies obtained by BICS for the different model parameters have been modified by ±10 % and their deviation with the natural frequency have also been calculated and shown in Figure 4.6. It can be observed from Figure 4.6 that even with the variation of the output frequencies obtained by BICS by either +10% or -10%, the deviation is within ±10 % of the natural frequency. Thus, the CUT can be designed using one set of model parameters and the same natural frequency value can be used for fault detection after fabrication using the BICS.

The CUT is then simulated after introducing faults using fault injection transistors one by one. Table 4.1 summarizes the output frequency of the BICS along with their deviation from the natural frequency.

Fault-1 simulates a physical short between drain and source of one of the transistors in multiplexer part of the circuit of Figure 4.4, Fault-2 simulates a physical short between drain and source of one of the transistors in multiplexer part of the circuit of Figure 4.4, Fault-3 simulates a physical short between gate and source of one of the transistors of the op-amp part of the circuit of Figure 4.4, Fault-4 simulates a physical short between drain and source of one of the transistors of the op-amp part of the circuit of Figure 4.4. Fault-5 simulates a gate-substrate short

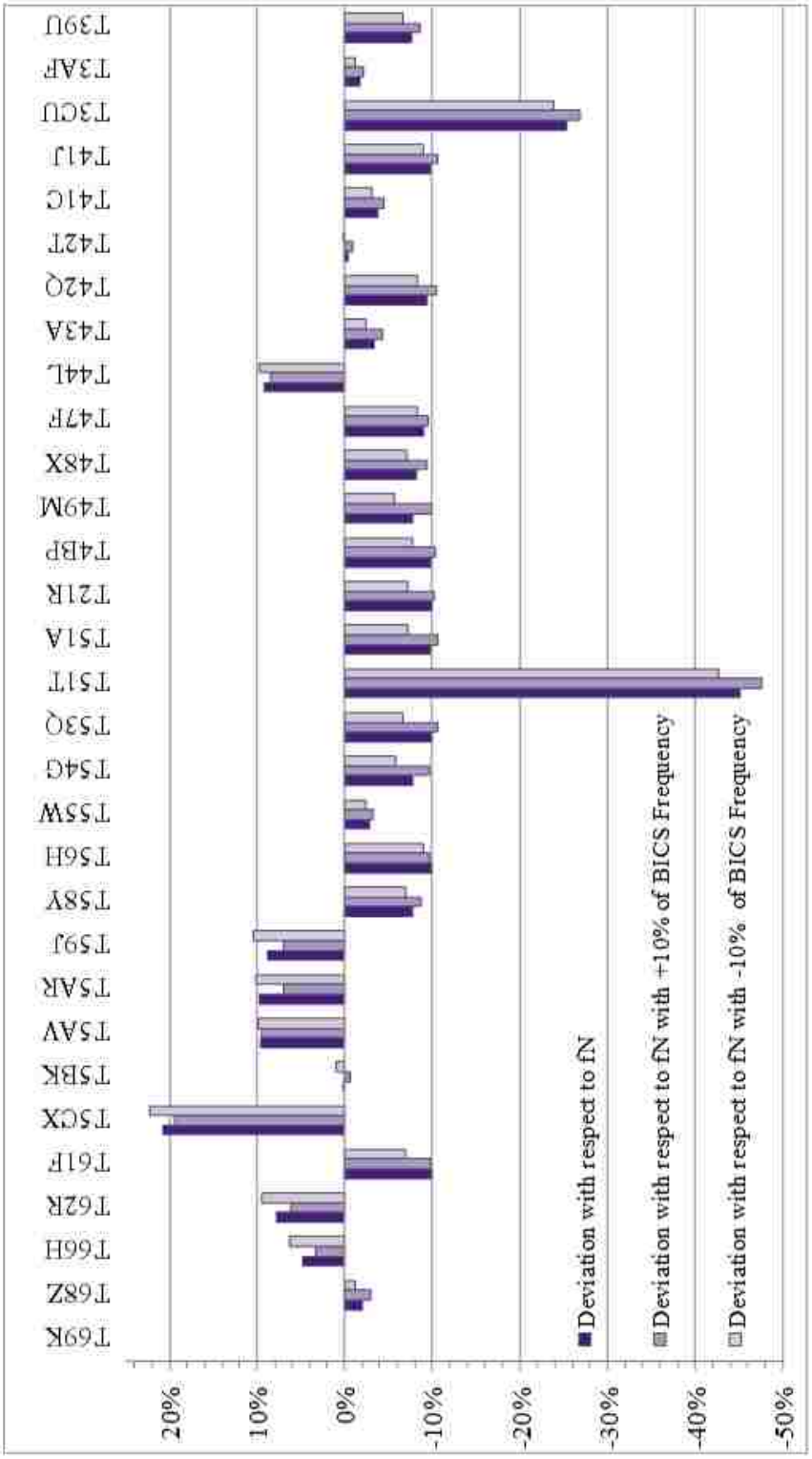


Figure 4.6. Deviation of BICS output frequency to natural frequency ($f_N$).

in one of the transistors of the op-amp part of the circuit of Figure 4.4. Fault-6 simulates a gate-drain short of one of the transistors of the op-amp part of the circuit of Figure 4.4, Fault-7 simulates a source-substrate short of one of the transistors of the sample-and-hold circuit part of the circuit of Figure 4.4 and Fault-8 simulates an inter-gate short between two transistors in the unit gain op-amp of the sample-and-hold circuit part of the circuit of Figure 4.4. From Table 4.1 it can be noted that the deviation is greater than ±10% and thus detecting the introduced faults.

Table 4.1. Deviation of BICS output frequency from natural frequency with induced faults.

| **Fault** | **Output Freq. of VCO (MHz)** | **Freq. of Ring Oscillator (MHz)** | **Output Freq. of the BICS (kHz)** | **Deviation (%)** |
|---|---|---|---|---|
| No Fault | 2.632 | 2.632 | 0 | 0 |
| Fault 1 | 3.226 | 2.632 | 594.227 | 22.58 |
| Fault 2 | 3.125 | 2.632 | 493.421 | 18.75 |
| Fault 3 | 2.326 | 2.632 | -305.998 | -11.63 |
| Fault 4 | 2.222 | 2.632 | -409.357 | -15.56 |
| Fault 5 | 2.326 | 2.632 | -305.998 | -11.63 |
| Fault 6 | 2.941 | 2.632 | 309.597 | 11.76 |
| Fault 7 | 2.326 | 2.632 | -305.998 | -11.63 |
| Fault 8 | 2.222 | 2.632 | -409.357 | -15.56 |

## 4.5 Conclusion

We have proposed and implemented a BICS for CMOS data converters fabricated in 0.5µm n-well CMOS process. The circuits are designed to overcome the problem of increase in absolute value of quiescent current due to increasing background current. It also overcomes the variation in the value of quiescent current due to the change in threshold voltage and leakage current caused by process variation in the circuit. Thus, the increase in quiescent current caused

due to defect can be estimated accurately in sub-micron CMOS data converters. The process variation effects on the $\Delta I_{DDQ}$ testing of the data converters are considered and simulated for various model parameters. The deviation of the output frequency of the BICS is observed to be less than ±10% for the model parameters and more than ±10% for various faults introduced in the data converter circuit using fault-injection transistors.

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# CHAPTER 5

# ON-CHIP FUNCTIONAL TESTABILITY OF CMOS ANALOG-TO-DIGITAL CONVERTERS BY LINEAR RAMP HISTOGRAM TECHNIQUE USING SYNCHRONOUS COUNTER AS REGISTER‡

## 5.1 Introduction

One of the most prominent BIST techniques for ADC used to determine the static parameters like offset, gain error and non-linearity is the histogram method [1, 2, 3] and this has been the focus of many research and papers recently. In histogram based BIST approach, an input signal (either sinusoidal or linear ramp) is applied to the ADC input and the number of times each code appears, commonly known as hits-per-code (HPC) on the ADC output (code frequency statistics) is recorded. The HPC is then analyzed to derive the static parameters like integral non-linearity (INL), differential non-linearity (DNL), offset voltage and gain error in terms of ADC's least significant bit (LSB). In histogram based BIST, to collect the HPC for an n-bit ADC, we require access to $2^n$ on-chip memory. In the absence of on-chip memory, histogram technique with external code detection unit is used, which in turn increases the test time. Currently significant research has been carried out on optimizing histogram technique for data converters [4-7].

Also other methods like Servo-Loop test, FFT test are used to verify the performance metrics of the ADC. Servo-Loop testing is based on feedback loop that forces the ADC to any desired code transition edge, and the output code generated by the ADC is compared against a

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value programmed into the search register [2, 3]. A typical servo-loop consists of an integrator which generates the feedback signal by integrating either the positive or negative reference voltage depending on the comparator output, which compares the ADC digital output code with the desired code [2, 3]. The main potential limitation of the servo-loop testing is the delay introduced by the feedback loop. The FFT test method is similar to the histogram technique, where the data is stored as a file or in a memory buffer instead of plotting as a normalized histogram. After the completion of the test measurement, the data is processed using the Fast Fourier transform to analyze the quantization noise and harmonic distortion caused by INL or DNL. Hence this method can be used to compute signal-to-noise ratio (SNR), the effective number of bits (ENOB), aperture uncertainty, noise, missing codes and the nonlinearities. But in FFT test the applied input signal to the ADC should not coincide with the harmonics caused by the nonlinearity of the ADC. Also in FFT test it's not possible to measure the SNR accurately. Hence, histogram based BIST is focused mainly in the research.

In this work, a design for on-chip linear ramp histogram technique for CMOS analog-to-digital converter is proposed and implemented. In this chapter, Section 2 gives a brief overview of the histogram technique. The formulae used to calculate the parameters are presented here. Section 3 deals with the proposed architecture and explains each unit of the design and its implementation. Section 4 discusses the results and the effectiveness of the design.

## 5.2 Histogram Technique

As explained earlier, histogram technique is among the most classical approaches to test ADC. In the histogram technique, a periodic waveform that covers the entire full scale range

(FSR) is applied to the ADC's analog input. The number of times each digital code appears or hits-per-code (HPC) is registered and stored. These HPC are then plotted as a function of the digital output code. The histogram techniques are classifies into sine-wave or linear ramp depending upon the type of input signal applied to the circuit under test (CUT). However since the linear histogram technique allows the reduction of the required memory for the storage of the ideal histogram rather than the sinusoidal one, we have focused on it in this work. Also, since in the sinusoidal histogram due to the non-uniform distribution of the HPC, complex trigonometric computations are needed to derive the ADC parameters. By using the linear-ramp input due to the uniform distribution of the HPC, simple linear computation can be used to derive the ADC parameters as described in the following section. Figure 5.1 shows an example of an ideal 8-bit ADC histogram with a linear ramp input [8-10].

The HPC for a particular digital code depends on the time that is spent at a specific code, since ideally for a triangular wave the time that is spent at each code is the same. Hence an ideal 8-bit ADC will have a rectangle histogram distribution, whose width is $2^{bits}$ ($2^8 = 256$). Height of the histogram is dependent on the time spent at a specific code in a triangular wave and the number of triangular wave used in the technique. The on-chip linear ramp histogram technique has been implemented by sending triangular (or linear ramp) wave as the input which is generated on-chip using a linear ramp generator. An integral number of periods of the input triangular waveform are sent so as to ensure that each code has equal probability of occurrence. The numbers of periods of the input triangular waveform sent to the ADC input are in accordance with the coherent sampling condition. Further care has to be also taken to choose an

input frequency that is not a multiple of the sampling frequency so that the sampling points are different during each input signal cycle. The peak-to-peak amplitude of the input triangular waveform is slightly higher than the full scale range (FSR) of the ADC in order to cover all digital codes.

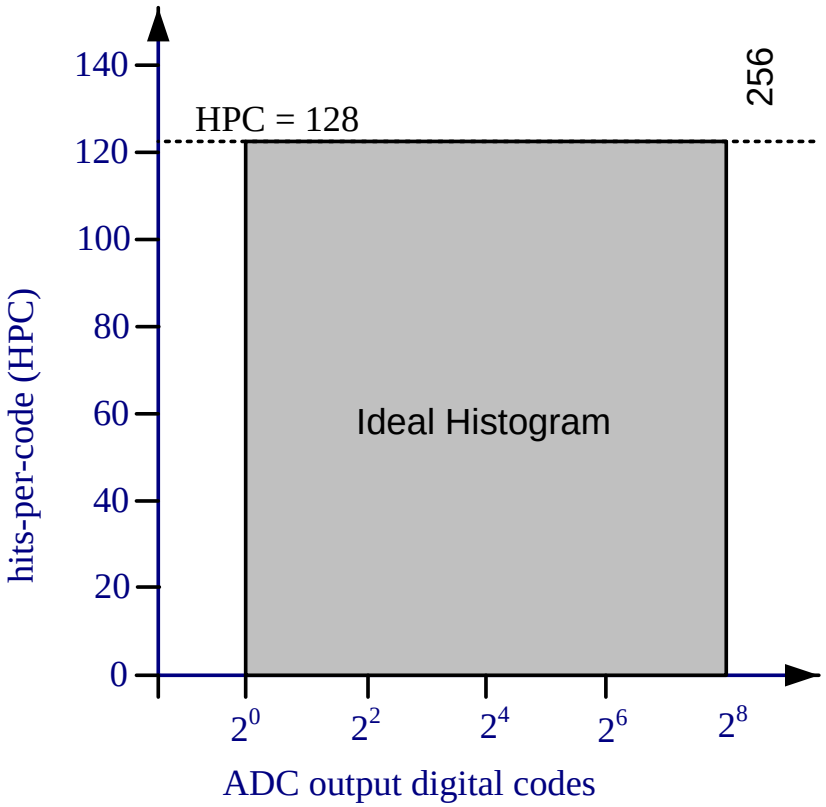


Figure 5.1. Example of an 8-bitADC histogram [8-10].

### 5.2.1 ADC Parameters

In this section, we will derive the linear computation required to evaluate the different ADC performance metrics or parameters using linear ramp histogram technique [11]. The step

size of an ideal ADC is 1 LSB (least significant bit). Here 'n' refers to the no of bits of ADC being used.

$$LSB = \frac{FSR}{2^n} \tag{5.1}$$

Due to the quantization process and the non-idealities in the circuit, the actual behavior of the ADC deviates from the ideal behavior and the magnitude of this deviation from the ideal transfer function of an ADC is termed as an error. Offset, gain and non-linearity errors are the primary static parameters of an ADC.

Offset error is the horizontal difference in LSB between the actual transition and the ideal one at the lowest digital code (00000000 for an 8-bit ADC). This difference is reflected in terms of the hits-per-code (HPC) of the first and last code. The derivation of the formula can be seen in Eq. (5.2) [11].

$$OFFSET = \frac{HPC(0) - HPC\left(2^n - 1\right)}{2 \times HPC_T} \tag{5.2}$$

Where, the theoretical hits-per-code ($HPC_T$) is the average number of samples in the non-extreme codes as shown in Eq. (5.3).

$$HPC_T = \frac{\sum_{i=1}^{i=2^n-2} HPC(i)}{2^n - 2} \tag{5.3}$$

Gain error is the horizontal difference in LSB between the actual transition and the ideal one at the highest digital code (11111111). This is reflected as the ratio between the ideal hits-

per-code ($HPC_{ideal}$) and the actual HPC. Since the ratio varies from code to code it has been proposed in Eq. (5.4) [11] to calculate the inverse gain error as per the formula given below.

$$\text{GAIN ERROR} = \frac{\sum_{i=1}^{i=2^n-2} HPC(i)}{HPC_{ideal} \times \left(2^n - 2\right)} \tag{5.4}$$

Differential nonlinearity (DNL) is the difference between the actual separation between two adjacent codes and 1 LSB. The HPC of a code reflects the code width, the greater the HPC the greater is the code width. The DNL for ADC is calculated according to the formula given below [11].

$$DNL(i) = \frac{HPC(i)}{HPC_T} - 1 \tag{5.5}$$

Integral nonlinearity (INL) is the deviation of the actual transfer function from the ideal and can be computed with this test by compiling a cumulative histogram. In other words, it is equal to the summation of the DNL errors along the converters transfer function [11].

$$INL(k) = \sum_{i=1}^{i=k} DNL(i) \tag{5.6}$$

## 5.3 On-Chip Linear Ramp Histogram Design

As explained earlier, the histogram technique is the statistical analysis of counting the number of occurrences of the digital output code from the ADC (CUT) whose input is a linear ramp or a sinusoid waveform. Since, the linear histogram technique allows reducing the memory overhead drastically; we have proposed a design for implementation of on-chip testability of

CMOS analog-to-digital converter using linear ramp histogram technique. The block diagram of the proposed on-chip linear ramp histogram technique is as shown in Figure 5.2.

The proposed design implements the required components on-chip and the parameters INL, DNL, gain error and offset error are measured and computed simultaneously leading to lower test times. The block diagram consists of a linear ramp generator, analog-to-digital converter or circuit-under-test (CUT), code detection unit (CDU), and interface/control unit. In the proposed design, the ADC can be operated in either test mode or normal mode by using multiplexer and a select signal between the ADC (CUT) and linear ramp generator and also between the ADC and the code detection unit. In normal mode of operation, the ADC is connected to the analog input and the digital output code is connected directly to the pad frame. In test mode of operation, the linear ramp from the linear ramp generator is connected to the ADC input and the digital output code is connected to the code detection unit.

### 5.3.1 Linear Ramp Generator Design Implementation

In linear histogram ramp technique, the major requirements for the linear ramp generator are as follows. The area of the ramp generator should be small to lower cost, the quality of the generator should exceed the ADC tested and the ramp width should be programmable [11, 12]. Also the generated linear ramp signal should be error free to improve the test quality (error in ramp linearity and slope introduces INL and DNL in ideal ADC). In this design, the basic linear ramp can be generated by charging the capacitor by a constant current [11-13] as shown in Figure 5.3. The resulting voltage across the capacitor is a linear ramp proportional with time (t). The linear ramp generator consists of a switch to control the duration of the ramp and a switch to

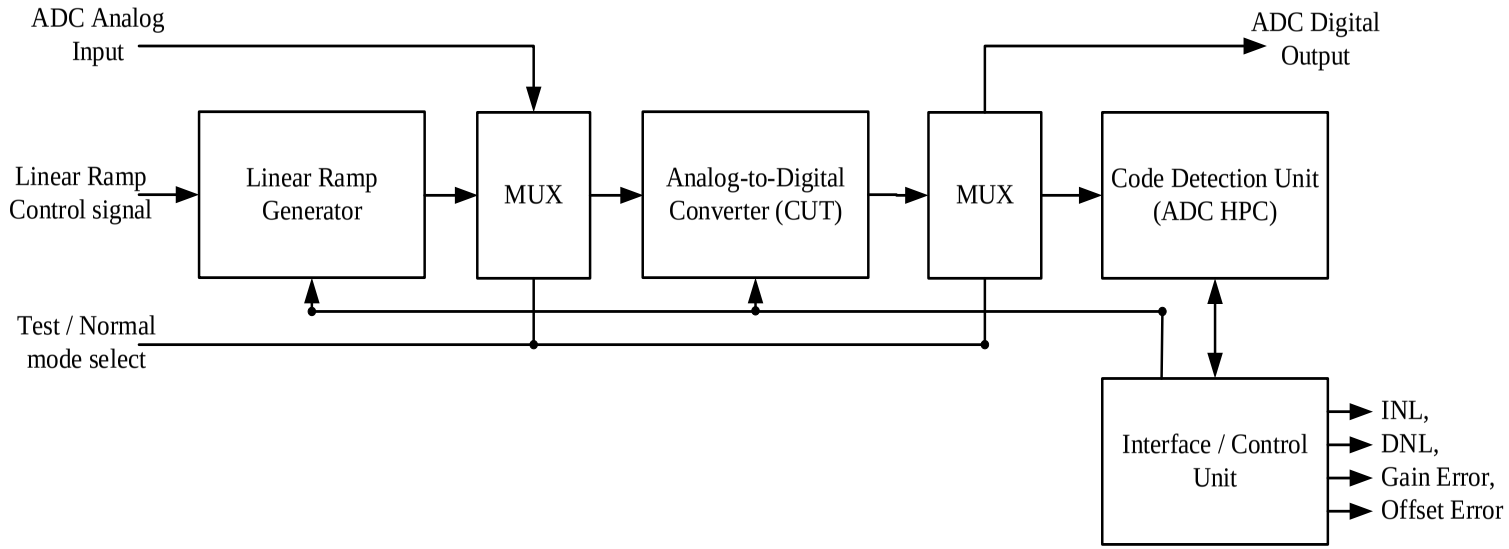


Figure 5.2. Block diagram of on-chip linear ramp histogram technique for ADC [14].

initialize the generator, in addition to the current source and the charging capacitor. The circuit implementation of the linear ramp generator is as shown by the schematic in Figure 5.4. The layout of the linear ramp generator is as shown in Figure 5.5.

But there exist inaccuracies in the circuit due to variation of the current source and the capacitor values during fabrication. Hence, we need to use an adaptive or corrective scheme [11-13], which uses two reference signals to define the period of the ramp (Step) and the reference voltage ($V_{ref}$). Here the current source value of the ramp generator is adjusted to the proper value, so that the ramp voltage converges with the reference voltage within the given period. The corrective scheme is based on a very simple capacitive structure and comprises of 3 blocks, ramp generator circuit, comparator and ramp rate control circuit as shown in Figure 5.6.

### 5.3.2 Interface/Control Unit

The interface/control unit is one of the main components and controls all the other components in the proposed design. This also keeps track of the each code and updates the registers throughout the complete test. At the end of the linear ramp, this unit also serves to transfer the required HPC for computation of ADC parameters (INL, DNL offset error and gain error) to a register or to the pad frame. This unit also contains some registers to store the intermediate value needed for computation of various ADC parameters.

### 5.3.3 Code Detection Unit (CDU) Design Implementation

In the proposed design, the code detection unit is the major component and it detects the hits-per-code (HPC) for the ADC digital output code. The block diagram of the proposed code

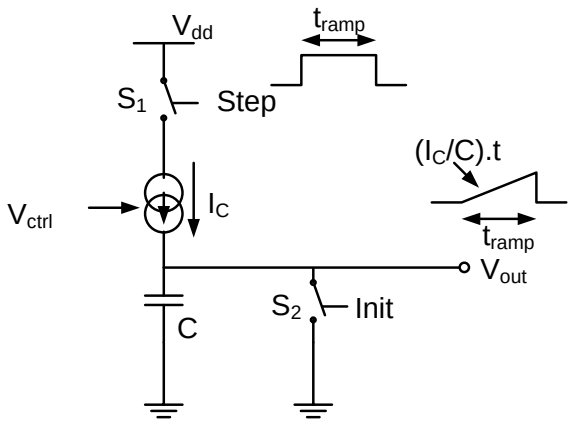


Figure 5.3. Principle of linear-ramp generator [12].

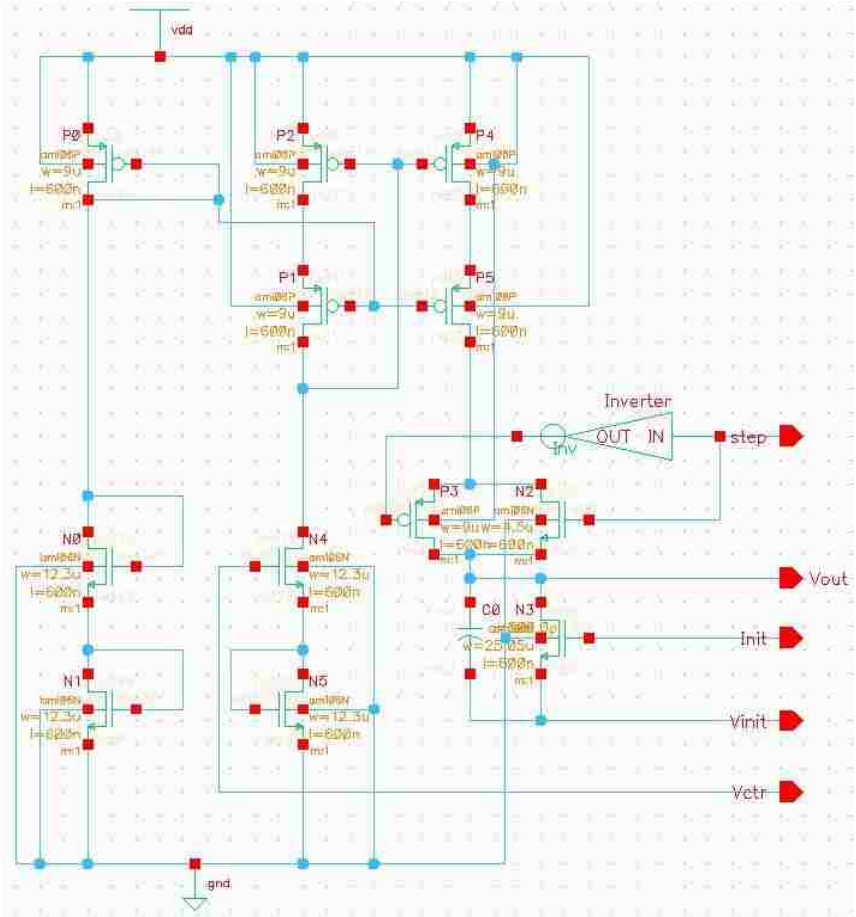


Figure 5.4. Schematic of the designed linear ramp generator.

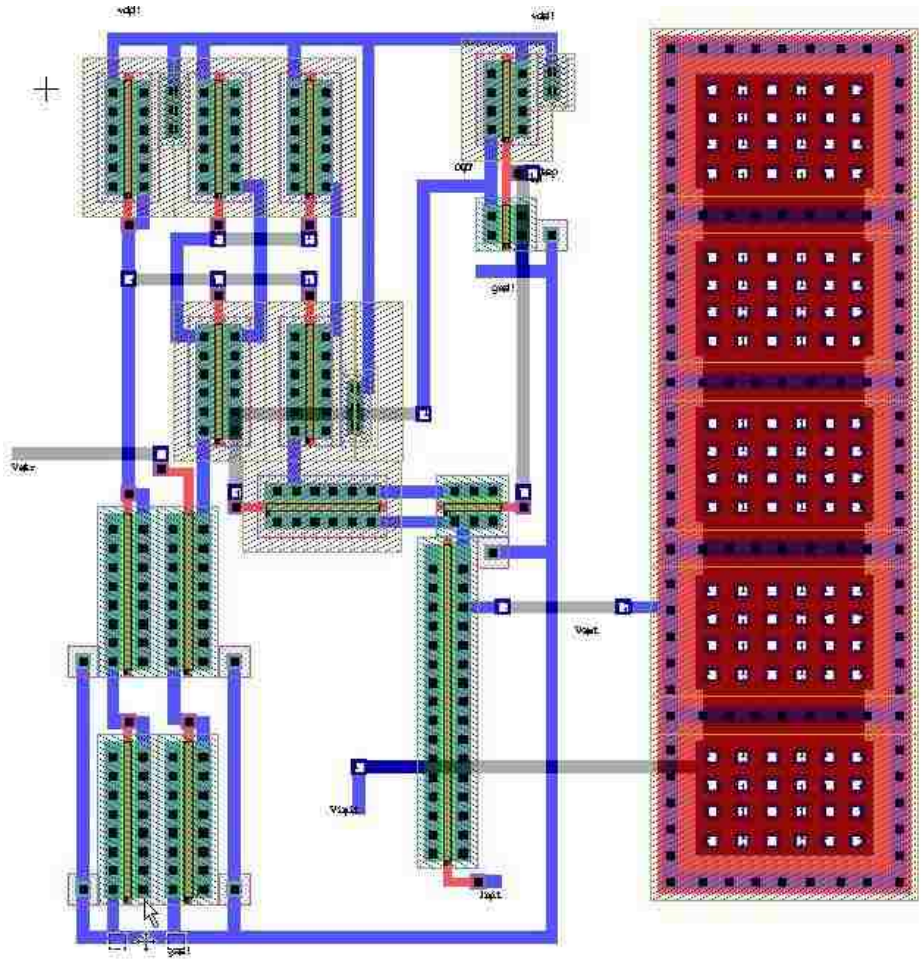

Figure 5.5. Layout of designed linear ramp generator.

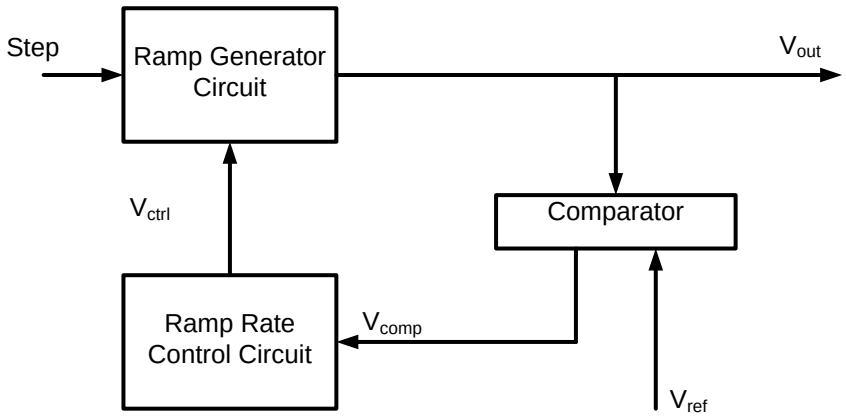


Figure 5.6. Block diagram of the corrective scheme [12].

detection unit is as shown in Figure 5.7. It consists of a 16 X 16 register bank (256 registers) to store the HPC for the 8-bit ADC as we require $2^8$ registers, and two 4-to-16 decoders to select the appropriate register in the register bank for the ADC digital output code.

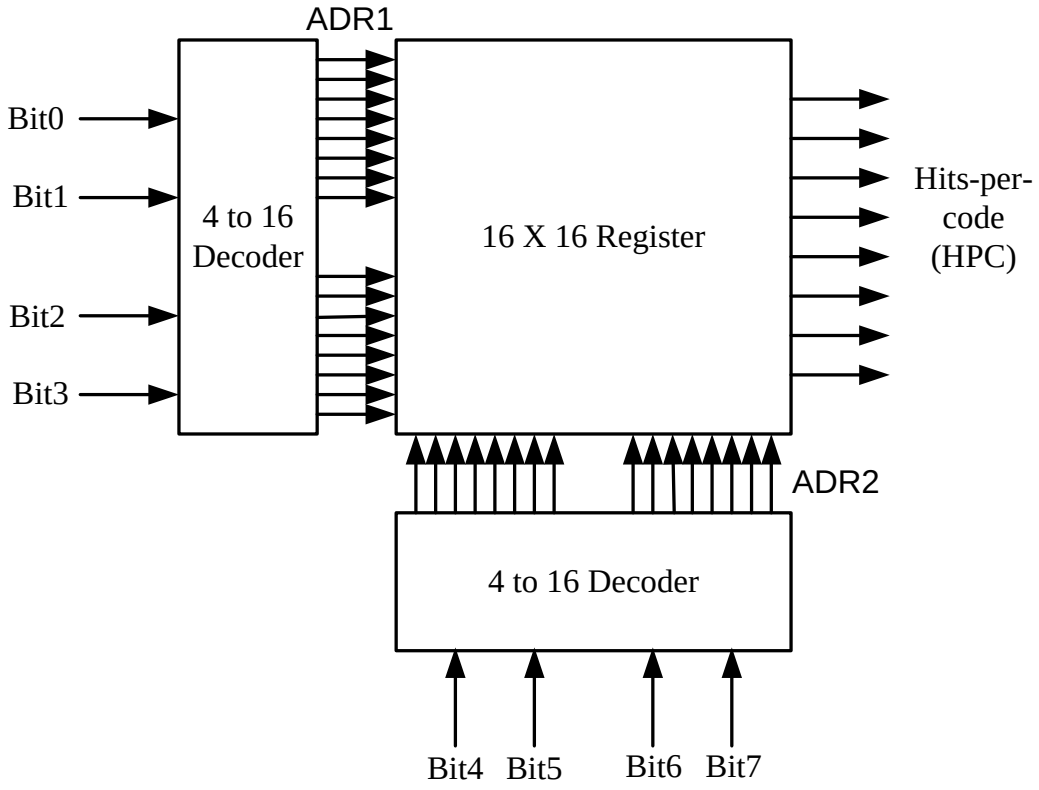


Figure 5.7. Block diagram of code detection unit (CDU) [14].

The 4-to-16 decoders are used to decode the 8-bits from the ADC to 16 X 16 bits, which are then used to select the appropriate register in the register bank to store or fetch the HPC for the ADC tested. The lower 4 bits from the ADC are used in the first 4-to-16 decoder to produce the output address1 bit 0 to bit 15 (ADR1[0:15]) which is used as row selector and the higher 4 bits from the ADC are used in the second 4-to-16 decoder to produce the output address2 bit 0 to bit 15 (ADR2[0:15]) which is used as column selector. The 16-bit address1 and address2 are then

used by the register bank to select the appropriate register in the register bank. The 4-to-16 decoders are used in both the read/write process of the selected register in the register bank.

In the CDU during the write process, the ADC digital output code are used by the two 4-to-16 decoders and the appropriate register in the register bank is selected. After the register in the register bank is selected, the HPC is accumulated and stored in the register for each occurrence of the ADC digital output code. During the read process, the interface/control unit selects the appropriate register to fetch the HPC stored in the respective register and use it for the computation of the ADC parameters. Hence during the read process, the 8-bits to the two 4-to-16 decoders are generated by the interface/control unit and the ADC is isolated from the CDU using multiplexers.

#### 5.3.3.1 4-to-16 Decoder Design Implementation

The 4-to16 decoders are used in the code detection unit (CDU) to decode either the digital output code of the ADC to be tested during write process or the digital code generated by the interface/control unit during the read process and generate the register select signals address1 (ADR1[0:15]) and address2 (ADR2[0:15]). These signals are used to select the appropriate register in the register bank either to write or read the HPC. The 4-to-16 decoders are designed and implemented using four inverter and sixteen 4-input AND gates [15]. The schematic and layout of the 4-to-16 decoders design are as shown in Figure 5.8 and Figure 5.9, respectively. As discussed earlier in the implemented 4-to-16 decoders, the first 4-to16 decoder uses the lower 4-bits and is used as the row selector whereas, the second 4-to-16 decoder uses the higher 4-bits and is used as the column selector.

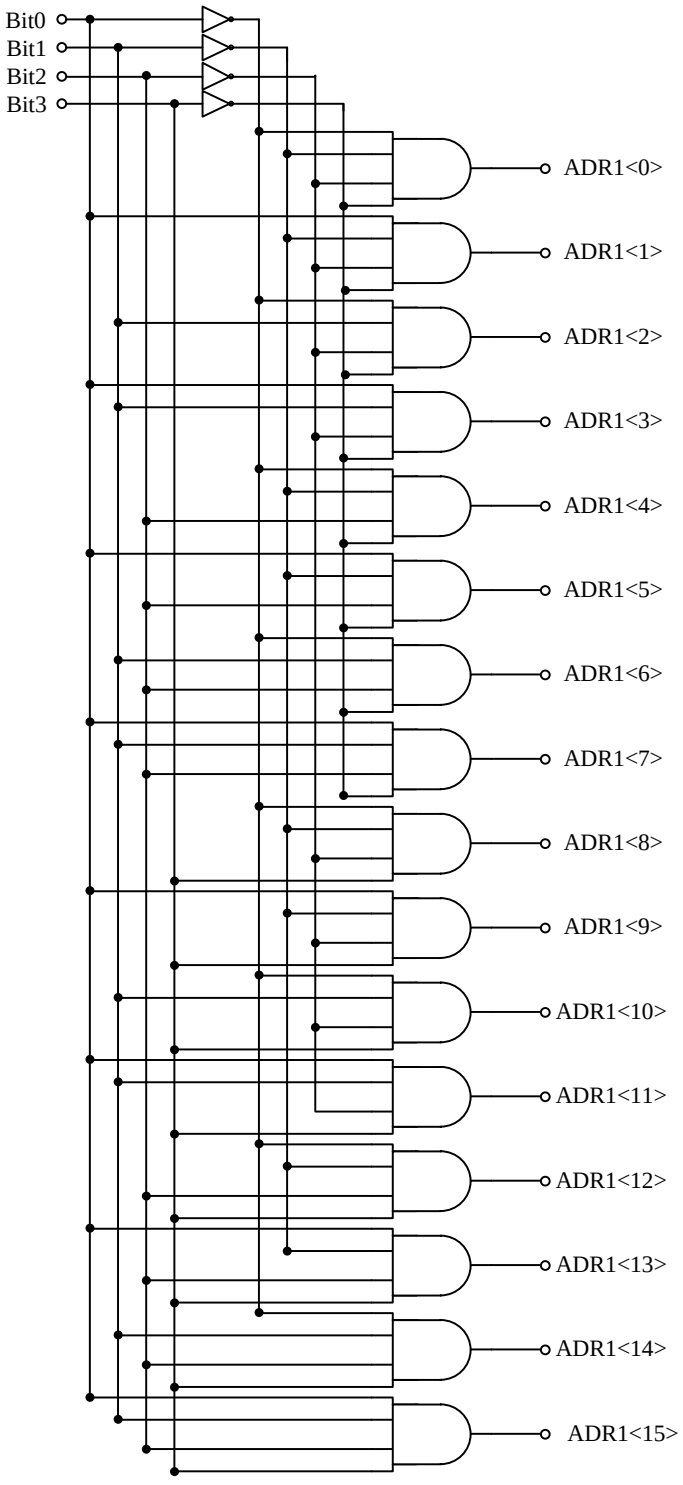


Figure 5.8. Schematic of the 4-to16 decoder circuit [15].

5.3.3.2 Register Design Implementation

The block diagram of the register used in the 16 X 16 register bank is shown in Figure 5.10 and the design implementation consists of a synchronous counter to accumulate the HPC for each occurrence of the ADC digital output code, a readout circuit and read/write enable circuit. The16-bit address1 (ADR1[0:15]) and address2 (ADR2[0:15]) from the two 4-to-16 decoders along with the read/write signal are used in the read/write enable circuit to select the appropriate register in the register bank during the read or write process. During the write process the 8-bit ADC digital output is used by the two 4-to-16 decoders and the write enable signal by the read/write enable circuit to select the appropriate register and increment the count (HPC) in the synchronous counter by 1. This is achieved by using an AND gate whose inputs are ADR1, ADR2, CLK and write enable (WR) and the output is fed to the clock of the synchronous counter. The count or HPC is incremented by 1 in the synchronous counter (register) every time the code is repeated. During the read process the interface/control unit generates the required 8-bit code which is used by the two 4-to-16 decoders and the read enable signal by the read/write enable circuit to select the appropriate register and fetch the contents or count (HPC) stored in the selected register. This is also achieved by the AND gate whose inputs are ADR1, ADR2 and RD and the output is used to enable the readout circuit.

The synchronous counter used in the register implementation is designed by using JK flip flop and AND gate and is shown in the schematic in Figure 5.11 [15]. The synchronous up counter is designed by using eight JK flip flop and six 2-input AND gates. The design is implemented by enabling each JK flip flop in the design to toggle, when outputs of all the preceding flip flops are high. The first JK flip flop in the design toggles on every cock pulse and

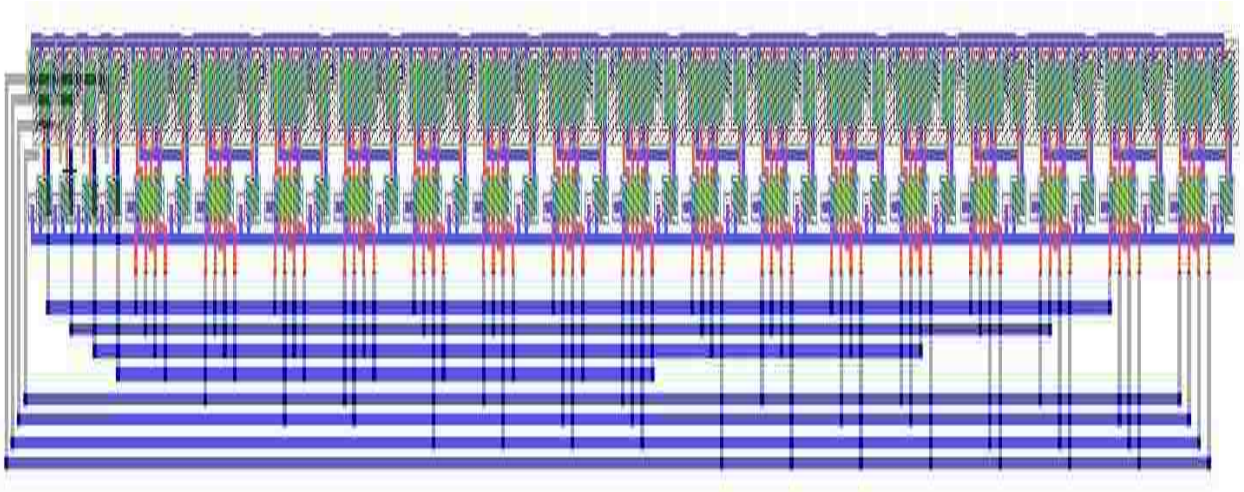

Figure 5.9. Layout of area optimized 4-to-16 decoder.

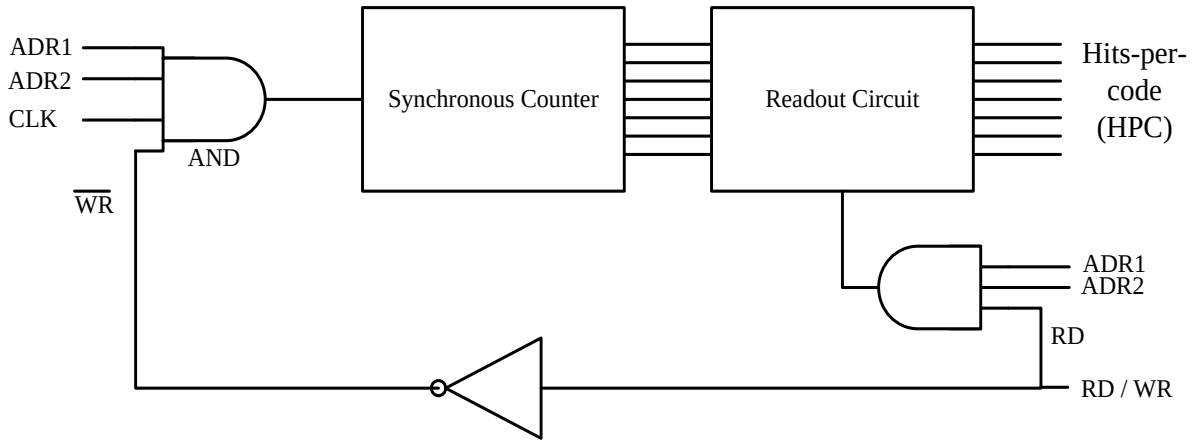


Figure 5.10. Block diagram of register using synchronous counter for CDU [14].

hence the J and K input are connected to $V_{DD}$ to have them high at all time. The second JK flip flop toggles only when Count0 (output of first JK flip flop) is high and hence the J and K inputs are connected directly to Count0. The other JK flip flop toggles when all the lower order output bits are high and hence use AND gates to set the J and K inputs. The layout of the 8-bit synchronous counter design implemented using JK flip flop is shown in Figure 5.12.

During the read process in the register, the count or HPC are fetched by enabling the readout circuit of the selected register in the register bank as explained earlier. The readout circuit design has been implemented using tri-state buffer as shown in Figure 5.13 [15]. The tri-state buffer is controlled by the signal $V_{rd}$ and is fed by the output of the AND gate whose inputs are ADR1, ADR2 and RD/WR. The complete layout of the implemented register design using synchronous counter for code detection unit (CDU) including the readout circuit is shown in Figure 5.14.

## 5.4 Results and Discussion

The on-chip testability of CMOS ADC using linear-ramp histogram technique comprising of the linear-ramp generator and the code detection unit were designed in 0.5 µm n-well CMOS process. Due to area constraint in the pad frame, the CDU is designed using an 8 X 1 register bank to test 3-bit ADC which can be expanded to 16 X 16 register bank as explained in the proposed design. The design was tested at the post-layout simulation and experimental stage. The chip layout of the on-chip linear-ramp histogram design is shown in Figure 5.15. The linear-ramp generator was simulated in the post-layout stage using Cadence® Virtuoso and the simulated output is as shown in Figure 5.16.

Concerning the linear-ramp generator, we obtain a very compact structure that occupies a small area of the complete layout (half of the area is used by the capacitor). The linear-ramp generator was also tested with an ideal ADC and the CDU to verify a flat histogram with very low values of INL and DNL. This also verifies the functionality of the code detection unit (CDU).

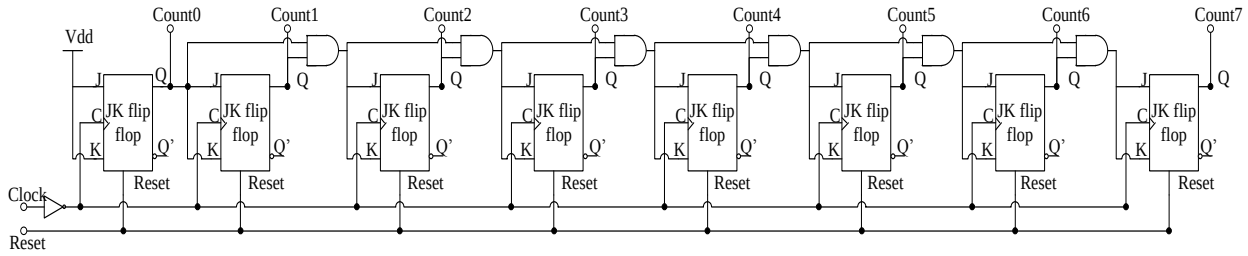


Figure 5.11. Schematic of 8-bit synchronous counter using JK flip flop [15].

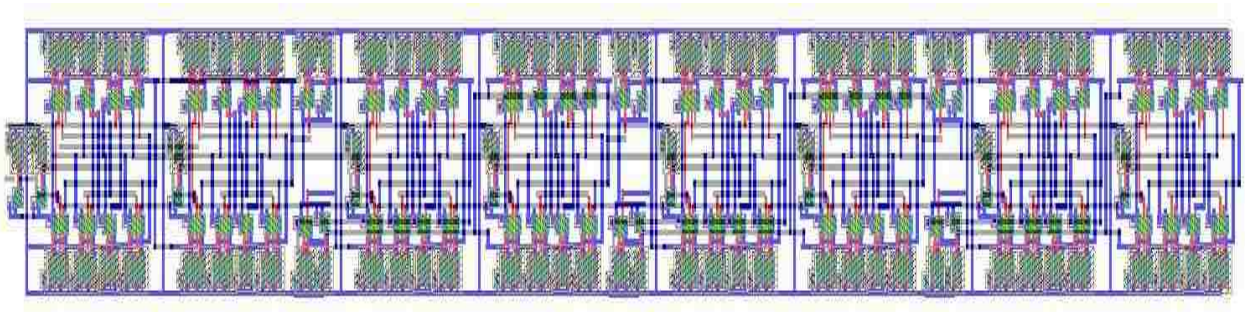

Figure 5.12. Layout of area optimized 8-bit synchronous counter using JK flip flop.

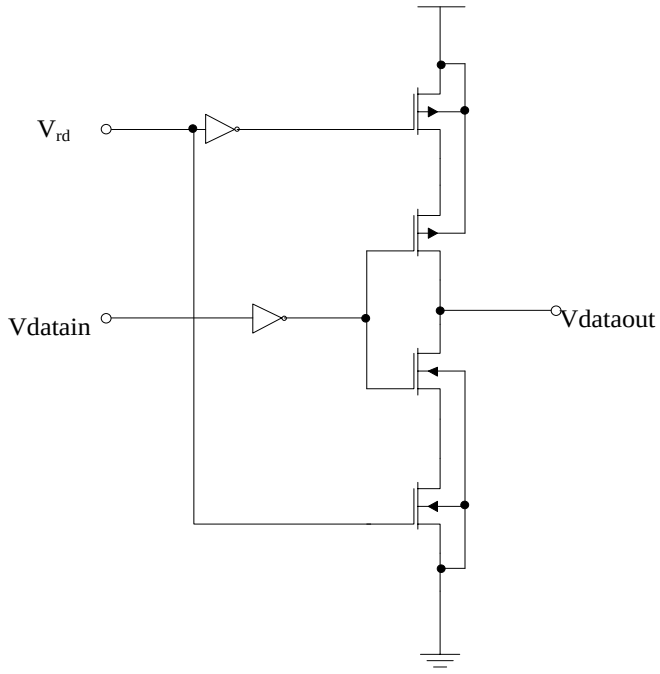


Figure 5.13. Schematic of readout circuit design [15].

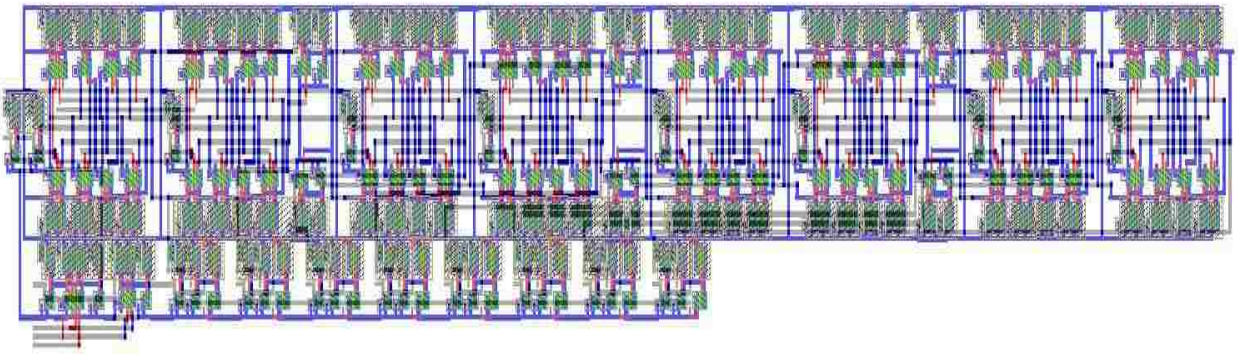

Figure 5.14. Layout of the implemented register design using synchronous counter.

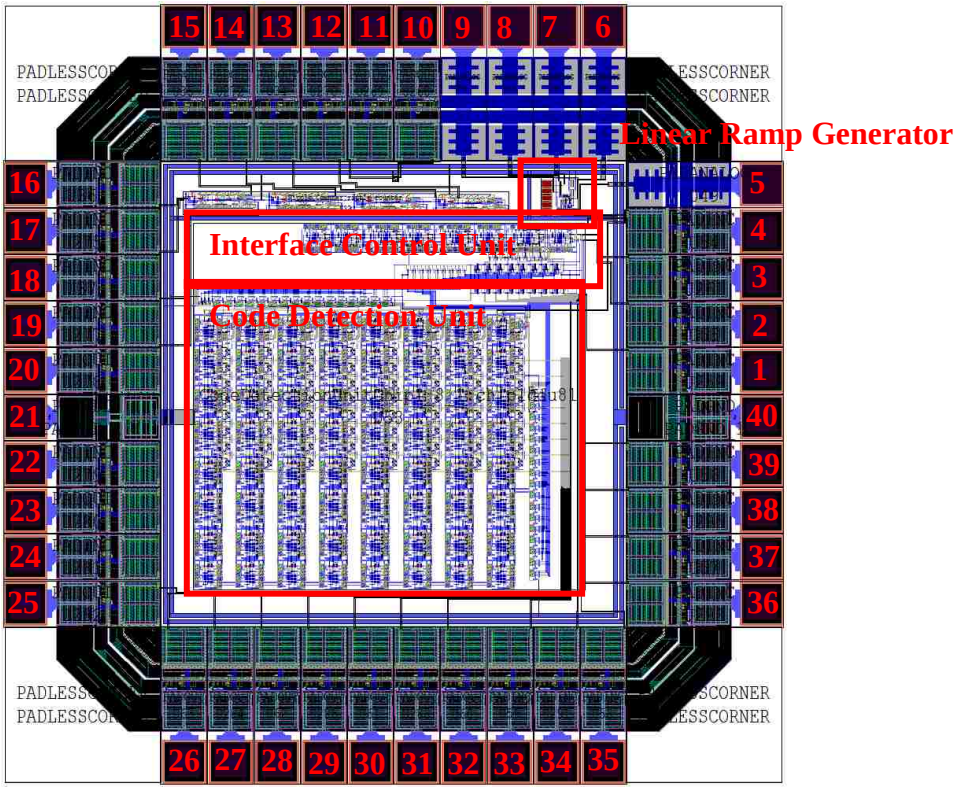


Figure 5.15. Chip Layout of on-chip testability of CMOS ADC using linear-ramp histogram technique.

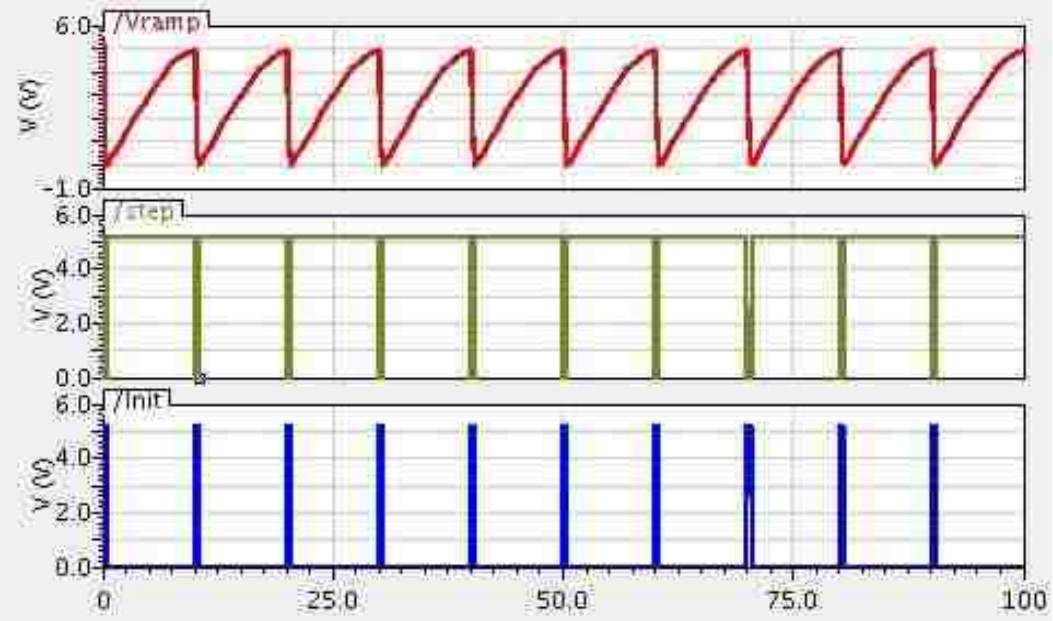


Figure 5.16. Simulation results for post-layout linear-ramp generator.

The code detection unit (CDU) was further experimentally verified using the fabricated chip with a 3-bit ADC as the CUT. The experimental setup is shown in Figure 5.17 and uses 3 most significant bits of 8-bit output from National Semiconductor ADC0804 with the linear ramp generator and code detection unit design fabricated. The test setup of Fig 5.17 is explained in detail in Appendix C.

The linear ramp histogram plot output obtained from the hits-per-code is shown in Figure 5.18. From the linear-ramp histogram, using the linear computation explained in Section IV, the various ADC static parameters for the 3-bit ADC are calculated. The experimental INL and DNL were then plotted for each ADC digital output code as shown in Figure 5.19. From the calculation and the plot, the INL and DNL are within ± 0.34609 LSB and ± 0.317804 LSB. The offset and gain error for the 3-bit ADC were also calculated and are within ±0.189684 LSB and ±0.001664 LSB.

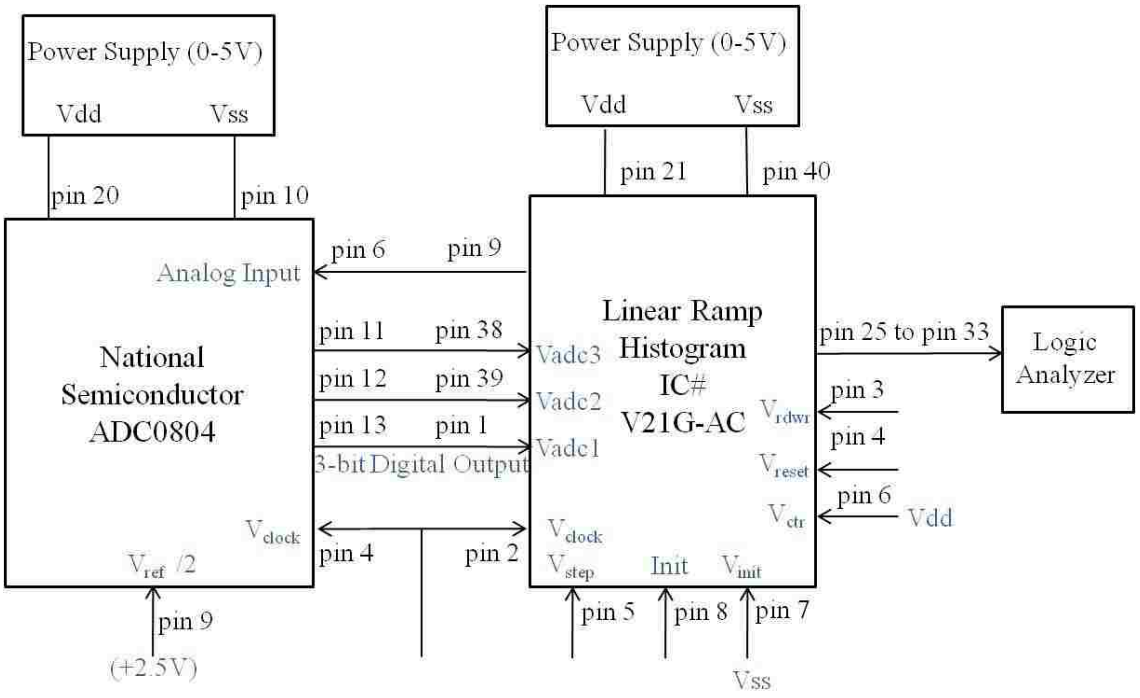


Figure 5.17. Experimental test setup for on-chip testability of CMOS ADC by linear ramp histogram technique using synchronous counter as register.

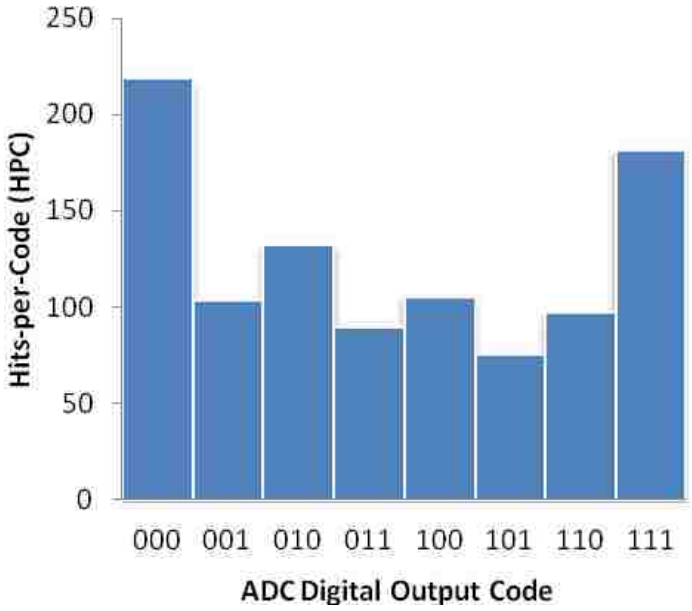


Figure 5.18. Experimental linear-ramp histogram plot for a 3-bit ADC.

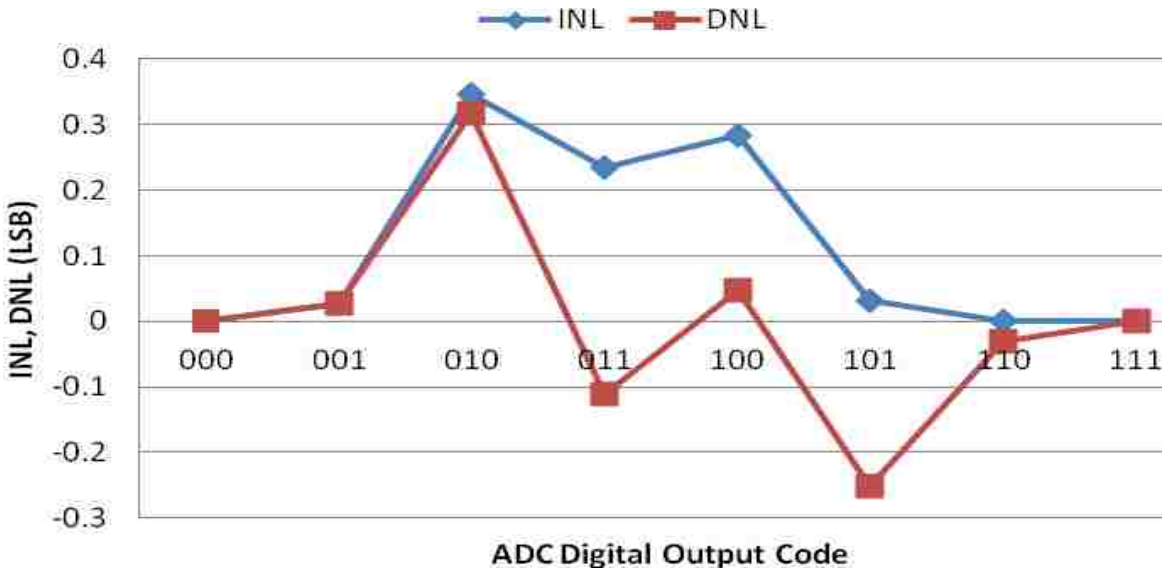


Figure 5.19. Experimental INL and DNL plot for 3-bit ADC calculated using on-chip linear-ramp histogram.

## 5.5 Conclusion

An efficient and low-cost design for complete on-chip testability of CMOS ADC using linear-ramp generator is proposed and designed in 0.5µm n-well CMOS process for deriving the static parameters like integral non-linearity (INL), differential non-linearity (DNL), offset voltage and gain error in terms of ADC's least significant bit (LSB). The linear-ramp generator is designed by charging a capacitor using a constant current and the post-layout simulation results are presented. The CDU is tested for functionality using a 3-bit ADC (National Semiconductor ADC0804) experimentally. On-chip 3-bit ADC could not be integrated in the fabricated design due to space limitation. The on-chip histogram technique can be used as an effective test technique which can reduce the test cost and time for calculating static parameters

of ADC. The technique can also be combined with the quiescent current testing to improve the fault coverage.

## 5.6 References


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# CHAPTER 6

# HARDWARE OPTIMIZED ON-CHIP FUNCTIONAL TESTABILITY OF CMOS ANALOG-TO-DIGITAL CONVERTERS BY LINEAR RAMP HISTOGRAM TECHNIQUE USING 6T-SRAM AS REGISTER

## 6.1 Introduction

In histogram based BIST approach, an input signal (either sinusoidal or linear ramp) is applied to the ADC input and the number of times each code appears, commonly known as hits-per-code (HPC) on the ADC output (code frequency statistics) is recorded. The HPC is then analyzed to derive the static parameters like integral non-linearity (INL), differential non-linearity (DNL), offset voltage and gain error in terms of ADC's least significant bit (LSB) [1, 2, 3]. The on-chip testability solution for CMOS ADC using the linear ramp histogram technique has been proposed, designed and fabricated in 0.5 μm n-well CMOS process in Chapter 5. In the design, the code detection unit (CDU) consists of synchronous counters designed using JK flip flops, used as registers or the on-chip memory to store the hits-per-code (HPC) for each unique code from the ADC digital output. The stored HPC are then fetched by the interface/control unit and used to compute the ADC parameter for the ADC tested. Due to area constraint, significant research has been carried out on optimizing [4-7] and hence in this work further optimization of area in the design by substituting the synchronous counters with 6T-SRAM (6 transistor SRAM design) as registers in CDU has been presented.

In this work, a design for area optimized on-chip linear ramp histogram technique for CMOS analog-to-digital converter using 6T-SRAM as registers is proposed and implemented. The proposed design is based on the on-chip linear ramp histogram technique for CMOS analog-

to-digital converter implemented in Chapter 5 [8] and reuses the linear ramp generator and interface/control unit while optimizing the code detection unit by using 6T-SRAM as registers. The code detection unit design and implementation using 6T-SRAM cells is explained in the Section 2. The design and implementation of the 6T-SRAM cell is also discussed in detail.

## 6.2 Code Detection Unit Design Implementation using 6T-SRAM

In the on-chip linear ramp histogram technique for CMOS ADC, the code detection unit is the major component and occupies most area in the circuit for testability implemented. As discussed in Chapter 5 and shown in Figure 5.7, the CDU consist of 16 X 16 register bank (with 256 or $2^8$ registers) to store the HPC for the 8-bit ADC and two 4-to-16 decoders to select the appropriate register on the register bank for the ADC digital output code [9-12]. In this design, 6T-SRAM cells are used to better optimize the design and reduce the area overhead for the test circuitry.

The 4-to-16 decoders in the CDU are used to select the appropriate register in the register bank to store or fetch the HPC for the ADC tested as explained earlier. The design implementation and functionality of the two 4-to-16 decoders in the CDU as discussed in detail in the Chapter 5 is reused for the design implementation of the CDU using 6T-SRAM. The lower 4 bits from the ADC are used in the first 4-to-16 decoder to produce the output address1 bit 0 to bit 15 (ADR1[0:15]) which is used as row selector and the higher 4 bits from the ADC are used in the second 4-to-16 decoder to produce the output address2 bit 0 to bit 15 (ADR2[0:15]) which is used as column selector. The 16-bit address1 and address2 are then used by the register bank

to select the appropriate register. The 4-to-16 decoders are used in both the read/write process to select the appropriate register in the register bank.

In the CDU during the write process, as explained earlier the ADC digital output code from the 8-bit ADC is used by the two 4-to-16 decoders and the appropriate register in the register bank is selected. After the register in the register bank is selected, the HPC is fetched, incremented and stored in the register for each occurrence of the ADC digital output code. During the read process, the interface/control unit selects the appropriate register to fetch the HPC stored in the respective register and use it for the computation of ADC parameters [12]. Hence during the read process, the 8-bits to the two 4-to-16 decoders are generated by the interface/control unit and the ADC is isolated from the CDU using multiplexers.

### 6.2.1 Register Design Implementation

The block diagram of the register used in the 16 X 16 register bank using 6T-SRAM is shown in Figure 6.1 and the design implementation consists of 8-bit 6T-SRAM to store the HPC for each occurrence of the ADC digital output code, precharge circuit, sense amplifier, column select MUX and read/write circuit [13]. The16-bit address1 (ADR1[0:15]) and address2 (ADR2[0:15]) from the two 4-to-16 decoders along with the read/write signal are used in the SRAM cell and the column select MUX to select the appropriate register (8-bit SRAM) in the register bank during the read or write process. During the write process the 8-bit ADC digital output is used by the two 4-to-16 decoders and the write enable signal by the read/write circuit to select the appropriate register and increment the content or HPC by 1 using an arithmetic circuit. This is achieved by fetching the HPC or register content of the selected appropriate register for

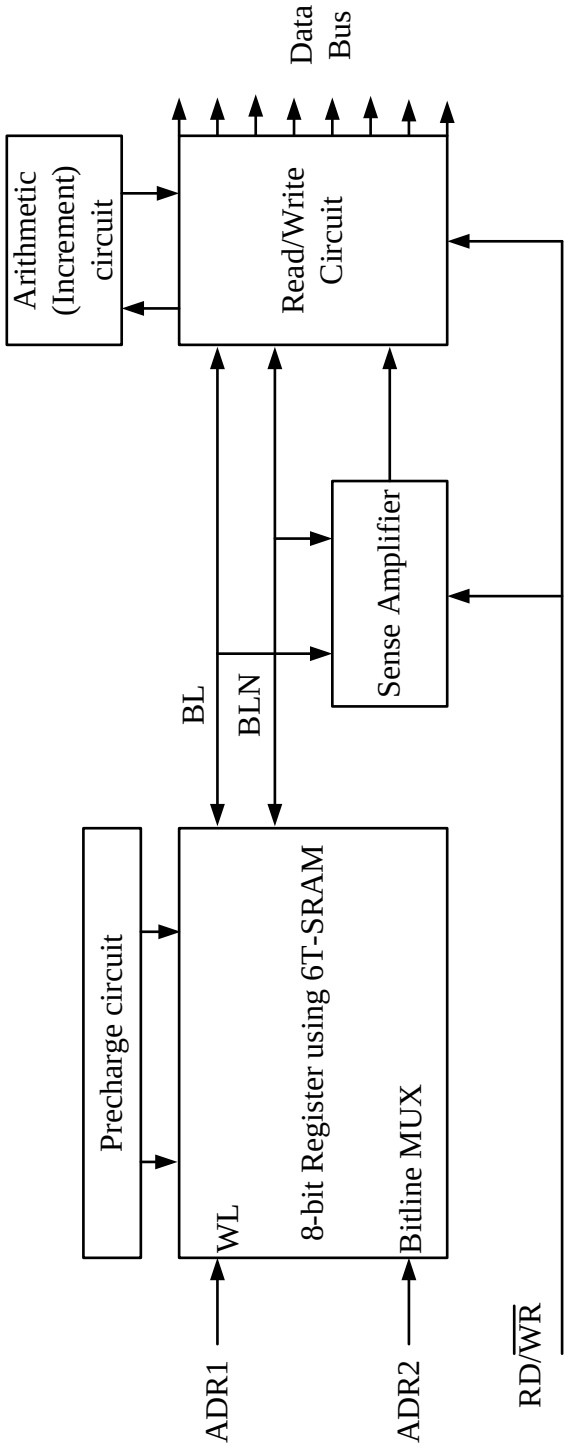


Figure 6.1. Block diagram of register using 6T-SRAM for CDU.

the ADC digital output and incrementing it by 1 in the arithmetic circuit and storing it back in the same register. Hence, the process of fetching the register content or HPC, incrementing and storing it back needs to be completed for each occurrence of the ADC digital output and is done by using the interface control unit and read/ write enable signal with twice the frequency of clock input. During the read process the interface/control unit generates the required 8-bit code which is used by the two 4-to-16 decoders and the read enable signal by the read/write circuit to select the appropriate register (8-bit SRAM) and fetch the contents or HPC stored in the selected register. During the read process a test enable signal is also used to isolate the arithmetic circuit from the register bank.

#### 6.2.1.1 6T-SRAM

The popular, full CMOS 6 transistor cell configuration was used to design the SRAM memory cell. Figure 6.2 shows the schematic of the 6T-SRAM cell [13]. The 6T-SRAM cell consists of two cross-coupled inverters connected with the two NMOS transistors on both ends. Each NMOS transistor is connected to an inverter on one side and bit line on the other side. The data value is stored in the net connected to the left side of the N3 NMOS in Figure 6.2. The inverse data value is stored in the net connected to the right side of the N4 NMOS in Figure 6.2. The input signal WL in the Figure 6.2 comes from the row decoder and allows the cell to be connected to the complementary bit lines during reading and writing and disconnects otherwise. Figure 6.3 shows the layout of the designed SRAM cell.

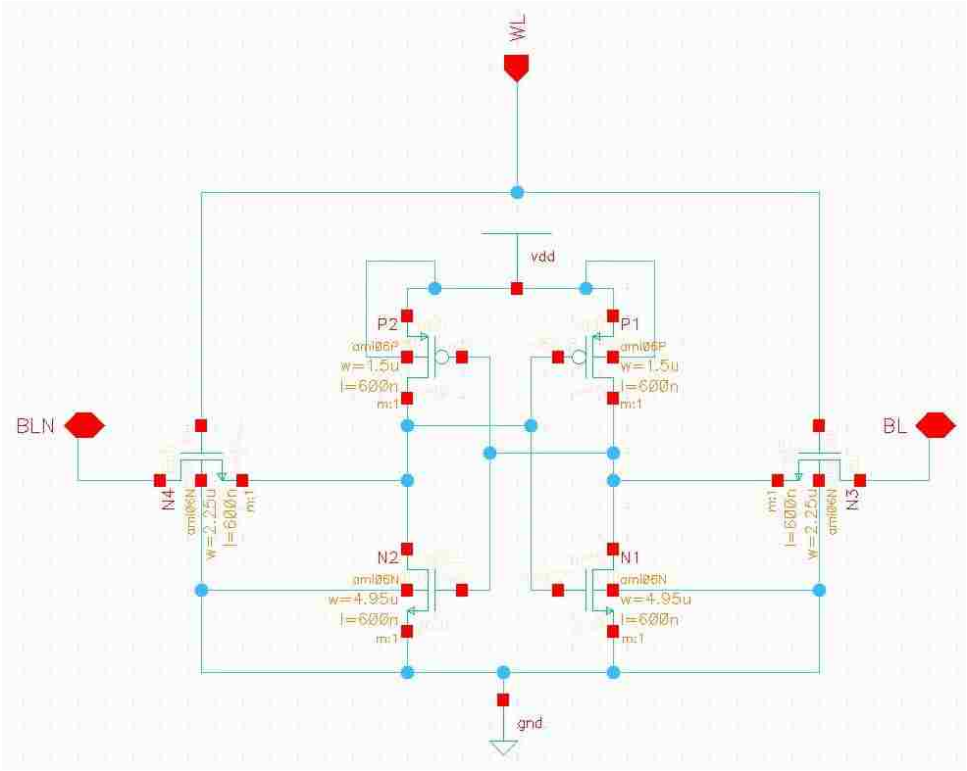


Figure 6.2. Schematic of a 6T-SRAM cell [13].

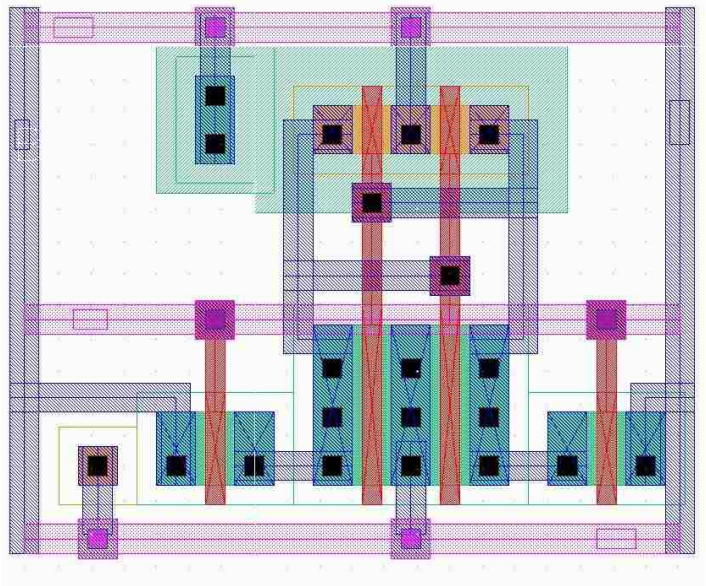

Figure 6.3. Layout of a 6T-SRAM cell.

#### 6.2.1.2 Precharge Circuit

The precharge circuit is designed to charge the bit-lines (BL) and inverse bit-lines (BLN) to 5V. The precharge enables the bit-lines to be charged high at all times except during the write and read cycle. Figure 6.4 shows the schematic of the precharge circuit [13]. In the precharge circuit the PMOS transistors are 1.5 µm each, the smallest width possible. Figure 6.5 shows the layout of the precharge circuit. In this design for the register bank, a precharge circuit was used for each column of SRAM cells.

#### 6.2.1.3 Sense Amplifier

To access data from the SRAM cells in the register, sense amplifier circuit is used. The sense amplifier also helps reduce the delay times and minimize power consumption in the overall SRAM register bank by sensing small difference in voltage on the bit lines (BL and BLN). The schematic of the sense amplifier used in this design is shown in Figure 6.6 [13]. A low-voltage sense amplifier was designed and implemented in the design to support high performance. In the register bank, 8 sense amplifier circuits are used, one for each bit in the registers (8-bit SRAM).

In the sense amplifier design, cross-coupled inverters are used to sense small changes in the voltage on the bit-line (BL) and inverse bit-line (BLN). The sense amplifiers are used in the register bank during the read operation of the 6T-SRAM cell to amplify the voltage coming off the two bit lines. Hence, in read cycle the read circuit and the sense amplifier are enabled and the cross-coupled inverters of the sense amplifiers sense the difference in voltage between the bit-line (BL) and inverse bit-line (BLN) thereby giving an output of 1 or 0 depending on the voltage levels sensed. The read circuit and the sense amplifier are isolated from the remaining circuit in

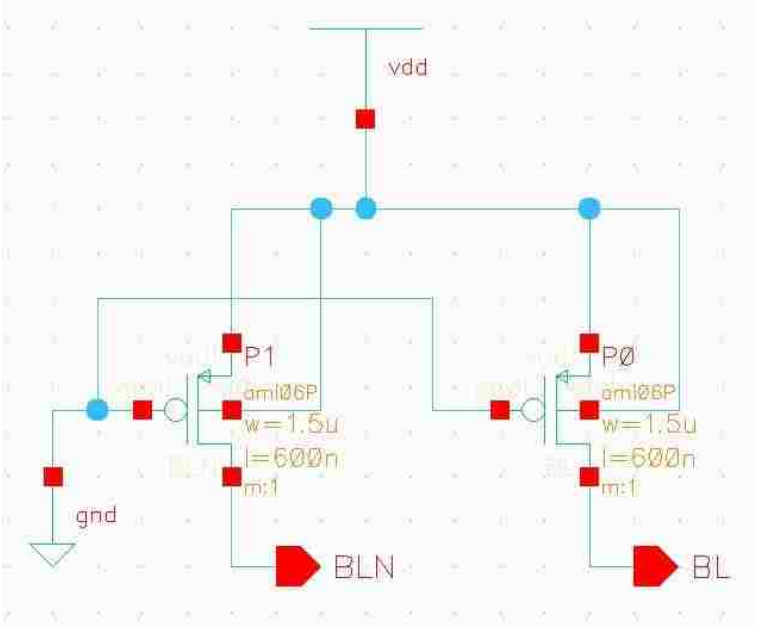


Figure 6.4. Schematic of the precharge circuit [13].

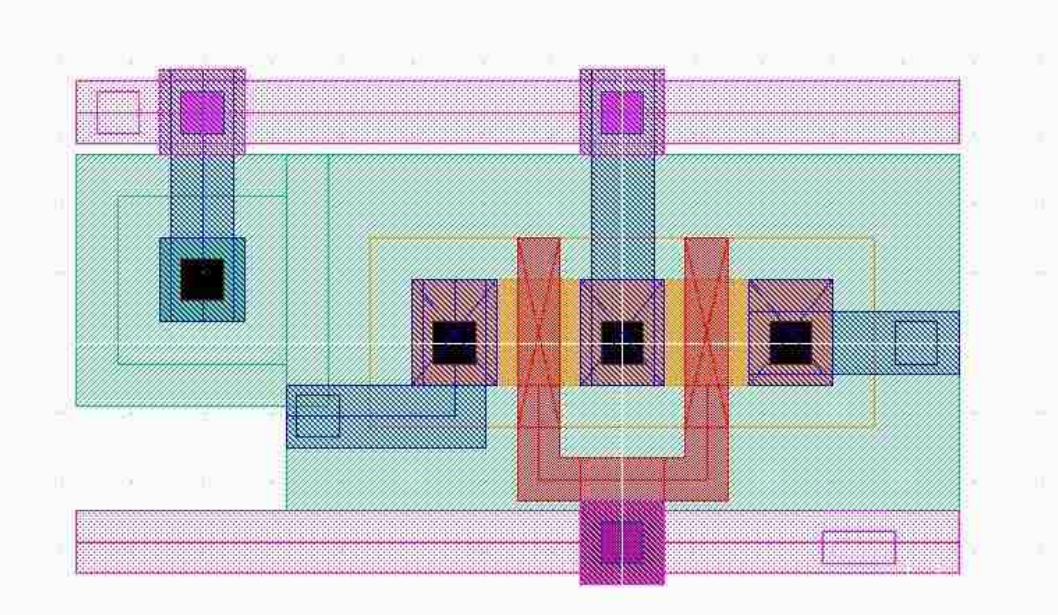

Figure 6.5. Layout of the precharge circuit.

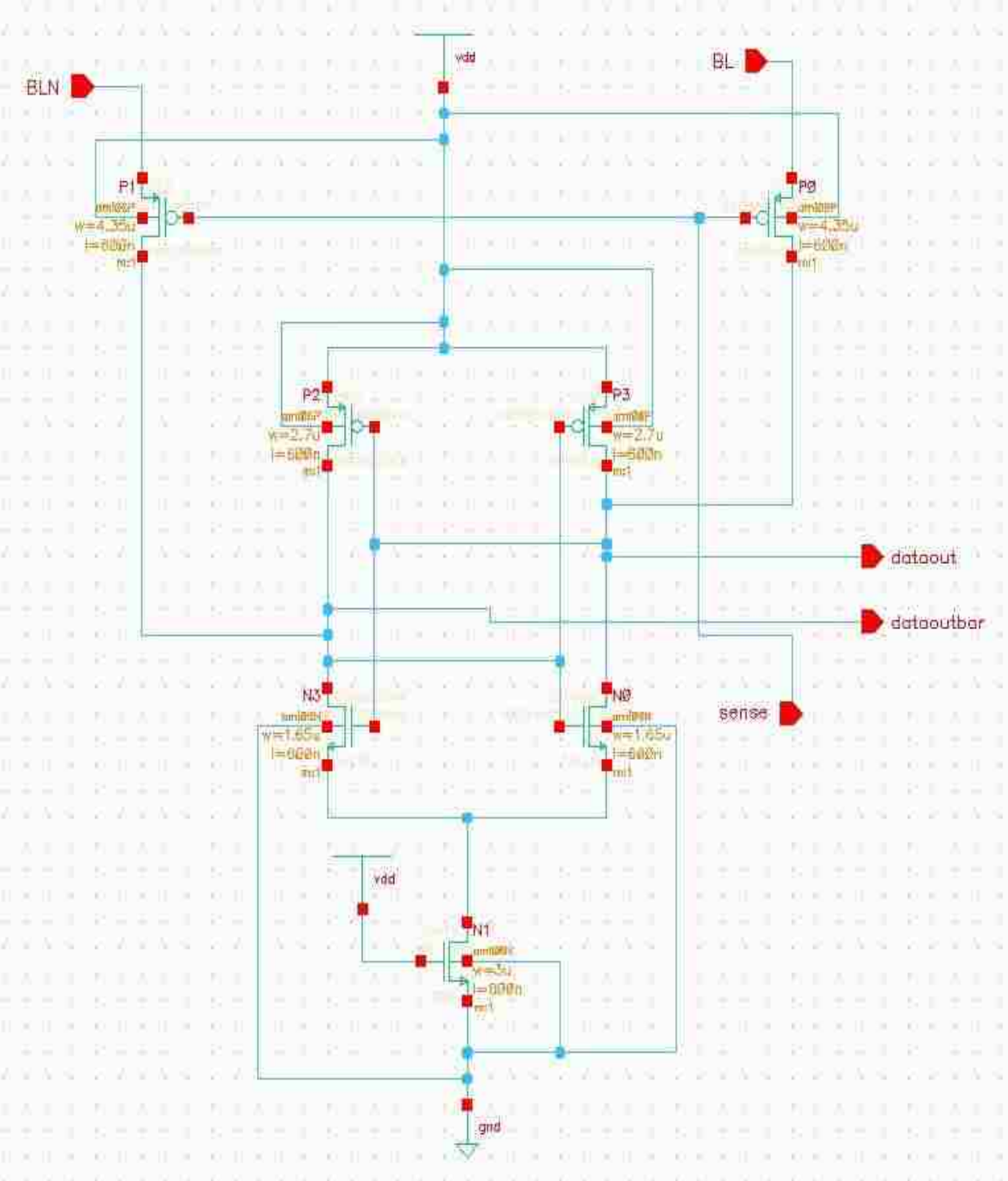


Figure 6.6. Schematic of sense amplifier circuit [13].

the register bank by using two PMOS transistors (P0 and P1) connected between the bit lines of the SRAM cells and the sense amplifiers and controlled by the sense signal. Figure 6.7 shows the layout of the sense amplifier. During optimization of the layout, care was taken to create optimized layout for each unit that can be easily interface with others. The distance between the two bit lines in each unit is same, so that the precharge circuit, SRAM cell and sense amplifier can be seamlessly interfaced.

#### 6.2.1.4 Read/Write Circuit

In this design, during read and write process the read/write circuit is used to either fetch the data from SRAM cells in the selected register or write the data to SRAM cells in the selected register and is shown in Figure 6.8 [13]. The read/write circuit is a peripheral circuit that has been implemented using tri-state buffers controlled by the read/write signal (Vrdwrbar) connected to the data bus to either put data on the data bus or read data from it. During write process, the write enable (Vrdwrbar = 0) is set and the data from the Vdatain is transferred to the data bus (Vdatabus) through a tri-state buffer and then transferred to the bit-lines (BL and BLN) of the selected register in the register bank through another tri-state buffer to store the data. The other tri-state buffer connecting the output (Vdataout) from the sense amplifier to the data bus is isolated. Meanwhile during the read process, the read enable (Vrdwrbar = 1) is set and the data from the sense amplifier output (Vdataout) is transferred to the data bus (Vdatabus) through a tri-state buffer. The other tri-state buffers connecting the Vdatain to the data bus (Vdatabus) and data bus (Vdatabus) to the bit-lines (BL and BLN) are isolated. The optimized layout of the designed read/write circuit is as shown in Figure 6.9.

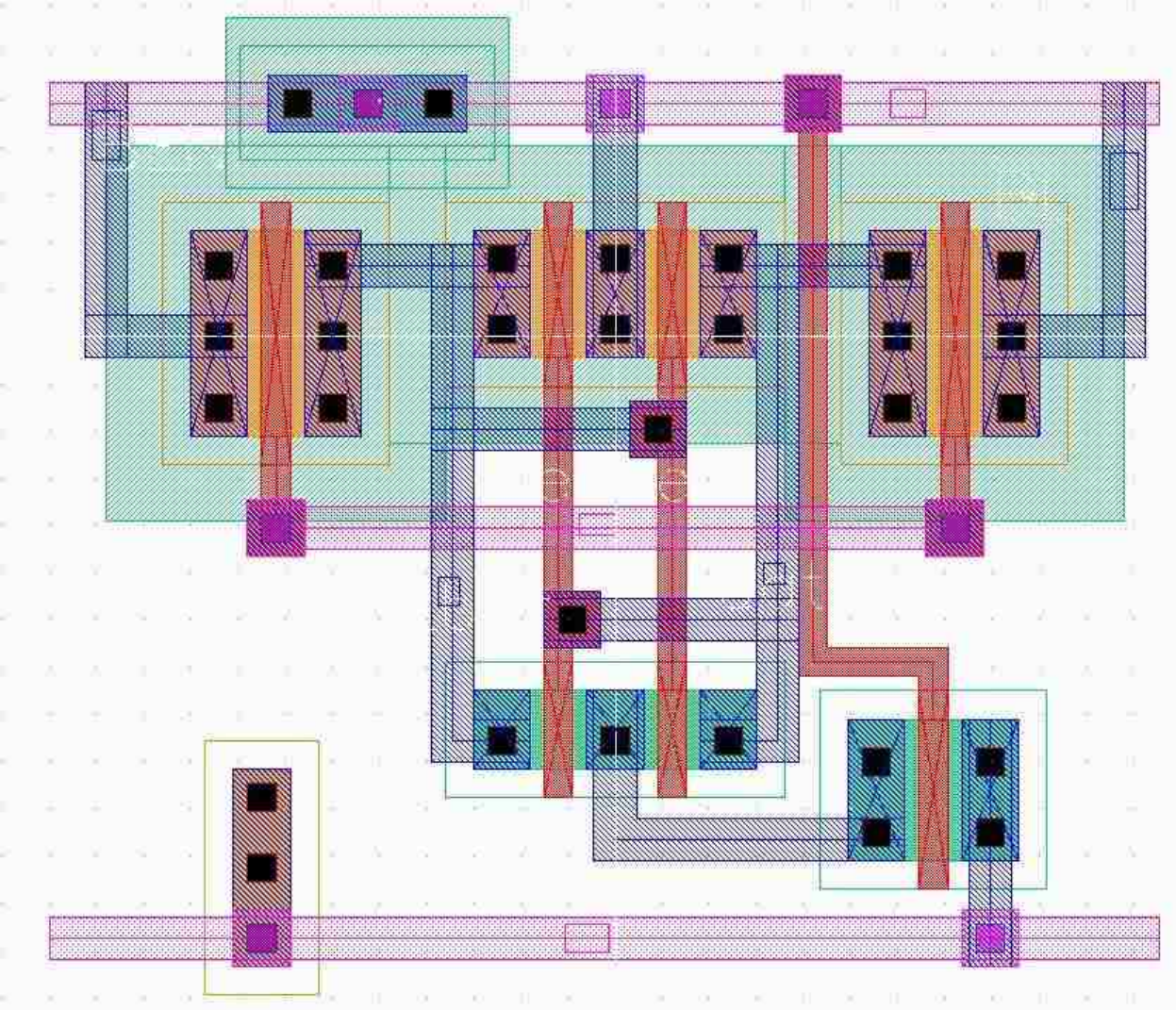

Figure 6.7. Layout of sense amplifier circuit.

6.2.1.5 Arithmetic Circuit

The arithmetic circuit used to increment the HPC in the CDU for each occurrence of the ADC digital output is designed using an area optimized binary full adder circuit. The area efficient design of the binary full adder is created with minimum number of transistors with optimization done at both logic level and the circuit level [13]. The binary full adder used for the

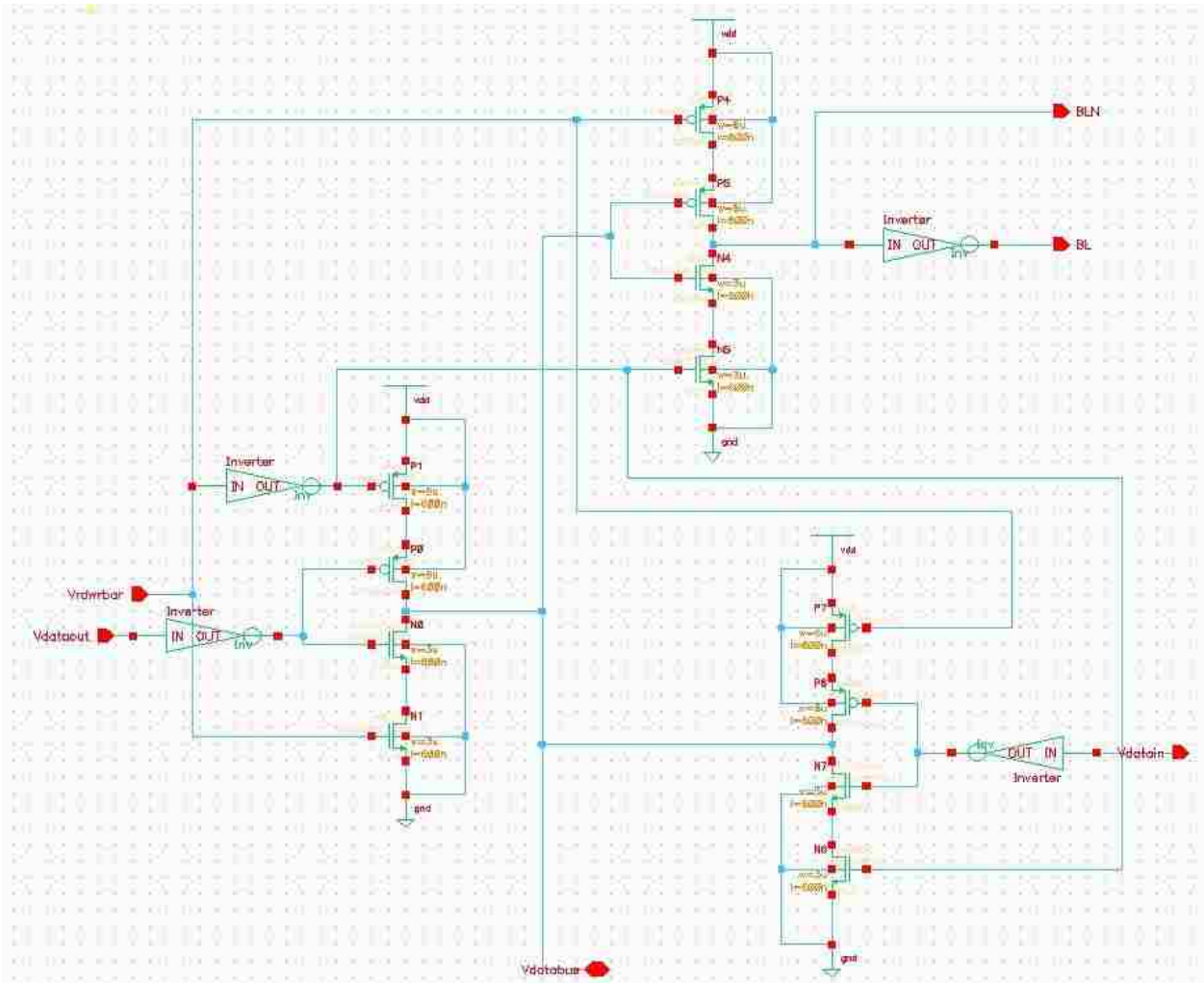


Figure 6.8. Schematic of read/write circuit [13].

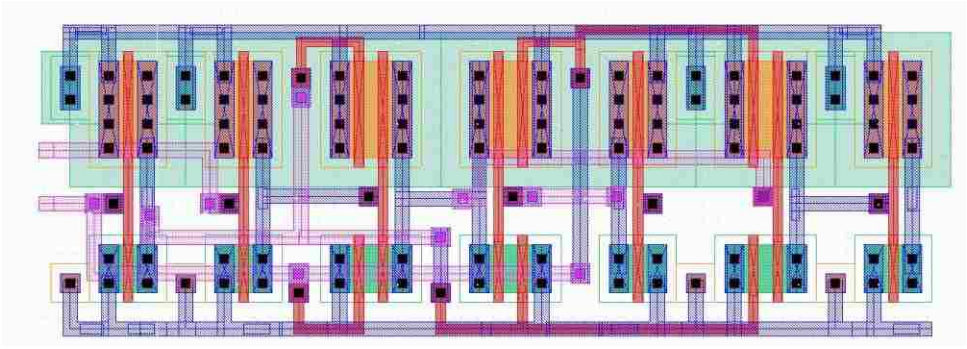

Figure 6.9. Layout of read/write circuit.

arithmetic circuit uses transmission gate and consist of a total count of 18 transistors. The schematic showing the sizing of the transistors in the binary full adder circuit is shown in Figure 6.10. The 8-bit arithmetic circuit is designed to increment by 1 by connecting the data from the register to input A, connecting input B to 0 and the carry out $C_{out}$ of the preceding significant bit adder is used as Carry in, $C_{in}$. The carry input for the least significant bit adder is taken as 1 to increment and the carry out for the most significant bit adder is ignored. The layout of the 8-bit arithmetic circuit designed to operate to increment by 1 is shown in Figure 6.11.

## 6.3 Results and Discussion

The on-chip testability of CMOS ADC using linear-ramp histogram technique using 6T-SRAM as registers comprising of the linear-ramp generator and the code detection unit were designed in 0.5 µm n-well CMOS process. Due to area constraint in the pad frame, the CDU is designed using a 4-to-16 decoder, a 3-to-8 decoder and a 16x8 register bank to test a 7-bit ADC which can be expanded to 16x16 register bank as explained in the proposed design and is shown in Figure 6.12.

The design was tested at the post-layout simulation and experimental stage. The chip layout of the on-chip linear-ramp histogram using 6T-SRAM design is shown in Figure 6.13. The linear-ramp generator designed in the earlier chapter and included in the current padframe was simulated in the post-layout stage using Cadence® Virtuoso and the simulated output is shown in Figure 6.14. The 6T-SRAM cell, sense amplifier, Read/Write circuit and CDU designed using 6T-SRAM were also simulated in the post-layout stage using Cadence® Virtuoso.

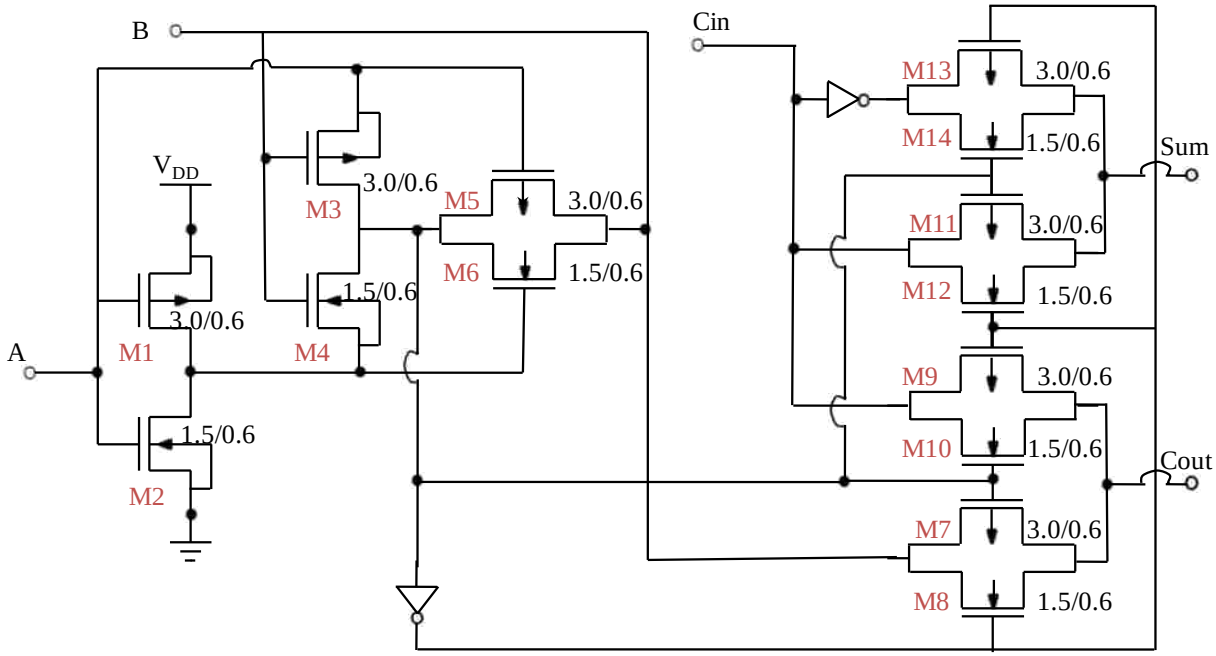


Figure 6.10. Schematic of 18 transistor binary full adder circuit [13].

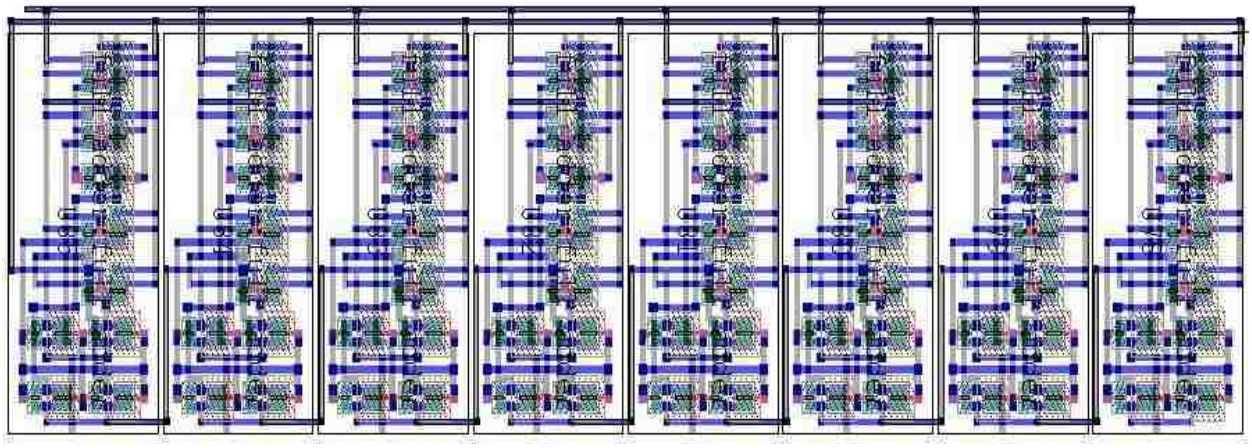

Figure 6.11. Layout of 8-bit arithmetic circuit designed using 18 transistor binary full adder circuits to operate as increment by 1.

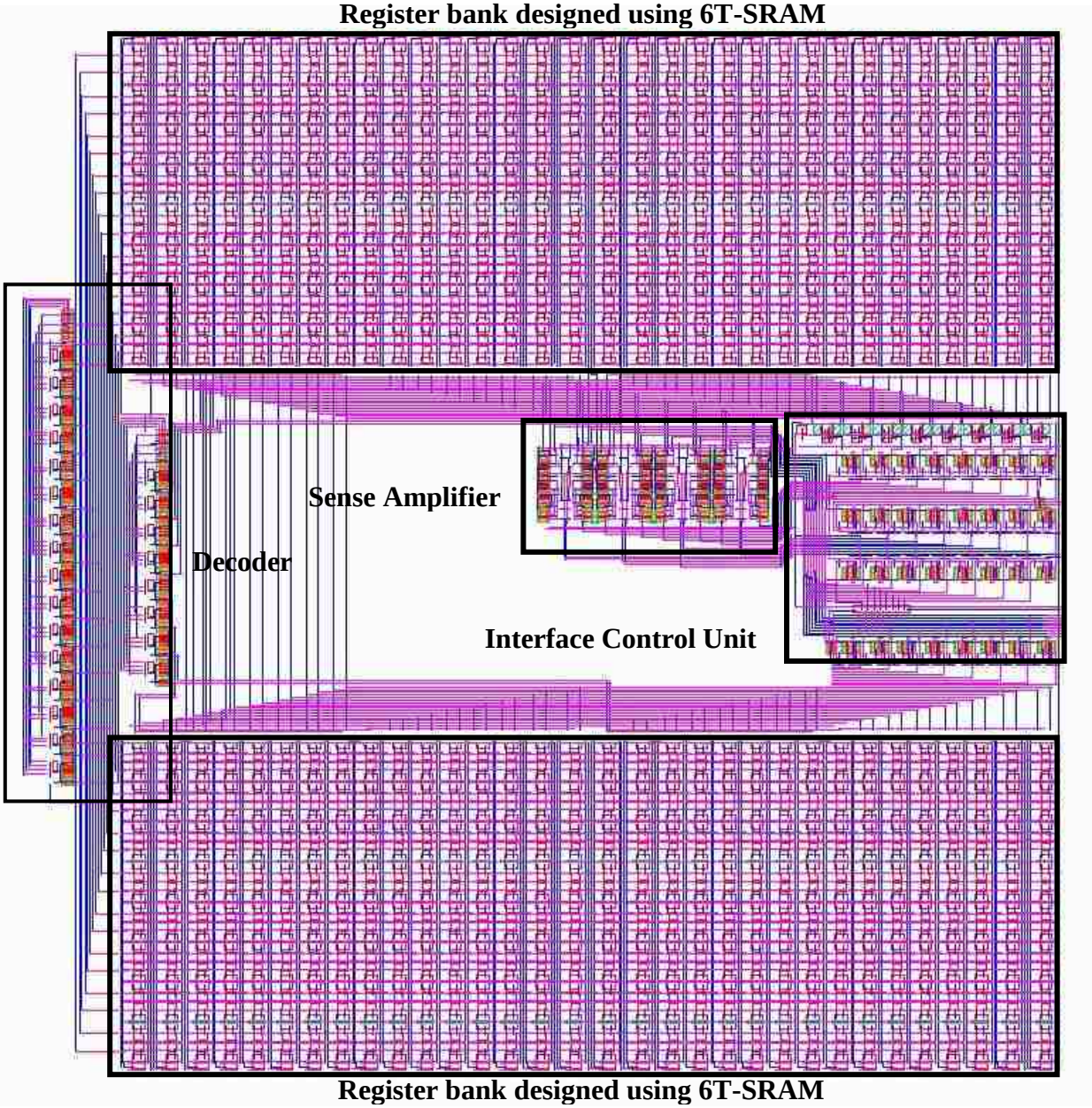


Figure 6.12. Layout of CDU consisting of16x8 register bank designed using 6T-SRAM for 7-bit ADC.

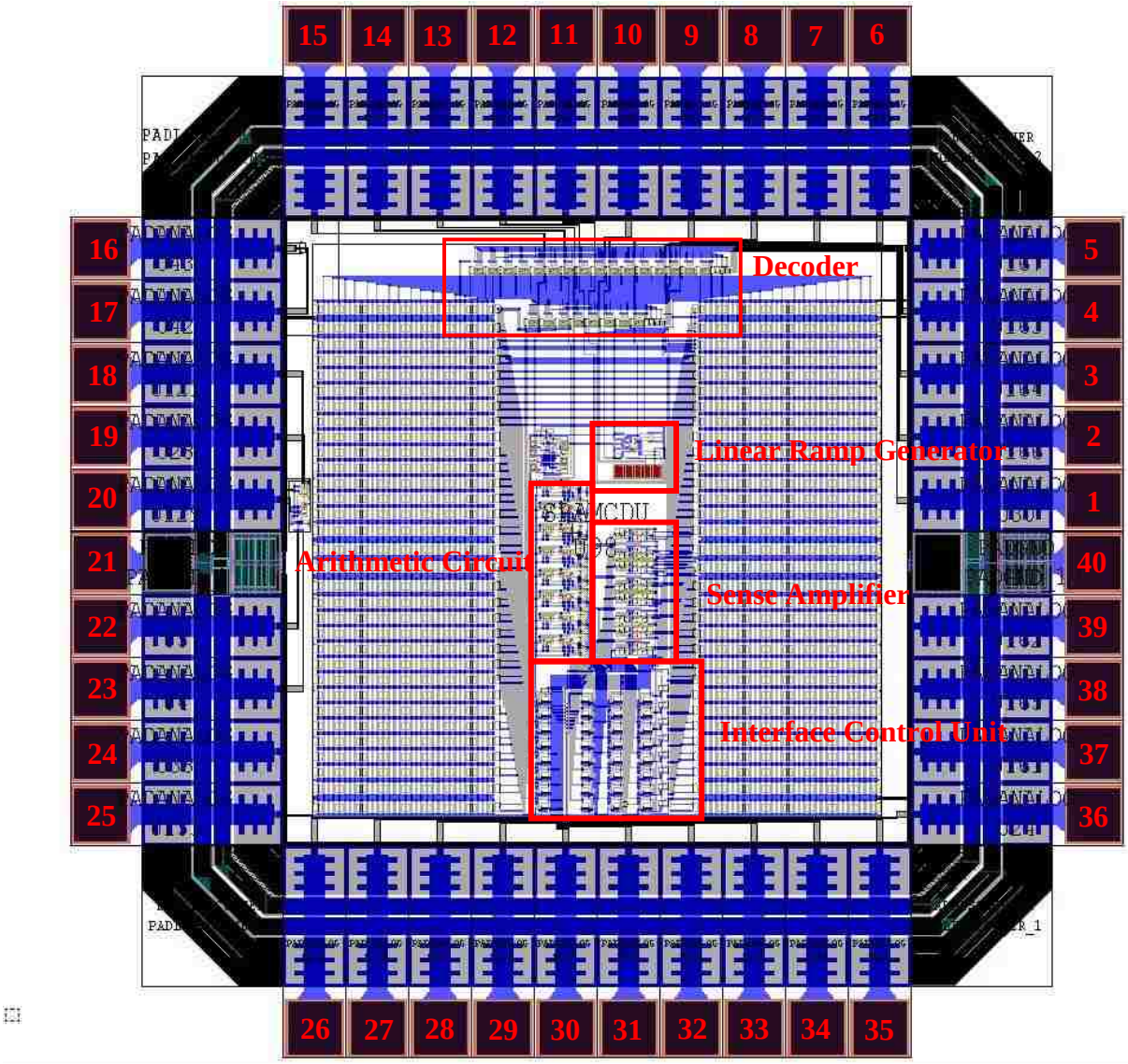


Figure 6.13. Chip Layout of on-chip testability of CMOS ADC using linear-ramp histogram technique using 6T-SRAM as registers.

The post-layout simulation result of 6T-SRAM cell is shown in Figure 6.15. In the 6T-SRAM cell, the data available on bit-lines (BL and BLN) are transferred to two cross-coupled inverters when input signal WL (enable) is high. The post-layout simulation result of sense amplifier is shown in Figure 6.16. When the PMOS transistors (P0 and P1) used to isolate the sense amplifier from the remaining circuit as shown in Figure 6.4 are enabled by using the control sense signal during the read process, the cross-coupled inverters in the sense amplifier amplify the voltage coming off the bit-lines. When BL is high, BLN is low and sense is low, the output is high or 1. Similarly when BL is low, BLN is high and sense is low, the output is low or 0. The post-layout simulation of the read/write circuit is also simulated and is shown in Figure 6.17. The data from the sense amplifier is transferred to the data bus (Vdatabus) during read process or the data that needs to be stored in the 6T-SRAM cell is transferred from the Vdatain to the data bus (Vdatabus) through a tri-state buffer and then transferred to the bit-lines (BL and BLN). The linear-ramp generator and the CDU were also tested with an ideal 7-bit ADC to verify a flat histogram with very low values of INL and DNL. This verifies the functionality of the code detection unit (CDU) designed using 6T-SRAM cells as registers.

## 6.4 Conclusion

A hardware optimized design for complete on-chip testability of CMOS ADC by linear ramp histogram technique using 6T-SRAM as register has been proposed and designed in 0.5µm n-well CMOS process for deriving the static parameters like integral non-linearity (INL), differential non-linearity (DNL), offset voltage and gain error in terms of ADC's least significant

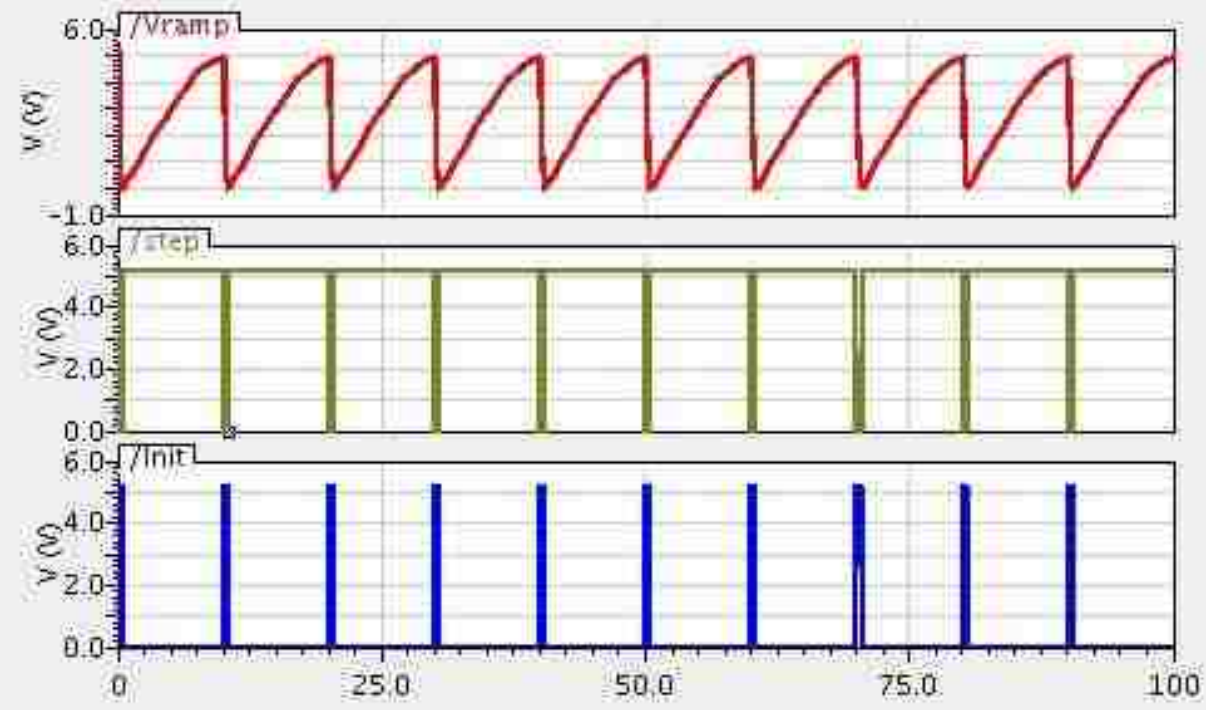


Figure 6.14. Simulation results for post-layout linear-ramp generator.

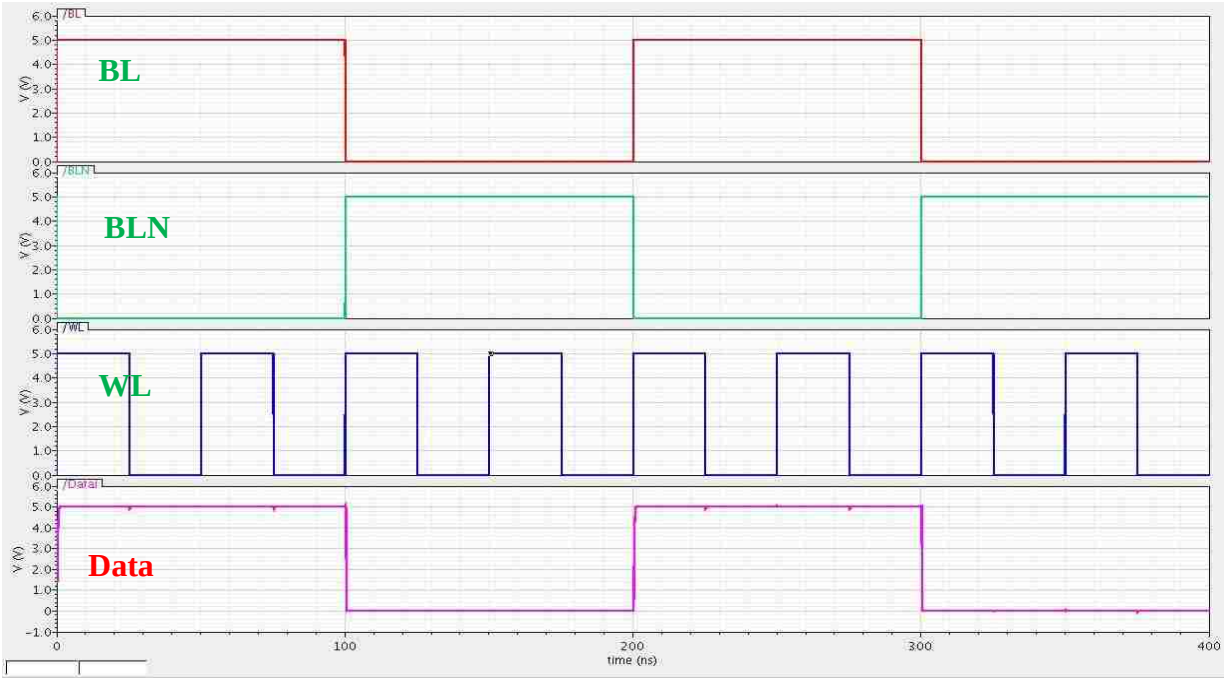


Figure 6.15. Simulation results for post-layout 6T-SRAM cell.

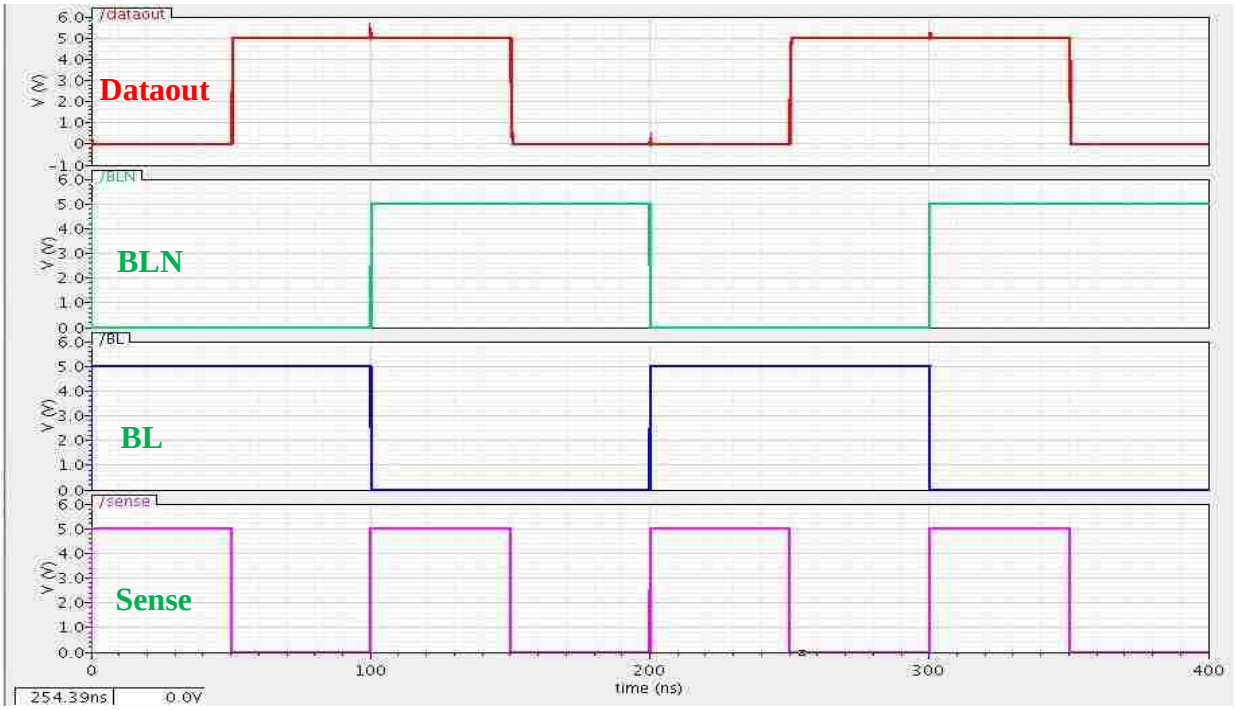


Figure 6.16. Simulation results for post-layout sense amplifier circuit.

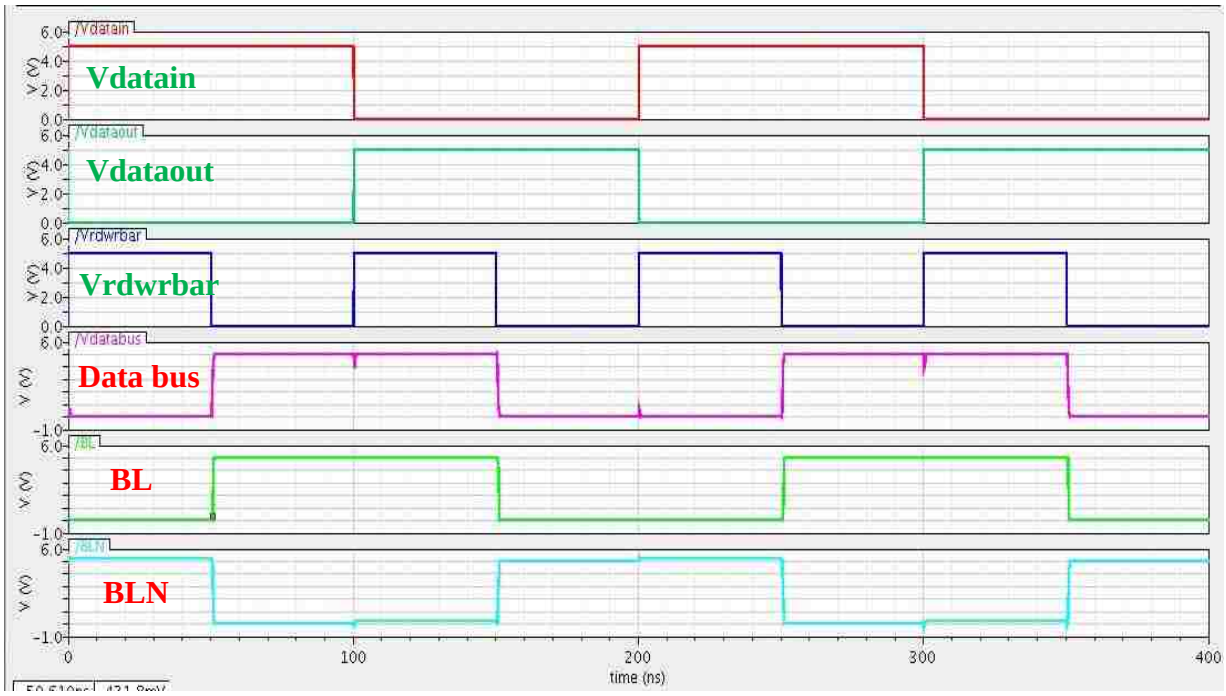


Figure 6.17. Simulation results for post-layout read/write circuit

bit (LSB). In this work, the registers in the code detection unit have been optimized and designed using 6T-SRAM instead of synchronous counter. The linear ramp generator, 6T-SRAM and the CDU are tested for functionality in the post layout stage using Cadence® Virtuoso. The on-chip histogram technique can be used as an effective test technique which can reduce the test cost and time for calculating static parameters of ADC. The technique can also be combined with the quiescent current testing to improve the fault coverage.

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# CHAPTER 7

# CONCLUSION AND SCOPE OF FUTURE WORK

## 7.1 Conclusion

The demand for mixed-signal System-on-Chip (SOC) has been growing steadily, fueling the development of compact and efficient systems by integrating digital, analog and mixed-signal circuits. In mixed-signal SOC, data converters are an integral part and are essential in interfacing the analog world of sensors and transducers with the digital world of signal processing and data handling. This presents difficulty since digital circuits use digital technologies that offer fast transistors biased at low voltages and they do not mix well with high precision analog circuits. Also, data (analog-to-digital) converters should consume a small amount of power since SOC circuits often target portable applications and should be resource efficient and noise tolerant. Analog-to-digital conversion based on delta-sigma ($\Delta\Sigma$) modulation offers an optimal solution as these trade resolution in time (bandwidth) for resolution in amplitude, so that low precision analog circuits can be used in the design.

In this research, a programmable second order oversampling CMOS delta-sigma analog-to-digital converter designed in 0.5 µm n-well CMOS processes using programmable cascaded integrator comb decimation filter is presented for integration in sensor nodes for wireless sensor networks. In this designed ADC, the output resolution depends directly on the oversampling ratio and the order of the modulator and the CIC decimation filter. By introducing programmability and reusing the integrators in the designed digital CIC decimation filter, the low-power energy efficient ADC can be operated at three different oversampling ratios of 16, 32 and 64 to give

three different resolutions of 9, 12 and 14 bits, respectively. This is made possible by using coder and clock divider circuits which work with enable signals to select the appropriate oversampling ratio for which the decimator has to be operated. In the sensor module, the resolution of the ADC has direct impact on energy consumption and hence by using the programmable ADC, the resolution can be programmed depending upon the need thereby impacting the power consumption. The signal-to-noise ratio (SNR), input dynamic range (DR), spurious free dynamic range (SFDR) and signal-to-noise distortion ratio (SNDR) are experimentally measured to be 75.6dB, 70dB, 72.3dB and 71dB at oversampling ratio of 64, 62.3dB, 58dB, 57dB and 55.5dB at oversampling ratio of 32 and 45.3dB, 45dB, 41.6dB and 40.4dB at oversampling ratio of 16. The designed programmable ADC can be operated with an oversampling clock frequency of up to 25 MHz.

Test cost for data converters and the need for faster and complex test equipments has increased, testing of data converters using BIST has been the focus of this research. We have developed and implemented a BICS for $\Delta I_{DDQ}$ based fault detection testing of CMOS data converters in 0.5µm n-well CMOS process. The designed BICS takes into account the increase in background current of defect-free circuits and also overcomes the effects of process variation. Process variation causes variation in quiescent current due to the change in threshold voltage and the effective leakage current in the CUT. The BICS uses frequency as the output for fault detection. The output frequencies of the BICS for various model parameters are simulated to check for the effect of process variation on the frequency deviation. The deviation of the output frequency of the BICS is observed to be less than ±10% for the model parameters and more than

±10% for various faults introduced in the data converter circuit using fault-injection transistors. In the designed work, the BICS is on-chip for better testability and higher testing speeds.

We have also designed and implemented a functional testing of CMOS ADC by using on-chip linear ramp histogram technique in 0.5µm n-well CMOS process. The CDU in the linear ramp histogram technique was designed using synchronous counter as register to store the hits-per-code for each occurrence of ADC digital output code. The design also includes an on-chip linear ramp generator which generates a linear ramp by charging a capacitor using a constant current. The HPC in the CDU are used to derive following static parameter of the ADC: integral non-linearity (INL), differential non-linearity (DNL), offset voltage and gain error in terms of ADC's least significant bit (LSB). The designed CDU was tested for functionality using a 3-bit ADC. The INL, DNL, offset and gain errors are experimentally calculated to be within ±0.34609 LSB, ±0.317804 LSB, ±0.189684 LSB and ±0.001664 LSB.

A design for hardware optimized on-chip functional testability of CMOS ADC by linear ramp histogram technique using 6T-SRAM as register is also been proposed and implemented in 0.5µm n-well CMOS process. The register in the code detection unit is optimized and designed using 6T-SRAM cell instead of synchronous counter. The CDU is designed using a 4-to-16 decoder, a 3-to-8 decoder and a 16 X 8 register bank to test a 7-bit ADC and the post layout simulation results have been presented.

## 7.2 Scope of Future Work

The designed programmable second order oversampling CMOS delta-sigma analog-to-digital converter can be interfaced with on- or off-chip CNT type nanosensors and other sensors

to implement a wireless sensor network for detection of traces of toxic gases and chemicals. CNT-FET inverter with metallic SWCNT interconnection exposed to thionyl chloride ($SOCl_2$) was characterized for sensing in our previous work and can be interfaced on- or off-chip with the programmable ADC depending upon the technology and compatibility with the CMOS technology in integration.

The designed BICS for $\Delta I_{DDQ}$ testing of CMOS data converters can be further extended to take into account the effects of reliability issues such as the hot carrier effects and negative bias temperature instability on testability. The BICS can also be extended to different mixed-signal circuits and can be used efficiently without affecting the functionality of the CUT. In the functional testing of ADC using on-chip linear ramp histogram technique, optimization at the hardware level can be improved to reduce the number of registers needed to store the HPC for the ADC.

# APPENDIX A

# SPICE MOS MODEL PARAMETERS FOR 0.5μm N-WELL CMOS TECHNOLOGY FROM MOSIS (http://www.mosis.com/)

## A.1 n-MOS Transistor Model Parameters

.MODEL NMOS NMOS (LEVEL = 7 VERSION = 3.1 TNOM = 27 TOX = 1.38E-8 XJ = 1.5E-7 NCH = 1.7E17 VTH0 = 0.6206755 K1 = 0.9154941 K2 = -0.1070065 K3 = 23.1322127 K3B = -10.118157 W0 = 2.578041E-8 NLX = 1.004874E-9 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 0.7455079 DVT1 = 0.3803402 DVT2 = -0.5 U0 = 454.9970557 UA = 1.178822E-13 UB = 1.468939E-18 UC = 8.099128E-12 VSAT = 1.980587E5 A0 = 0.6470937 AGS = 0.1501036 B0 = 1.922533E-6 B1 = 5E-6 KETA = -4.48048E-3 A1 = 3.937357E-5 A2 = 0.3 RDSW = 950.3826959 PRWG = 0.1146132 PRWB = 8.477104E-3 WR = 1 WINT = 2.512136E-7 LINT = 4.599276E-8 XL = 1E-7 XW = 0 DWG = -4.777866E-9 DWB = 2.160953E-8 VOFF = -9.792248E-5 NFACTOR = 0.9637953 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0 ETA0 = 2.059644E-3 ETAB = -2.60819E-4 DSUB = 0.0679985 PCLM = 2.189859 PDIBLC1 = 9.878026E-5 PDIBLC2 = 2.114418E-3 PDIBLCB = 0.0668401 DROUT = 2.351591E-3 PSCBE1 = 3.480502E8 PSCBE2 = 1.845207E-6 PVAG = 0 DELTA = 0.01 RSH = 80.9 MOBMOD = 1 PRT = 0 UTE = -1.5 KT1 = -0.11 KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9 UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 1.93E-10 CGSO = 1.93E-10 CGBO = 1E-9 CJ = 4.161289E-4 PB = 0.8283848 MJ = 0.4275867 CJSW = 3.259973E-10 PBSW = 0.8 MJSW = 0.1846732 CJSWG = 1.64E-10 PBSWG = 0.8 MJSWG = 0.2019414 CF = 0 PVTH0 = 0.0277539 PRDSW = 180.4529442 PK2 = -0.0767092 WKETA = -8.914329E-3 LKETA = -2.154684E-3)

## A.2 p-MOS Transistor Model Parameters

.MODEL PMOS PMOS (LEVEL = 7 VERSION = 3.1 TNOM = 27 TOX = 1.38E-8 XJ = 1.5E-7 NCH = 1.7E17 VTH0 = -0.9152268 K1 = 0.553472 K2 = 7.871921E-3 K3 = 8.9476091 K3B = 0.5321457 W0 = 1E-8 NLX = 1.004257E-9 DVT0W = 0 DVT1W = 0 DVT2W = 0 DVT0 = 0.4713552 DVT1 = 0.18506 DVT2 = -0.3 U0 = 201.3603195 UA = 2.48572E-9 UB = 1.005454E-21 UC = -1E-10 VSAT = 1.139712E5 A0 = 0.7835701 AGS = 0.120596 B0 = 8.005994E-7 B1 = 2.880961E-8 KETA = -4.865785E-3 A1 = 5.760921E-4 A2 = 0.5104845 RDSW = 3E3 PRWG = -0.0219752 PRWB = -0.0907724 WR = 1.01 WINT = 2.298706E-7 LINT = 9.979707E-8 XL = 1E-7 XW = 0 DWG = 2.212012E-9 DWB = -1.864478E-8 VOFF = -0.0484713 NFACTOR = 0.4480928 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0 ETA0 = 9.407653E-3 ETAB = -0.2 DSUB = 1 PCLM = 2.3394089 PDIBLC1 = 0.0769106 PDIBLC2 = 4.01984E-3 PDIBLCB = -0.0292094 DROUT = 0.2662061 PSCBE1 = 8E10 PSCBE2 = 8.957714E-8 PVAG = 0 DELTA = 0.01 RSH = 106 MOBMOD = 1 PRT = 0 UTE = -1.5 KT1 = -0.11 KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9 UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5 CGDO = 2.28E-10 CGSO = 2.28E-10 CGBO = 1E-9 CJ = 7.095753E-4 PB = 0.8613744 MJ = 0.4858698 CJSW = 2.182984E-10 PBSW = 0.8921837 JSW = 0.1908523 CJSWG = 6.4E-11 PBSWG = 0.8 MJSWG = 0.2261452 CF = 0 PVTH0 = 5.98016E-3 PRDSW = 14.8598424 PK2 = 3.73981E-3 WKETA = 9.043859E-3 LKETA = -0.0103186)

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[1] R. Soundararajan, A. Srivastava and J. Kamar, "A programmable second order oversampling CMOS sigma-delta analog-to-digital converter for wireless sensor networks," *Proceedings of the 12th International Conference on Information Technology (ICIT 2009)*, pp. 227-232, December 21-24, 2009.

From: Mohanty, Saraju <Saraju.Mohanty@unt.edu>
Date: Mon, Oct 22, 2012 at 1:30 PM
Subject: RE: Request for Copyright Permission for ICIT 2009
To: Rajiv Soundararajan <rsound1@tigers.lsu.edu>

Hi:

You have my approval for advancement of research.

Best Wishes,

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Saraju P. Mohanty, Ph. D.
Associate Professor, Dept. of CSE
Univ. of North Texas, Denton, TX 76203.
Email-ID: saraju.mohanty@unt.edu
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Fax: 1-940-565-2799.

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From: Rajiv Soundararajan [mailto:rsound1@tigers.lsu.edu]
Sent: Monday, October 22, 2012 12:09 PM
To: Mohanty, Saraju
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Dear Dr. Saraju Mohanty,

I am the co-author along with Dr. Ashok Srivastava for the following paper entitled "A programmable second order oversampling CMOS sigma-delta analog-to-digital converter for wireless sensor networks" published in Proceedings of the 12th International Conference on

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[2] R. Soundararajan and A. Srivastava, "A programmable second order oversampling CMOS sigma-delta analog-to-digital converter for low-power sensor interface electronics," *Proceedings of SPIE: Nano-, Bio-, and Info-Tech Sensors and Systems*, vol. 7646, pp. 7646P-1-7646P-11, March 7-11, 2010.

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Date: Wed, Oct 24, 2012 at 7:33 PM
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Sent: Tuesday, October 23, 2012 12:10 PM
To: Karen Thomas
Subject: FW: Request for Copyright Permission

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Sent: Monday, October 22, 2012 10:27 AM
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Subject: Request for Copyright Permission

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Thanks and Regards
Rajiv Soundararajan

[3] R. Soundararajan and A. Srivastava, “A programmable oversampling CMOS delta-sigma analog-to-digital converter for low-power interface electronics,” *Journal of Low Power Electronics*, vol. 8, No. 3, pp. 336-346(11), June 2012.

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Date: Tue, Oct 23, 2012 at 1:42 AM

Subject: Re: Request for Copyright Permission JOLPE Volume 8, Number 3 (June 2012)
To: Rajiv Soundararajan rsound1@tigers.lsu.edu
Cc: Patrick.Girard@lirmm.fr, saraju.mohanty@unt.edu

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Thanks and Regards
Rajiv Soundararajan

==========

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[4] R. Soundararajan, A. Srivastava and S. Yellampalli, "Process variation effects on $\Delta I_{DDQ}$ testing of CMOS data converters," *Proceedings of the 53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2010)*, pp. 284-287, August 1-4, 2010.

| | |
|---|---|
| **Title:** | Process variation effects on $\Delta I_{DDQ}$ testing of CMOS data converters |
| **Conference Proceedings:** | Circuits and Systems (MWSCAS), 2010 53rd IEEE International Midwest Symposium on |
| **Author:** | Soundararajan, R.; Srivastava, A.; Yellampalli, S.S. |
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[5] R. Soundararajan, A. Srivastava, and S. Yellampalli, "$\Delta I_{DDQ}$ testing of a CMOS digital-to-analog converter considering process variation effects," *Circuits and Systems*, vol. 2 No. 3, pp. 133-138, doi: 10.4236/cs.2011.23020, July 2011.

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Date: Mon, 22 Oct 2012 14:15:34 -0400
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Thanks and Regards
Rajiv Soundararajan

[6] A. Srivastava, and R. Soundararajan, "Testing of trusted CMOS data converters," *Proceedings of 2012 IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2012)*, pp. 350-355, August 19-21, 2012.

| | |
|---|---|
| **Title:** | Testing of Trusted CMOS Data Converters |
| **Conference Proceedings:** | VLSI (ISVLSI), 2012 IEEE Computer Society Annual Symposium on |
| **Author:** | Srivastava, A.; Soundararajan, R. |
| **Publisher:** | IEEE |
| **Date:** | 19-21 Aug. 2012 |

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# APPENDIX C

# TEST SETUP FOR ON-CHIP TESTABILITY OF CMOS ANALOG-TO-DIGITAL CONVERTER BY LINEAR RAMP HISTOGRAM TECHNIQUE USING SYNCHRONOUS COUNTER AS REGISTER

## C.1 Linear Ramp Generator

The test setup for the linear ramp generator in the fabricated design is as follows,

1. Connect Vdd (5V) to pin 21 and Vss (0V) to pin 40.
2. Connect **Vstep** (pin 5) to a pulse signal with voltage level 5V to 0V and time period 10µs or as needed by the test setup and duty cycle as low as possible. This allows the capacitor array to charge slowly and discharge as quickly as possible creating a linear ramp.
3. Connect **Vctr (**pin 6) to 5V supply or Vdd.
4. Connect **Vinit** (pin 7) to 0V supply or Vss.
5. Connect **Init** (pin 8) to a pulse signal with a voltage level of 0V to 5V and time period 10µs or as needed by the test setup and duty cycle as low as possible similar to step 2. This signal is used to initialize the capacitor array.
6. The frequency of the input should be carefully adjusted along with the input voltages to achieve a proper linear ramp output. The control of the input signal should be such that the linear ramp output covers the full scale range of the ADC to be tested.
7. The output of the linear ramp generator is achieved at pin 9.

## C.2 Linear Ramp Generator with 3-bit ADC and Code Detection Unit

The test setup for the linear ramp generator and the code detection unit designed in Chapter 5 with 3-bit ADC (National Semiconductor ADC0804) [1] is as follows,

1. Place the circuit under test (National Semiconductor ADC0804) and connect it according to the datasheet [1]. The output from the linear ramp generator is connected to the analog input (pin6) of the ADC. The 3 most significant bits (pin 11, pin 12, pin 13) of the 8-bit output are used as inputs to the code detection unit of the fabricated IC (pin 38, pin 39, pin 1). Our fabricated design described in Chapter 5 doesn't contain any ADC due to space limitation and only consist of a linear ramp generator and a code detection unit to register the HPC. Check the operation of the ADC to make sure it is working perfectly for the applied analog input.
2. Connect Vdd (5V) to pin 21 and Vss (0V) to pin 40 of the fabricated IC.
3. Connect the output of the ADC (pin 13, pin 12, pin 11) to the input pins (**Vadc1, Vadc2, and Vadc3**) of the fabricated IC. The MSB bit-3 (pin 11) of the ADC is connected to the **Vadc3** (pin 38), bit-2 (pin12) of the ADC is connected to the **Vadc2** (pin 39) and the LSB bit-1 (pin13) is connected to **Vadc1** (pin 1).
4. Connect **Vreset** (pin 4) to Vss (0V) supply to reset the circuit and then to Vdd (5V) for the normal operation of the CDU. This reset signal resets the JK flip-flop present in the CDU and doesn't control the linear ramp generator or the ADC. Hence the linear ramp input should take into account the reset signal for the proper number of linear ramp input to be sent to the ADC, so that the ideal hits-per-code of 128 is achieved.
5. Connect **Vrdwr** (pin 3) of the fabricated IC to a pulse signal from a function generator with voltage level of 5V to 0V. The pulse width, time period and the duty cycle are decided based on the linear ramp input and the time needed to read all the HPC from the CDU. During the

time when Vrdwr is ‘1’, the linear ramp is connected to the input of the ADC and the HPC are recorded in the CDU. Hence the time needed for the Vrdwr to be ‘1’ is dependent on number of linear ramp input selected, its frequency, sampling frequency of the ADC and other factors affecting the CDU to achieve an ideal HPC of 128. So we need to pay close attention in determining the time period and pulse width. Also when Vrdwr is ‘0’ the circuit is designed to readout the contents of the CDU counters to download the HPC recorded for the linear computation to be done externally. For this design this is determined by the 8 registers to be read and the time to read each register. The design has the in-built MUX which is controlled by the Vrdwr in activating the process of recording the HPC when each output digital code occurs in the ADC and in downloading the HPC for the manual linear computation of the static parameters using the HPC.

6. Connect **Vclock** (pin 2) of the fabricated IC to a pulse signal from a function generator. The frequency of the function generator is determined by the sampling frequency of the ADC, frequency of the input linear ramp, time spent at each code and ideal HPC count of 128. The pulse signal from the function generator is also connected to **Vclock** (pin4) of the CUT.
7. Using the downloaded HPC (pin 25 to pin 33) from the CDU we should be able to calculate the static parameters of the ADC.

## C.3 Reference

[1] National Semiconductor ADC0804 (ADC Single SAR 10ksps 8-bit Parallel 20-Pin PDIP Rail) datasheet URL - http://www.national.com/ds/AD/ADC0804.pdf

# VITA

Rajiv Soundararajan was born on May 21, 1979 in Dharapuram, Tiruppur, India. He received his M.S. in Engineering Science (Electronics) from Louisiana State University in December 2009, M.S. degree in Electrical Engineering from Arizona State University in May 2003 and B.S. (B.E.) degree in Electrical and Electronics Engineering from Barathiar University, India in April 2000. His research interest is in the area of digital, analog and mixed-signal VLSI design and testability. He is enrolled in the Division of Electrical and Computer Engineering, Louisiana State University, Baton Rouge, Louisiana since August 2004.