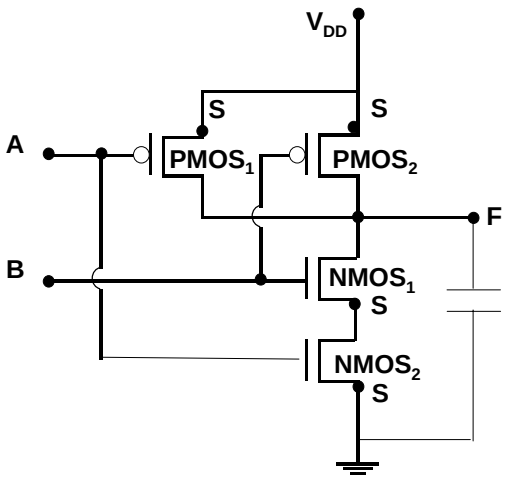
Lecture 24

Today we will

- Review charging of output capacitance (origin of gate delay)
- Calculate output capacitance
- Discuss fan-out
- Discuss “complementary” nature of CMOS

ORIGIN OF GATE DELAY



When the inputs A and B change such that the output F changes,

the output cannot change instantaneously; the output capacitance must be charged or discharged.

This is GATE DELAY.

REVIEW: PULL-DOWN DEVICES

In our logic circuits, the NMOS transistors have

- Gate terminal connected to V_{IN}
- Source terminal connected to ground directly, or through another NMOS

This means

- When **V_{IN}** is **high**, **NMOS** transistors are "**on**". They help **pull-down** V_{OUT} to ground, by conducting current to discharge the output capacitance.
- When **V_{IN}** is **low**, **NMOS** transistors are "**off**". They act as open circuits from source to drain.

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REVIEW: PULL-UP DEVICES

In our logic circuits, the PMOS transistors have

- Gate terminal connected to V_{IN}
- Source terminal connected to V_{DD} directly, or through another PMOS

This means

- When **V_{IN}** is **low**, **PMOS** transistors are "**on**". They help **pull-up** V_{OUT} to V_{DD}, by conducting current to charge the output capacitance.
- When **V_{IN}** is **high**, **PMOS** transistors are "**off**". They act as open circuits from source to drain.

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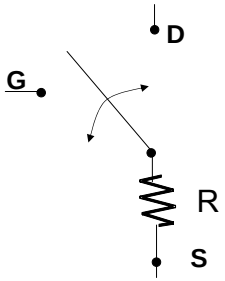
REVIEW: MODEL FOR GATE DELAY ANALYSIS

There is a model for the behavior of transistors in a CMOS logic circuit to analyze charging/discharging of the output capacitance.

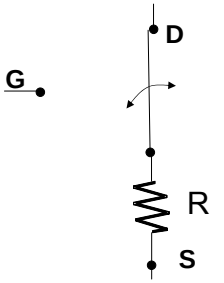
$V_{IN} = 0$ (for NMOS)
$V_{IN} = V_{DD}$ (for PMOS)



The resistance R is the effective resistance for the device during the first half of the transition.

Each device can have different R!

$V_{IN} = V_{DD}$ (for NMOS)
$V_{IN} = 0$ (for PMOS)



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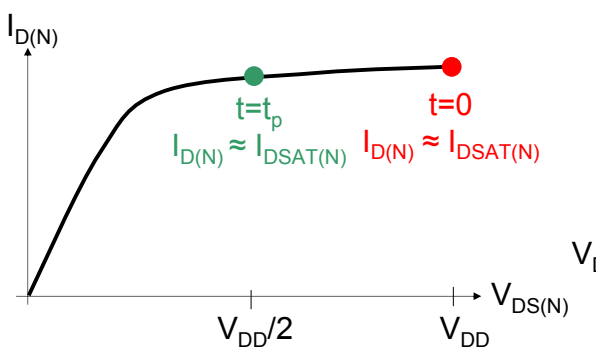
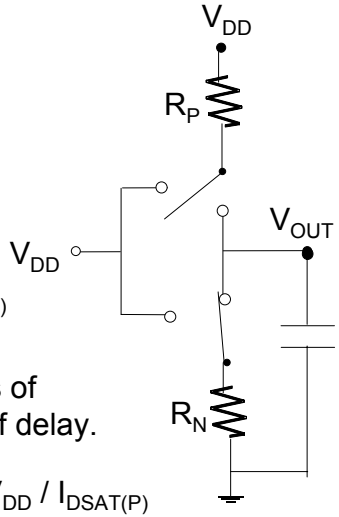
REVIEW: CALCULATING EFFECTIVE RESISTANCE

Consider pull-down, when V_{OUT} must go from V_{DD} to 0 V.





We calculate R_N by averaging the values of $V_{DS(N)}/I_{D(N)}$ at the beginning and ending of delay.

$R_N = \frac{3}{4} V_{DD} / I_{DSAT(N)}$ $R_P = -\frac{3}{4} V_{DD} / I_{DSAT(P)}$

CALCULATING OUTPUT CAPACITANCE

Two major sources of capacitance:

1. The transistor gates in the next stage
2. The metal connection to the next stage

Both can be computed using the parallel plate capacitor formula:

$$C = A\frac{k\,\varepsilon_0}{d}$$

A is the area of the plates,
k is the dielectric constant of the insulator in between the plates,
e_0 is the permittivity of free space, and
d is the distance in between the plates.

We denote $C_{OX} = \frac{k\,\varepsilon_0}{d}$ since this is fixed by fabrication process.

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CALCULATING OUTPUT CAPACITANCE

Each transistor gate terminal attached to the output contributes a gate capacitance

$$C_G = W\,L\,C_{OX}$$

where W and L are the channel dimensions and C_{OX} is the capacitance of the gate per unit area (parameters from I_D vs. V_{DS}).

Each metal connection at the output contributes a capacitance also given by the parallel plate capacitor formula, but with different length, width, and capacitance per unit area.

$$C_I = W_I\,L_I\frac{k\,\varepsilon_0}{d} = W_I\,L_I\,C_{OX(I)}$$

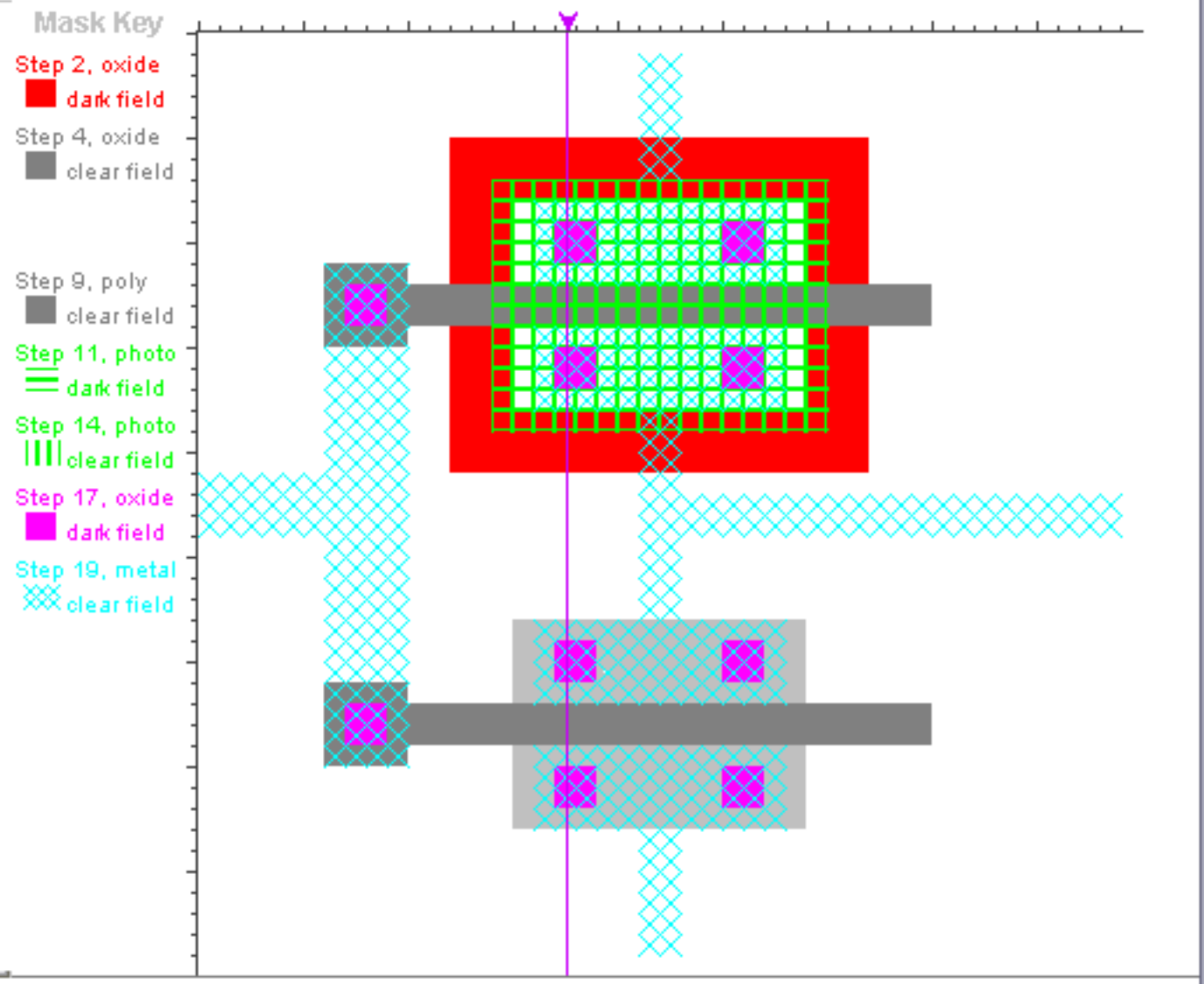
SIMPLer

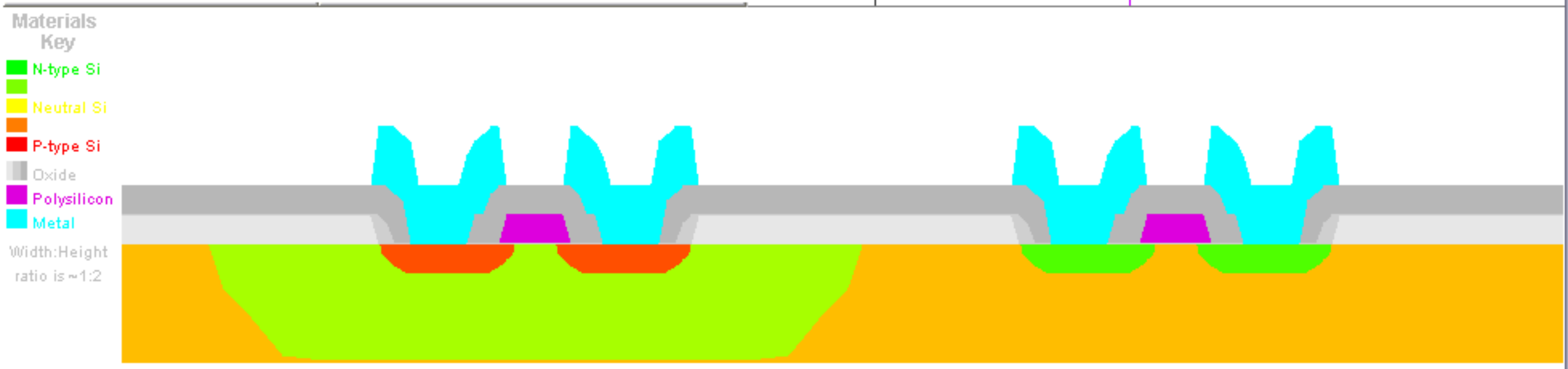
File Options

The purple color represents polysilicon, a conductor, which serves as the gate connection.

The gate is deposited early in the process, and polysilicon withstands the heat involved in the fabrication steps to follow.

Notice the very thin oxide layer separating the gate from the substrate.





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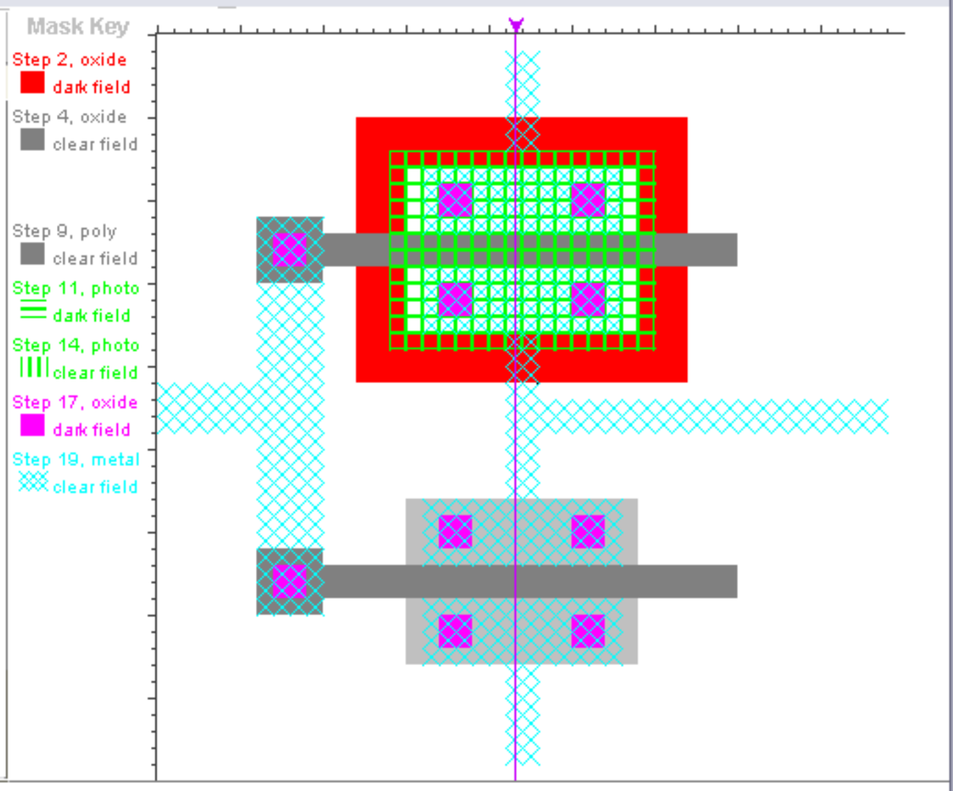
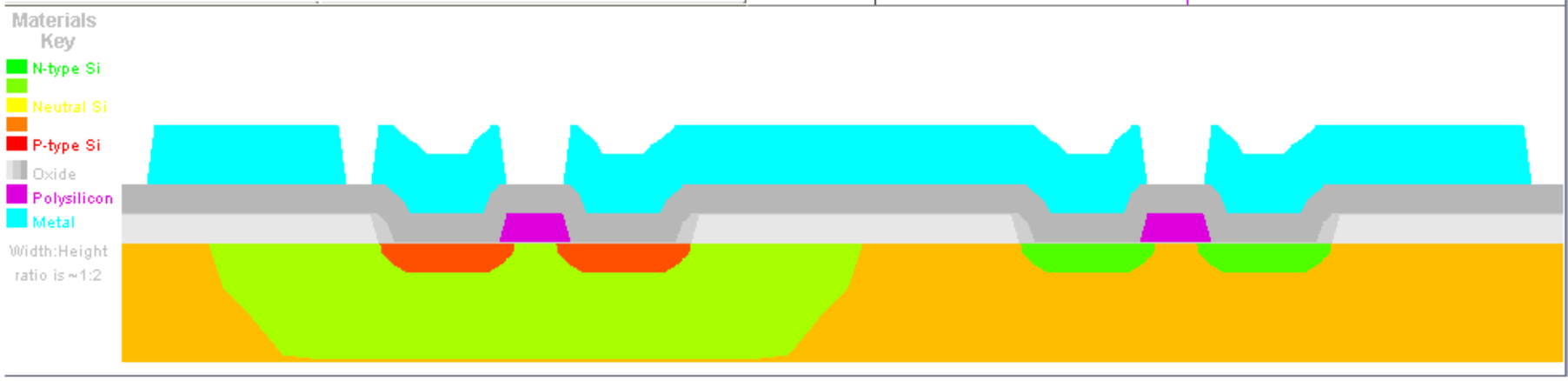
This cross-section shows the metal connection (aqua) between inverter transistors.

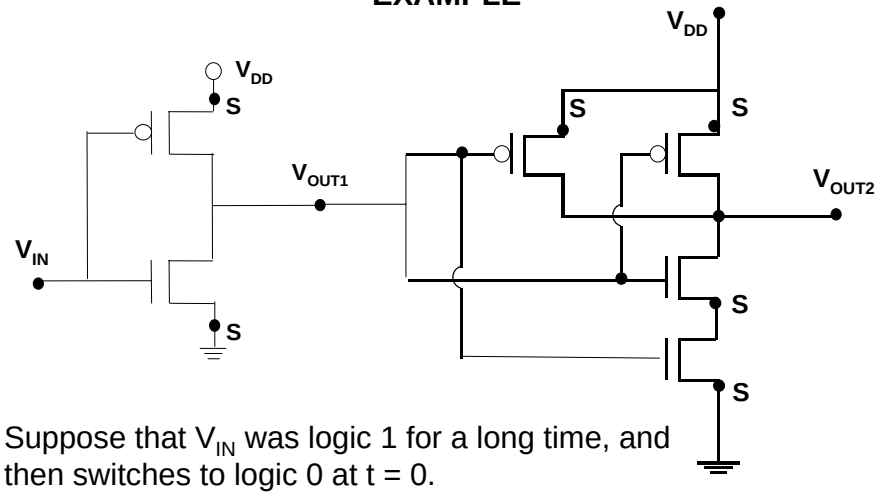
The metal is separated from the silicon substrate by a layer of oxide insulator.

This is a source of output capacitance.





EXAMPLE



Suppose that V_{IN} was logic 1 for a long time, and then switches to logic 0 at t = 0.

Find the propagation delay through the inverter.

EXAMPLE

Use

V_{DD} = 5 V

$V_{TH(N)} = -V_{TH(P)}$ = 1 V

C_{OX} = 5 fF/μm² for both transistors

L = 2 μm for both transistors

W = 2 μm for both transistors

λ = 0 for both transistors

μ_N= 50000 mm² / (V s)

μ_P= 25000 mm² / (V s)

W_l = 2 μm

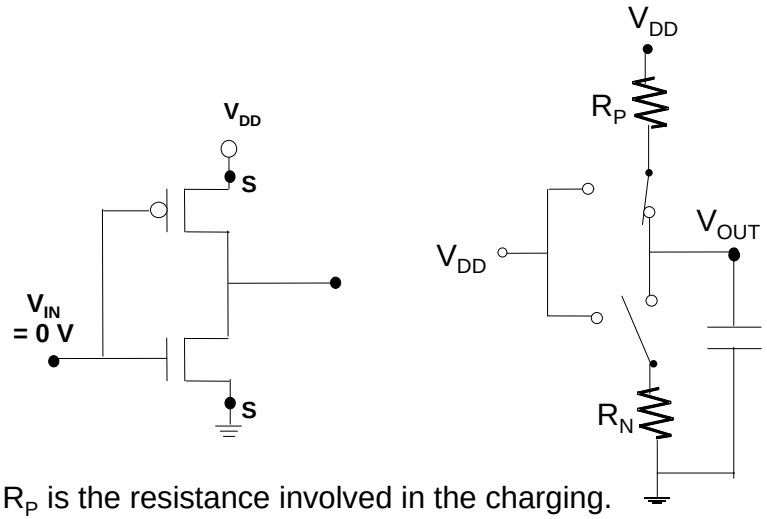
L_l = 200 μm

$C_{OX(l)}$ = 0.1 fF/μm²

Calculate the effective resistance and total output capacitance due to gate and interconnect capacitance.

EXAMPLE

Since V_{IN} is now low, V_{OUT1} must go from low to high. **Pull-up**



R_P is the resistance involved in the charging.

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EXAMPLE

R_P =

Now calculate C_{OUT}:

There are 4 transistor gates attached to inverter output, and one wire connecting the inverter output to the NAND input.

C_{OUT} =

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EXAMPLE

C_G =

C_I =

C_{OUT} =

t_P =

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FAN-OUT

Consider our previous example.

Suppose that we connected N NAND gates to the output of the inverter.

Each NAND gate adds 4 more gate capacitances and another interconnect capacitance.

C_{OUT} =

t_p =

The fan-out, or number of logic gates that can be attached to an output, is limited by propagation delay considerations.

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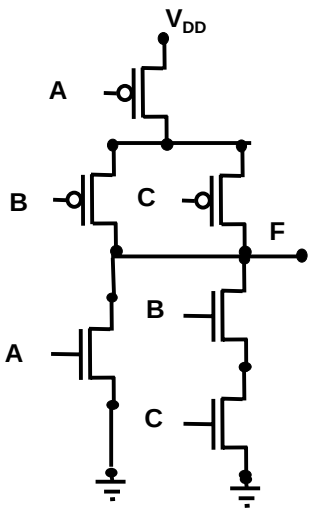
LOOKING AT CMOS CIRCUITS



One can often "see" the logical operation in a CMOS circuit by looking at either the top or bottom half of the circuit.

For example, looking at the top half of this circuit, we see that the output will be connected to V_{DD} (F is high) when:

(B OR C is low) AND A is low

$F = (\overline{B} + \overline{C})\,\overline{A}$

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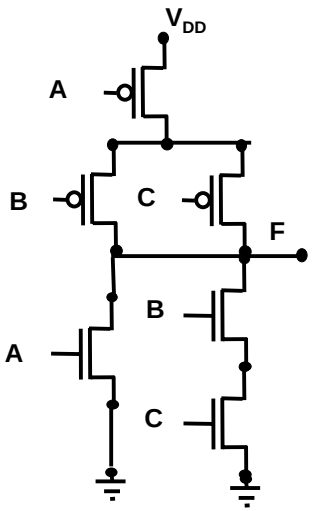
LOOKING AT CMOS CIRCUITS



The bottom half of the circuit always results in the same equation as the top half, just rewritten via DeMorgan (that's why output is always defined).

Looking at the bottom half of this circuit, we see that the output will be connected to ground (F is low) when:

(B AND C are high) OR A is high

$\overline{F} = B\,C + A$

$F = \overline{B\,C + A}$