Computers and Electrical Engineering 81 (2020) 106542

Contents lists available at ScienceDirect

Computers and Electrical Engineering

journal homepage: www.elsevier.com/locate/compeleceng

Improved structured filter design and analysis for perturbed phase-locked loops via sector and $\mathcal{H}_\infty$ norm constraints with convex computations ☆

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ARTICLE INFO

Article history:
Received 25 September 2018
Revised 12 December 2019
Accepted 18 December 2019
Available online 7 January 2020

Keywords:
Nonlinear PLL
Sector constraint
Structured filter
Convex
$\mathcal{H}_\infty$ Norm
Matrix inequalities,

ABSTRACT

This work focuses on designing a structured filter in a phase-locked loop (PLL) system that is perturbed by nonlinear effects from the phase comparator. The filter is designed based on $\mathcal{H}_\infty$ control synthesis which is also optimized along with the stability condition of the nonlinear PLL model. The improvement on the design technique is introduced via relaxations of the $\mathcal{H}_\infty$ norm constraint on the system's frequency response and integration with the nonlinearity's sector bound. The resulting problems are then formulated into matrix inequalities where the solvability conditions are provided via convex computation approaches. Numerical results and computer simulations demonstrate that the tracking capability of the PLL can be enforced via the proposed methods which then lead to a wider lock-in range and a faster acquisition time as compared to existing techniques.

1. Introduction

Phase-locked loops (PLLs) have been around since the early 1930s during which the initial interest was synchronization of local oscillators in FM demodulations. The early use of PLLs at that time, however, was limited due to low performance and high cost factors. As the technology advances with time, many PLL circuits nowadays are fabricated in single integrated circuit (IC) forms and are available in the marketplace at relatively low costs [1,2]. The integration of PLLs with other circuit components also becomes more convenient and makes them flexible for a broad range of applications such as signal conditioning, FK/FSK demodulations, carrier phase tracking and clock synthesizers [3–6].

Designing a high performance PLL attains rapid attention among IC developers and engineers over the past few decades [7,8]. A basic PLL consists of a phase comparator (PC), a loop filter (LF), and a voltage controlled oscillator (VCO) which are connected to form a feedback loop. In a modern communication system, a never-ending challenge to deliver a versatile PLL for analog/mixed-signal circuits on today's system-on-chip (SoC) ICs becomes the industry priority [9]. Since the PLL systems are used for various applications, there is no unique way to design this circuit. Hence, various combination of PCs, LFs, and VCOs can be considered to produce a flexible PLL circuit, and continuous development of these essential components is highly beneficial for the improvement of PLL system performance.

The dynamic behaviour of the PLL is greatly influenced by the filter as it is not only responsible to remove unwanted components of the phase comparison frequencies, but also introduces poles to the closed-loop system. This component will

☆ This paper is for regular issues of CAEE. Reviews processed and recommended for publication to the Editor-in-Chief by Associate Editor Dr. Fatos Xhafa.

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https://doi.org/10.1016/j.compeleceng.2019.106542
0045-7906/

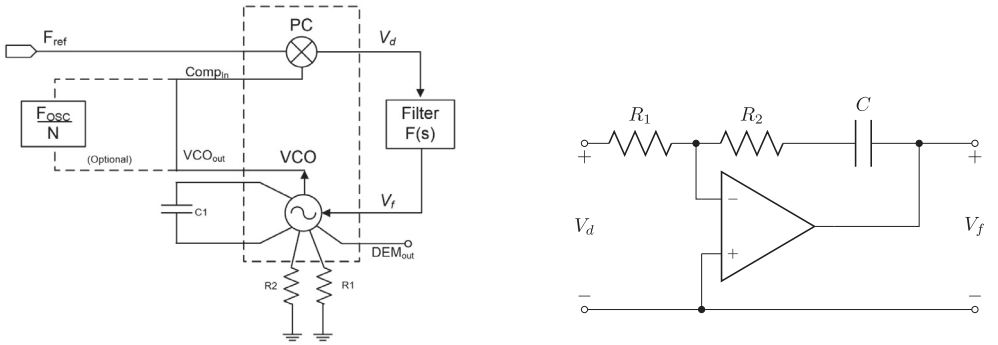
affect the bandwidth and the key performances of PLL in general such as the operating frequency range and acquisition time. Since the structure of the filter for any PLL applications is not rigid, the options to design this component exist in various approaches [10,11]. Applications in data communication systems, for instance, require high order Bessel-type filter to produce superior loop dynamics and improve the jitter performance [11]. For other applications where the lock-in time or acquisition time is not a major concern, and the main requirement is only to synchronize two frequencies, a simple RC or passive filter will be sufficient. When a simple passive filter is required but the phase margin needs to be increased or the phase noise performance needs to be enhanced, the lag-lead filter will be advantageous as its zero can be used to modify the system's frequency response [12,13]. In applications that involve high speed or high frequency signals where the acquisition time and lock-in range are of major concerns, the active proportional and integrating (PI) filter is the most popular type, and is also one of the commonly preferred filters in complementary metal-oxide-semiconductor (CMOS) IC design circuit for general purpose PLL [5,11].

Numerous heuristic techniques have been reported in the literature to tune the parameters of the filter in order to accommodate different performance criteria related to the PLL's frequency response [14,15]. In [16,17], for instance, the phase margin is specified a priori to provide a good jitter tolerance and guarantee a stable operation for high order PLLs. The associated peak amplitude, damping factor and bandwidth have also become the main interest in several design considerations since they are known to dominate the transient state of the system. Similar to the phase margin technique, these parameters can be preassigned to meet the desired performance requirements, and the classical control method is usually employed to obtain the coefficients of the filter. These analytical design procedures, nonetheless, do not guarantee optimal values of the filter's parameters. In order to provide a more systematic design technique that is able to optimize the filter, a modern control approach via $\mathcal{H}_\infty$ synthesis has been adopted in a number of studies on PLL filter design [18–21]. This method allows the designer to parameterize the filter while minimizing the peaking in the sensitivity and complementary sensitivity of the closed-loop system [22], hence ensuring the tracking capability of the PLL in the presence of disturbances or noise for some targeted applications.

Despite the effectiveness of the proposed techniques, the stability of the PLL is not guaranteed as the system is inherently nonlinear due to the characteristics of the VCO and the PC [23–25]. This issue has sparked a great interest among researchers to study the nonlinear model of the PLL and the impacts of the nonlinearity on its stability and operating frequency range [26]. A detailed nonlinear nature of the PLLs can be found in [27] where two broad categories of PCs are highlighted, which are multiplier (memoryless device) and sequential circuit (memory device). The multiplier is usually a simple device such as an analog mixing phase detector or an XOR gate while the sequential circuit is usually built via combinations of logic flip-flops and gates. Each of them leads to different types of nonlinearities that can be described mathematically in terms of the phase difference of the input and output signals. Prior work by [3] provides an intuitive insight about these nonlinear effects on the PLL based on a graphical technique known as phase plane portrait. In this method, however, the analysis is restricted to low order (i.e. first and second) PLLs. For higher order systems where the nonlinearity is sector restricted, the Lyapunov methods which are based on energy functions [28] are more relevant but the analysis may become unmanageable as the order gets higher. Another approach that can guarantee the stability of the nonlinear PLL system is via the circle criterion, which was initially derived in frequency domain [29]. The analysis based on this criterion is also suitable for higher order systems as it can be converted to time domain conditions to form linear matrix inequalities that can be efficiently solved via convex optimization methods [30].

While the aforementioned nonlinear analysis techniques may suffice to ensure stability, a suitable approach to design the filter is also crucial as it greatly affects the operating frequency range and acquisition time. As most existing design techniques are heuristic in nature, searching for optimal filter parameters to satisfy both design requirements as well as stability conditions when the system is driven into its nonlinear region may be cumbersome. In this work, the focus is on a PLL system with a structured active PI filter which is perturbed by the nonlinear effects from the PC. The design technique for the filter is based on the $\mathcal{H}_\infty$ control synthesis which is also optimized along with the stability condition for the nonlinear PLL model. The improvement on the design technique is introduced via relaxations of the $\mathcal{H}_\infty$ norm constraint of the system's frequency response and integration with the nonlinearity's sector bound. The resulting problems are then formulated into matrix inequalities where the solvability conditions are provided via convex computation approaches. The analysis on the impacts of the $\mathcal{H}_\infty$ norm bound relaxations on the PLL's frequency and time domain responses is also presented. We show that the tracking capability of PLL can be enforced via the proposed methods which then lead to a wider lock-in range and a faster acquisition time as compared to existing methods in the literature. Another advantage of the proposed methods is the low computational complexity which also allows a systematic approach to design the PLL with a specified bandwidth and acquisition time.

The rest of the paper is structured as follows: Section 2 explains the motivation of the work and the PLL design framework in the context of linear and nonlinear control systems. Section 3 describes the methodology and the main results which are presented in terms of convex searches of the filter's parameters subject to different design requirements and constraints. Section 4 presents the computer simulations and numerical results from the proposed methods which include the impacts of different $\mathcal{H}_\infty$ norm bounds on the PLL's frequency and time-domain responses, and explicit procedures for PLL design with specified bandwidth and acquisition time. The performance of the proposed methods in comparison with existing techniques are also included in this section. The last section concludes the results. The standard notations are used throughout this paper; $\Re$, $\Re^+$, and $\Re^{n\times p}$ denote the fields of real numbers, positive real numbers and real $n \times p$ matrices respectively, $\bar{\sigma}(A)$ indicates the maximum singular values of A.



(a) Block diagram of HCT4046A (b) Active PI filter structure

Fig. 1. Block diagram of CMOS PLL with an active PI filter.

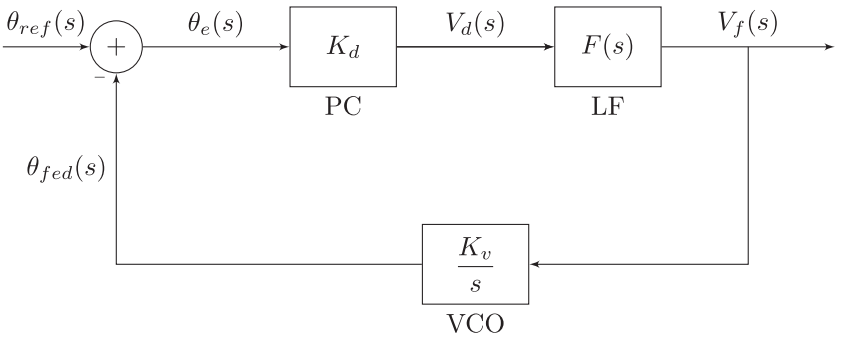


Fig. 2. General PLL block diagram in phase domain.

2. Motivation and design framework

The block diagram of a PLL circuit in one of the CMOS IC family is shown in Fig. 1a. This chip contains a VCO, an optional frequency divider and three selections of PC (i.e. XOR gate, J-K and R-S flip-flops). To offer a more flexible design, the filter, $F(s)$, and the frequency divider are connected externally, allowing support for different applications. A quite similar structure is also available in CD4046B PLL device but with only two selections of PC.

The circuit diagram of an active PI filter is illustrated in Fig. 1b, where the structure of the filter is given by:

$$F(s) = \frac{\tau_2 s + 1}{s\tau_1}. \tag{1}$$

with $\tau_2 = CR_2$ and $\tau_1 = CR_1$. As the PLL starts to operate, the output of the VCO will be multiplied with the input or reference signal at the PC, which then produces low and high frequency components. Assuming all the high frequency components have been attenuated by the filter, the corresponding block diagram in phase domain reduces to Fig. 2 where $\theta_{ref}(s)$, $\theta_{fed}(s)$ and $\theta_e(s)$ denote the phase of the reference signal, VCO output and phase error respectively. K_d represents the dimensionless gain of the PC, while K_v (rad/s/Volt) denotes the gain of the VCO which is also represented by a simple integrator.

The closed-loop transfer function can then be written as:

$$\begin{aligned} T(s) &= \frac{K_T\left(\frac{\tau_2 s+1}{s\tau_1}\right)}{s + K_T\left(\frac{\tau_2 s+1}{s\tau_1}\right)} \\ &= \frac{K_T(\tau_2/\tau_1)s + K_T/\tau_1}{s^2 + (K_T\tau_2/\tau_1)s + K_T/\tau_1} \\ &= \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \end{aligned} \tag{2}$$

where $K_T = K_d K_v$ defines the loop gain, ζ is the damping factor and ω_n is the natural frequency.

Various techniques have been proposed for the PLL filter design to meet different requirements for improved time domain response, such as minimizing the peak overshoot which depends on ζ, and reducing the settling time by increasing the value

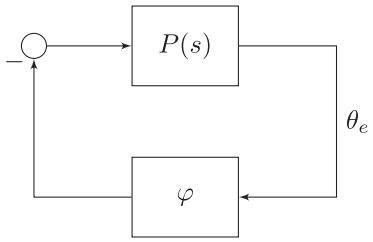


Fig. 3. Lur'e Structure.

of ω_n. In another approach related to relative stability, the useful relationship [31]:

$$\phi_m = tan^{-1} \frac{2\zeta}{\sqrt{-2\zeta^2 + \sqrt{1+4\zeta^4}}} \tag{3}$$

allows one to design a good filter by driving the value of the phase margin, ϕ_m, to the desired range, as there are situations where some of the component values need to be confined within a certain bound. These include the case when there is a partially integrated loop filter or if the VCO input capacitance is an issue, which in turn restricts the loop bandwidth. In either case, constraining the ϕ_m by limiting ζ may be one of the solutions as it is able to maximize the bandwidth.

Another method of designing the filter is via the frequency domain approach, which is the main interest of this paper. Let M_ω be the peak amplitude in the frequency response of $T(s)$; the key design parameter in this work is M_ω which relates to ζ and ϕ_m by the following approximations:

$$M_\omega \approx \frac{1}{2\zeta\sqrt{1-\zeta^2}}, \quad M_\omega \approx \frac{1}{2\sin(0.5\phi_m)}, \quad \text{for} \quad \zeta \leq 1/\sqrt{2} \tag{4}$$

Hence, limiting the phase margin also translates to constraining the value of M_ω. In the context of modern control, this peak value is termed as $\mathcal{H}_\infty$ norm which is defined as follows:

$$||T||_\infty := \sup_{R(s)>0} \bar{\sigma}[T(s)] = \sup_{\omega\in\Re} \bar{\sigma}[T(j\omega)]. \tag{5}$$

Although a PI filter theoretically guarantees stability and zero tracking error in general, it has been shown in the literature [19,32] that the PLL will fall out of lock when the system is driven into its nonlinear region. This has become another issue within the PLL design framework where its stability is affected by the nonlinear behavior of the components. In this scope, the nonlinear effect from the PC is prioritized and we assume that the PLL is working under the VCO's linear range. In the light of [30], the PLL system can be restructured into linear and nonlinear blocks as depicted in Fig. 3, where $P(s)$ is the forward loop transfer function of the feedback system in Fig. 2, and φ represents the nonlinearity resulting from the PC which has been shown to satisfy a certain sector constraint.

This configuration is well-known as the Lur'e structure [29]. A recent work in [19] proposed a search for optimal values of a general filter form with poles at the origin via minimization of M_ω to unity while satisfying the nonlinearity's constraint. Although the simulation presented in [19] shows better performance as compared to the linear approximation method (i.e. only M_ω is minimized without considering the nonlinearity) in terms of the lock-in and pull-in range, the tracking capability is still limited when the input frequency gets higher. Hence, there is no systematic way to design the filter for a PLL system that is subject to nonlinearity in general. Moreover, fixing the maximum value of M_ω to unity does not allow one to select the filter's parameters or the system's bandwidth if they are limited due to the design requirements or other restrictions.

In this work, a new design technique is introduced where the maximum value of M_ω is relaxed within a prespecified bound, and the filter's parameters are optimized alongside with the nonlinearity's constraint in a single convex computation. The details of the proposed methods are presented in the following section.

3. Methodology and main results

The value of M_ω can be minimized by using the optimal $\mathcal{H}_\infty$ control technique where the closed-loop system needs to be first restructured into the framework as in Fig. 4. The lower block, $F(s)$, is the filter to be designed while the upper block, $H(s)$ is the equivalent system subject to the inputs θ_{ref} and V_f, and outputs θ_{fed} and V_d. The optimization problem can be solved either in frequency-domain or time-domain of which the latter is an approach well-known as matrix inequality searches. These methods are stated in the following lemma:

Lemma 1 *[22]. Given a LTI system $J(s) = C_J(sI - A_J)^{-1}B_J + D_J$, and a positive value of $\gamma > 0$. The following statements are equivalent.*

(i) A is Hurwitz stable and $\|J(j\omega)\|_\infty \leq \gamma$ for all $\omega \in \Re$.

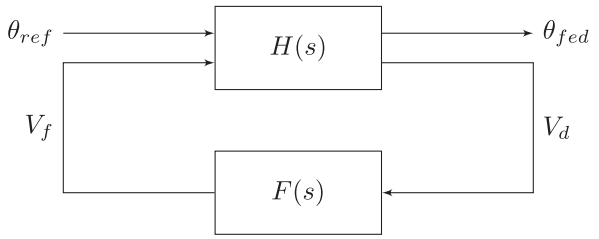


Fig. 4. $\mathcal{H}_\infty$ control framework.

(ii) There exists a matrix $P = P^T > 0$ such that the following matrix inequality holds,

$$\begin{bmatrix} A_J^T P + PA_J & PB_j & C_J^T \\ B_J^T P & -\gamma I & D_J^T \\ C_J & D_J & -\gamma I \end{bmatrix} \leq 0. \tag{6}$$

Via Lemma 1, the value of M_ω can be minimized to γ, and the parameters of $F(s)$ can be obtained when $M_\omega = \gamma$. This, however, is a standard optimal $\mathcal{H}_\infty$ control strategy which assumes $F(s)$ has no fixed structure. Hence, if $F(s)$ is of a PI form as in (1), a modification on this is necessary. The following lemma will be introduced first as it provides a suitable state space representation of the closed-loop system that can preserve the convexity of the search in the subsequent proposition.

Lemma 2. *Let*

$$K_0 = \frac{K_T \tau_2}{\tau_1}, \quad \text{and} \quad K_1 = \frac{K_T}{\tau_1} \tag{7}$$

and given

$$T(s) = \frac{K_0 s + K_1}{s^2 + K_0 s + K_1}. \tag{8}$$

The corresponding state space can then be written as follows:

$$T \sim \left[\begin{array}{c|c} A_L + B_{L2}\mathbf{C}_L & B_{L1} \\ \hline \mathbf{C}_L & 0 \end{array}\right] \tag{9}$$

where

$$A_L = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}, \quad B_{L1} = \begin{bmatrix} 0 \\ 1 \end{bmatrix}, \quad B_{L2} = \begin{bmatrix} 0 \\ -1 \end{bmatrix}, \quad \mathbf{C}_L = [K_1 \quad K_0]. \tag{10}$$

Proof. From the transfer function in (8), we can obtain

$$T \sim \left[\begin{array}{c|c} A_T & B_T \\ \hline C_T & D_T \end{array}\right] = \left[\begin{array}{cc|c} 0 & 1 & 0 \\ -K_1 & -K_0 & 1 \\ \hline K_1 & K_0 & 0 \end{array}\right] \tag{11}$$

via controllable canonical transformation. By partitioning A_T into $A_L + B_{L2}\mathbf{C}_L$, the two state space in (11) and (9)-(10) are then equivalent. □

The following proposition presents a method which modifies the structure of Fig. 4 into another suitable form and also allows the search for the filter's parameters when M_ω is constrained within a prespecified bound.

Proposition 1. *Consider the closed-loop system in Fig. 2 with the closed-loop transfer function given in (2). Suppose M_ω is the maximum peak amplitude of the closed-loop frequency response, and it is desired that $M_\omega \in [1, \gamma_u]$ and $\gamma_u \in \Re^+$. If there exist a positive definite matrix $\mathbf{X} \in \Re^{n_a \times n_a}$, a row matrix $\mathbf{C}_1 \in \Re^{1 \times n_a}$ and $\gamma \in \Re^+$ such that the following optimization problem is feasible:*

$$\min \quad \gamma \quad \text{s.t.}$$

$$\gamma - \gamma_u \geq 0, \tag{12}$$

$$\begin{bmatrix} A_L\mathbf{X} + B_{L2}\mathbf{C}_1 + \mathbf{X}A_L^T + \mathbf{C}_1^T B_{L2}^T & B_{L1} & \mathbf{C}_1^T \\ B_{L1}^T & -\gamma I & 0 \\ \mathbf{C}_1 & 0 & -\gamma I \end{bmatrix} < 0, \tag{13}$$

then solving $\mathbf{C}_L = \mathbf{C}_1\mathbf{X}^{-1}$ *gives the design coefficients* K_1 *and* K_0 *as defined in (7).*

Proof. Let $U = [K_1 \quad K_0]\bar{X}$ where $\bar{X} = [X_1 \quad X_0]^T$. By replacing V_f with U, and V_d with $\bar{X}$, the lower block in Fig. 4 can be transformed into C_L, and the upper block will be modified as:

$$\tilde{H}(s) = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix}. \tag{14}$$

As $H_{21} = 0$, it follows that $\theta_{fed} = H_{11}\theta_{ref}$. Hence the problem of $\mathcal{H}_\infty$ control for this system reduces to $||T(j\omega)||_\infty \le \gamma$ for all $\omega \in \Re$. By using the state space in (9) from Lemma 2, and invoking Lemma 1, we can get

$$\begin{bmatrix} (A_L + B_{L2}\mathbf{C}_L)^T\mathbf{P} + \mathbf{P}A_L + B_{L2}\mathbf{C}_L & \mathbf{P}B_{L1} & \mathbf{C}_L^T \\ B_{L1}^T\mathbf{P} & -\gamma I & 0 \\ \mathbf{C}_L & 0 & -\gamma I \end{bmatrix} \le 0. \tag{15}$$

Applying the congruence transformation with diag(*X, I, I*) where $X = P^{-1}$ and a change of variable $\mathbf{C}_1 = \mathbf{C}_L\mathbf{X}$, inequality (13) will be obtained. The constraint (12) follows from the requirements $\gamma > \gamma_u$, which can be included without sacrificing the convexity of the search. Hence the result. □

The method above will give optimal values of the filter's parameters when M_ω is minimized subject to $\gamma \in [1, \gamma_u]$. In the case where a more specific range of the acquisition time is required in the performance criteria, the bounds on M_ω need to be modified. The following proposition allows one to specify the desired bounds for M_ω and the maximum acquisition time.

Proposition 2. *Suppose the design specification requires that* $\gamma = ||T||_\infty$ *is bounded by*

$$\gamma_l < \gamma < \gamma_u, \quad \gamma_l \ge 1, \tag{16}$$

and the acquisition time, τ_a*, satisfies*

$$\tau_a \le \tau_{amax}. \tag{17}$$

Select $Y \ge 4/\tau_{amax}$*. Under the conditions of Proposition 1, if the inequalities (13), (18), and (19):*

$$\gamma - \gamma_u \le 0, \quad \gamma - \gamma_l \ge 0, \tag{18}$$

$$A_L\mathbf{X} + B_{L2}\mathbf{C}_1 + \mathbf{X}A_L^T + \mathbf{C}_1^T B_{L2}^T + 2Y\mathbf{X} < 0 \tag{19}$$

are satisfied, then solving $\mathbf{C}_L = \mathbf{C}_1\mathbf{X}^{-1}$ *gives the desired design coefficients* K_1 *and* K_0 *as defined in (7).*

Proof. The approximation for the acquisition time is $\tau_a \approx 4/\zeta\omega_n$, hence the design procedure requires $\zeta\omega_n > \tau_{amax}$, or in other words, the locations of the poles need to be on the left side of a vertical strip defined by $-Y = -\zeta\omega_n$. Therefore, by selecting $Y \ge 4/\tau_{Lmax}$, this condition can be guaranteed via the constraint in (19) [33]. The remaining of the proof follows from changing the optimization problem in Proposition 1 into a feasibility test on the constraints in (13) and (18). □

The methods in Propositions 1 and 2 allow some amount of overshoot in the frequency response to accommodate a faster acquisition time. They are, however, derived under the assumption that the PLL is working under the linear range, which are more suitable for systems with phase detectors of flip-flop types or tri-state phase-frequency detector with a charge pump. For systems with classical mixing phase detectors (analog multiplier) [30] or XOR gates as in Fig. 1a, their linear range are relatively smaller than those with the flip-flops, hence the performance will deteriorate faster when the input frequency is increased. In this regard, the nonlinearity can be included in the design procedure by rearranging the system into the Lur'e structure in Fig. 3. If the analog multiplier is used for input and output signals of sinusoidal wave pulses, for instance, the resulting nonlinearity resembles a sine function, i.e.

$$\varphi(.) = \sin(\theta_e). \tag{20}$$

where θ_e is the phase error or difference between the input and output signals. In another case where the input and output signals are of square pulses, and either an analog multiplier or an XOR gate is used as a PC, the resulting nonlinearity can be approximated by [27] :

$$\varphi(.) \approx \frac{4}{\pi}\sum_{n=0}^{5}\frac{(-1)^n}{(2n+1)^2}\sin[(2n+1)\theta_e] \tag{21}$$

Assuming φ does not leave the $(-\pi, \pi)$ region, both types of nonlinearities share some common properties, i.e. the nonlinearities are static, memoryless and satisfy the sector and slope bounds as follows [19]:

$$0 \le \frac{\varphi(q)}{q} \le k_c \qquad \forall q \ne 0 \tag{22}$$

and

$$k_l(q_1 - q_2) \le \varphi(q_1) - \varphi(q_2) \le k_u(q_1 - q_2) \quad \forall q_1 \ne q_2 \tag{23}$$

where $k_c, k_l, k_u \in \Re^+$ represent the sector, lower slope and upper slope bounds of the nonlinearity respectively. Under these conditions, the closed-loop system is absolutely stable if the Nyquist plot of $P(j\omega)$ lies on the right of a vertical line which crosses $-1/k_c$ on the real axis. In other words,

$$Re[P(j\omega)] > -\frac{1}{k_c} \quad \forall \omega \in \Re. \tag{24}$$

This condition is well-known as the circle criterion [34]. Similar to the optimal $\mathcal{H}_\infty$ control method, the condition can be tested either in frequency domain or time-domain. The following lemma shows the connection between the two.

Lemma 3. *[34]*

Suppose $P(s) = C_p(sI - A_p)^{-1}B_p + D_p$ is the transfer function in the forward path in Fig. 3, the following statements are equivalent.

(i) The closed-loop system in Fig. 3 is absolutely stable if A_p is Hurwitz and nyquist plot of $P(s)$ lies on the right half plane defined by $Re[s] = -1/k_c$.

(ii) There exists a matrix $Q = Q^T > 0$ such that the following matrix inequality holds,

$$\begin{bmatrix} A_p^T Q + Q A_p & Q B_p - C_p^T \\ B_p^T Q - C_p & -2k_c^{-1} \end{bmatrix} < 0. \tag{25}$$

It is worth noting that Lemma 3 cannot be applied directly to the PLL system as the forward loop transfer function is critically stable. The Lur'e structure however can be modified by using the loop transformation technique. The following corollary provides an extension of the result in Proposition 1 which takes into account the nonlinearity for the search of the filter's parameters.

Corollary 1. *Suppose the PLL system contains a nonlinearity which satisfies the bounds in (22)-(23). Under the conditions of Proposition 1, if there exist a positive definite matrix $\mathbf{X} \in \Re^{n_a \times n_a}$, a row matrix $\mathbf{C}_1 \in \Re^{1 \times n_a}$ and $\gamma \in \Re^+$ such that γ can be minimized subject to the constraints in (12)-(13) and (26),*

$$\begin{bmatrix} A_L\mathbf{X} + k_l B_{L2}\mathbf{C}_1 + \mathbf{X}A_L^T + k_l \mathbf{C}_1^T B_{L2}^T & B_{L1} - \mathbf{C}_1^T \\ B_{L1}^T - \mathbf{C}_1 & -2(k_c + k_l)^{-1} \end{bmatrix} \le 0, \tag{26}$$

then solving $\mathbf{C}_L = \mathbf{C}_1\mathbf{X}^{-1}$ gives the desired design coefficients K_1 and K_0 as defined in (7).

Proof. Applying the loop transformation with k_l at the feedback [19], the equivalent upper block in Fig. 3 will be $P_n(s) \sim (A_n, B_n, C_n, 0)$ where $A_n = A_L - k_l B_{L2} C_L$, $B_n = B_{L1}$ and $C_n = C_L$, and the transformed nonlinearity will satisfy the sector condition in (22) with k_c replaced by $k_c + k_l$. The application of Lemma 3 is then straightforward, and performing a similar congruence transformation as in the proof of Proposition 1 will give the result. □

If $\gamma_u \to 1$ in (12), the result in Corollary 1 reduces to the method proposed in [19]. The following corollary gives an equivalent result as in Proposition 2 but with the sector constraint included.

Corollary 2. *Suppose the design specification requires that the $\mathcal{H}_\infty$ norm of $T(j\omega)$ is bounded as in (16), and the acquisition time satisfies (17). Under the conditions of Proposition 2 and Corollary 1, if the inequalities (13), (18), (19) and (26) are satisfied, then solving $\mathbf{C}_L = \mathbf{C}_1\mathbf{X}^{-1}$ gives the desired design coefficients K_1 and K_0 as defined in (7).*

Proof. The result immediately follows by combining the feasibility test in Proposition 2 and the sector constraint in Corollary 1. □

It is worth to note that the coefficients K_1 and K_0 obtained via the proposed methods above may lead to a low closed-loop bandwidth as the design requirements only prioritize the $\mathcal{H}_\infty$ norm and sector constraints. This will be undesirable if we require a wider lock-in range in the PLL design specification. The following result proposes another design method to accommodate this issue.

Corollary 3. *Let $K_1 = q_1$ and $K_0 = q_0$ be the parameters obtained from the previous design with $||T||_\infty = \gamma_q$, and β be the corresponding closed-loop bandwidth. If*

$$\hat{K}_0 = M_q q_0 \quad \text{and} \quad \hat{K}_1 = M_q^2 q_1, \quad M_q > 1 \tag{27}$$

are used in place of K_0 and K_1 respectively for the filter's parameters in the nonlinear PLL model, the resulting closed-loop bandwidth will be $\hat{\beta} \approx M_q\beta$ with the same value of $||T||_\infty$.

Proof. From (2), we can rewrite the filter as follows:

$$F(s) = K_0 + K_1/s = 2\zeta\omega_n + \frac{\omega_n^2}{s}. \tag{28}$$

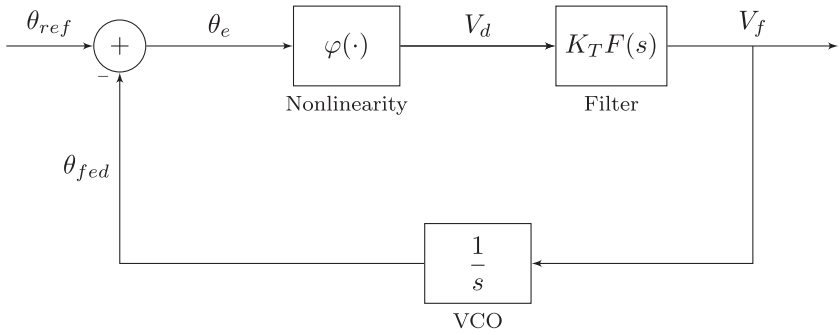


Fig. 5. PLL model with sector-bounded nonlinearity.

Since the bandwidth of the second order system in (2) is proportional to ω_n, multiplying K_1 with M_q, and K_0 with M_q^2 as in (27) is also equivalent to multiplying ω_n with M_q. Hence, the resulting closed-loop bandwidth will also be approximately scaled by M_q. □

4. Computer simulations and numerical results

This section is divided into three parts; Section 4.1 presents the analysis of the impacts of changing the bounds of γ to the frequency and time domain responses; Section 4.2 shows the application of the proposed methods to design the PLL with specified bandwidth and acquisition time, and Section 4.3 extends the methods to design the PLL with higher bandwidth. The computer simulations were performed using MATLAB and Simulink, and the optimizations were solved using Sedumi and Yalmip toolboxes.

The nonlinear PLL model considered for the computer simulations is shown in Fig. 5 where φ represents the sector-bounded nonlinearity. The model is also equivalent to the linear one when φ is replaced by a unity gain.

For brevity purposes, we write "Prop." for "Proposition", "Cor." for "Corollary", "NPM" for nonlinear PLL model, and "LPM" for linear PLL model. The input frequency is represented by ω_{in} while the lock-in range is represented by ω_L. We denote ϕ_1 for the nonlinearity described in (20), and ϕ_2 for the nonlinearity described in (21). The following relation:

$$\tau_a = \tau_L + \tau_p \tag{29}$$

where τ_L = lock-in time, and τ_p = pull-in time is also important to distinguish between the lock-in time and the acquisition time. The lock-in time in general is the time the PLL acquires lock if the input is within the lock-in range (i.e. $\omega_{in} \leq \omega_L$), while the pull-in time is defined as the time the PLL acquires lock when $\omega_{in} > \omega_L$ (which results in cycle slipping) [26]. In other words, if $\omega_{in} \leq \omega_L$, then

$$\tau_a \approx \tau_L \tag{30}$$

whereas if $\omega_{in} > \omega_L$, we get

$$\tau_a \approx \tau_p. \tag{31}$$

Hence τ_a will be relatively longer due to the cycle slipping.

4.1. Impact of γ_u on the frequency and time domain responses of LPM and NPM

This section analyses the impact of γ_u on the frequency and time domain responses of LPM and NPM. When only the $\mathcal{H}_\infty$ norm and sector constraints are considered in the optimization problem and feasibility test, the important differences between the linear methods (Propositions 1 and 2) and nonlinear methods (Corollaries 1 and 2) are highlighted as follows:

(i) For γ_u approximately between 1.1 and 1.7, the linear and nonlinear methods only show small differences in terms of M_ω as shown in Fig. 6. As γ_u increases, Corollaries 1 and 2 start to diverge below their linear counterparts. Their corresponding bandwidth, β, on the other hand, decrease with γ_u, and it is seen that the bandwidth from the nonlinear methods are slightly lower than those from the linear methods.

(ii) For the time domain response, the peak amplitude M_t for a 1Hz step input increases with γ_u as illustrated in Fig. 7. Simulations via LPM model show higher values from Propositions 1 and 2 than the values obtained from their nonlinear counterparts (Corollaries 1 and 2). When the nonlinearity is included in the model, similar differences can also be observed, but with all values slightly higher than the LPM model simulations. The values consistently increase even a small increase (i.e. 2Hz) in the step input is fed into the system.

(iii) A different trend is seen from the acquisition time from the LPM and NPM simulations as shown in Fig. 8 where Propositions 1 and 2 lead to shorter τ_a than their nonlinear counterparts do. As the input frequency increases,

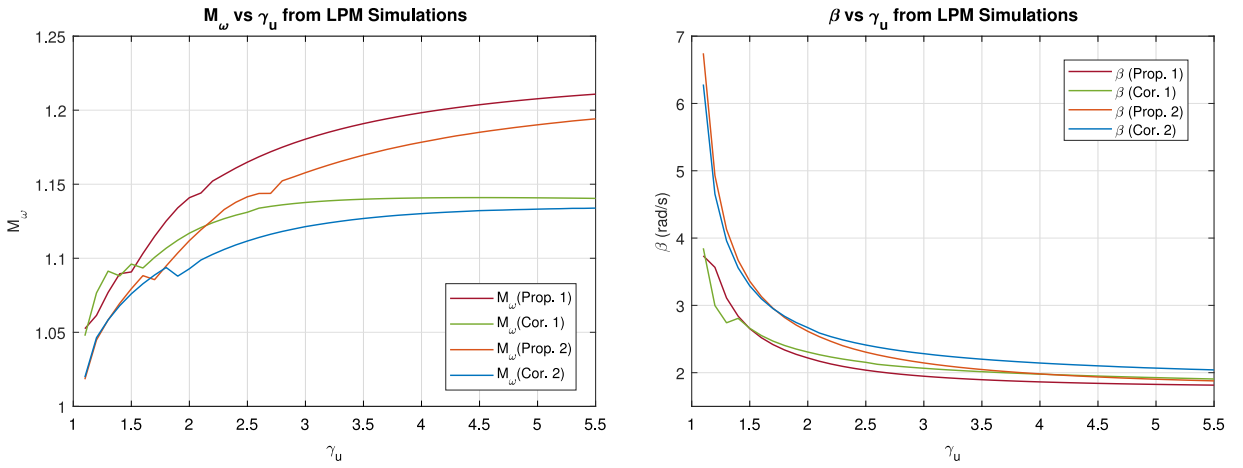


Fig. 6. Impact of γ_u on the LPM's frequency response (M_ω and β) via Propositions 1, 2 and Corollaries 1, 2.

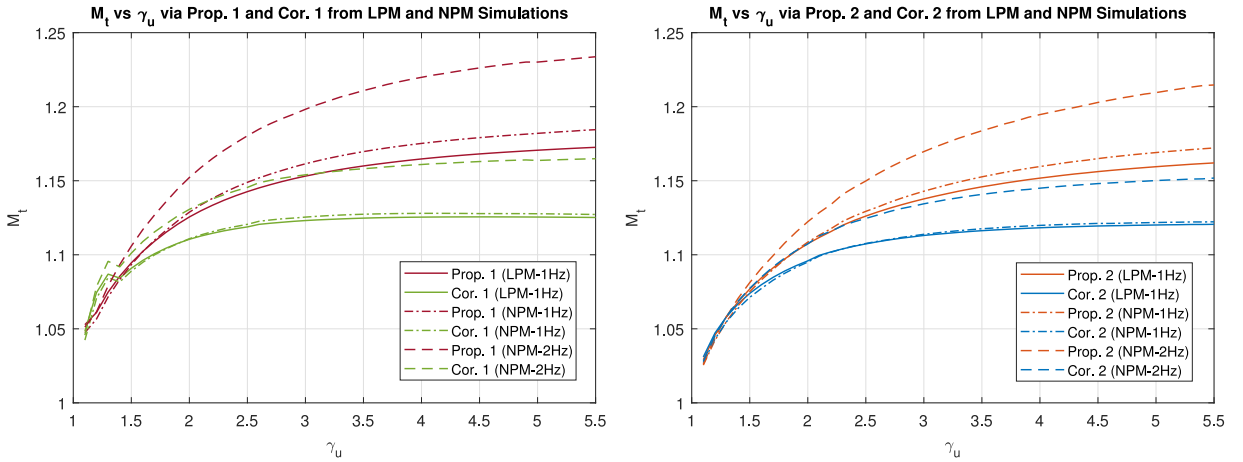


Fig. 7. Impact of γ_u on M_t via Proposition 1, 2 and Corollaries 1, 2 from LPM and NPM simulations.

the simulations take longer time to lock when Corollaries 1 and 2 are applied as compared to the results from Propositions 1 and 2.

From the comparisons, it can be concluded that with the inclusion of the sector constraint in Corollaries 1 and 2, the resulting M_ω and M_t decrease with γ_u, hence better performance in terms of overshoot in frequency and time domain responses can be achieved. The differences shown in M_t and τ_a from Figs. 7 and 8 as the input frequency increases clearly show the effects from the nonlinearity which can degrade the PLL performance. The acquisition time, nonetheless, is longer when Corollaries 1 and 2 are applied, and this indicates another constraint on the locations of the poles need to be included in the feasibility test if one is to design a PLL with a shorter τ_a.

4.2. Design with specified bandwidth and faster acquisition time

Suppose the design specification requires a maximum acquisition time of 130ms, i.e. $\tau_{amax} \approx 130$ ms for an input frequency step. Under Proposition 2 (and Corollary 2) conditions, we can select $Y \approx 32$. Suppose further, the upper bound of γ is given by $\gamma_u = 1.3$. The feasible solutions are

$$K_0 = 354.2, \quad K_1 = 12961.3 \tag{32}$$

via application of Proposition 2, and

$$K_0 = 442.4, \quad K_1 = 17097.6 \tag{33}$$

via application of Corollary 2. Assume $K_\mathrm{d} = 1$, and $K_v = 1 \times 10^5$ rad/s/Volt (a typical range for the VCO gain). Setting $R_1 = 800\,k\Omega$ gives $(R_2, C) = (1.3\,k\Omega, 352\,\mu F)$ via Proposition 2, and $(R_2, C) = (1.7\,k\Omega, 278\,\mu F)$ via Corollary 2. Fig. 9(a) shows the plot of τ_a against input frequency step where the values of τ_a are obtained from the simulations of NPM with ϕ_1 and

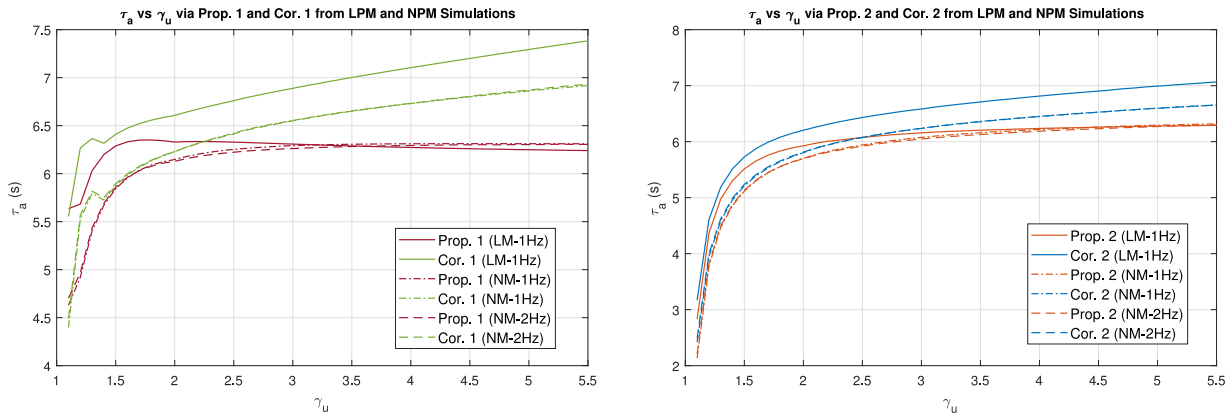


Fig. 8. Acquisition time vs γ_u via Proposition 1 and Corollary 1 (left); and via Proposition 2 and Corollary 2 (right) from both LPM and NPM simulations.

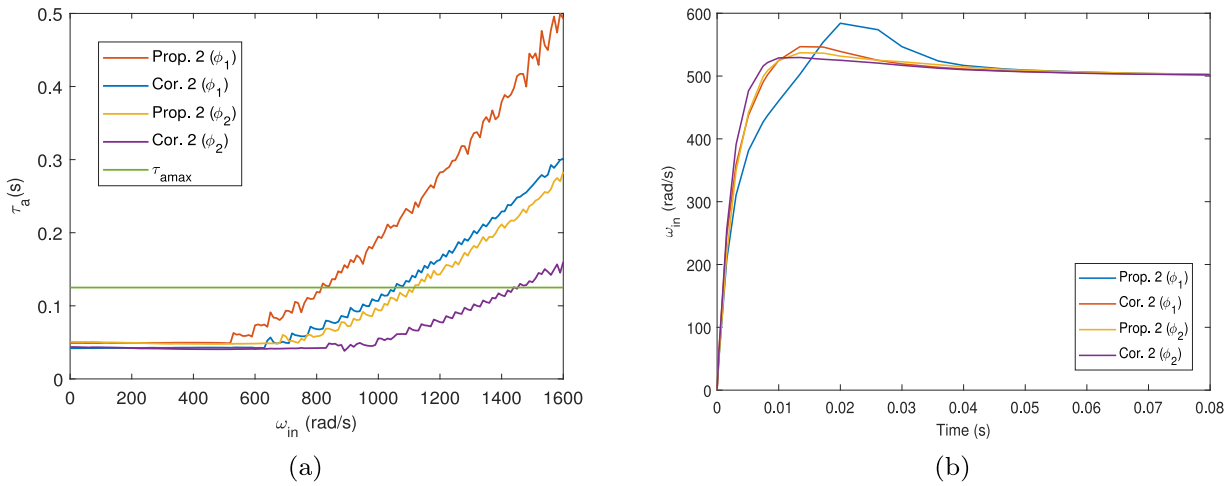


Fig. 9. (a) Acquisition time vs input frequency; (b) Step responses when $\omega_{in} = 500$ rad/s.

ϕ_2. It can be observed that at low input frequencies (approximately below 500 rad/s), the NPM behaves quite similar to a linear system as the acquisition time does not really change when the input changes. As the frequency increases, higher locking range within the desired τ_a can be achieved from the filter designed via Corollary 2 as compared to that from Proposition 2 for both types of nonlinearities. In other words, Corollary 2 leads to faster responses when the input frequency increases. The responses when $\omega_{in} = 500$ rad/s is shown in Fig. 9(b) via both methods and for both types of nonlinearities. The consistency of the performance between both methods can also be observed in Fig. 10 when higher input frequencies are forced into the NPM.

4.3. Design with higher bandwidth

This section is intended to provide a comparison with the recent methods in the literature which propose filter design for higher bandwidth. We write "NonM" as the nonlinear method proposed in [19], and "LinM" as the linear method compared in [19] when the nonlinearity constrained is removed.

From the plot of β vs γ_u in Fig. 6, we can see that the closer the value of γ_u to 1, the higher the bandwidth, and since Proposition 2 and Corollary 2 provide relatively higher β and lower M_ω, they will be used to compare with NonM and LinM.

The resulting filters obtained via NonM and LinM are $(K_0, K_1) = (6.82 \times 10^5, 319.3)$ and $(K_0, K_1) = (8.79 \times 10^5, 587.9)$ respectively. In order to apply Proposition 2 and Corollary 2, we set $\gamma_u = 1.0008$ which is very close to 1. The parameters obtained are $(K_0, K_1) = (85.4, 2.72)$ via Proposition 2 with $\beta \approx 85.3$, and $(K_0, K_1) = (94.5, 4.3)$ via Corollary 2 with $\beta \approx 94.4$. Note that these bandwidths result in a limited lock-in range. By applying the method from Corollary 3, we can scale β to the desired bandwidth by multiplying K_1 with M_q, and K_0 with M_q^2. This allows one to achieve a much higher lock-in range while preserving the $\mathcal{H}_\infty$ norm and sector constraints from the previous design. In this example, we set the desired bandwidth to be $M_q\beta$ with $M_q = 100000$. The resulting filter's parameters for all methods are listed in Table 1 together with

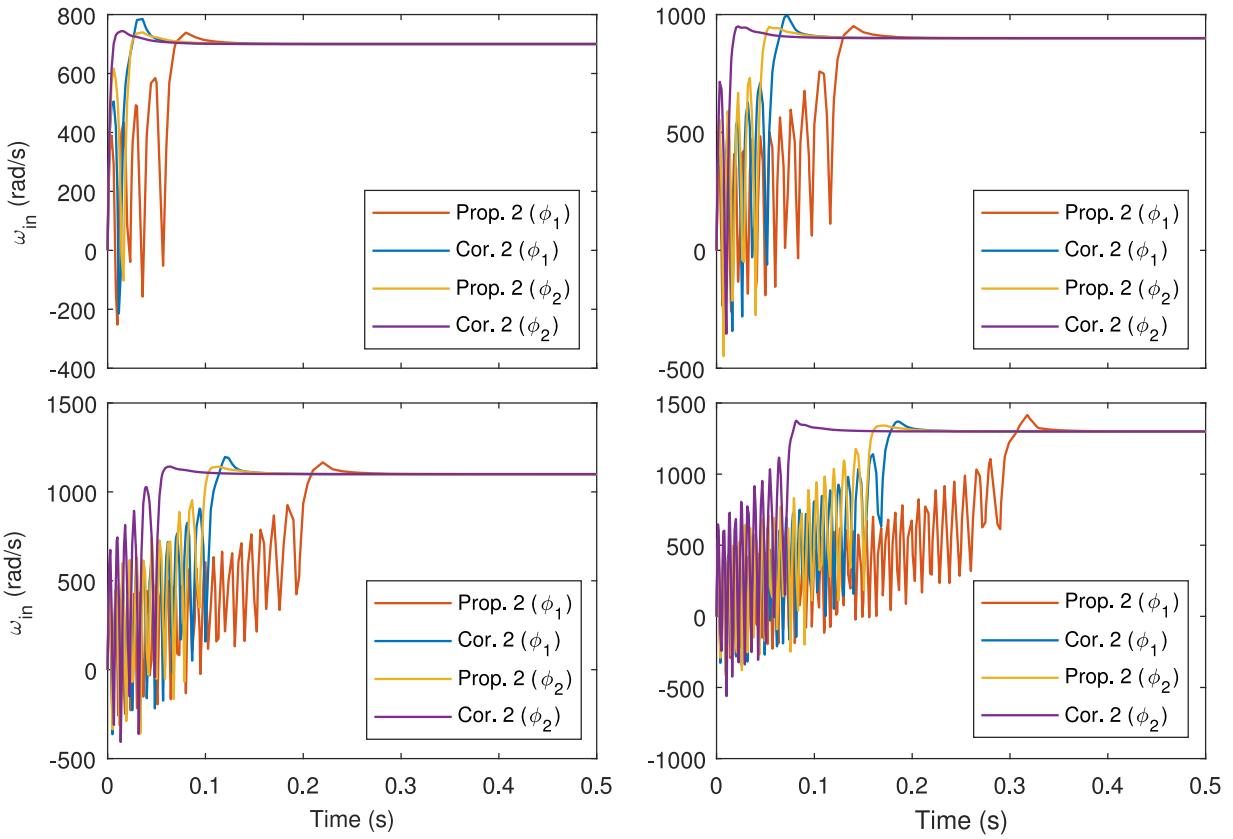


Fig. 10. Step responses for higher input frequencies. From top left to bottom right: $\omega_{in} = 700$ rad/s, $\omega_{in} = 900$ rad/s, $\omega_{in} = 1100$ rad/s, and $\omega_{in} = 1300$ rad/s. Corollary 2 leads to a much shorter acquisition time as compared to other methods.

Table 1
Design coefficients and the corresponding values for R_1, R_2 and C when $K_d = 1$ and $K_v = 1 \times 10^5$ rad/s/V.

Method	Design coefficients		Filter's parameters		
	K_0	K_1	$R_1(\Omega)$	$R_2(k\Omega)$	$C(F)$
Proposition 2 + Corollary 3	8.54×10^6	2.72×10^{10}	1×10^3	85.4	3.68×10^{-9}
Corollary 2 + Corollary 3	9.45×10^6	4.30×10^{10}	1×10^3	94.5	2.23×10^{-9}
LinM	1.42×10^6	0.91×10^3	8×10^5	68.2	137×10^{-6}
NonM	5.76×10^6	1.95×10^3	8×10^5	87.9	64.1×10^{-6}

Table 2
Comparisons between Proposition 2 + Corollary 3, Corollary 2 + Corollary 3 and existing methods in terms of peak amplitude, bandwidth, and lock-in range for both types of nonlinearity.

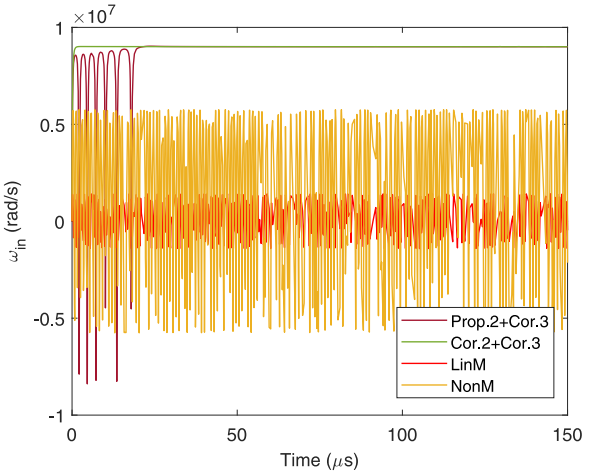
Method	γ_u	M_ω	β (10^6 rad/s)	ω_L^{n1} (10^6 rad/s)	ω_L^{n2} (10^6 rad/s)
Proposition 2 + Corollary 3	1.0008	1.0002	8.52	8.5	13
Corollary 2 + Corollary 3	1.0008	1.0002	9.43	9.42	14
LinM	N/A	1.0000	1.41	1.41	2.1
NonM	N/A	1.0000	5.75	5.75	8.73

the corresponding component values. The comparisons of the methods in terms of M_ω, β and lock-in range (ω_L^{n1} for NPM with ϕ_1, and ω_L^{n2} for NPM with ϕ_2), are summarized in Table 2.

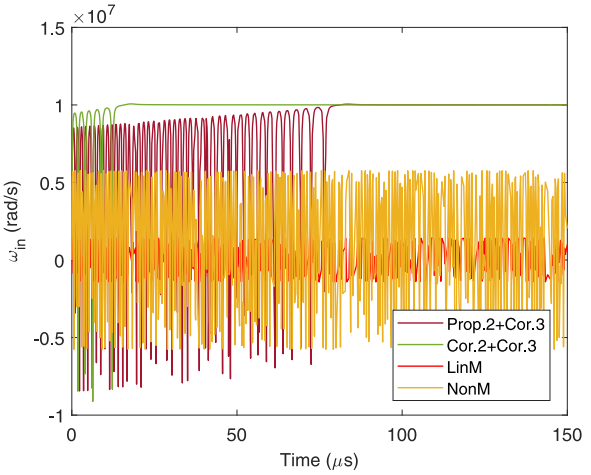
As Proposition 2 + Corollary 3 and Corollary 2 + Corollary 3 lead to higher bandwidths (with Corollary 2 + Corollary 3 being the highest), the lock-in range for both are also much wider than those from LinM and NonM as can be compared from the 5th and 6th columns in Table 2. The comparisons on the acquisition time for all methods with both types of nonlinearities are summarized in Table 3 where it can be clearly seen that as the input frequency increases, the filters designed via Proposition 2 + Corollary 3 and Corollary 2 + Corollary 3 are able to drive the NPM to the lock state much

Table 3
Acquisition time comparison with both types of nonlinearity when the input frequency is increased; "NL" indicates the PLL does not lock.

ω_{in}	τ_a(µs) for NPM with ϕ_1				τ_a(µs) for NPM with ϕ_2			
(rad/s)	Proposition 2 + Corollary 3	Corollary 2 + Corollary 3	LinM	NonM	Proposition 2 + Corollary 3	Corollary 2 + Corollary 3	LinM	NonM
1×10^0	0.518	0.487	2.76	0.71	0.536	0.499	2.94	0.743
1×10^1	0.706	0.751	2.79	0.72	0.737	0.787	2.93	0.755
1×10^2	0.555	0.527	2.77	0.71	0.583	0.511	2.94	0.745
1×10^3	0.496	0.429	2.77	0.72	0.524	0.452	2.94	0.764
1×10^4	0.478	0.417	2.76	0.69	0.505	0.445	2.94	0.730
1×10^5	0.462	0.428	2.78	0.70	0.491	0.449	2.88	0.742
1×10^6	0.479	0.430	3.41	0.69	0.488	0.439	2.78	0.689
5×10^6	0.536	0.479	NL	1.01	0.493	0.442	NL	0.677
8×10^6	0.804	0.603	NL	NL	0.457	0.404	NL	0.640
9×10^6	18.8	0.769	NL	NL	0.484	0.421	NL	NL
1×10^7	85.4	12.9	NL	NL	0.482	0.446	NL	NL
1.4×10^7	NL	NL	NL	NL	39.3	0.422	NL	NL
1.5×10^7	NL	NL	NL	NL	NL	13.8	NL	NL

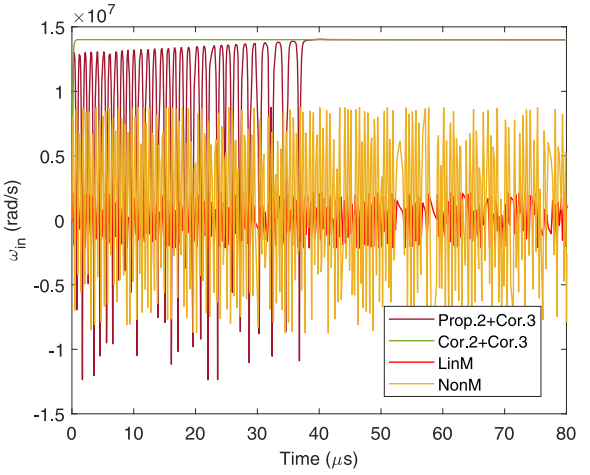


(a) Step response when $\omega_{in} = 9 \times 10^6$ rad/s.

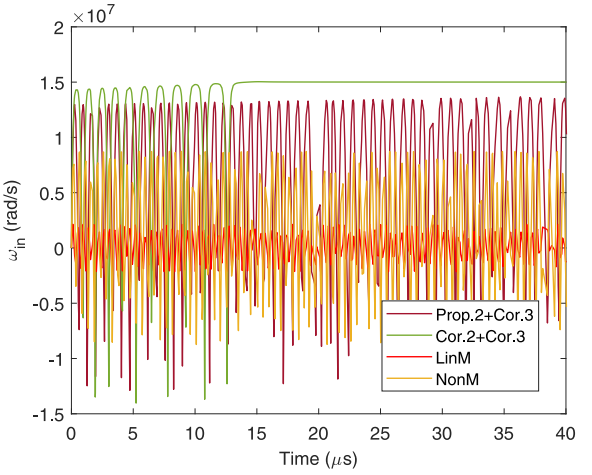


(b) Step response when $\omega_{in} = 1 \times 10^7$ rad/s.

Fig. 11. Step responses when high input frequencies are fed into the NPM with ϕ_1. The pull-in time is shorter via Corollary 2 + Corollary 3 than that via Proposition 2 + Corollary 3. The PLL via LinM and NonM on the other hand fail to lock.



(a) Step response when $\omega_{in} = 1.4 \times 10^7$ rad/s.



(b) Step response when $\omega_{in} = 1.5 \times 10^7$ rad/s.

Fig. 12. Step responses when high input frequencies are fed into the NPM with ϕ_2. The PLL acquires lock through the pull-in process via Corollary 2 + Corollary 3. The PLL via Proposition 2 + Corollary 3, LinM and NonM on the other hand fail to lock.

faster than those designed via LinM and NonM. The performance of Corollary 2 + Corollary 3 is also higher than that of Proposition 2 + Corollary 3 since the filter is designed by taking into account the constraint of the nonlinearity. The lock-in range for all methods are higher with ϕ_2 than ϕ_1 as the triangular-shaped nonlinearity theoretically has a wider linear range as compared to that of the sine-wave nonlinearity [27].

Another important observation from Table 3 is the value of τ_a which drastically increases whenever ω_{in} exceeds the lock-in range (ω_L as listed in Table 2). This also implies the PLL can still acquire lock but requires more time due to cycle slips (hence $\tau_a \approx \tau_p$), a scenario commonly known as the pull-in process. This is illustrated in Fig. 11(a) where $\omega_{in} > \omega_L^{n1}$ via Proposition 2 + Corollary 3. In Fig. 11(b), the pull-in process occurs for both NPMs via Proposition 2 + Corollary 3 and Corollary 2 + Corollary 3 as ω_{in} exceeds both lock-in range, but the acquisition time via Corollary 2 + Corollary 3 is much shorter than that via Proposition 2 + Corollary 3. Examples of the same scenario for NPM with ϕ_2 are shown in Fig. 12 where only Corollary 2 + Corollary 3 is able to drive the PLL to the lock state. Proposition 2 + Corollary 3 and the existing methods on the other hand fail to do so.

5. Conclusions

Improved active Proportional-Integral filter design methods for phase-locked loops have been proposed where the main techniques rely on the relaxations of the $\mathcal{H}_\infty$ norm constraint of the system's frequency response, i.e. γ_u, and integration with the nonlinearity's sector bound. As the resulting problems are presented in terms of linear matrix inequalities, optimal solutions can be easily obtained via convex optimizations. We have also introduced a technique that can be useful for nonlinear phase-locked loop designs that require high bandwidths. The computer simulations demonstrate that the performance of the phase-locked loop system is greatly enhanced via the proposed methods in terms of the lock-in range and acquisition time as compared to existing methods in the literature.

For future works, the techniques introduced can be applied to phase-locked loops with other filter forms for different design requirements. The applications, may, however require some modifications or manipulations of the matrix inequalities to ensure the search for the filter's parameters remains convex.

Declaration of Competing Interest

The authors declare that they do not have any financial or nonfinancial conflict of interests.

CRediT authorship contribution statement

Siti Juliana Abu Bakar: Data curation, Investigation, Writing - original draft. **Nur Syazreen Ahmad:** Methodology, Supervision, Writing - review & editing. **Patrick Goh:** Validation, Visualization.

Acknowledgment

The authors would like to thank Ministry of Education (Malaysia) for the financial support under Fundamental Research Grant Scheme (203/PELECT/6071347).

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