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Asymmetric isolated unidirectional multi-level DC-DC power converter

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ABSTRACT

This paper proposes an asymmetric unidirectional isolated multi-level DC-DC power converter (AUIMLDDPC). A three-winding transformer (TWT) is used as the interface between a half-bridge inverter (HBI) and two full-bridge rectifiers (FBRs). The turn numbers for two secondary windings of TWT are not the same. Thus, it results in unequal DC output voltages of the two FBRs. A selection circuit is adopted to control the unequal DC output voltages of two FBRS to be connected in series or stand-alone, and thus, generates a non-zero two-level voltage to control the magnitude of the output DC voltage of the proposed AUIMLDDPC. An output L-C filter is applied to filter out the high frequency harmonic of the non-zero two-level voltage. The secondary windings with unequal turn numbers for TWT can reduce the voltage change of the non-zero two-level voltage. Therefore, it can reduce the L-C filter capacity. To validate the performance of the proposed AUIMLDDPC, a hardware prototype is developed. The experimental results are as expected.

1. Introduction

Multi-level DC-AC inverter can effectively reduce the voltage jump caused by the operation of switching so that the switching loss, *dv/dt*, electromagnetic interference (EMI) and harmonics are decreased [1–4] as compared with conventional DC-AC inverter [5]. In addition, multi-level inverter can use a small capacity output filter, and it results in the compact power density. The advantages of multi-level DC-DC power converter are similar to those of multi-level inverter, and it can be classified as isolated and non-isolated [6–9] types. The transformer can provide galvanic isolation and avoid the leakage current and the electric shock [10,11] in the isolated type. Hence, it can increase safety. The power flow of isolated multi-level DC-DC power converter may be bidirectional [12,13] or unidirectional [6,8,9]. The unidirectional isolated DC-DC power converters have been used in the battery chargers for data centers [9], electric vehicles [14] and renewable power generation systems [15] recently. This paper addresses the half-bridge inverter (HBI) based isolated multi-level DC-DC power converter.

Several isolated unidirectional multi-level DC-DC power converters (UIMLDDPCs) were used for reducing the filter capacity and improving efficiency [6,8]. Three UIMLDDPC topologies, three-level single-transformer series HBI (TLSTSHBI), three-level dual-transformer series HBI (TLDTSHBI) and three-level diode-clamped HBI (TLDCHBI), have been published in [6]. The TLSTSHBI topology uses one transformer, two HBIs and a full-bridge rectifier (FBR). The TLDTSHBI topology uses two transformers, two HBIs and one FBR. Both series HBI topologies require two HBIs. Hence, it complicates the hardware and control circuits. Besides, the cost is increased. The TLDCHBI topology requires four switches, and it has the disadvantages that the difference in the turn-off characteristics between the two series switches may generate unbalance voltage stress and damage these two series switches [6]. In [8], an UIMLDDPC with three-winding transformer (TWT) was published. The multi-level voltage of this power converter is formed by a TWT, a HBI, two FBRs a series/parallel selection circuit to generate a non-zero two-level voltage. The turn numbers of two secondary windings for the TWT are equal, and then the DC output voltages of the two FBRs are the same. Thus, the voltage swing for the non-zero two-level voltage is half of the maximum value of non-zero two-level voltage.

This paper proposes an asymmetric unidirectional isolated multi-level DC-DC power converter (AUIMLDDPC) improved from the UIMLDDPC [8]. The output voltage in front of the output filter is a non-zero two-level voltage with unequal magnitude and the magnitude of the lower voltage level is larger than half that of the high voltage level in the proposed AUIMLDDPC. Therefore, the proposed AUIMLDDPC has advantages of reducing the voltage swing and harmonics of the output voltage in front of the output

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filter. As a result, the output filter capacity can be further reduced and a diode is saved as compared with UIMLDDPC in [8]. A hardware prototype of the proposed AUIMLDDPC is built and tested to validate its performance.

2. Circuit topology and operation modes

Fig. 1 shows the topology of the proposed AUIMLDDPC. This topology is improved from [8], and it is composed of a HBI, a TWT, two FBRs, a selection circuit and an output filter combined by L-C. The TWT contains a winding (N_p) in the primary side and two windings (N_s, N_t) in the secondary side. The HBI is switched in constant duty ratio of 0.5 to generate a square-wave voltage on the primary winding N_p of TWT. The duty ratio fixed at 0.5 for HBI results in the symmetrical square waveform across the windings (N_p) in the primary side of transformer and then output two square voltages to two FBRs to generate two unequal DC voltages due to unequal windings. The output voltage is regulated only by using the selection circuit to control the unequal DC output voltages of two FBRS to be connected in series or stand-alone. Therefore, the output voltage is not necessary to be fed to the control circuit of primary side to control the duty ratio for HBI, and an isolation feedback is avoided. Hence, both the design of transformer and the control of HBI are simplified.

Two windings N_s and N_t of the transformer secondary side provide square-wave voltages connecting to the two FBRs, respectively. The turn numbers for the windings N_s and N_t of the transformer secondary side are not the same, and the output DC voltages (V_{C3} and V_{C4}) of two FBRs are unequal. The turn number of N_s is smaller than that of N_t, and V_{C3} is smaller than V_{C4}. The selection circuit (S_3, D_9) controls the DC output voltages of two FBRs to be connected in series or stand-alone. V_{out_FBR} is the summation of V_{C3} and V_{C4} when two FBRs are connected in series (S_3 is turned on), and V_{out_FBR} is V_{C4} when two FBRs operate in the condition of stand-alone (S_3 is turned off). As compared with [8], the major difference includes that a diode is saved in the selection circuit and the turn numbers of the N_s and N_t are not the same. In addition, the operation of selection circuit is not series/parallel in [8] but series/stand-alone in the proposed AUIMLDDPC. In UIMLDDPC [8], the output voltage in front of the output filter is a non-zero two level voltage with equal magnitude. It results that the magnitude of the high voltage level is double that of the low voltage level. In the proposed AUIMLDDPC, the output voltage in front of the output filter is a non-zero two-level voltage with unequal magnitude, and the magnitude of the lower voltage level is larger than half that of the high voltage level. Therefore, the proposed AUIMLDDPC has advantages of reducing the voltage change of the output voltage in front of the output filter. As a result, the output filter capacity can be further reduced and a diode is saved as compared with UIMLDDPC in [8].

The turn ratios of the transformer are defined as:

$$n_1 = \frac{N_s}{N_p} \tag{1}$$

$$n_2 = \frac{N_t}{N_p} \tag{2}$$

The operation for the proposed AUIMLDDPC can be divided into four modes, and the operating circuits are shown in Fig. 2 and described as following:

2.1. Mode I

The operating circuit of this mode is shown in Fig. 2(a). In Fig. 2 (a), S1 is turned on, and S_2 as well as $\underline{S_3}$ are turned off. The red bold line shows that V_{out_FBR} can be represented as:

$$V_{out_FBR} = V_{c4} = (V_{in} n_2)/2 \tag{3}$$

2.2. Mode II

The operating circuit of this mode is shown in Fig. 2 (b). As seen in Fig. 2(b), S2 is turned off, and S_1 as well as S_3 are turned on. The red bold line shows that V_{out_FBR} can be represented as:

$$V_{out_FBR} = V_{c3} + V_{c4} = (V_{in} n_2)/2 + (V_{in} n_1)/2 \tag{4}$$

2.3. Mode III

The operating circuit of mode III is shown in Fig. 2(c). As can be seen, S_2 is turned on, and S_1 as well as S_3 are turned off. The red bold line shows that V_{out_FBR} can be represented as:

$$V_{out_FBR} = V_{c4} = (V_{in} n_2)/2 \tag{5}$$

2.4. Mode IV

In this mode, S_1 is turned off, and S_2 as well as S_3 are turned on. The operating circuit of mode IV is shown in Fig. 2(d), and the red bold line shows that V_{out_FBR} can be represented as:

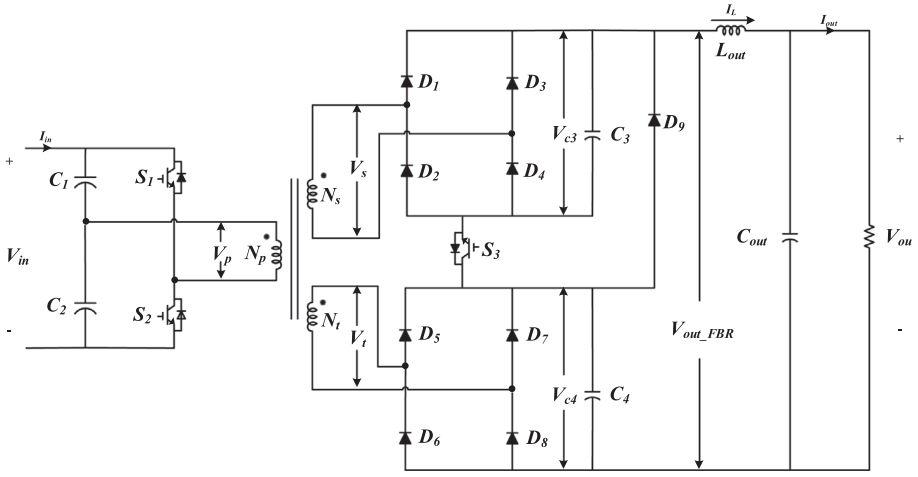

Fig. 1. Proposed AUIMLDDPC.

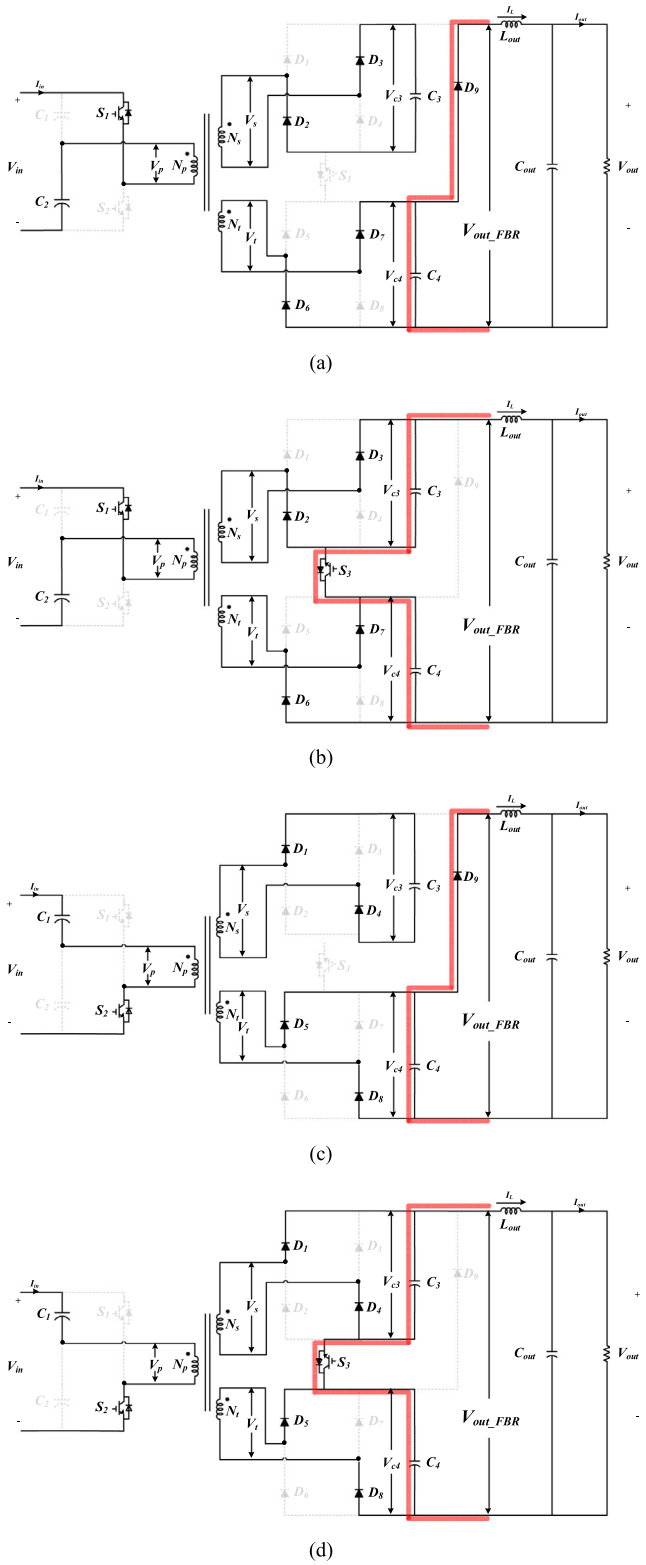

Fig. 2. Operating circuits of the proposed AUIMLDDPC, (a) mode I, (b) mode II, (c) mode III, (d) mode IV.

$$V_{out_FBR} = V_{c3} + V_{c4} = (V_{in}n_2)/2 + (V_{in}n_1)/2 \tag{6}$$

From the above description, the voltage V_{out_FBR} is switching between two voltage levels of V_{C4} and $(V_{C3} + V_{C4})$. It should be noted that V_{C3} is smaller than V_{C4}. The voltage swing in front of the output L-C filter for the proposed AUIMLPPC is only V_{C3}, hence, the voltage swing is smaller than that in UIMLDDPC [3,5]. Therefore, the capacity of the output filter in the proposed AUIMLDDPC can be further decreased as compared with that of previous HBI based UIMLDDPCs.

3. Design consideration

Fig. 3 shows the related signals for the proposed AUIMLDDPC. The operating frequencies for S_1 and S_2 are f_s, and that for S_3 is $2f_s$. The duty ratios of S_1 and S_2 are 0.5. The output voltage is the average voltage of V_{out_FBR}, and represented as:

$$V_{out} = \frac{V_{in}}{2}(D * n_1 + n_2) \tag{7}$$

As shown in (7), it can be found that the duty ratio (D) of S_3 is used to adjust the output voltage of the proposed AUIMLDDPC. Considering the input voltage of AUIMLDDPC may be a battery set, the input voltage will be decreased when the state of charge (SOC) of battery set is dropped. If the varied range of input voltage is between $V_{in,min}$ and $V_{in,max}$, the design of n_1 and n_2 are shown as:

$$n_1 \geq \frac{2V_{out}}{V_{in,min}} - n_2 \tag{8}$$

$$n_2 \leq \frac{2V_{out}}{V_{in,max}} \tag{9}$$

It can be seen in Fig. 3(f) that the output voltage in front of the output filter varies between $(V_{in}n_2)/2 + (V_{in}n_1)/2$ and $(V_{in}n_2)/2$. Because n_2 is larger than n_1 in proposed AUIMLDDPC, the output voltage in front of the output filter is a non-zero two-level voltage with unequal magnitude and the magnitude of the lower voltage level is larger than half that of the high voltage level. Therefore, the voltage swing in the proposed AUIMLDDPC is smaller than that in UIMLDDPC [8].

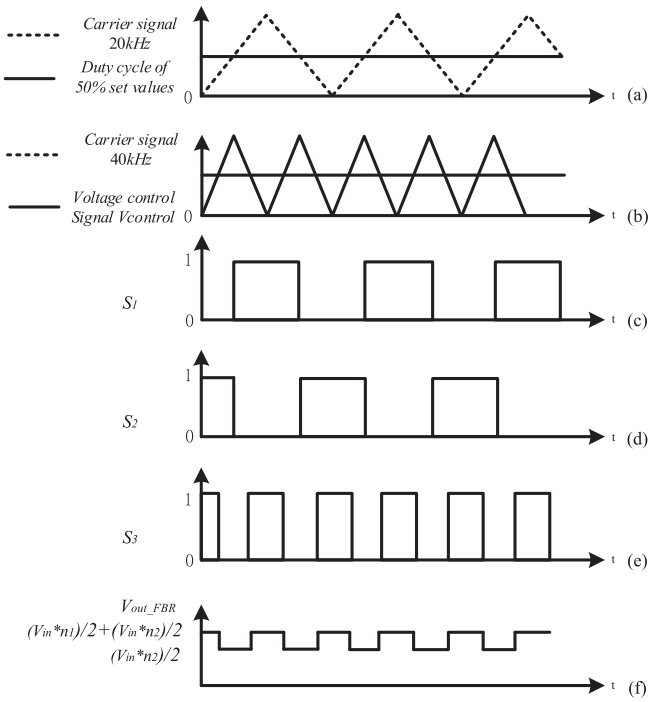

Fig. 3. Related signals of the proposed AUIMLDDPC, (a) control and carrier signals of S_1 and S_2, (b) control and carrier signals of S_3, (c) gate signal of S_1, (d) gate signal of S_2, (e) gate signal of S_3, (f) waveform of V_{out_FBR}.

If the varied range of the input voltage is small, n_1 will be very small as compared to n_2. Accordingly, the voltage variation of V_{out_FBR} is very small, and thus, the capacity of output filter can be reduced significantly as compared with that of previous HBI based UIMLDDPCs in which the voltage change across the output L-C filter is fixed (half of the maximum voltage across the output L-C filter). In addition, the turn number of N_S is reduced to save the cost of wire and core and then the power loss can be reduced. For example, the varied range of input voltage is 20%, then, the voltage variation of V_{out_FBR} is only 20% of the output voltage variation of two FBRs in UIMLDDPC [8].

The current change of L_{out} for the AUIMLDDPC can be represented as:

$$\Delta I_{Lout} = \frac{(Vin\frac{n_2}{2}) + (Vin\frac{n_1}{2}) - V_{out}}{2L_{out}f_s} D \tag{10}$$

where fs is the switching frequency of S_3. The inductor L_{out} can be determined while the current change of L_{out} is specified. The ripple of output voltage for the AUIMLDDPC can be derived as:

$$\Delta V_o = \frac{\Delta I_L}{16 C_{out} f_s} \tag{11}$$

The capacitor C_{out} can be obtained while the ripple of output voltage $_t$ is specified.

4. Experimental results

A hardware prototype is built and tested to verify the performance of the proposed AUIMLDDPC. Table 1 shows the major parameters used in the prototype.

Fig. 4 shows the measured waveforms of the gate signals for switching devices. It can be found that the gate signals for switching devices S_1 and S_2 are complementary, and the driving frequency of the gate signal for S_3 is two times that of S_1 and S_2. The driving voltages of MOSFET are 15 V and −5 V for turning on and off, respectively. The negative voltage is adopted in the driver of MOSFET to avoid the unexpected conduction.

Fig. 5 shows the experimental results of the proposed AUIMLDDPC in front of the output L-C filter. V_p is the voltage across the winding Np, V_p, V_s is the voltage across the winding N_s, and V_t is the voltage across the winding N_t. The voltage difference is due to the different turn numbers of three windings in TWT. Three windings, N_p, N_s and N_T, of transformer (TWT) in the proposed AUIMLDDPC is 12:8:16. It results that the output voltages of both FBRs are 133.3 V and 266.7 V, respectively. As a result, the voltage in front of output filter is a non-zero two-level voltage where two voltage levels are 266.7 and 400, respectively. The voltage swing of the output voltage in front of the output filter is only 133.3 V. However, N_p:N_{s1}:N_{s2} of three-winding transformer (TWT) in the UIMLDDPC [8] is 24:26:26. It results that the output voltage in front of output filter is a non-zero two-level voltage where two voltage levels are 200 and 400, respectively. The voltage swing of the output voltage in front of the output filter is 200 V. As seen in Fig. 5(d), the non-zero two-level voltage is composed of 266.7 V and 400 V. The voltage swing of the output voltage in front of the output filter is only 133.3 V which is smaller than 200 V in the UIMLDDPCs [8]. Thus, the proposed AUIMLDDPC has the feature that the swing voltage is further reduced. Therefore, the capacity of the output filter can be further reduced. Another advantage of the proposed AUIMLDDPC is n_2 always larger than n_1. Thus, a diode is saved and the power conversion efficiency is improved.

Fig. 6 is the experimental results when the proposed AUIMLDDPC is working in 3.2 kW. Fig. 6(a) shows that the voltage V_{out_FBR} is changed between 266.7 V and 400 V, and the inductor current is always higher than zero, it shows the converter is working in continuous conduction mode.

Fig. 7 shows both of the voltages and currents for the input side and the output side of the proposed AUIMLDDPC. As seen in Fig. 7 (a) and 7(b), the input voltage is 400 V and the input current is

Table 1
Major parameters of the prototype.

Parameters	
P_{out}	3.2 kW
V_{out}	380 V
V_{in}	400 V
switching frequency of S_1 and S_2	20 kHz
switching frequency of S_3	40 kHz
C_1 and C_2	940 μF
C_3 and C_4	50 μF
N_p:N_s:N_t	12:8:16
Leakage inductance of transformer	1.84 μH
magnetizing inductance of transformer	2.24 mH
L_{out}	28 μH
C_{out}	2200μF
Fast Recovery Epitaxial diode	DSEI60-06A
SiC Schottky diode	CREE C3D20065D
CoolMOS Power MOSFET	SPW47N60C3
SiC MOSFET	CREE C3M0065090D

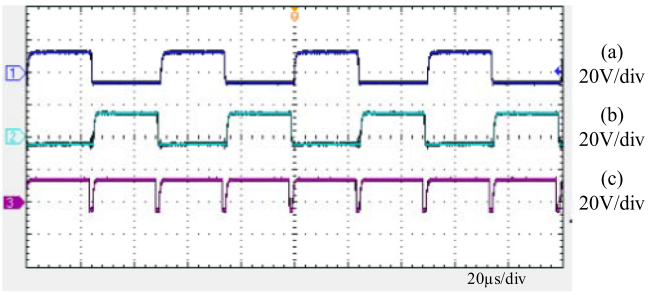

Fig. 4. Measured waveforms of the gate signals for switching devices,(a) S_1, (b) S_2, (c) S_3.

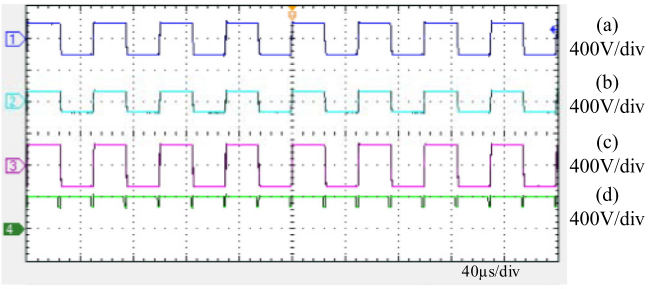

Fig. 5. Experimental results for the proposed AUIMLDDPC, (a) V_p, (b) V_s, (c) V_t , (d) V_{out_FBR}.

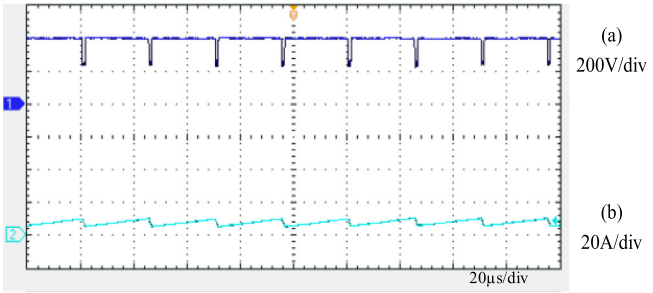

Fig. 6. Experimental results for the proposed AUIMLDDPC, (a) V_{out_FBR}, (b) i_L.

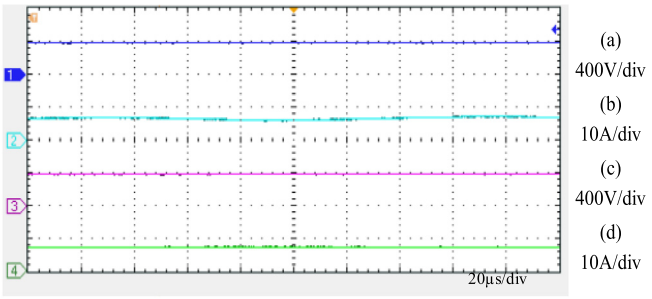

Fig. 7. Experimental results for the proposed AUIMLDDPC, (a) input voltage V_{in}, (b) input current I_{in}, (c) output voltage V_{out}, (d) output current I_{out}.

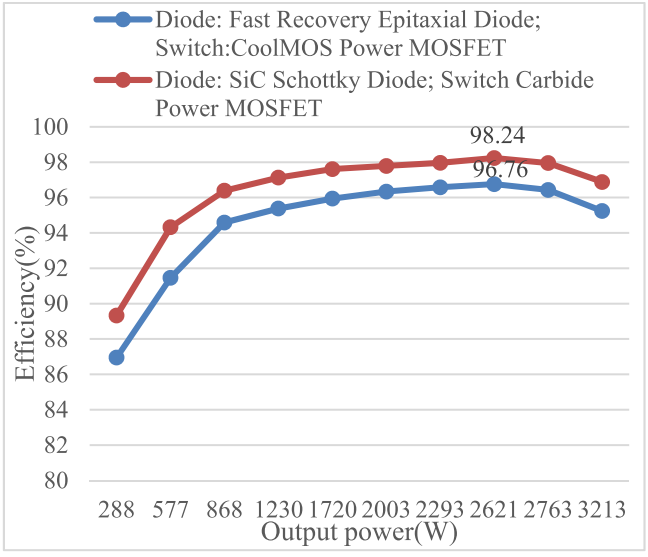

Fig. 8. Efficiency curves of the AUIMLDDPC.

6.68A. Fig. 7(c) and 7(d) show that the output voltage is 380 V and the output current is 6.91A. The proposed isolated multi-level DC-DC converter outputs 2.6 kW DC power.

Fig. 8 shows the curves of conversion efficiency for the proposed AUIMLDDPC. Neglecting the power loss of control and driver circuits in the measured results of conversion efficiency. As seen in Fig. 7, the highest efficiency of the AUIMLDDPC which uses the Fast Recovery Epitaxial diode and CoolMOS Power MOSFET is 96.76% at 2.6 kW, and the highest efficiency of the AUIMLDDPC which uses the SiC Schottky diode and SiC MOSFET is 98.24% near 2.6 kW.

Table 2 shows the comparison of the previous UIMLDDPCs and the proposed AUIMLDDPC. As seen in Table 1, the topologies of TLSTSHBI, TLDTSHBI and TLDCHBI [5] require four switches. Both the UIMLDDPC [8] and the proposed AUIMLDDPC requires only three switches. Moreover, one diode in the proposed AUIMLDDPC can be saved as compared with UIMLDDPC [8]. According to the Table II, the filter capacity of the proposed AUIMLDDPC is smaller than the previous UIMLDDPCs.

5. Conclusions

This paper proposes an AUIMLDDPC generating two unequal DC voltages to form a non-zero two-level voltage by designing unequal turn numbers for two secondary windings of TWT. As seen in the experimental results, the non-zero two-level voltage is composed of 266.7 V and 400 V. The voltage swing of the output voltage in front of the output filter is only 133.3 V which is smaller than 200 V in the UIMLDDPCs [6,8]. Hence, the filter inductor (28μH) in the proposed AUIMLDDPC is smaller than that (88μH) in the UIMLDDPC [8]. Consequently, the salient features of the proposed AUIMLDDPC are that the swing voltage is further reduced and a diode is saved. the capacity of the output filter can be further reduced. In the condition of neglecting the power loss of control and driver circuits, the experimental result shows that the highest efficiency of the proposed AUIMLDDPC using Fast Recovery Epitaxial diode and CoolMOS Power MOSFET can reach to 96.76%, and the highest efficiency of the proposed AUIMLDDPC using SiC Schottky diode and SiC MOSFET can reach to 98.24%.

Table 2
Comparison of the previous UIMLDDPCs and the proposed AUIMLDDPC.

Topology	Transformer	Switch	Diode	Output filter capacity
TLSTSHBI [6]	1	4	4	Large
TLDTSHBI [6]	2	4	8	Medium
TLDCHBI [6]	1	4	6	Medium
UIMLDDPC [8]	1	3	10	Medium
AUIMLDDPC	1	3	9	Small

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