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# A novel SOI LDMOS with substrate field plate and variable-k dielectric buried layer

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ABSTRACT

A novel silicon-on-insulator (SOI) lateral double-diffused metal-oxide-semiconductor (LDMOS) structure has been proposed. The new structure features a substrate field plate (SFP) and a variable-k dielectric buried layer (VKBL). The SFP and VKBL improve the breakdown voltage by introducing new electric field peaks in the surface electric field distribution. Moreover, the SFP reduces the specific ON-resistance through an enhanced auxiliary depletion effect on the drift region. The simulation results indicate that compared to the conventional SOI LDMOS structure, the breakdown voltage is improved from 118 V to 221 V, the specific ON-resistance is decreased from 7.15 mΩ·cm$^2$ to 3.81 mΩ·cm$^2$, the peak value of surface temperature is declined by 38 K.

## Introduction

Silicon-on-insulator (SOI) technology has great advantages over bulk silicon technology in manufacturing power integrated circuit (IC), such as ideal isolation performance, low power dissipation and free of latch-up effect [1–4]. However, the vertical breakdown voltage ($V_{B,\ V}$) supported by the SOI layer and the buried oxide layer is low, which limits the application of the SOI device in the high voltage field. In order to address this limitation, some works have been carried out [5–10]. A feasible method for increasing the $V_{B,V}$ is to change the triple relationship ($E_I \approx 3E_S$) between the electric field in the buried oxide layer ($E_I$) and the electric field in the SOI layer ($E_S$) using the low-k dielectric buried layer [11,12]. Nevertheless, the low-k dielectric with the low thermal conductivity aggravates self-heating effect [13]. On another aspect, the longer drift region is usually adopted for the higher lateral breakdown voltage ($V_{B,L}$). Unfortunately, the specific ON-resistance ($R_{on,sp}$) is approximately proportional to the 2.5 times of the breakdown voltage (BV) in the conventional LDMOS, which dramatically worsens $R_{on,sp}$ as the BV increases. To alleviate the contradiction between BV and $R_{on,sp}$, the reduced surface field (RESURF) technology, the field plate technology and the super-junction technology are widely used [14–17]. However, the field plate biased to the gate will increase $C_{gd}$ and reduce the second mechanism in RF power LDMOS devices [18,19]. The field plate biased to the source can decrease $C_{gd}$, but the JFET effect degrades the drain current [20]. In order to make the substrate share $V_{B,\ V}$ and alleviate the self-heating effect, Partial SOI technology has been adopted in some works [21–29]. However, the higher leakage current and thermomechanical stress in the PSOI LDMOS lead to significant device reliability problems [30].

In this paper, we propose a novel silicon-on-insulator lateral double-diffused metal-oxide-semiconductor (LDMOS) with substrate field plate and variable-k dielectric buried layer (SFP-VK LDMOS). The substrate field plate (SFP) composed of polysilicon not only introduces new electric field peaks and modulates the surface electric field, but also depletes the drift region auxiliarily. The variable-k dielectric buried layer (VKBL) further optimizes the surface electric field. Meanwhile, the electric field of dielectric buried layer is enhanced by the low-k dielectric under the drain. In addition, the higher thermal conductivity of polysilicon and the window connected SFP with the substrate alleviate self-heating effect. Compared to the conventional field plate structure, the higher FOM of SFP-VK LDMOS is achieved. The $C_{gs}$ and $C_{gd}$ which affect the dynamic performances of the device are reduced in the proposed structure. Moreover, SFP located in the dielectric buried layer has little impact on the current flowing along the surface of device, so the current degradation caused by hot carrier effect and JFET effect is suppressed.

## Structure and mechanism

The schematic cross section of the proposed SFP-VK LDMOS is illustrated in Fig. 1(a). The step SFP is inserted into the dielectric buried layer, and connected to the substrate through a silicon window under the source. The VKBL is divided into two parts. One is low-k dielectric buried layer located at the drain side, and another is silica. In the lateral direction, the SFP and VKBL introduce two new electric field peaks, which reduce the electric field peaks at the two PN junctions in the

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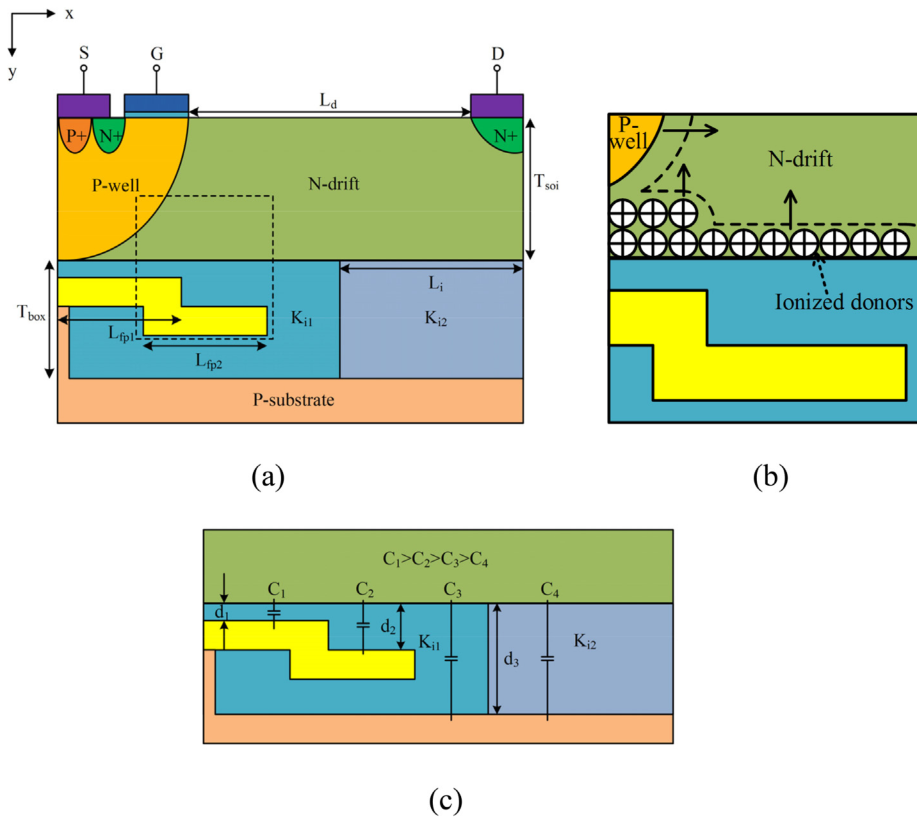



**Fig. 1.** (a) Schematic cross section of the proposed SFP-VK LDMOS. (b) Schematic of the SFP (solid arrow denotes the direction of the depletion). (c) Depletion mechanism in the vertical direction.

**Table 1**
Device parameters used in the simulation.

| Parameter | SFP-VK LDMOS | C-LDMOS |
|---|---|---|
| Drift length, $L_d$ | 10 µm | 10 µm |
| Drift concentration, $N_d$ | $1.9 \times 10^{16}$ cm$^{-3}$ | $0.8 \times 10^{16}$ cm$^{-3}$ |
| Thickness of SOI layer, $T_{soi}$ | 1 µm | 1 µm |
| Thickness of BOX layer, $T_{box}$ | 1 µm | 1 µm |
| Top part length of SFP, $L_{fp1}$ | 4 µm | – |
| Bottom part length of SFP, $L_{fp2}$ | 4 µm | – |
| Permittivity of left BOX layer, $K_{i1}$ | 3.9 | 3.9 |
| Permittivity of right BOX layer, $K_{i2}$ | 2 | 3.9 |
| Length of right BOX layer, $L_i$ | 5 µm | – |
| Substrate concentration, $N_{sub}$ | $3 \times 10^{14}$ cm$^{-3}$ | $3 \times 10^{14}$ cm$^{-3}$ |

lateral P-well/N-drift/N+ structure, and modulate the electric field distribution together along the device surface. In the vertical direction, the low-k dielectric buried layer share more vertical voltage under the drain than the silica in the conventional SOI-LDMOS structure, thus shields the silicon layer and avoid the premature breakdown under the drain.

As shown in Fig. 1(a) which depicts the proposed SFP-VK LDMOS, $L_i$ and $L_d$ represent the length of the low-k dielectric buried layer and the drift region, respectively. $L_{fp1}$ and $L_{fp2}$ denote the length of the top part and the bottom part of the SFP, respectively. $T_{box}$ and $T_{soi}$ are the thickness of the buried oxide layer and the SOI layer, respectively. $K_{i1}$ and $K_{i2}$ denote the permittivity of the silica and low-k dielectric, respectively.

In the off state, the SFP is biased to the ground through the silicon window. The potential of the SFP relative to the drift region is negative, thus depletes drift region auxiliarily in the vertical direction, as shown in Fig. 1(b). It is noteworthy that the number of ionized donors varies with the distance between SFP and SOI layer. The SOI layer/dielectric buried layer/substrate can be considered as the MIS capacitance. We assume that $C_1$, $C_2$, $C_3$ and $C_4$ are capacitances per unit area in different regions, as shown in Fig. 1(c). According to the condition of $d_3 > d_2 > d_1$ and $K_{i1} > K_{i2}$, $C_1 > C_2 > C_3 > C_4$ can be deduced, so the depletion of the drift region in the vertical direction becomes gradually weakened from source to drain. It is known that low-K dielectric improves vertical breakdown voltage, but weakens the depletion in the drift region on the basis of the previous analysis. The introduction of SFP in the dielectric buried layer enhances auxiliary depletion and offsets the negative effect on drift region concentration due to low-k dielectric. Therefore, excellent device performance can be achieved with the combination of the SFP and VKBL.

The performance of the SFP-VK LDMOS is investigated using Silvaco TCAD. The physical models include CVT, CONSRH, AUGER, CONMOB, FLDMOB, LAT.TEMP and IMPACT. The Gummel and Newton iterative algorithms are used to solve the Poisson equation and the drift-diffusion equation. The conventional LDMOS structure (C-LDMOS) is also simulated for the sake of comparison. The related device parameters of the two structures are listed in Table 1.

The SFP-VK LDMOS and C-LDMOS have been optimized to satisfy the RESURF principle. The ionization rate distribution for both the conventional and the proposed structures at breakdown are given in Fig. 2(a) and (b). The lower impact generation rate of the device surface compared to the bulk indicates the surface electric field is reduced and thus breakdown points are transferred to the bulk.

Fig. 3(a) and (b) illustrate the equipotential contours distributions at breakdown for the proposed structure and C-LDMOS, respectively. In Fig. 3(a), the equipotential lines in the SFP-VK LDMOS are very dense and uniformly spaced along the horizontal direction due to the reshape effect of the SFP and VKBL. However, the equipotential lines of the C-LDMOS in Fig. 3(b) mainly distribute in the two ends of the drift region, and rarely in the middle. It makes the source and drain side easier to accumulate high electric field and cause surface breakdown. Comparing the number of equipotential lines in the black dashed rectangular, the

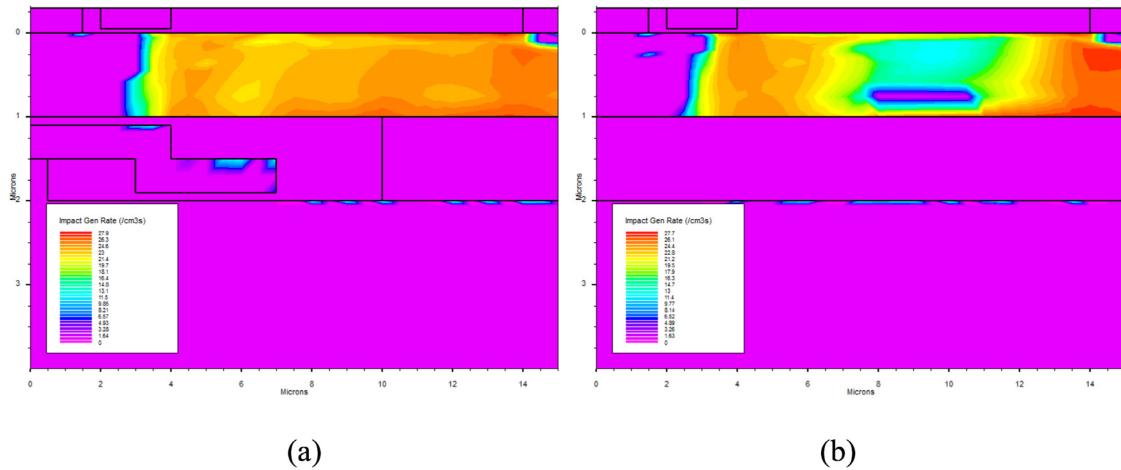



**Fig. 2.** The ionization rate distribution at breakdown: (a) SFP-VK LDMOS; (b) C-LDMOS.

potential distribution of C-LDMOS is more intensive than SFP-VK LDMOS under the drain, indicating that the low-k dielectric buried layer in the SFP-VK LDMOS shields the SOI layer. Therefore, the higher breakdown voltage can be reached in the SFP-VK LDMOS.

Fig. 4(a) shows the comparison of the OFF-state I-V characteristics between the proposed structure and C-LDMOS. It is obvious that the BV of the SFP-VK LDMOS reaches 221 V, while that of C-LDMOS is only 118 V. Compared to the C-LDMOS, the BV of the SFP-VK LDMOS has been improved by 87.3%. Fig. 4(b) provides the comparison of output I-V characteristic curves between the two structures. When $V_{GS} = 7.5$ V and $V_{DS} = 40$ V, the drain current of SFP-VK LDMOS is up to $1.4 \times 10^{-4}$ A/μm, which is increased by 37% in comparison with $1.02 \times 10^{-4}$ A/μm of C-LDMOS. The drain current of SFP-VK LDMOS at $V_{GS} = 5.5$ V is a little smaller than C-LDMOS, but nearly equals at $V_{GS} = 6.5$ V due to the quasi-saturation effect of C-LDMOS at $V_{GS} \geq 6.5$ V. In the linear region, the curves belonged to SFP-VK LDMOS are steeper than C-LDMOS, indicating that the lower specific ON-resistance can be obtained in the former. Therefore, stronger current output capability can be achieved in the proposed structure.

Fig. 5(a) shows surface electric field distribution in the two structures at y = 0.001 μm. For the SFP-VK LDMOS, it is clear that two new electric peaks A and B are introduced due to the SFP and VKBL. Moreover, the peaks O and O' decrease compared to the peaks P and P′ of C-LDMOS, indicating a more even electric field distribution along the surface. It is noted that the average electric field strength of the proposed structure in the central section of the drift region is about $2 \times 10^{5}$ V/cm, which is much higher than $7 \times 10^{4}$ V/cm of the C-LDMOS. Therefore, the area under the electric field curve along the surface of the proposed structure is much larger than that of C-LDMOS, indicating higher breakdown voltage in the former. Fig. 5(b) illustrates the electric field distribution in the proposed structure along y = 0.001 μm and y = 0.999 μm. Obviously, peaks A′ and B′ correspond to peaks A and B, respectively. This further confirms that the electric field modulation effect along the surface is produced by the SFP and VKBL.

Fig. 6 provides the vertical electric field and potential distribution at breakdown under the drain in the two structures. For the SFP-VK LDMOS, the $E_I$ (represents the electric field strength in the BOX layer) is approximately 200 V/μm and the $E_S$ (represents the electric field strength in the SOI layer) is about 33 V/μm, which nearly satisfies the expression $E_I \approx 6E_S$. It is noted that the $E_I$ in the C-LDMOS is only 95 V/μm, which is much lower than the $E_I$ in the proposed structure due to the higher permittivity of BOX layer under the drain. As revealed in Fig. 6, the BOX layer in the proposed structure shares more voltages than that of the C-LDMOS, leading to a higher vertical breakdown voltage.

## Results and discussion

Fig. 7(a) and (b) show BV of the SFP-VK LDMOS versus the $N_d$ with different $L_{fp1}$, $K_{i1}$ and $K_{i2}$. As shown in Fig. 7(a), the peak of the breakdown voltage first increases and then decreases as $K_{i1}$ increases from 2 to 6. Too small or too large $K_{i1}$ will increase the difference between $K_{i1}$ and $K_{i2}$, which will lead to an exorbitant electric field peak

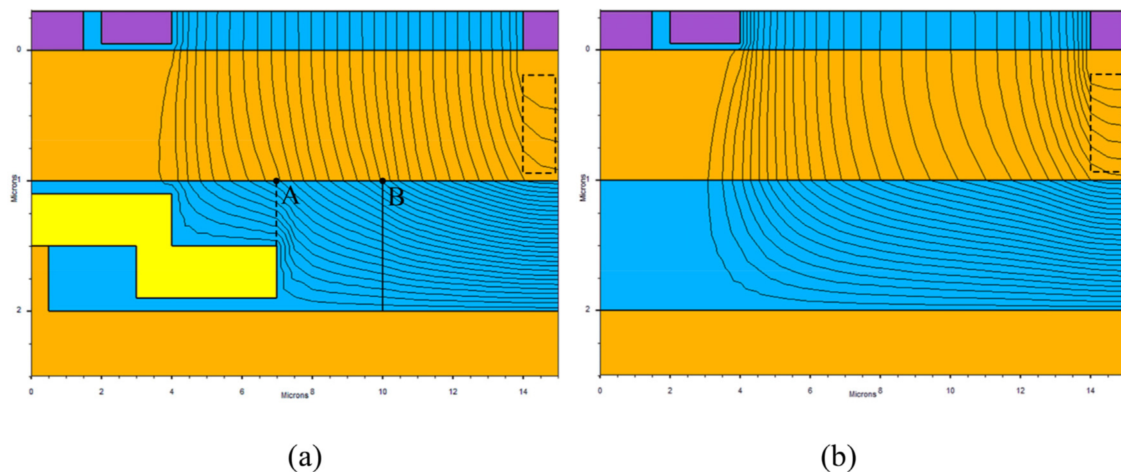



**Fig. 3.** Equipotential contours distributions at breakdown: (a) SFP-VK LDMOS; (b) C-LDMOS.

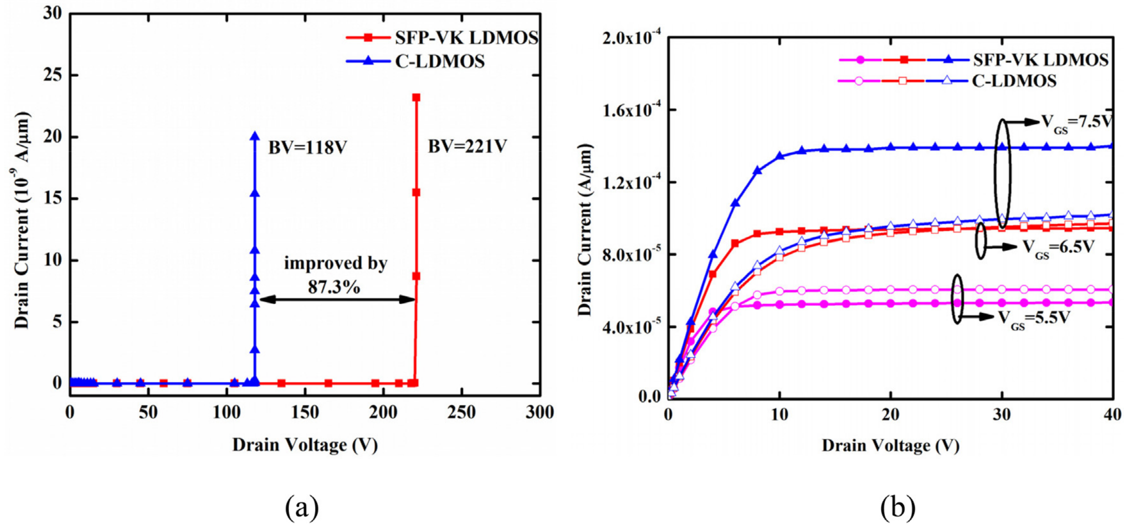



**Fig. 4.** (a) OFF-state I-V characteristics. (b) Output I-V characteristics.

produced by VKBL. Therefore, the optimal value can be reached at $K_{i1} = 3$ or $K_{i1} = 3.9$. Similarly, 2 is selected as the optimal value of $K_{i2}$. As illustrated in Fig. 7(b), it is remarkable that the peak of the breakdown voltage decreases from 221 V to 196 V as the $L_{fp1}$ increases from 4 μm to 6 μm. Too large $L_{fp1}$ means the top part of the SFP extends too much to the right, which makes the effect of the electric field modulation become worse. Since too small $L_{fp1}$ will weaken the auxiliary depletion, 4 μm is selected as the optimal value of $L_{fp1}$. Similarly, base on the RESURF principle, 4 μm and 5 μm are selected as the optimal value of $L_{fp2}$ and $L_i$, respectively.

Fig. 8(a) and (b) illustrate the electric field distribution with different $L_{fp2}$ and $L_i$ along y = 0.999 μm. As shown in Fig. 8(a), the electric peak produced by SFP shifts from A1 to A3 as the $L_{fp2}$ increases from 3 μm to 5 μm. Since the field distribution is of the most uniform when the value of $L_{fp2}$ is 4 μm, it is selected as optimal value. Similarly, the electric peak produced by VKBL shifts from B3 to B1 as the $L_i$ increases from 4 μm to 6 μm, as illustrated in Fig. 8(b). Owing to the more even electric field distribution, optimal value of $L_i$ is selected as 5 μm.

Fig. 9(a) and (b) show $R_{on,sp}$ of the SFP-VK LDMOS versus the $N_d$ with different $L_{fp1}$ and $L_{fp2}$. The insets in Fig. 9(a) and (b) are $R_{on,sp}$ versus $N_d$ when BV reaches the maximum value. For $N_d > 1 \times 10^{16}\,cm^{-3}$, the $R_{on,sp}$ nearly doesn't vary with $L_{fp1}$ and $L_{fp2}$, because depletion region produced by SFP almost doesn't affect the

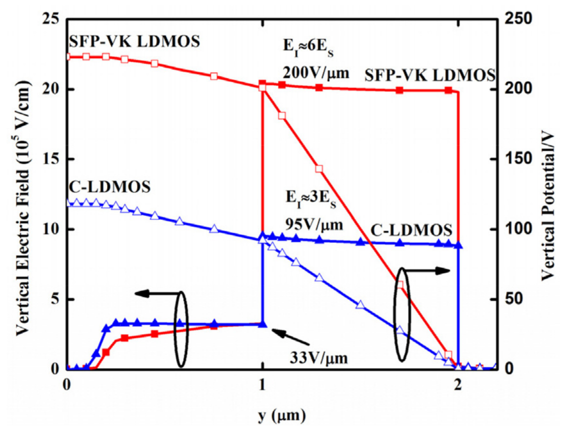



**Fig. 6.** Vertical electric field and potential distribution at breakdown under the drain for SFP-VK LDMOS and C-LDMOS.

current flowing along the device surface, which is beneficial to the reduction of $R_{on,sp}$. It can be seen from the insets that the $R_{on,sp}$ get the minimum value while both $L_{fp1}$ and $L_{fp2}$ equal 4 μm.

Fig. 10(a) and (b) show dependences of $R_{on,sp}$ on $K_{i1}$, $K_{i2}$, $L_i$, $L_{fp1}$ and

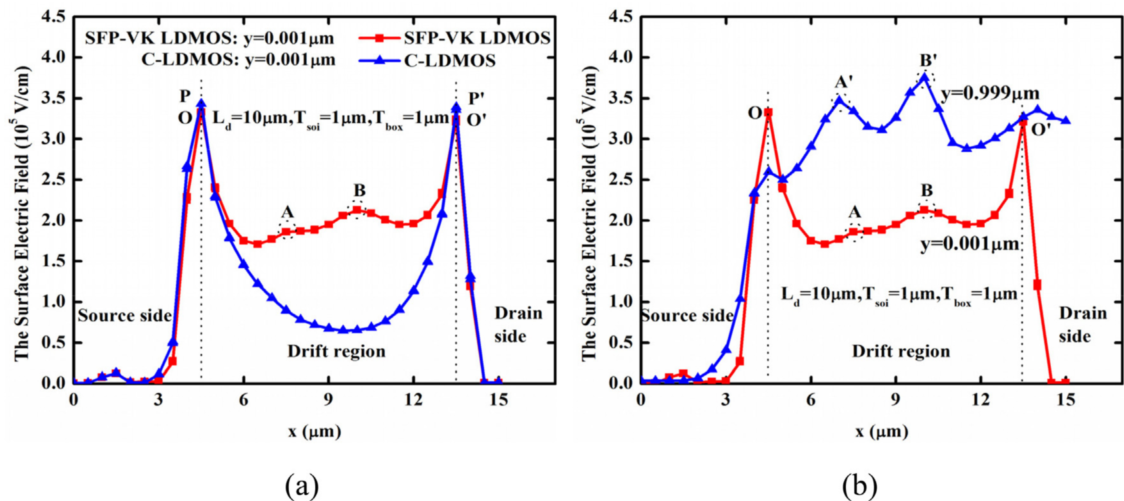
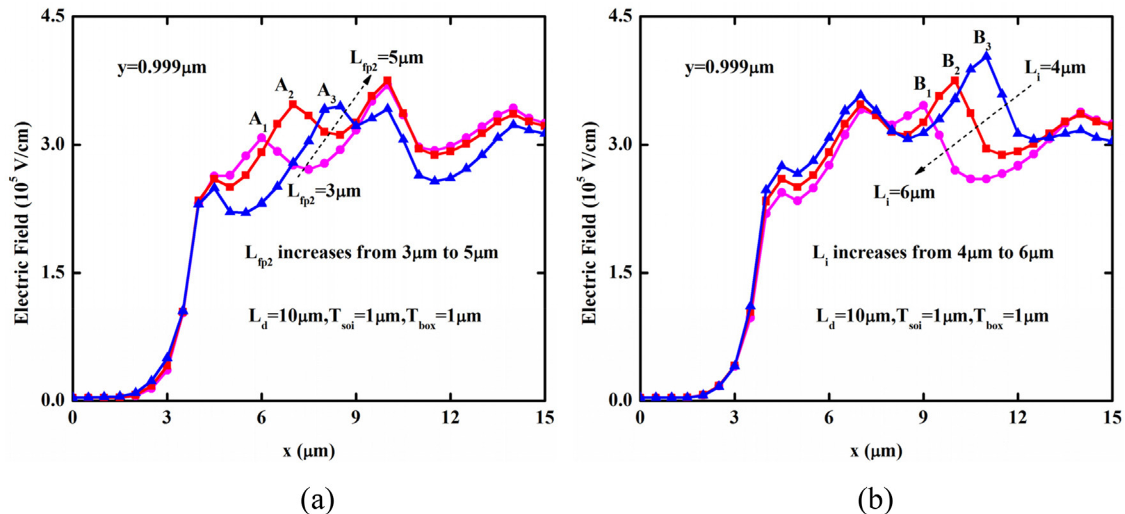



**Fig. 5.** (a) Surface electric field distribution for SFP-VK LDMOS and C-LDMOS. (b) The electric field distribution along y = 0.001 μm and y = 0.999 μm.

(a)

(b)

**Fig. 7.** (a) BV of the SFP-VK LDMOS versus the $N_d$ with different $K_{i1}$ and $K_{i2}$. (b) BV of the SFP-VK LDMOS versus the $N_d$ with different $L_i$, $L_{fp1}$ and $L_{fp2}$.




(a) (b)

**Fig. 8.** (a) The electric field distribution with different $L_{fp2}$ along y = 0.999 μm. (b) The electric field distribution with different $L_i$ along y = 0.999 μm.

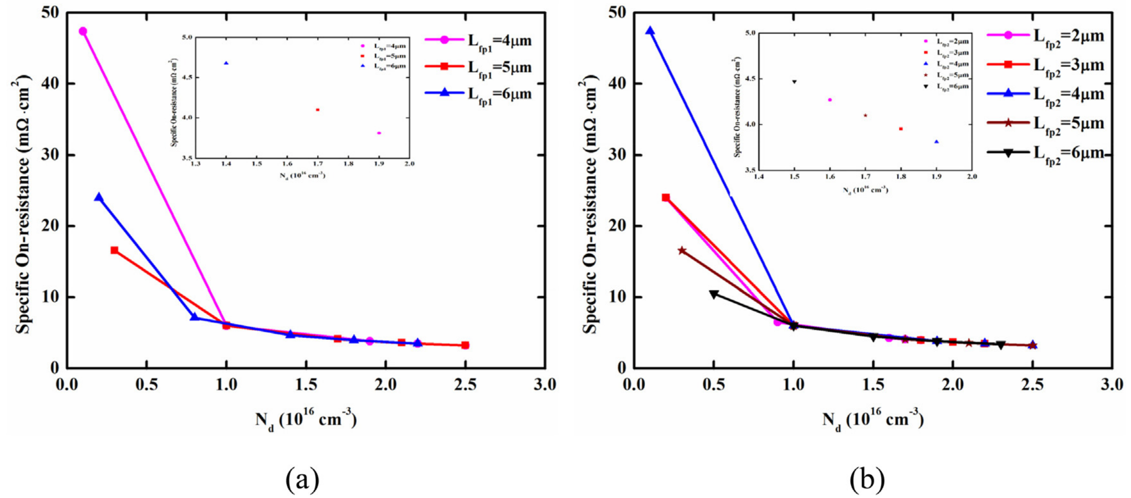



**Fig. 9.** (a) $R_{on,sp}$ of the SFP-VK LDMOS versus the $N_d$ with different $L_{fp1}$. (b) $R_{on,sp}$ of the SFP-VK LDMOS versus the $N_d$ with different $L_{fp2}$. (The insets represent $R_{on,sp}$ versus $N_d$ at the maximum BV).

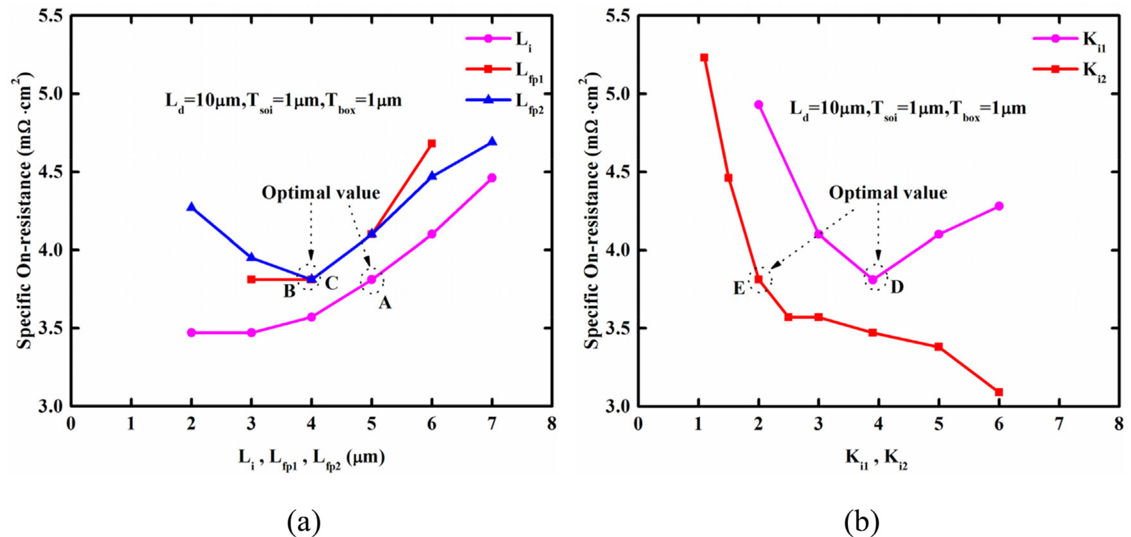



**Fig. 10.** (a) Dependences of $R_{on,sp}$ on $L_i$, $L_{fp1}$ and $L_{fp2}$ for the SFP-VK LDMOS. (b) Dependences of $R_{on,sp}$ on $K_{i1}$ and $K_{i2}$ for the SFP-VK LDMOS.

$L_{fp2}$ for the SFP-VK LDMOS. Obviously, the $R_{on,sp}$ monotonously decreased with the increase of $K_{i2}$ or the decrease of $L_i$. When $K_{i2} > 2$ or $L_i < 5\,\mu m$, the curves show a slowly declined trend. It is also clear that the $R_{on,sp}$ can obtain minimum values when $L_{fp1}$, $L_{fp2}$ and $K_{i1}$ equal 4 μm, 4 μm and 3.9, respectively. Considering both the BV and $R_{on,sp}$, the optimal values of five parameters are selected, as shown in Fig. 10(a) and (b).

Fig. 11(a) and (b) illustrate the lattice temperature distributions in the proposed structure and C-LDMOS. The substrate temperature is 300 K, and the voltage applied to the gate is 6.5 V. As shown in Fig. 11(a), the temperature of SFP-VK LDMOS is lower than C-LDMOS. The max temperature of the SFP-VK LDMOS is 332 K and 343 K at $V_{DS} = 15$ V and $V_{DS} = 20$ V, while that of C-LDMOS is 358 K and 381 K. As revealed in Fig. 11(b), it can be found that the maximum temperature of SFP-VK LDMOS occurs at the source side and that of C-LDMOS at the drain side. Moreover, the temperature fluctuation of C-LDMOS is bigger than SFP-VK LDMOS in the SOI layer. It indicates the heat cannot be dissipated through the BOX layer of the former in time and accumulates in the SOI layer, which is easier to form local hot spots. In contrast to C-LDMOS, the higher thermal conductivity of the polysilicon SFP in the proposed structure makes the temperature decrease steeply near the SFP, and thus limits the generation of local hot spots.

Fig. 12(a) and (b) show $C_{gs}$ and $C_{gd}$ of three different field plate structures. The same device size is used except the length of the field plate, which is dependent on the maximum BV. It is noted that the smallest $C_{gs}$ is obtained using substrate field plate. Moreover, the $C_{gd}$ of substrate field plate structure is closed to that of source field plate structure. Therefore, the best dynamic performance is achieved in the substrate field plate structure.

Fig. 13 compares the tradeoff relationship between the BV and $R_{on,sp}$ for the proposed device and other LDMOS devices. The results indicate that the performance of the proposed structure breaks through the limit of silicon due to the well-distributed surface electric field with the larger mean of the lateral electric field. It is notable that the highest FOM value (FOM = $BV^2/R_{on,sp}$) is obtained in the proposed structure, which proves to have a better compromise between the BV and $R_{on,sp}$.

Fig. 14 shows the simple process flow of SFP-VK LDMOS. Before the fabrication, two wafers should be prepared. Step (a) is to form the silicon window for the connecting between substrate and SFP. Steps (b) and (c) are to etch the oxide trench for the SFP. Steps (d) and (e) are to etch polysilicon for the shape of SFP. Steps (f)–(h) are for the formation of VKBL by etching oxide and CVD low-K dielectric. Step (i) are for the bonding between wafer1 and wafer2. Step (j) includes the remaining processes which are the same as traditional CMOS processes.

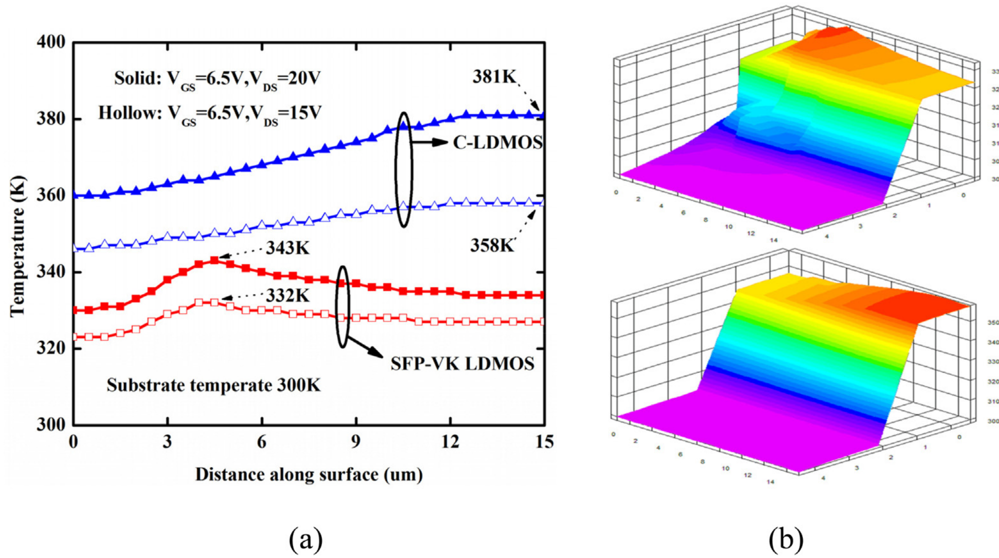



**Fig. 11.** (a) The lattice temperature distributions of the SFP-VK LDMOS and C-LDMOS along y = 0.001 μm. (b) The lattice temperature distribution of the SFP-VK LDMOS and C-LDMOS. ($V_{GS}$ = 6.5 V, P = 1 mW/μm).

### Conclusions

In summary, a novel SFP-VK LDMOS is proposed. The SFP modulates the surface electric field and enhances the auxiliary depletion effect in the vertical direction. The VKBL increases the electric field in the dielectric buried layer under the drain and further optimizes the surface electric field. The BV is dramatically improved owing to the well-distributed electric field produced by the SFP and VKBL. Moreover, the enhanced auxiliary depletion effect of the SFP effectively reduces the $R_{on,sp}$. The BV of the SFP-VK LDMOS is improved by 87.3% and the $R_{on,sp}$ is decreased by 46.7% in comparison with the C-LDMOS. Meanwhile, the temperature characteristics are superior to that of the C-LDMOS [31–39].

### Acknowledgments

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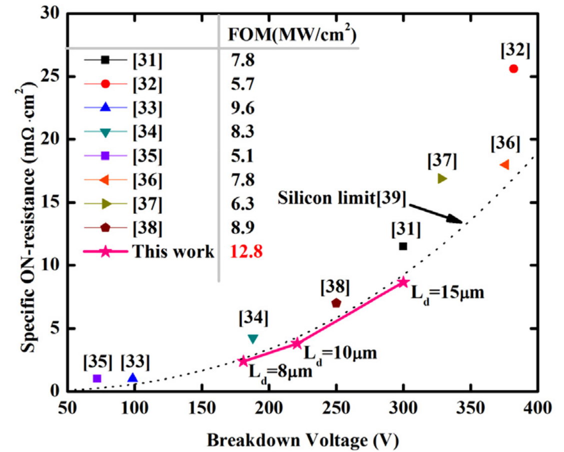


**Fig. 13.** BV versus $R_{on,sp}$ tradeoff relationship for different types of LDMOS and this brief.

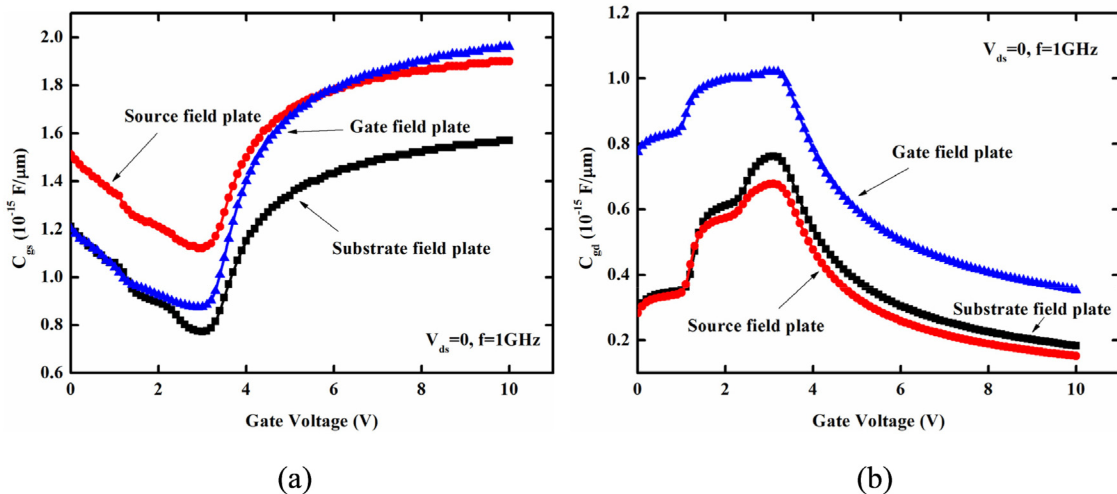


**Fig. 12.** Capacitance versus gate voltage in three different field plate structures ($V_{ds}$ = 0, f = 1 GHz): (a) $C_{gs}$; (b) $C_{gd}$.

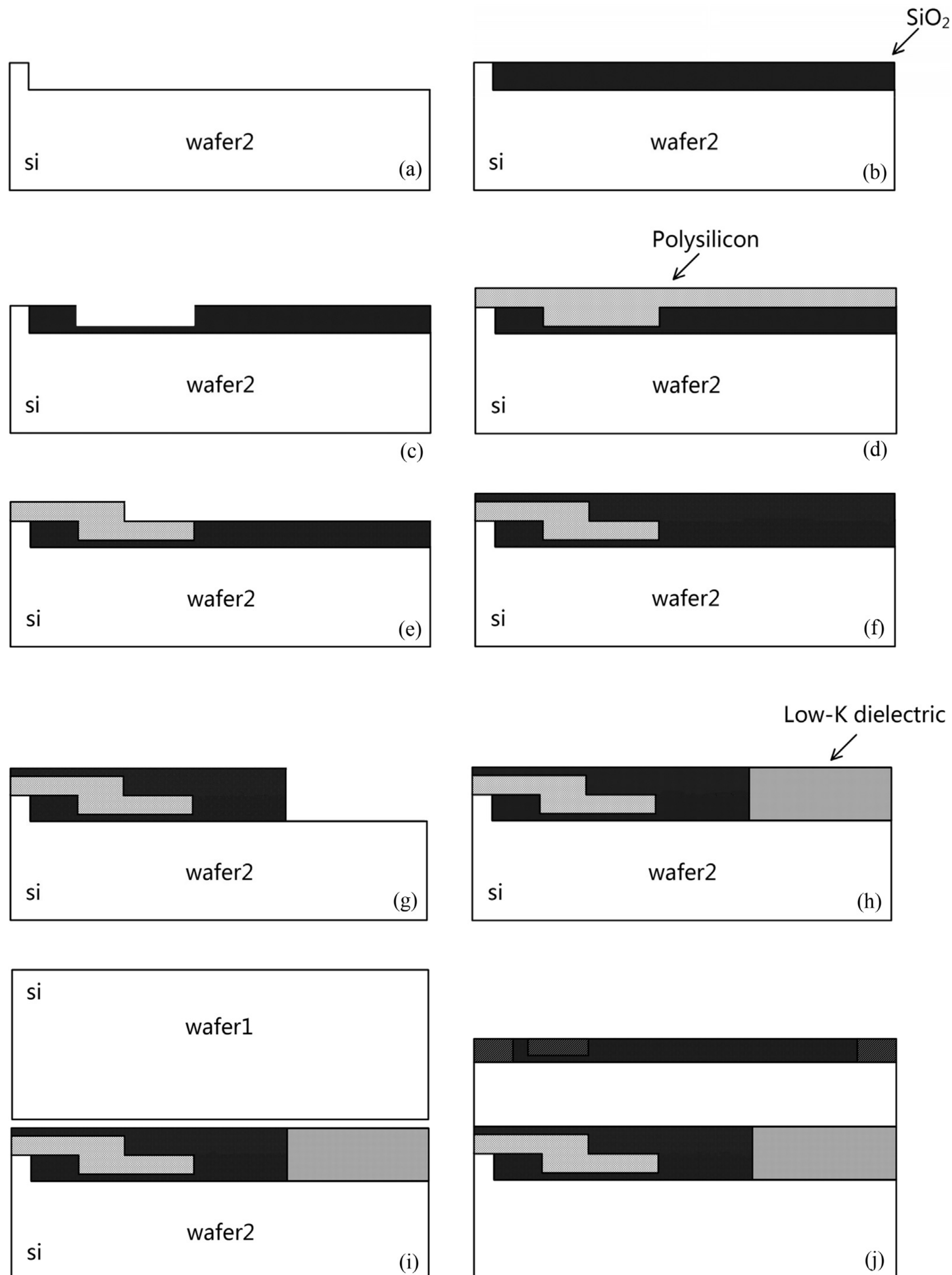


**Fig. 14.** The simple process flow of SFP-VK LDMOS: (a) etching wafer2; (b) CVD SiO2; (c) etching SiO2; (d) CVD polysilicon; (e) etching polysilicon; (f) CVD SiO2; (g) etching SiO2; (h) CVD low-K dielectric; (i) bonding wafer1 and wafer2; (j) complete the preparation of the remaining part of the device.

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