Results in Physics 10 (2018) 964–966

Contents lists available at ScienceDirect

Results in Physics

journal homepage: www.elsevier.com/locate/rinp

Characteristic of an adiabatic charging reversible circuit with a Lithium ion capacitor as an energy storage device

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ARTICLE INFO

Keywords:
Adiabatic
Reversible circuit
Lithium ion capacitor
Stepwise charging

ABSTRACT

An adiabatic reversible circuit was designed for charging a Lithium ion capacitor. The duty ratio of the switching transistors is digitally controlled by a microprocessor. A Lithium ion capacitor has the minimum and the maximum operating voltage. Therefore, the charging voltage is set to be in that range. Using this energy storage system, it is clarified from the experiment that the efficiency is 95.5% during charging and also discharging process. Then the total efficiency is 91.2% during one cycle, which is the best value in the proposed stepwise adiabatic charging circuit.

Reversible circuit is attracting much attention in physics and also electrical engineering [1–11] because it has the characteristic of dissipationless charging of a supercapacitor. Until now, the previous experiment shows that charging efficiency is 94.0% when an electric double-layer capacitor (EDCL) is used [11]. However, the charging and discharging efficiency during one cycle is not discussed well. Therefore, the total efficiency is discussed in this article. In this experiment, to charge a capacitor fast and also efficiently, electric components, such as an inductor and transistors, are set on a printed wiring board by soldering. Due to this, circuit resistance is much decreased. Also a Lithium ion capacitor (LiC) is used because of its higher energy density per volumes than EDCL. This enables a compact energy storage system.

Fig. 1 shows an adiabatic circuit. A microprocessor (PIC16F627A) is used to output the Pulse Width Modulation (PWM) signal [9,11]. Power supply voltage is 5.0 V. Therefore, high and low voltage is 5 and 0 V. The PWM signal is input to inverter (4049B) for increasing current drivability. The output of the inverter is input to the gate of power MOSFETs. The pMOS and nMOS transistors are 2SJ438, and 2SK2231, respectively. The output of two power MOSFETs, is connected to LiC through the inductor. In this article, for realizing a compact storage system, LiC is used instead of EDCL as discussed already. The LiC has the maximum operating voltage, 3.8 V, and the minimum, 2.2 V. Therefore, the output voltage is set to be in this range. The power supply voltage of power MOSFETs is set as 3.56 V. During charging, d is changed from 64/96, 68/96, …, 92/96, 1. During discharging, d is changed from 1, 92/96, …, 68/96, 64/96. Three physical values were measured. One is the capacitor voltage, V_C, another is the current from the inductor to the capacitor, I_C, and the other is the current from the power supply to the inductor, I_P. These were measured with three digital multimeters.

Fig. 2 shows the timewise change in V_C. Here, the number of voltage steps is eight. V_C is in the range of 2.4–3.5 V, which corresponds to $d = 0.667$ and $d = 1$. If charging time is sufficiently long, V_C will reach to the power supply voltage, 3.56 V. Fig. 3 shows the timewise change in I_C. During charging ($0 \le t \le 380$ s), I_C is positive, while it is negative during discharging ($380 \le t \le 760$ s). This means the current direction is opposite. Fig. 4 shows charge amount Q flowing into capacitor, which is written as $Q = \int I_C\, dt$. The charge amount difference ΔQ between the maximum and the minimum is 38.9C from Fig. 4. On the other hand, the voltage difference ΔV between the maximum and the minimum is 1.08 V from Fig. 2. Then, the capacitance value is estimated as 38.9/1.08 = 35.9F.

Fig. 5 shows the timewise change in I_P. When the capacitor is charged and discharged, I_P is positive and negative. This means that, during discharging, the current flows from the capacitor to the power supply through the inductor.

Here, charging efficiency η_1 is considered. During charging, the work done by the power supply W_1 is written as $Q_1 V$, where Q_1 is the charge amount flowing *from* power supply and V is the power supply voltage. Q_1 is written as $Q_1 = \int I_P\, dt$. Then, Q_1 is shown in Fig. 6 and the value is 33.3C. The V is 3.56 V, so W_1 is estimated to be 118.4 J. On the other hand, the increase in electrostatic energy during charging E_1 is written as $E_1 = C({V_M}^2 - {V_{m1}}^2)/2$, where V_M is the maximum capacitance voltage and V_{m1} is the minimum one during charging. The V_M and V_{m1} are 3.48 and 2.41 V, respectively. The C is 35.9F. Using these values, E_1 is calculated to be 113.0 J. The η_1 is defined as E_1/W_1 and calculated to be 95.5%.

Next, the discharging efficiency η_2 is calculated in the same way.

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https://doi.org/10.1016/j.rinp.2018.08.016
Received 2 May 2018; Received in revised form 7 August 2018; Accepted 7 August 2018
Available online 12 August 2018

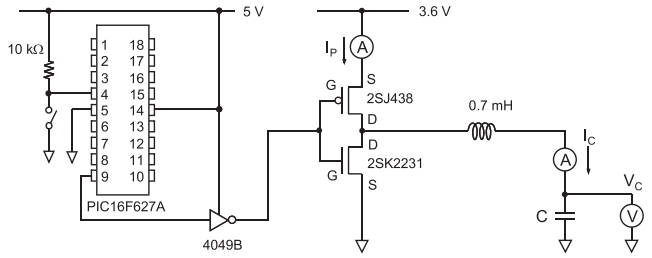

Fig.1. Circuit controlled by microprocessor and measurement system.

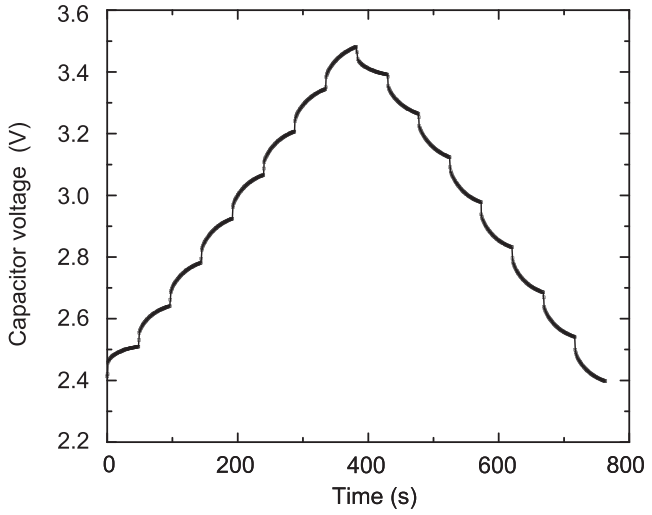

Fig. 2. Capacitor voltage as a function of time.

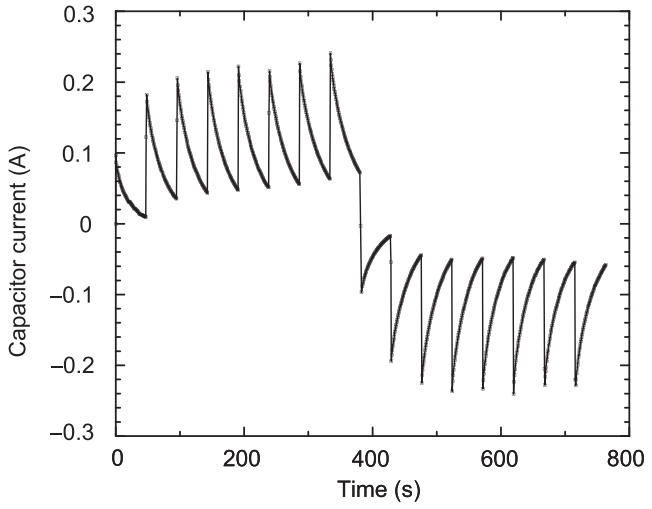

Fig. 3. Capacitor charging current as a function of time.

During discharging, the work received by the power supply W_2 is written as Q_2V, where Q_2 is the charge amount flowing *into* power supply during discharging. The Q_2 is shown in Fig. 6 and the value is 30.7C. So W_2 is estimated to be 109.3 J. On the other hand, the decrease in electrostatic energy during discharging E_2 is written as $E_2 = C(V_M{}^2 - V_{m2}{}^2)/2$, where V_{m2} is the minimum capacitance voltage during discharging. The V_{m2} is 2.40 V. Then, E_2 is calculated to be 114.4 J. The η_2 is defined as (W_2/E_2) and calculated to be 95.5%.

The total efficiency η during charging and discharging is calculated as $\eta = \eta_1\eta_2$ and it is 91.2%. Next, the relation between η and the value of Q_2/Q_1 is considered. The η_1 and η_2 are E_1/W_1 and W_2/E_2. The E_1 is almost equal to E_2 in this experiment, and this is satisfied in the usual

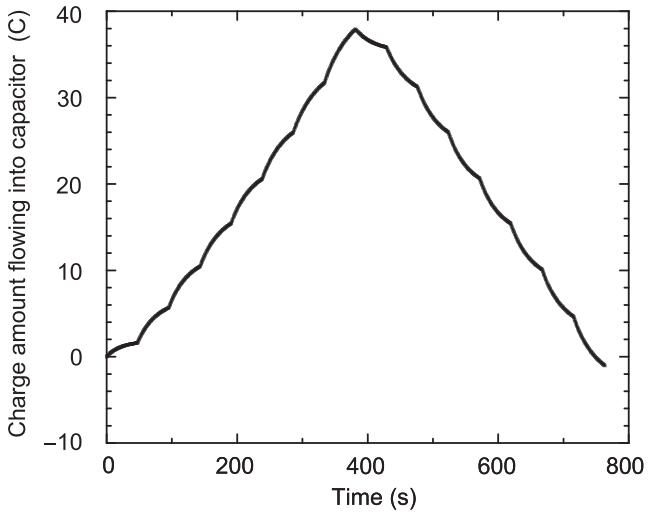

Fig. 4. Charge amount flowing into capacitor.

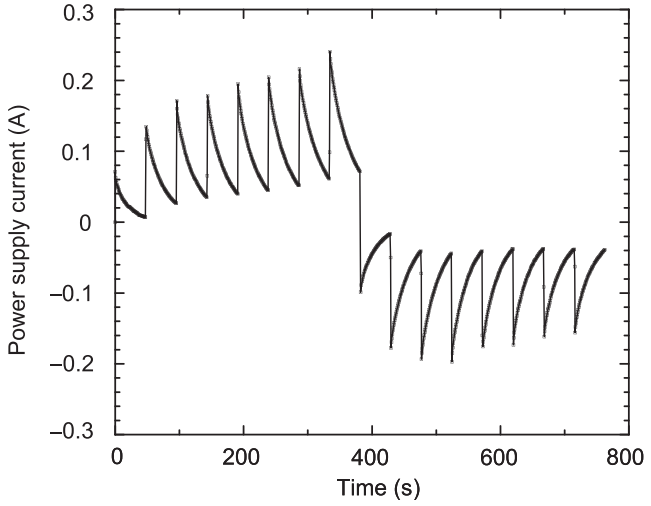

Fig. 5. Power supply current as a function of time.

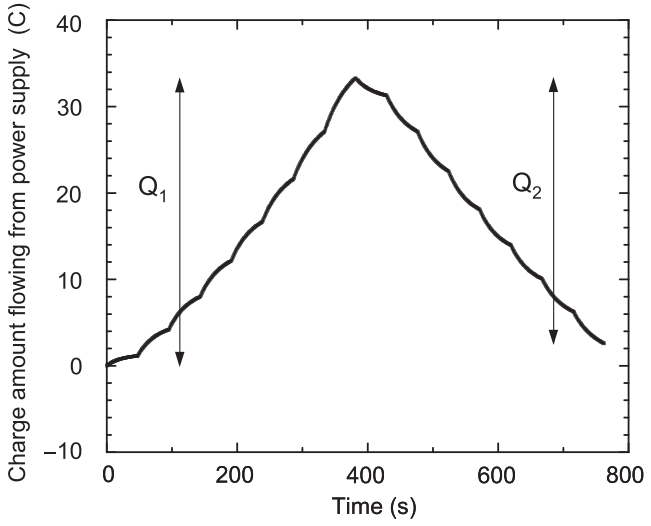

Fig. 6. Charge amount flowing from power supply.

case. So, η is almost equal to $W_2/W_1 = Q_2/Q_1$. Therefore, if Q_2 is close to Q_1, η approaches to 1. In the previous work, the value of Q_2/Q_1 is 0.75, which means η is not high [11]. On the other hand, in this work,

the value of Q_2/Q_1 is high and it is 0.923 from Fig. 6: it is not just the same as η because E_1 is not equal to E_2 strictly.

Here, the resistance of the circuit R is discussed. In [11], R was 3 Ω. This value is mainly due to the resistance of the wire on the breadboard and also the contact resistance between electronic components and the wire. On the other hand, due to the soldering, R in this article decreases to 0.6 Ω. This results from the switching transistor resistance, 0.2 Ω, inductor resistance, 0.1 Ω, and the wire resistance, 0.3 Ω.

As the resistance of pMOS and nMOS transistor is the same value as 0.2 Ω, the energy dissipation of the circuit E_{diss} is calculated to be $\int RI_C^2 dt$. The R is 0.6 Ω. The average current flowing *into* or *from* the capacitor is 0.15 A from Fig. 3. The charging time T is 380 s. Then, E_{diss} is estimated to be $0.6 \times 0.15^2 \times 380 = 5.13$ J. During charging, W_1 is 118.4 J and E_1 is 113.0 J. Then, E_{diss} is calculated as $W_1 - E_1 = 5.4$ J, which is almost consistent with the estimated value. During discharging, E_2 is 114.4 J and W_2 is 109.3 J. In this case, E_{diss} is calculated as $E_2 - W_2 = 5.1$ J, which is consistent with the estimated value. This discussion shows that the circuit resistance 0.6 Ω is valid.

If SiC transistors and the inductor with the lower resistance are used, it will reduce R more. The charging circuit with the low resistance would enable a large current flow. This means high speed operation would be possible.

Next, the theoretical charging efficiency η_{1th} is discussed. Here, V_C is assumed to change from $2V/3$ to V, which is the same as the experimental situation. The stepwise value of V_C is changed as $2V/3$, $17V/24$, $18V/24$, … , $23V/24$, and $24V/24$. In the first step during charging, V_C is charged from $2V/3$ to $17V/24$. Then, the charge amount of $CV/24$ flows into capacitor. The d is $2/3 + 1/24 = 17/24$, so the charge amounts from the power supply and GND are $17CV/24^2$ and $7CV/24^2$, respectively [9]. We define W_{si} as the work done by the power supply during the ith step charging. Then, W_{s1} during the first step is written as $W_{s1} = 17CV^2/24^2$. Similarly, in the second step, V_C is charged from $17V/24$ to $18V/24$, and the charge amount of $CV/24$ flows into capacitor. From $d = 18/24$, the charge amount from the power supply is $18CV/24^2$. Therefore, W_{s2} during the second step is written as $W_{s2} = 18CV^2/24^2$. Then, the total work $W_{s1\text{-}8}$ during charging is calculated as $W_{s1\text{-}8} = (17 + 18 + \cdots + 23 + 24)CV^2/24^2 = 41CV^2/144$. On the other hand, E_1 is written as $E_1 = C(V^2 - 4V^2/9)/2 = 5CV^2/18$. Therefore, η_{1th} is calculated to be $\eta_{1th} = E_1/W_{s1-8} = 97.6\%$. This value is almost consistent with the experimental value. The theoretical discharging efficiency η_{2th} is calculated in the same way and it is 97.5%, which is also almost consistent with the experiment.

Next, we consider the situation that the step width is not equal. Here, the following case of V_C change is considered: $2V/3$, $2V/3$, $13V/18$, $13V/18$, $14V/18$, $15V/18$, $16V/18$, $17V/18$, $18V/18$, which is the same as the six-step charging. In this case, η_{1th} is similarly calculated to be 96.8%. Therefore, inequality of the steps causes the decrease in charging efficiency. However, this decrease is very small and negligible in eight-step charging.

In this experiment, the high η value is realized. It is due to the realization of low resistance in the circuit due to setting on a printed wiring board. This high efficiency shows the proposed circuit is suitable for an energy storage application.

This work was supported by JSPS KAKENHI Grant Number 15K05964.

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